# Electronics Emulation for Real-Time Fault Location in Power Systems

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To my family.

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*Lausanne, le 29 mai 2017* F. G.

# Abstract

This thesis presents a high-speed hardware platform dedicated to emulate electrical power networks for fault location. The solution implements an algorithm based on the Electromagnetic Time-Reversal (EMTR) principle, which allows locating faults in various types of network and topology. Although the technique is highly robust and accurate, its processing is complex and time consuming if solved with classical digital approaches. Therefore, a dedicated computation platform optimized for processing speed was developed in order to allow its real-time implementation and make it compatible with smart grids.

Two different power network modelling approaches are presented. The first one is based on a finite element representation of the distributed-parameter transmission line. A lossless line, initially characterized by a per-unit length inductance and capacitance, is replaced by a series of identical ladder-connected inductor–capacitor (LC) elements. The second model is based on the general solution of the telegrapher's equations describing the signals propagating along the transmission line. In this method, the travelling waves' propagation taking place in the line is simulated with cascaded discrete-time delay elements.

A possible implementation by means of analog circuits is then presented for each line model. The discretized parameter LC line is simulated by transconductance–capacitor (also called gyrator–C or gm–C) topologies, more suitable for microelectronic implementation. On the other hand, the discrete-time delay element of the second method is implemented by switched-capacitor (SC) circuits. The processing time associated to each method can be scaled down according to the microelectronic parameters of the LC line, or by increasing the sampling frequency of the discrete-time model. Through this time scaling, the hardware emulation allows a fault location within a time of up to a hundred times shorter than with classical digital implementations of similar accuracy. The impact of the non-ideal effects associated to the microelectronic implementation, such as the CMOS active elements finite gain, offset and dynamic range, or the switched-capacitor charge injection, etc., is evaluated for each model. Associated design constraints are then derived in order to ensure a given fault location accuracy that will be similar to that of classical digital methods.

**Abstract**

Since the switched-capacitor model is characterized by higher robustness and accuracy than the LC line, it is therefore preferred for a silicon implementation. The results obtained after a CMOS AMS 0.35 µm process implementation have shown that the discrete-time model allows a fault location within 160 ms, versus a few seconds with a classical digital method, with similar resolution (1%). The speed improvement obtained through the presented method is essential, potentially allowing real-time fault management in power grids. Finally, the impact of the magnitude quantization on the line model, offering perspectives of full digital implementations, is evaluated. A possible extension of the model for the simulation of interconnected or multi-conductor lines is also discussed.

Key words: [**Electronics**] analog CMOS integrated-circuits design, Application Specific Integrated-Circuits (ASIC), continuous-time circuits, discrete-time circuits, transconductor-capacitor circuits (gyrator-C, gm-C), switched-capacitor circuits; [**Power systems**] power network simulation, real-time simulation, analog emulation, smart-grids, power systems protection, fault location, Electromagnetic Time-Reversal (EMTR), electromagnetic transients simulation, transmission line modelling.

# Résumé

Cette recherche présente une plateforme hardware haute vitesse dédiée à l'émulation de réseaux électriques pour la localisation de défauts. La solution implémente un algorithme basé sur le retournement temporel électromagnétique (EMTR). La fiabilité ainsi que la précision de la méthode ont fait leurs preuves, et ce, pour diverses topologies et types de réseaux électriques. Toutefois, la complexité de la méthode, se traduisant par un temps de calcul non négligeable dans le cas d'une résolution numérique traditionnelle, rend son application peu compatible avec les caractéristiques en temps réel des réseaux intelligents. D'où la nécessité de mettre au point une plateforme de calcul dédiée, optimisée sur la vitesse de résolution.

Deux approches distinctes de modélisation de réseaux électriques sont présentées : la première est basée sur une représentation par éléments finis de la ligne de transmission à constantes physiques réparties. La ligne sans pertes, initialement caractérisée par une inductance et capacité par unité de longueur, est substituée par une série d'inductances et de condensateurs (LC) identiques connectés en échelle ; le second modèle se base sur la solution générale des équations du télégraphiste décrivant les signaux propagés dans les lignes de transmission. Dans cette méthode, la propagation des ondes progressive et rétrograde évoluant dans la ligne est simulée par la mise en cascade d'éléments de retard à temps discret.

Une réalisation possible au moyen de circuits analogiques est ensuite proposée pour chaque modèle de ligne. Ainsi, l'élément LC de la ligne à constantes localisées est simulé au moyen d'une topologie à transconducteur-capacité, aussi appelée gm-C. Dans la seconde approche, l'élément de retard à temps discret est implémenté par un circuit à capacités commutées. Le temps de simulation de chaque méthode respective peut être ajusté au moyen des constantes électriques pour la ligne LC, ou au moyen de la fréquence d'échantillonnage dans le cas du modèle à temps discret. Cette compression temporelle permet une résolution du problème dans un temps jusqu'à cent fois inférieur à celui d'une implémentation numérique traditionnelle, pour une précision similaire. L'impact des effets non-idéaux associés à l'implémentation analogique, tels que le gain fini, l'offset et la dynamique des éléments actifs ou l'injection de charge dans les circuits à capacités commutées, etc., est évalué pour chaque modèle. Des contraintes de design correspondantes sont ensuite établies afin d'assurer une résolution finale définie sur la localisation de défauts, similairement aux méthodes numériques traditionnelles.

**Résumé**

Le modèle de ligne à capacités-commutées étant de manière générale plus robuste et plus précis que le modèle LC, il est donc préféré pour une implémentation silicium. Les résultats de son implémentation dans une technologie CMOS AMS 0.35µm ont montré que le modèle en question permet une localisation de défaut en 160ms contre quelques secondes avec une méthode numérique, et ce, pour une résolution similaire (1%). Cette amélioration amenée par l'émulation hardware dédiée est essentielle et permet potentiellement la localisation temps réel de défauts dans les réseaux électriques. Finalement, l'impact de la quantification en amplitude du modèle de ligne, ouvrant la possibilité d'une réalisation purement digitale, ainsi que son extension à l'émulation de lignes interconnectées ou multiconductrices sont aussi abordés.

Mots clefs : [**Electronique**] conception de circuits intégrés analogiques CMOS, circuits intégrés spécifiques à une application (ASIC), circuits à temps continu, circuits à temps discret, circuits à transconducteur-capacité (gyrateur-C, gm-C), circuits à capacités commutées ; [**Réseaux électriques**] simulation de réseaux électriques, simulation temps réel, émulation analogique, réseaux intelligents, protection des réseaux haute tension, localisation de défauts, retournement temporel (RT), simulation de transitoires électromagnétiques, modélisation de lignes de transmission.

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# 1 Introduction

ELECTRICITY has definitely changed the face of our society from the second half of the last century. Omnipresent and almost as essential as access to clean water, it has become a fundamental of our lifestyle and economy nowadays. As the world population is expanding, and through strong economic growth, especially for developing non-OECD nations (Organization for Economic Cooperation and Development), global energy demand is still increasing. Furthermore, the net electricity generation in OECD nations has increased by 42% from 1990 to 10.2 trillion kWh in 2012, and a further increase of 38% is estimated by 2040 [1]. This energy supply is only possible with a reliable energy network that links the power generation units to the consumer.

Mainly built after the Second World War, the European power system has evolved from small, non-competitive, isolated networks to interconnected national and even international grids. This transition, induced by the rapid growth of the demand for electricity, still presents huge challenges in term of the reliability and security of the energy supply. For this purpose, the smart grid concept, involving modern functionalities and a control that takes into account the information exchanged between the utility company and its customers, has been introduced.

The reliability of the power network is a great challenge, which involves real-time control and maintenance procedures to avoid outages and the resulting excessive costs, which can sometimes have catastrophic consequences. For instance, the US–Canadian blackout in 2003 affected fifty million people, for four days, with an estimated cost of ten billion USD, for the US alone [2]. Power interruptions can be caused by network transient instabilities or by fault occurrences on a power line. These faults can be induced by conductor swing, mechanical failure of insulators, or natural incidents such as lightning, falling trees, ice, etc. When a fault occurs, it has to be located as soon as possible by a fault location device in order to disconnect the faulted line and adequately reconfigure the power network to restore power delivery, or, if this is not possible, to minimize the non-supplied zones ([3],[4]). Furthermore, accurate fault location is necessary to avoid long and costly searches for the fault by the maintenance team for its repair.

Through the massive integration of new power sources in the network (renewable energy, e.g., wind farms, hydroelectric and solar stations), new topologies are required, and thus, more flexible fault location methods. Fast and accurate fault location in power networks has been studied for several years and many different approaches have been presented. Among them, three categories can be distinguished: techniques that compare the pre- and post-fault voltage and current phasors, (phasor-based techniques or impedance measurement techniques); methods that measure the electromagnetic transient travelling waves that have originated at the fault (travelling-wave based methods); and techniques based on Artificial Neural Networks (ANN). The phasor-based method is limited by several assumptions and simplifications that impact the accuracy of the fault location [4]. Furthermore, its applicability to certain grid topologies, as in the case of active networks, with many generation units, can provide non-negligible inaccuracies in the fault location. On the other hand, travelling-wave based methods are considered as more accurate and can be applied to complex network topologies ([11],[12]). However, these methods require high bandwidth measurement points on the line and are characterized by complex signal processing. Artificial Neural Network techniques are often characterized by long and complex learning processes that require a great deal of computational power, and their applicability to real systems is limited by their extensive training ([15],[16]). Taking into account the research done on the topic of fault location, and the rapid and complex evolution of today's power systems, there is a need for a faster and more accurate fault location method compatible with different network types and topologies.

## 1.1 Thesis Contribution

A high-speed dedicated hardware platform aimed at the implementation of a highly accurate and robust travelling-wave based fault location method has been developed. The combination of a very demanding algorithm in terms of computational resources and a high-speed hardware emulator allows a precise fault location in complex network topologies, within a very competitive time-scale. With similar accuracy, the developed power network emulator allows locating the fault within a time frame up to a hundred times shorter than classical digital solutions, making real-time applications realistic. With its association of real-time capability, accuracy, flexibility and robustness, the presented fault location hardware solution seems to be the response to the needs of today's power systems.

The implemented fault location algorithm is based on the Electromagnetic Time-Reversal (EMTR) principle ([25],[26],[27],[28],[29]). This novel method exploits the reversibility in time of the telegrapher's equations, which describe signals propagated along a transmission line, to retrace the electromagnetic transients that originated at the fault back to their source. This iterative processing consists in a kind of cross-correlation computation of the fault-originated transients (the response of the faulty network) with the response of a network replica, which allows successively moving an estimated fault along it. Finally, the fault is located through the cross-correlation maximum, which occurs when the fault coordinate

coincides with the *guessed fault* location of the emulated network. Despite its high robustness and accuracy, proven for different network topologies, the method is limited by a long and complex processing. This bottleneck, essentially due to the emulation of the power network, requires the development of an alternative simulation platform optimized for processing speed, in order to meet the smart-grid expectations of a real-time capability.

This research introduces different hardware transmission line modelling approaches aimed at the high-speed emulation of a power network within the framework of the presented fault location method. The first model is based on a finite-element representation of a distributed parameter lossless transmission line. In this approach, the line is mapped to a ladder consisting of $N$ identical inductor–capacitor (LC) elements, each modelling a finite length increment of the line. The accuracy of the mapping is determined by the number of elements composing the line, which thus sets the resolution of the fault location. On the other hand, the processing speed is set by the line propagation time, which can be scaled by means of the LC parameters. A possible implementation by means of transconductor–capacitor circuits, also called gyrator–C or gm–C circuits, is presented. The associated design constraints are derived and the non-ideal effects usually plaguing CMOS analog circuits are evaluated. It is shown that this straightforward approach can be applied for a high-speed location of the fault, for a given accuracy set by the line discretization and corresponding implementation constraints. A time calibration is however required to minimize the impact of the random variations of the equivalent LC elements on the accuracy of the model.

A second approach to modelling the transmission line, based on discrete-time circuits, is presented. According to the general solution of the telegrapher's equations, this method simulates the propagation of the travelling waves along the line through many cascaded sampled-data delay elements. This second approach discretizes the line model in space and in time, and thus is intrinsically insensitive to any variations in the delay elements associated to the non-ideal effects of the implementation, such as mismatches between the components. The processing speed of the discrete-time solution is determined by the sampling frequency, and as with the LC model, its accuracy is determined by the discretization of the line. However, the data sampling inherent in a discrete-time method can add a distortion, and consequently generate inaccuracies, in particular for the interpolation of faults situated between consecutive line taps. First, an implementation of the discrete-time model by means of switched-capacitor (SC) topologies is presented. the Associated non-ideal effects and their impact, for instance, on the processing speed, are evaluated within the framework of the fault location, and the corresponding design constraints are derived.

Finally, an alternative to the presented discrete-time modelling approach, involving magnitude quantization, is introduced. Although the signal quantization impacts the method's accuracy, it allows fully digital realizations, avoiding many of the non-ideal effects associated to analog circuits. Consequently, an implementation by means of simple shift registers and logic arithmetic circuits is presented. Additional extensions of the simple lossless transmission line model to multidimensional propagation medium emulation are evaluated. In this context,

the emulation of complex network topologies with interconnected or multi-conductor lines is studied.

## 1.2 Outline of the Thesis

After this introduction, eight other chapters follow:

**Chapter 2** presents the state of the art of the location of faults in power networks, and compares the different methods in term of their accuracy, complexity, and robustness, in terms of contemporary requirements for power systems. A novel fault location method applying the Electromagnetic Time-Reversal (EMTR) principle is introduced. The EMTR method and its ability to focus a field on a target in multidimensional propagation media is first demonstrated. Then, its applicability to fault location in unidimensional media (power lines) is presented in two phases: the measurement of the electromagnetic transient originating from the fault; its time inversion and iterative *back-propagation* in the network model and focussing on the fault location. The fault location process is evaluated analytically, considering the power network model as an ideal lossless transmission line.

**Chapter 3** presents the two different transmission line modelling approaches applied to power network emulation: a finite element LC model based on the discretization of the distributed parameter line; and a discrete-time model based on the general solution of the telegrapher's equations. The parameters determining the processing speed and accuracy are determined for each approach, and the impact of the spacial and temporal discretization of the models is evaluated in terms of the fault location accuracy. The factors that limit the accuracy, such as lumped elements mismatch in the LC model, or the finite sampling frequency in the discrete-time model, are also discussed.

The implementation of the lumped inductor–capacitor line model is presented in **chapter 4**. In this approach, the discrete line element is simulated by means of a gyrator–capacitor circuit, also called a transconductor–capacitor (gm–C) circuit, more suitable for microelectronic integration. The impact of the non-ideal effects inherent to CMOS implementations is evaluated in terms of the propagation speed error, equivalent line losses, and associated fault location inaccuracies. The corresponding design constraints are derived depending on the specified processing speed and desired accuracy, determined by the line model discretization. In view of a silicon integration, practical design aspects, such as the circuit sizing, global power consumption, and chip area, are also considered.

**Chapter 5** presents the implementation of the second emulation approach, based on discrete-time circuits. In this model, the elementary delay constituting the line is realized with switched-capacitor (SC) topologies. Similarly to the implementation of the lumped parameter model, the parasitics associated to the CMOS switched-capacitor circuits are evaluated in terms of processing speed limitations, equivalent model losses, which translate to inaccuracies in the fault location. The associated design constraints are derived according to the expected

processing speed and accuracy, and the related integrated-circuit power consumption and silicon area are estimated.

According to the design constraints defined in the previous chapter, **chapter 6** presents the transistor-level implementation of the switched-capacitor line model. The architecture of the elementary switched-capacitor delay cell and corresponding circuitry is detailed, and related simulation results are presented. A circuit for the evaluation of the propagated signal energy, required for the fault location, is also presented. The transistor biasing, current consumption, silicon area, and some layout aspects are also discussed in this chapter.

**Chapter 7** presents the measurement results and validations of the SC line integrated-circuit implementation presented in Chapter 6. The properties of the implemented discrete-time model are first evaluated in terms of the equivalent line losses and speed characteristics, and optimized using the tunable parameters. Then, the implemented circuit is evaluated within the frameword of fault location and its associated accuracy, speed, and current consumption are measured and discussed in the same context.

After the full validation of the SC realization of the discrete-time model, **chapter 8** presents an alternative implementation with a magnitude quantification. The impact of the amplitude discretization on the model's accuracy and its consequences for the fault location are discussed. A fully digital realization based on shift registers and arithmetic logic circuits is presented. The corresponding implementation constraints, in terms of circuit area and maximum speed, are evaluated according to the required quantification. Afterwards, the possible extension of the single line models developed in this research to complex network topologies, such as interconnected or multi-conductor lines, is discussed. Similarly to the discrete-time model, the line interconnection is analysed according to the travelling waves approach and a multi-phase line is simulated with a modal transformation, which allows considering coupled lines as independent conductors.

**Chapter 9** summarizes the different steps that have organized this research and highlights its main results. The general approach and reflections that have motivated the adopted choices are recalled. Finally, it compares qualitatively the results and contributions of the power network hardware emulation to classical digital solutions and discusses the possible extensions of the method and related challenges according to the requirements of power systems.

# 2 Fault Location in Power Networks

This chapter presents the state of the art of power network fault location and outlines its challenges and limitations according to the method, the power grid parameters, and the topologies. Then, a novel fault location technique based on the Electromagnetic Time-Reversal (EMTR) principle is introduced. The EMTR principle is first presented within its context, then, its applicability to the location of a fault in a transmission line network is demonstrated. It is shown that this novel technique provides high accuracy and robustness according to the network parameters, which satisfies today's needs.

## 2.1 State of the Art

Power network fault location has been a topic of interest since the second part of the twentieth century. Mainly involving power transmission networks, characterized by high voltage lines transporting power across long distances (a few hundreds of kilometers), research has also been largely about power distribution networks, with lower voltage lines at local scales (a few tens of kilometers). Present fault location techniques can be classified into three different categories:

- The pre- and post-fault voltage and current phasors analysis (impedance-based method) deduces the fault location according to the measured line impedance ([3],[4],[5],[6]). Although this approach is the most straightforward, its accuracy depends on many parameters, such as the network characteristics, the fault impedance (which can be only roughly estimated), the system loading, etc. The accuracy is also affected by the assumptions made about the power system, such as the linearity of the fault loop impedance, the assumption of a fully passive network, which omits the presence of active sources, or by ignoring the possible transformer current saturation when a fault occurs. However, the precision of the impedance measurement method can be improved if additional observation points are placed on the line, with the so called multi-end or multi-terminal techniques ([7],[8],[9],[10]), as distinct from the single-end technique. Nevertheless, the operation relies on the communication between observation points and adds a lot of complexity to the fault location process. Furthermore, the phasors technique cannot be applied to high-voltage DC networks (HVDC), which is an important concern in modern power systems.

- Travelling waves or wavelet-based methods deduce the fault location according to measured electromagnetic transients that travel along the line after a fault occurrence ([3],[4],[11],[12],[13],[14]). This technique is highly accurate and is independent of the fault impedance. Moreover, it offers a good flexibility regarding the network topology, can be applied to active networks (with many generation units), and is compatible with HVDC networks. On the other hand, this technique requires large bandwidth acquisition equipment to measure the high frequency transients and a detailed network model and line properties. Moreover, the present algorithms are often characterized by a complex signal processing. Similarly to the phasors-based method, additional observation points (multi-end) can be added on the line to increase the process accuracy. However, the fault location precision strongly depends on the quality of the communication between the terminals, on the GPS signal, and needs a common and accurate time basis.

- Methods based on Artificial Neural Networks (ANN) have been widely studied in the literature ([15],[16],[17],[18]). These methods rely on pattern recognition algorithms based on the transient waveform originating from the fault, or on the network status (unsupplied zones, state of the relays, etc.). These heuristic techniques are often characterized by long learning processes that require complex computations, and their

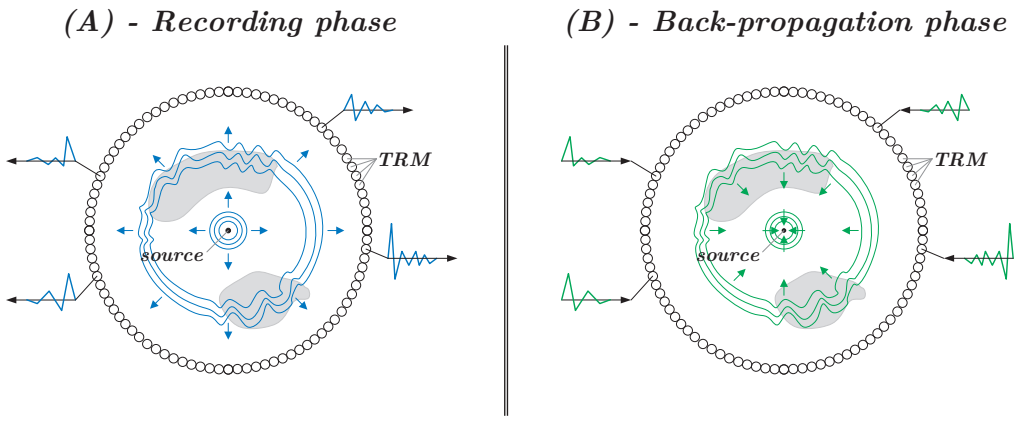


Figure 2.1: The time-reversal process (adapted from [32]) illustrated through the *recording phase* (A) and the *back-propagation phase* (B).

applicability to real systems is limited by this extensive training.

## 2.2 Electromagnetic Time Reversal

Time Reversal (TR) is a physical principle to focus a field in time and space in inhomogeneous and non-dissipative media. Based on the time-reversal invariance of a wave equation, the time-reversal technique allows a wave propagation backward to its source. This method has been applied for biomedical purposes, for imaging or for lithotripsy with ultrasonic waves ([32],[33],[34],[35]), and is also used as a signal processing algorithm for communications (e.g., cancellation of reverberation issues), for submarines with acoustic waves ([42],[44]) and with electromagnetic waves (EM) in telecommunications ([36]-[37]-[38]-[39]-[41]).

### 2.2.1 Basic Principles

Considering a non-dissipative and inhomogeneous medium, the field radiated by an acoustic or electromagnetic source is recorded by a surrounding array of transducers, also called *Time-Reversal Mirrors* (TRM, [35],[39]), as shown in the *recording phase*, (A) in Fig. 2.1. Based on the principle of reciprocity, the *time-reversal cavity*, formed by the TRMs, retransmits the recorded signals inverted in time, so that the resulting wave travels back and converges at the initial source position, as illustrated by the *back-* or *reverse-propagation* phase, (B) in Fig. 2.1.

#### Practical Implementation

A time-reversal cavity, formed by an infinite number of TRMs, cannot be practically realized. Only a finite number of transducers can be implemented, which translates into losses of information in term of regeneration of the original signal and focusing quality. This conse-

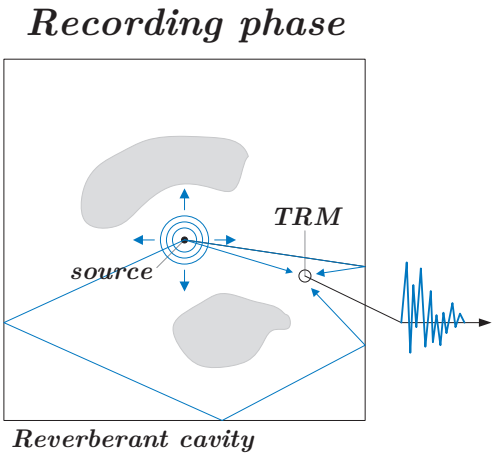


Figure 2.2: Single TRM probe time-reversal principle (adapted from [43]).

quence can be minimized if the source is situated in a reverberant cavity ([44],[45],[46]). The additional signal information contained in the measured echoes implies that it suffices to consider only a single TRM probe, as illustrated in the recoding phase in Fig. 2.2.

### 2.2.2 Electromagnetic Time-Reversal Principle Applied to Transmission Lines

Before applying the electromagnetic time-reversal method to power networks, the time-reversal invariance of the telegrapher's equations (2.1),[47], characterizing the signals propagated along transmission lines, should be first verified.

$$\frac{\partial^2}{\partial x^2}V(x,t)-L'C'\frac{\partial^2}{\partial t^2}V(x,t)=0 \tag{2.1a}$$

$$\frac{\partial^2}{\partial x^2}I(x,t)-L'C'\frac{\partial^2}{\partial t^2}I(x,t)=0 \tag{2.1b}$$

$V(x,t)$ and $I(x,t)$ are the line voltage and current, respectively, at an instant $t$ and line position $x$, and $L'$ and $C'$, the distributed per unit length inductance, respectively, the capacitance. By applying the *time-reversal operator* $t \rightarrow -t$ [25], so that a given function becomes

$$f(x,t) \quad \rightarrow \quad f(x,-t), \tag{2.2}$$

it is seen that both $V(x,t)$ and $V(x,-t)$, respectively $I(x,t)$ and $I(x,-t)$, are solutions of

the equation (2.1a), respectively (2.1b), satisfying thus the EMTR application criteria. This condition is fulfilled since the time derivatives of the functions are of even order, which is the case for the lossless transmission line equation. In a lossy line, the telegrapher's equations [47] become

$$\frac{\partial^2}{\partial x^2}V(x,t) - L'C'\frac{\partial^2}{\partial t^2}V(x,t) - (R'C' + G'L')\frac{\partial}{\partial t}V(x,t) - G'R'V(x,t) = 0 \tag{2.3a}$$

$$\frac{\partial^2}{\partial x^2}I(x,t) - L'C'\frac{\partial^2}{\partial t^2}I(x,t) - (R'C' + G'L')\frac{\partial}{\partial t}I(x,t) - G'R'I(x,t) = 0 \tag{2.3b}$$

where $R'$ and $G'$ are the distributed per unit length resistance, and conductance respectively. Since the functions contain a time derivative of odd order, $V(x,-t)$ and $I(x,-t)$ are not a solution of equations (2.3), and thus, are not time-reversal invariant. This result shows that the time-reversal principle cannot be applied to dissipative media, or to lossy lines, in the present case.

## 2.3 Fault Location in a Power Network Using the EMTR Principle

Previous research ([25],[26],[27],[28],[29]) has led to a fault location technique based on the electromagnetic time-reversal principle aimed at power transmission networks. Power transmission lines are characterized by low losses and can be considered as lossless in the first approximation, making thus the time-reversal principle applicable. In this fault location technique, the presented EMTR method is applied to a unidimensional propagation medium that is the power network. When a fault occurs, consequent transients take place in the network, similarly to a source that transmits a signal in a propagation medium. These fault originated transients, called *fault signatures*, are then measured at a single or multiple observation points (TRMs) placed along the network. The fault signatures are then time-reversed and back-propagated in a replica of the power network. From the time-reversal principle, it is known that the back-propagated signals will converge at the fault coordinate, generating an energy maximum at this location. Consequently, the fault coordinate is sought by iteration, repeating the back-propagation phase while moving a *guessed fault* along the network replica and measuring the corresponding signal energy. Finally, the guessed fault location that yields the highest energy level can be considered as the closest to the real fault coordinate.

The power network fault location process using the EMTR principle is detailed in the following paragraphs according to two phases: the propagation and measurement of the fault-originated transients (fault signatures) in a simple power network described by its electrical schematic; and the iterative back-propagation of the time-reversed fault signatures in a network model and measurement of the signal energy at corresponding guessed faults in order to locate the

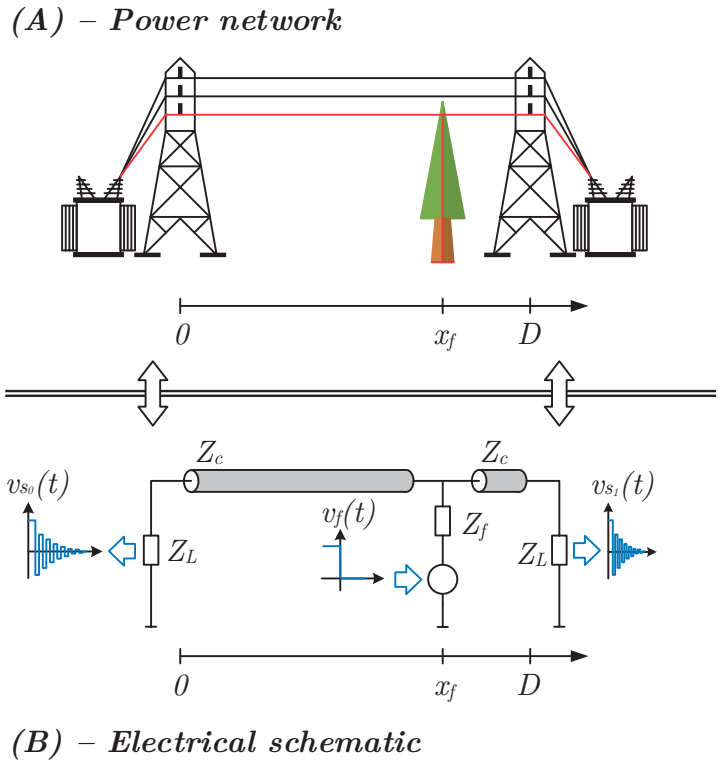


Figure 2.3: Fault on a power transmission line of length $D$ and equivalent electrical schematic.

energy convergence point, and hence the coordinate of the fault.

### 2.3.1 Propagation and Measurement of Fault-Originated Transients

The transient phenomena that take place after a fault can be explained by analyzing the equivalent electrical schematic of the faulted power network. Fig. 2.3-(A) illustrates the simplest case of a fault, where a single phase line of length $D$ bounded by two transformers is shorted to ground (e.g., by a tree) at an unknown coordinate $x_f$. Fig. 2.3-(B) illustrates the equivalent electrical schematic of the situation, where the power line is represented by a lossless transmission line of surge impedance $Z_c$ separated into two pieces by the fault location $x_f$. The power transformers at the line ends are symbolized by equal load impedances $Z_L$ and the fault at $x_f$ by a fault impedance $Z_f$ and a series fault voltage source $v_f(t)$.

The fault occurrence is emulated by a negative voltage step, down to zero, on the fault voltage source that symbolizes the voltage drop on the power line due to a short to the ground. According to the theory of transmission lines [48], the consequent incident and reflected waves ($V_x^+$ and $V_x^-$ respectively, where $x$ is the position) propagate from the fault along both

line sections. When a wave reaches the $k^{th}$ line boundary (load or fault location), it is reflected in the opposite direction according to the corresponding reflection coefficient $\rho_k \in [-1;1]$, so that

$$\rho_k = \frac{V_k^-}{V_k^+}. \tag{2.4}$$

The incident and reflected waves propagate and reflect along the line until they are totally attenuated. Finally, the fault signatures $v_{s_0}(t)$ and $v_{s_1}(t)$ measured at the line boundaries $k = \{0;1\}$, such as any voltage $V_x$ and current $I_x$ at an $x$ coordinate of the line, are obtained as functions of the incident and reflected waves as

$$\begin{cases} V_x = V_x^+ + V_x^- \\ Z_c I_x = V_x^+ - V_x^-. \end{cases} \tag{2.5}$$

The reflection coefficient defined in (2.4) is a parameter that depends on the line surge and corresponding termination impedance $Z_k$, as shown by

$$\rho_k = \frac{Z_k - Z_c}{Z_k + Z_c}. \tag{2.6}$$

Typically, a line terminated by a transformer is seen as an open-circuit for the travelling waves originating from the fault, which is constituted by high-frequency components [30]. Consequently, the corresponding load reflection coefficient stated in Fig. 2.3-(B) is close to $\rho_L \simeq 1$. The fault impedance can be assumed of much lower value than the line surge impedance, translating thus to a fault reflection coefficient close to $\rho_f \simeq -1$ [25]. Finally, any line interconnection would be characterized by a negative reflection coefficient.

**Fault Signature**

The electromagnetic transient originating from the fault, the so called fault signature, can be considered as a footprint of the faulted network. This transient response directly depends on the network topology, parameters, fault location and is of prime importance in the presented fault location technique. The following paragraphs analyze the shape of the fault signature occurring in the faulted line illustrated by Fig. 2.3. The corresponding fault signatures $v_{s_0}(t)$ and $v_{s_1}(t)$, measured at the line boundaries $k = 0$ and $k = 1$ respectively, for a fault occurring at coordinate $x_f = 70\%D$ are illustrated in the transient simulation results in Fig. 2.4.

Both signatures are characterized by an exponential attenuation and have a duration $T_{s_k}$ proportional to the propagation time $T_{p_k}$ of line sections delimited by the corresponding

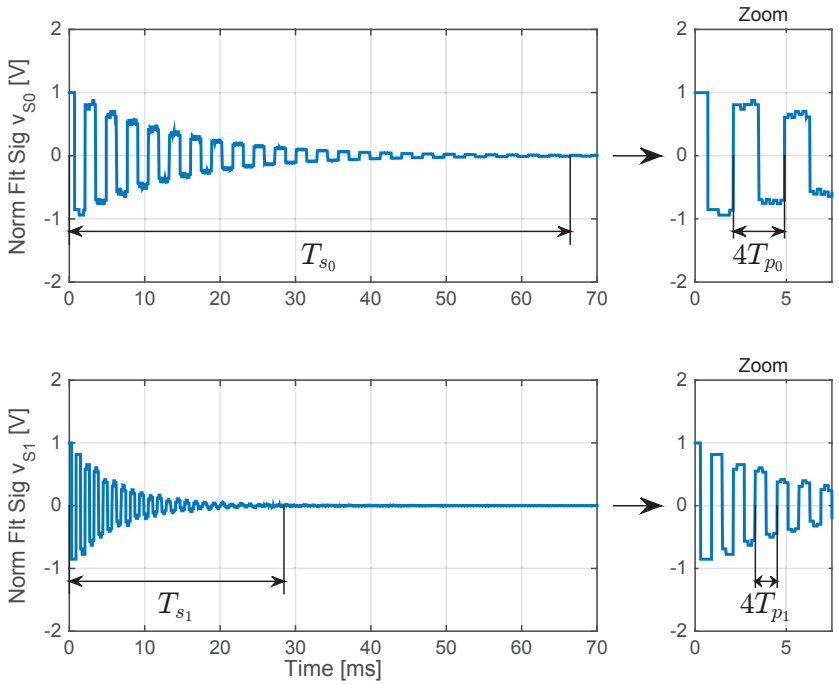


Figure 2.4: Transient simulation of the normalized fault signatures $v_{s_0}(t)$ and $v_{s_1}(t)$ at corresponding line terminations $k = \{0;1\}$.

boundary and the fault, at $x_f$. The oscillating character of the signatures is due to the negative reflection coefficient of the fault $\rho_f \simeq -1$, which inverts the phase of each reflected wave. The oscillation period is given by $4T_{p_k}$. The $k^{th}$ termination fault signature duration $T_{s_k}$ is calculated in the appendix A.1 and is defined for $\rho_f \simeq -1$ as

$$T_{s_k} = -10\frac{T_{p_k}}{ln|\rho_L \rho_f|}. \tag{2.7}$$

With typical line parameters, the fault signature duration reaches the order of magnitude of

$$T_{s_k} \simeq 200 T_{p_k}. \tag{2.8}$$

It is worth noting that the complexity of the signatures increases with the network topology and that they conserve this simple nature in the case of a single faulted line only.

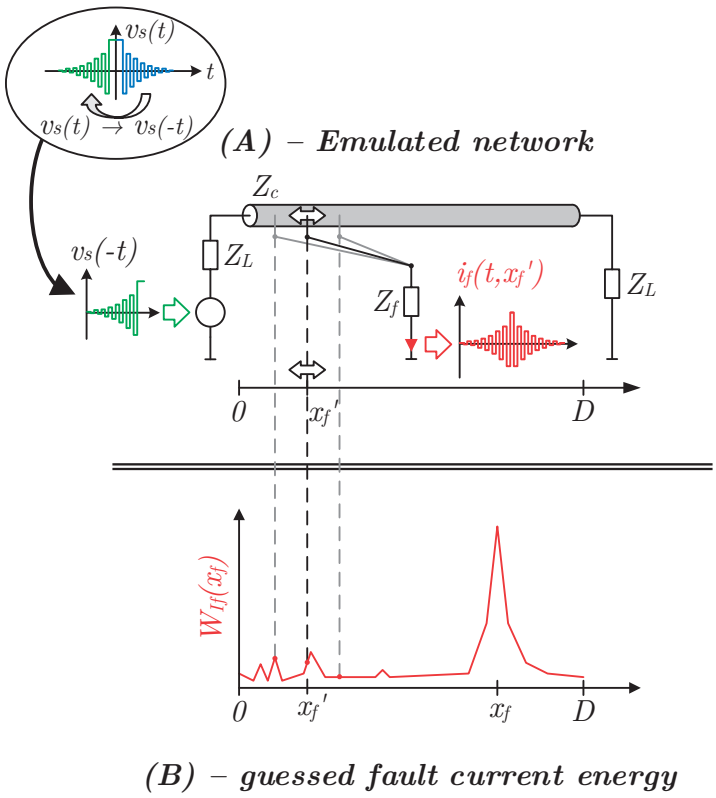


Figure 2.5: Back-propagation phase of the time-reversed fault signature (A) and corresponding guessed fault current energy plot (B).

### 2.3.2 Back-Propagation of the Time-Reversed Fault Signature

The second phase of the fault location method is the back-propagation of the time-reversed fault signatures in a replica of the faulted power network and the localization of the signal energy convergence point, and hence the corresponding coordinate of the fault. As illustrated in Fig. 2.5, this procedure takes place in a network model realized according to the real network topology and line parameters, which are assumed to be known. Similarly to the faulted network illustrated in Fig. 2.3, this line, of the same length $D$, is bounded by two high impedance loads $Z_L$ and allows simulating guessed faults at different locations along it. The guessed fault is represented by a low value of fault impedance $Z_f$ at a coordinate $x'_f$. In the presented situation, only a single fault signature $v_s(t)$ is time reversed and back-propagated from the network model input, at $x = 0$. Indeed, as stated in subsection 2.2.1, the reverberant nature of the propagation medium produced by the boundary reflection coefficients allows considering only a single observation point (TRM) without losing any focusing information. This simplification is a great advantage of the presented method, which allows accurately locating the fault with a single observation point only, avoiding thus any synchronization or

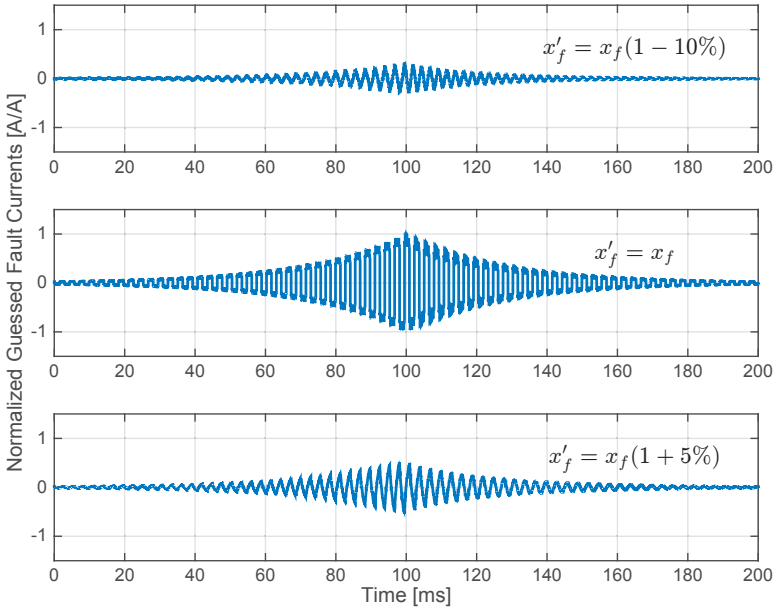


Figure 2.6: Simulated EMTR fault currents for different guessed faults $x'_f$.

communication constraints present in multi-terminal fault location techniques. Consequently, only the fault signature $v_{s_0}(t)$ is considered, and renamed as $v_s(t)$ for future analysis.

As illustrated in Fig. 2.5-(A), the fault signature is time reversed, so that $v_s(t) \rightarrow v_s(-t)$, and iteratively back-propagated, while the guessed fault is moved along the line model. At each back-propagation, a corresponding fault current $i_f(t, x'_f)$ is measured, as shown by the transient simulations for different guessed fault locations $x'_f$ in Fig. 2.6. As confirmed by the time-reversal theory, the current energy is the highest when the guessed fault and the real fault coordinates coincide, so that $x'_f = x_f$. This energy maximum, illustrated in the current energy plot as a function of the guessed fault in Fig. 2.5-(B), allows locating the fault.

### Fault Location Duration

The duration of the process depends on the number of back-propagation iterations, and hence, on the number of guessed faults simulated along the line. This value is directly related to the process resolution, which limits the accuracy of the fault location. According to the simulation results in Fig. 2.6, a single back-propagation iteration lasts at most twice the fault signature time $T_s$, since the same duration is needed for the signal propagation as for its reflection in the line model. Consequently, the duration of the fault location process, as a function of the resolution $r$, can be defined as

$$T_{EMTR} = \frac{2 \cdot T_s}{r}. \tag{2.9}$$

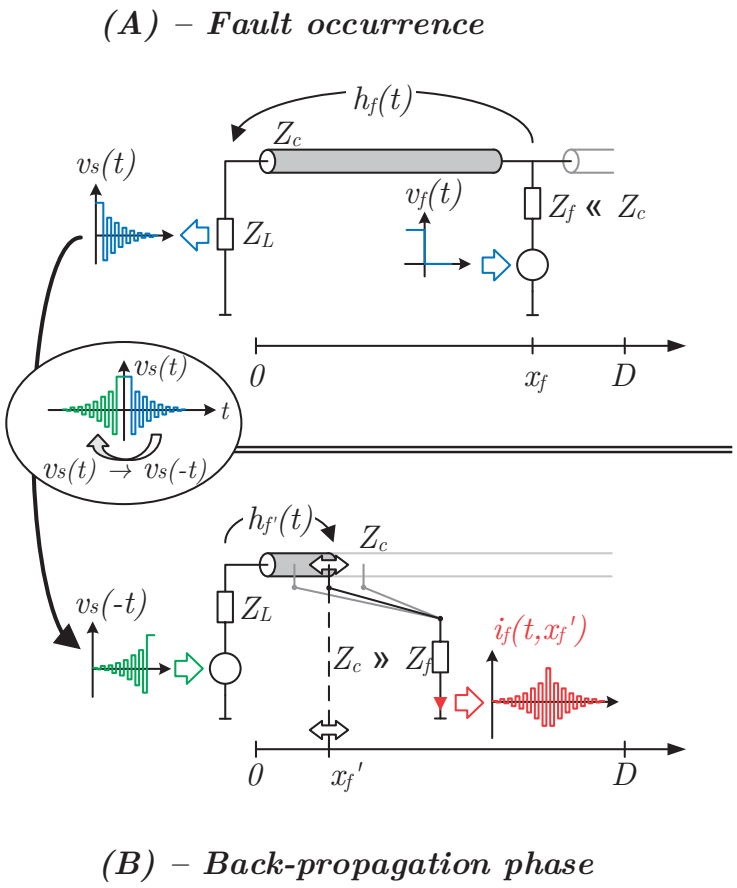


Figure 2.7: EMTR fault location process in a power transmission line. The fault occurrence (A) is followed by the back propagation phase (B).

According to the fault signature time estimated in (2.7), a typical power transmission line of length 100 km would provide a fault signature of $T_s \simeq 80$ ms, so that a fault could be located within approximately $T_{EMTR} \simeq 16$ s, with one percent resolution. This duration is not compliant with the power network real-time requirements, since it expects a fault location within the same order of magnitude as the opening time of a power switch, a few hundred milliseconds. This weak point can be circumvented by scaling in time the network model and the back-propagated fault signature, and hence the simulation time as well. This down-scaling is realized through the hardware network model presented in the following chapter.

### 2.3.3 Fault Location Process Analytical Demonstration and Interpretation

In order to validate the fault location method using the EMTR principle, the process, illustrated in Fig. 2.7, is analyzed mathematically in the following paragraphs. For this purpose, some

assumptions on the real and the emulated lines, displayed in (A) and (B) respectively, have been made: the fault impedance $Z_f$ is taken to be of much lower value than the line surge impedance, so that the line section above the fault is shorted, and thus, neglected; the line surge, loads and fault impedances for the real and emulated networks are taken to be equal, so that the equivalent loads and fault reflection coefficients $\rho_L$ and $\rho_f$ refer to both the real and emulated lines.

### Time Domain Analysis

Referring to Fig. 2.7-(A), the fault signature $v_s(t)$ measured at the line input can be expressed as the time domain convolution [77] between the fault voltage $v_f(t)$ and the system impulse response $h_f(t)$:

$$v_s(t) \quad = \quad v_f(t) * h_f(t). \tag{2.10}$$

Through Fig. 2.7-(B), it can be similarly shown that the resulting guessed fault current $i_f(t, x'_f)$ is proportional to the time-reversed fault signature $v_s(-t)$ convolved with the emulated line input-to-guessed-fault path response $h'_f(t)$ so that

$$i_f(t, x'_f) \quad \propto \quad v_s(-t) * h'_f(t). \tag{2.11}$$

Combining (2.10) with (2.11) yields

$$i_f(t, x'_f) \quad \propto \quad v_f(-t) * \underbrace{h_f(-t) * h'_f(t)}_{\phi_{f'f}(t)}, \tag{2.12}$$

which shows that the EMTR guessed fault current is simply proportional to the cross-correlation function $\phi_{f'f}(t)$ between the real and emulated faulted lines $h'_f(t)$ and $h_f(t)$ respectively [77]. Equation (2.12) confirms then that the fault current, and hence its energy, is maximized when both channels are identical, thus, when the real and the guessed faults coincide, as stated by the time-reversal method.

**Frequency Domain Analysis**

From the analytical solution of the guessed fault current stated in (2.12), the allure of the EMTR process result can be obtained through the frequency responses of the real and emulated lines, respectively, given by

$$H_f\left(j\omega, x_f\right) = \frac{(1-\rho_f)(1+\rho_L)}{2}\frac{e^{-j\beta x_f}}{1-\rho_f\rho_L e^{-2j\beta x_f}} \tag{2.13a}$$

$$H'_f\left(j\omega, x'_f\right) = \frac{(1-\rho_L)(1+\rho_f)}{2}\frac{e^{-j\beta x'_f}}{1-\rho_L\rho_f e^{-2j\beta x'_f}}, \tag{2.13b}$$

where $\beta$ is the phase constant, a function of the pulsation $\omega$ and the per unit length line inductance $L'$ and capacitance $C'$, so that

$$\beta \quad = \quad \omega\sqrt{L'C'}. \tag{2.14}$$

Knowing that the time-reversal operator translates from the time domain to the frequency domain,

$$f(-t) \quad \overset{\mathscr{F}}{\longleftrightarrow} \quad F^*(j\omega), \tag{2.15}$$

where $\mathscr{F}$ denotes the Fourier transform and $^*$ the complex conjugate, the cross-correlation of the real and emulated lines stated in (2.12) translates into the frequency domain as

$$\Phi\left(j\omega\right) \quad = \quad H_f^*\left(j\omega, x_f\right) H'_f\left(j\omega, x'_f\right). \tag{2.16}$$

Consequently, by combining (2.12), (2.13) and (2.16), and, as a simplification, considering the loads as open circuits and the faults as shorts, so that $\rho_L \to 1$ and $\rho_f \to -1$, the magnitude of the frequency domain guessed fault current becomes

$$\left|I_f\left(j\omega, x'_f\right)\right| \quad \propto \quad \left|\Phi\left(j\omega\right)\right| \propto \left|\frac{1}{cos\left(\beta x_f\right) cos\left(\beta x'_f\right)}\right|. \tag{2.17}$$

Finally, the fault can be located through the evaluation and location of the maximum of the

guessed fault current energy [77] as a function of $x'_f$, defined as

$$W_{I_f}(x'_f) = \int_{-\infty}^{+\infty} \left| I_f(j\omega, x'_f) \right|^2 d\omega. \tag{2.18}$$

This energy is a maximum when the cross-correlation function in (2.17) is a maximum, and this occurs when $x'_f = x_f$. From the cross-correlation function it can also be seen that other local maxima occur at each odd multiple or divisor of the fault location, so that

$$x'_{f_{max}} = \begin{cases} (1+2m)x_f \\ \\ \frac{x_f}{1+2m}, \end{cases} \tag{2.19}$$

and local minima occur at each even multiple or divisor:

$$x'_{f_{min}} = \begin{cases} 2mx_f \\ \\ \frac{x_f}{2m}, \end{cases} \tag{2.20}$$

where $m$ is a positive integer. These assumptions are confirmed by the EMTR fault location simulations realized with faults situated at 10% and 90% of the line length $D$, as illustrated in the upper, respectively, lower plot in Fig. 2.8. The graphic compares the guessed fault current energies $W_{I_f}$ simulated with two different sets of reflection coefficients $|\rho_L \rho_f| = \{0.8; 0.95\}$, without any of the formerly mentioned simplifying assumptions. Each simulation result confirms the presence of a global maximum at $x'_f = x_f$, which allows locating the fault. This maximum is followed by local maxima, called echoes, and minima, as predicted by (2.19) and (2.20). As shown in the upper graph, an attenuation of the expected echoes situated at $5x_f$, $7x_f$ and $9x_f$ can be noticed. This attenuation is caused by the reflections that occur in the line section beyond the fault location, which has been neglected in the theoretical calculations. Due to its minor impact, this phenomenon won't be considered. Both graphs in Fig. 2.8 show that the sharpness of the curve depends on the magnitude $|\rho_L \rho_f|$ of the reflection coefficients. The widths of the maxima increase proportionally to $x_f$, while the sharpness varies with the reflection coefficients, which act similarly to a quality factor. However, the reflection coefficient doesn't impact the maxima location, which makes the accuracy of the method independent of the value of the impedance, and thus very robust [25].

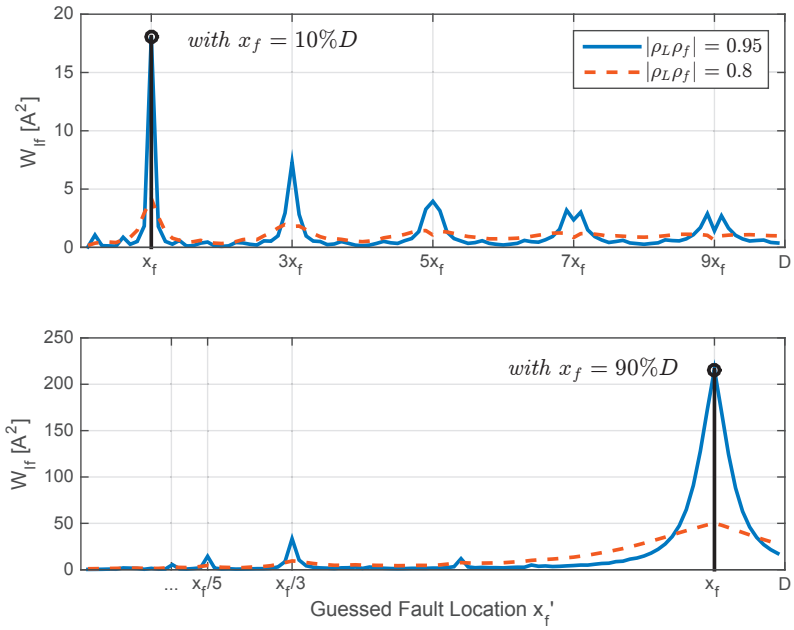


Figure 2.8: Fault current energy $W_{I_f}$ as a function of the guessed fault location $x'_f$, with reflection coefficients set to $|\rho_L\rho_f| = \{0.95, 0.8\}$ and faults situated at $x_f = \{10\%D, 90\%D\}$ for the upper and lower graph respectively.

## 2.4 Conclusion

This chapter has presented the state of the art of the existing fault location techniques aimed at power networks. The three principal categories, that is, the methods base on phasors, on travelling waves, and on an artificial neural network, were discussed in terms of their advantages, drawbacks, and applicability regarding the needs of power networks nowadays. A novel travelling-wave based fault location method that applies the principle of electromagnetic time reversal (EMTR) was also presented. This novel method is based on the time-reversal invariance of the telegrapher's equation that describes any signal wave along the network transmission lines. It provides high accuracy, despite the complexity of the network or the presence of additional generation units in the grid, which satisfies the needs of the power systems of today. Moreover, this method works accurately with a single observation point and thus avoids the synchronization constraints present in multi-terminal methods. However, as with many travelling-wave based methods, the EMTR-based technique is characterized by a complex signal processing that translates into a long simulation time, not compliant with the real-time requirements of power networks. For this reason, the next chapter explores a possible hardware implementation of the method for a faster simulation that would meet the expectations.

# 3 Power Network Emulation

This chapter discusses the possible implementation of a power network analog emulator to execute the back-propagation phase (Section 2.3.2) of the fault location method using the electromagnetic time-reversal (EMTR) principle. Nowadays, this step is executed within a digital FPGA-based emulator that provides convincing results in terms of accuracy, but is still limited by its long processing duration, which makes real-time implementations difficult. For this reason, a dedicated hardware model providing shorter simulation durations is explored. Despite its dependency on electrical parameters and a restrained programmability, the proposed analog alternative provides a real improvement in terms of processing speed, making thus real-time implementation possible. This chapter presents two different analog line models: the first is based on the infinitesimal transmission line model discretization by means of series interconnected inductors-capacitors (LC) elementary cells; and the second is based on a discrete-time approach, where the line is represented by a series of elementary delays, implementable by switched-capacitor (SC) circuits. Both approaches are evaluated in terms of processing time, fault location accuracy, and their limitations caused by the line model spatial, and respectively temporal, discretization intrinsic to the methods.

## 3.1 Power Network Analog Emulation

After the measurement of the fault signature following a fault occurrence, the heart of the EMTR-based fault location method is the iterative back-propagation of the time-reversed signature in the network replica. This repetitive process is completed in order to locate the energy convergence point, which will hence locate the fault. In previous research ([25],[26],[27],[28], [29]), this operation was executed within an FPGA-based network simulator that provided reliable results in terms of fault location accuracy, but was limited by its long simulation time caused by the complexity of the processing. In this case, a back-propagation iteration cycle lasts about 60 ms [29]. Considering a power transmission line with a typical length of 100 km, from the power systems expectations, a resolution of 1 km, so 1%, would be targeted, implying thus that the back-propagation iteration has to be repeated one-hundred times. Consequently, the duration of the entire process of fault location would last a few seconds, which is much higher than the reference time given by the opening time of a power switch of a few hundred milliseconds. This excessive simulation duration would penalize the real-time functionalities of the grid (e.g. in terms of the reconfiguration time of the power network) in case of a fault occurrence.

This chapter presents an analog alternative to the digital FPGA-based network emulator providing considerable improvements in processing speed, making the real-time implementation of the fault location method possible. In the past, analog emulation has already been used as a power system real-time simulator. For instance, previous research has applied it as a predictive tool to solve power network stability issues ([19],[20],[21],[22],[23]), as it can replicate the physical phenomena taking place in the network with a certain scale factor, and thus scale the processing time accordingly. However, this improvement in terms of computational speed is paid for by certain consequences: the emulator is sensitive to electrical parameters, and the corresponding tolerance, mismatch and variation (e.g. with temperature); the programmability of the system is restrained by the hardware model; and the development time and cost of such a dedicated system can be also much higher than other computer- or FPGA-based digital solutions, as illustrated in Fig. 3.1.

The sensitivity of an analog emulator to electrical parameters and parasitics (e.g. mismatch, parameter tolerance, non-linearity, offset, etc.) is unavoidable and can affect the accuracy of the simulation. However, there are many different options to minimize these undesirable factors. Indeed, the appropriate selection of the topology of the emulator and its calibration is essential and can simply cancel the impact of some parasitics on the process. Moreover, an Integrated-Circuit (IC) implementation of the circuitry improves the control of the electrical parameters, increases the matching characteristics, minimizes the parasitics, etc., and therefore limits their impact on the emulator's behavior. For these reasons, the presented analog emulator will be implemented as an Application Specific Integrated Circuit (ASIC).

In addition to the uncertainties caused by the electrical parameters, the emulator itself is also a cause of inaccuracies. The selected network model, its resolution, the signal sampling, etc.,

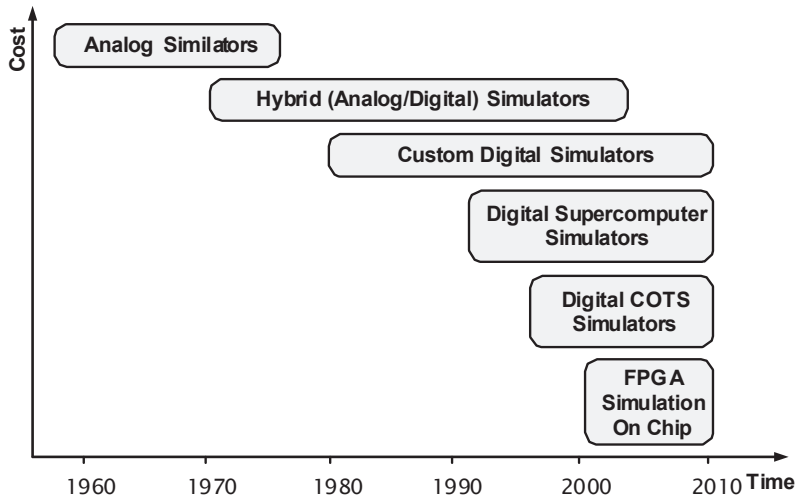


Figure 3.1: Evolution of real-time simulation (from [24]).

can affect the precision of the process, and this, independently of the nature of the emulator (analog or digital). Therefore, particular attention has to be paid to the model's ability to imitate real behavior, according to the process conditions.

As a premise of the design of the analog emulator, it is necessary to quantify the impact of all the pre-cited sources of inaccuracy, and consequently define a maximum tolerance for the fault location process that meets the expectations of the power network. Consequently, the following chapter defines the requirements for the analog emulator in terms of fault location resolution and processing time, and presents two different implementation approaches. In the first method, the transmission line is mapped into a ladder of identical inductor-capacitor (LC) cells, each modelling a discrete line element. The second approach emulates the line with a series of elementary delay cells, implementable with simple switched-capacitor (SC) circuits. The impact of the line model, its discretization and time sampling, intrinsic to the methods, will be also discussed.

## 3.2 Process Duration and Resolution

Whether analog or digital, a practical implementation of the emulated line requires its discretization into $N$ elements between which the guessed fault could be switched, at each back-propagation iteration. This space (or time) quantization defines the fault location minimum resolution as

$$r = \frac{1}{N} \tag{3.1}$$

and consequently the processing time, proportional to the number of back-propagation iterations. The trade-off *processing time* versus *fault location resolution* has to be considered carefully, so that the thinner EMTR process maxima (referring to the fault current energy in Fig. 2.8) remains detectable in a sufficiently short duration, in order to satisfy the real-time conditions. In the present case, the resolution is set to $r = 1\%$ of the line length, similarly to existing digital fault location solutions. Consequently, a fault can be located within 1 km, considering a typical power transmission line that is 100 km long. Therefore, this resolution sets the line discretization according to (3.1), so that

$$N = 100. \tag{3.2}$$

### 3.2.1 Line Model Discretization

The signal propagation in a lossless transmission line is not affected by distortions since the phase propagation velocity is independent of the frequency. As illustrated in Fig. 3.2-(A), a lossless line can be therefore characterized by its length $D$, or equivalently, by its corresponding propagation time [48] given by

$$T = D\sqrt{L'C'}, \tag{3.3}$$

where $L'$ and $C'$ are the distributed per unit length line inductance, and capacitance. Similarly, the emulated line of length $D$, or propagation time $T$, can be discretized into $N$ length elements $\Delta D$, or respectively time delay elements $\Delta T$, at which the guessed fault is successively evaluated (Fig. 3.2-(B)). Hence, the guessed fault location $x'_f$, or corresponding line propagation time $t'_f$, is assimilated to a discrete guessed fault tap $n'_f$, so that

$$\begin{cases} x'_f = n'_f \Delta D \\ \\ t'_f = n'_f \Delta T. \end{cases} \tag{3.4}$$

The spatial or temporal quantization of the emulated line doesn't affect the result of the fault current by itself, however, it induces a loss of accuracy in the location process due to the finite resolution.

### 3.2.2 Duration of the Process of Fault Location

In the presented hardware model, the behavior of the power network to emulate is imitated by an analog circuit, according to a given scale factor $\kappa \ll 1$. Consequently, the physical phenomena taking place in that network, similarly to the processing time, are scaled in time

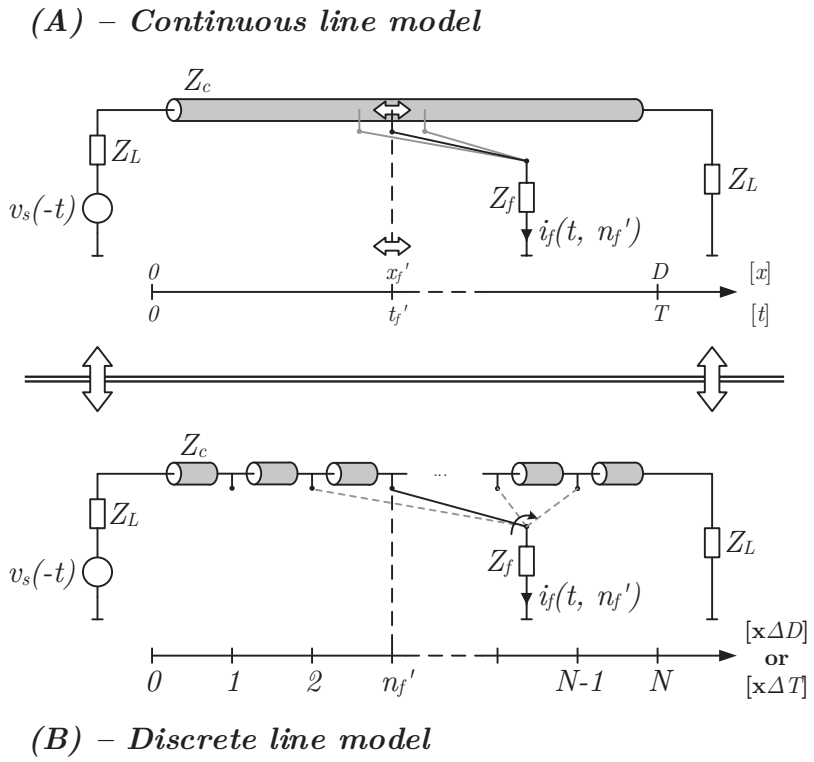


Figure 3.2: Continuous power transmission line model (A) and its discretized equivalence (B).

proportionally. Therefore, the duration of the entire fault location process given by (2.9) and linked to this time scale factor $\kappa$ becomes then

$$T_{EMTR} = \frac{2 \cdot \kappa \cdot T_s}{r}, \tag{3.5}$$

where $T_s$ is the duration of the fault signature and $r$ the process resolution. The back-propagated time-reversed fault signature has to be scaled in time by the same factor to match the emulated line. The following analysis shows that the line propagation time can be scaled in a realistic way by a factor $\kappa = r = 1\%$, so that the full process duration lasts only twice as long as the fault signature ($T_s \simeq 80$ ms according to Section 2.3.2), and thus, yields $T_{EMTR} \simeq 160$ ms. As a consequence, this duration is much shorter than the one obtained with the FPGA-based method. This speed gain is a definite improvement in comparison to other classical numerical methods and makes real-time implementation realistic.

## 3.3 Lumped Inductor-Capacitor Line Model

The first analog emulation approach is based on the discretization of the infinitesimal lossless line model. In this method, the distributed parameters transmission line, defined by its per unit length inductance $L'$ and capacitance $C'$ (Fig. 3.3-(A)-(B)) is replaced by a ladder of

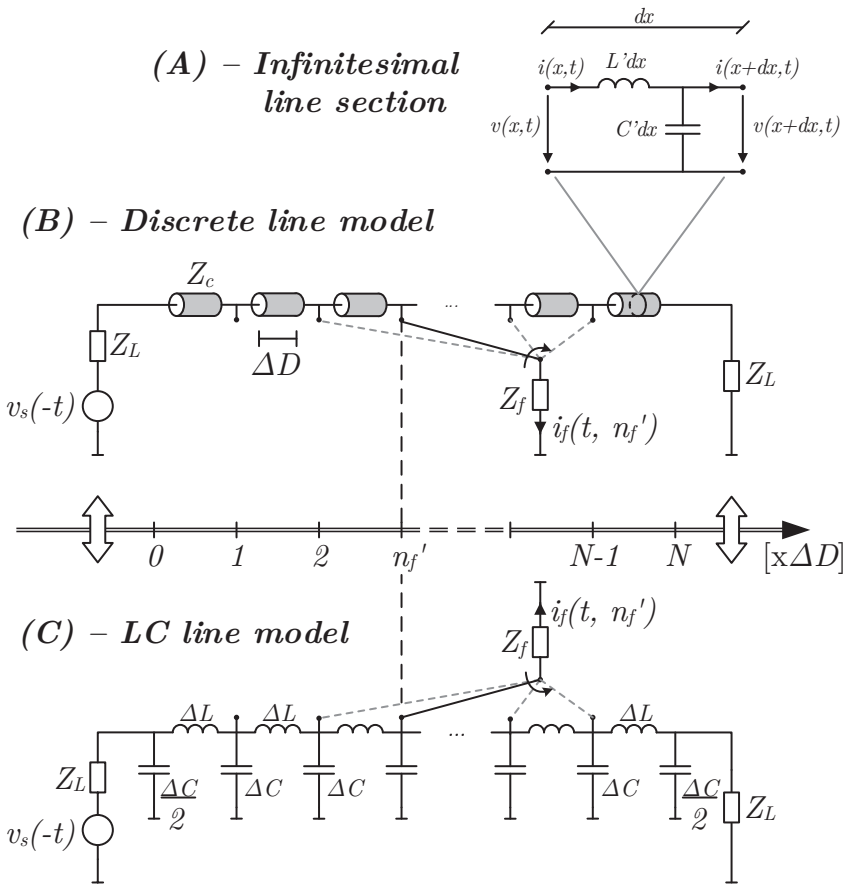


Figure 3.3: Discretized distributed parameters line and equivalent lumped LC model.

inductor capacitor cells (Fig. 3.3-(C)). This derived lumped parameters line model consists of $N$ equivalent LC PI cells, each composed of a series inductor $\Delta L$ bounded by two shunt capacitors of $\Delta C/2$. The LC line parameters are set so that each cell has an equivalent inductance, and respectively capacitance, to a $\Delta D$ section of the real line scaled by the factor $\kappa$ so that

$$\begin{cases} \Delta L = \kappa L' \Delta D \\ \\ \Delta C = \kappa C' \Delta D. \end{cases} \tag{3.6}$$

Consequently, the cumulated inductance $L$, and capacitance $C$, of the full LC line of $N$ equivalent elements is similarly given by

$$\begin{cases} L = N\Delta L = \kappa D L' \\ \\ C = N\Delta C = \kappa D C', \end{cases} \tag{3.7}$$

| Distributed Line | | Discrete Line |
|---|---|---|
| $Z_c = \sqrt{\frac{L'}{C'}}$ | = | $Z_c = \sqrt{\frac{\Delta L}{\Delta C}}$ |
| $T_L = D\sqrt{L'C'}$ | $\xrightarrow{\cdot\kappa}$ | $T_{LC} = N\sqrt{\Delta L \Delta C}$ |
| $\omega_o \to \infty$ | | $\omega_N = \frac{2N}{\sqrt{LC}}$ |

Table 3.1: Characteristics of the distributed and discrete parameters line models.

where $D$ is the length of the entire distributed parameters line. The LC discrete line model equals the distributed parameters line if the number of LC elements $N$ tends to infinity, so that the discrete inductor $\Delta L$ and capacitor $\Delta C$ appear as infinitesimals. In practice, both models can be considered as equivalent if this number of LC elements is sufficiently high. Therefore, both the distributed parameters and the LC line model can be characterized by the equations in Table 3.1. The line surge impedance $Z_c$, given by the ratio of the inductive and capacitive parts, is the same for both line models. However, the total line propagation time of the LC line $T_{LC}$ is shorter by a factor of $\kappa \ll 1$ than the distributed parameters line $T_L$, which highlights the time scaling of the model, and so its corresponding simulation time. The zero-dB cutoff pulsation is infinite regarding the infinitesimal line model, however, with finite $\Delta L \Delta C$ components, the corresponding parameter $\omega_N$ is finite and is proportional to the line discretization $N$.

### 3.3.1 Line Model Validation

The distributed parameters line model and the LC model are equivalent only if the discretization is infinite ($N \to \infty$) or very high. However, for lower discretizations, a divergence between both line behaviors is to be expected. To quantify this error, the accuracy of the LC line model is evaluated by comparing its transfer function with that of the distributed parameters line definition at equal size, thus, with $\kappa = 1$. For this purpose, the ideal transmission line of length $D$ and its equivalent LC discretization by $N$ are set with an equal cumulated inductance and capacitance that yields $L = N\Delta L = DL'$, and respectively $C = N\Delta C = DC'$. Both lines are terminated by reflection coefficients, $\rho_L \simeq 1$ at the line input and $\rho_f \simeq -1$ at its output, similarly to the cases studied in Section 2.3.3. From (2.13b), the transfer function of the distributed

parameters line is given by

$$H_L\left(j\omega, D\right) = \frac{(1-\rho_L)(1+\rho_f)}{2}\frac{e^{-j\beta D}}{1-\rho_L\rho_f e^{-2j\beta D}} \tag{3.8a}$$

$$\beta = \omega\sqrt{L'C'}. \tag{3.8b}$$

On the other hand, the LC line transfer function calculated in Appendix B.1 is given as a function of its discretization $N$, and yields

$$H_{LC}(j\omega, N) = \frac{1}{a_0 cos(NX) + j a_1 sin(NX)} \tag{3.9a}$$

$$a_0 = 2\frac{1-\rho_L\rho_f}{(1-\rho_L)(1+\rho_f)} \tag{3.9b}$$

$$a_1 = \frac{1-\rho_f}{1+\rho_f}\frac{2}{\sqrt{4-\Delta\beta^2}} + \frac{1+\rho_L}{1-\rho_L}\frac{\sqrt{4-\Delta\beta^2}}{2} \tag{3.9c}$$

$$X = Arctan\left(\frac{\Delta\beta\sqrt{4-\Delta\beta^2}}{2-\Delta\beta^2}\right) \tag{3.9d}$$

$$\Delta\beta = \omega\sqrt{\Delta L\Delta C} = \frac{\omega}{N}\sqrt{LC}, \tag{3.9e}$$

Equations (3.9) are defined in the range $\omega \leq \omega_N$, regarding Table (3.1). The magnitude of the transfer functions of both line models are compared in Fig. 3.4, where the distributed parameters line has a length of $D = 1$ and its lumped approximation is shown for $N = \{1, 2, 5\}$ elements. Without loss of generality, the reflection coefficients are set to $\rho_L = 0.99$ and $\rho_f = -0.99$. The response magnitude confirms that the discretized model is a good approximation of the transmission line for bandwidths much lower than the zero-dB frequency $\omega_N$. However, in the case of a fault location, where fault signatures of high bandwidth travel in the line, a low number $N$ of PI cells will clearly affect the accuracy of the process. This distortion translates to an equivalent emulated line length error, and so to a proportional fault location error $\delta x_f$. As calculated in Appendix B.2, the latter can be evaluated by comparing the position of the first resonance in the transmission line transfer function and that of its lumped approximation.

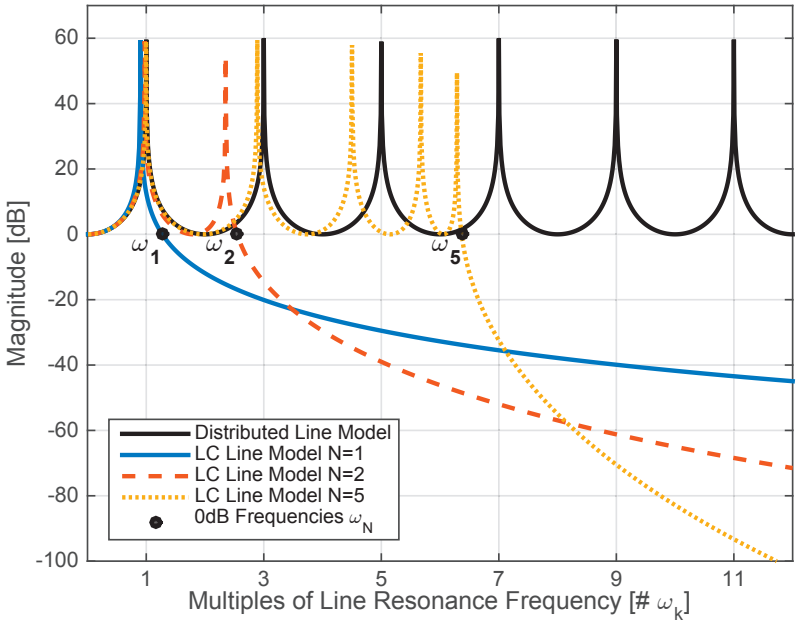


Figure 3.4: Magnitudes of the transfer functions of the distributed and lumped LC line models.

Therefore, the fault location error $\delta x_f$ as a function of the evaluated discrete fault tap $n_f$ is

$$\delta_{x_f}(n_f) = \frac{1}{N}\left(\frac{\frac{\pi}{4n_f}}{sin\left(\frac{\pi}{4n_f}\right)} - 1\right). \tag{3.10}$$

This result is confirmed by transient fault location simulations in Fig. 3.5. The error is a maximum for faults situated near the line input, when the remaining line piece between its input and the fault is only constituted of a few LC cells. For higher fault location values, the error tends rapidly to zero. Considering an emulated line made of $N = 100$ LC elements, the maximum error caused by the line model distortion is about 0.1% at $n_f = 1$. This error is negligible since the minimum resolution set by the number of taps $N$ at which a guessed fault can be simulated is equal to $r = 1/N = 1\%$.

### 3.3.2 Matching Analysis

In a microelectronic implementation, a calibration of the total emulated line delay is mandatory to consistently set the time scale of the time-reversed, back-propagated fault signature. However, random variations of the elementary lumped LC section are unavoidable. This analysis evaluates the impact of statistical variations of the line parameters on the accuracy of the fault location. For this purpose, the emulated line is considered as a series combination of $N$ transmission lines of length $\Delta D$, with associated propagation time $\Delta T$ and reflection

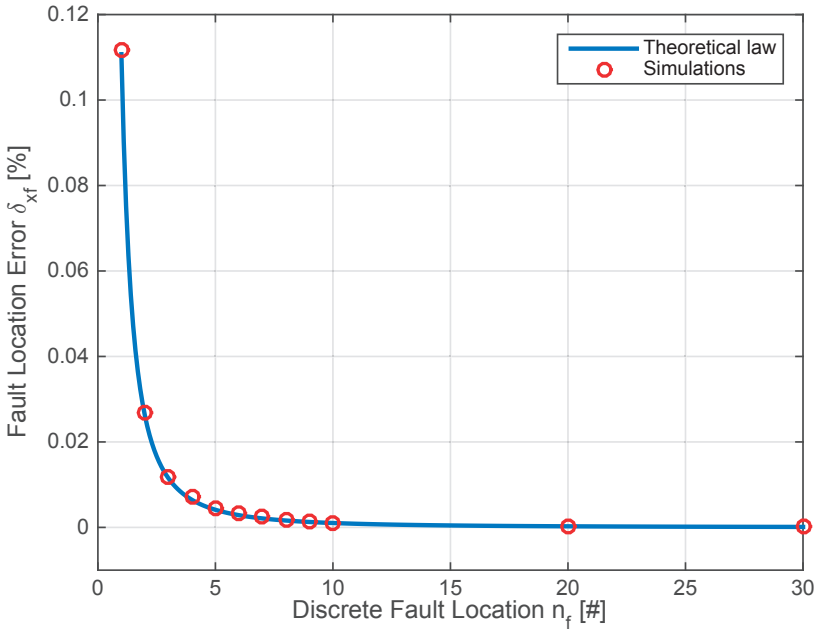


Figure 3.5: Equation (3.10) and simulations of the fault location relative error $\delta_{x_f}$.

coefficients $\rho_L$ and $\rho_f$. Simulations and [25] showed that the variations of the reflection coefficients has no significant impact on the precision of the fault location, and thus only statistical variations of $\Delta T$ are considered in the analysis. The propagation time error translates into a line length error, or equivalently a fault location error. Assuming that a calibration procedure, based on the measurement or control of the total line propagation time $T$, is performed, the standard deviation of the fault location error cumulated at the $n_f^{th}$ line tap after calibration is calculated in Appendix B.3 and yields

$$\sigma\left(\frac{n_f}{N}\right) = \frac{\sigma(\Delta T)}{T}\frac{(N-n_f)\sqrt{n_f}+n_f\sqrt{N-n_f}}{N}, \tag{3.11}$$

where $\sigma(\Delta T)$ is the single line segment standard deviation. Fig. 3.6 compares (3.11) to Monte Carlo simulations of the line response after calibration, with a standard deviation per element of $\sigma(\Delta T)/T = 1\%$. As expected, the error resulting from random parameter variations after calibration is highest in the middle of the line. Accordingly, a target maximum fault location error of 1% at $\pm 3\sigma$ requires that the matching accuracy of the elementary lumped LC delay is better than 2.4% rms, an acceptable constraint for an analog IC implementation.

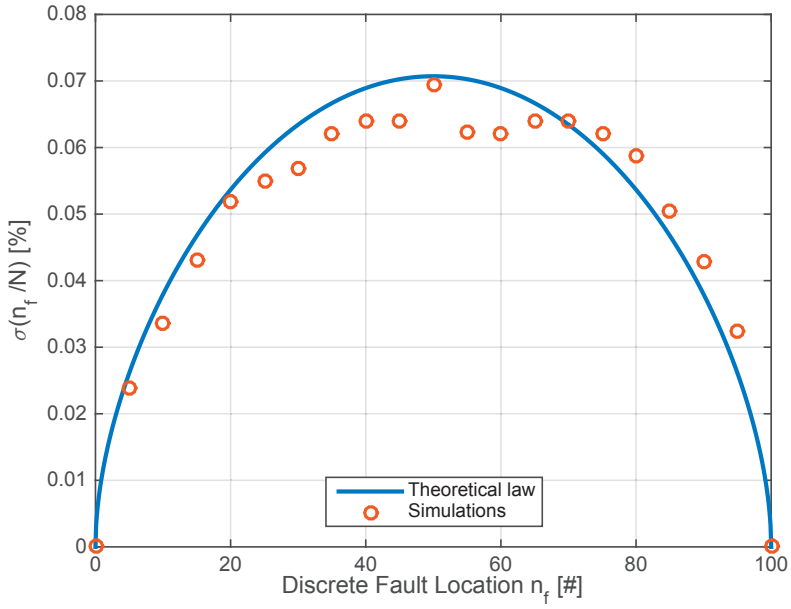


Figure 3.6: LC line fault location relative error as a function of the random mismatches after calibration.

### 3.3.3 Summary

This section has presented an inductor-capacitor ladder based circuit aimed at power network transmission line emulation. The model is based on the discretization of the distributed parameters line definition into a finite number $N$ of lumped LC elements forming a PI shape. Theoretical analysis has shown that the emulated line propagation time, and so the duration of the fault location process, can be simply scaled by scaling the inductors and capacitors of the ladder by a factor $\kappa \ll 1$, which brings the real-time expectations within reach. In addition, it has been demonstrated that the model accuracy, and thus, that of the fault location process, increases with the number of PI cells emulating the line, according to the formula (3.10). In the worst case, when a single PI element emulates the line section, the equivalent fault location error reaches 0.1%, which is much lower than the 1% targeted process resolution, and is therefore negligible. Another undesirable effect degrading the model's accuracy is the random variation of the elementary cell parameters, equivalent to a propagation time error. Despite a mandatory time calibration, this mismatch affects the fault location precision and is greatest for faults occurring in the middle of the line, as stated by the formula (3.11). However, this error can be maintained below the process percent resolution with acceptable analog IC design constraints, which makes it tolerable. Through this analysis, the validity and the limitations of the LC line model have been demonstrated. It has been shown that with given constraints, the model is adequate for the power network emulation in the presented fault location context, and that the targeted percent resolution can be reached. Besides the sources of error caused by the model itself, additional inaccuracies linked to the microelectronic

implementation also affect the fault location process, as studied in Chapter 4.

## 3.4 Discrete-Time Line Model

The second power network emulation approach is based on a discrete-time representation of the general solution of the telegrapher's equation describing the signals propagated in a transmission line (2.1). As presented in Section 2.3.1, the voltage and current at any line coordinate can be assumed as a sum, or difference respectively, of an incident and reflected wave propagated along the line. Consequently, the discrete transmission line in Fig. 3.7-(A) can be replaced by two parallel and unidirectional delay paths for the forward and backward propagated waves, and corresponding reflection coefficients $\rho_k$ at the boundaries, as illustrated in the block diagram in Fig. 3.7-(B). Each path consists of a row of $N$ identical delays $\Delta T$, corresponding to the propagation time of a section $\Delta D$ of the initial line. The elementary delay can be accurately implemented with discrete-time circuits, such as with switched-capacitors, controlled by a sampling period set to $\Delta T$. The line discretization implies a discretization of equations (2.5) defining the voltage $V_n$, and respectively current $I_n$ at each $n^{th}$ line tap, as a function of the incident $V_n^+$ and reflected $V_n^-$ waves, so that

$$\begin{cases} V_n &= V_n^+ + V_n^- \\ Z_c I_n &= V_n^+ - V_n^-. \end{cases} \tag{3.12}$$

These propagated waves evolve independently along the line until they reach an end or the fault, where they are reflected or transmitted according to the corresponding coefficient $\rho_k$. Both line ends are characterized by a reflection coefficient $\rho_L$ that weights and reflects the incoming wave in the opposite direction. At the guessed fault position $n'_f$, a signal fraction is reflected in the opposite direction, as the other part is transmitted to the following line section, according to the reflection or transmission coefficients $\rho_r$, and $\rho_t$ respectively. From calculations in Appendix B.4, the fault equivalent transmission and reflection coefficients as a function of the fault reflection coefficient $\rho_f$ are given by

$$\begin{cases} \rho_t &= 2\frac{\rho_f+1}{\rho_f+3} \\ \rho_r &= \rho_t - 1. \end{cases} \tag{3.13}$$

Since the fault has a very low impedance in comparison to the surge impedance, the fault reflection coefficient is close to $\rho_f \simeq -1$, so that the wave is mostly reflected and almost not transmitted to the following line section, as shown by (3.13). In this precise case, the line section beyond the fault has a very low influence and could be neglected in a first approximation.

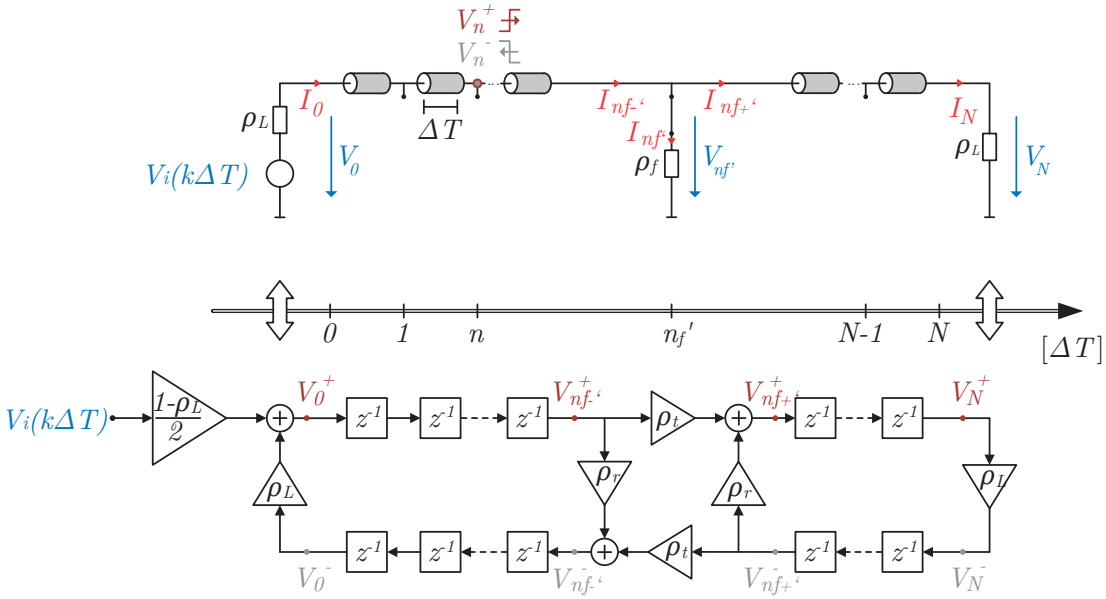


Figure 3.7: Ideal transmission line model and equivalent sampled-data model.

According to the discrete line model block diagram in Fig. 3.7-(B), the normalized fault current to be measured results from the difference between the line currents just before and after the fault, at positions $n'_{f-}$ and $n'_{f+}$ respectively, and translates in the propagation wave domain to

$$Z_c I_{n'_f} = -2\rho_r \left( V^+_{n'_{f-}} + V^-_{n'_{f+}} \right). \tag{3.14}$$

### 3.4.1 Time Basis

A discrete-time implementation offers a precise time basis and avoids any matching issues between the delay elements, and thus, an associated time calibration of the line is not necessary. Moreover, the cumulated propagation delay over the full line can be directly set and scaled by the switching frequency of the system, thus scaling the fault location process duration accordingly. Similarly to the LC line model, a time scale factor of $\kappa = 1\%$, equivalent to an increase of the clock frequency by a factor of 100, scales the process duration accordingly, and thus brings the power system real-time expectations within reach.

### 3.4.2 Impact of the Sampling

The discrete-time line implementation implies a sampling of the processed signals, which limits their frequency bandwidth, and thus can add distortion in the fault location. To illustrate this effect, the fault location result calculated through the discrete-time line model frequency response is analyzed in the following section. In parallel to continuous-time, the frequency domain representation of the unity delay $\Delta T$ translates to its discretized equivalence in the $z$-domain as

$$e^{-j\omega\Delta T} \rightarrow z^{-1}. \tag{3.15}$$

Therefore, in parallel to (2.13b), the discrete-time line response constituted by $N$ unity delays and bounded by reflection coefficients for the load of $\rho_L$ and the fault of $\rho_f$ in the $z$-domain yields

$$H_{DT}(z,N) = \frac{(1-\rho_L)(1+\rho_f)}{2}\frac{z^{-N}}{1-\rho_L\rho_f z^{-2N}} \tag{3.16}$$

and is defined in a bandwidth limited by the Nyquist frequency set by $f_N = \frac{1}{2\Delta T}$. Similarly to (2.17), the fault current magnitude as a function of the normalized pulsation $\Omega = \pi f / f_N$ can be approximated by

$$\begin{aligned} \left|I_f\left(j\Omega, n'_f\right)\right| &\propto \left|H_L\left(j\Omega, \frac{t_f}{\Delta T}\right)\cdot H_{DT}\left(j\Omega, n'_f\right)\right| \\ &\propto \underbrace{\frac{1}{\left|cos\left(\Omega\frac{t_f}{\Delta T}\right)\right|}}_{|H_L|}\cdot\underbrace{\frac{1}{\left|cos\left(\Omega n'_f\right)\right|}}_{|H_{DT}|} \end{aligned} \tag{3.17}$$

where $H_L$ is the sampled faulted line frequency response, with a fault situated at a propagation time $t_f$ from its input. The time discretized EMTR result is obtained through the evaluation of the RMS fault current in the range $\Omega \in [-\pi;\pi]$, set by the sampling frequency. Since (3.17) is periodic, its RMS value can be calculated without distortions only if its periodicity, or an integer multiple of it, coincides with the observation window set by $\pm f_N$. This precise case occurs when the ratio $t_f/\Delta T$ is an integer, which is rarely the case since a fault can occur at any position. This distortion is however minimized by the emulated line response $|H_{DT}(j\Omega, n'_f)|$ that acts as a windowing, as it attenuates the response for frequencies near $f_N$. In the case of faults situated far from the line input, translating to a high ratio $t_f/\Delta T$, the RMS value is evaluated over a high number of period, making this side effect negligible.

### 3.4.3 Summary

This section has presented a second power network emulation approach based on the scheme of the travelling waves propagating in the transmission lines. The line model, composed of many time delay elements, is implementable with discrete-time circuits offering an accurate time basis that avoids any matching issues between the delay elements, and thus, any associated time calibration. However, the sampling, intrinsic to the method, limits the frequency bandwidth of the circuit, which can add distortion to the processed signal. Nevertheless, analytical and simulation results have shown that this issue has a minor impact on the fault location process. In addition to the distortions caused by the nature of the model, sources of uncertainty due to the microelectronic implementation of the delay line as switched-capacitor circuits have to be considered, as studied in Chapter 5. The line propagation time set by the cumulated delays, and so also the duration of the fault location process, is driven by the system switching frequency, which can be set within a great order of magnitude. Similarly to the LC line model, the fault location simulation time can be scaled by a factor $\kappa = 1\%$, meeting the power network real-time expectations.

## 3.5 Inductor-Capacitor and Discrete-Time Line Model Simulations

This section compares the EMTR simulation results in typical conditions realized in the discrete-space LC and discrete-time line models and evaluates the impact of the quantification and sampling on the accuracy of the location of the fault. For this purpose, Fig. 3.8 illustrates critical fault location scenarios of faults occurring between two consecutive taps of the discrete line. This simulation is performed for different maxima width, corresponding to faults situated near the line input or output, and with various reflection coefficient magnitudes, $|\rho_L \rho_f|$. Each plot compares simulation results, obtained with continuous, LC and discrete-time line models, according to a quantification of $N = 100$.

The upper graph presents a favorable location case providing a wide maximum, resulting from a fault that has occurred far from the line input. The fault situated at 90.5% of the line length $D$ is easily localized in each line models through an interpolation of the two adjacent discrete peaks at taps 90 and 91. According to the assumptions of Section 3.4.2, distortions due to the sampling are negligible for faults situated far from the line output. As a consequence, both the LC and sampled-data line model simulation results are highly concordant. The middle graph illustrates a more critical situation, where a sharp maximum occurs between two consecutive taps, near the line beginning, at 3.5% of the line length. The peak is thinner than the process resolution, and therefore, not detected with any line model. To circumvent this issue, the magnitude of the reflection coefficients of the emulated line can be lowered in order to enlarge the maxima (Section 2.3.3), and so make them identifiable. This situation is illustrated in the lower graph, where the same fault signature is back propagated in an emulated line with reflection coefficients decreased to $|\rho_L \rho_f|_{emul} = 0.64$. The global and local maximum become identifiable for both the LC and discrete-time line models. The magnitude of the emulated

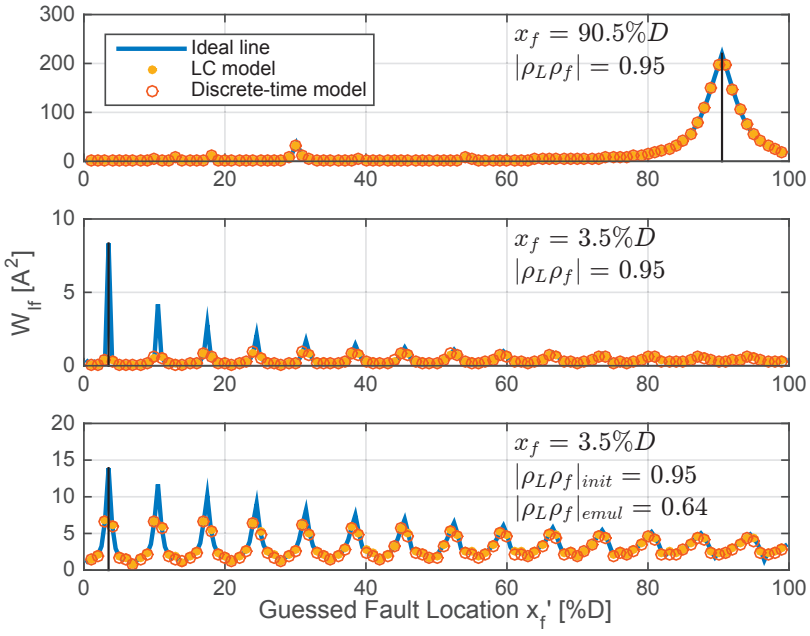


Figure 3.8: EMTR fault location simulations realized in a continuous line (blue), space-discrete LC (orange spots) and time-discrete line models (red circles). The corresponding fault current energies $W_{I_f}$ are displayed for three different scenarios: in the upper graph, a fault occurrence at 90.5%$D$, with initial faulted and emulated line reflection coefficients magnitudes set to $|\rho_L \rho_f|$ = 0.95; in the middle graph, a fault occurrence at 3.5%$D$, with the same reflection coefficients; in the lower graph, a fault occurrence at 3.5%$D$, with an initial faulted line and emulated line reflection coefficients magnitudes set respectively to $|\rho_L \rho_f|_{init}$ = 0.95 and $|\rho_L \rho_f|_{emul}$ = 0.64.

line's reflection coefficients can be adjusted between 0.3 and 1, for a fault situated near the line's beginning, between 0% and 10% of the line length, so that the maximum becomes identifiable and distinguishable from its following echoes. A slight but negligible difference can be noticed between the space-discretized LC and sampled-data simulation results in the two lower graphs. This error in the discrete-time model appears because the periodicity of the fault signature approaches the magnitude of the sampling period.

### 3.5.1 Evaluation of the Line Models

Through the simulations and theoretical analysis realized in this chapter, it can be concluded that both the discrete-space LC and the discrete-time model can be efficiently applied to the fault location method with a sufficient accuracy to ensure the required process resolution of 1%. In the case of the LC model, simulations and analysis have shown that despite random variations of the parameters and their resulting implementation constraints, the error due to the LC model itself are negligible. On the other hand, the discrete-time model slightly

distorts the absolute value of the fault current energy, but affects the fault location process in a negligible way. However, from the simulation results it can be seen that the most probable source of fault location misinterpretation is the discretization of the line into a finite number of taps $N$, at which a guessed fault is successively evaluated. Indeed, if the discretization is too low, sharp fault location maxima, occurring for high magnitude line reflection coefficients and for faults close to the line input, can be missed. Nevertheless, this source of error is independent of the nature of the emulator (digital or analog) and experiments have shown that it can be circumvented by lowering the line model reflection coefficient, which flattens the maxima, and make them thus easier to localize.

## 3.6 Conclusion

This chapter has presented the requirements in terms of processing speed and accuracy for a power network emulator necessary for the back-propagation phase of the fault location method using the EMTR principle. While the presented FPGA-based method provides adequate characteristics in terms of fault location accuracy, its long simulation duration necessitated by its complicated calculations makes difficult any real-time implementations, which is essential for today's power systems. An alternative solution based on analog emulation has been presented. Although the precision of such a hardware model is limited by several constraints, such as its sensitivity to the electrical parameters, it allows reproducing the physical phenomena according to a scale factor that scales the processing time accordingly. It is expected that an IC implemented analog emulator could execute the fault location process within a time scaled by 100 referring to classical methods, with a similar accuracy. For this purpose, two different analog emulation approaches have been presented. In the first one, the power lines are emulated by means of $N$ interconnected lumped LC cells. It has been shown how the finite discretization of the line into LC cells and their random variations affect the model's accuracy, and consequently which implementation constraints and calibration are required to meet the accuracy expectations. The second emulation approach is a discrete-time model based on travelling waves propagating along the line. Thanks to an accurate time basis, this solution is not affected by the random variation of the parameters. However, the sampling, intrinsic to the method, adds a slight distortion to the processed signal. Nevertheless, according to analysis and simulation, this factor is negligible. Both analog emulation approaches provide similar processing speeds, and can ensure a percent resolution in a realistic way, so that a fault can be located within 1 km assuming a typical power transmission line of length 100 km, similarly to today's digital solutions.

# 4 Inductor-Capacitor Line Model Implementation

The previous chapter has demonstrated that the lumped inductor-capacitor line model is suitable for the power network emulation used within the back-propagation phase of the presented fault location technique. Indeed, the processing speed improvement provided by the method, in comparison to classical digital solutions, allows real-time applications, while it offers a sufficient fault location accuracy that ensures the targeted 1% resolution, adequate for typical power systems. This chapter presents a possible IC implementation of the LC line model by means of gyrator-capacitor combinations, also called transconductor-capacitor or gm-C combinations. In this solution, each line inductor is replaced by a corresponding gm-C cell, providing the same properties and more suitable for integration. The corresponding gyrator-C line model characteristics are consequently derived from the ideal circuit representation. However, non-ideal effects caused by the microelectronic implementation, such as finite transconductors output conductance, finite input voltage range, offset, parasitic capacitances, etc. affect the line's behavior and can translate to equivalent fault location errors. Each source of inaccuracy is evaluated independently, in terms of its impact on the line model and on the fault location precision, and corresponding implementation constraints are derived, in order to ensure the expected percent resolution.

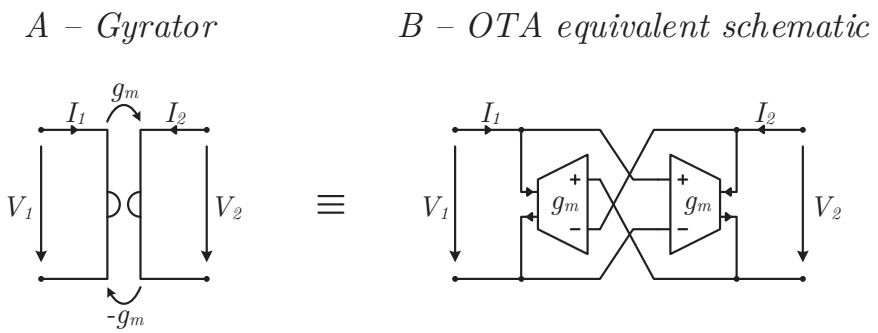


Figure 4.1: Two-port gyrator symbol (A) and equivalent transconductors circuit (B).

## 4.1 Transconductor-Capacitor Line Model

Integrated-circuit implementations of physical inductors is often limited by the large surface required on the chip, the parasitic capacitances between metal tracks, and a bad quality factor due to the metal series resistance. For these reasons, the inductors of the presented LC line model are simulated by gyrator-capacitor combinations, also called transconductor-capacitor or gm-C combinations [54], more suitable for integration. As displayed in Fig. 4.1-(A), a gyrator is a two port that couples the currents and voltages of opposite sides by a transconductance $g_m$ so that

$$\begin{cases} g_m V_1 &= I_2 \\ -g_m V_2 &= I_1. \end{cases} \tag{4.1}$$

This behavior can be reproduced with Operational Transconductance Amplifiers (OTA) of the same transconductance $g_m$, as shown in Fig. 4.1-(B). Similarly, as demonstrated in Appendix D.1, an elementary LC line PI cell can be replaced by an equivalent gm-C circuit that combines this kind of topology with capacitors, as displayed in Fig. 4.2-(A-B). Therefore, the inductor $\Delta L$ is emulated by OTA of identical transconductances $g_m$ and a capacitor of value given by

$$\Delta C = g_m^2 \Delta L. \tag{4.2}$$

Consequently, the entire LC line behavior is reproduced by multiplying $N$ times the same topology and gives a final circuit composed of $2N$ identical OTA of $g_m$ and capacitors of $\Delta C$, as shown in Fig. 4.2-(C-D). From Table 3.1, the according line propagation time and surge

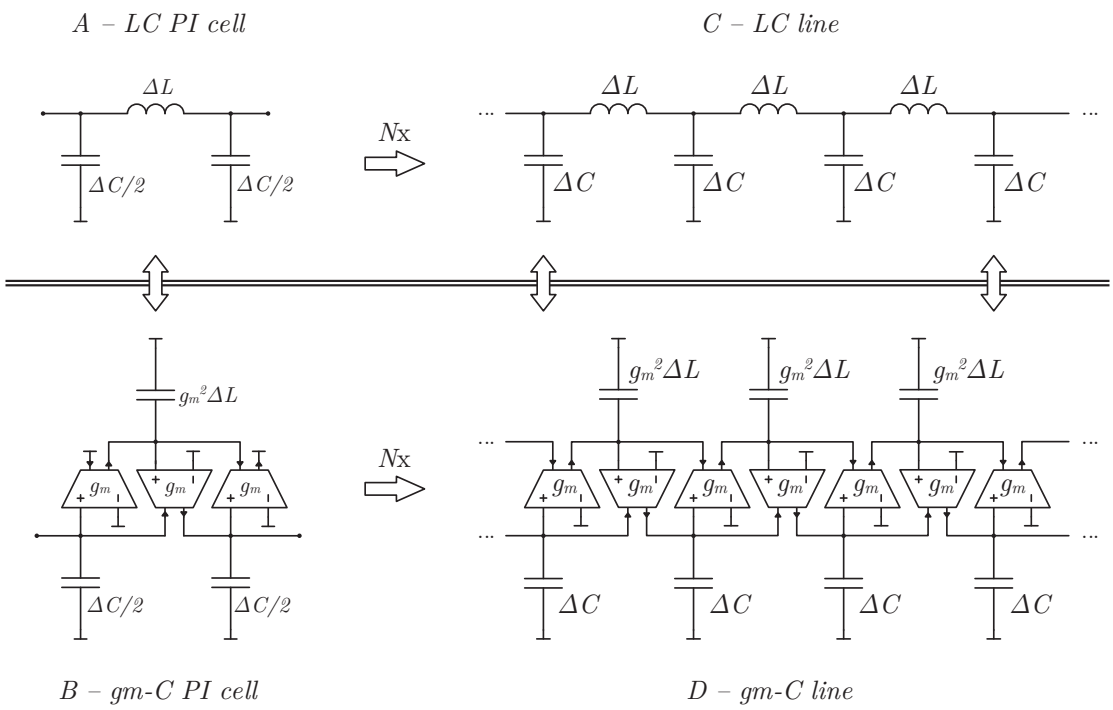


Figure 4.2: Inductor-capacitor PI cell (A) with its equivalent gm-C circuit (B) and LC line (C) with its gm-C equivalence (D).

impedance of the gm-C line, considering a high number of cells $N$, can be easily derived as

$$T = N\sqrt{\Delta L \Delta C} = N\frac{\Delta C}{g_m} \tag{4.3}$$

$$Z_c = \sqrt{\frac{\Delta L}{\Delta C}} = \frac{1}{g_m} \tag{4.4}$$

and shows that the line is directly characterized by the microelectronic parameters.

## 4.2 Line Model Imperfections

In an OTA-C circuit implementation in CMOS technology, care should be taken to minimize the impact of the non-ideal effects associated with active elements $g_m$, such as finite DC gain (or equivalently OTA output conductance), parasitic input and output capacitances, linearity, offsets, and mismatches. These undesirable effects can impact the ideal line model behavior and the fault location process accordingly. Therefore, this section evaluates the consequences of these non-ideal effects and derives associated design constraints that ensure the expected fault location accuracy.

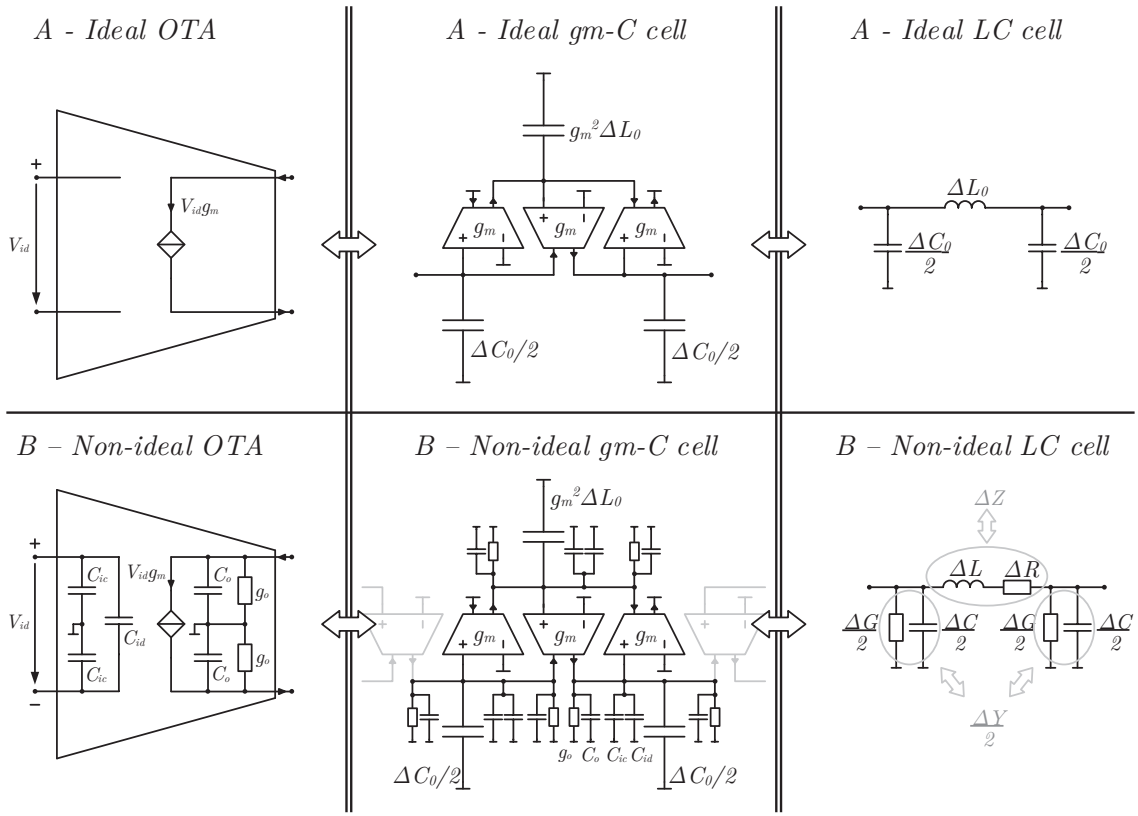


Figure 4.3: Comparison of the ideal (A) and non-ideal (B) OTA and resulting gm-C and LC PI cells.

### 4.2.1 OTA Finite DC-Gain and Parasitic Capacitances

This section evaluates the impact of the OTA input and output parasitic capacitances and the finite output conductance on the emulated line model. For this purpose, both ideal and non-ideal OTA macro models and their corresponding gm-C and LC PI cells are compared in Fig. 4.3 (A) and (B) respectively. While the equivalent LC PI cell is perfectly emulated by ideal gm-C circuits, the non-ideal OTA parasitic capacitances affect the equivalent PI cell inductor and capacitor, and the finite conductance adds an equivalent series resistance $\Delta R$ and shunt conductance $\Delta G$ to the LC model. Consequently, according to transmission line theory [48], the ideal line model becomes lossy, and thus, is characterized by complex and frequency dependent surge impedance and propagation constant that yield

$$\begin{cases} Z_c(j\omega) = \sqrt{\dfrac{\Delta Z}{\Delta Y}} = \sqrt{\dfrac{\Delta R + j\omega\Delta L}{\Delta G + j\omega\Delta C}} \\ \gamma(j\omega) = \sqrt{\Delta Z \Delta Y} = \sqrt{\left(\Delta R + j\omega\Delta L\right)\left(\Delta G + j\omega\Delta C\right)} = \alpha(\omega) + j\beta(\omega), \end{cases} \tag{4.5}$$

where $\alpha$ characterizes the line losses and $\beta$ the phase constant. In addition to the losses, which are not compliant with the time-reversal application hypothesis, the frequency dependency of the parameters causes supplementary distortions of the propagated signal. Indeed, the phase constant $\beta$ is no longer linear in the frequency, and thus, the propagated signal allure varies along the line, making its discretization no longer consistent. However, since the gm-C line topology is symmetric and if the matching of the OTA and the capacitors is assumed as perfect, the line properties greatly simplify. In this case, the equivalent line parameters derived from the gm-C circuit considering the parasitics yield

$$\begin{cases} \Delta C &= \Delta C_0 + C_s \\ \Delta L &= \dfrac{\Delta C}{g_m^2} \\ \Delta G &= 2g_o \\ \Delta R &= \dfrac{\Delta G}{g_m^2}, \end{cases} \tag{4.6}$$

where $\Delta C_0$ is the ideal capacitor, $g_o$ the OTA output conductance and $C_s$ the total stray capacitance, composed of the OTA input common and differential mode capacitance, $C_{ic}$ and $C_{id}$ respectively, and the output capacitance $C_o$ so that

$$C_s = 2C_o + C_{ic} + C_{id}. \tag{4.7}$$

Consequently, with (4.6), the line parameters in (4.5) simplify to

$$\begin{cases} Z_c &= \sqrt{\dfrac{\Delta Z}{\Delta Y}} = \dfrac{1}{g_m} \\ \gamma &= \sqrt{\Delta Z \Delta Y} = \overbrace{\dfrac{2}{A_v}}^{\alpha} + j\overbrace{\omega\dfrac{\Delta C}{g_m}}^{\beta} \end{cases} \tag{4.8}$$

where the OTA DC gain $A_v$ is defined as

$$A_v = \frac{g_m}{g_o}. \tag{4.9}$$

The result in (4.8) shows that the topology symmetry and matching is essential for the model since it cancels any frequency dependency of the surge impedance $Z_c$ and losses $\alpha$, and makes

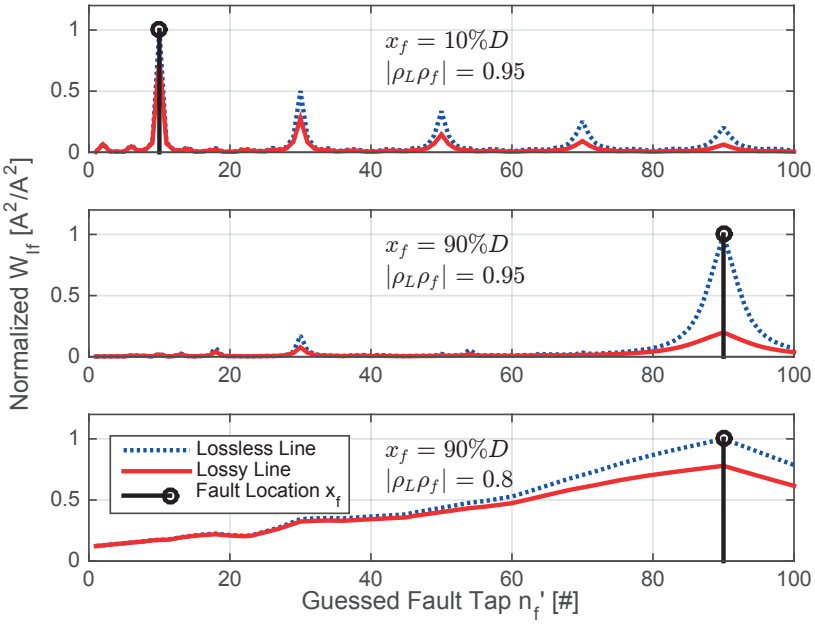


Figure 4.4: EMTR fault location simulations realized in $N = 100$-element emulated lossless and lossy lines with $\alpha_{dB} = 0.004$ dB per element.

the phase constant $\beta$ linear in the frequency, avoiding thus any distortion issues. Furthermore, each line characteristic can be set simply and independently according to the cell capacitors, OTA transconductances and voltage DC-gain. Despite these simplifications, a non-zero OTA output conductance, however, is equivalent to losses in the transmission line, which cannot be simply compensated. Their impact on the fault location and the corresponding DC-gain requirements that ensures a targeted accuracy are studied in the next section. On the other hand, through the proposed topology, the OTA parasitic capacitances can be identified as functional capacitors and properly accounted for in the design phase. These stray capacitances will not modify any of the line properties other than its delay (4.3), which must be calibrated in any case.

### 4.2.2 Impact of Parasitic Losses in the Line Model

As shown in Section 2.2.2, the EMTR process application is restricted to non-dissipative propagation media, which means that both the power line, from which the fault signature originated, and the emulated line model have to be lossless. The power line can be considered so, since the circuit application is principally aimed for power transmission networks, characterized by low losses. On the other hand, the equivalent line losses induced by the finite transconductor DC-gain $A_v$ add distortions in the fault location process. The impact of the finite gain is illustrated through three different EMTR process simulations executed in an emulated line with and without losses, as shown in Fig. 4.4.

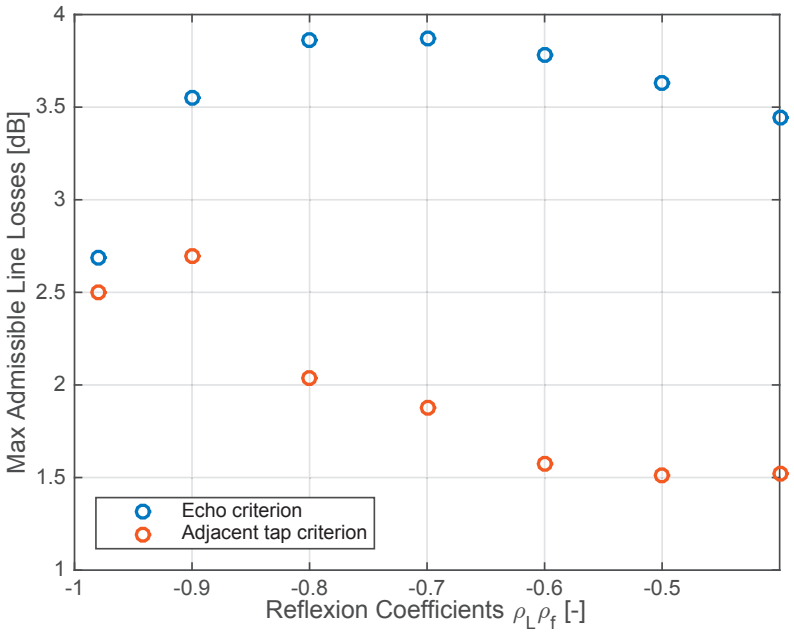


Figure 4.5: Maximum admissible line losses for a proper fault location according to the *Echo criterion* and the *Adjacent tap criterion*.

The upper graph shows a case where the fault location is close to the line input. The global maximum matches with the discrete fault location $n_f$ and is followed by decreasing echoes at positions given by (2.19). The maxima are subject to higher attenuations in the lossy line case, especially those situated far from the line input, more exposed to the per unit length losses. This effect has negligible consequences on the location accuracy for faults situated near the line input. The second graph illustrates a critical situation with a fault situated close to the line end, where the lossy line global maximum is subject to a stronger attenuation. The order of magnitude of the global maximum at $n_f$ is similar to its echo at $n_f/3$ and can lead to a fault location misinterpretation. The lower graph illustrates the same situation with lower magnitude reflection coefficients $|\rho_L\rho_f|$, up to now assumed to be high. As predicted in Section 2.3.3, lower reflection coefficient amplitudes make smoother curves, and thus, the maxima are less perceptible. Since per unit length losses have a higher attenuation effect on taps situated far from the line input, smoother maxima can appear as shifted to the left, generating an error.

Referring to previous simulations, two criteria for the maximum admissible losses can be established, so that the fault remains identifiable within the given resolution. The *Echo criterion* defines the losses for which the highest echo, at $n_f/3$, reaches the same magnitude as the global one at $n_f$. The *Adjacent tap criterion* defines the losses for which the expected global maximum at $n_f$ has the same energy as its adjacent tap at $n_f - 1$, according to the resolution $r = 1/N$. Both criteria define the maximum admissible losses of the line section,

delimited by its input and the discrete fault location at $n_f$, to avoid misinterpretation of the fault location maximum. Simulations displayed in Fig. 4.5 represent these criteria as a function of the reflection coefficients in the application range according to [25]. For high amplitude reflection coefficients, both limitation criteria allow a similar attenuation level in the line section. The *Adjacent tap criterion* becomes more restrictive for lower reflection coefficients, since the maxima are smoother, and limits the losses to 1.5 dB at the most critical point. As a design constraint, regardless of the reflection coefficients and the losses criteria, the line section loss shouldn't exceed 1 dB to ensure a proper fault location. As a consequence, considering the worst case for a fault situated at the line end, with $n_f = N$, the maximum admissible losses between two observation taps is given by

$$\alpha_{dBmax} = \frac{1dB}{N}. \tag{4.10}$$

Therefore, after converting the losses from Decibels to Nepers with

$$\alpha_{dB} = \alpha \cdot 20 \cdot log_{10}(e), \tag{4.11}$$

the minimum admissible transconductor DC-gain for a proper fault location can be calculated through (4.8) and yields

$$A_v \geq \frac{40 \cdot N \cdot log_{10}(e)}{1dB} \tag{4.12}$$

and reaches about $A_v \geq 1750V/$ V for a line discretization of $N = 100$. A folded cascode linear OTA architecture should then be considered to provide the necessary DC-gain [55].

### 4.2.3 Impact of the OTA Offset

The impact of the OTA equivalent input offset on the fault location is evaluated in this section. As illustrated in Fig. 4.6, two different offsets are considered so that $V_{os_{2n}}$ and $V_{os_{2n+1}}$ correspond to the even, and respectively odd, OTA offset of the line. In the LC line model, the even OTA offset $V_{os_{2n}}$ can be simply considered as a current offset of value $g_m V_{os_{2n}}$ in parallel to each equivalent inductors. This DC current is shorted by the lossless inductor, and in consequence, has no effect on the line and on the fault location. Without loss of generality, the odd OTA offset $V_{os_{2n+1}}$ can be removed from the gyrator-C loop and applied in series with the capacitor $\Delta C$. The boundary and fault impedances ($Z_L$ and $Z_f$) appear in parallel to their corresponding $\Delta C$ capacitor. At the DC level, capacitors behave as open-circuits so that every offset source which isn't connected to an impedance is dangling. In consequence, only the three sources connected to an impedance, namely $V_{os_1}$, $V_{os_{2n_f+1}}$ and $V_{os_{2N+1}}$ have an impact on the fault

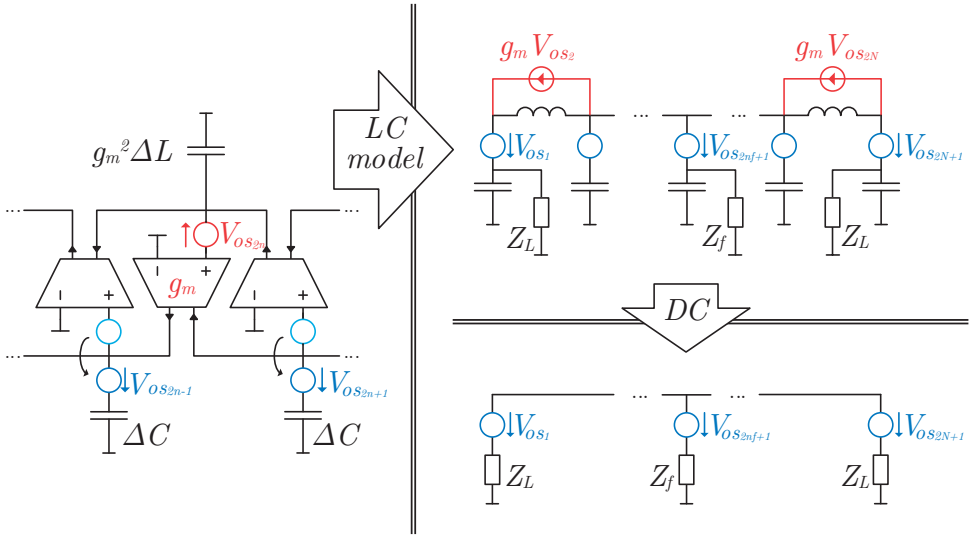


Figure 4.6: OTA offset propagation in the gm-C line.

current, that then yields

$$I_{os_{Z_f}} = \frac{V_{os_1}}{Z_f}\frac{Z_L /\!\!/ Z_f}{Z_L + Z_L /\!\!/ Z_f} - \frac{V_{os_{2n_f+1}}}{Z_f}\frac{Z_f}{Z_f + Z_L /\!\!/ Z_L} + \frac{V_{os_{2N+1}}}{Z_f}\frac{Z_L /\!\!/ Z_f}{Z_L + Z_L /\!\!/ Z_f}$$

$$= \frac{V_{os_1} - 2V_{os_{2n_f+1}} + V_{os_{2N+1}}}{Z_L + 2Z_f} \tag{4.13}$$

In the ideal case, the OTA, their systematic offset is identical, cancelling thus each other's effect. However, their statistical component combines and affects the fault impedance current $I_f$, and so also the fault location itself. The fault current standard deviation as a function of that of the OTA offset $\sigma_{Vos}$ is then given by

$$\sigma(I_f) = \sigma_{Vos}\frac{\sqrt{6}}{Z_L + 2Z_f}. \tag{4.14}$$

Simulations and (4.14) confirm that the offset is independent of the fault location. This interesting property avoids OTA saturation problems linked to an offset accumulation along the line, although it doesn't prevent a fault location error. An offset calibration can be realized by the circuit measuring the fault current in order to cancel this undesirable effect.

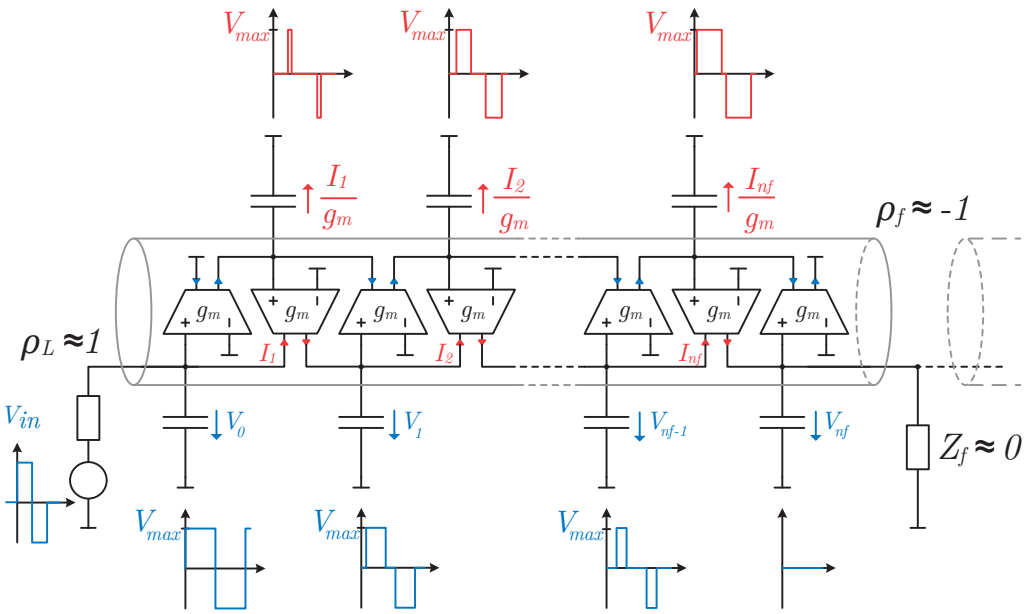


Figure 4.7: Gm-C line transient behavior following a single period of a typical fault signature applied at the input.

### 4.2.4 Impact of the Non-Linearity of the OTA

The consistency of the line model simulated by gm-C topologies is dependent on the signal magnitude, referring to the OTA linear range. The transconductance variation, a function of the input differential voltage, affects the line delay time given by (4.3), and hence the fault location accuracy. This section presents a design criterion based on the ratio between the line input voltage and the OTA linear range to ensure a given fault location resolution. For this purpose, the gm-C line transient behavior is analyzed when a single period of a typical fault signature (Section 2.3.1) is applied at the line input, as shown in Fig. 4.7. Without loss of generality, this approach can be extended to the entire fault signature through the superposition principle. In a first approximation, the fault impedance is considered as a short-circuit, then, only the line section from its input to the fault is taken into account. The period of the input signal is twice the line section propagation time, thus providing the highest voltage amplitudes along the line, and so the highest transconductance deviations. By combining (2.5) and (4.4), the voltage and the current along the $n^{th}$ line tap are respectively determined by the sum and the difference of incident and reflected travelling waves as shown by

$$\begin{cases} V_n &= V_n^+ + V_n^- \\ \dfrac{I_n}{g_m} &= V_n^+ - V_n^-. \end{cases} \tag{4.15}$$

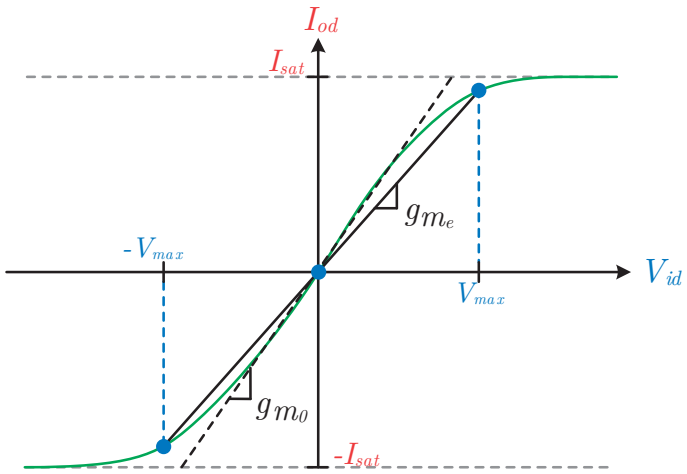


Figure 4.8: OTA transfer characteristic limited by the OTA saturation current $\pm I_{sat}$.

The voltages $V_n$ and the image of the currents $I_n / g_m$ can be observed at each odd, respectively, even, OTA input. Since the reflection coefficient magnitudes are close to one, both travelling waves have the same amplitude $V_{max}$. Hence, the voltage and the current at each line tap are characterized by alternate pulses of various width and amplitudes of $\pm V_{max}$ and $\pm g_m V_{max}$ respectively. In consequence, the maximum OTA input voltage for the linearity analysis is defined as $V_{id_{max}} = V_{max}$, where $V_{max}$ is the largest voltage step measured at the line input.

### Quantification of the Distortions

Fig. 4.8 illustrates a typical OTA transfer characteristic and its small-signal transconductance $g_{m_0}$. The non-linear effect can be quantified by an equivalent first order large-signal transconductance $g_{m_e}$, defined according to the maximum differential input voltage $V_{id_{max}}$. The relative error between the large- and the small-signal transconductance $\delta_{g_m}$ is defined as a limitation criterion for the fault location error. In the following example, this criterion is applied to a gm-C line composed of a differential pair OTA in strong inversion, providing thus a higher linearity range. Therefore, the output differential current $I_{od}$ is given by

$$I_{od} = g_{m_0} V_{id} \sqrt{1 - \left( \frac{V_{id}}{2(V_{GS} - V_{Th})} \right)^2}, \tag{4.16}$$

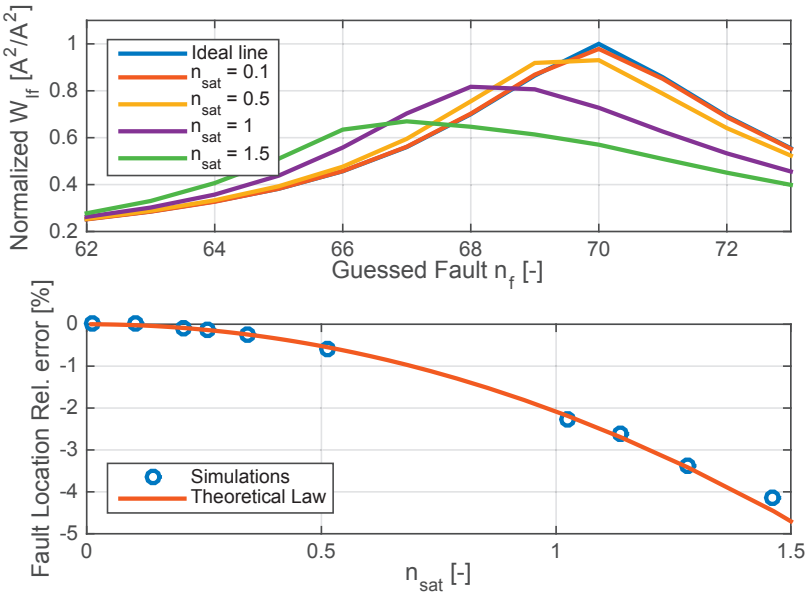


Figure 4.9: EMTR Fault location with various OTA input over gate overdrive voltage ratios $n_{sat}$ (upper graph) and equivalent fault location errors (lower graph).

where the input over gate overdrive voltage ratio can be also denoted as

$$n_{sat} = \frac{V_{id}}{V_{GS} - V_{Th}}. \tag{4.17}$$

The equivalent transconductance error is deduced from the third order approximation of (4.16) and yields

$$\delta_{g_m} = -\frac{1}{8}\left(\frac{V_{id}}{V_{GS} - V_{Th}}\right)^2. \tag{4.18}$$

Over the whole of the back propagation phase, the amplitude of the time reversed fault signature applied to the gm-C line is not constant but decreases with an exponential envelope, as shown in Fig. 2.6. Therefore, the transconductance error will vary accordingly. Based on an exponentially weighted mean of the gm error in (4.18), the equivalent fault location error as a function of the input over gate overdrive voltage ratio can be expressed as

$$\delta_{NL} = -\frac{1}{48}\left(\frac{V_{id}}{V_{GS} - V_{Th}}\right)^2. \tag{4.19}$$

Simulations of the fault location process in an $N = 100$ element gm-C line with various input

over gate overdrive voltage ratios $n_{sat}$ have been realized, and the results are displayed in the upper graph in Fig. 4.9. The simulation was performed with a back propagated time-reversed signature of a fault occurrence at 70% of the total line length. The lower graph represents the simulated fault location maximum relative error superposed with the theoretical law calculated in (4.19). The simulation in the upper graph shows that the reduction of the transconductor linearity flattens the measured energy maximum and shifts it toward the line input. Both the simulations and the theoretical law confirm a quadratic dependency of the process accuracy on the non-linearities. A maximum input over gate overdrive voltage ratio of $n_{sat} = 0.5$ can be tolerated, and the fault location error then remains below 0.5%, and thus ensures the 1% expected resolution. This given ratio can be simply increased using a linearized input OTA, as shown by [56].

## 4.3 Silicon Area, Speed and Power Consumption

The die area for a 100-element gm-C line implementation, consisting of $2N$ capacitors of 0.5 pF each and $2N$ folded cascode OTA with $g_m = 25\,\mu$S, can be conservatively estimated to be two blocks of 0.2 mm$^2$ in a standard 0.35 $\mu$m CMOS process. Consequently, the full circuit area, including the calibration system, the fault current measurement circuit and the control logic, can be estimated to be less than 1 mm$^2$.

In this configuration, the processing speed can be estimated to be 1 ms per iteration, which is one-hundred times faster than current digital solutions, allowing thus real-time implementations.

Regarding the power consumption, the OTA current is set according to the input linear range limited to $V_{GS} - V_T = 1$ V, considering a power supply of $V_{DD} = 3.3$ V. With a transconductance of 25 $\mu$S, the current consumption per OTA reaches then 25 $\mu$A for a differential pair and is simply doubled for folded cascode OTA. Hence, the full line composed of $2N$ OTAs has a total consumption of 10 mA, so about 33 mW. Finally, the full circuit power consumption can be estimated to less than 50 mW.

## 4.4 Conclusion

The EMTR principle can be applied to fault location using the proposed gm-C line emulator. In addition to the intrinsic granularity of the lumped LC approximation of a lossless transmission line, the fault location accuracy is mostly limited by component mismatches (dominating in the middle section of the line), by the OTA's linear range, and by losses that accumulate along the line. A finer segmentation improves the intrinsic accuracy but makes the circuit more sensitive to the DC-gain of the active transconductors. Altogether, a spatial resolution of 1% appears to be a reasonable target for such an analog emulator, given its speed advantage. Compared to a propagation time of a power line of 100 km, analog segmented emulation will typically exhibit a time shrink factor by two orders of magnitude ($\kappa = 1/100$), allowing the location of a fault in a few hundred milliseconds within the targeted resolution of 1%. This processing time is comparable to the power relay opening delay time after a fault occurrence, thus bringing real-time processing within reach.

# 5 Switched-Capacitor Line Model Implementation

This chapter presents a possible implementation of the second power network emulator model based on discrete-time delays. This sampled-data emulator is realized by chains of interconnected elementary switched-capacitor (SC) circuits that simulate the analog delay. The elementary delay cell and derived topologies implementing the line boundaries at its input, output or at the fault position are presented. It is shown how a line model can be realized through simple switched-capacitor topologies that avoid any issues linked to parameter mismatch, finite linearity ranges of the active circuits, and offset, without any calibration procedure. However, the emulator's processing speed and accuracy are still limited by the additional non-ideal effects associated to switched-capacitor CMOS circuits, such as charge injection, clock feedthrough, finite switch conductance, OTA finite transconductance, and equivalent DC-gain. Consequently, the impact of these parasitics on the line model and on the fault location is discussed, and related design constraints are derived in order to ensure meeting the expectations.

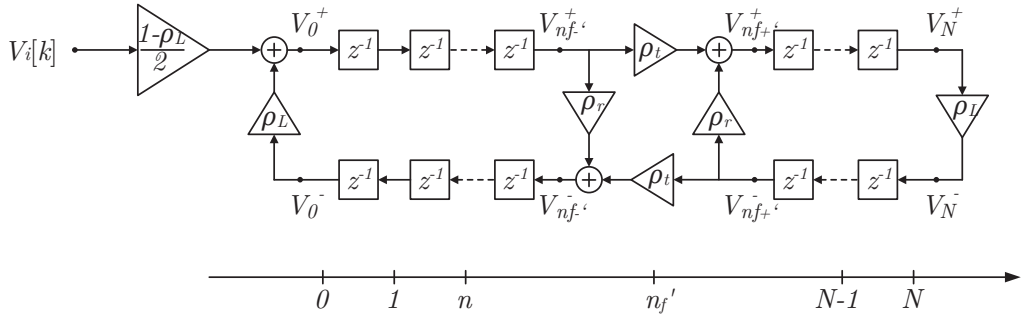


Figure 5.1: Discrete-time transmission line model.

## 5.1 Switched-Capacitor Implementation of the Delay Line

The delay cell represented in the discrete-time emulated line block diagram in Fig. 5.1 will be implemented by means of switched-capacitor cells [62], as illustrated in Fig. 5.2-(A-B). SC circuits provide an accurate delay time settable by the clock period $\Delta T$. The elementary cell is composed of two subcircuits providing half of the sampling period delay, each one built with an inverting amplifier, a capacitor, and two switches. The input signal is sampled on the capacitor during the first clock phase and connected as a feedback to the inverting amplifier acting as a voltage follower during the second phase. Consequently, the delayed signal is available at the cell output only during the second phase, as illustrated in the transient response to a voltage ramp in Fig. 5.2-(C). This sample and hold operation is repeated for the second subcircuit, providing a total delay of $\Delta T$.

The presented delay topology offers two observation points at $V_{n+1/2}$ and $V_{n+1}$, so that the required resolution of 1% is achievable with $N/2 = 50$ full delay elements of $\Delta T$. According to the block diagram of Fig. 5.1, the total line, including two delay lines for the forward and backward propagation of the wave, is composed of $N = 100$ full delay elements of $\Delta T$, or $2N = 200$ half-delay elements of $\Delta T/2$.

### 5.1.1 Charge Transfer and Switching Frequency

At each switching clock phase, the cell capacitors are charged or discharged within a time set by the inverter transconductance $g_m$ and the capacitor value $C$. The charge transfer is completed when the corresponding capacitors can be considered as totally charged or discharged. In switched-capacitor circuits, it is important to set the switching period sufficiently high so that this charge transfer can be properly terminated within the corresponding phase. Considering this critical time, the maximum switching frequency can be set accordingly. The charge transfer duration can be calculated through the transfer function of two adjacent cell capacitor voltages, referring to Fig. 5.2-(B). Considering $V_{C_0}$ and $V_{C_{1/2}}$ as the capacitor voltages of corresponding

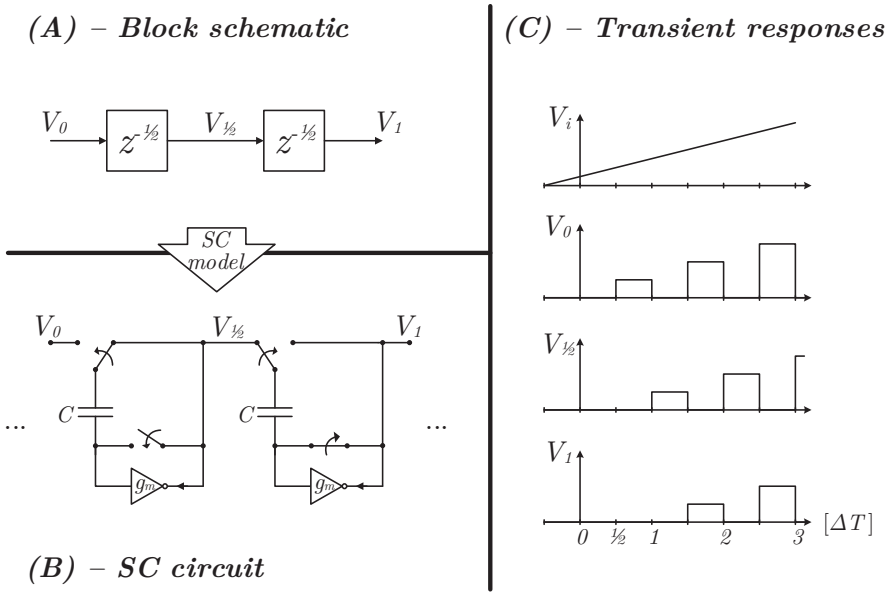


Figure 5.2: Block schematic (A) and SC circuit (B) of a sampling period delay element and corresponding transient response to a voltage ramp at the input (C).

cells $n = 0$ and $n = {}^1/_2$ respectively, the associated transfer function can be expressed as

$$\frac{V_{C_{1/2}}}{V_{C_0}} = \frac{1}{1 + j\omega\tau}, \tag{5.1}$$

where the time constant $\tau$ is given by

$$\tau = \frac{C}{g_m/2}. \tag{5.2}$$

To ensure good performance, this time constant has to be about seven to ten times smaller than one-half of the switching period, so that

$$\tau \leq \frac{1}{7..10} \cdot \frac{\Delta T}{2}. \tag{5.3}$$

Referring to the result in (5.2), high switching frequencies can be reached by increasing the OTAs transconductance through their biasing current and by reducing the size of the capacitors, which, however, increases the circuit's sensitivity to clock feedthrough, charge injection, and thermal noise.

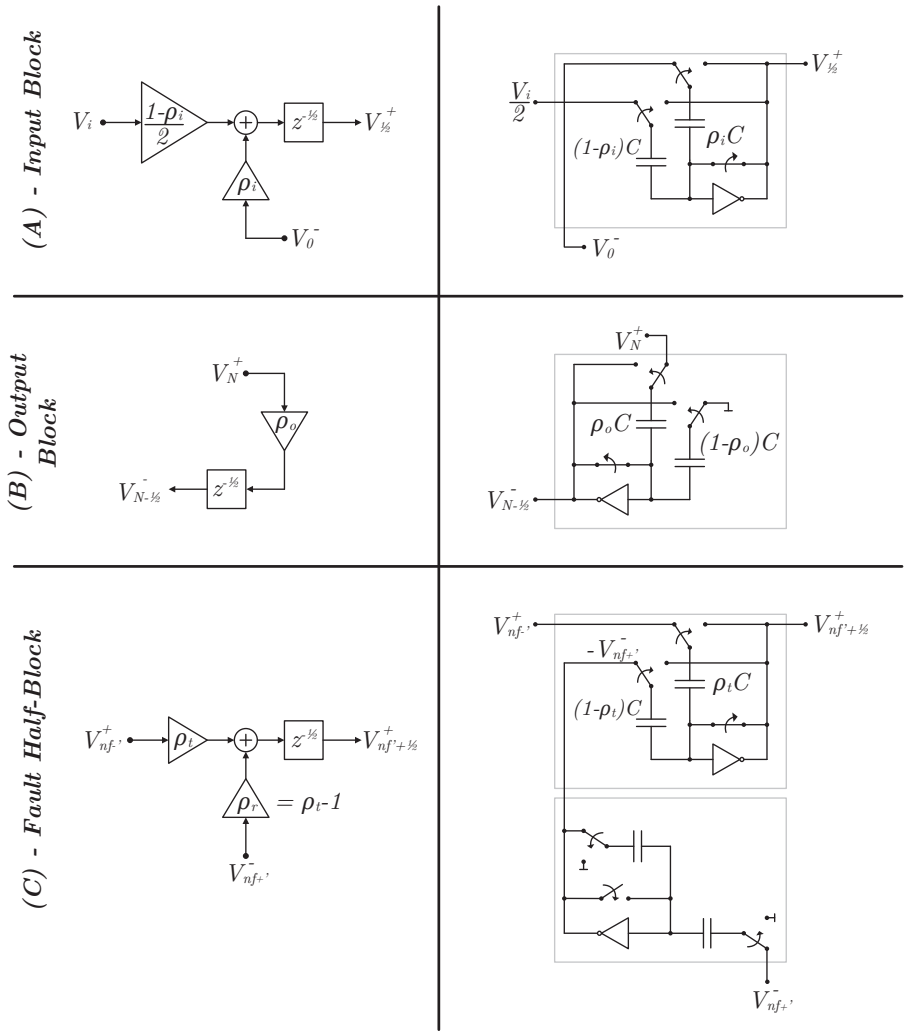


Figure 5.3: Block diagram and equivalent switched-capacitor circuits of the input (A), output (B) and half of the fault cell (C) characterized by their corresponding reflection coefficients $\rho_i$, $\rho_o$ and $\rho_t$.

### 5.1.2 Boundary Cells

The reflection coefficient subcircuit blocks, present at the line input, output and at the guessed fault location, can be realized by switched-capacitor summing amplifiers, as shown in Fig. 5.3. These blocks consists of an extended version of the unity delay cell with two inputs weighted by the corresponding reflection coefficient $\rho$ and by its complement to 1. The implementation of the input termination, represented in (A), is straightforward since the reflected wave is the result of the incident one weighted by $\rho_i$, and summed with one-half of the input signal weighted by $1-\rho_i$. The output termination (B), consisting of a single reflection coefficient $\rho_o$, is realized with the same cell, with the complementary input set to the reference. The guessed fault circuit, consisting of two symmetric adders, one of which is represented in (C), adds the incident wave weighted by $\rho_t$ to the reflected wave weighted by the inverted complement to 1.

This function is realized with an inverter circuit placed before the adder cell's complementary input.

## 5.2 Imperfections due to the Microelectronic Implementation

Switched-capacitor circuits implemented in CMOS technologies are exposed to non-ideal effects that alter the circuit's behavior, and thus, the fault location. Indeed, the parasitics associated to switches, such as charge-injection, clock feedthrough, and finite conductance, or non-ideal effects linked to the transconductors, such as the offset and finite output conductance, can limit the process speed and accuracy. This section analyses and quantifies the impact of each of these non-ideal effect within the context of fault location, and establishes the associated design constraints to ensure meeting the expectations.

### 5.2.1 Impact of the OTA Offset

The equivalent OTA offset can be considered as a constant voltage source $V_{os}$ placed at the input of an ideal OTA, as shown in Fig. 5.4, where a half delay cell is represented during the sampling phase (A), at sample $k$, and during the holding phase (B), at $k+1/2$. After all the charges have been transferred, the signals settle, so that the OTA output current is null, and thus, its input voltage accordingly. Consequently, the capacitor voltage $V_C$ during the sampling and holding phases is obtained through a combination of the offset and input and output voltages, $V_0$ and $V_{1/2}$ respectively, so that

$$\begin{cases} V_C[k] &= V_0[k] - V_{os} \\ V_C[k+1/2] &= V_{1/2}[k+1/2] - V_{os}. \end{cases} \tag{5.4}$$

Since the offset $V_{os}$ is constant and the capacitor voltages during the sampling and holding phases are equal, so that $V_C[k+1/2] = V_C[k]$, the equations in (5.4) combine and give

$$V_{1/2}[k+1/2] = V_0[k] \tag{5.5}$$

Thanks to the auto-zero delay cell topology, the signal is transmitted from the circuit input to its output with a half period delay, without any influence of the OTA offset, which can be thus neglected.

### 5.2.2 OTA Finite DC-Gain and Switches Conductance

Each closed switch is characterized by a finite conductance that impacts the charge transfer between capacitors when they are switched. A bad switch conductance slows down the

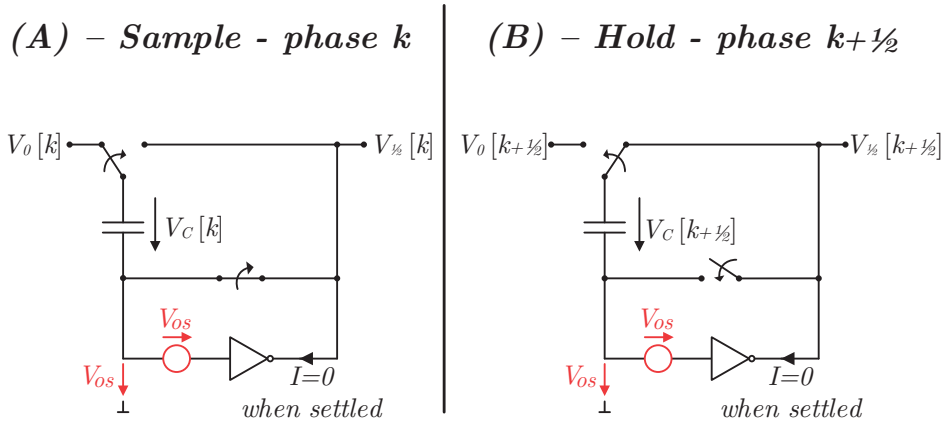


Figure 5.4: Sampling (A) and holding phases (B) of the half delay cell with parasitic OTA offset.

charge transfer, and thus limits the switching frequency, and hence also the fault location processing time. Consequently, a minimum allowable switch conductance has to be defined in order that the process be affected only negligibly. In addition, the impact of the finite OTA DC-gain, or equivalently output conductance, has to be evaluated since it limits the charge transfer between the cells, which translates to losses in the emulated line. The impact of these parasitics is analyzed through the transfer function between two half delay cells, considering the capacitor and feedback switch conductances, $g_{sc}$ and $g_{sf}$ respectively, and the OTA output conductance $g_o$, as illustrated in Fig. 5.5. The charge transfer between the cells $n = 0$ and $n = {}^1/_2$ is evaluated through the current $I_{1/2}$ flowing from one cell to the other. According to the capacitors' voltages $V_{C_0}$ and $V_{C_{1/2}}$ referring to the corresponding cell, and the finite DC-gain defined as $A_v = g_m/g_o$, this current yields

$$\begin{cases} I_{1/2} &= g_m\left(V_{C_0} - V_{1/2}\left(1+\dfrac{1}{A_v}\right)\right) \\ I_{1/2} &= j\omega C V_{C_{1/2}}, \end{cases} \tag{5.6}$$

where $V_{1/2}$ is the voltage between the two cells defined as

$$V_{1/2} = I_{1/2}\left(\frac{1}{g_{sc}} + \frac{1}{j\omega C} + Z_{eq}\right). \tag{5.7}$$

By combining (5.6) and (5.7) with the input equivalent impedance of the OTA assuming the feedback switch given by

$$Z_{eq} = \frac{1}{g_m}\cdot\frac{A_v + g_m/g_{sf}}{A_v+1}, \tag{5.8}$$

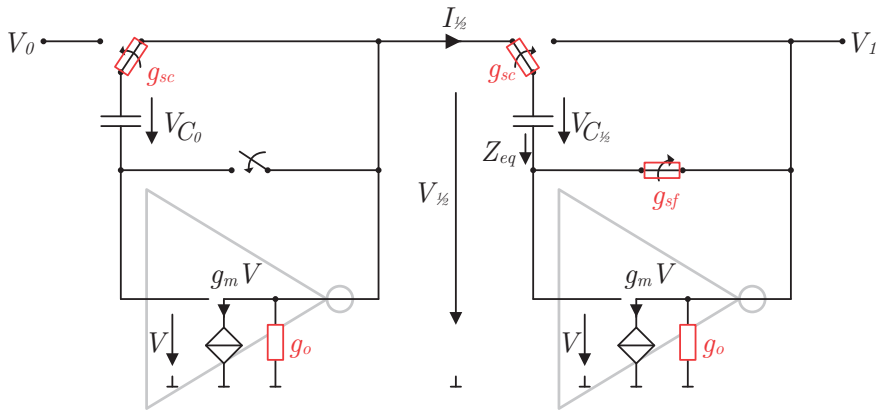


Figure 5.5: Charge transfer among the delay cell considering the switches and OTA output conductances.6

the transfer function between the capacitors voltage of associated cells $n = 0$ and $n = {}^1/_2$ can be expressed as

$$\frac{V_{C_{1/2}}}{V_{C_0}} = K \cdot \frac{1}{1 + j\omega\tau}, \tag{5.9}$$

where $\tau$ is the charge transfer time constant and $K < 1$ represents the cell losses.

### Equivalent Losses

The equivalent losses in the switched-capacitor line model can be approached similarly to those taking place in the transconductor-capacitor line model studied in Section 4.2.2. From equation (4.10), it is known that the maximum tolerable losses for proper fault location are 1 dB for the total line. Therefore, the maximum attenuation of the switched-capacitor cell has to be defined accordingly. According to (5.9), the equivalent half delay cell losses as a function of the OTA DC-gain $A_v$ are given by the attenuation factor that yields

$$K = \frac{1}{1 + \frac{1}{A_v}}. \tag{5.10}$$

Hence, the total line attenuation yielding $K^N$, assuming $N = 100$ half delay elements, should remain below the loss threshold of 1 dB. Consequently, with (5.10), the minimum allowable OTA DC-gain is given by

$$A_v \geq \frac{1}{10^{\frac{\alpha_{dB}}{20N}} - 1} \tag{5.11}$$

and reaches $A_v \geq 870V/\,\mathrm{V}$ in the present case. A cascoded OTA architecture could then be considered to provide the necessary DC-gain [62].

#### Charge Transfer Duration

The time constant of the charge transfer between two SC cells, taking into account the finite OTA DC-gain and the switches' conductances, is calculated through (5.9) and yields

$$\tau = \frac{C}{g_m/2} \cdot \frac{1}{1+\frac{1}{A_v}} \cdot \left(1 + \frac{\delta_{sf}}{2A_v} + \left(1+\frac{1}{A_v}\right)\frac{\delta_{sc}}{2}\right) \tag{5.12}$$

$$\simeq \frac{C}{g_m/2} \cdot \left(1 - \frac{1}{A_v} + \frac{\delta_{sc}}{2}\right), \tag{5.13}$$

where the capacitor and feedback switches' conductance are defined as a function of a corresponding factor $\delta \ll 1$ and the OTA transconductance $g_m$, so that

$$\begin{cases} g_{sc} = \dfrac{g_m}{\delta_{sc}} \\ g_{sf} = \dfrac{g_m}{\delta_{sf}}. \end{cases} \tag{5.14}$$

The result in (5.13) shows that a sufficiently high gain and a low capacitor switch conductance ratio $\delta_{sc} \ll 1$ have only a negligible effect on the charge transfer. On the other hand, the impact of the feedback switch conductance is quasi-null and can be thus designed independently.

### 5.2.3 Switch Charge Injection and Clock Feedthrough

Non-ideal effects related to the clock feedthrough and the channel charge injection that occur during the MOSFET switches' transitions is evaluated through the sampling and holding phases illustrated in Fig. 5.6-(A-C). To perform a proper charge transfer, the capacitor switches toward the cell input and output, $\varphi_C$ and $\varphi'_C$ respectively, have to be driven by non-overlapping complementary phases, and the feedback switch $\varphi_f$ has to open before $\varphi_C$, as shown in the phases diagram in (C). Since the feedback switch opens first, and consequently isolates the capacitor's negative electrode, any other injected charges than those from $\varphi_f$ won't affect the charge balance. Therefore, only the feedback switch has to be designed in order to limit its charge injection.

As illustrated in (A), the charge injection, which occurs when $\varphi_f$ opens, can be equivalently represented by a charge source $\delta Q$ connected at the inverter input. Consequently, the capac-

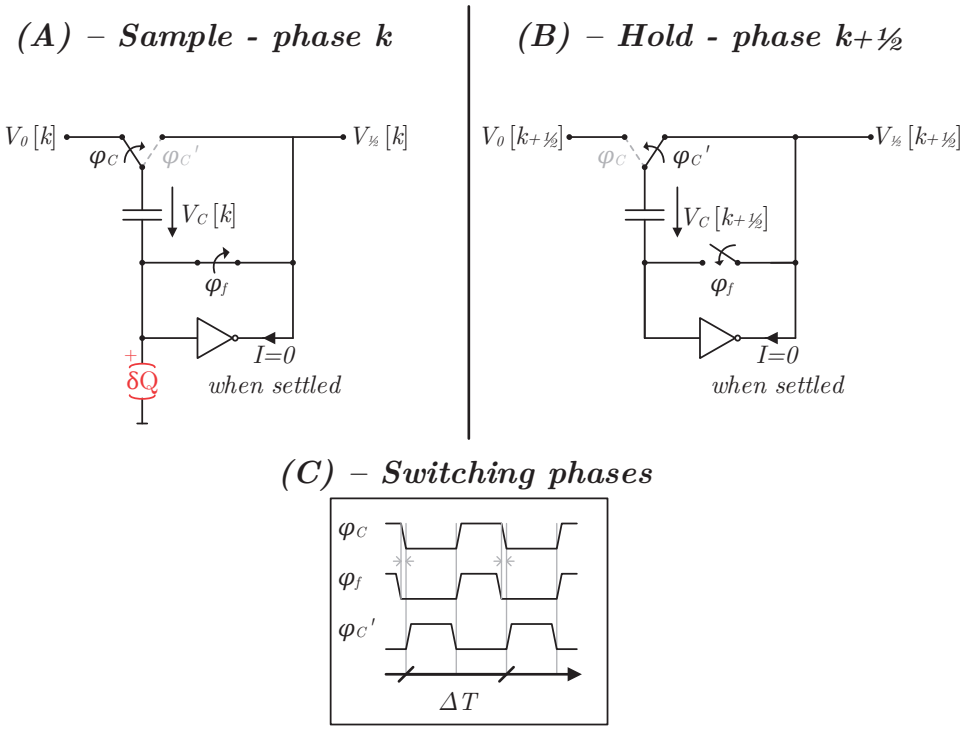


Figure 5.6: Sampling (A) and holding phases (B) of the half delay cell taking into account the injected charges $\delta Q$ and according switching diagram (C).

itor voltage $V_C$ during the sampling and holding phases can be written as a function of the input and output voltages, $V_0$ and $V_{1/2}$, respectively, so that

$$\begin{cases} V_C[k] &= V_0[k] - \dfrac{\delta Q}{C} \\ V_C[k+1/2] &= V_{1/2}[k+1/2]. \end{cases} \tag{5.15}$$

Since $V_C[k+1/2] = V_C[k]$, the equations in (5.15) combine, and thus,

$$V_{1/2}[k+1/2] = V_0[k] - \frac{\delta Q}{C} \tag{5.16}$$

These injected charges can be assimilated to an elementary cell offset that accumulates along the forward and backward propagation line paths illustrated in Fig. 5.1. The resulting offset at each $n^{th}$ line tap of the forward and backward propagation path, $V^{+}_{os_n}$ and $V^{-}_{os_n}$ respectively, is evaluated in Appendix E.1. Assuming that the input and fault reflection coefficients are of high

magnitude, so that $\rho \simeq \rho_L \simeq -\rho_r \simeq 1$, this equivalent offset calculated in (E.4)–(E.7) yields then

$$\begin{cases} V^+_{os_n} & \simeq & V_{os} \cdot \left( n'_f \cdot \dfrac{1-\rho}{2} + n \right) \\ V^-_{os_n} & \simeq & V_{os} \cdot \left( n'_f \cdot \dfrac{1-\rho}{2} - n \right), \end{cases} \tag{5.17}$$

where the cell offset is set by the injected charges, so that $V_{os} = -\delta Q/C$. Equations (5.17) show that both offsets have the highest amplitude at the last line tap, when $N = n = n'_f$, and reach approximately $V^+_{os_N} \simeq -V^-_{os_N} \simeq NV_{os}$. This systematic offset can be adequately removed by a calibration procedure to avoid errors during the evaluation of the fault current energy. However, care should be taken to maintain this offset below an admissible value to avoid any significant degradation of the dynamic range. It can be necessary to apply clock feedthrough reduction techniques ([58],[59],[60],[61]) to satisfy this criterion.

## 5.3 Speed, Consumption and Silicon Area

Using transconductors of $g_m = 500\,\mu$S each and capacitors of 1 pF, through (5.3), a clock frequency of 12.5 MHz can be considered, so that the emulated line propagation time scales by a factor $\kappa = 1/100$ referring to ~ 400 us in a typical 100 km power line. Consequently, the fault location process lasts about 200 ms for 1% resolution, making real-time implementation realistic.

The half delay cell consumption is dominated by the necessary biasing current to provide the desired amplifier transconductance. For CMOS transistors in weak inversion, offering the highest current efficiency ($g_m/I_d$), these currents can be evaluated as

$$I_Q \quad = \quad k\frac{g_m}{2} nU_T, \tag{5.18}$$

where $U_T$ is the thermal voltage and $n$ the slope factor. The integer $k \geq 1$ is set by the amplifier topology and is equal to one for a simple push-pull CMOS inverter. In the latter case, the minimum bias current is about $10\,\mu$A, or $20\,\mu$A for each elementary delay cell. A full 100-tap line, consisting of twice fifty delay elements for the forward and backward propagation paths, would therefore consume at least 2 mA, which is in the same order of magnitude as the gm-C line model.

The die area of a $N = 100$ taps line, consisting of $2N$ 1 pF capacitors and $500\,\mu$S transconductors, will not exceed a few square millimeters in a commercially available CMOS process with a typical specific MIM capacitance of $1-2$ nF/mm$^2$. This area takes into account the control logic and the additional switched-capacitor circuitry for the calculation of the fault current energy.

## 5.4 Conclusion

A switched-capacitor (SC) line emulation approach for the fault location method using the EMTR principle has been presented. The power line emulator based on a voltage-wave propagation topology includes many identical unit delay elements. This sampled data approach allows a simple and accurate control and scaling of the processing time by means of a single clock frequency. Analog delay elements implemented with switched-capacitor techniques are intrinsically insensitive to component mismatches and transconductor non-linearity, as opposed to the gm-C implementation presented in Chapter 4. While the gm-C solution would require a complex calibration process, the line delay in the SC approach is controlled only by the number of elements and the switching frequency, which make it therefore preferred for integration. The impact of non-ideal effects such as amplifier limited gain and speed, offsets, parasitic charge injection and finite conductance in switches, were discussed and related design constraints were derived. Analyses have shown that a fault location resolution and accuracy of typically 1% are achievable with standard performance fully-integrated components, while being typically 100 times faster than conventional numerical solvers. In integrated circuit form, the power consumption and silicon area of an emulated 100-tap line is conservatively estimated to $2-10$ mA and $1-2$ mm$^2$, and would typically allow a fault location within a few hundred milliseconds. This significant speed improvement makes real-time fault management possible.

# 6 Switched-Capacitor Line Circuit Design

This chapter presents the transistor level design and practical aspects of the switched-capacitor line model silicon implementation. As studied in previous chapters, the switched-capacitor line is by construction more robust and less sensitive to non-ideal effects associated to micro-electronic implementation than the gm-C model, and is therefore preferred for integration. The circuit is implemented in an AMS 0.35 µm CMOS process, well known in the laboratory and presenting good characteristics for analog circuits for a reasonable per silicon area price. Moreover, this technology provides a sufficient voltage supply ($V_{dd}$ = 3.3 V) that allows cascoded transistor topologies. As a first part of the design, an elementary switched-capacitor cell that combines all the functions, from the simple delay to the boundary and fault cells, is presented. It is shown how this block can be combined to constitute the full line according to its configuration. Within this block, the OTA transistor level architecture and its biasing circuit are presented, and corresponding characteristics, such as its transconductance, dynamic, current consumption, are deduced by simulation. The switched-capacitor elementary cell equivalent losses, offset and speed constraints are also determined through transient simulations of the circuit. Finally, the architecture of the energy measurement circuit that computes the fault current energy is also presented.

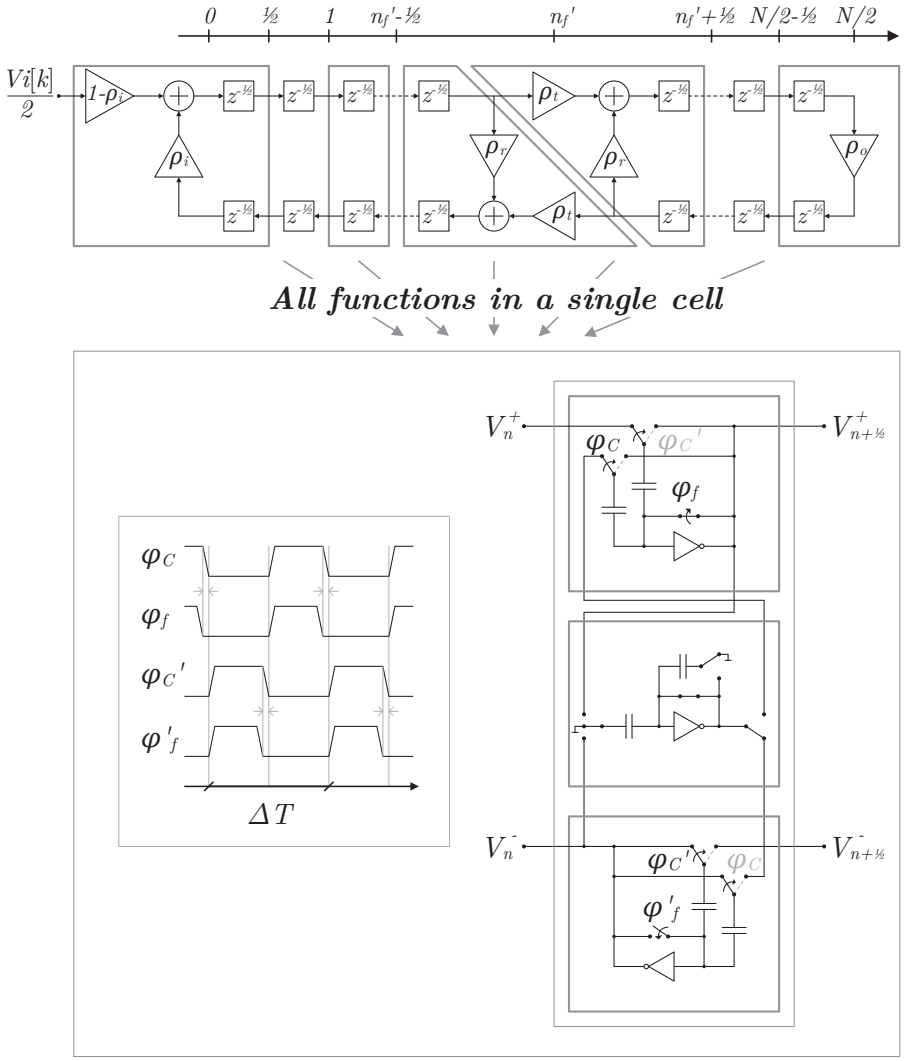


Figure 6.1: Discrete-time transmission line model realized with a combination of the elementary switched-capacitor cell.

## 6.1 Elementary Delay Cell

The discrete-time line model is made up of interconnected elementary cells that combine the functions of the simple delay in Fig. 5.2 and the boundary cells at the line input, output and at the fault location in Fig. 5.3. The line to be implemented and the all in one bidirectional delay realized with switched-capacitor circuits are illustrated in Fig. 6.1. The cell is composed of a forward and backward propagation delay and a switched-capacitor inverter necessary to simulate a fault occurrence.

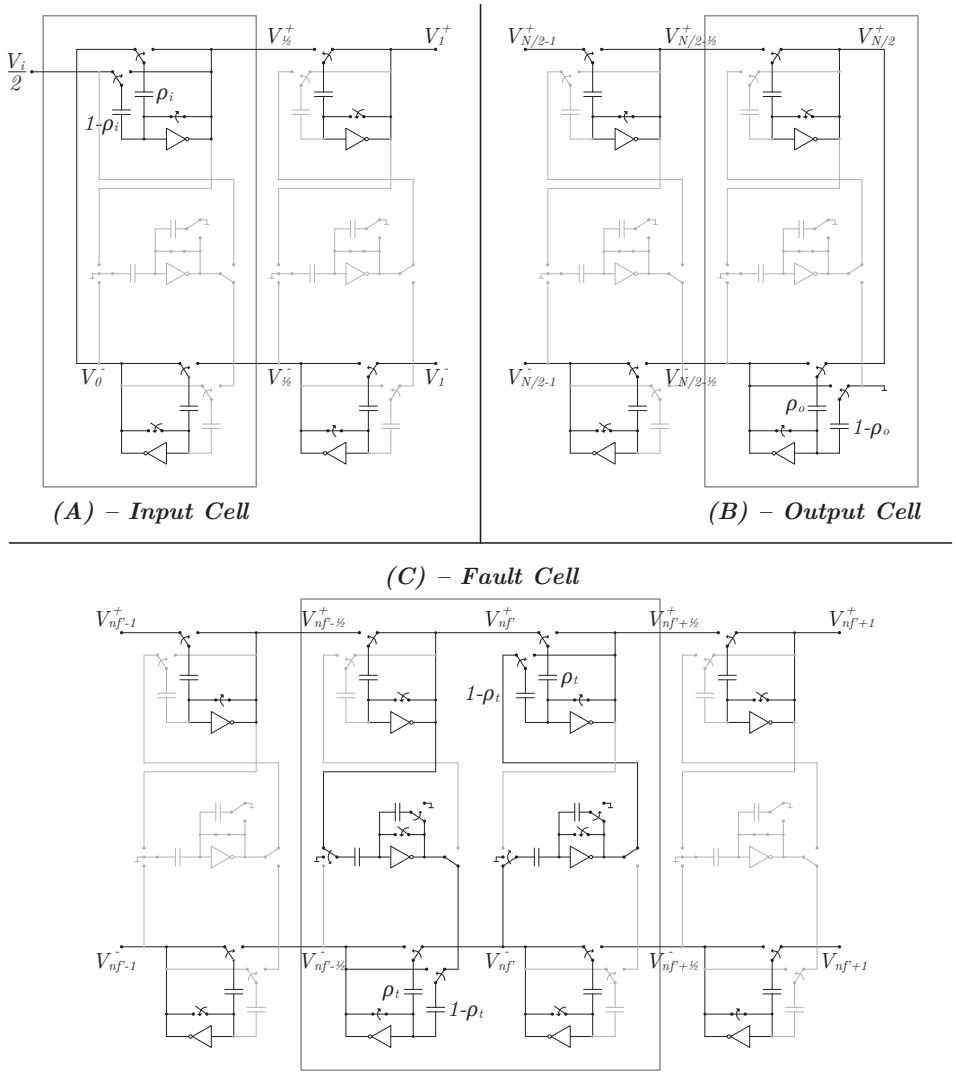


Figure 6.2: Input (A), output (B) and fault (C) configuration of the elementary switched-capacitor elementary cell.

### 6.1.1 Switch Phases

As displayed in the schematic in Fig. 6.1, the forward propagation path capacitor switch is cadenced by two complementary non-overlapping phases, $\varphi_C$ and $\varphi'_C$, that control the switch branch toward the $n$ and $n+1/2$ cells respectively. In the opposite way, the capacitor switch phases of the backward propagation cell are simply permuted. To achieve a proper charge transfer, the feedback switch of the corresponding forward and backward propagation paths, $\varphi_f$ and $\varphi'_f$ respectively, has to be closed before the capacitor phase, $\varphi_C$ and respectively $\varphi'_C$, as illustrated in the chronogram. The switching phases are generated locally in each elementary cell according to a general digital clock *DCLK*, common for the whole chip. This distributed phase generation allows a better control of their timing that avoids any overlapping, which is of prime importance for SC circuits. However, particular attention has to be paid to the

general clock distribution, which should avoid any propagation delay between two adjacent elementary cells. Following cells should be disposed sufficiently close to each other on the layout so that the delay between their two corresponding clocks is minimized.

### 6.1.2 Elementary Cell Configurations

The elementary cell can be configured as a simple delay cell, or as an input, output or fault cell according to associated digital flags. The different configurations are displayed in Fig. 6.2-(A-C). In (A), the first cell is configured as a line input cell that sums the backward propagated wave with the half of the input signal, weighted by the input reflection coefficient $\rho_i$ and its complement to one. In this case, the inverter block in the middle is simply deactivated. The line output termination is represented in (B), where the forward propagated wave is reflected in the opposite direction and weighted by the output reflection coefficient $\rho_o$. In this case, the inverted block is also deactivated. The fault (C) is realized with two elementary cells with activated inverters, which control the propagated wave fraction that is reflected or transmitted to the following line section, according to the fault transmission coefficient $\rho_t$.

## 6.2 Operational Transconductance Amplifier Design

According to the analysis made in Chapter 5, the cell OTA should provide at least a transconductance of $g_m \geq 500\,\mu$S and a DC gain of $A_v \geq 870$, to satisfy the circuit minimum processing speed and maximum losses expectations. An AB-class cascode architecture is selected [62], as it can provide a sufficient DC gain with a convenient output voltage range ($1-2$ V), assuming a $V_{dd} = 3.3$ V voltage supply in the implemented AMS $0.35\,\mu$m C35B4C3 process. Moreover, the third order transfer characteristic of the AB-class topology ensures an optimal behaviour for large signals as well as for small ones and avoids any slew-rate limitation. The non-linearity and uncontrolled offset, inherent to this architecture, can be simply ignored as they have no impact on the fault location process, as demonstrated previously. The OTA simplified transistor level schematic is illustrated in Fig. 6.3.

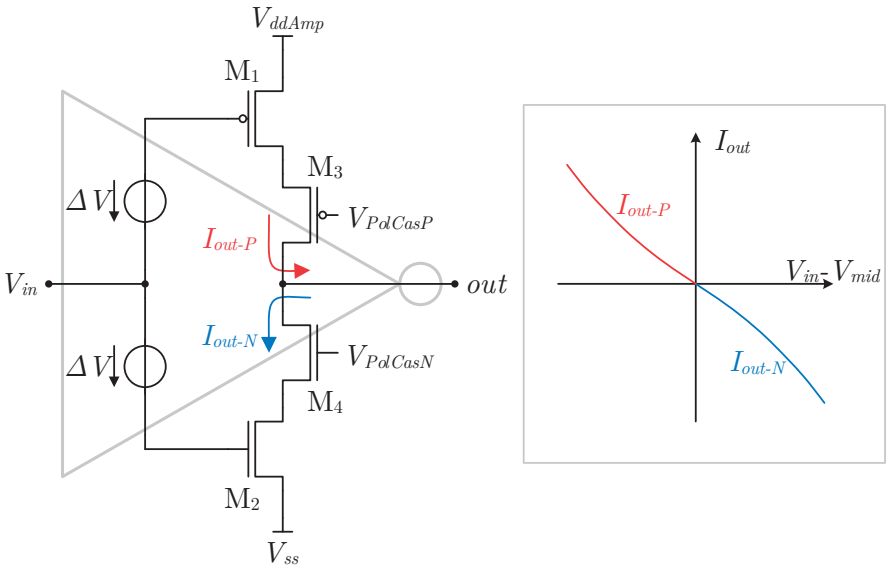


Figure 6.3: Transistor level of the AB-class cascode OTA and its third order transfer characteristic.

### 6.2.1 Transistor Sizing

According to [62], the AB-class amplifier small signal transconductance is equal to the sum of those of transistors $M_{1-2}$. Considering the MOS pair of same $g_{m_{1-2}}$, the total amplifier transconductance can be written as $g_m = 2g_{m_{1-2}}$. On the other hand, the amplifier voltage gain $A_v$ depends on the ratio between $g_m$ and the output conductance $g_o$, so that

$$A_v = \frac{g_m}{g_o} \simeq \underbrace{\frac{g_{m_{1-2}}}{g_{ds_{1-2}}}}_{A_{v_{1-2}}} \cdot \underbrace{\frac{g_{m_{3-4}}}{g_{ds_{3-4}}}}_{A_{v_{3-4}}}, \tag{6.1}$$

considering the transconductances $g_m$ and drain-to-source conductances $g_{ds}$ as equal for each transistor pair $M_{1-2}$ and $M_{3-4}$. This result is equivalent to the multiplication of each transistor pair intrinsic gain $A_{v_n}$. The design goal is to maximize the OTA transconductance and DC gain while maintaining a reasonable output voltage dynamic, which is set by the MOS saturation voltages. Increasing the quiescent current $I_d$ increases the transconductance from a proportional factor to a square root factor, depending on the transistor inversion coefficient [64]. This current is directly controlled by the gate-to-source voltage of transistors $M_{1-2}$ set by $\Delta V$. However, a current increase will decrease the output dynamic and the gain by increasing proportionally the drain-to-source conductances given by

$$g_{ds} \simeq \frac{I_d}{U_a L}, \tag{6.2}$$

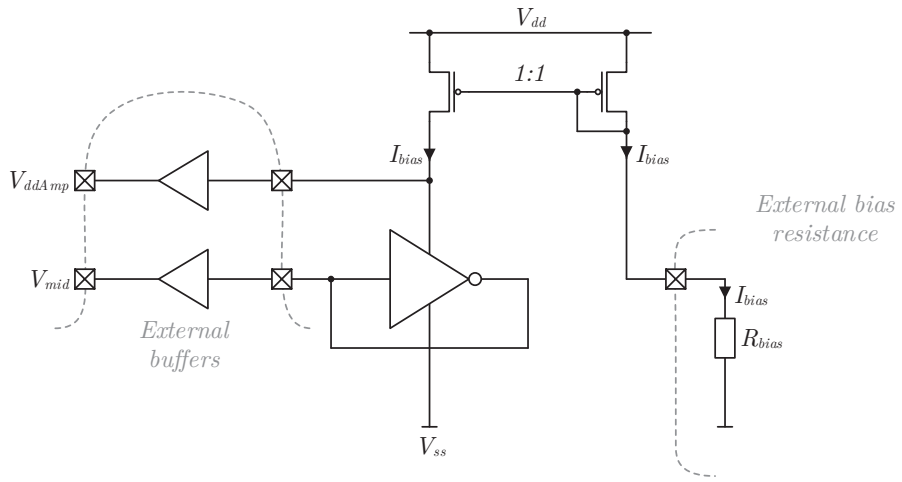


Figure 6.4: OTA biasing circuit.

where $U_a$ is the Early voltage and $L$ the transistor length. The optimal configuration is reached when the MOS transistors are in moderate inversion, providing thus a good compromise between the transconductance and DC gain. The $\Delta V$ voltage shift at the amplifier input is necessary to increase the output dynamic. However, this value should be properly set so that transistors' $M_{1-2}$ gate-to-source voltage can at least reach their corresponding threshold voltage $V_{T0}$ to ensure their conduction. Hence,

$$V_{ddAmp} \geq V_{T0_P} + 2\Delta V + V_{T0_N}, \tag{6.3}$$

where the OTA supply voltage is limited by $V_{ddAmp} < V_{dd}$, and $V_{T0_N} \simeq 0.48$ V and $V_{T0_P} \simeq 0.68$ V. The voltage shift $\Delta V$ is realized with voltage follower MOS transistors. A more detailed OTA MOS transistor schematic with dimensions is presented in Appendix F.1. After layout, the implemented OTA takes the area of a rectangle of $50 \times 90\,\mu\text{m}^2$.

### 6.2.2 Biasing Circuitry

The OTA positive supply $V_{ddAmp}$, the midrange voltage reference $V_{mid}$, the current mirrors and cascode transistor bias voltages are generated by a biasing circuit common for all the on-chip OTA. A simplified version of this circuit is illustrated in Fig. 6.4. The voltage supply $V_{ddAmp}$ settles naturally after imposing the current of an OTA at equilibrium, with shorted input and output. This voltage is buffered off-chip and is used as a general OTA supply for the whole circuit. Similarly, the midrange voltage $V_{mid}$ is also buffered and used as a general midrange voltage reference. The mirrored OTA bias current $I_{bias}$ is fixed by a corresponding off-chip resistor $R_{bias}$ and can be adjusted accordingly. As stated in Section 6.2.1, this bias current is a direct control over the OTA transconductance and can be adjusted in consequence. A more detailed OTA biasing circuit is presented in Appendix F.2.

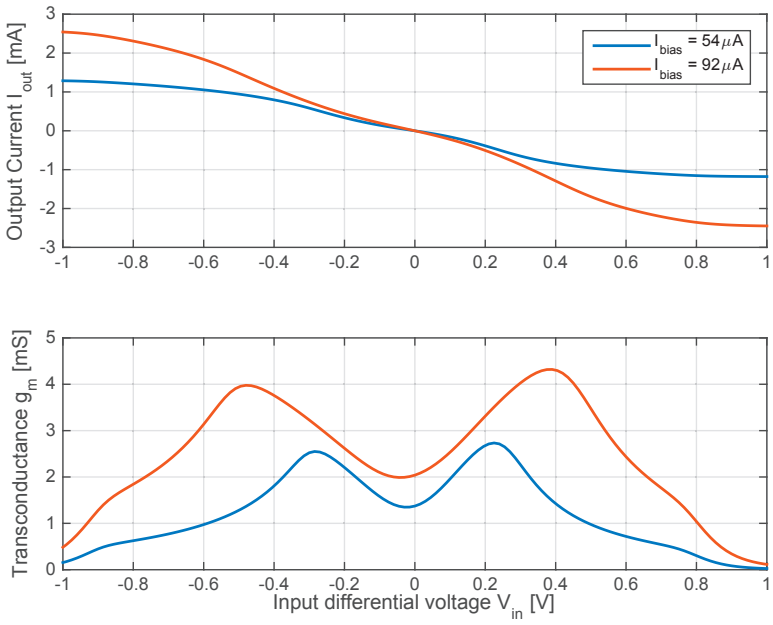


Figure 6.5: OTA output current (up) and transconductance (down) for two different bias currents.

### 6.2.3 Simulation Results

As shown in Appendix F.3, DC simulations of the OTA and its biasing circuit, with a bias current of $I_{bias} = 54\,\mu$A, provide an OTA supply voltage of $V_{ddAmp} = 2.99$ V and a voltage reference close to midrange, at $V_{mid} = 1.36$ V, as expected.

The OTA output current $I_{out}$ and transconductance $g_m$, as a function of the input voltage, are illustrated in the DC-sweep simulation plots in Fig. 6.5. The simulation is realized for OTA bias currents set to $I_{bias} = \{54\,\mu\text{A};\ 92\ \mu\text{A}\}$, which corresponds to off-chip normalized resistors $R_{bias} = \{47\ \text{k}\Omega;\ 27\,\text{k}\Omega\}$, respectively. As expected, the third order output current characteristic of the AB-class topology increases the large signal transconductance until it reaches saturation. Globally, the transconductance increases with the OTA bias current. The minimum transconductance is reached at approximately $V_{in} \simeq V_{mid}$ (and not exactly, due to the N and PMOS asymmetries) and is $g_{m_0} = \{1.35\,\text{mS};\ 2\ \text{mS}\}$, depending on the corresponding bias current. Both transconductances are more than sufficient, considering the minimum expected of $500\,\mu$S. The input dynamic can be defined as the voltage range for which the transconductance exceeds $g_{m_0} - 10\%$. These values reach $\Delta V_{in} = \{1.5\ \text{V};\ 1.8\ \text{V}\}$, depending on the simulation case.

The OTA output resistance $1/g_o$ as a function of the output voltage is illustrated by the DC-sweep simulation plot in Fig. 6.6, with the same biasing conditions. As expected, a current increase obviously decreases the output resistance and the output dynamic. When the output

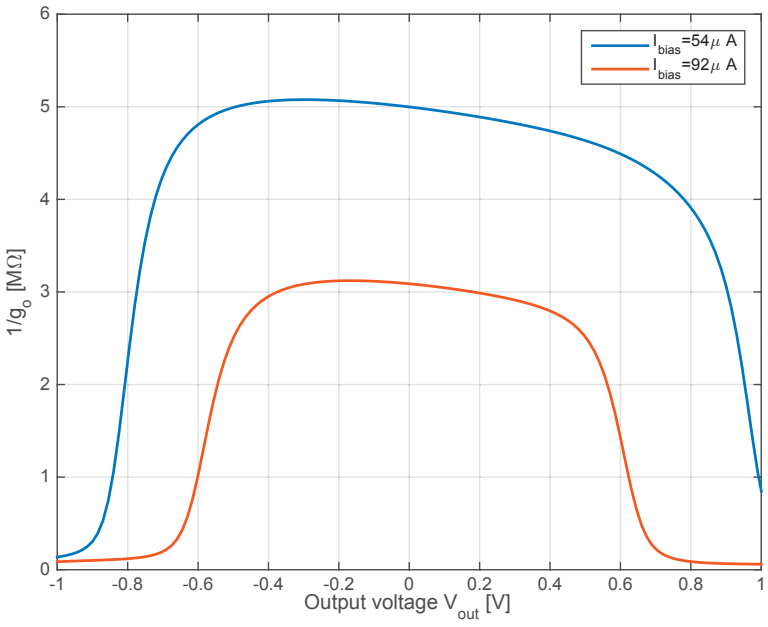


Figure 6.6: OTA inverted output conductance for two different bias currents.

voltage is at midrange, the output resistance reaches $1/g_{o_0} \simeq \{5\ \text{M}\Omega; 3.1\ \text{M}\Omega\}$ for respective bias currents. Consequently, and according to the result in Fig. 6.5, the OTA gain at input and output midrange voltage can be respectively estimated to $A_{v_0} = g_{m_0}/g_{o_0} = \{6750; 6150\}$, which is more than enough, considering the minimum expected gain of $870\,V/\,\text{V}$. The gain difference between the two simulations occurs as $g_m$ increases slower than $g_o$, according to the current $I_{bias}$. The output dynamic can be defined as the output voltage range for which the output resistance exceeds $1/g_{o_0} - 10\%$. These values reach $\Delta V_{out} = \{1.3\ \text{V}; 0.9\ \text{V}\}$, referring to the respective simulation case, and correspond to the expected range considering a cascoded topology.

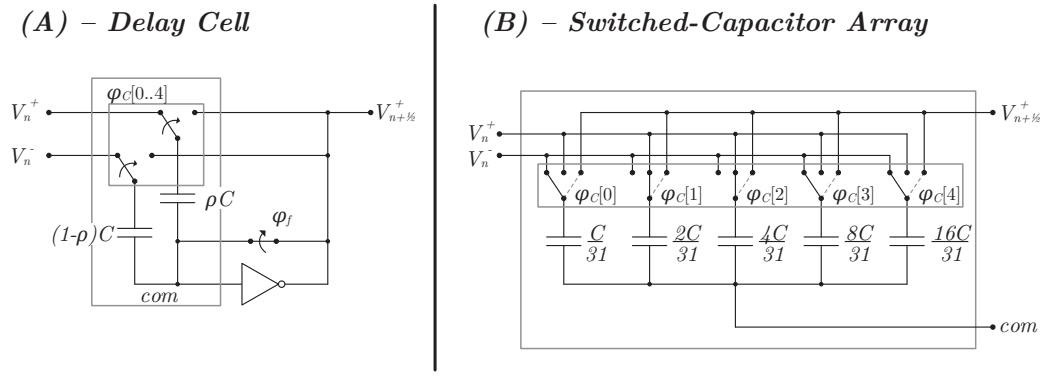


Figure 6.7: Delay cell (A) and equivalent switched-capacitor array implementation (B).

## 6.3 Switched-Capacitor Array

This section discusses the practical aspects of the switches and capacitor implementations in the elementary delay cell. As displayed in Fig. 6.7-(A), the sum weighted by the reflection or transmission coefficients $\rho \in [0;1]$ and its complement to one, is realized through switched-capacitors of proportional value. This capacitor repartition can be set according to a switched-capacitor array (B) of length $N_b$, where each tap can be switched toward the forward or backward propagated signal input, $V_n^+$ and $V_n^-$ respectively. The array is composed of capacitor fractions $C/(2^{N_b}-1)$ increasing by the power of 2 between successive positions. In the present case, the capacitor array can be set with a $N_b = 5$-bit resolution, allowing a sufficiently fine adjustment of the corresponding reflection and transmission coefficients. The full array, composed of 31 square shaped capacitors $C/31$ of cumulative value set to $C = 1$ pF, is implemented in Poly1-Insulator-Poly2 capacitors (PIP) of 0.86 nF/mm$^2$ specific capacitance and takes a total area of $31 \times 64\,\mu$m$^2$. The PIP capacitor module is selected since it is less dependent to the voltage variations than the MOS capacitors, and is one of the two capacitor modules available in the used AMS 0.35µm C35B4C3 process.

### 6.3.1 Capacitor Switches

For a proper charge transfer, the total switch on-conductance $g_{sc}$ should be distributed over the $N_b$ array positions proportionally to the corresponding capacitor values. Consequently, each $n^{th}$ array branch constituted of a capacitor of $2^nC/31$ and a switch of conductance $2^n g_{sc}/31$ has the same time constant $\tau = C/g_{sc}$. As stated in Chapter 5, the total switch capacitor on-conductance $g_{sc}$ should be much higher than the OTA transconductance $g_m$, so that it doesn't impact the charge transfer. In the present case, this value reaches $g_{sc} = 6.5$ mS, which satisfies this criterion since previous simulations gave $g_m \leq 2$ mS. The total CMOS switch array silicon area is a rectangle of $65 \times 75\,\mu$m$^2$.

### 6.3.2 Feedback Switch

As discussed in Section 5.2, the feedback switch has to be designed in order to minimize its parasitic charges injected into the capacitor when the switch closes. This non-ideal effect translates to an equivalent cell offset that accumulates over the line. Although this offset can be simply compensated by calibration during the fault current energy evaluation, it should remain below an acceptable level to avoid significant degradation of the linear range. The equivalent cell offset can be quantified through the evaluation of the charges present in the N and PMOS channels of the considered CMOS switch before it opens. According to [59], these channel charges are given by

$$\begin{cases} Q_N &= -W_N L_N C_{ox} \left( V_{gs_N} - V_{T_N} \right) \\ Q_P &= W_P L_P C_{ox} \left( V_{gs_P} - V_{T_P} \right), \end{cases} \tag{6.4}$$

where $W_{N-P}$ and $L_{N-P}$ are the width and respectively length, $V_{gs_{N-P}}$ the gate-to-source voltage and $V_{T_{N-P}} = \{0.8\text{ V};\ 1\text{ V}\}$ the threshold voltage simulated in the present conditions, at $V_s = V_{mid} = 1.36$ V, for the corresponding N or PMOS transistors. According to the impedance on both switch sides, the clock sharpness and the synchronisation between the CMOS complementary phases, the channel charges splits from either switch sides when it opens. In the present case, due to the time delay of the inverter necessary to generate the complementary NMOS phase, the PMOS switch opens slightly before the NMOS. Consequently, the NMOS transistor is still closed when the PMOS opens, so that the PMOS charges are absorbed and doesn't influence the process in first approximation. Therefore, only the NMOS channel charges impact the capacitor $C$ charge balance. The equivalent cell offset is then given by

$$V_{os} = \frac{\alpha Q_N}{C}, \tag{6.5}$$

where $\alpha \in [0;1]$ is the charges partition between each switch sides. According to (6.4) and (6.5), it can be seen that the injected charges, and hence the equivalent offset, are minimized when the transistors area $WL$ is a minimum. Moreover, since the finite conductance of the feedback switch doesn't influence the duration of the charge transfer, it can be sized independently with a minimum transistor width. Consequently the NMOS dimensions are set to $W_N|L_N = 0.5|0.35\,\mu$m and those of the PMOS to $W_P|L_P = 2|0.35\,\mu$m, so four times wider to ensure a proper conductance symmetry. With an oxide capacitance per unit area of $C_{ox} = 4.66\,fF/\mu m^2$, a gate-to-source voltage of $V_{gs_N} = V_{dd} - V_{mid} = 1.94$ V and considering that the channel charges of the NMOS channel split equivalently on both transistor sides, so that $\alpha = 0.5$, the equivalent cell offset in (6.5) with (6.4) is evaluated to $V_{os} = -670\,\mu$V, which is close to the transient simulated values of $V_{os} = -750\,\mu$V. As stated in Section 5.2.3, this offset accumulates along the line and is maximum at its end and for faults situated at the last tap. In this case, it is estimated at $NV_{os} = -75$ mV, considering a line of $N = 100$ elements. According

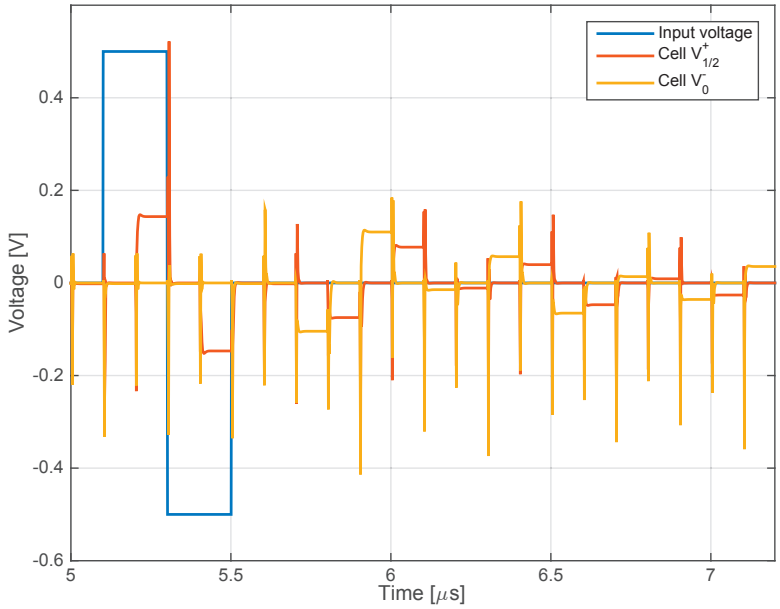


Figure 6.8: Alternated impulse response of the switched-capacitor line of $N = 4$ elementary cells, with a fault at $n_f = 3$.

to the OTA simulation results in Section 6.2.3, this accumulated offset remains below 10% of the linear range, and is thus acceptable.

## 6.4 Switched-Capacitor Line Transient Simulations

A switched-capacitor line, composed of $N = 4$ elementary cells with a guessed fault at tap $n'_f = 3$, is validated through transient simulations. Alternate positive and negative impulses are applied at the line input and the corresponding responses are observed at the first forward propagation path cell output $V^+_{1/2}$ and at the last backward propagation path cell output $V^-_0$, as illustrated in Fig. 6.8. The line is configured with input, output and fault reflection coefficients of $\rho_i = \rho_o = -\rho_r = 22/31 = 0.7097$ and a clock frequency set to 5 MHz. For both observation points, the simulation plot shows the propagation and fading of the impulses according to the reflection coefficients. It can be seen that the reflection coefficients are properly implemented with a negligible relative error of ±0.5%. Losses of $\alpha_{dB} \simeq \{0.00273\text{ dB};\ 0.00266\text{ dB}\}$ can be observed between successive line elements for positive and negative impulses respectively, which extrapolated to a line of $N = 100$ cells reach about 0.27 dB, which is greatly below the maximum tolerated losses 1 dB.

The signal settling time is evaluated for small and large signals on the zoomed plot of the forward propagation path first cell output $V^+_{1/2}$, illustrated in Fig. 6.9. The small signal impulse response presents a bigger overshoot and settles more slowly than the large signal response

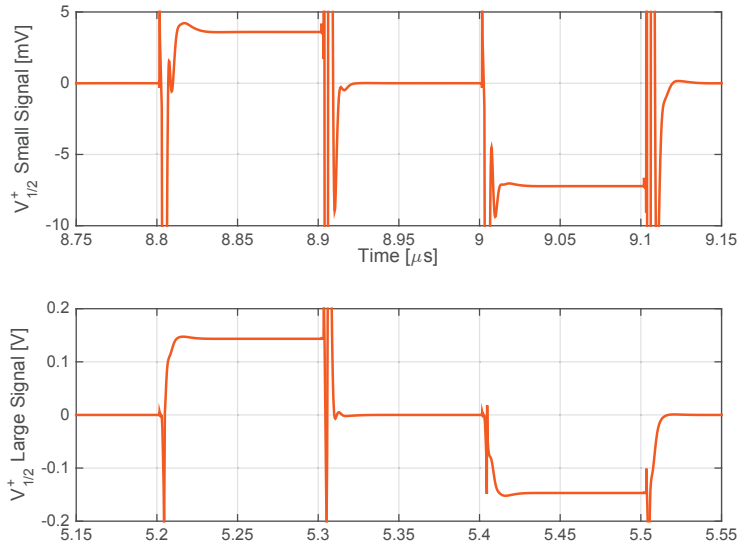


Figure 6.9: Forward propagating path first cell output voltage $V^+_{1/2}$ small and large signal impulse response.

due to the lower transconductance in this range. The signal $5\tau$ settling time is evaluated at $T_{set} \simeq \{32\text{ ns};\ 24\text{ ns}\}$ for small, respectively large, signal simulations. These results allow a maximum processing speed of $f_{max} = 1/2T_{set} \simeq \{15.6\text{ MHz};\ 20.8\text{ MHz}\}$, respectively, for the two cases. In both situations, the simulated maximum frequency is above the minimum expected 12.5 MHz.

## 6.5 Energy Measurement Circuit

The fault current energy measurement circuit is equivalently replaced by a measure of the line input voltage energy. Simulations showed that both signals are proportional, so would provide similar fault location properties. The line input voltage measurement is preferred to the fault current one, since the corresponding circuit is only connected at the line input and doesn't need to be switched all along the line, as the guessed fault moves, during the process. The voltage energy is computed through the circuit shown in Fig. 6.10. The square value of the sampled input voltage $V_C$ is contained in the current $I$, derived from the quadratic transfer characteristic of a MOS transistor in strong inversion. The biasing current $I_T$, much lower than $I$, is set to pre-bias the MOS around the threshold voltage $V_T$, where its transfer characteristic is quadratic. The current $I$ is then integrated in a capacitor external to the chip and gives a proportional voltage $V_{int}$. The presented circuit computes the energy of positive signal phases, its complementary circuit has to be designed to compute the negative ones. The signal offset propagating along the line is compensated by the externally adjustable bias voltage $V_{os-comp}$ calibrated in advance.

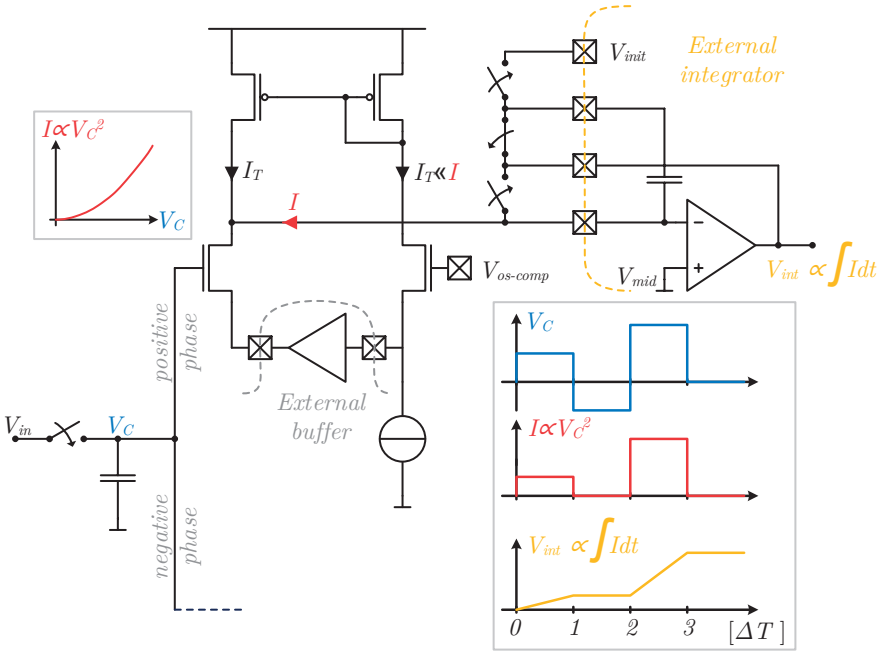


Figure 6.10: Transistor-level schematic of the fault current energy measurement circuit.

The energy measurement circuit has been simulated with alternate decreasing impulses applied at the circuit input $V_C$. As displayed in Fig. 6.11, each complementary part of the circuit computes an image of the integral of the square of positive and respectively negative input signal phases. It can be seen that the positive part is only slightly influenced by the negative signal phases, and conversely. Although this dependence can be reduced through the bias voltage $V_{os-comp}$, it cannot be totally cancelled. The total integral $V_{int}$ is obtained by the difference between both positive and negative circuit results. Extensive simulations have shown that the accuracy of the signal energy calculation has a negligible impact on the fault location precision. Although the signal energy presents probably the best results in terms of discrimination of the fault location maximum, it could be replaced, for instance, by the integration of the signal rectified value, without any significant loss of accuracy. In the present case, simulations have shown that the implemented energy measurement circuit, displayed in Fig. 6.10, allows a proper fault location within the expected percent resolution, and is therefore adapted to the method.

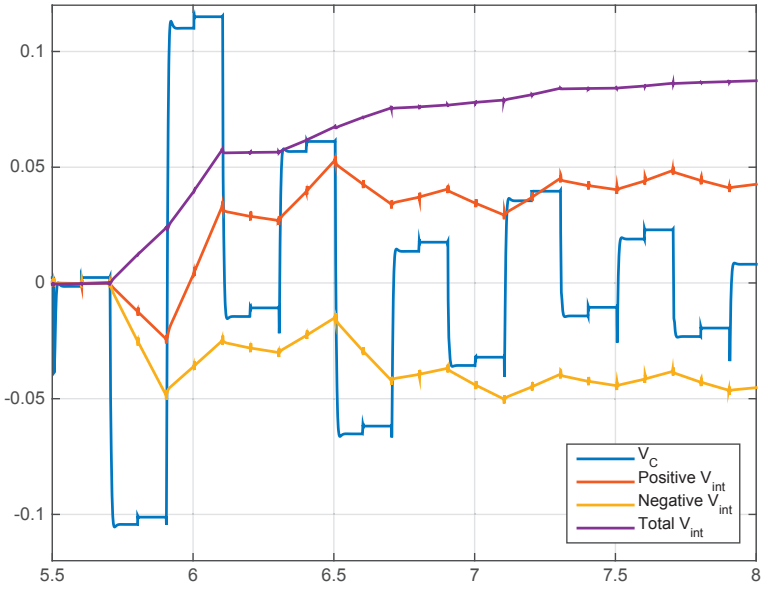


Figure 6.11: Energy measurement circuit transient simulation.

## 6.6 Discrete-Time Line Implementation, Circuit Area and Current Consumption

The switched-capacitor line model is implemented in an integrated circuit designed in the AMS 0.35 $\mu$m CMOS C35B4C3 process. For layout shaping reasons, the full line is composed of $N = 96$ elementary delay cells instead of one-hundred, which slightly reduces the expected percent fault location resolution to $r = 1/N = 1.042\%$. On silicon, each elementary delay cell covers a rectangle of $310 \times 195\,\mu\text{m}^2$ and the total circuit, composed of $N = 96$ cells, the energy measurement circuit and clock buffering logic, takes about $3 \times 3$ mm$^2$, excluding the pad ring. The picture of the full integrated circuit is illustrated by the photo in Fig. 6.12.

The line static consumption is proportional to the OTA static current $I_{bias}$, set off-chip by the bias resistor. Considering a full line of $N = 96$ elementary cells, including $2N + 2$ OTAs for the forward and reverse propagation paths, plus two SC inverter circuits for the fault simulation, and the OTA bias circuit that consumes $6I_{bias}$ (Appendix F.2), the total static current consumption can be extrapolated to $(2N + 8)I_{bias}$, and hence $200I_{bias} = 10.8$ mA, with $I_{bias} = 54\,\mu$A.

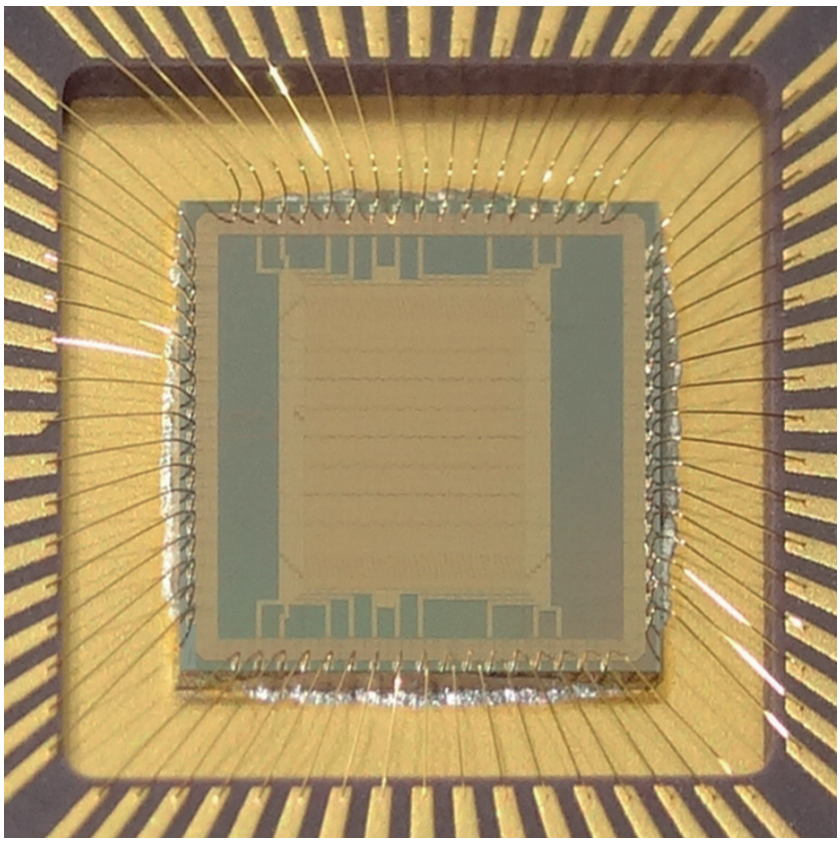

Figure 6.12: Integrated-circuit implementation of the switched-capacitor line. The circuit is implemented in an AMS 0.35 $\mu$m CMOS process and measures 9 mm$^2$ excluding the pad-ring.

## 6.7 Conclusion

This chapter has presented the last steps of the switched-capacitor line model development before silicon implementation in an AMS 0.35 $\mu$m CMOS process. The switched-capacitor bidirectional delay, the elementary cell of the discrete-time line to be implemented, was introduced. Within this circuit, a transistor level architecture of the OTA was selected and adequately sized to meet the transconductance, DC-gain and dynamic expectations established in the previous chapter. A corresponding biasing circuit that allows a control of the OTA static current, and consequently transconductance, by means of an off-chip resistor, was also implemented. The CMOS switches were designed according to the minimum conductance and maximum charge injection constraints discussed in the previous chapter. Finally, the working principle and topology of the circuit that measures the fault signal energy was also introduced. Global simulations showed that the circuit expectations have been met in general, allowing thus its safe implementation in silicon. After layout, the full chip, excluding the pad ring, covers a squared area of $3 \times 3$ mm$^2$, for a static current consumption extrapolated to 10.8mA.

# 7 Measurements

This chapter presents the measurement results and characterizations of the switched-capacitor line chip. The Application Specific Integrated-Circuit (ASIC) is evaluated through a micro-controller-based test bench that allows to back-propagate successively the time-reversed fault signature in the implemented line, for different guessed fault locations. The fault location process results are then redirected to a computer and displayed in Matlab. Over this interface, the integrated-circuit speed and accuracy are evaluated in the frame of the fault location, with different circuit configurations, bias currents and switching frequencies. The fault location precision, mainly limited by the line parasitic losses, is also characterized according to various bias and frequency configurations. Finally, the static current consumption, dominated by the transconductance amplifiers bias current, and the dynamic current, associated to the switching circuitry, are also measured and compared to the expected values.

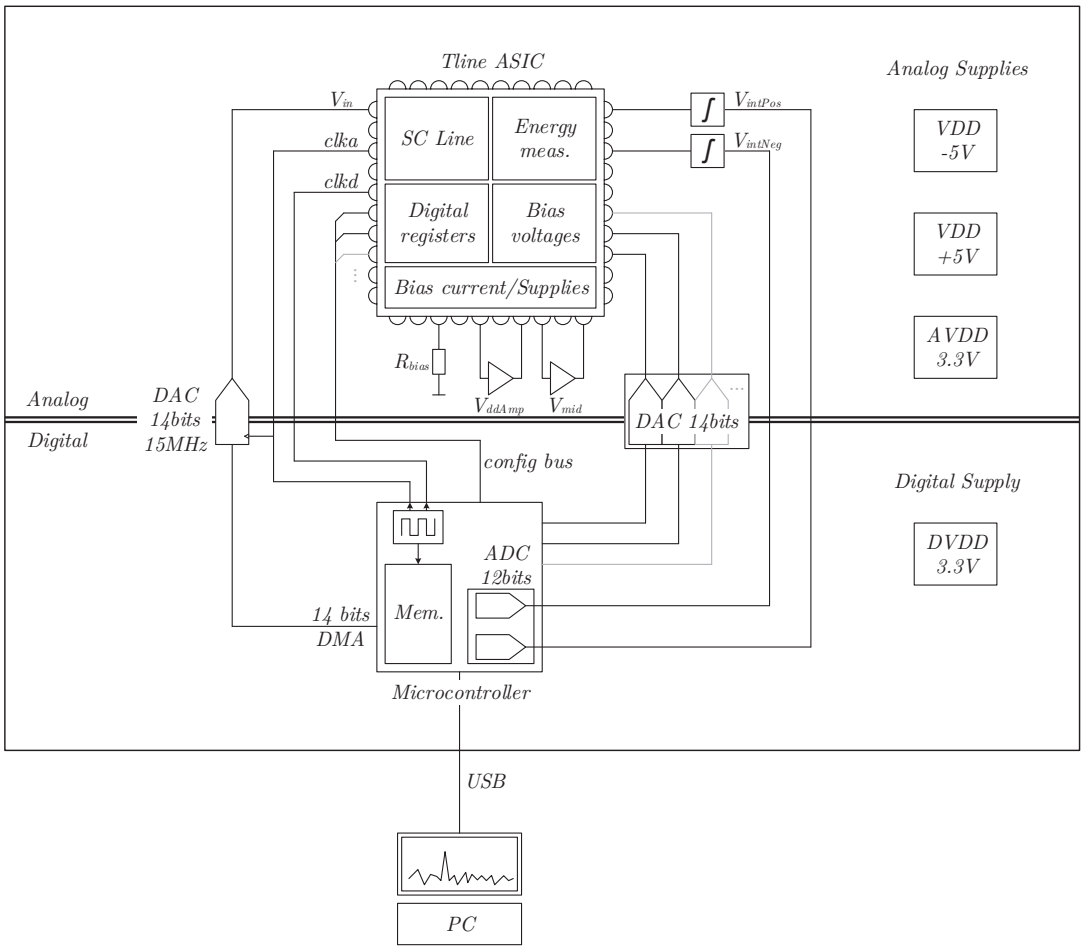


Figure 7.1: Test bench block diagram.

## 7.1 Test Bench

The switched-capacitor line ASIC is evaluated on the Printed Circuit Board (PCB) test bench described by the block diagram in Fig. 7.1. The circuit configuration, analog signal generation and measurement and computer USB interfacing is realized through the STM32F405 32 bit/168 MHz Microcontroller Unit (MCU). The microcontroller operates the back-propagation of the time-reversed fault signature, previously transferred from computer to local memory, into the ASIC through a 14 bit Digital-to-Analog Converter (DAC). The 14 bit data bus interfacing the MCU memory with the DAC is realized with the Direct Memory Access (DMA) protocol, in order to provide a sufficient transfer speed to reach the expected sampling frequency of $f_s$ = 15 MHz. The DAC and the ASIC switched-capacitors are cadenced by the analog clock *clka* generated by the microcontroller crystal oscillator. Before the back-propagation of the fault signature, the guessed fault tap and the line reflection coefficients are configured by the MCU through the *config* bus, synchronized by the digital clock *clkd*, set up to 50 MHz. The guessed fault signal energy is obtained after each back-propagation phase at the output of the

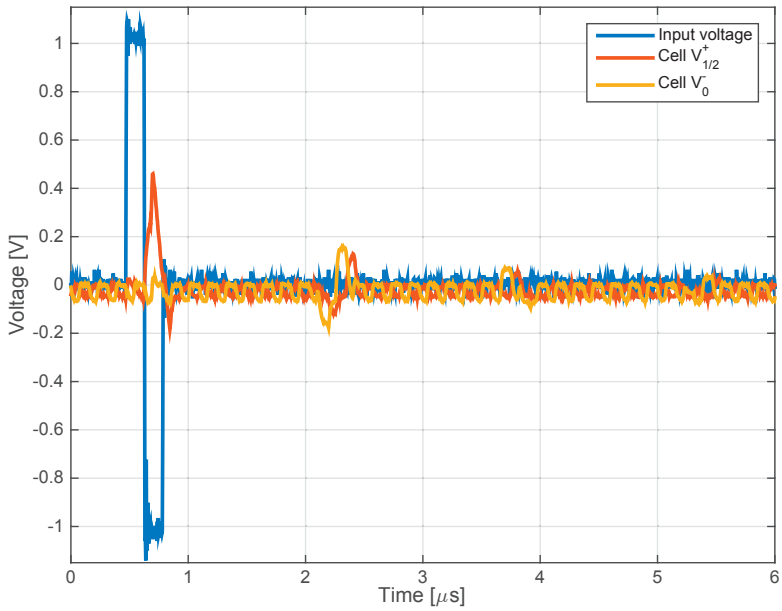


Figure 7.2: Impulse response of the switched-capacitor line with a fault at tap $n'_f = 10$.

positive and negative off-chip integrator blocks. Both signals are then digitized in the MCU internal 12 bit Analog-to-Digital Converters (ADC), their difference is transferred to the PC and displayed in the Matlab interface for the $N$ guessed fault cases.

The PCB is supplied by separated analog and digital voltage sources and grounds to minimize the analog signals perturbations caused by digital switching. Consequently, the PCB analog part is powered by voltage regulators of $AVDD = 3.3$ V, principally aimed at the ASIC, and ±5 V for additional buffers, operational amplifiers and for the analog supply of AD/DA converters. On the other hand, the digital part is supplied by $DVDD = 3.3$ V used for the microcontroller, the USB interface and the digital supply of AD/DA converters. The buffering of the OTA supply $V_{ddAmp}$ and the midrange voltage reference $V_{mid}$ is realized off-chip, as is the case for the adjustment of the bias current through the resistor $R_{bias}$. Additional 14 bit digital-to-analog converters are also used to set up the energy measurement circuit and its offset compensation.

## 7.2 Transient Analysis

The switched-capacitor line is evaluated through its impulse response observed at the forward propagation path first cell output $V^+_{1/2}$ and at the backward path last cell output $V^-_0$. To avoid any perturbations caused by the signal probing, each observed nodes are copied to corresponding ASIC output pads by source-follower MOS transistors. Similarly to the transient simulations in Section 6.4, positive and negative impulses are applied at the line input, with a guessed fault at tap $n'_f = 10$ and reflection coefficients set to $\rho_i = \rho_o = -\rho_r = 22/31$. As displayed in Fig. 7.2,

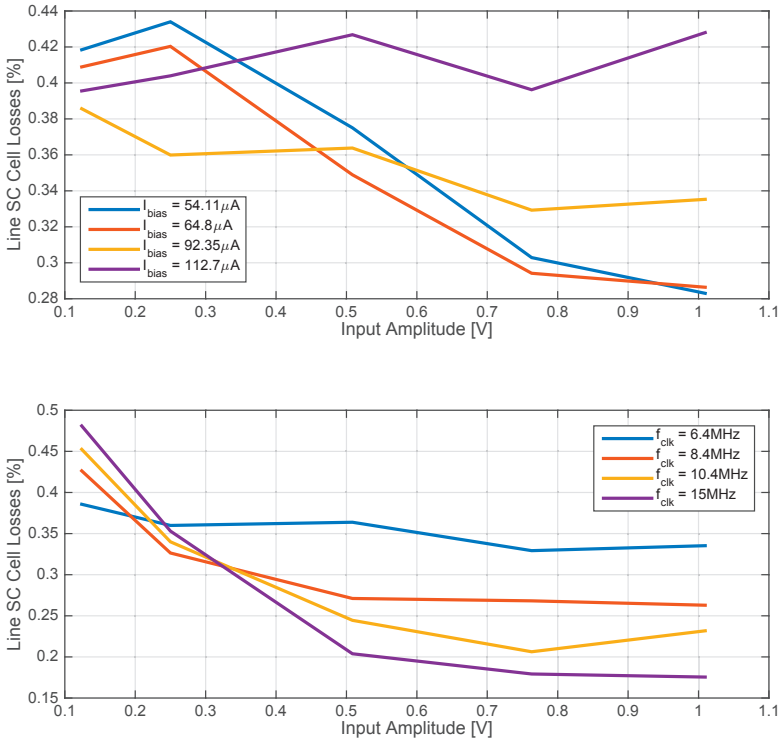


Figure 7.3: Cell losses as a function of the input voltage amplitude for different bias currents (upper graph) and switching frequency (lower graph).

despite the measurement noise perturbation, alternate impulses of amplitudes decreasing as a function of the reflection coefficients can be noticed at both observation points and at expected times.

### 7.2.1 Switching Frequency and Bias Current

The impact of the OTA bias current and switching frequency on the charge transfer between following SC cells can also be evaluated through the line impulse response. Similarly to the amplifier finite gain, an uncompleted charge transfer caused by an excessive switching frequency or insufficient OTA transconductance (set by the bias current) can be considered as equivalent losses in the line. Since the losses affect the fault location accuracy, an optimal switching frequency and bias current have to be set in order to provide a sufficient processing speed and a reasonable current consumption, while ensuring the targeted resolution of 1%. These optima can be deduced from the cell losses measured as a function of the line input amplitude displayed in Fig. 7.3. The upper graph represents the losses with various bias currents and a clock frequency set to $f_s = 6.4$ MHz, and the lower plot displays the losses with various switching frequencies and a bias current of $I_{bias} = 92\,\mu$A. The line input, output and

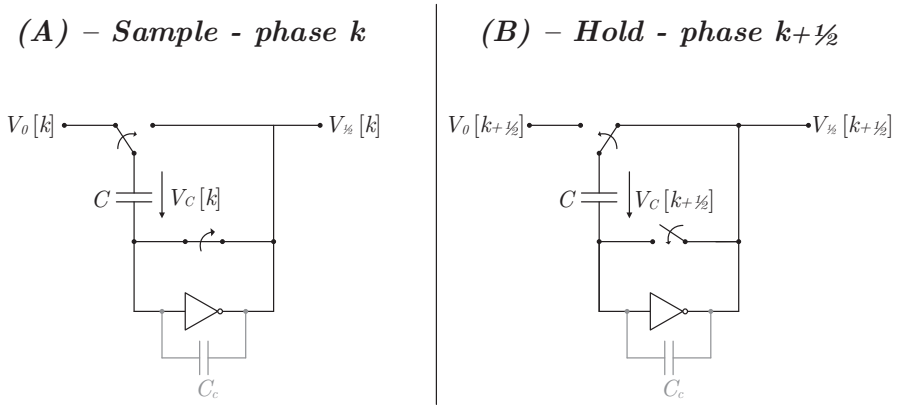


Figure 7.4: Sampling (A) and holding (B) phases of the SC cell with parasitic cross-coupling capacitance $C_c$ between the OTA input and output.

fault reflection coefficients are set to $\rho_i = \rho_o = -\rho_r = 0$, in order to maximize the amplitude of the propagated signal, and the average cell losses are evaluated between line taps 10 and 90.

In both cases, losses tend to decrease for higher voltage amplitudes, since the transconductance increases for larger signals, as shown by simulations in Section 6.2.3. When the bias current increases, the transconductance increases too, thus improving the charge transfer, and therefore reducing the equivalent losses. On the other hand, a bias current increase reduces the OTA DC gain and tends to increase the losses. An optimum is found for a bias current equal to $I_{bias} = 92\,\mu$A, which is higher by a factor of 1.7 than the expected consumption, but still reasonable. According to the lower graph, the equivalent losses increase with frequency in the small signal range. This phenomenon appears to be inverted for larger signals, but it is caused by signal overshoot, and thus, shouldn't be considered so. Consequently, a frequency optimum, offering a sufficient processing speed versus fault location accuracy, can be set to $f_s = 6.4$ MHz. Although this value is more than twice as low as the expected frequency, its consequent processing time increase can be compensated by evaluating the time-reversed fault signature in a reduced time window with the same accuracy [28].

With a bias current and a switching frequency set to $I_{bias} = 92\,\mu$A, and respectively $f_s = 6.4$ MHz, the measured cell losses reach on average 0.36% of the input signal ($\alpha_{dB} = 0.03$ dB), which is much higher than the expected $\alpha_{dBmax} = 0.01$ dB corresponding to the maximum 1 dB losses accumulated over the entire line. The source and the impact of these equivalent losses is discussed in the following section.

### 7.2.2 Equivalent Losses Induced by Parasitic Coupling Capacitance

According to previous observations, losses of $\alpha_{dB} = 0.03$ dB were measured for each elementary delay cell. This value is about three times higher than the maximum expected one allowing a proper fault location, as defined by (4.10). Through layout parasitic analysis, it can

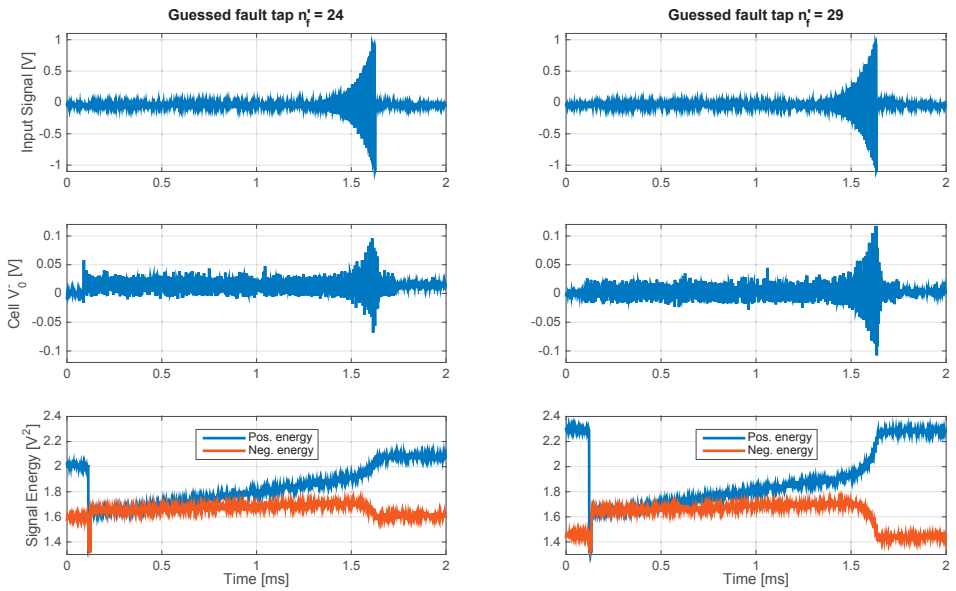


Figure 7.5: EMTR process transient measurements for a fault situated at $x_f = 30\%D$ and guessed fault taps at $n'_f = \{24; 29\}$.

be shown that these equivalent losses are caused by a non-negligible cross-coupling parasitic capacitance ($C_c \simeq 4$ fF) that exists between each cell OTA input and output, as displayed in Fig. 7.4-(A-B). Although this parasitic capacitance $C_c$ is shorted during the sampling phase (A), it is connected in parallel to the capacitor $C$ in the holding phase (B), and thus, splits the total accumulated charges in $C$. Consequently, the transmitted signal is attenuated by a factor of

$$K_{cc} = \frac{C}{C + C_c} \tag{7.1}$$

and reaches $K_{cc} = 0.996$, assuming $C = 1$ pF. This attenuation factor corresponds to cell losses of $\alpha_{dB} = 0.035$ dB, which is on the same order of magnitude as the measured ones. According to Fig. 4.5, a fault can be properly located if the losses between the line input and the fault coordinate remain below $\alpha_{dBTot} = 2.5$ dB, if the reflection coefficient are of high magnitude. In this case, considering the measured cell losses of $\alpha_{dB} = 0.03$ dB, a fault remains properly detectable until the $n'_{f_{max}} = \alpha_{dBTot}/\alpha_{dB} = 83$ line tap. This issue with the losses can be solved by optimizing the circuit layout in such a way that the parasitic capacitance between the OTA input and output is minimized.

## 7.3 Fault Location Measurements

The back-propagation phase of a time-reversed signature corresponding to a fault occurrence at $x_f = 30\%D$, where $D$ is the line length, is illustrated by transient measurements displayed in Fig. 7.5. The measurements in the right plots are realized with a guessed fault at line tap $n'_f = 29$, which correspond to $30.2\%D$, considering the line resolution of 1.04% set by the number of cells $N = 96$. According to the given resolution, this tap is the closest to the real fault location and should consequently yield the highest energy level. The left plots display the measurements realized with a guessed fault at line tap $n'_f = 24$, so $25\%D$, and should be consequently yielding a lower energy level. The upper graphs represent the back-propagated time-reversed fault signature in the emulated line, the middle graphs show the resulting voltage at observation point $V_0^-$ and the lower graphs show the corresponding positive and negative phase energy of signal $V_0^-$.

As expected, the line voltage at observation point $V_0^-$ is visibly of higher magnitude at the emulated guessed fault tap $n'_f = 29$ than at $n'_f = 24$. Consequently, the fault signal energy, consisting of the difference between the positive and negative energy phases, is also a maximum for $n'_f = 29$, allowing thus the location of the fault. Experiments and [28] have shown that a signal energy computation with a reduced time window can still provide accurate fault location results. Consequently, the back-propagation phase duration is divided by two, compared to that in Section 3.2.2, so that the energy is computed only during the fault signature duration. In the present case, a back-propagation phase lasts about 1.67 ms, and therefore the entire fault location process consisting of $N = 96$ iterations lasts 160 ms. This is much faster than the few seconds obtained with existing FPGA-based fault location methods [29] and makes thus real-time implementations realistic.

### 7.3.1 Final Results

The fault location process is executed in the SC line ASIC and the corresponding results are compared with the simulations realized in a lossless line and in the gm-C line model presented in Chapter 4, as illustrated in Fig. 7.6. The process is executed in lines with reflection coefficients set to $\rho_i = \rho_o = -\rho_r = 0.94$ for three critical cases. The upper graph represents a fault occurrence close to the line input, at 3% of the line length $D$, and hence close to the corresponding resolution limit of 1.04%. The measurements and simulations reveal a guessed fault current energy maximum at the expected location. The shape of the curve is very similar for the three cases. The middle graph represents a critical case, with a fault situated at $10\%D$, i.e., halfway between taps 10 and 11, at $9.38\%D$ and $10.42\%D$ respectively, referring to a line discretization of $N = 96$. The fault location is correctly interpolated and the expected result is obtained for the measurements as for the simulations, despite the finite resolution. The lower graph illustrates a fault case situated close to the line end at $80\%D$, and thus more affected by the per unit length equivalent line losses present in the switched-capacitor and gm-C line models. It can be seen that an attenuation as a function of

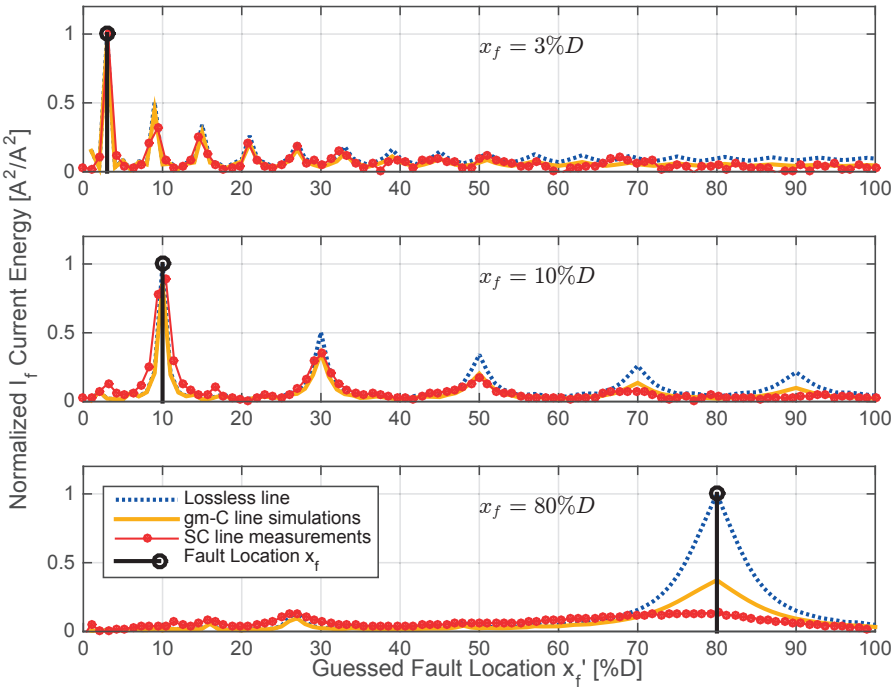


Figure 7.6: Fault location result for faults situated at 3%, 10% and 80% of the total line length and reflection coefficients set to $\rho_i = \rho_o = -\rho_r = 0.94$.

the guessed fault position occurs and damps the global maximum, leading to possible fault location misinterpretation. This undesirable effect is more pronounced in the SC line case due to the parasitic capacitances between the cell OTA input and output, as studied in Section 7.2.2. According to the evaluated cell losses, $\sim 80\%D$ is the farthest fault location that can be properly located with the present ASIC. This issue can be solved by a layout optimization in a way to limit this parasitic capacitance, but would require a new silicon implementation of the circuit.

Although a further increase of the reflection coefficient magnitude affects the fault location results in a negligible way, lower coefficient magnitudes smoothen the maxima and make it less detectable, as shown in the measurements and simulation comparisons in Fig. 7.7. In this case, setting the reflection coefficients to $\rho_i = \rho_o = -\rho_r = 0.84$ still allows a proper location of faults situated from the beginning to the middle of the line, but makes the case of a fault at the line end, at $80\%D$, undetectable.

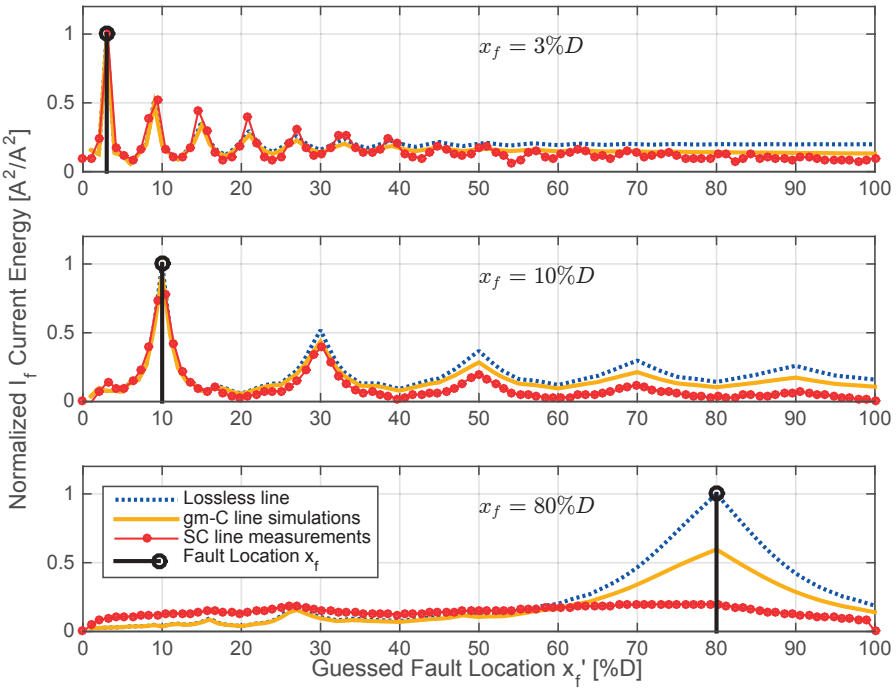


Figure 7.7: Fault location results for faults situated at 3%, 10% and 80% of the total line length and reflection coefficients set to $\rho_i = \rho_o = -\rho_r = 0.84$.

## 7.4 Current Consumption

With a switching frequency of $f_s = 6.4$ MHz, the circuit current consumption reaches 23 mA, including a static component of $I_{Vddamp} = 16$ mA, that principally supplies the $2N$ OTAs, and a dynamic part of $I_{DVDD} = 6$ mA and $I_{AVDD} = 1$ mA, for the switching circuitry. The static current supplied by $V_{ddAmp}$ reaches the order of magnitude of $200 I_{bias} = 18$ mA with $I_{bias} = 92\,\mu$A, as expected in Section 6.6. On the other hand, the dynamic current is hard to estimate through simulation since it is strongly affected by parasitic capacitances. The current consumption as a function of frequency is given in Fig. 7.8. As expected, the circuit consumption is dominated by the OTA static current.

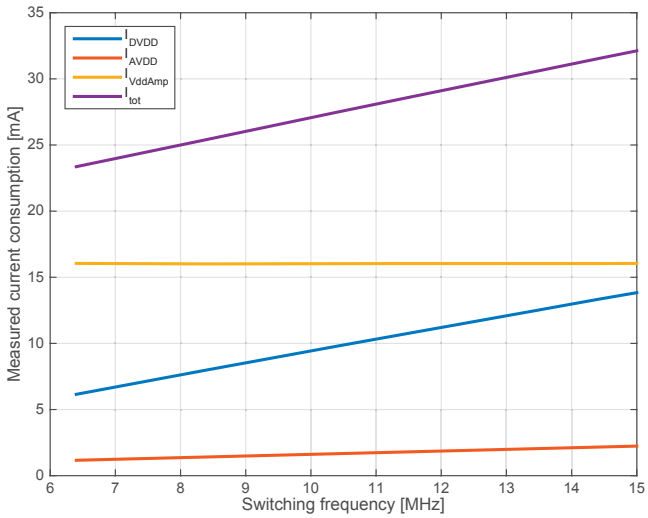


Figure 7.8: Static, dynamic and total current consumption as a function of switching frequency.

## 7.5 Conclusion

The present measurements have demonstrated that the implemented SC line ASIC is globally functional and allows a fault location with the EMTR method on most of the line length, with a resolution close to one percent, with a processing time of a few hundred milliseconds. The circuit bias current and switching frequency have been adjusted for optimal performance through measurements realized with the presented test bench. Compared to the theoretical expectations, the bias current has been increased and the clock frequency decreased to improve the charge transfer between following SC cells, and thus limit the equivalent line losses. A reasonable ASIC current of 23 mA, including 16 mA of static current and 7 mA of dynamic current at 6.4 MHz, is then measured. On the other hand, the switching frequency reduction decreases the fault location processing speed. This process duration increase can, however, be compensated for by a reduction of the observation time window during the back-propagation phase, so that a single fault location phase lasts only 1.67 ms, as opposed to the 60 ms with the existing FPGA-based solution. This time gain over classical digital solutions allows a fault location within 160 ms, considering a resolution of 1%, which is in the same order of magnitude as the reference opening time of a power switch, and thus, allows a real-time implementation of such a system. Transient measurements have revealed the presence of additional losses in the line caused by the presence of a non-negligible cross-coupling capacitance between each OTA input and output. These losses accumulate along the line and make the location of faults far from the line input ($> 80\%D$) difficult or impossible. This unexpected effect doesn't compromise the method and can be avoided by a minimization of the OTA input to output parasitic capacitance through circuit layout optimization. However, this would require a new silicon implementation of the circuit.

# 8 Line Model Enhancements

Previous chapters have shown that the presented models and corresponding implementations are well suited to the fault location method using the EMTR principle, and provide much faster results than existing digital solutions with a similar resolution. This chapter presents an alternative to the discrete-time line model and discusses the applicability of the method to simulate more complex network topologies. The impact of the magnitude quantization on the discrete-time model is considered. Although the quantization produces a distortion of the signal, and consequently an additional fault location inaccuracy, it allows fully digital implementations, thus avoiding many of the non-ideal effects associated to analog circuits. Moreover, digital circuits are compatible with higher clock frequencies and finer process implementations, providing thus significant processing speed increases and silicon area reductions. The second part of this chapter presents a possible enhancement of the simple single-phase line studied up to now, to more complex network topologies, such as interconnected or multi-conductor lines. It is shown that line interconnections can be simulated according to the travelling waves approach by an associated functional block. On the other hand, the modelling of coupled lines, particularly in inhomogeneous propagation media, requires additional circuitry and a modal decomposition of the system, so that the problem can be solved by independent equivalent lines, easier to implement.

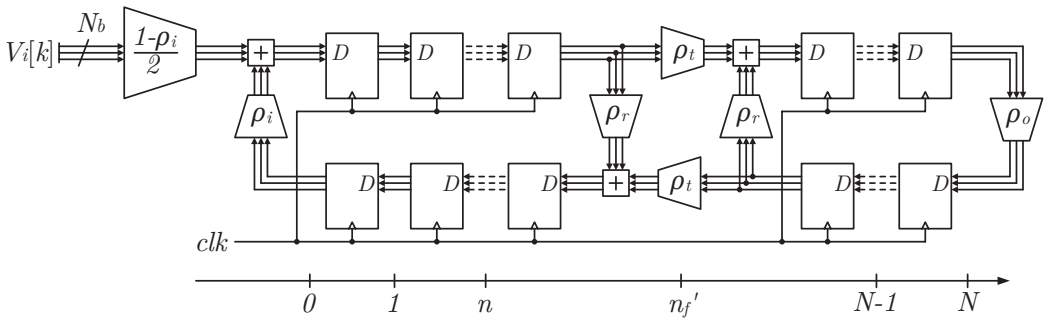


Figure 8.1: $N_b$-bit fully digital implementation of discrete-time line model.

## 8.1 Discrete-Time and Magnitude Quantified Line Model

By adding magnitude quantization, the discrete-time line model introduced in Chapter 3 allows simpler implementations. Indeed, similarly to the switched-capacitor line, the same model can be implemented with digital circuits. As shown in Fig. 8.1, the delay elements can be realized with D latches and the input, output, and guessed fault blocks by combinations of logical adders and multipliers. As opposed to any analog realization, the fully digital version avoids many associated non-ideal effects. There simply are no line losses limiting the fault location accuracy, and finer implementation processes allow reaching much higher clock frequencies, thus increasing the processing speed proportionally. However, the quantization inherent in the model digitization has to be set adequately to limit the associated distortion added to the process, which impacts the fault location accuracy.

### 8.1.1 Impact of the Quantization

The impact of the quantization can be evaluated according to the Signal-to-Noise Ratio (SNR) between the resulting EMTR signal energy $W_{EMTR}$ and its corresponding quantization noise $\sigma\left(W_{Q_N}\right)$. This noise can be deduced by considering the equivalent noise sources associated to the input signal quantization and the result truncation occurring after each multiplication. The equivalent discrete-time line model taking into account the noise sources $Q_{N_0}$ to $Q_{N_3}$ is displayed in Fig. 8.2. According to the calculations in Appendix G.1, these noise sources combine and accumulate along the line so that an equivalent noise can be observed at the fault signal measurement tap $V_0^-$ (tap defined in Section 6.5). From this there can be derived the equivalent quantization noise standard deviation $\sigma\left(W_{Q_N}\right)$ of the fault signal energy $W_{EMTR}$. Therefore, the resulting signal-to-noise ratio [77] is given by

$$SNR = \frac{W_{EMTR}}{\sigma\left(W_{Q_N}\right)}, \tag{8.1}$$

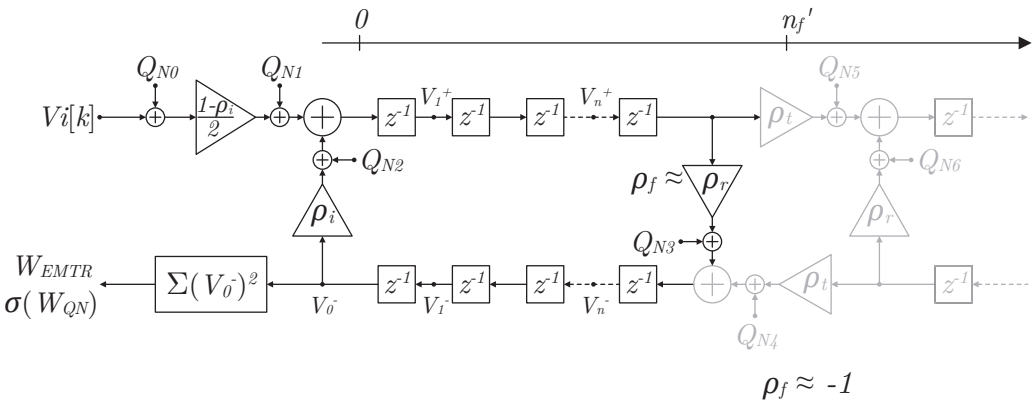


Figure 8.2: Equivalent discrete-line model with quantization noise.

with the EMTR fault signal energy maximum calculated in Appendix C.1 in (C.17), and its noise standard deviation calculated in (G.14):

$$\begin{cases} W_{EMTR} &= \dfrac{n_f}{8}\cdot\rho_f^2\cdot\dfrac{\left(1-\rho_f\right)^2\cdot\left(1-\rho_i^2\right)^2\cdot\left(1+\left(\rho_i\rho_f\right)^2\right)}{\left(1-\rho_i\rho_f\right)^2\cdot\left(1-\left(\rho_i\rho_f\right)^2\right)^3}, \\ \sigma\left(W_{Q_N}\right) &= \dfrac{\sigma_{Q_N}^2}{4}\cdot\sqrt{N_i}\cdot\dfrac{4+\rho_f^2\left(9-2\rho_i+\rho_i^2\right)}{1-\left(\rho_i\rho_f\right)^2}. \end{cases} \tag{8.2}$$

In the noise calculation, $N_i$ represents the number of integration periods required to compute the signal energy, and $\sigma_{Q_N}$, the quantization noise standard deviation associated to $Q_{N_0}$ to $Q_{N_3}$ given by (G.5), and redefined as

$$\sigma_{Q_N} = \frac{1}{2^{N_b}\cdot\sqrt{12}}, \tag{8.3}$$

where $N_b$ is the quantization. The SNR tendency can be evaluated in a rough estimation considering a first order approximation of (8.1) with (8.2), and assuming that $\rho_i = -\rho_f = \rho \in [0;1]$, so that

$$SNR \simeq \frac{n_f\cdot\left(\rho-4\right)}{144\cdot\sigma_{Q_N}^2\cdot\sqrt{N_i}}. \tag{8.4}$$

Since the fault signature duration (Appendix A.1), and consequently, the resulting energy, are proportional to the fault location $n_f$, the faults situated close to the line end are less affected by

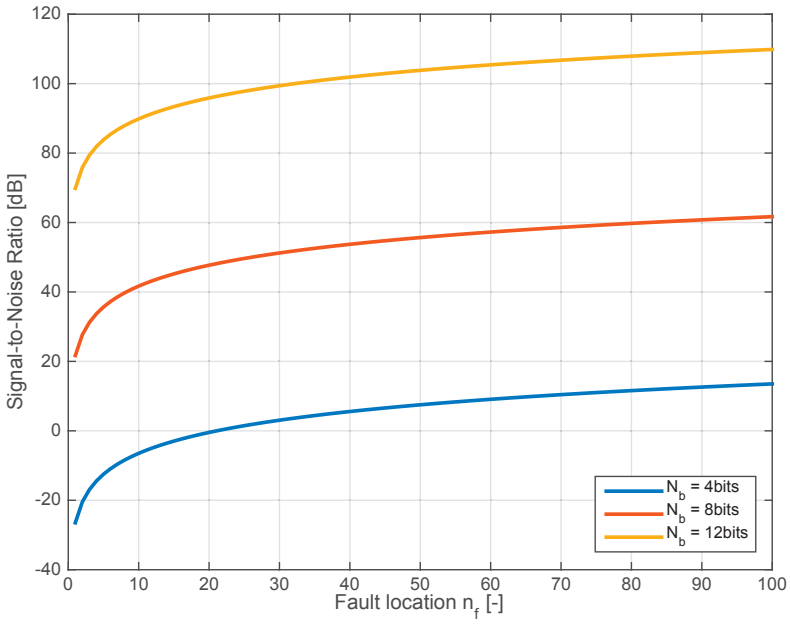


Figure 8.3: Signal-to-noise ratio as a function of the guessed fault for different quantizations.

the noise. On the other hand, the noise level increases with the number of integration periods $N_i$. This parameter has to be adjusted to fit the time window corresponding to the signal energy duration, and thus avoid the integration of unnecessary signal and its corresponding noise. Since the signal energy and the noise level increase with $\rho$, both components compensate so that the magnitude of the reflection coefficient has a lower impact on the SNR.

The SNR associated to the signal energy and noise definitions in (8.2) is evaluated in a typical case, with $\rho_i = 0.99$, $\rho_f = -0.96$ and $N_i = 40k$, referring to the fault signature length and a process resolution of 1%. The graph in Fig. 8.3 illustrates this SNR as a function of the discrete fault tap $n_f$, for different quantizations ($N_b = \{4;\ 8;\ 12\}$). While $N_b = 4$ bits offers poor SNR results, a quantization of 8 bits provides between 20 dB and about 60 dB SNR, from the line input to its end. In the frame of the fault location, this value is sufficient to distinguish two neighboring guessed fault taps, even close to the line input, where typically a ratio of 10 is observed between the fault location maximum at $n_f$, and the neighbors at $n_f \pm 1$ (Section 2.3.3).

### 8.1.2 Full Digital Implementation of the Discrete-Time Line Model

In a digital line model, each signal propagating along the line is associated to a corresponding binary value. According to the alternative nature of the propagating signals and the floating point character of the reflection/transmission coefficients defined in the range $\rho \in [-1;1]$, a set of signed floating-point binary numbers is required for a proper encoding of the model's

| *Decimal* | *Signed Binary* | | | |
|---|---|---|---|---|
| | $\pm$ | $2^{-1}$ | $2^{-2}$ | ... |
| + 0,75 | 0 | 1 | 1 | |
| + 0,50 | 0 | 1 | 0 | |
| + 0,25 | 0 | 0 | 1 | |
| 0,00 | 0 | 0 | 0 | |
| - 0,25 | 1 | 1 | 1 | |
| - 0,50 | 1 | 1 | 0 | |
| - 0,75 | 1 | 0 | 1 | |

*Two's complement* $\overline{X}+1$

Figure 8.4: Decimal/binary equivalence of 3 bits encoded signed floating-point numbers.

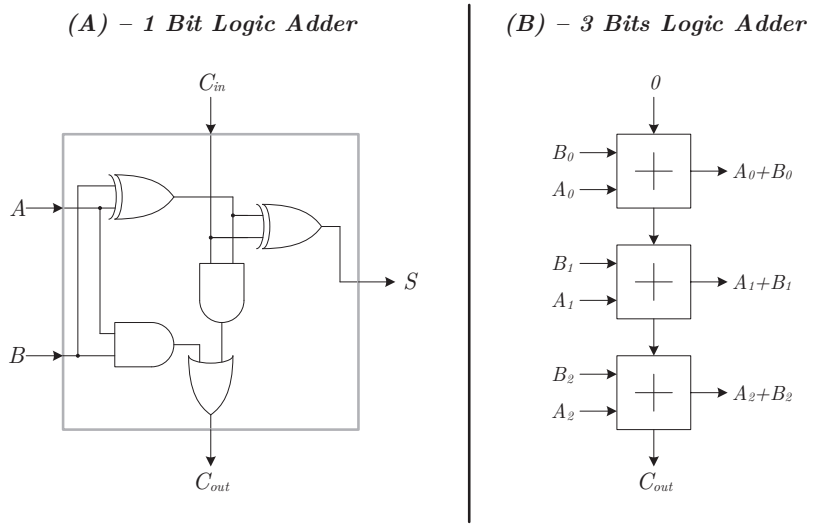


Figure 8.5: Single-bit adder (A) and 3-bit adder combination (B).

magnitudes. The signed numbers can be encoded with the two's complement representation, while any rational value can be represented by sums of powers of two with negative exponents[74]. Without loss of generality, the encoded absolute magnitudes can be normalized to one, so that the Most Significant Bit (MSB) defines the sign, and the $N_b - 1$ other digits represent the number's absolute value, equal to the sum of the negative exponent powers of two, from $2^{-1}$ to $2^{-(N_b-1)}$. As an example, Fig. 8.4 displays the decimal/binary equivalence of the $N_b = 3$ bits encoded signed floating-point numbers.

### Implementation of the Logic Adder and Multiplier

The signed addition and multiplication implemented at the line boundaries can be realized with combinational circuits providing a quasi-instantaneous computation result, according to the logic gates' propagation delay. The $N_b$-bit addition is realized by a series combination of

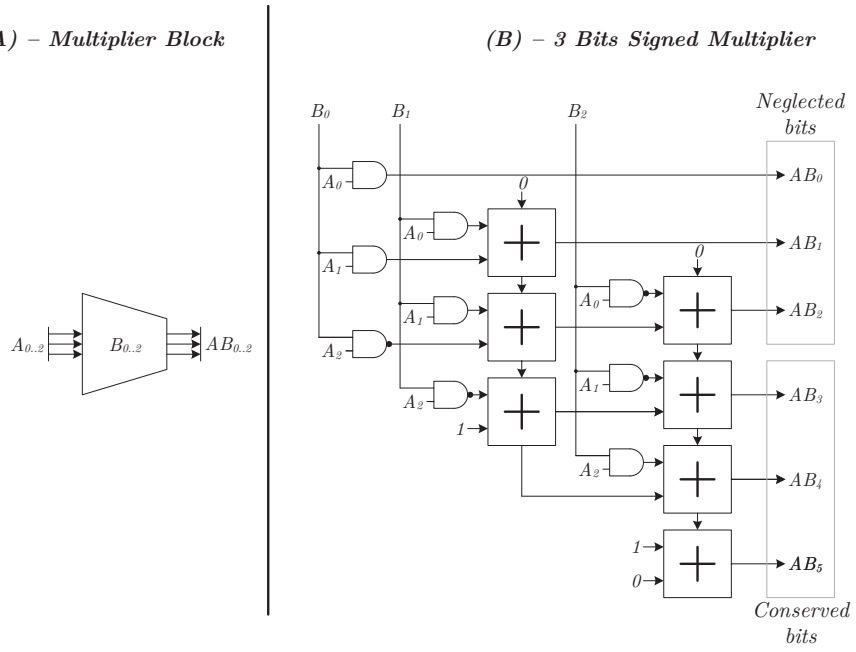


Figure 8.6: 3-bit multiplier block (A) and equivalent logic diagram (B).

$N_b$ full bit adders implemented with logic gates [74], as illustrated in Fig. 8.5-(A-B). On the other hand, the $N_b$-bit multiplication cannot be implemented through simple combinations of elementary blocks and needs to be realized in many phases. As illustrated in Fig. 8.6, the $N_b$-bit signed multiplication is realized successively through a one-to-$N_b$ bit multiplication and addition repeated $N_b$ times [75]. The signed multiplication is realized with AND/NAND logic gates and the addition with the circuit described in Fig. 8.5-(B). As shown in Fig. 8.6-(B), the resulting size of an $N_b$-bit multiplication is $2N_b$ bits. Since only one-half can be kept, the $N_b$ Least Significant Bits (LSB) of the result are lost, generating a corresponding error. This truncation error is limited by the quantization step set by $2^{N_b-1}$.

Due to the complexity of the operation, the circuitry required to perform an $N_b$-bit multiplication increases by about $N_b^2$, which is a limiting factor taking into account the proportional silicon area and associated cost. Furthermore, as the size of the multiplier increases, the global propagation time increases with $N_b$, limiting thus the maximum system frequency, and hence the processing time. Consequently, the quantization has to be set adequately in order to limit the associated impact of the noise on the accuracy of the fault location while keeping a reasonable circuit area and sufficient processing speed.

### 8.1.3 Processing Speed and Silicon Area

The fault location processing speed is set by the clock frequency cadencing the D latches. This frequency is limited by the block having the longest propagation time in the circuit. Due to its cascaded topology, the slowest operation is the multiplication and addition executed at the

| Circuit | Gate Count [-] | Area [$\mu m^2$] | Max Delay [ns] |
|---|---|---|---|
| NAND | 1 | 8.8 | 0.05 |
| AND | 1.5 | 11 | 0.1 |
| D Flip-Flop | 6 | 41.7 | 0.25 |
| Full Adder | 7 | 50.5 | 0.3 |

Table 8.1: Characteristics of different TSMC 0.18 µm digital blocks. The propagation delay is given for a load capacitance of 5 fF in typical condition.

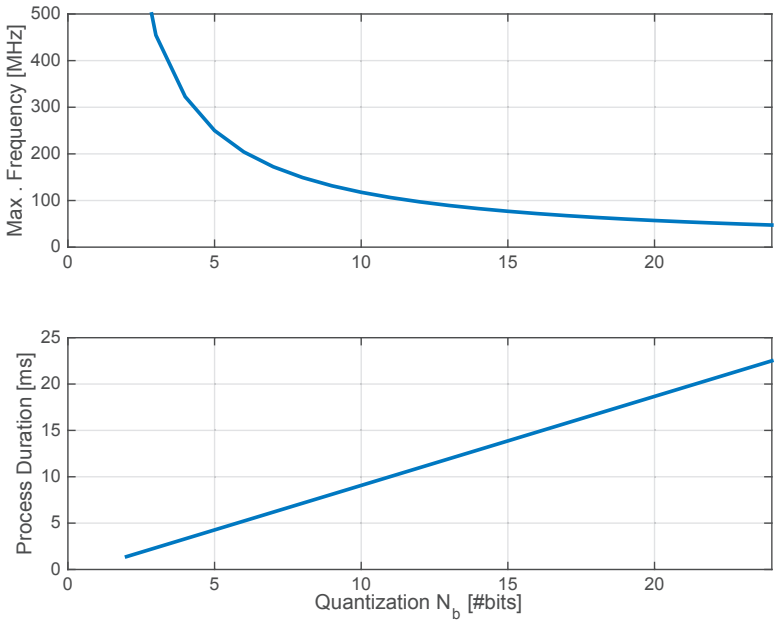


Figure 8.7: Maximum clock frequency (up) and full process duration (down) for a TSMC 0.18 µm digital implementation.

line boundaries, referring to the discrete-time digital line model in Fig. 8.1. According to the $N_b$-bit multiplier and adder topologies in Fig. 8.5 and Fig. 8.6, the longest propagation time is measured between the input LSB and the output MSB, and can be estimated to be

$$T_{D_{max}} \simeq (3N_b - 2) \cdot T_{FADD}, \tag{8.5}$$

where $T_{FADD}$ is the full bit adder propagation delay. According to the delay times in a typical CMOS 0.18 µm technology (TSMC 0.18 µm) listed in Tab. 8.1, the maximum frequency defined by $f_{max} = 1/T_{D_{max}}$ is expressed as a function of the quantization in Fig. 8.7. The corresponding fault location processing time is extrapolated in the lower graph, according to the measurement results obtained with the SC line in Chapter 7, specifying a fault location within 160 ms for a clock frequency of 6.4 MHz. Consequently, a quantization set to $N_b = 12$ bits, which

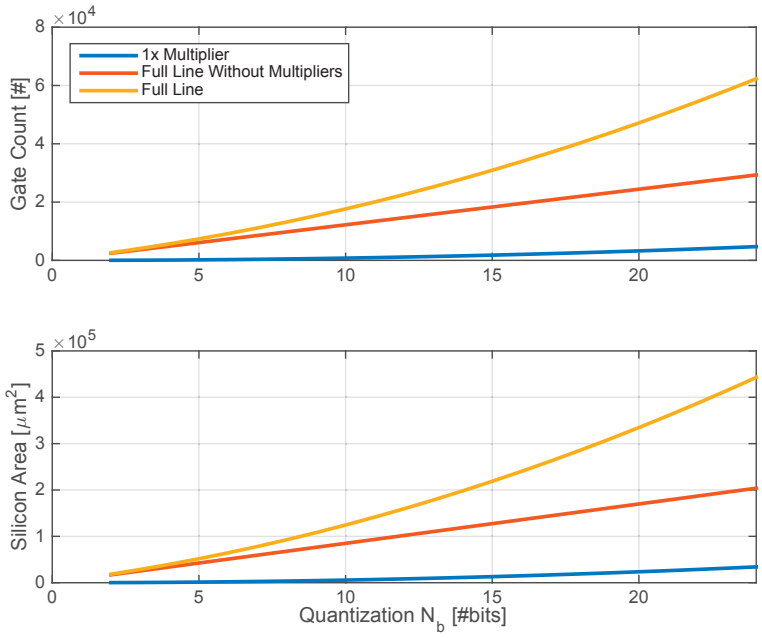


Figure 8.8: Transistor gate count (up) and silicon area in a TSMC 0.18 µm process (down).

ensures adequate SNR properties, allows resolving the fault location process within 11 ms at the most, at a clock frequency of 97M Hz. For a similar resolution, this result is about 15 times shorter than with the switched-capacitor line solution, and more than two decades shorter than with the FPGA-based method.

### Silicon Area

The total circuit area is evaluated according to an equivalent *gate count*, independent of the implementation process, and as a function of the different blocks area implemented in a TSMC 0.18 µm technology. Referring to the line model of discretization $N$ and quantization $N_b$ displayed in Fig. 8.1, the total count of D flip-flops $DFF$ composing the line reaches

$$LINE \longleftarrow 2N_bN \cdot DFF. \tag{8.6}$$

From Fig. 8.5 and Fig. 8.6 there can be deduced the count of $AND$, $NAND$ and full bit adders $FADD$ composing an $N_b$-bit adder, respectively, multiplier:

$$\begin{cases} ADD_{N_b} \longleftarrow N_b \cdot FADD \\ MULT_{N_b} \xleftarrow{\sim} N_b(N_b-1) \cdot FADD + (N_b-1)^2 \cdot AND + 2N_b \cdot NAND \end{cases} \tag{8.7}$$

Considering the gate counts and silicon area of the corresponding blocks displayed in Tab. 8.1, the total gate count and silicon area of a single multiplier, the full line without and the full line including the multipliers, is shown in Fig. 8.8 as a function of the quantization $N_b$, for $N = 100$. While the $N$-tap line takes the most area and highest gate count for low quantizations, the multipliers quickly dominate for higher $N_b$ due to the quadratic character of the function describing the required circuitry. With a quantization of $N_b = 12$ bits, ensuring adequate SNR properties, the total circuit gate count is estimated to be 22.6 k and the silicon area in a TSMC 0.18 µm process as 0.16 mm$^2$, so about 56 times lower than the switched-capacitor implementation of 9 mm$^2$ presented in Chapter 6.

### 8.1.4 Discrete-Time Digital Implementation Summary

From previous evaluations, the digital implementation of the discrete-time line model seems to be a real improvement compared to its switched-capacitor equivalent. The non-ideal effects associated to MOS switched-capacitor circuits and their corresponding impact on the model, such as losses, are avoided. A quantization of $N_b = 12$ bits provides an equivalent signal-to-noise ratio estimated to more than 60 dB, which is more than enough to ensure the target resolution of 1%. Moreover, considering a TSMC 0.18 µm CMOS process implementation, a fault location processing speed of about 11 ms is estimated, so about 15 times less than the switched-capacitor line, and two decades less than the FPGA-based method. The silicon area of a 100-tap digital line is estimated to 0.16 mm$^2$, so about 56 times smaller than the switched-capacitor implementation of 9 mm$^2$. Considering its straightforward implementation and the optimistic processing speed characteristics, the digital realization of the discrete-time line seems very favorable for real-time fault location.

## 8.2 Implementation of the Network Connectivity

The discrete-time line model, introduced for the first time in Fig. 3.8, can be extended to larger power networks with line interconnections by following the same construction principle. Indeed, the line interconnection can be realized by an equivalent block inserted at the lines' junction. Fig. 8.9-(A-B) illustrates the transmission line schematic and respectively the equivalent discrete-time diagram of an interconnection between $K = 3$ lines of corresponding surge impedances $Z_{c_k}$ each, where $k \in [0; K-1]$. Based on the incident and reflected wave approach, an incident wave $V_i^+$ that reaches the interconnection from the $i^{th}$ line end is reflected by the ratio $\rho_{r_i}$ in the same line, in the opposite direction, and transmitted into the $k \neq i$ other connected lines, weighted by a ratio $\rho_{t_i}$. This symmetrical structure is repeated for each $k^{th}$ interconnected line end. The reflection, respectively, transmission, coefficients of

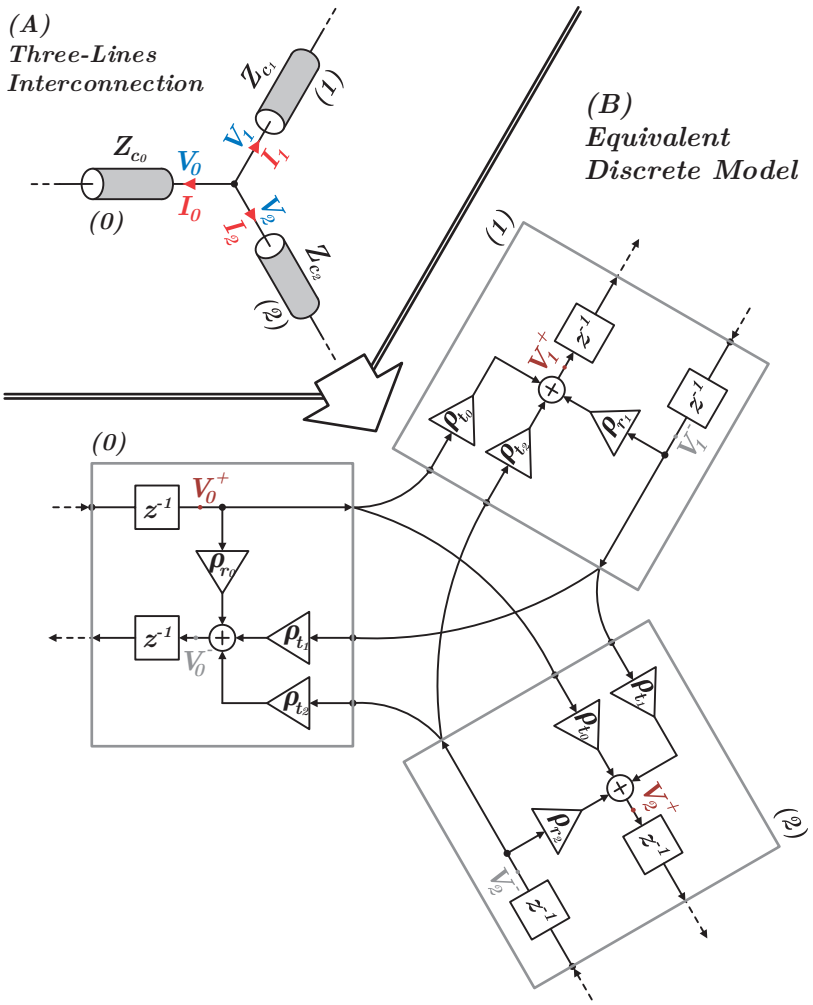


Figure 8.9: Interconnection between $K = 3$ transmission lines (A) and equivalent block diagram based on the incident-and-reflected wave approach (B).

the $i^{th}$ line are found through their definition (2.6) and (3.13) redefined hereafter as

$$\begin{cases} \rho_{r_i} &= \dfrac{Z_i - Z_{c_i}}{Z_i + Z_{c_i}} \\ \\ \rho_{t_i} &= \rho_{r_i} + 1, \end{cases} \tag{8.8}$$

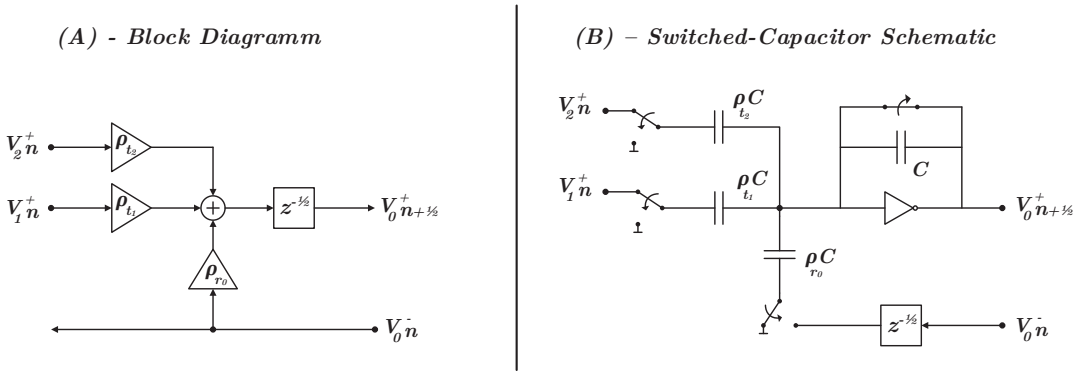


Figure 8.10: Interconnection diagram block (A) and equivalent switched-capacitor circuit (B).

where $Z_{c_i}$ is the surge impedance of the line itself and $Z_i$ the equivalent impedance seen from the corresponding line end. In the interconnected line case, (8.8) becomes

$$\begin{cases} \rho_{r_i} = \dfrac{2}{Z_{c_i}} \cdot \dfrac{1}{\sum\limits_{k=0}^{K-1} \frac{1}{Z_{c_k}}} - 1 \\ \rho_{t_i} = \dfrac{2}{Z_{c_i}} \cdot \dfrac{1}{\sum\limits_{k=0}^{K-1} \frac{1}{Z_{c_k}}}. \end{cases} \tag{8.9}$$

### 8.2.1 Switched-Capacitor Implementation

As an example, the line interconnection block of the line end (0) and its corresponding switched-capacitor implementation [57] are displayed in Fig. 8.10. The bloc consists of an SC adder that sums the $n^{th}$ sample of the incoming waves of each interconnected line, weighted by their respective reflection or transmission coefficient. The SC bloc delivers the outgoing wave delayed by one-half of the sampling period. The transmission coefficients $\rho_{t_k}$ are positive, while the reflection coefficient $\rho_{r_k}$ is negative in the considered cases, with line surge impedances of similar orders of magnitude for each line. In the SC topology, this negative reflection coefficient is considered as positive ($-\rho_{r_k}$) and subtracted from the result, so that all the implemented capacitances have positive values. The sign inversion is realized by the inversion of the corresponding input switch phase, implying thus the addition of a half period delay to be in phase with the other signals.

## 8.3 Multi-Conductor Line Emulation

As most power systems are based on multi-phase lines, a possible extension of the single line model to this kind of topology is explored. Due to the existence of mutual couplings between the different phases, the modelling approaches studied in the previous chapters cannot be directly transposed to the simulation of faults in multi-conductor systems. For this reason, modal transformation, a method for decoupling the phases based on an eigenvalue decomposition, can be applied ([65],[66],[67],[68],[69],[70],[71]). Consequently, an $N_p$-phase line can be decomposed into $N_p$ independent lines for each propagated mode, by employing a linear transformation. In this condition, the implementation of the decoupled lines can be realized through the single-line models previously studied. This section describes a distributed-parameter three-phase transmission line and its corresponding modal transformation. In the framework of fault location, a possible realization based on the travelling waves approach, implementable with the discrete-time model, is presented.

### 8.3.1 Three-Phase Line Characterization

In addition to the parameters of each phase considered independently, multi-conductor propagation media are characterized by cross-coupling components between the different phases ([65], [69]). As described in Fig. 8.11, each phase can be defined according to its specific per unit length inductance $L'$, capacitance $C'$, resistance $R'$, and conductance $G'$, plus the associated coupling components. Consequently, the line constituted by $N_p$ phases is characterized by the corresponding per unit length parameters, which make up $N_p \times N_p$ symmetric matrices[1] $[L']$, $[C']$, $[R']$ and $[G']$. According to these parameters, the corresponding infinitesimal impedance $[Z]$ and admittance $[Y]$ matrices are given by

$$\begin{cases} [Z] &= [R'] + j\omega[L'] \\ [Y] &= [G'] + j\omega[C']. \end{cases} \tag{8.10}$$

Considering only the lossless multi-conductor line, the per unit length resistance $[R']$ and conductance $[G']$ matrices are zero.

[1] The $[C']$ matrix doesn't correspond to the physical line capacitances of the infinitesimal representation, a transform is available in [70]

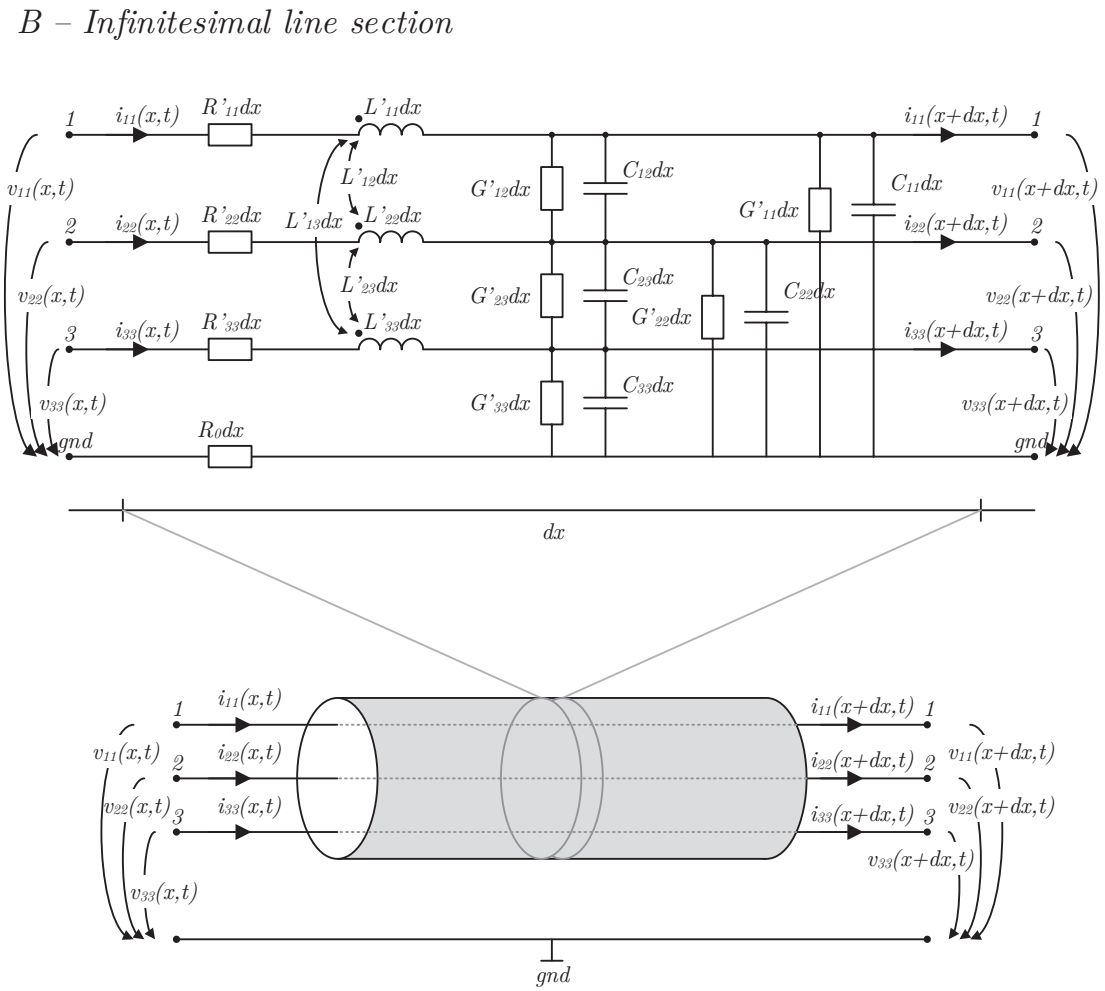


Figure 8.11: Three-phase line (A) and infinitesimal section of length $dx$ (B).

### 8.3.2 Multi-Conductor Line in Homogeneous Medium

Similarly to single-phase transmission lines, the voltage and currents propagating along a multi-conductor line can be described by the telegrapher's equations defined in (2.1). Considering the associated voltage and current matrices $[V]$ and $[I]$, these equations become

$$\begin{cases} \dfrac{d^2[V]}{dx^2} = [Z][Y][V] \\ \dfrac{d^2[I]}{dx^2} = [Y][Z][I]. \end{cases} \tag{8.11}$$

In homogeneous and lossless media, the mutual inductances and capacitances between the conductors compensate each other. Therefore, the product of the impedance and admittance matrices in (8.11) can be permuted, and is equal to the square of the propagation constant matrix $[\gamma]$ given by

$$[Z][Y] = [Y][Z] = [\gamma]^2 = \begin{bmatrix} \gamma_{11}^2 & 0 & 0 \\ 0 & \gamma_{22}^2 & 0 \\ 0 & 0 & \gamma_{33}^2 \end{bmatrix}. \tag{8.12}$$

In this particular case, the propagation constant matrix is diagonal, which means that the coupling between the lines in the telegrapher's equation is zero, and that each phase can be considered independently. Since these mutual effects cancel, a lossless three-phase line in a homogeneous medium can be emulated by three independent lines according to the models studied in the previous chapters.

### 8.3.3 Multi-Conductor Line in Inhomogeneous Medium

Unfortunately, the natural environment in which the power lines evolve is in general inhomogeneous, and thus, doesn't provide the simplification properties as in homogeneous media. In this case, the impedance and admittance matrices product in (8.12) is non-diagonal and cannot be permuted, so that

$$[Z][Y] \quad \neq \quad [Y][Z]. \tag{8.13}$$

According to the telegrapher's equation in (8.11), a non-diagonal $[Z][Y]$ and $[Y][Z]$ matrices implies that every voltages and currents along each phase are coupled with the neighboring conductors. In comparison to the multi-phase line representation in lossless a homogeneous medium, the complexity of the situation has highly increased, and cannot be directly simulated through the discrete-time line modelling approach.

### Modal Transformation

For the sake of implementation, the complex representation of the cross-coupled multi-conductor line in inhomogeneous media can be converted to an equivalent problem avoiding the coupling between phases. This transformation consists in diagonalizing the matrix products $[Z][Y]$ and $[Y][Z]$ of the telegrapher's equation with the modal approach. There is a method based on an eigenvalue decomposition [79]. This diagonalization is obtained by solving the corresponding eigenvalue equations given by

$$\begin{cases} [Z][Y][T_v] &= [T_v][\gamma]^2 \\ \\ [Y][Z][T_i] &= [T_i][\gamma]^2, \end{cases} \tag{8.14}$$

where $[T_v]$ and $[T_i]$ are the matrices of eigenvectors of the corresponding equations associated to the voltages, respectively, currents, and $[\gamma]^2$ is the diagonal matrix of eigenvalues common for both cases. Consequently, the voltages and currents along the line can be converted from their natural magnitudes $[V]$ and $[I]$ to their modal equivalents $[v]$ and $[i]$ employing the associated transformation matrix, so that

$$\begin{cases} [V] = [T_v][v] \iff [v] = [T_v]^{-1}[V] \\ \\ [I] = [T_i][i] \iff [i] = [T_i]^{-1}[I]. \end{cases} \tag{8.15}$$

Similarly, this transformation can be applied to (8.11) and gives the telegrapher's equation for modal magnitudes:

$$\begin{cases} \dfrac{d^2[v]}{dx^2} &= \underbrace{[T_v]^{-1}[Z][Y][T_v]}_{[\gamma]^2}[v] \\ \\ \dfrac{d^2[i]}{dx^2} &= \overbrace{[T_i]^{-1}[Y][Z][T_v]}^{[\gamma]^2}[i]. \end{cases} \tag{8.16}$$

Since the propagation constant matrix $[\gamma]$ is diagonal, each modal voltage or current equation is decoupled and can be solved independently. Through this linear transformation, each multi-conductor network can be decomposed into an equivalent network of independent lines of specific surge impedances and propagation speeds given by $\omega/Re[\gamma]$, and thus, can be represented through the line models studied in previous chapters.

### 8.3.4 Modal Representation of the Boundary Conditions

Similarly to the modal transformation of the line voltages and currents, the same principle applies to the line and boundary impedances defining the corresponding reflection coefficients. Indeed, from equations (8.15), there can be deduced the equivalent modal impedance or admittance of the line, so that

$$\begin{cases} [z] &= [v][i]^{-1} = [T_v]^{-1}[V]([T_i]^{-1}[I])^{-1} = [T_v]^{-1}\underbrace{[V][I]^{-1}}_{[Z]}[T_i] \\ \\ [y] &= [i][v]^{-1} = [T_i]^{-1}[I]([T_v]^{-1}[V])^{-1} = [T_i]^{-1}\overbrace{[I][V]^{-1}}^{[Y]}[T_v], \end{cases} \tag{8.17}$$

which finally, simplifies to

$$\begin{cases} [z] &= [T_v]^{-1}[Z][T_i] \\ \\ [y] &= [T_i]^{-1}[Y][T_v]. \end{cases} \tag{8.18}$$

In the same way, the line input and output modal impedances $[z_i]$ and $[z_o]$ can be obtained from their natural equivalents $[Z_i]$ and $[Z_o]$ through (8.18), so that

$$\begin{cases} [z_o] &= [T_v]^{-1}[Z_o][T_i] \\ \\ [z_i] &= [T_v]^{-1}[Z_i][T_i]. \end{cases} \tag{8.19}$$

Finally, from the modal surge impedance defined by

$$[z_c] = [y]^{-1}[\gamma], \tag{8.20}$$

the input or output modal reflection coefficient $[\rho_i]$ and $[\rho_o]$ associated to the corresponding impedances $[z_i]$ and $[z_o]$ can be obtained through the definition of the reflection coefficients in (2.6), so that

$$[\rho_k] = \frac{[z_k]-[z_c]}{[z_k]+[z_c]}. \tag{8.21}$$

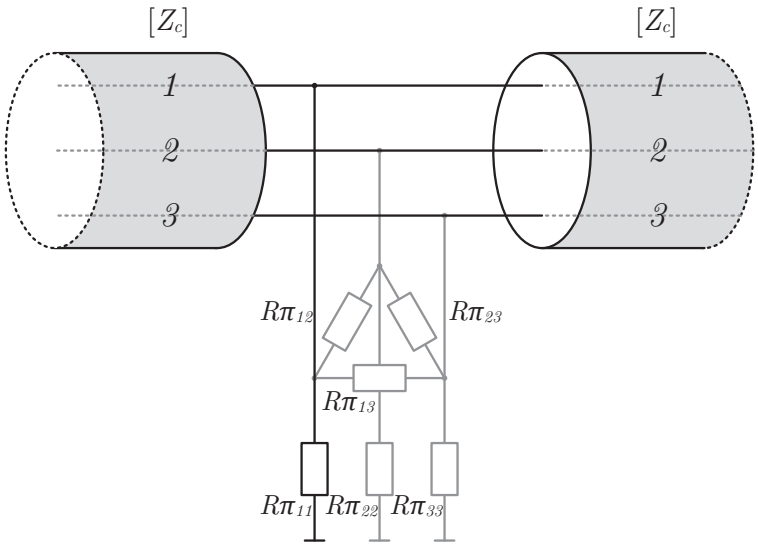


Figure 8.12: Mapping of the possible multi-phase fault occurrences on a 3x3 PI resistive network.

**Representation of the Fault Impedance**

In multi-conductor networks the number of possible fault types increases in comparison to the single line. Indeed, the following fault types can potentially occur [31]: single-phase-to-ground, double-phase-to-ground, three-phases-to-ground, and phase-to-phase. In the framework of fault location, these faults can be mapped on a corresponding resistive network connected in PI, as shown in Fig. 8.12 in the case of a three-phase line. From the corresponding $3 \times 3$ symmetric matrix given by

$$[R_\pi] = \begin{bmatrix} R_{\pi_{11}} & R_{\pi_{12}} & R_{\pi_{13}} \\ R_{\pi_{21}} & R_{\pi_{22}} & R_{\pi_{23}} \\ R_{\pi_{31}} & R_{\pi_{32}} & R_{\pi_{33}} \end{bmatrix}, \tag{8.22}$$

there can be deduced an equivalent fault impedance matrix $[Z_f]$ according to a transformation detailed in [72], so that

$$[Z_f] = \begin{bmatrix} \frac{1}{R_{\pi_{11}}+R_{\pi_{12}}+R_{\pi_{13}}} & -\frac{1}{R_{\pi_{12}}} & -\frac{1}{R_{\pi_{13}}} \\ -\frac{1}{R_{\pi_{12}}} & \frac{1}{R_{\pi_{12}}+R_{\pi_{22}}+R_{\pi_{23}}} & -\frac{1}{R_{\pi_{23}}} \\ -\frac{1}{R_{\pi_{13}}} & -\frac{1}{R_{\pi_{23}}} & \frac{1}{R_{\pi_{13}}+R_{\pi_{23}}+R_{\pi_{33}}} \end{bmatrix}^{-1}. \tag{8.23}$$

Consequently, the fault on the line and its corresponding fault impedance matrix can be considered similarly to an interconnection between lines, as evaluated in Section 8.2. Indeed, the situation is equivalent to an interconnection between two lines of surge impedance $[Z_c]$

and the fault of impedance $[Z_f]$ seen as a third line. Therefore, from the modal fault impedance, calculated equivalently to (8.18), so that

$$[z_f] \quad = \quad [T_v]^{-1}[Z_f][T_i], \tag{8.24}$$

the fault in a multi-conductor line can be characterized by equivalent modal reflection and transmission coefficient matrices $[\rho_r]$ and $[\rho_t]$. Through (8.9), these coefficients yield

$$\begin{cases} [\rho_r] \quad = \quad \dfrac{2}{[z_c]} \cdot \dfrac{1}{\sum\limits_{k=0}^{K-1} \frac{1}{[z_k]}} - [Id_3] \quad = \quad \dfrac{2}{[z_c]} \cdot \dfrac{1}{\frac{2}{[z_c]} + \frac{1}{[z_f]}} - [Id_3] \\ [\rho_t] \quad = \quad \dfrac{2}{[z_c]} \cdot \dfrac{1}{\sum\limits_{k=0}^{K-1} \frac{1}{[z_k]}} \quad = \quad \dfrac{2}{[z_c]} \cdot \dfrac{1}{\frac{2}{[z_c]} + \frac{1}{[z_f]}}, \end{cases} \tag{8.25}$$

with the modal line surge impedance $[z_c]$ from (8.20) and the identity $3 \times 3$ matrix $[Id_3]$.

### 8.3.5 Fault Simulation in a Three-Phase Line

According to the modal transformation and the line boundary characterization discussed in the previous sections, a multi-conductor line model based on the travelling waves approach is presented in the framework of fault location. The fault occurrence on a three-phase line of length $D$ and its equivalent model based on the travelling waves approach and modal transformation is displayed in Fig. 8.13.

The time-reversed fault signature back-propagated at the three-phase line input is converted to modal input voltages according to the transformation matrix $[T_v]$, as shown in (8.15). The corresponding signals are then propagated into the modal transmission lines defined by their surge impedance $[z_c]$ and propagation constant $[\gamma]$ matrices, according to modal transformations of the real line impedance $[Z]$ and admittance $[Y]$ matrices.

The modal reflection coefficients $[\rho_i]$ and $[\rho_o]$ at the line input and output boundaries can be defined according to the equivalent input and output resistor matrices $[R_i]$ and $[R_o]$, and their corresponding impedance matrix calculated with (8.23). Since no coupling is assumed at the boundaries, no coupling occurs at the modal inputs and outputs, and consequently, the corresponding modal reflection coefficients matrices are diagonal.

Since the fault, characterized by its equivalent resistor matrix $[R_\pi]$, is in general totally random and asymmetric, its corresponding modal reflection $[\rho_r]$ and transmission $[\rho_t]$ coefficients matrices are asymmetric too. Consequently a transmission or reflection coupling occurs between each forward and backward propagation path of each phase, so that $4N_p^2 = 36$

coupling can be accounted for, where $N_p = 3$ is the number of phases.

Finally, the fault current or associated voltage required for the fault location evaluation can be deduced from the modal representation. Indeed, any modal current or voltage can be converted from the modal to the natural representation of the network according to the current $[T_i]$ or voltage $[T_v]$ transformation matrices, as shown in (8.15).

**Three-Phase Line Implementation: Discussion**

The three-phase line model presented in Fig. 8.13 is realizable with different combinations of the discrete-time line model previously studied. Indeed, the possible implementation of decoupled lines has been demonstrated during this research, and any coupling elements at the line boundaries can be implemented according to the topology presented in Fig. 8.10. The different propagation times associated to the modal lines can be proportionally set by various numbers of delay elements composing each line. Therefore, a fine adjustment of the different propagation times could require a higher number of line delays, probably higher than in the case of the $N = 100$ elements considered in this research. Consequently, a higher number of line elements would increase the cumulative losses, if implemented with the presented switched-capacitor solution. Hence, the consideration of the discrete-time line full digital implementation avoiding these losses seems more appropriate. In addition, according to the complexity of the connectivity associated to the simulation of the fault reflection coefficients, a digital realization, less sensitive to parasitic capacitances and characterized by a simpler implementation, is probably more adequate than any analog solution.

Although the implementation of the multi-conductor line based on the modal representation seems realistic, an alternative based on the finite element modelling of the distributed parameters line might be realizable too. Similarly to the lumped line approach presented in Chapter 2, the coupled phases represented in Fig. 8.11 could be mapped on many LC elements taking into account the mutual coupling between the conductors. In the same way, this representation could be implemented with equivalent transconductor–capacitor (gm–C) circuits.

It may be that a model closer to the physical representation of the line, such as the lumped approach, appears more straightforward than a method based on complex mathematical transformations. However, a gm–C implementation of a lumped parameter multi-conductor line, taking into account every coupling, may be much more complex than a model based on a modal transformation, implementable with simple delays and arithmetic functions. In addition, the programmability of a multi-conductor line implemented with lumped elements would imply a corresponding parametrization of each equivalent inductance and capacitance, and would require a complex time calibration to minimize the impact of element mismatches. Taking into consideration all these discussed aspects, a fully digital implementation of the discrete-time approach based on the modal transformation seems to be the best option to emulate faults in multi-conductor networks.

## 8.4 Conclusion

This chapter has presented various improvements of the presented line model within the framework of fault location using the EMTR principle. First, an alternative to the discrete-time line model with a magnitude quantification was presented. It has been shown that this solution allows full digital implementations by means of shift registers and arithmetic functions, avoiding thus many of the non-ideal effects associated to analog circuits. With 12-bit quantification, this improved method allows locating a fault about 15 times faster than with the switched-capacitor, and more than two decades faster than with the FPGA-based implementation, obtaining a similar accuracy. And since digital circuits are compatible with finer process implementations, its overall circuit area on the silicon is estimated to be 56 times smaller than the analog SC implementation. According to these estimations, the discrete-time digital solution seems to be optimal for real-time fault location in electrical power systems. The second part of this chapter has explored the possible extension of the developed single-line model to more complex network topologies. In this context, an approach based on travelling waves simulating the interconnections between many power lines has been introduced. In addition, the emulation of multi-conductor lines has been evaluated. For this purpose, an equivalent model based on a modal transformation of the multi-phase line has been presented. A possible implementation by means of digital discrete-time circuit has been discussed.

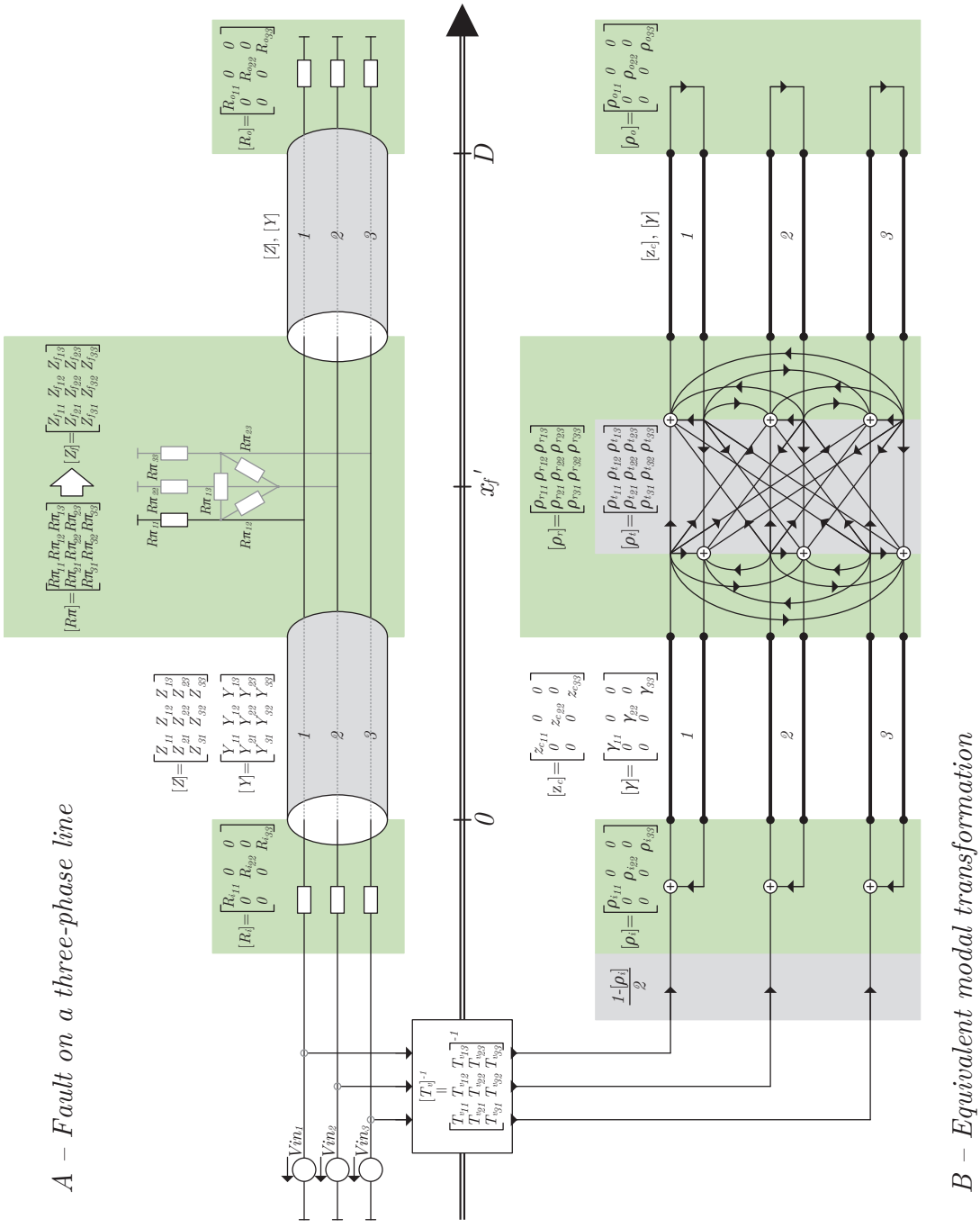


Figure 8.13: Fault on a three-phase line (A) and its modal decomposition (B).

# 9 Conclusion

The requirements of modern power systems have motivated the research of a new high performance fault location method. In this context, an algorithm based on the Electromagnetic Time-Reversal (EMTR) principle providing an accurate fault location seemed to be an adequate solution to the problem. Due to the method's complexity, an associated calculation platform optimized for its processing speed has been developed, in order to meet the expectations on the part of a smart grid of real-time capability. In an era where digital programmable systems have become more and more powerful, this research has explored the potential of a dedicated hardware simulator to implement the fault location method with greater efficiency. Despite a higher development cost and a reduced flexibility, dedicated solutions still perform better than programmable systems in solving very demanding cases. Different power network modelling approaches defined on a high level of abstraction were presented, and the corresponding integrated-circuit implementations were then considered. The impact of various modelling aspects, such as the discretization, the data sampling, and the quantization, were evaluated within the framework of fault location. From continuous-time to digitized discrete-time models, specific analog or digital hardware implementations with different accuracies and levels of complexity were studied. The programmability of such a dedicated hardware solution and its possible extension to the simulation of various network topologies was also evaluated.

It appears that the application EMTR to fault location presented in Chapter 2 is very efficient. Research in the field has highlighted the accuracy and robustness of the method for many different types of network and levels of complexity. According to these conclusions, there are many reasons to believe that the fault location solution using the EMTR principle is the response to the needs of today's power systems. However, the long and complex processing involved in this method in the case of a classical digital implementation is a major performance bottleneck, which goes against real-time capability, a key of today's smart-grid concept. It is this weak point that has motivated the search for a less time consuming implementation alternative, providing similar accuracy.

Despite their reduced programmability, dedicated hardware platforms optimized for processing speed seemed to be an adequate solution to the problem. Consequently, Chapter 3 has introduced two different power line models aimed at the implementation of the presented fault location method. The first approach models the distributed parameters physical line by means of a series of many discrete inductor and capacitor (LC) elements. The method has demonstrated its efficiency and showed that its accuracy depends on the number of elements composing the line. Indeed, a finer discretization brings the LC model closer to the definition of the physical line with distributed parameters. The second approach is based on the general solution of the telegrapher's equation describing the travelling waves propagating along the transmission line. This method is implemented with many discrete-time delay elements simulating the paths of the travelling wave, and arithmetic functions which emulate the wave's reflections and combinations at the line boundaries. This sophisticated approach, based on mathematical solutions, exactly describes the behavior of a lossless line, as opposed to the LC model. However, even though the representation of the transmission line by finite elements induces an associated error in the LC model, this error rapidly becomes negligible as the line discretization increases. Both models were developed following a top–down approach, by reducing the line to a combination of simple, well characterized, canonical elements, that is, the LC element in the case of the LC line, and a delay cell in the case of the discrete-time model. Consequently, these line pieces could be assembled as a function of the desired network topology to be implemented. The number of elements composing the line sets its discretization, and thus, the resolution of the fault location process. Therefore, the accuracy of the process can be set in a highly flexibile manner, according to the requirements of the power system.

The processing speed is set by the intrinsic time constant of the LC element, or, in the case of the discrete-time model, by the clock frequency. These parameters can be scaled down, thus providing incomparably short processing times, depending on the limitations of the implementation. Possible implementations of the LC line and the discrete-time models have been presented in Chapters 4 and 5. For each line model, a topology has been presented in order to implement the corresponding canonical line element. In the first approach, the LC element is implemented by a transconductor–capacitor (gm–C) circuit, more suitable for integration. On the other hand, the delay element of the discrete-time line model is implemented by an equivalent switched-capacitor (SC) circuit. At this point, the selection of an adequate topology is of prime importance, since each related non-ideal effect impacts the line model's speed or accuracy. Indeed, the influence of the non-idealities that usually plague CMOS analog circuits, such as the finite gain of the active elements, offset, dynamic range, clock-feedthrough of the SC circuits, charge injection, etc., has to be considered. Each parasitic has been evaluated separately and was translated into an equivalent fault location error, so that the associated design constraint could be derived. In conclusion, this analysis has shown that both presented approaches could be implemented while ensuring the targeted processing speed and resolution with realistic design constraints. However, the SC approach was preferred for integration since it is generally less impacted by analog parasitics and avoids the element mismatches and associated time calibration of the LC model.

After the successful fault location results obtained with the SC line's silicon implementation presented in Chapter 7, various improvements of the line model were evaluated. Chapter 8 has presented an alternative implementation and possible extensions of the line model to more complex network topologies. A discrete-time line with quantified magnitude was introduced. Despite an additional error caused by the quantization, it has been shown that adding modelling constraints at a high level of abstraction allows very simple implementations with their associated advantages. Indeed, a fully digital implementation, avoiding many of the parasitics linked to analog circuits, and providing higher processing speeds for smaller silicon areas, is possible. Afterwards, the extension of the single phase line model to complex topologies has been studied. Although the simulation of interconnected or multi-conductor lines seems more straightforward with a lumped LC model, which is closer to the physical representation of the line, the resulting implementation and associated time calibration can become very complex. On the other hand, the discrete-time model, based on a mathematical representation of the line's behavior, doesn't allow simple model transformations to simulate complex network topologies. In the case of simulation of multi-conductor lines, it requires a modal transformation of the system, which increases the model's complexity but remains simply implementable with digital circuits. Regarding the complexity of the multi-conductor modelling and the associated programmability required to configure the fault location emulator, the digital implementation of the discrete-time model seems more appropriate than any analog alternative.

This research has shown that hardware solutions are able to implement the EMTR-based power network fault location method. Besides an extensive development cost, dedicated emulation methods can provide much faster processing results than classical digital solutions for a similar accuracy. This significant speed improvement is essential, potentially allowing real-time fault management in power grids. However, programmability, especially for the simulation of complex networks, remains a weak point of the hardware model, as opposed to the aptly-named digitally programmable solutions. Nevertheless, this research has shown that hybrid solutions emulating the network through dedicated hardware platforms implemented digitally could be an adequate compromise.

Lausanne, May 29, 2017

François GAUGAZ

# A Fault Signature Characterization

## A.1 Duration of the Fault Signature

In this section, the duration of a fault signature occurring in a single faulted line (Fig. 2.3) is calculated. The fault impedance is considered much smaller than the line surge impedance ($\rho_f \simeq -1$) so that the network can be treated as two independent line sections delimited by the boundary and the fault location. Consequently, the considered line section is terminated by the reflection coefficients $\rho_L$ and $\rho_f$ at the load and fault side respectively, and has a propagation time of $T_p$. At each forward and reverse propagation cycle of the wave into the line, the signal is successively weighted by a factor $\rho_L\rho_f$, so that the fault signature as a function of the time $t$ is given by

$$v_s(t) = V(\rho_L\rho_f)^{\left\lceil \frac{t}{2T_p} \right\rceil}, \tag{A.1}$$

where $V$ is the fault voltage drop amplitude. Since the fault signature has an exponential envelope, it can be written

$$\left| \frac{v_s(t)}{V} \right| = |\rho_L\rho_f|^{\left\lceil \frac{t}{2T_p} \right\rceil} = e^{-\left\lceil \frac{t}{\tau} \right\rceil}. \tag{A.2}$$

Consequently, the fault signature duration can be estimated as $T_s = 5\tau$, where $\tau$ is the exponential envelope time constant. Then from (A.2), it yields

$$|\rho_L\rho_f|^{\left\lceil \frac{T_s}{2T_p} \right\rceil} = e^{-5}. \tag{A.3}$$

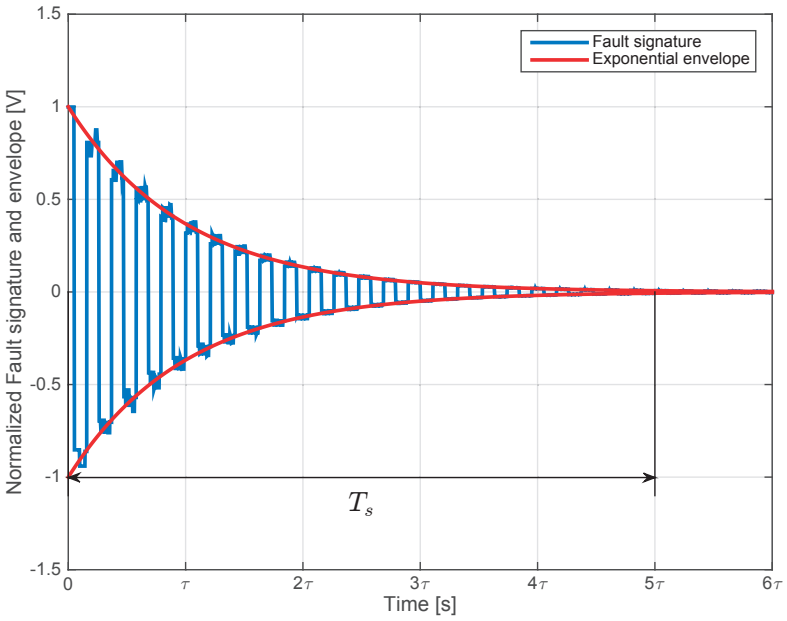


Figure A.1: Fault signature and its exponential envelope.

And finally, the fault signature duration is obtained as

$$T_s = -10\frac{T_p}{ln|\rho_L\rho_f|}. \tag{A.4}$$

# B Transmission Line Models Calculations

## B.1 LC Line Transfer Function

The transfer function of the LC line model displayed in Fig. 3.3-(C) is calculated in this appendix. As a simplification, the fault impedance is considered of much lower value than the line surge impedance, so that the line section beyond the fault can be neglected. Consequently, the transfer function is calculated from the line input voltage source to the fault impedance voltage, considering a series of a number $N$ of PI cells constituted of an inductor $\Delta L$ bounded by two capacitors of $\Delta C/2$. Such complex transfer function is calculated through the chain (or ABCD) matrix combination of each inductor and capacitor element [51], then converted to scattering parameter, from which the transfer function is deduced. Given that the series impedance $Z = j\omega\Delta L$ and shunt conductance $Y = j\omega\Delta C$, with equivalent schematic exposed in Fig. B.1, are characterized by the chain matrices

$$A_Z = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}, \quad A_Y = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}, \tag{B.1}$$

the resulting PI cell matrix composed by a series impedance $Z$ surrounded by two shunt conductances $Y/2$, as shown in the lower schematic of Fig. B.1, yields

$$\begin{aligned} A_{PI} &= A_{\frac{Y}{2}} A_Z A_{\frac{Y}{2}} = \begin{bmatrix} 1 & 0 \\ \frac{Y}{2} & 1 \end{bmatrix} \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{Y}{2} & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1+\dfrac{ZY}{2} & Z \\ \dfrac{Y}{4}(4+ZY) & 1+\dfrac{ZY}{2} \end{bmatrix}. \end{aligned} \tag{B.2}$$

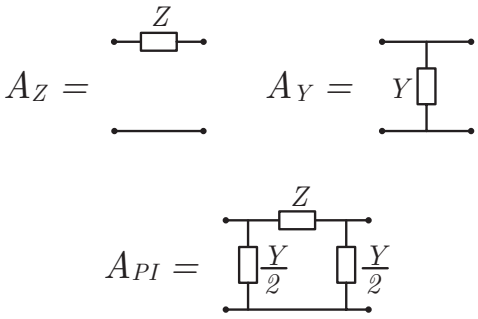


Figure B.1: ABCD matrices schematics of a series impedance $A_Z$, shunt conductance $A_Y$ and PI cell $A_{PI}$.

Considering that the line surge impedance, and respectively the line phase constant [48] are given by

$$Z_c = \sqrt{\frac{Z}{Y}} \tag{B.3}$$

$$\gamma = \sqrt{ZY}, \tag{B.4}$$

it can be deduced that

$$Z = Z_c\gamma \tag{B.5}$$

$$Y = \frac{\gamma}{Z_c}. \tag{B.6}$$

Hence, matrix (B.2) becomes

$$A_{PI} = \begin{bmatrix} \frac{2+\gamma^2}{2} & Z_c\gamma \\ \frac{\gamma(4+\gamma^2)}{4Z_c} & \frac{2+\gamma^2}{2} \end{bmatrix}. \tag{B.7}$$

Then the total line ABCD matrix of a series of $N$ PI elements is equal to the $N^{th}$ power of the matrix $A_{PI}$ so that

$$A_{NPI} = A_{PI}^{N} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}. \tag{B.8}$$

From the chain matrix of the line, composed of a series of $N$ PI cells in (B.8), can be derived the scattering parameter $S_{21}$, according to the source and load impedance, $Z_1$ and $Z_2$ respectively [49], so that

$$S_{21} = \frac{2\sqrt{Z_1 Z_2}}{A_{11}Z_2 + A_{12} + A_{21}Z_1 Z_2 + A_{22}Z_1} \tag{B.9}$$

And finally, from (B.9) and [50], the transfer function of the LC line of $N$ PI cells yields

$$H_{PI}(j\omega) = \frac{S_{21}}{2}\sqrt{\frac{Z_2}{Z_1}}. \tag{B.10}$$

Since the line is lossless, the parameter $\alpha$ of the phase constant is null, so that

$$\gamma \longrightarrow j\beta. \tag{B.11}$$

Hence, (B.10), valid for $\beta \leq 2$, becomes

$$H_{PI}\left(j\omega\right) = \frac{2^{2+N}\frac{Z_2}{Z_c}\sqrt{4-\beta^2}}{\left(4+\frac{Z_1 Z_2}{Z_c^2}\left(4-\beta^2\right)\right)\left(W^N-(W^*)^N\right)+2\frac{Z_1+Z_2}{Z_c}\sqrt{4-\beta^2}\left(W^N+(W^*)^N\right)} \tag{B.12a}$$

$$W = 2-\beta^2+j\beta\sqrt{4-\beta^2}. \tag{B.12b}$$

With

$$\begin{cases} W^N-(W^*)^N = |W|^N\left(e^{jN\angle W}-e^{-jN\angle W}\right) = 2j|W|^N sin\left(jN\angle W\right) \\ W^N+(W^*)^N = |W|^N\left(e^{jN\angle W}+e^{-jN\angle W}\right) = 2j|W|^N cos\left(jN\angle W\right), \end{cases} \tag{B.13}$$

and from (2.6)

$$Z_k = Z_c\frac{1+\rho_k}{1-\rho_k}, \tag{B.14}$$

the LC line of $N$ elements transfer function (B.12) finally yields

$$H_{LC}(j\omega, N) = \frac{1}{a_0 cos(NX) + j a_1 sin(NX)} \tag{B.15a}$$

$$a_0 = 2\frac{1-\rho_L\rho_f}{(1-\rho_L)(1+\rho_f)} \tag{B.15b}$$

$$a_1 = \frac{1-\rho_f}{1+\rho_f}\frac{2}{\sqrt{4-\Delta\beta^2}} + \frac{1+\rho_L}{1-\rho_L}\frac{\sqrt{4-\Delta\beta^2}}{2} \tag{B.15c}$$

$$X = \angle W = Arctan\left(\frac{\Delta\beta\sqrt{4-\Delta\beta^2}}{2-\Delta\beta^2}\right) \tag{B.15d}$$

$$\Delta\beta = \omega\sqrt{\Delta L \Delta C}, \tag{B.15e}$$

where $\rho_L = \rho_1$, $\rho_f = \rho_2$ and $\Delta\beta = \beta$ according to the notation and schematic in Fig. 3.3-(C).

## B.2 LC Line Model Fault Location Error

The distortion caused by the lumped LC line model discretization $N$ can be evaluated by matching the first maximum of the ideal line frequency response (3.8) with that of the LC model (B.15). Both responses are displayed in Fig. 3.4. Since analysis in Section 2.3.3 have shown that the maxima location is independent of the reflection coefficient values, as a simplification, it can be assumed that $\rho_L \to 1$ and $\rho_f \to -1$, which means that the load and fault impedances are respectively infinite and null. Consequently, the response magnitude of the distributed parameters line definition of length $D$ given by (3.8) yields

$$\left|H_L\left(j\omega, D\right)\right|_{\substack{\rho_L \to 1 \\ \rho_f \to -1}} \propto \frac{1}{\left|cos\left(\beta D\right)\right|} \tag{B.16a}$$

$$\beta = \omega\sqrt{L'C'}. \tag{B.16b}$$

similarly, the LC line model response magnitude given by (B.15) becomes

$$\left|H_{LC}(j\omega,N)\right|_{\substack{\rho_L\to 1\\ \rho_f\to -1}} \propto \frac{1}{|cos(XN)|} \tag{B.17a}$$

$$X = Arctan\left(\frac{\Delta\beta\sqrt{4-\Delta\beta^2}}{2-\Delta\beta^2}\right) \tag{B.17b}$$

$$\Delta\beta = \omega\sqrt{\Delta L\Delta C}. \tag{B.17c}$$

Both functions (B.16)-(B.17) maxima occur respectively when

$$\begin{cases} \beta_k D &= \dfrac{\pi}{2} + k\pi \\ X_k N &= \dfrac{\pi}{2} + k\pi, \end{cases} \tag{B.18}$$

where $k$ is an integer. By combining (B.18) with (B.16b), (B.17b) and (B.17c), the resonance pulsations of the distributed parameters and LC line are given by

$$\begin{cases} \omega_{L_k} &= \dfrac{\pi(1+2k)}{2D\sqrt{L'C'}} \\ \omega_{LC_k} &= \sqrt{\dfrac{2}{\Delta L\Delta C}}\cdot\sqrt{1\pm cos\left(\dfrac{\pi(1+2k)}{2N}\right)}, \end{cases} \tag{B.19}$$

and the first resonance pulsation for $k = 0$ yields then

$$\begin{cases} \omega_{L_0} &= \dfrac{2}{\sqrt{L'C'}}\cdot\dfrac{\pi}{4D} \\ \omega_{LC_0} &= \dfrac{2}{\sqrt{\Delta L\Delta C}}\cdot sin\left(\dfrac{\pi}{4N}\right). \end{cases} \tag{B.20}$$

In order to find the equivalent length $D_{eq}$ of the LC line constituted of $N$ PI cells, both resonance pulsations are equalized while $D \to D_{eq}$ so that

$$D_{eq} = \frac{\pi}{4}\cdot\sqrt{\frac{\Delta L\Delta C}{L'C'}}\cdot\frac{1}{sin\left(\frac{\pi}{4N}.\right)} \tag{B.21}$$

Since $\Delta L = L'\Delta D$ and $\Delta C = C'\Delta D$, the discrete equivalent line length $N_{eq}$ of a line of $N$ elements is obtained through (B.21), so that

$$N_{eq} = \frac{D_{eq}}{\Delta D} = \frac{\frac{\pi}{4}}{sin\left(\frac{\pi}{4N}\right)}. \tag{B.22}$$

From this result can be computed the fault location error according to the guessed fault tap $n_f$ referred to the full line of length $N$. To do so, $N \rightarrow n_f$ and $N_{eq} \rightarrow n_{f_{eq}}$, so that (B.22) becomes

$$\begin{aligned} \delta_{x_f}(n_f) &= \frac{1}{N} \cdot \frac{n_{f_{eq}} - n_f}{n_f} \\ &= \frac{1}{N}\left(\frac{\frac{\pi}{4n_f}}{sin\left(\frac{\pi}{4n_f}\right)} - 1\right). \end{aligned} \tag{B.23}$$

## B.3 LC Line Statistical Fault Location Error

This section computes the fault location error due to the emulated line parameters statistical variation. The line is considered as a series combination of $N$ line sections of equivalent propagation time $\Delta T$ and associated relative error $\delta_n$, defined by its standard deviation $\sigma_{\Delta T}$. Each $n^{th}$ line section is then characterized by its propagation time given by

$$\Delta T_n = (1+\delta_n)\Delta T. \tag{B.24}$$

Considering the calibrated line propagation time set by

$$T_{cal} = N\Delta T, \tag{B.25}$$

the time from the line input to the fault tap $n_f$ after calibration is given by the cumulated time to the fault over the total line propagation time ratio normalized by $T_{cal}$. With (B.24-B.25) it yields

$$T_{n_f} = T_{cal} \cdot \frac{\sum_{i=1}^{n_f} \Delta T_i}{\sum_{j=1}^{N} \Delta T_j} = N\Delta T \cdot \frac{\sum_{i=1}^{n_f} (1+\delta_i)}{\sum_{j=1}^{N} \left(1+\delta_j\right)}. \tag{B.26}$$

The standard deviation of the cumulated time to the fault tap after calibration is then obtained through

$$\sigma\left(T_{n_f}\right) = N\Delta T \cdot \sigma\left(\frac{n_f + \sum_{i=1}^{n_f} \delta_i}{N + \sum_{j=1}^{N} \delta_j}\right). \tag{B.27}$$

Without loss of generality, an offset of $-n_f/N$ can be added in (B.27) so that

$$\begin{aligned}
\sigma\left(T_{n_f}\right) &= N\Delta T\cdot\sigma\left(\frac{n_f+\sum_{i=1}^{n_f}\delta_i}{N+\sum_{j=1}^{N}\delta_j}-\frac{n_f}{N}\right).\\
&= N\Delta T\cdot\sigma\left(\frac{N\left(n_f+\sum_{i=1}^{n_f}\delta_i\right)-n_f\left(N+\sum_{j=1}^{N}\delta_j\right)}{N\left(N+\sum_{j=1}^{N}\delta_j\right)}\right)\\
&\simeq \frac{\Delta T}{N}\cdot\sigma\left(N\sum_{i=1}^{n_f}\delta_i-n_f\sum_{j=1}^{N}\delta_j\right)\\
&\simeq \frac{\Delta T}{N}\cdot\sigma\left(\left(N-n_f\right)\sum_{i=1}^{n_f}\delta_i-n_f\sum_{j=n_f+1}^{N}\delta_j\right).
\end{aligned}\tag{B.28}$$

And since both variables of the sums are uncorrelated, equation (B.28) becomes

$$\sigma\left(T_{n_f}\right) \simeq \frac{\Delta T}{N}\cdot\left(\left(N-n_f\right)\cdot\sigma\left(\sum_{i=1}^{n_f}\delta_i\right)-n_f\cdot\sigma\left(\sum_{j=n_f+1}^{N}\delta_j\right)\right)\tag{B.29}$$

Since the standard deviation of an error sum characterized by the same distribution $\sigma$ yields

$$\sigma\left(\sum_{i=1}^{K}\delta_i\right) = \sigma\sqrt{K},\tag{B.30}$$

quation (B.29) gives

$$\sigma\left(T_{n_f}\right) \simeq \sigma_{\Delta T}\Delta T\cdot\frac{\left(N-n_f\right)\sqrt{n_f}-n_f\sqrt{N-n_f}}{N}.\tag{B.31}$$

And finally, the standard deviation of the fault location error according to the fault location $n_f$ yields

$$\sigma\left(\frac{n_f}{N}\right) \simeq \frac{\sigma(\Delta T)}{T} \cdot \frac{\left(N-n_f\right)\sqrt{n_f} - n_f\sqrt{N-n_f}}{N}. \tag{B.32}$$

## B.4 Discrete-Time Model Fault Reflection and Transmission Coefficient Calculation

As shown in Fig. 3.7, the fault on a line can be substituted by an equivalent reflection $\rho_r$ and transmission coefficient $\rho_t$ according to the travelling incident and reflected waves description. Referring to a fault and a line surge impedance $Z_f$ and $Z_c$ respectively, a corresponding fault reflection coefficient is obtained through

$$\rho_s = \frac{Z_s - Z_l}{Z_s + Z_l}, \tag{B.33}$$

where $Z_s$ is the impedance on the source side and $Z_l$ on the load side. At the fault location, the incident wave travels from the line to toward the fault, symbolized by a fault impedance in parallel with the rest of the line. In this case, $Z_s \rightarrow Z_c$ and $Z_l \rightarrow Z_c // Z_f$ so that the equivalent reflection coefficient yields

$$\rho_r = \frac{Z_c - Z_c // Z_f}{Z_c + Z_c // Z_f} = -\frac{1}{2\dfrac{Z_f}{Z_c} + 1}. \tag{B.34}$$

Since the system is lossless, the non-reflected fraction of the signal is transmitted to the following line section so that the transmission coefficient yields

$$\rho_t = 1 + \rho_r. \tag{B.35}$$

And according to the fault coefficient calculated as

$$\rho_f = \frac{Z_f - Z_c}{Z_f + Z_c}, \tag{B.36}$$

and through

$$\frac{Z_k}{Z_c} = \frac{1+\rho_k}{1-\rho_k}, \tag{B.37}$$

calculated with (B.33), the transmission coefficient as a function of the fault coefficient $\rho_f$ from (B.34) gives

$$\rho_t = 2\frac{\rho_f+1}{\rho_f+3}. \tag{B.38}$$

Consequently, with (B.35), the reflection coefficient gives

$$\rho_r = \frac{\rho_f-1}{\rho_f+3}. \tag{B.39}$$

# C Discrete-Time EMTR Analytical Calculations

## C.1 Discrete-Time Fault Signal Energy Analytical Calculation

This section describes the analytical computation of the fault signal energy maximum that occurs when the discrete fault location equals the guessed fault one, so that $n_f = n'_f$. As a simplification hypothesis, the fault impedance is taken to be of much lower value than the line surge impedance, so that the line section beyond the fault can be neglected. According to the fault current calculated in (2.12), the discrete-time fault signal after back-propagation of the time-reversed fault signature into the emulated line can be obtained through

$$v_{EMTR}[k] = \underbrace{v_f[-k] * h_f[-k]}_{v_{sig}[-k]} * h'_f[k], \tag{C.1}$$

where $v_{sig}[k]$ is the fault signature obtained by the convolution between the fault voltage $v_f[k]$ and the faulted line response $h_f[k]$, and $h'_f[k]$ is the emulated line impulse response. The faulted and emulated line discrete-time impulse responses can be obtained through the inverse Fourier transform [78] of the corresponding line transfer functions defined in (2.13a) and (2.13b). These responses yield

$$h_f[k] = \begin{cases} \frac{(1-\rho_f)(1+\rho_L)}{2} \cdot \left(\rho_L \rho_f\right)^{\frac{k}{2n_f}} & \forall \frac{k}{2n_f} \in \mathbb{N} \\ 0 & \text{otherwise,} \end{cases} \tag{C.2}$$

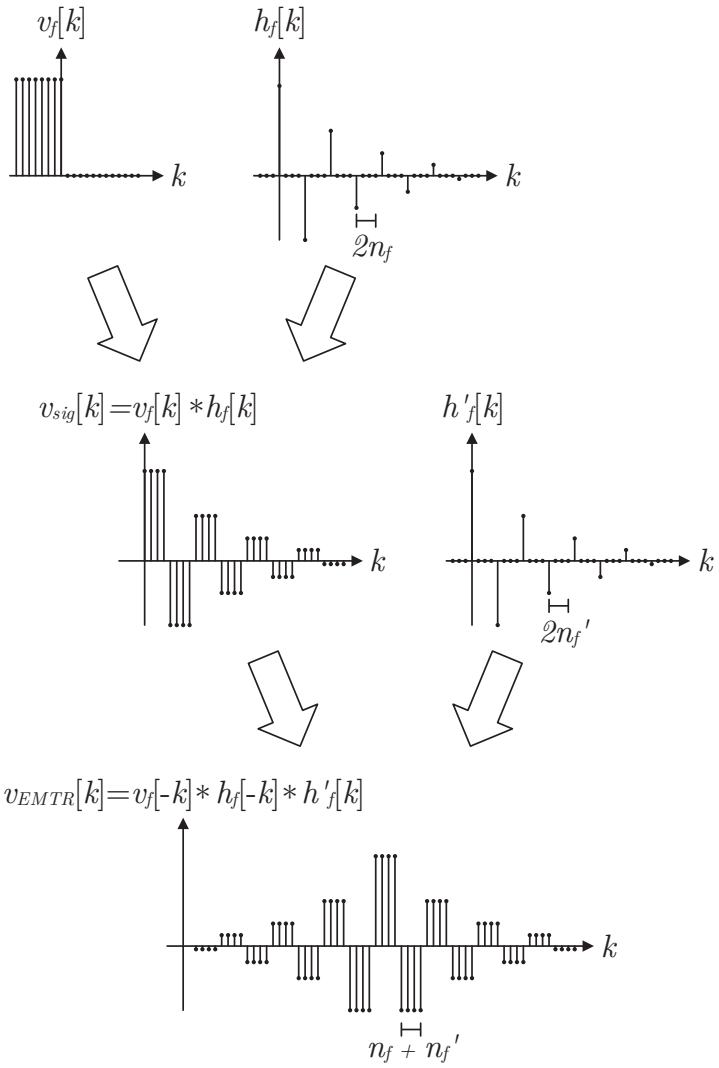


Figure C.1: Discrete-time fault signal graphical calculation illustrated for $n_f = n'_f = 2$.

and

$$h'_f[k] = \begin{cases} \frac{(1-\rho_L)(1+\rho_f)}{2} \cdot \left(\rho_L \rho_f\right)^{\frac{k}{2n'_f}} & \forall \frac{k}{2n'_f} \in \mathbb{N} \\ 0 & \text{otherwise,} \end{cases} \tag{C.3}$$

where $\rho_L$ denotes the load reflection coefficient at the line input and $\rho_f$, the fault one, at the line output. As shown by their corresponding plots in Fig. C.1, both responses correspond to alternate exponentially decreasing impulses spaced by $2n_f$ and $2n'_f$, referring to the faulted, respectively, emulated line. According to the signal processing theory [78] and (C.1), the fault

signature is given by the discrete-time convolution product between the fault voltage and the faulted line response so that

$$v_{sig}[k] = v_f[k] * h_f[k] = \sum_{m=-\infty}^{\infty} v_f[k-m] \cdot h_f[m]. \tag{C.4}$$

Since $v_f[k]$ is a down to zero voltage step, symbolizing the voltage drop after the short on the power line, with (C.2), the result in (C.4) becomes

$$\begin{aligned} v_{sig}[k] &= \frac{(1-\rho_f)(1+\rho_L)}{2} \cdot \sum_{m=\frac{k}{2n_f}}^{\infty} (\rho_L \rho_f)^m \\ &= \frac{(1-\rho_f)(1+\rho_L)}{2} \cdot \frac{(\rho_L \rho_f)^{\frac{k}{2nf}}}{1-\rho_L \rho_f}, \end{aligned} \tag{C.5}$$

for $\frac{k}{2n_f} \in \mathbb{N}$. From (C.5), the fault signature defined as

$$v_{sig}[k] = \begin{cases} \frac{(1-\rho_f)(1+\rho_L)}{2} \cdot \frac{(\rho_L \rho_f)^{\frac{k}{2nf}}}{1-\rho_L \rho_f} & \forall \frac{k}{2n_f} \in \mathbb{N} \\ 0 & \text{otherwise.} \end{cases} \tag{C.6}$$

According to (C.1), the fault signal is obtained by the discrete-time cross-correlation [78] between the fault signature and the emulated line response given by

$$v_{EMTR}[k] = v_{sig}[-k] * h'_f[k] = \sum_{m=-\infty}^{\infty} v_{sig}[k+m] \cdot h'_f[m]. \tag{C.7}$$

With (C.3) and (C.6), considering that $n_f = n'_f$, last equation can be partially calculated for $\frac{k}{2n_f} \in \mathbb{N}$, and gives

$$\begin{aligned} v_{EMTR}[k] &= \frac{\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)}{4} \cdot \frac{1}{1-\rho_L\rho_f} \cdot \sum_{m=2n_f i}^{\infty} \left(\rho_L\rho_f\right)^{\frac{k+m}{2nf}} \cdot \left(\rho_L\rho_f\right)^{\frac{m}{2nf}} \\ &= \frac{\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)}{4} \cdot \frac{\left(\rho_L\rho_f\right)^{\frac{k}{2nf}}}{1-\rho_L\rho_f} \cdot \sum_{i=0}^{\infty} \left(\rho_L\rho_f\right)^{2i} \\ &= \frac{\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)}{4} \cdot \frac{\left(\rho_L\rho_f\right)^{\frac{k}{2nf}}}{\left(1-\rho_L\rho_f\right)\cdot\left(1-\left(\rho_L\rho_f\right)^2\right)}. \end{aligned} \tag{C.8}$$

Consequently, with (C.8), the total fault signal can be defined as

$$v_{EMTR}[k] = \frac{\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)}{4} \cdot \frac{\left(\rho_L\rho_f\right)^{\left|\left\lfloor\frac{k}{2nf}\right\rfloor\right|}}{\left(1-\rho_L\rho_f\right)\cdot\left(1-\left(\rho_L\rho_f\right)^2\right)}, \tag{C.9}$$

for $k \in \mathbb{Z}$. Since $v_{EMTR}[k]$ is symmetric around $k = 0$, the computation of its energy [78] simplifies to

$$W_{EMTR} = \sum_{k=-\infty}^{\infty} v_{EMTR}[k]^2 = 2 \cdot \sum_{k=0}^{\infty} v_{EMTR}[k]^2 - v_{EMTR}[0]^2. \tag{C.10}$$

According to the graph of signal $v_{EMTR}[k]$ in Fig. C.1 and equation (C.10), the fault voltage energy can be written as

$$\begin{aligned} W_{EMTR} &= \left(\frac{\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)}{4}\cdot\frac{1}{\left(1-\rho_L\rho_f\right)\cdot\left(1-\left(\rho_L\rho_f\right)^2\right)}\right)^2\cdot 2n_f\cdot\left[2\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^{2k}-1\right] \\ &= \left(\frac{\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)}{4}\cdot\frac{1}{\left(1-\rho_L\rho_f\right)\cdot\left(1-\left(\rho_L\rho_f\right)^2\right)}\right)^2\cdot 2n_f\cdot\left[\frac{2}{1-\left(\rho_L\rho_f\right)^2}-1\right] \\ &= 2n_f\cdot\left(\frac{\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)}{4}\cdot\frac{1}{\left(1-\rho_L\rho_f\right)\cdot\left(1-\left(\rho_L\rho_f\right)^2\right)}\right)^2\cdot\frac{1+\left(\rho_L\rho_f\right)^2}{1-\left(\rho_L\rho_f\right)^2} \\ &= \frac{n_f}{8}\cdot\left(\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)\right)^2\cdot\frac{1+\left(\rho_L\rho_f\right)^2}{\left(1-\rho_L\rho_f\right)^2\cdot\left(1-\left(\rho_L\rho_f\right)^2\right)^3} \end{aligned} \tag{C.11}$$

And assuming that $\rho_L=-\rho_f=\rho$, (C.11) simplifies to

$$\begin{aligned} W_{EMTR} &\simeq \frac{n_f}{8}\cdot\left(1-\rho^2\right)^4\cdot\frac{1+\rho^4}{\left(1+\rho^2\right)^2\cdot\left(1-\rho^4\right)^3} \\ &\simeq \frac{n_f}{8}\cdot\frac{\left(1-\rho^2\right)\cdot\left(1+\rho^4\right)}{\left(1+\rho^2\right)^5}, \end{aligned} \tag{C.12}$$

and in first order approximation for $\rho$ close to 1, it yields

$$W_{EMTR} \simeq \frac{n_f\cdot\left(1-\rho\right)}{64}. \tag{C.13}$$

This final result shows that the fault location result energy maximum varies linearly with the discrete fault location $n_f$ and decreases when the reflection coefficients magnitude increase. High magnitude reflection coefficients occur when the input impedance is high and the output one is low referring to the line surge impedance. Consequently, the signal back-propagated from the line input and observed at its output is of minimum magnitude.

### C.1.1 Fault Signal Energy Measured at tap $V_0^-$

Section 6.5 explained that for simplification reasons, the fault location isn't realized through the fault current energy evaluation, but through the energy of the equivalent signal at the last backward propagation path tap $V_0^-$. Since the voltage at tap $n_f$ is the sum of forward and

backward propagated waves so that

$$V_{n_f} = V_{n_f}^{+} + V_{n_f}^{-} = V_{n_f}^{-} \cdot \frac{1+\rho_f}{\rho_f}, \tag{C.14}$$

where $V_{n_f}^{-} = \rho_f V_{n_f}^{+}$, it can be written

$$V_{n_f}^{-} = V_{n_f} \cdot \frac{\rho_f}{1+\rho_f}. \tag{C.15}$$

And since the wave at the backward propagation path input and at the fault are the same signal simply delayed by $n_f/2$, so that $V_0^{-}[k] = V_{n_f}^{-}[k - n_f/2]$ and that $V_{EMTR} = V_{n_f}$, with (C.15), it can be written

$$V_0^{-}[k] = \frac{\rho_f}{1+\rho_f} \cdot V_{EMTR}[k - n_f/2]. \tag{C.16}$$

With (C.10), the energy of signal $V_0^{-}$ after back-propagation of the time reversed fault signature becomes

$$\begin{aligned} W_{EMTR_0^{-}} &= \left(\frac{\rho_f}{1+\rho_f}\right)^2 \cdot W_{EMTR} \\ &= \frac{n_f}{8} \cdot \left(\frac{\rho_f}{1+\rho_f}\right)^2 \cdot \left(\left(1-\rho_f^2\right)\left(1-\rho_L^2\right)\right)^2 \cdot \frac{1+\left(\rho_L\rho_f\right)^2}{\left(1-\rho_L\rho_f\right)^2 \cdot \left(1-\left(\rho_L\rho_f\right)^2\right)^3} \\ &= \frac{n_f}{8} \cdot \rho_f^2 \cdot \frac{\left(1-\rho_f\right)^2 \cdot \left(1-\rho_L^2\right)^2 \cdot \left(1+\left(\rho_L\rho_f\right)^2\right)}{\left(1-\rho_L\rho_f\right)^2 \cdot \left(1-\left(\rho_L\rho_f\right)^2\right)^3}, \end{aligned} \tag{C.17}$$

and assuming that $\rho_L = -\rho_f = \rho$, (C.17) simplifies to

$$\begin{aligned} W_{EMTR_0^{-}} &\simeq \frac{n_f}{8} \cdot \rho^2 \cdot \frac{\left(1+\rho\right)^2 \cdot \left(1-\rho^2\right)^2 \cdot \left(1+\rho^4\right)}{\left(1+\rho^2\right)^2 \cdot \left(1-\rho^4\right)^3} \\ &\simeq \frac{n_f}{8} \cdot \rho^2 \cdot \frac{\left(1+\rho\right) \cdot \left(1+\rho^4\right)}{\left(1-\rho\right) \cdot \left(1+\rho^2\right)^5}. \end{aligned} \tag{C.18}$$

# D Transconductor-Capacitor Combinations

## D.1 Transconductor-Capacitor Equivalent Schematics

This section presents an equivalent gyrator-C combination that substitutes the series inductors of the LC PI cell. This conversion is demonstrated considering a general case, where a series impedance $Z$ is simulated by an equivalent transconductor-admittance circuit. For this purpose, Fig. D.1-(A) illustrates the initial series impedance $Z$, while (B) and (C) display the equivalent gyrator-Y and respectively transconductor-Y circuits, composed of identical transconductors $g_m$ and a shunt admittance $Y$. According to the schematics in (B-C) the following equations can be derived:

$$\begin{cases} I_1' &= g_m V_1 \\ I_2' &= -g_m V_2 \\ I_2 &= -I_1 = g_m V_Y \\ -\left(I_1' + I_2'\right) &= Y V_Y . \end{cases} \tag{D.1}$$

Consequently, the equivalent series impedance can be obtained as

$$Z = \frac{V_1 - V_2}{I_1} = \frac{Y}{g_m^2} \tag{D.2}$$

In the case of the series inductor of the LC line, the series impedance and shunt conductance become $Z \rightarrow j\omega\Delta L$ and $Y \rightarrow j\omega\Delta C$ respectively, so that (D.2) becomes

$$\Delta L = \frac{\Delta C}{g_m^2} \tag{D.3}$$

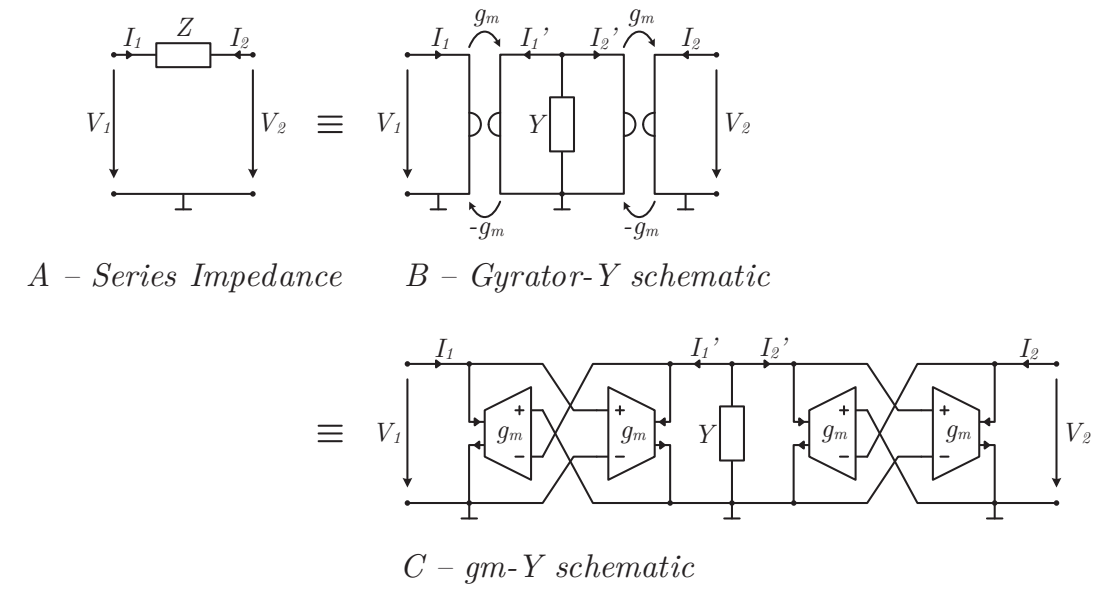


Figure D.1: Series inductor (A) and its equivalent gyrator-C schematic (B) and transconductor-C circuit (C).

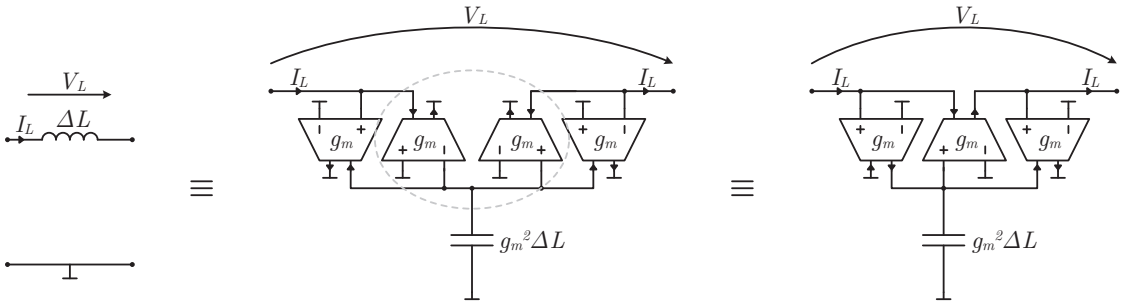


Figure D.2: Series inductor and equivalent gm-C circuit and simplified three OTA version.

and can be emulated by the circuit and its simplification illustrated in Fig. D.2, derived from Fig. D.1-(C).

# E Switched-Capacitor Line Parasitics Calculations

## E.1 Equivalent Cell Offset Propagation

This section analyses the propagation of an equivalent delay cell offset caused by the switch charge injection and clock feedthrough in the discrete-time line model illustrated in Fig. 5.1. For this purpose, each delay cell is considered with an equivalent and equal offset $V_{os}$ summed at its output. The fault on the line is considered as close to a shortcut so that from (B.39) its corresponding reflection coefficient is $\rho_f \simeq \rho_r \simeq -1$, and therefore, the line section beyond the fault can be neglected. Consequently, a line of $2N$ forward and backward propagation paths delay cells is considered with input and output reflection coefficients $\rho_L$ and $\rho_f$ respectively. The cumulated offset at the $n^{th}$ forward propagation tap $V^+_{os_n}$ can be considered as a sum of each cell offset contribution reflected along the line so that

$$\begin{aligned} V^+_{os_n} = & \underbrace{\sum_{k=0}^{\infty} V_{os}\left(\rho_L\rho_f\right)^k}_{Cell\ 1^+} + \ldots + \underbrace{\sum_{k=0}^{\infty} V_{os}\left(\rho_L\rho_f\right)^k}_{Cell\ n^+} + \\ & + \underbrace{\sum_{k=1}^{\infty} V_{os}\left(\rho_L\rho_f\right)^k}_{Cell\ (n+1)^+} + \ldots + \underbrace{\sum_{k=1}^{\infty} V_{os}\left(\rho_L\rho_f\right)^k}_{Cell\ N^+} + \\ & + \underbrace{\sum_{k=0}^{\infty} \rho_L V_{os}\left(\rho_L\rho_f\right)^k}_{Cell\ N^-} + \ldots + \underbrace{\sum_{k=0}^{\infty} \rho_L V_{os}\left(\rho_L\rho_f\right)^k}_{Cell\ 1^-}, \end{aligned} \tag{E.1}$$

which simplifies to

$$\begin{aligned}
V_{os_n}^{+} &= n\cdot\sum_{k=0}^{\infty}V_{os}\left(\rho_L\rho_f\right)^k+(N-n)\cdot\sum_{k=1}^{\infty}V_{os}\left(\rho_L\rho_f\right)^k+N\cdot\sum_{k=0}^{\infty}\rho_L V_{os}\left(\rho_L\rho_f\right)^k \\
&= N\cdot\sum_{k=0}^{\infty}V_{os}\left(\rho_L\rho_f\right)^k-(N-n)\cdot V_{os}+N\cdot\sum_{k=0}^{\infty}\rho_L V_{os}\left(\rho_L\rho_f\right)^k \\
&= V_{os}\cdot\left(N\cdot\left(1+\rho_L\right)\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^k+n-N\right) \\
&= V_{os}\cdot\left(N\cdot\left(1+\rho_L\right)\cdot\frac{1}{1-\rho_L\rho_f}+n-N\right) \\
&= V_{os}\cdot\left(N\cdot\frac{\rho_L+\rho_L\rho_f}{1-\rho_L\rho_f}+n\right). \qquad \text{(E.2)}
\end{aligned}$$

Considering $\rho_L=-\rho_f=\rho$, equation (E.2) yields then

$$V_{os_n}^{+} = V_{os}\cdot\left(N\cdot\frac{\rho-\rho^2}{1+\rho^2}+n\right), \qquad \text{(E.3)}$$

and if $\rho\simeq 1$, it can be written

$$V_{os_n}^{+} \simeq V_{os}\cdot\left(N\cdot\frac{1-\rho}{2}+n\right). \qquad \text{(E.4)}$$

Similarly, the cumulated offset at the $n^{th}$ backward propagation tap $V_{os}^{-}$ yields

$$\begin{aligned}
V_{os_n}^{-} &= N\cdot\sum_{k=0}^{\infty}\rho_f V_{os}\left(\rho_L\rho_f\right)^k+(N-n)\cdot\sum_{k=0}^{\infty}V_{os}\left(\rho_L\rho_f\right)^k+n\cdot\sum_{k=1}^{\infty}V_{os}\left(\rho_L\rho_f\right)^k \\
&= N\cdot\sum_{k=0}^{\infty}\rho_f V_{os}\left(\rho_L\rho_f\right)^k+N\cdot\sum_{k=0}^{\infty}V_{os}\left(\rho_L\rho_f\right)^k-n\cdot V_{os} \\
&= V_{os}\cdot\left(N\cdot(1+\rho_f)\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^k-n\right) \\
&= V_{os}\cdot\left(N\cdot\frac{1+\rho_f}{1-\rho_L\rho_f}-n\right) \qquad \text{(E.5)}
\end{aligned}$$

Considering $\rho_L = -\rho_f = \rho$, equation (E.5) yields then

$$V_{os_n}^{-} = V_{os} \cdot \left( N \cdot \frac{1-\rho}{1+\rho^2} - n \right), \tag{E.6}$$

and if $\rho \simeq 1$, it can be written

$$V_{os_n}^{-} \simeq V_{os} \cdot \left( N \cdot \frac{1-\rho}{2} - n \right). \tag{E.7}$$

# F Circuit Design Complement

## F.1 OTA Transistor Level Schematic

The full OTA transistor level schematic with transistor dimensions width $W$ and length $L$ is displayed in Fig. F.1. In addition to the simplified schematic in Fig. 6.3, this version details the input source follower N and PMOS with their corresponding current mirror biased by $V_{mir_N}$ and $V_{mir_P}$ respectively. A current ratio between the output and the input branch can be reasonably set from 1 to 10, to provide a sufficient OTA transconductance, while keeping a relatively low current in the input branch, adequate for the source follower transistors. The input and output branch currents are respectively set by the mirror bias $V_{mir_{N-P}}$ and cascode bias $V_{PolCas_{N-P}}$. Input Miller Poly capacitors are added in parallel to the voltage followers to limit the signal overshoot. Their value is defined through transient simulations. MOS decoupling capacitors are added on the cascode transistor biasing nodes $V_{polCas_N}$ and $V_{polCas_P}$ to avoid parasitic glitches. And finally, enable and disable MOS switches are disposed on the principal transistors gate and in series with the source followers, in order to shut down the OTA when not used.

## F.2 OTA Biasing Circuit Transistor Level Schematic

As illustrated in the full OTA biasing circuit in Fig. F.2, the OTA current is controlled by the output current sink $I_{bias}$, at the pad *IbiasOut*. According to the N and P current mirrors proportions, the full OTA current, equal to $I_{bias}$, is distributed with a ratio of $^8/_9 : ^1/_9$ between the output and input OTA branches. The OTA current mirror bias voltages $V_{mir_{N-P}}$ and cascode bias voltages $V_{PolCas_{N-P}}$ are generated with the same transistors as in the OTA, according to a width multiplication factor that sets the desired current. The cascode stage RPoly resistors are set so that the OTA output dynamic is maximized, while the cascodes source voltage allows the transistor at their source to be properly saturated.

According to the current mirror multiplicity, the biasing circuit consumption can be estimated to approximately $4I_{bias}$ on supply $V_{dd}$ and $2I_{bias}$ on supply $V_{ddAmp}$, so $6I_{bias}$ in total. The

OTA itself consumes a current of $I_{bias}$ on supply $V_{ddAmp}$.

## F.3 OTA and Biasing Circuit DC Simulations

Fig. F.3 and respectively F.4 illustrate the OTA and biasing circuit DC simulations with node voltages, transistor currents, voltages and conductances. These simulations are performed with an OTA bias current set to $I_{bias} = 54\mu A$, set by a corresponding normalized off-chip resistor of $R_{bias} = 47k\Omega$. In this configuration, the OTA supply voltage reaches $V_{ddAmp} = 2.99V$ and the voltage reference is approximately at midrange at $V_{mid} = 1.36V$.

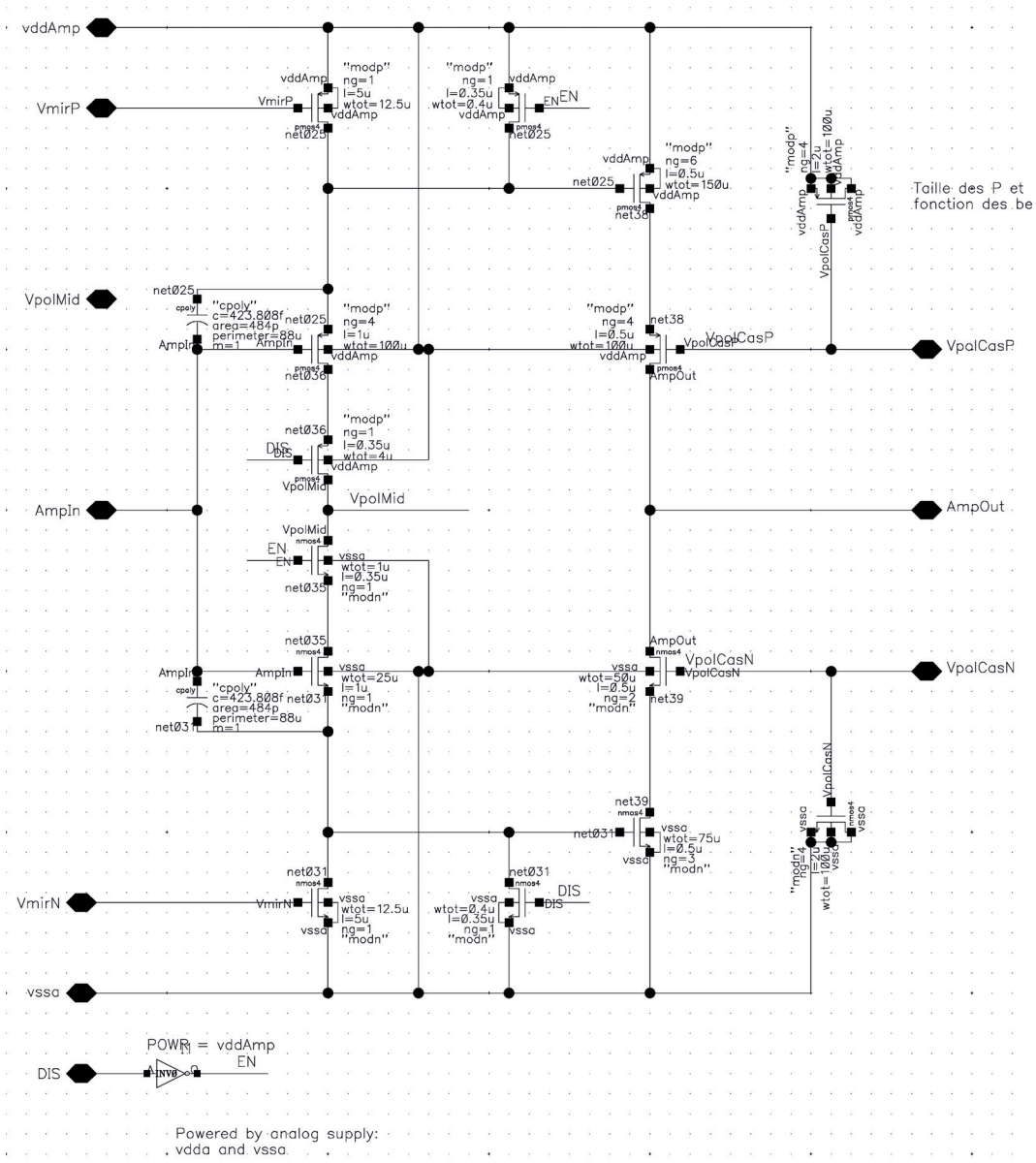


Figure F.1: OTA transistor level schematic.

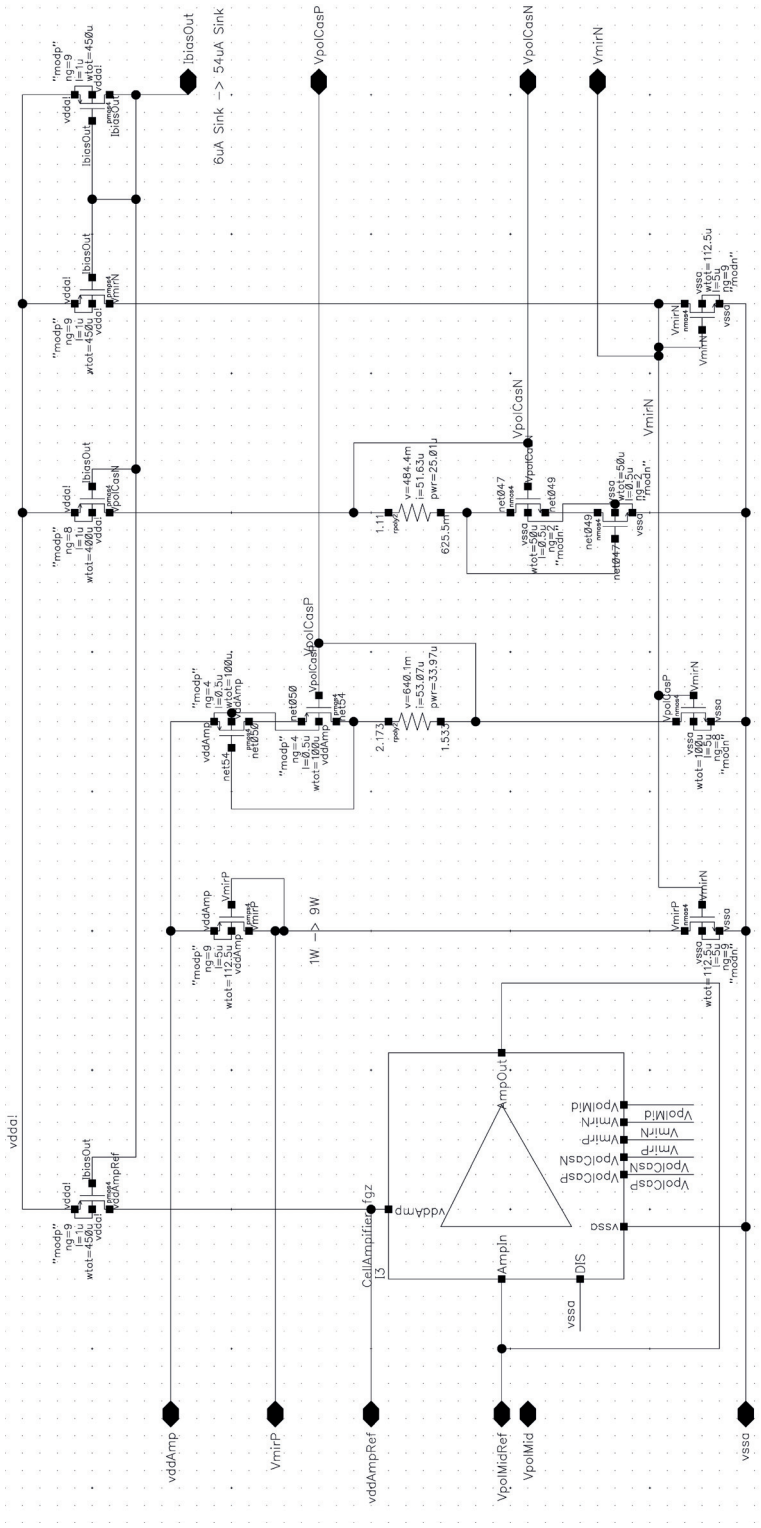


Figure F.2: Transistor level schematic of the OTA bias circuit.

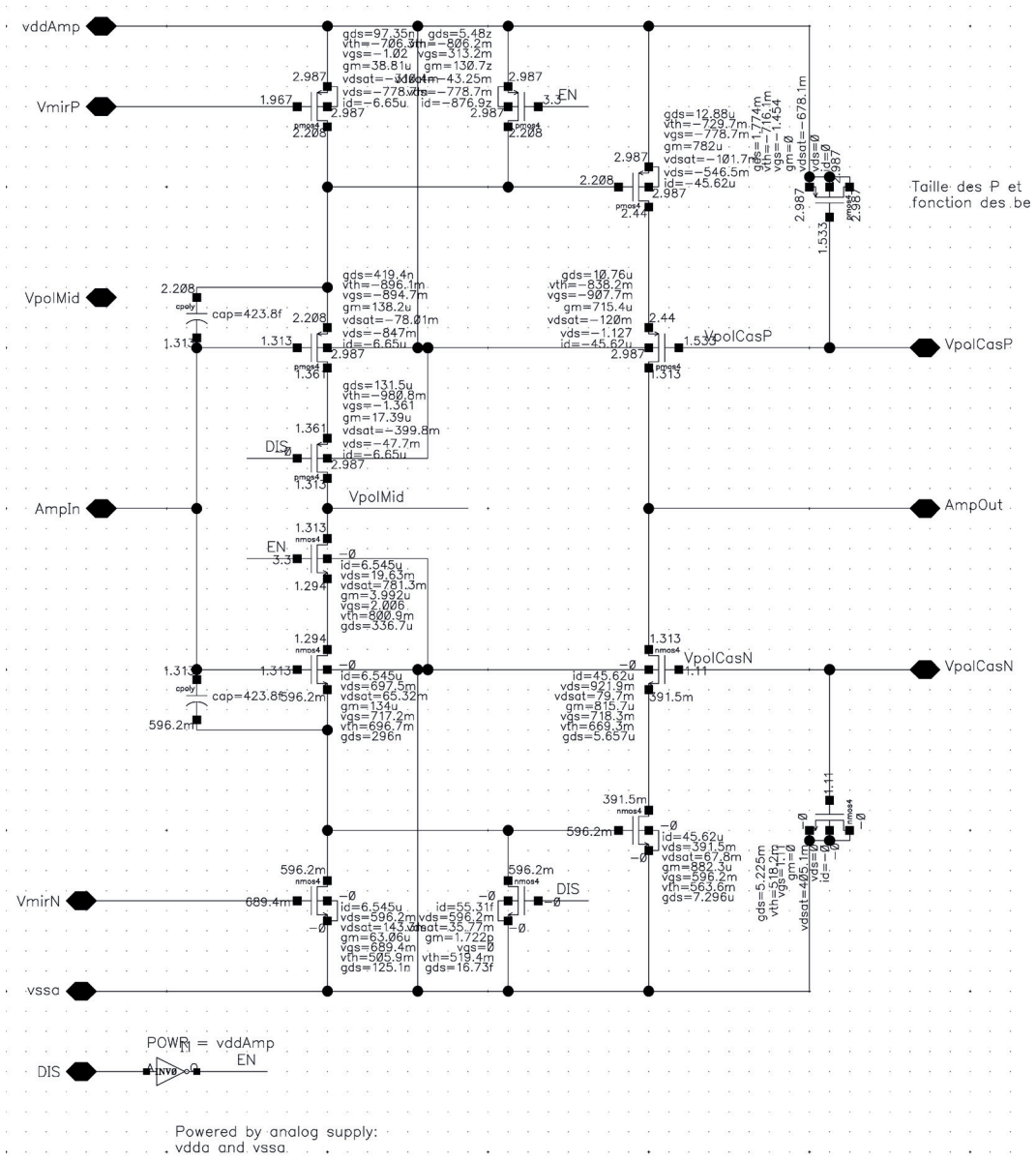


Figure F.3: OTA DC simulation.

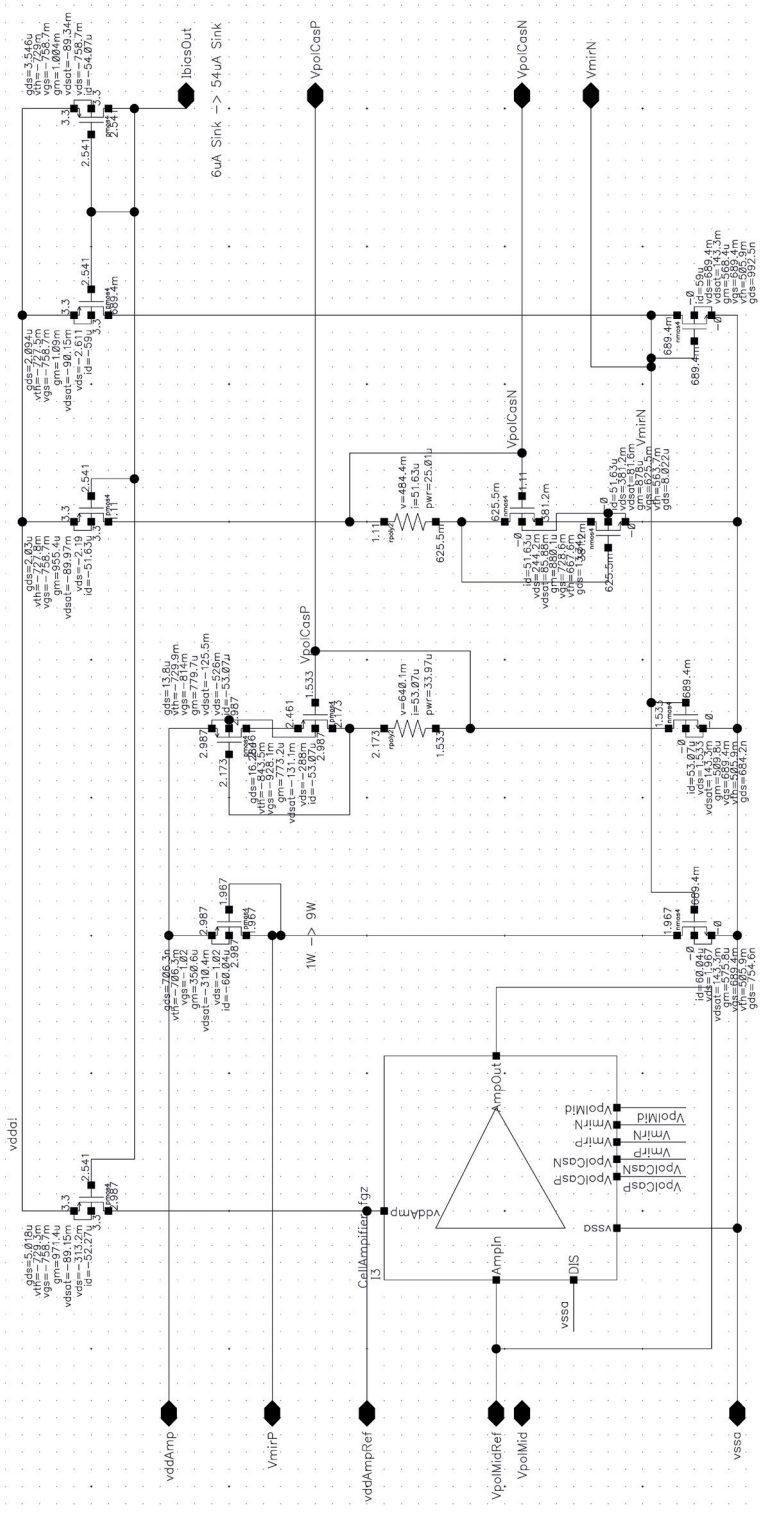


Figure F.4: OTA bias circuit DC simulation.

# G Impact of the Discrete-Time Line Model Quantization

## G.1 Digital Discrete-Time Line Model Quantization Noise

The impact of the quantization noise in the digital discrete-line model is evaluated in the frame of the fault location. This analysis is based on the discrete-time line model in Fig. 8.9, taking into account the equivalent quantization noise sources $Q_{N_0}$ to $Q_{N_3}$, placed at the circuit input and after each multiplier. As defined in [78], each noise source is characterized by the same standard deviation according to the quantification step $\Delta$. Considering the quantization error as uniform between $-\Delta/2 < e < \Delta/2$ and zero elsewhere, the probability density function [76] yields then $p_e = 1/\Delta$, since the total probability is 1:

$$1 = \int_{-\infty}^{+\infty} p_e \, de \tag{G.1}$$

$$= \int_{-\Delta/2}^{+\Delta/2} \frac{1}{\Delta} de. \tag{G.2}$$

Hence, the quantization noise variance yields

$$\sigma_{Q_N}^2 = \int_{-\infty}^{+\infty} p_e e^2 \, de \tag{G.3}$$

$$= \int_{-\Delta/2}^{+\Delta/2} \frac{1}{\Delta} \cdot e^2 \, de = \frac{\Delta^2}{12}, \tag{G.4}$$

and defines the quantization noise standard deviation as

$$\sigma_{Q_N} = \frac{\Delta}{\sqrt{12}}, \tag{G.5}$$

with a quantization step given by $\Delta = 1/2^{N_b}$, where $N_b$ is the quantization. According to the discrete-time line model in Fig. 8.9, the resulting noise from sources $Q_{N_0}$ to $Q_{N_3}$ observed at a forward propagation tap $V_n^+$ is characterized by the variance

$$\begin{aligned}
\sigma^2\left(V_n^+\right) &\overset{A}{=} \sigma^2\left(\frac{1-\rho_L}{2}\cdot\sum_{k=0}^{\infty}Q_{N_{0_k}}\left(\rho_L\rho_f\right)^k\right)+\sigma^2\left(\sum_{k=0}^{\infty}Q_{N_{1_k}}\left(\rho_L\rho_f\right)^k\right)+ \\
&+ \sigma^2\left(\sum_{k=0}^{\infty}Q_{N_{2_k}}\left(\rho_L\rho_f\right)^k\right)+\sigma^2\left(\rho_L\cdot\sum_{k=0}^{\infty}Q_{N_{3_k}}\left(\rho_L\rho_f\right)^k\right) \\
&\overset{B}{=} \sigma_{Q_N}^2\cdot\left(\frac{1-\rho_L}{2}\right)^2\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^{2k}+\sigma_{Q_N}^2\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^{2k}+ \\
&+ \sigma_{Q_N}^2\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^{2k}+\sigma_{Q_N}^2\cdot\rho_L^2\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^{2k} \\
&= \sigma_{Q_N}^2\cdot\sum_{k=0}^{\infty}\left(\rho_L\rho_f\right)^{2k}\cdot\left(\frac{1-\rho_L}{2}+2+\rho_L^2\right) \\
&= \sigma_{Q_N}^2\cdot\frac{9-2\rho_L+5\rho_L^2}{4\left(1-\left(\rho_L\rho_f\right)^2\right)},
\end{aligned} \tag{G.6}$$

where $\rho_L = \rho_i$ and $\rho_r \simeq \rho_f$, and according to the variance properties [76]

$$\begin{cases}
A \longrightarrow \sigma^2(X+Y) = \sigma^2(X)+\sigma^2(Y)+\underbrace{2Cov(X,Y)}_{0} \\
B \longrightarrow \sigma^2(aX) = a^2\sigma^2(X) \\
C \longrightarrow \sigma^2(X\cdot Y) = \sigma^2(X)\cdot\sigma^2(Y)+\overbrace{\sigma^2(X)\cdot(E(Y))^2}^{0}+\overbrace{\sigma^2(Y)\cdot(E(X))^2}^{0}
\end{cases} \tag{G.7}$$

where $X$ and $Y$ are zero mean uncorrelated variables and $a$ a constant. From (G.6), the quantization noise standard deviation observed at a forward propagation tap $V_n^+$ is

$$\sigma\left(V_n^+\right) = \frac{\sigma_{Q_N}}{2}\cdot\sqrt{\frac{9-2\rho_L+5\rho_L^2}{\left(1-\left(\rho_L\rho_f\right)^2\right)}}. \tag{G.8}$$

Assuming that $\rho_L = -\rho_f = \rho$, (G.8) simplifies to

$$\sigma\left(V_n^+\right) \simeq \frac{\sigma_{Q_N}}{2}\cdot\sqrt{\frac{9-2\rho+5\rho^2}{1-\rho^4}}. \tag{G.9}$$

Similarly, the quantization noise variance at backward propagation tap $V_n^-$ is given by

$$\begin{aligned}\sigma^2\left(V_n^-\right) &\overset{A}{=} \sigma^2\left(\frac{1-\rho_L}{2}\cdot\rho_f\cdot\sum_{k=0}^{\infty}Q_{N_{0_k}}\left(\rho_L\rho_f\right)^k\right)+\sigma^2\left(\rho_f\cdot\sum_{k=0}^{\infty}Q_{N_{1_k}}\left(\rho_L\rho_f\right)^k\right)+\\ &+ \sigma^2\left(\rho_f\cdot\sum_{k=0}^{\infty}Q_{N_{2_k}}\left(\rho_L\rho_f\right)^k\right)+\sigma^2\left(\sum_{k=0}^{\infty}Q_{N_{3_k}}\left(\rho_L\rho_f\right)^k\right)\\ &= \sigma_{Q_N}^2\cdot\frac{4+\rho_f^2\left(9-2\rho_L+\rho_L^2\right)}{4\left(1-\left(\rho_L\rho_f\right)^2\right)}\end{aligned} \tag{G.10}$$

Then, the quantization noise standard deviation observed at backward propagation tap $V_n^-$ is

$$\sigma\left(V_n^-\right) = \frac{\sigma_{Q_N}}{2}\cdot\sqrt{\frac{4+\rho_f^2\left(9-2\rho_L+\rho_L^2\right)}{\left(1-\left(\rho_L\rho_f\right)^2\right)}}. \tag{G.11}$$

Assuming that $\rho_L = -\rho_f = \rho$, (G.11) simplifies to

$$\sigma\left(V_n^-\right) \simeq \frac{\sigma_{Q_N}}{2}\cdot\sqrt{\frac{4+\rho^2\left(9-2\rho+\rho^2\right)}{1-\rho^4}}. \tag{G.12}$$

### G.1.1 Fault Signal Energy Quantization Noise

The fault signal energy is computed through the discrete-time integral of the squared value of $V_0^-$. Considering the quantization noise of the corresponding signal $v_{N_0}^-$, its energy cumulated

over $N_i$ periods yields

$$\begin{aligned}\sigma^2\left(W_{Q_N}\right) &= \sigma^2\left(\sum_{k=0}^{N_i}\left(\nu^-_{N_{0_k}}\right)^2\right)\\ &\overset{C}{=} \left(\sigma^2\left(V^-_{n=0}\right)\right)^2\cdot N_i,\end{aligned} \tag{G.13}$$

according to (G.7-C). This last result combined with (G.11) gives the equivalent quantization noise standard deviation of the energy signal:

$$\sigma\left(W_{Q_N}\right) = \frac{\sigma^2_{Q_N}}{4}\cdot\sqrt{N_i}\cdot\frac{4+\rho_f^2\left(9-2\rho_L+\rho_L^2\right)}{1-\left(\rho_L\rho_f\right)^2}. \tag{G.14}$$

Assuming that $\rho_L = -\rho_f = \rho$, (G.14) simplifies to

$$\sigma\left(W_{Q_N}\right) \simeq \frac{\sigma^2_{Q_N}}{4}\cdot\sqrt{N_i}\cdot\frac{4+\rho^2\left(9-2\rho+\rho^2\right)}{1-\rho^4}, \tag{G.15}$$

and in first order approximation for $\rho \simeq 1$, it becomes

$$\sigma\left(W_{Q_N}\right) \simeq \frac{3\sigma^2_{Q_N}}{4}\cdot\frac{\sqrt{N_i}}{1-\rho}. \tag{G.16}$$

This last result shows that the equivalent quantization noise of the energy signal increases with the number of integration cycles $N_i$ and for high magnitude reflection coefficients, in which case the noise successively cumulates and reflects at the line boundaries with a negligible attenuation.

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**PERSONAL INFORMATIONS**

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| Date of Birth : | 28th February 1986 | Nationality: | Swiss/Czech (European passport) |
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**EDUCATION**

| | |
|---|---|
| September 2008 - June 2017 | **ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE (EPFL),** Switzerland<br>**PhD:** Electronics emulation for real-time fault location in power systems, under the supervision of Prof. Kayal and Dr. Krummenacher (start in August 2013).<br>**Master in Electronics and Microelectronics Engineering** (February 2012) master project grade **6/6**<br>**Bachelor in Electronics Engineering** (Aug. 2011) with the grade **5.4/6** (final ranking **3/31**)<br>One year abroad at the **TECHNISCHE UNIVERSITAET BERLIN** (Sep. 2010-Jul. 2011) |
| September 2004 - February 2008 | **HAUTE ECOLE D'INGENIERIE ET DE GESTION DU CANTON DE VAUD (HEIG-VD),**<br>Yverdon-les-Bains, Switzerland<br>**Diploma in Electrical Engineering** (February 2008) with the grade **5.25/6** |
| August 2001 - July 2004 | **ECOLE TECHNIQUE, ECOLE DES METIERS DE LAUSANNE (ETML),** Switzerland<br>**Apprenticeship in Electronics** and **Technical Secondary School Diploma** (July 2004) |

**RESEARCH AND WORK EXPERIENCE**

| | |
|---|---|
| April 2012 - July 2013 | **Improvement of a Swiss-produced 0.18um CMOS flash non-volatile memory**<br>**EM Microelectronic** (Marin, Switzerland) and **EPFL**, in collaboration with Mr. Marinelli, the Drs. Acovic, Krummenacher, Pastre and the Prof. Kayal.<br>**Design and optimization** of functional blocks in a flash memory circuit. |
| September 2011 - February 2012 | **Smart battery management system for Ni-Zn energy packs,** (grade **6/6**)<br>Master project at EPFL under the supervision of the Drs. Krummenacher, Pastre and the Prof. Kayal.<br>Design of functional blocks of an analog integrated circuit aimed to monitor the charge/discharge of Ni-Zn energy packs. |
| February - July 2010 | **Wattmeter design,** (grade **5.5/6**)<br>Bachelor project at **EPFL** under the supervision of the Prof. Kayal<br>Development of a low-cost wattmeter for domestic uses. |
| March 2007 - January 2008 | **Eye position measuring per Electrooculography (EOG),** (grade **5.4/6**)<br>Diploma Thesis at **HEIG-VD** (Yverdon-les-Bains, Switzerland) under the supervision of the Prof. Correvon.<br>Development of a mixed-signal electronic device that measures the eyes position based on the Electrooculography principle (EOG). |
| August - October 2006 | **Measurement of the bioimpedance**<br>Summer job at **HEIG-VD** under the supervision of the Prof. Correvon.<br>Development of a biomedical electronic device for measuring the bioimpedance. |
| August - September 2003 | **Power electronics**<br>Internship with the **Bobst Group** (Mex, Switzerland).<br>Measuring electrical characteristics of AC/DC converters and building an autotransformer. |

**LIST OF PUBLICATION**

- F. Gaugaz, F. Krummenacher and M. Kayal, "High-speed analog processing for real-time fault location in electrical power networks," IEEE NEWCAS, June 2015.
- F. Gaugaz, F. Krummenacher and M. Kayal, "OTA-C based high-speed analog processing for real-time fault location in electrical power networks," Springer Analog Integrated Circuits & Signal Processing, vol. 89, no. 1, pp. 61-67, April 2016.
- F. Gaugaz, F. Krummenacher andM. Kayal, "Implementation guidelines for a real-time fault location system in electrical power networks," IEEE BEC, October 2016.
- F. Gaugaz, F. Krummenacher and M. Kayal, "Implementation of a high-speed discrete-time analog emulator for real-time fault location in electrical power networks," IEEE NEWCAS, June 2017.
- F. Gaugaz, F. Krummenacher and M. Kayal, "High-speed analog sampled-data signal processing for real-time fault location in electrical power networks," IET Circuits, Devices & Systems, to be published.

**PRIZES AND AWARDS**

- IEEE NEWCAS 2015 conference Best Student Paper Award (2nd rank)

**COMPUTER SKILLS**

| | |
|---|---|
| Development: | Cadence (Design and layout), Orcad, Spice, Matlab, HDL Designer |
| Programming: | C, Assembler, VHDL, Ada, Delphi |

**LANGUAGES**

| | |
|---|---|
| French | mother tongue |
| English | level B2, fluent |
| German | level B2, fluent (one year experience in Berlin) |
| Czech | mother tongue |

**INTERESTS**

| | |
|---|---|
| Music: | guitar, singing and piano, participating in different projects (AL STONE, etc.) |
| Sport: | Judo (black belt), skiing and swimming |