Master Project, 2017, Microtechnique Piezoelectric Nano-Balance for RNA Detection

Advanced NEMS group

Student: Christian Clerc

PhD Assistant: Andrea Lozzi

Professor: Guillermo Villanueva

03.04.2017

Table des matières

1. Introduction 5
1.2 Contour mode resonator 5
1.3 Contents of the report and major goals 6
2. First process flow 6
2.1 Process flow of the lab 6
Steps before the first mask 6
First mask 7
Second mask 7
Third mask 7
2.2 Andrea's design and results 8
3. Second Process Flow 9
3.1 Top and bottom electrodes 9
Top plate electrode 9
Bottom interdigitated electrode 9
Lift off process flow with AZ1512 resist on LOR resist 9
Lift off of sputtered platinum 9
Conclusion 15
3.2 Bring liquid on the CMR 15
Droplet on resonator tests 15
Size of the resonator comparing to the size of the droplets 16
Small droplets dry 16
Liquid is sucked on the pads 18
Contact angle studies 18
Conclusion 20
3.3 PDMS Channel 21
Process flow of PDMS channel 22
Detailed procedure to make PDMS channel and PDMS bonding 22
Fabrication of channels 23
Bonding and liquid test on different design of channel and different substrate. 26
Uncooked PDMS for symmetric channel 27
Asymmetric PDMS channel 30

Discussion ... 31
Process flow changes ... 31
3.4 Changes of the behavior of the resonator ... 32
Calculation of the loading resistance and the parasitic capacitance ... 32
Change of the C_0 capacitance ... 34
Change of R_L Resistance ... 36
Discussion ... 37
Process flow changes ... 37
4. Final Process Flow ... 38
4.2 First mask ... 38
4.3 Second mask ... 38
4.4 Third mask ... 39
4.5 Fourth mask ... 39
4.6 Fifth mask ... 40
5. Simulations and design settings ... 40
5.1 Parameters and sweeping ... 41
Swept parameters ... 41
Fixed parameters ... 41
5.2 Simulation results ... 42
5.3 Parameters sweeping for the final designs ... 43
6. Fabrication ... 43
6.1 Dose test ... 43
6.2 First mask fabrication ... 45
Exposure results ... 45
Sputter deposition and lift off ... 47
7. Conclusion ... 48
8. Bibliography ... 51
9. Appendices ... 53
9.1 Details of fabrication and machine parameters in CMi ... 53
Test wafer #59844 one time development ... 53
Test wafer #59846 two times development ... 54
Test wafer #59845 other recipe development ... 55

HR 1 already released structures 55
Test wafer #69843 bonding test 56
HR wafer 53 oxide 1um dose test 56
HR wafer 54 oxide 1um fabrication........ 56
HR wafer 55 oxide 1um fabrication........ 57
9.2 Results of the simulations........ 58
500 nm Aluminum nitride thickness 58
250 nm Aluminum nitride thickness 60
100 nm Aluminum nitride thickness 62
9.3 Process flow and design........ 63
Process flow........ 63
Process flow with design 68
9.4 Wafer organization 71

1. Introduction

A process flow to build a piezoelectric nano-balance for µRNA detection is studied and developed. µRNA are micro single stranded DNA that is found in mammalian's and plant's cells. µRNA are useful to detect early stage of different diseases like different types of cancer because tumor cells can be detected with µRNA [1] [2] [3] [4]. Different methods exist to detect µRNA as the northern blotting [5], RT-PCR [6] and microarrays [7]. However, these methods have some limitations, northern blotting is complex and has a low detection efficiency. RT-PCR and the microarrays detection demonstrated a good limit of detection but they require a lot of expensive material to build the setup [8]. Therefore, the research on some new detection methods are currently developed as electrochemical methods [9], isothermal amplifications [10] and nanoparticle-derived probes [11]. In these new techniques, nano-balance resonator for mass sensing is used. To perform mass sensing, a sensitive layer to the specific µRNA must be deposited on the surface of the resonator. If the sample contains the targeted µRNA, it fixes on the surface and induces a shift of the resonance frequency of the resonator. They have the tremendous advantage to have a very low limit of detection [12], a good sensitivity [13] and the setup can be easier.

1.2 Contour mode resonator

Contour Mode Resonator (CMR) for MEMS-radio is studied in the Advanced NEMS group by Andrea Lozzi. The group has already a deep knowledge of this type of resonator and the idea is to use this resonator as a gravimetric sensor. The advantage of the CMR are that the resonance frequency can be lithographically [13] set, low motional resistance and high quality factor is demonstrated [14], high frequency can be achieved and wide range of resonance frequency can be set [15]. Figure 1 shows a 3D scheme of the CMR with a cross section.

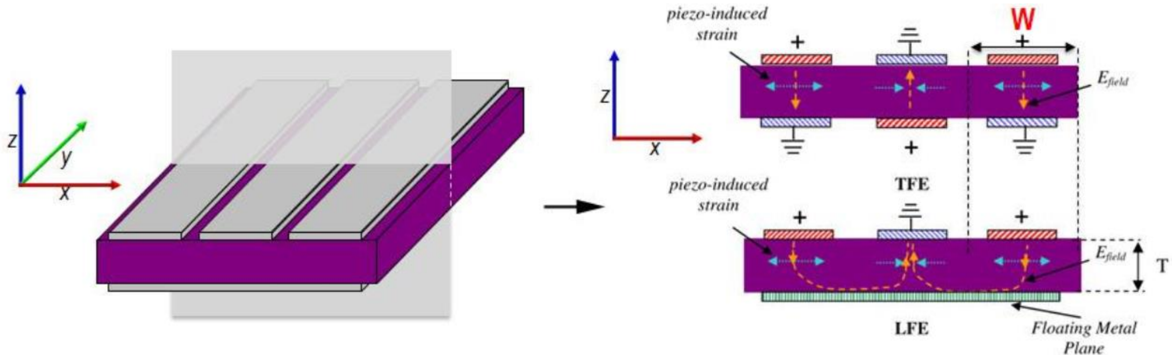


Figure 1 – (Left) 3D scheme of the CMR; (right) Cross section of the CMR: (Up) Thickness field excitation of the contour mode resonator and lateral field excitation. The top electrodes are interdigitated fingers and the bottom electrode is a floating plate [16]

The electric field E_{field} generates a deformation in the in-plane x direction through the d_{31} piezoelectric coefficient creating an acoustic wave of length $\lambda = 2W$. The resonance frequency

is set by the pitch of the electrodes W. The approximation of the resonance frequency is shown in the equation (1):

$$f_r = \sqrt{\frac{E_{eq}}{\rho_{eq}}} \cdot \frac{1}{2W} \quad (1)$$

Where f_r is the resonance frequency, E_{eq} is the equivalent young modulus of the layers, ρ_{eq} is the equivalent density of the layers and W is the pitch of the electrodes. If the bottom electrode is a platinum layer, the piezoelectric is the aluminum nitride layer and the top electrode is a platinum layer with respectively a thickness of 100 nm, 1 µm and 100 nm, the resonance frequency is around 220 MHz. [16].

1.3 Contents of the report and major goals

In this report, Andrea's process flow is studied. Then, changes on the process flow are done in function of the requirements needed to do a gravimetric sensor. The major goal to achieve are:

- To have a top gold layer on the resonator so that it can be functionalized to do µRNA detection.
- To think how to achieve a good sensitivity
- Bring liquid in the resonator
- Reduce the motional resistance of the CMR and keep the quality factor as high as possible.
- Reduce the parasitic capacitance of the CMR

In function of these major goals, a 5-masks process flow is presented and fabrication of the bottom electrode layer is done.

2. First process flow

2.1 Process flow of the lab

Andrea Lozzi from the group Advanced Nems in EPFL has already established a process flow to design contour mode resonators with lateral field excitation. The design of the top electrode is interdigitated fingers and the bottom electrode is a plate. The process flow is a 3-mask design:

Steps before the first mask

All the necessary layers for the structure are deposited and the chip is done by etching with different masks. Figure 2 shows the steps done before the first deposition of the photoresist.

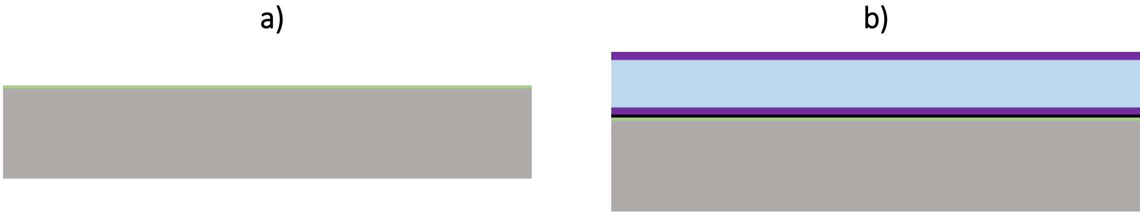


Figure 2 - Steps before first mask of Andrea's design: (a) A wafer with a 400 nm Silicon Nitride is LPCVD deposited with low stress. (b) Sputter deposition of 15 nm titanium adhesion layer, of 100 nm platinum bottom electrode layer, of 1 µm aluminum nitride piezoelectric active layer and of 100 nm platinum top electrode layer.

First mask

The first mask is shown in Figure 3. It is to pattern the top electrode, tracks and pads:

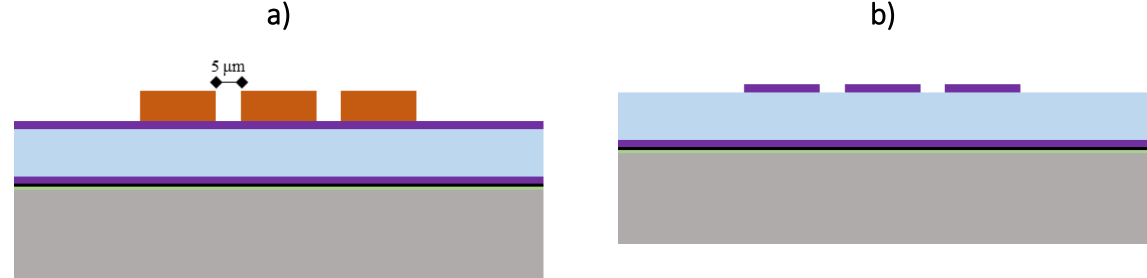


Figure 3 – First mask of Andrea's design: (a) Photolithography patterning of the top electrode, pads and tracks. (b) Etching to design the interdigitated top electrodes, pads and tracks. The resist is then striped off.

Second mask

The second mask is shown in Figure 4. It is to pattern the resonator shape, the size of the anchors and to have access to the bottom plate electrode for the 2-port resonator:

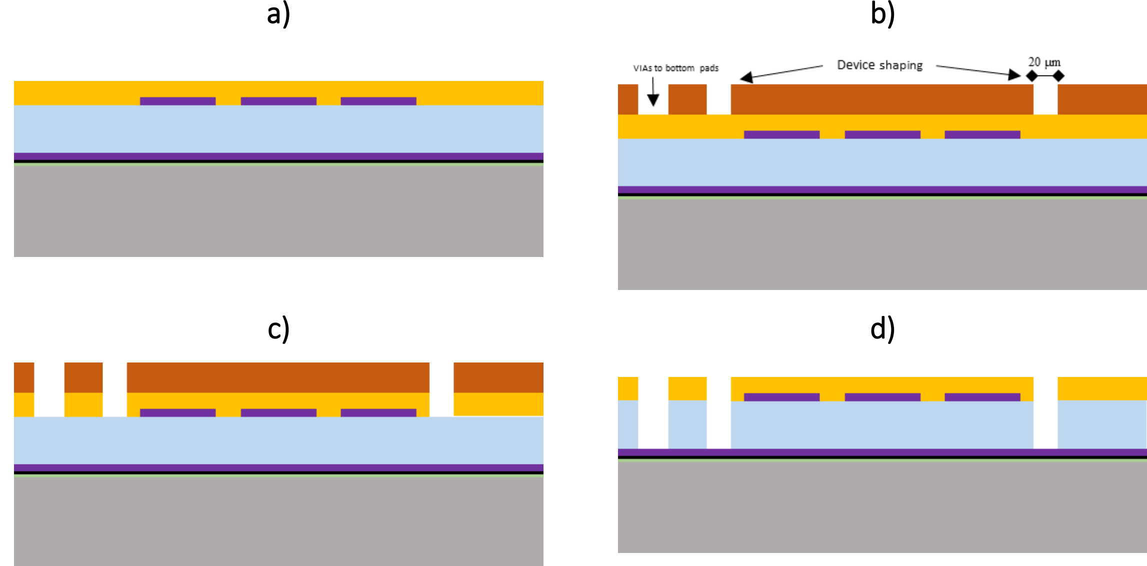


Figure 4 – Second mask of Andrea's design: (a) Sputter deposition of Silicon oxide to have hard mask layer. (b) Photolithography patterning of the resonator, anchors and bottom electrodes access. (c) Etching of the silicon oxide hard mask for the patterning of the resonator, anchors and bottom electrodes access, then the resist is stripped. (d) Etching of the Aluminum Nitride until the bottom electrodes.

Third mask

Third mask is shown in Figure 5. The aim of this mask is to protect the bottom pads, thus to have the electric access to get the S_{12} transmission coefficient on the 2-port design. Then the release of the resonator is done.

Figure 5 – Third mask of Andrea's design: (a) Photolithography to protect the electric bottom electrode access. (b) Etching of platinum, titanium until silicon is reached, then the resist is stripped. (c) Anisotropic etching of Si, then the SiO2 mask is stripped. (d) Isotropic etching of Si to do the release of the resonator.

[16]

2.2 Andrea's design and results

Andrea did mainly 2 different designs: 1-port design enable to measure the reflective power coefficient S_{11} of the CMR and the 2-port design enable to measure the transmission power coefficient S_{12} of the CMR. Figure 6 shows 2 images with the optical microscope of Andrea's deisgn.

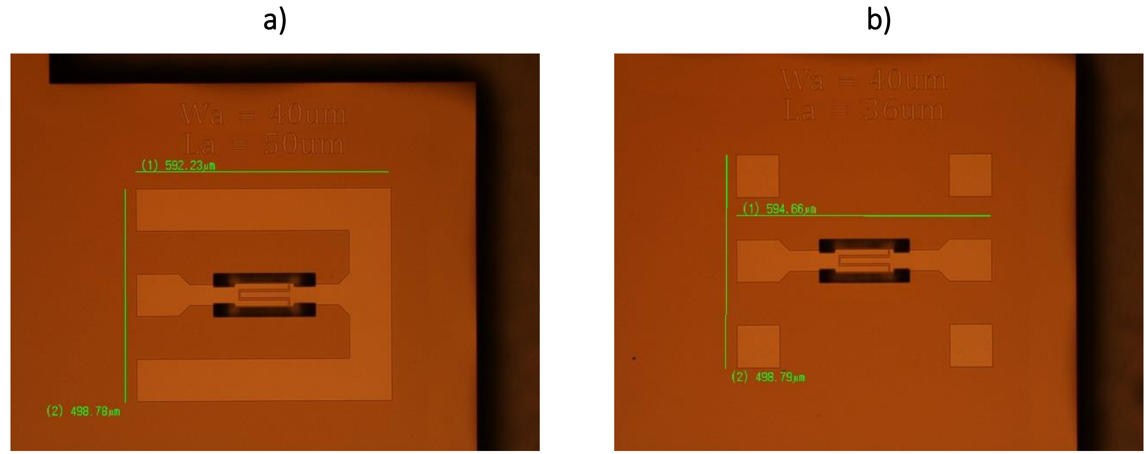


Figure 6 – Andrea's CMR design. At the middle of both images, the interdigitated electrodes with the track and pads around. (a) 1-port CMR: The pads are on the left and the reflective power coefficient can be measured; (b) 2-port design: The pads are on both sides and the transmission power coefficient can be measured.

The first remark is that Andrea's design density is very high. The resonator, the tracks and the pads occupy 600 µm width and 500 µm large with a space of 400 µm between each design.

This process flow is not used for the project. The process flow is changed in function of the different requirements in the project. The aim to present it in the report is to show from what the project has started.

3. Second Process Flow

This chapter discusses about the changes that need to be done on the process flow to accomplish the different goals of the project. The final process flow is in the appendixes section 9.3 on page 63.

3.1 Top and bottom electrodes

Top plate electrode

In this project, the top metal of the resonator needs to be a gold plate so that it can be used for µRNA detection. To increase the sensitivity of the resonator, the area of the functionalized gold must be as big as possible. Therefore, the top electrode of the resonator is chosen to be a plate. The gold is deposited by evaporation and patterned with lift off process flow.

Bottom interdigitated electrode

Since the top electrode is a plate, the bottom electrodes must be interdigitated electrodes to have a lateral field excited CMR. The bottom layer is thus patterned with the lift off process. Therefore, the interdigitated electrodes are underneath the resonator and is not in direct contact with the liquid. The contact with the liquid to the electrodes would create short circuits. It can destroy the resonator and it is very bad for the measurements. The electric tracks are done at the bottom layer level too. Thus, the electrodes are connected to the pads. Then, vias is etched to have access to the pads (as in Andrea's process flow, see Figure 4). For the further steps of the process flow, these bottom pads need to be protected by a mask (the same as the 2-port resonator, see Figure 5).

Lift off process flow with AZ1512 resist on LOR resist

Figure 7 shows the process flow of the patterned interdigitated electrodes with the pads and the tracks.

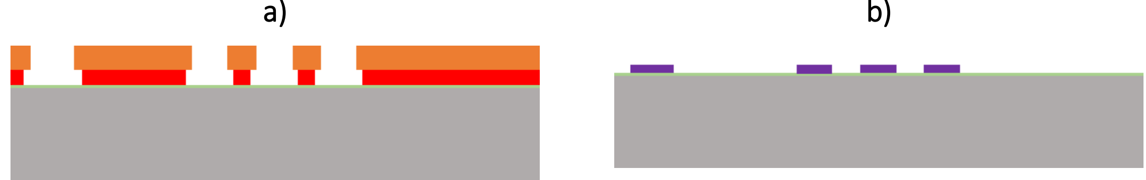


Figure 7 - Lift off process flow: (a) Coating and exposure of the AZ1512 resist on LOR resist. The exposure creates this under etch design to avoid fences on the edge of the platinum; (b) Platinum is sputtered deposited and the resists are then removed. A 10 nm titanium layer must be deposited before the platinum to have a better adhesion of the platinum of the oxide.

Lift off of sputtered platinum

This section discusses about the lift off process. Lift off patterning with platinum sputter deposition can show some concern. In fact, lift off process can create some fences at the edges of the design because the platinum can be deposited on the wall of the resist. This phenomenon

is dramatic and can decrease the quality factor of the resonator. In fact, in the next step of the process, the piezoelectric active layer is not properly deposited and won't be efficient if there are fences on the design. Moreover, some design rules must be checked in function of the difference between dimension at the mask level and the dimension at the wafer level. We check if dimensions of the design remain during the whole lift off process. The platinum can be deposited underneath AZ1215 photoresist (see Figure 7), thus the dimensions are bigger. For example, an over exposure or an over developed resist can make the electrodes dimension bigger. This section sets the correction of the dimension due to lift off process.

One time development

More details on the fabrication and machine parameters are shown in the appendices in the section *"Test wafer #59844 one time development"* on page 53.

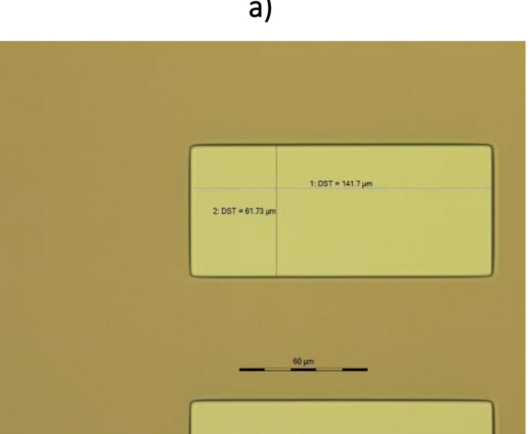
A CMi test wafer is taken. Coating of 620 nm AZ1512 resist on 480 nm LOR. Exposure is done and the resist is then developed once.

Figure 8 shows the result of the lift off process with the LOR resist after the development step.

Exposure parameters:

- Dose: $80\,\frac{mJ}{cm^2}$
- Defoc: -3
- Wavelength: $405\ nm$

a)



b)

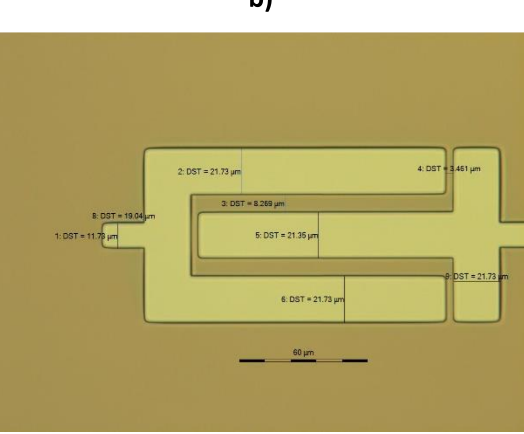


Figure 8 – After the resist development: (a) A plate of exposure dimensions of 60x140 µm² with a lift off correction of around 1.7 µm; (b) Exposure mask settings of the interdigitated electrode: Electrodes width: 20 µm, Anchor length: 18 µm, Anchor width: 10 µm, bus width: 20 µm. The lift off correction is around 1.7 µm.

We can see that the photoresist is over exposed. The dimensions are more than 1 µm bigger than the mask dimensions.

Then, Figure 9 shows the result of the final step of the lift off process. After the development of the LOR resist, 10 nm titanium and 100 nm platinum are sputtered deposited. Then a **lift off removal procedure** is done:

- Put the wafer in the remover 1165 bath during 3h
- Rinse the wafer with remover 1165
- Put 2 times the wafer in the remover 1165 with ultra sound during 300 seconds
- Put the wafer in the remover 1165 during one night
- Rinse the wafer with remover 1165
- Put the wafer in a IPA bath during 130 seconds
- Rinse the wafer in 2 different water bath during 10 seconds each
- Rinse with water
- Dry with air

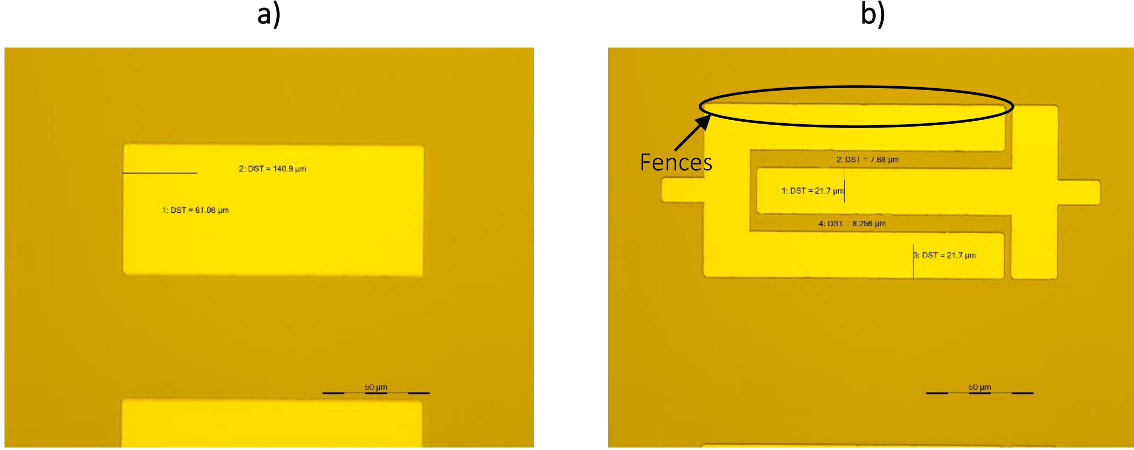


Figure 9 – Once developed resist, after the sputtered platinum deposition and the resist removal: (a) Plate of exposure dimension of 60x140 µm². The black border on the edges of the design are fences; (b) Interdigitated electrodes with the same dimension as the one in Figure 8. Fences are along the whole edge of the design.

We can see that there are fences at the edge of the design showed by black border. The wafer is put in ultra sound bath but no difference is noticed. The fences are strong enough to withstand ultra sound.

Two times development

More details on the fabrication and machine parameters are shown in the appendices in the section *"Test wafer #59846 two times development"* on page *54*.

To avoid these fences, the idea is to develop twice the photoresist with the same recipe. The LOR photoresist is etched further and can avoid the growth of these fences.

First, Figure 10 shows the result lift off process with the LOR photoresist after the development step. A CMi test wafer is taken. 620 nm 1512 AZ photoresist is deposited on 480 nm LOR photoresist is done. Then exposure is done and the photoresist is developed twice.

Exposure parameters:

- Dose: $65\,\frac{mJ}{cm^2}$
- Defoc: -3
- Wavelength: $405\ nm$

Exposure dose is reduced because the photoresist is developed twice and was over exposed in last section (see “Figure 8).

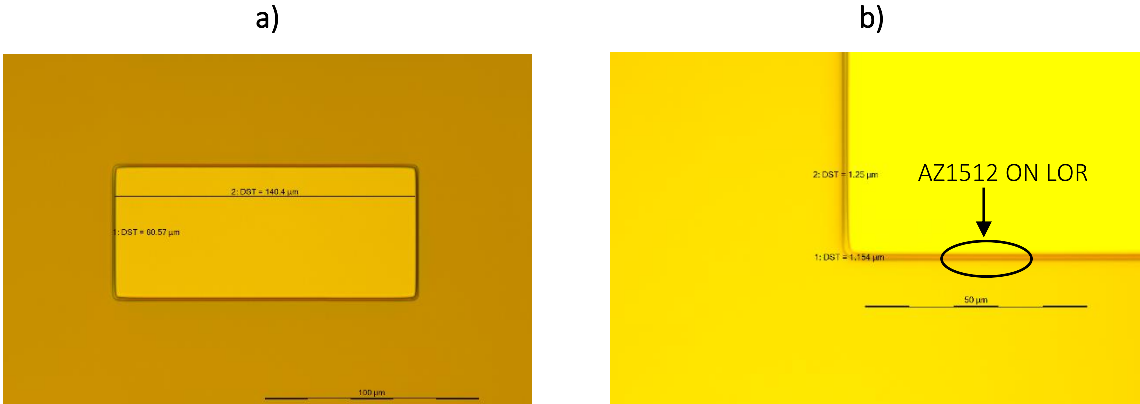


Figure 10 - After the twice photoresist development: (a) A plate of exposure dimensions of 60x140 μm^2 with a lift off correction of 0.5 µm; (b) Zoom of the left image. The under etched LOR photoresist can be clearly seen. Compared to Figure 8, the under etching of the LOR photoresist is clearly bigger when the photoresist is developed twice.

We can see that the twice developed photoresist has no significant effect on the AZ1512 photoresist however, the LOR photoresist is more under etched than the once developed photoresist. In fact, the dimension of the plate (AZ1512 photoresist) is even smaller because the exposure dose is lowered. But the under etched LOR photoresist increases due to twice developed photoresist.

Then, Figure 11 shows the result of the final step of the lift off process. After the development of the LOR photoresist, 10 nm Titanium and then 100 nm platinum is sputtered deposited. The lift off removal procedure is performed (see section *“One time development”* on page 10).

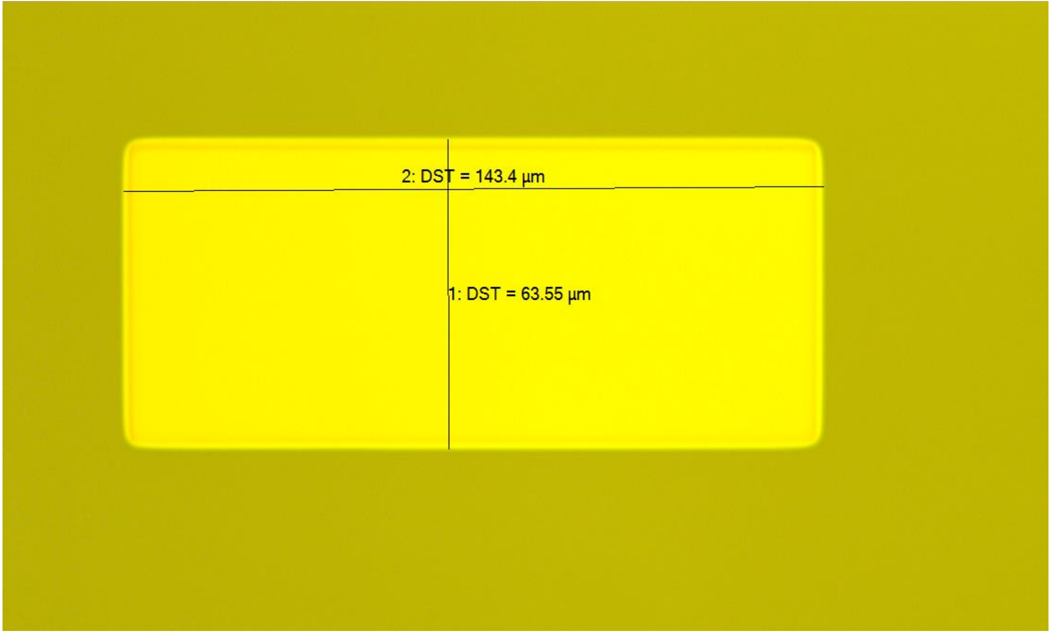


Figure 11 - Twice developed photoresist, after the sputtered platinum deposition and the photoresist removal. A plate of exposure dimensions of 60x140 µm^2 with a lift off correction of more than 3 µm. No black border thus so no fence.

When the photoresist is developed twice, the fences disappear. In fact, the twice developed photoresist make a bigger space under the AZ1512 resist which avoids the fences to grow on the wall of the photoresist. Just few designs contain some fences which can be removed by putting the wafer some more time in the ultrasound bath. However, the dimensions are getting bigger. There is a lift off correction of more than 3 µm.

Other recipe development

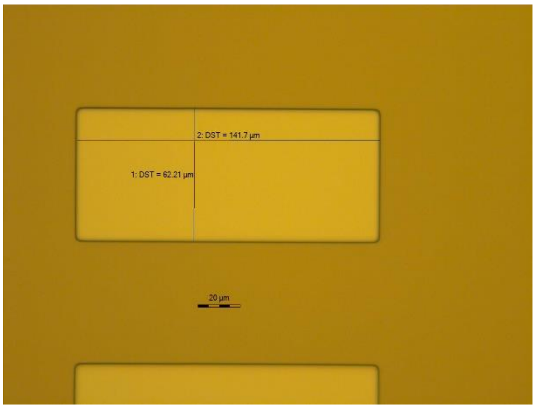
More details on the fabrication and machine parameters are shown in the appendices in the section "Test wafer #59845 other recipe development" on page55.

To try to avoid fence and at the same time, having correct dimension. Another development recipe is tried on the same coating. Figure 12 shows the result of lift off process with the LOR photoresist after the other recipe development step. A CMi test wafer is taken. Coating of 620 nm AZ1512 photoresist on 480 nm LOR photoresist is done. Exposure is done and the photoresist is then developed with the other recipe for a coating of 680 nm AZ1512 photoresist on 820 nm LOR photoresist.

Exposure parameters:

- Dose: $65 \frac{mJ}{cm^2}$
- Defoc: -3
- Wavelength: $405\ nm$

a) b)



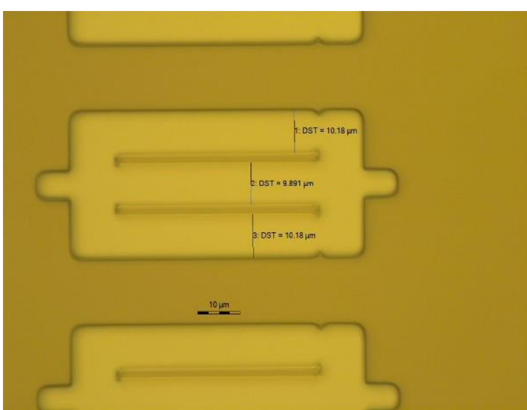
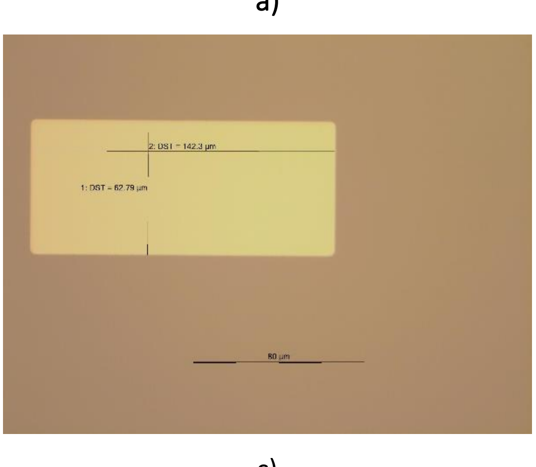


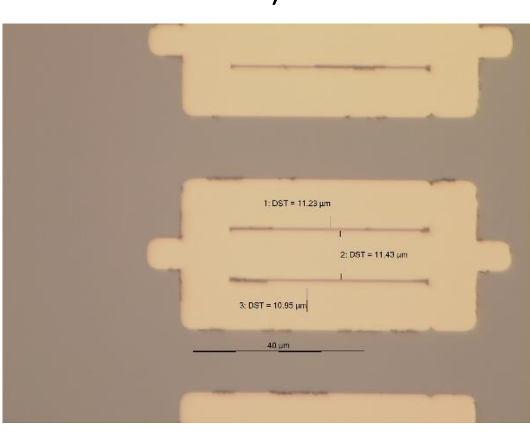
Figure 12 - After the other photoresist development: (a) A plate of exposure dimensions of 60x140 μm^2 with a lift off correction of around 2 µm; (b) Interdigitated electrodes with mask exposure dimension: Electrodes width: 8 µm. The space between electrodes tends to disappear because of the lift off correction.

The other development recipe doesn't solve the lift off correction problem. It is even worse than the two times developed photoresist.

Figure 13 shows the result of the final step of the lift off process. After the development of the LOR photoresist, 10 nm Titanium and then 100 nm platinum is sputtered deposited. The **lift off removal procedure** is done (see section *"One time development"* on page 10).

a) b)





c) d)

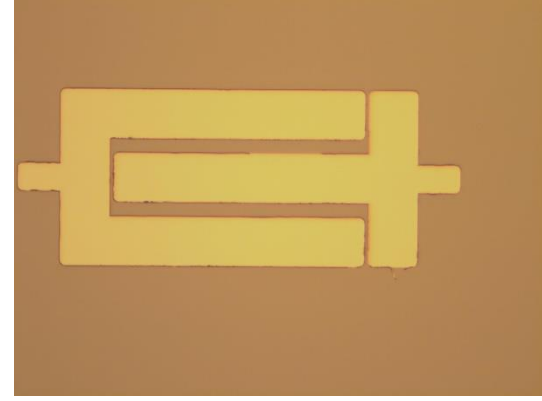


Figure 13 - Other developed photoresist, after the sputtered platinum deposition and the photoresist removal: (a) Plate of exposure dimension of 60x140 µm². Lift off correction of around 2.5 µm. Plate seems to be fence free; (b) Interdigitated electrodes with the same dimension as the one in Figure 12. There are still some remaining fences; (c) Other plate of exposure dimension of 60x140 µm² with fences; (d) Interdigitated electrodes structures with fences.

There are some designs which are fence free but most of them contain some fences. Even after the ultra sound treatments, the fences are not removed. Moreover, there is a lift off correction of around 2.5 µm. Therefore, the other recipe doesn't solve the dimension's problem.

Conclusion

The top electrode is a plate and the bottom electrode is interdigitated fingers and are done with lift off process. Consequently, 2 masks are needed. To do lift off patterning, the coating of 620 nm AZ1512 photoresist on 480 nm LOR photoresist is chosen. After exposure, the photoresists are **developed twice** with the corresponding recipe. Since the dimensions of the structures increases of 3 µm, this must be taken in account. Therefore, to have **the wanted dimension, the border of the structures must be shrunk to 1.5 µm.**

3.2 Bring liquid on the CMR

The aim in this chapter is to bring liquid on the CMR. The liquid shouldn't go on the pads where the probe must do electric contact because the probe can be destroyed. Previous design of the lab will be used but the process flow and the design of lab will be changed in function of the results in this chapter.

Droplet on resonator tests

The first idea is to accurately deposit a droplet on one of the already made wafer of the laboratory. To deposit the smallest droplet as possible, a syringe with a capillary tube of inner diameter size of 25 µm is built:

- Take a plastic syringe with inner diameter size of 1 mm
- Take a tube with an inner diameter size of 25 µm (outer diameter 50 µm)
- With a tweezer, take gently the tube and put it inside the syringe. The tube should be the end piece of the syringe.

- With the help of some wax and a solder, seal the tube and syringe together (between syringe inner wall and tube outer wall).
- There should be no liquid leakage between the syringe inner wall and the tube outer wall

With the help of an optical microscope, some droplets are deposited on the wafer. Many concerns about this technic are noticed:

Size of the resonator comparing to the size of the droplets

Many tries are done to deposit droplets on the resonator. Figure 14 shows the images of ones of the two best deposition of the droplet on the resonator.

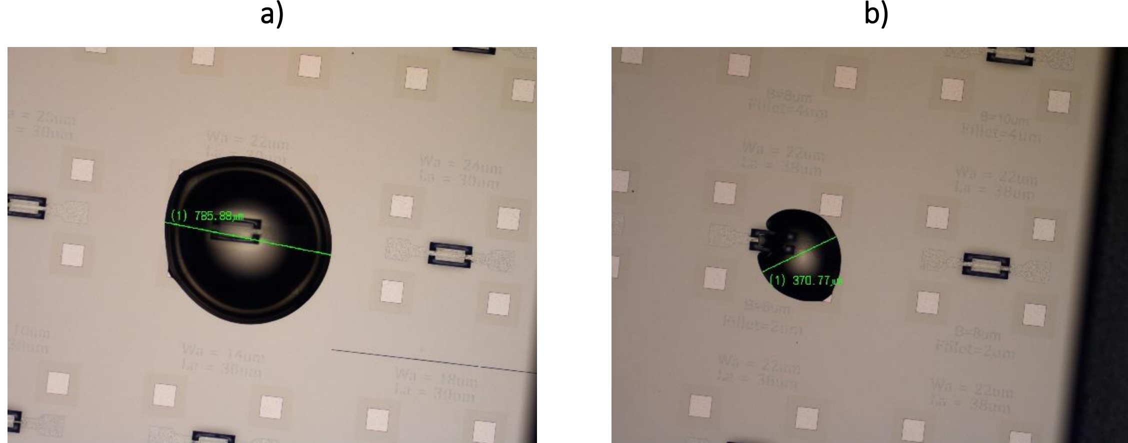


Figure 14 - Droplet deposition on Andrea's design: (a) The droplet has a bigger size (789 µm) than the whole design (resonator + pads). (b) The droplet can fit in the design without touching the electrodes but the droplet is not accurately deposited and aligned

These two images show two different issues of this technic. On the left, the droplet is too big for Andrea’s design. The image on the right shows how hard is it to deposit the droplet accurately on the resonator even if its size is small enough.

Small droplets dry

Figure 15 shows 4 consecutive pictures of the same droplet on the device with an interval time of around 30 seconds.

a) b)

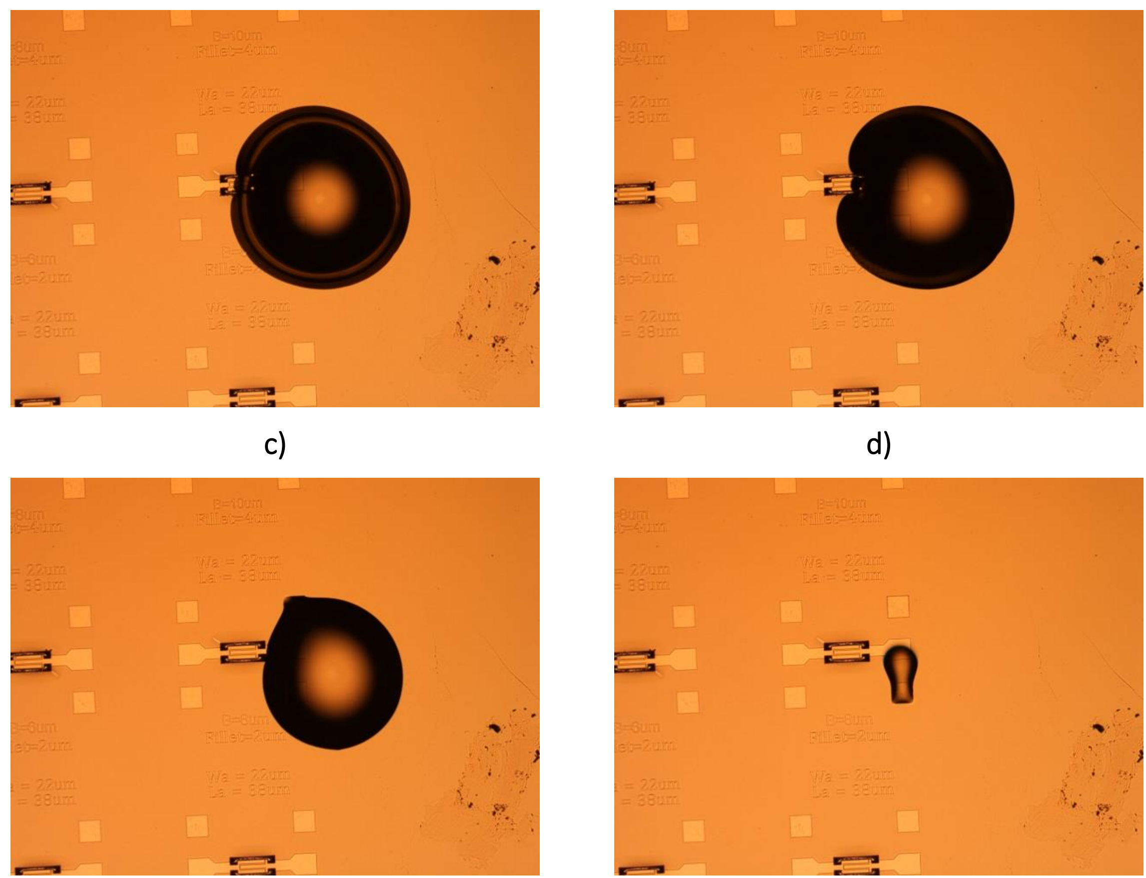


Figure 15 – 4 consecutives pictures of the same droplet with an interval of around 30 seconds between each picture. The size of the droplet decrease faster when the droplet is smaller.

The droplet gets smaller because of evaporation. The evaporation rate depends on the temperature of the droplet therefore the light intensity of the microscope and room temperature. It also depends on the room humidity. The evaporation rate is higher when the room is dry. We can see that, smaller the droplet is, faster its area footprint decrease. The reason why is that the surface (which is in contact to the air) to the volume of the droplet ratio increases. So, the evaporation rate which is proportional to the contact area to the air of the droplet becomes higher comparing to its volume therefore the mass.

$$A \propto evaporation\ rate \qquad V \propto mass \tag{2}$$

So:

$$\frac{A}{V} \propto \frac{evaporation\ rate}{mass} \tag{3}$$

If $\frac{A}{V}$ increases, $\frac{evaporation\ rate}{mass}$ increases too.

A is the contact area to the air of the droplet. V is the volume of the droplet.

Liquid is sucked on the pads

Figure 16 shows another phenomenon during the evaporation of the droplet. The two pictures are taken with an interval of 1 minute.

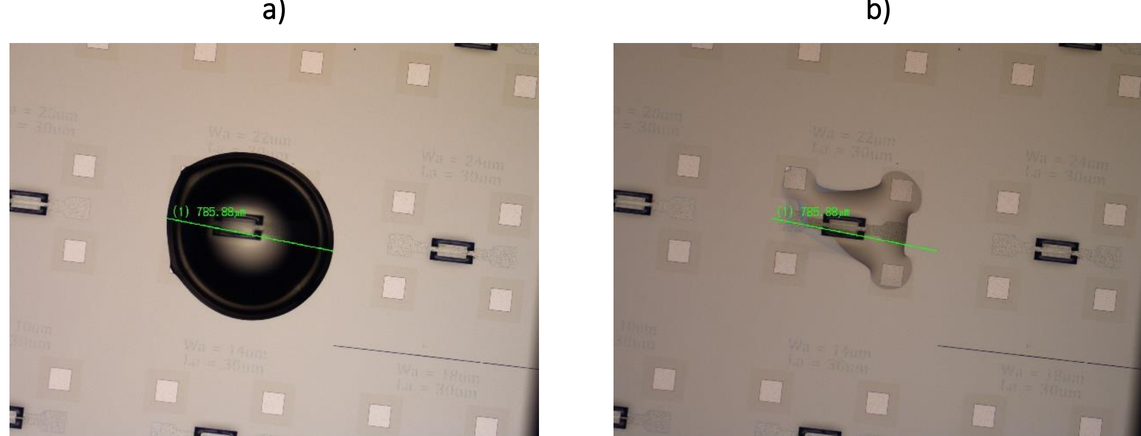


Figure 16 - Liquid is sucked on the pads: (a) Droplet of the size 789 um deposited on the device. (b) After 1 minute the droplet evaporate and stay on the electrodes

The droplet on the second picture on the right stays on the pads. It was first explained because platinum has a smaller contact angle than the aluminum nitride, thus platinum is more hydrophilic than aluminum nitride but after the studies of contact angle (see section *"Contact angle studies"* on page *18*), the reason why the liquid stays on the pads is because they are bottom layer pads. The liquid is just flowing down to the pads like a liquid flowing down in a hole.

Contact angle studies

This section studies the contact angle of liquid on different surfaces. There are 2 reasons to study contact angle:

The first reason is to know if some liquid goes underneath the resonator. In fact, on a round shape wall channel, the capillary pressure equation is:

$$P_C = -\frac{2\sigma_{liquid}\cos\theta}{r} \quad (4)$$

For a rectangular shape wall of channel, the capillary pressure equation is:

$$\mathrm{P_C} = -2\sigma_{liquid}\cos(\theta)\cdot\left(\frac{1}{h}+\frac{1}{w}\right) \quad (5)$$

[17]

In the project, the gap h (which correspond to the height of a channel) between the resonator and the bulk is smaller than the length w (which correspond to the width of a channel) of the gap.

$$w \gg h$$

$$P_C = -\frac{2\sigma_{liquid}\cos\theta}{h} \quad (6)$$

σ is the surface tension between air and the liquid, θ is the contact angle of the liquid on the surface of the channel, r, h, and w, is the radius, the height and the width of the channel respectively.

In the knowledge that the surface tension and the geometrical dimensions of the channel are positive values, if:

$$0° < \theta < 90°$$

The surface is then hydrophilic, the capillary pressure is negative and the liquid is sucked underneath the resonator by capillary pressure effect.

If:

$$90° < \theta < 180°$$

The surface is then hydrophobic, the capillary pressure is positive and the liquid doesn't go underneath the resonator.

Figure 17 shows a hydrophilic interaction with the wall of the channel. The motion of the liquid goes from the left to the right and fills the space occupied by the air because of capillary pressure.

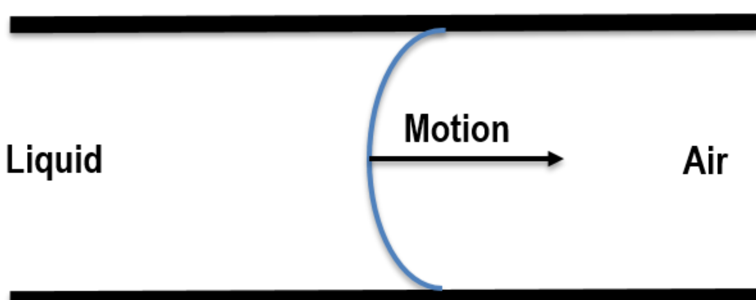


Figure 17 - Capillary pressure in the channel with a hydrophilic wall. The motion goes to the right and fills the channel

The main material between the resonator structure and the bulk is the sputtered deposited aluminum nitride.

The second reason to study contact angle is to know why the liquid stays on the pads (see Figure 16). In fact, if the platinum is more hydrophilic thus a smaller contact angle than the aluminum nitride, it would explain that the water goes on the pads.

Contact angle measurements:

In this section is described how the contact angle is measured and which settings and material is used.

2 wafers from the clean room with:

- 15 nm sputter deposited aluminum nitride

- 25 nm sputtered deposited platinum on 15 nm sputtered deposited titanium

Krüss DSA-30E machine is used to measure the contact angle. 3 droplets are deposited on each wafer and contact angle measurements are done 20 times for each droplet (10 measurements on the left side of the droplet and 10 measurements on the right side of the droplet). Figure 18 shows 2 pictures of the deposited droplets on the wafers.

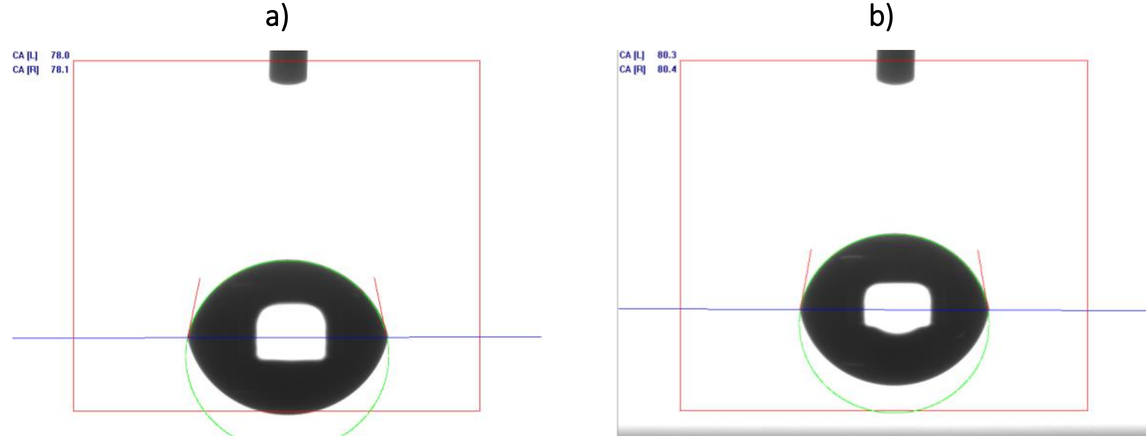


Figure 18 - Contact angle measurements: (a) Water on aluminum nitride; (b) Water on platinum. The blue line defines the surface profile on which the droplet is deposited. The convex geometry is the reflection of the droplet. On top of the image is the nozzle to deposit the droplet. Top left of the pictures shows the contact angle value in degrees of the image.

Table 1 shows the value of the mean of the 60 measurements done on each surface.

Water on aluminum nitride [°]	Water on platinum [°]
77.5	79.8

Table 1 – Contact angle measurement of water on aluminum nitride and platinum

The aluminum nitride is more hydrophilic than the platinum. So, it cannot be explained that the liquid is sucked on the pads because of the surface tension (see Figure 16 on page 18).

Water on aluminum nitride has a contact angle smaller than 90°. Consequently, liquid can be sucked underneath the resonator with the capillary pressure and the liquid goes on the interdigitated electrodes. To avoid the short circuits, a wafer from CMi with a thermal silicon oxide layer is taken. This passivated layer protects the interdigitated electrodes from the liquid. The other way to avoid liquid on the interdigitated electrodes is to coat the walls with Teflon (PTFE) which has a contact angle of around 110°.

[18]

Conclusion

The fact that the liquid goes on the pads is dramatic for measurements. It creates shortcuts which drives a too high current. The droplet dries also too fast which limits the amount of time to do measurement. Another issue is the complexity of dropping precisely a droplet on the resonator which has a size of around 200x50 μm^2. To avoid short-circuits between the interdigitated electrodes, because liquid may be sucked underneath the resonator, is to

passivate electrodes with oxide. Thus, a silicon with a wet oxide layer is taken from CMi. Therefore, platinum electrodes are deposited on a silicon oxide. Another way to bring liquid must be found and is discussed in the following chapter.

3.3 PDMS Channel

The idea is to fabricate a PDMS channel and to bond it irreversibly on the wafer. One channel covers a whole chip with aligned resonators in parallel. The process is well known and irreversible bonding works perfectly fine on flat glass. Therefore, the liquid is brought to the resonator without evaporation problems and the liquid is constrained in the channel. It avoids that the liquid goes on the pads. If there is a good bonding, there is thus no leakage. This chapter will define the process flow to fabricate and bond PDMS on substrate. Then different bonding condition is tested on different substrate, different design of channel will be done to test qualitatively the bonding.

The goal in this chapter is to find some design rules in the process flow of Andrea defined in the previous chapter (see section 2.1). In fact, the channel will add some other constrained: The walls of the channel need some space to have a good bonding thus no leakage of liquid. This parameter will define how far the pads must be pushed away from the resonator. The channel width defines how difficult the alignment of the channel to the chip will be and increases the dead volume. Increasing the channel height increases the dead volume but decrease the risk of bonding of the ceiling of the channel to the resonator during bonding process. The substrate to bond must be defined because it will change the process flow and the design mask of Andrea.

Figure 19 shows the channel configuration.

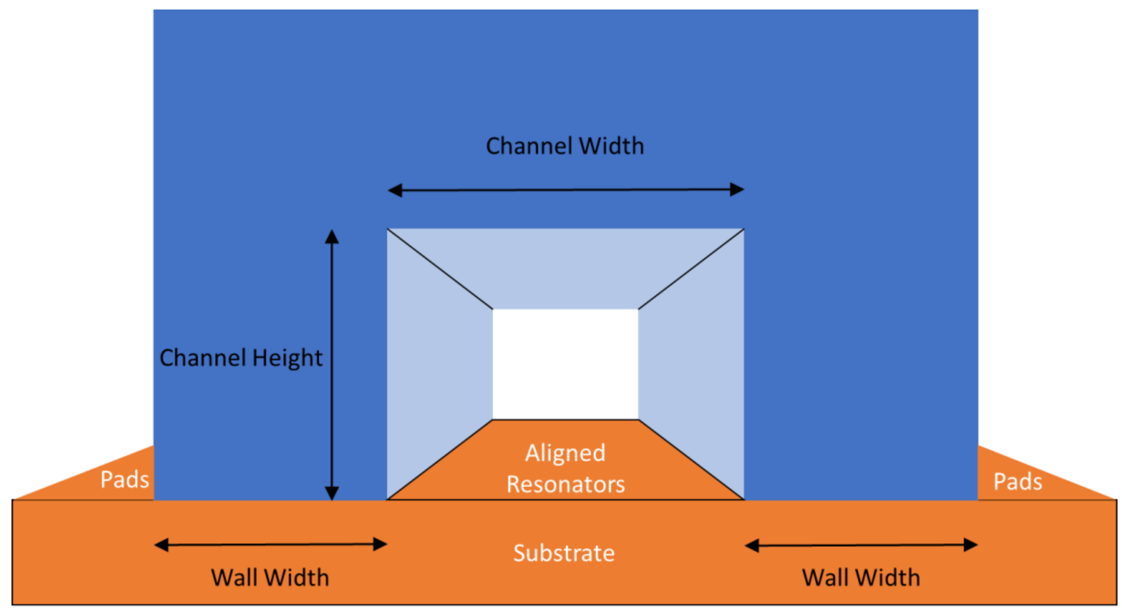


Figure 19 – 3D Cross section of the channel configuration on the substrate: 1 channel covers many resonators. The wall width defines how far the pads are pushed away from the resonators, the channel width defines how difficult the alignment channel-resonator will be.

Process flow of PDMS channel

Figure 20 shows the process flow to make channel with PDMS

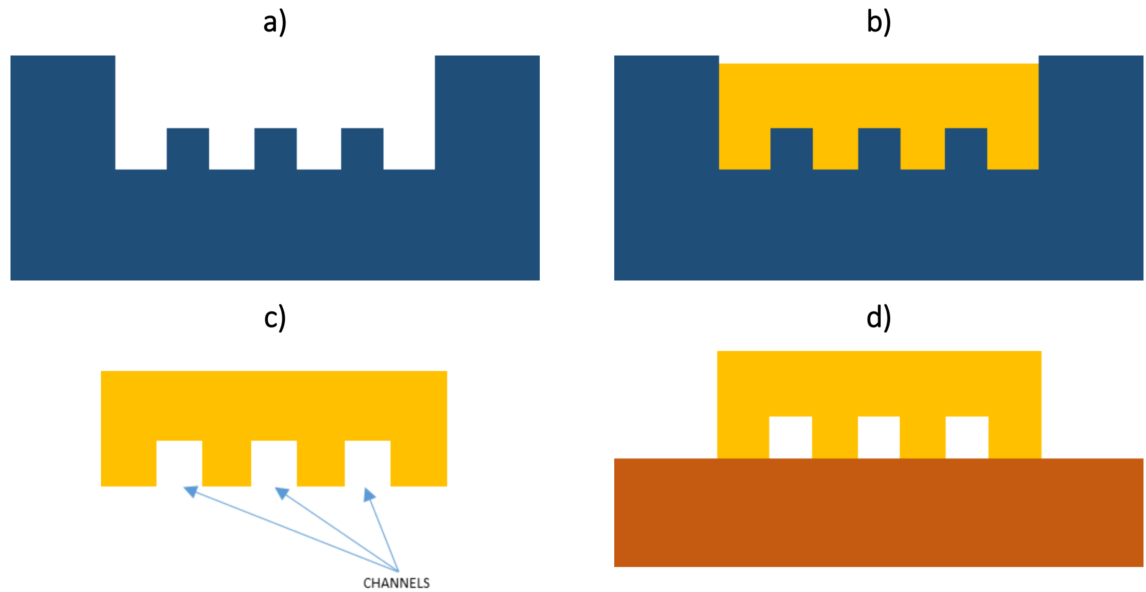


Figure 20 - Process flow of PDMS channel: (a) A negative mold is made with the help of 3D printer. (b) The PDMS (liquid) is flown down in the mold and put in a hoven. (c) The cooked PDMS is peeled off from the mold. (d) PDMS is irreversibly bonded to the substrate with the help of oxygen plasma surface treatment.

Detailed procedure to make PDMS channel and PDMS bonding

Here is detailed the procedure to make the PDMS channel and the PDMS bonding:

To make the 3D negative mold

- Design the negative mold on a 3D software. Always let a sacrificial part to be able to peel off the PDMS without destroying the channel
- The ".stl" file is launched in the formlab "From +1" printer. Parameters:
  - No support structures
  - Layer thickness 25 µm
  - Resin: Clear V2
- 10 min in the first Isopropanol bath (IPA) when the mold is finished
- 10 min in the second IPA bath to remove some unpolymerized resin of 3D printer
- Let it dry during 3 hours and exposed to the sunlight to do a bad polymerization of the remaining resin
- Put in a IPA beaker and put the beaker in an ultrasound bath during 5 minutes to remove the badly polymerized resin.
- Let the mold dry

To make the PDMS channel

The PDMS Sylgard® 184 Silicon Elastomer (Base + curing agent) is used:

- Put the mold in a 1% mass soap bath mix with DI water to make the peeling off easier.

- Let the mold dry.
- Mix during 5 min the PDMS base and the curing agent with a mass ratio of 10/1 respectively.
- Put the PDMS in the mold.
- Put the mold in vacuum during 5 min to remove bubbles in the PDMS.
- Put the mold in a hoven at 80 C° during 3 hours.
- Peel off the PDMS.
- Punch through the PDMS channel to make the outlet and the inlet of the channel.

To make the bonding on the substrate

The machine used to do plasma surface treatment is the Femto from electronic diener plasma surface technology:

- Rinse both surfaces with
    - Acetone
    - Isopropanol Alcohol
    - Deionized water
    - Dry with azote
- Put the PDMS and the substrate in the chamber, the surfaces to bond must be upward.
- Expose to oxygen plasma:
    - 0.6 mbar
    - 100 W
    - 0.2 min => 12 seconds
- With a tweezer, put the two surface to bond together and press them.
- Put the assembly in the hoven with some weight on it or put the assembly on a hot plate at 80 C° during 5 minute and maintain strongly the pressure.

To re-use the same negative mold to fabricate additional channel

- Put the mold in a IPA beaker and put the beaker in an ultra sound bath during 5 minutes to remove some residue of PDMS.
- Check if there is some PDMS on the mold. If yes, go to first step.
- Go to "*To make the PDMS channel*" procedure.

Fabrication of channels

Two different mold designs are made with different wall width and different channel width:

Channel width tested: 0.5 mm, 0.75 mm, 1 mm.
Wall width tested: 0.5 mm, 1 mm, 2 mm.
The height of the channel is 1 mm.

Consequently, 18 different designs are fabricated and are shown in Figure 21 and in Figure 22. The designs are made on SolidWork.

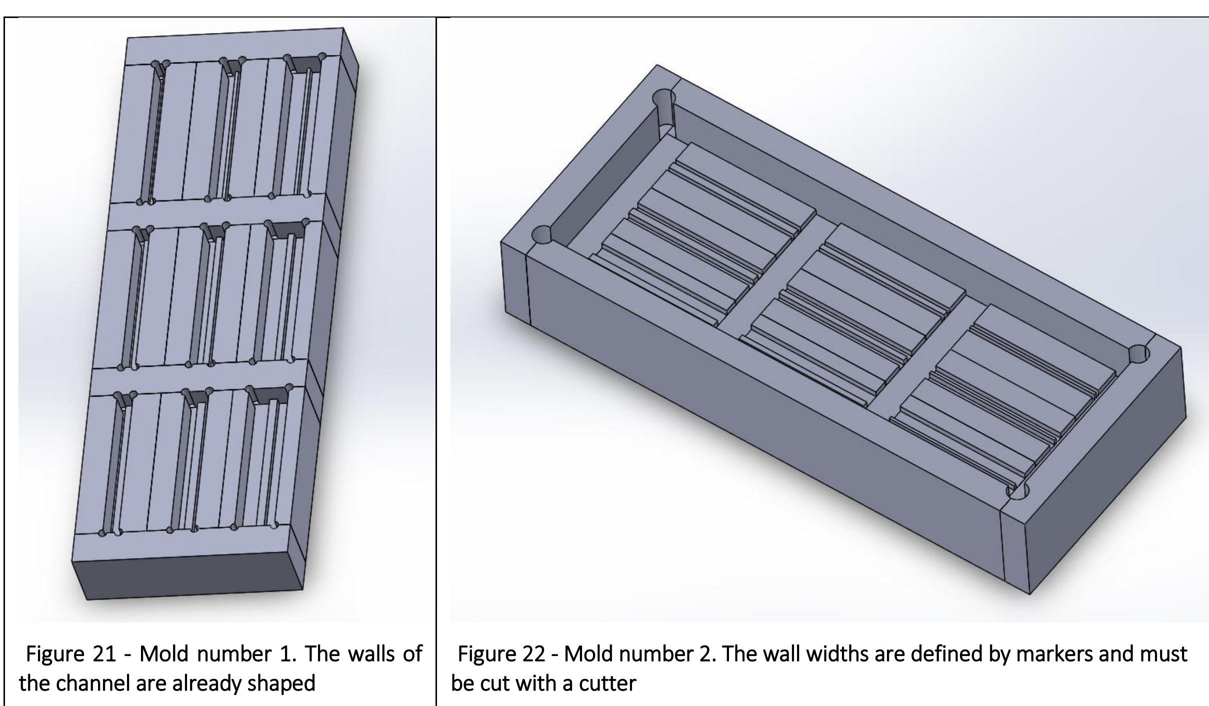
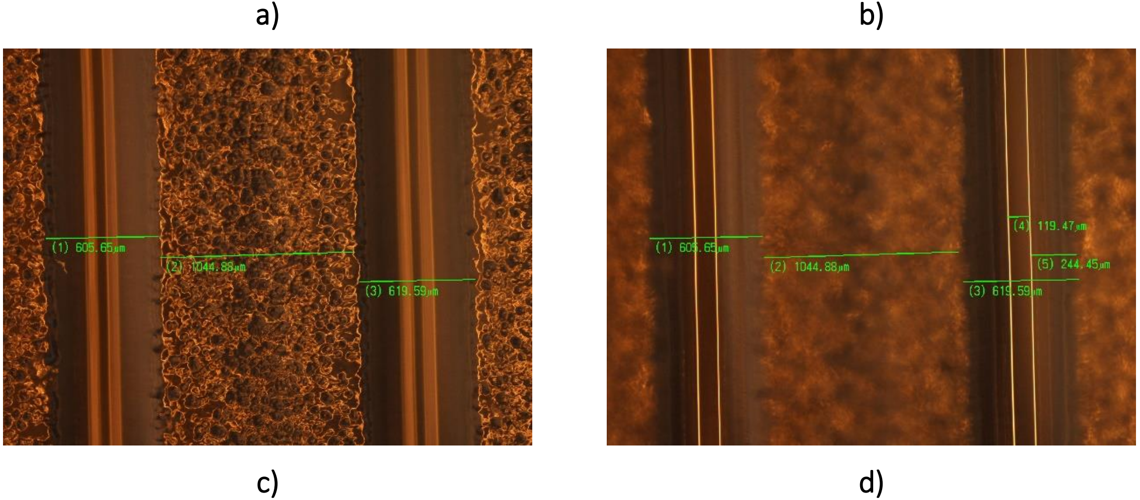


Figure 21 - Mold number 1. The walls of the channel are already shaped

Figure 22 - Mold number 2. The wall widths are defined by markers and must be cut with a cutter

The reason why these two designs are tested is because of the peeling off. Due to the aspect ratio of the design in the first mold, we could have some concern to peel off the PDMS. However, peeling of the PDMS in both design is not a problem.

Figure 23 shows different picture of different design of the negative mold after the 3D printing and the 3 hours waiting exposed to the sunlight (see section “*To make the 3D negative mold”)*.



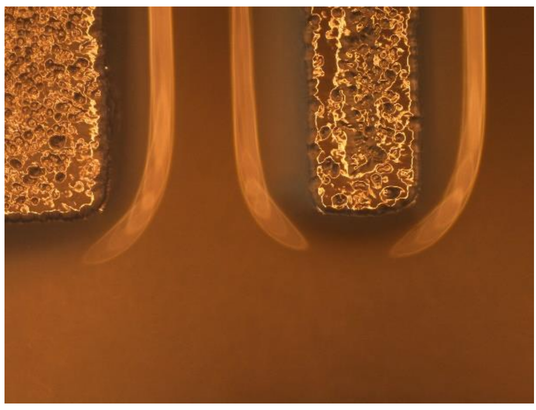
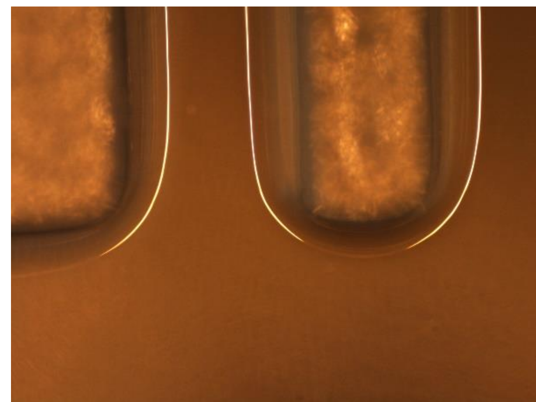



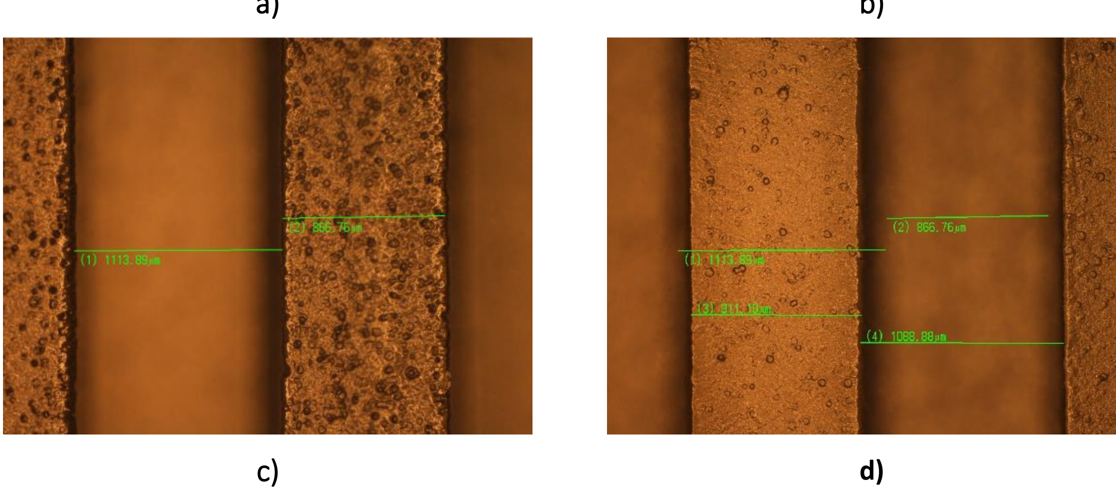
Figure 23 - Pictures of the channel of the 3D printing of the negative mold: (a) 1 mm channel width and 0.5 mm wall width focused on the channel. (b) 1 mm channel width and 0.5 mm wall width focused on wall contact. (c) and (d) End part of channel with different focus with a wall width of 1 mm and channel width of 0.5 mm

We can notice that there are some bright lines when the optical microscope is focused on the wall contact (Right images, Figure 23). This is due to the bad polymerization of some remaining resin which makes some round shape due to reflow at the corner of the channel (see especially image (d) of Figure 23). The badly polymerized resin is removed by using ultra sound.

Figure 24 shows the picture in the optical microscope of the negative mold for channels after the ultrasound bath in IPA.

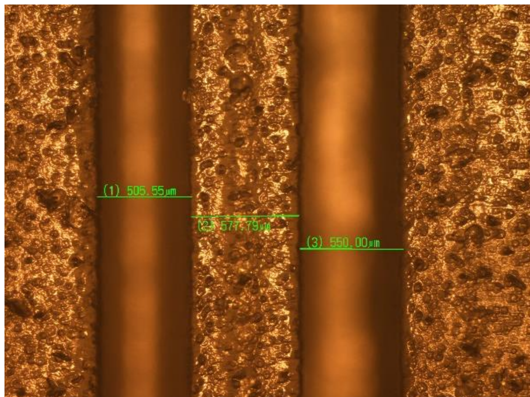
a)

b)



c)

d)



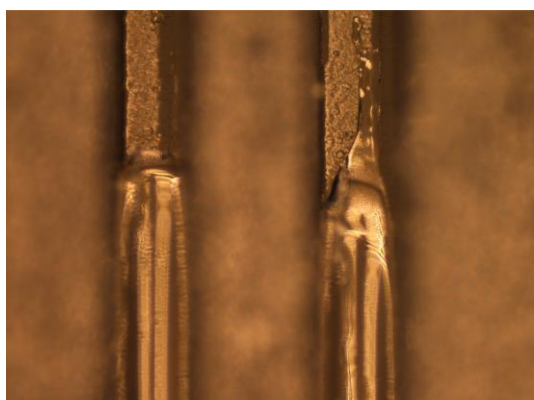


Figure 24 - Channels after Ultra Sound: (a) Channel width of 0.75 mm and wall width of 1 mm focused on the channel. (b) Channel width of 0.75 mm and wall width of 1mm focused on the wall width contact. (c) Channel width of 0.5 mm and wall width of 0.5 mm focused on the channel. (d) Channel width of 0.5 mm and wall width of 0.5 mm focused on the wall contact.

We can see in Figure 24 on image (a) and (b) that the remaining resin is removed. However, in smaller features, we can see on the image (d) that for a wall width of 0.5 mm, it can have some remaining resin which is dramatic because wall width contact must be as flat as possible because this area needs to be used for the bonding to the substrate.

Bonding and liquid test on different design of channel and different substrate.

This section gives the results of the PDMS bonding of different wall width of channels, different channel widths. These channels are tested on different types of substrates. Bonding test succeeds if the channel needs to be destroyed to remove the PDMS on the substrate. 2 different conditions of bonding are used: Just after the plasma exposure, we test different waiting time before making the contact between the two surfaces: 30 seconds and 60 seconds to simulate the requiring time to align the PDMS and the substrate. Then the assembly is put directly to the hoven with 5 Kg weight on it. Another test is made to know if there is any liquid leakage from the channel. channels of wall width of 0.5 mm, 1 mm and 2mm are tested and different channel widths (0.5 mm, 0.75 mm and 1 mm). Liquid test is done by punching through the PDMS on each side of the channel. the test fails, if there is any leakage when the liquid is flowing or if the liquid cannot be sucked in. In the tables **"S"** under **"Fluidic test"** means when the liquid is sucked in the channel by applying a negative pressure with a syringe, **"P"** under **"Fluidic test"** means when the liquid is pushed in the channel by applying a positive pressure with a syringe.

Sputtered Aluminum Nitride

Bonding on sputtered aluminum nitride is tested. After many tries and different bonding conditions. **The PDMS doesn't bond to Aluminum Nitride** at all. Liquid test cannot be done.

Thermal Silicon Oxide

Thermal silicon Oxide layer is tested and results are given in Table 2. A cleaned wafer from CMi with thermal silicon oxide layer is taken.

		Wall width	**Wall width**	**Wall width**

Channel Width [mm]	Time [s]	0.5 [mm]			1 [mm]			2 [mm]		
		Irreversible Bonding	Fluidic Test		Irreversible Bonding	Fluidic Test		Irreversible Bonding	Fluidic Test	
			S	P		S	P		S	P
0.5	30	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
	60	No	No	No	Yes	Yes	No	Yes	Yes	Yes
0.75	30	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
	60	No	No	No	Yes	Yes	No	Yes	Yes	Yes
1	30	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
	60	No	No	No	Yes	Yes	No	Yes	Yes	Yes

Table 2 - Bonding test of PDMS channel on thermal silicon oxide layer. Under the liquid test, S shows the liquid test when the liquid is sucked in the channel (negative pressure) P shows the liquid test when the liquid is pushed in the channel (positive pressure).

The bonding on the thermal silicon works for a wall width of 2 mm with all the different applied conditions. The 1 mm wall width channel fails the liquid test when bonding is done 60 seconds after the plasma exposure and when the liquid is pushed in the channel. The 0.5 mm wall width channel fails all the test when there is a waiting time of 60 seconds after the plasma exposure. The 0.5 mm wall width channel also fails the push in test after a waiting time of 30 seconds. We can see that the width of the channel has no influence on the quality of the bonding because it has no influence on the area of the bonding. Therefore, in the following tests, the same width of channel is considered.

Sputtered Silicon Oxide

Sputtered silicon oxide is tested. In fact, to have a good PDMS bonding, the roughness of the substrate should be low. The roughness of the thermal silicon oxide is lower than the sputtered one. So, we can expect that the bonding of PDMS on sputtered silicon oxide can be less good. However, to have sputtered silicon oxide would simplify the process flow of the contour mode resonator because it can be deposit on top. To have a silicon oxide layer, an old wafer of the lab made by Andrea with CMR is taken. 200 nm of low rate deposition silicon oxide is deposited (Details of thin films deposition go in "HR 1 already released structures" on page 55) . Then the bonding tests are done. The **PDMS doesn't bond to sputtered silicon oxide at all.** The reason why bonding doesn't work is because that Andrea's design has a lot of relief. In fact, the design has some depth difference of the scale of few micrometers. Thus, the condition of bonding is bad.

Uncooked PDMS for symmetric channel

The idea is to lower the time of cook of the PDMS in the hoven at 1h30 instead of 3h. Therefore, the PDMS will be softer and some uncooked PDMS remains on the surface of the channel. This

allows the PDMS to fit better on the sputtered silicon oxide surface. Plus, the residues of uncooked PDMS is sticky and can help the bonding. So, the same bonding tests are done with uncooked PDMS.

Aluminum nitride

The **bonding of the uncooked PDMS on aluminum nitride doesn't work**. It means that, in these condition (plasma exposure parameters, waiting time after exposure), aluminum doesn't react with PDMS.

Thermal silicon oxide

Tests are done on the same wafer as the previous tests on the thermal silicon oxide wafer of CMi. Results of bonding are shown in Table 3.

Time [s]	Wall width 0.5 [mm]			Wall width 1 [mm]			Wall width 2 [mm]		
	Irreversible Bonding	Liquid Test		Bonding	Liquid Test		Bonding	Liquid Test	
		S	P		S	P		S	P
30	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
60	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes

Table 3 - Bonding test of uncooked PDMS channel on thermal silicon oxide layer. Under the fluidic test, S shows the liquid test when the liquid is sucked in the channel (negative pressure), P shows the fluidic test when the liquid is pushed in the channel (positive press

When the PDMS is uncooked, the test shows better results. In fact, the uncooked PDMS doesn't fail the Irreversible bonding for 0.5 mm wall width channel with a waiting time of 60 seconds after plasma exposure, plus the suck in test on the 0.5 mm wall width channel succeeds with the waiting time of 60 seconds after plasma exposure.

Sputtered silicon oxide

This time, no old wafer is taken but a test wafer of CMi is taken to avoid reliefs on the surface of the wafer. 200 nm of low rate deposition silicon oxide is deposited on the wafer (see fabrication details in the appendices *"Test wafer #69843 bonding test"*) on page 56. Bonding test is done and results are shown in Table 4. Notice that, in this test, the assembly is also put on the hot plate at 80 C°.

Time [s]	Wall width 0.5 [mm]		Wall width 1 [mm]		Wall width 2 [mm]	
	Irreversible Bonding	Fluidic Test	Irreversible Bonding	Fluidic Test	Irreversible Bonding	Fluidic Test

		S	P		S	P		S	P
30 hoven	No	Yes	Yes	Middle	Yes	Yes	Middle	Yes	Yes
30 Hot plate	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
60 Hot plate	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes

Table 4 - Bonding test of uncooked PDMS channel on sputtered silicon oxide layer. Under the fluidic test, S shows the liquid test when the liquid is sucked in the channel (negative pressure), P shows the fluidic test when the liquid is pushed in the channel (positive pressure).

There is clearly an improvement of the results. In section "Sputtered Silicon Oxide" in page 27, PDMS irreversible bonding doesn't work on sputtered silicon oxide. Uncooked PDMS improves the bonding. The fact that the wafer has no relief at the order of few microns makes a better contact between the PDMS and the silicon oxide. Moreover, putting the PDMS on a hot plate after plasma exposure and waiting time improves the quality of the bonding because it is possible to maintain the pressure correctly on the whole contact area of the assembly. In fact, putting the assembly in the hoven with weight can create some issues: The weight is not well distributed on the whole area and it means that some part of the wall contact of the channel are not bonded.

Discussion

To conclude, to obtain a good bonding, the PDMS should be cooked for 1h30, so that uncooked PDMS is obtained. Therefore, the surface is sticky and the PDMS is softer and can fit better to the area of the sputtered silicon oxide. Moreover, just after the bonding, it is better to put the PDMS on a hot plate at 80 C° and maintain the pressure (with the hands) to make a good contact between the two surfaces to bond. Then, the bonding of the channel with a wall width of 0.5 mm is not good enough to bring liquid. Therefore, the minimum width to have is 1 mm. So, the minimum **distance between the pads and the resonator is set to 2 mm** to have margin to align the channel. Another remark is about the channel height. In fact, if the maintained pressure on the hot plate is too strong, there is a risk that the ceiling of the channel touches the resonator. This would be dramatic because it can make a bonding between the ceiling of the channel and the resonator. Thus, the resonator cannot be used anymore. Therefore, in the following tests, the channel height is increased.

Asymmetric PDMS channel

If the 1-port CMR design is used, there is only the pads at one side of the resonator. Therefore, the wall width is constrained only on one side of the resonators (see Figure 19). There isn't any constrains on the other side, consequently the wall width can be bigger. The idea is to try different wall width on the bigger side while having a wall width of 1 mm on the pads side (see in last section *"Discussion"* on page 29). Uncooked PDMS and the hot plate technic is used. The goal of this design is to have a stronger and more reliable irreversible bonding. This is called the asymmetric PDMS channel.

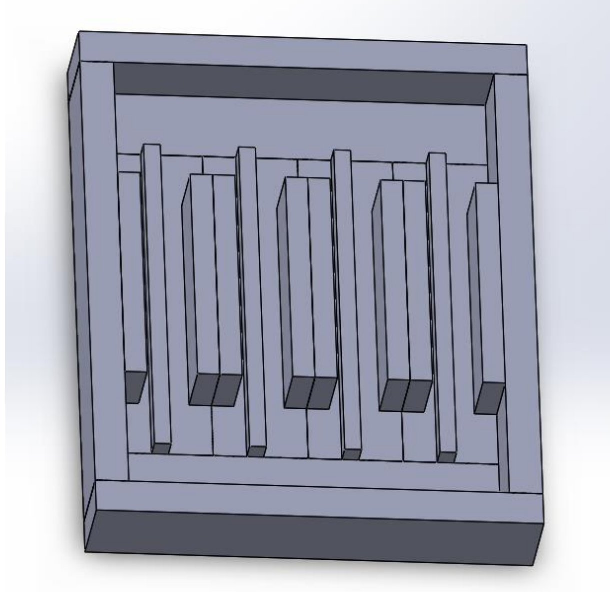


Figure 25 – Negative mold of the asymmetric channels with a pads side wall width of 1 mm. The other side wall width is (from left to right) 2 mm, 3 mm, 4 mm, 5 mm. The channel height is 1.5 mm.

A mold with 4 different channels is made with the following dimension:

Pads side wall width: 1 mm.
Other side wall width: 2 mm, 3 mm, 4 mm, 5 mm.
Channel height: 1.5 mm

The channel height is increased because there is a possibility that the ceiling of the channel touches the resonator when pressure is maintained between channel and the substrate.

Figure 25 shows the negative mold to do asymmetric PDMS channel. The sacrificial space between the end of channels and the wall of the mold (flat part) is important to make the peeling off of the PDMS easier.

Table 5 shows the results of the bonding test of the asymmetric channels

Other side (from the pads) wall width											
2 mm			3 mm			4 mm			5 mm		
Irrever. Bonding	Fluidic Test		Irrever. Bonding	Fluidic Test		Irrever. Bonding	Fluidic Test		Irrever. Bonding	Fluidic Test	
	S	P		S	P		S	P		S	P
Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 5 - Bonding test of asymmetric and uncooked PDMS channel on sputtered silicon oxide layer. Under the fluidic test, S shows the liquid test when the liquid is sucked in the channel (negative pressure), P shows the fluidic test when the liquid is pushed in the channel (positive pressure).

Results in Table 5 show that all the different channel bond well to the sputtered silicon oxide. Moreover, all the channels pass both fluidic test with success. The height of the channel is big enough to avoid that the ceiling of the channel touches the resonator.

Discussion

All the different asymmetric channels pass successfully the test condition described in section "*Bonding and liquid test on different design of channel and different substrate*." on page 26. For the future design of the wafer. The wall width of the pads side of the channel is 1 mm thick. The width of the other side is at least 3 mm to assure a good and reliable bonding. So, the **pads are 2 mm away from the resonator** to have margin to align the channel on the resonator. Sputter deposited silicon oxide is the chosen surface to bond the PDMS.

Process flow changes

Sputter deposited silicon oxide is needed on top of the design. When the top gold plate is deposited, a silicon oxide layer is sputter deposited as hard mask. The idea is to deposit a thick layer and let the silicon oxide where the channel has to bond. This layer is protected with the pads protection mask layer (see Figure 26 image (e)). Just after the release, there is still the pads and wall contact protection mask. Dry etch with HF vapor is done to remove the silicon oxide on the gold plate (Figure 26 image (f)).

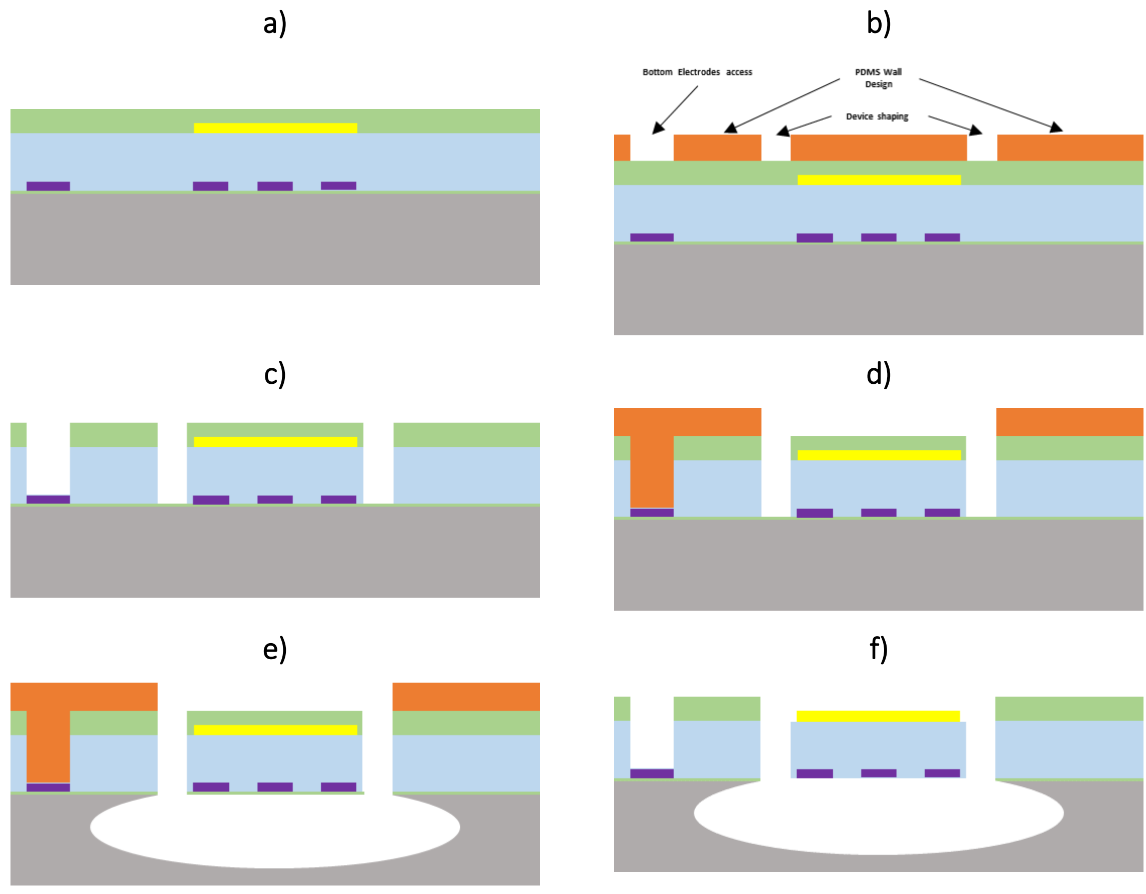


Figure 26 – Process flow changes to have a top sputter silicon oxide layer to be able to bond a PDMS channel on: (a) After the lift off patterning of gold, hard mask silicon oxide is sputter deposited. This layer is also used to bond the channel; (b) Coating and exposure of the photoresist for the device shaping, the channel wall contact protection and the bottom pads access; (c) Etching of the hard mask + etching of the aluminum nitride until the silicon oxide is reached; (d) Coating and exposure of the photoresist to protect the pads and the sputtered silicon oxide top layer; (e) Etching of the silicon oxide + anisotropic etching of silicon (bosh process) + release of the resonator with isotropic etching of the silicon; (f) Dry etching of the silicon oxide with vapor HF. The photoresist is then removed.

3.4 Changes of the behavior of the resonator

This chapter discusses about the electric change of the resonator behavior due to the design changes made on the previous chapters.
The model of the resonator can be defined only by electronic components. Figure 27 shows the electronic model of the resonator.

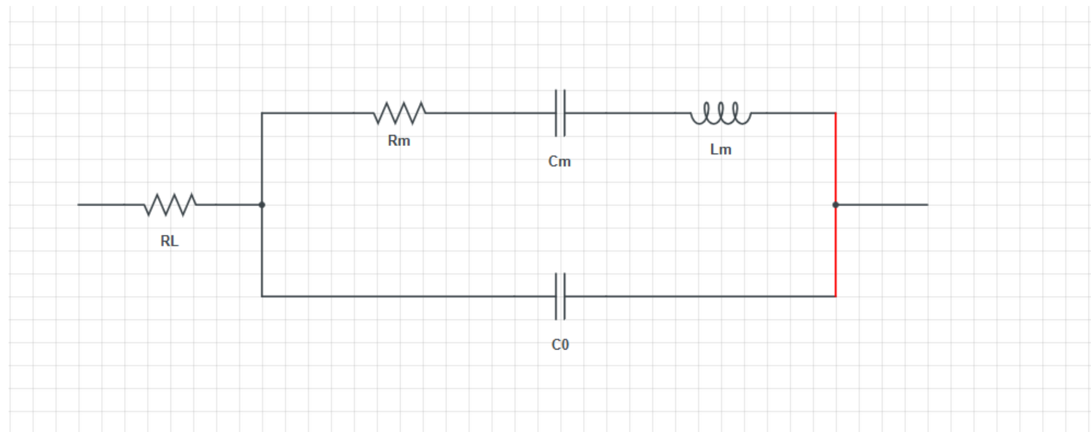


Figure 27 – Electronic circuit model of the resonator: Rm, Cm and Lm are respectively the motional resistance, capacitance and inductance of the resonator. It describes the internal properties of the resonator. C_0 is the so-called parasitic capacitance generated between the electrodes of the resonator, tracks and pads. Electrical loading is defined by R_L and is the resistance of the tracks which link the resonator to the pads.

As defined in the last chapter (see section 3.3) the tracks which electrically link the resonator to the pads is longer. It increases the loading resistance R_L and the parasitic capacitance C_0 of the resonator. So, more power is lost in the R_L resistance and more current flows in the capacitance C_0 for the same working frequency. It means that less power is transmitted to the resonator.

Calculation of the loading resistance and the parasitic capacitance

To calculate R_L the general formula to calculate resistances is used:

$$R_L = \rho \frac{L}{W \cdot T} \tag{7}$$

ρ is the resistivity of the material, L, W and T are respectively the length, the width and the thickness of the track.

The circuit used to define the loading resistance is shown in Figure 28.

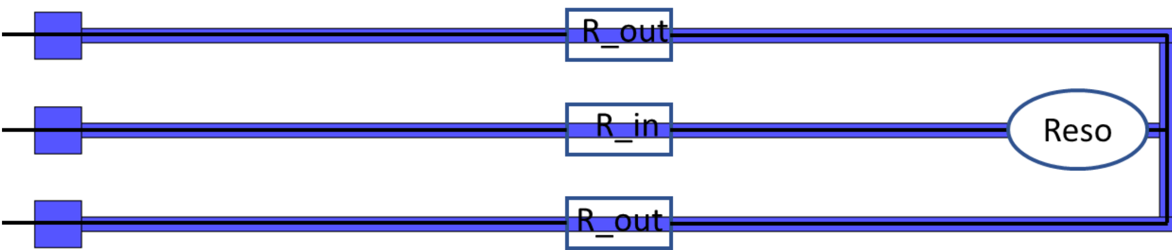


Figure 28 - Circuit for the calculation of R_L loading resistance. The resistance created by the interdigitated fingers electrodes is neglected.

The overall loading resistance is thus:

$$R_L = R_{in} + \frac{R_{out}}{2} \tag{8}$$

To calculate C_0, the general formula to calculate capacitance is used:

$$C_0 = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{9}$$

ε_0 is the vacuum permittivity, ε_r is the relative permittivity of the material between the electrodes, A is the area defined by the electrodes (here defined by $W \cdot L$) and d is the distance between the electrodes.

The circuit used to define the parasitic capacitance is shown in Figure 29

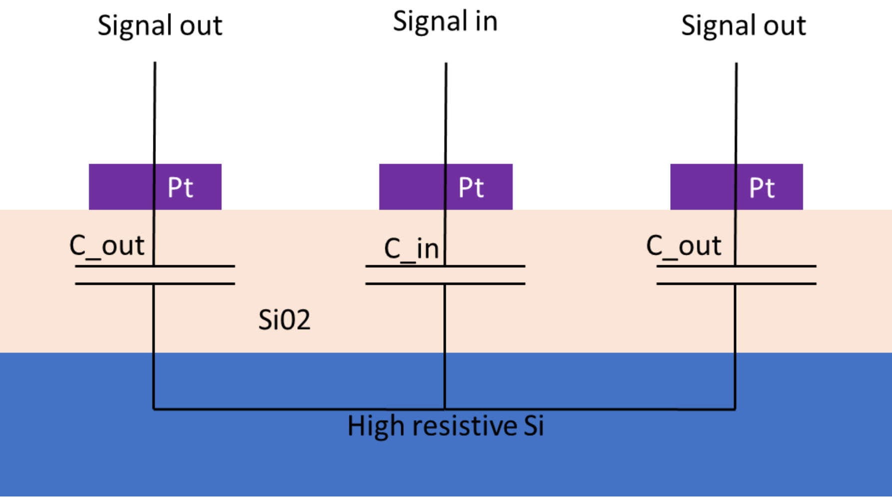


Figure 29 – Circuit for the calculation of C_0 parasitic capacitance. The high resistive silicon is considered as a conductive material. The capacitance created by the interdigitated fingers electrodes is neglected.

The overall C_0 capacitance is thus:

$$C_0 = \frac{2C_{out} \cdot C_{in}}{2C_{out} + C_{in}} \tag{10}$$

Table 6 shows the necessary values to compute the parasitic capacitance and the loading resistance.

	In signal track	Out Signal Track
$\boldsymbol{\rho_{Pt}}$ $[\boldsymbol{\Omega m^{-1}}]$	$1.035 \cdot 10^{-7}$	$1.035 \cdot 10^{-7}$
$\boldsymbol{L}$ $[\boldsymbol{mm}]$	2.1	2.5
$\boldsymbol{W}$ $[\boldsymbol{\mu m}]$	100	100
$\boldsymbol{T}$ $[\boldsymbol{nm}]$	50	50
$\boldsymbol{\varepsilon_0}$ $[\boldsymbol{Fm^{-1}}]$	$8.854 \cdot 10^{-12}$	$8.854 \cdot 10^{-12}$
$\boldsymbol{\varepsilon_{SiO_2}}$	3.9	3.9
$\boldsymbol{d}$ $[\boldsymbol{nm}]$	250	250
$\boldsymbol{R_L}$ $[\boldsymbol{\Omega}]$	43.5	51.8
$\boldsymbol{C_0}$ $[\boldsymbol{pF}]$	29.1	34.5

Table 6 – Necessary parameters to calculate $\boldsymbol{R_L}$ and $\boldsymbol{C_0}$.

Table 7 shows the comparison between the values from Andrea's design and the Project's design with the value taken in Table 6.

	R_L $[\Omega]$	C_0 $[pF]$
Andrea's design	7.8	1.6 (1 experimentally)
Project's design	69.3	20.4

Table 7 - Comparison of the value of $\boldsymbol{R_L}$ and $\boldsymbol{C_0}$ between Andrea's design and the Project design.

The loading resistance and the parasitic capacitance increases dramatically. It decreases strongly the quality factor of the resonator and it transmitted power.

Change of the C_0 capacitance

This section focus on the change of the C_0 capacitance and its impact. According to the process flow, there are 2 ways of reducing the C_0 capacitance:

- Reduce the Area
- Increase the distance d between the two electrodes of the capacitance

To reduce the area, the track width is reduced, to increase the distance d. The thickness of the thermal silicon oxide layer is increased.

Figure 30 shows the plot of the C_0 parasitic capacitance in function of the track width and the thickness of the silicon oxide layer.

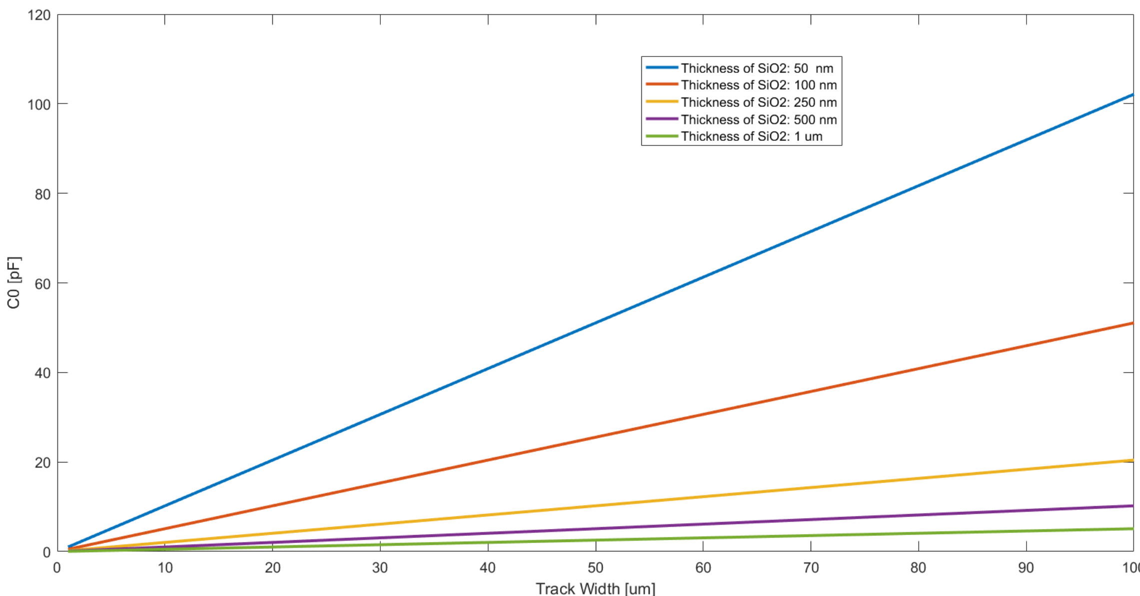


Figure 30 – Plot of the parasitic capacitance C_0 in function of the track width in "x axes" and the thickness of the silicon oxide layer in different colors.

To strongly reduce the C_0 parasitic capacitance, **a track width of 30 µm is chosen** and a layer of **1 µm thickness of silicon oxide is deposited.**

Reducing the track width, strongly increases the loading resistance R_L. Figure 31 shows the plot of the platinum track resistance in function of the track width.

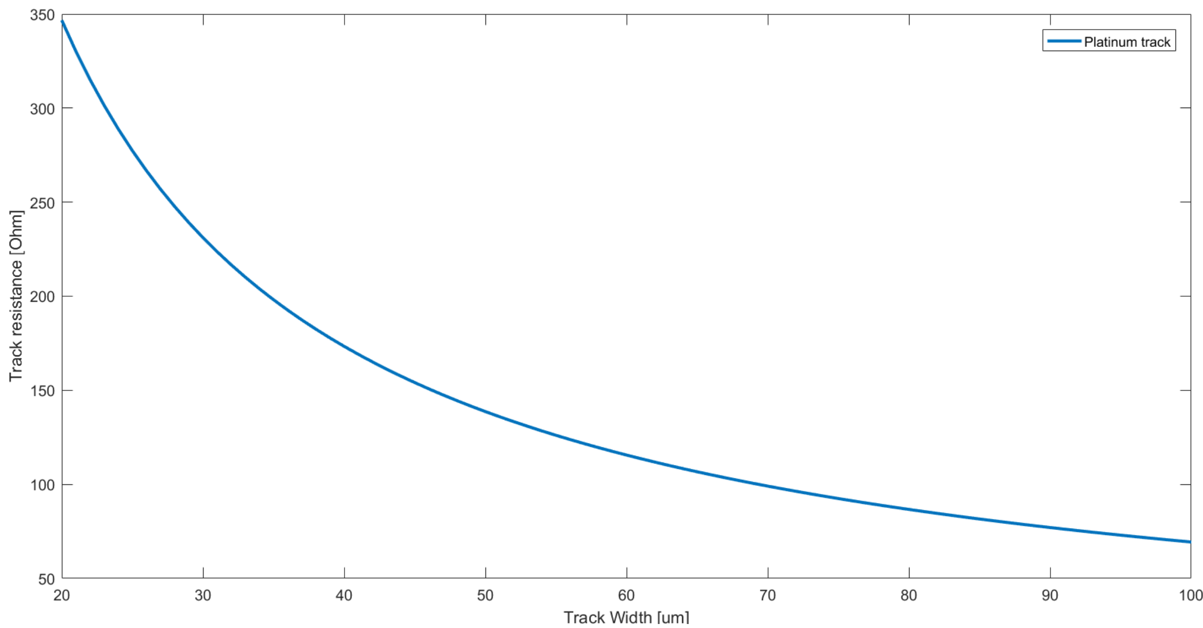


Figure 31 – Plot of the track resistance in function of the track width. The loading resistance increases when the track width is decreased.

Table 8 shows the value of the loading resistance and the parasitic capacitance when the track width is set at 30 µm.

R_L [Ω]	C_0 [pF]
231.2	1.5

Table 8 – Value of the R_L loading resistance and the C_0 parasitic capacitance when the track width is reduced to 30 µm.

Having a high loading resistance is not acceptable because it loads the resonator and it the efficiency of the transmitted power.

Change of R_L Resistance

This section focus on the reducing of the R_L loading resistance. According to the design rules established in the last sections (The length of the track cannot be reduced: see section *"Discussion"* on page *31*; the width of the track is set at 30 µm: see section *"Change of the C0 capacitance"* on page 34). To reduce the loading resistance, the only parameter to change is the thickness of the track. The idea is to add a new mask in the process flow and deposit some aluminum on the platinum. The aluminum is more conductive than the platinum and it increases the overall thickness of the track. Figure 32 shows the plot of the loading resistance in function of the thickness of the aluminum layer on the platinum.

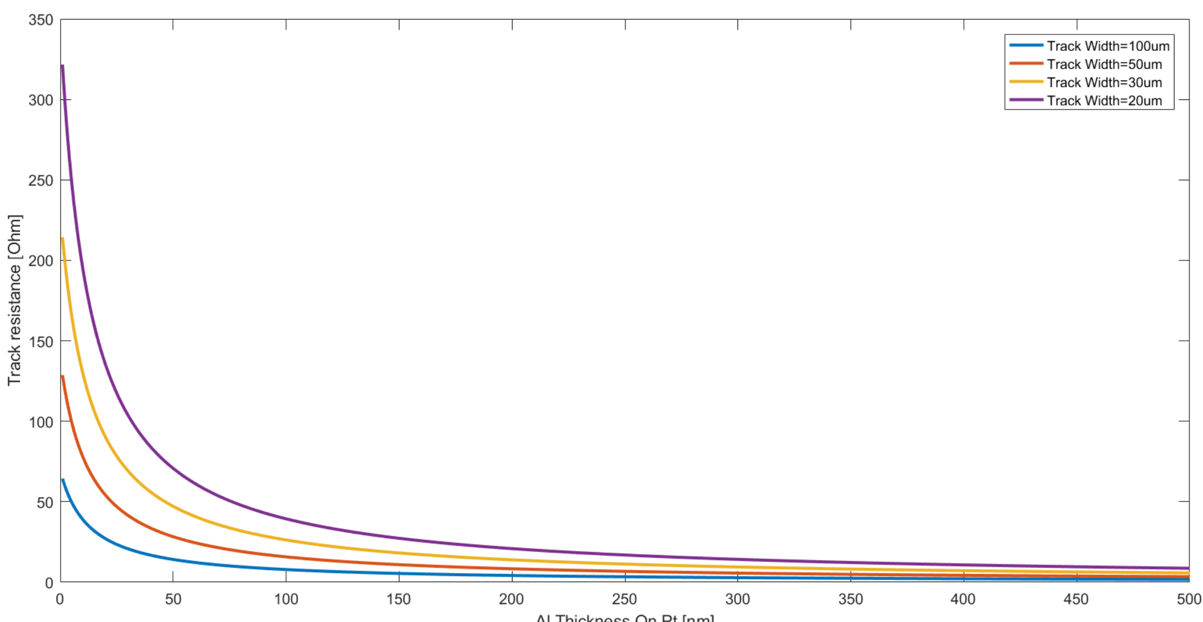


Figure 32 – Plot of the track resistance R_L in function of the thickness of the aluminum deposited on the 50 nm platinum and of the width of the track.

The contact resistance between platinum and the aluminum is neglected. Platinum and aluminum are calculated as if they are electrically in parallel as shown in Figure 33.

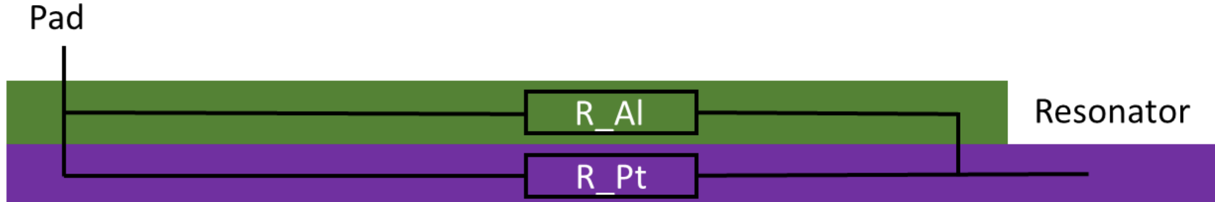


Figure 33 – Schematic that shows how the loading resistance is calculated when an aluminum layer is deposited on the platinum track. Contact resistance is neglected.

Thus, the loading resistance is:

$$R_L = \frac{R_{Al} \cdot R_{Pt}}{R_{Al} + R_{Pt}} \quad (11)$$

The deposition of the aluminum on the platinum lower the track resistance and doesn't change the parasitic capacitance. The thickness of the aluminum layer is set at 300 nm. Table 9 shows the theoretical value of the loading resistance and the parasitic capacitance.

R_L [Ω]	C_0 [pF]
9.5	1.5

Table 9 shows the value of the loading resistance R_L and the parasitic capacitance C_0 when the track width and the thickness of the aluminum layer on the platinum track are set at 30 µm and 300 nm respectively.

The value of the loading resistance is acceptable and is slightly higher than Andrea's design (see Table 7). The disadvantage of increasing the thickness of the aluminum layer is the increasing of the relief of the chip surface. Therefore, the bonding of the PDMS channel is more difficult. However, the depth difference due to the track thickness is not more than 350 nm (50 nm of platinum and 300 nm of aluminum). Moreover, two additional layer are added in the process flow. The soft PDMS can fit on these small changes of depth. The last concern is the wire bonding on aluminum pads. CMi staff says that wire bonding on aluminum pads is one of the most standard method.

Discussion

To decrease the C_0 parasitic capacitance, **the width of the track is decreased to 30 µm**, additionally a **silicon oxide layer of 1 µm is deposited between the high resistive silicon and the bottom platinum layer** (step done by CMi staff). To decrease the R_L loading resistance, an **additional mask is added in the process flow to lift off pattern a 300 nm thick aluminum layer on the platinum track.**

Process flow changes

To add a new layer of aluminum on the platinum track, lift off process flow is used. Consequently, it requires a new mask for the process flow. Figure 34 shows the additional step to do to pattern the aluminum conductive layer.

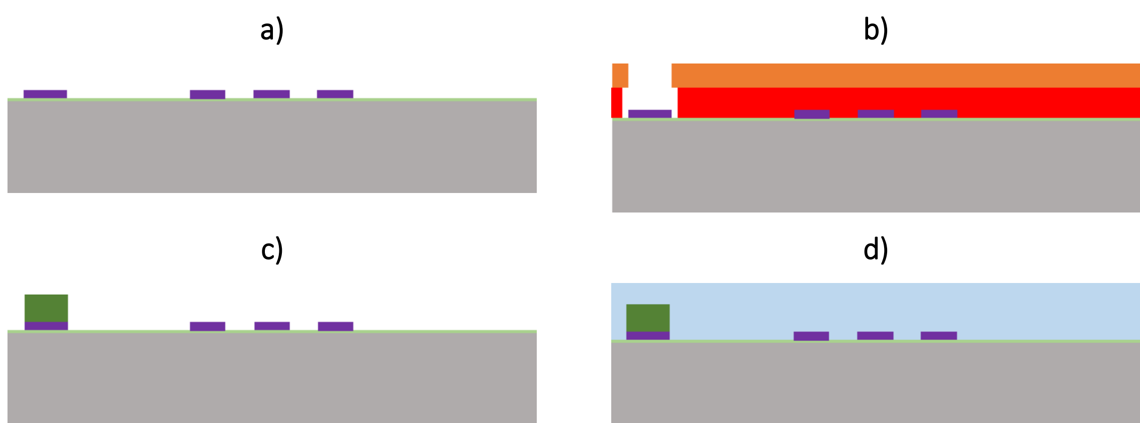


Figure 34 – Process flow changes to add the aluminum layer on the platinum track: (a) The platinum track, pads and interdigitated finger are lift off patterned; (b) Coating and exposure of the AZ1512 photoresist on LOR photoresist; (c) Aluminum is sputtered deposited on the tracks and pads. The photoresists are then removed. (d) We continue with the deposition of the aluminum nitride to deposit the active piezoelectric layer and resonator structures.

This new patterning of aluminum adds some intermediary step in the process flow between the lift off platinum and the sputter deposition of aluminum nitride. The only concern is if there is some residue of photoresist on the platinum of the interdigitated electrodes. The adhesion of the aluminum nitride layer would be bad and the resonator would be less efficient.

4. Final Process Flow

In this chapter, the complete process flow of the CMR resonator of this project is presented. It is a 5 masks process flow and each mask is presented in the following sections:

A more detailed process flow with the design evolution is shown in the appendices. See section “*Process flow and design*” on page 63.

4.2 First mask

The first mask is used to do lift off patterning of the bottom platinum interdigitated electrodes, track and pads.

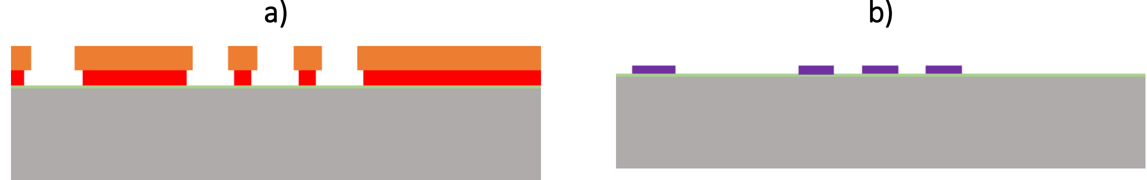


Figure 35 – First mask of the final process flow of the project: A high resistive intrinsic silicon wafer with 1 µm wet oxide is taken. (a) Coating and exposure of the AZ1512 resist on LOR photoresist; (b) Platinum is sputtered deposited and the photoresists are then removed.

4.3 Second mask

The second mask is used to do lift off patterning of the aluminum conductive layer on top of the platinum pads and tracks.

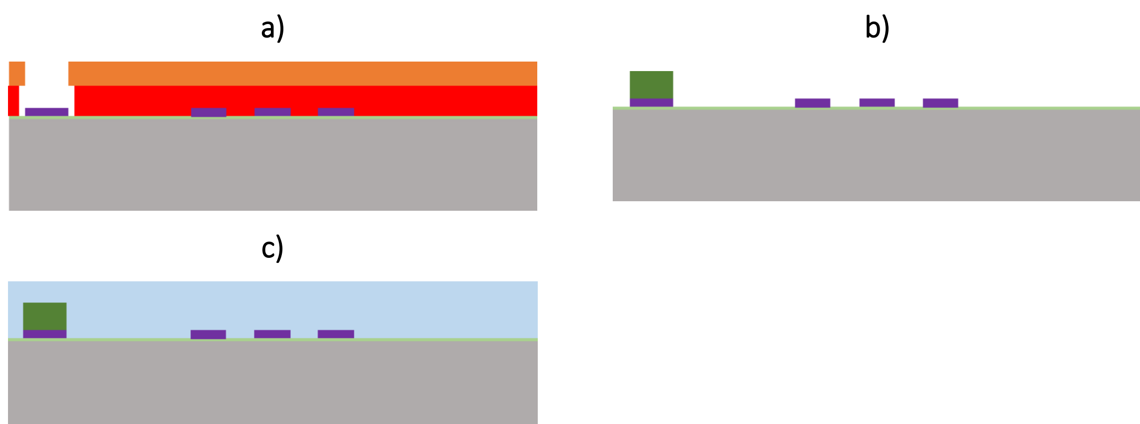


Figure 36 – Second mask of the final process flow of the project: (a) Coating and exposure of the AZ1512 photoresist on LOR photoresist; (b) Aluminum is sputtered deposited on the tracks and pads. The photoresists are then removed; (c) We continue with the deposition of the aluminum nitride to deposit the active piezoelectric layer and resonator structures.

4.4 Third mask

The third mask is used to lift off patterning of the top gold plate electrode.

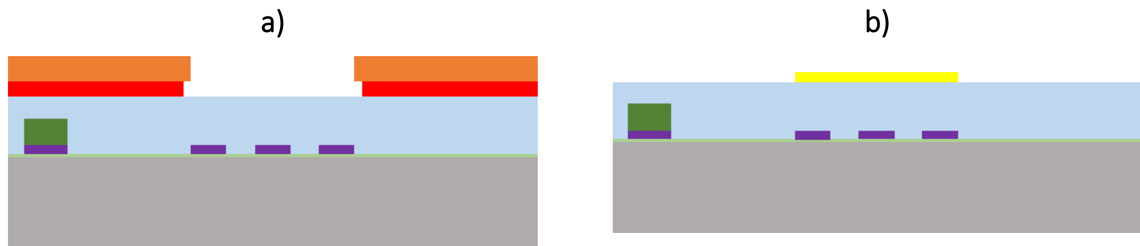
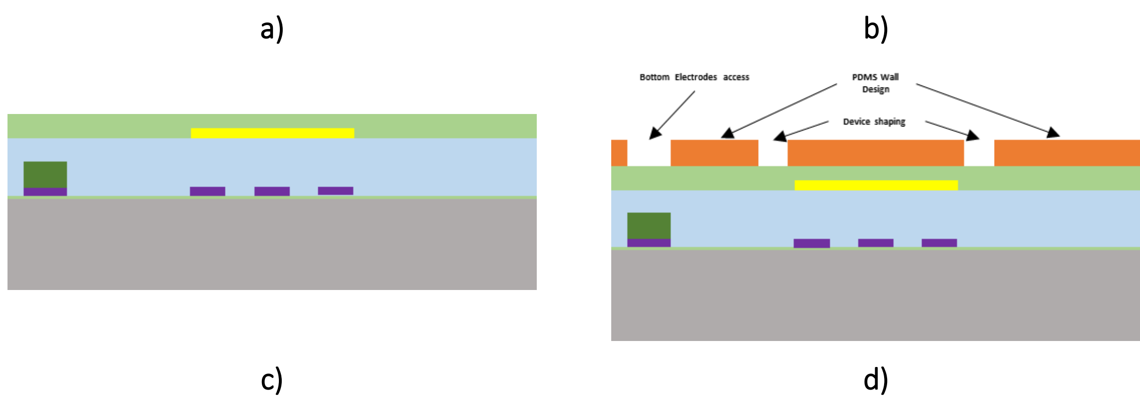


Figure 37 - Third mask of the final process flow of the project: (a) Coating and exposure of the AZ1512 photoresist on LOR photoresist; (b) Top Gold plate electrode is deposited by evaporation. The photoresists are then removed.

4.5 Fourth mask

The fourth mask is used to design the resonator shape, to have access to the bottom pads and to protect the silicon oxide surface where the PDMS must bond during the etching.



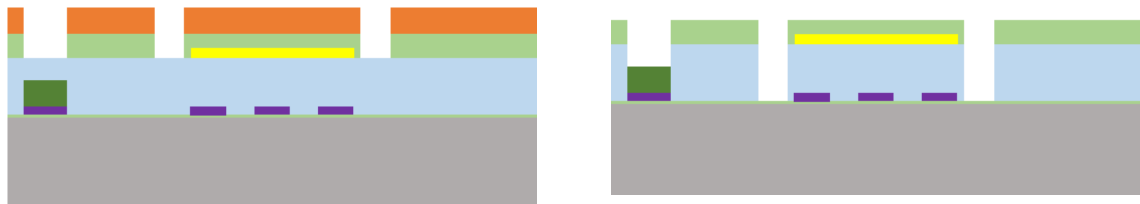


Figure 38 - Fourth mask of the final process flow of the project: (a) Hard mask silicon oxide is sputter deposited. This layer is also used to bond the channel; (b) Coating and exposure of the photoresist for the device shaping, the channel wall contact protection and the bottom pads access; (c) Etching of the hard mask; (d) Etching of the aluminum nitride until the silicon oxide is reached; (d)

4.6 Fifth mask

The fifth mask is used to protect the bottom pads and the silicon oxide surface where the PDMS must bond.

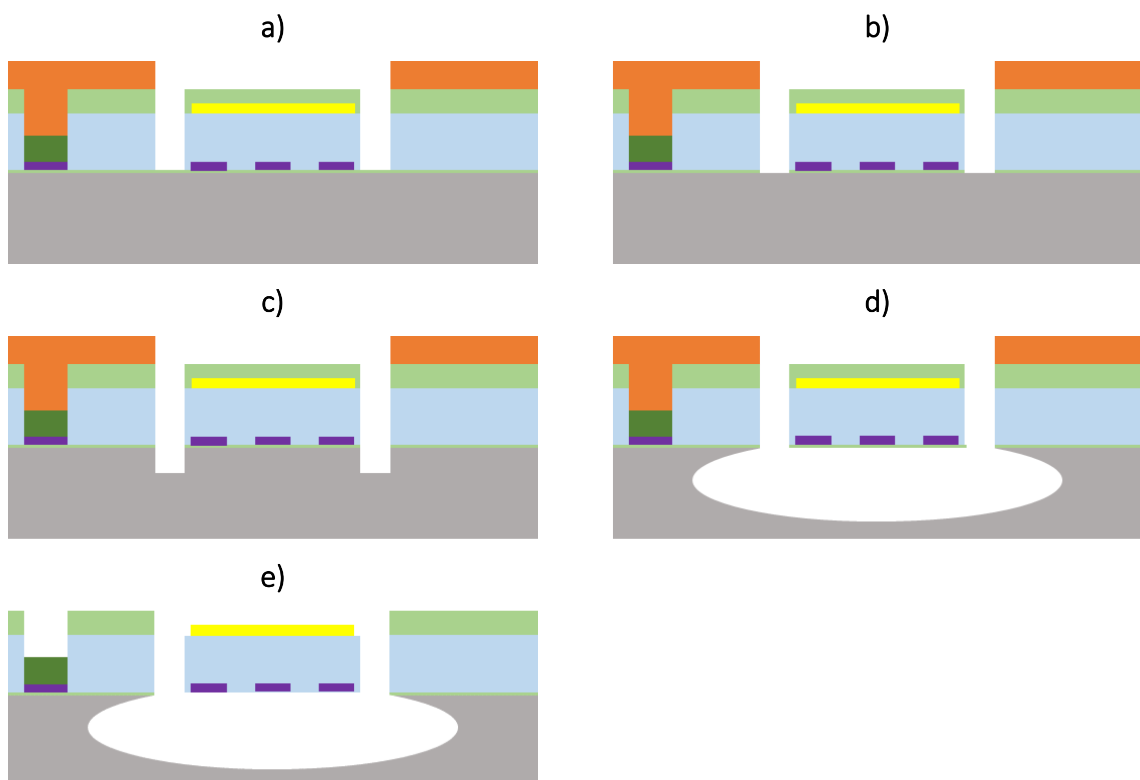


Figure 39 – Fifth mask of the final process flow of the project: (a) Coating and exposure of the photoresist to protect the pads and the sputtered silicon oxide top layer; (b) Etching of silicon oxide until silicon is reached; (c) Anisotropic etching of silicon (bosh process); (d) Isotropic etching of silicon to do the release of the resonator; (f) Dry etching of the silicon oxide with vapor HF. The photoresist is then removed.

5. Simulations and design settings

This chapter discusses about the resonator dimension to set according to the result of the CMR simulations. The aim of the simulations is to find the best quality factor. It focuses on the length of the resonator, the anchor width and the anchor length optimization. A dedicated software is used and simulates one quarter of the resonator and the rest is simulated by symmetry. Simulation

files of Andrea are taken. Figure 40 shows the results of one simulation and shows how the CMR is built. The simulated CMR is an aluminum nitride layer sandwiched between a platinum 3 fingers interdigitated electrodes and a platinum plate.

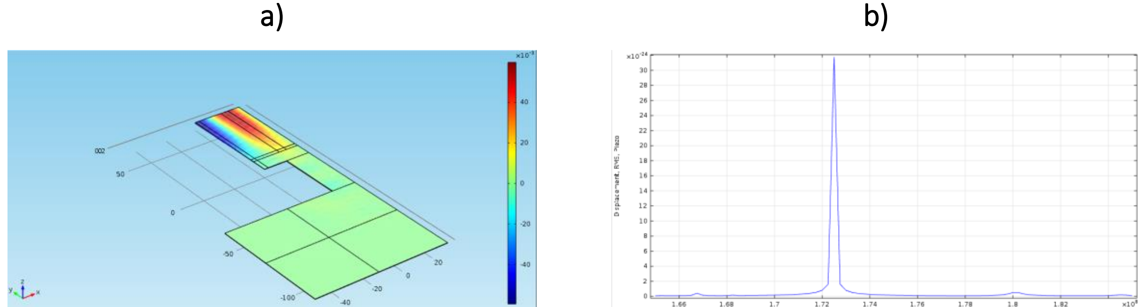


Figure 40 – (a) Picture of the simulation result of one quarter of the CMR. Colors show the displacement of the material in the "x" direction. The figure shows the resonance frequency of a CMR. The red zone is mostly between the electrodes (higher displacement in "x"); (b) Plot of the root mean square displacement of the CMR in "x" direction (in the red zone in the (a) image) in function of the frequency which correspond to the resonance frequency mode in the image (a).

5.1 Parameters and sweeping

Swept parameters

The length of the resonator, the width of the anchor and the length of the anchor are the parameter to sweep. In fact, acoustic waves losses are highly dependent on these parameters. They can go through the anchor and are lost in the bulk called the perfectly matched layer. Table 10 shows the values of the swept parameters.

Parameter	Min [µm]	Max [µm]	Step [µm]	# Step
$L_{resonator}$	130	150	2	11
W_{anchro}	10	30	2	11
L_{anchor}	20	40	5	5

Table 10 – Values of the swept parameters

3 different thicknesses of the aluminum nitride are simulated. Table 11 shows their values.

$\boldsymbol{T_{AlN}\ [nm]}$	100	250	500

Table 11 - Values of the different thicknesses of aluminum nitride for the simulation

Fixed parameters

$\boldsymbol{T_{electrodes}}$	50 nm
$\boldsymbol{W_{resonator}}$	60 µm
$\boldsymbol{Pitch}$	20 µm
$\boldsymbol{Bus}$	10 µm

$W_{electrodes}$	15 µm (75% of the pitch)
W_{PML}	40 µm
L_{PML}	40 µm

Table 12 - Relevant parameters for the simulation of the CMR

5.2 Simulation results

Simulation of all the swept parameters is done and all the results are given in the appendices in *"Results of the simulations"*. Only some relevant results are shown in this section.

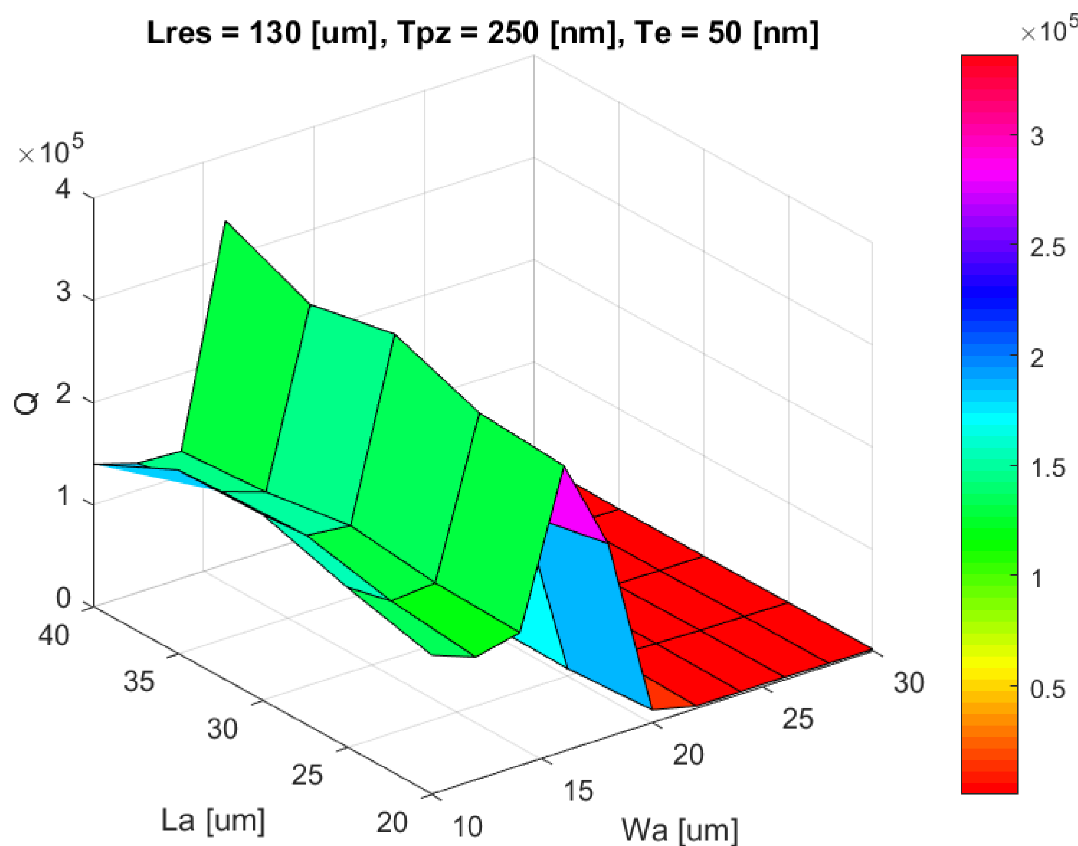


Figure 41 – Simulation results of a resonator length $L_{resonator}$ of 130 µm.

Figure 41 shows that there is an optimum anchor width to maximize the quality factor. For the fabrication, this optimum value must be found. Knowing that there are differences between simulations and experimental results, different width of anchor is chosen for the design of the resonators. 2 different anchor lengths are chosen and the resonator length is fixed at 130 µm.

5.3 Parameters sweeping for the final designs

Find the wafer organization in the appendices (see section *"**Error! Reference source not found.**"* on page **Error! Bookmark not defined.**). Table 13 shows the sweeping parameters for the design mask for the CMR.

Parameter	Min [µm]	Step [µm]	Max	#
W_{anchor}	10	3	28	7
L_{anchor}	Twice 20	20	Twice 40	4
Pitch	18.5	0.5	21.5	8

Table 13 - Parameters sweeping for the final design

As said in the chapter *"Simulation results"* on page 42, the anchor width is swept to find the it optimum value to maximize the quality factor of the CMR. 2 anchor lengths are chosen and the pitch is swept from 18.5 µm to 21.5 µm. It is one of the advantages of CMR to have different resonance frequency on the same wafer which depends on the pitch of the electrodes. One chip of the wafer contains 8 resonators with every different pitch. The channel covers one chip. Consequently, space is needed above and below each chip for the channel outlet and inlet. One dye contains 4 chips in which the anchor length is swept. The wafer contains 8 dies to sweep the anchor length. One dye on the wafer (see section *"Wafer organization"* on page *71*.) is called special dye. This special dye contains chips of resonators in which, the ground signal of all the resonators is connected and the entry signal of all the resonators is connected. The aim of this design is to be able to measure every resonator by probing only once. It is doable because the resonators of one chip have all different pitches thus different resonance frequency. The drawback of this technic is the fact that the parasitic capacitance, generated by tracks, is dramatically increased.

6. Fabrication

The fabrication of the CMR is done on a high resistive wafer with 1 µm of wet oxide thermalized at 1250°C.

6.1 Dose test

Coating of 620 nm AZ1512 photoresist on 480 nm LOR photoresist is done on the wet oxide layer of the high resistive wafer. Exposure of the photoresist is done with different doses. Figure 42 shows the mask design for the dose test.

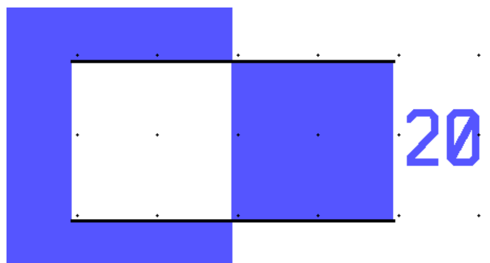


Figure 42 – Mask design of one of the structure to do dose test: The exposed design is in blue. To have the right dose, edge of the structure must follow the black line.

To succeed the dose test, the edges of the structure must follow the straight black line in Figure 42. If the exposed area (white square) is bigger than the non-exposed area (blue square), the photoresist is over exposed. In the reversed case, the photoresist is under exposed.

Exposure parameter:

- Dose:

Min	Step	Max	#
$20 \frac{mJ}{cm^2}$	$5 \frac{mJ}{cm^2}$	$130 \frac{mJ}{cm^2}$	23

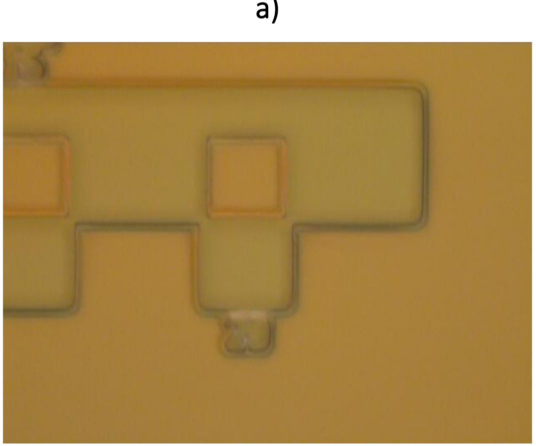
- Defoc: -3
- Wavelength $405\ nm$
- Design width:

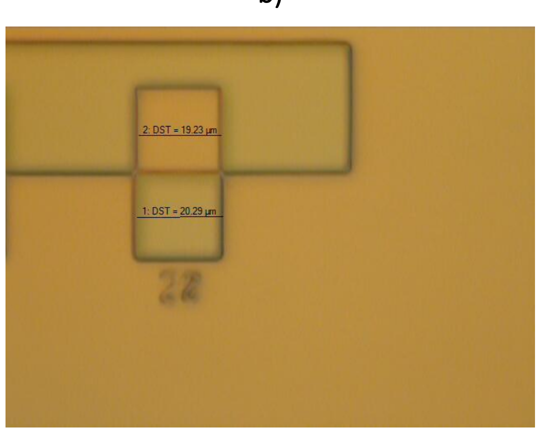
Min	Step	Max	#
$1\ \mu m$	$1\ \mu m$	$20\ \mu m$	20

Then the photoresist is developed twice with the corresponding photoresist recipe.

Figure 43 shows the result of the same design after the 2 times development with different exposure doses.

a) b)





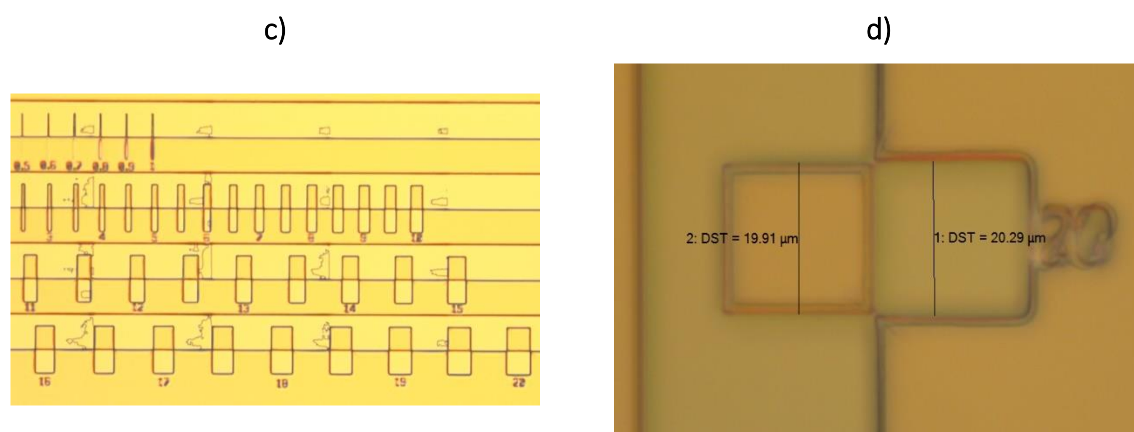


Figure 43 – Dose test results: (a) 20 µm width structure with a dose of $\mathbf{100}\,\frac{mJ}{cm^2}$. The photoresist is over exposed because the exposed area is bigger; (b) 20 µm width structure with a dose of $\mathbf{20}\,\frac{mJ}{cm^2}$. The photoresist is well exposed because the edge of the structure follows a straight line; (c) Dose of $\mathbf{20}\,\frac{mJ}{cm^2}$ shows some concerns with some photoresist left between designs. It may be underexposed; (d) 20 µm structure with a dose of $\mathbf{30}\,\frac{mJ}{cm^2}$. The photoresist is well exposed because the edge of the structure follows a straight line.

Figure 43 (b) shows that the $20\,\frac{mJ}{cm^2}$ is the correct exposure dose for the first mask and the dimensions of the structure are correct. However, image (c) shows some concerns because there are some residues left between the structures which is a sign of under exposure. Image (d) shows that the exposure dose of $30\,\frac{mJ}{cm^2}$ is correct and there is no residue of photoresist on the design.

6.2 First mask fabrication

Exposure results

A high resistive wafer with a wet oxide layer of 1 µm is taken and is exposed to design the bottom electrode, tracks and pads layer. The wafers are coated, exposed and twice developed. Figure 44 shows the results after the twice development for an exposure dose of $20\,\frac{mJ}{cm^2}$. Dose of $20\,\frac{mJ}{cm^2}$ is anyway tried because the signs of under exposure were considered as low. The detailed fabrication and machine parameter are in the appendices in the section *"HR wafer 54 oxide 1um fabrication"* on page *56*.

a) b)

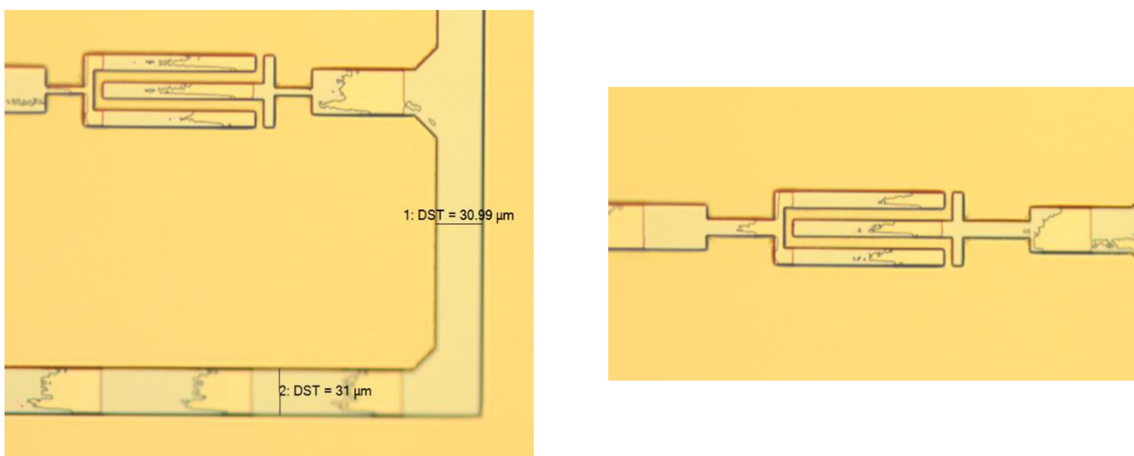
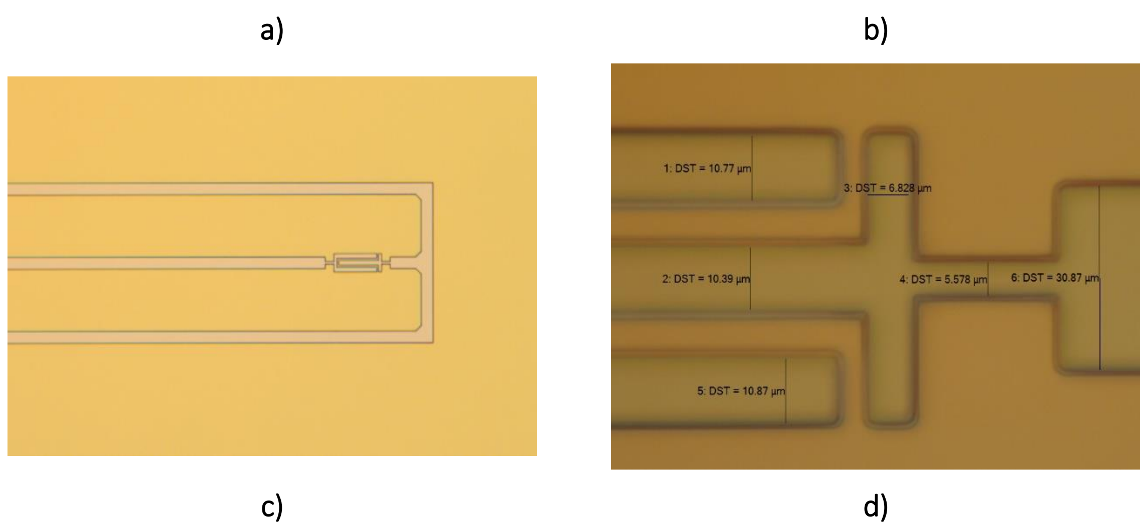


Figure 44 – The 2 images contain some residue of photoresist and some vertical lines which is clearly a sign of under exposure of the mask. (a) Track and interdigitated electrodes; (b) Interdigitated electrodes.

The photoresist is clearly underexposed. Vertical lines and residues of photoresist remains in the design where it shouldn't. Process is not kept on for this wafer.

Figure 45 shows the results after the twice development for an exposure dose of $30\,\frac{mJ}{cm^2}$. The detailed fabrication and machine parameter are in the appendices in the section *"HR wafer 55 oxide 1um fabrication"* on page57.



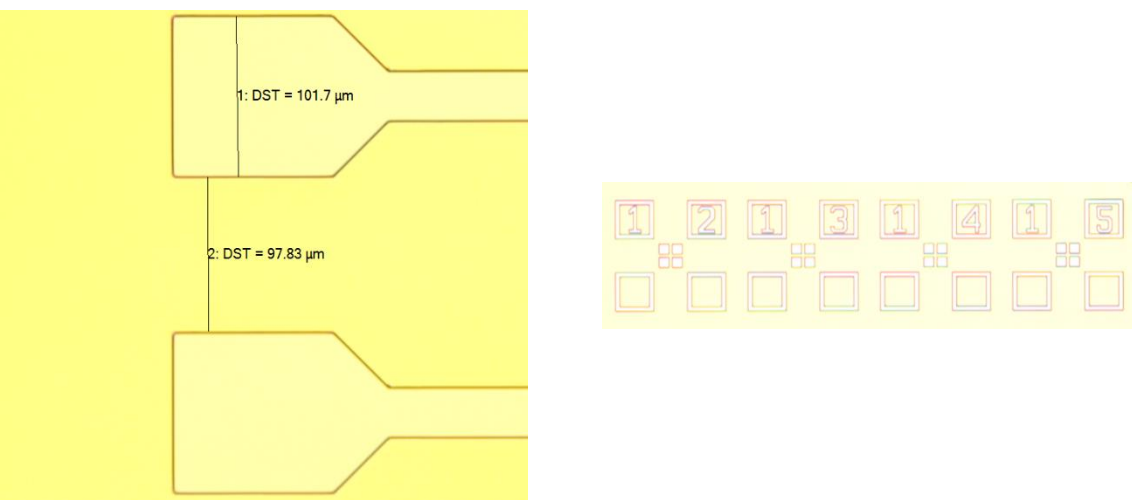
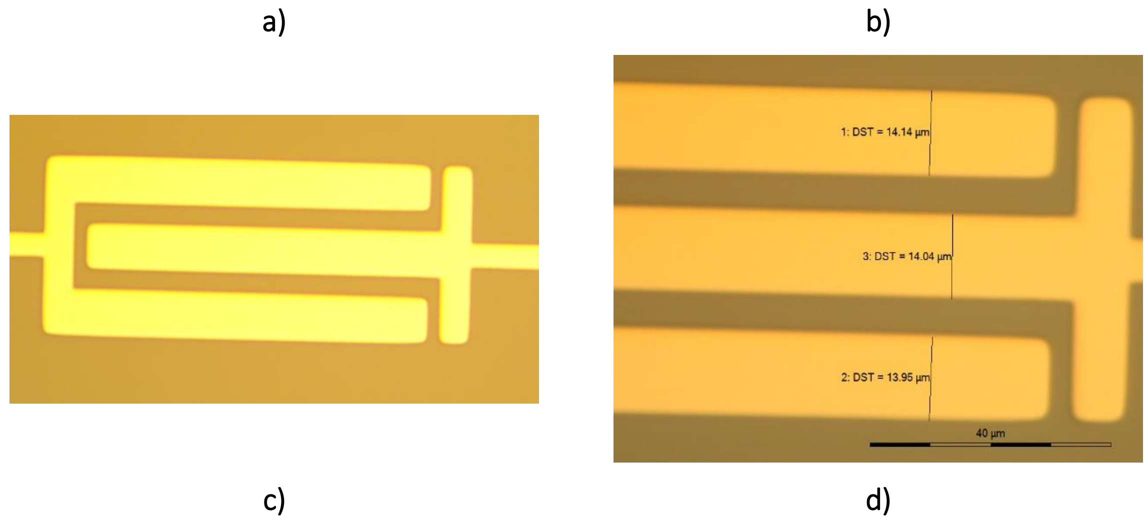


Figure 45 – Results for an exposure dose of $30\,\frac{mJ}{cm^2}$. The exposure dose is correct and there is no sign of under exposure: (a) Resonator + tracks; (b) Electrodes width 11 µm, Bus width 7 µm; Track width on the anchor 5 µm, Track width 30 µm; (d) Alignment marks.

Exposure dose of $30\,\frac{mJ}{cm^2}$ shows superior results. The dimensions of the design are correct and there is no sign of under exposure. The process is continued on the same wafer.

Sputter deposition and lift off

10 nm titanium and 50 nm platinum is sputter deposited. Then a **lift off removal procedure** is done: see appendices.



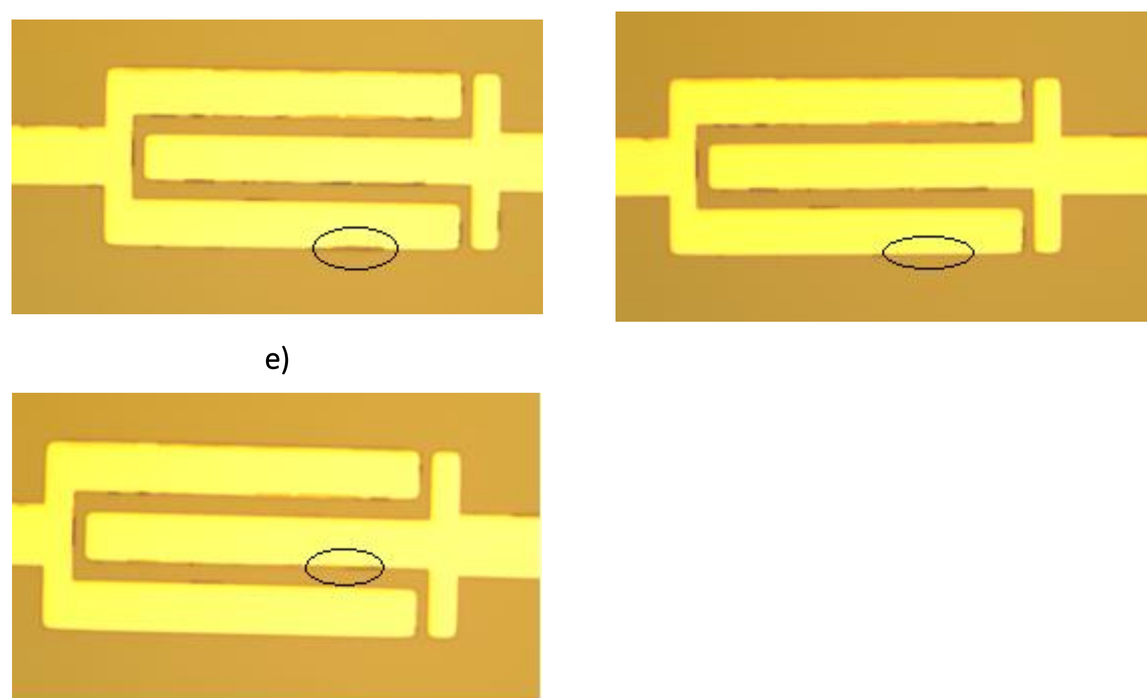


Figure 46 – (a) Most part of the wafer doesn't show any fences. (b) Electrodes width of 14 µm. The targeted dimension is 15 µm and the mask dimension is 12 µm; (c) Bottom right part of the wafer contains fences; (d) Some fences are removed after flipping the wafer in the ultrasound bath but it is not enough; (e) After 10 minutes ultrasound in zone 14 of the clean room in IPA, fences are smaller than in image (d).

On image (a) in Figure 46, the design doesn't show any fences for almost the complete wafer. However, at the bottom right part of the wafer, some design show some fences (image (c)). Image (d) shows that some fences are removed after flipping the wafer in the ultrasound bath but the removal is not complete. The ultrasound may be to low or the wafer should be in another position so that the ultrasound is more efficient. The ultrasound in the zone 14 of the clean room should be better because the wafer is put on the horizontal position. Image (e) shows that the fences are smaller. Image (b) shows 14 µm bottom electrodes width. The targeted dimension is 15 µm. In fact, the mask design has an electrode width of 12 µm with a lift off correction of 3 µm. The lift off correction should be decreased to 2 µm to have a correct targeted dimension. This change in comparison to the lift off studies is because the substrate is changed, thus the dose too.

7. Conclusion

In this report, the process flow of the lab is studied and changed in function of the requirements of the project. The device is a contour mode resonator with an aluminum nitride piezoelectric layer sandwiched between two metals. Top metal is a gold because it needs to be functionalized to detect RNA. Top metal is a plate to maximize the sensitive area of the device. The bottom metal is interdigitated electrodes to make the resonator working in contour mode. The shaping of the electrodes and resonator structure are done by etching. Lift off technic is used to pattern platinum bottom interdigitated electrodes, tracks and pads. Lift off is used to

pattern gold top plate electrodes. Each lift off process requires a mask for the design. Studies on the lift off process is done: To avoid fences from the edges of the electrodes, **the photoresist is developed twice**. A lift off correction value is needed and its value is a **shrinking of 3 µm** of the targeted design when the exposure is done on CMi test silicon wafer.

Then, to bring liquid on the CMR, depositing a droplet on Lab's design is not possible because the pads are to close from the CMR. It is also difficult to deposit accurately the droplet on the active surface. Moreover, the droplet dries too fast to have enough time to do measurements. Therefore, PDMS channel is used to bring liquid on the CMR. **Bonding studies** of different PDMS channels is done. PDMS doesn't bond to aluminum nitride. PDMS bonds on sputtered silicon oxide without liquid leakage with a **minimum wall width of 1 mm**. 1-port design of the Lab is used so **the 1 mm wall width** channel is limited only on one side of the channel**.** Asymmetrical channel is made with **another side wall width of 3 mm** to have a more reliable bonding. The PDMS assymmetrical channel bonds to sputtered silicon oxide without liquid leakage. Therefore, **the pads of the device are pushed away from the resonator of 2 mm** to have margin to align the channel. Contact angle studies show that the **liquid can flow underneath the resonator** which can lead to some short circuits of the bottom electrodes. Thus, the bottom electrodes are passivated with a silicon oxide layer.

The pads are pushed away from the resonator, thus the tracks are longer. Consequently, **the parasitic capacitance and the tracks resistance are higher**. To reduce the parasitic capacitance, the **track width is set to 30 µm** and the **passivated silicon oxide thickness is chosen to be 1 µm**. To decrease the load resistance of the CMR, **an aluminum conductive layer is sputter deposited on the platinum track and pads** with lift off patterning. Theoretical results of the parasitic capacitance and the load resistance give a result of **1.5 pF** and **9.5 Ω** respectively which are closely the same value as the lab's design.

The final process flow is a **5-masks process flow**. The 3 first masks are to lift off pattern the bottom electrodes, the conductive track and the top electrodes. The 4th mask designs the resonator shape and the access to the bottom pads and protect the surface where the channel must bond. The 5th mask protects the bottom pads and the surface where the channel must bond.

Simulation is done to determine which parameter is relevant to sweep in the design of the wafer. Simulation are used to maximize the quality factor of the CMR too. The anchor width is the most important parameter to find the best quality factor of the CMR. **Anchor width is swept from 10 µm to 28 µm with a step of 3 µm. The resonator length is 130 µm**, two **anchor lengths** are chosen: **20 µm and 40 µm**. One channel covers one chip which contain all the same resonators with **different pitch** (from **18.5 µm to 21.5** µm with a step of 0.5 µm) to have different resonance frequency. One special dye of the wafer contains chips in which the grounds of all the resonators are connected and the entry signal of all the resonators are connected. It enables to do the probing of the whole chip only once.

Fabrication and dose test is done on a high resistive wafer with a 1 µm wet oxide layer provided by the CMI staff. Dose test sets the dose at $30\,\frac{mJ}{cm^2}$. The first lift off pattern of platinum is successfully deposited with some remaining fences which can be removed with ultrasound.

The next steps to continue the project is to keep on the process flow. Since all the design rules and process flow are known, the CMR can be fabricated, assembled with PDMS channel and then tested.

8. Bibliography

[1] K. A. Cissell, Y. Rahimi, S. Shrestha, E. A. Hunt and S. K. Deo, "Bioluminescence-Based Detection of MicroRNA, miR21 in Breast Cancer Cells," *Analytical Chemistry,* vol. 80, no. 7, pp. 2319-2325, 2008.

[2] H. Zhou, J.-M. Guo, Y.-R. Lou, X.-J. Zhang, F.-D. Zhong, Z. Jiang, J. Cheng and B.-X. Xiao, "Detection of circulating tumor cells in peripheral blood from patients with gastric cancer using microRNA as a marker," *J Mol Med,* vol. 88, pp. 709-717, 2010.

[3] N. Yanaihara, N. Caplen, E. Bowman, M. Seike, K. Kumamoto, M. Yi, R. M. Stephens, A. Okamoto, J. Yokota, T. Tanaka, G. A. Calin, C.-G. Liu, C. M. Croce and C. C. Harris, "Unique microRNA molecular profiles in lung cancer diagnosis and prognosis," *Cancer Cell,* vol. 9, p. 189–198, 2006.

[4] J. L. Abell, J. M. Garren, J. D. Driskell, R. A. Tripp and Y. Zhao, "Label-Free Detection of Micro-RNA Hybridization Using Surface- Enhanced Raman Spectroscopy and Least-Squares Analysis," *Journal of the American Chemical Society,* vol. 134, pp. 12889-12892, 2012.

[5] A. Valoczi, C. Hornyik, N. Varga, J. Burgyan, S. Kauppinen and Z. Havelda, "Sensitive and specific detection of micro- RNAs by northern blot analysis using LNA-modified oligo-nucleotide probes," *Nucleic Acids Res.,* vol. 32(22), p. e175, 2004.

[6] C. Chen, D. A. Ridzon, A. J. Broomer, Z. Zhou, D. H. Lee, J. T. Nguyen, M. Barbisin, N. L. Xu, V. R. Mahuvakar, M. R. Andersen, K. Q. Lao, K. J. Livak and K. J. Guegler, "Real-time quantification of microRNAs by stem-loop RT-PCR," *Nucleic Acids Res.,* vol. 33(20), p. e179, 2005.

[7] W. Li and K. Ruan, "MicroRNA detection by microarray," *Anal. Bioanal. Chem.,* vol. 394, no. 4, pp. 1117-1124, 2009.

[8] T. Tian, J. Wang and X. Zhou, "A review: microRNA detection methods," *Org. Biomol. Chem.,* vol. 13, pp. 2226-2238, 2015.

[9] F. Li, J. Peng, J. Wang, H. Tang, L. Tan, Q. Xie and S. Yao, "Carbon nanotube-based label-free electrochemical biosensor for sensitive detection of miRNA-24," *Biosens. Bioelectron,* vol. 54, pp. 158-164, 2014.

[10] C. Li, Z. Li, H. Jia and J. Yan, "One-step ultrasensitive detection of microRNAs with loop-mediated isothermal amplification (LAMP)," *Chem. Commun.,* vol. 47(9), pp. 2595-2597, 2011.

[11] W. Hwang do, I. C. Song, D. S. Lee and S. Kim, "Smart magnetic fluorescent nanoparticle imaging probes to monitor microRNAs," *Small,* vol. 6(1), pp. 81-88, 2010.

[12] A. Heidari, YoonYong-Jin, M. I. Lee, L. Khine, M. K. Park and J. Ming Lin Tsai, "A novel checker-patterned AlN MEMS resonator as gravimetric sensor," *Sensors and Actuators A,* vol. 189, pp. 298-306, 2013.

[13] M. Rinaldi, C. Zuniga, N. Sinha, M. Taheri and G. Piazza, "Gravimetric Chemical Sensor based on the Direct Integration of SWNTs on AlN Contour-Mode MEMS Resonators," *2008 IEEE International Frequency Control Symposium,* pp. 443-448, 2008.

[14] G. Piazza, P. J. Stephanou and A. Pi, "One and two port piezoelectric higher order contour-mode MEMS re sonator for mechanical signal processing," *Solid State Electronic,* vol. 51, no. 11-12, pp. 1596-1608, 2007.

[15] M. Rinaldi, C. Zuniga and G. Piazza, "5-10 GHz AlN Contour-Mode Nanoelectromechanical Rsonators," *IEEE 22nd International Conference on Micro Electro Mechanical Systems,* pp. 916-919, 2009.

[16] A. Lozzi, *Internal Report: Contour Mode Resonator,* Lausanne, 2016.

[17] N. Ichikawa, K. Hosokawa and R. Maeda, "Interface motion of capillary-driven flow in rectangular microchannel," *Journal of Colloid and Interface Science,* vol. 280, pp. 155-164, 2004.

[18] D. Enterprises, "Accu Dyne Test: Surface Energy Data for PTFE," 2009. [Online]. Available: http://www.accudynetest.com/polymer_surface_data/ptfe.pdf. [Accessed 15 January 2017].

9. Appendices

9.1 Details of fabrication and machine parameters in CMi

Be aware, CMi staff may change their recipe's names.

Test wafer #59844 one time development

Photolithography:

Task	Recipe or parameter	Machine
Take a CMi test wafer	Wafer #59844	-
Coating: 620 nm AZ1512 on 480 nm LOR resist	#0171 AZ1512.ONLOR.0um48	ACS200 3 gen
Exposure of the resist	λ:405 nm Dose:80 $\frac{mJ}{cm^3}$ Defoc: -3	Heidelberg MLA150
Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen

Thin films: Spider Pfeiffer

Slots #, wafer #	Tasks	Thickness;Time	Recipe	Step #
25, Dummy	Clean Pt	-	Pt_clean_target	1
23, Dummy	Clean Ti	-	Ti_clean_target	1
21, #59844	Ti + Pt	10 nm + 100 nm; 7 s + 24 s	Ti_Pt_1	2

Zone 1: Plade solvent – Photolithography we bench

Task	Time
Remover 1165 bath	3h
Rinse with the remover 1165	-
Remover 1165 bath with ultras sound	2 X 300s
Rinse with the remover 1165	-
Remover 1165 bath	12h
Rinse with the remover 1165	-
Isopropanol bath	130s
1st water bath	10s
2nd water bath	10s

Test wafer #59846 two times development

Photolithography:

Task	Recipe or parameter	Machine
Take a CMi test wafer	Wafer #59846	-
Coating: 620 nm AZ1512 on 480 nm LOR resist	#0171 AZ1512.ONLOR.0um48	ACS200 3 gen
Exposure of the resist	λ:405 nm Dose:65 $\frac{mJ}{cm^3}$ Defoc: -3	Heidelberg MLA150
Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen
Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen

Thin films: Spider Pfeiffer

Slots #, wafer #	Tasks	Thickness;Time	Recipe	Step #
25, Dummy	Clean Pt	-	Pt_clean_target	1
23, Dummy	Clean Ti	-	Ti_clean_target	1
19, #59846	Ti + Pt	10 nm + 100 nm; 7 s + 24 s	Ti_Pt_1	2

Zone 1: Plade solvent – Photolithography we bench

Task	Time
Remover 1165 bath	3h
Rinse with the remover 1165	-
Remover 1165 bath with ultras sound	2 X 300s
Rinse with the remover 1165	-
Remover 1165 bath	12h
Remover 1165 bath with ultras sound	2 X 300s
Rinse with the remover 1165	-
Isopropanol bath	130s
1st water bath	10s
2nd water bath	10s
Dry	

Test wafer #59845 other recipe development

Photolithography:

Task	Recipe or parameter	Machine
Take a CMi test wafer	Wafer #59846	-
Coating: 620 nm AZ1512 on 480 nm LOR resist	#0171 AZ1512.ONLOR.0um48	ACS200 3 gen
Exposure of the resist	λ:405 nm Dose:65 $\frac{mJ}{cm^3}$ Defoc: -3	Heidelberg MLA150
Develop the resist	#0972 CMIDev.AZ1512ONLOR.0um82	ACS200 3 gen

Thin films: Spider Pfeiffer

Slots #, wafer #	Tasks	Thickness;Time	Recipe	Step #
23, Dummy	Clean Pt	-	Pt_clean_target	1
21, Dummy	Clean Ti	-	Ti_clean_target	1
25, #59845	Ti + Pt	10 nm + 100 nm; 7 s + 24 s	Ti_Pt_1	2

Zone 1: Plade solvent – Photolithography we bench

Task	Time
Remover 1165 bath	3h
Rinse with the remover 1165	-
Remover 1165 bath with ultras sound	2 X 300s
Rinse with the remover 1165	-
Remover 1165 bath	12h
Rinse with the remover 1165	-
Isopropanol bath	130s
1st water bath	10s
2nd water bath	10s

HR 1 already released structures

Thin films: Spider Pfeiffer

Slots #, wafer	Tasks	Thickness;Time	Recipe	Step #
25, Dummy	Clean SiO_2	-	SiO_2_clean_target	1

23, HR 1	SiO_2	200 nm; 17min18s	SiO_2_F_1	2

Test wafer #69843 bonding test

Thin films: Spider Pfeiffer

Slots #, wafer	Tasks	Thickness;Time	Recipe	Step #
25, Dummy	Clean SiO_2	-	SiO_2_clean_target	1
23, #69843	SiO_2	100 nm; 8min39s	SiO_2_F_1	2

HR wafer 53 oxide 1um dose test

Photolithography:

Task	Recipe or parameter	Machine
Take a HR wafer with 1um oxide	Wafer HR ox1um	-
Coating: 620 nm AZ1512 on 480 nm LOR resist	#0171 AZ1512.ONLOR.0um48	ACS200 3 gen
Exposure of the resist	λ:405 nm Dose:$[20:5:130]\,\frac{mJ}{cm^3}$ Defoc: -3	Heidelberg MLA150
1st Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen
2nd Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen

HR wafer 54 oxide 1um fabrication

Photolithography:

Task	Recipe or parameter	Machine
Take a HR wafer with 1um oxide	Wafer HR ox1um	-
Coating: 620 nm AZ1512 on 480 nm LOR resist	#0171 AZ1512.ONLOR.0um48	ACS200 3 gen
Exposure of the resist	λ:405 nm Dose:$20\,\frac{mJ}{cm^3}$ Defoc: -3	Heidelberg MLA150
1st Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen
2nd Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen

HR wafer 55 oxide 1um fabrication

Photolithography:

Task	Recipe or parameter	Machine
Take a HR wafer with 1um oxide	Wafer HR ox1um	-
Coating: 620 nm AZ1512 on 480 nm LOR resist	#0171 AZ1512.ONLOR.0um48	ACS200 3 gen
Exposure of the resist	λ:405 nm Dose:30 $\frac{mJ}{cm^3}$ Defoc: -3	Heidelberg MLA150
1st Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen
2nd Develop the resist	#0971 CMIDev.AZ1512ONLOR.0um48	ACS200 3 gen

Thin films: Spider Pfeiffer

Slots #, wafer #	Tasks	Thickness;Time	Recipe	Step #
25, Dummy	Clean Pt	-	Pt_clean_target	1
23, Dummy	Clean Ti	-	Ti_clean_target	1
19, #HR 55 ox1um	Ti + Pt	10 nm + 50 nm; 7 s + 12 s	Ti_Pt_1	2

Zone 1: Plade solvent – Photolithography we bench

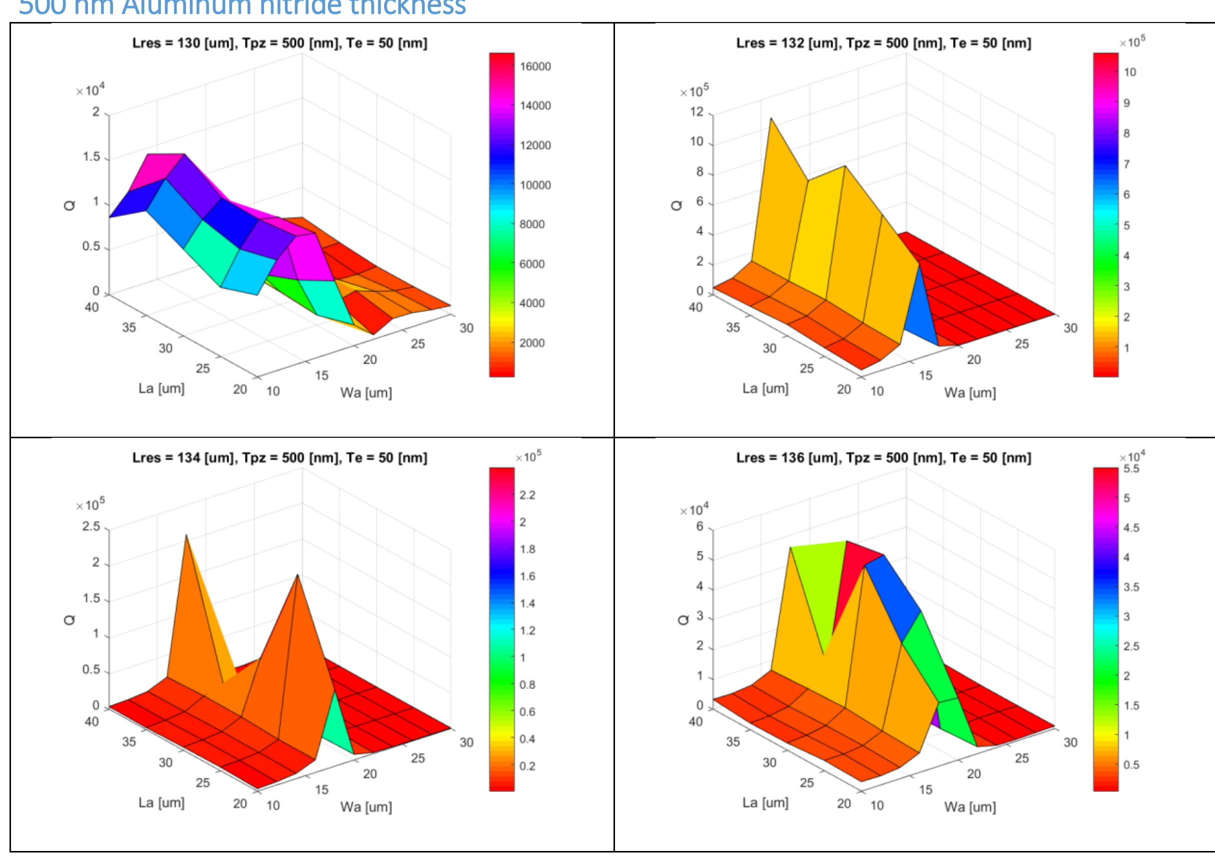
Task	Time
Remover 1165 bath	3h
Rinse with the remover 1165	-
Remover 1165 bath with ultras sound	2 X 300s
Rinse with the remover 1165	-
Remover 1165 bath	12h
Remover 1165 bath with ultras sound	2 X 300s
Rinse with the remover 1165	-
Isopropanol bath	130s
1st water bath	10s
2nd water bath	10s
Rinse with water	
Dry with air	-

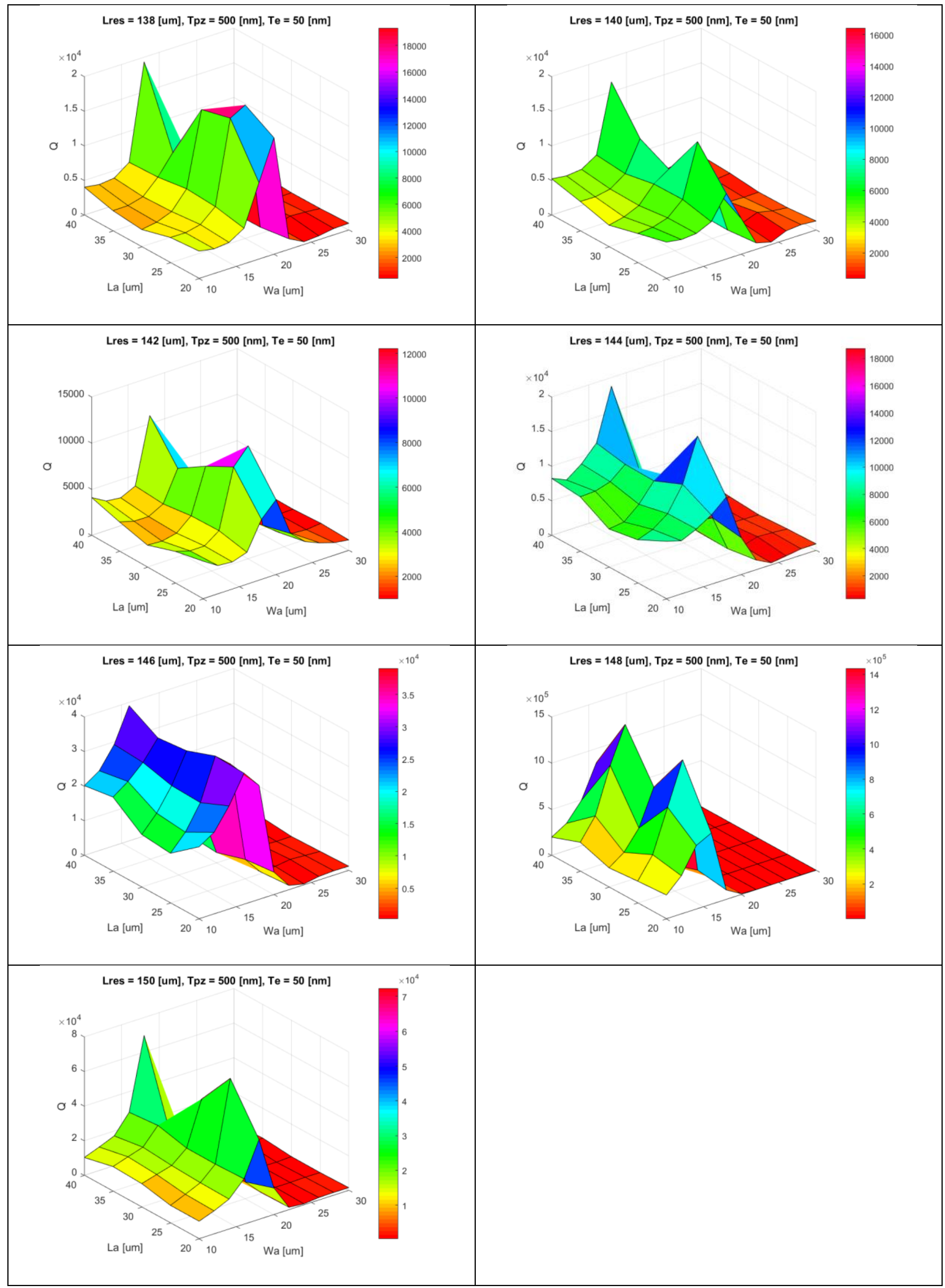
Zone 14: Wet bench solvent

Task	Time
Isopropanol bath with ultrasound	10 min
Rinse with water	-
Dry with air	-

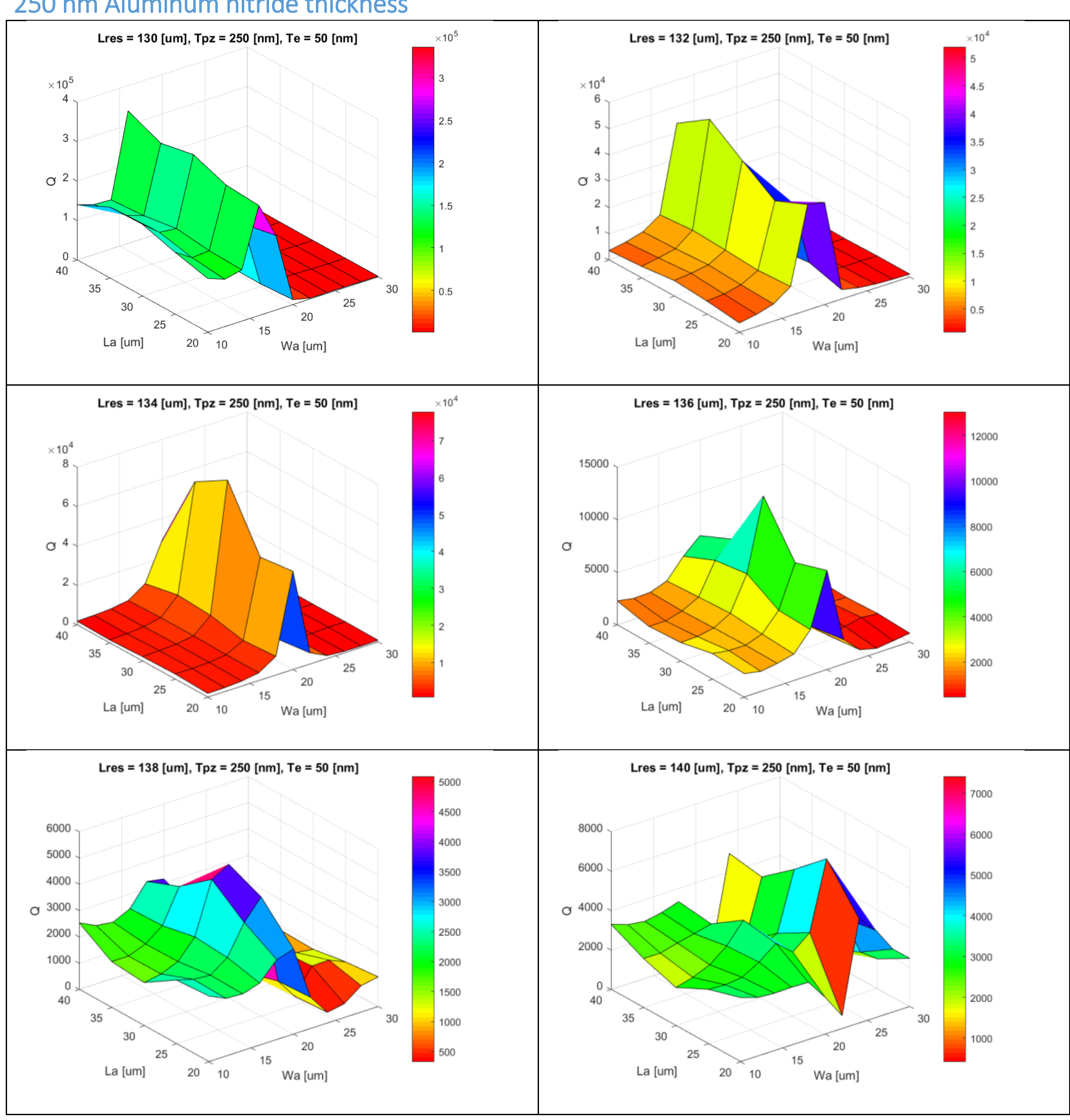
9.2 Results of the simulations

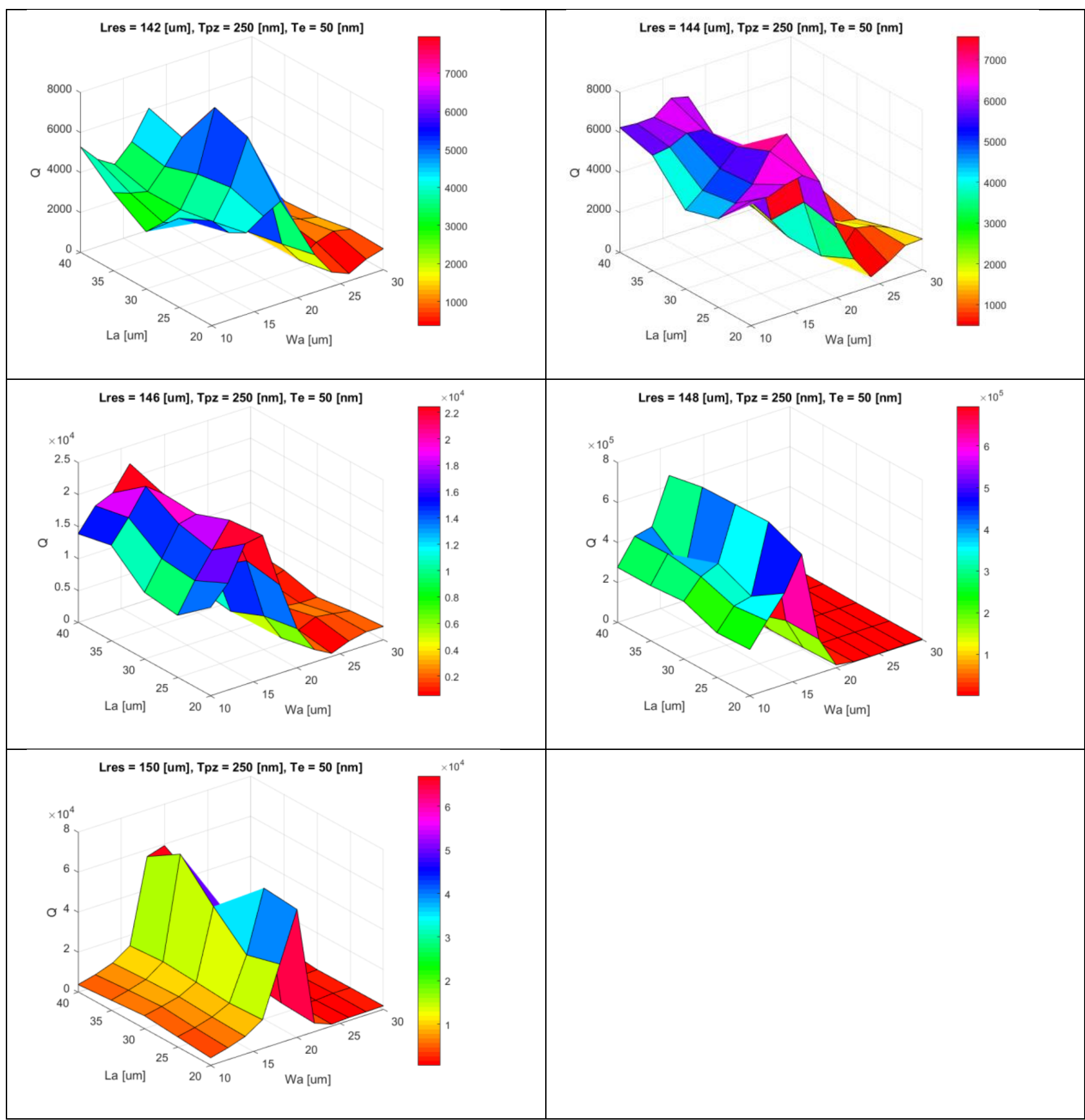
500 nm Aluminum nitride thickness



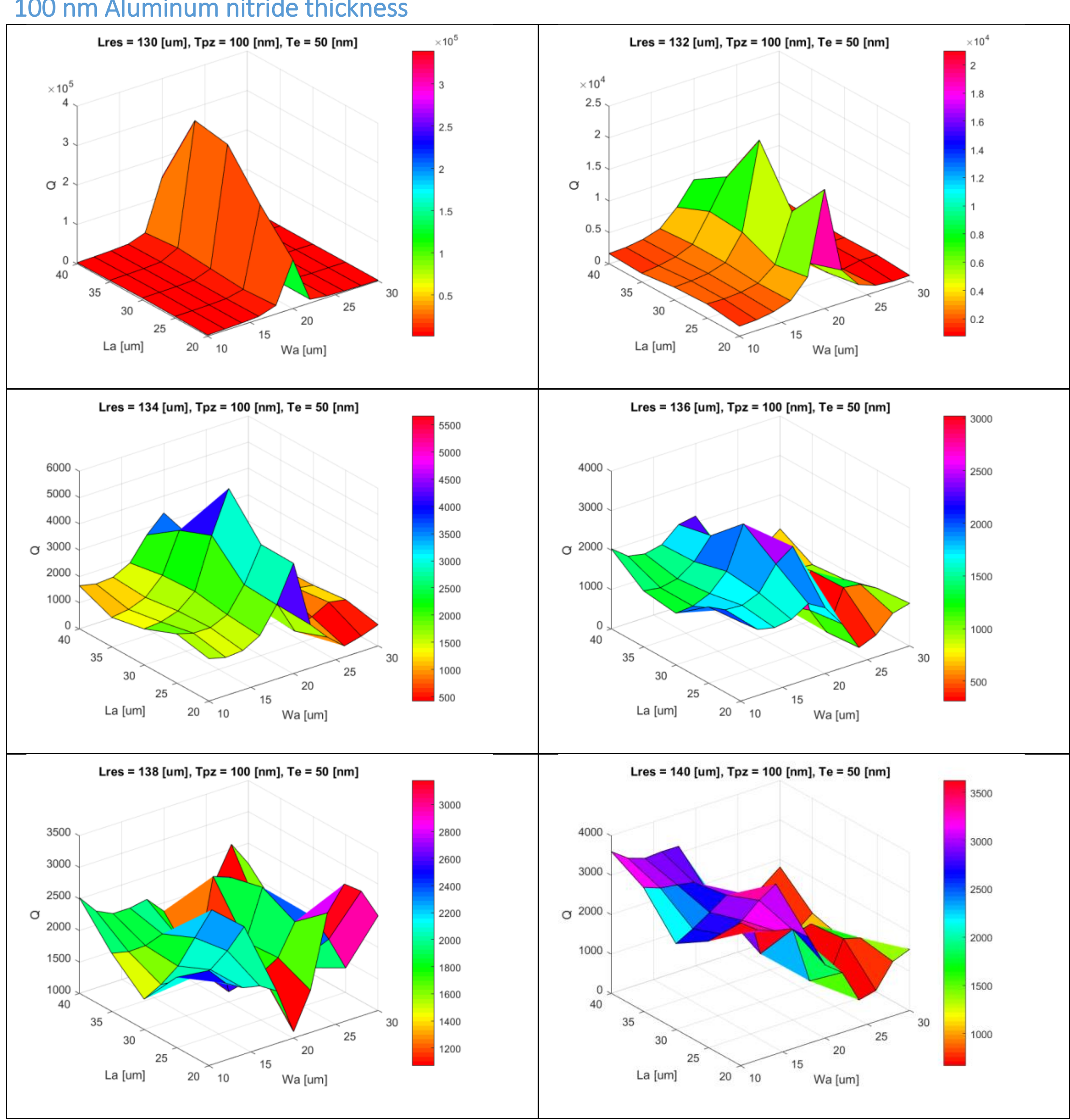

Lres = 138 [um], Tpz = 500 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]
Lres = 140 [um], Tpz = 500 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]
Lres = 142 [um], Tpz = 500 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]
Lres = 144 [um], Tpz = 500 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]
Lres = 146 [um], Tpz = 500 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]
Lres = 148 [um], Tpz = 500 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]
Lres = 150 [um], Tpz = 500 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]

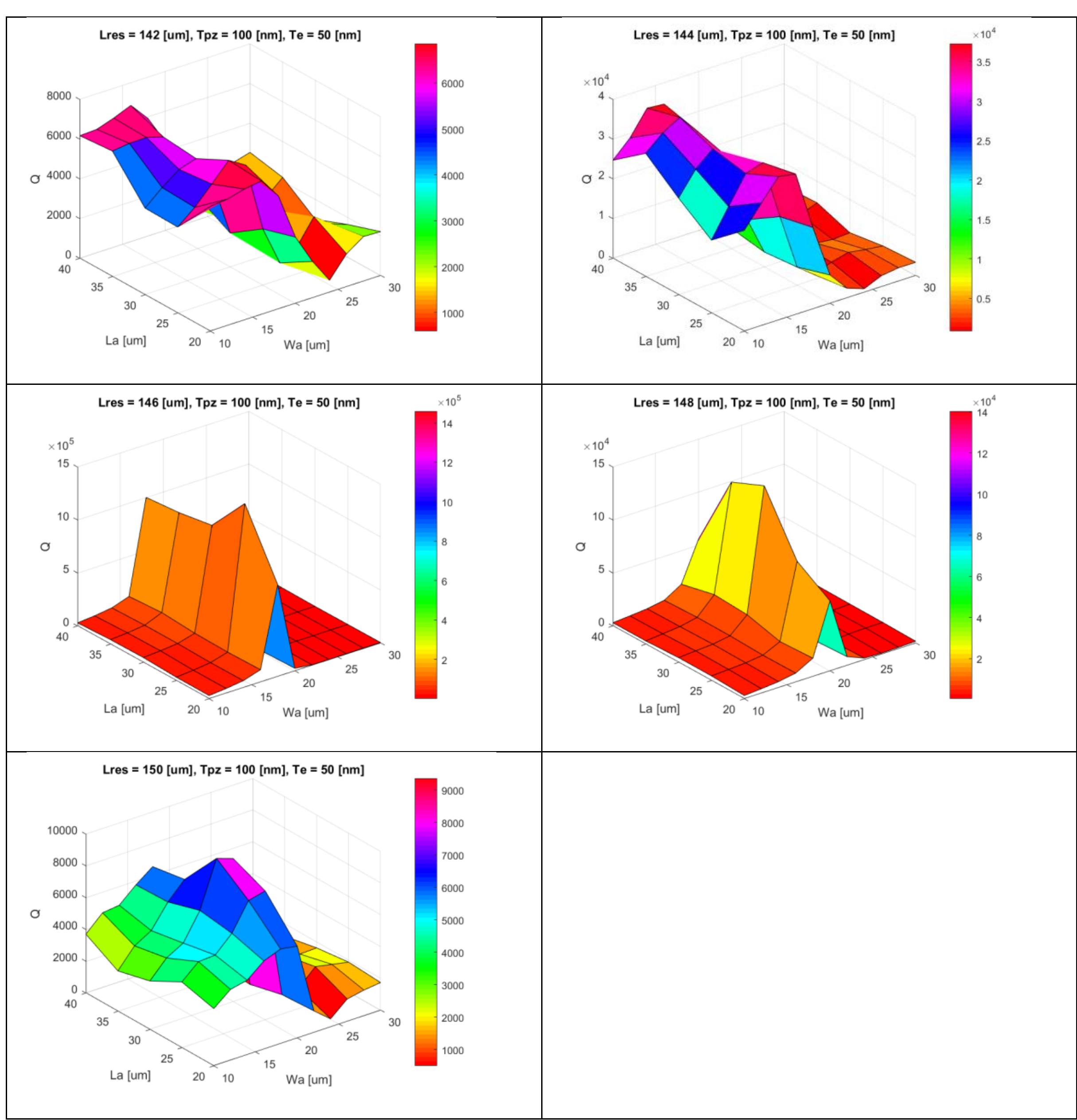
250 nm Aluminum nitride thickness




Lres = 142 [um], Tpz = 250 [nm], Te = 50 [nm]
Lres = 144 [um], Tpz = 250 [nm], Te = 50 [nm]
Lres = 146 [um], Tpz = 250 [nm], Te = 50 [nm]
Lres = 148 [um], Tpz = 250 [nm], Te = 50 [nm]
Lres = 150 [um], Tpz = 250 [nm], Te = 50 [nm]
Q
La [um]
Wa [um]

100 nm Aluminum nitride thickness





9.3 Process flow and design

Process flow

<u>Contour Mode Resonator for MEMS-mass detection</u>

Technologies used
!! remove non-used !!

Mask fabrication, sputtering, positive resist, Dry etching, Wet etching, SEM.			
Photolith masks			
Mask #	Critical Dimension	Critical Alignment	Remarks
1	5 µm	First Mask	IDT bottom electrodes + tracks + pads
2	30 µm	5 µm	Conductive track + conductive pads
3	60 µm	1 µm	Gold top electrodes
4	10 µm	1 µm	Resonator body + Bottom pads access+surf. prot.
5	30 µm	10 µm	bottom pads protection + surface protection
Substrate Type			
Silicon <100>, Ø100mm, 525um thick, Single Side polished, Prime, no type, 0.1-0.5 Ohm.cm			
Si: SiO2: Pt: Al: Au: AlN:			

Step	Process description	Cross-section after process
00	*Deposition of 1µm of wet oxide. T=1250°C (CMi staff)*	
01	*Photolith* *Machine: ACS200–MLA150* *PR: AZ1215 on LOR – 0.62um on 0.48um* *Mask: CD = 5um* *Mask #1:* IDT bottom electrodes & tracks	

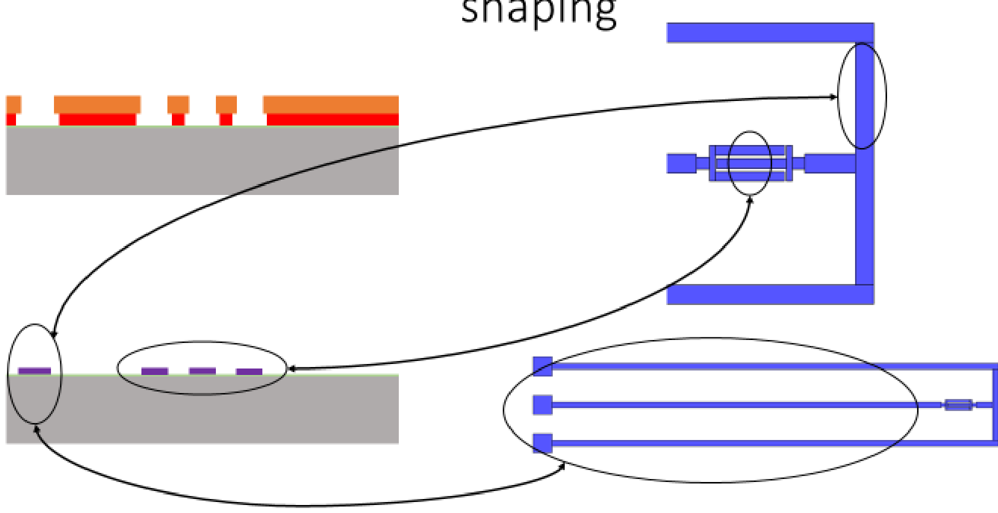
02	*Metal sputtering* *Machine: Pfeiffer Spider 600* *Metal: Ti/Pt* *Thickness: 0.01/ 0.05 µm* ***Lift off***	
03	*Photolith* *Machine: ACS200–MLA150* *PR: AZ1215 on LOR* *– 0.62um on 0.48um* *Mask: CD = 30um* *Mask #2:* Conductive track and pads	
04	*Metal sputtering* *Machine: Pfeiffer Spider 600* *Metal: Al* *Thickness: 0.3 µm* ***Lift off***	
05	*Aluminum Nitride sputtering* *Machine: Pfeiffer Spider 600* *Metal: AlN* *Thickness: 0.250 µm*	
06	*Photolith* *Machine: ACS200–MLA150* *PR: AZ1215 on LOR* *0.62um on 0.48um* *Mask: CD = 30um* *Mask #3:* top gold electrode	
07	*Evaporation* *Machine: EVA600 or EVA760 or LAB 600H* *Thickness: 0.05 um* *Materials: Au* ***Lift off***	

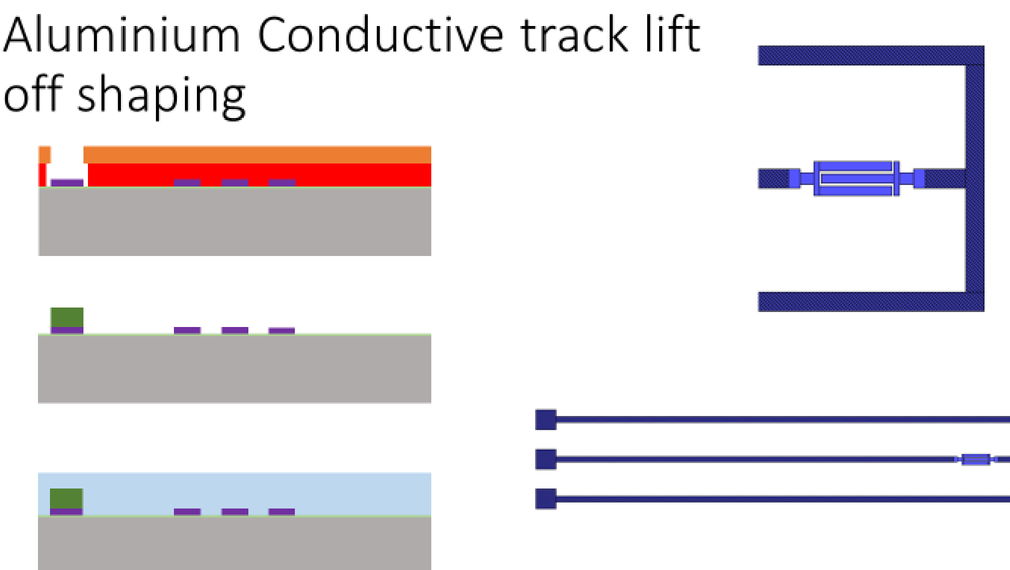
08	*Metal sputtering* *Machine: Pfeiffer Spider 600* *Materials: SiO2 high quality* *Thickness: 0.5 µm*	
07	*Photolith* *Machine: RiteTrack–MLA150* *PR: AZ ECI – 3-5 µm* *Mask: CD = 10 µm* *Mask #4:* resonator body + bottom pads access and surface protection	Bottom Electrodes access PDMS Wall Design Device shaping
08	*Dry Etch* *Material: SiO2* *Machine: STS/Alcatel601* *Depth: 0.5 µm*	
09	*Dry Etch* *Material: AlN* *Machine: STS / IBE* *Depth: 0.5 µm* *Etch rate AlN:0.3 um/min* *Etch rate Pt:0.035 um/min*	
10	*Photolith* *Machine: RiteTrack–MLA150* *PR: AZ ECI – 3-5 µm* *Mask: CD = 30 µm* *Mask #5:* bottom pads and surface protection	

11	*Dry Etch* *Material: Si0₂.* *Machine: IBE/STS* *Depth: 0.1/0.4 um*	
12	*Dry Etch* *Material: Si* *Machine: Alcatel 601 Bosh process anisotropic Si etching* *Depth: ~10 μm* + **Resist strip** + ***SiO2 strip***	
13	*Dry Etch* *Material: Si* *Machine: Alcatel 601isotropic Si etching* *Depth: Release*	
14	*Dry Etch* *Material: Si02* *Etchant: vapor HF*	

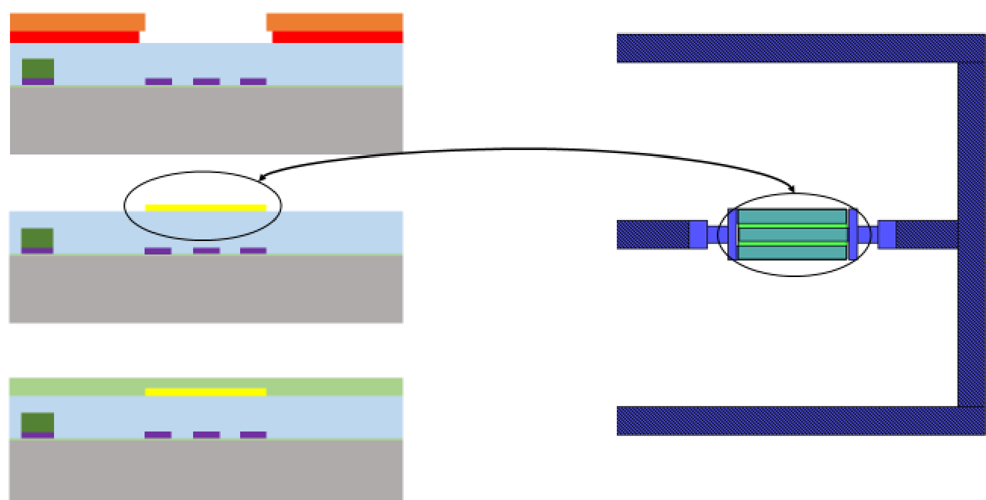
Process flow with design

Bottom Platinum electrode and track lift off shaping

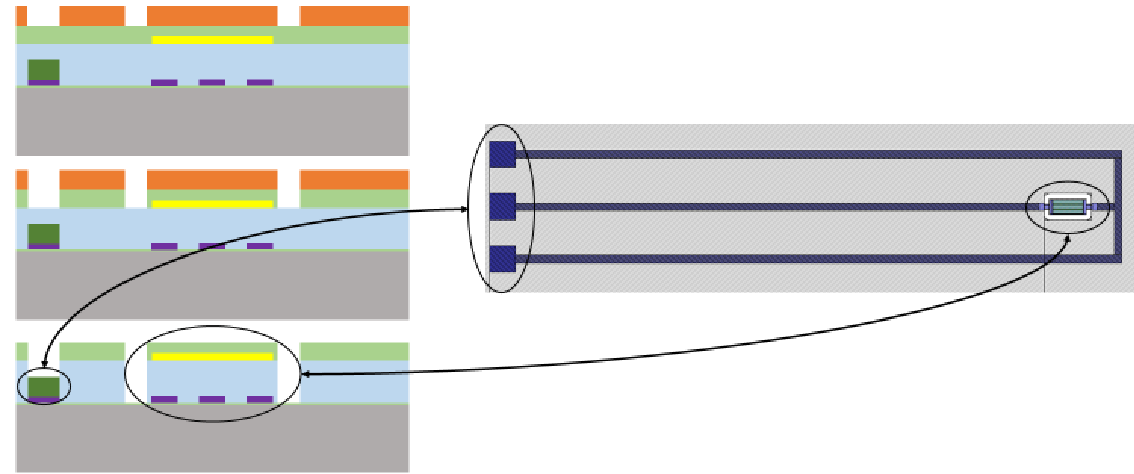




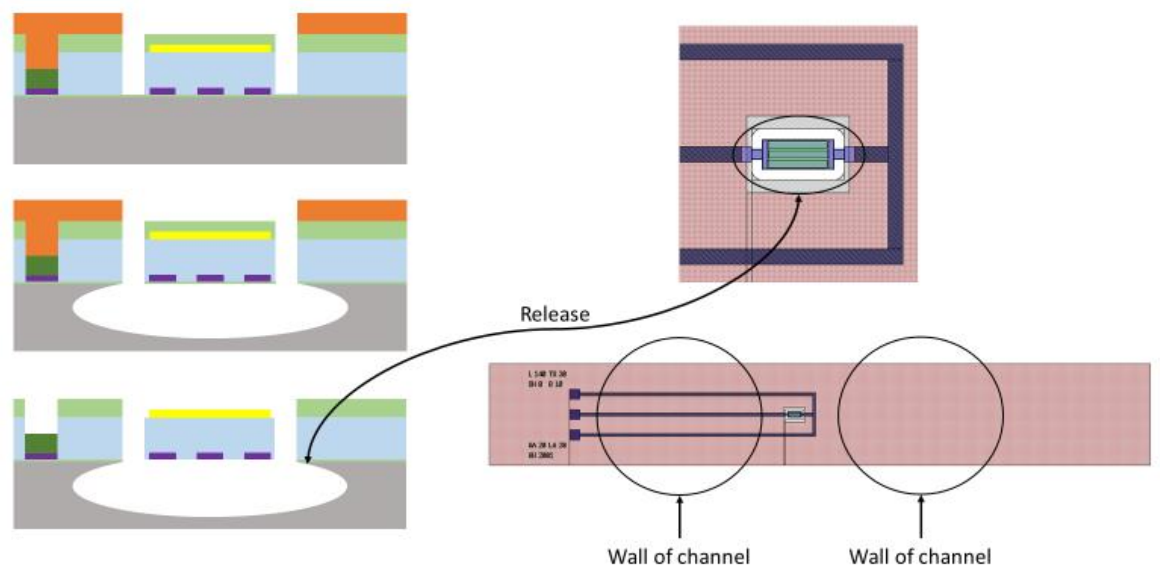
Top gold electrode lift off shaping



Resonator shaping and track covering (AlN)



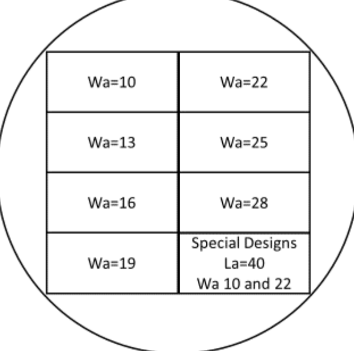
Release of the resonator



9.4 Wafer organization

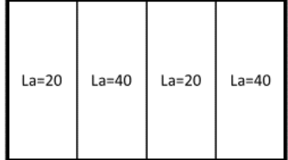
Wafer: 4.5 cm radius for design space Width Sweep

- 8 dies
  - Parameter Sweep
    - 7 anchor widths
      - Wa=[10:3:28] µm
  - Special Dye
    - Resonators:
      - Ground connected
      - Entry Signal connected
      - Anchor Length: 40 µm
      - Anchor Width: [10,22] µm



Dye: Anchor length sweep for one anchor width

- Dye Size: 15mmx30mm
- Contains:
  - 4 chips of size 15mmx7.5mm
  - Parameter Sweep
    - 4 chips 20 X Anchor Length [20,40] µm



Chip: Pitch Sweep for one anchor size

- Size:15mmx7.5mm
- Contains:
  - 8 resonators of size:15mmx7.5mm
  - Parameter Sweeping (Up to down order):
    - 7 resonators Pitch = [18.5:0.5:21.5] µm
    - 1 resonator Pitch = 20 µm

P=18.5
P=19
P=19.5
P=20
P=20.5
P=21
P=21.5
P=20