



© 2017 IEEE

PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of

Virtual Submodule Concept Applied to the Modular Multilevel Converter

A. Christe and D. Dujic

This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of EPFL's products or services. Internal or personal use of this material is permitted. However, permission to reprint / republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee. org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.

Virtual Submodule Concept Applied to the Modular Multilevel Converter

Alexandre Christe, Drazen Dujic Power Electronics Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland alexandre.christe@epfl.ch, drazen.dujic@epfl.ch

Abstract

The design phase of a modular multilevel converter (MMC) needs to be supported by suitable tools for the submodule loss evaluation. This paper proposes a fast MMC cell loss calculation based on the virtual submodule (VSM) concept. Compared to other proposed tools, the impact of the circulating current control is directly taken into account and different modulation schemes can be easily com-To verify the proposed concept, the results are compared with the losses obtained from a switched model with closed-loop control, where the analytical MMC key waveforms are approached in the steady state. The proposed method provides a great flexibility and a significant reduction of the simulation / computational time otherwise needed to evaluate SM losses under various operating conditions.

1. Introduction

While the behavior and control of MMCs have been thorougly described in the literature since its introduction [1], performant design tools are at the moment still missing. This paper focuses on semiconductor and capacitor losses for MMC with unipolar cells, although the proposed method could be straight-forwardly extended to other MMCs topologies.

The MMC prototype, currently under development, has the following rating: $10\,\mathrm{kV}$ DC bus, $0.5\,\mathrm{MVA}$ apparent power and uses 96 submodules (SMs) with low voltage IGBT semiconductors that can be configured into unipolar or bipolar submodule (SM) [2], [3]. The targeted application is the interconnection of the widely deployed $400\,\mathrm{V}$ LVAC grid, or corresponding microgrid, with the emerging MVDC grids $(10\,\mathrm{kV})$ is considered in our case). For that reason,

the converter has to deal with a large voltage ratio and the use of a transformer for galvanic isolation and voltage adaption is mandatory, as shown in Fig. 1, or elaborated in [4] for the case of integrated transformer.

To support system design, this paper proposes a semi-numerical method for loss calculation of the MMC SM using the VSM concept. Authors of [5], [6] have obtained semiconductor losses by simulation or numerically considering direct modulation for HVDC application in mind, with a DC circulating current and without considering the capacitor losses [7]. In contrast, the proposed method allows for a fast estimation of the SM losses under different operating conditions, control schemes (e.g. effects of the circulating current injection strategy) and modulation methods under the assumption of a stable operation of these schemes in steady-state. To verify the validity of the proposed method, a comparison with a fully switched converter model has been carried out.

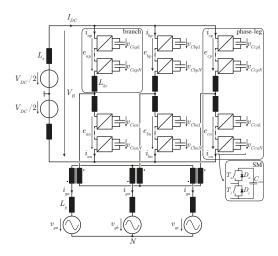


Fig. 1: MMC with external line frequency transformer (LFT) for DC/3-AC conversion with large voltage ratio. Each branch comprises N_{sm} series-connected unipolar SMs.

2. Analytical description of the closed-loop MMC waveforms

The key difference of this method with other already proposed methods is that it is based on closed-loop MMC waveforms. If the circulating current control is assumed to be working, then the measured waveforms correspond to their references. Several scenarios have to be accounted for, depending on whether or not a second harmonic circulating current is used, the addition of a common mode voltage and any combination of the two. The branch voltage and current equations are presented below.

$$e_{p/n} = \frac{V_{DC}}{2} \left(1 \mp k_{AC} \cos \left(\omega t - \frac{2\pi(k-1)}{3} \right) \mp v_{CM} \right)$$

$$- \left(R_{br} i_{p/n} + L_{br} \frac{\mathrm{d}}{\mathrm{d}t} i_{p/n} \right) \qquad (1)$$

$$i_{p/n} = \underbrace{\frac{I_{DC}}{3}}_{\text{DC term}} \underbrace{\pm \frac{1}{2} \hat{i}_g \cos \left(\omega t + \phi - \frac{2\pi(k-1)}{3} \right)}_{\text{fundamental AC term}}$$

$$\underbrace{+ \hat{i}_{\text{circ},2} \cos \left(2\omega t + \theta_2 - \frac{2\pi(k-1)}{3} \right)}_{\text{optional 2}^{\text{nd harmonic term}}} \qquad (2)$$

where V_{DC} is the DC link voltage, $k_{AC}=2\hat{v}_g/V_{DC}$ the voltage ratio between the three-phase AC and DC grids, ω the grid frequency, $k\in\{1,2,3\}$ the phase number, S the apparent power of the con-

verter and ϕ the load angle. The grid current $(\hat{i}_g$ and $\phi)$ is fully determined from the power exchange between the DC bus and the AC grid.

$$\hat{i}_g = \frac{2S}{3\hat{v}_g} = \frac{2S}{3k_{AC}V_{DC}/2}$$
 (3)

$$\hat{i}_{\text{circ},2} = \frac{\hat{v}_g \hat{i}_g}{2V_{DC}} = \frac{S}{3V_{DC}} \tag{4}$$

The DC current is determined by taking the negative root of a quadratic equation [8]. It is important to stress that for best accuracy the branch impedance $(R_{br}$ and $L_{br})$ have to be accounted for in the model [9].

$$I_{DC} = \left[V_{DC} - \sqrt{V_{DC}^2 - 8R_{br} \left(\frac{\hat{v}_g \hat{i}_g}{2} \cos(\phi) + 2R_{br} \left(\frac{\hat{i}_g^2}{8} + \frac{\hat{i}_{\text{circ},2}^2}{2} \right) \right)} \right] / (4R_{br})$$
 (5)

The result of the analytical description of the MMC waveforms in closed-loop is presented in Fig. 2 for the parameters in Table 1.

3. Virtual submodule concept

Once that the analytic expressions of the MMC key waveforms are obtained, they need to be appropriately distributed to each SM. The modulation can be

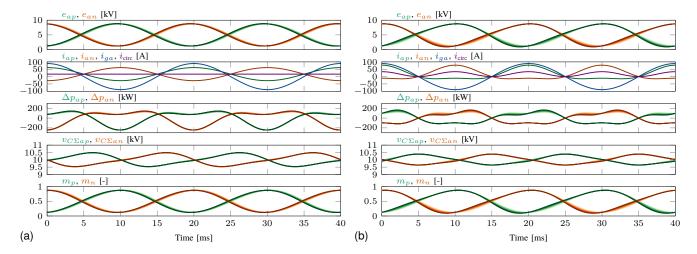


Fig. 2: Branch representative waveforms with: (a) DC circulating current and (b) DC plus 2^{nd} harmonic circulating current injection. The branch inductance value is swept from $0\,\mathrm{H}$ (light shade) to $50\,\mathrm{mH}$ (dark shade) to highlight the impact of the branch inductance voltage drop. The currents are not impacted by L_{br} , as they are set for a given power transfer and no ripple is considered.

Tab. 1: System parameters

V_{DC}	$10\mathrm{kV}$	S	$0.5\mathrm{MVA}$	N_{sm}	16
R_{br}	0.1Ω	k_{AC}	0.75	C_{sm}	$1.9\mathrm{mF}$
k_{DC}	1	L_{br}	$10\mathrm{mH}$	R_{esr} a	$110\mathrm{m}\Omega$

^aPer individual capacitor

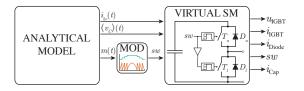


Fig. 3: Functional VSM concept, where the MOD block is implemented with a single carrier and a quantizer. It produces an output identical to a collection of all switching events from any modulation scheme.

modified in order to capture and direct all switching events to only one VSM, as shown in Fig. 3.

In the conventional multilevel PWM principle, for both phase-disposition PWM (PD-PWM) and phase-shifted PWM (PS-PWM), each switching event is obtained from a reference/carrier intersection. The transformation to an implementation with a single carrier combined with a quantizer, that is selected for the modulation (MOD) block in Fig. 3, is shown in Fig. 4. The quantizer signal is first obtained from a threshold comparison with each carrier band defined by $[1/N_{sm}\,:\,1/N_{sm}\,:\,1]$ and marked with +. Note that the quantizer signals are identical for both modulation methods, as they only depend on the number of carrier bands, i.e. on N_{sm} , but not on the carrier phase. Then a single carrier PWM is created with a modified reference obtained by substracting the quantizer signal to the reference signal and compressing all carriers into one. As each carrier has the same phase for PD-PWM, there is no phase jump in the compressed carrier signal, in contrast to alternate phase-opposition disposition PWM (APOD-PWM) (identical to PS-PWM), where a 180° phase-shift is present between each neighboring carrier bands, leading to 180° phase jump in the compressed carrier signal each time a carrier band is crossed (+). Finally, the PWM pattern is obtained by summing the quantizer and single carrier PWM output. Note that at first sight the single carrier modulation seems to produce additional switching events compared to the conventional implementation, but this is due to a required

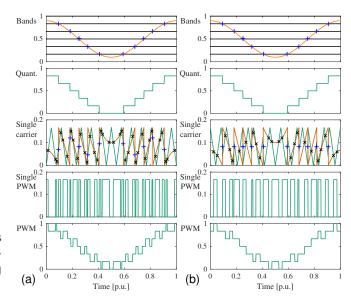


Fig. 4: PWM modulator principle with single carrier and quantizer, where the reference/carrier intersections are represented by **x** and the reference/carrier band intersections by **+**: (a) for PD-PWM with pulse number $p=2N_{sm}+1$ and (b) for APOD-PWM with pulse number $p=2N_{sm}$. For APOD-PWM the single carrier has a frequency that jumps by 180° each time the quantizer changes its output. For illustration purpose, a sinusoidal modulation index with $N_{sm}=6$ is shown.

compensation of changes in the quantizer signal that doesn't lead to a switching signal in the resulting PWM pattern (+ in the single carrier plots). A motivation for such an implementation in the context of MMC is that the position of a SM within a branch is not linked with a specific carrier band, in the case of a branch balancing method based on a sorting algorithm.

To evaluate the MMC losses using the VSM concept, the analytical model is combined with a PWM modulator, from which the switching instants are fetched, as shown in Fig. 5. The analytical expressions are evaluated over the simulation horizon for a given set of parameters and then loaded into 1D look-up tables (LUTs). The modulation block is implemented with the single carrier and quantizer as illustrated in Fig. 4. Multiple consecutive turn-ON or turn-OFF events, that happen in a multilevel switching pattern, are correctly handled by the VSM implementation, that doesn't rely on a pair of physical switches. Then the VSM constructs the signals that are routed to the loss tool. As the branch current, capacitor voltage and modulation index are used

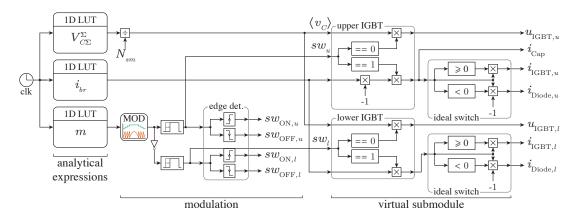


Fig. 5: Detailed VSM concept implementation.

as inputs, the VSM concept is insensitive to the circulating current injection strategy or modulation method. The switching instants are collected with the edge detection block (turn-ON and turn-OFF) and stored for further post-processing and loss calculations.

4. MMC switched model

To compare the analytical method based on the VSM concept with realistic waveforms from a fully switched MMC model, circuit simulations are performed with PLECS / Simulink. The comparison is carried with two modulation methods: (i) PD-PWM and (ii) PS-PWM. The considered apparent branch switching frequencies are $3\,\mathrm{kHz}$ for PD-PWM and $2.95\,\mathrm{kHz}$ for PS-PWM. This corresponds to a SM switching frequency of $187.5\,\mathrm{Hz}$ and $184.375\,\mathrm{Hz}$, respectively. The presence of a branch balancing method is the underlying requirement for the derivation of the macroscopic level control diagram. The fundamental objective is to ensure an equal energy transfer between all SMs. They are briefly described hereafter for each modulation method.

4.1. PD-PWM

In order to control the SM switching frequency, the sorting algorithm is not run at every sampling time but rather at every switching event. It is inspired from the Reduced Switching Frequency method proposed originally in [10]. This prevents the insertion of additional switching events that would be induced by a sorting algorithm executed at the appar-

ent branch switching frequency, with group swapping between the bypassed and inserted SMs.

4.2. **PS-PWM**

Equal switching frequency among all SMs of the same branch is an inherent feature of PS-PWM, as a different carrier is assigned to each SM. On the other hand, it requires a modified branch balancing algorithm [11], that can be partially circumvented in the case of non-integer frequency ratio between the grid frequency and the SM carrier frequency, as it leads to self balancing [12].

4.3. Control diagram

The state-of-the-art MMC control is selected, according to [13]. It is implemented in a cascaded manner, with internal current controllers and external capacitor voltage controllers. The complete control diagram is shown in Fig. 6. Unlike classical topologies, the control of an MMC can be divided into two parts: (i) the inner state variables control (circulating current and capacitor voltages) and (ii) the external state variables control (AC grid current, DC voltage). Under the assumption of a working branch balancing algorithm, that ensures a controlled spread among the capacitor voltages within a branch, a macroscopic converter model can be advantageously used for control purpose. The capacitor voltage control is divided in 2 objectives: (i) the total energy control (TEC), which ensures that the total energy in the converter is kept constant as

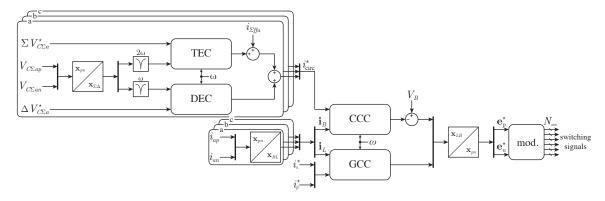


Fig. 6: Control structure adopted for the simulations assuming MMC connection to a stiff MVDC grid. The relevant control blocks are: total energy controller (TEC), differential energy controller (DEC), circulating current controller (CCC) and grid current controller (GCC).

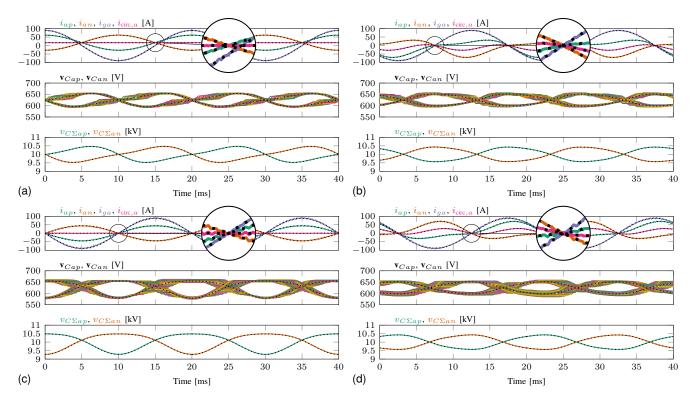


Fig. 7: Steady-state closed-loop responses (colored lines) versus analytical waveforms (dashed lines) in phase-leg a: (a) PD-PWM with DC circulating current for $\phi=0$, (b) PD-PWM with DC plus 2^{nd} harmonic circulation current for $\phi=3\pi/4$, (c) PS-PWM with DC circulating current for $\phi=\pi/2$ and (d) PS-PWM with DC plus 2^{nd} harmonic circulating current for $\phi=\pi/4$.

well as equally distributed between the three phaselegs and (ii) the differential energy control (DEC), which ensures that the energy is equally distributed between the upper and lower branch of the same phase-leg. In the literature, TEC is also referred as horizontal balancing and DEC as vertical energy balancing [14].

4.4. MMC waveforms in closed-loop

The relevant waveforms from the analytical model and from the closed-loop switched model are compared for various load angles and the two considered circulating current injection strategies in Fig. 7. Aside from both the branch current ripple and capacitor voltage spread that cannot be captured in

the analytical model, they are in very good agreement. This also demonstrates the performance of the control algorithm: a perfectly DC circulating current (Fig. 7a+c) or a DC with superimposed 2nd harmonic circulating current (Fig. 7b+d) are obtained in steady-state.

5. Loss tool

To compare the results, a common loss tool collects the waveforms of interest either from the VSM or the fully switched model. The input waveforms are sampled at $200\,\mathrm{kHz}$. The waveforms of interest are: (i) the voltage across both upper and lower IGBTs, (ii) the current through the IGBTs and the diodes as well as the capacitor current and (iii) the switching instants, which are mandatory in order to determine the switching losses (its functional description is illustrated in Fig. 8). Different semiconductor devices can be easily compared, as they are loaded from a database - though based on data sheet parameters. Multiple simulation sweeps for each device are not required, as device specific parameters are not required for the simulation. Proper scalings and interpolations are built into the loss tool, aiming to minimize the errors due to the limited number of sampled points provided for the switching loss energies. Additional calculated data provided as outputs are also indicated at the bottom of the loss tool.

6. Verification and comparison

To provide a complete analysis of the error between the VSM method and the loss values obtained from the detailed switched model, extensive simulations

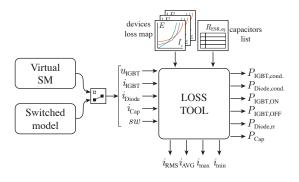


Fig. 8: Loss calculation tool diagram.

for different operating points are carried. The losses are computed in the positive branch of phase-leg a, but any other branch could have been selected. The waveforms are recorded over ten fundamental AC grid periods before the loss tool is invoked, in order to mitigate the instantaneous loss difference between the SMs. The average losses per SM are obtained from the VSM (representing a complete branch) by simple division by N_{sm} .

The conduction losses are accurately estimated by the VSM method, as based on the branch current RMS value, which is unaffected by the branch current ripple. The switching losses are less accurately estimated by the proposed method. The reason behind is that they depend on the instantaneous switched branch current and SM capacitor voltages. The accuracy dependency is inversely proportional to the apparent branch switching frequency. However, as the switching losses are several orders of magnitude smaller than the conduction losses, the overall semiconductor losses are in good agreement. The complete results, for each modulation method and circulating current injection strategy, are presented in Fig. 9. For each operating point, the left side stacked bars correspond to the VSM

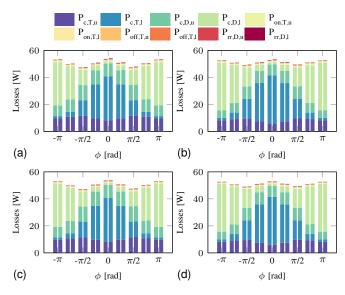


Fig. 9: Averaged semiconductor loss comparison between the VSM method (left side stacked bars) and the switched model (right side stacked bars): (a) PD-PWM with DC circulating current, (b) PD-PWM with DC plus 2nd harmonic injection circulating current, (c) PS-PWM with DC circulating current and (d) PS-PWM with DC plus 2nd harmonic injection circulating current.

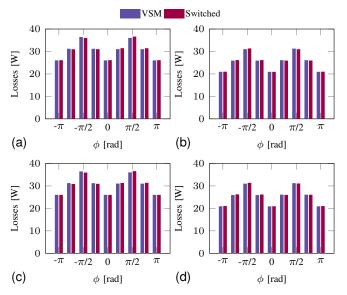


Fig. 10: Averaged SM capacitor bank losses comparison between the VSM concept (left side bars) and the switched model (right side bars): (a) PD-PWM with DC circulating current, (b) PD-PWM with DC plus 2nd harmonic injection circulating current, (c) PS-PWM with DC circulating current and (d) PS-PWM with DC plus 2nd harmonic injection circulating current.

method and the right side stacked bars to the averaged semiconductor losses of the switched model. The split of different loss contributions in function of the load angle ϕ can be easily identified. At the same time, the loss split and the overall losses are almost identical to the results obtained from the VSM concept, demonstrating that the MOD block is able to correctly capture and compress the original switching patterns. Similarly, the averaged capacitor losses are presented in Fig. 10.

The relative errors plots on the total averaged semiconductor and capacitor losses are presented in Fig. 11 and are computed as:

$$\varepsilon = \frac{x_{\text{switched}} - x_{\text{VSM}}}{x_{\text{VSM}}} \cdot 100 \tag{6}$$

Given the assumption required for the VSM concept, a very good accuracy is obtained, as the loss estimation error is below $2\,\%$ for both semiconductor and capacitor losses. The source of this error comes from the branch current ripple and the SM capacitor voltage spread that are not captured by the VSM. These could be mitigated by an enhanced analytical description which goes beyond the objectives of this work. It is important to state that the

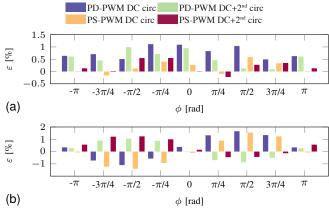


Fig. 11: Relative error plots for each modulation method and circulating current injection strategy: (a) semiconductor average losses and (b) capacitor average losses.

branch current ripple envelope is not simply dependent from the instantaneous branch modulation index, apparent switching frequency and branch inductance value. Similarly, the capacitor voltage spread is not linearly proportional to the apparent branch switching frequency or average capacitor voltage ripple. The proposed concept could be easily extended to include thermal considerations of the MMC design, assuming that the thermal network parameters are available. The VSM allows for a very fast evaluation of the MMC SM's stresses, while considering directly the influence of the circulating current control strategy and impact of different modulation schemes. The detailed switched models takes 300 s for a single operating point to collect data for the loss tool over 10 fundamental cycles, while the VSM takes only $0.5 \, \mathrm{s}$.

7. Conclusion

Starting from a set of relatively simple branch current and voltage equations, with deterministic circulating current injection strategy enabled by a circulating current controller, the averaged MMC converter waveforms have been derived. Those waveforms have been used as inputs for the semiconductor loss tool in combination with the proposed VSM concept. The proposed concept has been compared with switched models of the MMC under two PWM modulation schemes: (i) PD-PWM and (ii) PS-PWM. A compression of a large number of switching pulses is required for the applica-

tion of the VSM concept, which can be easily realized with a quantizer and one suitable carrier. It has been shown that there is a good agreement between the predicted (analytically) and obtained (switched) converter waveforms in steady-state, under the conditions of limited voltage spread among the capacitor voltages of the same branch and limited branch current ripple (compared to the branch current average value). Moreover, the loss difference is within the usual safety margin that is taken for any industrial grade product during the design process. A simulation time benchmarking revealed a speed gain in the range of 600 between the seminumerical and switched simulations. This significant gain is a real advantage for the VSM concept, as a complete converter loss map for any possible operating point can be obtained almost instantaneously. The necessity to run loss calculation in closed-loop operation is fully justified by the particular role of the circulating current in an MMC, and with the aid of the VSM concept, this problem is significantly simplified without any loss of information.

Acknowledgment

This work is part of the Swiss Competence Centers for Energy Research (SCCER) initiative which is supported by the Swiss Commission for Technology and Innovation (CTI) with focus on Future Swiss Electrical Infrastructure (FURIES).

References

- [1] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares stromrichterkonzept für netzkupplungsanwendungen bei hohen spannungen," in *ETG-Fachtagung*, 2002.
- [2] E. Coulinge, A. Christe, and D. Dujic, "Electrothermal design of a modular multilevel converter prototype," in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2016, pp. 1–8.
- [3] A. Christe, E. Coulinge, and D. Dujic, "Insulation coordination for a modular multilevel converter prototype," in 18th European Conference on Power Electronics and Applications (EPE 2016), 2016, pp. 1–10.

- [4] A. Christe and D. Dujic, "Galvanically isolated modular converter," *IET Power Electronics*, vol. 9, no. 12, pp. 2318–2328, 2016.
- [5] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.
- [6] J. Freytes, F. Gruson, P. Delarue, F. Colas, and X. Guillaud, "Losses estimation method by simulation for the modular multilevel converter," in *IEEE Electrical Power and Energy Conference (EPEC)*, Oct. 2015, pp. 332–338.
- [7] S. Rodrigues, A. Papadopoulos, E. Kontos, T. Todorcevic, and P. Bauer, "Steady-state loss model of half-bridge modular multilevel converters," *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2415–2425, May 2016.
- [8] A. Lopez, D. E. Quevedo, R. Aguilera, T. Geyer, and N. Oikonomou, "Reference design for predictive control of modular multilevel converters," in 4th Australian Control Conference (AUCC), Nov. 2014, pp. 239–244.
- [9] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4568–4579, Sep. 2014.
- [10] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.
- [11] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
- [12] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier pwm," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 268–283, Jan. 2015.
- [13] N. Cherix, "Functional description and control design of modular multilevel converters: Towards energy storage applications for traction networks," PhD thesis, École Polytechnique Fédérale de Lausanne, 2015.
- [14] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 349–357, Jan. 2015.