Ambipolar Triple Cation Perovskite Field Effect Transistors and Inverters

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Organolead halide perovskites (ABX_3 where A is organic or inorganic cation, B is metal cation, and X is halogen anion) have significant attention as light absorber for highly efficient perovskite solar cells. Although having optimal bandgap, high absorption coefficient, and long-range exciton diffusion length,[1–3] methylammonium lead iodide ($MAPbI_3$) deteriorates at 85 °C due to the volatility of MA (methylammonium) cation.[4] Formamidinium lead iodide ($FAPbI_3$) is an interesting material due to its enhanced absorption in the red than that of $MAPbI_3$; however, the structural stability of α-phase is not good and slowly converts into a yellow hexagonal δ-phase. The inorganic perovskite, $CsPbX_3$, where Cs cation is less volatile, therefore is suitable to improve thermal stability[4–13] but it is also to circumvent the δ-phase impurities, which acts as recombination centers hampering further progress. There has been a growing interest in $MAPbI_3$ perovskite for use in light-emitting field effect transistors,[14] hybrid perovskite phototransistor,[15] and hybrid halide perovskite field effect transistors (PFETs).[16] Mei et al. were able to demonstrate PFETs with balanced ambipolar hole (μ_h) and electron (μ_e) mobilities of 1.3 and 1 cm^2 V^{-1} s^{-1} at room temperature.[16]

Here, we address the issues of thermal stability by integrating the inorganic Cs and organic cations in perovskite film, resulting in suppression of the photoinactive hexagonal δ-phase for PFETs. With precise tuning the inorganic cation stoichiometry in series $Cs_x(MA_{0.17}FA_{0.83})_{1-x}Pb(Br_{0.17}I_{0.83})_3$ (triple cation) compositions, where x ranges from 0% to 30%, we noticed the photoinactive hexagonal phase has been eliminated, achieving the high quality defect-free, thermally and structurally stable perovskite films with a bandgap of 1.6 eV. We have fabricated solution-processed ambipolar perovskite PFETs featuring both μ_e and μ_h exceeding 2 cm^2 V^{-1} s^{-1}, respectively, using triple cation perovskite. The output voltage gains of >20 were achieved from the complementary-like inverters. These ambipolar PFETs

and inverters exhibit the best performance among perovskite PFETs. The present work demonstrates that triple cation perovskite can provide the ambipolar PFETs and complementary metal-oxide-semiconductor (CMOS)-like circuits for next generation, large-area microelectronics with low manufacturing cost.

The PFETs with bottom contacts and a top gate were constructed by spin coating the triple cation precursor solution in anhydrous dimethylformamide:dimethylsulfoxide (DMF:DMSO) 4:1 (v:v) on the substrates (**Figure 1**a). The perovskite solution was deposited in two steps at 1000 and 6000 rpm for 10 and 30 s, respectively. Solvent treatment was conducted during the second step, where 100 µL chlorobenzene was poured on the spinning substrate followed by annealing at 100 °C for 1 h. Triple cation PFETs with various Cs amounts were fabricated, and their respective transfer and output characteristics are compared in Figures S1–S6 (Supporting Information). Figures S1–S6 (Supporting Information) illustrate transfer curves of the ambipolar triple cation PFETs, and $I_{DS}^{1/2}$ versus V_{DS} plot as a function of Cs cation. As Cs increased from 0% to 10%, the mobility increased monotonically from 1.95×10^{-2} to 1.25 cm^2 V^{-1} s^{-1} for holes and from 4.81×10^{-2} to 4.11×10^{-2} cm^2 V^{-1} s^{-1} for electrons (Table S1, Supporting Information). However, no significant change in the charge-carrier mobilities was observed when Cs is higher than 15%. Figure 1b,c demonstrates the transfer characteristics for the p- and n-channel PFETs (Cs = 15%), respectively, with poly(methyl methacrylate) (PMMA) as a gate dielectric, in which ambipolar charge-transport characteristics were observed. Figure 1d,e represents the typical output characteristics with good current modulation. PMMA was selected since it can be processed at low temperature, soluble in a solvent orthogonal to triple cation, and contains negligible −OH groups that could trap electrons. When V_{DS} is low, the potential for the hole and electron injection cannot exceed the threshold voltage simultaneously. As a result, only one carrier can be accumulated, and the devices work in the unipolar model. Under these conditions, the transistors exhibit a very high I_{ON}/I_{OFF} ratio, typically higher than 10^4 at a high gate voltage ($V_{GS} = 130$ V). The charge-carrier mobilities were determined using the drain current (I_{DS}) in the saturation region; $I_{DS} = \frac{1}{2}(W/L)\mu C_i(V_G - V_T)^2$. Table S1 (Supporting Information) summarizes the maximum and average p- and n-channel mobilities. The maximum μ_h and μ_e mobilities are calculated to be 2.1 and 2.5 cm^2 V^{-1} s^{-1}, respectively. To the best of our knowledge, this is the highest carrier mobility for the perovskite PFETs.[17] The incorporation of Cs cation (Cs = 0%–30%) has notable effect on the performance of ambipolar triple cation PFETs.

We have exposed freshly prepared PFETs to ambient air and monitored the p- and n-channel performance as a function of

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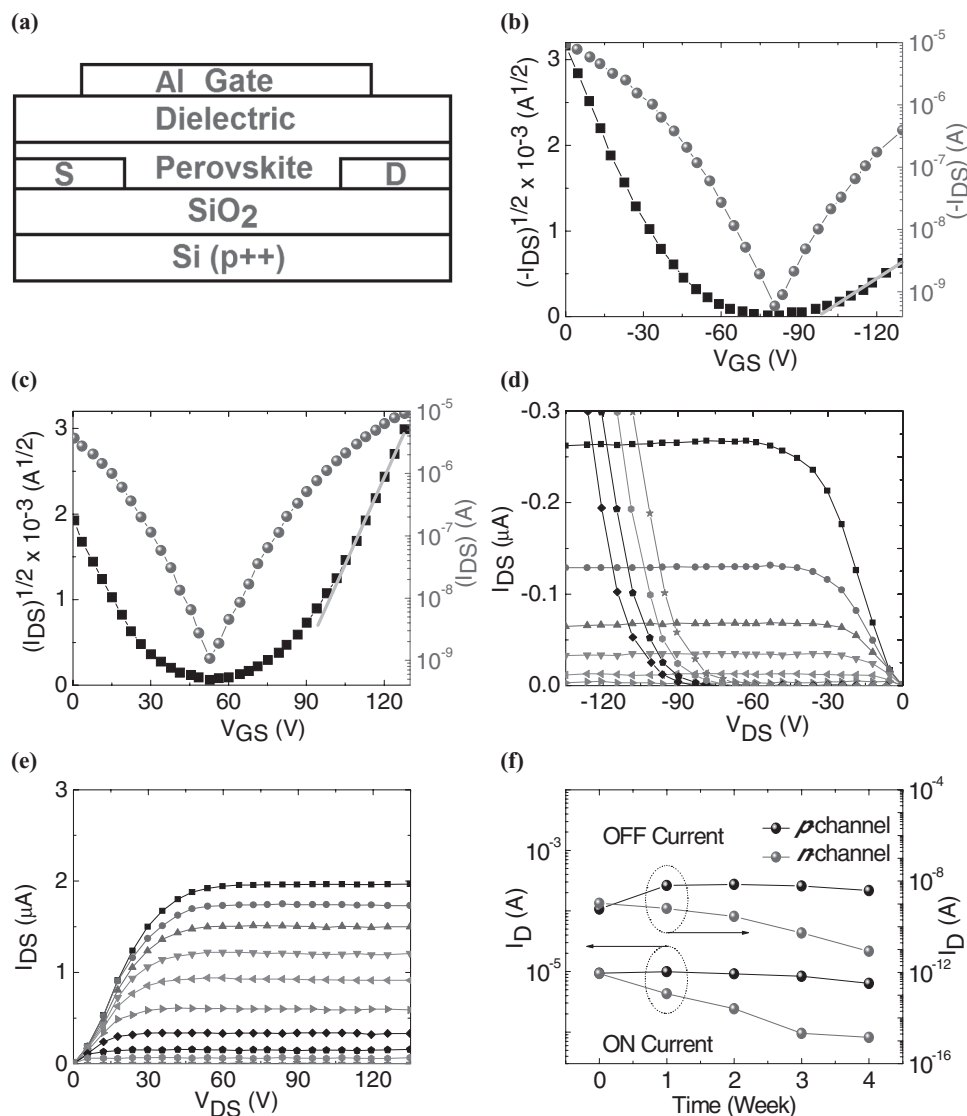
Figure 1. Device structure and characteristics. a) Schematic diagram of triple cation perovskite field-effect transistors (channel length and width were 20 µm and 1 mm, respectively). b) Transfer characteristics in the p-channel and c) n-channel of triple cation ambipolar transistor; $V_{DS} = -100$ and 100 V. The slope used in mobility calculation reported in this study is shown by the solid line. The corresponding output characteristics of PFETs annealed at 200 °C for d) p- and e) n-type channels; $V_{GS} = 0$–90 V with a step of 10 V. f) Evolution of the OFF and ON currents for both p-channel (measured at $V_D = -80$ V, and $V_{GS} = -90$ V) and n-channel (measured at $V_D = 80$, and $V_{GS} = 90$ V) as a function of exposure time to ambient air over a period of 4 weeks on degraded devices. Devices were stored in the dark and in air with a relative humidity in the range 45%–65%.

exposure time. The relative humidity of the ambient atmosphere during testing was fluctuating in the range 45%–65%. Figure 1f displays the ON and OFF currents of the PFETs as function of exposure time to ambient air over a period of 4 weeks on degraded devices. The ON currents for p- and n-channel decrease slightly with time but the fluctuation for the OFF currents are relatively high. It can be seen that carrier transport (holes and electrons) remains almost unaffected by the ambient air with small variations observed mainly in the OFF currents of both channels. We note that these changes do not significantly affect the operation of the PFETs. Similarly, the hole and electron mobility remains unaffected by the presence of ambient air with only the slight decrease in μ_e and small increase in μ_h. These observations suggest that perovskite thin films loaded with Cs cation demonstrate better stability to moisture probably due to the suppressed yellow hexagonal-to-black phase transition by structural stabilization. Such good stability is not surprising since triple cation perovskite is known to exhibit environmentally stable photovoltaic performance.[13] In our previous study, we demonstrate that perovskite thin films slowly degrade (at 130 °C for 3 h) when loaded with 10% Cs cation, whereas the perovskite thin films experience severe degradation after heat treatment, by an observable decrease in absorption coefficient. Hence, we believe that with appropriate amount of Cs cation could stabilize the perovskite structure. We have fabricated 36 PFETs where the average mobility is 2.39 and 2.02 cm^2 V^{-1} s^{-1} for the electron and the hole, respectively (Figure S7a,b, Supporting Information).

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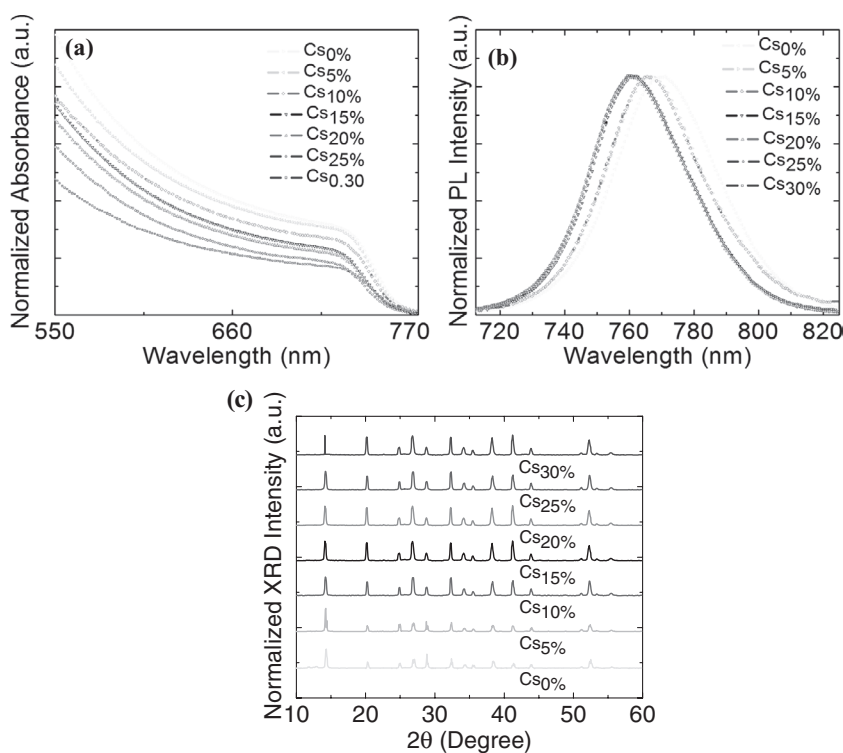
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As shown in **Figure 2**a, perovskite film displays a broad absorption down to the near-infrared region, while the photoluminescence (PL) peaks at ≈770 nm (Figure 2b) and an optical gap of ≈1.6 eV (Figure 2a). From absorption and emission spectra, a blueshift of 8 nm in the absorption can be seen as Cs cation increases from 0% to 30%, which is consistent with theoretical calculation that inorganic Cs has a minor effect on the bandgap of perovskite. We also found that triple cation formed uniform and continuous film along with big grain size.

To further understand the influence of Cs cation on the structural of the perovskite, we investigated the X-ray diffraction (XRD) patterns for the thin films with the composition $Cs_x(MA_{0.17}FA_{0.83})_{1-x}Pb(Br_{0.17}I_{0.83})_3$ in which x was varied from 0% to 30%. Figure 2c shows XRD pattern with perovskite peaks at ≈14°, 28° and 43° (for all thin films) corresponding to (110), (220), and (314) tetragonal plane perovskite phase, respectively.[18,19] Weak diffraction patterns at 11.6° and 12.7° were observed for Cs_0, suggesting the presence of the yellow hexagonal δ-phase of $FAPbI_3$ and cubic PbI_2, respectively. However, the photoinactive nonperovskite phase and cubic PbI_2 diffraction peaks disappeared with incorporation of Cs. The impact of Cs cation on the crystal lattice of $Cs_x(MA_{0.17}FA_{0.83})_{1-x}Pb(Br_{0.17}I_{0.83})_3$ can be understood with the formation of black perovskite phase from yellow nonperovskite phase, where the tolerance factor (t) shifted toward a cubic structure ($0.8 < t < 1$) from higher than 1 of hexagonal structure.[20] This indicates that the introduction of Cs cation into the perovskite precursor solution not only induces the gradual formation of the black perovskite phase by bringing the perovskite system into a new equilibrium state or by suppressing of the hexagonal yellow phase of perovskite but also stabilizes the perovskite phase as well as induces highly uniform perovskite grains.[21]

The balanced performance of p- and n-channel PFETs as well as the fact that both transistors strictly behave as normally off transistors at zero gate voltage enables the construction of CMOS like inverters. The circuit consists of two PFETs, with a triple cation as the active layer. The two PFETs in a complementary inverter were designed with an input and output terminals, which is the same as a conventional CMOS inverter. The load and driver TFTs of a PFET inverter are biased to power supply (V_{DD}) and ground potential, respectively. Here, the power and ground terminals are interchangeable because the unit PFETs are virtually identical.
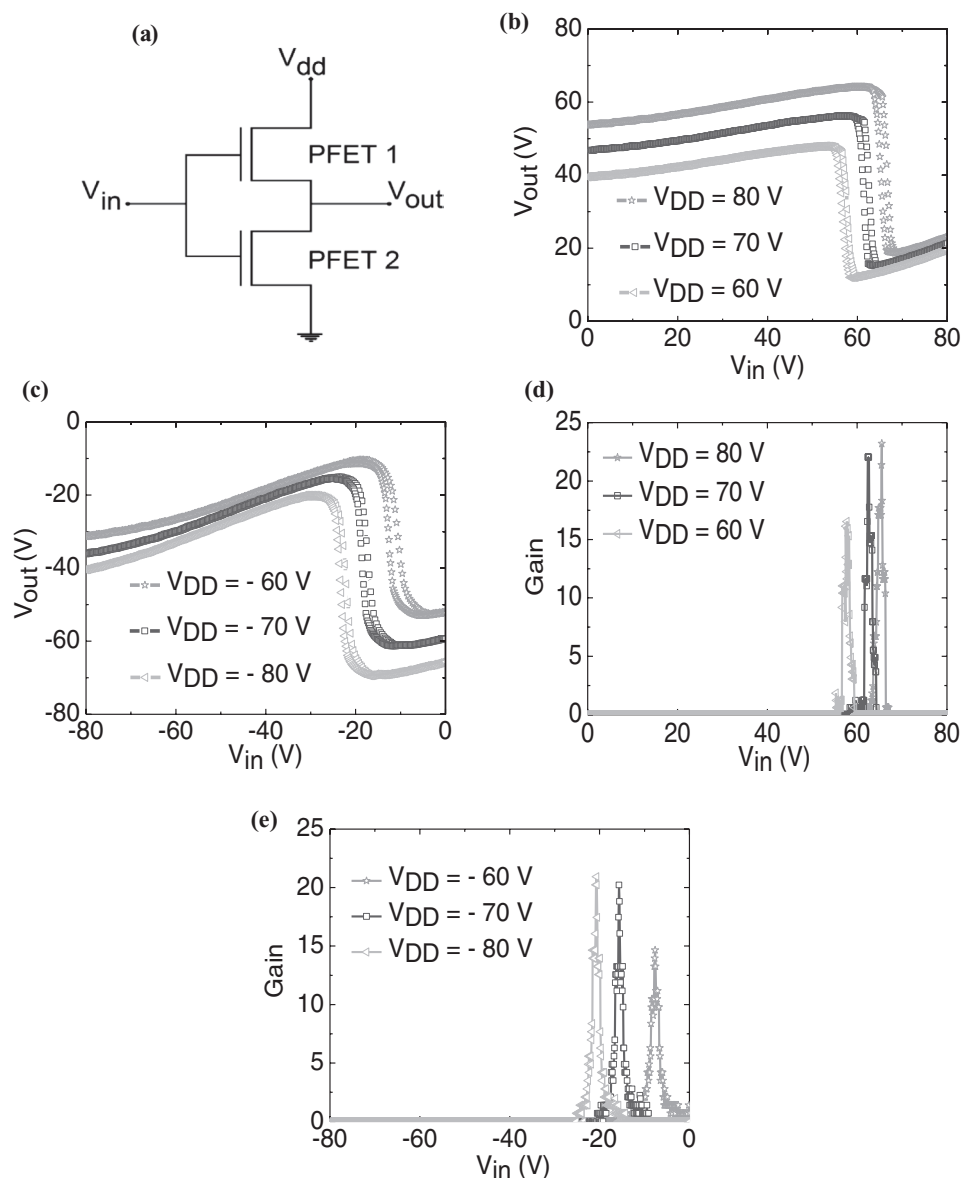
Figure 3 shows the voltage transfer characteristics (V_{OUT} vs V_{IN}) of the inverters with various supplied voltages, V_{DD}. At the steady state where V_{IN} is either near 0 V or near the supplied voltage, V_{OUT} has an offset from the ideal output voltage (V_{DD} or 0 V). The amount of offset decreases as V_{IN} approaches the switching point. The minima of I_{DS} in the transfer curves of the transistors shifted from 0 V of the gate. One of the distinctive features of ambipolar over unipolar inverters is that the ambipolar inverter can efficiently be operated in the first and third quadrants, which is due to the tunable channel conductivity for electrons and holes. A schematic image of such a complementary inverter circuit is displayed in Figure 3a together with the voltage transfer characteristics (VTCs) of the PFETs and the static gain measured in two quadrants: with positive operation voltages of V_{DD} = 60, 70, and 80 V (Figure 3b). The inverter operates in the first quadrant for all operation voltages, gains above 16 were measured with maximum gain of 23 for V_{DD} = 80 V (Figure 3d), whereas under negative operation voltages of V_{DD} = −60, −70, and −80 V (Figure 3c), the inverter operates in the third quadrant with maximum gain of 21 for V_{DD} = −80 V (Figure 3e). The sharp switching is one of the main advantages of complementary logic gates. Similar switching characteristics were observed from the first and third quadrants depending solely on the polarity of the applied biases. This means that the constituent transistors have comparable performance and there is negligible variation in the capability of the transistors on a common substrate. The high gain comes from the sharp output voltage change at the transition region for p- and n-channel PFETs. To the best of our knowledge, these are the first reported ambipolar PFETs and inverters.

In conclusion, air-stable, solution processed, and low-temperature processing offered via replacing methyl ammonium cation by triple cation in perovskite exhibits significant stability, and ambipolar charge transport in solution-processed perovskite field-effect transistors exceeding 2 cm² V⁻¹ s⁻¹. With these, we developed thin film field-effect transistor-like inverters, where we attained maximum gain of 23 in the first quadrant for V_{DD} = 80 V. The triple cation perovskite will open new pathway

Figure 2. Material characteristics. a,b) Absorption and photoluminescence spectra of triple cation perovskite films used in this study. c) XRD pattern of similar films.

Figure 3. CMOS-like ambipolar triple cation perovskite inverter. a) Schematic configuration for the inverter based on two identical PFETs (channel length and width were 20 μm and 1 mm, respectively.). b,c) Voltage transfer characteristics for CMOS-like inverters with triple cation as the absorber layer measured at different supply voltage ranging from b) 60 to 80 V in the first quadrant, and c) −60 to −80 V in third quadrant. The maximum gain was determined to be d) 23 and e) 21 in the first and third quadrants, respectively. V_{in}: input voltage; V_{out}: output voltage; V_{DD}: supply voltage.

not only understand fundamental properties but also providing a low-temperature solution processable for next generation thin film transistors and inverters.

Experimental Section

Materials: The organic cations were purchased from Dyesol; the lead compounds were purchased from TCI (Tokyo chemical industry); and CsI was purchased from abcr GmbH. The "mixed" perovskite precursor solutions were deposited from a precursor solution containing FAI (formamidinium iodide,1 M), PbI_2 (1.1 M), MABr (0.2 M), and $PbBr_2$ (0.2 M) in anhydrous DMF:DMSO 4:1 (v:v). Then CsI, predissolved as a 1.5 M stock solution in DMSO, was added to the mixed perovskite

precursor to achieve the desired triple cation composition. PMMA and decyltrichlorosilane (DTS) were purchased from Argos Organic Chemicals.

Fabrication and Characterization of FET Devices: Bottom-contact, top-gated PFETs were constructed on Au-patterned source and drain electrodes that were placed on an insulating substrate. The contacts were defined by photolithography and deposited using e-beam evaporation and lift-off. The source and drain electrodes were patterned using standard photolithography and were formed on a heavily p-doped Si substrates with thermally grown prepatterned SiO_2 substrates (500 nm) which were sequentially clean in acetone, toluene, and isopropyl alcohol for 15 min each, later dried in an oven at 120 °C for 15 min, then exposed for 1.5 h to UV light in air before finally the clean prepatterned UV treated SiO_2 substrates surface were treated with DTS for 0.5 h by immersion in a 1% by volume of DTS in toluene.

The triple cation perovskite semiconductor layer was then spin coated on source and drain electrodes in a two steps program at 1000 and 6000 rpm for 10 and 30 s, respectively, in a nitrogen-filled glove box. During the second step, 100 µL of chlorobenzene was poured on the spinning substrate 15 s prior to the end of the program. The thickness of perovskite layer was ≈250 nm. For the as-spun PFETs, the samples were then annealed at 100 °C for 1 h in a nitrogen-filled glove box. For the annealed PFETs, the samples were further annealed at 150 °C for 20 min. Later, PMMA (M_w = 319 kg mol^{-1}) dissolved in anhydrous n-butyl acetate (45 mg mL^{-1}) was spin coated at 600 rpm onto the perovskite film (PMMA thickness = 550 nm). The samples were subsequently annealed at 80 °C for 30 min and kept under high vacuum (10^{-6} – 10^{-7} Torr) overnight (>10 h) to remove any residual solvent. Finally, Au top-gate electrode was deposited by thermal evaporation through a shadow mask onto the dielectric. The Agilent 4156C precision semiconductor parameter analyzer was used to monitor all electrical measurements. TFTs' current–voltage characteristics were measured in dark and at room temperature in air, where the voltage scan rate was at 10 mV s^{-1}. The TFT's turn-on voltage (V_{ON}) was taken as the gate voltage (V_{GS}) at which the drain current (I_{DS}), measured with drain voltage (V_{DS}) = 0.1 V, started to monotonically increase. The field-effect mobility (µ) was determined using $\frac{\partial |I_{DS}|^{1/2}}{\partial V_G}$. Samples measured had channel lengths of 20 µm and channel widths of 1 mm. The environmental stability of the devices was also checked by exposing the transistors to low-humidity air and then again measuring the current–voltage characteristics at regular time intervals for a total of 4 weeks.

Scanning Electron Microscopy: The scanning was conducted using a SEM, Hitachi S-4700.

X-Ray Diffraction: XRD measurements were carried out using X'PERT PRO of PANalytical Diffractometer with a Cu Kα source (wavelength of 1.5405 Å).

Photoluminescence: PL spectra were recorded using a lock-in technique with JASCO FP-6500 composed of two monochromators for excitation and emission, a 150 W Xe lamp with shielded lamp house, and a photomultiplier as light detector.

UV–vis Spectroscopy: Absorption spectra were collected with a Varian Cary 300 UV–vis spectrophotometer with an internally coupled integrating sphere.

Thickness Measurements: The film thickness was measured using a Dektak AlphaStep Profiler.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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