Virtual Submodule Concept for Fast Semi-Numerical Modular Multilevel Converter Loss Estimation

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Abstract—During the design phase of a modular multilevel converter (MMC), an accurate loss evaluation of the submodule (SM) plays an important role. In this paper, a method based on the analytical description of the MMC key waveforms that allows to directly obtain the average semiconductor and capacitor losses that each SM will experience is introduced, under different operating conditions or control schemes. To verify the proposed concept, the results are compared with the losses obtained from a switched model with closed-loop control, where the analytical MMC key waveforms are approached in steady state. The proposed method provides a great flexibility and a significant reduction of the simulation/computational time otherwise needed to evaluate SM losses under various operating conditions.

Index Terms—Modular multilevel converters (MMCs), pulse width modulation (PWM), semiconductor losses.

I. Introduction

Modular multilevel converters (MMCs) have been quickly adopted by the industry for HVDC applications, outperforming existing voltage-source converters and line-commutated inverters both in terms of efficiency and controllability. Thanks to their modular nature, a single submodule (SM) has to be designed. In that design process, an accurate loss evaluation is mandatory. Unlike classical topologies, MMC features an additional degree of freedom: the circulating current—an internal quantity used to control the converter's internal energy balance. The circulating current can be shaped by some control objective and its harmonic content is subject to variation, involving both DC and AC components of certain frequencies. During operation, this affects the semiconductor losses and has to be accounted for. In contrast to conventional converter topologies, it makes sense to calculate the losses in closed-loop operation, where the shape of the circulating current can be accurately

determined. This is further motivated by the fact that the required branch inductance values for direct modulation operation, where the circulating current is not actively controlled, are much larger compared to the case with active circulating current control, as attested by the impedance comparison in [1], which revisited the findings from [2]. Hence, if the circulating current is actively controlled, the sensitivity to the choice of the branch inductance is significantly reduced, as it is almost fully decoupled from the shape of the circulating current, as long as the provided inductance allows to get control over the circulating current.

Regarding the modulation, two concurrent pulse width modulation (PWM) methods are found in the literature: 1) based on level-shifted PWM combined with a sorting algorithm (as originally proposed in [3]) and 2) based on phase-shifted PWM (PS-PWM) (as initially proposed in [4]) with an inherent branch balancing capability if the switching frequency is not an integer multiple of the fundamental AC grid frequency [5]. With the latter method, some uncertainty stemming from the sorting algorithm has to be managed or circumvented, as the link between the apparent switching frequency (branch voltage waveform) and the SM switching frequency is not obvious. So far, to the best knowledge of the authors, the influence of the modulation scheme and branch balancing method on the SM losses has not been evaluated. While the conduction losses depend on the operating point of the converter and thus cannot be reduced through control means once the circulating current harmonic content is set, the switching losses directly depend on the switching frequency experienced by each SM, its position inside the switching sequence and associated voltages and currents.

The MMC prototype, currently under development, has the following rating: 10 kV DC bus, 0.5 MVA apparent power and uses 96 SMs with low-voltage insulated gate bipolar transistor (IGBT) semiconductors (Semikron, SK 100 GH 12T4 T) that can be configured into unipolar or bipolar SM [6], [7]. The targeted application is the interconnection of the widely deployed 400 V low voltage AC (LVAC) grid, or corresponding microgrid, with the emerging medium voltage DC (MVDC) grids (10 kV is considered in our case) [8]. For that reason, the converter has to deal with a large voltage ratio and the use of a transformer for galvanic isolation and voltage adaption is mandatory. The MMC with external low frequency transformer (LFT) is presented in Fig. 1.
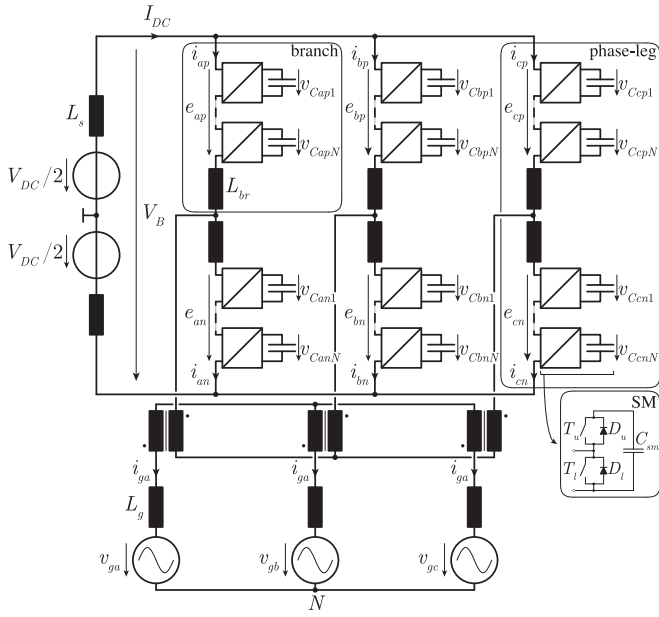
Fig. 1. MMC with external low frequency transformer (LFT) for DC/3-AC conversion with large voltage ratio. Each branch comprises N_{sm} series-connected unipolar submodules (SMs).

To aid system design, this paper proposes a semi-numerical method for loss calculation of the MMC SM using the virtual submodule (VSM) concept. The MMC semiconductor losses were obtained by simulation [9], [10] or numerically considering direct modulation for HVDC application in mind, with a DC circulating current and without considering the capacitor losses [11]. In contrast, the proposed method allows for a fast estimation of the SM losses under different operating conditions, control schemes (e.g., effects of the circulating current injection strategy), and modulation methods under the assumption of a stable operation of these schemes in steady state. To verify the validity of the proposed method, a comparison with a fully switched converter model has been carried out.

This paper is organized as follows: Section II presents the analytical description of the key MMC waveforms relevant for the scope of the paper. The proposed method is described in Section III. The switched model along with a brief description of its control scheme are presented in Section IV, and is used for benchmarking purposes. The loss tool and its integration into the models is presented in Section V. Simulation results along with a comparative assessment are presented in Section VI. Summary and conclusion are provided in Section VII.

II. ANALYTICAL DESCRIPTION OF THE MMC KEY WAVEFORMS

The analytical averaged model accounts for all parasitic elements in the circuit, especially the branch inductance L_{br}, which was the main motivation of [12] compared to the simplified models of [13], [14], as well as the circulating current in steady state, where no large branch energy imbalances occur. The derivation starts from the expressions of the branch voltage ($e_{p/n}$) and current ($i_{p/n}$). Two scenarios for the branch voltage have to be accounted for in (1), depending on the presence or not of a

common mode (CM) voltage term made from a combination of one or more triplen harmonics, which can be used to extend the linear modulation range up to $k_{AC} = 2/\sqrt{3}$. In addition, two scenarios can be analyzed regarding the shaping of the circulating current in (2): 1) no second harmonic circulating current, which corresponds to a circulating current suppression controller alike behavior and 2) second harmonic circulating current injection, which was initially proposed in [13] to reduce the capacitor voltage ripple. Consequently, the branch current contains three terms:

1) a DC term, which corresponds to the active power exchange between the DC and AC grids;
2) a fundamental frequency AC term, which corresponds to half the AC grid current i_g;
3) an optional second harmonic circulating current term, with amplitude $\hat{i}_{circ,2}$ and phase $\theta_2 = \phi$

$$e_{p/n} = \frac{V_{DC}}{2}\left(1 \mp k_{AC}\cos\left(\omega t - \frac{2\pi(k-1)}{3}\right) \mp v_{CM}\right)$$
$$- \left(R_{br}i_{p/n} + L_{br}\frac{d}{dt}i_{p/n}\right) \qquad (1)$$

$$i_{p/n} = \underbrace{\frac{I_{DC}}{3}}_{\text{DC term}} \underbrace{\pm \frac{1}{2}\hat{i}_g\cos\left(\omega t + \phi - \frac{2\pi(k-1)}{3}\right)}_{\text{fundamental AC term}}$$
$$\underbrace{+ \hat{i}_{circ,2}\cos\left(2\omega t + \theta_2 - \frac{2\pi(k-1)}{3}\right)}_{\text{optional second harmonic term}} \qquad (2)$$

where V_{DC} is the DC-link voltage, $k_{AC} = 2\hat{v}_g/V_{DC}$ the voltage ratio between the three-phase and DC grids, ω the grid frequency, $k \in \{1, 2, 3\}$ the phase number, S the apparent power of the converter and ϕ the load angle. The expressions for $\hat{i}_g$ and $\hat{i}_{circ,2}$ are given in the following equations:

$$\hat{i}_g = \frac{2S}{3\hat{v}_g} = \frac{2S}{3k_{AC}V_{DC}/2} \qquad (3)$$

$$\hat{i}_{circ,2} = \frac{\hat{v}_g\hat{i}_g}{2V_{DC}} = \frac{S}{3V_{DC}}. \qquad (4)$$

The expression for the DC current is subject to a quadratic equation, whose negative root is generally selected [15]

$$I_{DC} = \left[V_{DC} - \sqrt{V_{DC}^2 - 8R_{br}\left(\frac{\hat{v}_g\hat{i}_g}{2}\cos(\phi)\right) + 2R_{br}\left(\frac{\hat{i}_g^2}{8} + \frac{\hat{i}_{circ,2}^2}{2}\right)}\right] / (4R_{br}). \qquad (5)$$

The next steps resemble the method used to size the branch capacitor: The branch power variation is obtained by taking the product of (1) and (2). Then, by integration, the branch energy variation is obtained and centered around 0, which is further transformed into a capacitor voltage ripple ($\langle v_{C\Sigma p/n}\rangle = \sqrt{2(E_{C0} + \tilde{E}_{Cp/n})/C_{br}}$ with $E_{C0} = C_{br}(k_{DC}V_{DC})^2/2$ to ac-
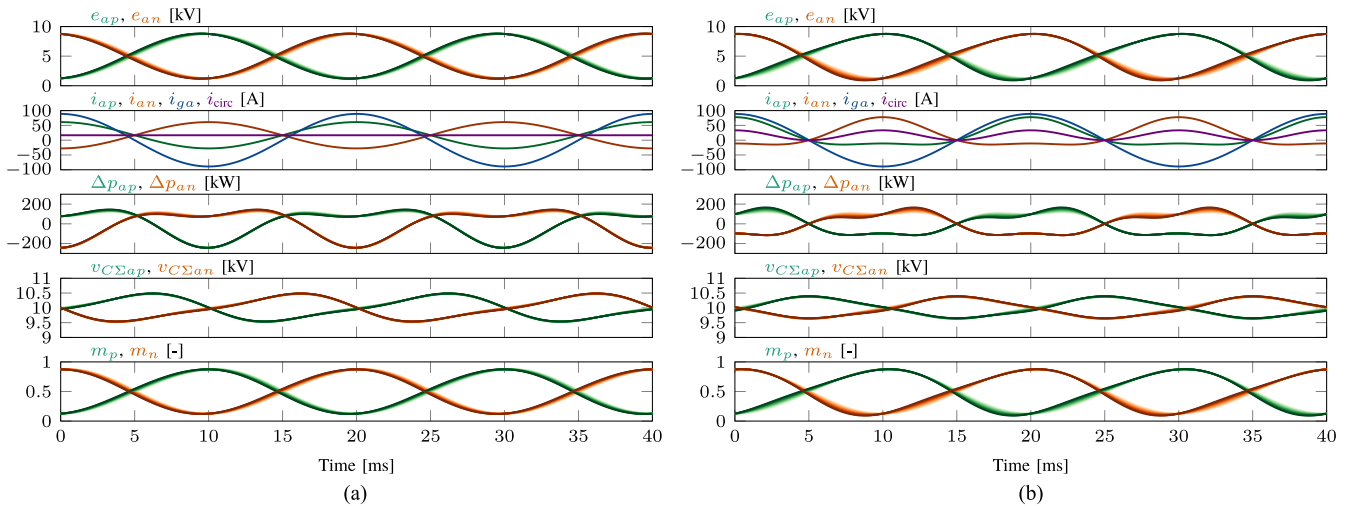
Fig. 2. Branch representative waveforms with: (a) DC circulating current and (b) DC plus second harmonic circulating current injection. The branch inductance value is swept from 0 H (light shade) to 50 mH (dark shade) to highlight the impact of the branch inductance voltage drop. The currents are not impacted by L_{br}, as they are set for a given power transfer and no ripple is considered.

TABLE I
SYSTEM PARAMETERS

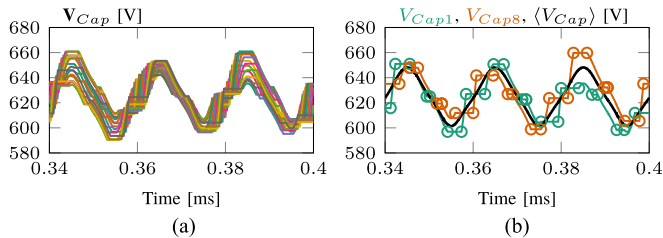| V_{DC}	10 kV	S	0.5 MVA	N_{sm}	16
R_{br}	0.1 Ω	k_{AC}	0.75	C_{sm}	1.9 mF
k_{DC}	1	L_{br}	10 mH	R_{esr} [a]	110 mΩ

[a] Per individual capacitor.

Fig. 3. Branch ap capacitor voltages over three fundamental grid periods obtained from a switched model with PS-PWM and $\phi = 0$: (a) 16 SMs capacitor voltages and (b) 2 out of 16 SMs capacitor voltages versus branch average in black. The switching instants are indicated by circles. Note that as the SM switching frequency (187.375 Hz) is not an integer multiple of the grid frequency, each SM capacitor voltage has not the same periodicity as the grid frequency.
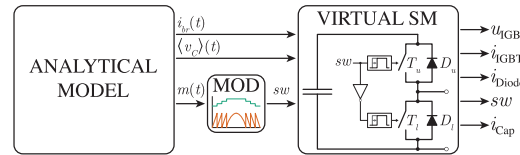

Fig. 4. Functional VSM concept, where the MOD block is implemented with a single carrier and a quantizer. It produces an output identical to a collection of all switching events from any modulation scheme.

capture them in the VSM concept). Otherwise, there will be an error coming from the nonlinearity of the switching losses.
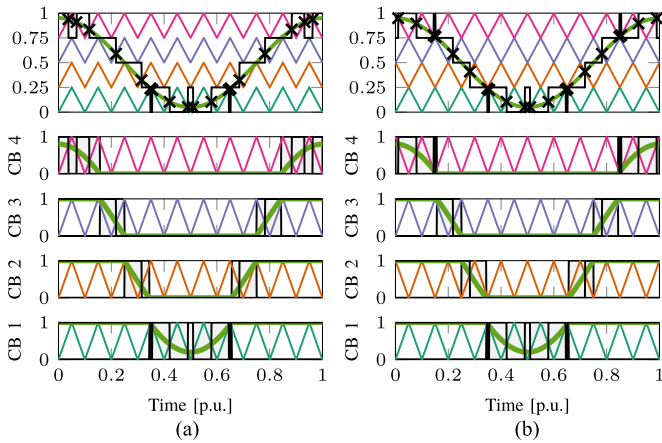
III. VSM CONCEPT

Considering the operating principle of an MMC and the previously introduced assumptions, all the relevant waveforms are identical for each SM. The modulation can be modified in order to capture and direct all switching events to only one VSM, as shown in Fig. 4. The VSM concept allows for significant simplifications, and its validity is restricted under the conditions already discussed. Thus, a slight deviation from a purely analytical method is required in order to compress multiple PWM signals into a representative train of pulses.

A. MOD Block

The classical case is presented in Fig. 5, for both PD-PWM on the right-hand side and PS-PWM (or APOD-PWM, as the obtained switching pattern is identical) on the left-hand side. All the switching events that occur in the four carrier bands, that are by essence two-level switching waveforms (alternating turn-ON—turn-OFF—turn-ON sequence) are summed up in order to obtain the multilevel switching pattern. Each switching event is denoted by a ✖ symbol. The carrier bands are defined as the levels $\{0, 1/N_{\mathrm{sm}}, \ldots, 1\}$, i.e., $N_{\mathrm{sm}} + 1$ voltage levels are synthesized by a branch with two-level unipolar SMs. Each carrier band is "active" only when the reference signal is between the

count for a capacitor charging level as $V_{C\Sigma}^{\star} = k_{\mathrm{DC}} V_{\mathrm{DC}}$) that finally leads to the branch modulation index expressions $m_{p/n} = e_{p/n}/\langle v_{C\Sigma p/n} \rangle$. The analytical expressions for these quantities can be found in [12].

The relevant waveforms are illustrated in Fig. 2. They are directly plotted using the above derived set of expressions and the parameters of Table I.

Please note that the underlying assumptions here are that the voltage deviation of each capacitor in a branch with respect to the average branch capacitor voltage is negligible to compute the switching losses (see Fig. 3) and that the branch current ripple is small enough to be neglected (it is not an objective to

Fig. 5. From multilevel PWM to carrier bands for $N_{sm} = 4$ for (a) phase-disposition PWM (PD-PWM) and (b) alternate phase-opposition disposition PWM (APOD-PWM). The resulting switching pattern, in black in the top plots, is obtained by summing each individual switching pattern from the carrier bands (with proper $1/N_{sm}$ scaling). The gray shaded areas on the carrier bands plots show the "active" carrier, which defines the carrier used for the single-carrier PWM. Please note that for illustration purpose a sinusoidal reference signal has been selected, but the single-carrier PWM is not limited to sinusoidal reference.
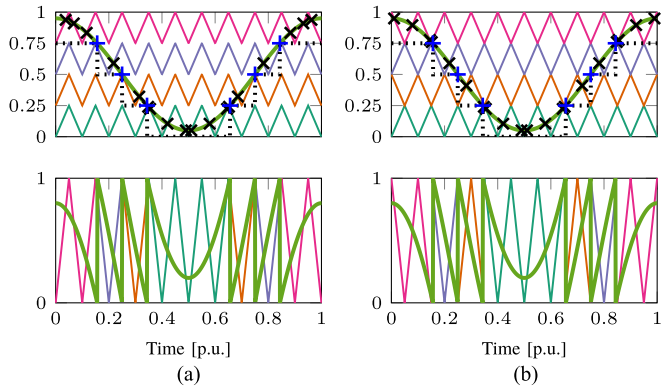
Fig. 6. Single-carrier principle for $N_{sm} = 4$ for (a) PD-PWM and (b) APOD-PWM. The quantizer signal (dotted curve in the upper plots) is similar to a floor function and is only a function of the reference signal and N_{sm}. For the single-carrier PWM (lower plots), first the single carrier is collected from the different gray shaded areas and then is compared with the single-carrier reference signal.

upper and lower bound of one carrier band. Hence, those intervals could be all connected together to form the single-carrier PWM.

The single-carrier PWM principle is shown in Fig. 6, again for both PD-PWM and PS-PWM/APOD-PWM. In the top plot, the dotted line corresponds to the quantizer signal, defined as floor $(N_{sm} \cdot \text{ref}) / N_{sm}$. The intersection of the reference with the carrier bands are denoted by a ✚ symbol. Those events do not coincide with the switching transitions of Fig. 5. The single carrier is constructed by merging the active carrier regions into one signal. For PD-PWM, as the carriers are identical for all bands, the single carrier waveform does not differ from any band carrier waveform. This differs for PS-PWM/APOD-PWM, as the carrier waveforms are phase-shifted by 180° between neighbor-
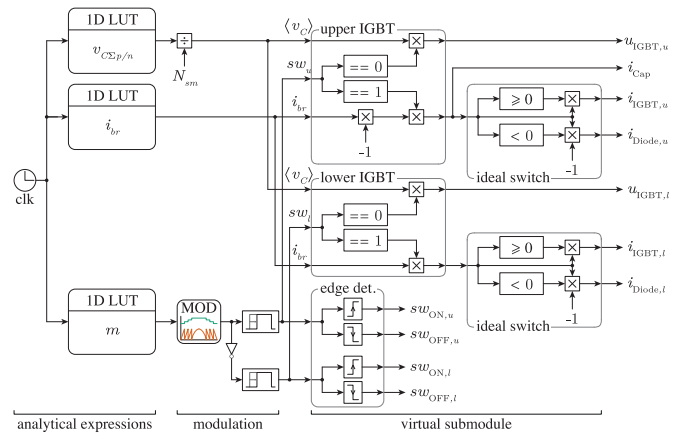
Fig. 7. Detailed VSM concept implementation. $v_{C\Sigma p/n}$, i_{br}, and m are obtained from the analytical model.

ing carrier bands. Therefore, these 180° phase jumps persist in the single carrier waveform. The information contained in the single-carrier switching pattern itself would result in a two-level switching waveform, if the transitions in the quantizer (✚) are not subtracted to it. In the end, the original multilevel switching sequence can be retrieved.

B. VSM Block

To evaluate the MMC losses using the VSM concept, the analytical model is combined with a PWM modulator, from which the switching instants are fetched, as shown in Fig. 7. The analytical expressions are evaluated over the simulation horizon for a given set of parameters and then loaded into 1D look-up tables. The modulation block is implemented with the single carrier and quantizer as illustrated in Fig. 6. Multiple consecutive turn-ON or turn-OFF events, that happen in a multilevel switching pattern, are correctly handled by the VSM implementation that does not rely on a pair of physical switches. Then, the VSM constructs the signals that are routed to the loss tool. As the branch current, capacitor voltage, modulation index, and switching sequence are used as inputs, the VSM concept implementation is unchanged to account for changes in them. The switching instants are collected with the edge detection block (turn-ON and turn-OFF) and stored for further postprocessing and loss calculations. To verify the validity of this concept, a fully switched model of the MMC has been developed in PLECS, as presented next.

IV. MMC SWITCHED MODEL

To compare the analytical method based on the VSM concept with realistic waveforms from a fully switched MMC model, circuit simulations are performed with PLECS/Simulink. The comparison is carried with two modulation methods: 1) PD-PWM and 2) PS-PWM. The former is considered as a centralized modulation method, while the latter can be implemented in a distributed manner. The considered apparent branch switching frequencies are 3 kHz for PD-PWM and 2.95 kHz for PS-PWM. This corresponds to an SM switching frequency of 187.5 and

184.375 Hz, respectively. The presence of a branch balancing method is the underlying requirement for the derivation of the macroscopic level control diagram. The fundamental objective is to ensure an equal energy transfer between all SMs. They are briefly described hereafter for each modulation method.

A. PD-PWM

In order to control the SM switching frequency, the sorting algorithm is not run at every sampling time but rather at every switching event. It is inspired from the reduced switching frequency method proposed originally in [16]. This prevents the insertion of additional switching events that would be induced by a sorting algorithm executed at the apparent branch switching frequency, with group swapping between the bypassed and inserted SMs. Regarding its practical implementation, it is possible to avoid the sorting lists by a substitution with min/max searches, as in steady-state operation only one SM per branch is inserted/bypassed. This is particularly advantageous from a computational load point of view.

B. PS-PWM

Equal switching frequency among all SMs of the same branch is an inherent feature of PS-PWM, as a different carrier is assigned to each SM. On the other hand, it requires a modified branch balancing algorithm [17], that can be partially circumvented in the case of noninteger frequency ratio between the grid frequency and the SM carrier frequency, as it leads to self-balancing [5]. A simple proportional controller compares the instantaneous branch average capacitor voltage with the local averaged measurement and slightly modifies each cell modulation index reference, in combination with the sign of the branch current.

C. Control Diagram

The state-of-the-art MMC control is selected, according to [18]. It is implemented in a cascaded manner, with internal current controllers and external capacitor voltage controllers. The complete control diagram is shown in Fig. 8. Unlike classical topologies, the control of an MMC can be divided into two parts: 1) the inner state variables control (circulating current and capacitor voltages) and 2) the external state variables control (AC grid current, DC voltage). Under the assumption of a working branch balancing algorithm, that ensures a controlled spread among the capacitor voltages within a branch, a macroscopic converter model can be advantageously used for control purpose. The capacitor voltage control is divided in two objectives: 1) the total energy control (TEC), which ensures that the total energy in the converter is kept constant as well as equally distributed between the three phase-legs and 2) the differential energy control (DEC), which ensures that the energy is equally distributed between the upper and lower branch of the same phase-leg. In the literature, TEC is also referred as horizontal balancing and DEC as vertical energy balancing [19].
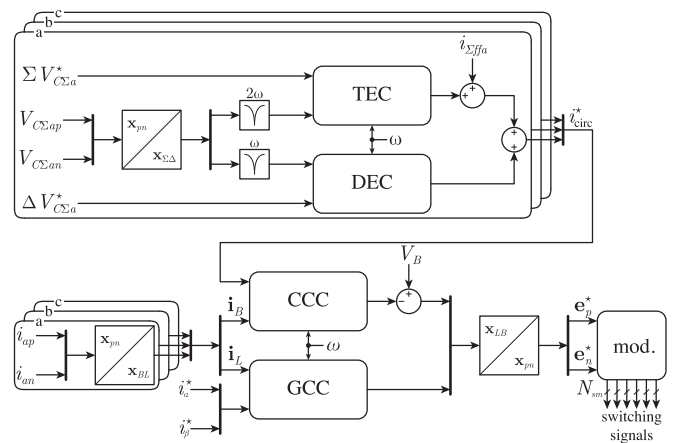

Fig. 8. Control structure adopted for the simulations assuming MMC connection to a stiff MVDC grid. The relevant control blocks are: total energy controller (TEC), differential energy controller (DEC), circulating current controller (CCC), and grid current controller (GCC).

D. MMC Waveforms in Closed-Loop

The relevant waveforms from the analytical model and from the closed-loop switched model are compared for various load angles and the two considered circulating current injection strategies in Fig. 9. Aside from both the branch current ripple and capacitor voltage spread that cannot be captured in the analytical model, they are in very good agreement. This also demonstrates the performance of the control algorithm: A perfectly DC circulating current [see Fig. 9(a) and (c)] or a DC with superimposed second harmonic circulating current [see Fig. 9(b) and (d)] are obtained in steady state.

V. LOSS TOOL

To compare the results, a common loss tool collects the waveforms of interest either from the VSM or the fully switched model. The input waveforms are sampled at 200 kHz. The waveforms of interest are as follows:

1) the voltage across both upper and lower IGBTs;
2) the current through the IGBTs and the diodes as well as the capacitor current;
3) the switching instants, which are mandatory in order to determine the switching losses (functional description presented in Fig. 10).

Details about the loss calculation are presented in the Appendix. Different semiconductor devices can be easily compared, as they are loaded from a database—though based on datasheet parameters. Multiple simulation sweeps for each device are not required, as device specific parameters are not required for the simulation. Proper scalings and interpolations are built into the loss tool, aiming to minimize the errors due to the limited number of sampled points provided for the switching loss energies. Additional calculated data provided as outputs are also indicated at the bottom of the loss tool.
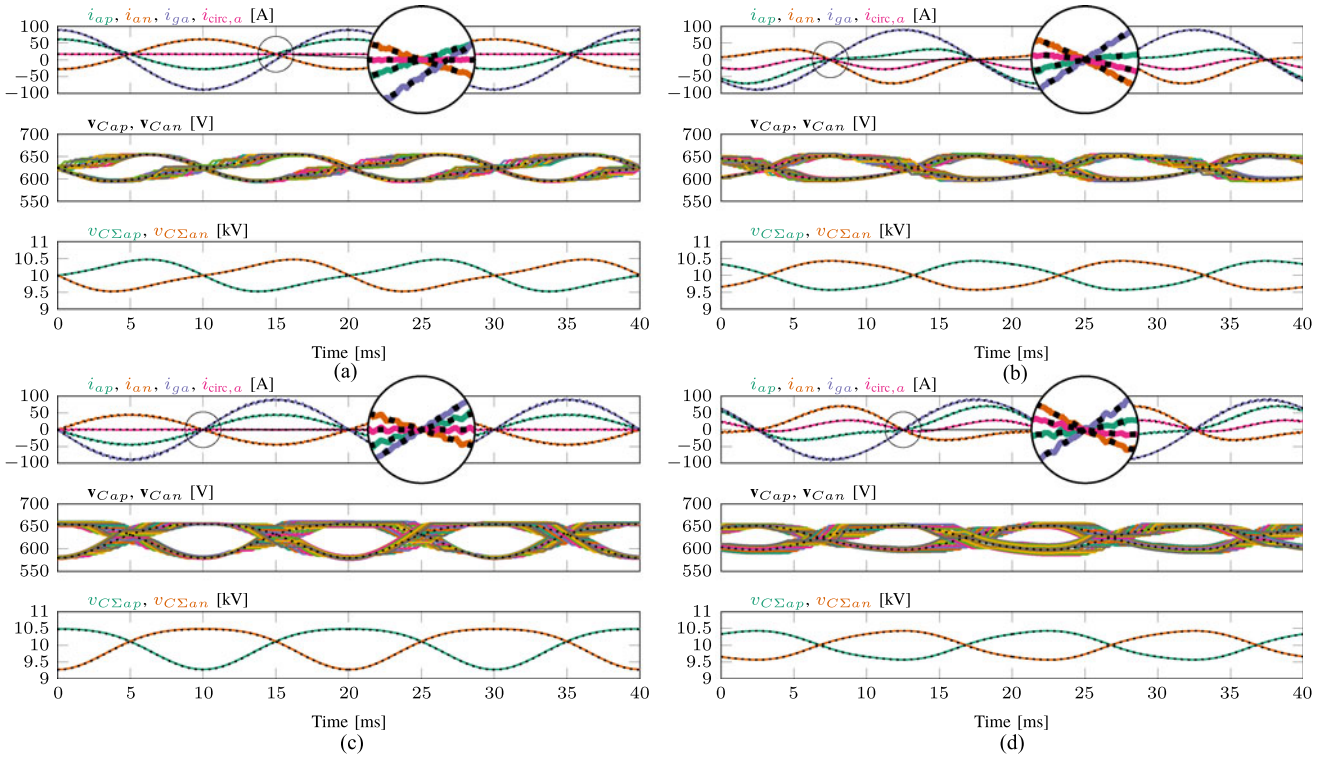
Fig. 9. Closed-loop responses (colored lines) versus analytical waveforms (dashed lines) in phase-leg a: (a) PD-PWM with DC circulating current for $\phi = 0$, (b) PD-PWM with DC plus second harmonic circulation current for $\phi = 3\pi/4$, (c) PS-PWM with DC circulating current for $\phi = \pi/2$, and (d) PS-PWM with DC plus second harmonic circulating current for $\phi = \pi/4$. The circles located at $t = 25\,\mathrm{ms}$ are magnifications of the thin black circles areas.
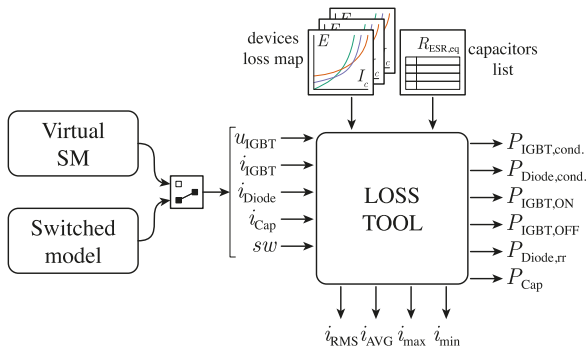

Fig. 10. Loss calculation tool diagram.

Fig. 11. Detailed semiconductor losses comparison for PS-PWM with DC circulating current and $\phi = 0$. SM1 to SM16 are the individual semiconductor losses from the switched model.

VI. VERIFICATION AND COMPARISON

To provide a complete analysis of the error between the VSM method and the loss values obtained from the detailed switched model, extensive simulations for different operating points are carried. The losses are computed in the positive branch of phase-leg a, but any of the other branches could have been selected. The waveforms are recorded over ten fundamental AC grid periods before the loss tool is invoked, in order to mitigate the *instantaneous* loss difference between the SMs. The average losses per SM are obtained from the VSM (representing a complete branch) by simple division by the number of SMs in a branch.
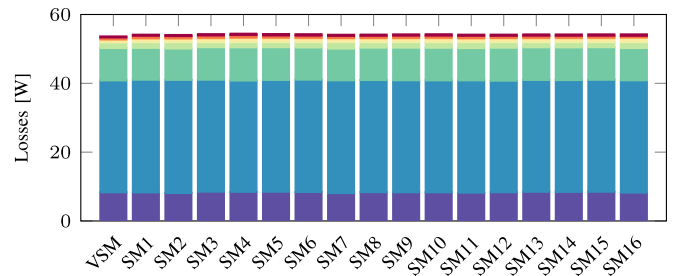
As it can be seen in Fig. 11, the semiconductor losses (the same stands for capacitor losses) are well balanced across all the SMs within a branch. Consequently, from now on only the mean value is considered. A subset of results, with one load angle per modulation method and circulating current harmonic content, is presented in Table II. As it can be seen, the semiconductor losses obtained using the VSM are in good agreement with each SM from the detailed switched model. The conduction losses are very accurately estimated by the VSM method, as based on the branch current RMS value, which is unaffected by the branch current ripple. The switching losses are less accurately estimated by the proposed method. The reason behind is that they depend on the instantaneous switched branch current and SM capacitor voltage. The accuracy dependency is inversely

TABLE II
DETAILED LOSS NUMBERS COMPARISON BETWEEN THE VSM CONCEPT
AND THE SWITCHED MODEL FOR ONE OPERATING POINT PER MODULATION
METHOD AND CIRCULATING CURRENT HARMONIC CONTENT

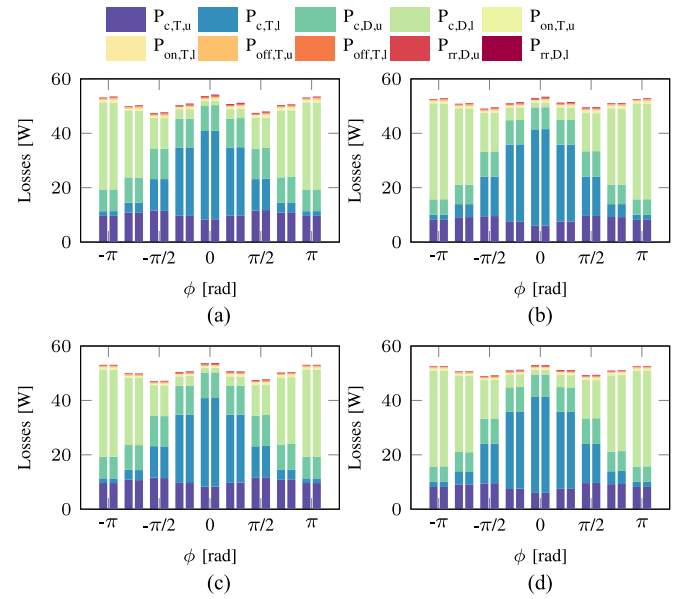| i_{circ}		DC		DC plus second	
Model		VSM	SW	VSM	SW
ϕ [rad]		0		$3\pi/4$	
PD-PWM	$P_{\text{c,T,u}}$	8.34	8.36	9.21	9.19
	$P_{\text{c,T,l}}$	32.50	32.58	4.73	4.77
	$P_{\text{c,D,u}}$	9.41	9.42	7.18	7.20
	$P_{\text{c,D,l}}$	1.64	1.64	28.06	27.89
	$P_{\text{on,T,u}}$	0.16	0.20	0.69	0.71
	$P_{\text{on,T,l}}$	0.63	0.87	0.26	0.32
	$P_{\text{off,T,u}}$	0.14	0.17	0.46	0.48
	$P_{\text{off,T,l}}$	0.50	0.58	0.15	0.19
	$P_{\text{rr,D,u}}$	0.07	0.08	0.24	0.25
	$P_{\text{rr,D,l}}$	0.23	0.31	0.11	0.13
	$P_{\text{tot,semi}}$	53.62	54.21	51.08	55.46
	P_{Cap}	26.03	26.13	26.12	25.98
ϕ [rad]		$\pi/2$		$\pi/4$	
PS-PWM	$P_{\text{c,T,u}}$	11.56	11.73	7.51	7.48
	$P_{\text{c,T,l}}$	11.57	11.55	28.30	28.29
	$P_{\text{c,D,u}}$	11.24	11.35	9.07	9.02
	$P_{\text{c,D,l}}$	11.26	11.12	4.55	4.48
	$P_{\text{on,T,u}}$	0.49	0.47	0.27	0.25
	$P_{\text{on,T,l}}$	0.49	0.47	0.66	0.64
	$P_{\text{off,T,u}}$	0.22	0.31	0.13	0.19
	$P_{\text{off,T,l}}$	0.22	0.33	0.35	0.40
	$P_{\text{rr,D,u}}$	0.19	0.19	0.12	0.10
	$P_{\text{rr,D,l}}$	0.19	0.18	0.23	0.22
	$P_{\text{tot,semi}}$	47.43	47.71	51.19	51.08
	P_{Cap}	36.03	36.59	26.11	25.99

All entries are in [W].

Fig. 12. Averaged semiconductor loss comparison between the VSM method (left side stacked bars) and the switched model (right side stacked bars): (a) PD-PWM with DC circulating current, (b) PD-PWM with DC plus second harmonic injection circulating current, (c) PS-PWM with DC circulating current, and (d) PS-PWM with DC plus second harmonic injection circulating current.
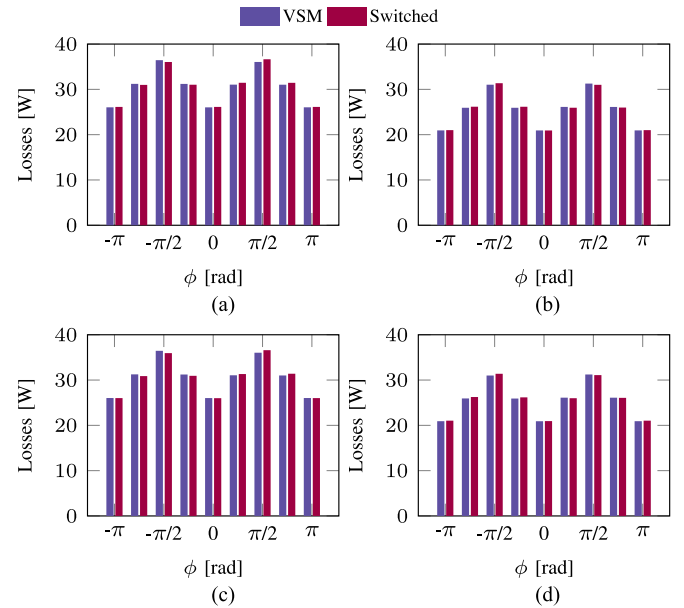

Fig. 13. Averaged SM capacitor bank losses comparison between the VSM concept (left side bars) and the switched model (right side bars): (a) PD-PWM with DC circulating current, (b) PD-PWM with DC plus second harmonic injection circulating current, (c) PS-PWM with DC circulating current, and (d) PS-PWM with DC plus second harmonic injection circulating current.

proportional to the apparent branch switching frequency. However, as the switching losses are few orders of magnitude smaller than the conduction losses, the overall semiconductor losses are in good agreement. The complete results, for each modulation method and circulating current injection strategy, are presented in Fig. 12. The left-hand side stacked bars correspond to the VSM method and the right-hand side stacked bars to the averaged semiconductor losses of the switched model. The split of different loss contributions in function of the load angle ϕ can be easily identified. At the same time, the loss split and the overall losses are almost identical to the results obtained from the VSM concept, demonstrating that the MOD block is able to correctly capture and compress the original switching patterns. Similarly, the averaged capacitor losses are presented in Fig. 13.

The relative errors plots on the total averaged semiconductor and capacitor losses are presented in Fig. 15 and are computed as

$$\varepsilon = \frac{x_{\text{switched}} - x_{\text{VSM}}}{x_{\text{VSM}}} \cdot 100. \tag{6}$$

Given the assumption required for the VSM concept, a very good accuracy is obtained, as the loss estimation error is below 2% for both semiconductor and capacitor losses. The source of this error comes from the branch current ripple and the SM capacitor voltage spread that are not captured by the VSM. These could be mitigated by an enhanced analytical description which

goes beyond the objectives of this work. It is important to state that the branch current ripple envelope is not simply dependent from the instantaneous branch modulation index, apparent switching frequency and branch inductance value. Similarly, the capacitor voltage spread is not linearly proportional to the
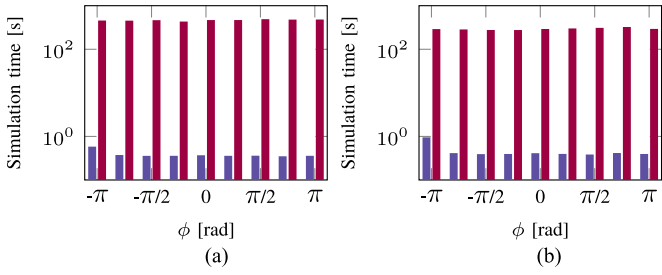
Fig. 14. Computational time benchmarking between the VSM method and the switched model: (a) PD-PWM with DC circulating current and (b) PS-PWM with DC circulating current. The time overhead for $\phi = -\pi$ corresponds to the loading time of the model in Simulink. The time overhead due to the sorting algorithm is clearly visible between PD-PWM and PS-PWM. Similar results are obtained for DC plus second harmonic injection circulating current.
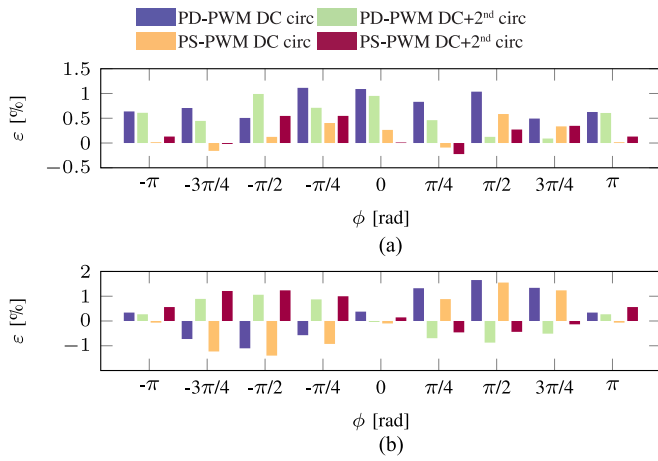
Fig. 15. Relative error plots for each modulation method and circulating current injection strategy: (a) semiconductor average losses and (b) capacitor average losses.

apparent branch switching frequency or average capacitor voltage ripple (as shown in Fig. 3). The proposed concept could be easily extended to include thermal considerations of the MMC design, however this is outside the scope of the presented work. The VSM allows for a very fast evaluation of the MMC SM's stresses, while considering directly the influence of the circulating current control strategy and impact of different modulation schemes. A benchmarking of the simulation times for obtaining the inputs of the loss tool (as the execution of the loss tool is negligible) between the VSM concept and a switched model has been performed on the same computer. The results are shown in Fig. 14.

VII. CONCLUSION

Starting from a set of relatively simple branch current and voltage equations, with deterministic circulating current injection strategy enabled by a circulating current controller, the averaged MMC converter waveforms were derived. Those waveforms were used as inputs for the semiconductor loss tool in combination with the proposed VSM concept. The proposed

concept was compared with switched models of the MMC under two PWM modulation schemes: 1) PD-PWM and 2) PS-PWM. A compression of a large number of switching pulses is required for the application of the VSM concept, which can be easily realized with a quantizer and one suitable carrier. It was shown that there is a good agreement between the predicted (analytically) and obtained (switched) converter waveforms in steady state, under the conditions of limited voltage spread among the capacitor voltages of the same branch and limited branch current ripple (compared to the branch current average value). With a higher apparent branch switching frequency, the impact of the assumptions associated with the VSM method is expected to be reduced. Moreover, the loss difference is within the usual safety margin that is taken for any industrial grade product during the design process. The speed gain is in the range of 600 between the semi-numerical and switched simulations. This significant gain is a real advantage for the VSM concept, as a complete converter loss map for any possible operating point can be obtained almost instantaneously. The necessity to run loss calculation in closed-loop operation is fully justified by the particular role of the circulating current in an MMC, and with the aid of the VSM concept, this problem is significantly simplified without any loss of information.

APPENDIX

To evaluate the losses, either from the PLECS switched model, or the VSM concept, relevant information is captured (e.g., turn-ON event, turn-OFF event, device voltage and current). The losses are split between conduction and switching losses (turn-ON, turn-OFF, and diode reverse recovery losses) and calculated using (7)–(11). As datasheet curves for the switching energies are used, the data points are interpolated for calculation— p^3 stands for piecewise cubic interpolation:

$$P_{\text{IGBT,cond.}} = i_{\text{IGBT,avg}}V_{CE} + i^2_{\text{IGBT,RMS}}R_{\text{IGBT,ON}} \tag{7}$$

$$P_{\text{Diode,cond.}} = i_{\text{Diode,avg}}V_F + i^2_{\text{Diode,RMS}}R_{\text{Diode,ON}} \tag{8}$$

$$P_{\text{IGBT,ON}} = \sum \frac{p^3(i_{\text{IGBT}}, E_{\text{IGBT,ON}}, i_{\text{IGBT,ON}})u_{\text{IGBT,ON}}}{V_{CS}T_{\text{window}}} \tag{9}$$

$$P_{\text{IGBT,OFF}} = \sum \frac{p^3(i_{\text{IGBT}}, E_{\text{IGBT,OFF}}, i_{\text{IGBT,OFF}})u_{\text{IGBT,OFF}}}{V_{CS}T_{\text{window}}} \tag{10}$$

$$P_{\text{Diode,rr}} = \sum \frac{p^3(i_{\text{IGBT}}, E_{\text{IGBT,rr}}, i_{\text{IGBT,ON}})u_{\text{IGBT,ON}}}{V_{CS}T_{\text{window}}} \tag{11}$$

where T_{window} is the window of time over which the losses are computed.

The 1.9 mF capacitor bank is realized with six 400 V electrolytic capacitors. Only ohmic losses from equivalent series resistance (ESR) are considered and used for the capacitor loss calculation in the loss tool

$$P_{\text{cap}} = R_{\text{ESR},eq}i^2_{\text{Cap}}. \tag{12}$$

REFERENCES

[1] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

[2] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 57–68, Jan. 2012.

[3] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares stromrichterkonzept für netzkupplungsanwendungen bei hohen spannungen," in *Proc. ETG-Fachtagung*, 2002, pp. 1–7.

[4] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[5] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier pwm," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 268–283, Jan. 2015.

[6] E. Coulinge, A. Christe, and D. Dujic, "Electro-thermal design of a modular multilevel converter prototype," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, May 2016, pp. 1–8.

[7] A. Christe, E. Coulinge, and D. Dujic, "Insulation coordination for a modular multilevel converter prototype," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, 2016, pp. 1–9.

[8] A. Christe and D. Dujic, "Galvanically isolated modular converter," *IET Power Electron.*, vol. 9, no. 12, pp. 2318–2328, 2016.

[9] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, Aug. 2010.

[10] J. Freytes, F. Gruson, P. Delarue, F. Colas, and X. Guillaud, "Losses estimation method by simulation for the modular multilevel converter," in *Proc. IEEE Elect. Power Energy Conf.*, Oct. 2015, pp. 332–338.

[11] S. Rodrigues, A. Papadopoulos, E. Kontos, T. Todorcevic, and P. Bauer, "Steady-state loss model of half-bridge modular multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2415–2425, May 2016.

[12] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4568–4579, Sep. 2014.

[13] M. Winkelnkemper, A. Korn, and P. Steimer, "A modular direct converter for transformerless rail interties," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 2010, pp. 562–567.

[14] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[15] A. Lopez, D. E. Quevedo, R. Aguilera, T. Geyer, and N. Oikonomou, "Reference design for predictive control of modular multilevel converters," in *Proc. 4th Aust. Control Conf.*, Nov. 2014, pp. 239–244.

[16] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[17] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[18] N. Cherix, "Functional description and control design of modular multilevel converters: Towards energy storage applications for traction networks," Ph.D. thesis dissertation, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 2015.

[19] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Jan. 2015.
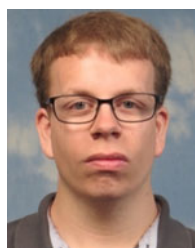
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