Optical device suggestion

SPDC based single-photon source with frequency up-conversion multiplexed architecture

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Abstract

We describe a single-photon source based on an array of spontaneous parametric down-conversion (SPDC) modules multiplexed by an integrated structure composed of electro-optic switches and delay wave-guides.

The suggested optical device allows to increase the photon source frequency compared to the SPDC laser pumping frequency and enhances both stability, controllability, and efficiency.

This device transforms the spatial multiplexing into a temporal multiplexing with temporary photon storage. The photons are stored into different delay lines and temporally sequentialized. This train of photon can then be used in high frequency emission and compensation of photon lack among the pumping cycles.

The implementation consists of a **crossed multiplexed architecture using electro-optic switches**. The architecture first drives the downconverters array outputs into several layers of **delay lines** organized in **shared and by-passable binary delay register**. The architecture then includes a **routing tree** driving all the photons into a single output.

Background

Most of SPDC based sources work with a temporal or a spatial multiplexing, thus have the same frequency as pumping or a (low) divisor. In both isolated case, the multiplexing cannot control more than one photon and the Poissonian statistics of SPDC leads to a waste of photons or a stronger multi-photon rate. Some SPDC based sources also try to use photon storage into different kinds of loops without meeting great success.

We aimed at creating a high efficiency device, eliminating the waste of photons and the stability problems due to probabilistic behavior of spontaneous downconversion. We also wanted a different way of thinking. The tools are known, the direction is different, but the result is there, and better. It takes a logical and optimistic look toward advanced research on quantum computer.

The main advantages of the frequency up-conversion toward the pumping rate is the reduction of length of the integrated optics and the possibility to overtake heralding detector problems. While progress of integrated MZI interferometers, integrated wave-guides or photonic crystals is prompt, single-photon detector technology, number-resolving or non-number-resolving, is still far from the same level of development.

This suggested device offers the possibility to build an advanced integrated optical device, moreover functional element of a future quantum computer, whose design gives the most of its flexibility to its detectors and the most of its potential to its optical control.

General scheme

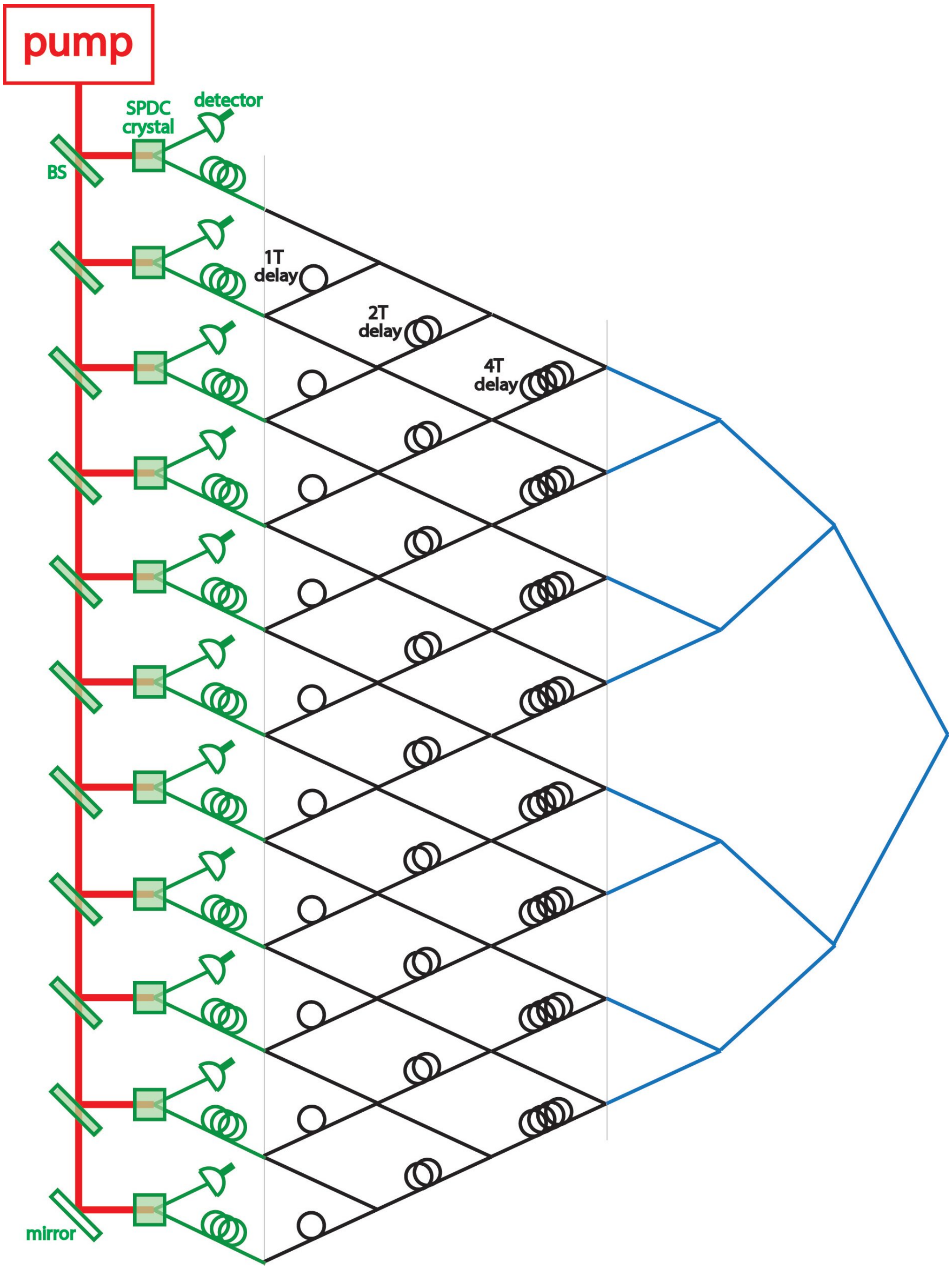

Figure 1: General scheme of a single-photon source with 11 SPDC crystals and $0T$ to $7T$ delay register. (red) Pumping laser. (green) Downconverters (pair generator, heralding detector and heralding decision delay). (black) Crossed by-passable delay register. (blue) Routing tree.

Detailed description of elements

Downconverters

The pump laser illuminates a array of $\chi^{(2)}$ non-linear crystals, creating both idler and signal photons. The idler photons are sent to heralding detectors connected to a processor unit (FPGA). The signal photons are sent into the integrated architecture through delay fibers to let time for the processor unit to take path decisions.

The delay fibers have slightly different lengths to correct the entering time differences among emitted photons due to the growing distance between the pump and each crystal of the array.

The number of SPDC modules can be chosen and optimized for the symmetry of the linear then logarithmic routing into the single output. In the hypothesis of a photon driving demonstration, single-photon or multi-photon are driven in the same way through standard MZI switches. Thus, a small number of downconverters (below twenty) can be chosen with an exaggerated photon rate. For a demonstration of efficient single-photon source, number of downconverters must be higher (from a few tens to more than hundred).

Crossed by-passable binary delay register

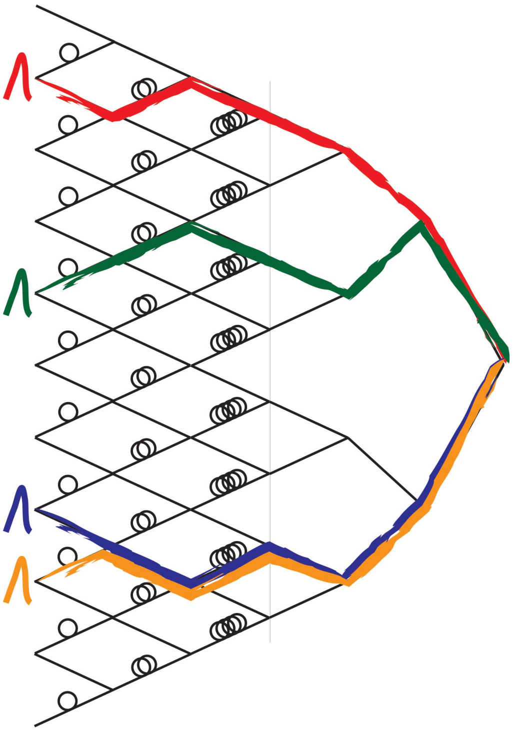

Figure 2: 0-7T delay register paths. Delays: red: $2T$, green: $3T$, blue: $4T$, yellow: $5T$.

The crossed by-passable delay register (CBDR) structure is the heart of the invention. It distributes the photons in a train of period T. The CBDR can achieve photon delays between $0T$ to $2^N - 1T$ with N number of delay steps. Thus, a 3-step register can delay photons from 0 to $7T$ (Fig. 2).

In a given architecture, due to the asymmetry of the structure, control of boundary photons is more or less limited as shown on Table 1. It is not an important problem if we choose good actuation rules (see *fast-to-slow top-to-down driving* in the next sections) or if we simply remove one or two boundary downconverters.

SPDC N°	Inaccessible states	SPDC N°	Inaccessible states
1	1T, 2T, 3T, 4T, 5T, 6T, 7T	N-2	0T
2	3T, 5T, 6T, 7T	N-1	0T, 1T, 2T, 4T
3	7T	N	0T, 1T, 2T, 3T, 4T, 5T, 6T

Table 1: Limitation of control of boundary downconverters for a 0-7T register structure

Routing tree

This structure simply drives the different delayed photons into a single output. The amount of switches increases in a logarithmic scale of the number of delayed single-photon inputs. It also allows to drive out of the structure the possible excess of photons.

Due to the low single-photon generation probability per downconverter (usually lower than 10%), part of the tree may be placed before or in between the steps of the crossed binary delay register or in between. In this case, a more complex driving of photons needs to be established to avoid photon bunching (but more opportunities to drive out concurrent or excess) or to consider it (using MZI switches in different configurations) (Fig. 3).

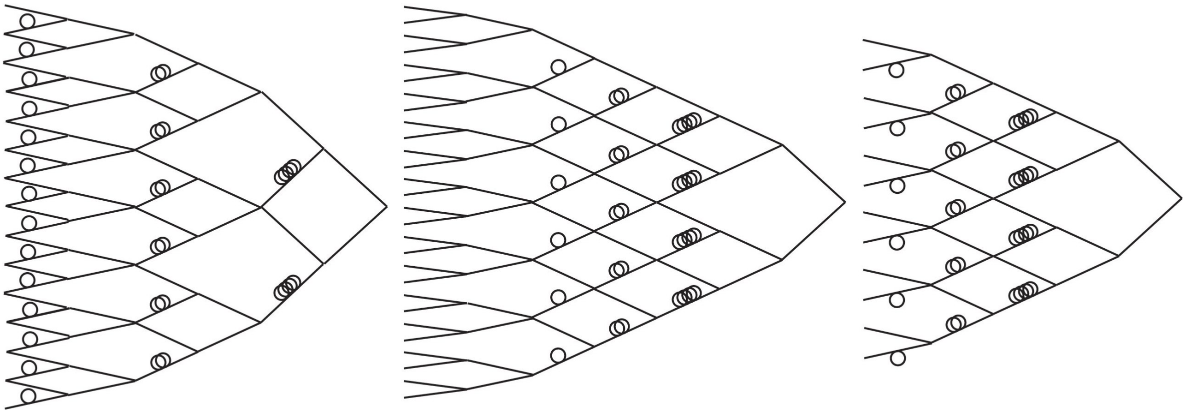

Figure 3: Alternative structures. (left) Routing in between delaying. (center) Routing before and after delaying. (right) Reducing of one layer of switches, parity trade-off.

Detailed functioning

Frequency up-conversion

The CBDR structure and routing tree build a T-periodic photon train at each pumping pulse on the downconverter array. The rate of downconverter and the number of downconverters is matched in order to obtain enough photons to emit a train of several photons at the frequency of the pumping. The photon source frequency is thus a multiple of the pump frequency. With a 0-$7T$ by-passable binary delay register, the longest photon train is 8. In this example, the maximal frequency multiplication is 8.

The maximal photon source frequency is fixed by the CBDR implementation to the first delay step T. The device frequency can be divided by skipping register steps and drive some photons out of the routing tree.

By trade-off on stability or multi-photon emission rate, the pumping period can be changed and lowered by several T, the frequency multiplication is thus lower.

Stability enhancement

Multiplying frequency needs a constant number of photons per pump pulse. Probabilistically, it needs in average much more photons than the frequency multiple. It is achievable by increasing again the downconverter number or pump power, but will lead to multi-photon emissions and large waste of photons.

Keeping the source frequency below the maximum frequency multiple make possible a *temporary photon storage* of the excess photons into the longest delay lines. Photons can be delayed up to the next pump cycle and so will be emitted in the first place in this new pumping period. A little photon excess can be used during the next pulse, and a small lack can be corrected by the storage from the previous pulse (Fig. 4). This 1-cycle ahead memory allows to reduce the SPDC array average rate almost down to the frequency conversion multiple.

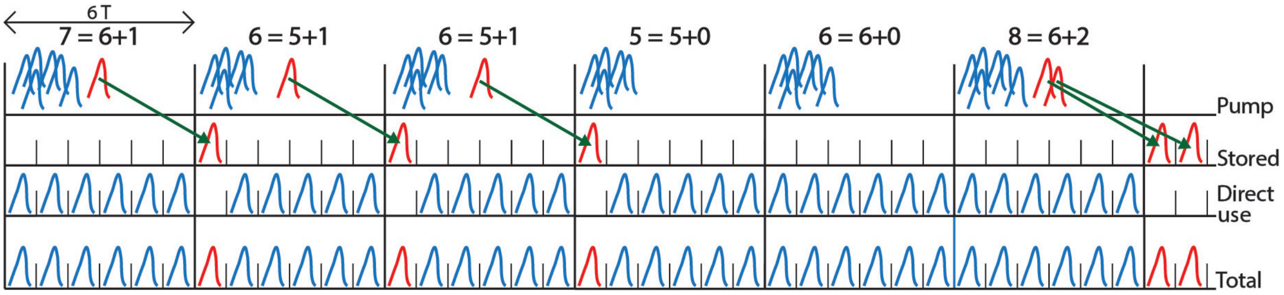

Figure 4: Photon source frequency 6 times higher than pump rate. 1 or 2 photon excess (red) is stored and used at the beginning of the next cycle before the newly produced photons.

With the 0-$7T$ register example and by lowering the frequency multiplication to 6, two photons can be stored for the next pulse cycle. 1 or 2-photon excess can be used during the next pulse, and 1 or 2-photon lack can be corrected by the storage from the previous pulse (Fig. 4). In these conditions, probability of lack of photon at the output drops significantly, since it only occurs when several successive low photon numbers are issued from the downconverter array.

The size of the downconverter array will be a factor of stability in addition to increase the total photon rate. Stability can once more be improved easily by adding a feedback to increase the pumping power for the next cycle to refill the temporary photon storage.

Switching decisions

The best strategy to operate the suggested device and avoid CBDR limitation problems or photon bunching problems is to adopt a *fast-to-slow top-to-down* driving approach. It consists in allocating fastest photons (low delays) to slowest photons (high delays) from the top to the bottom of the CBDR structure.

In this operating mode, we reduce the need of inaccessible paths due to CBDR limitations and avoid any bunching of photons. Photons may share the same path, but at different times (Fig. 2).

With this approach, during a pumping cycle, each switch of the CBDR structure and the routing tree needs to be permuted *at most once* and all in the same direction (figure out the permutations in the CBDR and in the routing tree switches needed to drive the photon train out on Fig. 2). The use of photon storage for stability enhancement slightly changes this property by delaying some permutations to the next pump cycle.

Advantages to prior art

- Frequency up-conversion of the laser pumpimg rate to the photon source output
- Tolerate low detector speed
- High stability of the output photon rate
- Possibility of feedback on the next cycle due to the efficient photon storage
- High controllability at fixed source frequency (pump power, pump frequency, power or frequency feedback on next pump pulse)
- High control of the trade-off between frequency rise/multi-photon rate/output stability
- Few waste of photon
- Efficient use of multiplexing and customizable structure (SPDC number and CBDR level)
- Easy up-to-down switching programming