Silicon-rich silicon-carbide hole-selective rear contacts for crystalline silicon based solar cells

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ABSTRACT

The use of passivating contacts compatible with typical homo-juntion thermal processes is one of the most promising approaches to realize high efficiency silicon solar cells. In this work, we investigate an alternative rear passivating contact targeting facile implementation to industrial *p*-type solar cells. The contact structure consists of a chemically grown thin silicon oxide layer,

which is capped with a boron-doped silicon-rich silicon-carbide ($SiC_x(p)$) layer and then annealed at 800°C–900°C. Transmission electron microscopy reveals that the thin chemical oxide layer disappears upon thermal annealing up to 900°C, leading to degraded surface passivation. We interpret this in terms of a chemical reaction between carbon atoms in the $SiC_x(p)$ layer and the adjacent chemical oxide layer. To prevent this reaction, an intrinsic silicon inter-layer was introduced between the chemical oxide and the $SiC_x(p)$ layer. We show that this intrinsic silicon inter-layer is beneficial for surface passivation. Optimized passivation is obtained with a 10-nm-thick intrinsic silicon inter-layer, yielding an emitter saturation current density of 17 fA cm^{-2} on *p*-type wafers, which translates into an implied open-circuit voltage of 708 mV. The potential of the developed contact at the rear side is further investigated by realizing a proof-of-concept hybrid solar cell, featuring a heterojunction front side contact made of intrinsic amorphous silicon and phosphorus-doped amorphous silicon. Even though the presented cells are limited by front side reflection and front side parasitic absorption, the obtained cell with a V_{oc} of 694.7 mV, a *FF* of 79.1% and an efficiency of 20.44% demonstrates the potential of the p^+/p-wafer full side passivated rear-side scheme shown here.

1. Introduction

State-of the art commercial homo-junction c-Si solar cells are limited by voltage losses due to recombination of charge carriers at the direct metal-semiconductor interfaces. Partial rear contacts (PRC) are currently being implemented by the industry to limit contact recombination by restricting the contact area. However, as a reduced contact area fraction also leads to increased series resistance, PRC cells are inherently limited by a trade-off between minimized recombination and series resistance.[1-2] In addition, the realization of partial rear contacts requires an additional

patterning step, which increases the process complexity. An alternative way to mediate contact recombination is the concept of "passivating contacts" that consists of a thin buffer layer for surface passivation, capped with an additional layer which selectively collects one type of charge carrier. A prime example of passivating contacts are silicon heterojunctions (SHJ), in which surface passivation is provided by intrinsic amorphous silicon (a-Si:H) and carrier selectivity by doped a-Si:H. Recently, Kaneka-Japan reported a record efficiency of 26.33% for a c-Si solar cell using an interdigitated back contacted (IBC) SHJ design.[3] Nevertheless, since the electronic quality of a-Si:H deteriorates at temperatures above 250°C, SHJ solar cells are incompatible with industrial firing through metallization schemes as these include processing at temperatures up to 800°C. For enhanced temperature stability and compatibility with standard solar cell manufacturing processes based on diffusion and firing, a promising approach consists in using silicon oxide as a thin buffer layer capped with doped poly-silicon, semi-insulating poly-silicon (SIPOS) or doped Si-based mixed-phase layers,[4-8] which are thermally annealed to diffuse dopants into the c-Si wafer. Recently, a remarkable efficiency of 25.1% was demonstrated using a similar approach as a rear *n*-contact in an *n*-type solar cell with a boron diffused front side.[9] The contact structure consists of a chemically[10] or photo-chemically[11] grown ultra-thin SiO_x buffer layer capped with a phosphorus-doped amorphous silicon (a-Si:H(*n*))[8, 12] layer deposited by plasma enhanced chemical vapour deposition (PECVD). After an hydrogenation step to passivate electronic defects, this contact structure yields an emitter saturation current density (J_0) of 7 fA cm^{-2} and a contact resistance of below 5 mΩ cm^2.[13] Analogous structures were used for hole-selective contacts using boron-doped amorphous silicon (a-Si:H(*p*)), resulting however in slightly lower performance compared to electron-selective contacts. Their lower performance is commonly explained by the high surface recombination velocity occuring at boron-diffused surfaces that are

passivated with SiO_x[14] and additional defect-creation by boron diffusion through the SiO_x buffer layer.[15] For in-situ doped layers deposited by PECVD, J_0 values of around 50 fA cm^{-2} and implied open circuit voltages (iV_{oc}) of 680 mV were obtained.[16] Using ion implantation techniques, slightly better results with J_0 of 22 fA cm^{-2} and iV_{oc} of 696 mV have been demonstrated.[17-18] Peibst et al. showed impressively low J_0 values down to 8 fA cm^{-2} with p-type poly-Si deposited by PECVD technique on thermally grown buffer oxide.[19] Also, Nemeth et al. reported an iV_{oc} of 700 mV with hole selective contact as high-low junction using a thermal SiO_x as a thin buffer oxide.[20] Yan et al. demonstrated an approach to form *p*-type passivating contacts based on PECVD of undoped a-Si followed by thermal diffusion of boron from a BBr_3 and attained the J_0 values of 16 fA cm^{-2}.[21] An additional practical complication of hole-selective contacts is the blistering of the a-Si:H(*p*) layer, which poses severe processing restrictions to the deposition and thermal annealing processes.[20, 22] For lean process integration, single-side deposition and in-situ doping are desired. Also a passivating hole contact should ideally be co-annealed using the thermal process of phosphoryl chloride ($POCl_3$) diffusion or the contact firing.

In this study, an alternative full area rear passivating contact fabricated by PECVD and thermal annealing is investigated with targeting a facile implementation to industrial *p*-type solar cells. The contact consists of a triple layer stack comprising a chemically grown SiO_x, an intrinsic silicon (Si(*i*)) inter-layer, and a boron-doped silicon-rich silicon-carbide (SiC_x(*p*)) layer. The choice of SiC_x is motivated by several advantages: the material is more resilient to blistering than a-Si:H when deposited on chemical SiO_x, as C-H bonds are more stable than Si-H bonds with respect to hydrogen effusion.[23-24] Moreover, as SiC_x is stable in standard wet chemical solutions used in Si solar cell fabrication, the rear contact can also serve as rear side protection through the entire cell process, providing large flexibility for the latter. The structural transformations of the passivating

contact during the annealing step is discussed along with the influence of the intrinsic Si inter-layer in between chemical SiO_x and $SiC_x(p)$. Finally, a proof-of-concept hybrid solar cell, which features a developed passivated back contact and an heterojunction front side contact made of intrinsic a-Si:H and phosphorus-doped a-Si:H(*n*), is presented.

2. Experimental

Passivating hole contacts were investigated using symmetrical structures based on either 280 µm thick double side polished 4-inch *p*-type float-zone <100> c-Si wafers with a resistivity of 2.8 Ωcm or 250 µm thick chemically polished 4-inch *p*-type float-zone <100> c-Si wafers with a resistivity of 2 Ωcm. After standard wet chemical cleaning, an ~1 nm SiO_x layer was formed by wet chemical oxidation using HNO_3 solution at 80°C[10, 25], referred to as "chemical SiO_x". Subsequently, $SiC_x(p)$—amorphous *as deposited* state— was deposited on both sides by PECVD operated at 40.86 MHz with silane (SiH_4), hydrogen (H_2), trimethylboron (TMB) and methane (CH_4) as process gases. The typical substrate temperature and power density were kept constant at 200°C and 0.06 W cm^{-2}, respectively, during the deposition. The samples were then annealed for 5 minutes in an inert gas atmosphere at a temperature of 800°C. This was followed by a hydrogenation step to passivate electronic defects at the c-Si wafer / chemical SiO_x interface using SiN_x as a hydrogen donor layer. The surface passivation properties were investigated by photo-conductance decay (PCD) technique, giving access to the effective minority-carrier lifetime as a function of the excess minority carrier density and the resulting implied open circuit voltage (iV_{oc}) values. The method of Kane and Swanson[26] was applied to extract the emitter saturation current density (J_0) at an excess carrier density of 5×10^{15} cm^{-3}. The spatial homogeneity of the passivation was analyzed using photoluminescence imaging (PLI). The transfer length measurement (TLM) technique with linear contact pads array[27] was applied to extract the contact

resistivity on *p*- type wafer. The structural changes occurring upon annealing at 800°C and 900°C were characterized using transmission electron microscopy (TEM) performed in either an FEI Titan Themis or an FEI Tecnai Osiris, both operated at 200 kV. In addition to the acquisition of high-resolution (HR)TEM micrographs, scanning TEM (STEM) images were recorded using a high-angle annular dark field (HAADF) detector and were combined with energy-dispersive X-ray spectroscopy (EDX) to obtain a chemical assessment of the layers of interest. For this purpose, TEM lamellae were prepared from samples after deposition and annealing at 800°C and 900°C, respectively, using the conventional focused ion beam (FIB) lift-out technique in a Zeiss Nvision 40 workstation. The crystallinity of the contact layers after annealing was analyzed by grazing incidence X-ray diffraction spectroscopy (GI-XRD) using a Bruker D8 Discover Tool with the Cu-Kα (λ=1.542 Å) radiation source at a fixed incidence angle of 0.3°.

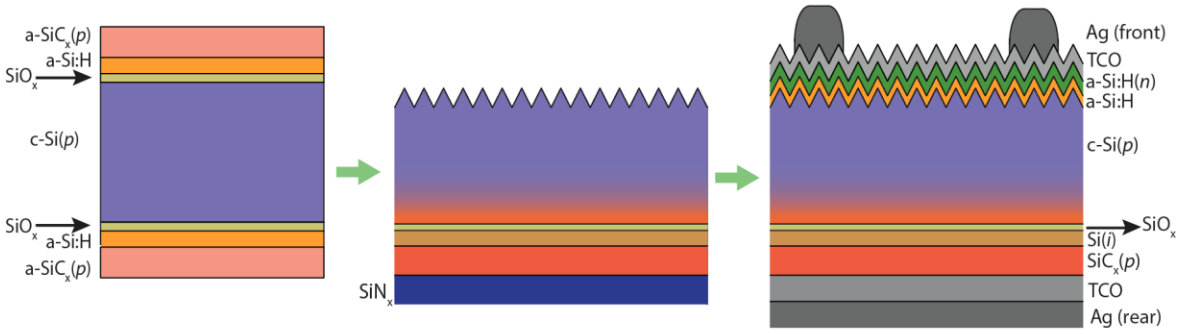

Figure 1. Process flow and final device structure. The p^+ region at the rear side of the c-Si(*p*) wafer created by in-diffusion of boron from the a-SiC$_x$(*p*) layer and the structural change of the deposited layers upon annealing at high temperatures (≥ 800°C) are indicated in the sketch by change in the colors.

After the analysis of the symmetric lifetime samples, they were further processed to realize as solar cells. The rear side of the wafer was protected, while the layer stack on the front side was etched and textured in potassium hydroxide solution. After removal of the rear protection layer, the wafers

were cleaned in standard wet chemistry and finally dipped in 5% diluted HF to remove the native oxide. Subsequently, a 7 nm intrinsic a-Si:H passivation layer and a 6 nm phosphorus-doped a-Si:H(*n*) electron collection layer were prepared by PECVD on the front side. To extract the collected carriers efficiently and to increase the light in-coupling into the wafer, 70 nm and 200 nm indium tin oxide (ITO) were sputtered onto the front and rear sides of the cells, respectively. The active cell area was defined by depositing the ITO layers through a 2.2 cm × 2.2 cm shadow mask. A silver reflector / contact was sputtered onto the rear side and silver paste was screen-printed to realize the front metallization grid, followed by curing for 25 minutes at 190°C in a belt furnace. The process flow and final device structure are depicted in Figure 1. Current-voltage (*I-V*) characteristics of the cells were measured at 25°C with a source-meter (Keithley, 2601A), using an AAA solar simulator (Wacom) calibrated to 100 mW cm^{-2} with a c-Si reference cell. Furthermore, the cells were measured by suns–V_{oc} to obtain the series-resistance-free pseudo *I–V* curves. The external quantum efficiency (EQE) and reflectance (R) were measured using the Loana (pv-tools) tool and the internal quantum efficiency (IQE) calculated according to IQE = EQE / (1-R).

3. Results and discussion

3.1 . Structural Properties

The structure of the hole selective contact and its evolution during thermal annealing was investigated by TEM. STEM HAADF images together with corresponding EDX maps and line scans are shown in Figure 2 for the contact structure in *as deposited* state and after annealing for 5 minutes at 800°C and 900°C. The EDX data confirms that the thin dark line observed at the c-Si wafer interface in the STEM HAADF images shown in Figure 2(a)-(b) corresponds to the chemical

SiO_x. In the *as deposited* state, depicted in Figure 2(a), a clearly defined, sharp interface is observed between the c-Si wafer and the chemical SiO_x. After annealing at 800°C, contact structure preserves the sharp interface [see Figure 2(b)]. After annealing at 900°C as shown in Figure 2(c), however, the chemical SiO_x layer at the Si wafer interface is not present any more. C appears to be incorporated into the a recrystallized Si layer that presents epitaxial re-growth with the c-Si wafer [see Figure 3(a)]. The HRTEM micrograph and corresponding Fourier transform also highlight the presence of stacking faults along the (111) crystalographic planes (seen as streaks in the reciprocal space transform). These stacking faults are likely induced by thermal stressing[28-29] due to the presence of C in the Si lattice. In addition to c-Si reflections, a reflection at 4 nm^{-1}, which corresponds to the (111) planes of cubic (beta-) SiC, is also measured in the Fourier transform [see Figure 3(a)].

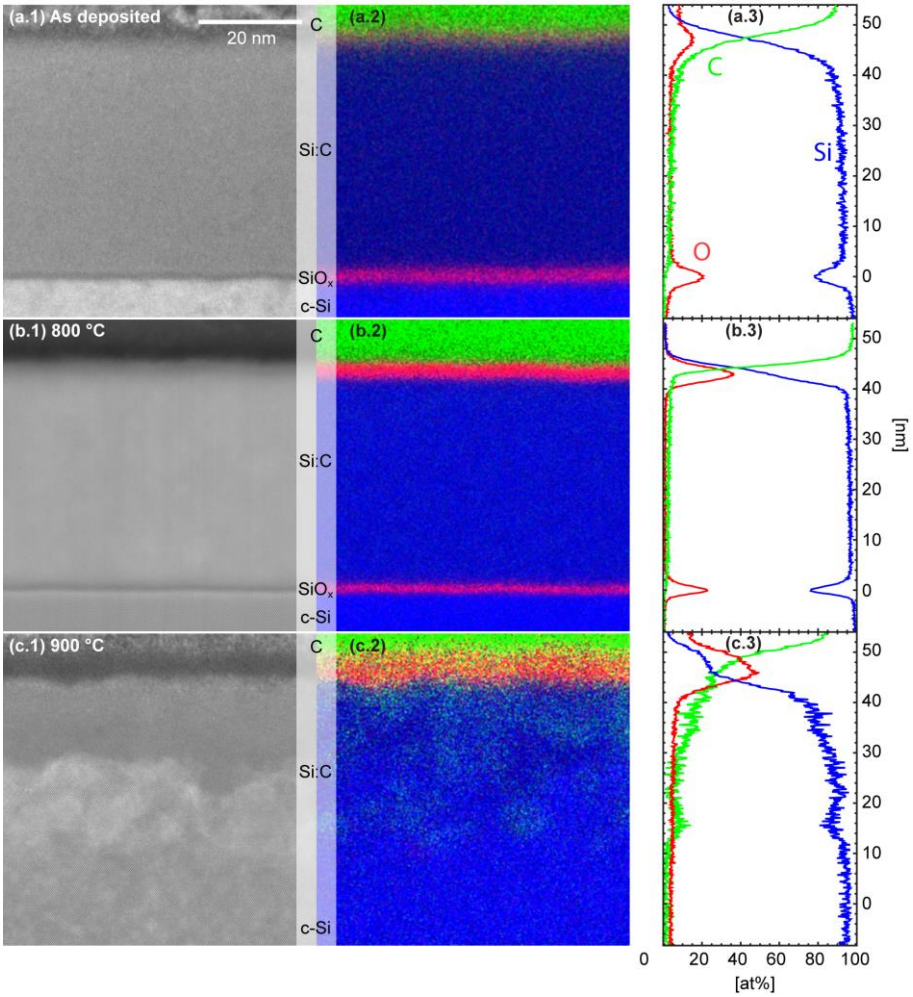

Figure 2. STEM-HAADF micrographs (left), corresponding EDX maps (middle), and EDX line scans (right, quantified using the Cliff-Lorimer methods[30]) of the c-Si wafer / SiO_x / a-SiC_x(*p*) contact structure. (a) As-deposited, and after thermal annealing for 5 minutes at (b) 800°C and (c) 900°C.

Furthermore, the crystallinity of the structures was investigated by GI-XRD technique. Figure 3(b) shows the diffraction patterns of the samples annealed at 800°C and 900°C. The peaks appearing at diffraction angles of 28.4°, 47.4°, 56.3° are attributed to the (111), (220) and (311) reflections of Si crystals. The expected reflections of cubic SiC at 35.4°, 60.0°, 71.8°, which correspond to the (111), (220) and (311) planes, respectively, are also indicated in Figure 3(b). The full-width-half-maxima of the Si-related peaks (excluding the (111) peak arises mainly from the wafer) are narrower for the sample annealed at 900°C, which is the signature of a larger mean

crystallite size.[31] Additionally, after annealing at 900°C a peak at 35.4°, which corresponds to the (111) reflection from cubic SiC, becomes visible, confirming SiC crystallization observed by TEM [c.f. Figure 3(a)]. The results are in agreement with previous studies, which also reported a degraded surface passivation after annealing at temperatures above 875°C due to a local break-up of the SiO_x buffer layer with epitaxial re-growth of the deposited Si layer.[32] However, to the best of our knowledge, there is no report showing the complete disappearance of the SiO_x layer. Chemical bonding in a-SiC_x layers prepared by PECVD technique strongly depends on the deposition parameters and related plasma regime.[23, 33] Especially in the low power regime identified by Solomon *et al*.,[34] the decomposition probability of CH_4 is much lower than that of SiH_4[35-36] and CH_4 is dissociated only by the reaction of the CH_4 molecules with the species created by the decomposed SiH_4. Since there is no primary decomposition of CH_4, carbon (C) atoms are incorporated in the layer mostly as CH_3 groups. As these establish only one bond to the a-Si network, they are only poorly incorporated in the latter. Upon heating, hydrogen effuses from the amorphous network at temperatures far below 800°C,[33] leaving "dehydrogenated" C atoms that are only bond to one Si atom. Overall, it suggests that the SiO_x layer reacts with the loosely bond C according to at least one of the reactions $zC + xSiO_2 \rightarrow xSi + yCO$ or $3C + SiO_2 \rightarrow SiC + 2CO$,[37] and the oxygen effuses in gaseous form as CO or CO_2. While the reported reaction temperatures are higher than the annealing temperature employed here, it should be noted that the C source is in immediate contact with the chemical SiO_x layer and the total O quantity rather low. Upon thermal annealing of a-SiC_x layers, SiC crystallites are usually observed as soon as Si crystallites are detected despite the higher crystallization energy of SiC. This effect is explained by the heterogeneous nucleation of SiC at the Si crystals lowering the activation energy for crystalline growth.[38] While O effuses as CO from the layer, the remaining C forms SiC, partially

grown as crystallites on or into the c-Si wafer surface epitaxially. The chemical SiO_x layer is still visible in the TEM images after annealing at 800°C. However as the chemical SiO_x layer vanishes after annealing at 900°C for 5 minutes, we speculate that also after annealing at 800°C for 5 minutes, the chemical SiO_x layer has likely already been weakened by reaction with C since the symmetrical lifetime sample employing this contact structure attains only an iV_{oc} of 685 mV.

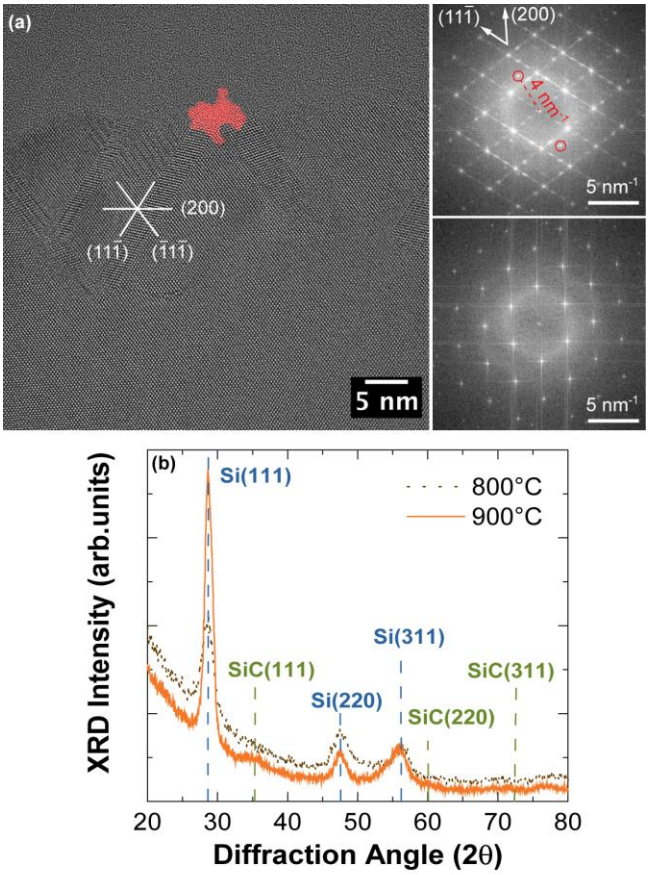

Figure 3. (a) HRTEM image of the sample annealed at 900°C together with Fourier transforms computed from the recrystallized SiC_x region containing stacking faults (top right) and at the position of the c-Si wafer (bottom right) (b) GI-XRD diffractograms after annealing at 800°C and 900°C. The dashed lines indicate the positions of the Si (111), (220) and (311) reflections at 28.4°, 47.4° and 56.3° and of the cubic SiC (111), (220) and (311) reflections at diffraction angles of 35.4°, 60.0°, 71.8°.

As structural defects act as recombination centers, an untainted interface between the chemical SiO_x and c-Si wafer is indispensable for good surface passivation. To mitigate the mentioned

chemical reaction of the chemical SiO_x with the C from the deposited $SiC_x(p)$ layer, we introduce an additional intrinsic Si inter-layer in between the chemical SiO_x and the a-$SiC_x(p)$ layer during the deposition. Figure 4 shows the iV_{oc} and J_0 values for the contact structures that have different inter-layer thicknesses after annealing at 800°C with a dwell time of 5 minutes. It is observed that the intrinsic Si inter-layer boosts the iV_{oc} from 685 mV up to 708 mV and lowers the J_0 down to 17 fA cm^{-2} for the sample with a 10 nm thick inter-layer. Based on the diffusivity of C in Si,[39] we assume that for very thin intrinsic Si inter-layer, C atoms can still reach the chemical SiO_x, which might explain the lower performance of the samples with 2-nm and 4-nm-thick intrinsic Si inter-layer. As the intrinsic Si inter-layer thickness increases further from 10 nm to 15 nm, the iV_{oc} shows a drastic decay to 670 mV. We tentatively explain this with a reduced dopant diffusion from the $SiC_x(p)$ layer to the c-Si wafer, which weakens the field effect passivation. Corresponding J_0 values show an agreement with the iV_{oc} values and decrease with increasing intrinsic Si inter-layer thickness.

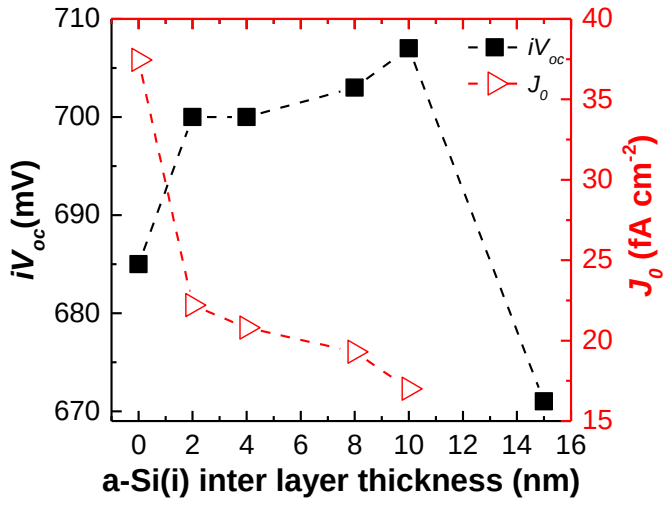

Figure 4. The impact of the intrinsic Si inter-layer thicknesses on implied open circuit voltage (iV_{oc}) and emitter saturation current density (J_0) of the contact structure after annealing at 800°C for 5 minutes and subsequently hydrogenating with SiN_x.

The microstructure of a sample with 10 nm-thick intrinsic Si inter-layer after annealing at 800°C is shown in Figure 5. The HAADF image shows a sharp and well preserved c-Si / chemical SiO_x interface, and the SiO_x layer is clearly resolved in the EDX map as well. The EDX map further shows that C concentration in the top most layer is 4.8 ± 1%, while the C content in the intrinsic Si inter-layer is below the detection limit. According to the Fourier transform computed from the HRTEM micrograph [see Figure 5(d)], the intrinsic Si buffer layer is highly crystalline after the annealing process. Based on these findings, we speculate that the presence of the intrinsic Si inter-layer hinders the reaction of the chemical SiO_x with C from the $SiC_x(p)$ layer and thus enables an untainted interface between the chemical SiO_x and the c-Si wafer with excellent surface passivation as shown in Figure 4.

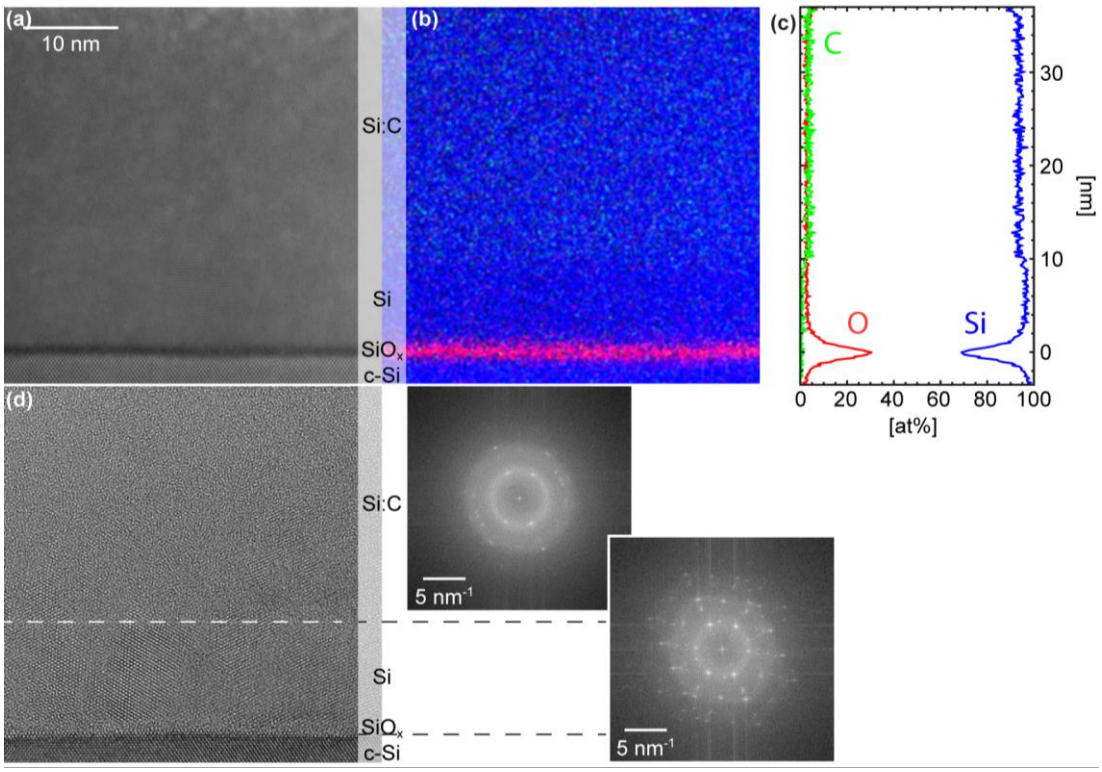

Figure 5. TEM characterization of the c-Si wafer/chemical SiO_x/ intrinsic Si buffer / $SiC_x(p)$ contact structure after annealing at 800°C for 5 minutes. (a) STEM HAADF image, (b) EDX map together with (c) EDX line scan and (d) HRTEM micrograph along with Fourier transforms computed at the position of both the buffer layer (bottom) and the a-$SiC_x(p)$ (top).

In order to optimize the contact structure further, the optimum inter-layer thickness of 10 nm was selected. The effect of the CH_4 gas flow during the deposition of the a-SiC_x(p) layer was investigated, while keeping all other process gases constant. The dependence of the iV_{oc} and J_0 on CH_4 flow is shown in Figure 6 for samples annealed for 5 minutes at temperatures of 800°C, 825°C and 850°C. For all investigated CH_4 flows, the best annealing temperature is 800°C. J_0 is decreasing with increasing CH_4 flow for the samples annealed at 850°C, but is worse than all other investigated conditions. In general, the passivation deteriorates with annealing temperatures higher than 800°C due to either more pronounced diffusion of the boron that increases the Auger recombination and the defect states at the chemical SiO_x / wafer interface, the reaction of C with the chemical SiO_x or the combination of both effects. Even though the intrinsic Si inter-layer is introduced to protect the chemical SiO_x interface, at high temperatures C may still diffuse through the intrinsic layer and reach the chemical SiO_x. For the latter, among the samples annealed at 800°C and 825°C, the best results were achieved with a CH_4 flow of 15 sccm. These excellent results demonstrate that boron-doped SiC_x is a promising material to realize hole-selective contacts in combination with an interfacial chemical SiO_x and an additional intrinsic Si inter-layer.

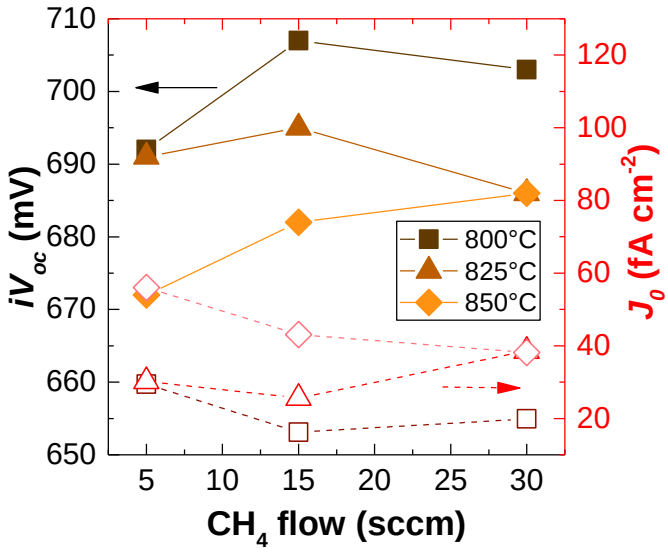

Figure 6. Measured implied open circuit voltage (iV_{oc}) and emitter saturation current density (J_0) of the contact structure annealed at different temperatures and subsequently hydrogenated with SiN_x, as a function of the CH_4 flow. Filled symbols represent the iV_{oc} and open symbols represent the J_0.

3.2 Cell Results

To investigate the potential of the chemical SiO_x / Si(i) / SiC_x(*p*) contact stack at the device level, the best symmetrical lifetime samples were processed to form solar cells. In addition, we varied the dopant—TMB—flow in order to explore eventually more favorable conditions, considering that the high doping level of the layer might increase surface recombination and therefore increase J_0. One side of the symmetrical lifetime sample was etched back, textured, and finished with a standard heterojunction front side as described in detail above.

Table 1. iV_{oc} and J_0 values of the Cell A and Cell B after a-Si:H(*i/n*) deposition and completed hybrid cell parameters.

	a-SiC_x(*p*)	After –*i/n*		Cell Parameters					
Sample	TMB flow [sccm]	iV_{oc} [mV]	J_o [fA cm^{-2}]	J_{sc} [mA cm^{-2}]	*FF* [%]	V_{oc} [mV]	η [%]	pV_{oc} [mV]	*pFF* [%]
Cell A	1.9	713	12.8	36.95	77.2	678.0	19.4	684	80.1
Cell B	1.5	717	12.3	37.20	79.1	694.7	20.4	699	82.2

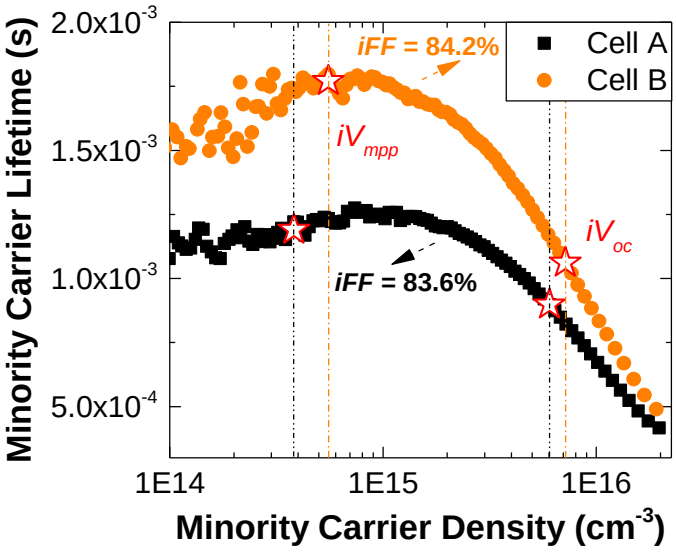

Figure 7. Effective carrier lifetimes of the samples after a-Si:H(i/*n*) front side PECVD deposition as a function of the excess carrier density together with associate implied voltages at maximum power point and in open circuit conditions.

The iV_{oc} and J_0 values after deposition of the a-Si:H(i/*n*) layer stack, *I-V* parameters of the completed cells as well as the pV_{oc} and *pFF* values at one-sun, are given in Table 1 for the best cells out of three on each wafer. The characteristic form of the lifetime curves reveal a direct information about the nature of the sample's surface passivation—chemical or field-effect—. The low injection level where the minority carrier density is lower than 10^{15} cm^{-3}, is mostly known to be associated with field-effect passivation. In Figure 7, the injection dependence of the minority carrier lifetimes for the samples after deposition of the a-Si:H(i/*n*) front side together with associated implied *FF* (*iFF*) and implied voltages at maximum power point and open circuit conditions are shown. After deposition of the a-Si:H(*i/n)* stack on the front side, for both samples the low injection tailing which implies the weak field-effect passivation is observed. Even though the tailing is slightly more pronounced for the cell B prepared with 1.5 sccm TMB flow, the same sample shows better chemical passivation. Overall, both cells prepared with TMB flow of 1.9 sccm (cell A) and 1.5 sccm (cell B) yield an iV_{oc} of above 710 mV and a J_0 of around 13 fA cm^{-2}.

However, cell A —the cell with the more heavily doped a-SiC_x(*p*) at the rear side— has slightly worse cell parameters. Although both samples were processed following the same fabrication steps, the texturization of the front sides might not be the same since they were processed at different time periods and the texturization was not optimized for this purpose. Additionally we measure a contact resistivity of 17 mΩ cm^{-2} on the sample prepared with the TMB flow of 1.5 sccm on *p*-type wafer. However, since the front side of the cell employs a standard silicon heterojunction electron contact which has a contact resistivity of 200 mΩ cm^{-2} on *n*-type,[40] the *FF* of the cell could be limited by the front side.

Figure 8(a) depicts the EQE, reflectance, and IQE spectra. Cell A exhibits a considerably higher reflectance in the blue part of the spectrum, which is the signature of a non-optimized front texturization. This results in a reduced J_{sc}, but most likely is also negatively effecting the V_{oc} and *FF*. It has to be noted also that the J_{sc} of 37 mA cm^{-2} is a typical value for standard SHJ solar cells, and is limited by parasitic absorption in the a-Si:H layers on the front side.[40] Figure 8(b) shows the *I-V* characteristics of the best cell obtained (cell B). In conclusion, the chemical SiO_x / intrinsic Si inter-layer / SiC_x(*p*) rear side structure allows excellent rear passivation, and has proven good cell performance with both doping conditions, enabling a V_{oc}=694.7 mV and a *FF*=79.1%. The developed rear contact thus demonstrates great potential to eliminate the patterning processes necessary for fabrication of PRC cells while boosting the V_{oc}.

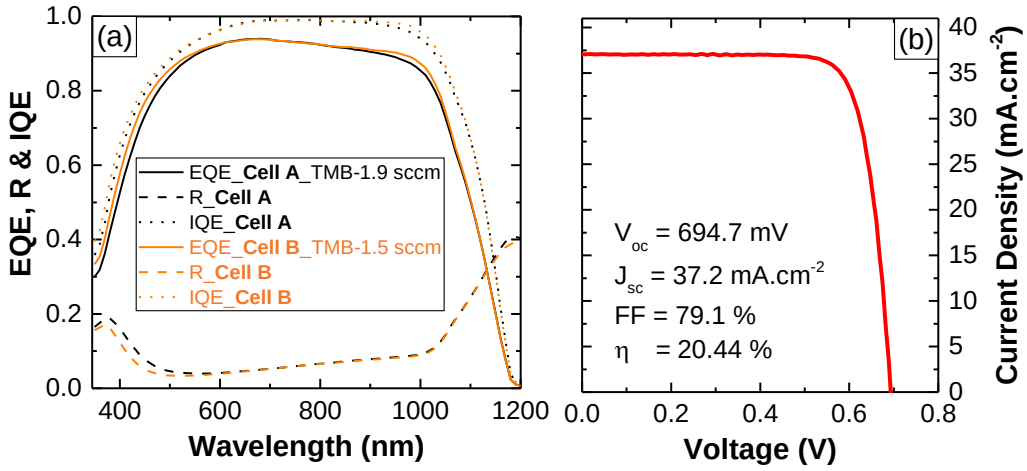

Figure 8. (a) EQE, reflectance (R), and IQE spectra of both cells, (b) I-V characteristic of the best cell (cell B).

4. Conclusion

In conclusion, we have presented a thermally stable hole-selective rear contact for *p*-type c-Si solar cells prepared by PECVD with in-situ doping. The contact consists of a chemical SiO_x / intrinsic Si inter-layer / $SiC_x(p)$ layer stack. Detailed structural analyses showed that the C-free intrinsic Si inter-layer is needed to obtain an optimized chemical SiO_x / c-Si wafer interface and high quality high-low juntion after the thermal process. An optimum annealing temperature of 800°C was identified. By optimizing the carbon content in doped SiC_x layer, iV_{oc} values of up to 708 mV and J_0 values of 17 fA cm^{-2} were demonstrated on symmetrical lifetime test structures. To show the potential of the passivating rear contact at device level, we presented a proof-of-concept solar cells with standard SHJ electron selective contact at the front side. The presented cells are limited by the front side reflection due to issues related to texturization and parasitic absorption in the SHJ electron contact employed on the front side. Despite these limitations, a V_{oc} of 694.7 mV, a *FF* of 79.1% and an efficiency of 20.44% demonstrate the potential of this $SiC_x(p)$ rear side scheme. We believe that the developed hole-selective contact would be an ideal replacement for partial rear

contact designs in industrial solar cells that employ a diffused $POCl_3$ front side. Indeed, such design eliminates the need for laser structuring of the passivation layer, which is currently necessary at the rear of PRC cells.

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