A Multiport Medium Voltage Isolated DC-DC Converter

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***Abstract*—A multiport medium voltage (MV) isolated DC-DC converter with integrated energy storage, suited for connection of low voltage (LV) and medium voltage (MV) DC grids is presented. A multi-stage structure, adapted for MV ratings, is composed of multiple identical submodules connected in an Input-Series-Output-Parallel (ISOP) configuration. Each submodule has three fully bidirectional ports, that are galvanically isolated. This is achieved by means of a three-winding medium frequency transformer, where each leakage inductance combined with a resonant capacitor creates a resonant tank, benefiting from soft switching operation. Each submodule has two additional buck/boost stages, to actively control the power exchange with external DC circuits. The inner resonant stage is operated in open-loop and adapts its mode of operation based on the actual power flow. The remaining ports, dedicated to the storage, can be operated independently from the power flow between the MV and LV side, in order to charge or discharge the storage elements. Switched mode simulations are used to verify and demonstrate various operational modes and performance of the converter.**

***Index Terms*—MVDC, Multiport, DC-DC, Resonant Converter**

I. Introduction

The weakness of the renewable energy sources is their climate dependency and consequent volatility, which can be partly compensated by a judicious geographic distribution and further supported through the integration of storage technologies. This implies a need for new types of grids, able to support more interconnections, integrate energy buffers while providing flexible and reliable operation. To avoid unnecessary power circulation and save some capacity in the transport infrastructures, the energy should be stored close to its production in order to be consumed by the surrounding loads. This would limit the grid solicitation only to temporary flow of the surplus or lack of power. The MVDC grids are seen as feasible solution to the link between low/medium voltage generation/distribution and existing high voltage transmission lines [1]. They can reinforce existing and future power distribution networks efficiently, considering that renewable and energy storage technologies are inherently DC and low-voltage by nature, respectively [2].

To enhance reliability, flexibility and efficiency of the charge-discharge cycle of the storage elements, the multiport DC-DC converters offer interesting prospects [3]. Although the converters based on the connection of multiple ports through a non-isolated common DC bus offer a certain simplicity of control, they have a limited range of voltage conversion ratio. The literature presents some galvanically isolated topologies based on multi-winding transformers derived from the Dual-Active-Bridge (DAB) and extended with a third winding [4] and [5] or even two additional ports [6]. While they have the advantages of the freedom to set the turn ratio accordingly, allowing grids of different voltages to be interfaced, their power flow control is done through phase-shift or PWM that results in a reduced soft switching operation range. A multiport resonant converter, having Medium Frequency Transformers (MFTs) combined with distributed resonant capacitors, is presented in [7], with one source port and two load ports operated in open loop. Similarly, [8] presents topology with two sources and one load where the power flow and the load sharing are regulated through a phase-shift control. While these two LLC resonant converters demonstrate some benefits in terms of soft switching, they are suitable only for low voltage and low power applications.

The MV insulation constraints can be overcome by the use of some multi-stacked-stage structures, reducing the voltage stresses on the semiconductor devices. Such a solution has many advantages as highlighted in [9]. The overall system availability/reliability is increased, due to redundancy of the key elements and due to the distribution of the electrical and thermal stresses between the stages. In the case of a large voltage conversion ratios, the ISOP structure has some advantages due to the split of the voltage on the series side (high-voltage/low-current) and the current sharing on the parallel side (low-voltage/high-current). The ISOP structure has been demonstrated for a power electronic traction transformer where multiple LLC resonant circuits are used in a multi-stage configuration [10] while the IPOS resonant topology is presented in [11].

The topology of a novel medium voltage multiport converter is proposed in this paper. It is the ISOP combination of multiple submodules based on the structure presented in [12]. The multiport converter is suited for bidirectional interfacing of MVDC and LVDC grids, through the two main ports, while the third port of each submodule is dedicated to the connection of low voltage storage elements with reduced ratings (e.g. 0.2 p.u.). Each submodule is composed by a three winding MFT and additional capacitors creating a distributed LLC resonant tank. The resonant components are tuned on the three sides

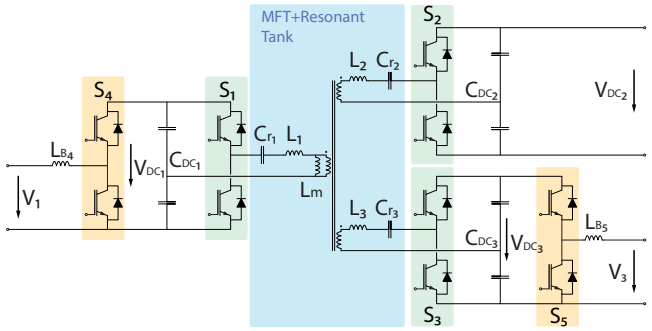

Fig. 1. Topology of a basic submodule with five switching cells and multiwinding MFT with distributed resonant tank.

following [13], in order to allow an extended soft switching operation range, compared to solutions based on the multiple active bridge structure. As the MFT provides a galvanic isolation between the ports and the different submodules, the storage elements (ES) can be freely selected for each port, allowing a hybrid combination of batteries and ultra-capacitors, in an optimal configuration.

The topology of a basic submodule and its operating principles are presented in section II, while the complete multi-stage modular medium voltage structure, design considerations and control scheme are explained in section III. Simulation results obtained with PLECS switched model are shown in section IV while summary and conclusions are provided in section V.

II. Basic Submodule

The inner part of the converter is a three winding MFT with a turn ratio according to the desired output voltages and connected to three half-bridges (S_1, S_2 and S_3 in Fig 1). To benefit from soft switching and achieve high efficiency, each winding's leakage inductance, combined with an external capacitor, creates a resonant tank with the resonant frequency f_{res}. The resonant part is operated in open loop (half-cycle discontinuous conduction mode) without any complex control scheme, and behaves the same way as a DC transformer. The ports that are providing the power are actively switched, while the load ports are turned off and their freewheeling diodes are used as passive rectifiers. When the port is active, its semiconductors are modulated with a constant switching frequency $f_{sw,res}$, below the resonant frequency ($f_{sw,res}/f_{res} = f_n \leq 1$), and with a fixed duty cycle of around 50%. There are several possible operating modes based on the power flow direction [13]. To avoid large current transients during start-up or change of mode of operation from passive to active, the duty cycle follows a ramp from 0 to 50%. Typical current waveforms in such structure are shown in Fig. 2, for different operating conditions.

Since no active control is applied on the inner resonant stage, the power flow is regulated by two additional stages (S_4 and S_5) on the ports 1 and 3. These stages are based on bidirectional switching cells and are operated either as buck or boost converter depending on the actual mode of operation.

III. ISOP Multiport Isolated DC-DC converter

To reach MV and high power ratings, a multi-level ISOP structure is adopted (see Fig 3). A number of N submodules are connected in series on their port 1, while in parallel on their port 2. Remaining N ports (each submodule's port 3) are independent and serve to connect different storage elements (ES). Newly created MV port 1 and LV port 2 are supporting the main power flow, while the N ports 3.1 to 3.N are auxiliary storage ports with reduced ratings, where connected ES elements can be independently charged or discharged.

Thanks to the ISOP structure and fixed frequency operation of the inner resonant stage, the converter does not need any active balancing of voltages on the MV side. Practical realization will inherently produce some deviations of components from their designed values, but as long as these are within

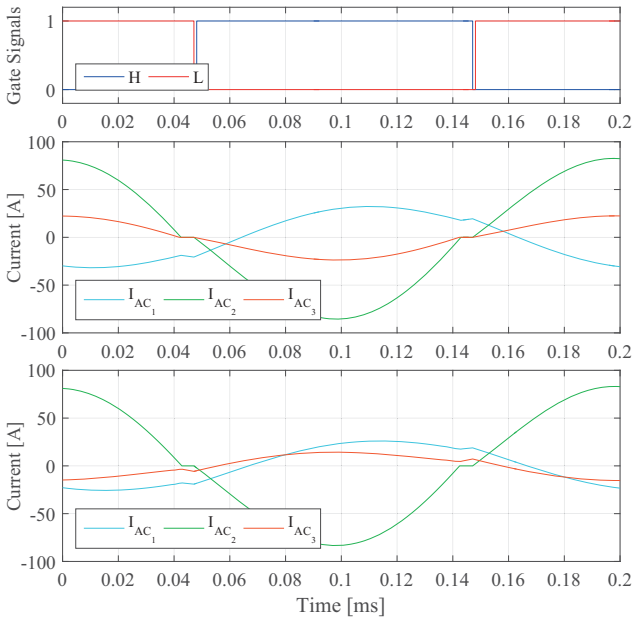

Fig. 2. Typical waveform in a multiport LLC structure: The upper plot shows the gate signals applied to the active ports. The middle plot shows the three currents in the resonant stage when the port 1 is actively switched and the ports 2 and 3 are passive (rectifiers). The bottom plot shows a case where the ports 1 and 3 are actively switched and supporting the load on the port 2.

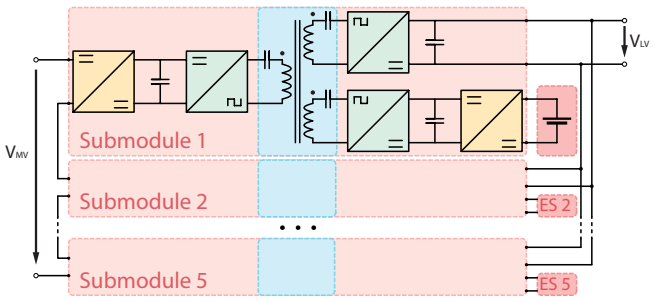

Fig. 3. A multiport medium voltage isolated DC-DC converter with $N = 5$ submodules in ISOP configuration.

TABLE I
RATINGS AT CONVERTER LEVEL

Power	Voltage
P_{MV} = 500 kW	V_{MV} = 10 kV $\pm$ 20%
P_{LV} = 500 kW	V_{LV} = 750 V $\pm$ 20%
P_{ES} = 100 kW	V_{ES} = 300 V $\pm$ 33%

TABLE II
RATINGS AT SUBMODULE LEVEL

Power	DC Voltage	Input/Output Voltage
P_1 = 100 kW	V_{DC_1} = 2500 V	V_1 = 2000 V
P_2 = 100 kW	V_{DC_2} = 750 V	V_2 = 750 V
P_3 = 20 kW	V_{DC_3} = 450 V	V_3 = 300 V

TABLE III
LLC RESONANT TANK PARAMETERS

Turn Ratio = 250:75:45	L_m =3.1mH
$f_{sw,res}$ = 5kHz	f_n = 0.95
L_1 = 41.00 μH	C_{r1} = 22.81 μF
L_2 = 3.69 μH	C_{r2} = 283.21 μF
L_3 = 7.40 μH	C_{r3} = 130.00 μF

TABLE IV
DC LINK CAPACITORS PER PORT

Voltage Ripple	DC Capacitors
ΔV_1 = 63 V	C_{DC_1} = 250 μF
ΔV_2 = 20 V	C_{DC_2} = 500 μF
ΔV_3 = 12 V	C_{DC_3} = 620 μF

certain margins the voltage balancing is maintained, as shown in the next section.

The number of submodules depends on the operating voltages, selected semiconductors and eventually desired redundancy (not considered in this work). Considering boost nature of operation on the MV side, V_{DC_1} has to be bigger than $V_{MV_{max}}/N$. For the simulation studies, power and voltage ratings are implemented based on a high power MV prototype currently under development, and are given in Tables I and II. Considering 4.5 kV IGBT devices, $N = 5$ submodules are required with a rated $V_{DC_1} = 2.5$ kV on the MV side.

The DC capacitors C_{DC_i} are sized considering the voltage ripple specification of 2.5% and following the method described in [12]. Resulting parameters are shown in table IV. Note that a phase-shift of $2\pi/N$ [rad] may be introduced between the resonant stage of each submodule. Since the output are connected in parallel on the LV side, it results in a reduction of the voltage ripple on V_{LV}. This has to be considered during the sizing of C_{DC_2}.

The components of the inner resonant stage are sized following the methodology developed in [13]. The principle is to design the transformer and the elements of the distributed resonant tank for the soft switching conditions on all the three ports. Each port is characterized by an operating voltage and a maximum load modelled with an equivalent AC resistance $R_{ac_{1,2,3}}$, using the first harmonic approximation (FHA). To each R_{ac} corresponds a $L_{r_{max}}$, defined in [12], which is the maximal resonant inductor of the equivalent single tank allowing an inductive behavior and zero voltage switching (ZVS). Then the $L_{equ_{1,2,3}}$, representing the resonant inductor of the equivalent single tanks seen from each port, are evaluated for all three ports and the whole operating range. Keeping $L_{equ} \leq L_{r_{max}}$ defines the space of allowed combination of L_1, L_2 and L_3. In addition, further criteria on the L_{equ} can be applied in order to refine the selection of $L_{1,2,3}$, for instance keeping L_{equ} the closest possible to $L_{opt_{1,2,3}}$, as defined in [12], or some criteria linked to the physical realization of the transformer (minimum realizable leakage inductance). Resulting parameters have to be adjusted, taking into account the DC link capacitors C_{DC_i} which appear in series with the resonant circuit. They are given in Table III.

The switching frequencies of the buck/boost stages S_4 and S_5, respectively $f_{sw,MV}$ and $f_{sw,ES}$, are subject to an optimization and generally are different from $f_{sw,res}$. Switching frequencies $f_{sw,MV}$ and $f_{sw,ES}$ are optimized considering selected semiconductor devices of S_4 and S_5 and switching losses due to hard switched operation. On the other hand, the choice of $f_{sw,res}$ represents a trade-off between different ports characterized with different rated voltages and suitable semiconductor voltage classes (limiting analysis to a selected half-bridge switching modules based on the Silicon semiconductors). Considering that V_{DC_1} is higher than V_{DC_2} and V_{DC_3}, high-voltage devices are used on the MV ports while the low-voltage devices are implemented on the LV and ES ports, resulting in $f_{sw,MV} \leq f_{sw,res} \leq f_{sw,ES}$.

The inductors $L_{B_{4.i}}$ of each submodule can be kept separate or combined into a single physical component of value L_{B_4}. Further, the N buck/boost stages can be interleaved with a $2\pi/N$ [rad] phase shift, which reduces the required inductance value for a given current ripple. Defining $V_{DC_{tot}}$ as the sum of all the $V_{DC_{1.i}}$, and assuming that these voltages are almost identical, one has $V_{DC_{tot}} = N(V_{DC_1} + \Delta V_{DC_1})$, where ΔV_{DC_1} represents the voltage variation due to the load regulation. In the case without interleaving, the voltage levels applied to L_{B_4} are defined in (1).

$$V_{L_{B4}} = \begin{cases} V_{MV} - V_{DC_{tot}} \\ V_{MV} \end{cases} \tag{1}$$

In the case of interleaving, the combined switched voltage is varying between two consecutive fractions of $V_{DC_{tot}}$ ($x_1, x_2 \subset [1, 2, 3, 4, 5]$) and is given by (3).

$$\frac{x_1}{N} \leq D'_4 \leq \frac{x_2}{N} \tag{2}$$

$$V_{L_{B4}} = \begin{cases} V_{MV} - x_1(V_{DC_1} + \Delta V_{DC_1}) \\ V_{MV} - x_2(V_{DC_1} + \Delta V_{DC_1}) \end{cases} \tag{3}$$

The duty cycle $D'_4 = 1 - D_4$ in steady state can be approximated by (4)

$$D'_4 = \frac{V_{MV}}{V_{DC_{tot}}} \tag{4}$$

TABLE V
BUCK/BOOST STAGES PARAMETERS

Buck/Boost MV (S_4)	Buck/Boost ES (S_5)
$f_{sw,MV}$ = 1 kHz	$f_{sw,ES}$ = 10 kHz
ΔI_{MV} = 5 A	ΔI_{ES} = 2 A
L_{B_4} = 10 mH	L_{B_5} = 5 mH

Thus the current ripple can be given without interleaving (5) and with interleaving (6).

$$\Delta I_{MV_{wo}} = \frac{D_4'(V_{MV} - V_{DC_{tot}})}{f_{sw,MV} L_{B_4}} \tag{5}$$

$$\Delta I_{MV_{wi}} = \frac{(D_4' - x_1/N) \cdot (x_2(V_{DC_1} + \Delta V_{DC_1}) - V_{MV})}{f_{sw,MV} L_{B_4}} \tag{6}$$

The buck/boost inductors are sized according to current ripple specifications and are given in Table V. A rather simple control scheme is deployed for the converter. Within the bandwidth of the power flow controller, the LV grid is considered as a load or a source with a fluctuating power and is modelled as a current source, while the MV grid and the storage elements are modeled as voltage sources. In this scenario, the voltage of the LV grid (V_{LV}) has to be regulated with the contributions from the MV grid and energy storage elements.

The resonant stage is operated in the open loop close to the resonant frequency, resulting in a DC gain close to unity, and can thus be neglected during the control loop synthesis. Thus the ISOP structure imply that all the DC capacitors of the converter can be modeled with their series/parallel combinations, taking into account the turn ratio of the transformer and resulting in the capacitor C'_{equ} (reported to the primary) given by (7). Its voltage is proportional to the regulated output voltage V_{LV}.

$$C'_{equ} = C_{DC_1} + \frac{n_2^2}{n_1^2} C_{DC_2} + \frac{n_3^2}{n_1^2} C_{DC_3} \tag{7}$$

The buck/boost stages S_4 of all the four submodules are operated with a common duty cycle D_4, which can be considered as the control input for the power contribution from/to

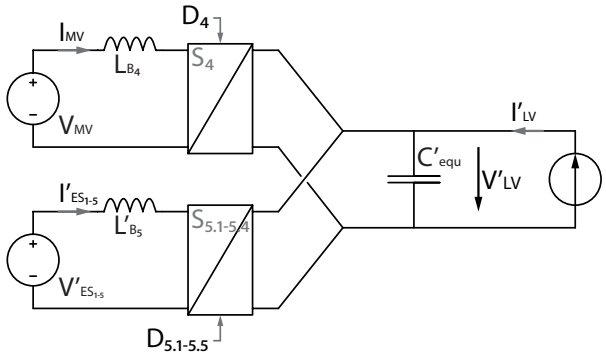

Fig. 4. Simplified model of the converter for the control. Everything is reported to the primary.

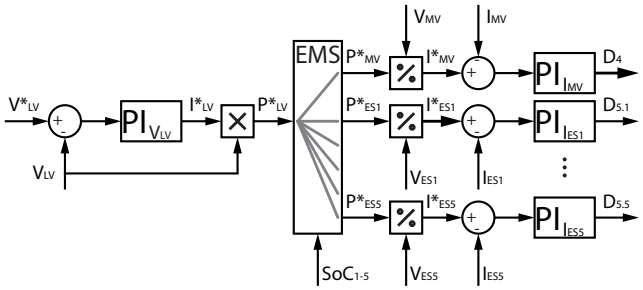

Fig. 5. Proposed control structure

the MV grid. The five duty cycles $D_{5.1}$ to $D_{5.5}$ of the storage ports are then allocated to the control inputs for the power contributions from/to the energy storage elements.

The proposed overall control structure is shown in Fig. 5. An outer voltage control loop and the voltage regulator $PI_{V_{LV}}$ gives a reference for the total current that should be injected or sinked into/from the equivalent C_{equ}. This current has to be shared between the MV side and different storage elements, according to an application related strategy (Energy Management System - EMS), in order to give a reference for each current controller. This defines the contribution of all MV and ES ports, and the current regulators $PI_{I_{MV}}$ and $PI_{I_{ES1}}$ to $PI_{I_{ES5}}$ generate the duty cycles D_4 and $D_{5.1-5.5}$ for the buck/boost stages $S_{4.1-4.5}$ and $S_{5.1-5.5}$. Even though not shown in details in Fig. 5, it is understood that EMS system receives data from the respective ES elements about their status (eg. state of charge (SoC) of batteries).

In the normal operation, the main purpose of the converter being to provide support to the grid with the energy storage, the direction of the power flow (charge or discharge) should be the same for the N submodules. Nevertheless, the structure can handle simultaneous charge and discharge of the storage element with some restrictions, related to electrical ratings of the ports. In steady-state, the power through the MV port is equally shared between the N submodules and supported (if needed) with ES ports. Adopting the convention that power is positive when it flows into the converter (at any port) one has:

$$P_{MV} = -P_{LV} - \sum_{i=1}^{N} P_{ES_i} \tag{8}$$

$$P_{MV_i} = \frac{P_{MV}}{N} \qquad i = 1, ..., N \tag{9}$$

Considering bi-directionality and multiple indepedent ports, various different operating modes of the converter are possible, as shown in the next section.

IV. SIMULATION RESULTS

Switched mode simulations of the complete system are carried out in PLECS. The simulation shows the operation of the voltage control loop for the LV side (V_{LV}) at half of the nominal power (power flow is from MV to LV side). At a given time, the discharge of the storage element 1 is activated, while 40 ms later, the charging of the storage element 2 is

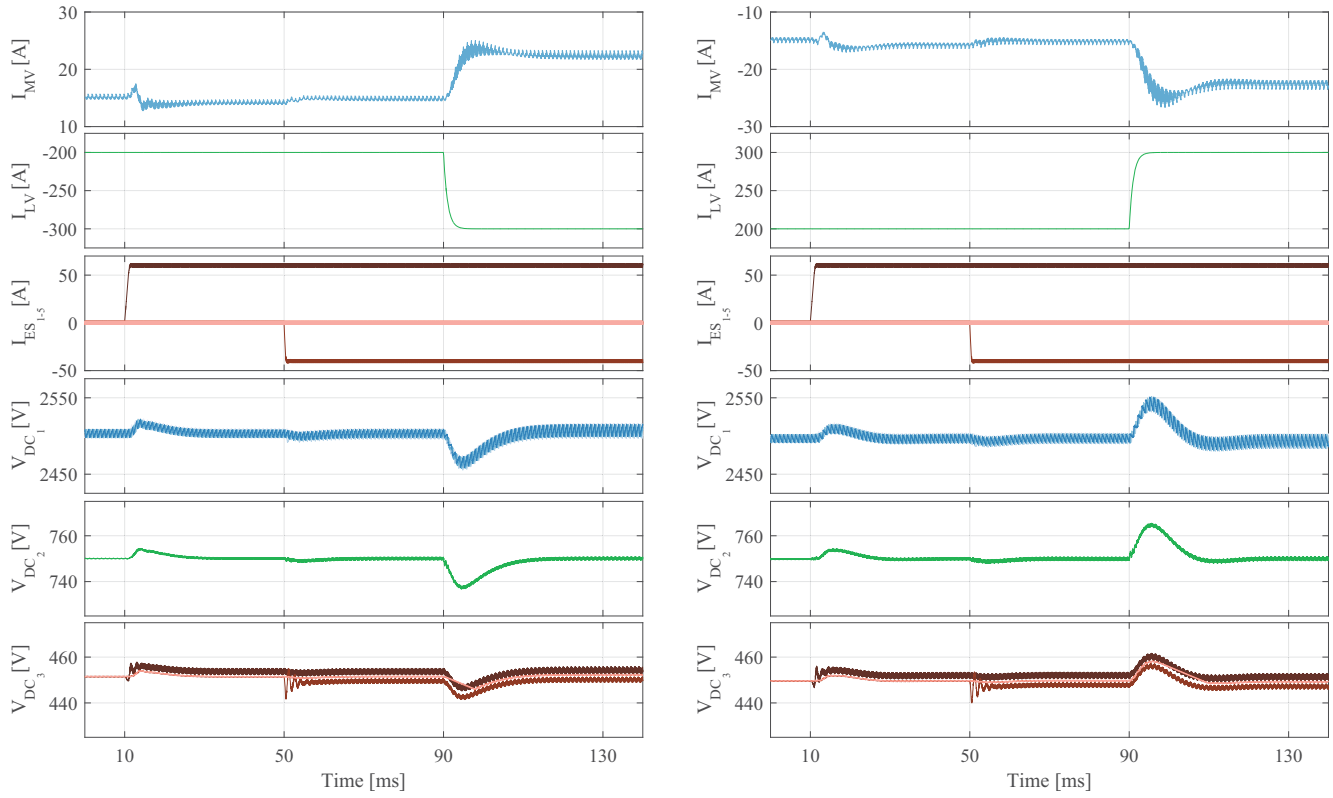

Fig. 6. At $t = 10$ ms, the storage discharge current I_{ES_1} is increased from 0 to 60 A, at $t = 50$ ms, the charge current I_{ES_3} is increased from 0 to -40 A and at $t = 90$ ms, the load/source current through the LV port is increased from 200 A to 300 A. V_{DC_2} is regulated to 750V while the $V_{DC_{1.i}}$ are adapted in order to supply the power requested by the low voltage port. In (a) the main power is flowing from the MV port to the LV port while it is reversed in (b). In both cases, cross regulation is visible on the $V_{DC_{3.i}}$.

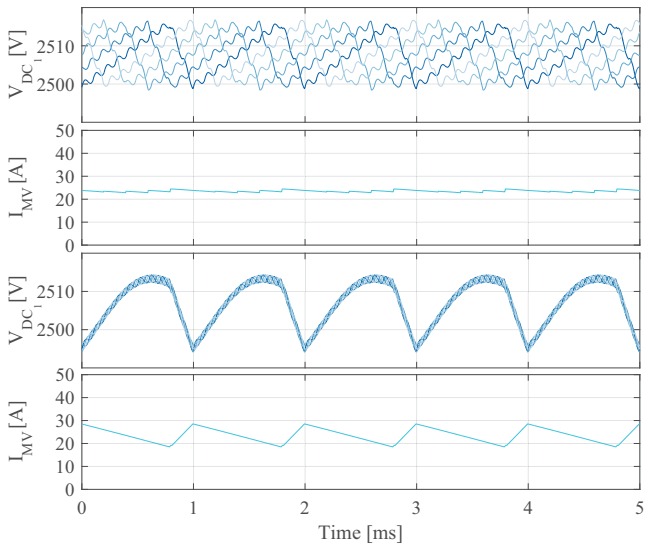

Fig. 7. The voltage ripple on the DC capacitors of each port 1 ($V_{DC_{1.1-5}}$) and the I_{MV} current ripple with (upper two plots) and without (lower two plots) interleaving of the buck/boost stages of the MV side. To illustrate better current ripple improvement, the simulation with interleaving is done with an inductor $L_{B_4} = 10$ [mH] and the simulation without interleaving with a $L_{B_4} = 200$ [mH].

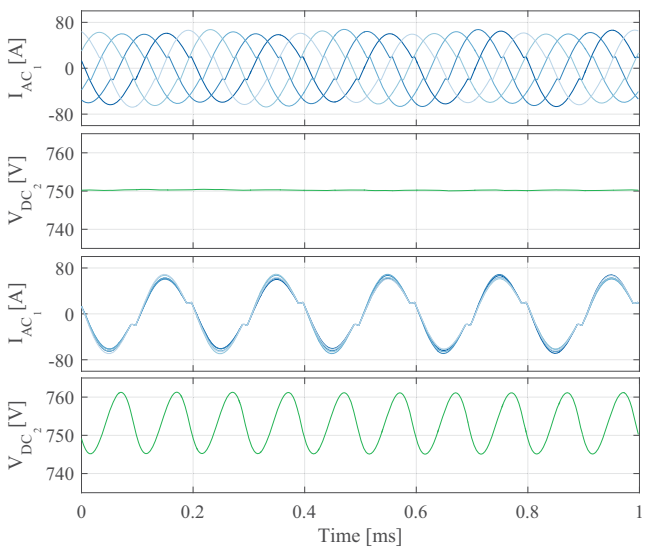

Fig. 8. The resonant current in each port 1 ($I_{AC_{1.1-5}}$) and the ripple on the output voltage V_{DC_2}, with (upper two plots) and without (lower two plots) interleaving of the resonant LLC stages.

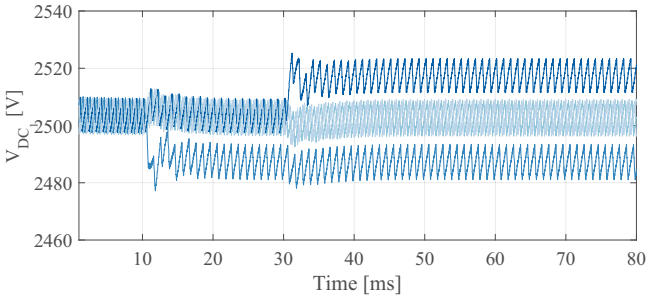

Fig. 9. Multiple DC link voltages on the MV side are shown, before and after an artificially introduced deviation of the resonant tank elements from their designed values is introduced. After $t = 10$ ms, the value of L_1 and Cr_1 of the submodule 2 have been increased by +20% while after $t = 30$ ms, the value of L_1 and Cr_1 of the submodule 4 have been decreased by -20%. The results show a consequent offset of less than 1% on the voltage (and thus the power), but no instability, and the converter continues to operate normally.

activated, followed by load increase of the LV side. This scenario is somewhat arbitrarily chosen in order to demonstrate the independent operation of the storage port of the different submodules, while the voltage regulation is done through the boost stage of the MV port. An overview of the complete sequence is shown in Fig. 6a, while the same sequence but with a reversed power flow between the MV and the LV port is shown in Fig. 6b.

The effects of the interleaving of the buck/boost stages on the MV side and the interleaving the LLC resonant stages are shown in Fig. 7 and Fig. 8, respectively, with further description provided in captions. Finally, the effect of deviations of the resonant tank elements from their designed values, on the voltage balancing on the MV side is illustrated in Fig. 9. It is reasonable to expected that deviations of the resonant tank elements can be maintained with $\pm 20\%$ deviations from desired values.

V. Conclusion

This paper presents the topology of a multiport medium voltage DC-DC converter. It is based on the ISOP combination of multiple identical submodules, each comprising an open-loop operated resonant stage, and closed-loop operated regulation stages on two out of three ports. In this way, conversion tasks have been clearly separated between voltage adaptation and galvanic isolation done with inner resonant stage and control realized with regulation stages. The operating modes of the converter have been described and a simple control scheme is proposed, allowing for full bi-directionality and power flow control. The converter is characterized with multiple auxiliary ports which are made available for the connection of LV energy storage elements, that can be freely mixed in terms of different technologies (e.g. ultra-capacitors and batteries). Thus, flexible and easily scalable grid supporting solutions can be realized, both in terms of power and energy. Furthermore, the presented topology allows further extensions for higher operating voltages by increasing the number of submodules connected in series (MFT insulation must be taken into account and will directly depend on the system operating voltage) or higher power with paralleling at the submodule or converter level.

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