Modeling and Simulation of Low Power Ferroelectric Non-Volatile Memory (NVM) Tunnel Field Effect Transistors (TFET) Using Silicon-doped Hafnium Oxide as Gate Dielectric

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Abstract

The implementation and operation of the ferroelectric nonvolatile memory (NVM) tunnel field effect transistors (Fe-TFETs) with silicon-doped HfO_2 is proposed and theoretically examined for the first time, showing that Fe-TFET can operate as ultra-low power nonvolatile memory even in aggressively scaled dimensions. A Fe-TFET analytical model is derived by combining the pseudo 2-D Poisson equation and Maxwell's equation. The model describes the ferroelectric TFET behavior when a time-dependent voltage is applied to the device with hysteretic output characteristic due to the ferroelectric's dipole switching. The theoretical results provide unique insights into how device geometry and ferroelectric properties affect the Fe-TFET transfer characteristic. The recently explored ferroelectric, silicon-doped HfO_2 is employed as the gate ferroelectric. With the ability to engineer ferroelectricity in HfO_2 thin films, a high-K dielectric well established in memory devices, the silicon doped HfO_2 opens a new route for improved manufacturability and scalability of future 1-T ferroelectric memories. In the current research, a Si:HfO_2 based Fe-TFET with large memory window and low power dissipation is designed and simulated. Utilizing our presented model, the device characteristics of a Fe-TFET that takes full benefits from Si:HfO_2 is compared with the same devices using well-known perovskite ferroelectrics.

Keywords: HfO_2, Analytical model, surface potential, ferroelectric, nonvolatile memory, FeTFET

☆This document is a collaborative effort.

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1. Introduction

Ferroelectric materials can be utilized as electrically switchable nonvolatile data storage elements as their polarization can change due to the external electric field. Recently, novel devices called ferroelectric TFETs [1], and ferroelectric FETs have been proposed as promising candidates for future nonvolatile memory applications [2-3]. In ferroelectric field effect devices, two stable states of the ferroelectric's polarization are used for data storage [4]. Nonvolatile data storage, fast writing, and nondestructive read-out operation have been reported for ferroelectric field effect transistors [5]. However, the industrial implementation of ferroelectric devices especially in nanoscale still missing due to the integration and scaling obstacles of conventionally used perovskite type ferroelectrics such as Lead Zirconate Titanate (PZT). The recently discovered ferroelectricity in HfO_2 thin films [6], enabled CMOS-compatible manufacturing of highly scaled ferroelectric devices down to $28nm$ ground rule [7-8].

By scaling devices down to nanoscale, power density becomes a challenging issue as the power density per area of the chip increases. The tunneling field effect transistors have been investigated intensely in recent years [9] due to their considerable potentials for ultra-low-power applications [10-11]. Using the advantages of both ferroelectric thin films for data storage and TFETs as energy efficient devices, it is possible to design a new class of nonvolatile memories, with a relatively large memory window, fast writing, non-destructive read-out operation, and low power consumption. In this work, we propose a comprehensive, quantitative model for investigation of FeTFETs. The successful design of a FeTFET for nonvolatile data storage requires a thorough understanding of the device operation principals. It is necessary to develop an analytical model for FeTFETs operation to optimize the design. Hence, an analytical model for FeTFETs is proposed and verified with Sentaurus TCAD [12] simulation tool. The model is developed by solving the 2-D Poisson equation [13] for a single gate TFET and considering the effect of the ferroelectric polarization on the surface potential. The polarization effect is calculated by solving Maxwell's first equation in the gate stack. A numerical method is employed to calculate the polarization hysteresis for both saturated and nonsaturated hysteresis loops [14]. Based on our proposed model, memory window of the Ferroelectric Memory Field-Effect Transistors (FeMTFETs) using different ferroelectric materials is investigated.

2. Device Modeling

2.1. Approach and Definitions

In this paper, an n-type SOI ferroelectric TFET is studied. The device is schematically depicted in Fig. 1. The length of the channel is $200nm$ to reduce short channel effects, the doping concentration of the lightly doped channel is $5 \times 10^{14} cm^{-3}$, the highly doped $p+$ source concentration is $1 \times 10^{20} cm^{-3}$ and the $n+$ doped drain is $1 \times 10^{18} cm^{-3}$ to suppress the ambipolar behavior [14]. The silicon doped HfO_2 is utilized as ferroelectric layer due to its unique

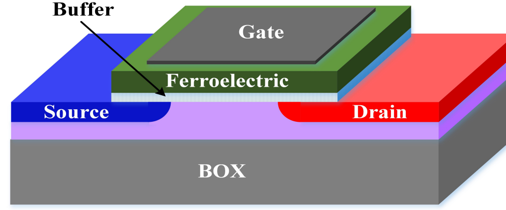

Figure 1: The device schematic of an SOI-FeTFET, the gate stack of a conventional single gate TFET is replaced with a series combination of a ferroelectric and linear dielectrics.

property of having ferroelectricity even in a $5nm$ thick, thin film [15-16]. For the model verification, we have used $10nm$ of Si:HfO$_2$ with $9\mu C/cm^2$ remanent polarization and $1.1MV/cm$ coercive field [7]. We will discuss how the relatively high coercive field and remanent polarization guarantee a large memory window (and retention time) in the Ferroelectric Memory TFET (FeMTFET).

To develop the ferroelectric TFET model, we have combined the switching analytical modeling of ferroelectric capacitors [17] with the Band-to-Band Tunneling modeling of TFETs. Wu et al. [13] proposed the analytical modeling of TFETs based on the gate and drain dual modulation effects by solving Poisson equation in the device channel. Miller et al. [14], [18-19] developed a compact model that accurately describes the dipole polarization switching in a ferroelectric capacitor utilizing Maxwell's first equation. We employed Maxwell's equation in series with Poisson equation to precisely calculate the surface potential profile along the channel. Finally, the device current is calculated by determining the surface potential around the tunneling junctions. The gate stack is considered as a ferroelectric on a linear dielectric. The proposed model is verified using Sentaurus TCAD commercial simulator.

2.2. Model

In this subsection, we describe the relation between the ferroelectric polarization and the surface potential in an MOS structure including a ferroelectric layer [14], [20]. The electrostatic equations are derived starting with Maxwell's equation

$$\nabla.D = \rho, \tag{1}$$

$$D = \epsilon_0 \epsilon E + P_d, \tag{2}$$

where D is the displacement, ρ is the free charge density, E is the electrical field, ϵ_0 is the vacuum permittivity, ϵ is the linear dielectric constant, and P_d is the contribution of the switching dipoles. Solving (1) and (2) in conjunction with the definition $E = -\nabla\phi$ (ϕ is the electrostatic potential):

$$V_{GB} = \phi_s - \frac{\sigma_s}{C_{stack}} - P_d(E_f)\frac{d_f}{\epsilon_0 \epsilon_f}. \tag{3}$$

In (3), C_{stack} describes the gate total capacitance, σ_s is the silicon charge, d_f and ϵ_f are ferroelectric thickness and relative permittivity and ϕ_s is the silicon surface potential. The ferroelectric polarization changes the surface polarization by a value of $P_d\,(d_f/\epsilon_0\epsilon_f)$.

We explain the FeTFET behavior by considering the effect of the polarization on the surface potential for a known polarization. Combining Maxwell's first equation with Wu's analytical solution for TFET surface potential [13], the surface potential in middle of the channel in the whole range of the operation can be given as

$$\begin{aligned}\phi_{ch} &= F + \frac{kT}{q} ln \left\{ \frac{q}{kT} \left[\frac{kT}{q} + \frac{\sqrt{F}}{\sqrt{F}+\gamma} \left(V_{GS} - V_{fb} + P_d \frac{d_f}{\epsilon_0 \epsilon_f} - F \right) + \right.\right. \\ &\left.\left. \frac{1}{2} \left[\frac{F}{(\sqrt{F}+\gamma)^2} - \frac{\gamma\,[F-2]}{2(\sqrt{F}+\gamma)^3} \right] \left(V_{GS} - V_{fb} + P_d \frac{d_f}{\epsilon_0 \epsilon_f} - F \right)^2 \right] \right\} \end{aligned} \tag{4}$$

$$F = \frac{1}{2} \left\{ V_{DS} + \Phi + \phi_{ch,dep} - \sqrt{(\phi_{ch,dep} - V_{DS} - \Phi)^2 + \delta^2} \right\}, \tag{5}$$

$$\phi_{ch,dep} = \left\{ \sqrt{V_{GS} - V_{fb} + P_d \frac{d_f}{\epsilon_0 \epsilon_f} + \frac{\gamma^2}{4}} - \frac{\gamma}{2} \right\}^2 . \tag{6}$$

where V_{fb} is the flat band voltage, γ is the body factor defines as $\sqrt{2\epsilon_{si} q N_{ch}}/C_{stack}$ (N_{ch} is the channel doping), δ is a small smoothing factor and $\phi_{ch,dep}$ is the surface potential in the gate control regime [13]. Φ is the surface potential needed for sufficient inversion charge to screen the gate modulation and can be expressed as $(kT/q)ln(N_{ch}N_{inv}/n_i^2)$, N_{inv} is the required inversion charge density to screen the gate voltage.

An accurate expression of the surface potential profile around the tunnel junction is needed to calculate the tunneling current. We use the pseudo 2-D Poisson equation to obtain the potential profile along the channel [21]. The parabolic approximation of the potential in a direction normal to the surface is adopted so that the Poisson equation can be reduced to the well-known form

$$\frac{d^2\phi_s(x)}{dx^2} - \frac{\phi_s(x) - \left(V_{GS} - V_{fb} + P_d \frac{d_f}{\epsilon_0 \epsilon_f} \right)}{\lambda^2} = \frac{q N_{ch}}{\epsilon_{si}}, \tag{7}$$

where $\lambda = \sqrt{\epsilon_{si} t_{si} / C_{stack}}$ is the characteristic length of the channel. Solving (7) by considering boundary conditions and the continuity of potential and electric field at the source-channel and channel-drain junctions, the surface potential profile around tunneling junctions can be obtained as

$$\phi_s(x) = \left(V_{GS(eff)} \right) + \left(\phi_{ch} - V_{GS(eff)} \right) \cosh \left(\frac{x - x_{sc}}{\lambda} \right) \cdots 0 \le x \le x_{sc}, \tag{8}$$

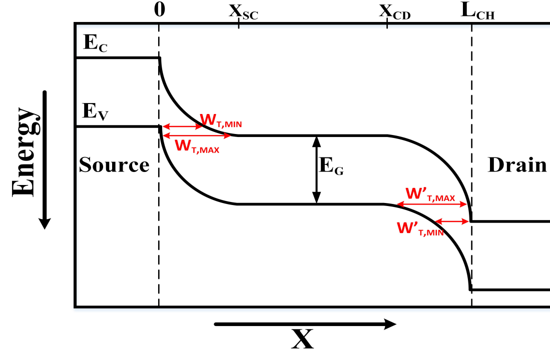

Figure 2: The energy bands in a tunneling field effect transistor that illustrates the maximum and minimum of the tunneling width in the source-channel and channel-drain junctions [13].

$$\phi_s(x) = \left(V_{GS(eff)}\right) + \left(\phi_{ch} - V_{GS(eff)}\right) \cosh\left(\frac{x - x_{sd}}{\lambda}\right) \cdots x_{cd} \leq x \leq L_{ch}, \quad (9)$$

$$x_{sc} = \lambda \cosh\left(\frac{V_{S0} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right), \quad (10)$$

$$x_{cd} = L_{ch} - \lambda. \cosh^{-1}\left(\frac{V_{D(eff)} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right). \quad (11)$$

In equations (8) to (11), V_{S0} subscribes to the source potential, $V_{D(eff)}$ is the potential in the drain region ($V_{D(eff)} = V_{S0} + V_{bi,SD} + V_{DS}$), $V_{GS(eff)}$ is the gate effective voltage ($V_{GS(eff)} = V_{GS} - V_{fb} + P_d(d_f/\epsilon_0\epsilon_f) - (qN_{ch}/\epsilon_{si})\lambda^2$), and ϕ_{ch} is the surface potential in the center of the channel that we have obtained before. The tunneling width at the source and drain junctions can be expressed as

$$\begin{aligned} W_{t,min} &= x\left(V_{S0} + {}^{E_g}/_{q}\right) - x\left(V_{S0}\right) = \\ &\quad x_{sc} - \lambda. \cosh^{-1}\left(\frac{V_{D(eff)} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right), \end{aligned} \quad (12)$$

$$\begin{aligned} W_{t,min} &= x\left(\phi_{ch}\right) - x\left(\phi_{ch} - {}^{E_g}/_{q}\right) = \\ &\quad \lambda \cosh^{-1}\left(\frac{V_{S0} + {}^{E_g}/_{q} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right). \end{aligned} \quad (13)$$

where $W_{t,min}$ and $W_{t,max}$ are the minimum and maximum tunnel width along the lateral tunnel path at the source-channel junction (the source-channel and

channel-drain tunneling width are schematically depicted in Fig. 2). Regarding Kane's model [22], the tunneling current can be calculated by integrating the tunneling probability over the effective tunneling length,

$$I_{tunnel,S\to C} = q.W. \int_{W_{t,min}}^{W_{t,max}} \int_{0}^{t_{si}} G_{Kane} dydx. \tag{14}$$

In (14), G_{Kane} is the Kane's tunneling probability factor. The tunneling current at the drain junction can be calculated similarly,

$$I_{tunnel,C\to D} = q.W. \int_{W'_{t,min}}^{W'_{t,max}} \int_{0}^{t_{si}} G_{Kane} dydx, \tag{15}$$

$$W'_{t,min} = x\left(V_{D(eff)}\right) - x\left(V_{D(eff)} - {}^{E_g}/_{q}\right), \tag{16}$$

$$W'_{t,max} = x\left(\phi_{ch} + {}^{E_g}/_{q}\right) - x\left(\phi_{ch}\right). \tag{17}$$

where, $W'_{t,min}$ and $W'_{t.max}$ are minimum and maximum of the lateral path at the channel-drain junction. Finally, the total value of the device output current can be expressed as,

$$I_{DS} = I_{tunnel,S\to C} + I_{tunnel,C\to D}. \tag{18}$$

2.3. Dipole Polarization

The value of the dipole polarization in each step depends on the previous history of the ferroelectric electric field. Thus the polarization is determined by integrating $dP_d(E_f)/dE_f$ from a specified initial condition. Since this form has been extensively discussed before for arbitrary field histories [18], the results are simply stated here. The saturated polarization hysteresis loop is defined by

$$P^{+}_{sat}(E_f) = P_s \tanh(\frac{E_f - E_C}{2\delta}), P^{-}_{sat} = -P^{+}_{sat}(-E), \tag{19}$$

where

$$\delta = E_c \left[\ln\left(\frac{1 + {}^{P_r}/_{P_s}}{1 - {}^{P_r}/_{P_s}}\right)\right],^{-1} \tag{20}$$

and + (or −) superscript signifies the positive (or negative) going branch of the loop. The derivative of the polarization is given by the following equations:

$$\frac{dP_d}{dE_f} = \Gamma \frac{dP_{sat}}{dE_f}, \tag{21}$$

$$\Gamma = 1 - \tanh\left[\left(\frac{P_d - P_{sat}}{\xi P_s - P_d}\right)^{1/2}\right]. \tag{22}$$

where $\xi = +1$ when $dE/dt > 0$ and $\xi = -1$ when $dE/dt < 0$.

The given equations express the FeTFET drain current as a function of the gate voltage history, device geometry, and material properties. In the following section, we will present a numerical analysis technique in order to obtain the FeTFET transfer characteristic.

2.4. Numerical Analysis Technique

Since the ferroelectric polarization depends on the history of the electric field, the drain current is calculated as a function of the applied gate voltage. The polarization can be obtained by integrating from a known value. For the first step, we should define the initial values for the gate voltage and the polarization. Note that the initial conditions must satisfy the physical requirement that the polarization lies on or within the hysteresis loop. We considered $V_g = V_{fb}$ and $P_d = 0$ as the initial condition. Having the polarization and the gate voltage, all TFET parameters are calculated using (1) to (18). Furthermore, the ferroelectric field and the silicon charge density can be calculated as follows:

$$\sigma_s = -\sqrt{2\epsilon_{si} kT N_{ch}} \left\{ q\frac{\phi_{ch}}{kT} + \left(\frac{n_i}{N_{ch}}\right)^2 \exp\left(q\frac{\phi_{ch} - V}{kT}\right) \right\}^{1/2}, \tag{23}$$

$$E_f = -\frac{\sigma_s + P_d(f)}{\epsilon_0 \epsilon_f}. \tag{24}$$

The approach to performing the integration from the initial conditions to a new set of conditions is to compute the m'th value of the relevant quantities, and numerically integrate. We now introduce subscript m, which signifies that the given quantity is evaluated at the m'th integration increment. First, we should solve equations 1 to 18 to find the m'th value for the surface potential. Then, we calculate the m'th value of the silicon surface charge and the electric field inside the ferroelectric film using equations (23) and (24). The polarization can be depicted as

$$P_d\left(E_{m+1}\right) = P_d\left(E_m\right) + \left(E_{m+1} - E_m\right) \frac{d}{dE} \left[P_d\left(E\right)\right]_{E_m}. \tag{25}$$

Considering (21) and (24), equation (25) can be rewritten as

$$P_d\left(E_{m+1}\right) = \frac{P_d(E_m) - \{[\sigma_s/\epsilon_0\epsilon_f] + E_m\}\left[(d/dE)\, P_d(E)\right]_{E_m}}{1 + (1/\epsilon_0\epsilon_f)\left[(d/dE)\, P_d(E)\right]_{E_m}}. \tag{26}$$

The next value of the polarization in each step can be obtained using (26). Sweeping the gate voltage and calculating the next value of the polarization in each step, we can compute the device surface potential and output current.

The model predicted results were verified by comparing with TCAD simulations. The device surface potential is presented in Fig. (3). First, we confirmed the surface potential in the middle of the channel which is the primary parameter to compute the potential profile and the drain current. The surface potential

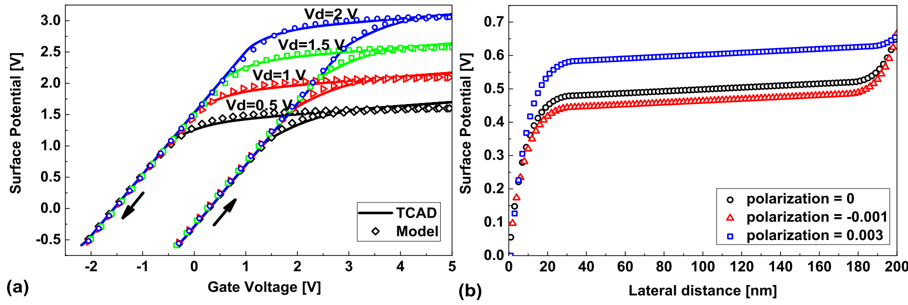

Figure 3: Ferroelectric TFET surface potential. (a) The device surface potential in the middle of the channel for different drain voltages and sweeping the gate voltage. (b) The surface potential profile along the channel and how it changes in the presence of the polarization. The gate voltage is $1V$ and the drain voltage is $1.5V$.

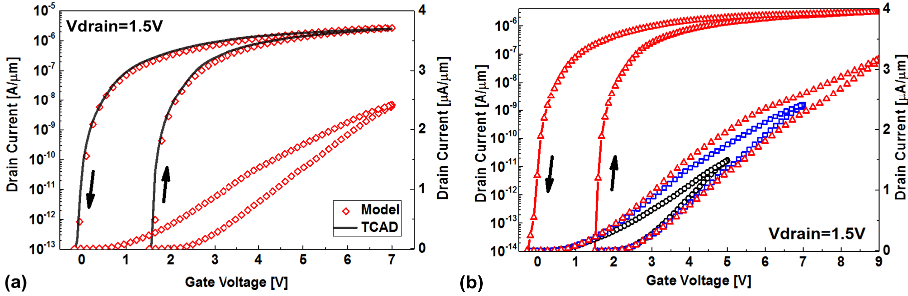

Figure 4: Ferroelectric TFET output current. (a) FeTFET model vs. TCAD results obtained for $1.5V$ drain voltage. (b) FeTFET drain current for different sweeps of the gate voltage.

profile in the middle of the channel for different drain voltages and sweeping the gate voltage is depicted in Fig. 3-(a). Results confirm that our proposed model replicates well with the TCAD simulations. The effect of the dipole polarization on the surface potential profile along the channel is presented in Fig. 3(b). Finally, the output current of the device is shown in Fig. (4). Fig. 4-(a) represents the output current while the drain voltage is $1.5V$. The device's transfer characteristic for $1.5V$ drain voltage and different sweeps of the gate voltage is illustrated in Fig. 4-(b).

3. Memory Window

The memory window (MW), a critical parameter in nonvolatile memories, is the threshold voltage difference between the two states of the device. The memory window should be large enough to ensure a significant retention time and ease of data detection in nonvolatile memory devices. In this section, we discuss the quantitative influence of the parameters that can affect the memory window based on our presented model and theoretically show the silicon doped

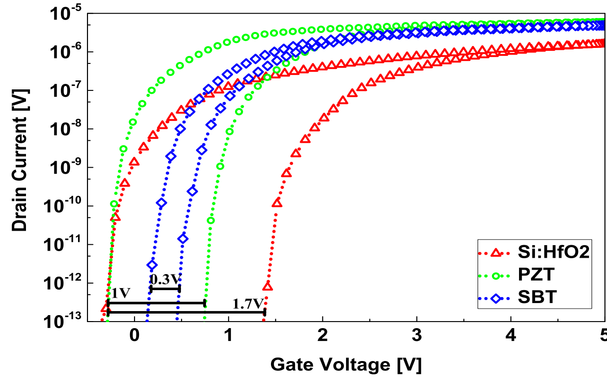

Figure 5: The transfer characteristic of FeTFETs using $10nm$ of PZT, SBT, and Si:HfO_2 as the gate ferroelectric. The device benefits from doped HfO_2 thin film provides larger memory window due to its high coercive field.

HfO_2 can be utilized in highly scaled nonvolatile memories.

3.1. Ferroelectric material

The memory window in a ferroelectric field effect transistor mostly depends on the ferroelectric coercive field and thickness. In this subsection, we compare the effect of the ferroelectric coercive field on the device's memory window using the same thickness of different ferroelectrics. The properties of two well-known perovskite ferroelectrics, Lead Zirconate Titanate (PZT) and Strontium Barium Titanate (SBT), is compared with Si:HfO_2 in Table 1. The recently discovered ferroelectric thin film, Si:HfO_2 [6-8], has a relatively high coercive field that ensures a large memory window.

Table 1: *The ferroelectric properties of PZT, SBT, and Si:HfO_2 [24].*

Ferro Material	$P_r(^{\mu C}/_{cm^2})$	$P_s(^{\mu C}/_{cm^2})$	$E_c(^{MV}/_{cm})$	ϵ_r
PZT	32	40	0.7	250
SBT	8	10	0.3	250
Si:HfO_2	9	9.5	1.1	32

The $I_d - V_g$ curves of FeTFETs are obtained for the same devices using $10nm$ of PZT, SBT, and Si:HfO_2 as the gate ferroelectric (Fig. 5). We used the same thickness of each material to eliminate the influence of the ferroelectric thickness on the MW. The current level difference is due to the different permittivity of the ferroelectric.

Based on the presented results in Fig. 5, Si:HfO_2 theoretically provides larger memory window compared to the well-known ferroelectric materials PZT and SBT. Up to $1.7V$ memory window is obtained for a device using $10nm$ of Si:HfO_2. Besides the theoretical advantages of Si:HfO_2 comparing perovskite ferroelectrics, due to the high relative permittivity of the PZT and SBT (over

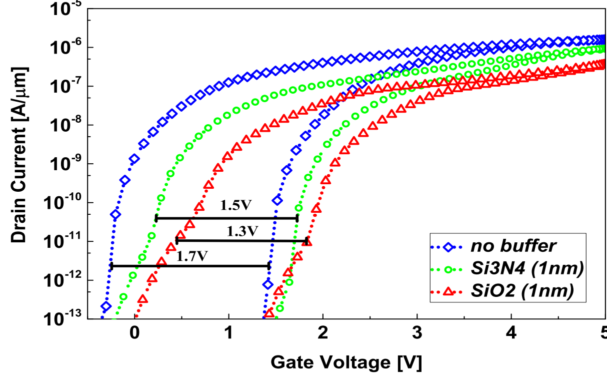

Figure 6: The transfer characteristic of a FeTFET using $10nm$ of Si:HfO$_2$ as the ferroelectric material and $1nm$ of SiO$_2$ and Si$_3$N$_4$ as the buffer layer. The device without buffer layer provides $1.7V$ memory window, $1nm$ of Si$_3$N$_4$ reduces the MW down to $1.5V$, and $1nm$ of SiO$_2$ provides $1.3V$ memory window.

200), it is challenging to fabricate a device with such a thin layer of these ferroelectric materials. Also, CMOS compatibility, scalability and the ability to deposit a high-quality layer by Atomic Layer Deposition (ALD) are some of the technological advantages of using Si:HfO$_2$.

3.2. Buffer layer

Due to the large number of defects, leakage current, and large lattice mismatch between perovskite ferroelectrics and silicon, it is always necessary to use a buffer layer with a proper interface with the substrate. However, the voltage drop over the buffer layer reduces the memory window.

To study the effect of the buffer layer on the MW, we utilized $10nm$ of Si:HfO$_2$ as the ferroelectric dielectric and $1nm$ of SiO$_2$ and Si$_3$N$_4$ as the buffer layer. Results are compared with a device using only $10nm$ of Si:HfO$_2$ as the gate stack in Fig. 6. Employing $1nm$ of SiO$_2$ drops the MW down to $1.3V$, but the device benefits from Si$_3$N$_4$ provides $1.5V$ memory window due to its higher relative permittivity. The negative influence of the buffer layer on the MW can be reduced in the case of high-K materials, but it can never be zero. Here, we highlight another advantage of the Si:HfO$_2$ ferroelectric thin film which is its proper interface with silicon. As a result, the doped HfO$_2$ ferroelectric thin film can be deposited directly on the silicon, and no buffer layer is required.

Besides reducing the memory window, using the buffer layer also increases the subthreshold slope which affects the response time and power dissipation.

3.3. Si:HfO$_2$ thickness

Another important parameter that affects the memory window is the ferroelectric thickness. The ferroelectric strongly affect the MW as it defines the total number of the dipoles. On the other side, the ferroelectric coercive field might change by varying the film thickness, especially in the case of the doped HfO$_2$.

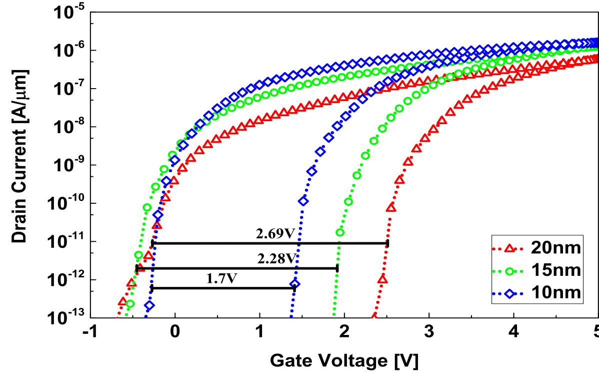

Figure 7: The $I_d - V_g$ curves of the FeTFETs using different thicknesses of Si:HfO_2.

Increasing the films thickness in Si:HfO_2 reduces the coercive field. The ferroelectric properties of the Si:HfO_2 with respect to the film thickness is depicted in Table 2.

Table 2: *The ferroelectric properties of Si:HfO_2 regarding the fims thickness [6-8].*

Thickness	$P_r(^{\mu C}/_{cm^2})$	$P_s(^{\mu C}/_{cm^2})$	$E_c(^{MV}/_{cm})$	ϵ_r
20nm	5.5	5.75	1.00	28.5
15nm	7.25	7.62	1.05	30.25
10nm	9	9.5	1.1	32

The transfer characteristic of the FeTFET using different thicknesses of Si:HfO_2 is illustrated in Fig. 7. Simulation results demonstrate that the coercive field decreases slightly by increasing the thickness, and the impact of the ferroelectric thickness is dominant. So, the device memory window increases by increasing the doped HfO_2 film thickness. $2.7V$ memory window is obtained for a FeTFET with $20nm$ of Si:HfO_2.

4. Nanometer scale FeTFET

Unique properties of the ferroelectric Si:HfO_2 like relatively low dielectric constant, CMOS compatibility, good interface with the silicon [23], and relatively high remanent polarization even in a $5nm$ thick, thin film [16] make it a promising candidate for the fabrication of future nonvolatile memories [6-8].

The Si:HfO_2 allows us to fabricate ferroelectric MOSFETs in nanoscale. However, on the nanometer scale, the high power consumption per area of the chip becomes a challenging issue. To eliminate the power dissipation problem we need to design energy efficient devices with low *off*-current. Tunneling field effect transistors have been proposed as energy efficient devices due to their low *off*-current and subthreshold slope. The FeTFET can be a decent candidate for

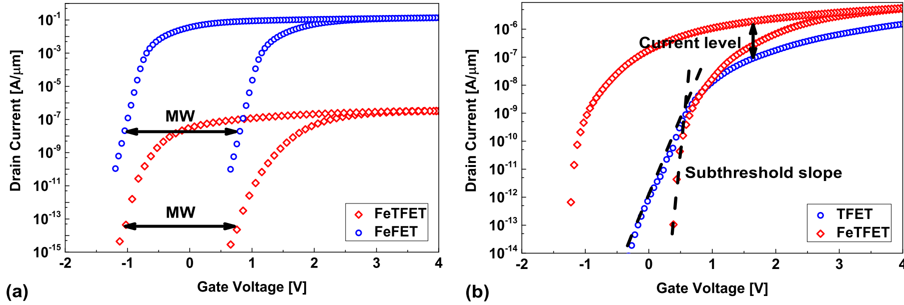

Figure 8: The transfer characteristic of a $28nm$ gate length FeFET vs. FeTFET using $10nm$ of Si:HfO_2 as the ferroelectric dielectric. Results confirm that the FeTFET provides the same memory window as the FeFET. (b) The negative capacitance effect enhances the output current level and subthreshold slope of the FeTFET comparing the conventional TFET.

future nonvolatile memories because of its ability to provide a sufficient memory window with low power dissipation. As we did not consider short channel effects in our model, results of the model may not be reliable for a nanometer scale device. Therefore, we used Sentaurus TCAD commercial simulator for this section.

In Fig. 8-(a), the transfer characteristic of a $28nm$ gate length single gate ferroelectric MOSFET is compared with FeTFET with the same dimensions. $10nm$ of Si:HfO_2 is used as the gate ferroelectric. Regarding the presented results in Fig. 8-(a), FeTFET provides the same memory window as FeFET with lower *off*-current (static power) [24] and also lower *on*-current. However, the TFET low output current is the main disadvantage of this device as it may not be sufficient to drive circuit capacitors. It should be noted that besides the ability of ferroelectrics for data storage, ferroelectric transistors also benefits from the ferroelectrics negative capacitance effect that amplifies the surface potential and boosts the output current [25-26]. In Fig. 8-(b), the $I_d - V_g$ characteristic of a $28nm$ FeTFET with $10nm$ of Si:HfO_2 is compared with a $28nm$ gate length TFET with the same equivalent oxide thickness. As a result of the ferroelectric's negative capacitance, the subthreshold slope of the device is decreased and the drain current is increased significantly. Simulation results show that the FeTFET meets our expectation for a low power random access nonvolatile memory providing sufficient memory window.

5. Conclusions

The device properties of a ferroelectric memory TFET is theoretically investigated. The recently discovered ferroelectric, silicon doped HfO_2, is integrated to the gate stack in order to highlight advantages of this ferroelectric thin film. The FeTFET analytical modeling is achieved by solving Maxwell's first equation (gate stack) in conjunction with Poisson equation (channel). Based on the proposed model, the memory window of the FeTFET is extensively investigated as

a key parameter of nonvolatile memories. Theoretical results represent that the Si:HfO_2 stands as a promising candidate for the future of nonvolatile memory transistors. Besides the outstanding properties of the Si:HfO_2 for the device fabrication, a large memory window is obtained as a result of the integration of the Si:HfO_2 thin film with tunneling field effect transistors. CMOS compatibility, scalability, and having a relatively low dielectric constant in parallel with having a large coercive field guarantee that FeTFETs using silicon doped HfO_2 can be utilized as the low power nanoscale memories.

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