Modeling and Simulation of Low Power Ferroelectric Non-Volatile Memory Tunnel Field Effect Transistors Using Silicon-doped Hafnium Oxide as Gate Dielectric[☆]

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Abstract

The implementation and operation of the nonvolatile ferroelectric memory (NVM) tunnel field effect transistors with silicon-doped HfO_2 is proposed and theoretically examined for the first time, showing that ferroelectric nonvolatile tunnel field effect transistor (Fe-TFET) can operate as ultra-low power nonvolatile memory even in aggressively scaled dimensions. A Fe-TFET analytical model is derived by combining the pseudo 2-D Poisson equation and Maxwell's equation. The model describes the Fe-TFET behavior when a time-dependent voltage is applied to the device with hysteretic output characteristic due to the ferroelectric's dipole switching. The theoretical results provide unique insights into how device geometry and ferroelectric properties affect the Fe-TFET transfer characteristic. The recently explored ferroelectric, silicon-doped HfO_2 is employed as the gate ferroelectric. With the ability to engineer ferroelectricity in HfO_2 thin films, a high-K dielectric well established in memory devices, the silicon-doped HfO_2 opens a new route for improved manufacturability and scalability of future 1-T ferroelectric memories. In the current research, a Si:HfO_2 based Fe-TFET with large memory window and low power dissipation is designed and simulated. Utilizing our presented model, the device characteristics of a Fe-TFET that takes full benefits from Si:HfO_2 is compared with the same devices

[☆]This document is a collaborative effort.

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using well-known perovskite ferroelectrics. Finally, the Fe-TFET is compared with a conventional ferroelectric memory transistor highlighting the advantages of using tunneling memory devices.

Keywords: HfO_2, analytical model, surface potential, ferroelectric, nonvolatile memory, Fe-TFET

1. Introduction

Ferroelectric materials can be utilized as electrically switchable nonvolatile data storage elements as their polarization can change by applying an external electric field. Recently, novel devices called ferroelectric TFETs [1], and ferroelectric FETs have been proposed as promising candidates for future nonvolatile memory applications [2, 3]. In ferroelectric field effect devices, two stable states of the ferroelectric's polarization are used for data storage [4]. Nonvolatile data storage, fast writing, and nondestructive read-out operation have been reported for ferroelectric field effect transistors [5]. However, the industrial implementation of ferroelectric devices especially in nanoscale still missing due to the integration and scaling obstacles of conventionally used perovskite type ferroelectrics such as Lead Zirconate Titanate (PZT). The recently discovered ferroelectricity in HfO_2 thin films [6], enabled CMOS-compatible manufacturing of highly scaled ferroelectric devices down to $28nm$ ground rule [6, 7].

By scaling devices down to the nanoscale, power density becomes a challenging issue as the power density per area of the chip increases. The tunneling field effect transistors have been investigated intensely in recent years [8] due to their considerable potentials for ultra-low power applications [9, 10]. Using the advantages of both ferroelectric thin films for data storage and TFETs as energy efficient devices, it is possible to design a new class of nonvolatile memories, with a relatively large memory window, fast writing, nondestructive read-out operation, and low power consumption. In this work, we propose a comprehensive, quantitative model for investigation of Fe-TFETs. The successful design of a Fe-TFET for nonvolatile data storage requires a thorough understanding of

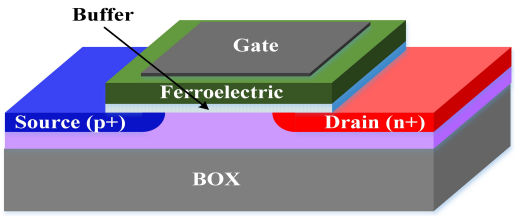

Figure 1: The device schematic of an SOI Fe-TFET where the gate stack of a conventional single gate TFET is replaced with a series combinations of a ferroelectric and a linear dielectric.

the device operation principals. It is necessary to develop an analytical model for Fe-TFETs design optimization. Hence, an analytical model for Fe-TFETs is proposed and verified with Sentaurus TCAD [11] simulation tool. The model is developed by solving the 2-D Poisson equation [12] for a single gate TFET and considering the effect of the ferroelectric polarization on the surface potential. The polarization effect is calculated by solving Maxwell's first equation in the gate stack. A numerical method is employed to calculate the polarization hysteresis for both saturated and nonsaturated hysteresis loops [13]. Based on our proposed model, memory window of the ferroelectric memory TFETs using different ferroelectric materials is investigated. It should be noted that short channel effects are neglected in the proposed model, and a $200nm$ gate length device is utilized for model verification. Finally, a $28nm$ gate length Fe-TFET benefits from Si:HfO_2 as the gate ferroelectric is designed and simulated using Sentaurus TCAD commercial simulator. Results confirm that the proposed device can be employed as the future of nonvolatile memories. Moreover, we present that the ferroelectrics negative capacitance improves the device's output current by boosting the gate potential.

2. Device Modeling

2.1. Approach and Definitions

In this paper, an n-type SOI ferroelectric TFET is studied. The device is schematically depicted in Fig. 1. The length of the channel is $200nm$ to suppress

short channel effects, the doping concentration of the lightly doped channel is $5\times10^{14}cm^{-3}$, the highly doped $p+$ source concentration is $1\times10^{20}cm^{-3}$ and the $n+$ doped drain is $1 \times 10^{18}cm^{-3}$ to eliminate the ambipolar behavior[13]. The silicon-doped HfO_2 is utilized as ferroelectric layer due to its unique property of exhibiting the ferroelectricity even in a $5nm$ thick, thin film [14, 15]. For the model verification, we have used $10nm$ of Si:HfO_2 with $9\mu C/cm^2$ remanent polarization and $1.1MV/cm$ coercive field [6]. We will discuss how the relatively high coercive field and remanent polarization guarantee a large memory window (and retention time) in the Ferroelectric Memory TFET.

To develop the ferroelectric TFET model, we have combined the switching analytical modeling of ferroelectric capacitors [16] with the Band-to-Band Tunneling modeling of TFETs. Wu et al. [12] proposed the analytical modeling of TFETs based on the gate and drain dual modulation effects by solving Poisson equation in the device channel. Miller et al. [17, 13, 18] developed the compact modeling of ferroelectric capacitors that accurately describes the dipole polarization switching by employing Maxwell's first equation. We employed Maxwell and Poisson equations consistently to precisely calculate the surface potential profile along the channel. Finally, the device current is calculated by determining the potential profile around the tunneling junctions. The computer aided design (TCAD) tool Sentaurus is used to verify the proposed model. The non-local band-to-band tunneling (BTBT) model is enabled to account tunneling mechanism [19]. In order to calculate the tunneling probability using the electron-hole wave vector throughout the tunneling path, the non-local model uses Wetzel-Kramer-Brillouin (WKB) approximation. Also, Fermi statistics and Shockley-Reed-Hall (SRH) recombinations are adopted while the gate tunneling is ignored. In order to incorporate the ferroelectric properties of the gate stack, we have enabled Ferro model in our simulations. Moreover, the standard library of Sentaurus TCAD is used for linear dielectrics (where the SiO_2 and Si_3N_4 relative permittivity is 3.9 and 7.5 respectively). These models are considered in all TCAD simulations unless otherwise mentioned. It should be noted that the ferroelectric layer is considered ideal from the point of view of

hysteresis loss related issues like fatigue (loss of switched charge owing to repetitive destructive reads), retention (decreasing the stored charge to a level where the positive and negative state of the polarization cannot be reliably sensed), and direct current breakdown (as a result of applying constant writing voltage) have been neglected [20].

2.2. Model

In this subsection, we describe the relation between the ferroelectric polarization and the silicon surface potential in a metal-ferroelectric-oxide-semiconductor structure [21]. The electrostatic equations are derived starting with Maxwell's equation,

$$\nabla.D = \rho, \tag{1}$$

$$D = \epsilon_0 \epsilon E + P_d, \tag{2}$$

where D is the displacement, ρ is the free charge density, E is the electrical field, ϵ_0 is the vacuum permittivity, ϵ is the linear dielectric constant, and P_d is the contribution of the switching dipoles. Solving (1) and (2) in conjunction with the definition $E = -\nabla\phi$ (ϕ is the electrostatic potential) leads us to:

$$V_{GB} = \phi_s - \frac{\sigma_s}{C_{stack}} - P_d(E_f)\frac{d_f}{\epsilon_0 \epsilon_f}. \tag{3}$$

In (3), C_{stack} describes the gate total capacitance, σ_s is the silicon charge, d_f and ϵ_f are ferroelectric thickness and relative permittivity and ϕ_s is the silicon surface potential. The ferroelectric polarization changes the surface potential by a value of $P_d\,(d_f/\epsilon_0\epsilon_f)$. The ferroelectric polarization can also be calculated using Landau-Khalatnikov (LK) theory [22, 23, 24]. Using Landau theory, (3) can be rewritten as follow:

$$V_{GB} - \phi_s + \frac{\sigma_s}{C_{Buffer}} = (2\alpha t_f)P_d(E_f) + (4\beta t_f)P_d^3(E_f) + (6\gamma t_f)P_d^5(E_f), \tag{4}$$

where α, β, and γ are the ferroelectric Landau parameters, t_f is the ferroelectric thickness, and C_{Buffer} is the capacitance of the buffer layer. The Fe-TFET modeling can be obtained using either (3) or (4). However, (3) is employed in this study to derive a simple analytical model for the device operation.

We explain the Fe-TFET behavior by considering the effect of the polarization on the surface potential for a known polarization. Combining Maxwell's first equation with Wu's analytical solution for TFET surface potential [12], the surface potential in middle of the channel for the whole range of the operation can be given as

$$\begin{aligned}\phi_{ch} &= F + \frac{kT}{q} ln \left\{ \frac{q}{kT} \left[\frac{kT}{q} + \frac{\sqrt{F}}{\sqrt{F}+\gamma} \left(V_{GS} - V_{fb} + P_d \frac{d_f}{\epsilon_0 \epsilon_f} - F \right) + \right. \right. \\ & \left. \left. \frac{1}{2} \left[\frac{F}{(\sqrt{F}+\gamma)^2} - \frac{\gamma \left[F - 2 \right]}{2(\sqrt{F}+\gamma)^3} \right] \left(V_{GS} - V_{fb} + P_d \frac{d_f}{\epsilon_0 \epsilon_f} - F \right)^2 \right] \right\} \quad (5)\end{aligned}$$

$$F = \frac{1}{2} \left\{ V_{DS} + \Phi + \phi_{ch,dep} - \sqrt{\left(\phi_{ch,dep} - V_{DS} - \Phi \right)^2 + \delta^2} \right\}, \quad (6)$$

$$\phi_{ch,dep} = \left\{ \sqrt{V_{GS} - V_{fb} + P_d \frac{d_f}{\epsilon_0 \epsilon_f} + \frac{\gamma^2}{4}} - \frac{\gamma}{2} \right\}^2, \quad (7)$$

where V_{fb} is the flat band voltage, T is the temperature, k is the Boltzmann's constant, q is the electrical charge of a single electron, γ is the body factor defines as $\sqrt{2\epsilon_{si} q N_{ch}}/C_{stack}$ (N_{ch} is the channel doping), δ is a small smoothing factor and $\phi_{ch,dep}$ is the surface potential in the gate control regime [12]. Φ is the required surface potential for sufficient inversion charge to screen the gate modulation and can be expressed as $(kT/q)ln(N_{ch}N_{inv}/n_i^2)$, and N_{inv} is the required inversion charge density to screen the gate voltage.

An accurate expression of the surface potential profile around the tunnel junction is needed to calculate the tunneling current. We use the pseudo 2-D Poisson equation to obtain the potential profile along the channel [25]. The parabolic approximation of the potential in a direction normal to the surface is adopted so that the Poisson equation can be reduced to the well-known form

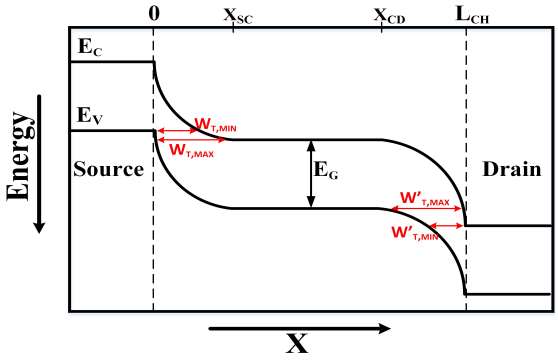

Figure 2: The energy bands in a tunneling field effect transistor indicating the maximum and minimum of the tunneling width in the source-channel and channel-drain junctions [12]. X_{SC} and X_{CD} represent the source and drain tunneling junction width.

$$\frac{d^2\phi_s(x)}{dx^2} - \frac{\phi_s(x) - \left(V_{GS} - V_{fb} + P_d\frac{d_f}{\epsilon_0\epsilon_f}\right)}{\lambda^2} = \frac{qN_{ch}}{\epsilon_{si}}, \tag{8}$$

where $\lambda = \sqrt{\epsilon_{si}t_{si}/C_{stack}}$ (t_{si} and ϵ_{si} represent the silicon thickness and relative permittivity) is the characteristic length of the channel [12]. Solving (8) by considering the boundary conditions and the continuity of potential and electric field at the source-channel and channel-drain junctions, the surface potential profile around tunneling junctions can be obtained as

$$\phi_s(x) = \left(V_{GS(eff)}\right) + \left(\phi_{ch} - V_{GS(eff)}\right)\cosh\left(\frac{x - x_{sc}}{\lambda}\right) \cdots 0 \le x \le x_{sc}, \tag{9}$$

$$\phi_s(x) = \left(V_{GS(eff)}\right) + \left(\phi_{ch} - V_{GS(eff)}\right)\cosh\left(\frac{x - x_{sd}}{\lambda}\right) \cdots x_{cd} \le x \le L_{ch}, \tag{10}$$

$$x_{sc} = \lambda\cosh\left(\frac{V_{S0} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right), \tag{11}$$

$$x_{cd} = L_{ch} - \lambda.\cosh^{-1}\left(\frac{V_{D(eff)} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right). \tag{12}$$

In the performed equations, V_{S0} subscribes to the source potential, $V_{D(eff)}$ is the potential in the drain region ($V_{D(eff)} = V_{S0} + V_{bi,SD} + V_{DS}$), $V_{GS(eff)}$ is the gate effective voltage ($V_{GS(eff)} = V_{GS} - V_{fb} + P_d(d_f/\epsilon_0\epsilon_f) - (qN_{ch}/\epsilon_{si})\lambda^2$), and ϕ_{ch} is the surface potential in the center of the channel that we have derived before. The tunneling width at the source junction can be expressed as

$$\begin{aligned} W_{t,min} &= x\left(V_{S0} + \frac{E_g}{q}\right) - x\left(V_{S0}\right) = \\ & x_{sc} - \lambda.\cosh^{-1}\left(\frac{V_{D(eff)} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right), \end{aligned} \tag{13}$$

$$\begin{aligned} W_{t,max} &= x\left(\phi_{ch}\right) - x\left(\phi_{ch} - \frac{E_g}{q}\right) = \\ & \lambda\cosh^{-1}\left(\frac{V_{S0} + \frac{E_g}{q} - \left(V_{GS(eff)}\right)}{\phi_{ch} - \left(V_{GS(eff)}\right)}\right). \end{aligned} \tag{14}$$

where $W_{t,min}$ and $W_{t,max}$ are the minimum and maximum of the tunneling width along the lateral tunneling path at the source-channel junction (the source-channel and channel-drain tunneling widthes are schematically depicted in Fig. 2). Regarding Kane's model [26], the tunneling current can be calculated by integrating the tunneling probability over the effective tunneling length,

$$I_{tunnel,S\to C} = q.W.\int_{W_{t,min}}^{W_{t,max}}\int_{0}^{t_{si}} G_{Kane}dydx. \tag{15}$$

In (15), G_{Kane} is the Kane's tunneling probability factor. The tunneling current at the drain junction can be calculated similarly,

$$W_{t,min}^{'} = x\left(V_{D(eff)}\right) - x\left(V_{D(eff)} - \frac{E_g}{q}\right), \tag{16}$$

$$W_{t,max}^{'} = x\left(\phi_{ch} + \frac{E_g}{q}\right) - x\left(\phi_{ch}\right). \tag{17}$$

$$I_{tunnel,C\to D} = q.W. \int_{W'_{t,min}}^{W'_{t,max}} \int_{0}^{t_{si}} G_{Kane} dy dx, \tag{18}$$

where, $W'_{t,min}$ and $W'_{t.max}$ are minimum and maximum of the lateral path at the channel-drain junction. Finally, the total value of the device output current can be expressed as,

$$I_{DS} = I_{tunnel,S\to C} + I_{tunnel,C\to D}. \tag{19}$$

2.3. Dipole Polarization

The value of the dipole polarization in each step is a function of the history of the applied electric field. Therefore, the polarization is determined by integrating $dP_d(E_f)/dE_f$ from a specified initial condition. Since this form has been extensively discussed before for the arbitrary field histories [17], the results are simply stated here. The saturated polarization hysteresis loop is defined by

$$P^+_{sat}(E_f) = P_s \tanh(\frac{E_f - E_C}{2\delta}), P^-_{sat} = -P^+_{sat}(-E), \tag{20}$$

where

$$\delta = E_c \left[\ln \left(\frac{1 + \frac{P_r}{P_s}}{1 - \frac{P_r}{P_s}} \right) \right], ^{-1} \tag{21}$$

and + (or −) superscript signifies the positive (or negative) going branch of the loop. The derivative of the polarization is given by the following equations:

$$\frac{dP_d}{dE_f} = \Gamma \frac{dP_{sat}}{dE_f}, \tag{22}$$

$$\Gamma = 1 - \tanh \left[\left(\frac{P_d - P_{sat}}{\xi P_s - P_d} \right)^{\frac{1}{2}} \right]. \tag{23}$$

where $\xi = +1$ when $dE/dt > 0$ and $\xi = -1$ when $dE/dt < 0$.

Considering (1) to (19), the Fe-TFET drain current can be calculated as a function of the gate voltage history, device geometry, and material properties

while the dipole polarization can be obtained using (20) to (23). In the following section, we will present a numerical analysis technique in order to obtain the Fe-TFET transfer characteristic.

2.4. Numerical Analysis Technique

Since the ferroelectric polarization depends on the history of the electric field, the polarization can be obtained by integrating from a known value. For the first step, we should define the initial values for the gate voltage and the polarization. Note that the initial conditions must satisfy the physical requirement that the polarization lies on or within the hysteresis loop. We considered $V_g = V_{fb}$ and $P_d = 0$ as the initial condition. Having the polarization and the gate voltage, all TFET parameters are calculated using (1) to (19). Furthermore, the ferroelectric field and the silicon surface charge density can be calculated as follows:

$$\sigma_s = -\sqrt{2\epsilon_{si}kTN_{ch}}\left\{q\frac{\phi_{ch}}{kT} + \left(\frac{n_i}{N_{ch}}\right)^2 \exp\left(q\frac{\phi_{ch}-V}{kT}\right)\right\}^{\frac{1}{2}}, \tag{24}$$

$$E_f = -\frac{\sigma_s + P_d(f)}{\epsilon_0\epsilon_f}. \tag{25}$$

The approach to perform the integration from the initial conditions to a new set of conditions is to compute the m'th value of the relevant quantities, and numerically integrate. We now introduce subscript m, which signifies that the given quantity is evaluated at the m'th integration increment. First, we should solve equations (1) to (19) to find the m'th value of the surface potential. Then, we calculate the m'th value of the silicon surface charge and the electric field inside the ferroelectric film using equations (24) and (25). The polarization can be expressed as

$$P_d\left(E_{m+1}\right) = P_d\left(E_m\right) + \left(E_{m+1} - E_m\right)\frac{d}{dE}\left[P_d\left(E\right)\right]_{E_m}. \tag{26}$$

Considering (22) and (25), equation (26) can be rewritten as

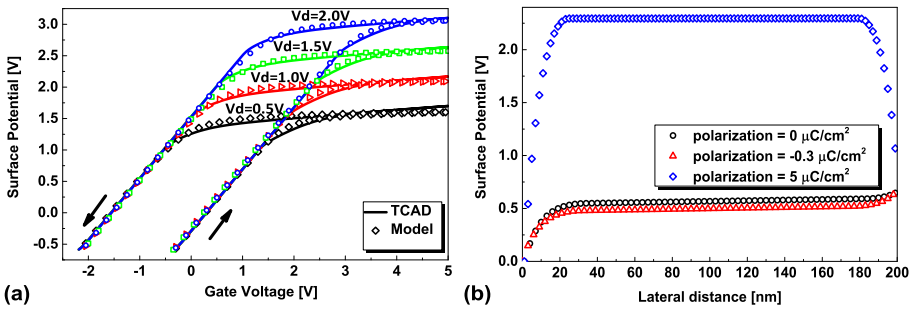

Figure 3: Ferroelectric TFET surface potential. (a) The model verification of the surface potential in the middle of the channel using different drain voltages and sweeping the gate voltage with Sentaurus TCAD simulations results. (b) The surface potential profile along the channel with the polarization as a parameter. Results are obtained using the proposed model for a device with $V_G = 1V$, $V_D = 1.5V$, and considering the gate oxide has 0, -0.003, and $0.05C/m^2$ polarization to illustrate how the positive and negative values of the polarization affect the potential profile.

$$P_d\left(E_{m+1}\right) = \frac{P_d(E_m) - \left\{\left[\frac{\sigma_s}{\epsilon_0 \epsilon_f}\right] + E_m\right\}\left[\left(\frac{d}{dE}\right) P_d(E)\right]_{E_m}}{1 + \left(\frac{1}{\epsilon_0 \epsilon_f}\right)\left[\left(\frac{d}{dE}\right) P_d(E)\right]_{E_m}}. \tag{27}$$

The next value of the polarization in each step can be obtained using (27). Sweeping the gate voltage and calculating the next value of the polarization in each step, the drain current is calculated as a function of the gate voltage.

The model predicted results were verified by comparing with TCAD simulation resuls. The device surface potential is presented in Fig. (3). First, we verified the surface potential in the middle of the channel which is the primary parameter to compute the potential profile and the drain current. The surface potential profile in the middle of the channel for different drain voltages and sweeping the gate voltage is illustrated in Fig. 3-(a). Results confirm that our proposed model replicates well with the TCAD simulations. The effect of the dipole polarization on the surface potential profile along the channel is presented in Fig. 3(b). The surface potential profile is calculated for a TFET with $1V$ gate voltage and $1.5V$ drain voltage considering the gate oxide performs no ferroelectricity, ferroelectric with $-0.003C/m^2$, and $0.05C/m^2$ values of polarization to

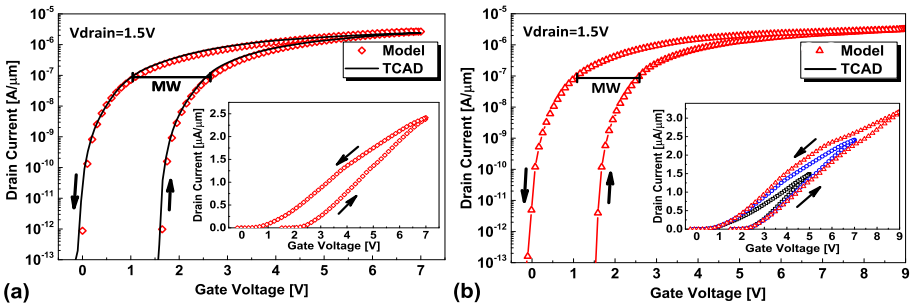

Figure 4: The ferroelectric TFET transfer characteristic for differnet drain and gate voltages. (a) The Fe-TFET model vs. TCAD results obtained for $1.5V$ drain voltage. (b) Fe-TFET drain current for different sweeps of the gate voltage.

illuminate the effect of the positive and negative values of the polarization on the potential profile. Finally, the output current of the device is shown in Fig. (4). Fig. 4-(a) represents the output current while the drain voltage is $1.5V$. The device's transfer characteristic for $1.5V$ drain voltage and different sweeps of the gate voltage is illustrated in Fig. 4-(b).

3. Memory Window

The memory window (MW), a critical parameter in nonvolatile memory devices, is the threshold voltage difference between the two states of the device. Here, the constant current method at $10^{-7}A/um$ is utilized for threshold voltage extraction [27]. The memory window should be large enough to ensure a significant retention time and ease of data detection in nonvolatile memories. In this section, we discuss the quantitative influence of different device parameters that affect the memory window based on our presented model and theoretically highlight the advantages of the silicon-doped HfO_2 ferroelectric thin film.

3.1. Ferroelectric material

It is well known that a Fe-FET memory window while the ferroelectric layer contains a sufficient remanent polarization and having the electric field higher than the material's coercive field mostly depends on the ferroelectric coercive

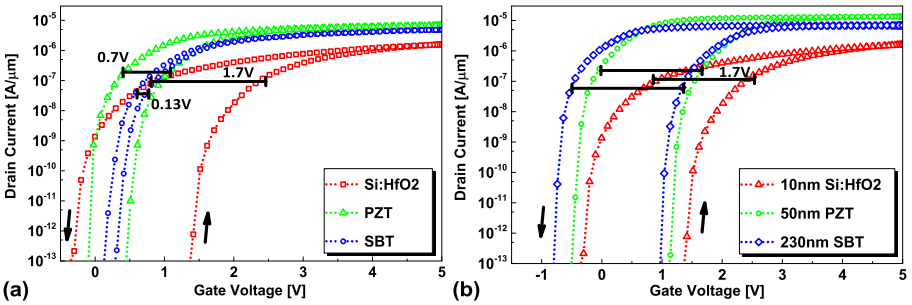

Figure 5: (a) The transfer characteristic of Fe-TFETs using $10nm$ of PZT, SBT, and Si:HfO_2 as the gate ferroelectric obtained by our proposed model. The device benefits from doped HfO_2 thin film provides larger memory window due to its high coercive field while all ferroelectrics has the same thickness. (b) The transfer characteristic of FeTFETs using different thicknesses of mentioned ferroelectric materials providing the same memory window. $10nm$ of Si:HfO_2, $50nm$ of PZT, and $230nm$ of SBT are required to provide $1.7V$ memory window.

field and thickness. In this subsection, we investigate the effect of the ferroelectric coercive field on the Fe-TFET memory window using the same thickness of different ferroelectrics. The properties of two well-known perovskite ferroelectrics, Lead Zirconate Titanate (PZT) and Strontium Barium Titanate (SBT), is compared with Si:HfO_2 in Table 1. The recently discovered ferroelectric thin film, Si:HfO_2 [28, 6], has a relatively high coercive field that ensures a large memory window [29, 30, 31, 32]*[33, 34, 35, 36, 37, 38, 39]*.

Table 1: *The ferroelectric properties of PZT [29, 30, 31, 32], SBT [33, 34, 35, 36, 37, 38, 39], and Si:HfO_2 [28].*

Ferro Material	$P_r(\frac{\mu C}{cm^2})$	$P_s(\frac{\mu C}{cm^2})$	$E_c(\frac{MV}{cm})$	ϵ_r
PZT	32	40	0.26	250
SBT	8	15	0.08	250
Si:HfO_2	9	9.5	1.1	32

The $I_d - V_g$ characteristics of a Fe-TFET using $10nm$ of PZT, SBT, and Si:HfO_2 are depicted in Fig. 5-(a). We have used the same thickness of each material to eliminate the influence of the ferroelectric thickness on the MW. The Fe-TFET that is using PZT or SBT as the gate ferroelectric provides higher

current level due to their higher relative permittivity comparing Si:HfO_2. The high dielectric constant of PZT and SBT reduces the voltage drop across the ferroelectric layer and enhances the silicon surface potential. Therefore, considering (11)-(14), the tunneling width at the source and drain tunneling junctions increases which lead to the improved tunneling current.

Based on the presented results in Fig. 5-(a), Si:HfO_2 theoretically provides larger memory window compared to the well-known ferroelectric materials PZT and SBT. Up to $1.7V$ memory window is obtained for a device using $10nm$ of Si:HfO_2. In Fig. 5-(b) different thicknesses of PZT and SBT are used to maintain the same memory window as the Fe-TFET using $10nm$ of Si:HfO_2. $50nm$ of PZT and $230nm$ of SBT is required to provide $1.7V$ memory window while $10nm$ of silicon-doped HfO_2 grant the same memory window. The theoretical results provide a great insight into the benefits of the silicon-doped HfO_2 ferroelectric thin film. Besides the theoretical advantages of Si:HfO_2 comparing perovskite ferroelectrics, due to the high relative permittivity of the PZT and SBT (over 200), it is challenging to fabricate a device with a thin layer of perovskites ferroelectrics. Moreover, CMOS compatibility, scalability and the ability to deposit a high-quality layer by Atomic Layer Deposition (ALD) are some of the technological advantages of using Si:HfO_2.

The presented MWs in Fig. 5 are lower than the theoretical maximum of the ferroelectric field effect devices memory window ($\sim 2E_c \times d$ which is $2.2V$ in the case of $10nm$ Si:HfO_2) due to the depolarization field and gate leakage current effects. The depolarization field always exists in a ferroelectric capacitor due to the finite dielectric constant of the semiconductor that causes incomplete charge compensation. Moreover, the injected electrons from the gate and semiconductor to the ferroelectric layer lead to the local charge compensation and reducing polarization [40].

3.2. Buffer layer

Due to the large number of defects, leakage current, and large lattice mismatch between perovskite ferroelectrics and silicon, it is always necessary to use

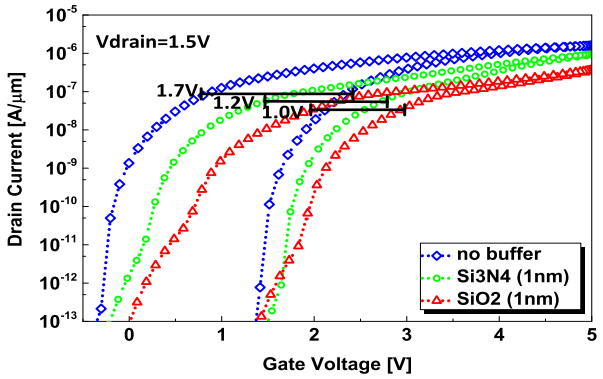

Figure 6: The output characteristic of a Fe-TFET using $10nm$ of Si:HfO_2 as the gate stack with devices using $10nm$ of Si:HfO_2 and $1nm$ of SiO_2 and Si_3N_4 as the buffer layer. The device without buffer layer provides $1.7V$ memory window, $1nm$ of Si_3N_4 reduces the MW down to $1.2V$, and $1nm$ of SiO_2 provides $1.0V$ memory window. The presented results are derived by employing the proposed model.

a buffer layer with a proper interface with the substrate. However, the voltage drop over the buffer layer reduces the memory window.

To study the effect of the buffer layer on the MW, we utilized $10nm$ of Si:HfO_2 as the ferroelectric dielectric and $1nm$ of SiO_2 and Si_3N_4 as the buffer layer. Results are compared with a device using only $10nm$ of Si:HfO_2 as the gate stack in Fig. 6. Employing $1nm$ of SiO_2 drops the MW to $1.0V$ while the use of $1nm$ of Si_3N_4 reduces the memory window to $1.2V$ as the voltage drop over the buffer layer reduces the ferroelectric voltage (electric field). The voltage drop over the buffer layer is considerable as SiO_2 and Si_3N_4 have lower relative permittivity comparing to the ferroelectric layer. Reducing ferroelectric voltage results in the formation of minor polarization hysteresis loops instead of the saturation polarization loop that reduces the memory window significantly [16, 13]. Moreover, the presence of the buffer layer reduces the silicon surface potential results in low energy carriers and insufficient tunneling through the source and drain tunneling barriers that lead to the deformation of the transfer characteristic and reduced saturation current. The negative influence of the buffer layer can be reduced in the case of high-K materials that lowers the

voltage drop across this layer, but it can never be zero. In this subsection, we emphasize on another advantage of Si:HfO_2 which is its proper interface with silicon. Therefore, the doped HfO_2 thin film can be deposited directly on the silicon, and no buffer layer is required. However, it should be noted that a thin layer of HfSiO forms at the interface during the deposition and annealing of the Si:HfO_2 which is called the dead layer. The dead layer performs no ferroelectricity, and it behaves like a buffer layer causing reduced memory window [6, 28]. As the dead layer is a related issue for all ferroelectric materials we have neglected this effect in our simulations.

Besides reducing the memory window, presence of the buffer layer also increases the subthreshold slope affecting the response time and power dissipation.

3.3. Ferroelectric thickness

Another important parameter that greatly affects the memory window is the ferroelectric thickness. The ferroelectric thickness strongly affects the MW as it specifies the total number of the dipoles ($MW \sim 2E_c \times d$ where E_c and d are the ferroelectric coercive field and thickness relatively [40]). Furthermore, the ferroelectric coercive field might change by varying the film thickness, especially in the case of the doped HfO_2. Increasing the films thickness in Si:HfO_2 reduces the coercive field. The ferroelectric properties of the Si:HfO_2 regarding the film thickness is depicted in Table 2.

The transfer characteristic of the Fe-TFET using different thicknesses of Si:HfO_2 is illustrated in Fig. 7. The coercive field slightly reduces by increasing the silicon-doped HfO_2 thickness. However, simulation results confirm that the

Table 2: *The ferroelectric properties of Si:HfO_2 regarding the fims thickness [6, 28].*

Thickness	$P_r(\frac{\mu C}{cm^2})$	$P_s(\frac{\mu C}{cm^2})$	$E_c(\frac{MV}{cm})$	ϵ_r
20nm	5.5	5.75	1.00	28.5
15nm	7.25	7.62	1.05	30.25
10nm	9	9.5	1.1	32

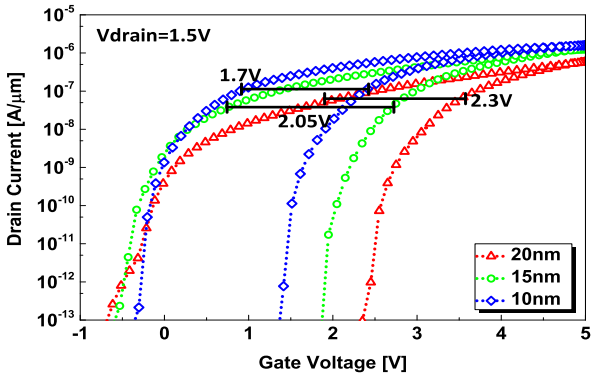

Figure 7: The $I_d - V_g$ curves of the Fe-TFETs using different thicknesses of Si:HfO_2. Results are obtained using our proposed model.

effect of the film thickness is dominant and the memory window enhances significantly by increasing the ferroelectric thickness. Up to $2.7V$ memory window is obtained for a device benefits from a $20nm$ layer thick Si:HfO_2.

4. Nanometer scale Fe-TFET

Unique properties of the ferroelectric Si:HfO_2 like relatively low dielectric constant, CMOS compatibility, good interface with the silicon [7], and relatively high remanent polarization even in a $5nm$ thick, thin film [15] make it a promising candidate for the fabrication of future nonvolatile memories [28, 6].

The unique properties of Si:HfO_2 allows us to fabricate ferroelectric MOSFETs down to the nanoscale. However, on the nanometer scale, the high power consumption per area of the chip becomes a challenging issue. To eliminate the power dissipation problem we need to design energy efficient devices with low *off*-current. Tunneling field effect transistors have been proposed as energy efficient devices due to their low *off*-current and steep *off* to *on* transition. The Fe-TFET can be a decent candidate for future nonvolatile memories due to its ability to provide a sufficient memory window with low power dissipation. As we did not consider short channel effects in our model, results of the model may not be reliable for a nanometer scale device. Therefore, Sentaurus TCAD com-

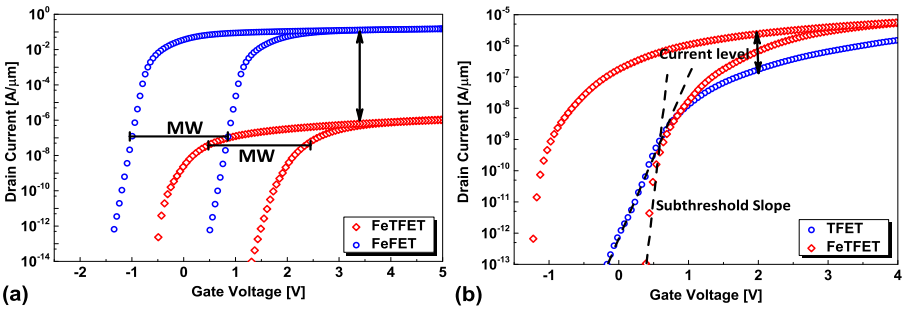

Figure 8: (a) The transfer characteristic of a $28nm$ gate length FeFET vs. Fe-TFET using $10nm$ of Si:HfO_2 as the ferroelectric. The drain voltage is considered $1V$ for all simulations which is the supply voltage of the $28nm$ ITRS node. Results confirm that the Fe-TFET provides the same memory window as the FeFET with lower power consumption. (b) The negative capacitance effect enhances the output current level and subthreshold slope of the Fe-TFET comparing the conventional TFET. Results are obtained using Sentaurus TCAD commercial simulator.

mercial simulator is employed for design and simulation of a $28nm$ gate length Fe-TFET.

In Fig. 8-(a), the transfer characteristic of a $28nm$ gate length single gate ferroelectric MOSFET is compared with Fe-TFET with the same dimensions. $10nm$ of Si:HfO_2 is used as the gate ferroelectric. Regarding the presented results in Fig. 8-(a), Fe-TFET provides the same memory window as FeFET with lower *off*-current (static power) and also lower *on*-current [40]. However, the TFET low output current is the main disadvantage of this device as it may not be sufficient to drive the circuit capacitors. It should be noted that besides the ability of ferroelectrics for data storage, ferroelectric transistors also benefits from the ferroelectrics negative capacitance effect that amplifies the surface potential and boosts the output current [41, 42]. In Fig. 8-(b), the $I_d - V_g$ characteristic of a $28nm$ Fe-TFET with $10nm$ of Si:HfO_2 is compared with a $28nm$ gate length conventional TFET with the same equivalent oxide thickness. As a result of the negative capacitance effect, the subthreshold slope of the device is decreased, and the drain current is increased significantly. Simulation results illustrate that the Fe-TFET meets our expectation for a low power random

access nonvolatile memory providing sufficient memory window.

5. Conclusions

The analytical modeling of ferroelectric TFETs is developed and examined using Sentaurus TCAD commercial simulator. The model is obtained by solving Maxwell's first equation in conjunction with Poisson equation. Based on the proposed model, the memory window of the Fe-TFET memory devices is extensively investigated as the key parameter of nonvolatile memories. The recently discovered ferroelectric, silicon-doped HfO_2, is integrated into the TFET gate stack in order to highlight the advantages of this ferroelectric thin film. Theoretical results represent that Si:HfO_2 stands as a promising candidate for the future of ferroelectric nonvolatile memories. Besides the outstanding properties of the Si:HfO_2 for the device fabrication, a large memory window is obtained as the result of the integration of this ferroelectric thin film with tunneling field effect transistors. Finally, a $28nm$ gate length Fe-TFET is designed and simulated providing the same MW as a $28nm$ Fe-FET consuming less power dissipation. Results confirm that the Fe-TFET using Si:HfO_2 can be ustilized as the ultra-low power nonvolatile memories. Moreover, the negative capacitnace effect in ferroelectric TFETs can solve the the tunneling devices main issue, low output current, by boosting the surface potential.

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