Condition for the negative capacitance effect in metal-ferroelectric-insulator-semiconductor devices

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Abstract. In this paper we report a complete study of the Negative Capacitance FET where we present the condition for the stabilization of the ferroelectric material in order to achieve the voltage amplification across the active layer. The theory is based on the Landau's theory of ferroelectrics combined with the surface potential model as described by Tsividis. We demonstrate the validity of the presented theory on the devices that we fabricated and measured. It can be observed a very good agreement with the measurements.

Keywords: ferroelectric, test structure, polarization, minor loops, negative capacitance, surface potential, NC-FET, P(VDF-TrFE), PVDF, negative capacitance condition

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1. Introduction

Salahuddin suggested the ferroelectric transistor could provide a new mechanism to amplify the surface potential above the gate voltage due to the negative capacitance effect[1, 2]. Several experiments showed proof of negative capacitance in ferroelectric materials[3, 4]. Recent studies propose a non-hysteretic behavior of negative capacitance FET with subtreshold less than $30mV/dec$ but the device is only in the simulation state[5]. Recently there were reported ferroelectric transistors with under-thermal characteristics that presented[6] both hysteresis and negative capacitance behavior[7–9]. The difference between the reported devices and the Salahuddin proposed transistor was that, due the diffusion[10] of the ferroelectric in the silicon, the insertion of a linear dielectric buffer layer was necessary. The ferroelectric stability condition in order to obtain the negative capacitance effect for this kind of devices was not reported before. This work describes the physical explanation of the stability condition, setting its boundaries based on the electrical and physical properties of the materials used. The condition is based on the basic Maxwell charge equations and the Tsividis model of the MOS transistor. The stated stability condition is then validated with measurements on fabricated devices that presented voltage amplification and hysteresis in the same time. Based on the presented theory, a complete set of equations is reported in order to design a negative capacitance transistor.

2. Negative capacitance condition

In this chapter we present the equation of the metal-ferroelectric-oxide-silicon transistor and we will state the theoretical condition in order for the negative capacitance to appear. First we consider a ferroelectric FET structure as presented in Figure 1.

It is a regular MOS transistor that has 2 dielectrics integrated in the gate stack, one linear and one ferroelectric. We are aiming to obtain the negative capacitance effect. For this we calculate the charge stability of the device. Based on Maxwell's equation, each layer can be defined as a capacitor and the entire gate stack can be considered as an in series combination of capacitors (see Figure 1). By applying a voltage on the gate, on each capacitor there will be the same charge. By applying Maxwell's equation we can obtain the charge distribution of a Ferroelectric FET. The electrical displacement is conserving at the junction of the ferroelectric and of the oxide[11] if we do not consider the trapped charges. Therefore we have the following relations:

$$\begin{aligned} &D_{Fe} = D_{ox}, \\ &\epsilon_0 \frac{V_{Fe}}{t_{Fe}} + P = \epsilon_0 k_{ox} \frac{V_{ox}}{t_{ox}}, \\ &P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - E_{Fe} t_{Fe} \epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} \psi_s. \end{aligned} \tag{1}$$

where D_{Fe} and D_{ox} are the displacement of the ferroelectric respectively the displacement of the oxide, P is the polarization, kox the relative permittivity of the oxide, ψ_s is the surface potential, t_{ox} and t_{Fe} are the thicknesses of the oxide layer respectively the ferroelectric layer, V_{Fe} is the voltage drop on the ferroelectric and V_{ox} is the voltage across the oxide.

Equation (1) presents the charge stability of the system, more precisely at a certain V_g what are the voltages that are settling in each layer.

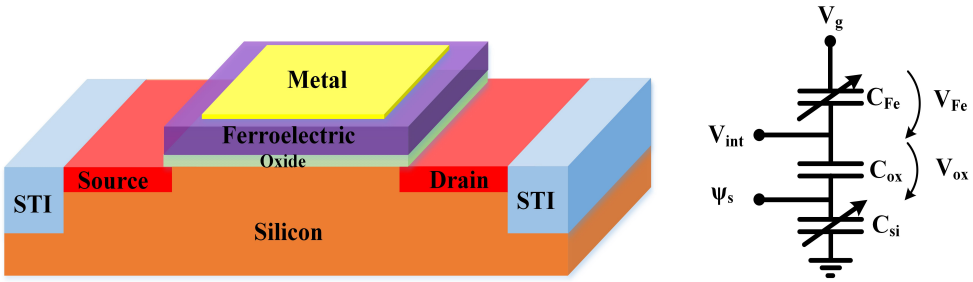

Figure 1. (Left)Generic ferroelectric transistor; (right) equivalent scheme of the gate capacitance. The capacitance of the ferroelectric and the one of the silicon are bias dependent.

In order for the negative capacitance to occur the slope of the charge line that is defined by the equation (1) must be smaller than the negative slope of the ferroelectric polarization as presented in Figure 2 [12].

In the case of the Figure 2a) the charge line is intersecting the polarization in only one point and the entire system is stable, contrary to the case presented in Figure 2b) where the charge line is intersecting the curve in 3 points and it presents instability thus hysteresis. Therefore the condition for stability of the system implying the negative capacitance effect to appear, the slope of the Δ must be smaller than the negative slope of the S shape hysteresis.

In order to calculate the slope of the charge line we must express the surface potential depending on the voltage on the ferroelectric, V_{Fe}. Due to the non-analytical expression of the surface potential, we will study the MOS transistors in different regimes. We will start with **strong inversion**. The surface potential in strong inversion has an almost constant value of $\psi_s = 2\phi_F + 6\phi_t$, where ϕ_F is the Fermi potential and ϕ_t is the thermal voltage.

In this case, based on equation (1) the charge line will have the following formula:

$$\Delta = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - E_{Fe} t_{Fe} \epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} \left(2\phi_F + 6\phi_t \right). \tag{2}$$

The slope of the charge line at a gate voltage that sets the transistor in strong inversion will be:

$$\frac{\partial \Delta}{\partial E_{Fe}} = -t_{Fe} \epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \right). \tag{3}$$

In **accumulation** there will be the same slope of the charge line as in strong inversion due to the fact that the surface potential is having approximately a constant value, minus a few ϕ_t.

Next we will analyze the case of **weak inversion**.

The surface potential in weak inversion can be approximated with a linear function. It is known that in weak inversion and depletion the reverse of the slope of the surface potential with respect to the gate voltage is [13]:

$$n = \left(\frac{d\psi_s}{dV_g} \right)^{-1} = 1 + \frac{\gamma}{2\sqrt{\psi_s}}, \tag{4}$$

where γ is the body factor.

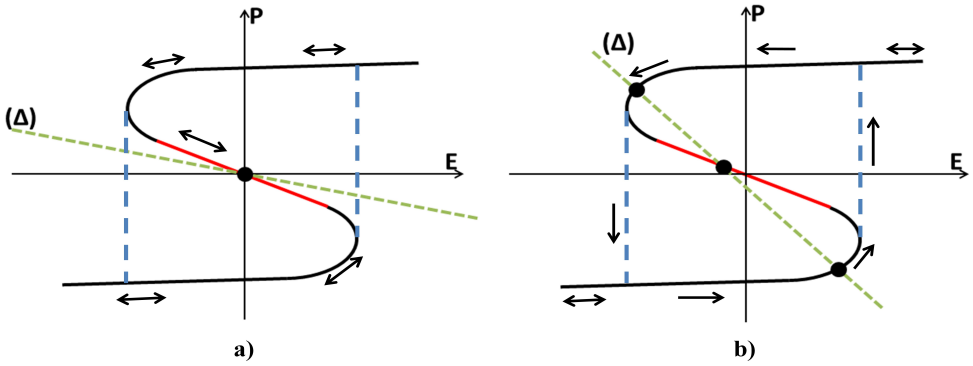

Figure 2. Charge line intersecting the polarization. Condition for stability in a) where no hysteresis is present. In b) the condition for the negative capacitance does not appear and we encounter the hysteresis. Adapted after[10].

The variation of the surface potential is not that powerful, it varies from ϕ_F to around $2\phi_F$ therefore the n does not vary a lot and we can do an approximation and do the average of the slope. Thus we will have an average slope at a value of the surface potential of $2\phi_F$.

$$n = 1 + \frac{\gamma}{2\sqrt{2\phi_F}}. \tag{5}$$

With this approximation we can consider a linear dependence of the surface potential with respect to the gate voltage. Coming back to equation (1) we will have

$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - V_{Fe}\epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}}\right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} \frac{V_{int}}{n}, \tag{6}$$

$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} + \frac{\epsilon_0 k_{ox}}{n t_{ox}} V_g - E_{Fe} t_{Fe} \epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \left(1 - \frac{1}{n}\right)\right). \tag{7}$$

The equation (7) describes the charge line for the NC-MOS transistor that is biased at a gate voltage that puts the transistor in weak inversion. Next we can calculate the slope of the charge line:

$$\frac{\partial \Delta}{\partial E_{Fe}} = -\epsilon_0 t_{Fe} \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \left(1 - \frac{1}{n}\right)\right). \tag{8}$$

This last result from equation (8) shows that the slope of the charge line is not constant at all gate voltages, meaning that the slope of the surface potential with respect to the voltage between the oxide and the ferroelectric is influencing the slope of the charge line. The $1/n$ parameter depends on the fabrication parameters. The slope of the charge line gets lower as the $1/n$ parameter gets higher implying that having a transistor that is switching faster will constitute an advantage in achieving negative capacitance.

In **depletion** the surface potential cannot be approximated with a linear function and the charge line will become a second degree equation. Again the important factor is the slope of the parabola. In order to have continuity, the slope of the line depending on the voltage must be

continuous and monotone therefore we can state that the charge line slope is high in accumulation, in depletion and weak inversion lowers gradually and in inversion is increasing again.

The charge line in all cases was calculated by approximating the surface potential. In accumulation and strong inversion the surface potential was considered constant, but actually there is a small variation with the gate voltage and in weak inversion it was considered depending linearly of the gate voltage. The slope was given by the $1/n$ parameter that we have considered to be constant but in reality is quasi-constant, as it varies from $n = 1 + \frac{\gamma}{2\sqrt{\phi_F}}$ to $n = 1 + \frac{\gamma}{2\sqrt{2\phi_F}}$, thus also the slope of the charge line will vary correspondingly in this regime. To achieve improved accuracy we could replace the n term with the derivative of the surface potential with respect to the internal voltage according to eq. (4).

Summarizing the study until now, we have reached the conclusion that the charge line has a changing slope with respect to the gate voltage applied on the gate; more precisely in accumulation the slope of the charge line is high then in depletion and weak inversion the slope is decreasing and again it is increasing in strong inversion reaching the same value as in accumulation.

As we stated in the first part of this study, in order for the negative capacitance to occur, the slope of the charge line must be smaller than the negative slope of the polarization as presented in Figure 2.

Next we will pass to the calculation of the slope of the negative part of the S-shape of the ferroelectric. The S shape hysteresis is defined according to Landau's theory [14]:

$$E = \alpha_0 \left(T - T_c\right) P + B\left(T\right) P^3, \tag{9}$$

where α_0 and $B(T)$ are material parameters, T_c is the currie temperature of the ferroelectric and the T is the temperature.

We will consider just the first order approximation and we will neglect the P^3 term.

$$E = \alpha_0 \left(T - T_c\right) P. \tag{10}$$

Therefore the derivative in the negative region is:

$$\frac{\partial P}{\partial E} = \frac{1}{\alpha_0 \left(T - T_c\right)}. \tag{11}$$

By using this formula together with the charge line slope calculation and putting the condition that the derivative of the polarization with respect to the field in ferroelectric should be higher than the slope of the charge line, we can set the condition for obtaining the negative capacitance effect.

$$\frac{\partial \Delta}{\partial E_{Fe}} \leq \frac{\partial P}{\partial E}. \tag{12}$$

In our measurements we have obtained polarization curves that presents negative capacitance and also hysteresis in the same time.

The slope of the charge line of the NC-MOS transistor is varying with the voltage applied on the gate. In the case we are having the 2 slopes close one to each other (the one of the charge line of the device and the one from the S shape polarization on the ferroelectric), then the stability of the system is not consistent for all gate voltages. At one point, the slope of the charge line reaches the value of the slope of the ferroelectric, the system is reaching equilibrium and the negative capacitance effect will be present; going further with the gate voltage the system, at one point, will exit stability because the slope of the charge line will increase above the one of the ferroelectric.

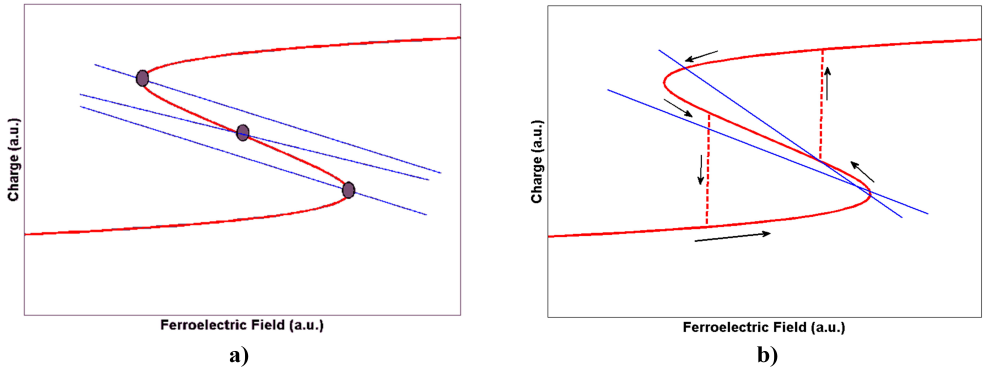

Figure 3. Charge line that is changing slope depending on the operation regime of the ferroelectric transistor. a) The slope of the charge line changes with the bias but the condition for stability remains on the entire range of voltages applied. b) The condition for the stability is fulfilled only on a small interval of applied voltages, this way negative capacitance together with hysteresis can be obtained.

The variation of the slope plus the possibility to obtain hysteresis and negative capacitance effect is qualitatively presented in Figure 3.

A big advantage in order for the negative capacitance to appear will be to have a surface potential derivative big enough so that the charge line slope will be small enough so that the system will be stable. Therefore good transistors with subthreshold slopes closer to $60mV/dec$ will have a larger zone where the negative capacitance can be observed.

3. Experimental verification of the theoretical conditions for negative capacitance

We will verify the stated conditions in the devices that we fabricated, described in[7]. The gate stack is composed by a P(VDF-TrFE) 70:30 and a thin layer of SiO_2. Between the two insulators a layer of Al was introduced in order to have access to the potential between the two. Along with the Al deposition, a layer of Al_2O_3 was formed. The TEM image of the section of the gate and the layer thicknesses are presented in Figure 4.

As presented in [7], the polarization curve is extracted and presented in Figure 5. The Al_2O_3 layer was taken in consideration for the extraction of the polarization. Also, in Figure 5 we present the derivative of the polarization with respect to the ferroelectric electric field in the negative slope of the polarization.

Next, the slope of the PVDF S shape polarization will be calculated.

The $\alpha_0 = 9.02 \times 10^{7\,J.m/C^2K} = 9.02 \times 10^{9\,J.m/cm.V.K}$ [15] and the $T_c = 355^\circ K$ [16] parameter were taken from the literature and we obtain the negative slope of the polarization of the material:

$$\frac{\partial P}{\partial E} = \frac{1}{\alpha_0 \left(T - T_c\right)} = -2.0157 \times 10^{-14} \frac{C}{cm.V}. \tag{13}$$

Figure 6 emphasizes the charge line measured slope (continuous line) and the slope of the calculated S shape polarization (dotted line). Where the slope of the charge line is smaller than the slope of the polarization, the system is stable. The dotted line represents the threshold imposed by the ferroelectric material in order for the system to achieve stability as stated in equation (12).

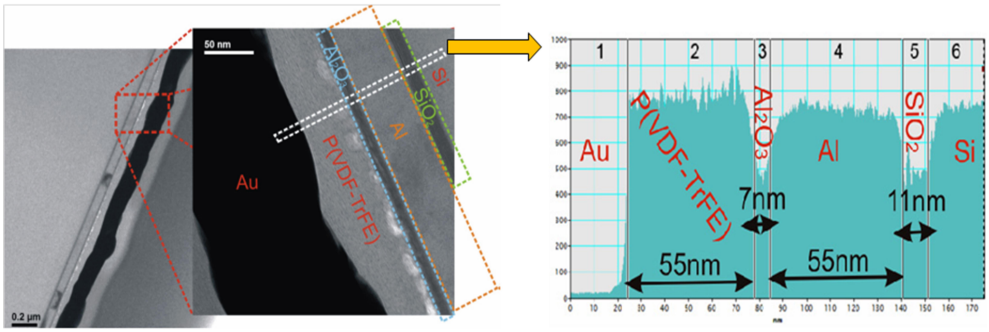

Figure 4. TEM picture and analysis of the layer thicknesses in the gate region.

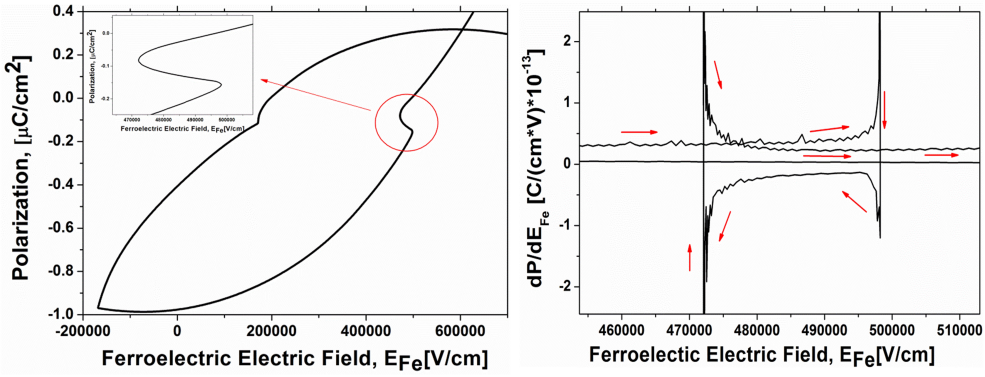

Figure 5. Polarization extracted from measurements and the derivative with respect to the ferroelectric field. The derivative corresponds to the charge line slope.

This result proves very accurately the theory stated in this paper. Even if the threshold of the ferroelectric does not cover all the zone of the negative capacitance, one can observe that it covers the zone where the system is stable. After this limit, noise starts prevailing and the system exits the stability regime.

We have stated that the slope of the charge line is changing according to the derivative of the surface potential with the internal potential.

The surface potential was extracted based on Tsividis model and its derivative was plotted in Figure 7.

Figure 7 shows that the slope of the charge line lowers sufficiently for the negative capacitance effect to occur if the derivative of the surface potential with respect to the internal potential is above a certain value. In our case the value is 0.723. A better MOS, with a subthreshold slope closer to $60mv/dec$, has the derivative of the surface potential closer to 1, meaning that the negative capacitance zone is extended, providing amplification over multiple decades of current.

Another question that arises is why we have not obtained negative polarization also on the other side of the hysteresis. In order for the system to achieve stability, the ferroelectric material

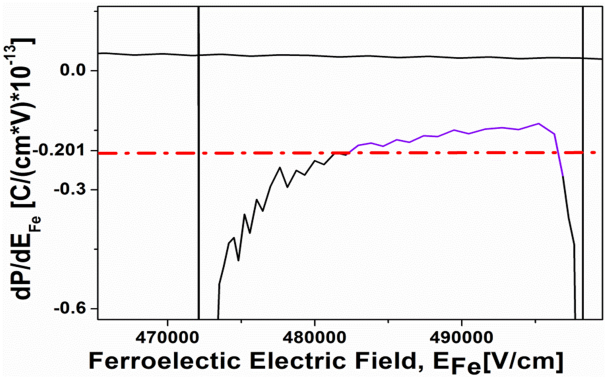

Figure 6. Negative capacitance area where the system reaches stability. This graph illustrates the condition from eq. (12) applied on the measured devices. The continuous line ($\partial P/\partial E$) is the measured value and the dotted line is the theoretical threshold limit calculated from the literature data, eq. (13), in order to achieve negative capacitance. We can observe that above this threshold, the measurement starts to go into an instability regime and the ferroelectric exits the negative capacitance regime.

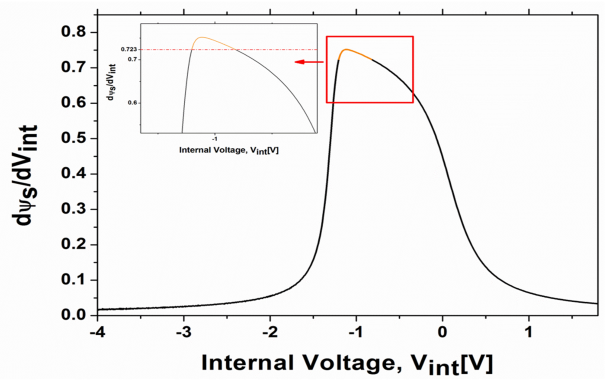

Figure 7. Surface potential derivative with respect to the internal potential. The highlighted zone corresponds to the points where we have obtained the negative capacitance. We can clearly see that the points that corresponds to the negative slope of the polarization are where the derivative of the surface potential has a value higher than 0.723. Better fabricated MOS transistors with a higher derivative of the surface potential with respect to the internal voltage will result a wider area of negative capacitance effect.

must be polarized at a certain value. In our case, due to the thin oxide, we could not fully polarize the material therefore we are exploring the minor loops of the ferroelectric. An inconvenience of this fact is that the ferroelectric curve can shift between two successive measurements as a result of the remained dipoles that are already polarized from the previous measurement. One can observe the asymmetry of the polarization curves towards the negative side.

4. Negative Capacitance - FET design rules

Next we will present a full set of equations in order to obtain negative capacitance devices.

In our case, when the slope of the charge line is slightly higher than the polarization in accumulation and inversion, the negative capacitance effect appears when the slope of the surface potential with respect to the internal potential (potential between the ferroelectric and oxide) is high. We can state theoretically and practically that the negative capacitance appears only in the weak inversion where the slope of the charge line is at minimum. Therefore we are reporting a complete set of equations in order to obtain negative capacitance effect in metal-ferroelectric-oxide-semiconductor devices:

$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} + \frac{\epsilon_0 k_{ox}}{n t_{ox}} V_g - V_{Fe} \epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \left(1 - \frac{1}{n} \right) \right), \tag{14}$$

$$\frac{\partial \Delta}{\partial V_{Fe}} = -\epsilon_0 \left(\frac{1}{t_{Fe}} + \frac{k_{ox}}{t_{ox}} \left(1 - \frac{1}{n} \right) \right) \leq \frac{1}{\alpha_0 \left(T - T_c \right)}, \tag{15}$$

$$n = 1 + \frac{\gamma}{2\sqrt{2\phi_F}},$$

$$\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{\epsilon_{ox}/t_{ox}},$$

$$\phi_F = \phi_t ln \frac{N_A}{n_i}.$$

With this algorithm we have given a complete set of equations in order to design a Negative Capacitance Ferroelectric MOS transistor. The following parameters should be considered (t_{ox}, t_{Fe}, N_A, α_0, T_c, ϵ_{ox}) in order to successfully design a NC-FET.

Having obtained a device that fulfills the negative capacitance condition, the obtained gain of the Fe-FET can be also calculated based on the negative slope of the polarization ($^{dP}/_{dFe}$) and the subthreshold slope of the equivalent MOS transistor under the ferroelectric layer [17]. The voltage amplification of the ferroelectric layer depends on its α_0 parameter, high amplification corresponds to low α_0 and also the condition of stability depends on the same parameter. Higher α_0 corresponds to wider zone of negative capacitance. The condition of stability is highly dependent on the ferroelectric material properties, its thickness and the electrical proprieties of the equivalent MOS transistor. This is the main reason that many trials to measure the negative capacitance had failed [18].

5. Conclusions

In this paper, the negative capacitance condition for the metal-ferroelectric-oxide-semiconductor device was presented. The theory was based on a physical model using basic Maxwell's equations and Tsividis model of the MOS transistor. The condition was verified on measured Fe-MOS devices that presented negative capacitance together with hysteresis. The devices were fabricated with an organic ferroelectric where we could observe voltage amplification and we found a very good agreement with the presented theory. A complete set of equations was presented in order to design a negative capacitance transistor.

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