Double-Gate Negative-Capacitance MOSFET with PZT gate stack on Ultra-Thin Body SOI: an Experimentally Calibrated Simulation Study of Device Performance

Ali Saeidi, Farzan Jazaeri, Igor Stolichnov, and Adrian M. Ionescu

Abstract—In this work, we propose and investigate the high performance and low power design space of non-hysteretic negative capacitance MOSFETs for the 14 nm node based on the calibrated simulations using an experimental gate stack with PZT ferroelectric to obtain negative capacitance effect. All necessary parameters are extracted by carefully characterizing experimentally fabricated ferroelectric capacitors, to ensure realistic simulation results. The ferroelectric thickness obtained by the proposed approach leads to the maximum enhancement in the non-hysteretic operation of negative capacitance transistors. We report a clear and significant double improvement in (i) subthreshold swing and (ii) gate overdrive, using negative capacitance effect. Simulations using Silvaco TCAD coupled with a realistic Landau model of ferroelectrics demonstrates that a 14 nm node UTBB FDSOI-FET can operate at 0.26 V instead of 0.9 V gate voltage using negative capacitance effect, with an average subthreshold swing of 55 mV/decade at room temperature. The double gate structure is proposed to overcome the large mismatch between the ferroelectric and MOS capacitor to enhance the negative capacitance effect and reduce the ferroelectric's optimized thickness. A 14 nm node DG-NCFET can operate at 0.24 V gate voltage with an average subthreshold swing of 45 mV/decade.

Index Terms—negative capacitance, ferroelectric, NCFET, UTBB FDSOI-NCFET, DG-NCFET.
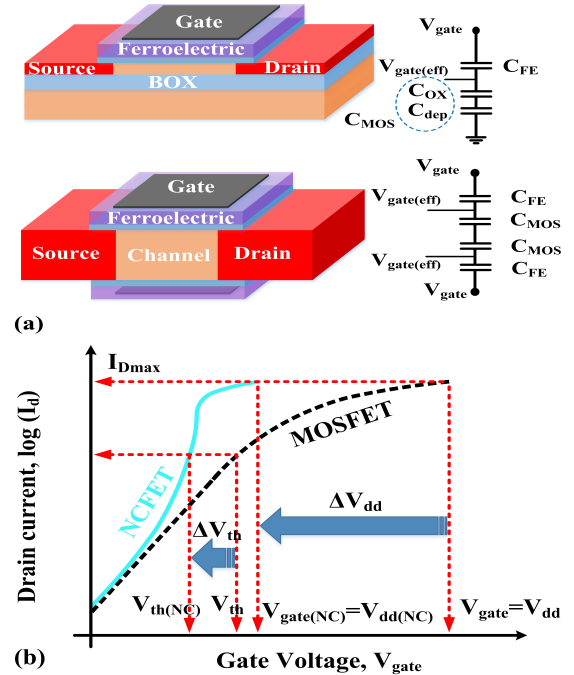

Fig. 1. (a) The device schematic and the simplified capacitance model of the UTBB FDSOI/Double-Gate NCFETs. It should be noted that the MOS capacitance (C_{MOS}) is a series combination of the oxide capacitance (C_{OX}) and the silicon depletion capacitance (C_{dep}). The NCFET can be considered as a ferroelectric capacitor in series with a conventional MOSFET. (b) Transfer characteristics of NCFET versus MOSFET highlighting the gain in terms of overdrive and reduction of threshold voltage, V_{th} and supply voltage, V_{dd}.

I. INTRODUCTION

CONVENTIONAL device scaling, which can lead to the increase in both the switching speed and the number density of MOSFETs under reasonable power consumption, had been the main guiding principle of the MOS-device engineering over these past years. However, under the sub-100-nm regime, the conventional device scaling has confronted the difficulty that the three fundamental indexes associated with the MOSFET performance, *on*-current, power consumption, and short-channel effects have the trade-off relationship with each other, owing to several physical and essential limitations directly related to the device miniaturization [1]. The power dissipation would be lowered significantly if FETs could be operated at lower gate voltages which is in contrast with having high *on*-current. In that pursuit, it was proposed that

Ali Saeidi, Igor Stolichnov, and Adrian M. Ionescu are with Laboratory of Micro and Nano-electronic Devices, Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, e-mail: ali.saeidi@epfl.ch & igor.stolitchnov@epfl.ch & adrian.ionescu@epfl.ch. Farzan Jazaeri is with Integrated Circuits Laboratory, Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, e-mail: farzan.jazaeri@epfl.ch.

the minimum voltage requirement could be overcome if the ordinary gate oxide could be replaced by another stack that provides an effective negative capacitance (NC) [2], [3]. For a MOSFET, a negative capacitor in the gate stack can make the total capacitance, looking into the gate, larger than the classical MOS capacitance. Thus, to induce the same amount of charge in the channel, one would require a smaller voltage than what would be needed classically. It is well established that ferroelectric materials can provide NC in a certain range of polarization (around P=0). By putting a dielectric capacitor (DE) of proper capacitance in series with the ferroelectric capacitor (FE), the FE can be biased in the negative capacitance state, and the FE-DE capacitance will be larger than that of the constituent DE capacitor [4], [5], [6].
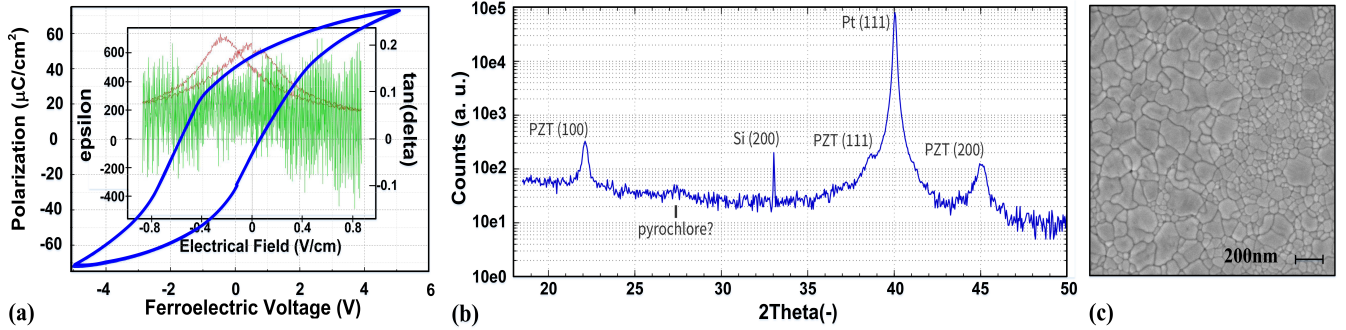
Fig. 2. The electrical and physical characterization of PZT ferroelectric thin film. 46 nm of PZT with 43/57 (Zr/Ti) ratio is deposited on a TiO$_2$(2 nm)/Pt(100 nm)/TiO$_2$/Ti/SiO$_2$/Si substrate by employing the sputtering technique. Pt top electrode is deposited at room temperature and patterned by shadow masking. The film polarization, permittivity, and the phase angle of the capacitance measurement hysteresis loops regarding the applied voltage (electric field) on the ferroelectric layer are depicted in (a). The relative permittivity, coercive field, and remanent polarization of the PZT thin film are 220-240, 260 KV/cm, and 30.2 μC/cm^2 respectively. XRD 2-theta profile (b) and SEM analysis (c) of the PZT thin film illustrate that the film is polycrystalline (see microstructures in SEM image) and textured 111-oriented, which is the most commonly used orientation. It should be noted that the ferroelectric capacitor is characterized independently which is possible due to the presence of the intermediate metallic film.

The operation principle of Negative Capacitance FETs (NCFETs) has been theoretically investigated [7], [8], [9], [10]. However, previous research studies related to the operation mechanism of NCFETs have some limitations. The previous findings of device performance investigations have been obtained considering either the analytical approach [10], [9], [11] or numerical simulations [12], [13] to study the device performance. Moreover, the presented approaches are not valid in advanced technology nodes since they are not including short channel and quantum mechanical effects. Those effects modify the charge distribution and electrostatic profile along the channel. The capacitance matching condition directly depends on the charge distribution which defines the MOS capacitance (MOS capacitance is the series combination of the oxide and the silicon capacitances). In this study, we combine both numerical simulations and analytical models to have a detailed study of nanoscale NCFETs. We design and explore the electrical properties of the 14 nm node (20 nm physical gate length) Ultra-Thin Body and Box Fully Depleted Silicon On Insulator (UTBB FDSOI) and Double-Gate (DG) NCFETs. The 2-D electrostatic effects that are expected to be pronounced in short devices are justified by averaging of the electrostatic fields in the metallic intermediate layer [2]. This intermediate metallic film provides the uniform electrostatic field inside the ferroelectric layer and makes us eligible to model the ferroelectric dielectric with 1-D Landau model. We also propose and examine a practical design guideline to have the maximum enhancement in the non-hysteretic operation of NCFETs [14]. We found that the NC not only improves the subthreshold slope (SS) but also increases the overdrive voltage significantly. Lastly, we propose the DG-NCFET to overcome the large mismatch between the MOS and ferroelectric capacitors and pin the MOS capacitance in a relatively large value which improves the NC amplification effect and reduces the optimized thickness of the ferroelectric to have the maximum enhancement in non-hysteretic operation of the device [14].

The single and double gate FeFET schematics including a simple capacitance model and the transfer characteristic of the NCFET versus the conventional MOSFET are depicted in Fig. 1. Simulation results have been obtained combining Silvaco TCAD commercial simulator [15] with Landau's theory of ferroelectrics. Results are reported for the devices at the state of the art of the technology, 14 nm CMOS node UTBB FDSOI FET [16] and DG-MOSFET with the same physical gate length. PZT is used as the gate ferroelectric, and Landau parameters are extracted by characterizing experimentally fabricated ferroelectric capacitors.

II. SIMULATION METHOD & DEVICE STRUCTURE

The device schematic of the UTBB FDSOI-NCFET and the DG-NCFET are presented in Fig. 1-a where the gate stack of a conventional MOSFET is replaced by a stack of a linear and a ferroelectric dielectric. An intermediate metallic film is considered between the linear and ferroelectric dielectrics which is chosen following the experimental results [2]. This layer averages out the non-uniform potential profile along the channel as well as any charge non-uniformity coming from the domain formation in the ferroelectric that makes the possibility to model the ferroelectric capacitor with 1-D Landau approach even in nanoscale devices. Ferroelectric negative capacitance transistors with the Metal-Ferroelectric-Metal-Insulators-Semiconductor (MFMIS) structure cannot be simulated even with the state of the art device simulators. The device can be considered as a series combination of a ferroelectric capacitor and a conventional MOSFET without imposing any boundary condition due to the presence of the intermediate layer. In this study, the device performance of an MFMIS structure is numerically calculated by combining Silvaco Atlas commercial simulator with the Landau-Khalatnikov (L-K) theory of ferroelectrics [17], [3].

According to the L-K equation, in the vicinity of a phase transition, the Gibbs free energy density (U) of the ferroelectric layer can be expanded in powers of the polarization (P).
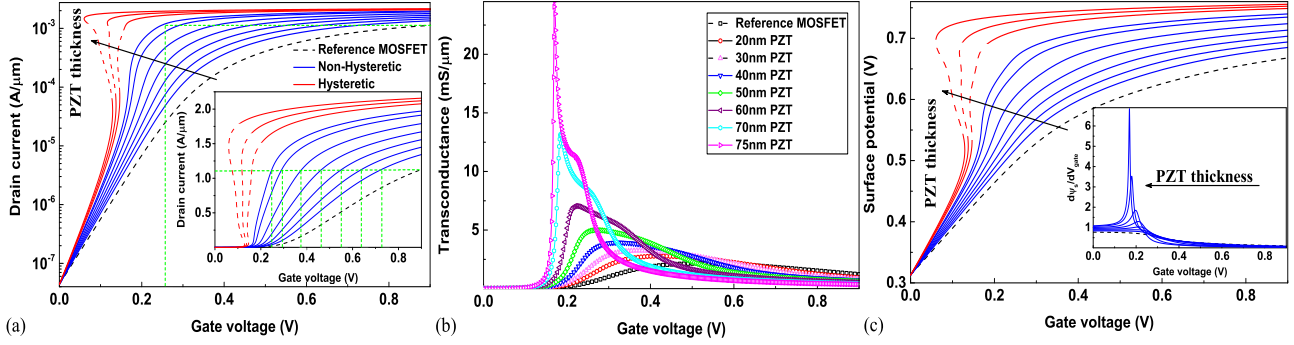
Fig. 3. UTBB FDSOI NCFET, the nominal channel length is 20 nm, the channel doping is 1×10^{15} cm^{-3}, the linear dielectric EOT is 0.9 nm, the drain voltage is 0.9 V, the BOX thickness is 25 nm, the *off*-current level is below 100 nA/μm, the saturation current for the reference device is 1.12 mA/μm (where V_{drain}=V_{dd}), and different thicknesses of PZT is used as the gate ferroelectric. (a) represents the I_d-V_g characteristic of the reference UTBB FDSOI FET [16] (dashed line) comparing the non-hysteretic (blue curves) and hysteretic (red curves) negative capacitance devices, (b) illustrates the transconductance improvement in non-hysteretic NC devices which is increasing by increasing the ferroelectric thickness, (c) explains how the surface potential of the MFIS structure is boosted due to the NC effect, and the inset figure demonstrates the surface potential derivative in non-hysteretic NCFETs.

$$U = \alpha t_f P^2 + \beta t_f P^4 + \gamma t_f P^6 - V_f P$$
$$= \alpha t_f Q^2 + \beta t_f Q^4 + \gamma t_f Q^6 - V_f Q, \qquad (1)$$

where α, β, and γ are material dependent constants (Landau parameters), t_f is the ferroelectric film thickness, V_f is the applied voltage across the ferroelectric layer, and Q is the electrical charge of the ferroelectric capacitor. The equilibrium state of the ferroelectric layer is determined by finding the minima of U, where we have

$$\frac{\partial U}{\partial Q} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 - V_f = 0. \qquad (2)$$

The Q-V_f relationship for the ferroelectric layer can be obtained as

$$V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5. \qquad (3)$$

Considering the presented structure in Fig. 1, (3) can be written as

$$V_{gate} - V_{gate(eff)} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5. \qquad (4)$$

where V_{gate} is the applied gate voltage and $V_{gate(eff)}$ is the intermediate contact potential. The left-hand side of (4) corresponds the voltage drop across the ferroelectric film, and its right-hand side represents the charge characteristic of a ferroelectric capacitor.

The MFMIS structure can be assumed as a series combination of a ferroelectric capacitor and a regular MOSFET. The 2-D electrostatics for the MOSFET has been carried out by mean of Silvaco TCAD commercial simulator taking into account the nonlocal path band-to-band model, standard Shockley-Reed-Hall recombination, drift-diffusion model, and quantum mechanical model. The analysis of the regular MOS part of the device can be simulated independently without imposing any boundary condition due to the presence of the metallic intermediate layer between the ferroelectric and linear dielectrics. Moreover, the potential is the same at any grid point of this intermediate layer and makes the possibility to

model the ferroelectric film with 1-D Landau approach. This 2-D hybrid Electrostatics for MOSFET and 1-D Landau model are solved self-consistently to simulate the NCFET [6].

PZT is used as the gate ferroelectric due to its numerous advantages like reliability, having a sufficient polarization value even in thin films, high dielectric constant, and most importantly its nanosecond polarization reversal [18]. However, PZT is not employed only for its technological advantages, but also for its robust properties regarding the film thickness variation. The ferroelectric properties mostly change regarding the film thickness [19]. However, no considerable variation was observed in the PZT properties for the films having a thickness below 100 nm. In order to obtain realistic simulation results for the FeFET operation, we used experimentally extracted Landau parameters of the PZT thin film. In that pursuit, 46 nm of PZT with 43/57 (Zr/Ti) ratio is deposited on a stack of TiO$_2$(2 nm)/Pt(100 nm)/TiO$_2$/Ti/SiO$_2$/Si by employing the sputtering technique. Pt top electrode is deposited by room temperature sputtering and patterned by shadow masking.

Electrical and physical characterization of the fabricated PZT thin film are presented in Fig. 2. The coercive field (E$_c$), remanent (P$_r$), and saturation polarizations (P$_s$) are extracted from the polarization-voltage hysteresis loop (Fig. 2-a) by averaging the value of the positive and negative going branches of the diagram. The PZT coercive field, remanent, and saturation polarization are 260 KV/cm, 30.2 μC/cm^2, and 70.3 μC/cm^2 respectively. XRD-2 theta profile (Fig. 2-b) and SEM analysis (Fig. 2-c) of the PZT thin film indicate that the film is polycrystalline and textured 111-oriented which is the most common orientation in PZT.

Landau coefficients (α, β, and γ) are determined based on the presented approach in [20] and employing the experimentally extracted values of the coercive field, remanent polarization, and saturation polarization. The PZT ferroelectric thin film Landau parameters are calculated as follows; α=-13.5$\times10^7$, β=3.05$\times10^8$, and γ=-2.11$\times10^7$ (SI unit) at room temperature. It is well-known that PZT properties alters regarding the Zr/Ti ratio, doping concentration, and the process temperature [21], [22], [23], [24]. However, considering the Landau equation, the charge-voltage characteristic of the ferro-
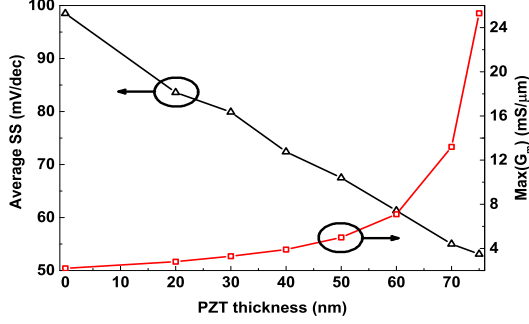
Fig. 4. The average SS (left y-axis) and the transconductance peak (right y-axis) with respect to the ferroelectric thickness for a 14 nm UTBB FDSOI-NCFET. The average SS below 60 mV/dec and the Max(G_m) higher than 25 mS/μm is obtained using 75 nm of PZT.
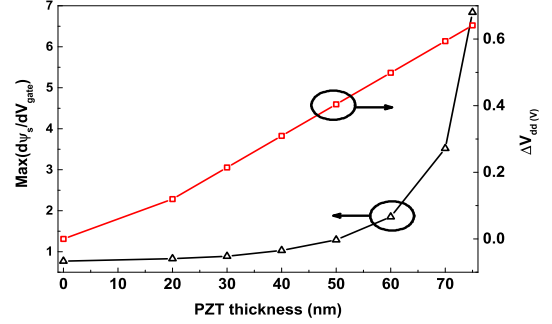

Fig. 5. The surface potential derivative peak (left y-axis) and the gate voltage reduction (right y-axis) in case of the 14 nm node UTBB FDSOI-NCFET. The surface potential derivative which is below 1 in conventional MOSFETs can be increased up to 7 using 75 nm of PZT. Due to the subthreshold swing and the overdrive enhancement caused by the NC effect the gate voltage can be reduced up to 72% with the same level of the output current (1.12 mA/μm).

electric capacitors also depends on the layer thickness that can compensate the Landau parameters variation. Although using a different ferroelectric material changes the NCFET behavior, however, using different thickness of the material can provide almost the same transfer characteristic. Therefore, we use the experimentally extracted Landau coefficients of a specific PZT capacitor highlighting the fact that the operation principle of the device would be the same for different ferroelectrics.

III. UTBB FDSOI-NCFET

In this section, we focused on a 14 nm CMOS node high-performance UTBB FDSOI nMOSFET as our reference device [16]. The device nominal gate length is 20 nm while each spacer has 3 nm width. The channel, BOX, and the gate equivalent oxide thickness are 6 nm, 25 nm, and 0.9 nm respectively. The channel is undoped (1×10^{15} cm^{-3}) and the source and drain doping level is $> 5\times10^{20}$ cm^3 to achieve low external resistance. The supply voltage is 0.9 V, the drain saturation current (at V_{drain}=V_{dd}) is 1.12 mA/μm, and the leakage current is below 100 nA/μm. The source contact is grounded, and the back gate (substrate) contact is used to adjust the threshold voltage.

The signature of the operation in the non-hysteretic NC region is a single valued gate capacitance characteristic (single-valued drain current or surface potential transfer characteristic). In Fig. (3) a and c, the blue curves indicate the non-hysteretic operation of the FeFET.

The key to the NC effect is that the negative differential capacitance of the ferroelectric ($C_{FE}<0$) compensates the positive capacitance (C_{MOS}) in the device such that the resulting gate capacitance C_{gate}=(C_{FE}^{-1}+C_{MOS}^{-1})$^{-1}$ can be made larger than C_{MOS} and boosts the surface potential [25]. The ferroelectric capacitor is effectively a negative one as the slope of the Q-V (P-E) characteristic of ferroelectric materials is negative around the origin.

The negative slope of the ferroelectric charge diagram is unstable and exhibit hysteretic jumps in charge (polarization). However, it has been shown that if the ferroelectric capacitor is placed in series with a positive capacitor, the negative capacitance segment can be effectively stabilized and provide voltage amplification [6], [2]. As long as the total capacitance

of the structure is positive, the system behaves like a positive capacitor with a value larger than both C_{MOS} and C_{FE}. The electrical properties of the 14 nm node UTBB FDSOI-NCFET is depicted in Fig. 3. Results are presented for sweeping the PZT thickness from 20 nm to 100 nm. As a general rule, high-t_f values (where t_f is the ferroelectric thickness) give rise to the hysteretic behavior (red curves in Fig. 3 a and c). Reducing t_f, hysteresis disappears, and voltage amplification can be reached. For low t_f values, the step-up conversion capability vanishes [12], [10]. As a consequence of these constraints, a key parameter of the device design is to properly tune t_f. The optimized thickness of the ferroelectric for NCFETs provides the maximum enhancement while the transfer characteristic of the device is still single valued. In our case, 75 nm of PZT provides the highest improvement before the device operation gets hysteretic. The transconductance improvement in non-hysteretic devices is illustrated in Fig. 3-b where the transconductance peak is boosted more than 10 times of its original value.

The unique signature of the NC effect in an MFIS (or MFMIS) structure is providing surface potential derivative greater than 1 (Fig. 3-c). The partial of the gate voltage regarding the surface potential can be written as

$$\frac{\partial V_{gate}}{\partial \psi_s} = 1 + \frac{C_{MOS}}{C_{FE}}, \tag{5}$$

that illustrates how the ferroelectric NC can provide voltage amplification and surface potential derivative greater than 1.

One of the most important parameters of switching devices is how steep they can switch from the *off*-state to the *on*-state. It is known that due to the Boltzmann thermal limit, the maximum slope of the *off* to *on* transition in conventional MOSFET devices cannot be less than 60 mV/dec. It has been reported that the step-up conversion in ferroelectric devices can be utilized to reduce the SS [6]. Simulation results (Fig. 3) demonstrate that the negative capacitance amplification starts in the subthreshold region and continues up to the overdrive region. This property can be used to increase the I_{ON}/I_{OFF} figure of merit for a prescribed supply voltage or reducing the
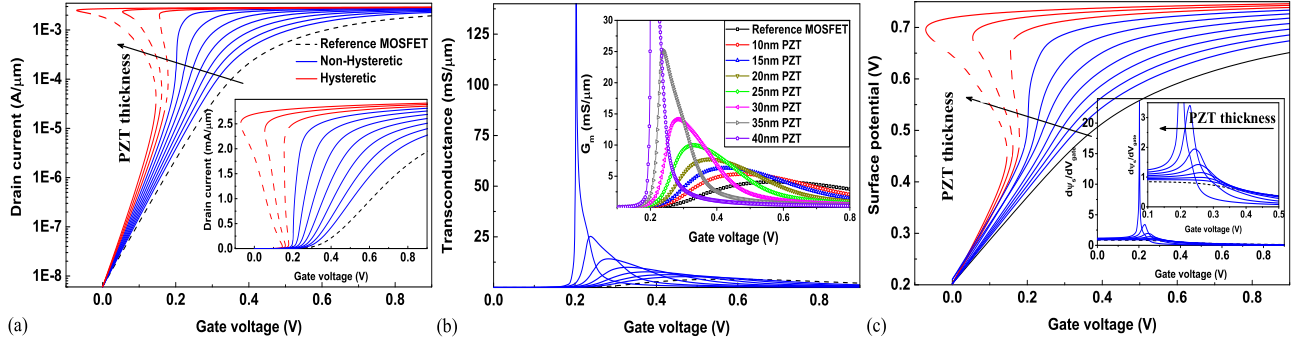
Fig. 6. The 14 nm node DG-NCFET, the nominal channel length is 20 nm, the channel doping is 1×10^{15} cm^{-3}, the linear dielectric EOT is 0.9 nm, the drain voltage is 0.9 V, the channel thickness is 6 nm, the *off*-current level is below 10 nA/μm, the saturation current for the reference device is 2.1 mA/μm (where V$_{drain}$=V$_{dd}$), and different thicknesses of PZT is used as the gate ferroelectric. (a) represents the I$_d$-V$_g$ characteristic of the reference DG-MOSFET (dashed line) comparing the non-hysteretic (blue curves) and hysteretic (red curves) NC devices transfer characteristic, (b) illustrates the transconductance improvement in non-hysteretic NC devices which is increasing by increasing the ferroelectric thickness, (c) explains how the surface potential of the MFIS structure is boosted due to the NC effect, and the inset figure demonstrates the surface potential derivative in non-hysteretic NCFETs which can be greater than 1 due to the negative capacitance effect.

required supply voltage for an arbitrary output current. The SS and overdrive voltage can be expressed as

$$SS = \frac{\partial V_{gate}}{\partial logI} = \frac{\partial V_{gate}}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial logI}, \qquad (6)$$

$$V_{OD} = V_{gate} - V_{TH}, \qquad (7)$$

where V_{OD}, V_{gate}, and V_{TH} are the overdrive voltage, the gate voltage, and the device threshold voltage respectively. The ferroelectric dielectric causes gate voltage amplification (in both subthreshold and overdrive regions) and threshold voltage reduction and reduce the required gate voltage sustaining the same level of the output current significantly. The average SS and the maximum of the transconductance regarding the ferroelectric thickness are depicted in Fig. 4. The average SS is calculated from zero gate voltage to the threshold voltage representing the effect of both overdrive and subthreshold swing enhancement. The average SS is reduced from 100 mV/dec (reference device) down to 55 mV/dec and the maximum of the transconductance (Max(G$_m$)) is increased from 2.2 mS/μm up to 25.3 mS/μm employing 75 nm of PZT as the gate ferroelectric. Moreover, the NC effect boosts the maximum of the transconductance from 2.2 mS/μm to 25.3 mS/μm. The gate voltage reduction (ΔV$_{dd}$) and the maximum of the surface potential derivative is presented in Fig. 5 where the surface potential derivative greater than 7 and up to 72% gate voltage reduction is obtained due to the NC effect. The 14 nm node UTBB FDSOI-NCFET using 75 nm of PZT as the ferroelectric dielectric can operate at 0.26 V instead of 0.9 V gate voltage providing the same I$_{ON}$/I$_{OFF}$ figure of merit.

IV. DOUBLE-GATE NCFET

One may consider the NCFET as a conventional transistor with an added amplifier. Considering a simple capacitance model (Fig. 1-a), the amplification factor of the NC effect can be expressed as

$$\beta = \frac{\Delta V_{MOS}}{\Delta V_{gate}} = \frac{C_{FE}}{C_{FE} + C_{MOS}}. \qquad (8)$$

In order to obtain a meaningful enhancement (large β), the magnitude of the ferroelectric NC ($|C_{FE}|$) and the MOS capacitor (C$_{MOS}$) needs to be relatively close. However, C$_{MOS}$ is not a constant and varies with the gate voltage; therefore, β is a voltage dependent parameter. On the other side, to have a non-hysteretic operation, the total capacitance of the gate (C$_{Gate}^{-1}$=C$_{FE}^{-1}$+C$_{MOS}^{-1}$) needs to be positive in the whole range of the gate voltage ($|C_{FE}|$ should be greater than C$_{OX}$). In a conventional single gate MOSFET with a uniformly doped substrate, the depletion capacitance and therefore the MOS capacitance could be much lower than C$_{OX}$ as C$_{MOS}$ is the series combination of the depletion capacitance and the oxide capacitance. So, the amplification factor cannot be significantly larger than 1 over a broad range of the gate voltage.

To have a significant amplification, we have to pin the depletion capacitance in a large value. By employing the fully depleted silicon on insulator structure, the depletion depth is anchored to the silicon thickness (6 nm) providing sufficient amplification over a wide range of the gate voltage. However, due to the BOX series capacitance, the MOS capacitance is not fixed in a relatively high value that matches with a small ferroelectric negative capacitance. The capacitance of the ferroelectric layer around the origin can be expressed as (1/2)αt$_f$ (V$_f \sim$ 2αt$_f \times$Q) where the parameter α is negative in ferroelectric materials as the key feature of the upconversion. A relatively low ferroelectric capacitance requires a large t$_f$ which is not appropriate for nanometer scale device fabrication as due to the high aspect ratio of the gate stack (20 nm physical gate length with nearly 80 nm height gate stack).

To reduce the optimized ferroelectric thickness and improve the NC amplification effect at the same time, we propose the DG-NCFET. In the symmetric double gate structure, the depletion thickness is pinned to half of the silicon thickness providing a high depletion capacitance. Moreover, in case of the double gate structure, there is no additional series capacitance to reduce the MOS total capacitance (as the BOX capacitance reduces the total C$_{MOS}$ in UTBB FDSOI-FET).

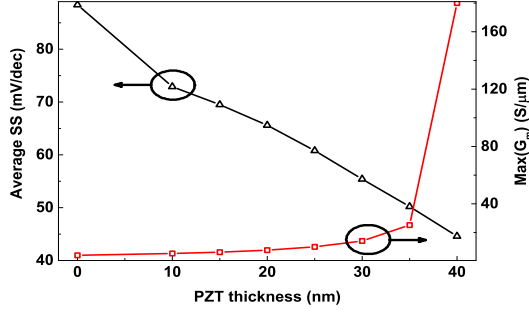Here, we designed and simulated a 14 nm CMOS node

Fig. 7. The average SS (left y-axis) and the transconductance peak (right y-axis) with respect to the ferroelectric thickness for a 14 nm node DG-NCFET. The average SS below 50 mV/dec and the Max(G_m) higher than 180 mS/μm is obtained using 40 nm of PZT.
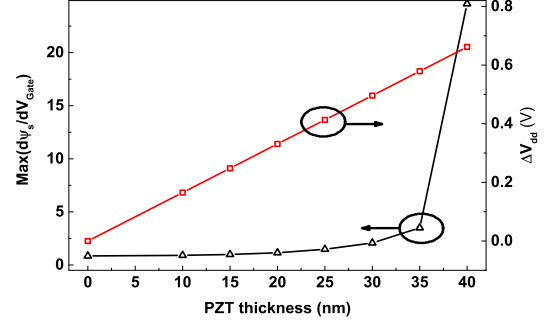

Fig. 8. The surface potential derivative peak (left y-axis) and the gate voltage reduction (right y-axis) in case of the 14 nm node DG-NCFET. The surface potential derivative which is below 1 in conventional MOSFETs can be increased up to 24 using 40 nm of PZT. Due to the SS and the overdrive enhancement caused by the NC we can reduce the gate voltage by 73% providing the same level of the output current (2.1 mA/μm).

DG-NCFET. The device nominal gate length, the channel thickness, and the gate equivalent oxide thickness is 20 nm, 6 nm, and 0.9 nm respectively. Again, we have considered 3 nm width for each spacer. The channel is undoped (1×10^{15} cm^{-3}) and the source and drain doping level is $>5 \times 10^{20}$ cm^3 to minimize the series resistance. The supply voltage is 0.9 V, the saturation current (at V$_{drain}$=V$_{dd}$) is 2.1 mA/μm, and the device leakage current is below 10 nA/μm. PZT is considered as the gate ferroelectric. Fig. 6 represents the electrical properties of the DG-NCFET sweeping the PZT thickness. The transform characteristic of the device is illustrated in Fig. 6-a where the PZT thickness is varying from 10 nm to 55 nm. As we discussed in the previous section, increasing the ferroelectric thickness improves the device performance but after a critical thickness the device operation gets hysteretic (red curves in Fig. 6-a and c belongs to the hysteretic NCFETs). The optimized thickness of the PZT for the DG-NCFET is 40 nm where we have the maximum enhancement for the non-hysteretic operation of the device. The transconductance of the non-hysteretic NC devices is compared with the reference DG-MOSFET in Fig. 6-b (the dashed-line indicates the reference MOSFET). The surface potential derivative regarding the gate voltage is depicted in the inset figure of Fig. 6-c where the surface potential derivative greater than one is obtained as the key feature of the NC effect in an MFIS structure.

Fig. 7 illustrates the device average SS (left y-axis) and the maximum of the transconductance (right y-axis). The average SS of the device (calculated by considering the device current at the zero gate voltage up to the threshold voltage) that indicates the steepness of the *off* to *on* transition is reduced from 84.4 mV/dec down to 44.6 mV/dec using 40 nm of PZT. The transconductance peak is also enhanced from 4.1 mS/μm (reference DG-MOSFET) to 180 mS/μm. The surface potential derivative regarding the PZT thickness is illustrated in Fig. 8 (left y-axis) where the maximum of the surface potential derivative is increased from 0.8 in the reference device up to 24.8 using the ferroelectric optimized thickness. As a result of the significant SS and overdrive enhancement caused by the NC effect, the gate voltage can be reduced without performance reduction. The supply voltage reduction (ΔV$_{dd}$) which is depicted in the right y-axis of Fig. 8 illustrates

that the gate voltage can be lowered down to 0.24 V by integrating 40 nm of PZT into the gate stack. Besides better electrical properties of the DG-NCFET comparing the single gate NCFET, the critical thickness of the ferroelectric (PZT in our case) is much lower in the double gate device than the UTBB FDSOI-NCFET. The optimized thickness of the PZT for the DG-NCFET is 40 nm while it is 75 nm in the case of UTBB FDSOI-NCFET.

V. Conclusions

In summary, a new design space for non-hysteretic negative capacitance MOSFETs has been proposed and examined on 14 nm CMOS node UTBB FDSOI/Double Gate-NCFETs. PZT is used as the gate ferroelectric, and Landau parameters are extracted by characterizing the experimentally fabricated PZT thin films. We have shown that the negative capacitance effect leads to both enhanced subthreshold slope and gate overdrive. It is demonstrated that the 14 nm UTBB FDSOI high-performance MOSFET can operate at 0.26 V gate voltage instead of 0.9 V with less than 100 nA/μm leakage current and 1.21 mA/μm saturation current using 75 nm of PZT as the gate ferroelectric. The device average subthreshold swing is reduced down to 55 mV/dec while the reference device's average SS is 100 mV/dec. It has also been presented that using the double gate structure reduces ferroelectric's optimized thickness by pinning the MOS capacitor in a relatively large value. A 14 nm DG-NCFET can operate at 0.24 V gate voltage (instead of 0.9 V) sustaining the same current level (2.1 mA/μm) by integrating 40 nm of PZT into the gate stack. Providing 44.6 mS/μm average SS and 180 mS/μm transconductance peak indicates that the DG-NCFET has a transfer characteristic closer to the ideal switch.

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Ali Saeidi received his Bachelor's Degree from University of Tehran in Electronic Engineering. After finishing his project on fabrication of Silicon nanotubes and silicon nanowires, he started his Master study working on fabrication of Biological sensors for cancer detection based on Silicon nanotubes and nanowires. In August 2014 he joined Professor Ionescu's Nanolab at EPFL as a PhD candidate. His current research focuses on exploration of negative capacitance ferroelectric devices and technologies.

Farzan Jazaeri received his Ph.D. degree in Microelectronics from Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland in 2015. In 2015, he joined the integrated circuits laboratory (ICLAB), EPFL working on electron-device modeling. He is a member of ICLAB, EPFL and his main research interest is on modeling of electron devices.

Igor Stolichnov has received his Master degree in solid state physics at Saint Petersburg State Polytechnical University in 1994 and PhD degree at Swiss Federal Polytechnical Institute, Lausanne (EPFL) in 2000. His scientific interests are focused on functional materials and their applications for memories and informatics where he is author of more than 80 publications. He is currently a member of staff of NANOLAB (EPFL) under supervision of professor Ionescu.

Adrian M. Ionescu is a Professor at the Swiss Federal Institute of Technology, Lausanne, Switzerland. He received the B.S./M.S. and Ph.D. degrees from the Polytechnic Institute of Bucharest, Romania and the National Polytechnic Institute of Grenoble, France, in 1989 and 1997, respectively. Dr. Ionescu has published more than 400 articles in international journals and conferences. He is director of the Laboratory of Micro/Nanoelectronic Devices (NANOLAB).