Master Thesis

Advanced NEMS Group

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2D Material-Based Bolometer

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Abstract

Measurement of thermal radiation through uncooled bolometers is at the heart of many industrial applications. From the development of the Honeywell silicon microstructure developed in 1982, no particular change in paradigm was recorded. The advent of 2D-materials offers a whole new promising future for bolometric measurements and thermal detection. 2D-materials have record properties extremely sensitive to external stimuli making them great candidates for boosting bolometers performance.

In this work, a method to model, fabricate and characterise 2D material-based bolometers is presented. The proposed design uses a suspended 2D-material beam as thermal sensor and IR absorber. The model suggests an improvement of the state of the art on three different aspects. Reduction of thermal losses, tunable enhancement of absorption and increased bandwidth. An innovative read-out technique is also suggested.

Bolometers employing graphene as suspended beam were successfully fabricated. An optimised fabrication process is proposed and allow to consistently produce devices having optimal properties to host graphene. Electrical measurements on graphene beams lying on silicon dioxide showed good tunability of graphene resistance through electrostatic gating proving possible to enhance thermal radiation absorption in graphene. The results obtained offers a promising outlook toward the future of 2D material-based bolometers.

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1 | Introduction

This thesis presents the development of a 2D material-based bolometer. A lot of time was spent on the micro-fabrication of bolometers and therefore the majority of attention is focused upon this. The devices fabricated following this thesis could be used for a multitude of sensing applications, but in this report it was decided to follow the pathway of bolometers. However, before diving into technical explanations, it is probably worth spending some words elucidating what bolometers are and what the so called Two Dimensional materials (2D-materials) look like.

Bolometers (from Greek: $\beta o \lambda o$- means "thrown things" and -$\mu \epsilon \tau \rho o \nu$ means measurer) are thermal detectors specifically designed for thermal radiation. This definition is not univocal and some people like to define bolometers as being sensors used to detect the power of electromagnetic radiation. In this report it is preferred to stick to the more restrictive former definition. A thermal detector is a device that can transduce a variation in temperature into a change of another physical property, which can be easily measured. Thermal radiation, instead, is a type of radiation emitted though the relaxation of thermally excited particles. Planck described the power spectrum of thermal radiation the first time in 1900 with the nowadays named Plank's law:

$$u\left(\lambda, T\right) = \frac{2hc^2}{\lambda^5} \frac{1}{e^{\frac{hc}{\lambda k T}} - 1} \tag{1.1}$$

where: u is the radiated power per area, solid angle and wavelength λ, T is the temperature, h is the Plank constant, c is the speed of light and k is the Boltzmann constant. The total emitted power can be deduced from Plank's law and takes the name of Stefan–Boltzmann law:

$$P = A \epsilon \sigma T^4 \tag{1.2}$$

where: A is the emitting surface, ϵ is the emissivity and σ is the Stefan–Boltzmann constant. Plank's law is valid at thermal equilibrium for an idealised body

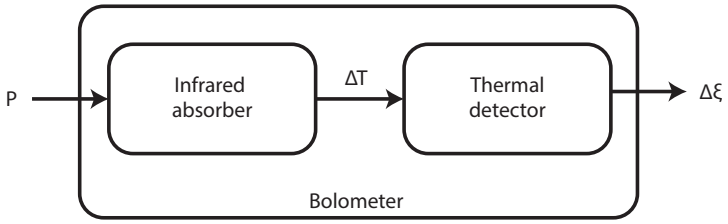

Figure 1.1 – Elements in a bolometer. The incoming thermal IR radiation power P is absorbed by the IR absorber and converted into a temperature variation ΔT. The thermal sensor transduces the temperature variation into a change in another physical quantity $\Delta\xi$, where ξ is often a voltage or current signal. Monolithic bolometers have the IR absorber and thermal sensor collapsed into one single physical element.

called "black body", which is a body that absorbs all incident radiation. Nevertheless, all bodies with a temperature different from the absolute zero emit thermal radiation. Plank's law tells that the power spectrum is uniquely defined for each fixed temperature. For instance, the peak of radiation for a body at room temperature (normally fixed at $T_r{\sim}295$K) is around $\lambda = 10\mu$m. Or again, the majority of radiation emitted by bodies with temperature close to room temperature lies in the InfraRed (IR) region of the electromagnetic spectrum. Hence, bolometers dedicated to thermal imaging of the world around us must be particularly good in absorbing the power of this portion of the electromagnetic spectrum. When this happens, the temperature of the sensing element of the bolometer changes and the signal transduced by the thermal detector is measured. Bolometers employed for thermal imaging such as night-vision goggles, infrared thermometers,...Operates in the range of $\lambda = 8 - 14\mu$m, which correspond to the transmitted window by air for a body with temperature close to room temperature. From now on with the word "bolometer", it is meant those devices dedicated to IR radiation detection . Bolometers are made of two elements: the IR absorber which transduces the absorbed radiation into a temperature variation and the thermal sensor which further transduces the thermal variation into (most likely) an electrical signal as shown in **figure 1.1**. In other words, a bolometer is an electromagnetic radiation detector dedicated to thermal radiation (specific application) whose transduction uses a variation in temperature (specific working principle). Obviously, they can detect all types of radiations in the range of wavelengths they operate on, but bolometers are generally used for thermal radiation. Two main groups of bolometers exist. Cooled

bolometers, which operate at low temperature and uncooled bolometers. The former have the advantage of reducing thermal noise (Johnson–Nyquist noise), which is an intrinsic limiting factor of all materials. On the other hand, the latter are, more easily reduced to small sized Micro ElectroMechanical Systems (MEMS) for portable devices. The adjective "uncooled" delineate a device that does not use artificial methods to alter its own temperature. Hence, uncooled bolometers generally operate at room temperature. Many transduction methods can be used in bolometers. Some examples are: resistive bolometers, pyroelectric bolometers and ferroelectric bolometers. For instance, in resistive bolometers, the absorbed IR radiation causes a change in resistance that can be electrically detected in different ways. The simplest is to apply a voltage and measure how the current changes in function of incident radiation.[1]

The discovery of *2D-materials* launches a whole new perspective for bolometers and bolometric measurements. In fact, these materials have extraordinary properties compared to their bulk relatives. 2D-materials belong to a larger category named nano-structural materials. The latter are defined as materials having at least one dimension at the nanometric scale. At this scale the electron wavelength is comparable to the material size. Hence, quantum confinement has an impact upon the band structure of materials and therefore upon their physical properties. Nano-structural materials are divided into three main categories:

- 0D-materials: quantum dots, nanoparticles binary arrays,...
- 1D-materials: nanowires, nanotubes, nanoribbons,...
- 2D-materials: nanosheets, nanoplates, nanowalls,...

It is generally meant that an xD material has nanoscale dimensions along 3-x directions. In this sense, dimensionality affects the physical properties of materials. Among 2D-materials one finds nanosheets. Nanosheets are further divided into three categories that define how 2D-materials are found in their bulk equivalent: layered van der Waals solids, layered ionic solids and surface assisted non-layered solids. The first are the most commonly known. Solids are organised in arrays of randomly oriented 2D-sheets bound to each other through van der Waals bounds. These 2D-materials can be obtained using different techniques: mechanical exfoliation, liquid exfoliation, epitaxial growth, Chemical Vapour Deposition (CVD),...Many 2D-materials have been isolated

[1] This paragraph was strongly based on reference [1].

up to these days, among them one finds graphene (zero-gap semimetal), MoS_2 (semiconductor), Black Phosphorous (semiconductor) and hBN (insulator) [2].[2]

In this thesis, *CVD-graphene* is used as IR absorber and thermal sensor as it will be extensively explained later. It is important to understand from the beginning that it doesn't have to be graphene. In fact, the approach developed in this thesis is similarly applicable to all 2D-materials and the most favourable one need to be chosen depending on the detection technique employed by the bolometer. In summary, the goal of this report is to provide a method to model, fabricate and characterise 2D material-based bolometers and justify their technological importance.

[2]This paragraph was strongly based on reference [3].

2 | Background

The purpose of this chapter is to give the necessary background to understand the importance of the steps undergone in this report as well as the motivation driving them. Many statements expressed in the introduction will be justified with a more scientific foundation.

Initially, a mathematical method to quantitatively compare bolometers performance will be presented. Then, the advantages of 2D-materials for bolometric measurements will be exhibited. Finally, the state of the art of bolometers and the fabrication techniques for graphene beams suspension will be discussed.

2.1 Bolometers modelling

ultra It is useful to have a model for bolometers that allows to predict their behaviour and more importantly to compare their performance independently from the transduction technology employed. Some figures of merit will be discussed in the following sections. The model is developed in a rather generic way and should provide a strong fundamental understanding of the problem to help comprehend the results taken from literature.

2.1.1 Mathematical model

The mathematical model considers uncooled monolithic bolometers (thermal sensor and IR absorber are collapsed into only one element) in opposition to uncooled hybrid bolometers (separated elements). The physical situation is rather complicated, but it can be simplified into a very simple model [4, 5]. **Figure 2.1** shows all the important elements one needs to account for when he describes bolometers behaviour and performance. One of the critical factors determining bolometers performance is noise. The latter can be divided in two categories, namely: interfering noise and random noise [6]. The former consist in thermal fluctuation noises in the IR absorber due to the environment, such

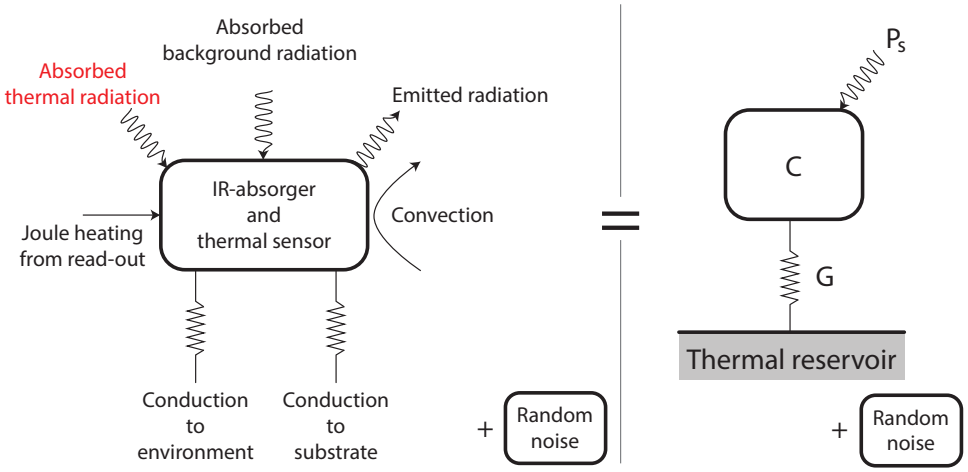

Figure 2.1 – Model of a monolithic bolometer. Physical situation on the left hand side and simplified mathematical model on the right hand side. C is the heat capacity of the IR absorber and thermal sensor component, G has units of thermal conductance and P_s is the power source. In red the target signal to be measured.

as: background radiation, emitted radiation, convection and conduction to the environment. While, the latter consists in all intrinsic forms of noise such as: Johnson–Nyquist noise, Flicker noise (also known as Pink or $1/f$ noise), Shot noise and phonon noise. It is said that a device is working at its background limit if all interfering noises are reduced to radiation only.

The *response in temperature* of a bolometer to a radiative incoming power can be mathematically determined. It is worth reminding the definition of thermal conductance:

$$G := \frac{\mathrm{d}P}{\mathrm{d}T} \tag{2.1}$$

where: P is power and T is temperature. In what follows, it is supposed that the surface area of the IR absorber and thermal sensor element is small enough to have the same temperature across the whole surface (no temperature spatial distribution). In this example, the read-out is performed by applying a bias voltage V_{bias} to the IR absorber and thermal sensor in order to measure a current change as a function of incoming radiation. The model structure is not modified by the read-out technique method. Temperature variations are considered to be small $\delta T/T \ll 1$. The first step toward modelling a monolithic bolometer is to define a generalised thermal conductance $G = G(T)$ such that:

$$\begin{aligned} G = G_{\text{joule effect}} + G_{\text{conduction to substrate}} + G_{\text{conduction to environment}} \\ + G_{\text{convection}} + G_{\text{emitted radiation}} \end{aligned} \tag{2.2}$$

It can be shown that each term on the right hand side of the equation can be generally expressed as a power law: $G(T) = G_0 T^{\chi}$ [4,7]. Some examples are:

$$G_{\text{emitted radiation}} = \frac{\mathrm{d}P_{\text{emitted radiation}}}{\mathrm{d}T} = 4A\epsilon\sigma T^3 \tag{2.3}$$

$$G_{\text{joule effect}} = \frac{\mathrm{d}P_{\text{joule effect}}}{\mathrm{d}T} = -\frac{V_{bias}^2}{TR}\frac{R - R_L}{R_L + R}\alpha \tag{2.4}$$

where the first one has been obtained from Stefan-Boltzmann law (equation (1.2)), while details for the second equation can be found in reference [4]. In this formulae: A is the total emitting surface, ϵ is the emissivity, σ is the Stefan–Boltzmann constant, R is the IR absorber and thermal sensor element resistance, R_L the internal resistance of the generator applying the bias voltage and α is the Temperature Coefficient of Resistance (TCR). The power source term can be written as:

$$P_s = P_s(t) = P_{\text{thermal radiation}} + P_{\text{background}} \tag{2.5}$$

Basically, what was done by defining the generalised conductivity was bringing the dissipative terms on the left hand side of the thermal equation and re-express them as conduction terms. Consider now that the temperature of the IR absorber and thermal sensor element is close to the substrate temperature T_s (equal if at thermal equilibrium with $P_s = 0$), say $T_s + \delta T$. The equation describing the behaviour of the IR-absorber and thermal sensor element temperature $T_s + \delta T$ is:

$$\begin{aligned} C\frac{\mathrm{d}\left(T_s + \delta T\right)}{\mathrm{d}t} + \int_{T_s}^{T_s+\delta T} G(T')\mathrm{d}T' &= \eta P_s(t) \\ C\frac{\mathrm{d}\left(\delta T\right)}{\mathrm{d}t} + G(T_s)\delta T &= \eta P_s(t) \end{aligned} \tag{2.6}$$

where: η is the absorbance. The equation was linearised thanks to $\delta T/T \ll 1$ and the thermal equilibrium condition $\mathrm{d}T_s/\mathrm{d}t = 0$ was used. This equation is readily solved using Fourier analysis:

$$\delta T(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} \delta T(\omega) e^{i\omega t}\mathrm{d}\omega \tag{2.7}$$

$$P_s(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} P_s(\omega) e^{i\omega t}\mathrm{d}\omega \tag{2.8}$$

Inserting these two equations in equation (2.6) gives:

$$\delta T(\omega) = \frac{1}{G}\frac{1}{1 + i\omega\tau}\eta P_s(\omega) \tag{2.9}$$

where the time constant $\tau = C/G$ was defined. Hence, the IR absorber of the bolometer behave as a low pass filter with cut off frequency $f_c = 1/(2\pi\tau) = G/(2\pi C)$. It is important here to notice the significance of C and G for thermal imaging as limiting bandwidth factors. [1]

The *sources of random noise* still have to be introduced in the model. Random noises are modelled as signals with zero average and no correlation v_n. A good way to deal with these kind of waveforms is to consider the mean square noise:

$$\overline{v_n^2} = \lim_{t\to\infty} \frac{1}{t} \int_{-t/2}^{t/2} v_n^2 dt' \tag{2.10}$$

When two of such signals are summed $v = v_{n_1} + v_{n_2}$ and the mean square noise is computed the uncorrelation between noise signals implies that $\overline{v_{n_1} v_{n_2}} = 0$ and therefore:

$$\overline{v^2} = \overline{v_{n_1}^2} + \overline{v_{n_2}^2} \tag{2.11}$$

However, noise signals are usually described by their spectral density function $S_n(f)$ such that:

$$\overline{v_n^2} = \int_0^\infty S_n(f)\,\mathrm{d}f \tag{2.12}$$

In general, it can be difficult to have a mathematical expression of the spectral density, but some examples are [5, 6]:

$$S_{\text{Johnson–Nyquist}} = 4kTR \tag{2.13}$$

$$S_{\text{phonon}} = 4kGT^2 \tag{2.14}$$

$$S_{\text{Flicker}} \sim K + \frac{K'}{f} \tag{2.15}$$

where: k is the Boltzmann constant and K and K' are some constants. All the elements presented in this chapter are critical in the quantification of bolometers performance as it will become clearer later.[2]

2.1.2 Figures of merit

There are many figures of merit that describe the performance of bolometers, the ones considered in this report are the responsivity ($\mathcal{R}$) and the Noise Equivalent Temperature Difference (NETD).

[1] This paragraph was based on references [4, 8].
[2] This paragraph was based on reference [6].

The *responsivity* is a function of the thermal radiation power. This quantity is defined for $P_s = P_{\text{thermal radiation}}$ and it is computed as the derivative of the output voltage signal V_{out} with respect to the icident radiant power P_s:

$$\mathcal{R} = \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}P_s} \tag{2.16}$$

This is an example for a voltage read-out. If, for instance, the output signal is a current, V_{out} must be replaced with I_{out}. Thus, the units of $\mathcal{R}$ vary depending on the read-out signal. This quantity can be seen as an output-input gain.

The *NETD* is defined as the necessary temperature change of an infinitely large black body emitting the source power $P_{\text{thermal radiation}}$ to increase the average signal to noise ratio $V_{\text{out}}/\sqrt{\overline{v_n^2}}$ (in case of voltage read-out) from zero to one. In other words it is the minimal temperature difference detectable by the bolometer. Mathematically:

$$\text{NETD} = \frac{4F^2 v_n}{\tau_o A_D \mathcal{R} \left(\Delta P/\Delta T\right)_{\lambda_1-\lambda_2}} \tag{2.17}$$

where: τ_o is the optics transmittance, A_D total pixel area and $F = 1/2\sin\theta$ with θ the angle which the marginal ray from the optics makes with the axis of the optics at the focal point of the image. $(\Delta P/\Delta T)_{\lambda_1-\lambda_2}$ is the change in power per unit area radiated by a blackbody at temperature T, with respect to T, measured within the spectral band from λ_1 to λ_2. This values for some intervals are listed in reference [1]. Since NETD $\propto v_n$, according to equation (2.11), the NETD values of different noise sources can be summed as follows:

$$\text{NETD}^2_{\text{total}} = \text{NETD}^2_{\text{noise source 1}} + \text{NETD}^2_{\text{noise source 2}} + \dots \tag{2.18}$$

Both these two quantities can be experimentally measured and used for comparison between bolometric devices. The theoretical model will serve as a guideline to establish which parameters have an impact on the improvement of bolometers.[3]

2.1.3 Discussion

Having a theoretical approach is advantageous because it allows to extrapolate what parameters are important to be tailored in order to improve the quality of bolometric measurement. Reference [7] offers a very similar, but more complete analysis than the one presented in the previous subsections. The model

[3] This subsection was strongly based on references [1, 8].

developed in that paper is valid for an array of resistive bolometers with bias current I_{bias} and voltage read-out. In a real situation many terms are often negligible, for instance, it is often true that $G_{\text{emitted radiation}} \ll G_{\text{conduction to substrate}}$ or $G_{\text{convection}} \approx 0$ specially for vacuum packages. What can be easily understood is that the improvement of bolometers rely mainly on three pillars: enhancement of the IR-radiation absorption, improvement of thermal isolation and reduction of the IR absorber mass and therefore reduction of the thermal capacity. A fourth important parameter that improve bolometric measurement is the increase of the measurement resolution on the read-out physical quantity (generally voltage). The latter is not part of the presented theoretical model. In Section 3 it will be stated how 2D-materials help improving bolometric sensors based on these pillars.

2.2 Advantages of 2D-materials

In the introduction of this work it was already discussed how dimensionality confer to 2D-materials extraordinary properties, very different from those of their bulk equivalents. In this section the properties of graphene will mainly be reviewed. The reason is that graphene was the 2D-material available when the fabrication process started and therefore it was the one used. It is reminded that the goal is not to claim that graphene should be employed, but to present an approach to fabricate and characterise 2D material-based bolometers independently of the material and justify their technological importance.

Graphene is a 2D-material, which was first isolated by mechanical exfoliation in 2004. One of the most widely used graphene type today is probably CVD-graphene, because it can be deposited in large sheets with still high levels of purity. Graphene is a monoatomic sheet of carbon atoms covalently bound in a honeycomb structure through hybridised sp^2 orbitals. Graphene is a zero band gap semimetal. It is interesting for bolometric applications because of its large absorption band extending through all the IR spectrum and its constant absorption strength on the whole spectrum [2, 9]. Graphene additionally exhibit extremely high carrier mobility at room temperature, extremely high Young's modulus ($\sim$ 1TPa) and excellent thermal conductivity (3000-5000 $\text{Wm}^{-1}\text{K}^{-1}$) [10]. Graphene is extremely flexible (can sustain elastic deformations of more than 20% and has high breaking strength of 42Nm^{-1}) and its sheet resistivity can theoretically be as low as $\sim 30\Omega\square$ [10, 11]. Additionally, the mass of graphene and all 2D-materials in general is extremely small due

to their nanometric thickness. Consequently, the heat capacity of these materials is dramatically affected and low (due to the small mass) [12]. But, on the other hand the specific heat of graphene is claimed to be slightly higher than that of graphite at room temperature and it is transparent to light (white light absorbance 2.3%) [10, 13]. Another interesting feature of graphene is the high in plane thermal conductivity (due to its strong sp^2 covalent bonds) and relatively low out of plane thermal conductance (limited by weak van der Waals coupling) [13]. This difference is highly affected by defects in the graphene sheet.

Nevertheless, the most attractive feature of 2D-materials is that their physical properties are extremely sensitive to external stimuli such as mechanical deformation, doping, external electric fields,... Thus, it possible to tune their properties at a highly controllable manner [10]. 2D-materials are naturally great candidates for Nano ElectroMechanical Systems (NEMS) applications. The isolation of graphene was quickly followed by many others such as: MoS_2, Black Phosphorous, hBN... And they all are interesting as they show extraordinary and tunable properties. The list of 2D-materials grows with time and each of them could be a good candidate for a particular bolometric application. It is therefore hugely profitable to have a generic approach to fabricate 2D material-based bolometers independently of the chosen 2D-materials.

2.3 State of the art

A general trend of the last many years in the electronics market has been miniaturisation and portability of electronic devices. This trend supported uncooled resistive bolometers as being easily reducible in size and low in energy consumption. Still most modern resistive bolometers derive from the pioneering Honeywell silicon microstructure developed in 1982 [1]. The latter is made of a suspended membrane over the electronics. The membrane is made of silicon nitride (the IR absorber) and sandwiches a thin film of vanadium oxide (having a large TCR, it acts as the thermal sensor). The Honeywell bolometer is an hybrid bolometer having physically separated IR absorber and thermal sensor. Many variations of this structure exist nowadays but the basic principle stays very similar. NETD achieved are of the order of $\sim$ 50mK. Using suspended membranes as a double advantage. First it reduces thermal losses to the environment and substrate and second a Fabry-Pérrot cavity can be created with the substrate in order to increase absorption. For IR detection in the spectral

interval of 8-14 μm a cavity size of $\sim \lambda/4 = 2.5\mu$m is required. [4]

A more recent innovation is the substitution of the bi-functional membranes of the Honeywell structure with ultra-thin Pt/Al_2O_3 films, where absorption and sensing are performed by one single element [14]. These structures have two interesting advantages: first thermal isolation (thinner membranes have lower conductance) and second the absorption can be tuned by varying the film thickness [15, 16]. NETD values of 163mK and time constants of 1ms were achieved with this technique.

2D-material based bolometers can take the form of suspended beams. It is therefore interesting to bring to light a study done in 2010 on a large array of suspended CVD-graphene beams found in reference [17]. They used two distinct fabrication techniques for the beams. The first were fabricated by transferring pre-patterned graphene beams onto trenches, while the seconds were fabricated by transferring unpatterned graphene, patterning the graphene on the substrate, depositing and patterning gold on top of graphene to generate electrical contact and releasing the graphene by wet etching and critical point drying. This technique is probably the most often employed to create graphene beams up to these days (see for instance [18–21]). They further claim and demonstrate that the resonance frequency of these beams can be modulated by either gate voltage or temperature. They additionally state that buckling, ripples and variable compression/shear/tension are the sources of differences in resonance frequencies among geometrical identical beams.

One of the latest published papers about uncooled thermal sensing using 2D-materials is presented in reference [21]. In their approach they exploit the tunable seedback effect of graphene for demonstrating thermal imaging. They claim to achieve responsivities $\mathcal{R}$ of the order of 7-9V/W at $\lambda = 10\mu$m and time constant τ =23ms. The carrier mobility of graphene seems to be the bottleneck of the intrinsic improvement of NETD. In fact, it is stated that improvements in the graphene transfer technique could enormously improve the carrier mobility and consequently reduce the NETD to values in the range of 30-150 mK. Currently, the experimentally measured NETD was 30-40K and since the latter is dependent on external factors such as the optics, it is claimed that a reduction to 1K could be reached only from extrinsic optimisation. Back in 2007, calculations showed that NETD values as low as 200mK can be achieved at room temperature and atmospheric pressure [7].

[4] This paragraph was based on references [1, 8].

3 | Design and motivation

This chapter is dedicated to the presentation of the schematic and working principle of the proposed device. Firstly, the schematic will be described and secondly the advantages with respect to the state of the art will be discussed.

3.1 Design schematic and working principle

Figure 3.1 shows the proposed device. A suspended graphene beam is connected to two gold electrodes named source and drain. A gold gate electrode for electrostatic doping of the graphene is placed under the graphene beam and forms a Fabry-Pérot cavity with the graphene beam. The graphene beam acts as the IR absorber and thermal sensor. Two different types of red-out can be employed with this bolometer. The more traditional one is through changes in beam resistance. While, the second utilises shifts in the beam resonant frequency.

3.1.1 Resistive read-out

The resistive read-out is the traditional way bolometers works. In this design the IR-radiation is absorbed by the graphene sheet. Absorption at the wavelength of interest is enhanced by the Fabry-Pérot cavity. The IR-radiation infer to the graphene a temperature increase dT proportional to its power and therefore a resistance variation dR can be detected:

$$\mathrm{d}R = R\alpha\mathrm{d}T \tag{3.1}$$

where: α is the TCR. A bias current can be applied in order to transform the variation in resistance into an easily measurable voltage variation. For this type of read-out, high values of TCR are favourable to increase responsivity. Graphene is not the most suitable material for this type of read-out method as it has low

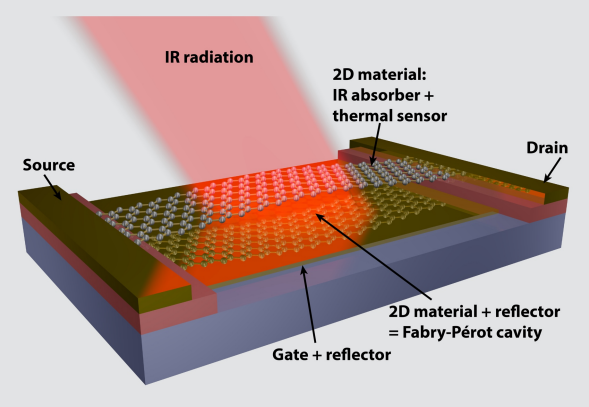

Figure 3.1 – Schematic of the proposed device. A graphene beam is suspended between two electrodes and functions as the IR absorber and thermal sensor. A gate electrode is placed under the graphene and create a Fabry-Pérot cavity with the graphene beam.

TCR coefficient $\alpha = -1.2 \cdot 10^{-3}\mathrm{K}^{-1}$ [22]. For sake of comparison vanadium oxide has a TCR coefficient of $\alpha = 65 \cdot 10^{-3}\mathrm{K}^{-1}$ [23].

3.1.2 Resonant frequency read-out

Frequency read-out is a more innovative method of detecting variations in temperature of the graphene beam. One way to measure the resonant frequency is to apply a constant source-drain voltage and a AC/DC voltage to the gate. The AC component is used to excite the graphene beam. In a continuum model the resonant frequency of a pinned-pinned beam, which is a good first approximation of the clamped-clamped beam, is given by [17, 24–27]:

$$f_{\mathrm{res,n}} = \frac{\pi n^2}{2L^2}\sqrt{\frac{EI_y}{\rho_m A_c}}\sqrt{1+\frac{\sigma_{\mathcal{T}} A_c L^2}{EI_y \pi^2 n^2}} \tag{3.2}$$

where: n is a positive integer, E is the Young's modulus, ρ_m is the beam mass density, I_y is the second moment of inertia with respect to the y-axis (set along the beam width), A_c is the beam cross-sectional area, L is the beam length and $\sigma_{\mathcal{T}}$ is the tensile stress. When tensile stress dominate ($\sigma_{\mathcal{T}} A_c L^2 / \left(EI_y \pi^2 n^2\right) \gg 1$) the equation simplifies. If the explicit dependences on temperature T and DC gate voltage $V_{\mathrm{G}}^{\mathrm{DC}}$ are introduced, one finds:

$$f_{\mathrm{res,n}}\left(T, V_{\mathrm{G}}^{\mathrm{DC}}\right) = \frac{n}{2L}\sqrt{\frac{\sigma_{\mathcal{T}}\left(T, V_{\mathrm{G}}^{\mathrm{DC}}\right)}{\rho_m\left(T\right)}} \tag{3.3}$$

For a beam with rectangular cross section of thickness t, the tensile stress dominance condition can be re-expressed geometrically: $\epsilon_{\mathcal{T}} \gg t^2\pi^2 n^2/(12L^2)$, where $\epsilon_{\mathcal{T}}$ is the tensile strain. The tensile stress depends on the DC gate voltage (initial displacement offset) and on the temperature of the beam. In fact, when the graphene beam is heated by the IR-radiation it has tendency to contract, hence increase the tensile stress and finally cause a shift in resonant frequency. This effect is further enhanced by the substrate expansion[1]. Mechanical deformations cause proportional changes in the graphene electrical resistance [28]. Hence, the resonant peak is reflected in the current measurement and shifts of the current peak can be detected by Fourier analysis. Similarly to the resistive read-out, it is favourable to have high linear expansion coefficients. The one of graphene is $\alpha_T \approx -8 \cdot 10^{-6}\mathrm{K}^{-1}$ [26, 29]. For sake of comparison for gold one finds $\alpha_T \approx 14 \cdot 10^{-6}\mathrm{K}^{-1}$.

3.2 Significance of the study

Bolometers fabricated from 2D-material have a great perspective for the future. Having suspended sheets improves thermal isolation to the surroundings and most of the heat loss is dictated by conduction to the anchors. The low beam mass enormously reduces the thermal capacity of the IR-sensor and therefore increases the bandwidth of the bolometer. Another fundamental aspect of 2D-material is the high level of tunability of their properties.

The absorbance of some of these materials may be low (for instance the one of graphene being 2.3% for white light), but this property can be electrostatically enhanced [30]. The electrical conductivity σ_e of the beam can be tuned by applying a DC gate voltage $V_{\mathrm{G}}^{\mathrm{DC}}$ (field effect) [31,32]. Consequently, the absorption being a function of the electrical conductivity $A(\sigma_e)$, it can be maximised by impedance matching [16]. Absorption can be further increased at a specific wavelength by the Fabry-Pérrot cavity.

Graphene on its side is interesting for resonant frequency read-out due to its mechanical properties. In fact, graphene is extremely flexible, it can sustain large elastic deformations and has very high breaking strength. This innovative read-out method could have a positive effect on the device dynamic range.

The fabrication of 2D-material suspended beams is often accomplished with the following fabrication steps: (i) 2D-material transfer on sacrificial layer, (ii)

[1]Assuming linearity: $\sigma_{\mathcal{T}}\left(T, V_{\mathrm{G}}^{\mathrm{DC}}\right) = \sigma_{\mathcal{T},0} - E(T)(\alpha_{T,\mathrm{graphene}} - \alpha_{T,\mathrm{substrate}})(T - T_r) + \sigma_{\mathcal{T}}\left(V_{\mathrm{G}}^{\mathrm{DC}}\right)$, where $\sigma_{\mathcal{T},0}$ is the initial tensile stress [24].

2D-material patterning, (iii) evaporation of gold on top of the 2D-material, (iv) patterning of source and drain electrodes and (v) release of 2D-material by sacrificial layer etching (usually wet etching followed by critical point drying). The fabrication proposed in this project has an advantageous difference: (i) evaporation and (ii) patterning of gold source and drain electrodes on sacrificial layer, (iii) graphene transfer, (iv) graphene patterning and (v) release of graphene by sacrificial layer etching (vapour HF). Graphene transfer is maximally delayed in the fabrication process. This is advantageous because any fabrication step done on top of graphene can significantly reduce graphene quality and graphene to electrode contact [33]. This is generally true for all 2D-materials. In this approach graphene will bind to the substrate through van der Waals forces.

4 | Fabrication

The goal of this chapter is to describe how the resonator described in the previous chapters can be transformed into a physical device. Two similar fabrication run were performed and they will be both described with a similar structure. The first part is dedicated to the description of the process flow and the microfabrication steps, while in the second part the mask and wafer layout will be discussed and justified. For each run, an extended description of the issues encountered is delineated and a brief summary and conclusion presented. Toward the end of the chapter, the devices obtained from the two runs will be compared. Detailed runsheets and recipies can be found in Appendix A and devices distribution on wafers and chips are shown in Appendix B.

4.1 First fabrication run

The purpose of the first fabrication run is primarily to reach the end of the process flow and complete all the necessary trainings needed to use the tools in the cleanroom. Few concerns will be devoted to the optimisation within the same run. The process flow will then be globally optimised for the second run. This pioneeristic approach allows to have both a larger picture and a more complete feedback of the main problems of the fabrication as a whole. Additionally, it makes possible to rapidly perform repetitive tests for non-conventional fabrication steps such as graphene patterning and graphene release.

4.1.1 Process flow

In this section the process flow of the fist fabrication run will be discussed in detail. The problems and issues encountered will be discussed in Section 4.1.3 and they give a strong feedback and solid starting point for the second fabrication run. The entire runsheet with all recipes used at the Center of Micronanotechnology (CMi) facility at Ecole Politechnique Fédérale de Lausanne (EPFL) can be found in Appendix A.

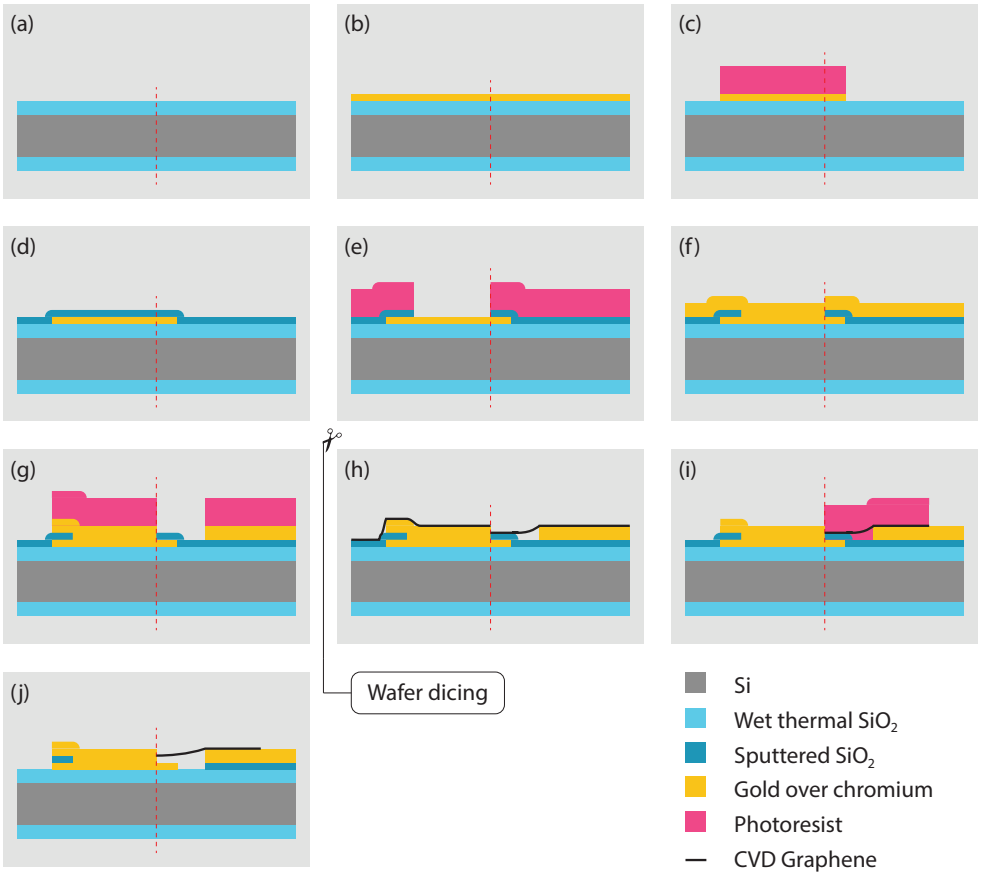

Figure 4.1 – First fabrication run process flow. All figures are split into two in order to avoid redundant information due to the symmetry of the devices. In fact, the dashed red line can be seen as an axis of symmetry. On the left-hand side the schematic representation of the cross section 1 shown in **figure 4.3**, while the cross section 2 is represented on the right hand side. (a) The starting point is a silicon wafer with wet thermal silicon dioxide on both sides. (b) A layer of Chromium/Gold is evaporated on one side. (c) The gold is patterned with a lithography step and wet etching. (d) A layer of silicon dioxide is sputtered on the wafer. (e) Patterning of the oxide with lithography and wet etching. (f) A second layer of Chromium/Gold is evaporated on the wafer. (g) Gold patterning via lithography and wet etching. At this stage the wafer are ready to be diced into single 10mm squared chips. (h) Graphene transfer. (i) The graphene is patterned through a lithography step and oxygen plasma etching. (j) Vapour HF etching of the silicon dioxide and graphene release.

The *process flow* is illustrated in **figure 4.1**. Suspended beams of graphene with electrodes will be realised through a four lithography process. First gold gate electrodes are defined via wet etching using resist as etch mask. A sacrificial oxide layer is deposited and patterned in Buffered HydroFluoric acid (BHF) using resist as etch mask. Source drain electrode are defined in a similar way as the gates. After dicing of the wafer graphene is transferred to individual chips and patterned in an O_2 plasma using resist as etch mask. Finally vapour HydroFluoric acid (HF) is used to release the patterned graphene.

The devices are fabricated on ∅100mm Single Side Polished (SSP) test p-type (0.1-100Ωcm) wafer with 285nm of wet thermal silicon dioxide (SiO_2) on both sides. The same wafers are used for other purposes than this fabrication and this specific oxide thickness is chosen to guarantee a good visibility of graphene on top of these wafers under white light [34]. In this project the silicon dioxide thickness is arbitrary and the oxide merely serve as dielectric. The first step is to evaporate a layer of 5nm of chromium and 25nm of gold on the front side of the wafer. Thin layers of metal are preferred to avoid the topography to have a negative impact on the next fabrication steps. It is well known that the gold has very poor adhesion on silicon dioxide substrates and therefore a thin layer of chromium is mandatory to promote its adhesion and prevent delamination.

The first lithography step is then performed and the gate layer is patterned into the Cr/Au layer by wet etching. The Critical Dimension (CD) of this lithography step is 2μm. The reason for choosing wet etching rather than ion beam etching or lift-off is a matter of decreasing the risk of having fences at the gold edges, while plasma etching was not an option for gold with the tools at our disposal. Having smooth gold edges will be crucial when the drain and source pads are patterned. In fact, fences would enormously increase the risk of breaking the graphene. All dicing marks and alignment marks for single chips and wafer are also patterned during this step. The advantage of using gold is that it does not oxidise.

A layer of 250nm, or 2.5μm silicon dioxide is sputtered on the wafer in argon atmosphere (referred to as low quality SiO_2) at room temperature. The thin layer of SiO_2 enhances the gate effect on the graphene layer and has a Fabry-Perrot resonance in the short infrared, while a 2.5μm thick layer increases the Fabry-Perrot effect in the long infrared region, which correspond to the peak of thermal radiation at room temperature.

The silicon dioxide is then patterned with a second lithography step and wet etching in BHF. The CD of this lithography step and the alignment are not

critical. The patterning of SiO_2 is necessary to guarantee the electrical contact between the gate layer and the gate pad on the drain and source layer. The silicon dioxide layer will then be used as a sacrificial layer for graphene release. This is a well known technique, but sputtered silicon oxide is rarely used for this purpose [35]. However, it was the best choice possible, since the majority of the tools available for SiO_2 deposition did not accept substrates with gold. The above mentioned sacrificial layer thicknesses were not successfully obtained because no deposition rate measurement test was done and the deposition rate provided by the CMi staff was not accurate (details in Appendix A).

A second layer of 25nm/100nm Cr/Au is evaporated on the wafers. This gold thickness prevents gold from delaminating during wire bonding and guarantees the mechanical support when probing. This layer was then patterned similarly to the first metal layer, but using a different etchant for chromium as suggested in Section 4.1.3. A third lithography step is therefore needed before wet etching the Cr/Au thin film. The CD of this lithography step is not critical, but the maximal error in the alignment should preferably be smaller than 500nm. Nevertheless errors in the range of 500nm - 2μm should not compromise the working principle of the bolometers.

At this stage, the wafers are ready to be saw diced into 10mm $\times$ 10mm chips. This is necessary because graphene films are only 7cm $\times$ 7cm and wet graphene transfer is better performed on small substrates. Furthermore, it is often found in literature that graphene is transferred before patterning the drain and source pads and the gold is actually deposited on top of graphene (see for instance [18–21]). This approach is disfavoured for two reasons. First, graphene quality is affected at each fabrication step and therefore it is profitable to delay the graphene transfer as much as possible [33]. Second, transferring the graphene earlier implies dicing the wafer earlier and consequently increase the number of fabrication steps on single chips and this would necessarily slows the fabrication down.

The graphene foils are transferred to the 10mm square chips following the process flow illustrated in **figure 4.2**. This procedure will be elucidated in more detail later in this section. After the transfer is completed, a fourth lithography is then performed in order to pattern the graphene in oxygen (O_2) plasma as suggested in references [36,37]. The etching is done at 200W for 30s in a chamber with a pressure of 0.5mbar and an O_2 flow of 200sccm.

In the last fabrication step the graphene is released with a vapour HF etch. Wet etching is not possible at this stage because the liquid surface tension would

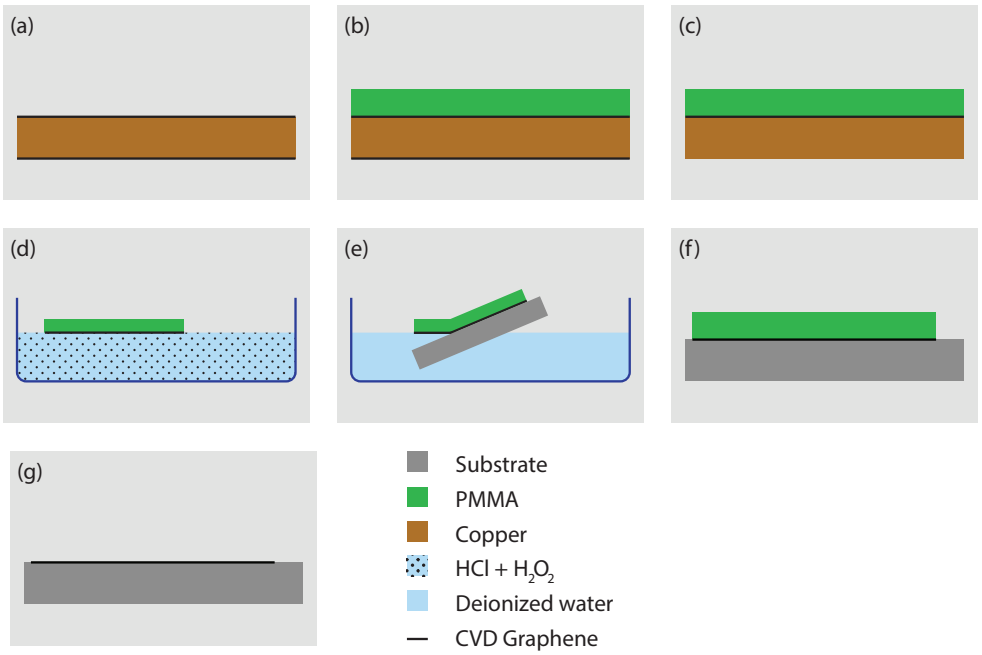

Figure 4.2 – Wet graphene transfer on a substrate. (a) The starting point is a copper thin film with CVD graphene on both sides. (b) A PMMA layer is spin-coated on top of the foil. (c) Graphene on one side of the copper foils is etched by oxygen plasma. (d) Copper is etched in a HCl+H_2O_2 solution. (e) The PMMA and graphene foil is transferred to the substrate using the fishing method. (f) The graphene is attached to the substrate prevalently by van der Waals bounds. (g) The PMMA is dissolved in acetone.

cause the graphene beam to collapse and stick to the substrate unless critical point drying is performed, but this would be more delicate and lengthy. During etching the chips are heated up to 60°C. At this temperature the difference in etch rate between wet thermal silicon dioxide and sputtered SiO_2 is greater than at room temperature [38, 39]. This increase in selectivity makes it easier to stop etching at the interface between the two silicon dioxide types. Moreover, the etch rate decreases with temperature and therefore it becomes easier to control the procedure at higher temperatures. It should be kept in mind that it is quite difficult to predict the etch rate of vapour HF specially because it is not linear in time. Another possibility could still be to release the graphene via wet etching and critical point drying but this technique was not tested during this project.

The *wet graphene transfer process flow* is shown in **figure 4.2** [40]. The Technical University of Denmark (DTU) is the provider of 7cm × 7cm copper foils with

CVD graphene on top. From the very beginning, it is advised to mark the front side of the foil with a marker, for instance with two dots. The foil may need to be gently flattened with the help of two wipes before starting the transfer.

Initially, the film is placed on a PolyDiMethylSiloxane (PDMS) coated wafer. The wafer with the foil is coated with a Poly-Methyl MathAacrylate (PMMA) film as follows. First the entire copper film must be covered with an 8% PMMA solution (8g of PMMA in 100ml of Anisole solvent). The wafer is spun for 1min with an acceleration of 1000rpm/s up to a constant speed of 1000rpm. Finally, the wafer is baked at 80°C under a lid for 20min to evaporate the solvent. The PMMA serve as mechanical support for the graphene. With the help of a scalpel, the foil can be removed from the wafer.

In order to enhance the copper etching, the graphene layer not in contact with the PMMA is etched in oxygen plasma at 50W (**figure 4.2c**). The foil can be now chopped in smaller pieces as large as the target chips size on which they have to be transferred to (approximately 0.7mm $\times$ 0.7mm). The copper etching is done at 60°C in 5% HCl with 10 drops of H_2O_2 per 100ml of HCl. The small foils are left floating in the solution with the copper facing the solution until the copper is completely etched.

With the help of a glass slide the PMMA-graphene foils are moved to a deionised water bath for rinsing. The technique used is called fishing and consist in exploiting the liquid surface tension to stick the foil onto the glass slide and prevent it from rolling on itself during transfer. In the meantime the target chips are cleaned in acetone and IsoPropyl Alcohol (IPA). Then, the PMMA-graphene foils are transferred onto the target chips using the fishing method as shown in **figure 4.2e**. The chips are then baked at 60°C for 3 hours. Finally, the PMMA is removed by submerging the chips in three acetone baths (the first one overnight). They are finally rinsed with IPA and left to dry.

4.1.2 Mask design

The mask design is described with a bottom-up approach. First, the elementary mask building blocks are described and only then it is shown how they are gathered into chips and wafers. All masks designs have been drawn using a software known as L-Edit. Four lithography steps are needed in the process flow, hence four layers will be designed: gate patterning, silicon dioxide patterning, drain source patterning and graphene patterning.

The fundamental elements of the mask and therefore the first to be presented

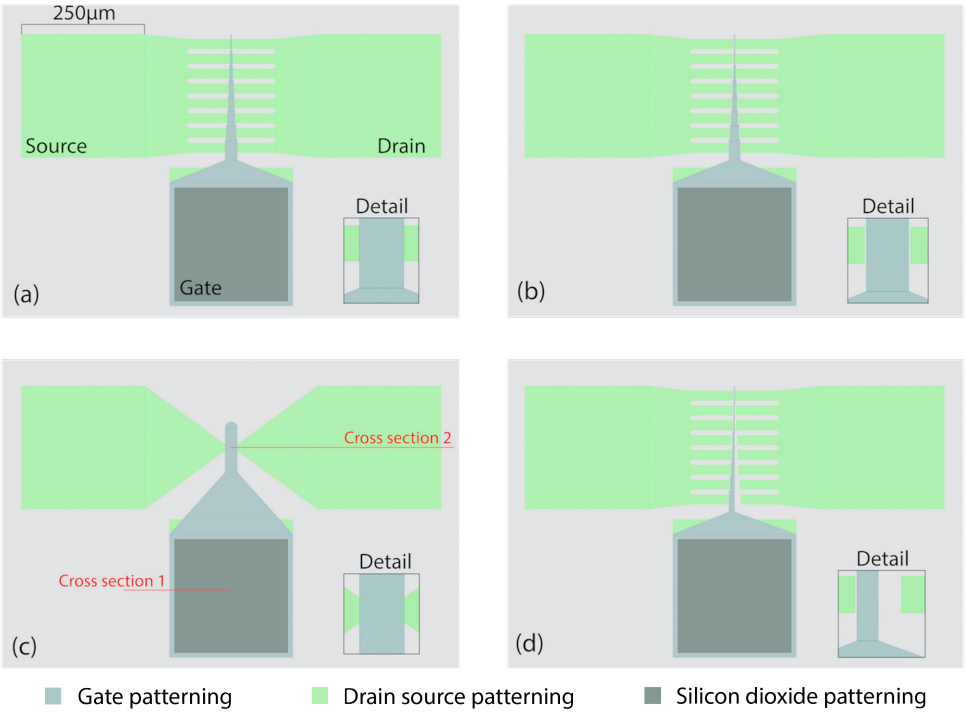

Figure 4.3 – Varieties of bolometer masks in the first fabrication run. (a) Zig-zag design with gate tip as wide as the gap between the source and drain electrodes, named EGT design. (b) Zig-zag design with gate tip slightly narrower than the gap between the electrodes, named NGT design. (c) Single-beam design with gate tip overlapping with the electrodes, named OGT design. Many similar designs of this type are present on the chips with varying gap width L_g (c) Zig-zag design with gate tip covering only half of the gap between drain and source, named HGT design. Cross sections 1 and 2 were used earlier to describe the process flow.

are the *bolometers* themselves. The maximal dimensions of suspended graphene beams that can be achieved with the fabrication technique employed in this project were unknown and therefore many different dimensions needed to be explored. For this reason, all designs shown in **figure 4.3** have different gaps L_g between the drain and source electrodes allowing different graphene beam lengths. The designs are named: (a) Equal Gate Tip (EGT), (b) Narrow Gate Tip (NGT), (c) Overlapping Gate Tip (OGT) and (d) Half Gate Tip (HGT). The width of the graphene beam is later tailored when the graphene mask is designed. The zig-zag designs (a), (b) and (d) allow to test many graphene beams lengths, once at a time, on a single device by simply changing the graphene mask. This is a great advantage because once the graphene dimensions are optimised, the to-

tality of devices can be used. However, design (c) has an additional parasitic capacitance between the drain-source electrodes and the gate tip. The latter would be much larger for an equivalent zig-zag design, consequently it is a better choice to adopt a single beam design and repeat it on the chips for different values of L_g. All bolometers types can be found in Appendix B. The gate tip metal thickness is the cause of a bump between the source and drain electrodes. The position of this bump could affect the graphene transfer and release procedure and therefore the three designs (a), (b) and (c) were made (the bump can be seen in **figure 4.24**). Each one of these designs has the bump in a different position as a consequence of the gate tip position with respect to the drain and source electrodes. The HGT device will be gathered on the wafer with the test structures that will be described later. When the bolometer is used as a resonator, the HGT design should make it easier to excite the graphene beams in their even modes. At this point, it should be reminded that each of the colour in these figures represent a mask for a photolithography step. The CD of all layers combined measures 2μm and the fabrication require a total of four lithography steps (the graphene lithography mask is omitted from **figure 4.3** and discussed later).

Another useful feature on the mask are the *test structures*. These structures not only allow to measure some of the electrical properties of graphene, but they also allow to estimate the graphene quality and to some extent the quality of the graphene transfer procedure. In fact, many of these electrical properties vary in function of the ripples on the graphene sheet, the number of defects in the graphene, the cleanliness of graphene and much more. Hence, by comparing these properties with the intrinsic theoretical values of pure graphene we can establish the quality of this 2D-material. Nevertheless, the primary usage of the test structures is to measure the contact resistivity ρ_c between gold and graphene and the sheet resistivity ρ_s of graphene. The graphene must be suspended in order to prevent these electrical properties from being affected by the insulating substrate on which it lie. **Figure 4.4** doesn't exhaustively show all test structures designed, but only the principal ones. On the chips there will be some variations in shapes and dimensions, but not in physical working principle. The sheet resistivity can be estimated by using the van der Pauw method and the structures (a) and (b) [41–43]. The contact resistivity can be estimated with the Cross Bridge Kelvin Resistor (CBKR) structure (d) following reference [44]. These two measurements can be combined by using the Transmission Line Measurement (TLM) structure (c) [42, 45, 46].

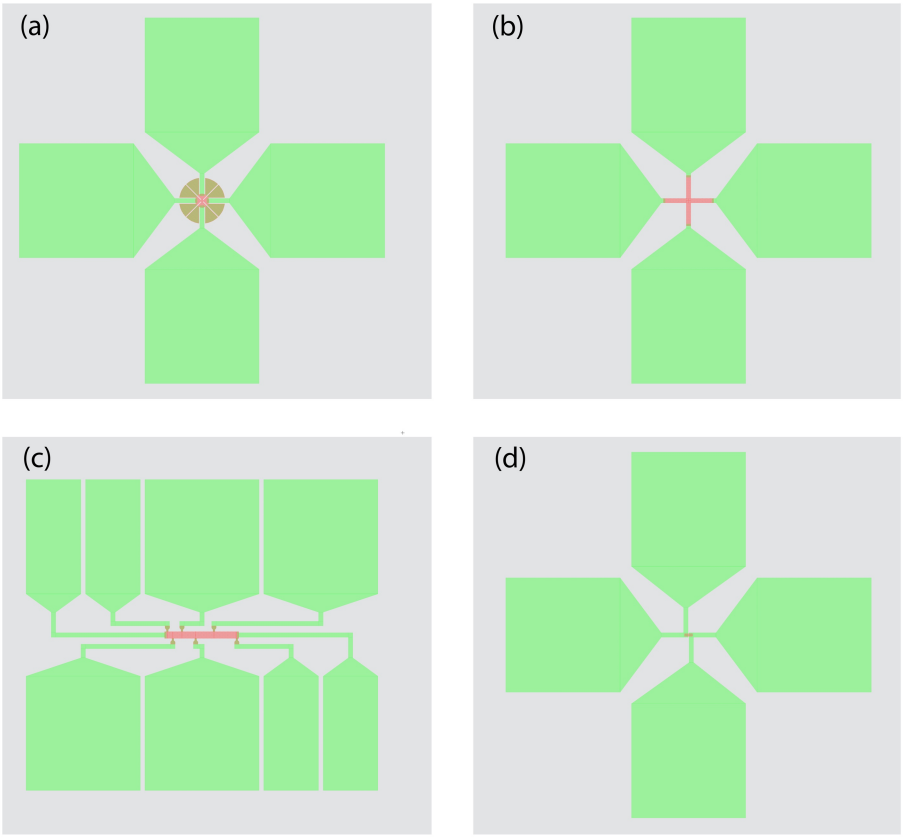

Figure 4.4 – Test structures for graphene characterisation. (a, b) Van der Pauw cloverfild and Greek cross structure for measuring the sheet resistivity and the Hall coefficient. (c) TLM for measuring sheet resistivity and contact resistivity. (d) CBKR for measuring contact resistivity.

Some *miscellaneous structures* will be now discussed. **Figure 4.5a** shows the alignment marks for lithography steps on wafers and chips and alignment marks for dicing of wafers into chips. These marks may strongly vary depending on the tools used and if automatic alignment is available on the image processing techniques employed by the tools softwares for automatically finding the crosses centres. The exposure grid shown in **figure 4.5b** was used to perform exposure tests on dummy wafers allowing to determine the optimal lithography parameters and it had equally been placed on the processed wafers and chips to verify the quality of the lithographies.

Figure 4.6 shows how all the features presented so far are *organised into chips and into the final wafer* design. There are four types of 10mm square chips. The first three contains each only one of the designs shown in **figure 4.3a,b,c**, while

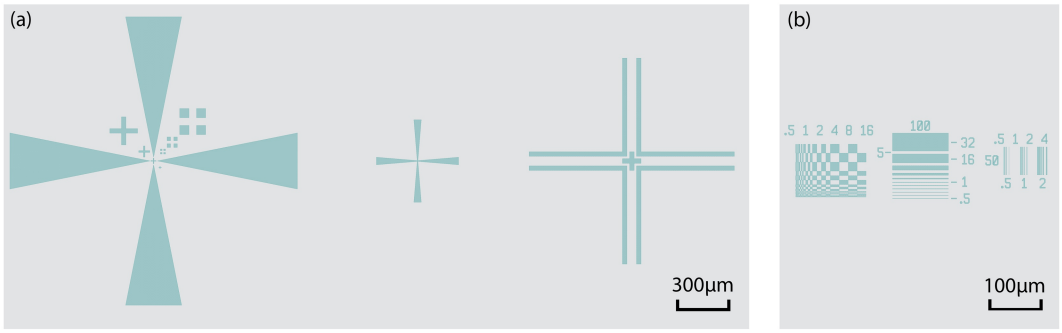

Figure 4.5 – (a) Starting from the left: alignment cross for the lithography steps on the wafer, alignment cross for the alignment of lithography steps on the chips and dicing cross for saw alignment. (b) Exposure grid for exposure tests and for verifying the quality of lithographies on the processed wafers and chips [47].

the fourth contains the test structures of **figure 4.4** and the HGT bolometer of **figure 4.3d**. The detailed distribution of the bolometers and test structures on the chips can be found in Appendix B. When placing the bolometers designs types on the mask it should be kept in mind that the graphene transfer is better at the centre of the chip. Each chip contains 96 bolometers and each bolometer is labeled by a row (R) and column (C) number, this makes is easier to identify them when observed under the microscope. Additionally, each chip has a label indicating the wafer number and a chip number. Each wafer contains 62 chips. Letters in the chip labels are $\sim$500μm tall allowing reading with the naked eye. This is comfortable when handling the chips after dicing. Thus, each bolometer is uniquely identified by a set of numbers: wafer number, chip number and column and row numbers. This numbering method is very useful because, for instance, some of the processes are not uniform across the wafer surface and therefore knowing the region where the bolometer comes from could give some insight on its properties. Both the wafer and the chips are equipped with the necessary exposure grids, alignment marks and dicing crosses. The chips are not randomly organised on the wafer. As it was mentioned earlier, the properties of the chips varies across the wafer surface and therefore it is preferred to place an equal number of EGT, NGT and OGT chips at each fixed distance from the wafer centre. Seven of the 62 chips on the wafer contains only test structures, three are in the centre and four on the edge.

The last structure to be discussed concerning the design is the *mask used for graphene patterning*. As already mentioned before, the suspension of graphene

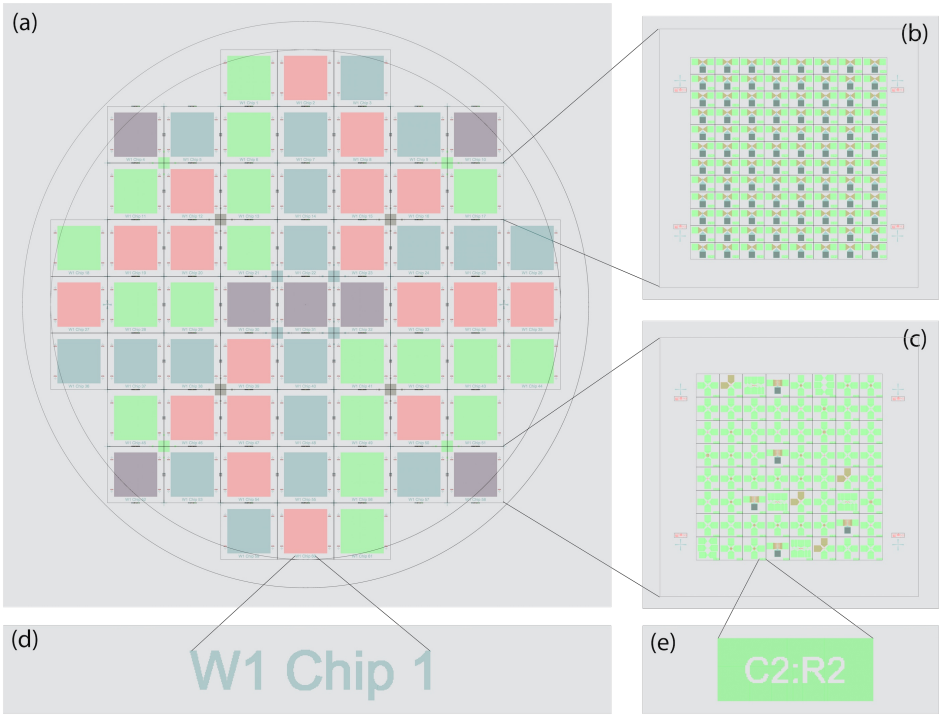

Figure 4.6 – (a) Simplified mask of the ∅100mm wafer. Each coloured square correspond to a different chip type. (b) Chip containing the bolometers (EGT, NGT or OGT). Each chip accomodate only one of the three types of bolometers. (c) Chip containing the test structures. (d) Label enumerating the wafer number and the chip number. (e) Label showing the column (C) number and row (R) number of the bolometer. The wafer and chips additionally contains the following structures: exposure grid for lithography steps verification, squares for metal and oxide thickness measurements, alignment marks for lithography layers, dicing crosses and alignment crosses and exposure grid for single chips.

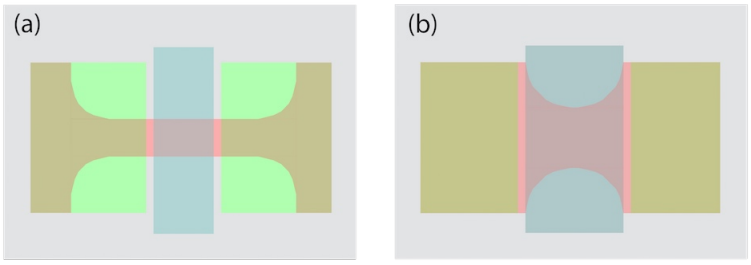

Figure 4.7 – Graphene masks for a NGT design. (a) Chronologically first design tested for the graphene beam. (b) Improved graphene beam design with better mechanical support. In red the graphene mask, in blue the gate tip and in green the drain and source electrodes.

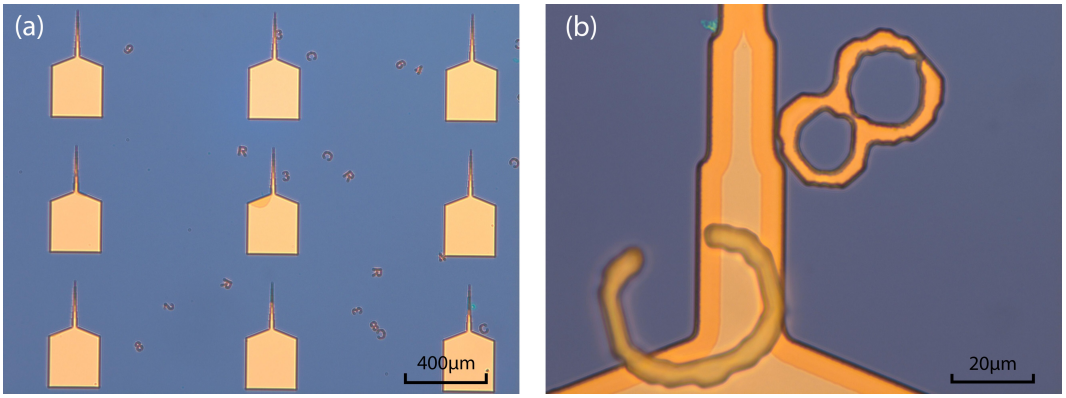

Figure 4.8 – Delamination of the chromium-gold layer on silicon dioxide during wet etching with the commercial chromium etchant: ready-to-use CR7 $(NH_4)_2Ce(NO_3)$ + $HClO_4$ and gold etchant: commercial ready-to-use $Kl(25g/l)+I_2(12g/l)$. (a) Only tiny structures were delaminating. (b) A rim was also generated during etching.

beams through the fabrication techniques used in this project has still to be explored and therefore the optimal beam shape is still unknown. Many designs will be tested to try having the best mechanical properties and preventing the beams from collapsing. The designs shown in **figure 4.7** are two examples of such. The contact surface area between the gold pads and the graphene must be large in order to minimise the contact resistance negative effects.

4.1.3 Issues encountered and solutions

Delamination of chromium-gold layer

The first problem encountered during the first fabrication run was the delamination of chromium-gold tiny structures from the thermal oxide of the wafer. This issue was first encountered after resist stripping after the first wet etch (3.x in **table A.1**). The evaporated metal layer was 5/25 nm of Cr/Au. **Figure 4.8** shows how the bolometers labels delaminated and flew all around the wafer. To compensate for the missing labels, they were re-drawn in the source-drain layer. The same delamination happened with some of the gate tips. Another minor problem during this fabrication step is the rim that can be seen in **Figure 4.8b**. In order to avoid slowing the fabrication down, the same issues were regenerated on a test wafer and possible solutions were explored on the test wafer instead of the processed wafers.

The test wafer had a pre-patterned layer of 10/100 nm Cr/Au on 285nm of

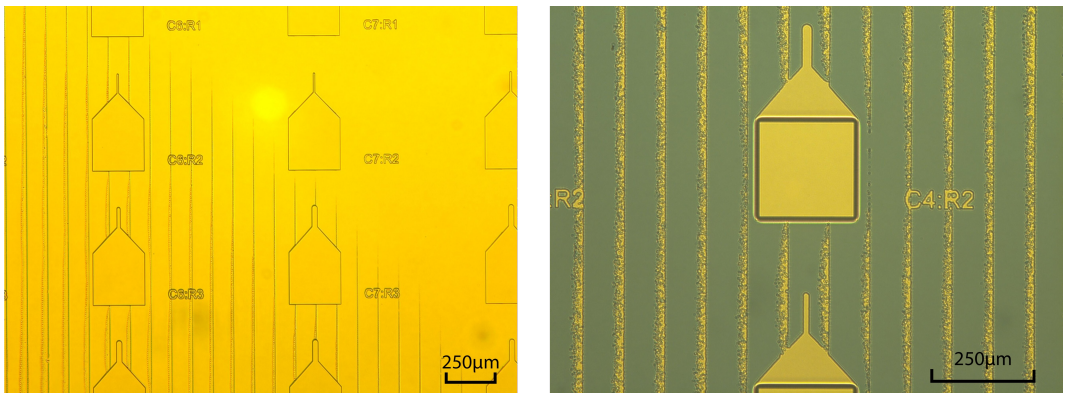

Figure 4.9 – Exposure non-uniformity across the wafer. The exposure grid showed a very good exposure in the centre of the wafer, while under-exposure stripes appeared on the bottom edge of the wafer. These stripes result in gold stripes after wet etching.

thermal silicon dioxide. To prevent similar problems for the source-drain layer, different etching of 10/100 nm Cr/Au were tested: (i) in the commercial ready-to-use CR7 $(NH_4)_2Ce(NO_3)$ + $HClO_4$ as was done with the processed wafer, (ii) in the ready-to-use solution: Cr selective over Cu $KMnO_4$ + Na_3PO_4 and (iii) in oxygen peroxide (H_2O_2) at 50° [48]. The ready-to-use CR7 etchant showed delamination of tiny structures but no rim, oxygen peroxide showed no etching of chromium at all and the Cr selective over Cu etchant showed no delamination and no rim whatsoever.

In conclusion the origin of the rim was not completely discovered, but the delamination problem was solved (for a 10/100 nm Cr/Au thicknesses and not 5/25 nm) by employing a different chromium etchant. This alternative was applied for the second wet etching (9.x in **table A.1**) and worked perfectly, no rim was observed either. This suggests that the origin of the rim could be the gold etchant (not used in this test) or the different Cr/Au thicknesses. This problem will be revisited in the second fabrication run. Later Scanning Electron Microscope (SEM) pictures seems to reveal that the rim was chromium over-etching.

Uniformity of the exposure intensity

In this fabrication run all lithography steps were done with direct writing with the same tool: the Heidelberg MLA150. This tool operates for h-lines photoresists only and the resolution is limited at around 1.2-2 μm, which is close to the CD of the masks presented earlier. It was observed that this tool can be source

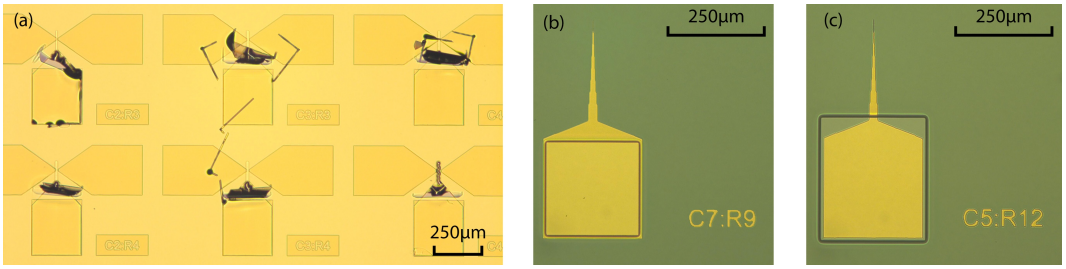

Figure 4.10 – Delamination of silicon dioxide on gold. (a) 250nm of low quality sputtered oxide delaminating away from gold. (b) 250nm of high quality sputtered oxide on gold. (c) New design minimising the contact area between high quality sputtered oxide and gold.

of exposure intensity non-uniformities across the wafer. This could be a consequence of the low quality of the vacuum clamping that doesn't flatten the wafer if slightly bent. Consequently, the distance between the writing head and the wafer is not constant across the surface and non-uniformities in exposure can arise. The result of this issue is shown in **figure 4.9**. The test exposure grid in the center of the wafer revealed a good exposure, while on the bottom edge of the wafer some stripes of resist appeared. This kind of resist strips are normally sign of under-exposure. Thus, the exposure was not uniform.

A solution for this issue is to use a much more versatile tool for direct writing named: Heidelberg VPG200. The latter has a much better vacuum clamping, it works for i-line photoresists, it has three different writing heads (20mm, 5mm and 2mm) reaching resolution well below 1μm even with the 5mm writinghead and multiple wafers can be loaded. This tool will be used for the second fabrication run with a 5mm writing head. The main drawbacks are: more difficult to perform alignments, a longer exposure time if the 5mm writing head is used. This machine was tested and never produced any stripe as the MLA150 did. Additionally, the lithography quality is observed to be superior to the one obtained at the MLA150.

Delamination of silicon dioxide

The low adherence of gold on silicon dioxide is a well known problem in literature and this is typically solved by introducing a adhesion layer of another metal between the gold and the oxide (in this project chromium was used). In the fabrication of bolometers, silicon dioxide is sputtered in argon atmosphere (low quality SiO_2) on gold and then patterned (**figure 4.1d,e**). The poor ad-

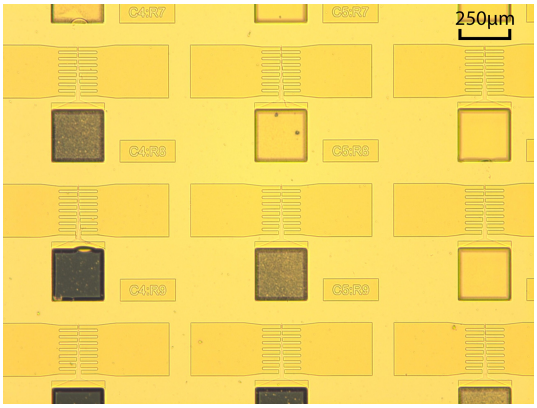

Figure 4.11 – Variations of the etch rate of silicon dioxide across the wafer due to the non-uniformity of the quality of silicon dioxide sputtered in argon atmosphere.

hesion between these two materials causes breakage and delamination of the oxide portions lying on gold as shown in **figure 4.10**. This issue is more frequent for thinner layers of silicon dioxide. The reason may be that in thicker layers, the SiO_2 lying on thermal silicon dioxide next to the gate pad offers the necessary mechanical support to the bands lying on gold to prevent them from breaking and delaminating. Again the fabrication was continued on these problematic wafers and solutions were tested on test wafers.

Higher quality SiO_2 is much denser and could provide the necessary mechanical support even for thin layers. A test wafer with the gate mask patterned on a 10/100 nm Cr/Au layer (instead of the usual 5/25 nm) was available and was used for testing solutions. This time, 250nm of silicon dioxide was sputtered in argon and oxygen atmosphere (high quality SiO_2) and then etched as it was done for the processed wafers. As shown in **figure 4.10b** the delamination disappeared. An even better design is shown in **figure 4.10c**. Given that the contact surface between gold and SiO_2 is minimised, the risk of delamination is reduced.

In the next fabrication run only high quality sputtered silicon dioxide will be used and the design shown in **figure 4.10c** will be adopted.

Quality of silicon dioxide across the wafer

Another problem caused by silicon dioxide sputtered in argon atmosphere (low quality SiO_2) is the non-uniformity of its quality across the wafer. In fact quality decreases from the centre to the edge of the wafer. The etch rate is consequently affected. It is higher on the edges and lower in the centre. In order to avoid ex-

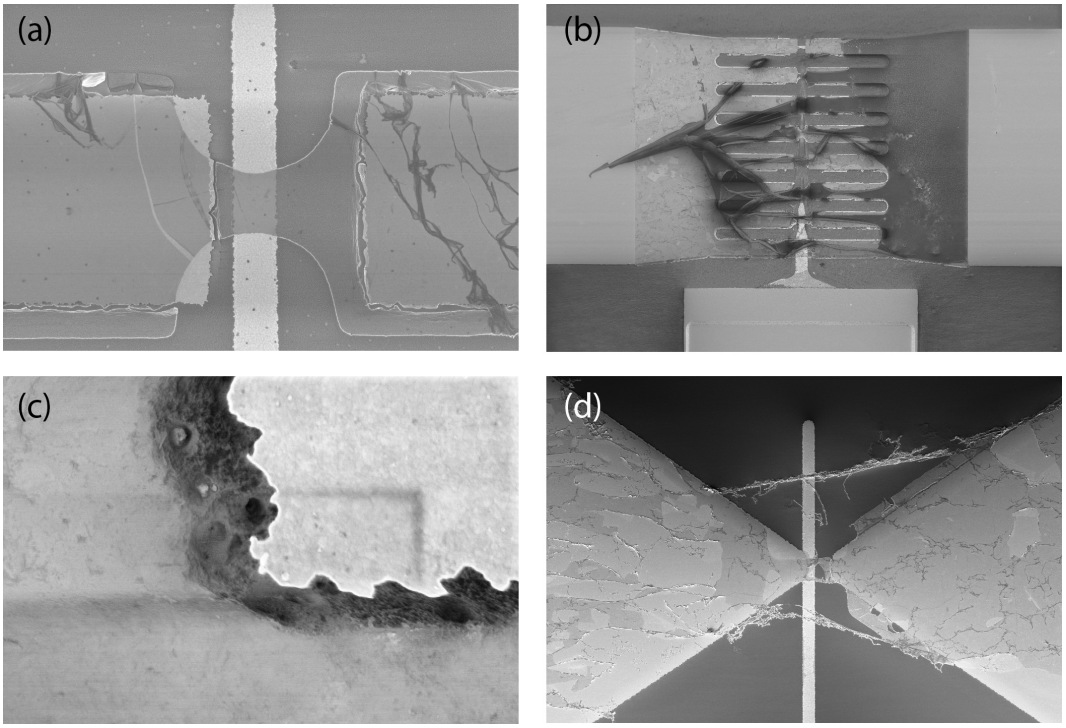

Figure 4.12 – Issues with graphene transfer, patterning and release. (a) Many graphene beams breaks at the edge of gold. (b) Photoresist residues are often found on graphene and it is difficult to get rid of them. (c) The jagged edges of gold could be a major cause of the graphene breakage at the gold edges. (d) Polymer residues and rolled-up chunk of graphene are also found.

treme over etching on the contour of the wafer some of the devices in the centre must be sacrificed because the silicon dioxide on gold pads is not completely removed. **Figure 4.11** clearly shows this non-uniformity.

This problem is also solved by the employment of high quality sputtered oxide. The uniformity is much higher and it is possible to etch all the SiO_2 from all devices in the centre of the wafer without having too much over etch on the contour of the wafer. It should be noted that if the gate is connected to an alternating source of current, the thin layer of silicon dioxide on the pad does not cause huge problems because it merely acts as a capacitance in series.

Issues with graphene transfer, patterning and release

Four main issues were encountered during graphene transfer, patterning and release. The first is the breakage of graphene at the gold edges as shown in **figure 4.12a**. This problem is probably enhanced by the jagged edges of the

gold (**figure 4.12c**). This is likely a consequence of the wet etching. Another problem is the difficulty of keeping the graphene clean. Residues of photoresist on graphene (**figure 4.12b**) and polymers with portion of rolled-up graphene (**figure 4.12d**) are often found.

Different solutions will be tested in the second fabrication run. For instance, lift-off with LOR could be used to have gold pads with smoother edges and therefore reduce the risk of breakage of graphene sheets. Different design of graphene masks were already tested in the first fabrication run (**figure 4.7**). Some design seemed to give more mechanical support to the graphene beam at the gold edges. To increase the cleanliness of the graphene, a protective layer or spin-on-glass silicon dioxide could be deposited onto the graphene before spin-coating the PMMA. This solution was explored, the spin-on-glass silicon dioxide was successfully etched by vapour HF when on a test wafer, but the wet graphene transfer was not working anymore because the graphene covered with SiO_2 was sinking in the etchant bath. Another option to reduce the polymer residues is to try different types of PMMA.

Generic improvements

Some additional improvements could be implemented. The first is related to the alignment mechanism of the lithography steps. The alignment marks shown in **figure 4.5a** were unnecessarily small and after exposure and development the small features got deformed. Consequently, the automatic alignment of the Heidelberg MLA150 was not working and thus all alignments were performed manually. In the future mask designs the alignment crosses must be improved to guarantee automatic alignment.

Moreover, as mentioned earlier, the etch rate of vapour HF is very difficult to control. As a consequence, it was very difficult to release the graphene without etching the thermal oxide on the wafer. A layer of AlO_2 could be deposited via Atomic Layer Deposition (ALD) on the thermal oxide. Aluminium oxide is not etched by vapour HF and it is an insulator. This layer would protect the thermal oxide from being etched.

It was also noticed during characterisation that the probe needles are easily aligned to the 250μm square pads. Thus, pads could be designed much smaller to increase the level of integration of bolometers on chips. The down side of having smaller pads is that the contact area between graphene and gold diminish and consequently the contact resistance increases.

Finally, the silicon oxide mask should be modified. Labels are patterned on

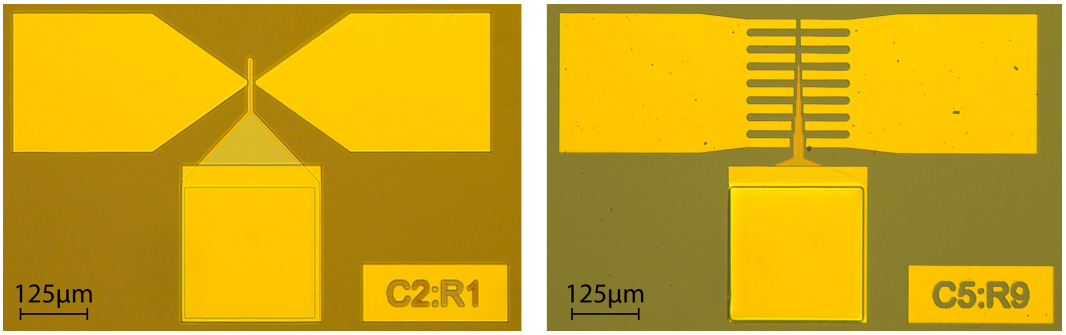

Figure 4.13 – Bolometers before graphene transfer. On the left hand side a OGT bolometer with a 300nm thick sacrificial layer of silicon dioxide, while on the right hand side a NGT device with a 3.2μm thick sacrificial layer of silicon dioxide.

the first gold layer and then covered with silicon dioxide. Consequently, they become invisible in the SEM because of the insulating properties of the SiO_2. Some openings should be added in order to make the labels visible.

4.1.4 Results

In this section the results of the first fabrication run will be discussed and presented. The goal is to highlight the positive outcomes, while the issues and possible solutions for the next fabrication run were extensively discussed in Section 4.1.3.

Figure 4.13 shows two bolometers just before dicing the wafer. The one on the left hand side is a OGT bolometer with a 300nm SiO_2 sacrificial layer, while the one on the right hand side is a NGT bolometer with a 3.2μm SiO_2 sacrificial layer. Although the first fabrication run was done hardly with any optimisation, the yield was higher than expected at this stage. However, no quantitative statistics was done. The most delicate part of the fabrication sill has to be done. **Figure 4.14** shows two suspended graphene beams produced successfully for a sacrificial layer of silicon dioxide of 3.2μm. The dimensions of the graphene beams in this pictures are approximately: length = 15μm and width = 8μm for the one on the left hand side, while length = 20μm and width = 10μm for the one on the right hand side. The yield at this stage was quite low, but it was observed that the structure on the right hand side survived more often than the other ones. This is probably due to a better mechanical support given by the graphene wings being outside the gold pad. Unfortunately, the low yield made impossible to make any statistics to extrapolate the optimal

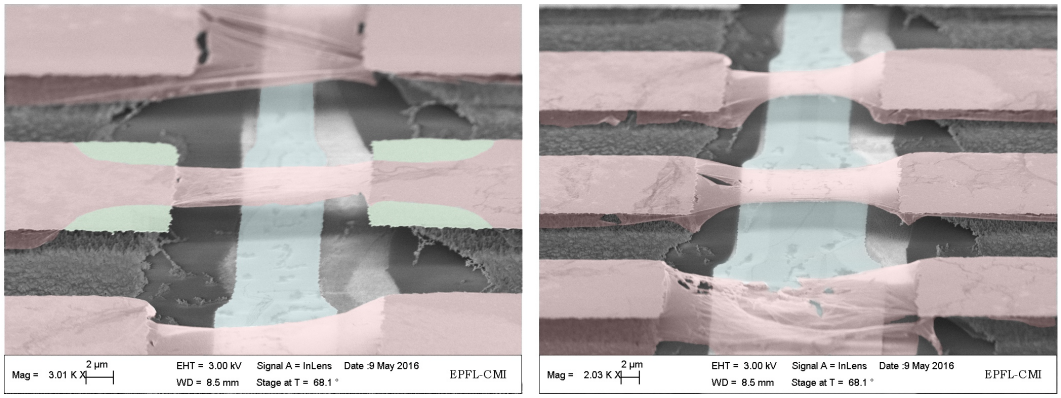

Figure 4.14 – SEM pictures of graphene beams obtained in the first fabrication run. The graphene masks designs and colours correspond to those previously shown for the masks designs. In this chip the gap between the graphene beam and the gate tip measures approximately 3.2μm. The graphene mask used for the fabrication of this chip was designed just to test the graphene release for different beam dimensions. This is the reason why, more than one beam connects the source to the drain.

graphene beam dimensions (from the fabrication point of view). It was still positively surprising to obtain such structures within the first fabrication run with practically any optimisation process.

4.1.5 Summary and conclusion

In summary the first fabrication run was very profitable. First, as expected, it gave a strong feedback and a number of solid improvements to be implemented in future fabrication runs. Second, it made possible to test the unconventional processes involving graphene. Last but not least, it was actually possible to obtain some very good structures such as those shown in **figure 4.14**. Some characterisation measurements are already possible on these devices.

Obviously the yield and quality of the devices still need improvement, but the results of this rather rushed first fabrication run were extremely positive and useful for the future. The outcome was actually better than expected.

4.2 Second fabrication run

The goal of the second fabrication run is to improve the fabrication of bolometers previously presented. This will be achieved primarily by following the feedback obtained during the first fabrication run. The target is to improve

both the yield and the quality. The major change is the use of lift-off instead of wet etching. There are many similarities with the first run and therefore only changes will be discussed. All subjects not treated can be considered similar or equal to those presented in Section 4.1. For instance, the test structures are unchanged and therefore they will not be presented.

The second fabrication run was only performed up to the dicing step before writing this thesis. Hence, graphene transfer, patterning and release will be performed only at a later time and will not be part of this report.

Detailed runsheets and recipies can be found in Appendix A and devices distribution on wafers and chips are shown in Appendix B.

4.2.1 Process flow

In this section the process flow of the second fabrication run will be discussed in detail. The problems and issues encountered will be discussed in Section 4.2.3. The entire runsheet with all recipes used at the CMi facility at EPFL can be found in Appendix A. The process flow contains four lithography processes and lift-off is used instead of wet etching.

The *process flow* of this run is illustrated in **figure 4.15**. The starting point is a ∅100mm SSP test p-type (0.1-100Ωcm) wafer with 285nm of wet thermal silicon dioxide (SiO_2) on both sides.

The first step was to pattern the gate electrodes on the wafers. Differently from what was done in the first run, now this is achieved with lift-off. If the directionality of the evaporation is not perfectly vertical, the deposition of gold on the side walls of the resist can generate fences on the gold structures. For this reason the lithography was done with a double layer: LOR plus resist. The LOR doesn't need to be exposed to be developed and it dissolves isotropically and faster than the resist lying on top of it. As a result, the LOR supports are narrower than the resist as shown in **figure 4.15b** and the risk of fences is reduced. The down side of lift-off is that patterns tends to be broadened compared to the mask design. It should additionally be kept in mind that the risk of having fences increases with the thickness of deposited metal because thin fences often breaks during lift-off. The CD of this lithography step is 1μm. The metal evaporation is done with 5/25 nm of Cr/Au and at the largest distance possible to increase directionality. The distance between the metal source and the target was 45cm in this case.

The sputtering and patterning of the silicon dioxide is performed as in Sec-

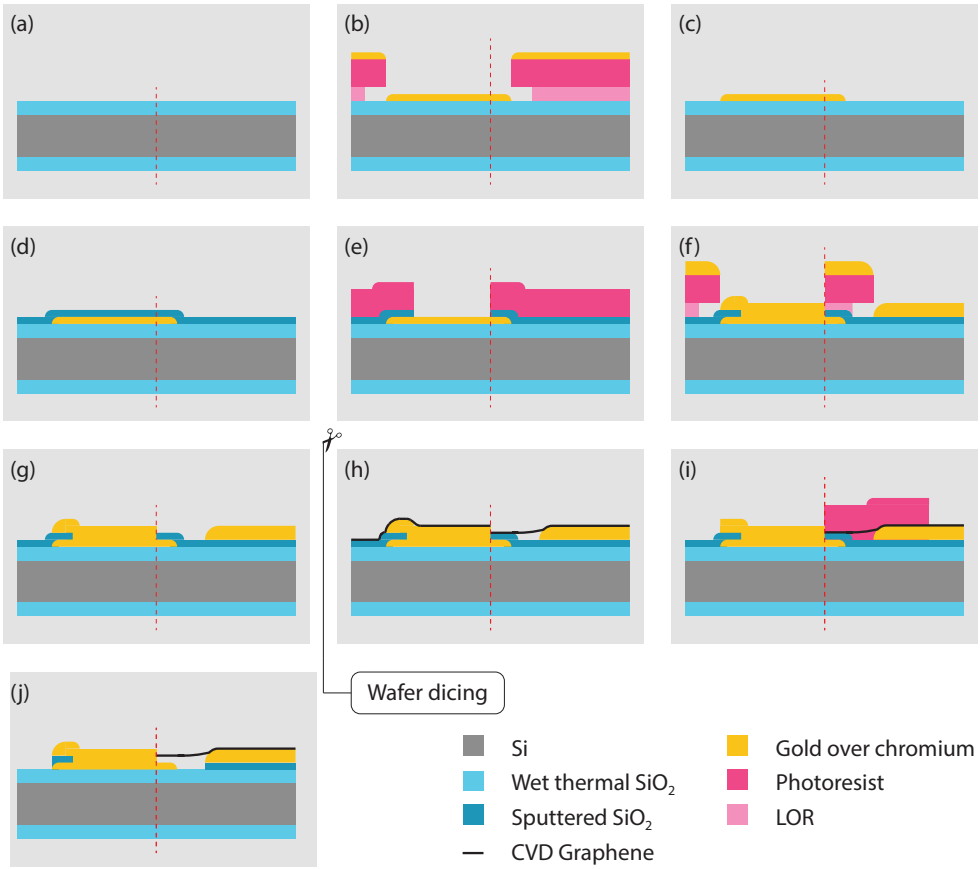

Figure 4.15 – Second fabrication run process flow. All figures are split into two in order to avoid redundant information due to the symmetry of the devices. In fact, the dashed red line can be seen as an axis of symmetry. On the left-hand side the schematic representation of the cross section 1 shown in **figure 4.16**, while the cross section 2 is represented on the right hand side. (a) The starting point is a silicon wafer with wet thermal silicon dioxide on both sides. (b and c) Lift-off is used to pattern the gate layer. This step includes a lithography step and a Chromium/Gold evaporation. (d) A layer of silicon dioxide is sputtered on the wafer. (e and f) Lift-off is used to pattern the source and drain layer as well. This step includes a lithography step and a Chromium/Gold evaporation. This drawing represent a NGT design. At this stage the wafer are ready to be diced into single 10mm square chips. (h) Graphene transfer. (i) The graphene is patterned through a lithography step and oxygen plasma etching. (j) Vapour HF etching of the silicon dioxide and graphene release.

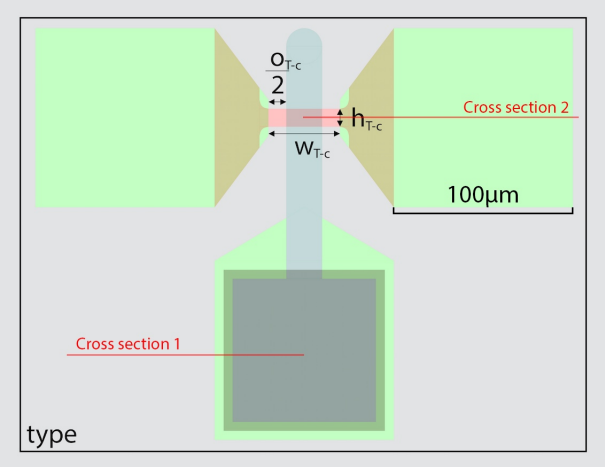

Figure 4.16 – Bolometer mask design in the second fabrication run. This design is generated by instancing a T-Cell. A T-Cell is a parametric `C` coded design. When the parameters: *type*, $w_{\text{T-c}}$, $h_{\text{T-c}}$ and $o_{\text{T-c}}$ are given to this particular type of cell, this design is automatically generated.

tion 4.1.1. The only difference is that 250nm or 2.5μm of silicon dioxide are now sputtered in argon and oxygen (O_2) atmosphere (high quality SiO_2). The etch time need to be increased as a consequence of the denser silicon dioxide.

The source and drain layer is patterned similarly to the gate layer, using lift-off. A thin film of 10/100 nm of Cr/Au is evaporated on the wafer at a distance of 45cm. This metal thickness is compatible with wire bonding. After lifting-off the wafers are ready to be diced into 10mm square chips as was done in the first fabrication run.

The fabrication was stopped just before dicing and will be pursued after completion of this thesis. For this reason the table in Appendix A is incomplete in the sense that the process stops after the second lift-off step. The graphene transfer will be performed following the wet transfer procedure shown in **figure 4.2** and the graphene patterning and releasing similarly to what was done in the first fabrication run.

4.2.2 Mask design

The strategy used to draw the mask for this fabrication run is slightly different compared to the previous one. Designs are still done using the L-Edit software.

L-Edit offers a very versatile way to draw masks, namely through T-Cells. T-Cells are basically parametric drawings coded in `C` language. The detail of the

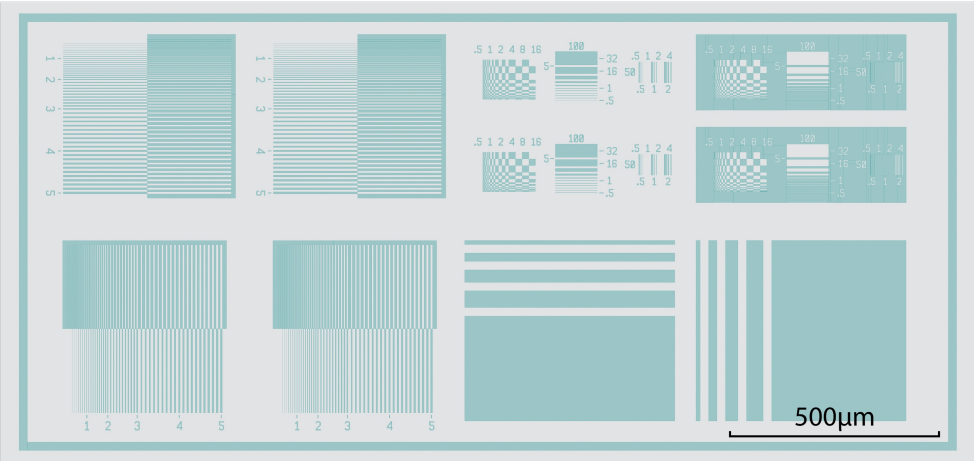

Figure 4.17 – Improved version of the exposure grid previously presented. this design is used for exposure tests and a portion of it is also placed all around the wafers and chips designs to help quantify the quality of the lithography steps.

C code is presented in Appendix C. Every time that a bolometer has to be designed in a mask it is done through the T-Cell and therefore through the C code. When the T-Cell is instanced, the program asks you four parameters: *type*, $w_{\text{T-c}}$, $h_{\text{T-c}}$ and $o_{\text{T-c}}$ and automatically draws the bolometer shown in **figure 4.16**. The *type* parameter is an integer that can have three different values: 1 = OGT design, 2 = NGT design and 3 = EGT design (here the parameter $o_{\text{T-c}}$ is not taken into account). Actually, the *type* variable is not strictly necessary for the moment because the full range of $o_{\text{T-c}}$ values could in principle generate all device types, but it may be useful for later modifications. There are two great advantages in using this method. The first one is that the different design are all automatically generating (time saving). And the second one is that all bolometers on the wafer are instanced through the same T-Cell, hence if the design must be changed it suffices to change the code and all bolometers on the wafer mask will change accordingly (versatility). A clear example of such changes are the modifications of the graphene mask to test different graphene beams structures. Devices are now smaller in response to the comments made in Section 4.1.3. The pads measure 100μm and one 10mm square chip can now accommodate 616 bolometers. The distribution of bolometers on chips is presented in Appendix B.

Exposure grid and alignment marks were also improved. The new exposure grid shown in **figure 4.17** has different designs with their negative equivalent. Having them one next to the other, makes it much easier to determine the level of over(under)-exposure of the wafer. It should be noticed that some tools don't

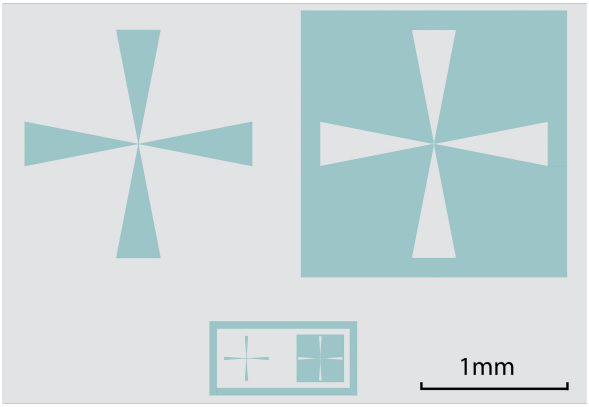

Figure 4.18 – Improved alignment marks for wafer (above) and chips alignment (below). Having the negative image of each design should lower the risk of having deformed alignment crosses.

have an equivalent resolution horizontally and vertically.

The *alignment marks* also have their negative just next to them (**figure 4.18**). This should reduce the risk of having deformed crosses (if one is deformed the other shouldn't). Now both the chips and the wafers designs have four alignment marks (four pairs) instead of only two as was done in the first run. This should further improve the alignment.

4.2.3 Issues encountered and solutions

In opposition to what was done in the first fabrication run, the majority of the issues discussed hereafter were already optimised within this fabrication run. The majority of the following issues were known and therefore solutions were pursued prior to the beginning of the second fabrication run.

Wet etching of chromium-gold layer revisited

During the second fabrication run, before switching to lift-off, some additional tests regarding the wet etching of the 5/25 nm of Cr/Au layer were performed. This issue was already partially discussed in Section 4.1.3-"Delamination of chromium-gold layer", but the solution found was not tested on such thin layers yet. All etching discussed hereafter were performed accordingly to the optimised procedure found in that section, but with two different types of resist. First with 1μm of resist type: ECI3007. When etched in the chromium etchant, pieces of resist were observed floating in the beaker. The final result is shown in

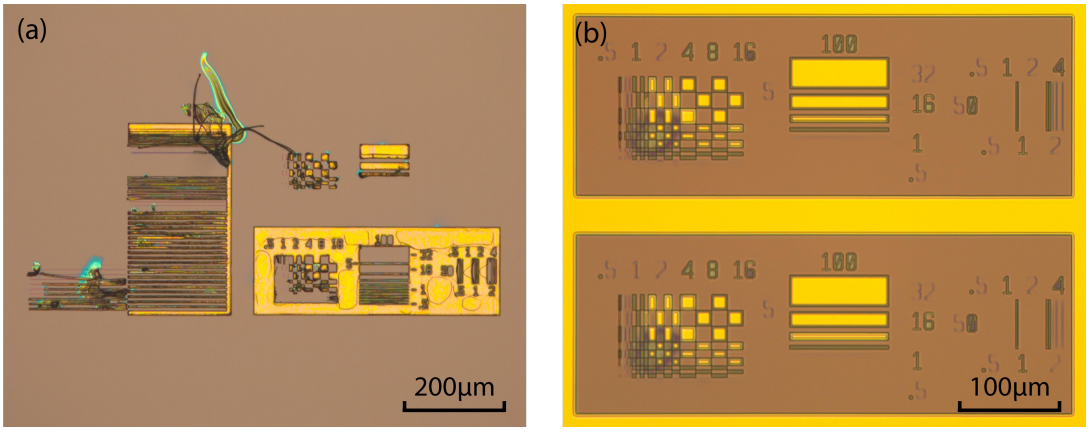

Figure 4.19 – Both figures show the status of some exposure grids just after wet etching of 5/25 nm of Cr/Au with still resist on them. (a) Resist type: ECI3007 with thickness: 1μm. (b) Resist type: AZ92xx with thickness: 2μm.

figure 4.19a. The second test was done with 2μm of resist type: AZ92xx (used in the first run). This did not work well either and a large over-etching of gold was observed (**figure 4.19b**).

In conclusion, the thin Cr/Au layer seems to be source of many problems when wet etching is performed. This kind of issues can significantly decrease the repeatability of the fabrication. Adding this to the previously discussed down sides of wet etching for this process, it further suggests that another procedure needs to be found.

Fences generated by lift-off

As it was already claimed earlier, it is critical that the drain and source gold pads have smooth edges. This is necessary in order to prevent the graphene from breaking when it is transferred and released. As can be seen in the pictures on the left hand side of figure **figure 4.20** the lift-off was initially problematic. Fences were generated by this processes for all gold thicknesses. They were less present for the 5/25 nm metallic thin film because they probably broke away during lift-off. In fact, fences are only present at the pads corners where the fence has more mechanical support. This results are unacceptable for this application.

The origin of the fences is the residual deposition of gold and chromium on the LOR due to the imperfect directionality of the evaporation. The development of the double layer resist plus LOR was done with a pre-made recipe in

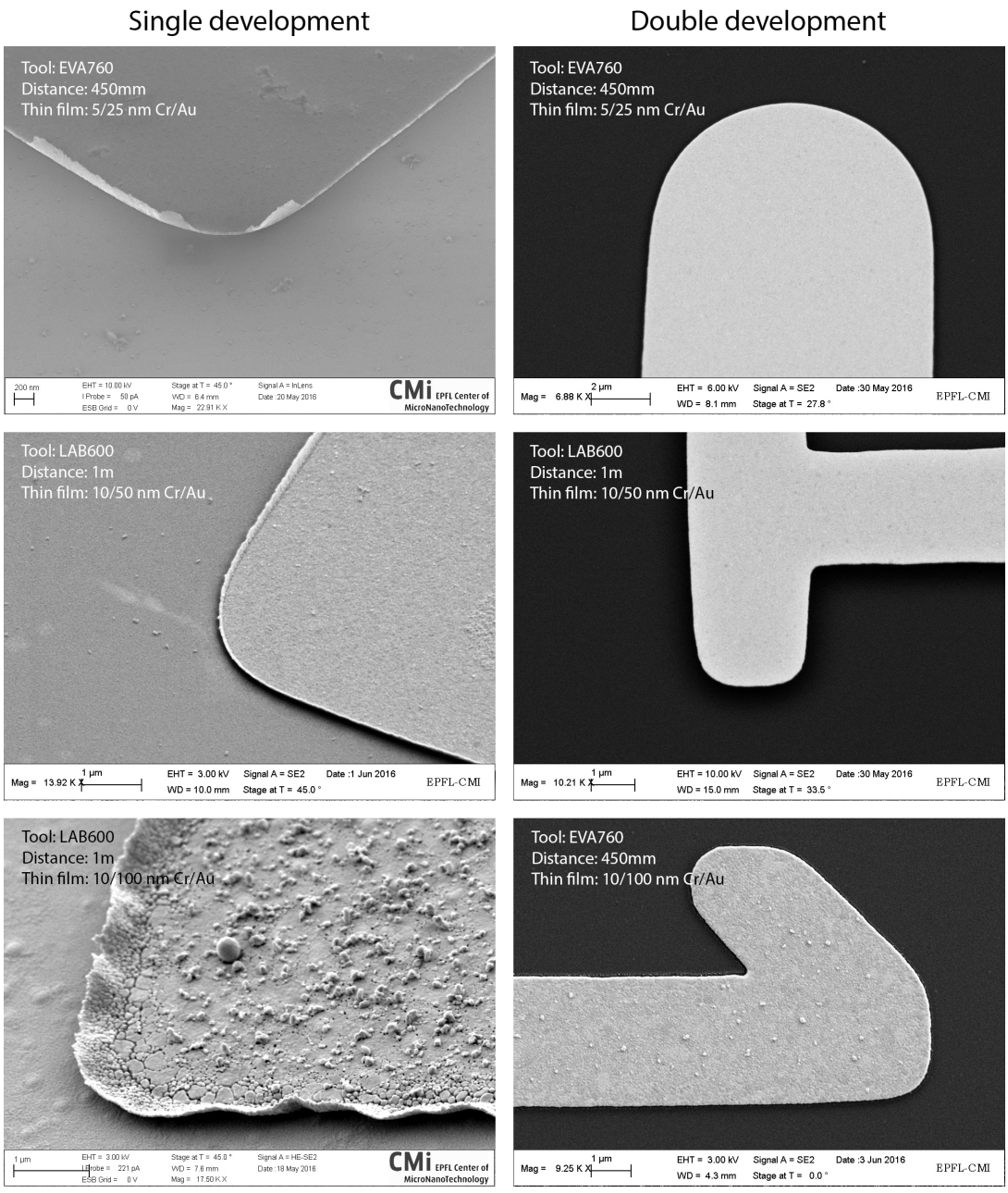

Figure 4.20 – The figures on the left hand side shows fences on gold pads due to residual deposition on the LOR in the lift-off steps. The problem is solved by developing twice (right hand side). In fact, this procedure further dissolves the LOR decreasing this risk of having fences. In fact, the pictures on the right hand side do not have fences whatsoever.

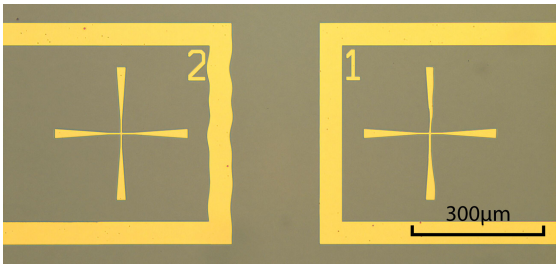

Figure 4.21 – Wiggly lines in lithography with the Heidelberg VPG200 tool. These kind of defects were rare and harmless for the fabrication process.

the ACS200 tool as can be seen in step 1.3 in **table A.2**. Developing the wafer twice prevalently affects the LOR because in opposition to the resist, it doesn't need to be exposed to be dissolved. By further shrinking the LOR features with a second development, fences completely disappeared for all thin film thicknesses as shown on the right hand side of **figure 4.20**.

This solution was successfully implemented in the second fabrication run (step 1.4 in **table A.2**). The reader should be aware that double developing the wafer could dissolve the totality of the LOR lying under the resist causing thin features to peel off. It was not the case for the designs used in this process flow, but this effect was observed in the exposure grid. In other words, this solution could provoke a loss of lithographic resolution and broadening of some features. Masks can be adapted accordingly.

Lithography quality on the wafer edges

Another minor harmless issue is related to the exposure using the Heidelberg VPG200 tool. Although the lithographies were of much higher quality and better alignment precision compared to those performed with the Heidelberg MLA150 tool, some imperfections were still observed. Namely, at the edges of the wafer few features resulted in wiggly lines as shown in **figure 4.21**. This was absolutely not a problem for this fabrication run, but the reader should be aware that this kind of seldom distortions may happen, specially on the wafer edges. No solutions were pursued to solve this problem.

4.2.4 Results

In this section the results of the second fabrication run are presented and discussed. **Figure 4.22** shows an optical microscope image of two bolometer types,

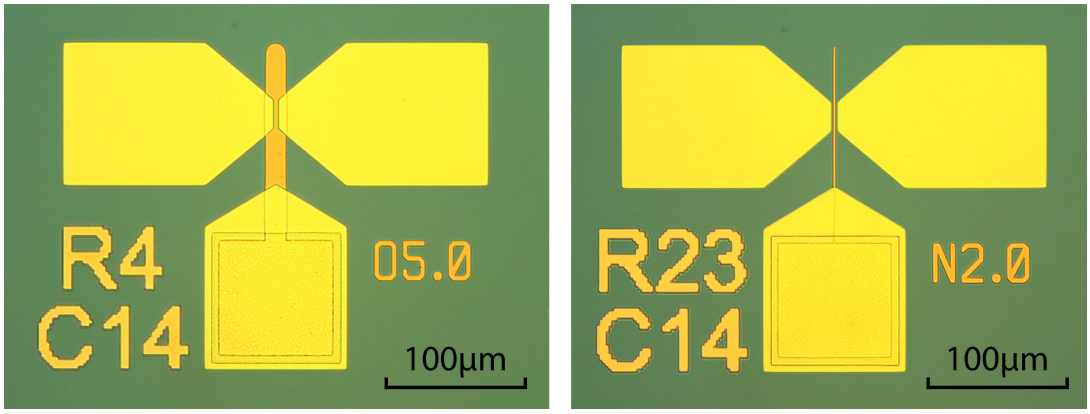

Figure 4.22 – Optical microscope image of the second run bolometers. On the left hand side the OGT design, while on the right hand side the NGT. The labels on the left of the gate pad define the location of the bolometer on the chip, while those on the right define the bolometer type.

namely the OGT on the left hand side and the NGT on the right hand side. Both bolometers have a sacrificial layer of approximately 250nm of SiO_2. All bolometers types were successfully fabricated and the high uniformity of SiO_2 across the wafer surface allowed to obtain a very high yield up to this point. Devices coming from all wafer regions (centre or edge) seem to have very similar geometry and properties. The only glitch observed at this point is the broadening of the gold features due to the double development and the natural consequence lift-off. This issue can easily be fixed by adapting the mask design.

Additional images taken with the SEM are shown in **figure 4.23**. The silicon dioxide mask for wet etching was designed to etch the bolometer column and row numbers, while the bolometer type label is covered by SiO_2. That is the reason why the former are the only visible in the SEM pictures.

Last, but not least, **figure 4.24** shows the detail of the the drain-source electrodes where the graphene beam is supposed to be suspended. The gold pads obtained with lift-off are extremely smooth at the edges. It can be seen that the bump generated by the gate tip thickness is in different positions depending to the design type (NGT on the left, while OGT on the right). This bump could affect the graphene transferring and release. Consequently both designs need to be explored to determine which one is more convenient. Clearly, an additional parasitic capacitance is present for the OGT design.

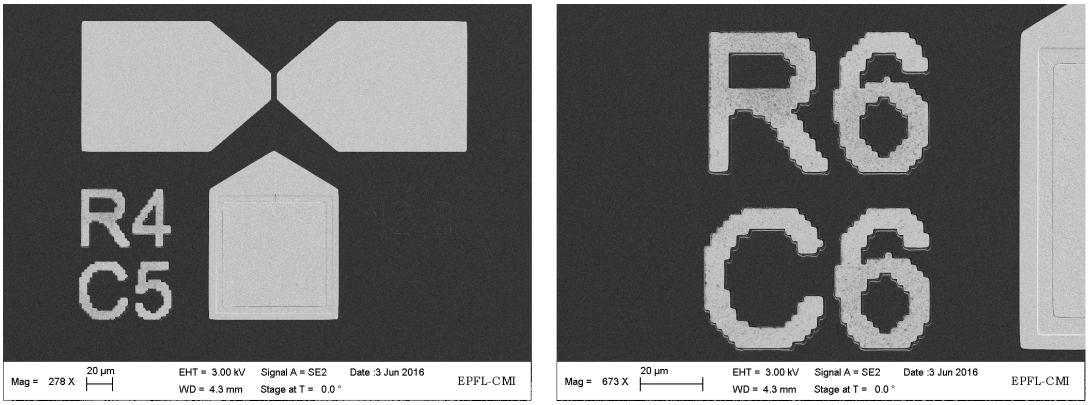

Figure 4.23 – SEM image of the second run bolometers. On the left hand side the whole bolometer, while on the left hand side the row and column numbering. Gold features covered by sputtered silicon dioxide are almost invisible.

4.2.5 Summary and conclusion

In summary the second fabrication run, which was completed up to the dicing step, was extraordinarily positive. The gold pads have good smoothness at the edges. The graphene transfer will be positively affected by this fact. As previously mentioned, hardly any non-uniformities across the wafer were observed (specially for thin sacrificial layers of SiO_2). Hence, the chips on the wafer edges are expected to have the same geometry and properties as those in the centre. This is already reflected in an higher yield. There are no regions on the wafer that looks better or different than others.

In conclusion, the outcome of the second run was promising and will hardly need further optimisations. The goals of the second fabrication run, to increase the yield and quality of devices, were succesfully fulfilled up to this fabrication point.

4.3 Comparison

From the discussions presented in Sections 4.1.4 and 4.2.4 it is already clear that the second fabrication run outcome showed a huge improvement. Among the improvements made, the most important are: higher yield, better uniformity of properties among chips coming from different wafer regions and smoother gold pads. All issues discussed in the first fabrication run up to the dicing step seem to be solved by the processes followed in the second run.

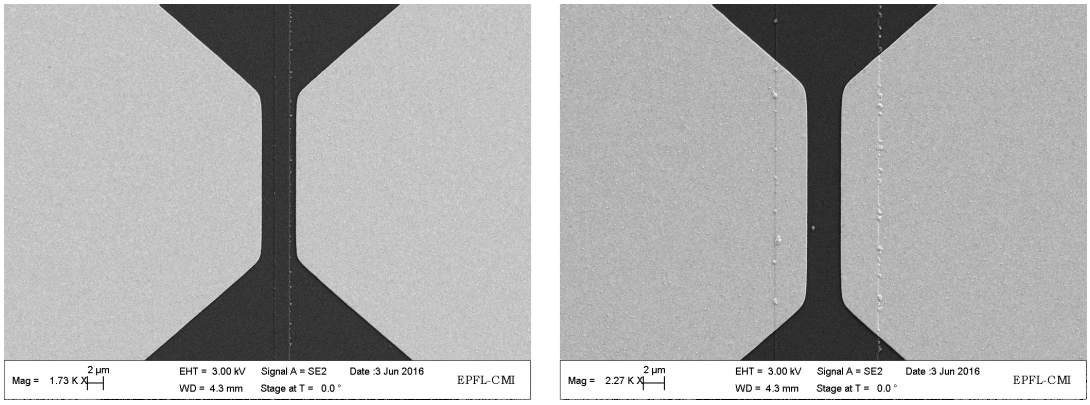

Figure 4.24 – SEM image of the meeting point of the source and drain electrodes. the suspended graphene beam is supposed to be suspended between this pads as was seen previously. On the right hand side the NGT design, while the OGT design on the right. They both have a 250nm sacrificial layer of SiO_2. The bump generated by the gate tip thickness is clearly seen in both images.

Despite that, the advantages of the second fabrication run are not only seen through the results. In fact avoiding wet etching makes the fabrication less painful and increases the repeatability of the process. In fact, inconsistent problems as those discussed in Section 4.2.3-"Wet etching of chromium-gold layer revisited" are completely avoided. There are almost no critical steps in the second run process flow and therefore it can be consistently repeated.

5 | Characterisation

In this chapter the firsts steps toward the electrical characterisation of graphene beams are discussed. Hereafter, graphene beams on silicon dioxide before release will be considered. The electrical properties of graphene are probably modified by the insulating silicon dioxide substrate and are probably different to those of suspended graphene beams. In fact, it is claimed that the high graphene conductivity is a consequence of quantum confinement. Electron scattering is limited into one plane and therefore less scattering channels are available resulting in longer free paths and higher conductivity. Intuitively, having a substrate may slightly mitigate the two-dimensional constraint affecting the electrical properties. The measurements done in what follows are made on chips fabricated following the process flow of the first fabrication run.

5.1 Graphene beams on silicon dioxide

In this section electrical measurements on graphene beams lying on silicon dioxide are studied. Two electrical characteristics of graphene are particularly important in what follows: sheet resistivity ρ_s and contact resistivity ρ_c of graphene on gold. The test structures shown in **figure 4.4** allow experimental measurements of these properties. Unfortunately, this was not done before writing this thesis due to time constraints. These measurements will be for sure explored in the future.

The contact resistivity between semiconductors and metals is crucial for electronic devices. Similarly the metal-graphene contact resistivity in graphene-based electronics critically affects its performance. Realising low contact resistance between graphene and metals is an ongoing challenge and the reported values range from hundreds to thousands of $\Omega\mu m^2$ [49]. There are models claiming that the contact resistivity is not ohmic and depends on the voltage applied across the junction [50]. Apparently, graphene-metal contacts shows unique characteristics, very different from those exhibited in semiconductors-

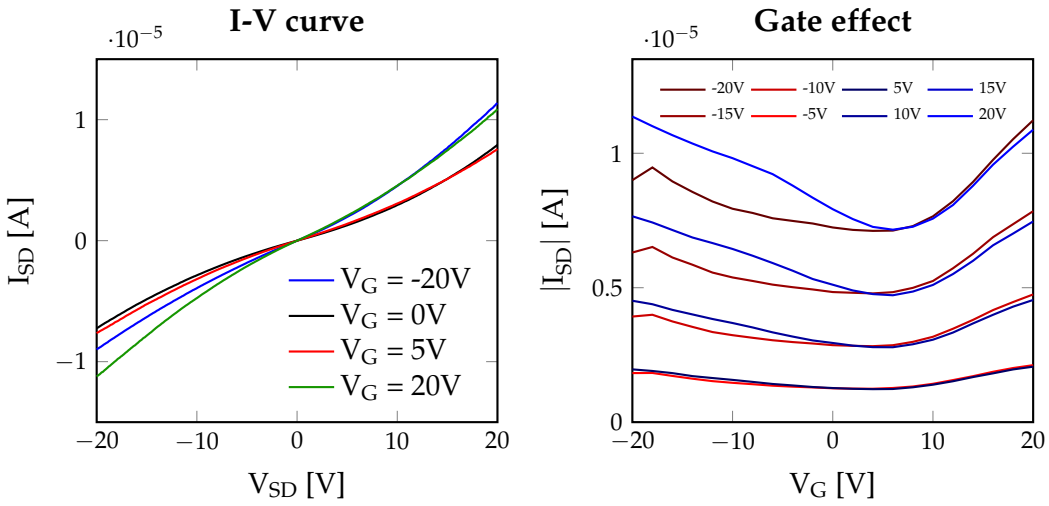

Figure 5.1 – I-V curve and gate effect on a graphene beam. I_{SD} is the current flowing between the source and drain, V_{SD} the source-drain applied voltage and V_G the gate voltage. The graphene beam was lying on a 300nm sacrificial layer of silicon dioxide and was 2μm long and 1μm wide. The metal-graphene contact surface was approximately $20 \cdot 10^3 \mu m^2$ per electrode. The right curves on the left hand side graph are drawn for V_{SD} ranging from 5V for dark blue to 20V for light blue with incrementing steps of 5V. While the red curves are drawn for V_{SD} ranging from -20V for dark red to -5V for light red with incrementing steps of 5V.

metals junctions [51].

Similarly, the graphene sheet resistivity is not quantitatively well defined. The values found in literature for CVD-graphene range from $\sim 30\Omega/\square$ to more than $\sim 2k\Omega/\square$ [40,49,52–54], with $\sim 30\Omega/\square$ being the intrinsic theoretical sheet resistivity [11,55].

The first set of measurements were performed on a set of OGT devices having 300nm of sacrificial layer of silicon dioxide. Many average beam resistances were measured on different devices and the values were observed to range between some tenths of kΩ to tenths of MΩ. This variability could be caused by many factors, for instance: broken graphene on the gold pads reducing the graphene-gold contact area, cleanliness of the graphene, ripples on the graphene,... An example of I-V curve and gate effect measurements are shown in **figure 5.1**. This first experiment was performed over an unusually wide V_{SD} range. In fact, the devices with low beam resistance broke down. A non linearity in the I-V curve and an asymmetry in the gate effect around zero are observed. The former may be caused by the graphene-metal contact resistance dependence on the applied voltage as suggested by the model developed in ref-

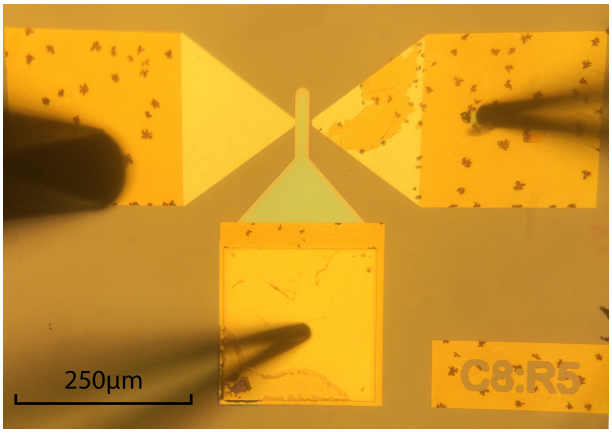

Figure 5.2 – Bolometer lying in the probe station after annealing. The gold on the source-drain pads was affected by the high temperature everywhere except for the regions where it is covered by graphene. It is now easy to notice that the contact resistance may be increased by the reduced graphene-gold contact surface on the right hand side gold pad.

erence [50]. While, the latter could be the consequence of graphene doping. A second asymmetry come to light looking at these figures, the curves for positive source-drain (bluish) voltages are not overlapping with those for negative voltages (reddish). Two possible origins of this effect are the necessity of applying all voltages for a certain time before measuring due to probable capacitive couplings and the heating of the device.

It is known that the contact resistance between a semiconductor and a metal can be improved by annealing. The same can be done for the graphene-metal interfaces and it can additionally reduce resist residues and dirt on graphene [30, 56, 57]. Hence, a group of devices were measured and later annealed at 400°C for 8 hours with a flow of H_2 (10 sccm) and Ar (100 sccm). The pressure in the furnace was 0.6 mbar. **Figure 5.2** shows the bolometer after annealing while probing. The gold on the source-drain pads was visibly affected in all regions where the graphene was not present. The explanation of this appearance change may lie in the gold diffusion into the silicon oxide.

Measurements of graphene beams before and after annealing are shown in **figure 5.3**. Many similar measurements were made on a number of bolometers and all showed a decrease in average beam resistance after annealing, which can be seen as an increased slope in the I-V curve. By "beam average resistance", it is here meant graphene beam plus graphene-gold contact resistances. As expected gate effects are mitigated by thicker layers of silicon dioxide. In fact,

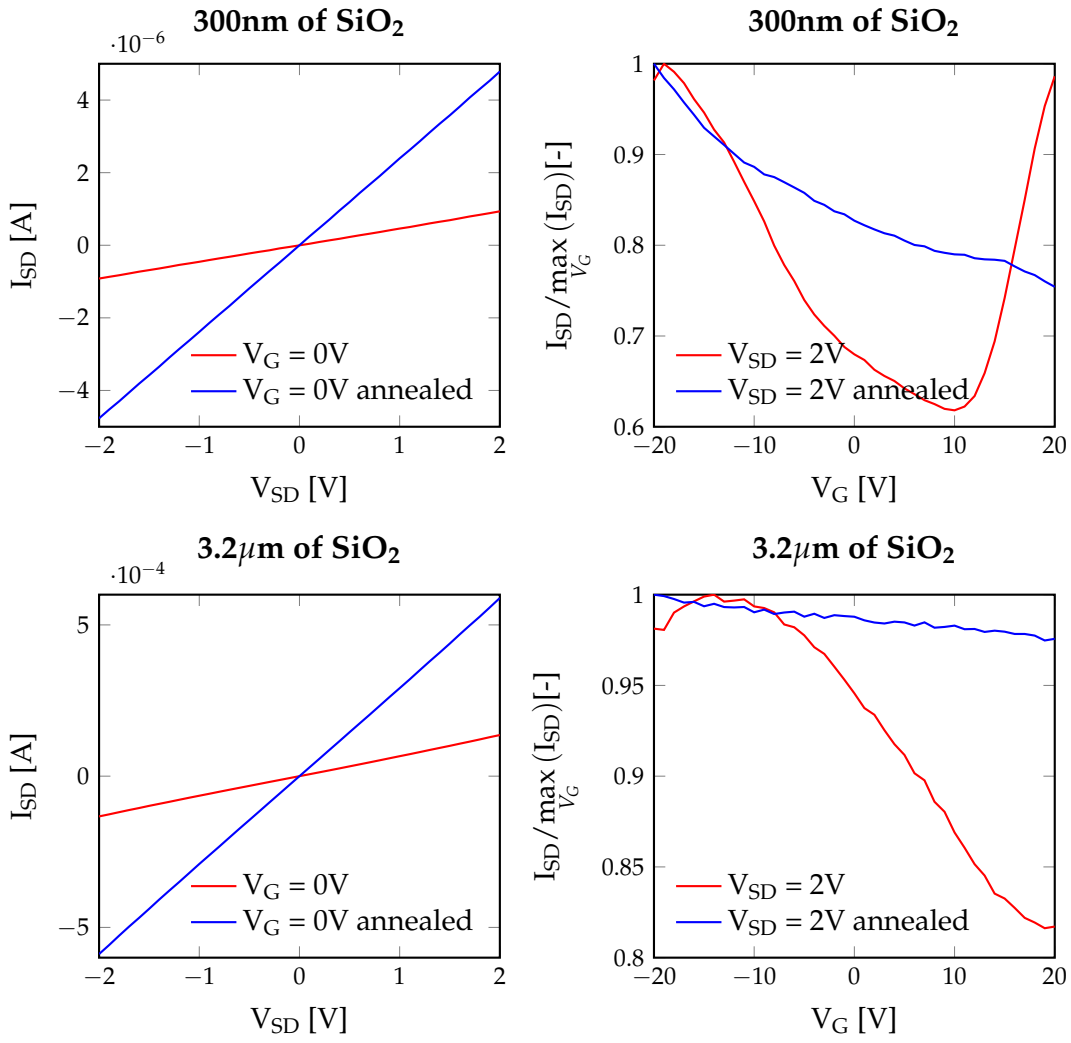

Figure 5.3 – Electrical response of a graphene beam before and after annealing. The plots on the top are made from measurements on the same bolometer with a 300nm silicon dioxide sacrificial layer, while the two at the bottom for a bolometer with a 3.2μm sacrificial layer. The graphs on the right hand side have been normalised in order to quantify the gate effects on the source-drain current. The maximal source-drain current (normalisation factor $\max_{V_G}(I_{SD})$) are the following, for 300nm of SiO_2 sacrificial layer: $1.4 \cdot 10^{-6}$A before annealing and $5.8 \cdot 10^{-6}$A after annealing, while for 3.2μm of SiO_2 sacrificial layer: $1.4 \cdot 10^{-4}$A before annealing and $5.9 \cdot 10^{-4}$A after annealing. The graphene beam details are: 20μm long and 10μm wide with metal-graphene contact surface of approximately $20 \cdot 10^3 \mu m^2$ per electrode for the panels on top, while 20μm long and 15μm wide with metal-graphene contact surface of approximately $25 \cdot 10^3 \mu m^2$ per electrode for those on bottom. The given contact surfaces do not take into account defects or missing portions of graphene.

before annealing, a $\sim$38% change in I_{SD} could be achieved by applying gate voltages in the range of $\pm$20V for 300nm of SiO_2, while only $\sim$18% for 3.2μm of SiO_2. The annealing process clearly affected the effects of the gate on the graphene beam as well. At this stage it is difficult to give an interpretation on this measurements and isolate the causes of these changes. Further studies and larger amount of data are needed. Additionally, it is probably worth waiting for the second fabrication run bolometers to be ready before further exploring the electrical properties and draw any conclusion.

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6 | Conclusion

The aim of this thesis was to provide a method to model, fabricate and characterise 2D material-based bolometers and justify their technological importance. To that end, a short review of the state of the art of bolometers was presented. Comparative advantages of bolometers employing 2D-materials as thermal sensors and IR absorbers were extrapolated from the mathematical expressions of bolometers figures of merit. A device design was then proposed and fabricated using graphene as particular choice of 2D-material. The fabrication was then optimised and a second fabrication run was performed. Finally, the gate effect and the I-V curve were measured on graphene beams lying on silicon dioxide.

The discovery of 2D-materials could boost bolometric devices to a paradigm shift. The developed mathematical model outline how the extraordinary tunable properties of 2D-materials can improve the state of the art. When suspended beams of 2D-materials are used as thermal sensor and IR absorber, three aspects can be improved. (i) Reduction of thermal losses to the surroundings, thermal flow to the anchors is the main heat loss in the beam and it is reduced by the nanometric thickness of the beam. (ii) Enhancement of the beam absorption, this is achieved by the exploitation of the gate effect and impedance matching. (iii) Reduction of the beam mass, reducing the heat capacity of the IR absorber causes an increase in bandwidth. An innovative read-out method that exploits variations in beam resonant frequency was also proposed. This method could increase the dynamic range of the bolometer thanks to the high flexibility of graphene. A classical resistive read-out is also possible with the same device.

Two fabrication run were performed to obtain 2D material-based bolometers structures using graphene. Graphene suspended beam structures were successfully fabricated at a low yield within the first run and a strong feedback on the fabrication processes was obtained. The origin of the main issues was the usage of wet etching for gold patterning and the low quality of sputtered silicon dioxide in argon atmosphere. These issues were successfully solved using

lift-off instead of wet etching and sputtering denser silicon dioxide thanks to a argon and oxygen atmosphere. The yield and quality of the second generation devices obtained with the second fabrication run were extensively superior compared to the previous ones. Graphene transfer and release was not tested on the second generation due to time constraints, but the smoothness of gold pads is promising for a better graphene transfer and release. The fabrication up to graphene transfer does not need further optimisation unless characterisation gives an opposite feedback. Improved methods to keep the graphene quality and cleanliness at high levels during the fabrication processes still need to be implemented. Transferring graphene after gold evaporation and graphene release using vapour HF were proven to be valid techniques.

Graphene beams lying on silicon dioxide were characterised through electrical measurements in a probe station. The beams were obtained with the first fabrication run and measured just before release. The I-V curve and gate effect were measured before and after annealing. Non-linearities were found in the I-V curve before annealing and the average beam resistance of different bolometers varied between tenths of kΩ to tenths of MΩ. Non-linearities could be the consequence of a non-ohmic contact resistance between gold and graphene as suggested in some models in literature. Annealing resulted in a consistent decrease in beam resistance reaching values down to the order of $\sim$10kΩ. Gate effect in the $\pm$20V range before annealing could infer variations in the source-drain current up to $\sim$38% for thinner layers of silicon dioxides. The gate effect was reduced after annealing. Some asymmetries and effects of annealing still need interpretation and more data is needed to draw conclusions. The effectiveness of the gate effect conceptually proves radiation absorption tunability in graphene via impedance matchng.

The promising results obtained during this thesis open many possible path for the future. One example could be the following. Graphene transfer, patterning and release need to be tested for the second generation of bolometers. An improvement of graphene beam quality and yield is expected. Characterisation of suspended graphene beams will then be possible, probably resulting in suggestions for design and fabrication optimisations. It will then be possible to use suspended sheets of graphene to prove bolometric measurements with resistive and resonant frequency read-out. The extent of tunability of absorption will then be tested. Finally, different 2D-materials will be tested to discover their capabilities in bolometric measurements and the validity of the fabrication process. Comparisons will be made through the presented figures of merit.

Appendices

A | Fabrication details

In this appendix are contained all details needed to reproduce the bolometers described in Section 4.1 and Section 4.2 at the CMi facility at EPFL.

The runsheet of the first fabrication run is presented in **table A.1**, while the second run can be found in **table A.2**. The procedure presented here reflects the original processes and not necessarily the best practices. For instance, in the first run, the first wet etching of chromium was done with the commercial ready-to-use CR7 $(NH_4)_2Ce(NO_3)$ + $HClO_4$ etchant (step 3.1B in **table A.1**), but as explained in Section 4.1.3, it would be better to use another etchant as it was done in step 9.1B in **table A.1**.

All the processes are assumed with an initial ∅100mm SSP test p-type (0.1-100Ωcm) wafer with 285 nm of wet thermal silicon dioxide (SiO_2) on both sides. Regarding the runsheet, the recipes and settings are only approximate and adapted for the very time when this thesis was written. Many tools undergo maintenance and the optimal parameters for a fixed substrate may change quite a lot in time. For this reason it is advised to anyone following this runsheet to:

- perform exposure tests on dummy wafers having the same substrates as the wafers to be processed. This should be done for all lithography steps. Both the Heidelberg MLA150 and VPG200 tool allow to expose matrices of a single design die with varying defoc values on one axis and varying intensities on the other. After developing a dummy wafer with such a matrix exposed, it should be fairly easy to determine the optimal parameters to be used. For the first fabrication run, exposure tests were done with the design shown in **figure 4.5**, while in the second run the design in **figure 4.17** was used. The optimal parameters can change from one week to another depending on maintenance schedules. For the single chips (fourth lithography) no exposure test was done. Different intensities and defoc were tested on different chips.

- ideally measure all etch rates on dummy wafers. This is the case specially for vapour HF, but also for wet etching. The etch rate could depend on

many factors (humidity in the cleanroom, quality of substrate, cleanliness of etchant,...) and therefore etching times can strongly vary from one day to another. The time listed in the table where usually counted as follows: start chronometer, dip wafers in solution and only when time is up, pull the wafer out and move them to the rinse bath. For vapour HF etching at the Idonus HF VPE-100, the following procedure was followed: place holder with wafer as lid, start chronometer, open chamber valve and pull rod to poor HF in chamber, when time is up pull rod to extract HF from chamber, wait 10s more, pull holder with wafer away, close chamber with lid and when no more HF is in the chamber, close chamber valve.

- check the deposition rate of sputtered silicon dioxide at the SPIDER600. The deposition rate provided by the CMi stuff are only indicative values and if a precise thickness is needed a deposition on a dummy wafer to determine the rate is mandatory. In the first fabrication run, the deposition rates provided by the CMi stuff were followed without verification. As a result, the thicknesses obtained were 300nm instead of 250nm and 3.2μm instead of 2.5μm. The user should keep in mind to take into account the rump up time when computing times. No dummy wafer tests are needed in the evaporator Alliance-Concept EVA 760, because it uses a feedback thickness measurement while evaporating.

- check that the recipe names have not changed.

Some metrological steps were added to the process flow as guideline, but the reader should take time to inspect the wafer or chip any time he thinks he could obtain useful information. It is best to examine the wafers before and after every step (and if possible take pictures of what you see). This extremely help ease troubleshooting when something goes wrong. It is additionally advised to place the flat side of the wafers in the same known position for every step and in every tool. It will then be easier to understand, for instance, the origin of non-uniformities on the wafers surfaces. In case the reader wants to use dry etching instead of wet etching, all oxygen plasma resist stripping should be done before wet stripping in order to soften the resist surface burnt by dry etching. Additionally, wafers spin rinses should be performed after descumimng, because contamination was sometimes observed after the Tepla GIGAbatch. All the optimisations described in Section 4.1.3 are not implemented in the runsheet of **table A.1** but only in the one of **table A.2**.

FIRST FABRICATION RUN

STEP	DESCRIPTION	TOOL	RECIPE, PARAMETERS AND NOTES
0.x	**Wafer preparation**		
0.1	Check SiO_2 thickness	Nanospec AFT-6100	Note: measure wet thermal silicon dioxide
1.x	**Metal evaporation**		
1.1	Cr/Au evaporation	Alliance-Concept EVA 760	Recipe: 250_Cr-Au_160-160. Parameters: 0.05kÅ of Cr and 0.25kÅ of Au. Note: Working distance 250mm
2.x	**Photolithography (1^{st})**		
2.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry.
2.2	Coating	ACS200	Recipe: 145_AZ9260_2um_HMDS. Preparation: Bake, HexaMethylDiSilazane (HMDS) and post bake. Edge Bead Removal (EBR) not needed. Note: resist type AZ92xx, thickness 2μm
2.3	Exposure	Heidelberg MLA150	Intensity: 175mJ/cm^2 and Defoc: 1
2.4	Develop	Rite Track 88	Recipe: AZ9269_2um. Procedure: develop and post bake. Note: run a dummy wafer before developing
2.5	Inspection	Optical microscope	-
2.6	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
3.x	**Wet Etching**		
3.xA	**Wet Etching of Au**		
3.1A	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Descum just before wet etching, because the oxygen plasma increase the hydrophilicity of the wafer
3.2A	Wet etching of Au	Arias Acid	Solution: commercial ready-to-use Kl(25g/l)+I_2(12g/l). Time: 1min10s
3.3A	Beaker rinse 1	Arias Acid	Time: 3min

3.4A	Beaker rinse 2	Arias Acid	Time: 3min
3.5A	Water gun	Arias Acid	Note: quick rinse of wafer out of holder
3.6A	Inspection	Optical microscope	-
3.xB	**Wet Etching of Cr**		
3.1B	Wet etching of Cr	Arias Acid	Solution: commercial ready-to-use CR7 $(NH_4)_2Ce(NO_3)$ + $HClO_4$. Time: 1min
3.2B	Beaker rinse 1	Arias Acid	Time: 3min
3.3B	Beaker rinse 2	Arias Acid	Time: 3min
3.4B	Water gun	Arias Acid	Note: quick rinse of wafer out of holder
3.5B	Inspection	Optical microscope	Note: important to verify that the are no more residues of Cr on the wafer. The resistance of the wafer could be probed as a further test
4.x	**RF Sputtering**		
4.1	Resist stripping	UFT resist	Note: follow the CMi procedure, heating at 70°C
4.2	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Cr is masked by Au
4.2	Inspection	Optical microscope	-
4.3	Metal thickness meas.	Bruker Dektak XT	Note: measure thickness on the square pads structures to prevent the bolometers from being damaged
4.4	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
4.5	SiO_2 sputtering	SPIDER600	Note: deposition of low quality SiO_2 (not the high quality SiO_2_F). Times: 40min40s for approx. 3.2μm and 4min17s for approx 300nm
4.6	Inspection	Optical microscope	-
4.7	SiO_2 thickness meas.	Nanospec AFT-6100	Note: sometimes it is advised to change the microscope magnification
5.x	**Photolithography (2^{nd})**		
5.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry

5.2	Coating	ACS200	Recipe: 145_AZ9260_2um_HMDS. Preparation: Bake, HMDS and post bake. EBR not needed. Note: resist type AZ92xx, thickness 2μm
5.3	Exposure	Heidelberg MLA150	Intensity: 165mJ/cm^2 and Defoc: 1. Alignment marks: (-35000,0) and (35000,0)
5.4	Develop	Rite Track 88	Recipe: AZ9269_2um. Procedure: develop and post bake. Note: run a dummy wafer before developing
5.5	Inspection	Optical microscope	-
5.6	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
6.x	**Wet Etching of SiO_2**		
6.1	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Descum just before wet etching, because the oxygen plasma increase the hydrophilicity of the wafer
6.2	Wet etching of SiO_2	Plade Oxide	Solution: BHF (7:1). Time: 45s for 300nm of SiO_2 and 3min35s for 3μm of SiO_2
6.3	Fast fill rinse	Plade Oxide	-
6.4	Tricke tank 2	Plade Oxide	-
6.5	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
6.6	Inspection	Optical microscope	-
6.7	Resist stripping	UFT resist	Note: follow the CMi procedure, heating at 70°C
6.8	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Cr is masked by Au
6.9	Inspection	Optical microscope	-
6.10	Oxide thickness meas.	Bruker Dektak XT	Note: measure thickness on the square pads structures to prevent the bolometers from being damaged
7.x	**Metal evaporation**		

7.0	Cr/Au evaporation	Alliance-Concept EVA 760	Recipe: 250_Cr-Au_160-160. Parameters: 0.1kÅ of Cr and 1kÅ of Au. Note: Working distance 250mm
8.x	**Photolithography (3rd)**		
8.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry.
8.2	Coating	ACS200	Recipe: 145_AZ9260_2um_HMDS. Preparation: Bake, HMDS and post bake. EBR not needed. Note: resist type AZ92xx, thickness 2μm
8.3	Exposure	Heidelberg MLA150	Intensity: 160mJ/cm^2 and Defoc: 1. Alignment marks: (-35000,0) and (35000,0)
8.4	Develop	Rite Track 88	Recipe: AZ9269_2um. Procedure: develop and post bake. Note: run a dummy wafer before developing
8.5	Inspection	Optical microscope	-
8.6	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
9.x	**Wet Etching**		
9.xA	**Wet Etching of Au**		
9.1A	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Descum just before wet etching, because the oxygen plasma increase the hydrophilicity of the wafer
9.2A	Wet etching of Au	Arias Acid	Solution: commercial ready-to-use Kl(25g/l)+I_2(12g/l). Time: 2min30s
9.3A	Beaker rinse 1	Arias Acid	Stir few seconds to quickly stop the etching
9.4A	Beaker rinse 2	Arias Acid	Time: 3min
9.5A	Beaker rinse 3	Arias Acid	Time: 3min
9.6A	Water gun	Arias Acid	Note: quick rinse of wafer out of holder
9.7A	Inspection	Optical microscope	-
9.xB	**Wet Etching of Cr**		

9.1B	Wet etching of Cr	Arias Acid	Solution: commercial ready-to-use Cr selective over Cu $KMnO_4$+Na_3PO_4. Time: 40s
9.2B	Beaker rinse 1	Arias Acid	Stir few seconds to quickly stop the etching
9.3B	Beaker rinse 1	Arias Acid	Time: 3min
9.4B	Beaker rinse 2	Arias Acid	Time: 3min
9.5B	Water gun	Arias Acid	Note: quick rinse of wafer out of holder
9.6B	Inspection	Optical microscope	Note: important to verify that the are no more residues of Cr on the wafer. The resistance of the wafer could be probed as a further test.
9.8B	Resist stripping	UFT resist	Note: follow the CMi procedure, heating at 70°C
9.9B	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Cr is masked by Au
9.10B	Inspection	Optical microscope	-
9.11B	Metal thickness meas.	Bruker Dektak XT	Note: measure thickness on the square pads structures to prevent the bolometers from being damaged
10.x	**Dicing**		
10.1	Coating	Rite Track	Recipe C_AZ92xx_4um. Note: spincoat 4μm of resist type AZ92xx
10.2	Dicing	Disco DAD321	The CMi staff performs the dicing procedure
11.x	**Graphene tranfer**		
11.1	2D material tranfer	Not in cleanroom	-
12.x	**Photolithography (4^{th})**		
12.1	Manual coating	SSE SB20	Recipe: STD_2000rpm. Note: poor a uniform layer of resist (ECI3007) across the chip
12.2	Bake	SSE SB20	Parameters: bake 1min at 90°. Note: measure the temperature with an external thermometer since the tool measurement is normally lower than the actual value. Clean back side of chips with acetone at the end

12.3	Exposure	Heidelberg MLA150	Intensity: 100mJ/cm^2 and Defoc: -8. Alignment marks: (-4200,3000), (4200,3000), (-4200,-3000) and (-4200,-3000)
12.4	Manual development	Wet bench	Parameters: 1min in AZ 726 MIF solution and then rinse 1min in a beaker with deionised water.
12.5	Inspection	Optical microscope	-
13.x	**Oxygen plasma etching**		
13.1	O_2 athmosphere etch	Tepla GIGAbatch	Recipe: Strip_Low_30s
13.2	Resist stripping	UTF resist	Note: follow the CMi procedure, heating at 70°C. It is advised to use an holder in which the surface with graphene of the chips do not risk to stick onto it due to the liquid surface tension. This could damage the graphene
13.3	Inspection	Optical microscope	-
13.4	Inspection	Zeiss LEO 1550	-
14.x	**Vapor HF etching**		
14.1	Vapour HF etch of SiO_2	Idonus HF VPE-100	Parameters: 7min for 300nm and 32min for 3.2μm
14.2	Inspection	Optical microscope	-
14.3	SiO_2 thickness meas.	Nanospec AFT-6100	Note: sometimes it is advised to change the microscope magnification
14.4	Inspection	Zeiss LEO 1550	Note: use low EHT voltage (1keV-3keV), high voltages could damage the structures

Table A.1 – Detailed runsheet for the first fabrication run at the CMi facility.

SECOND FABRICATION RUN

STEP	DESCRIPTION	TOOL	RECIPE, PARAMETERS AND NOTES
0.x	**Wafer preparation**		
0.1	Check SiO_2 thickness	Nanospec AFT-6100	Note: easure wet thermal silicon dioxide
0.2	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
1.x	**Photolithography (1st)**		
1.1	Coating	ACS200	Recipe: 171_CMi.AZ1512onLOE.0um48. Preparation: Bake, HMDS, post bake and EBR. EBR is not necessary. Note: resist type AZ1512, thickness 1.1μm on LOR thickness 0.48μm
1.2	Exposure	Heidelberg VPG200	Intensity: 5.2%, Defoc: -35%, zx: -110 and zy: -30
1.3	Develop	ACS200	Recipe: 171_CMi.AZ1512onLOE.0um48_2um
1.4	Develop	ACS200	Recipe: 171_CMi.AZ1512onLOE.0um48_2um. Note: this is not a typo, it has to be done twice
1.5	Inspection	Optical microscope	-
1.6	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
1.7	Descum	Tepla GIGAbatch	Recipe: Strip_Low_30s
1.8	Inspection	Optical microscope	-
2.x	**Metal Evaporation**		
2.1	Cr/Au evaporation	Alliance-Concept EVA 760	Recipe: 450_Cr-Au_50-50. Parameters: 0.05kÅ of Cr and 0.25kÅ of Au. Note: Working distance 450mm
2.2	Inspection	Optical microscope	-
3.x	**Lift-off**		
3.1	Dissolve resist	Plade Solvent	Time: 2h30min in static 1165 remover bath

3.2	Dissolve resist	Plade Solvent	Time: 10min in ultrasound 1165 remover bath
3.3	Dissolve resist	Plade Solvent	Time: 10min in static 1165 remover bath
3.4	VPA rinse	Plade Solvent	Time: 1 timer
3.5	First rinse bath	Plade Solvent	Time: 1 timer
3.6	First rinse bath	Plade Solvent	Time: 1 timer
3.7	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
3.8	Inspection	Optical microscope	-
3.9	Descum	Tepla GIGAbatch	Recipe: Strip_High_2min
3.10	Metal thickness meas.	Bruker Dektak XT	Note: measure thickness on metal squares
3.11	Inspection	Zeiss LEO 1550	Gold profile inspection
4.x	**RF Sputtering**		
4.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
4.2	SiO_2 sputtering	SPIDER600	Note: deposition of high quality SiO_2 (recipe: SiO_2_F). Time: 15min30s approx 250nm. Etch rate: 16.4nm/min
4.3	Inspection	Optical microscope	-
4.4	SiO_2 thickness meas.	Nanospec AFT-6100	Note: sometimes it is advised to change the microscope magnification
5.x	**Photolithography (2^{nd})**		
5.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
5.2	Coating	ACS200	Recipe: 145_AZ9260_2um_HMDS. Preparation: Bake, HMDS and post bake. EBR not needed. Note: resist type AZ92xx, thickness 2μm
5.3	Exposure	Heidelberg VPG200	Intensity: 55%, Defoc: -35%, zx: -110 and zy: -30
8.4	Develop	Rite Track 88	Recipe: AZ9269_2um. Procedure: develop and post bake. Note: run a dummy wafer before developing
5.5	Inspection	Optical microscope	-

5.6	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
6.x	**Wet Etching of SiO_2**		
6.1	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Descum just before wet etching, because the oxygen plasma increase the hydrophilicity of the wafer
6.2	Wet etching of SiO_2	Plade Oxide	Solution: BHF (7:1). Time: 2min40s for 250nm of SiO_2
6.3	Fast fill rinse	Plade Oxide	-
6.4	Tricke tank 2	Plade Oxide	-
6.5	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
6.6	Inspection	Optical microscope	-
6.7	Probe	Multimeter	Probe gold lines to check electrical conduction
6.8	Oxide thickness meas.	Bruker Dektak XT	Note: measure thickness on the square pads structures to prevent the bolometers from being damaged
6.9	Resist stripping	UFT resist	Note: follow the CMi procedure, heating at 70°C
6.10	Descum	Tepla GIGAbatch	Recipe: Strip_High_30s. Note: Cr is masked by Au
6.11	Inspection	Optical microscope	-
7.x	**Photolithography (3^{rd})**		
7.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
7.2	Coating	ACS200	Recipe: 171_CMi.AZ1512onLOE.0um48. Preparation: Bake, HMDS, post bake and EBR. EBR is not necessary. Note: resist type AZ1512, thickness 1.1μm on LOR thickness 0.48μm
7.3	Exposure	Heidelberg VPG200	Intensity: 6%, Defoc: -35%, zx: -110 and zy: -30
7.4	Develop	ACS200	Recipe: 171_CMi.AZ1512onLOE.0um48_2um
7.5	Develop	ACS200	Recipe: 171_CMi.AZ1512onLOE.0um48_2um. Note: this is not a typo, it has to be done twice

7.6	Inspection	Optical microscope	-
7.7	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
7.8	Descum	Tepla GIGAbatch	Recipe: Strip_Low_30s
7.9	Inspection	Optical microscope	-
8.x	**Metal Evaporation**		
8.1	Cr/Au evaporation	Alliance-Concept EVA 760	Recipe: 450_Cr-Au_50-50. Parameters: 0.10kÅ of Cr and 1kÅ of Au. Note: Working distance 450mm
8.2	Inspection	Optical microscope	-
9.x	**Lift-off**		
9.1	Dissolve resist	Plade Solvent	Time: 2h30min in static 1165 remover bath
9.2	Dissolve resist	Plade Solvent	Time: 10min in ultrasound 1165 remover bath
9.3	Dissolve resist	Plade Solvent	Time: 10min in static 1165 remover bath
9.4	VPA rinse	Plade Solvent	Time: 1 timer
9.5	First rinse bath	Plade Solvent	Time: 1 timer
9.6	First rinse bath	Plade Solvent	Time: 1 timer
9.7	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry
9.8	Inspection	Optical microscope	-
9.9	Descum	Tepla GIGAbatch	Recipe: Strip_High_2min
9.10	Metal thickness meas.	Bruker Dektak XT	Note: measure thickness on metal squares
9.11	Inspection	Zeiss LEO 1550	Gold profile inspection

Table A.2 – Detailed runsheet for the second fabrication run at the CMi facility. The dicing, graphene transfer, patterning and release will be pursued after handing in this thesis.

B | Devices distribution on chips and wafers

In this chapter the type of bolometers designed and their distribution on chips and wafers are presented with a higher level of detail.

First fabrication run devices distribution

At the moment of writing this thesis, the maximal dimensions of suspended graphene beams that could be achieved with the fabrication technique employed in this project were unknown and therefore all possible dimensions needed to be explored. Consequently, different bolometer design were created in order to accomodate a wide range of graphene beams dimensions. As can be easily deduced from **figure 4.3**, only the drain and source pads of the OGT design set a constraint on the graphene beam length. In principle, the width of graphene beams could always be changed, within sensible values, at the moment of designing the graphene mask. The mask design of OGT chips was conceived to already include the graphene layer and therefore the mask of these chips has fixed graphene beams dimensions (length and width) for all bolometers. On the contrary, the NGT and EGT can accomodate both many length and many width and therefore the graphene mask for these chips is designed just before exposure depending on the desired beams dimensions. The types of devices are listed in **table B.1**.

The graphene transfer quality is not uniform across the substrate and in general, it is more effective in the centre of the chip. Hence, if a statistic is needed to determine what graphene beam sizes are the most likely to survive, it is necessary to have the same amount of graphene beams types for each fixed distance from the chip centre. This is achieved by adopting a spiral repetitive distribution as shown in **figure B.1**. It should be reminded at this point, that each chip contains only one of the three class of bolometer design (OGT, NGT and EGT).

Design type	Graphene beam sizes length×width [μm^2] / Structure type
OGT	2x1, 2x2, 5x1, 5x2, 5x5, 10x1, 10x2, 10x5, 10x10, 20x1, 20x2, 20x5, 20x10, 20x10
NGT	Zig-zag structure can accommodate many beams dimensions
EGT	Zig-zag structure can accommodate many beams dimensions
Test structures	16 different types (names not explicitly written here)

Table B.1 – Types of bolometers with relative beam dimension. The test structures are not further discussed in this appendix, but the mask contains 16 different design types. The pad design of the OGT bolometer is the only one setting some constraints on the graphene beam sizes and therefore a different design for each beam length is needed.

10x5	10x10	20x1	20x2	20x5	20x10	2x1	10x2
10x10	20x1	20x2	20x5	20x10	2x1	2x2	5x1
5x2	5x5	10x1	10x2	10x5	10x10	20x1	20x2
5x1	10x5	10x10	20x1	20x2	20x5	20x10	20x5
2x2	10x2	10x2	10x5	10x10	20x1	2x1	20x10
2x1	10x1	10x1	2x1	2x2	20x2	2x2	2x1
20x10	5x5	5x5	5x2	5x1	20x5	5x1	2x2
20x5	5x2	5x1	2x2	2x1	20x10	5x2	5x1
20x2	20x1	10x10	10x5	10x2	10x1	5x5	5x2
20x5	20x2	20x1	10x10	10x5	10x2	10x1	5x5
2x2	5x1	5x2	5x5	10x1	10x2	10x5	10x10
20x10	20x10	2x1	2x2	5x1	5x2	5x5	10x1

Contact_R_Test_delta	Contact_R_Test_one	TLM	Bolo_Half_zigzag	Pauw30closed	Contact_R_Gold	Pauw30medium	Pauw30small
Contact_R_Test	Cross10x5	Cross15x7	Cross30x10	Cross50x10	Cross50x10_S	Cross50x10_S2	Cross10x5
Cross50x10_S2	Pauw30small	Cross15x7	Cross30x10	Cross50x10	Cross50x10_S	Contact_R_Test	Cross15x7
Cross50x10_S	Pauw30medium	Cross10x5	Bolo_Half_zigzag	Pauw30closed	Cross50x10_S2	Contact_R_Test_delta	Cross30x10
Cross50x10	Pauw30large	Pauw30small	Pauw30medium	Pauw30large	Contact_R_Test	Contact_R_Test_one	Cross50x10
Cross30x10	Pauw30closed	Bolo_Half_zigzag	TLM	Contact_R_Test_one	Contact_R_Test_delta	TLM	Cross50x10_S
Cross15x7	Cross10x5	Pauw30small	Pauw30medium	Pauw30large	Pauw30closed	Bolo_Half_zigzag	Cross50x10_S2
Contact_R_Gold	Pauw30large	Pauw30closed	Bolo_Half_zigzag	TLM	Contact_R_Test_one	Contact_R_Test_delta	Contact_R_Test

Figure B.1 – On the left hand side the distribution of OGT bolometers on chips, while on the right hand side the one of test structures. A spiral repetitive distribution was chosen to approximately have the same number of bolometers/test structures types for each fixed distance from the chip centre. In the grey bands the distribution is linear. In red the repetitive pattern.

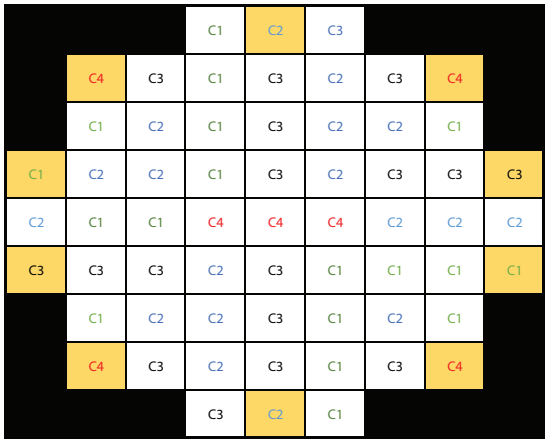

Figure B.2 – Distribution of chip types on wafers. C1: EGT chip , C2: EGT chip, C3: NGT chip and C4: test structures chip. Some of the chips are marked in yellow because are on the wafer edge and therefore some elements in the chips could be affected negatively.

Following the same reasoning, it is desired to have the chips equally distributed on the wafers as well. In fact, some of the fabrication processes are not uniform across the wafer. A clear example is the sputtering of silicon dioxide discussed in Section 4.1.3. Thus, the distribution shown in **figure B.2** was chosen. The wafers contains eighteen chips of each bolometer class (OGT, NGT and EGT) and seven test structures chips.

Second fabrication run devices distribution

The logic behind the process of gathering all bolometer designs into chips is the same as discussed in the previous section. Using a spiral distribution would be too time consuming for chips that can accomodate this many devices and therefore another distribution was chosen as shown in **figures B.3, B.4** and **B.5**. These figures show the parameters chosen to generate the designs from the T-Cells.

The chips distribution on wafers is still the one shown in **figure B.2**.

OGT chip, type =1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
1	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3
2	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7
3	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1
4	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3
5	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7
6	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15
7	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20
8	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3
9	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7
10	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1
11	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3
12	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7
13	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15
14	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20
15	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3
16	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7
17	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1
18	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3
19	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7
20	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15
21	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20
22	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3	10x2	10x3	2x1	2x2	2x1	2x2	10x2	10x3
23	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7	10x5	10x7	3x1	3x2	3x1	3x2	10x5	10x7
24	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1	10x10	20x1	3x3	4x1	3x3	4x1	10x10	20x1
25	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3	20x2	20x3	4x2	4x3	4x2	4x3	20x2	20x3
26	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7	20x5	20x7	4x4	5x1	4x4	5x1	20x5	20x7
27	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15	20x10	20x15	5x2	5x3	5x2	5x3	20x10	20x15
28	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20	20x17	20x20	5x5	10x1	5x5	10x1	20x17	20x20

o = 2.5

	w x h			w x h	
	1	2		1	2
1	2x1	2x2	1	10x2	10x3
2	3x1	3x2	2	10x5	10x7
3	3x3	4x1	3	10x10	20x1
4	4x2	4x3	4	20x2	20x3
5	4x4	5x1	5	20x5	20x7
6	5x2	5x3	6	20x10	20x15
7	5x5	10x1	7	20x17	20x20

o = 2.5

	w x h			w x h	
	1	2		1	2
1	2x1	2x2	1	10x2	10x3
2	3x1	3x2	2	10x5	10x7
3	3x3	4x1	3	10x10	20x1
4	4x2	4x3	4	20x2	20x3
5	4x4	5x1	5	20x5	20x7
6	5x2	5x3	6	20x10	20x15
7	5x5	10x1	7	20x17	20x20

Figure B.3 – Distribution of bolometers types on chips. This chip contains OGT bolometers only (T-Cell parameter *type* = 1). Various values of overlapping region ($o_{\text{T-c}}$) and graphene beam width and length ($h_{\text{T-c}}$ and $w_{\text{T-c}}$) were chosen and uniformly distributed.

NGT chip, type = 2

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
1	4x2	4x3	5x1	5x1	10x2	10x3	10x2	10x3	4x2	4x3	5x1	5x1	10x2	10x3	10x2	10x3	4x2	4x3	5x1	5x1	10x2	10x3
2	3x1	3x2	5x2	5x2	10x5	10x7	10x5	10x7	3x1	3x2	5x2	5x2	10x5	10x7	10x5	10x7	3x1	3x2	5x2	5x2	10x5	10x7
3	3x3	4x1	5x3	5x3	10x10	20x1	10x10	20x1	3x3	4x1	5x3	5x3	10x10	20x1	10x10	20x1	3x3	4x1	5x3	5x3	10x10	20x1
4	4x2	4x3	5x5	5x5	20x2	20x3	20x2	20x3	4x2	4x3	5x5	5x5	20x2	20x3	20x2	20x3	4x2	4x3	5x5	5x5	20x2	20x3
5	4x4	5x1	10x1	10x1	20x5	20x7	20x5	20x7	4x4	5x1	10x1	10x1	20x5	20x7	20x5	20x7	4x4	5x1	10x1	10x1	20x5	20x7
6	5x2	5x3	10x2	10x3	20x10	20x15	20x10	20x15	5x2	5x3	10x2	10x3	20x10	20x15	20x10	20x15	5x2	5x3	10x2	10x3	20x10	20x15
7	5x5	10x1	10x5	10x7	20x17	20x20	20x17	20x20	5x5	10x1	10x5	10x7	20x17	20x20	20x17	20x20	5x5	10x1	10x5	10x7	20x17	20x20
8	4x2	4x3	5x1	5x1	10x2	10x3	10x2	10x3	4x2	4x3	5x1	5x1	10x2	10x3	10x2	10x3	4x2	4x3	5x1	5x1	10x2	10x3
9	3x1	3x2	5x2	5x2	10x5	10x7	10x5	10x7	3x1	3x2	5x2	5x2	10x5	10x7	10x5	10x7	3x1	3x2	5x2	5x2	10x5	10x7
10	3x3	4x1	5x3	5x3	10x10	20x1	10x10	20x1	3x3	4x1	5x3	5x3	10x10	20x1	10x10	20x1	3x3	4x1	5x3	5x3	10x10	20x1
11	4x2	4x3	5x5	5x5	20x2	20x3	20x2	20x3	4x2	4x3	5x5	5x5	20x2	20x3	20x2	20x3	4x2	4x3	5x5	5x5	20x2	20x3
12	4x4	5x1	10x1	10x1	20x5	20x7	20x5	20x7	4x4	5x1	10x1	10x1	20x5	20x7	20x5	20x7	4x4	5x1	10x1	10x1	20x5	20x7
13	5x2	5x3	10x2	10x3	20x10	20x15	20x10	20x15	5x2	5x3	10x2	10x3	20x10	20x15	20x10	20x15	5x2	5x3	10x2	10x3	20x10	20x15
14	5x5	10x1	10x5	10x7	20x17	20x20	20x17	20x20	5x5	10x1	10x5	10x7	20x17	20x20	20x17	20x20	5x5	10x1	10x5	10x7	20x17	20x20
15	4x2	4x3	5x1	5x1	10x2	10x3	10x2	10x3	4x2	4x3	5x1	5x1	4x2	4x3	10x2	10x3	4x2	4x3	5x1	5x1	10x2	10x3
16	3x1	3x2	5x2	5x2	10x5	10x7	10x5	10x7	3x1	3x2	5x2	5x2	3x1	3x2	10x5	10x7	3x1	3x2	5x2	5x2	10x5	10x7
17	3x3	4x1	5x3	5x3	10x10	20x1	10x10	20x1	3x3	4x1	5x3	5x3	3x3	4x1	10x10	20x1	3x3	4x1	5x3	5x3	10x10	20x1
18	4x2	4x3	5x5	5x5	20x2	20x3	20x2	20x3	4x2	4x3	5x5	5x5	4x2	4x3	20x2	20x3	4x2	4x3	5x5	5x5	20x2	20x3
19	4x4	5x1	10x1	10x1	20x5	20x7	20x5	20x7	4x4	5x1	10x1	10x1	4x4	5x1	20x5	20x7	4x4	5x1	10x1	10x1	20x5	20x7
20	5x2	5x3	10x2	10x3	20x10	20x15	20x10	20x15	5x2	5x3	10x2	10x3	5x2	5x3	20x10	20x15	5x2	5x3	10x2	10x3	20x10	20x15
21	5x5	10x1	10x5	10x7	20x17	20x20	20x17	20x20	5x5	10x1	10x5	10x7	5x5	10x1	20x17	20x20	5x5	10x1	10x5	10x7	20x17	20x20
22	4x2	4x3	5x1	5x1	10x2	10x3	10x2	10x3	4x2	4x3	5x1	5x1	10x2	10x3	10x2	10x3	4x2	4x3	5x1	5x1	10x2	10x3
23	3x1	3x2	5x2	5x2	10x5	10x7	10x5	10x7	3x1	3x2	5x2	5x2	10x5	10x7	10x5	10x7	3x1	3x2	5x2	5x2	10x5	10x7
24	3x3	4x1	5x3	5x3	10x10	20x1	10x10	20x1	3x3	4x1	5x3	5x3	10x10	20x1	10x10	20x1	3x3	4x1	5x3	5x3	10x10	20x1
25	4x2	4x3	5x5	5x5	20x2	20x3	20x2	20x3	4x2	4x3	5x5	5x5	20x2	20x3	20x2	20x3	4x2	4x3	5x5	5x5	20x2	20x3
26	4x4	5x1	10x1	10x1	20x5	20x7	20x5	20x7	4x4	5x1	10x1	10x1	20x5	20x7	20x5	20x7	4x4	5x1	10x1	10x1	20x5	20x7
27	5x2	5x3	10x2	10x3	20x10	20x15	20x10	20x15	5x2	5x3	10x2	10x3	20x10	20x15	20x10	20x15	5x2	5x3	10x2	10x3	20x10	20x15
28	5x5	10x1	10x5	10x7	20x17	20x20	20x17	20x20	5x5	10x1	10x5	10x7	20x17	20x20	20x17	20x20	5x5	10x1	10x5	10x7	20x17	20x20

o = 1

	w x h			w x h	
	1	2		1	2
1	4x2	4x3	1	10x2	10x3
2	3x1	3x2	2	10x5	10x7
3	3x3	4x1	3	10x10	20x1
4	4x2	4x3	4	20x2	20x3
5	4x4	5x1	5	20x5	20x7
6	5x2	5x3	6	20x10	20x15
7	5x5	10x1	7	20x17	20x20

o = 2

	w x h			w x h	
	1	2		1	2
1	5x1	5x1	1	10x2	10x3
2	5x2	5x2	2	10x5	10x7
3	5x3	5x3	3	10x10	20x1
4	5x5	5x5	4	20x2	20x3
5	10x1	10x1	5	20x5	20x7
6	10x2	10x3	6	20x10	20x15
7	10x5	10x7	7	20x17	20x20

Figure B.4 – Distribution of bolometers types on chips. This chip contains NGT bolometers only (T-Cell parameter *type* = 2). Various values of overlapping region ($o_{\text{T-c}}$) and graphene beam width and length ($h_{\text{T-c}}$ and $w_{\text{T-c}}$) were chosen and uniformly distributed.

EGT chip, type = 3

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
1	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2
2	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2
3	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1
4	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3
5	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1
6	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3
7	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1
8	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2
9	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2
10	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1
11	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3
12	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1
13	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3
14	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1
15	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	10x2	10x3
16	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	10x5	10x7
17	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	10x10	20x1
18	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	20x2	20x3
19	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	20x5	20x7
20	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	20x10	20x15
21	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	20x17	20x20
22	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2	10x2	10x3	2x1	2x2
23	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2	10x5	10x7	3x1	3x2
24	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1	10x10	20x1	3x3	4x1
25	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3	20x2	20x3	4x2	4x3
26	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1	20x5	20x7	4x4	5x1
27	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3	20x10	20x15	5x2	5x3
28	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1	20x17	20x20	5x5	10x1

o = irrelevant

	w x h			w x h	
	1	2		1	2
1	2x1	2x2	1	10x2	10x3
2	3x1	3x2	2	10x5	10x7
3	3x3	4x1	3	10x10	20x1
4	4x2	4x3	4	20x2	20x3
5	4x4	5x1	5	20x5	20x7
6	5x2	5x3	6	20x10	20x15
7	5x5	10x1	7	20x17	20x20

Figure B.5 – Distribution of bolometers types on chips. This chip contains EGT bolometers only (T-Cell parameter $type = 3$). Various values graphene beam width and length ($h_{\text{T-c}}$ and $w_{\text{T-c}}$) were chosen and uniformly distributed.

C | T-Cell code

In this appendix a copy of the code used to draw the bolometers on the second fabrication run mask is presented. This code has not yet been optimised.

```
1
2  /*****************************************************************************
3   * Cell Name: Master_BoloDevice
4   * Creator  : Marco Di Gisi
5   *
6   * Revision History:
7   * 14 Apr 2016  Generated by L-Edit
8   *****************************************************************************/
9  #include <cstdlib>
10 #include <cmath>
11 #include <cstring>
12 #include <cstdio>
13 #include <string>
14 #include <time.h>
15
16 #define EXCLUDE_LEDIT_LEGACY_UPI
17 #include <ldata.h>
18
19
20 /* Begin --- Uncomment this block if you are using L-Comp. */
21 //#include <lcomp.h>
22 /* End */
23
24 /* TODO: Put local functions here. */
25 void Master_BoloDevice_main(void)
26 {
27   int iTmpUpiReturnCode = LUpi_GetReturnCode();
28   /* Begin DO NOT EDIT SECTION generated by L-Edit */
29   LCell        cellCurrent     = (LCell)LMacro_GetNewTCell();
30   int           type           = LCell_GetParameterAsInt(cellCurrent, "type");
31   double        h              = LCell_GetParameterAsDouble(cellCurrent, "h");
32   double        w              = LCell_GetParameterAsDouble(cellCurrent, "w");
33   double        o              = LCell_GetParameterAsDouble(cellCurrent, "o");
34   /* End DO NOT EDIT SECTION generated by L-Edit */
35
36   if(LUpi_GetReturnCode())
37   {
38     LDialog_MsgBox("Error: Tcell failed to read parameters.");
39     return;
40   }
41   LUpi_SetReturnCode(iTmpUpiReturnCode);
42
43
44   /*CODE WRITTEN BY MARCO DI GISI*/
45
46       //LOAD CELLS AND LAYERS
47
48         LFile pFile = LCell_GetFile(cellCurrent);
49         LLayer SourceDrain = LLayer_Find(pFile, "SourceDrain");
50         LLayer Gate = LLayer_Find(pFile, "Gate");
51         LLayer FreeGate = LLayer_Find(pFile, "FreeGate");
52         LLayer Graphene = LLayer_Find(pFile, "Graphene");
53         LLayer Outline = LLayer_Find(pFile, "Outline");
54
55       //CONVERSION IN um
56
57         LCoord H = h*1000;
58         LCoord W = w*1000;
59         LCoord O = o*1000;
60
61       //FIXED STRUCTURES
62
63         //Size of device
64         LObject OSize = LBox_New(cellCurrent, Outline, -175000, -205000, 175000, 75000);
```

```
65
66          //Pads design
67          LObject OLeftPad = LBox_New(cellCurrent, SourceDrain, -150000, -50000, -50000, 50000);
68          LObject ORightPad = LBox_New(cellCurrent, SourceDrain, 50000, -50000, 150000, 50000);
69          LObject OCentralPad = LBox_New(cellCurrent, SourceDrain, -50000, -180000, 50000, -80000);
70          LObject OGate = LBox_New(cellCurrent, Gate, -40000, -170000, 40000, -90000);
71          LObject OFreeGate = LBox_New(cellCurrent, FreeGate, -45000, -175000, 45000, -85000);
72
73          //Create arrays for polygon on the left
74          LPoint Lpt1 = LPoint_Set(-50000, 50000);
75          LPoint Lpt2 = LPoint_Set(-W/2, 10000);
76          LPoint Lpt3 = LPoint_Set(-W/2, -10000);
77          LPoint Lpt4 = LPoint_Set(-50000, -50000);
78          LPoint Larray [4] = {Lpt1, Lpt2, Lpt3, Lpt4};
79          //Draw polygon on the left
80          LObject OLeftPadPoly = LPolygon_New( cellCurrent, SourceDrain , Larray , 4);
81
82
83          //Create arrays for polygon on the right
84          LPoint Rpt1 = LPoint_Set(50000, 50000);
85          LPoint Rpt2 = LPoint_Set(W/2, 10000);
86          LPoint Rpt3 = LPoint_Set(W/2, -10000);
87          LPoint Rpt4 = LPoint_Set(50000, -50000);
88          LPoint Rarray [4] = {Rpt1, Rpt2, Rpt3, Rpt4};
89          //Draw polygon on the left
90          LObject OReftPadPoly = LPolygon_New( cellCurrent, SourceDrain , Rarray , 4);
91
92        //GRAPHENE STRUCTURE
93
94          //Strip
95          LObject OGrapheneStrip = LBox_New(cellCurrent, Graphene, -W/2-5000, -H/2, W/2+5000, H/2);
96
97          //Squares
98          LObject Sq1 = LBox_New(cellCurrent, Gate, -W/2-5000, -H/2, -W/2, -H/2-5000);
99          LObject Sq2 = LBox_New(cellCurrent, Gate, -W/2-5000, H/2, -W/2, H/2+5000);
100         LObject Sq3 = LBox_New(cellCurrent, Gate, W/2, -H/2, W/2+5000, -H/2-5000);
101         LObject Sq4 = LBox_New(cellCurrent, Gate, W/2, H/2, W/2+5000, H/2+5000);
102         //Cercles
103         LPoint C1 = LPoint_Set(-W/2, H/2+5000);
104         LPoint C2 = LPoint_Set(-W/2, -H/2-5000);
105         LPoint C3 = LPoint_Set(W/2, H/2+5000);
106         LPoint C4 = LPoint_Set(W/2, -H/2-5000);
107         LObject Circle1 = LCircle_New(cellCurrent, SourceDrain,C1, 5000);
108         LObject Circle2 = LCircle_New(cellCurrent, SourceDrain,C2, 5000);
109         LObject Circle3 = LCircle_New(cellCurrent, SourceDrain,C3, 5000);
110         LObject Circle4 = LCircle_New(cellCurrent, SourceDrain,C4, 5000);
111         //Boolean operation
112         LObject A[4] = {Sq1, Sq2, Sq3, Sq4};
113         LObject B[4] = {Circle1, Circle2, Circle3, Circle4};
114         LCoord resize = 1;
115         LCell_BooleanOperation( cellCurrent, LBoolOp_SUBTRACT,resize, A, 4, B, 4, Graphene, LTRUE );
116
117         //Create squares
118         LObject Sq5 = LBox_New(cellCurrent, Gate, -50000, -50000, -W/2-5000, 50000);
119         LObject Sq6 = LBox_New(cellCurrent, Gate, 50000, -50000, W/2+5000, 50000);
120         //Boolean operation
121         LObject C[2] = {OLeftPadPoly, OReftPadPoly};
122         LObject D[2] = {Sq5, Sq6};
123         LCell_BooleanOperation( cellCurrent, LBoolOp_AND,resize, C, 2,  D, 2, Graphene, LTRUE );
124         //Recreate polygons
125         LObject OLeftPadPoly_re = LPolygon_New( cellCurrent, SourceDrain , Larray , 4);
126         LObject OReftPadPoly_re = LPolygon_New( cellCurrent, SourceDrain , Rarray , 4);
127
128         //Create arrays for polygon on the right
129         LPoint Cpt1 = LPoint_Set(50000, -80000);
130         LPoint Cpt2 = LPoint_Set(0, -50000);
131         LPoint Cpt3 = LPoint_Set(0, -50000);
132         LPoint Cpt4 = LPoint_Set(-50000, -80000);
133         LPoint Carray [4] = {Cpt1, Cpt2, Cpt3, Cpt4};
134         //Draw polygon in the centre
135         LObject OCentrePadPoly = LPolygon_New( cellCurrent, SourceDrain , Carray , 4);
136
137
138       //TYPES OF STRUCTURES
139
140         //Overlapping
141         if(type==1){
142
143           //Tip
144           LObject OLeftPad = LBox_New(cellCurrent, Gate, -W/2-O/2, -90000, W/2+O/2, 50000-W/2-O/2);
145           LPoint Centre = LPoint_Set(0, 50000-W/2-O/2);
146           LObject Circle = LCircle_New(cellCurrent, Gate,Centre, W/2+O/2);
147
148         }
149         //Narrow
150         else if(type==2){
151
152           //Tip
153           LObject OLeftPad = LBox_New(cellCurrent, Gate, -W/2+O/2, -90000, W/2-O/2, 50000-W/2+O/2);
```

```
154           LPoint Centre = LPoint_Set(0, 50000-W/2+O/2);
155           LObject Circle = LCircle_New(cellCurrent, Gate,Centre, W/2-O/2);
156
157         }
158         //Equal
159         else{
160
161           //Draw polygon in the centre
162           LObject OCentrePadPoly = LPolygon_New( cellCurrent, SourceDrain , Carray , 4);
163           //Tip
164           LObject OLeftPad = LBox_New(cellCurrent, Gate, -W/2, -90000, W/2, 50000-W/2);
165           LPoint Centre = LPoint_Set(0, 50000-W/2);
166           LObject Circle = LCircle_New(cellCurrent, Gate,Centre, W/2);
167
168         }
169
170   /*****************************/
171 }
172 extern "C" int UPI_Entry_Point(void)
173 {
174   Master_BoloDevice_main();
175   return 1;
176 }
```

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Acronyms

DTU Technical University of Denmark. 21

CMi Center of Micronanotechnology. 17, 20, 36, 56, 57, 59, 60, 62, 63, 66, 67

2D-material Two Dimensional materials. 1, 3–5, 10–12, 15, 16, 24, 53, 54

ALD Atomic Layer Deposition. 33

BHF Buffered HydroFluoric acid. 19

CBKR Cross Bridge Kelvin Resistor. 24

CD Critical Dimension. 19, 20, 24, 29, 36

CVD Chemical Vapour Deposition. 3, 4, 10, 12, 21, 48

EBR Edge Bead Removal. 58, 60, 61, 64–66

EGT Equal Gate Tip. 23, 26, 39, 68–70, 72

EPFL Ecole Politechnique Fédérale de Lausanne. 17, 36, 56

HF HydroFluoric acid. 19–21, 33, 54, 56, 57

HGT Half Gate Tip. 23–25

HMDS HexaMethylDiSilazane. 58, 60, 61, 64–66

IPA IsoPropyl Alcohol. 22

IR InfraRed. 2–8, 10, 11, 13, 15, 53

MEMS Micro ElectroMechanical Systems. 3

NEMS Nano ElectroMechanical Systems. 11

NETD Noise Equivalent Temperature Difference. 8, 9, 11, 12

NGT Narrow Gate Tip. 23, 26, 34, 37, 39, 43, 44, 46, 68–71

OGT Overlapping Gate Tip. 23, 26, 34, 39, 43, 44, 46, 48, 68–71

PDMS PolyDiMethylSiloxane. 22

PMMA Poly-Methyl MathAacrylate. 22, 33

SEM Scanning Electron Microscope. 29, 34, 35, 44–46

SSP Single Side Polished. 19, 36, 56

TCR Temperature Coefficient of Resistance. 7, 11, 13, 14

TLM Transmission Line Measurement. 24

Glossary of mathematical symbols

$I_{\mathbf{SD}}$ Current flowing between the source and drain electrodes [A]. 48, 51

L_g Gap between source and drain electrodes in a bolometer design [m]. 23, 24

T_r Room temperature [K]. 2, 15

$V_{\mathbf{G}}$ Voltage applied to the gate electrode [V]. 48

$V_{\mathbf{SD}}$ Voltage applied between the source and drain electrodes [V]. 48

ρ_c Contact resistivity [Ωm^2]. 24, 47

ρ_s Sheet resistivity [Ω] or symbolically [$\Omega/\square$]. 24, 47

$h_{\mathbf{T\text{-}c}}$ Parameter of the T-Cell determining the graphene beam width. 38, 39, 71, 72

$o_{\mathbf{T\text{-}c}}$ Parameter of the T-Cell determining the spacing between the source-drain electrodes and the gate tip. 38, 39, 71

type Parameter of the T-Cell determining the type of bolometer. 38, 39, 71, 72

$w_{\mathbf{T\text{-}c}}$ Parameter of the T-Cell determining the graphene beam length and therefore the distance between the gate and source electrodes. 38, 39, 71, 72

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Bibliography

[1] Paul W. Kurse, Rudolph G. Buser, Michael F. Tompsett, Jun R. Choi, Raymond L. Filler, Charles M. Hanson, T.W. Kenny, Yonkee Kim, Paul W. Kruse, Nobukazu Teranishi, John R. Vig, and R. A. Wood. *Uncooled Infrared Imaging Arrays and Systems*. 2006.

[2] Fengnian Xia, Han Wang, Di Xiao, Madan Dubey, and Ashwin Ramasubramaniam. Two-dimensional material nanophotonics. *Nature Photonics*, 8(12):899–907, 2014.

[3] Ankur Gupta, Tamilselvan Sakthivel, and Sudipta Seal. Recent development in 2D materials beyond graphene. *Progress in Materials Science*, 73:44–126, 2015.

[4] M. Galeazzi and D. McCammon. Microcalorimeter and bolometer model. *Journal of Applied Physics*, 93(8):4856–4869, 2003.

[5] Massimiliano Galeazzi. Fundamental noise processes in TES devices. *IEEE Transactions on Applied Superconductivity*, 21(3 PART 1):267–271, 2011.

[6] Stephen D. Senturia. *Microsystem Design*, volume 1. Kluwer Academic Publishers, 2002.

[7] Frank Niklaus, Adit Decharat, Christer Jansson, and Göran Stemme. Performance model for uncooled infrared bolometer arrays and performance predictions of bolometers operating at atmospheric pressure. *Infrared Physics and Technology*, 51(3):168–177, 2008.

[8] Paul W. Kurse, Rudolph G. Buser, Michael F. Tompsett, Jun R. Choi, Raymond L. Filler, Charles M. Hanson, T.W. Kenny, Yonkee Kim, Paul W. Kruse, Nobukazu Teranishi, John R. Vig, and R. A. Wood. *Uncooled Infrared Imaging Arrays and Systems*, volume 47. 1997.

[9] Jun Yan, M-H. Kim, J. A. Elle, A. B. Sushkov, G. S. Jenkins, H. M. Milchberg, M. S. Fuhrer, and H. D. Drew. Dual-gated bilayer graphene hot-electron bolometer. *Nature Nanotechnology*, 7(7):472–478, 2012.

[10] H Zhang. Ultrathin Two-Dimensional Nanomaterials. *ACS nano*, (Xx):9451–9469, 2015.

[11] Jian-hao Chen, Chaun Jang, Shudong Xiao, Masa Ishigami, and Michael S Fuhrer. Intrinsic and extrinsic performance limits of graphene devices on SiO2. *Nature nanotechnology*, 3(4):206–9, 2008.

[12] F. H. L. Koppens, T. Mueller, Ph. Avouris, A. C. Ferrari, M. S. Vitiello, and M. Polini. Photodetectors based on graphene, other two-dimensional materials and hybrid systems. *Nature Nanotechnology*, 9(10):780–793, 2014.

[13] E Pop, V Varshney, and Ak Roy. Thermal properties of graphene: Fundamentals and applications. *Mrs Bulletin*, 1273(December):1–28, 2012.

[14] Fabian Purkl, Tim English, Gary Yama, J. Provine, Ashwin K. Samarao, Ando Feyh, Gary O'Brien, Oliver Ambacher, Roger T. Howe, and Thomas W. Kenny. Sub-10 nanometer uncooled platinum bolometers via plasma enhanced atomic layer deposition. *Proceedings of the IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, pages 185–188, 2013.

[15] Herman Bosman, Y. Y. Lau, and R. M. Gilgenbach. Microwave absorption on a thin film. *Applied Physics Letters*, 82(9):1353–1355, 2003.

[16] Gabriel Biener, Avi Niv, Vladimir Kleiner, and Erez Hasman. Metallic subwavelength structures for a broadband infrared absorption control. *Optics letters*, 32(8):994–996, 2007.

[17] Arend M. Van Der Zande, Robert A. Barton, Jonathan S. Alden, Carlos S. Ruiz-Vargas, William S. Whitney, Phi H Q Pham, Jiwoong Park, Jeevak M. Parpia, Harold G. Craighead, and Paul L. McEuen. Large-scale arrays of single-layer graphene resonators. *Nano Letters*, 10(12):4869–4873, 2010.

[18] O. Ryong-Sok, Makoto Takamura, Kazuaki Furukawa, Masao Nagase, and Hiroki Hibino. Effects of UV light intensity on electrochemical wet etching of SiC for the fabrication of suspended graphene. *Japanese Journal of Applied Physics*, 54(3), 2015.

[19] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer. Ultrahigh electron mobility in suspended graphene. *Solid State Communications*, 146(9-10):351–355, 2008.

[20] Peng Li, Zheng You, Greg Haugstad, and Tianhong Cui. Graphene fixed-end beam arrays based on mechanical exfoliation. *Applied Physics Letters*, 98(25):1–4, 2011.

[21] Allen L. Hsu, Patrick K. Herring, Nathaniel M. Gabor, Sungjae Ha, Yong Cheol Shin, Yi Song, Matthew Chin, Madan Dubey, Anantha P. Chandrakasan, Jing Kong, Pablo Jarillo-Herrero, and Tomás Palacios. Graphene-Based Thermopile for Thermal Imaging Applications. *Nano Letters*, 15(11):7211–7216, 2015.

[22] Q. Shao, G. Liu, D. Teweldebrhan, and A. A. Balandin. Higherature quenching of electrical resistance in graphene interconnects. *Applied Physics Letters*, 92(19):24–27, 2008.

[23] Bin Wang, Jianjun Lai, Hui Li, Haoming Hu, and Sihai Chen. Nanostructured vanadium oxide thin film with high TCR at room temperature for microbolometer. *Infrared Physics and Technology*, 57:8–13, 2013.

[24] T. Larsen, S. Schmid, L. Grönberg, A. O. Niskanen, J. Hassel, S. Dohn, and A. Boisen. Ultrasensitive string-based temperature sensors. *Applied Physics Letters*, 98(12):10–13, 2011.

[25] Silvan Schmid. Electrostatically Actuated All-Polymer Microbeam Resonators - Characterization and Application. *Scientific reports on Micro and Nanosystems Vol.6*, (18374):Der Andere Verlag, Zurich, Switzerland, 2009.

[26] Changyao Chen, Sami Rosenblatt, Kirill I Bolotin, William Kalb, Philip Kim, Ioannis Kymissis, Horst L Stormer, Tony F Heinz, and James Hone. Performance of monolayer graphene nanomechanical resonators with electrical readout. *Nature nanotechnology*, 4(12):861–867, 2009.

[27] Anja Boisen, Soren Dohn, Stephan Sylvest Keller, Silvan Schmid, Maria Tenje, T. Larsen, Silvan Schmid, L. Grönberg, A. O. Niskanen, J. Hassel, Soren Dohn, Anja Boisen, Luis Guillermo Villanueva, Michael Lee Roukes, Harrie A C Tilmans, Miko Elwenspoek, and Jan H J Fluitman. Fundamentals of Nanomechanical Resonators. *Sensors and Actuators: A. Physical*, 30(3):Der Andere Verlag, Zurich, Switzerland, 2011.

[28] Zongping Chen, Wencai Ren, Libo Gao, Bilu Liu, Songfeng Pei, and Hui-Ming Cheng. Three-dimensional flexible and conductive interconnected graphene networks grown by chemical vapour deposition. *Nature materials*, 10(6):424–428, 2011.

[29] Duhee Yoon, Young-Woo Son, and Hyeonsik Cheong. Negative Thermal Expansion Coefficient of Graphene Measured by Raman Spectroscopy. *Nano Letters*, 11(8):3227–31, 2011.

[30] Xinran Wang and Y Shi. Fabrication Techniques of Graphene Nanostructures. *Nanofabrication and its Application in Renewable Energy*, (32):1–30, 2014.

[31] K.S. Novoselov, A.K. Geim, S.V. Morozov, D Jiang, Y Zhang, S.V. Dubonos, I.V. Grigorieva, and A. A Firsov. Electric field effect in atomically thin carbon films. *Science*, 306:666–669, 2004.

[32] Max C. Lemme, Tim J. Echtermeyer, Matthias Baus, and Heinrich Kurz. A graphene field-effect device. *IEEE Electron Device Letters*, 28(4):282–284, 2007.

[33] Marc Drögeler, Christopher Franzen, Frank Volmer, Tobias Pohlmann, Luca Banszerus, Maik Wolter, Kenji Watanabe, Takashi Taniguchi, Christoph Stampfer, and Bernd Beschoten. Spin Lifetimes Exceeding 12 ns in Graphene Nonlocal Spin Valve Devices. *Nano Letters*, page acs.nanolett.6b00497, 2016.

[34] P. Blake, E. W. Hill, A. H. Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, and A. K. Geim. Making graphene visible. *Applied Physics Letters*, 91(6):13–15, 2007.

[35] J Bühler, F-P Steiner, and H Baltes. Silicon dioxide sacrificial layer etching in surface micromachining. *Journal of Micromechanics and Microengineering*, 7(1):R1–R13, 1997.

[36] Z. Moktadir. Graphene nanoelectromechanics (NEMS). pages 341–362, 2014.

[37] Mariana C Prado, Deep Jariwala, Tobin J Marks, and Mark C Hersam. Optimization of graphene dry etching conditions via combined microscopic and spectroscopic analysis.

[38] J.E. Holmes, P.J. and Snell. A vapour etching technique for the photolithography of silicon dioxide. *Microelectronics and Reliability*, 5(1):337–341, 1966.

[39] Man Wong, MM Moslehi, and RA Bowling. Wafer Temperature Dependence of the Vapor Phase HF Oxide Etch. *Journal of The Electrochemical ...*, 140(1):205–208, 1993.

[40] Ji Won Suk, Alexander Kitt, Carl W. Magnuson, Yufeng Hao, Samir Ahmed, Jinho An, Anna K. Swan, Bennett B. Goldberg, and Rodney S. Ruoff. Transfer of CVD-grown monolayer graphene onto arbitrary substrates. *ACS Nano*, 5(9):6916–6924, 2011.

[41] Leo J. van der Pauw. A method of measuring specific resistivity and Hall effect of discs of aribtrary shape. *Philips Research Reports*, 13(1):1–11, 1958.

[42] Alain C. Diebold. *Handbook of Silicon Semiconductor Metrology*. Marcel Dekker, New York, 2001.

[43] Keithley Instruments. Performing van der Pauw Sheet Resistance Measurements Using the Keithley S530 Parametric Tester. (3180), 2012.

[44] Stavitski, Klootwijk, Zeijl, Kovalgin, and Woolters. A Study of Cross-Bridge Kelvin Resistor Structures for Reliable Measurement of Low Contact Resistances. *IEEE Conference on Microelectronic Test Structures*, pages 199–204, 2008.

[45] Johanna Anteroinen, Wonjae Kim, Kari Stadius, Juha Riikonen, Harri Lipsanen, and Jussi Ryynänen. Extraction of Graphene-Titanium Contact Resistances using Transfer Length Measurement and a Curve-Fit Method. *World Academy of Science, Engineering and Technology*, 6(8):1457–1461, 2012.

[46] Shaoqing Wang, Dacheng Mao, Zhi Jin, Songang Peng, Dayong Zhang, Jingyuan Shi, and Xuanyun Wang. A more reliable measurement method for metal/graphene contact resistance. *Nanotechnology*, 26(40):405706, 2015.

[47] Joseph Carl Doll. *Advances in High Bandwidth Nanomechanical Force Sensors With Integrated Actuation*. PhD thesis, 2012.

[48] Kirt R. Williams, Kishan Gupta, and Matthew Wasilik. Etch Rates for Micromachining Processing-Part II. *Journal of Chemical Information and Modeling*, 53(9):1689–1699, 2013.

[49] Hua Zhong, Zhiyong Zhang, Bingyan Chen, Haitao Xu, Dangming Yu, Le Huang, and Lianmao Peng. Realization of low contact resistance close to theoretical limit in graphene transistors. *Nano Research*, 2015.

[50] Ferney A. Chaves, David Jiménez, Aron W. Cummings, and Stephan Roche. Physical model of the contact resistivity of metal-graphene junctions. *Journal of Applied Physics*, 115(16), 2014.

[51] Seung Min Song and Byung Jin Cho. Contact resistance in graphene channel transistors. *Carbon letters*, 14(3):162–170, 2013.

[52] Shuping Pang, Yenny Hernandez, Xinliang Feng, and Klaus Müllen. Graphene as transparent electrode material for organic electronics. *Advanced Materials*, 23(25):2779–2795, 2011.

[53] Gunho Jo, Minhyeok Choe, Sangchul Lee, Woojin Park, Yung Ho Kahng, and Takhee Lee. The application of graphene as electrodes in electrical and optical devices. *Nanotechnology*, 23(11):112001, 2012.

[54] Mark Griep, Emil Sandoz-Rosado, Travis Tumlin, and Eric Wetzel. Enhanced Graphene Mechanical Properties through Ultra-Smooth Copper Growth Substrates. *Nano Letters*, page acs.nanolett.5b04531, 2016.

[55] Ashok K. Sood, Isaac Lund, John W. Zeller, Yash R. Puri, Harry Efstathiadis, Pradeep Haldar, Nibir K. Dhar, Jay Lewis, and Priyalal Wijewarnasuriya. Development of graphene based detectors for EO/ IR applications. 9854:98540D, 2016.

[56] Wei Sun Leong, Chang Tai Nai, and John T L Thong. What Does Annealing Do to Metal-Graphene Contacts ? *Nano Letters*, pages 1–15, 2014.

[57] Osman Balci and Coskun Kocabas. Rapid thermal annealing of graphene-metal contact. *Applied Physics Letters*, 101(24), 2012.