Semester Project
Nano-SAW Devices for Wireless Identification

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I. Introduction

Surface Acoustic Wave (SAW) technology is omnipresent in the devices around us today, mainly used as passive bandpass filters in most radio systems like smartphones and TV antennas or as delay lines in telecommunications [1]. More recently, the possibility to use SAW devices for wireless identification has surfaced and generated the first widespread applications such as on the highways in Norway [2] over 2 decades ago. Their environmentally robust structure and passive use is very interesting for many applications in outdoor environments or chemically challenging places. It is possible to read many of them simultaneously and the amount of information that can be carried is much higher than printed barcodes [3].

This semester project was aimed at learning how to design and fabricate an RFID device based on SAW technology in a cleanroom and trying to optimize the parameters of the device while reducing its size. Optical lithography tools with feature sizes down to 2 μm will help achieve this before E-Beam lithography can further decrease the features in scale of the structures involved in a SAW RFID tag.

While creating an entire working wireless tag would take more time than available, the objective is to take this project as far as it can to pave the way for future students to search on this topic and increase knowledge about SAW devices' fabrication in the Advanced NEMS group at EPFL.

II. STATE OF THE ART

The basic principle of a SAW RFID tag is fairly simple. As illustrated with Fig. 1, the IDT structure can send a wave across the surface on a piezoelectric substrate, which is then partially sent back by every reflector on its way.

To generate this SAW, a RF pulse is emitted by the transceiver, received at the antenna of the device and has then enough power to generate the SAW wave, get reflected and sent back again through the antenna to the receiver to be read out, showing each reflector and their respective locations.
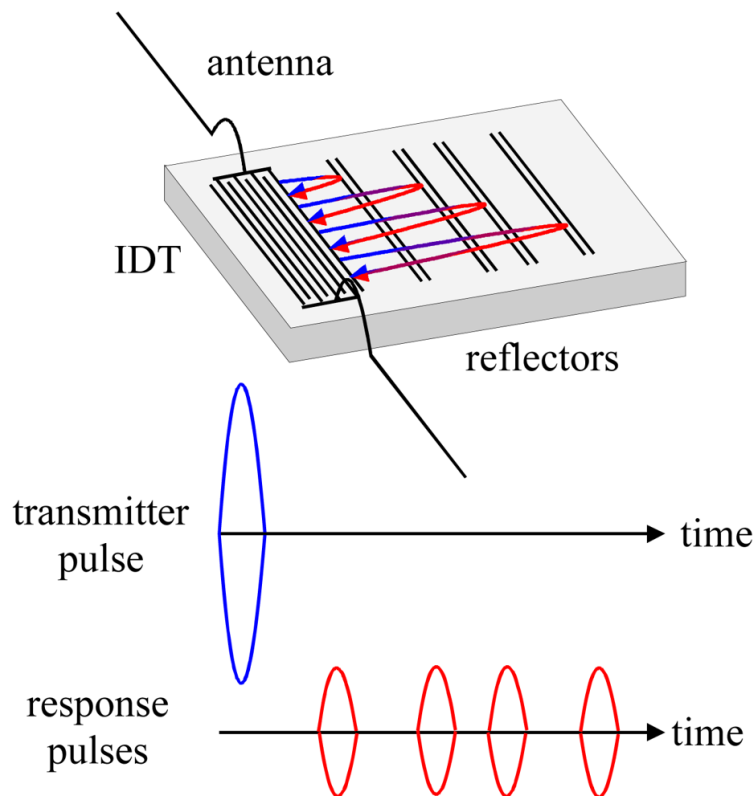

Figure 1: Basic principle of a SAW RFID tag. *http://www.mdpi.com/1424-8220/9/12/9805/htm, 26.5.2014*

Materials Used

For the wave to propagate, the substrate has to be piezoelectric. The electrical field appearing between the IDT fingers when a pulse is sent will generate a contraction or an expansion in the material which then immediately propagates as a wave in both directions. The two most common materials used in SAW device research are Lithium Niobate ($LiNbO_3$) and Lithium Tantalate ($LiTaO_3$) [1] [4], 2 single-crystalline quartzes of which specific cuts are used to have the highest piezoelectric coupling factor, but most people use Lithium Niobate, which has, according to [5], the higher piezoelectric coefficient of the 2.

We got our chips from SRICO, inc., Columbus, OH, USA. The wafer was diced into 14x15x0.5mm chips of X-cut (X axis normal to surface) Lithium Niobate.

The IDT fingers and reflectors should be good conductors, and easily processable with standard photolithography tools, hence they are made of metal. Usually Aluminum [1] or Gold, but Platinum on Titanium, Rhodium or Iridium have also been looked at for higher temperature applications [6]. We decided to use Gold because it can be thinner than Aluminum, has better conduction and doesn't oxidize.

RFID Tags

SAW RFID tags have the very useful feature to be wireless. The RF pulse, which ranges between 500 MHz up to 8 GHz with special ultra high frequency structures [1][3], emits with a power of around 10 mW, not more is needed for these ID tags to work, which is then sent back with less than a μW.

The advantage of SAW RFID tags, is that they can operate under any conditions, their working distance can be of several meters, and their fabrication is fairly simple and cost-effective [4].

To use them as ID tags, it is possible to use the reflectors as a code. Being either a 1 when there is a reflector and a pulse is sent back, or a 0 when it is absent. It is practically possible to have an almost infinite amount of different codes, devices with up to 128 bits were demonstrated in [7].

III. SAW DEVICE DESIGN

Interdigital Transducer (IDT) Models

Interdigital transducers (IDTs) are basically like static comb drives. They are used in a SAW device to generate the wave from a signal, or generate a signal from a wave. A standard IDT is shown in Fig. 2, it is made of alternating electrodes. The wavelength of the generated SAW is determined by the period of the IDT. Non-standard structures with varying widths can produce different SAWs, reflect them or not or get them to propagate in a single direction like SPUDTs, which will be seen later.
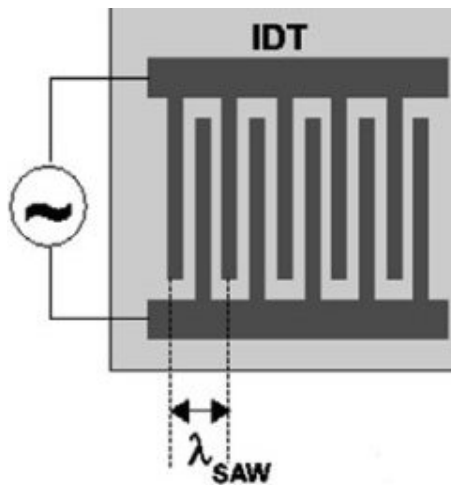

Figure 2: An illustration of a standard IDT. *www.bionano.re.kr*

Variable Parameters

There are various parameters which can be changed to get a better SAW device and could allow it to be reduced in size. The ones we explored are the following:

- IDT designs: A standard IDT will send a SAW in both directions, which results in a 50% loss of the signal intensity from the start. To prevent this, unidirectional IDTs called UDTs (Unidirectional transducers) can be designed that send the SAW in a signal direction. The IDTs we tested were taken from [8], and are shown in Fig. 3. The DART, a), b) and d) were implemented in this project, to find which one would give the more interesting results.

  As for the standard IDTs, we expected them to be the easiest to fabricate and show consistent results. Increasing the amount of fingers increases the wave intensity and its width, reducing the quality factor. It is therefore important to find the right value such that the individual reflections are not mixed with each other which would make it impossible to dissociate every pulse [9].

- Y-Z orientation: SAW propagation changes depending on the angle you send the wave at, because the piezoelectric coefficients vary a lot in Lithium Niobate's highly
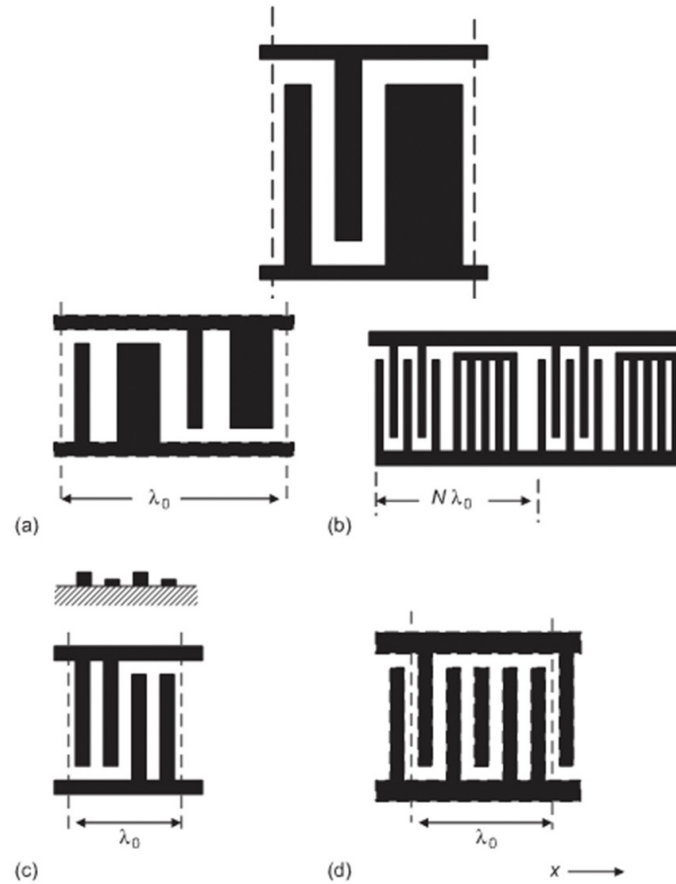
Figure 3: The different UDT that were used by different research groups. The DART (Distributed Acoustic Reflection Transducer) at the top, a) Hanma-Hunsinger UDT, b) Lewis-group UDT, c) Hartmann UDT (variable thickness) and d) Yamanouchi UDT.

asymmetric crystal. The chips we got were X-cut, meaning that the surface of the wafer is the Y-Z plane. The most intense SAW is expected to be along the Y-axis, as it is the one along which the piezoelectric coefficients appear to be the highest [10].

- Distance between the IDTs and the first reflector: various papers suggest that one should leave a minimum distance between the IDTs and the first reflector in RFID tags to avoid that the signal merges with the echoes of returning waves from the surrounding walls or other objects. According to [4], an appropriate time delay for this is about 1 μs, which is around $\frac{1e-6\ s\ \cdot\ 4000\ m/s}{2} = 2mm$ of distance for an average wave speed of 4000 m/s on a Lithium Niobate surface and divided by 2 because the wave travels twice this distance before it is caught again by the IDT. This problem is non existent for non-wireless SAW devices, and could shrink them drastically. However, it cannot be avoided when going back to wireless.

- Aperture size: the width of the IDTs define the width of the SAW wave as well, reducing it will reduce the power of the SAW which could give less accurate results.

- Reflectors: There are 2 types of reflectors that are commonly used, a simple one and an IDT version, as shown in Fig. XXX(clewin). The simple reflectors have the advantage to take less space and can therefore be used in a more dense configuration, whereas the IDT reflector will yield higher amplitude pulses which are more easily identifiable. It was suggested to enclose the simple reflectors with 2 IDT reflectors to locate the signal, but it could be interesting to make use of the IDT reflector only if the signal of simple reflectors becomes to small.

- Thickness: The thickness of the electrodes can be changed, we used 50nm Au on 10nm Cr, for adhesion purposes.

- Minimum finger line width: As shown in Fig. 2, the thinner the fingers, the smaller the SAW wavelength. This allows the device to be operated at higher frequencies which offers a number of advantages like increased sensitivity, reduces size and easier access to wireless bands, like the ISM band between 2400 and 2483 MHz, which can be used by anyone. But these frequencies require 0.3-0.4 μm wide IDT fingers. For this project we had access to optical lithography tools, which can offer down to 0.8 μm feature sizes when tuned properly. So to avoid excessive trials, we decided to go for a minimum feature size of 2 μm on our designs.

Probe Contact Pads

Once the devices look good enough in the cleanroom, they will be characterized using a probe station which uses GSG (ground-signal-ground) probes. These probes allow shielding like a coaxial cable does, by redirecting all the emitted and lost electrical field lines towards the two ground pads on either side of the signal pad. This is shown in Fig. 4

The probe station available at EPFL uses 150 μm spaced GSG probes and the pads were made of 100x100 μm squares.
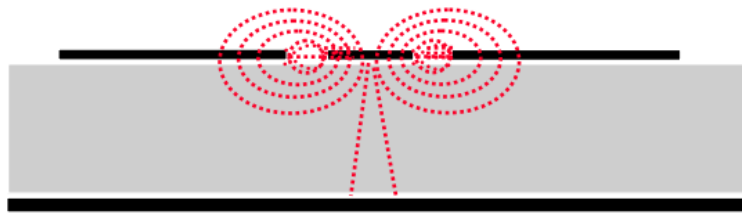

Figure 4: Basic principle of a GSG probe. Ref. [11]

IV. FABRICATION

Full Fabrication Process

Quick Stick 135

To use the chips we got from SRICO, Inc. which are 14x15x0.5 mm, with all the CMi cleanroom equipment easily, we have to glue them on standard silicon wafers. The substrates were provided to us by CMi and were dummy wafers with old rectangular patterns on them which made it very easy for us to manually put the chips in the very center, such that it easily aligns with our masks.

The Quick Stick from zone 6 was used, and the wafer was then put on the entrance zone hot plate at 135 degrees Celsius, Quick Stick is then applied and left to cool afterwards for at least half an hour. The speed of the pins going down was reduced to 30% due to Lithium Niobate's pyroelectricity, which reacts only to a gradient in temperature, this allows it to heat less fast and avoid any disturbance.
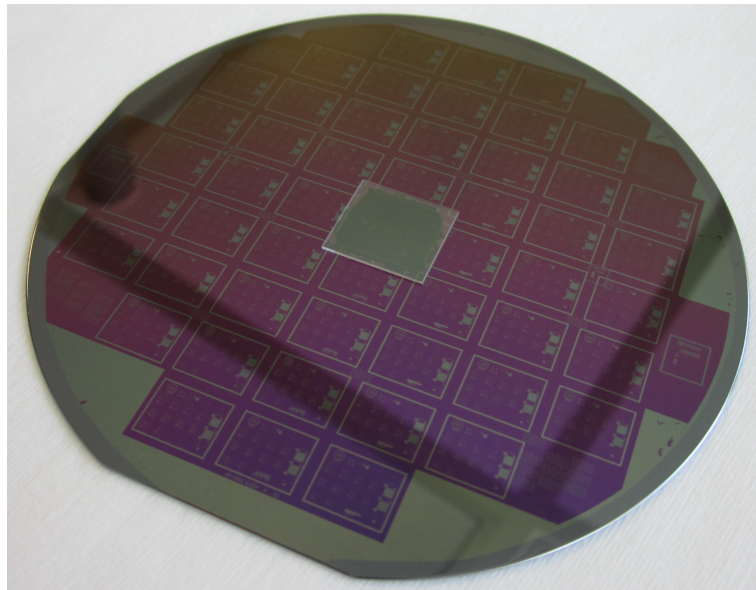
The result is shown in Fig. 5.

Figure 5: A Lithium Niobate chip glued on a silicon substrate using Quick Stick, alignment was done manually with the patterns on the wafer

Tepla Gigabatch Strip

Before coating the chips with resist, we were recommended to do a short stripping step using the Tepla Gigabatch Microwave plasma stripper from zone 2. The recipe that was used was "PR_Strip_Low_30s", which works with a 200W plasma for 30 seconds.

A trial with the "PR_Strip_High_30s", which works at 600W, resulted in the Lithium Niobate chip being removed, it fell on the bottom of the machine and was damaged severely

when we tried to get it out. Furthermore, the chips had been glued using Quick Stick for only 20 minutes, which might have actually caused this, and not the higher power.

EVG150 Coater and Developer

The photoresist (PR) we used was AZ2070 nLoF, which is meant to be used for lift-off and offers a higher resolution than a standard positive resist. The entire recipe used for the EVG150 is in the annex, and is the standard recipe for nLoF at CMi, except for the baking temperature, which was reduced due to Lithium Niobate's pyroelectricity.

XXX PR wall angle problems, increasing baking time increases the slope of walls.

Suess MA6 Exposer

This machine was used to expose the chips, using the following settings:

- Process: Lithography

- Exp time: variable

- Gap alignment: 100μm

- Type contact: hard

- HC wait times: 10s

- WEC Type: Cont

- N2 Purges: No

- WEC-Offset: OFF

All of our exposure times were between 4.5 and 5.2 seconds, which was around the recommended 4.8s for nLoF and our chip material. These variations allowed us to optimize the exposure time to get the best results.

Photoresist stripping

After every generation, the photoresist was stripped so that the chips could be reused for another trial. This was done using a Technistrip bath for a few minutes followed by a DI water rinse.

Lab600 Metallization

To apply a metallic layer on our chips, we used the Lab600 machine from zone 2. We used Au on Cr and Al layers from 10 to 50 nm.

Lift-off

Once the wafers are coated with Chromium and Gold, lift-off can take place. This requires the wafers to be placed in a SVC 14 bath for a few hours, it is best to leave it over night. Once that is over, a DI water rinse with an ultrasounds bath for 25 minutes cleans the wafers which then only need to be dried.

1st Gen.

Mask Design

1st Mask

The mask was designed to allow a first filter in all the different parameters we can change to get the best SAW device. The total design for a chip is shown in Fig. 6 and a close up of one of the devices in Fig. 7.
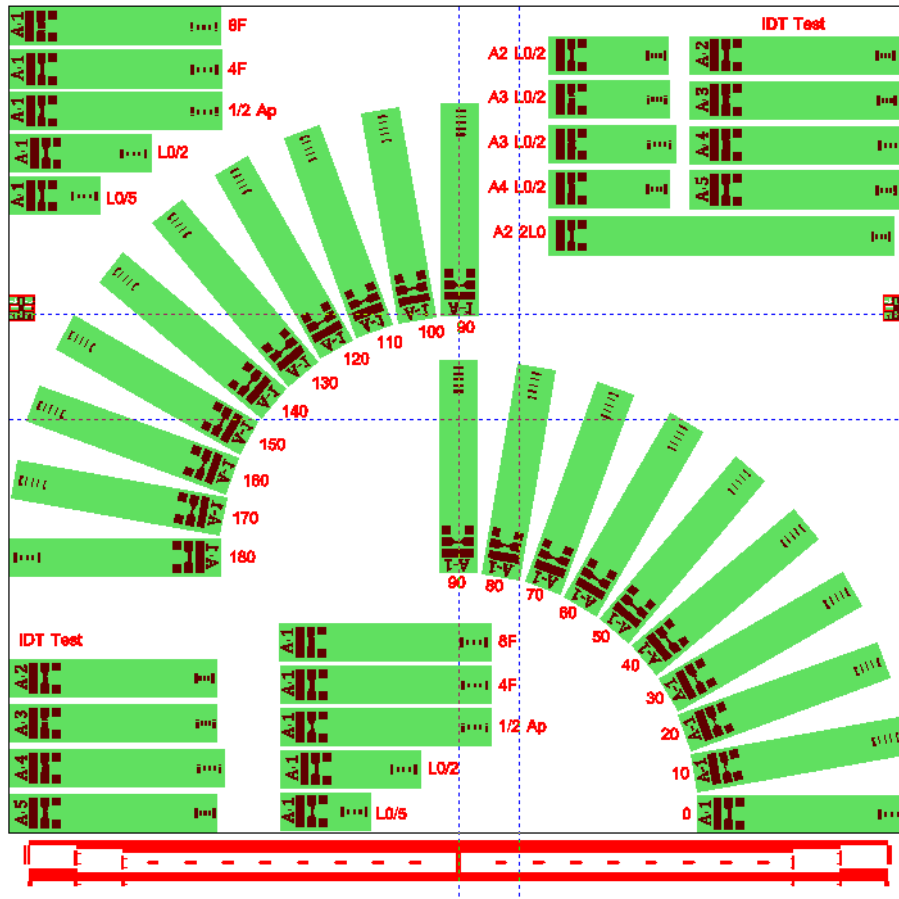

Figure 6: Design of the 1st mask as seen from clewin.

There are 3 subsymbols in this mask, an IDT test, an angle test and another test with various trials. All are used twice in different places on the mask to

- The IDT test is in the top left corner and lower right corner, it is using one different IDT design from [8] for every device, DART, Lewis, Hanma and Yamanouchi.

- The angle test will help find out which orientation in the x-y plane gives the best wave propagation, to get a full 180 degree test we used the same subsymbol twice starting with a 90 degree difference. All IDTs used for this test are standard, since we expect those to work without much effort to be able to focus on the angle testing and not IDT testing.
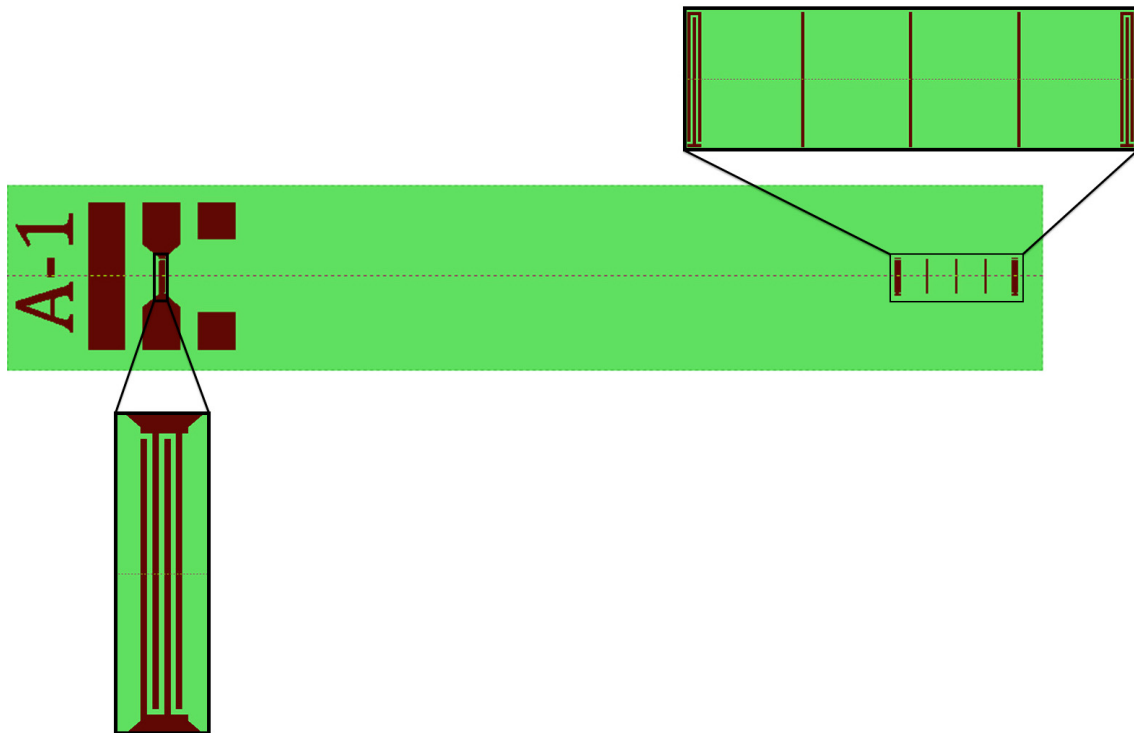
Figure 7: A close up of one of the devices, showing the IDTs and the reflectors.

- One subsymbol next to the upper left IDT test, tries to find out what a length reduction by half will change in the output. A 5th device with double length is also designed to see if a large delay time at the beginning is important or not. The changed length is from the IDT to the first reflector.

- The last subsymbol tries to find out multiple settings: the 8F and 4F test are simply standard IDTs but used 8 and 4 times respectively, to see how an increase in the amount of standard IDTs next to each other affects the SAW intensity and quality factor. The 1/2 Ap was supposed to see what a decrease of 50% in the aperture would do to the SAW device, but the design was done wrong, both fingers are shorted which won't create a SAW wave. The 2 lower designs are actually used to see a length reduction by half and by 5, like the previous subsymbol.

Furthermore, there are 2 alignment crosses on the left and the right for a second mask to be aligned and an alignment guide below to help for rough alignment.

6 additional squares are placed outside of the chip region to reduce the laser writing process of the mask while keeping some margin around the chip to see through. Since it is larger horizontally than vertically, it is important to verify that the mask is written with horizontal passes, otherwise writing time will be longer, since it will have to do many short vertical passes.

2nd Mask

A second mask was designed to create a small trench around the devices, this would have to be done with an E-Beam. It is meant to isolate the devices from each other, since

the SAW are travelling at the surface. A small gap would therefore simply block them, avoiding extra parasitic signals. The structures are simply the green rectangles of Fig. 6 and actually are of no use in fabrication, since we would want to use an ion beam to cut these trenches, which is not performed with a mask. A picture is shown in Fig. 8.
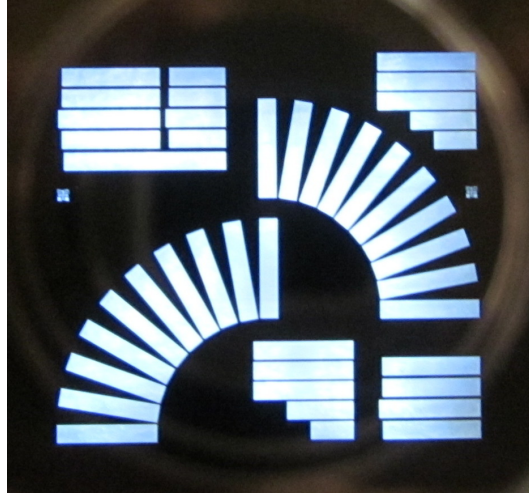

Figure 8: A picture of the second mask fabricated for the 1st generation showing the locations of the different devices.

Mask Fabrication

The mask fabrication was done during the formation and written with the wrong polarity. The Chromium was etched where the metal should have been deposited, which should have been the other way around when using the nLoF lift-off process.

All resulting wafers therefore had photoresist on the designs at the wrong place.

Remark: A small error occurred during the file conversion, saying "Box with zero width or length" indicating it occurred several times. It was solved by doing the following: ignore All Errors -> edit layer properties to add a gds number -> export in gdsii format.

Wafers, 7.5.2014

Before realizing the error, 2 chips went through the entire process flow with a final Cr-Au coating:

- The first wafer had an unexpected development problem, probably due to very recent formation we got to use the EVG150 and MA6, which made it hard for us to use the exposer properly, as can be seen in Fig. 9. All of the structures are very hard to distinguish and completely off.

- The second wafer showed some proper results, with most of the structures in place and distinguishable except for the reflectors, of which only the IDT ones were present a few times. Exposure time was probably the reason for this, which was too short
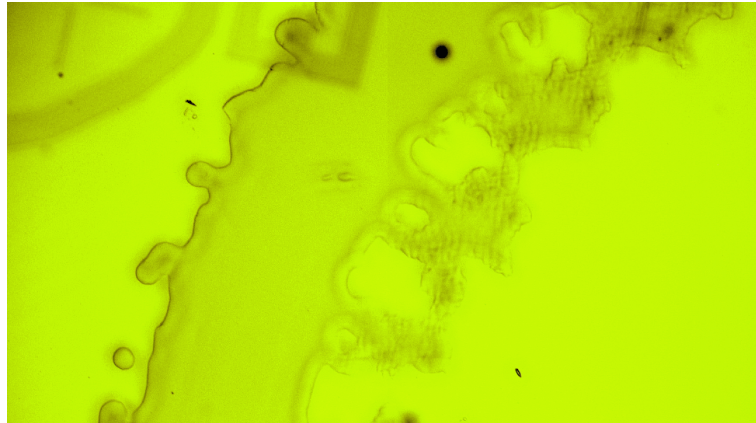
Figure 9: The first wafer after development under the microscope showing (probably) the angle test. (magnification = 5x)

to get the very fine structures to appear. Fig. 10 shows the structures after gold coating, before lift off.

The standard IDT which can be seen above shows some residues between the fingers, which is probably unremoved PR from the too short exposure. The IDT reflector below is incomplete, as it is missing the 2 connected fingers which should be on either side of this central finger.

Wafers, 21.5.2014

6 more wafers were coated, exposed and developed to adjust the exposure time for the next generation. from 4.4 to 5.4 seconds were tried, with a step of 0.2s every time.

The 2 first wafers with 4.4s and 4.6s were already stripped to be used again, but the 4 others were observed under the microscope, with the most interesting results occurring at 4.8s as can be seen in Fig. 11. The structures appear to be very close to the mask, with the gaps being clearly defined and of the same width as the fingers.
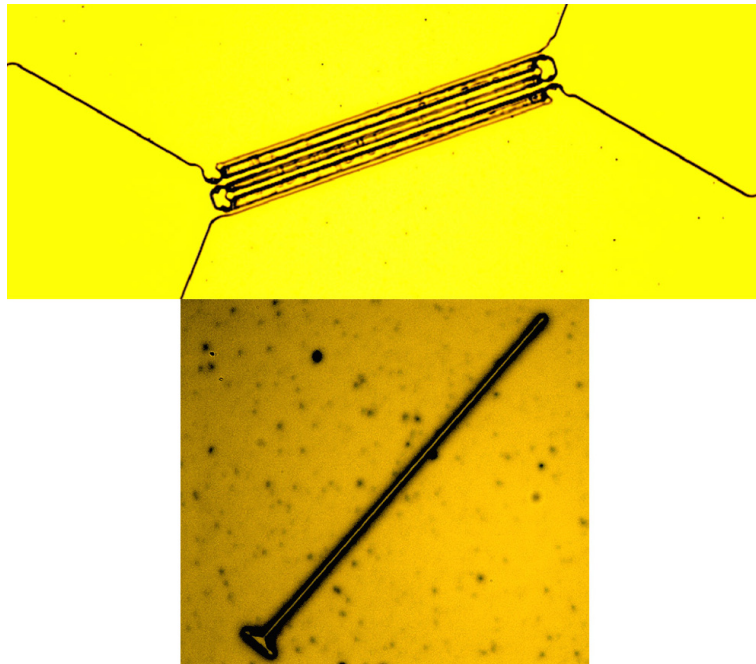
Figure 10: 2nd wafer after gold coating, shows a standard IDT and an incomplete IDT reflector. The length of these structures is 100 μm. (magnification = 50x)

2nd Gen.

Mask Design

Mask design was exactly the same as for 1st Gen., but the polarity was reversed such that it gives us the results we are expecting using the lift-off process.

Mask Fabrication

The mask fabrication went exactly as planned using the standard method. An Image of the mask is shown in Fig. 12 The most intricate structure (Lewis IDT) on the mask came out very well, as seen in Fig. 13.

Wafers 23.5.14

The first 2 wafers to be tested with the new mask turned out bad because I used the wrong side of the mask with the MA6, which resulted in the very poor structures shown in Fig. 14.

Wafers 28.5.14

The next wafers processed went very well. They were exposed with 6 different times: 4.5, 4.6, 4.7, 4.8, 4.9 and 5 seconds. A comparison of one of the structures is shown in Fig.
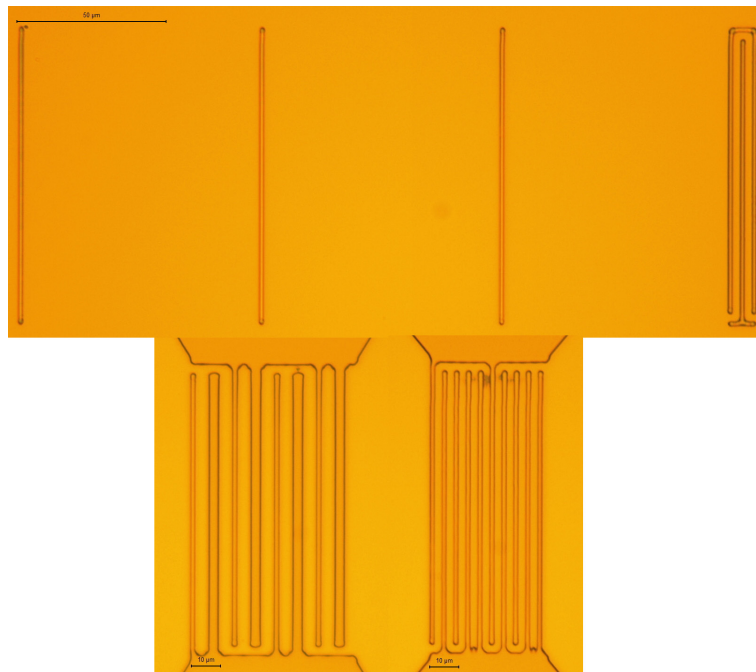
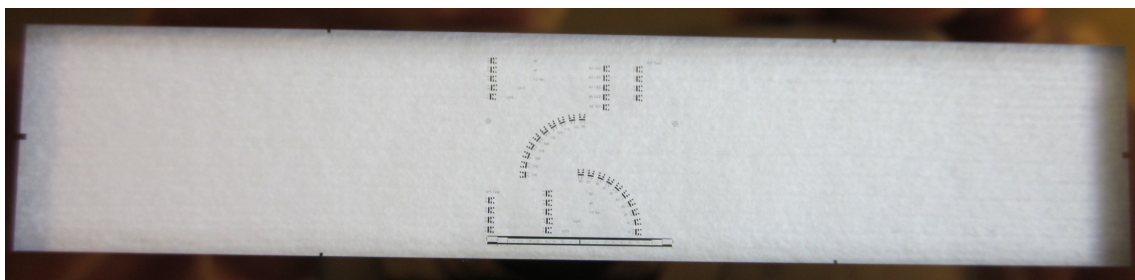Figure 11: Different structures on the 4.8s wafer. (magnification = 50x)

Figure 12: An image of the 2nd Gen. mask taken in CMi zone 6.

16. Some have 4 pairs of fingers and some 8, this to show the best possible IDT that was present on the wafer, the structures being just a repetition of a standard IDT.

The IDTs and the 2 cones on the top and at the bottom are where the PR has been removed. The other parts have been exposed, and hardened before development, which then stay in place.

Observations

What can be seen pretty well is the gap between the fingers increasing with a longer exposure time. It seems therefore interesting to keep increasing the exposure time until we reach an almost 2 μm gap and 2 μm finger, as it is on the mask, as long as it doesn't affect the development. The finger line width is around 2.6 μm and 4.2 μm for double width fingers on the 4.8s wafer.

The black parts we can see on the 5.0s wafer in Fig. 16 appear to be remains of PR which haven't been removed properly. Since those parts haven't been exposed, they should
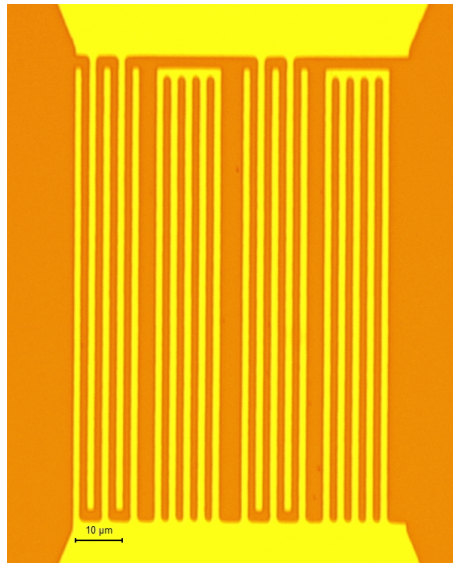
Figure 13: An image of the lewis type IDT on the mask under the microscope, yellow parts is the Cr, orange is etched. (magnification = 50x).

not have anything to do with the exposure time, and could only be the result of the development not being right. Another example of these PR remains are shown in Fig. 17, with the reflectors of the 4.7s wafer.

Another interesting result is shown in Fig. 18, where the remains appear in a periodic fashion on these IDTs. It is currently unknown to me how this could have happened and what this means for exposure and development.

The total amount of good structures was counted roughly as well. For the reflectors to be counted as good, the 2 IDT reflectors and the 3 simple reflectors had to be good, without any PR remains. It yielded the graph shown in Fig. 15. It can be seen that on average, there are more reflectors which turn out good than IDTs, this mainly because of some of the intricate structures like the Lewis IDT which never came out properly. There is a very big drop for the 5s wafer, where almost all of the structures had some PR left, it might be that it is the chip which had an unknown problem, since there is no clear fall for 4.8s and 4.9s, which are at the same levels than 4.5s and 4.6s respectively. It would have been interesting to process this chip again with another exposure time to see if that was the cause, or if these PR remains do appear because of a different exposure time.

This generation was the first to have most of the settings correct. The exposure time seems to need even more than 5.0s to obtain the correct spacing between the fingers and their own widths. But increasing it seems to get the non exposed parts to fail during development. Preventing us from exposing during a longer time.

Another idea is that it might come from the reflections of the Hg lamp during exposure. The chips being transparent, the light might reflect non-uniformly due to the Quick Stick underneath which isn't applied in a very clean way. To try and fix this, we thought about plating the back of the chips with a thin layer of Al, such that the reflections are uniform across the chip.
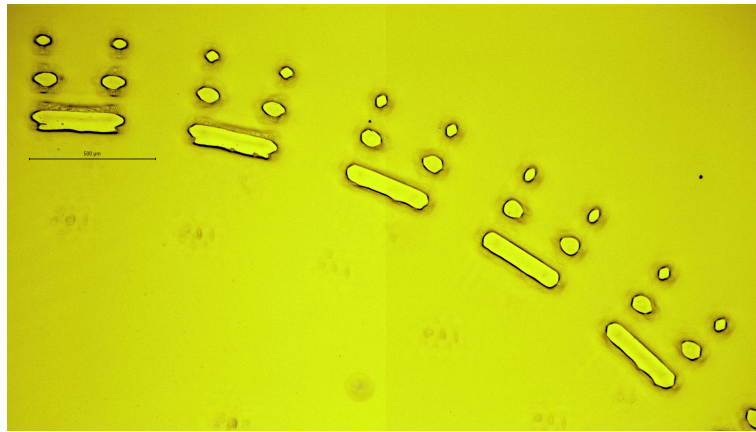
Figure 14: The first 2 wafers processed were made using the wrong side of the mask. (scale indicates 500 μm) (magnification = 5x)
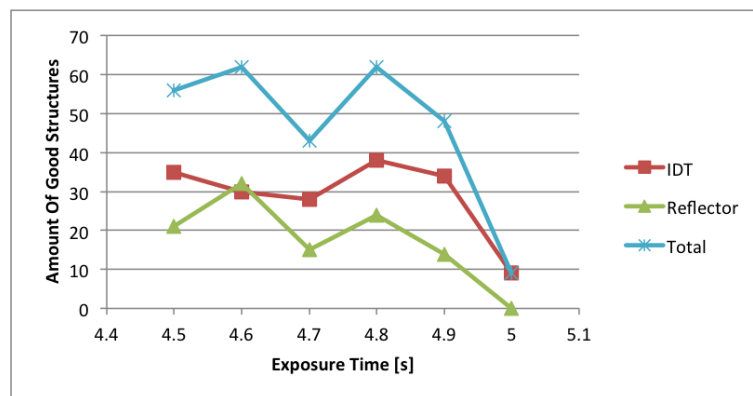

Figure 15: Evolution of the amount of good structures on a chip depending on the exposure time.

3rd Gen.

For this Gen., the back of the Lithium Niobate chips was coated with a thin Al film to try and improve the structures of 2nd Gen. To do this, we reused the chips we had until now, which had to be done without damaging the top surface. Only 5 of the 6 chips got a proper result.

The steps we took were the following:

- Strip the remaining resist.

- Manually put a thick layer of resist on the chips with a pipette to protect the top surface.

- Bake it for a few seconds and remove the chips as the Quick Stick loosens while it is on the hotplate.

  Remark: It might have been better to bake the resist, let the chips cool while attached on the wafers for a few hours, and then heat them again to remove them from the wafers, this would have made the manipulations cleaner.
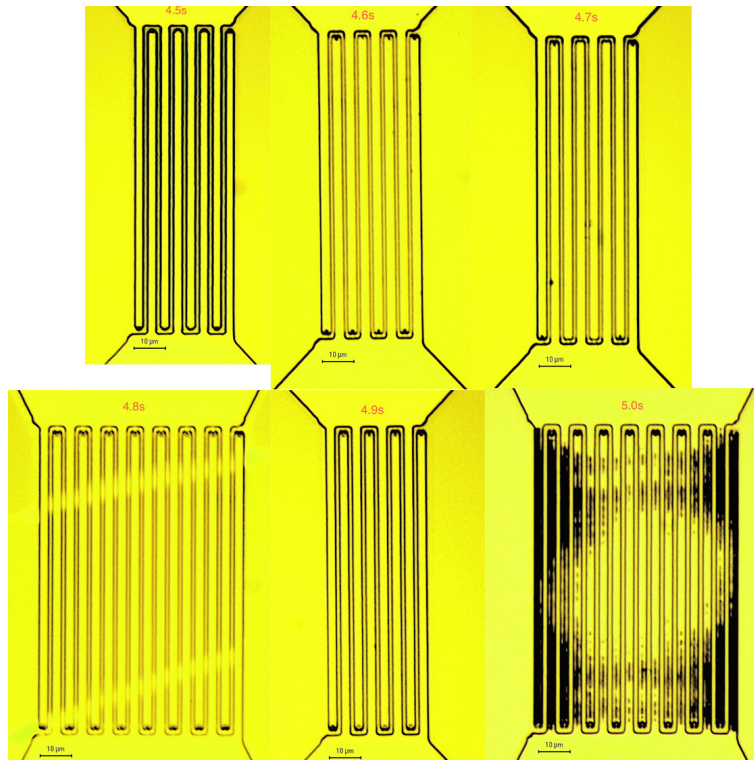
Figure 16: Comparison of a standard IDT for 6 different exposure times. (magnification = 50x)

- Manually remove the remaining Quick Stick from the backside of the chips with Acetone and then Isopropanol.

- Tape the chips on a clean wafer using Polyimide tape (for high Temperature applications) from zone 2 in CMi as shown on Fig. 19.

- Metallize the chips with 50nm Al using the Lab600.

- Remove the tape and Quick Stick the chips back on single wafers.

- Strip the thick layer of resist off the top side.

Mask

The mask we used was exactly the same as for 2nd Gen.

Wafers

A single batch of wafers were put through the entire process, of the 5 chips, one turned out to be very dirty and was expected to have only bad results. That chip was exposed during 4.5s, the 4 others with 4.6, 4.7, 4.8 and 4.9 seconds.
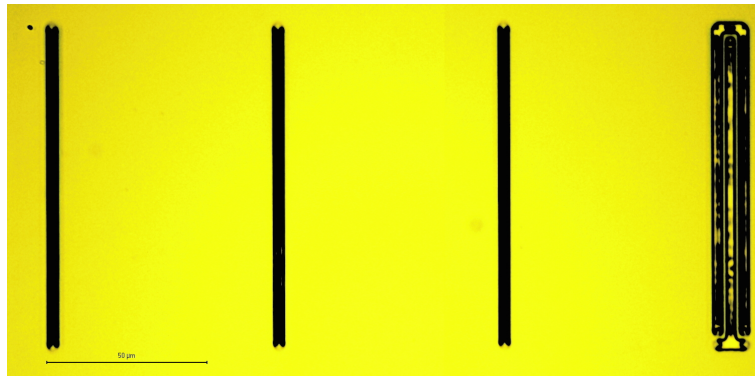
Before metallization

Figure 17: An image of the reflectors on the 4.7s wafer showing the PR remains. (magnification = 50x)
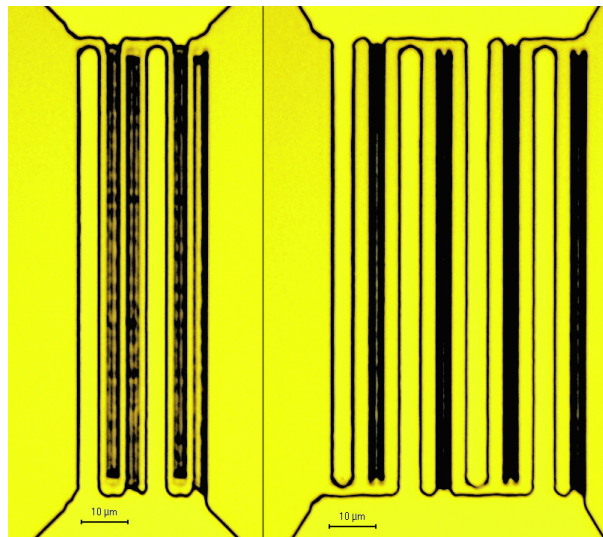

Figure 18: PR remains appearing in a periodic fashion for 2 different structures on the wafer with a 5.0s exposure. (magnification = 50x)

A comparison of the different exposures is shown in Fig. 20. What can be seen is that the gaps between the fingers are much clearer when increasing the exposure time, this is quite good if there weren't other clearly visible problems. On the 4.8 and 4.9s exposures, it can be seen that there is a thin wall at the top and bottom of the fingers, indicating that the PR hasn't been completely removed along the fingers, but that there is still some left.

This means that the PR below could have hardened significantly with an increasing exposure time of only 0.1s from the 4.7s wafer which didn't show any of this. It is apparently not due to a bad chip or bad luck, since it is clearly happening on the 2 longer exposed wafers and not at all on the 2 shorter exposed wafers.

This effect did not appear on as clearly on any of the other wafers we have processed so far, and could therefore come from the back Al metallization, however the exact reason behind this is still unknown to me.

The Al back plating did show some interesting results, mostly concerning the gaps between
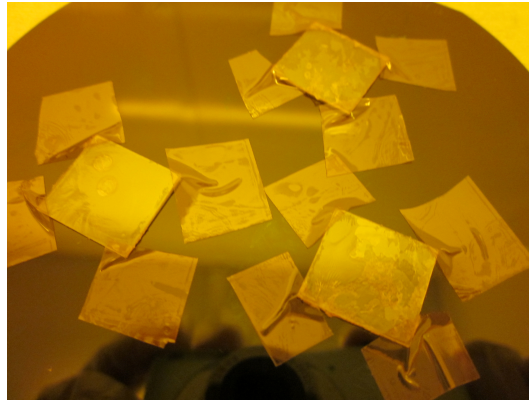
Figure 19: The chips taped on the wafers before metallization.

the fingers which seemed to have become larger than what we were experiencing before. In Fig. 21 a), a Lewis type IDT is the best result we have gotten from this structure, where usually it was hard to distinguish the gaps in the closed finger structure which repeats twice. Those gaps are fine PR structures, and are about as long as simple reflectors with the same 2 μm width.

Fig. 21 b) shows a pair of reflectors which was very frequently visible after development on the 5.0s exposure wafer. The reflectors have barely been removed during development, which looks like another step further from the black PR remains from previous generation. It again happened on a longer exposure time wafer, which means the development of the unexposed regions is affected by the exposure time a lot.

Lastly, Fig. 21 c) and d) show 2 characters which were written next to the devices to recognize them more easily under the microscope. The hole in the 'A' and the 2 holes in the '8' didn't show at all, while the structures are pretty big, compared to the 2 μm wide reflectors which have usually been the hardest to get.

After metallization

After observing the 4 chips, we decided to take the 4.6s and 4.7s wafers through metallization and lift off, even though they were probably worse than the wafers of Gen. 2. This was done to fabricate the devices properly until the end and to see if any interesting results would appear despite the somehow incorrect structures.

Fig. 22 shows some of the results after lift-off. Fig. 22 a) shows how most of the IDTs ended up on both wafers, completely removed, without anything in the center. Fig. 22 b) shows the best IDT that was found on both wafers, the gaps and finger line widths seem to be exactly as in the design with 2 μm, Fig. 22 c) displays the best group of reflectors that was found on both chips except for d) which is a group of reflectors that was on top of a region where there was no Al on the back because it was on the edge were the tape was holding it. It turned out to be exceptionally good.

This last image could mean that Al back metallization was actually a bad idea. While it is possible that those reflectors turned out so good because they were near the border and it experiences some very favorable conditions, it is also likely that has to do with the Aluminum.
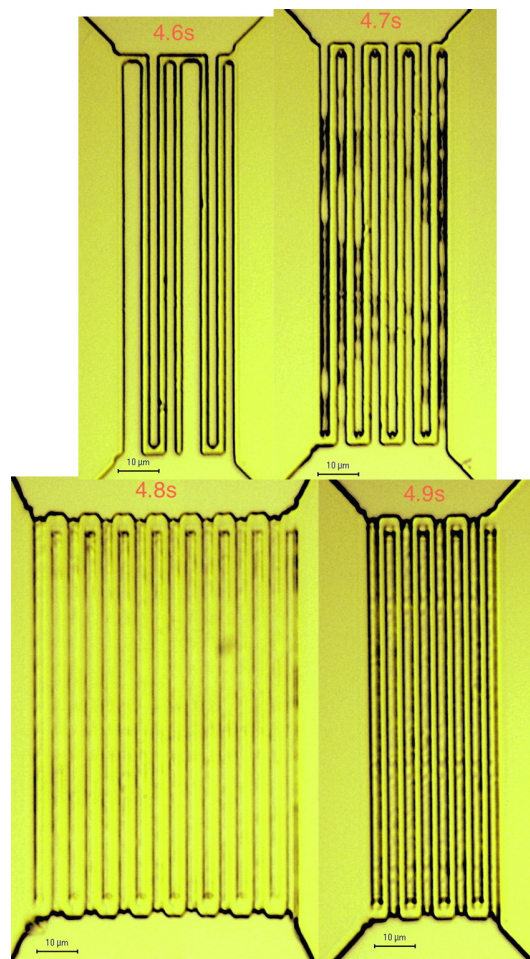
Figure 20: An evolution of the structures on the Al back coated chips depending on exposure time.

But even though most of the structures got destroyed, the ones that turned out good, got some exceptionally good results, with very fine lines, which weren't experienced until now. More tests will probably need to take place before a clear conclusion about this technique can be made.
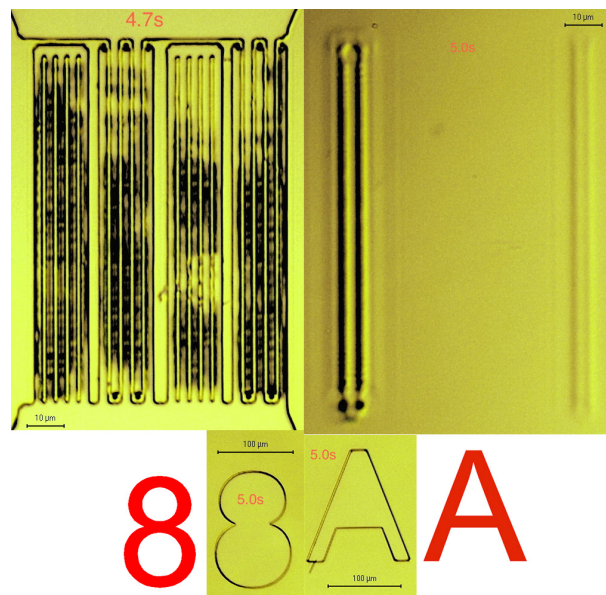
Figure 21: a) shows the lewis type IDT for a 4.7s exposure, it is the best result we have ever got for this very intricate structure. b) shows a group of reflectors for a 5.0s exposure, the PR has almost not been removed here. c) and d) show an 'A' and an '8' on the 5.0s exposure wafer, the centers have not been carved out at all.

V. Future Work

Getting the exposure right

From the results obtained during this project, it is clear that there is still some work to be done to obtain the perfect patterns on the chips. The last generation of chips we fabricated might have worked better if the chips were cleaned properly or if new chips would have been used. The profiles in Fig. 23 show the surface roughness for a chip before 3rd Gen. processing and a clean chip, there is no huge difference between them, even though the clean chip seems to be a bit more contained, with the same average but a smaller standard deviation than the used chip. One of our ideas was that all the generation these chips went through with the different processes, and removals of PR would damage the surface significantly enough to yield worse results for each additional generation, which is apparently not the case.

Other exposure times should be used to identify if above 5.0s is actually valid or if it indeed affects the development afterwards.

Only once the structures appear to be very close to the design should it be really interesting to characterize the chips without having flawed results due to the fabrication.

We could notice that the reproducibility of our tests wasn't very good, with large variations between the trials and incoherences between the failures on a same chip.
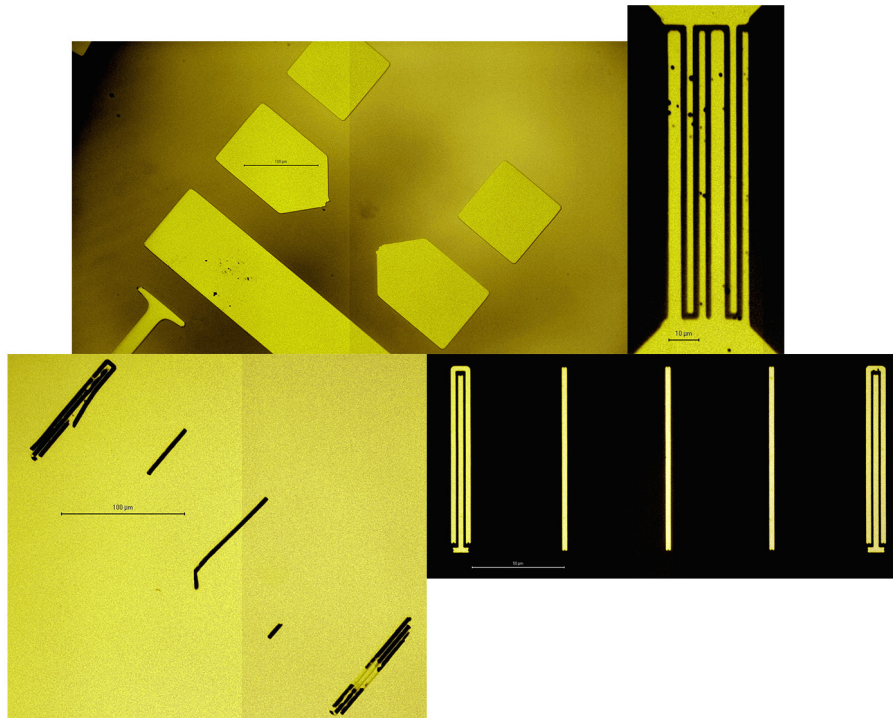
Figure 22: a) Most of the IDTs ended up completely removed b) This IDT turned out really well with proper gaps and finger line widths c) Almost all the reflectors were gone, and this one was the best group on both wafers except for d) This group of reflectors was one of the only parts of all chips to be on top of a region where there was no Al on the back, because it was on the edge were the tape was holding it. It turned out to be exceptionally good.

Testing the chips

The chips should be tested with a probe station to verify if the obtained signals (if there are any) correspond to the designed reflectors. It might be interesting to see the difference of the reflected pulse from a simple reflector or an IDT reflector. If it is very clear, it might be interesting to use only IDT reflectors which are suspected to send back pulses with higher amplitudes than simple reflectors.

All the different IDTs, orientations, lengths and apertures should be tested to evaluate which parameters can be changed while maintaining a proper signal, which will indicate what can be changed and what not.

Optimizing all the parameters and reducing size

Designing another mask with the help of all the data collected during the characterization should take place. Other sets of parameters can be tested, and the ones that worked from the 1st design can be pushed further in order to try and reduce the size of the SAW devices.
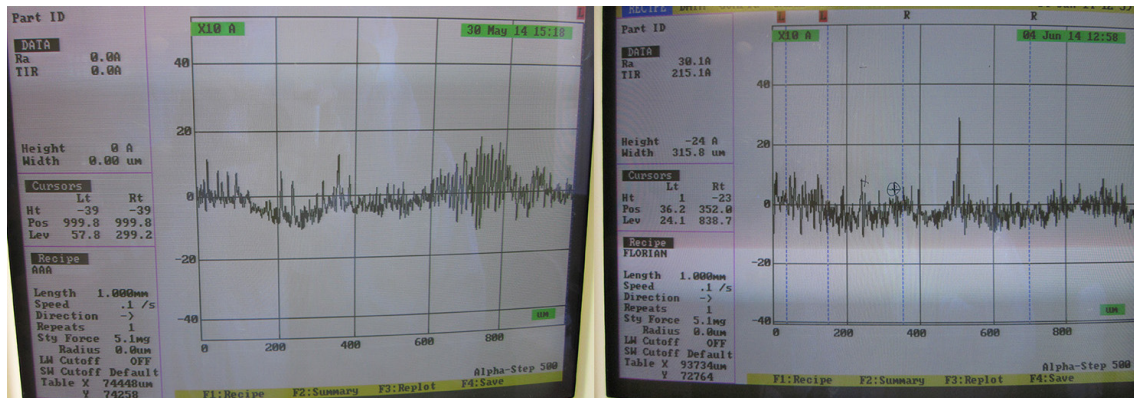
Figure 23: Profile of the chip before 3rd Gen. processing on the left, and the profile of a clean chip out of the box on the right.

Designing an antenna

The final step of the design of these devices is to design an antenna to allow wireless communication with the chips, which is the actual interesting way to use these SAW sensors, using the passive properties of it to allow them to be used in various environments.

Input from Victor Plessky suggested that the antennas were made to interact with the magnetic component of the RF waves instead of the electrical field. The standard antennas require more surface to intercept the waves which is a problem for miniaturization.

Ultra-thin $LiNbO_3$ chips

To further reduce the size of SAW devices, it would be interesting to use ultra thin Lithium Niobate chips, fabricated using the procedure shown in Fig. **??**. Only a few companies fabricate these around the world and are very expensive. The main principle is to implant Helium ions under the surface with a distance equal to the thickness of the chip wanted as shown in step 1. and 2.. In step 3., when heating the wafer, the helium ions break the wafer along a very fine surface, allowing this ultra thin chip to exist with a very good surface roughness. To keep this chip, the 1st wafer is bonded on another wafer before heating it up.

In step 4. the electrodes can be defined, a layer of Silicon oxide placed on top of them can be patterned to etch the release holes, and in the final step the structure can be made to hang by removing the thin layer of BCB that was put there before the wafer bonding.

It might be hard to work on both surfaces with these chips, since the top side is even more fragile than before. It can therefore be difficult to metallize the back of the chip if it is shown to clearly improve the structures.

E-Beam Lithography

To avoid most of the problems of the optical lithography which has been done in this project, it would be preferable to use E-Beam lithography, as it allows for very precise

structures and very high resolution structures. All of the reflectors and IDTs could be reduced in size. At CMi the feature size with this tool can reach below 10nm.

Since semester projects aren't very long, and the E-Beam being a very demanded machine, it was not possible to use it for this project, but it could be done for a master project.

VI. Conclusion

This project was for me the first occasion to work in the cleanrooms at EPFL and taught me how to work with multiple machines used extensively in MEMS fabrication.

The most important lesson I got from CMi is that it requires a lot of planning and dealing with many mistakes before getting interesting results. Many times, because of the recent formation, something would go wrong during the process, which then required me to book the machine and the others afterwards again a few days or a week later, slowing the fabrication drastically. This can become very frustrating and it was important for me to learn how to deal with failures without being able to correct them on the spot as I was used to for most of the projects I worked on during my studies.

In the end we were able to fabricate the SAW devices almost completely without having the time to characterize the chips. The results were interesting and definitely improved over time which was finally very interesting and kept us going. It was rather disappointing to not get as far as planned and prevented Kaitlin and I to split the project in 2 for each different device, which had us working together until the end of the project.

It is therefore pretty clear that the project was very ambitious for students without any prior knowledge of the cleanroom and no assistant supervising every step, but rather letting us experiment and fail alone to learn. As with most of the semester projects, the goal is to go as far as possible, usually without reaching an end.

Acknowledgements

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