Optimization of atomic layer deposition of aluminium oxide for suspended microchannel fabrication

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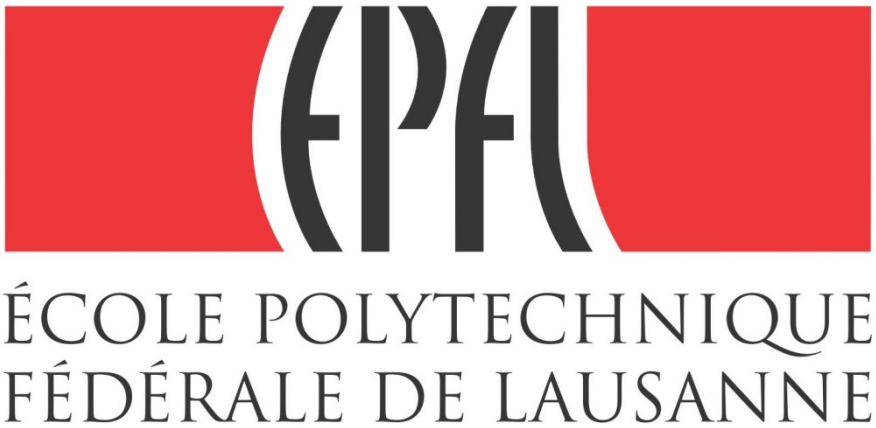

Abstract: This report presents the semester project of a Master student realised in the GR-LVT laboratory of the École Polytechnique Fédérale de Lausanne. The work was supervised by Prof. G. Villanueva and the PhD assistant A. De Pastina. The project consists in optimizing the process for suspended microchannels fabrication, based on the technology of atomic layer deposition of aluminium oxide.

Laboratory: GR-LVT

Professor: Guillermo Villanueva

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Table of Content

Introduction 2

1. Generalities 3

1.1. Motivation and applications 3

1.2. State of the Art 3

1.3. Atomic Layer Deposition of aluminium oxide 5

1.4. Process flow and fabrication 7

2. Results – design 1 9

2.1. Aluminium oxide vs parylene properties 9

2.2. First photolithography (mask 1); step 2 10

2.3. Al_2O_3 ALD – on design 1; step 3 11

2.3.1. Permeability tests 11

2.3.2. Tests to avoid cracks 12

i. Hard bake 12

ii. Al_2O_3 layer thickness 13

iii. ALD temperature 14

2.4. Second photolithography (mask 2); step 4 15

2.5. Al_2O_3 etching; step 5 15

2.6. SiN and Si etching by Bosch Process; step 6 16

2.7. Channels emptying; step 7 16

2.8. Parylene layer on Al_2O_3 19

3. Results – Design 2 20

3.1. Idea of a new design 20

3.2. First photolithography (mask 1) 20

3.3. Al_2O_3 ALD – on design 2 21

3.4. Second photolithography (mask 2) and etchings 22

3.5. Channel emptying 23

Conclusion and acknowledgements 25

Bibliography 26

Table of Figures and Tables 27

Appendix 28

- Runcard 28
- Process Flow 28

Introduction

This project is focused on atomic layer deposition of aluminium oxide to fabricate suspended microchannels. Few examples of the applications of such devices are blood analysis to detect cancerous cells or device cooling directly on the chip. The main objective is to simplify the current fabrication process implemented in GR-LVT group, which is complicated and long. In autumn 2015, a previous student worked on this project but used parylene as structural material for the microfluidic channels. The result was successful; however parylene is a very hydrophobic polymer and has bad mechanical properties. Aluminium oxide is a good alternative, as will be shown later. In this project, the deposition of aluminium oxide is based on ALD (atomic layer deposition) that gives very conform and uniform films.

First are presented motivations, state of the art, atomic layer deposition in detail and the process flow of the project. Then, results for the first and main design are presented in Part 2 in which a lot of tests were made to find solution to several problems occurred during the process. Finally, a new design was created to solve some problem and results are presented in Part 3.

This project was conducted in CMi cleanrooms at the EPFL and was supervised by A. De Pastina and Prof. Guillermo Villanueva from GR-LVT laboratory. It lasted from February 2016 until end of May 2016 and takes part in the Microengineering Master studies.

1. Generalities

1.1. Motivation and applications

This project focuses on the fabrication of suspended microchannels by atomic layer deposition of aluminium oxide. Suspended microchannel device allows analysing blood samples to detect especially cancerous cells. The concept is to measuring the frequency of a cantilever oscillator (1). The resonance frequency changes according to the properties of the environment around the oscillator, i.e. vacuum, air or liquid. In the case of immersion of the resonator into liquids, the friction between the liquid and the oscillator decreases by order of magnitudes the quality factor and worsens its mechanical performances.

A solution to reduce this friction, and thus to increase the quality factor, is to drive liquids into microchannels manufactured directly inside the cantilever oscillator. A cell passing inside this microchannel changes the mass and the stiffness of the cantilever, leading to a measurable frequency change.

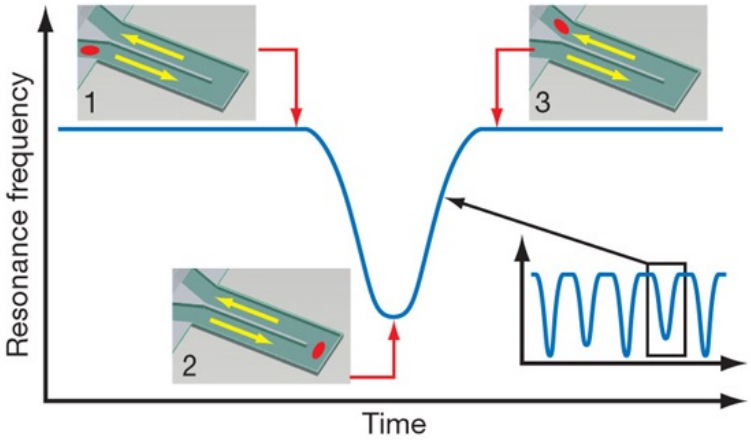


Figure 1: Change of cantilever frequency due to cell flowing **(1)**

Cancerous cells, bigger and softer than healthy cells, can be detected by this process.

Another application of this technology could be the cooling of electronic devices directly on the chip, by being able of placing microfluidic channels onto different substrates such as metals or PCBs. This is made possible thanks to a few steps and low thermal budget process flow that will be presented later in this report.

1.2. State of the Art

Atomic layer deposition (ALD) technique is widely used for fabrication of several emerging micro and nanodevices. Many oxides can be deposited by ALD, like Al_2O_3, ZrO_2, TiO_2, ZnO or Ru. Gate oxides are often grown by ALD to obtain very thin and uniform films. For example (2), high mobility FETs with high *k* material or non-volatile memory devices (Figure 2) can be manufactured. Few nanometer thick films with very good conformity allow an efficient tunnelling effect.

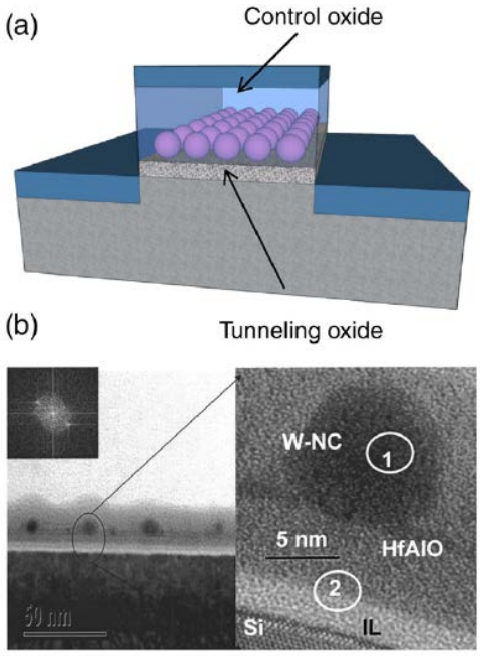


Figure 2: (a) Schematic drawing of nanocrystal (NC) memory and (b) cross sectional TEM images showing the HfAlO/W/HfAlO structure of nanocrystals (NC) embedded in HfAlO **(2)**

Another ALD application is the fabrication of nanotemplates with high aspect ratio nanoholes (2). A Si substrate is patterned by anodic aluminium oxide (AAO) and Ruthenium is deposited by ALD to fill the nanoholes. Then, the top layer and AAO are removed by dry etching and it's still only the Ru nanowires.

The Nanotechnology group of the IMTEK of Freiburg manufactured nanochannels based on ALD (3). They used TiO_2 ALD as structural material of the channels walls and used sub-100 nm dimensions for the photoresist pattern. Thus, there are several differences between those results and the current project.

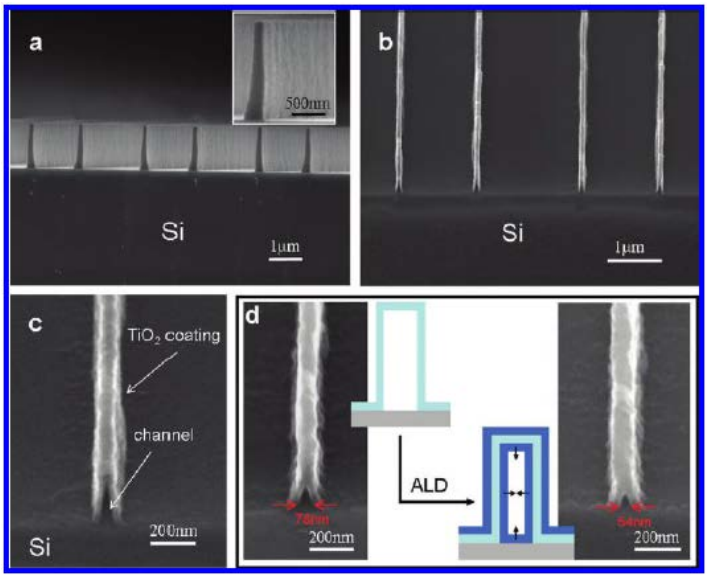


Figure 3: SEM images of (a) photoresist structures coated by a 35 nm ALD TiO_2 thin film, (b) a 45° tilted view of TiO_2 nanochannels, (c) a magnified view of b, and (d) a nanochannel before (left) and after (right) post-ALD deposition to scale down the channel dimensions **(3)**.

Khan and al. developed transparent microchannels (4). They used same dimensions as us and we have drawn inspiration a lot by this paper. The channel has 4x4 μm^2 cross section and the cantilever is 200µm length. However, to structure the microchannel walls, they deposited a 500nm layer thick of SRN (silicon-rich silicon nitride) by LPCVD. The deposition temperature isn't specified. The results which they obtained are very rewarding.

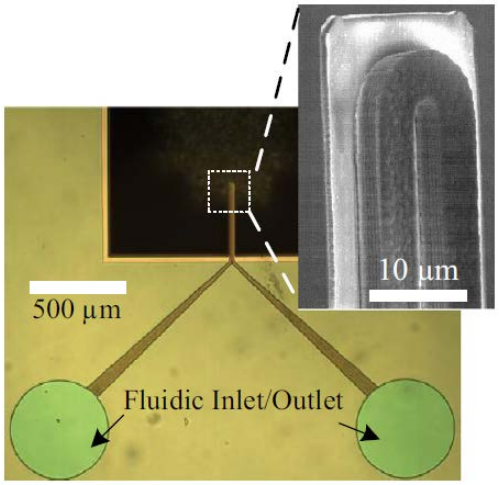


Figure 4: Released cantilever with fluidic inlet/outlet **(4)**

Finally, another Master student, A. Aupée, worked on the same project than me last semester (autumn 2015). However he tried to structure microchannel with parylene deposited by LPCVD (5). His project was successful, but due to the hydrophobicity and low stiffness of the parylene, that led to find a new material with better hydrophilic and mechanical properties. Aluminium oxide is a good candidate for several reasons (see chapter 2.1). So, I took over A. Aupée's process flow and adapted it for my project.

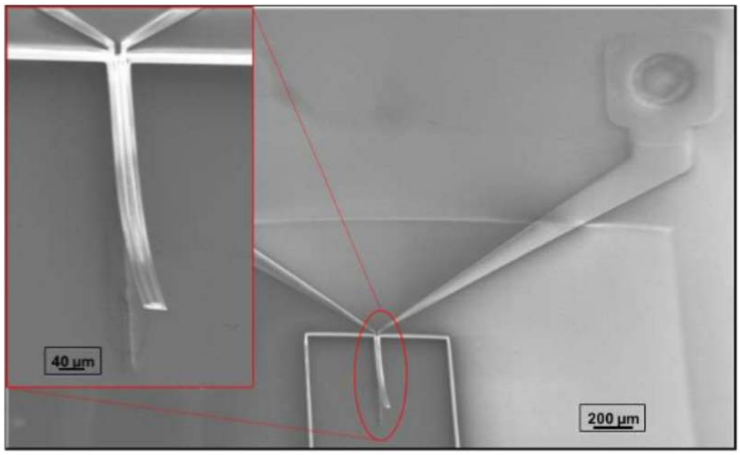


Figure 5: Microchannel manufactured with parylene - SEM picture – result of A. Aupée project **(5)**

1.3. Atomic Layer Deposition of aluminium oxide

Atomic layer deposition consists of deposition of a material, often an oxide, atomic layer by atomic layer. This technology allows to obtain very conformal and uniform thin films and can be also performed at low temperature. Due to the layer by layer process, only some hundred nanometers thick layers can be deposit. The majority of ALD reactions are made by two different gases, called precursors, and brought one after each other in the reactor. Let's focus on the Al_2O_3 ALD reaction.

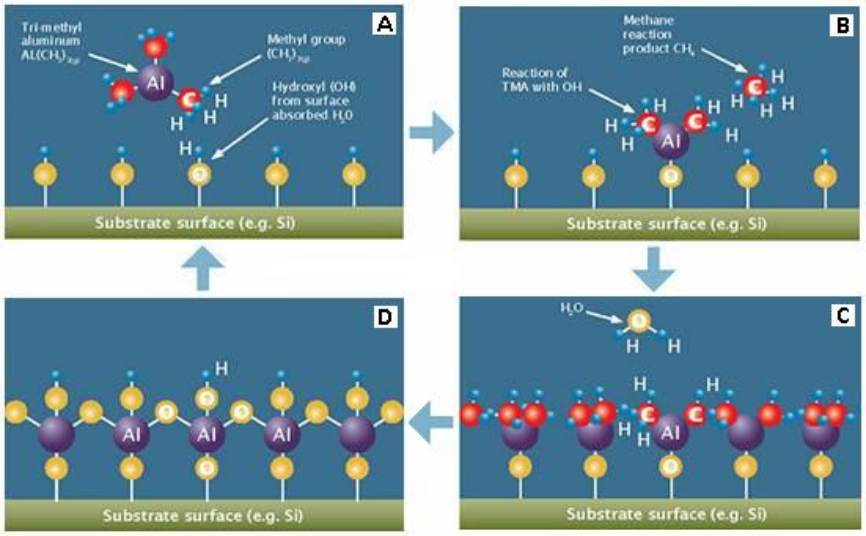


Figure 6: aluminium oxide ALD cycle in four steps **(6)**

Precursors used to growth Al_2O_3 films are H_2O and $Al(CH_3)_3$, trimethylaluminum (TMA). One cycle, which means one atomic layer thick, includes two reactions A and B and two nitrogen purges (7). First, the TMA is injected in the reactor and reacts with the native hydroxyl layer presents on the silicon substrate. Bimethylaluminium, bound to oxygen, and methane are produced. One nitrogen N_2 purge is done to eliminate TMA and methane excesses. For the reaction B, H_2O is injected, reacts with the bimethyaluminium and produces also methane. Finally, a last N_2 purge is done and the same initial hydroxyl surface is obtained.

$$OH^* + Al(CH_3)_3 \overset{A}{\Rightarrow} O - Al(CH_3)_2^* + CH_4$$
$$Al(CH_3)_2^* + H_2O \overset{B}{\Rightarrow} O - Al - OH^* + CH_4$$

The star notation represents the surface chemical compound and the indents, the bonds between molecules layers. As we can observe, at the end of reaction B we obtain the same surface as before reaction A and a new cycle can start. With the CMi's ALD machine, one cycle for aluminium oxide takes 3-4 seconds.

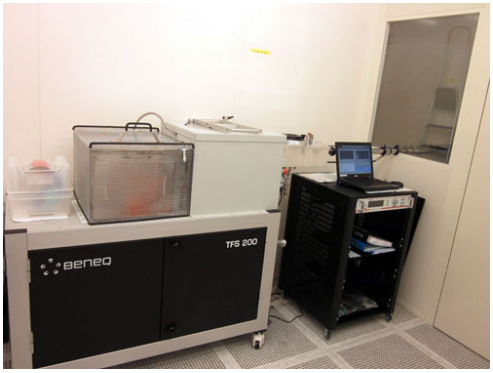


Figure 7: CMi's machine for ALD; BENEQ TFS200 **(8)**

1.4. Process flow and fabrication

As a reminder, we aim to manufacture microchannels on the top of a beam resonator. Ideally, this microchannel has to be transparent to see if the resist, used as sacrificial pattern layer, is removed at the end of the process and too allow visual inspection during experiments. Furthermore, we need material with a high elastic (or Young) modulus to obtain a high quality factor. As stated in the State of the Art (chapter 1.2), we have drawn inspiration from Khan and al. design (4). The process flow includes eighth different steps. It will be detailed below:

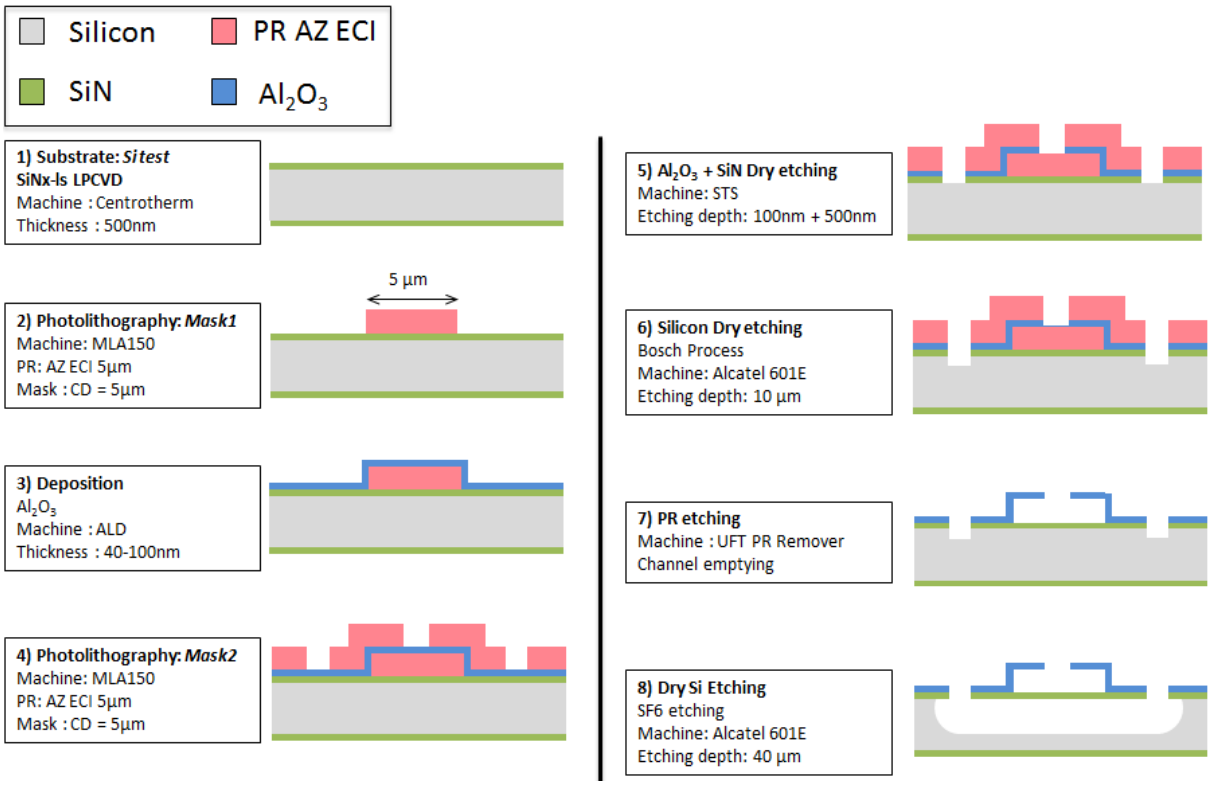


Figure 8: process flow of the project. Height steps have to be achieved. Two photolithographies, one deposition by ALD and several etchings to open the inlet/outlet and to remove the resist.

Step 1: 500nm thick low stress SiN layer is deposited by LPCVD. Silicon nitride is a biocompatible, transparent material and has a high elastic modulus of 260 GPa (9) which is bigger than silicon (170 GPa).

Step 2: the photoresist defined by the first photolithography is used as sacrificial layer. The microchannels have 5x5 μm^2 cross section and 500µm length. As we can observe in Figure 9, photoresist is kept all around the microchannels for an important reason: later in the project, we want to contact the actual microfluidic chip with a PDMS micropump device placed above which is used to lead fluidic samples inside our microchannel. However, the pressure applied on the chip to promote the PDMS bonding could be too strong and could break the channels. So this “security” resist supports part of the pressure and prevents channels from breaking or collapse.

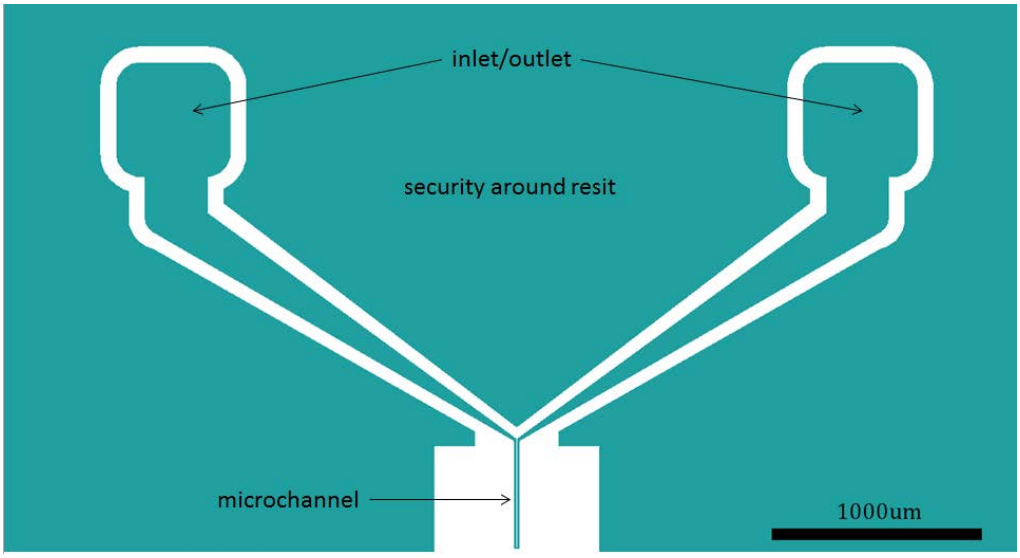


Figure 9: Mask 1 with inlet/outlet (to be opened with the next lithography), microchannel and security resist. Resist is green parts and SiN white ones

Step 3: we deposit a thin Al_2O_3 layer by ALD on the entire substrate. This aluminium oxide will define the microchannel walls.

Step 4: the second photolithography is made. It defines the inlet/outlet apertures and the cantilever releasing area. It especially protects the microchannel from the future etchings.

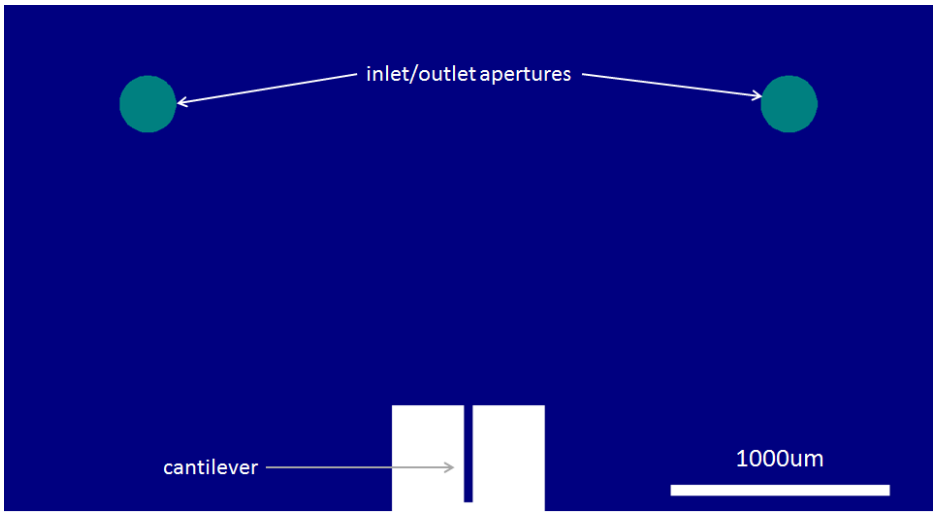


Figure 10: Mask 2 with inlet/outlet apertures and cantilever shape. Green parts are the resist of 1st photolithography, white part is SiN and blue part is the resist of the 2nd photolithography. Al_2O_3 is transparent but cover the entire wafer.

Step 5: Al_2O_3 and SiN are etched to open the inlet/outlet and the releasing area.

Step 6: the silicon substrate is etched by Bosch Process for 10µm depth. Because the 8th and last step is an isotropic etching, if it starts too close to the surface, it can etch the SiN layer of the cantilever and break the channel.

Step 7: During this phase, we remove the entire second resist layer (in blue on Figure 10) and the resist which is inside the channel by the inlet/outlet apertures

Step 8: Now the channel is empty, we can release the cantilever by dry Si isotropic etching with SF_6 chemistry.

2. Results – design 1

2.1. Aluminium oxide vs parylene properties

As mentioned in the State of the Art, in autumn 2015, A. Aupée realized same project but with parylene. At the end of his project, he concluded that big hydrophobicity of the parylene could be problematic to deliver liquid samples inside the channel. This would require applying big pressure and may break the channels. Instead, aluminium oxide is hydrophilic and liquids would be flowing in the device by capillarity forces. A very low pressure would be needed to maintain a constant flow. Below are presented the graphs of contact angle versus time (in days) of Al_2O_3 and parylene.

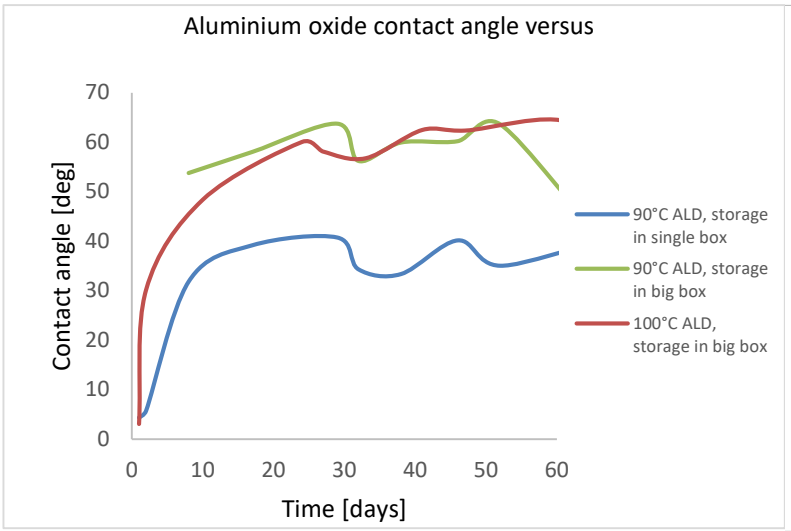


Figure 12: Al_2O_3 contact angle versus time. The contact angle could be low due to impurities on the wafer. With a washed wafer, we obtain a contact angle of about 40°. Al_2O_3 is hydrophilic

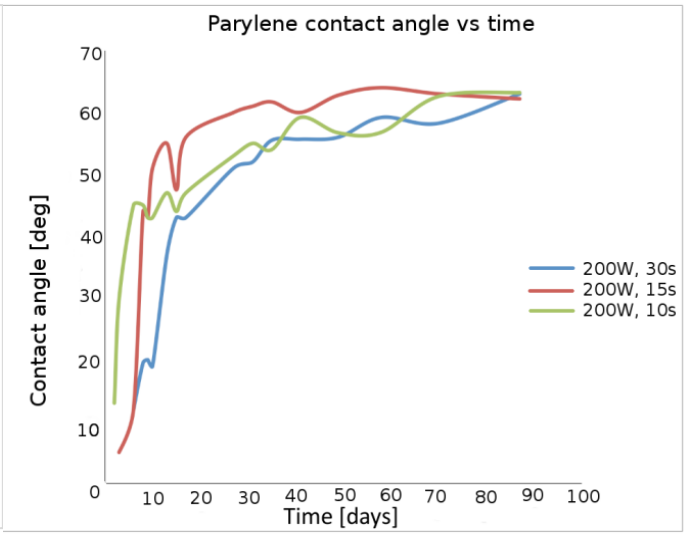


Figure 11: parylene contact angle versus time **(14)**. The contact angle doesn't excess 65°. Parylene is hydrophobic

The parylene contact angle graph was given by CMi staff. We can observe that the contact angle is larger than 60°, I personally measured an angle of 89,6° for a 2µm layer thick. Literature (10) indicates contact angles from 79° up to 97° according to parylene type (N, C or D).

Concerning aluminium oxide, I deposited a 100nm layer thick on three different silicon test wafers. Two depositions were made at 90°C and one at 100°C. Then, one 90°C wafer was stocked alone in a single box (blue curve in Figure 12) and two others in a big box with several other wafers. After each measurement, I washed wafers with deionized water to clean them. We can observe that wafers stocked in big box have bigger contact angle than one in the small box. We can conclude that the storage has an influence on the surface energy: we could suppose that, in the big box, the Al_2O_3 surface could be contaminated by dust and wastes from other wafers, also because the box is often opened.

D. Zhang and al. demonstrated clearly that cleaning method before the measurement influences a lot the contact angle results (11). For example, by cleaning with deionized water, they obtained a contact angle of water on Al_2O_3 of 40°(±2°). This corresponds to our results after wafer rinsing in DI water, just before contact angle measurement.

Al_2O_3 has a Young modulus of 345 GPa (12) and parylene from 2.4 GPa until 3.2 GPa depending of the parylene type (10), which is about one hundred times less. So aluminium oxide mechanical properties are potentially better and this material allows for higher quality factors. However, cells have lower Young modulus compared to aluminium oxide. Cell stiffness changes the overall resonator stiffness when they flow through the

channel. In order to be sensitive to this stiffness change, we have to make very thin channel walls, to avoid the aluminium oxide stiffness to be too much dominant.

2.2. First photolithography (mask 1); step 2

We begin with a wafer already coated by a 500nm thick low stress SiN layer (step 1 of the process flow) that is given by my PhD assistant. For the first photolithography, illustrated on Figure 9, we first took parameters that A. Aupée used, that were 400 $mJ \cdot cm^{-2}$ for the dose and *-2* for the defocus. However, this dose was too high and the resist was overexposed. So we performed a dose test to know which parameters would be the best. For doses at 400, 300 and 200 $mJ \cdot cm^{-2}$ the channel reference width is 10µm and for doses at 170 and 150 $mJ \cdot cm^{-2}$, the reference is 5µm wide. The defocus is *-2*.

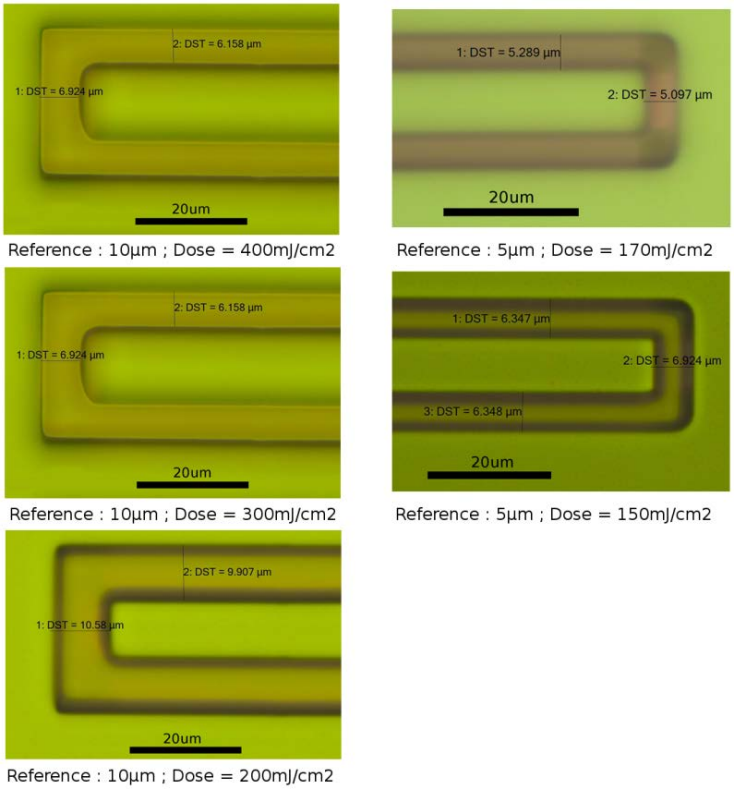


Figure 13: dose test for the 1st photolithography, defocus = *-2*. We conclude that a dose of 170 $\mathbf{mJ \cdot cm^{-2}}$ is ideal.

Dose of 150 $mJ \cdot cm^{-2}$ gives underexposed result and 300 and 400 $mJ \cdot cm^{-2}$ are overexposed. Doses of 200 and 170 $mJ \cdot cm^{-2}$ are quite optimal, so we selected 170 $mJ \cdot cm^{-2}$ for the next experiments. Finally, it's important to notice that during the semester the CMi staff made corrections on the photolithography machine (MLA150) and we adapted the defocus by consequence. From now on, we take **defocus = *-7***.

2.3. Al_2O_3 ALD – on design 1; step 3

After this first photolithography, we did ALD tests. Because of thermal drift of the ALD machine, it was impossible to deposit at 80°C (really bad surface result), so we start with 100nm Al_2O_3 deposition at 90°C (step 3 of the process flow). We observed that cracks appeared on the resist areas (green parts on Figure 14). Apparently, cracks propagate only on big parts and start from edges (see Figure 15). They don't appear in parts smaller than 150µm, so the channel isn't broken.

So we have to answer to questions: first, what is cracking? Photoresist or aluminium oxide? And is the channel still impermeable to solvent (chapter 2.3.1)? Secondly, which are the solutions to solve this problem (chapter 2.3.2)?

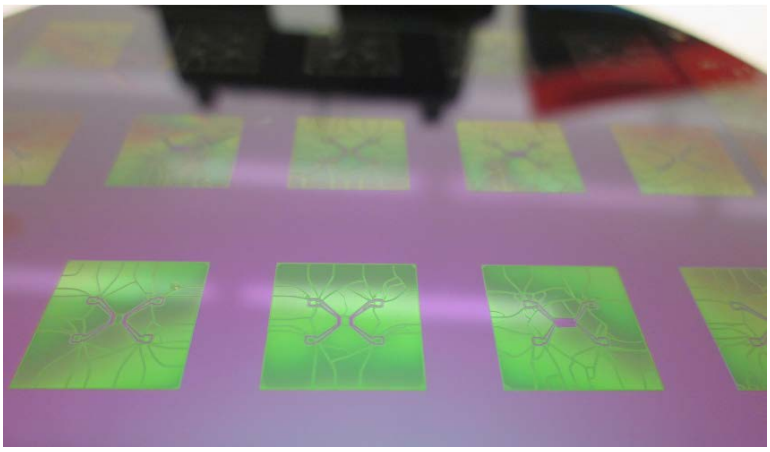


Figure 14: cracks appeared after 100nm Al_2O_3 ALD. We don't know if aluminium oxide or resist has cracked and we must to determine that by tests

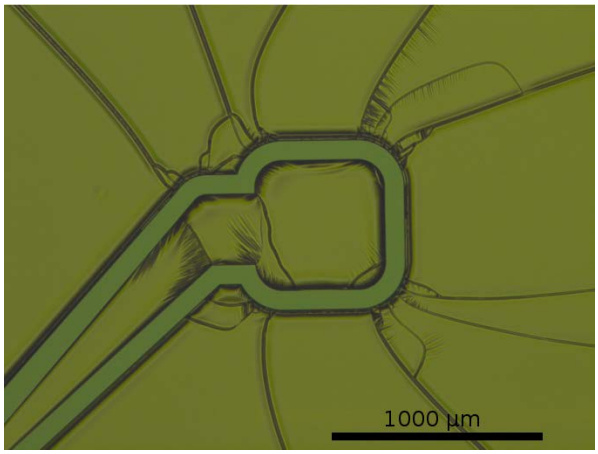


Figure 15: cracks in the inlet/outlet

2.3.1. Permeability tests

So we cleaved the wafer in two parts and made solvent test to see if the resist would be removed. A. Aupée used UFT 1165 solvent for his project, so we kept the same. We dip one part for 2min and the other for 10min. We can draw several conclusions. First, we observe that cracks disappear and Al_2O_3 is delaminated: so it means that cracks were in the aluminium oxide layer and not in the resist. Chips dip for 10min in the solvent are cleaner than ones dip for 2min only, because residues are removed more efficiently. Secondly, the resist isn't removed, so it means that there is still a thin intact layer of aluminium oxide that protects the resist below.

However, we don't know how thick is the delaminated aluminium oxide and how it could weaken the channel walls. So we have to find a way to avoid those cracks in the top Al_2O_3 layer. We can assume that resist expands during the ALD at 90°C and introduces too much stress in the aluminium oxide layer. So we can work either on the resist either on the atomic layer deposition parameters.

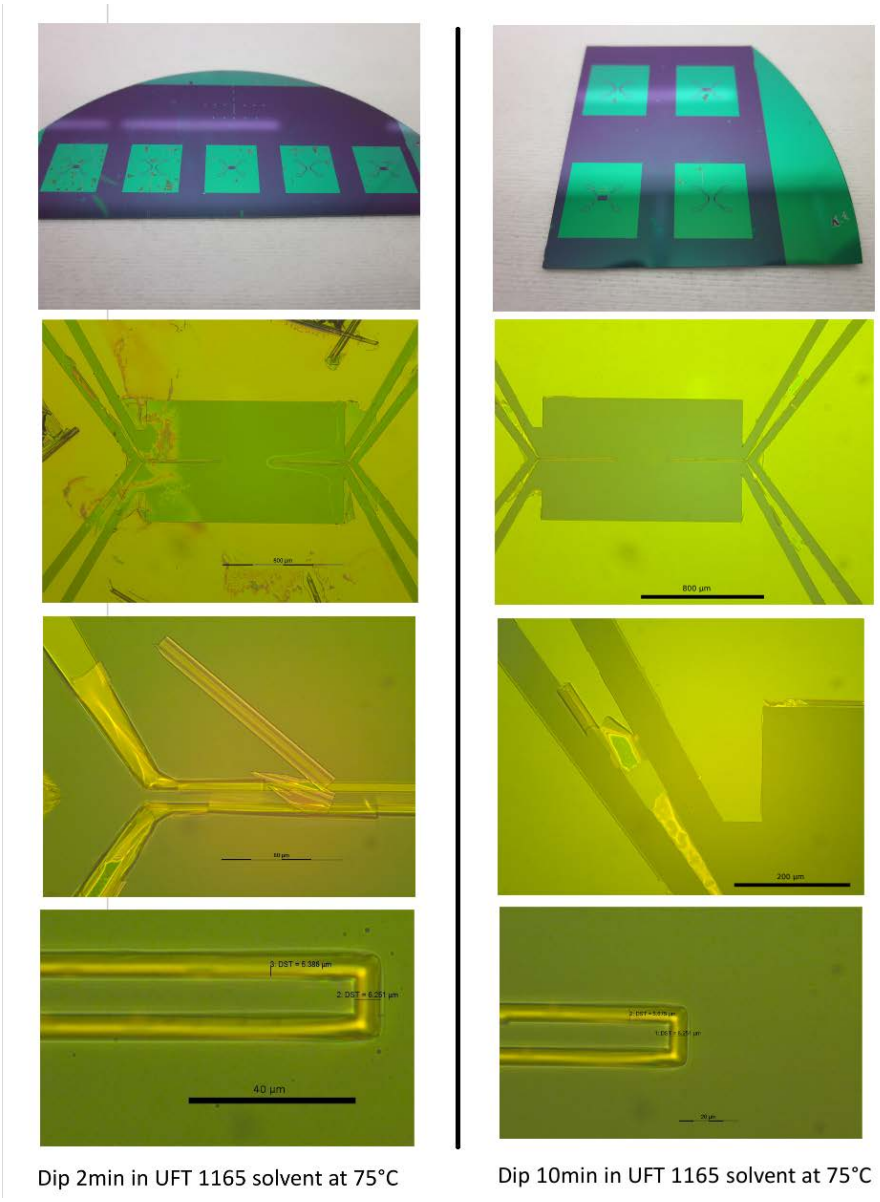


Figure 16: permeability test, chip dip in solvent. Aluminium oxide is delaminated and the channel is broken. We must determine if the solvent has an influence on the aluminium oxide or if this result is due to the cracks showed below.

2.3.2. Tests to avoid cracks

i. Hard bake

We worked first on the baking of the photoresist to make it stronger and avoid expansion during the ALD. After the resist development, we baked two wafers, one at 120°C and the other at 150°C for 30min. Then we deposited 100nm of Al2O3 at 90°C as previously and observed if cracks appear again. Colours of Figure 17 and Figure 18 were inverted to see better the cracks.

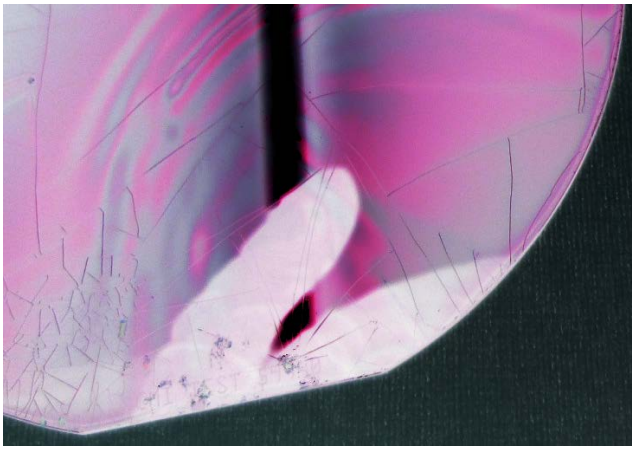


Figure 17: 100nm Al2O3, hard bake at 120°C. Cracks appear again.

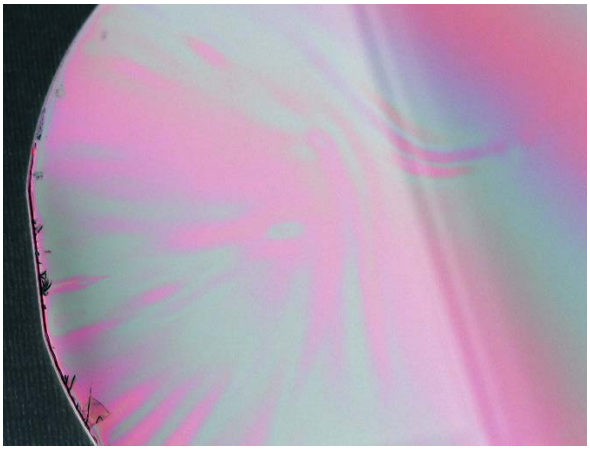


Figure 18: 100nm Al2O3, hard bake at 150°C. Cracks are remained because the resist is stronger and doesn't expand during the ALD.

We can clearly see cracks on the 120°C baked wafer, while no crack is visible on the 150°C baked one. So we can conclude that hard bake of the photoresist could be necessary to prevent the cracks occurrence. Now we have to determine if ALD parameters have also a role.

ii. Al_2O_3 layer thickness

We have drawn inspiration from Zacharias and al. mentioned in the State of the Art (3). They used 40nm of TiO_2 to manufacture channel walls, so we tried the same but with aluminium oxide. We vary here two parameters: baked or unbaked resist and 40nm or 100nm Al_2O_3 thick (Table 1). The ALD is made at 90°C.

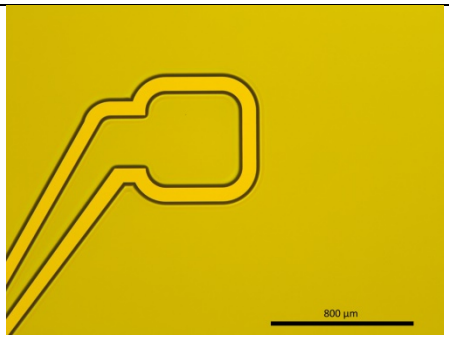
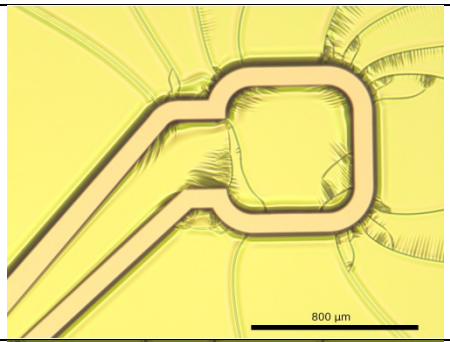
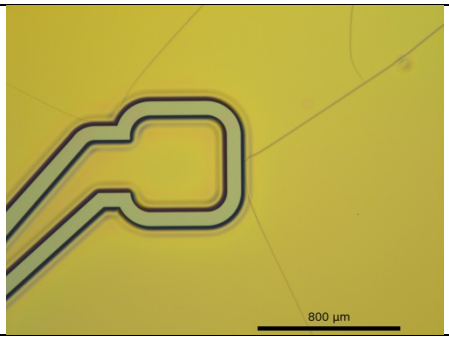
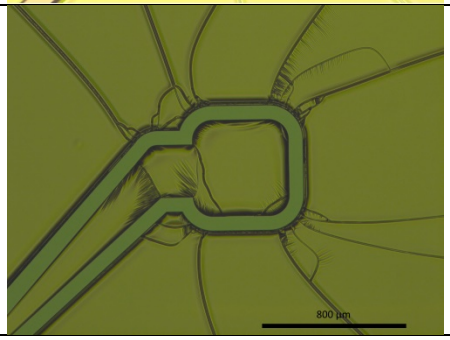
	Hard baked resist at 150°C	**Non baked resist**
40nm of Al_2O_3		
100nm of Al_2O_3		

Table 1: Al_2O_3 thickness versus resist hard bake. Best result with no crack is one with a hard bake at 150°C and an aluminium oxide thickness of 40nm.

Obviously on these pictures, we understand that bake the resist is necessary. Without it, cracks appear again and the aluminium oxide layer could delaminate later. However, even with hard bake resist, the 100nm thick aluminium oxide layer still contains some imperfections. To understand this, stresses introduced by different thicknesses of aluminium oxide layers were also measured and are presented in Table 2. The

measurements are made according to two wafer orientations: 0° and 90° and with an unbaked resist on simple silicon test wafers. We observe that internal constraints are twice bigger for layer of 100nm thick compared to 40nm. This can explain the occurrence of cracks in the 100nm layer, even with hard baked resist.

	0° (orientation 1)	**90° (orientation 2)**
40nm of Al_2O_3	88 MPa	123 MPa
100nm of Al_2O_3	257 MPa	251 MPa

Table 2: tensile stresses introduced by aluminium oxide layers

iii. ALD temperature

The last parameters to be tested are ALD temperature and solvents used. Until now, we did the deposition at 90°C by default, but in Zacharias paper (3), they deposit TiO_2 at 115°C, so we tried it with 40nm and 100nm layer thick. Obviously, we used hard baked resist at 150°C for 30min to prevent cracks. After deposition, we wanted to know if aluminium oxide is still delaminated by solvents, so we dip chips in four different that are UFT 1165, Technistrip, SVC and acetone.

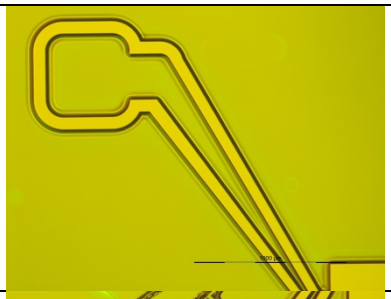
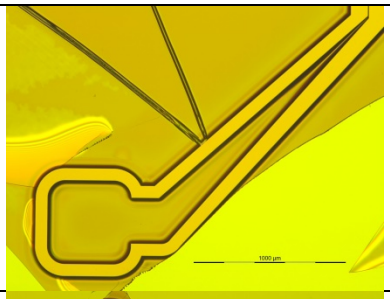
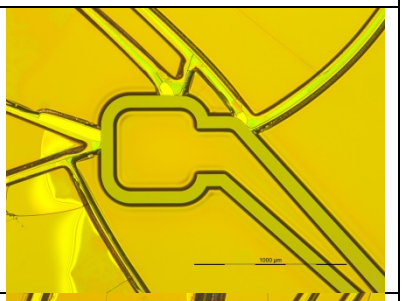
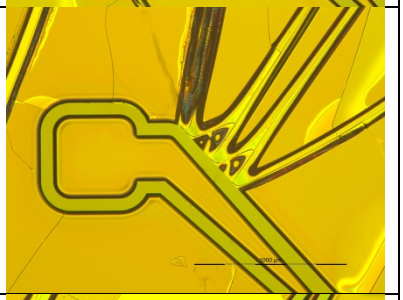
	40nm of Al_2O_3 ; ALD at 90°C	**40nm of Al_2O_3 ; ALD at 115°C**	**100nm of Al_2O_3 ; ALD at 115°C**
UFT 1165			
Technistrip			
SVC			
Acetone			

Table 3: chips dip for 1min in different solvents versus ALD temperature and layer thickness

We saw previously that the deposition of a 100nm thick aluminium oxide layer causes cracks, even with a baked resist. So, it isn't a surprise to notice that 100 nm Al_2O_3 delaminates in every solvent. 40nm layer thick seems to be a good option. However, ALD temperature plays also a role, because if we made it at 115°C, we see that every chip is also destroyed, while at 90°C and with UFT 1165 solvent, the surface is still intact. So, from now, we always select following parameters: **hard baked resist at 150°C for 30min, 40nm layer thick and ALD made at 90°C**. Like that, we prevent cracks and aluminium oxide delamination in solvents.

2.4. Second photolithography (mask 2); step 4

The design for the second photolithography is shown in Figure 10. We define here the inlet/outlet apertures and the cantilevers. Because of the presence of aluminium oxide on top of resist, compared to the first photolithography parameters, we increase the doses from 170 up to 200 $mJ \cdot cm^{-2}$, keeping the same defocus equal to -7.

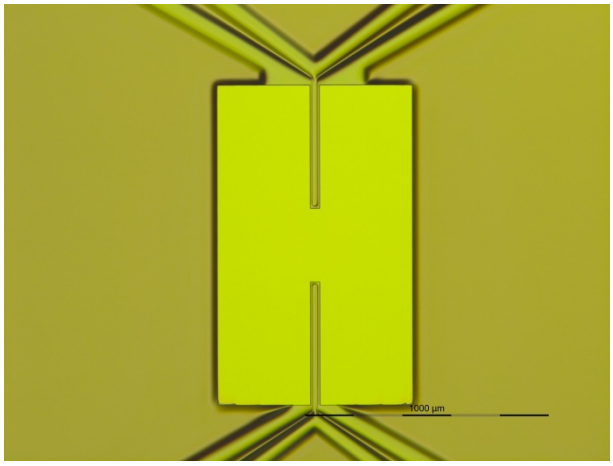


Figure 19: releasing area of the cantilever, yellow is low stress SiN

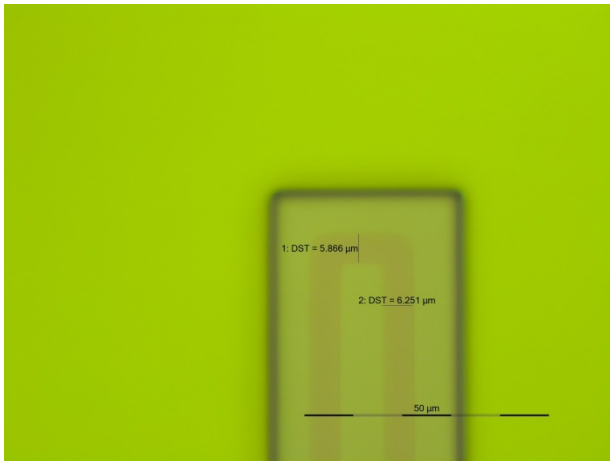


Figure 20: end of the cantilever with the microchannel

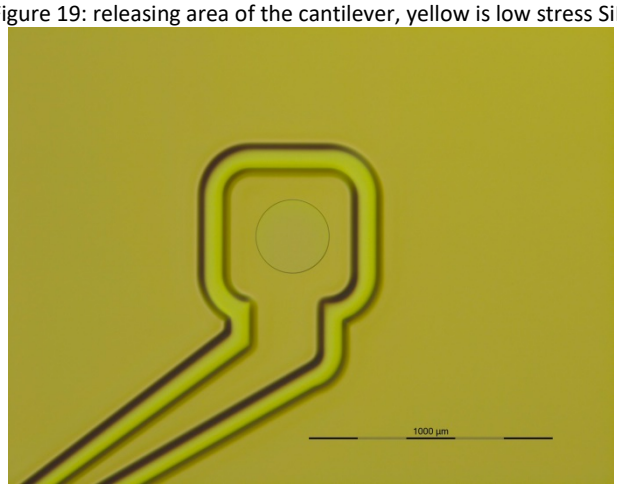


Figure 21: inlet/outlet aperture with 1st resist below

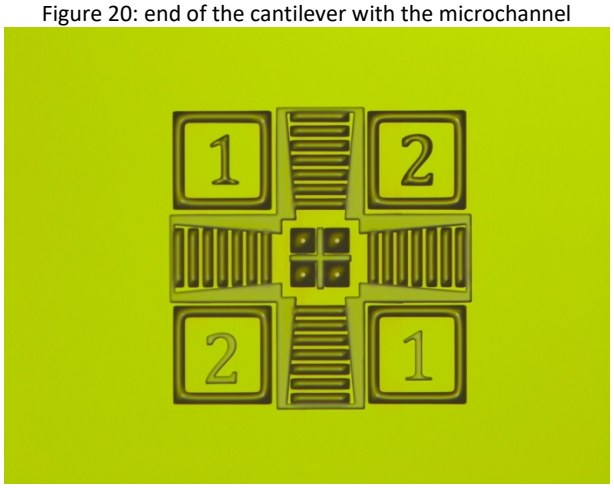


Figure 22: alignment cross after 2nd photolithography

2.5. Al_2O_3 etching; step 5

Now, we have to open aluminium oxide layer to reach first resist in the channel and SiN in the central releasing area. The channel is completely protected by the second resist and will not be etch during next steps. Here, we did a dry etching based on Cl_2, BCl_3 and Ar chemistry. The etch rate of aluminium oxide is 50nm/min (13) and I measured a rate of 200nm/min for the resist. Because we have 40nm of Al_2O_3, we decided to etch for **1min**. The recipe is called **"saphir"** and the etching has been performed at the STS Multiplex ICP in CMI. Eventual overetching would not be a problem because we have resist and SiN below, that we want to remove later. In Figure 23, orange area is SiN layer and brown is resist.

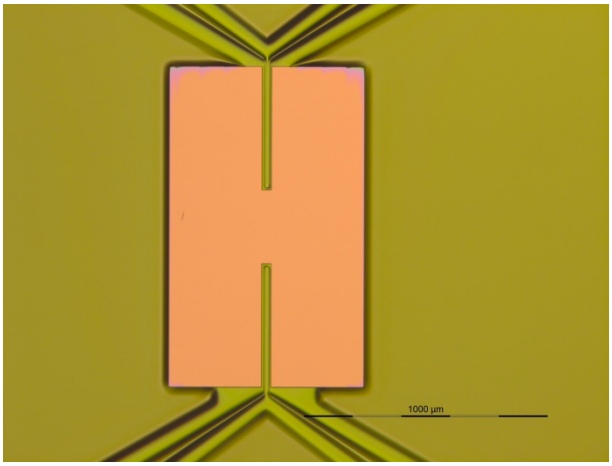


Figure 23: releasing area after Al_2O_3 etching

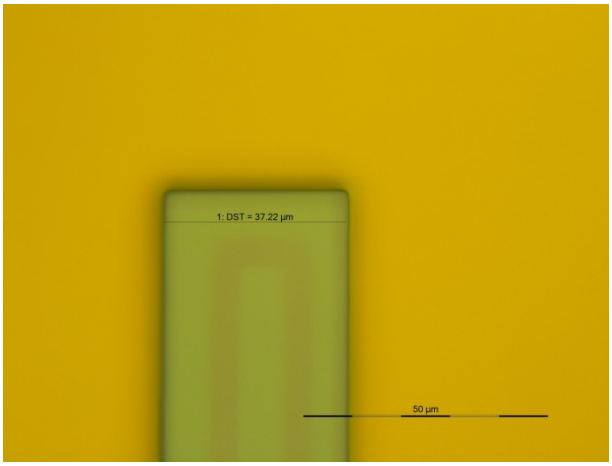


Figure 24: cantilever with channel after Al2O3 etching

2.6. SiN and Si etching by Bosch Process; step 6

Now the aluminium oxide is removed from the releasing area, we have to etch SiN and silicon substrate for a depth of 10µm with the Alcatel601 machine. The first recipe is called **"Nitrure_1"** and is running for **2min**. The second etching is made by Bosch Process and the recipe is called **"ANISO-ADP"** and is running for **3min**. As previously, the channel is protected by the second resist layer. These etchings slowly attack also resist inside the inlet/outlet aperture, but we remove it anyway in the next step.

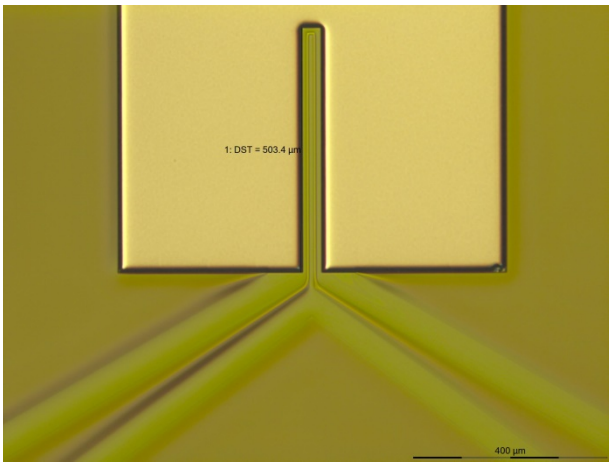


Figure 25: cantilever after Bosch Process

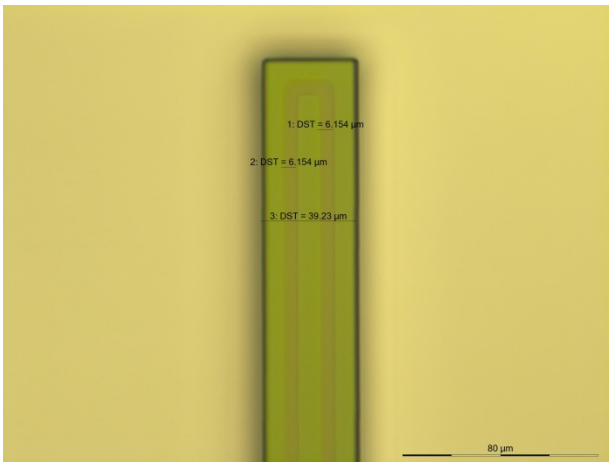


Figure 26: cantilever with channel after Bosch Process

2.7. Channels emptying; step 7

Now etchings are achieved and apertures are open, we have to remove resist from the channel (1st photolithography) and the top layer of resist that protected the cantilever from etchings. To reach that, we dip chips in different solvents for 3min as previously in chapter 2.3.2.iii to know which the best is. We focus mainly on the inlet/outlet because the resist should be removed first here.

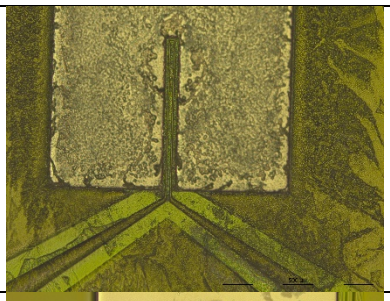
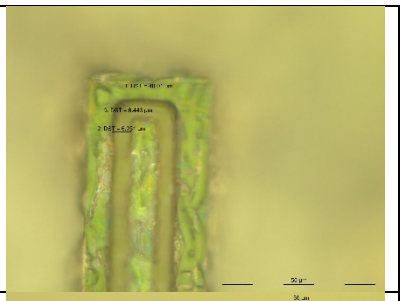
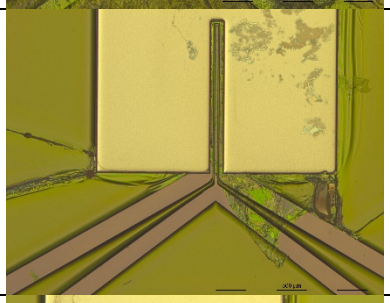
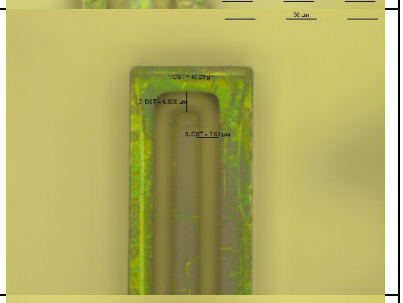
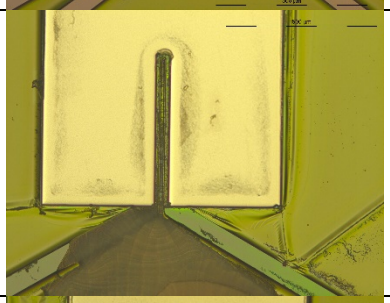
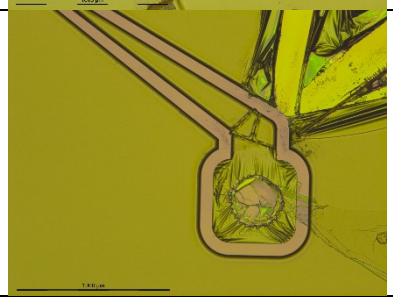
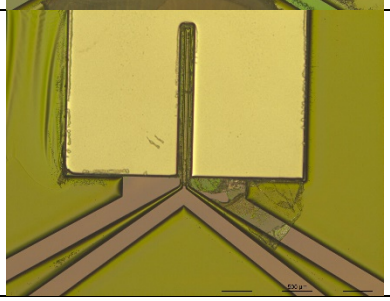
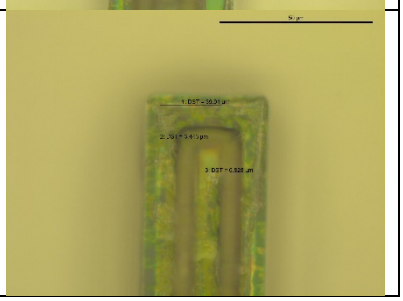
UFT 1165			
Technistrip			
SVC			
Acetone			

Table 4: solvent tests to empty the channel

As we can observe in Table 4, SVC and acetone destroyed the chip and aren't efficient. Technistrip doesn't affect too much the surface and create few cracks, but it doesn't remove resist efficiently. Concerning UFT 1165, we clearly see that result is really bad. That can be explained because the top layer of resist was burned by successive dry etchings and made it very hard. Apart from this dirty surface, the chip doesn't seem to be damaged below. Finally we decided to continue experiment with UFT 1165, because A. Aupée also tried solvent tests and concluded that one is the most efficient.

To strip well this burned resist, we do an O_2 plasma for 30 seconds before dipping the chip in the UFT 1165. We also vary the solvent temperature and the dipping time to optimize the process. We always focus on the inlet/outlet that's where we could have problems.

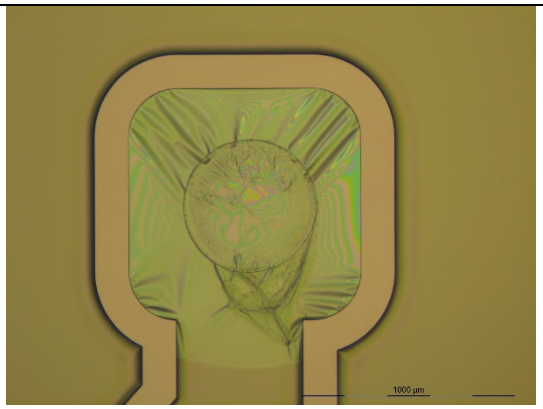
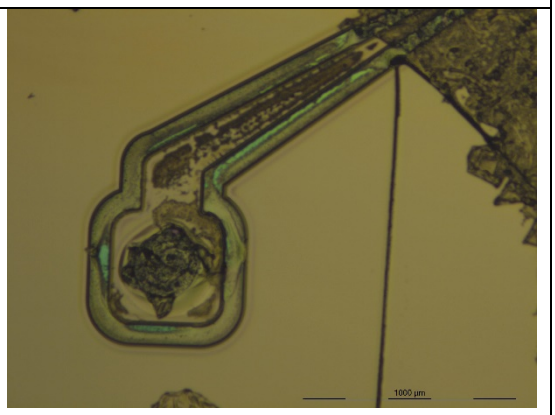
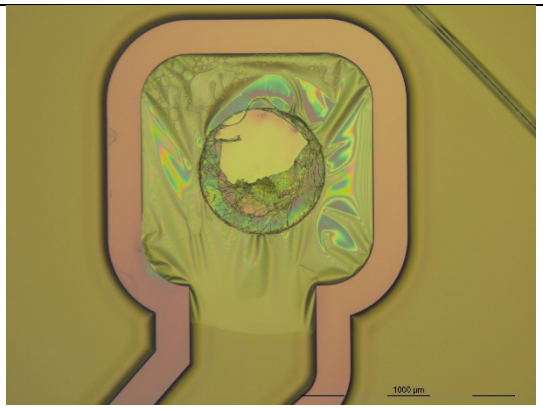
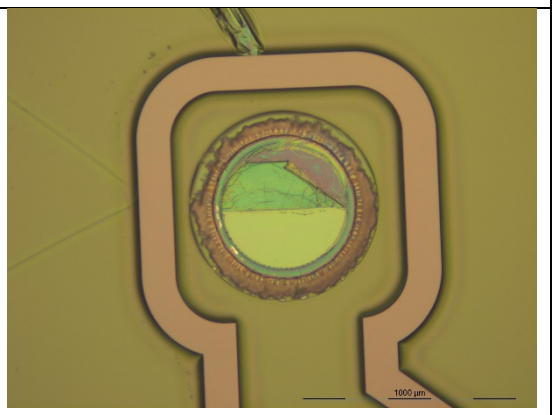
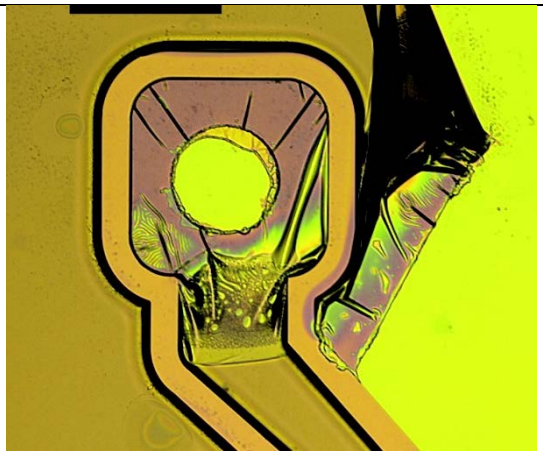
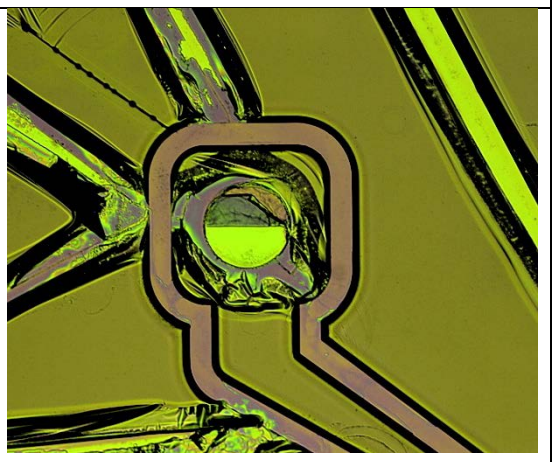
	UFT 1165 - High temperature (60°C)	**UFT 1165 - Room temperature**
Without O_2 plasma, dip for 3min in UFT 1165		
O_2 plasma for 30s, dip for 3min in UFT 1165		
O_2 plasma for 30s, dip for 8min in UFT 1165		

Table 5: O_2 plasma and solvent tests versus temperature

We observe that results are really better at high temperature, because the burned top resist is removed and because the channel resist is dissolved faster than room temperature. We see the resist inside the aperture is totally removed after 8min, probably because of the O_2 plasma attacked it. Unfortunately, cracks and delamination appears again. Furthermore, the Al_2O_3 layer collapses in the inlet/outlet, maybe because it's too thin and too weak. So we decided to add a 2µm parylene layer thick above aluminium oxide layer to strengthen it and prevent delamination. A. Aupée achieved his project successfully with parylene, so we hoped that it could work for this project.

2.8. Parylene layer on Al_2O_3

After ALD of aluminium oxide, CMi staff deposited 2µm of parylene and I performed the second photolithography. Before aluminium oxide etching, we have to etch parylene first with the SPTS machine. The recipe is called **"Polymide – Pi_vertical"** and is running for **1,5min**. Then, we achieve Al_2O_3, SiN and Si etchings as described in previous chapters (2.5 and 2.6). Finally, O_2 plasma is done to remove the burned resist. This time, we tried to dip chips longer in solvent to be sure that resist in the channel will be remove.

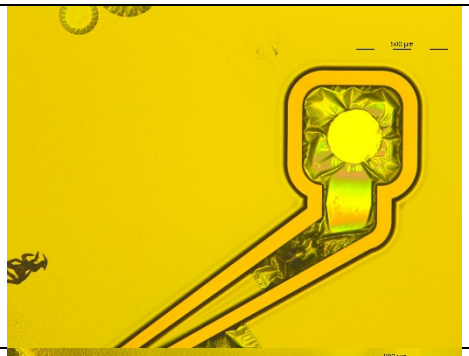
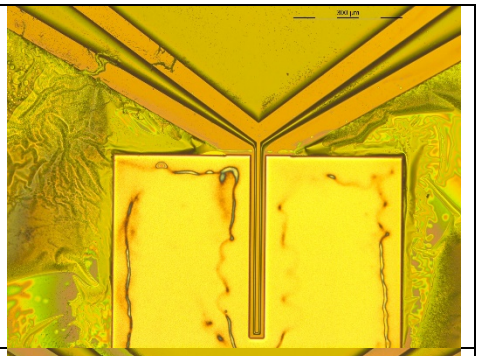
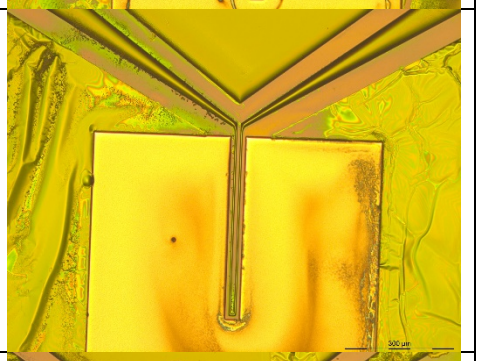
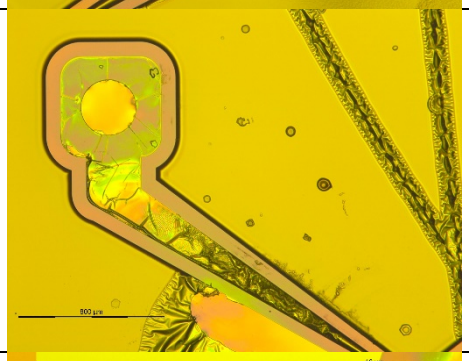
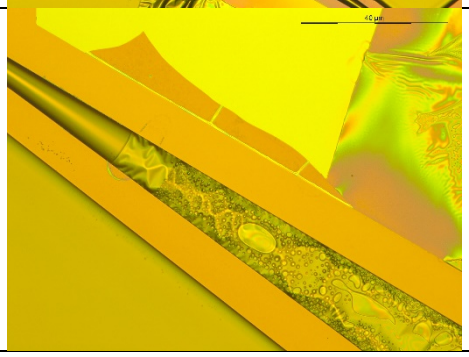
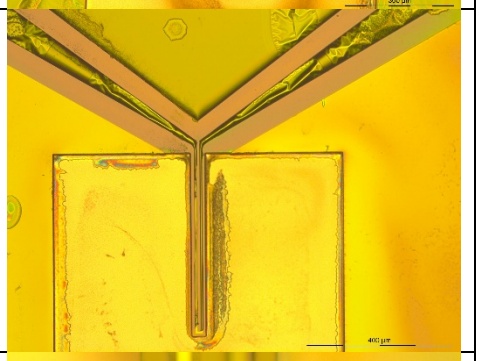
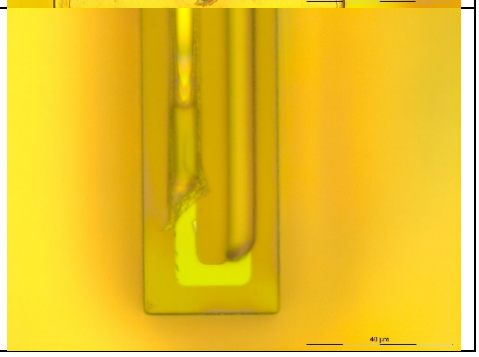
Dip in UFT 1165 for 30min at room temperature		
Dip in UFT 1165 for 30min at 60°C		
Dip in UFT 1165 for 12h at room temperature	 	 

Table 6: solvent test with parylene layer on top of Al2O3 layer

We can't see it on these pictures, but the parylene layer detached from the chip because of temperature or solvent. We observe that 30min dipping are not enough to remove this baked resist. Even after one night, it's still there and the channel is damaged. So apparently, we really need to not bake the resist inside the channel to remove it, but if we do that, cracks appears. One solution is developed in next chapter.

3. Results – Design 2

3.1. Idea of a new design

We've clearly seen above it's very difficult to remove the hard bake resist which is inside the channel. So we have to avoid this baking step and avoid cracks occurrence after ALD. We observed that those cracks appears in parts bigger than 150µm. So we decided to change the design by reducing every dimensions below this critical size. The inlet/outlet is also modified: we made a circular resist wall around the aperture to prevent liquid flood outside on the chip when we will insert some samples in the channel with the PDMS micropump device.

Secondly, the security resist, that avoids the channel breaking when applying pressure, was patterned in many single circles. Like that, we keep a large surface that absorbs pressure and we have structures smaller than 150µm in which, according to our hypothesis, no crack is supposed to appear.

3.2. First photolithography (mask 1)

As mentioned above, the design of the inlet/outlet and the security area was modified, while the channel didn't change. The new inlet/outlet size is 140 µm in diameter and the patterned circles, 100µm. We clearly see the around wall which avoids fluid flood when the PDMS micropump will be put on our chip. The dose is always 170 $mJ \cdot cm^{-2}$ and defocus equal to -7. The resist isn't baked to facilitate the stripping. So we hope that cracks will not appear with this new design.

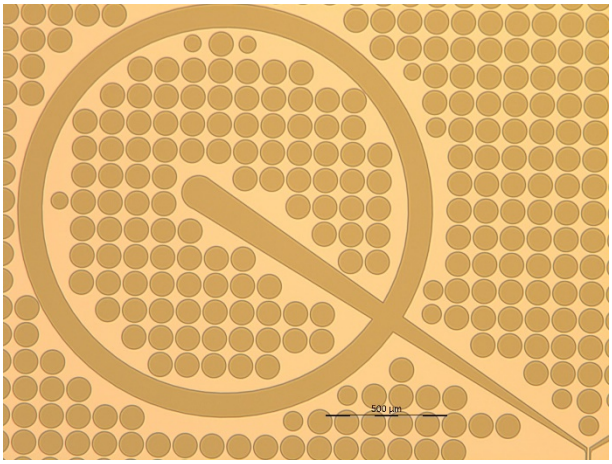


Figure 27: new inlet/outlet with antiflood wall, microchannel and security circles

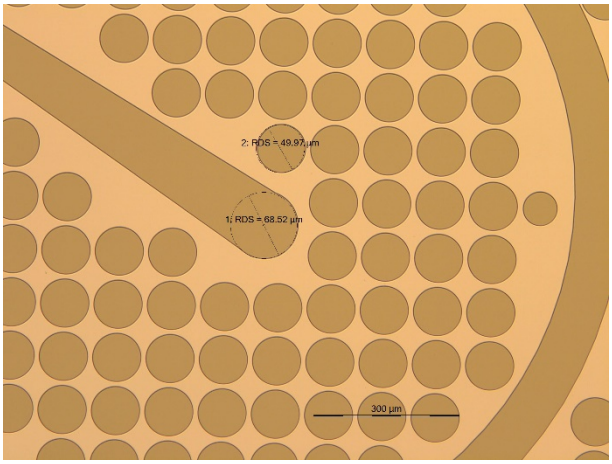


Figure 28: inlet/outlet detail

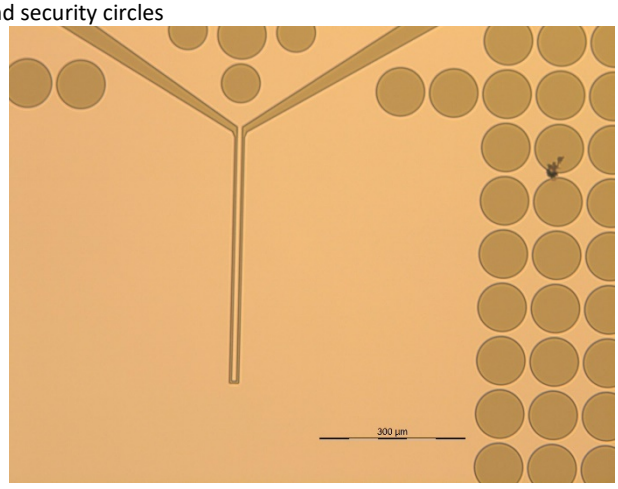


Figure 29: channel detail

3.3. Al_2O_3 ALD – on design 2

So we deposited 40nm of aluminium oxide at 90°C. Results are presented below in Figure 30-33.

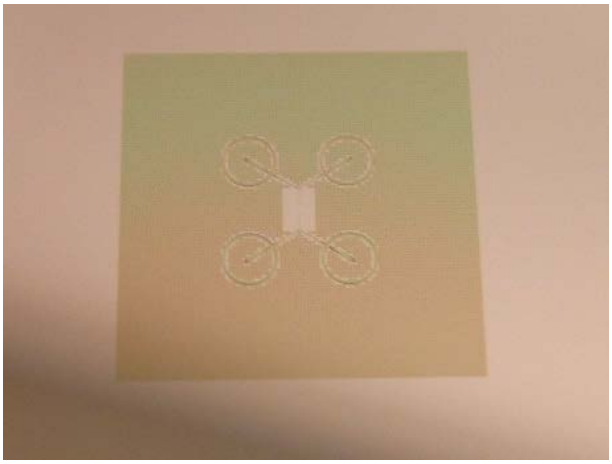


Figure 30: full chip with circular antiflood walls after ALD

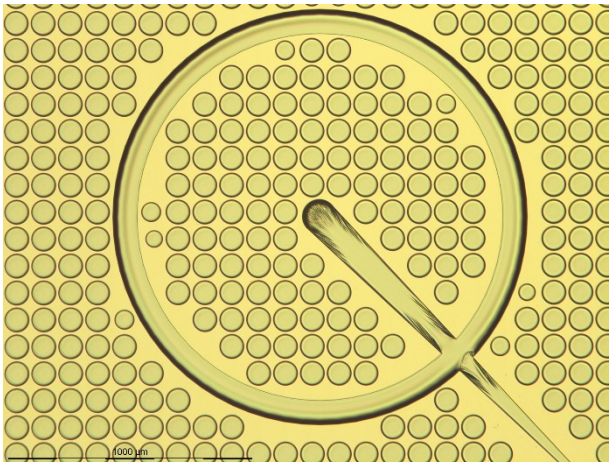


Figure 31: inlet/outlet detail after ALD

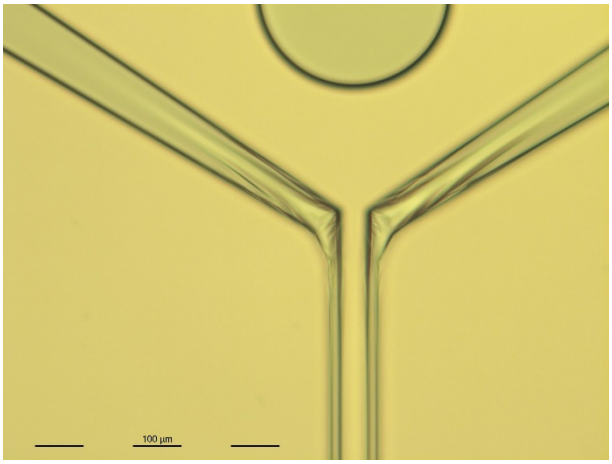


Figure 32: microchannel detail after ALD

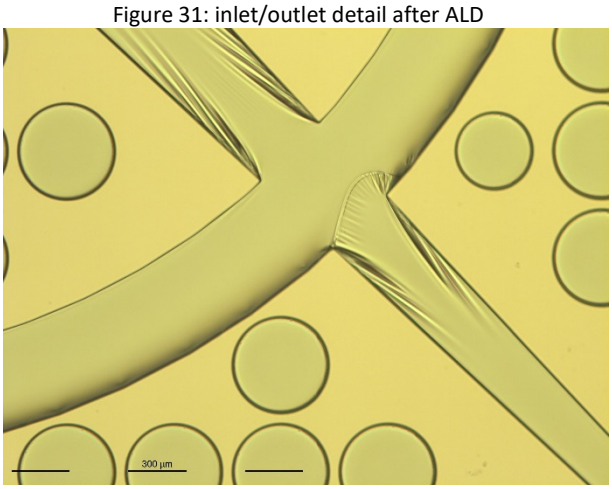


Figure 33: cross between channel and antiflood wall

With this new design, no crack appears after the ALD, so it's a success. However, some ripples occur close to sharp angles, as shown in Figure 33. So we changed a little bit the design to around these angles and the result is really better. Colours aren't the same because of different microscope filters when the pictures were taken.

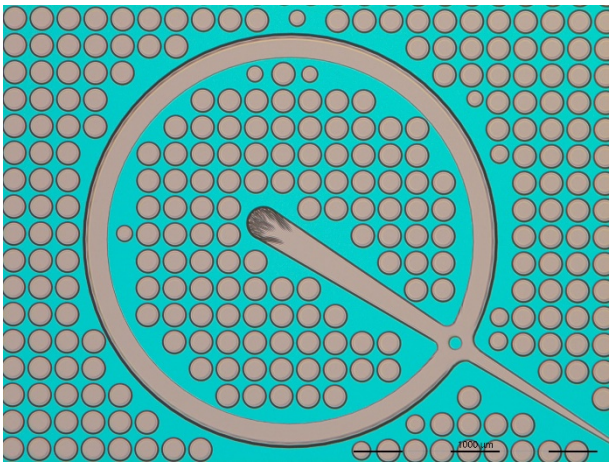


Figure 34: angles rounded to avoid ripples after ALD

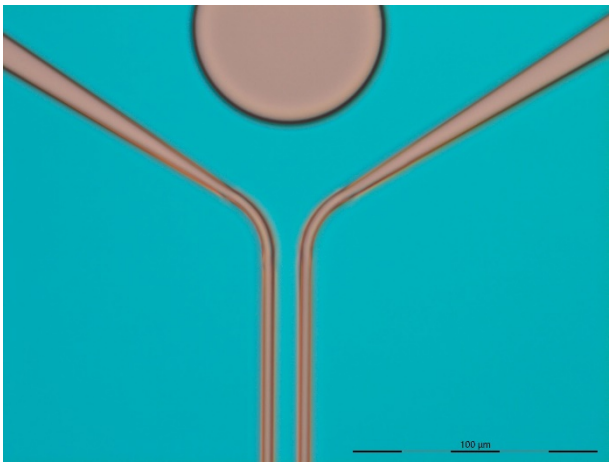


Figure 35: angles rounded to avoid ripples after ALD (2)

3.4. Second photolithography (mask 2) and etchings

It's important to notice that before each resit coating, we have to do a HMDS coating at 125°C for 30min to increase the adhesion between resist and SiN/Al_2O_3 substrate. Unfortunately, after the ALD step, this process damaged our chip, certainly due to the temperature that causes the reflow of the first resist below.

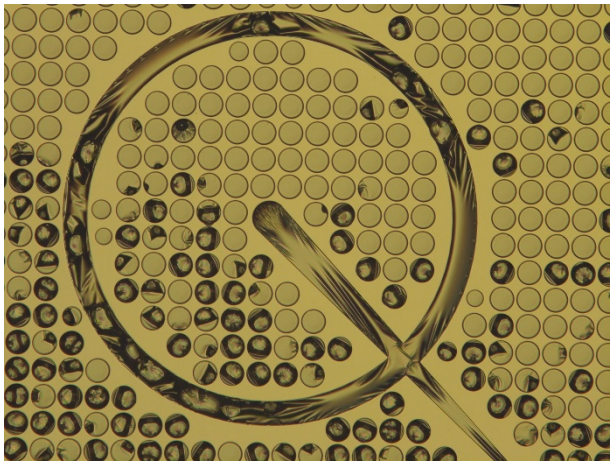


Figure 36: after ALD and HMDS for 30min

So to avoid this problem, we decided to deposit a thin 50nm layer of parylene above the aluminium oxide: indeed, because parylene isn't an oxide, we don't need to do HMDS deposition before the resit coating of the second photolithography. And we can see in Figure 37 that circles aren't broken. We had to modify also the second mask design to match apertures with the new channel end.

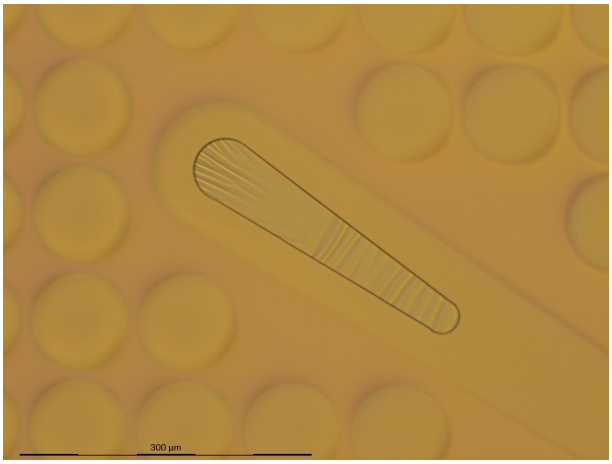


Figure 37: inlet/outlet aperture

Figure 38: releasing cantilever area

The new apertures are really well defined and we can see the little ripples of the aluminium oxide below. However, the realising area of the cantilever is very strange (Figure 38). We don't really know what happened, maybe contamination from some liquid or maybe the parylene layer reacted badly. We still decided to test the etchings of parylene and Al_2O_3 to see if these defaults will disappear.

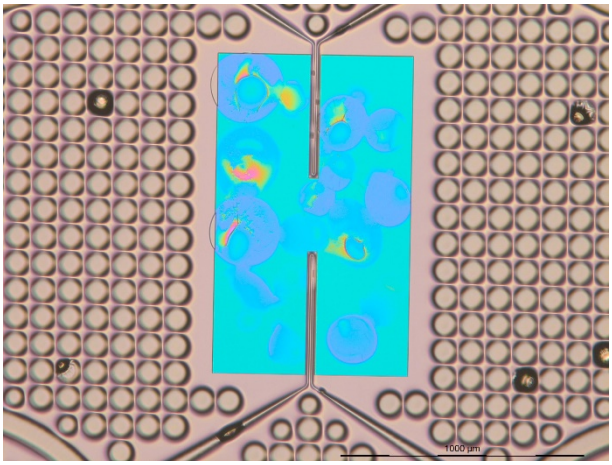


Figure 39: releasing area of the cantilever after parylene etching

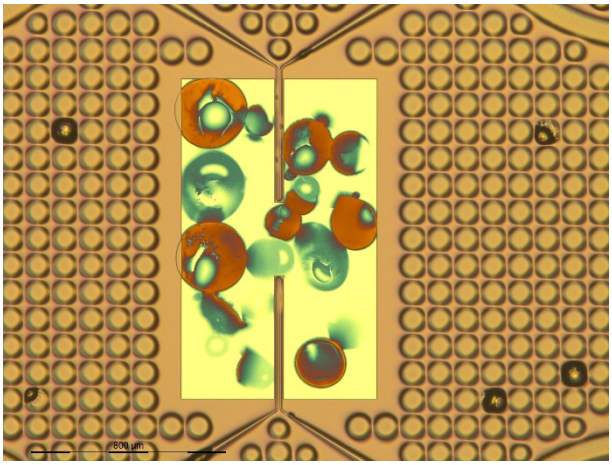


Figure 40: releasing area of the cantilever after Al_2O_3 etching

3.5. Channel emptying

Finally, after these etchings and the O_2 plasma to remove the burned resist, we dip the chips in the UFT 1165 solvent for 1, 3 and 5min at room temperature to see the evolution. Because the resist inside the channel isn't baked, we hope that it will be removed quickly and that the Al_2O_3 will be not damage.

We can observe the results in Table 7. First, we see that the defaults present in the releasing area are removed. However, it's difficult to identify which colours correspond to what. But by deduction, we can assume that green is SiN, blue is the first resist layer and yellow is the silicon substrate. Orange and pink are certainly the parylene and Al_2O_3 layer. We observe that the chip is destroyed after be dipped in solvent. We can't be sure why this destruction occurs and what causes it, some other tests should be lead. Unfortunately, I didn't have enough time to perform them. But some propositions are made in the conclusion to improve the results and avoid this systematic destruction after dipping in solvent.

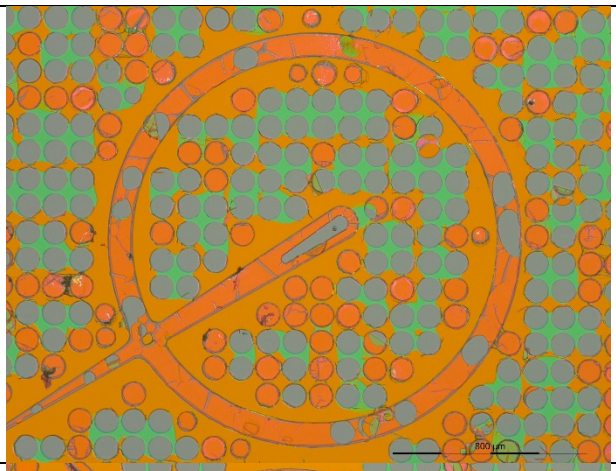
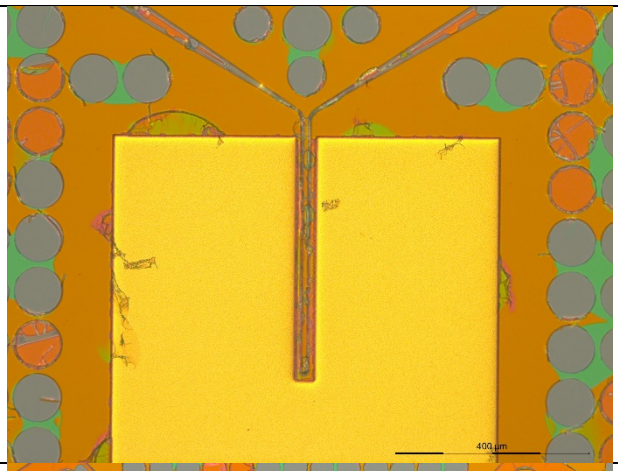
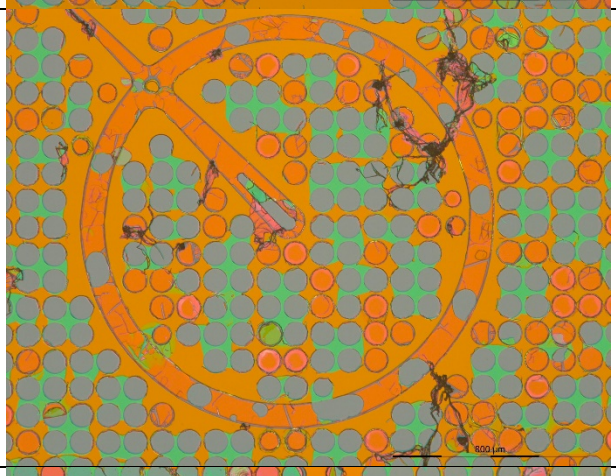
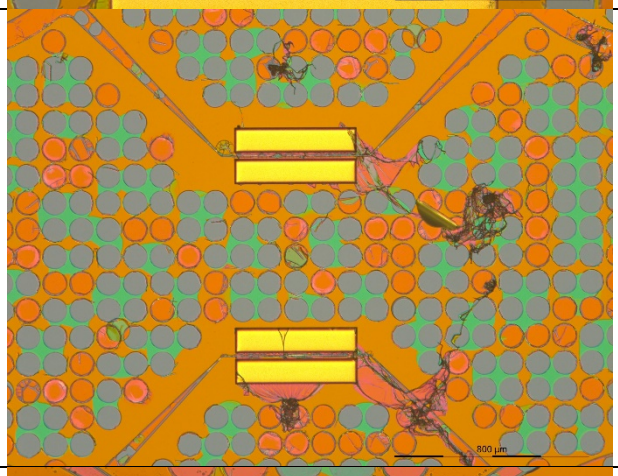
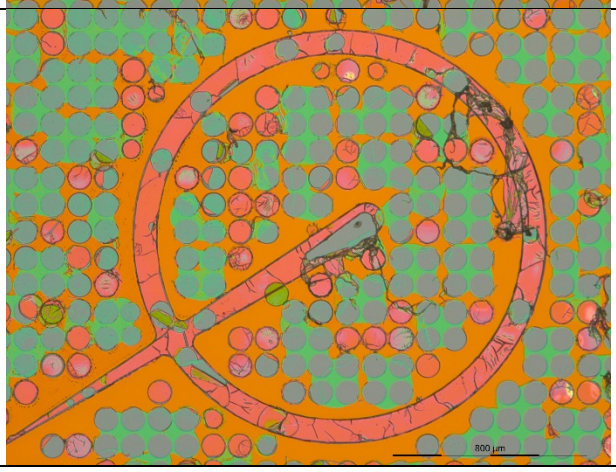
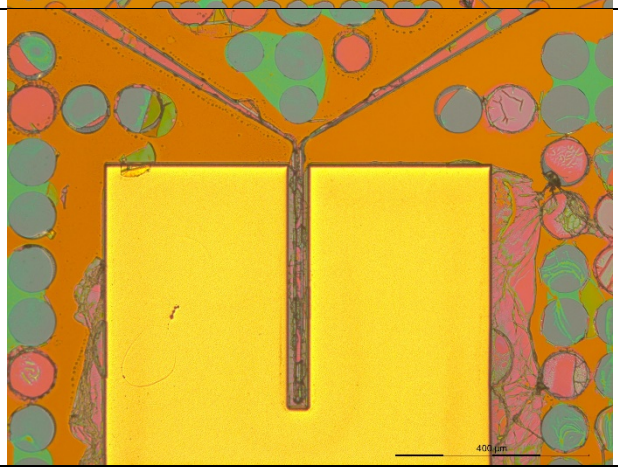
Dip 1min in UFT 1165		
Dip 3min in UFT 1165		
Dip 5min in UFT 1165		

Table 7: emptying channel tests with UFT 1165 on the design n°2

Conclusion and acknowledgements

After four months of work, we learned a lot concerning deposition of aluminium oxide. We had a lot of problems that we tried to solve one by one. First, cracks occurrences were really challenging and tests to find a solution took a lot of time. The use of a hard bake resist seemed to be a good idea, but unfortunately, the resist became too hard and it was impossible to remove it later. Aluminium oxide thickness played also an important role. We began with 100nm, but we've continued after with 40nm and we observed collapse. We had to do a compromise between the cracks and the strength of the layer.

Channel empting is still a big problem. Apparently, the solvent causes delamination of aluminium oxide if we dip too long. Solutions aren't trivial, but I propose below some ideas to improve the results and prevent the chips destruction.

We could deposit a really thicker layer of aluminium oxide for several reasons: first, it could prevent the collapse, because the walls will be stiffer. Even if cracks appear, we could deposit one or two additional layers of 100nm to achieve up to a 200nm or 300nm layer thick. So these cracks would exist only in the first layer, not in the next ones and could be not problematic when we dip the chip in the solvent. Those tests could be really interesting. We could also change the resist, find one which is easier to strip. Or we could optimize the solvent choice. In some literature, they strip their resist AZ 5214 with an acetone bath for 12h (3).

I really appreciate to lead this project in cleanrooms. It was a first experience for me and, even if I had a lot of problems, it was a pleasure to search solutions and resolves challenges. I'm still thinking that aluminium oxide could be a good option to manufacture transparent microchannel. It has good mechanical properties and ALD gives very confirm film. I think the key is in the layer thickness and we have to find the optimal one.

I would like to thank my PhD assistant, Annalisa De Pastina, for her smart advices, her precious time and her contagious motivation. Prof. Guillermo Villanueva was also an excellent supervisor with a strong experience and always with solutions ideas.

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Table of Figures and Tables

Figure 1: change of cantilever frequency due to cell flowing (1) 3
Figure 2: (a) Schematic drawing of nanocrystal (NC) memory and (b) cross sectional TEM images showing the HfAlO/W/HfAlO structure of nanocrystals (NC) embedded in HfAlO (2) 4
Figure 3: SEM images of (a) photoresist structures coated by a 35 nm ALD TiO_2 thin film, (b) a 45° tilted view of TiO_2 nanochannels, (c) a magnified view of b, and (d) a nanochannel before (left) and after (right) post-ALD deposition to scale down the channel dimensions (3). 4
Figure 4: Released cantilever with fluidic inlet/outlet (4) 5
Figure 5: microchannel manufactured with parylene - SEM picture – result of A. Aupée project (5) 5
Figure 6: aluminium oxide ALD cycle in four steps (6) 6
Figure 7: CMi's machine for ALD; BENEQ TFS200 (8) 6
Figure 8: process flow of the project. Height steps have to be achieved. Two photolithographies, one deposition by ALD and several etchings to open the inlet/outlet and to remove the resist. 7
Figure 9: Mask 1 with inlet/outlet (to be opened with the next lithography), microchannel and security resist. Resist is green parts and SiN white ones 8
Figure 10: Mask 2 with inlet/outlet apertures and cantilever shape. Green parts are the resist of 1st photolithography, white part is SiN and blue part is the resist of the 2nd photolithography. Al_2O_3 is transparent but cover the entire wafer. 8
Figure 11: parylene contact angle versus time (14). The contact angle doesn't excess 65°. Parylene is hydrophobic 9
Figure 12: Al_2O_3 contact angle versus time. The contact angle could be low due to impurities on the wafer. With a washed wafer, we obtain a contact angle of about 40°. Al_2O_3 is hydrophilic 9
Figure 13: dose test for the 1st photolithography, defocus = *-2.* We conclude that a dose of 170 $mJ \cdot cm - 2$ is ideal. 10
Figure 14: cracks appeared after 100nm Al_2O_3 ALD. We don't know if aluminium oxide or resist has cracked and we must to determine that by tests 11
Figure 15: cracks in the inlet/outlet 11
Figure 16: permeability test, chip dip in solvent. Aluminium oxide is delaminated and the channel is broken. We must determine if the solvent has an influence on the aluminium oxide or if this result is due to the cracks showed below. 12
Figure 17: 100nm Al2O3, hard bake at 120°C. Cracks appear again. 13
Figure 18: 100nm Al2O3, hard bake at 150°C. Cracks are remained because the resist is stronger and doesn't expand during the ALD. 13
Figure 19: releasing area of the cantilever, yellow is low stress SiN 15
Figure 20: end of the cantilever with the microchannel 15
Figure 21: inlet/outlet aperture with 1st resist below 15
Figure 22: alignment cross after 2nd photolithography 15
Figure 23: releasing area after Al_2O_3 etching 16
Figure 24: cantilever with channel after Al2O3 etching 16
Figure 25: cantilever after Bosch Process 16
Figure 26: cantilever with channel after Bosch Process 16
Figure 27: new inlet/outlet with antiflood wall, microchannel and security circles 20
Figure 28: inlet/outlet detail 20
Figure 29: channel detail 20
Figure 30: full chip with circular antiflood walls after ALD 21
Figure 31: inlet/outlet detail after ALD 21
Figure 32: microchannel detail after ALD 21
Figure 33: cross between channel and antiflood wall 21

Figure 34: angles rounded to avoid ripples after ALD 21
Figure 35: angles rounded to avoid ripples after ALD (2) 21
Figure 36: after ALD and HMDS for 30min 22
Figure 37: inlet/outlet aperture 22
Figure 38: releasing cantilever area 22
Figure 39: releasing area of the cantilever after parylene etching 23
Figure 40: releasing area of the cantilever after Al_2O_3 etching 23

Table 1: Al_2O_3 thickness versus resist hard bake 13
Table 2: tensile stresses introduced by aluminium oxide layers 14
Table 3: chips dip for 1min in different solvents versus ALD temperature and layer thickness 14
Table 4: solvent tests to empty the channel 17
Table 5: O_2 plasma and solvent tests versus temperature 18
Table 6: solvent test with parylene layer on top of Al2O3 layer 19
Table 7: emptying channel tests with UFT 1165 on the design n°2 24

Appendix

- **Runcard**
- **Process Flow**

Projet : Optimization of atomic layer deposition of aluminium oxide for suspended microchannel fabrication
Operator : Mathieu Aberle
Created : 10.06.2016 **Last revision** : 10.06.2016
Substrates : **Silicon test wafers,100/P/SS/01-100**; silicon <100>, 100mm, 525um, p-type, single side, Test, 0.1-100 Ohmcm

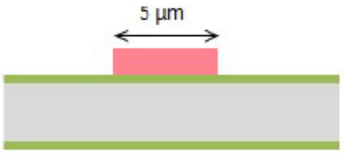
Step N°	Description	Equipement	Program / Parameters	Target	Actual	Remarks	Name	Date
1	**SiNx-ls LPCV**							
1.1	LPCVD low stress silicon nitride deposition,	Z3/Centrotherm	done by CMi	500nm				
2	**PHOTOLITHOGRAPHY - Mask 1**							
2.1	HMDS	Z1/YES3	Prog. 5. in zone 1 Prog. 0. in zone 6					
2.2	AZ ECI coating	Z1/RiteTrack 88	AZ_ECI_5um	5 um				
2.3	PR expose	Z5/MLA150	1st mask, MAB_layer1_250520 170 mJ/cm2 ; defocus = -7					
2.4	PR develope	Z1/ RiteTrack 88	Dev_AZ_ECI_5um					
3	**ATOMIC LAYER DEPOSITION**							
3.1	Al2O3 ALD	Z4/TFS200 ALD	recipe "Al2O3 40nm 90C"	40nm 90°C		The tickness can be tuned for future tests		
4	**PHOTOLITHOGRAPHY - Mask 2**							
4.1	HMDS	Z1/YES3	Prog. 5. in zone 1 Prog. 0. in zone 6			If needed, ideally avoid it if possible		
4.2	AZ ECI coating	Z1/RiteTrack 88	AZ_ECI_5um	5 um				
4.3	PR expose	Z5/MLA150	2nd mask, MAB_layer2_250516 200 mJ/cm2 ; defocus = -7					
4.4	PR develope	Z1/RiteTrack 88	Dev_AZ_ECI_5um					
5	**OXIDE DRY ETCHING**							
5.1	Al2O3 etching	Z2/STS Multiplex	recipe "_saphir" ; 1min	40nm 1min				
6	**SILICON AND SiNx-ls DRY ETCHING**							
6.1	Si3N4 etching	Z2/ Alcatel 601E	recipe "Nitrure_1" ; 2min	500nm 2min				
6.2	Si etching	Z2/ Alcatel 601E	recipe "ANISO-ADP" ; 3min	10um 3min		Bosch Process		
7	**LIFT-OFF**							
7.1	Oxygen plasma	Z2/Tepla GiGAbatch	Strip_High_30s	30sec				
7.2	Remover UFT 1165	Z14/Wetbench_Solvent	Dip until resist is removed			Ideal dip time must be determined		
7.3	First rinse	Z14/Wetbench_Solvent	DI Rinse					
7.4	Second rinse	Z14/Wetbench_Solvent	DI Rinse					
7.5	IPA	Z14/Wetbench_Solvent	IPA Rinse					
8	**SILICON DRY ETCHING**							
8.1	Si etching	Z2/ Alcatel 601E	Si_release program ; SF6 chemistry 5min	5min				

Optimization of atomic layer deposition of aluminium oxide for suspended microchannel fabrication

Process Flow

1) Substrate: *Si test*
SiNx-ls LPCVD
Machine : Centrotherm
Thickness : 500nm

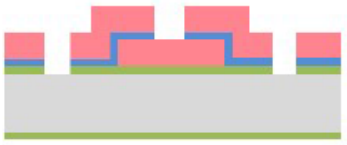
2) Photolithography: *Mask1*
Machine: MLA150
PR: AZ ECI 5µm
Mask : CD = 5µm



3) Deposition
Al_2O_3
Machine : ALD
Thickness : 40-100nm

4) Photolithography: *Mask2*
Machine: MLA150
PR: AZ ECI 5µm
Mask : CD = 5µm

5) Al_2O_3 + SiN Dry etching
Machine: STS
Etching depth: 100nm + 500nm



6) Silicon Dry etching
Bosch Process
Machine: Alcatel 601E
Etching depth: 10 µm

7) PR etching
Machine : UFT PR Remover
Channel emptying

8) Dry Si Etching
SF6 etching
Machine: Alcatel 601E
Etching depth: 40 µm

Author : Mathieu Aberle