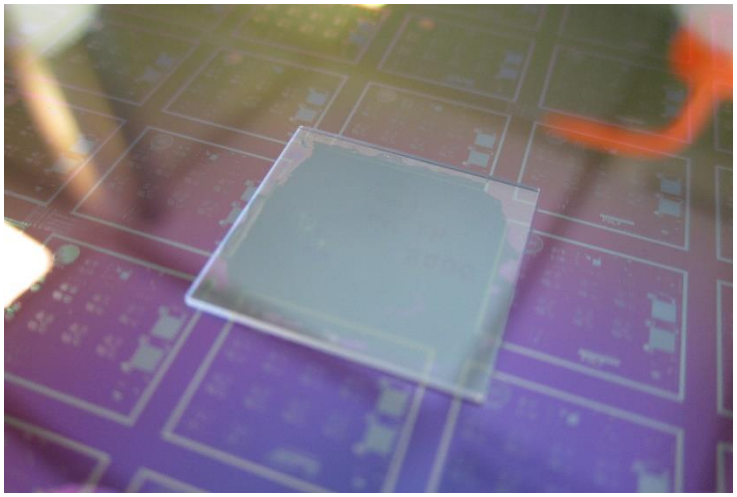
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Nano SAW Devices For Sensing Applications



Spring 2014 Semester Project

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Introduction

Surface acoustic wave (SAW) devices have been studied since the 1960s, starting with the conception of interdigital transducers to generate and detect the waves and the use of piezoelectric materials to propagate the waves. SAW devices have been fabricated for a variety of applications, including resonators, oscillators, bandpass filters, delay lines and MEMS sensors, pumps and mixers. They are used in millions of electronic devices today and have been demonstrated to be useful in a wide range of MEMS applications [1].

SAW resonators are used for radio and telecommunications because they can be operated at higher frequencies than quartz crystals and are good for non-tuneable applications. SAW devices are fabricated in electronic circuits as filters, oscillators or transformers. In microfluidics, SAWs are used to create pumping or mixing in microchannels, as well as be coupled to a microfluidic array for sensing applications. For the pumping and mixing, the mismatch of sound velocities between the substrate and the fluid are used to create inertial forces and fluid velocities, causing vibration, actuation and liquid transport [2]. Finally, SAW devices are used for RFID tags and for MEMS SAW sensors to detect temperature, pressure. MEMS SAW sensors are also used for biomedical applications to detect mass deposition or viscosity changes [3][4][5][6].

SAW devices are passive, in that they do not require any power to function. Their fabrication is simpler than many MEMS devices, usually requiring a small number of fabrication steps and using the most common metallizations, etching methods and photolithography. All the fabrication techniques are well known and studied and little has to be changed in order to fabricate devices for SAW applications. Also, one can wirelessly interact with SAW devices because enough time delay can be given in between the input and output signal, therefore allowing the devices to be used at long range. Since SAWs do not travel far into the bulk of most materials, not much more than one or two SAW wavelengths of thickness of piezoelectric material is necessary. Given the known fabrication methods, uncomplicated design, minimum amount of material to create the devices, the wireless application and that no power is necessary to run the device, SAW devices are usually cheap and useful in a variety of MEMS applications.

One limitation to SAW devices is the size necessary for adequate creation and later detection of a signal. Many SAW devices seen in papers are order of mm large in order to create enough power in the signal. Another issue with SAW devices is the limitations on the fabrication of the devices by the resolution of the current fabrication methods. For instance, the resolution of photolithography is normally one micron in most cleanrooms. However, even two microns can be difficult to produce, even with the most optimized fabrication process. To move to smaller dimensions, e-beam lithography must be used or special types of photolithography, which takes much longer and more expertise than regular photolithography. Finally, piezoelectric materials are normally costly and require extra consideration during fabrication to insure no discharging occurs due to the material's electric properties. However, even with these limitations, SAW devices are commonly seen in research and industry.

As seen in literature [3][4][5], most of the fabricated devices are on order of millimeters large, work at 440 MHz, meaning wavelengths of around 3 µm, and use $LiNbO_3$ as the piezoelectric material, which will be called LNO throughout the rest of this paper. Given the examples of these papers, one goal of this project was to design and fabricate SAW sensors on LNO chips with the best resolution photolithography in CMi to test our general ability to fabricate such devices at EPFL. In the future, the project will move to the nanometer scale to test whether nano SAW devices are possible. Papers on the subject of SAW devices usually offer one design but do not make an effort to finds limits on miniaturization in terms of widths, apertures and full length of devices. They do not test different designs of interdigital transducers (IDTs) or reflectors or change the angle of propagation to see the influence on the

piezoelectric coupling and the wave velocity. The other goal of this project was to study as many different devices as possible during the first fabrication runs to find the best layouts for future device designs.

In this report, the theory of SAW devices will be discussed, including the wave production and propagation, the piezoelectric materials, the different components of SAW devices and modelling them. Then the layout of the experiment will be explained and the design parameters of the first fabrication runs will be detailed. After this, the first fabrication trials and their results will be presented. Finally, the results of the fabrication trials and the theoretical study will be used to offer improvements to future work.

Theory of SAW Devices

SAWs are surface acoustic waves that propagate across the surface of a solid or liquid. Solid piezoelectric materials like quartz or LNO are used to create and propagate SAWs from an applied potential to an interdigital transducers. These materials, depending on their properties, can have a high piezoelectric coupling factor and create large wave velocities for fast detection. To create the actual sensors, reflectors and IDTs are placed on the piezoelectric surface to interact with, propagate and collect SAWs. Two common layouts of SAW devices are shown in Fig 1. On the left, a two port IDT configuration is used along with direct contact of a potential difference to the IDTs to produce the SAWs. On the right, a one port IDT configuration with wireless contact is coupled with reflectors to create the SAW device.

The basic operation of a SAW delay line device with two or one ports is as follows: the applied potential to the IDTs, whether direct or wirelessly, is translated by the input IDT into SAWs that propagate across the piezoelectric material's surface. These SAWs are partially reflected and partially transmitted by any sensors and ID tags that have been placed in the direction of the SAWs. The transmitted waves travel to the output IDT in a two port configuration and are translated into a signal or the reflected travel back to the input IDT and are translated into a signal. The time delay line takes advantage of the speed of the waves across the surface; the IDT and reflectors are physically separated a certain distance from each other on the surface so that the SAWs take time to propagate to the reflectors, interact with them and return the information to the IDTs. The distance in between reflectors gives a time difference between signal peaks when receiving SAWs back from each reflector. A network analyzer arranges the reflected peaks in the time domain that depends on the distance from the IDT. The phase shift, separation between the peaks and the times that peaks are received are used to determine feedback such as the ID tag, temperature or pressure as well as wave velocity.

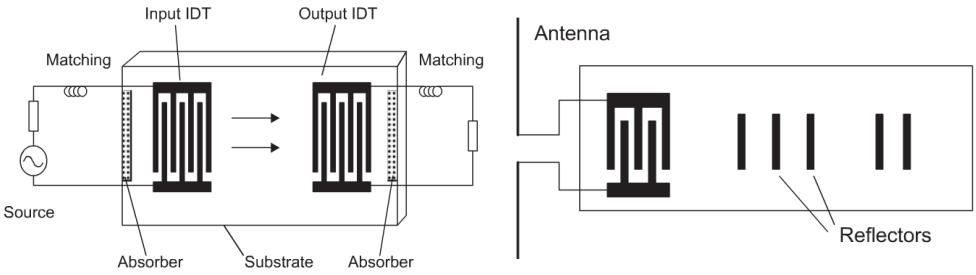

Fig 1 Schematic of two simple saw devices with two ports and one port, directly and wirelessly connected left and right respectively. [1].

Surface Acoustic Waves

Acoustic waves can be generated in the form of bulk and surface waves in a solid or a liquid. Acoustic waves in solids are a propagating phenomenon involving strains in displacing atoms from their equilibrium state and stresses from internal forces within the solid moving the atoms back. This phenomena occurs at a localized displacement point and propagates out to further and further points. In an isotropic material, the propagation expands out in all directions of the solid, but the speed of propagation is different depending on the type of wave produced. Acoustic waves consist of two types of waves: longitudinal and transverse, also called shear. Longitudinal waves are where the displacement of atoms is parallel to the propagation direction, while transverse waves displace atoms normal to the propagation direction. The two types of waves propagate independently of any boundaries of the solid, do not travel far in the solid and have frequency-independent velocities, typically around 6000 and 3000 m/s for longitudinal and transverse waves respectively. The equation for the speed of sound in solids with waves that do not travel far into the solid is:

$$v_s = \sqrt{\frac{Y}{\rho}} \qquad 1$$

Where Y is the Young's modulus of the solid and ρ is the density of the solid. Surface acoustic waves, also named Rayleigh waves, propagate across the surface of a solid; their amplitude decays exponentially when moving away from the surface. Rayleigh waves consist of both longitudinal and transverse waves and have velocities slightly less than transverse waves [1]. Fig 2 visualizes the displacements of atoms with longitudinal and transverse waves versus SAWs.

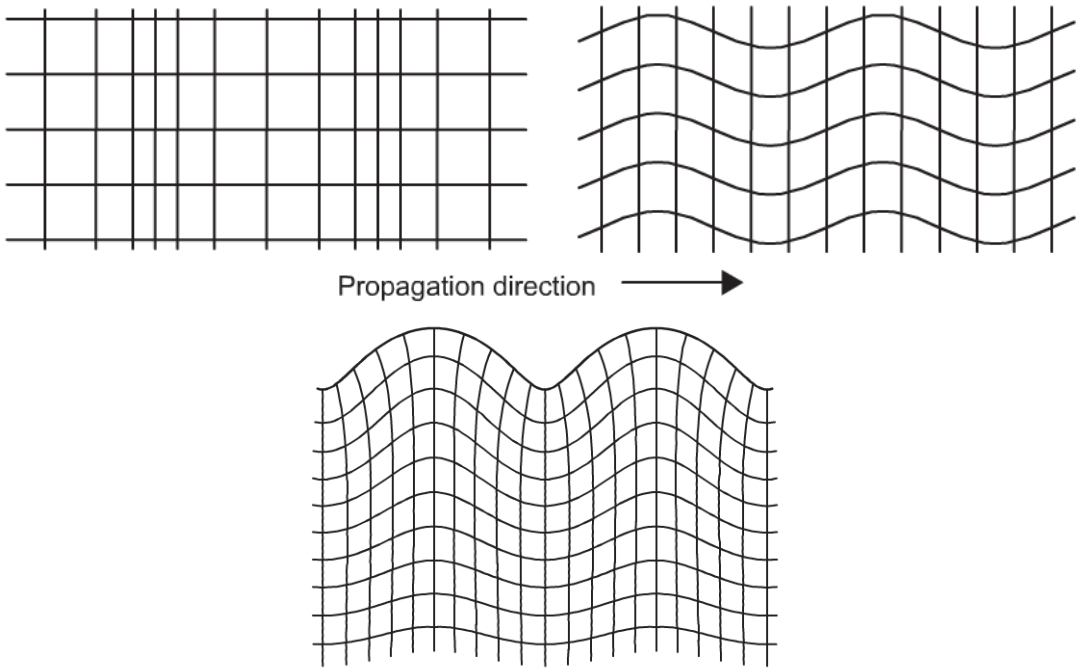

Fig 2 Longitudinal Waves, Transverse Waves, Rayleigh Waves Representation in Top Left, Top Right and Bottom Images Respectively. Propagation of all waves is in the right direction [1].

The definitions of plane waves and Rayleigh waves in a half-space for isotropic and anisotropic materials are defined in [1]. For anisotropic materials, the plane wave solutions for the displacement **u** and the electric potential Φ are:

$$\boldsymbol{u} = \boldsymbol{u}_0 e^{i(\omega t - \boldsymbol{k}\cdot\boldsymbol{x})} \; and \; \Phi = \Phi_0 e^{i(\omega t - \boldsymbol{k}\cdot\boldsymbol{x})} \qquad 2$$

Where ω is the frequency, **k** is the wave vector and $\boldsymbol{u}_0$ and Φ_0 constants that are independent of position **x** and time t.

The Rayleigh wave solutions are found by adding two components of plane waves, transverse and longitudinal, called partial waves. The axes for the Rayleigh wave analysis are set up on the surface of the solid as shown in Fig 3. The definition of the wave vectors is important in defining the wave solutions for the Rayleigh wave. Since the Rayleigh waves do not vary in the x_2 direction, the wave vectors therefore have a zero x_2 component. However, the Rayleigh wave does vary in the x_1 direction by $e^{-i\beta x_1}$, based off the plane wave solution and ϐ denoting the wavenumber of the Rayleigh wave. Finally, the x_3 components of the Rayleigh wave for the transverse and longitudinal wave vectors $\mathbf{k}_t$ and $\mathbf{k}_l$ are equal to $\frac{\omega^2}{V_t^2} - \beta^2$ and $\frac{\omega^2}{V_l^2} - \beta^2$ respectively, also based off the plane wave solutions. Therefore, given that the wave vector is defined in general as $\mathbf{k}=[k_1, k_2, k_3]$, the components for the transverse and longitudinal wave vectors are [1]:

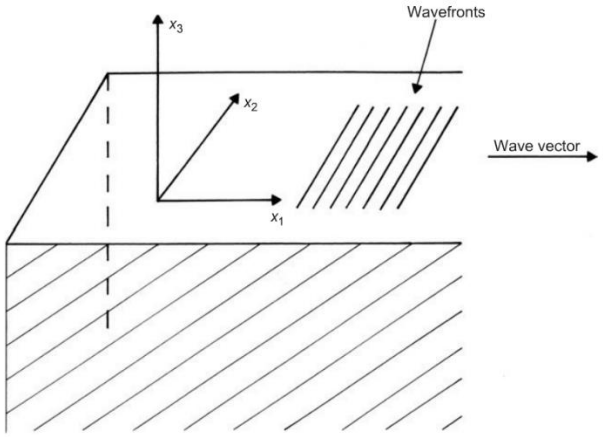

Fig 3 Schematic of axes for Rayleigh wave analysis

$$\boldsymbol{k}_t = \left[\beta, 0, \frac{\omega^2}{V_t^2} - \beta^2\right] \; and \; \boldsymbol{k}_l = \left[\beta, 0, \frac{\omega^2}{V_l^2} - \beta^2\right] \qquad 3$$

Where V_t and V_l are the transverse and longitudinal wave velocities. In the Rayleigh wave analysis for an isotropic material, there is no electrical component because there is no piezoelectricity. To find the wave solutions for a Rayleigh wave in an anisotropic material, an electrical boundary condition must be made at the surface, due to the material properties. This adds an additional component to the isotropic solutions, found in section 2.3.1 of [1]. However, there are multiple solutions that must be considered, divided up into a free-surface case and a metallized surface case, to deal with the electrical boundary condition. After some derivation, shown in section 2.3.2 of [1], the individual Rayleigh wave solutions for the displacement **u** and electric potential Φ are found for both cases. The total solutions for the displacement and electric potential are found by summation over the individual real solutions for both cases. Both the solutions for plane waves and Rayleigh waves can only be found by numerical solutions, due to the complexity of their equations.

Piezoelectric Materials

The piezoelectric effect is only found in some anisotropic materials, where anisotropic means that the properties of the material are different depending on the plane of reference and there is no central

symmetry in the crystal lattice. When SAWs are produced in a piezoelectric material, the waves induce strain by displacing atoms from their equilibrium state; the materials create forces that stress the atoms back into their equilibrium position. Single crystal piezoelectric materials offer the best results for SAW devices because they have low losses. For these materials, the crystal orientation determines the speed and amplitude of the SAWs as well as the piezoelectric coupling. The important properties of a material in general for SAW devices are the wave velocity, piezoelectric coupling, the effect of changes in temperature, diffraction, attenuation and the level of bulk wave generation [1].

To understand the piezoelectric effect, the elasticity, strain of the material must be defined. It is assumed that the piezoelectric material is elastic and linear such that the stress is proportional to strain as described by Hooke's law. It is also assumed that the material is an insulator and there are no free charges. To begin, the strain on a particle within the material is related to the displacement from its equilibrium location, shown in the following formula:

$$S_{kl}(x_1, x_2, x_3) = \frac{1}{2}\left(\frac{\partial u_k}{\partial x_l} + \frac{\partial u_l}{\partial x_k}\right), \quad i, j = 1,2,3 \tag{4}$$

Where x denotes the equilibrium position and u denotes the displacement, which is independent of time in this definition and is dependent on x. All displacements or rotations of the material as a whole solid do not cause internal strain.

The stress tensor T_{ij} describes the internal forces on any plane within the material and is related to the strain tensor S_{kl} by:

$$T_{ij} = \sum_k \sum_l c^E_{ijkl} S_{kl} - \sum_k e_{kij} E_k \tag{5}$$

Where $c^E_{ijkl}$is the stiffness tensor, a fourth-rank tensor with at most 21 independent elements correlating to the physical properties of the piezoelectric material. Both the stress and strain tensors are symmetric, such that $T_{ij} = T_{ji,}\ S_{kl} = S_{lk}$. The stress tensor components are dependent on the electric field E but the superscript of E in the stiffness tensor means that it is the stiffness tensor for a constant electric field. e_{ijk} is the piezoelectric tensor, a third-rank tensor which will be described for LNO in the following section. Knowing the definitions for the strain and strain tensors, as well as the stiffness and piezoelectric tensors, the electric displacement D can then be defined:

$$D_i = \sum_j \varepsilon^S_{ij} E_j + \sum_j \sum_k e_{ijk} S_{jk} \tag{6}$$

Where ε^S_{ij} is the permittivity tensor for a constant strain. The mechanical equation of motion for a piezoelectric material is found by making the approximation that elastic disturbances move slower than electromagnetic ones, such that $E_i = -\frac{\partial \Phi}{\partial x_i}$, meaning the rules of electrostatics can apply. Φ is the electric potential and x_i is the position in the i direction. Combining Equation 3 with Equation 4 gives the equation of motion:

$$\rho \frac{\partial^2 u_i}{\partial t^2} = \sum_j \sum_k e_{kij} \frac{\partial^2 \Phi}{\partial x_j \partial x_k} + \sum_l c^E_{ijkl} \frac{\partial^2 u_k}{\partial x_j \partial x_l} \tag{7}$$

Since there are no free charges, div **D** = 0 and the following formula can also be made by combining Equations 4 and 5:

$$0 = \sum_i \sum_j \varepsilon_{ij}^S \frac{\partial^2 \Phi}{\partial x_i \partial x_j} - \sum_l e_{ijk} \frac{\partial^2 u_j}{\partial x_i \partial x_k} \quad 8$$

The plane wave solutions found in Equation 1 can be substituted into Equations 6 and 7 to find the acoustic wave solutions for various piezoelectric materials. If the determinant of the coefficients is set to zero, four solutions will arise. Three of these solutions are non-disperse acoustic waves, one longitudinal and two transverse. Because of the anisotropy, each solution has phase velocities and electric potentials that are dependent on the propagation direction. This is an alternative method to finding the acoustic wave solutions than described in the Surface Acoustic Waves section of this report, but both are equally valid for finding the solutions. All equations were taken from [1].

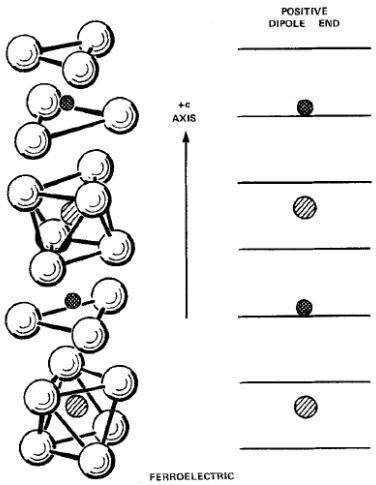

Fig 4 Ferroelectric phase atom position chart for lithium niobate [7].

Lithium Niobate

LNO is a common material used for SAW devices due to the relatively high wave velocities and piezoelectric coupling. It is a man-made material that is ferroelectric and widely used in electro-optic, acoustic, dielectric and many other applications due to having large electro-optic, pyro-electric and photo-elastic coefficients. The standard method for fabricating LNO is by the Czochralski method.

Fig 4 shows the atomic structure for LNO in the ferroelectric phase. The structure consists of planar sheets of oxygen atoms that are in a distorted hexagonal configuration with the interstices of the structure filled one-third of the time by lithium, one-third by niobium and one-third of the time is left vacant. Fig 4 shows the order of the filling of the interstices in the plus c direction, which goes as niobium, vacancy and lithium repeatedly [7]. The crystal structure of LNO is trigonal and has a three-fold symmetry about the c axis seen in Fig 4. It can therefore be described by two different unit cells: hexagonal and rhombohedral. The hexagonal version is shown in Fig 5; the rhombohedral can be seen in [7]. In Fig 5, the principal axes and mirror planes that the crystal structure is symmetric on are shown. The principal axes are used to describe the tensor properties of LNO. In addition, the cut of LNO is designated on these axes or angles to these axes.

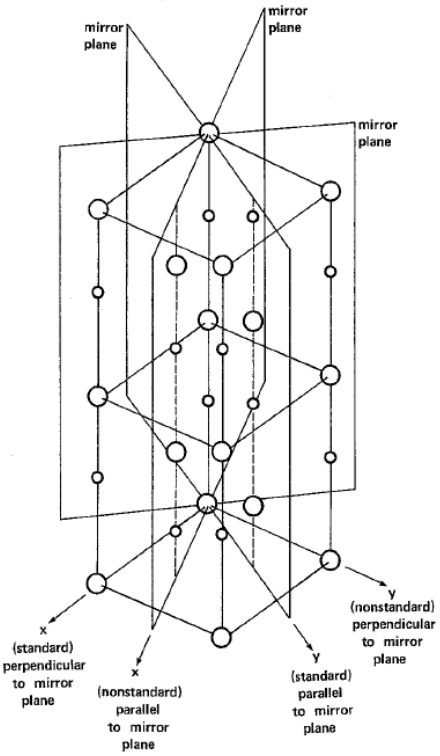

Fig 5 Hexagonal unit cell for lithium niobate with x, y, and z principal axes, left and right images respectively [7].

The orientation of the material is important in finding the wave solutions described in the previous sections. The Cartesian directions X, Y and Z are defined by convention in relation to the crystal lattice and most materials contain their crystal orientation

within their title, such as Y-Z LNO. The nomenclature for the cut of LNO is Axis 1-Axis 2-cut, where Axis 1 is the axis normal to the surface of the chip or wafer and Axis two is the chip or wafer orientation on the surface of the chip or wafer. For example, in this project, XY-cut LNO is used.

The permittivity tensor for LNO looks like the following, due to the crystal symmetry on the mirror axis seen in Fig 5:

$$\varepsilon_{ij} = \begin{bmatrix} \varepsilon_{11} & 0 & 0 \\ 0 & \varepsilon_{11} & 0 \\ 0 & 0 & \varepsilon_{33} \end{bmatrix} \quad 9$$

The values for ε_{11} and ε_{33} are shown from several papers in the left image of Fig 6 [8]. It is common to normalize the permittivity in terms of the vacuum permittivity, creating dimensionless constants called the relative permittivities or dielectric constants. The piezoelectric tensor is a third rank tensor and for LNO, the tensor in matrix form looks like [7]:

$$e_{ijk} = \begin{bmatrix} 0 & 0 & 0 & 0 & d_{16} & -2d_{22} \\ -d_{22} & d_{22} & 0 & d_{15} & 0 & 0 \\ d_{31} & d_{31} & d_{33} & 0 & 0 & 0 \end{bmatrix} \quad 10$$

The elastic constants, piezoelectric constants, dielectric constants without normalization and the mass density are also shown in the right chart of Fig 6 for LNO and lithium tantalate.

$\varepsilon_{11}^T/\varepsilon_0$	$\varepsilon_{33}^T/\varepsilon_0$	$LiNbO_3$
84	30	WARNER ET AL. [15]
84.6	28.6	YAMADA ET AL. [17]
85.1	28.7	SMITH & WELSH [13]
84.1	28.1	NAKAGAWA ET AL [12]

	$LiNbO_3$	$LiTaO_3$
Elastic constants in 10^{10} N/m^2		
c_{11}^E	19.839 ± 0.089	23.28 ± 0.36
c_{12}^E	5.472 ± 0.097	4.65 ± 0.46
c_{13}^E	6.513 ± 0.193	8.36 ± 0.43
c_{14}^E	0.788 ± 0.004	-1.05 ± 0.02
c_{33}^E	22.790 ± 0.324	27.59 ± 0.50
c_{44}^E	5.965 ± 0.008	9.49 ± 0.04
Piezoelectric constants in C/m^2		
e_{15}	3.69 ± 0.06	2.64 ± 0.27
e_{22}	2.42 ± 0.04	1.86 ± 0.10
e_{31}	0.30 ± 0.08	-0.22 ± 0.28
e_{33}	1.77 ± 0.12	1.71 ± 0.55
Dielectric constants in ε_0		
ε_{11}^S	45.6 ± 1.5	40.9 ± 3.9
ε_{33}^S	26.3 ± 1.6	42.5 ± 2.6
Mass density in kg/m^3		
ρ	4628	7454

Fig 6 Left: Dielectric constants from four different papers for lithium niobate. Right: Various material parameters for lithium niobate and lithium tantalate.

The electromechanical coupling coefficient K^2 is defined in terms of the piezoelectric coefficient e, the elastic constant c and the dielectric permittivity ε, shown in Equation 9[1]:

[1] http://books.google.ch/books?id=RM6fvMhN4V0C&pg=PA19&source=gbs_toc_r&cad=3#v=onepage&q&f=false

$$K^2 = \frac{e^2}{c\varepsilon} \qquad 11$$

[8] and [9] discuss the dependence of the coupling coefficient on the angle of propagation inside piezoelectric, but do not provide the documentation for exactly how to derive the relationship between the two. However, both provide graphs for various cuts of LNO, though not of XY-cut. Several values of K^2 versus cuts of LNO are shown in Fig 7 [9].

$LiNbO_3$					
Mode	h/λ	V, m/s	h/λ_m	V_m, m/s	K^2, %
— X-cut, Z propagation direction, h × f = 1527 m/s —					
A_0	0.5	3053.9	0.507	3002.6	3.4
SH_0	0.42	3577.0	0.42	3577.0	0
S_0	0.225	6778.2	0.23	6630.4	4.3
— X-cut, Y+170^0 propagation direction, h × f = 220 m/s —					
A_0	0.145	1527.4	0.145	1521.3	0.8
SH_0	0.05	4411.6	0.06	3580.4	37.7
S_0	0.035	6487.1	0.035	6395.5	2.8
— X-cut, Y+30^0 propagation direction, h × f = 352 m/s —					
A_0	0.195	1801.9	0.195	1797.4	0.5
SH_0	0.09	4039.1	0.09	3987.6	2.6
S_0	0.05	7036.3	0.06	5981.4	30.0
— Y-cut, X propagation direction, h × f = 218 m/s —					
A_0	0.145	1544.9	0.145	1513.8	4.0
SH_0	0.05	4353.0	0.06	3594.0	35.0
S_0	0.035	6607.1	0.035	6604.4	0.08

Fig 7 Various cuts of LNO versus the electromechanical coupling coefficient K^2

Other examples of common LNO cuts are shown in Fig 8 compared to quartz and lithium tantalate. The chart in Fig 8 give a comparison of the wave velocities, the percent of piezoelectric coupling between the electric and acoustic fields the relative permittivity, the temperature coefficient of delay TCD, advantages, disadvantages and common applications. Depending on the application, different axes or angles on these axes may be desired, whether for faster wave velocities or larger piezoelectric coefficients or little dependence on changes in temperature [1].

	Y–Z lithium niobate ($LiNbO_3$)	128°*Y–X* lithium niobate ($LiNbO_3$)	*ST–X* quartz (SiO_2)	36°*Y–X* lithium tantalate* ($LiTaO_3$)
v_f (m/s)	3488	3979	3159	4212
$\Delta v/v$	2.4%	2.7%	0.06%	2.4%
$\varepsilon_\infty/\varepsilon_0$	46	56	5.6	50
TCD (ppm/°C)	94	75	0	32
Advantage	Low diffraction, strong coupling	Low bulk waves, strong coupling	Small TCD	Strong coupling, moderate TCD
Disadvantage	Large TCD, strong bulk waves	Large TCD	Weak coupling	
Suitability	Wide-band filters, RACs, convolvers	Wide-band filters	Narrow-band filters, resonators, pulse compression	Low-loss filters, RF filters

RAC: reflective array compressor.
*Leaky wave, special considerations apply – see text.

Fig 8 Common cuts for LNO compared to quartz and lithium tantalate [1].

Components of a SAW Device

There are two components of SAW devices that will be discussed in this report: the IDT and the reflectors. The method of providing the potential difference and characterization in this project would have been made directly by using ground-signal-ground (GSG) contact probes. Three bonding pads measuring 100 by 100 μm^2 are placed on each side of the IDTs to connect to GSG probes to the IDTs. An antenna could also have been attached to the IDTs to provide the signal.

IDTs

Interdigital transducers change an applied potential difference into a periodic electric field that creates surface acoustic waves within the piezoelectric material. IDTs also work in the reverse fashion, such that they can translate incident waves into a potential difference. Due to the electric and mechanical coupling with piezoelectric materials, the applied electric field is changed into a mechanical stress that propagates across the surface of the material as discussed in the section on piezoelectric materials. Five IDT designs were studied in this project: standard IDT, distributed acoustic reflection transducer (DART) single phase unidirectional transducer (SPUDT), Hanma-Hunsinger SPUDT, Lewis SPUDT and Yamanouchi FEUDT.

The standard IDT is a reflective transducer, meaning that there are internal wave reflections due to the electrodes. The other four IDTs are SPUDTs, a special type of non-reflective transducer. Normally, non-reflective transducers has large insertion losses due to the need to suppress unwanted multiple transit signals, but unidirectional transducers are designed for low reflectivity as well as low losses. SPUDTs generate waves with different amplitudes in two directions and if the directivity of the waves is strong enough, the transducer becomes an acoustic-electric two port device that works on single phase voltage driving. SPUDTs need internal reflectivity so the design of the electrodes, also called fingers, includes some asymmetry in the widths and gaps [1].

The most generated frequencies of surface acoustic waves by IDTs are dependent on the pitch of the IDTs and therefore determine the best operating frequency of the SAW device. The electrode width is dependent on the fabrication process. For photolithography, the best resolution is around one micron in most cleanrooms while smaller dimensions can be reached with electron beam lithography. Most papers use electrode widths of 2.5 µm [3][4]. The power of the SAWs can be increased by repeating the IDT design in a sequence next to each other, as well as increasing the aperture of the IDTs.

All five types of IDTs studied in this report can be seen in Fig 9, Fig 10 and Fig 11. The period of the IDT is given as p in the standard IDT and λ_0 for the DART, Yamanouchi, Hanma and Lewis. The standard IDT has the simplest design and is the easiest to simulate. The electrode widths and gap widths are the same size and the top and bottom portions of the IDT contain the same design. It's best operating frequency is one-fourth of the electrode width. It is commonly seen in papers concerning SAW sensors. However, the signal generated by the standard IDT moves in both directions parallel to the IDT, splitting the power of the generated SAWs in half.

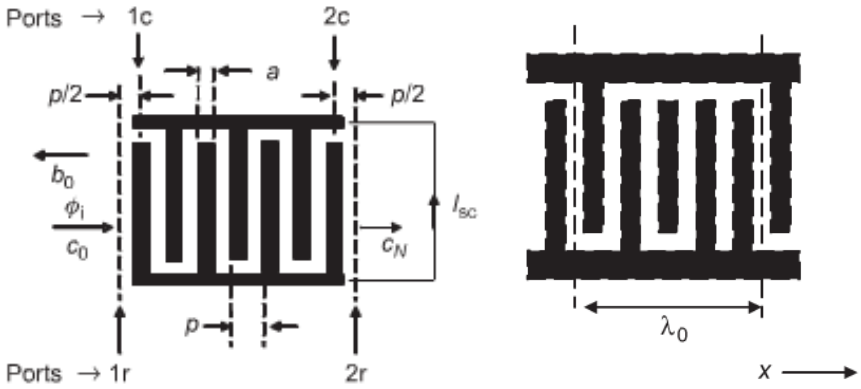

Fig 9 Standard IDT, left. Yamanouchi FEUDT, right [1].

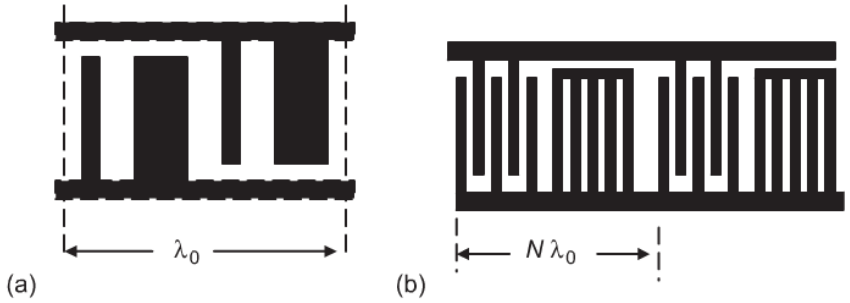

Fig 10 a) Hanma-Hunsinger SPUDT b) Lewis SPUDT [1].

Fig 11 DART SPUDT [4]. Two periods are shown.

The DART has an asymmetric design consisting of two electrodes with a width of $\lambda_0/8$, one electrode with a width of $\lambda_0/4$ and gaps of $\lambda_0/8$. The DART can be designed in many other ways, depending on the application and is seen often in literature with several designs. Although the wave propagation from a DART is much more difficult to understand and simulate, DARTs generate strong SAWs in one direction and could require less repeating structures to produce the same power as a standard IDT. For miniaturization, this may become a critical parameter.

The Hanma and Hunsinger SPUDT was the first type of SPUDT produced. The electrode widths $\lambda_0/16$ and gaps of $3\lambda_0/16$ and the gap widths are $\lambda_0/8$. The narrowness of the electrode widths in this design make it necessary to produce large period structures, which create large SAW wavelengths. Therefore, the frequencies the IDT work at are lower, but the transduction is stronger than for a DART structure. The Lewis IDT alternates sets of standard IDTs with reflective gratings. The electrodes and gaps are the same size, but there is a double gap width between the IDTs and reflective gratings. The period

and therefore the SAW wavelength are quite large. This IDT can be used in non-reflective and reflective conditions, all strengths of piezoelectric substrates and the design can be adapted to deal with internal reflections. However, this design is not often used due to have the reflectivity and transduction centers in different regions of the IDT, unlike together in the other IDT designs. Finally, the Yamanouchi FEUDT includes floating electrodes that becomes the reflection centers of the IDT, due to the symmetry of the IDT around the floating electrode. Otherwise, the electrode and gap widths are the same size. FEUDTs are usually only used with strongly piezoelectric materials because the reflection coefficient is proportional to the piezoelectric coupling based on the design of the IDT [1].

Reflectors

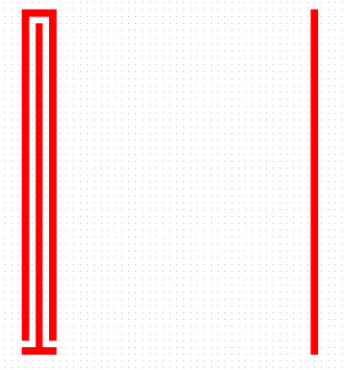

Fig 12 IDT style and simple reflectors, left and right respectively

In order to use SAWs as sensors for properties such as temperature and pressure, reflectors are used to interact with the propagating SAW waves. Shorted gratings are normally used, which are simply metal lines shaped like the fingers of the IDT. The two common types of reflectors, simple and IDT style, are shown in Fig 12. Increasing the number of lines in a reflector increasing the amount of interaction it will have with the SAWs and produce a stronger peak or dip in the output signal. Stronger peaks will give better resolution of the results, particularly for very small devices that create low signals. A reflector array was designed so that the first and last reflectors were IDT style while the middle reflectors were simple style. This was so that during signal analysis, the first and last peaks of the reflectors would be larger than those in the middle. The first and last reflectors were just to recognize the beginning and end of the signals from the reflectors, while the middle reflectors could be set up for ID tags or temperature sensors and provide the actual information from the SAW device.

LNO is very sensitive to temperature variation, which means that it has a large temperature coefficient of delay. This property affects the propagation and reflection of SAWs by altering their time delay and phase, which can be used to determine temperature from the output signal of a SAW device. To make the temperature sensor, three reflectors are placed at large distances from each other on the piezoelectric surface. The phase difference generated by the reflectors as a function of temperature is found by the following formula [3]:

$$\Phi_T = k * 2\pi f * (\Delta\tau_{31} - 2\Delta\tau_{21}) \qquad 12$$

Where k is equal to the ratio of the third-to-first reflector distance to the second-to-first distance, f is the frequency of the SAWs, τ_{31} is the time delay between the third and first reflectors and τ_{21} is the time delay between the second and first reflectors. An example of a SAW device with reflectors for temperature sensors is shown in the right image of Fig 1. The first reflector is the closest (first) reflector to the IDTs. It is possible to use only two reflectors to make a temperature sensor, but if the phase shift becomes larger than 360°, it can become an issue.

ID tags like RFID can also be implemented using reflectors on the piezoelectric surface. If set at regular intervals in a row, the presence or absence of peaks in the output signal can correspond to a binary system of measurement. Each reflector in the row represents one bit and having even eight reflectors, for example, would give 2^8 possible combinations for unique identification.

Pressure sensing with SAW devices requires a sealed cavity to give a reference pressure, as well as temperature sensors to isolate the pressure sensing from temperature variations. However, pressure sensors work similar to temperature sensors by using the same idea for the design of the reflectors. For pressure detection, the external pressure on the cavity causes time and phase angle shifts of the reflection peaks that are measured in the output signal [3].

Modelling SAW Devices

The modelling of SAW devices is complicated because of the complex creation and propagation of SAWs that is dependent on the setup of the IDTs and the piezoelectric material. Two options for modelling SAW devices are coupling of modes and equivalent circuit. Both are seen in literature for simulation of the IDTs of SAWs. Both types of models are interchangeable when trying to model the signal and currents that will come from a certain circuit. However, the theory behind creating these models was more than could be understood during this project. For more information on coupling of modes and equivalent circuit, see [1][10][11].

COMSOL Multiphysics can also be used to try to simulate SAW devices, but even with a sample file that contained a standard IDT design, it was unclear how to properly simulate propagating SAWs. However, COMSOl Multiphysics can be easily used to find the resonance frequencies for a given IDT configuration by altering the sample file. The results of finding the resonance frequency for a standard-style 2 finger IDT are shown in Fig 13. The fingers are 1 µm wide and the gap width is also 1 µm. The change in the shape of the IDT denotes displacement of the surface due to the application of the resonance frequency and the color code shows change in displacement on the area of the IDT. For designing IDTs, COMSOL Multiphysics would be useful in finding the best frequencies to work at during characterization.

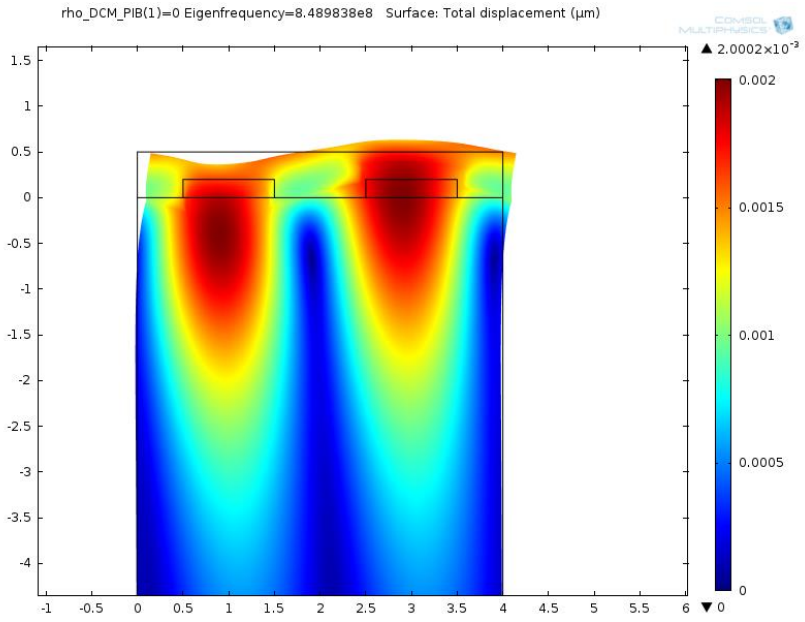

Fig 13 Resonance frequency results for a standard IDT with 1 µm wide fingers.

Experiment

In this project, the first goal was twofold: to test as many designs and parameters as possible in the first mask while optimizing the first fabrication runs for the best resolution across the whole design. With this in mind, five different IDTs and two types of reflectors were designed in the first mask, as discussed in the previous section. The most common configuration seen in papers about SAW devices [3][4] had apertures of at least 50 times the SAW wavelength, total lengths around 8 mm long, distances between the propagation point and first reflectors around 3 mm and a critical dimension of 2-4 microns. Given these recommendations, the aperture of most of the devices was around 50 times the wavelength or slightly less than this, the length between the IDTs and first reflectors was around 2-3 mm and the critical dimension of 2 microns was for the thinnest electrode widths. All five IDTs and two types of reflectors were designed with this common configuration twice in the design of the first mask. In addition, the DART IDT was designed twice with:

- half of the aperture
- twice the length between the IDT and first reflector
- half of the length between the IDT and first reflector
- one fifth of the length between the IDT and first reflector
- four sets of finger pairs in the IDT
- eight sets of finger pairs in the IDT

The DART, Hanma, Lewis group type and Yamanouchi were also designed with half the length between the IDT and first reflector. Finally, a standard IDT with the common configuration was designed in two 90° arrays with a step of ten degrees to span 180° in total. In this way, both the zero and ninety degree SAW devices were designed twice. In total, 43 devices were designed on the first mask, which can be seen in Fig 14. All IDT fingers end 2 µm away from the beginning of their opposing fingers and there are gaps of 2 or 4 µm between fingers, depending on the design of the IDT or reflector.

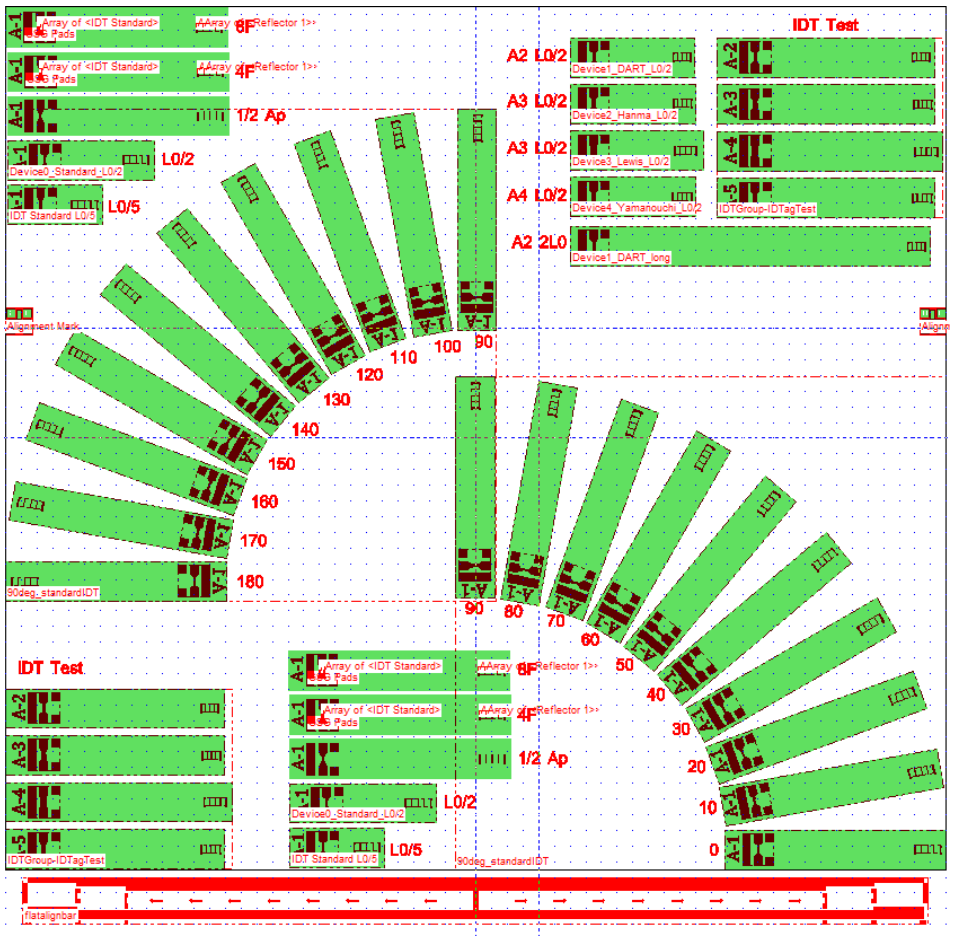

Fig 14 Mask design for first fabrication runs. A1 is standard IDT, A2 is DART SPUDT, A3 is Hanma, A4 is Lewis and A5 is Yamanouchi. 8F means 8 fingers pairs in the IDT, 4F means 4 finger pairs in the IDT, ½ Ap means half the aperture for the IDT, L0/2, L0/5 and 2L0 mean 1/2 , 1/5 and twice the distance between the IDTs and the first reflectors.

The IDTs were labelled next to the bonding pads for easy recognition with a microscope during fabrication. The adapted SAW devices also included extra identifiers, as close to the devices as possible. Two box alignment marks were placed at exactly the same y position and on opposite sides of the mask. An alignment bar was placed at the bottom of the mask design so that the chip could be aligned on top of the wafer to the masks. Fig 15 shows the standard IDT device from the mask design. Fig 16 and Fig 17 are enlargements of the standard IDT, bonding pads and reflector array seen in Fig 15.

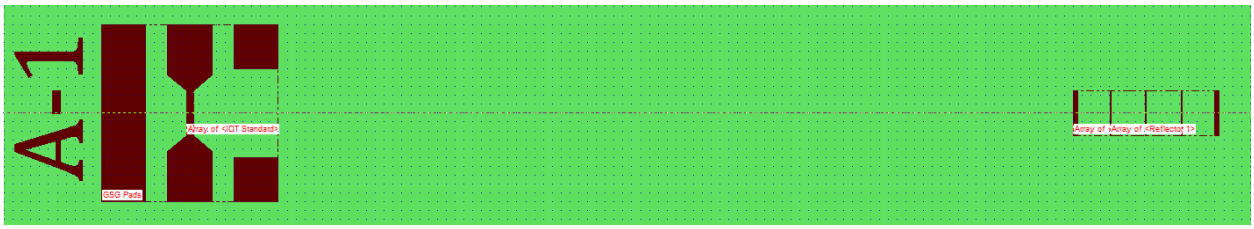

Fig 15 Example of one SAW device with standard IDT and array of reflectors.

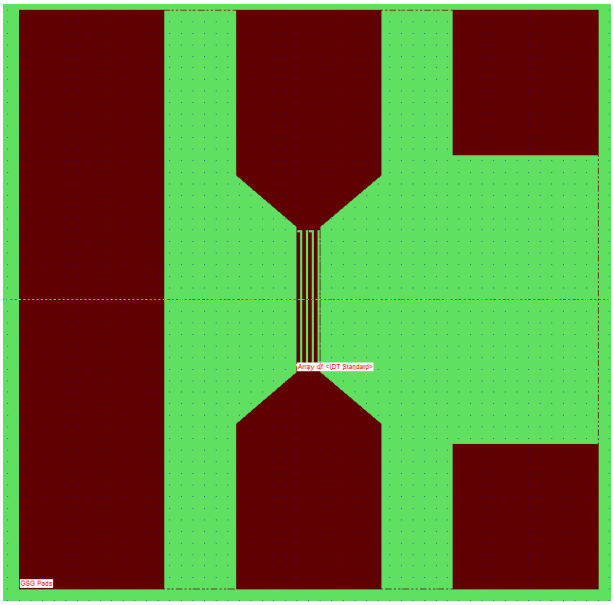

Fig 16 Standard IDT with bonding pads in Clewin mask design.

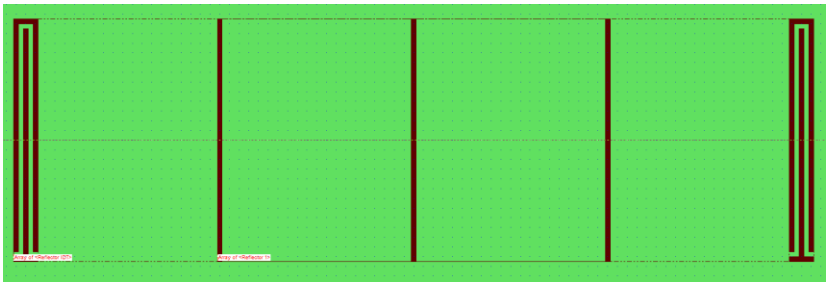

Fig 17 Reflector array for all SAW devices in Clewin mask design.

Fabrication

For the first fabrication runs of the SAW devices, 1.4 by 1.5 cm2 bulk X-cut Y LNO chips were used. Fifteen of these 0.5 mm thick chips were made by SRICO, Inc. The longer side of the chips was the y direction, while the shorter side was the z direction. To better facilitate the fabrication process in the cleanrooms, the chips were glued onto silicon wafers. By doing this, almost no changes needed to be made while using the cleanroom machines. To adapt to the piezoelectric material, any temperature changes within fabrication steps were changed so that the temperature gradient was smaller. The full fabrication process includes the following steps: mask design and fabrication, QuickStick application, oxygen plasma cleaning, photolithography, metallization and liftoff.

Mask Design and Fabrication

In order to do photolithography, masks must be made that will be used to expose designs onto positive or negative photoresists on top of the chips. The mask design was completed in CleWin, a simple mask design software; to see the design, see Fig 14. The CleWin file was doubled checked with the CMi staff for any errors and then converted to be used on the laser lithography system Heidelberg DWL200 in Zone 1 of CMi, shown in Fig 18[2]. The DWL200 takes the design and writes the design with a laser in the photoresist on top of a 5 by 5 in^2 chromium covered glass plate. Once the laser is done exposing the photoresist with the design, the photoresist was developed in a wet bench next to the laser writing machine. After this, the exposed photoresist that was developed was rinsed away in a deionized (DI) water bath and the photolithography part of the mask making was complete. The plate was visually examined to see if there were any large errors.

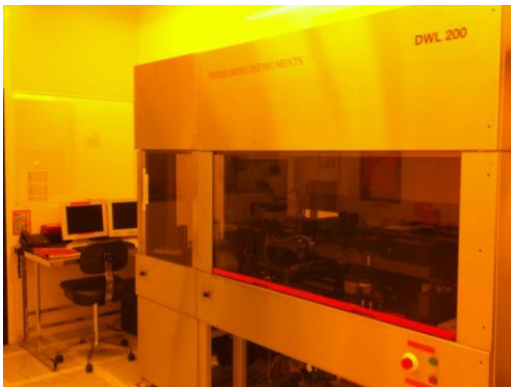

Fig 18 Heidelberg DWL200

The rest of the fabrication process took place at the wet benches in Zone 6 of CMi. To actually create the mask, the plate was placed in a chromium etch bath (acid formula: HCL04 + Ce (NH4) 2 (NO3) 6 + H2O) for 90 seconds to etch the chromium that was not protected by photoresist on the glass. Once the etching was complete, the plate was placed in a quick deionized water tank (QDR) to stop the etching process. After the automatic cycling was complete in the QDR, the mask was rinsed in an Ultra-Clean (UC) Cascade tank with an automatic cycle to thoroughly rinse away the etching acid and chromium. Then the photoresist was stripped in a Technistrip P1316 bath for 10 minutes, then rinsed again with the QRD and UC Cascade tanks. The plate was dried with a N_2 gun and left in the open air of the cleanroom for two hours and was ready for use.

Quickstick Application

To glue the LNO chips to silicon wafers so that fabrication would be more easily done, the Süss RC-8 THP hot plate in Zone 6 of CMi, seen in Fig 19[3], was used to apply QuickStick in between them. After choosing program 19 and double checking that the hot plate temperature was 120°C on the hot plate control pad, a silicon wafer with patterning was placed on top of three spikes that slowly lowered onto the hot plate. The silicon wafer heated quickly to 120°C after coming into contact with the hot plate and a very small amount of QuickStick was applied to the center of the wafer. The LNO chip was placed on top of the QuickStick and softly pushed down to insure good, even contact and a few air bubbles as possible. Once the chip had good contact and was centered as desired on the silicon wafer, the silicon wafer was brought up away from the hot plate and removed to cool slowly on a room temperature surface. The results of gluing are shown in Fig 20. Every effort was made to eliminate air bubbles and evenly coat the QuickStick in between the LNO chip and silicon wafer.


Fig 19 Süss RC-8 THP hot plate shown on the right, underneath the mesh cover.

[2] http://cmi.epfl.ch/photo/home_photo.php
[3] http://cmi.epfl.ch/photo/home_photo.php

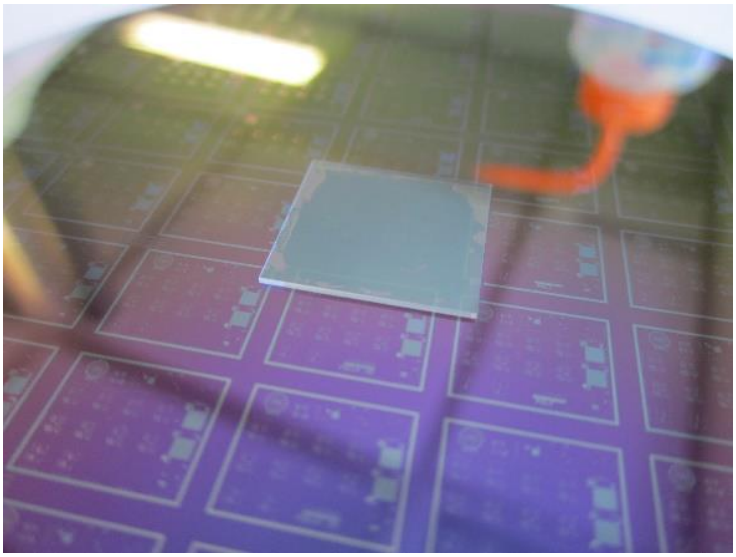

Fig 20 LNO chip on patterned silicon wafer with a layer of QuickStick in between.

0_2 Plasma Cleaning

The surface of the LNO chip was cleaned after gluing or photoresist stripping to provide as clean a surface as possible for photolithography. The Tepla Gigabatch plasma stripper in Zone 2 of CMi, seen in Fig 21[4], included a low power descrum recipe that was used to clean the surfaces. To use the machine, the descrum recipe was selected on the control pad, the wafers with chips facing the inside were placed on the quartz holder, the door was closed, the program ran for five minutes and then the wafers were taken out from the plasma stripper.

Fig 21 Tepla Gigabatch plasma stripper with wafers inside.

Photolithography

The photolithography process was shared between the EVG150 coater and developer system and the Süss MA6/BA6 double side mask aligner in Zone 6 of CMi. Both machines can be seen in Fig 22. During this project, these two machines were used the most in an effort to optimize the patterning of the photoresist for later metallization and liftoff. In order to get good resolution of the design with features of critical dimension 2 µm, an image reversal process was used with photoresist AZ nLOF 2000. In this image reversal process, the negative photoresist was exposed with a negative mask and then baked to later be developed as a positive photoresist. In the end, unexposed photoresist would be removed after development.

For photoresist deposition, the desired program was selected on the computer and the wafers with LNO chips were placed in the left cassette. They were loaded onto the EVG150 by selecting the

[4] http://cmi.epfl.ch/etch/Tepla.php

cassette slots on the computer where the wafers were. Once the program started, each wafer was coated in the photoresist, then spun for 40 seconds, and finally soft baked for 1050 seconds at 115°C.

The exposure was conducted on the MA6/BA6 with hard contact and a 10 mW/cm^2 UV lamp. Top side alignment was done using the alignment bar at the bottom of the mask and the edge of the chip on top of the silicon wafer. The exposure time was tested in multiple exposure runs to find the best developed results.

The image reversal was done in the EVG150 by thermal treatment for 90 seconds at 115°C. The wafers were loaded again onto the EVG150, this time on the right cassette; the development program includes the image reversal treatment. The development is done for 40 seconds with AZ726MIF (an organic developer) and then the wafers were rinsed and dried before returning to the cassette.

Fig 22 EVG150 and Süss MA6/BA6, left and right respectively[5].

Metallization and Liftoff

Fig 23 LAB 600H

After the photolithography was completed with good results, the Leybold Optics LAB 600H evaporator in Zone 4 of CMi, shown in Fig 23[6], was used to metallize the LNO and create the SAW devices. For this project, it was decided to use 10 nm of chromium and 50 nm of gold over 150 nm of Al due to the better conductivity of gold. To use the LAB 600H, the wafers with patterned photoresist on the chips were placed on carrying plates inside the machine. The crucibles of for chromium and gold were checked to insure good quality and the door to the machine was closed after cleaning the O-ring of the door. Once the door with locked with the levers, the program HRN-Cr-Au was selected and the thicknesses for chromium and gold were written in kÅ. The program took one and a half hours to complete and then the wafers could be taken from the LAB 600H.

The liftoff process occurred at the wet bench in Zone 13 of CMi. Because of the fine structures on the chips and the QuickStick gluing, SVC-14 photoresist stripper was chosen for the liftoff. The wafers that had been metallized were placed in tall glass containers filled with the photoresist stripper fluid and left overnight to gently liftoff the photoresist from the chip surface while

[5] http://cmi.epfl.ch/photo/home_photo.php
[6] http://cmi.epfl.ch/thinfilms/home_thinfilms.php

leaving the SAW devices. An ultrasound bath was used at the end, while the wafers were inside the glass containers, to maximize the success of the liftoff. Then the wafers were rinsed gently with a DI water gun and dried with a N_2 gun.

After two exposure tests, it was decided to metallize the backsides of the LNO chips to provide a surface with consistent reflectivity. To do this metallization, LNO chips were covered in a thick layer of photoresist and removed from silicon wafers that they had been glued to by using the RC-8 hot plate. The QuickStick was softly removed from the backside of the LNO chips and then the chips were taped to clean silicon wafers, shown in Fig 24. The LAB 600H was used to evaporate 100 nm of aluminum onto the chips, in the same process described above for chromium-gold evaporation. After the metallization was complete, the chips were removed from the silicon wafers and glued with QuickStick to clean silicon wafers with a metallized patterning. The thick photoresist was stripped using SVC-14 in tall glass containers in an ultrasound bath for 25 minutes.

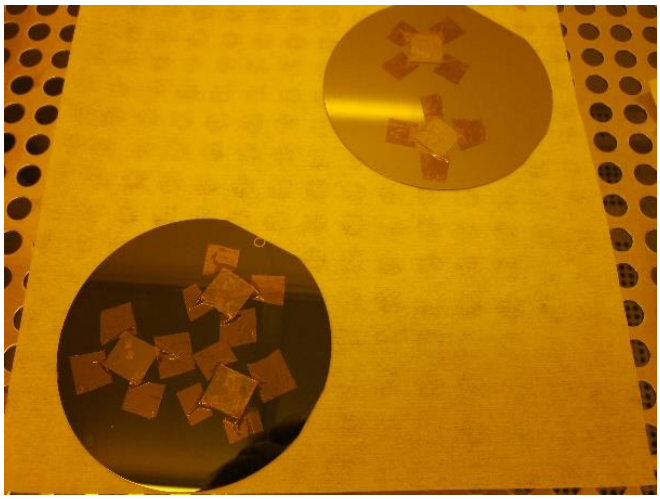

Fig 24 Chips taped to silicon wafers for aluminum metallization of chip backsides.

Results

Mask Fabrication

Three masks were made during this project for fabricating the SAW devices. First, two positive masks were made for metallization and wet etching. The positive masks had chromium everywhere but where the SAW devices were. The wet etch mask was for a possible later fabrication step, where the SAW devices would be isolated from each other by etching away the material in between them. The positive metallization mask was made due to the mistaken belief that a positive mask had been needed during the photolithography process. However, because an image reversal process was being used in the photolithography, the positive mask was the opposite polarity needed. This mistake was not discovered until after the first exposure test and the first full fabrication run. A third, negative mask for metallization was fabricated after the mistake was discovered and was used for the second and third exposure tests and second full fabrication.

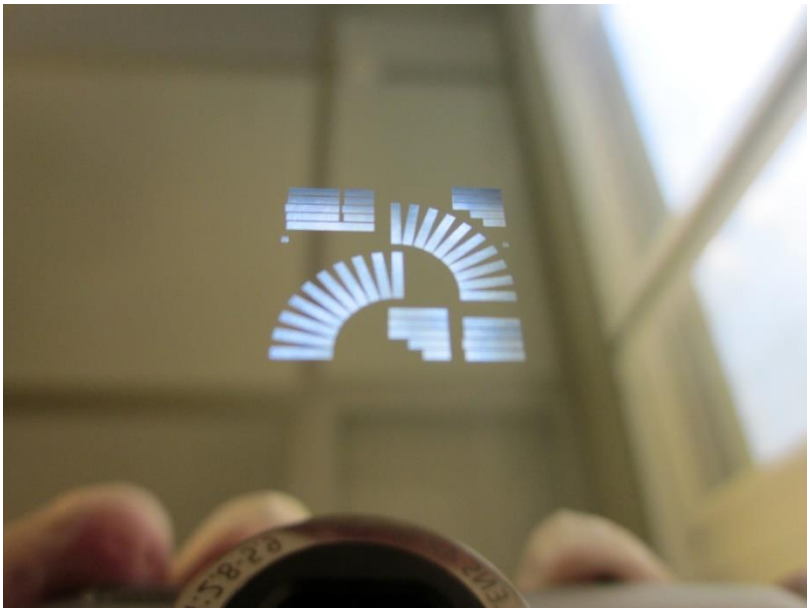

Fig 25 Positive Mask for Wet Etch

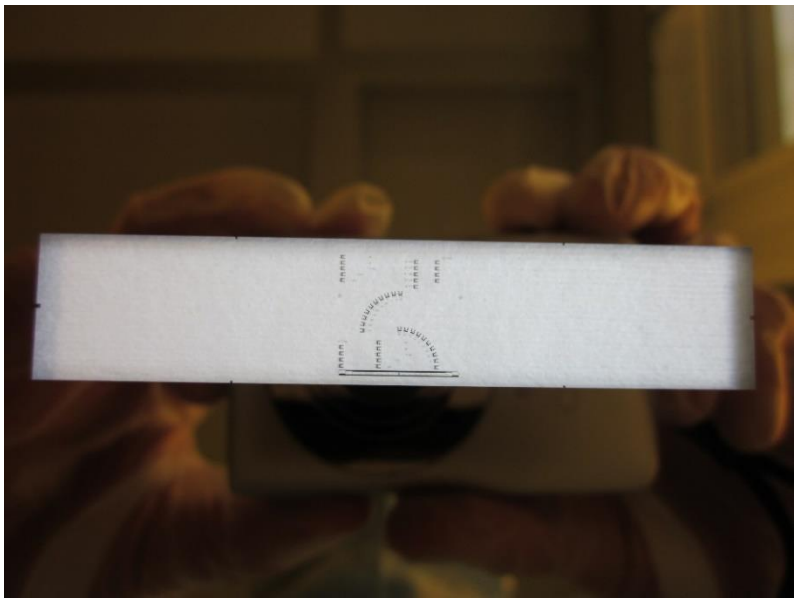

Fig 26 Negative Mask for Metallization

Fig 25 is the positive mask for wet etching and Fig 26 is the negative mask for metallization. It was nearly impossible to take a photo of the positive mask for metallization due to high reflectivity and so has not been included in this report. In Fig 25, one can see metal everywhere except where the designs for the devices are on the positive mask, while the negative mask has chromium just where the devices are and the metal was etched away otherwise in a large rectangle on the mask. In order to reduce the laser writing time for creating the negative mask and since not all of the chromium needed to be taken away on the plate for the SAW devices' fabrication, starting and ending points were provided in the mask design for the laser write to know when to start and stop exposing the photoresist.

The polarity was good on the negative mask for the photolithography but the negative mask was mirrored on the x-axis compared to the positive mask. Therefore, left became right and vice versa. Also, it was seen that in the mask, even though our design was 2 µm for the gaps in between the electrodes, the masks created gaps that were larger than 2µm. Fig 27 shows two examples of where the gap widths are larger than the electrode widths in the IDTs in the negative mask for metallization. There were other errors on the masks, but these were due to errors in the mask design, not the fabrication.

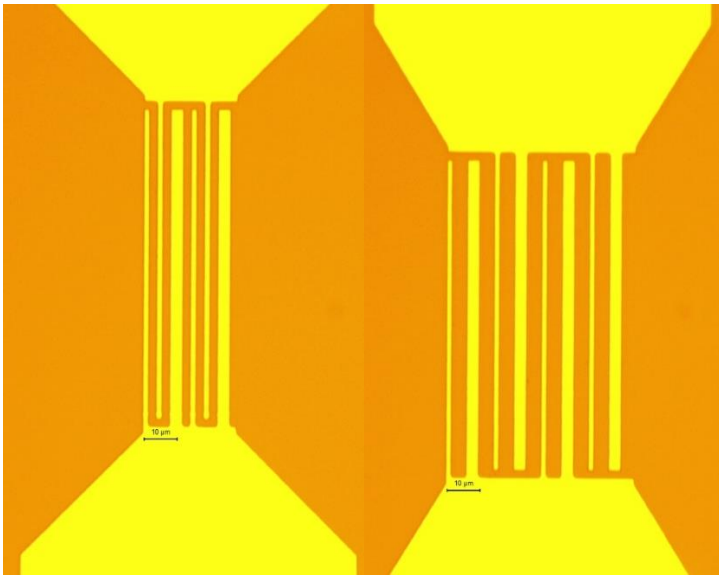

Fig 27 SAW DART and Hanma IDTs in negative mask for metallization.

Profilometer

The Tencor Alpha-Step 500 surface profiler in Zone 15 of CMi was used to measure the surface roughness of the LNO chips. The profile tip went at a speed of 0.1 mm/s across 1 mm of the chip surfaces. The results of the roughness on the top and bottom of a chip can be seen in Fig 28 and Fig 29. The surface roughness of the top side and bottom side is estimated to be ±10 nm with spikes in roughness up to 30 nm. However, these estimates are with data that was difficult to calibrate as well as measure with a good speed and length of measurement.

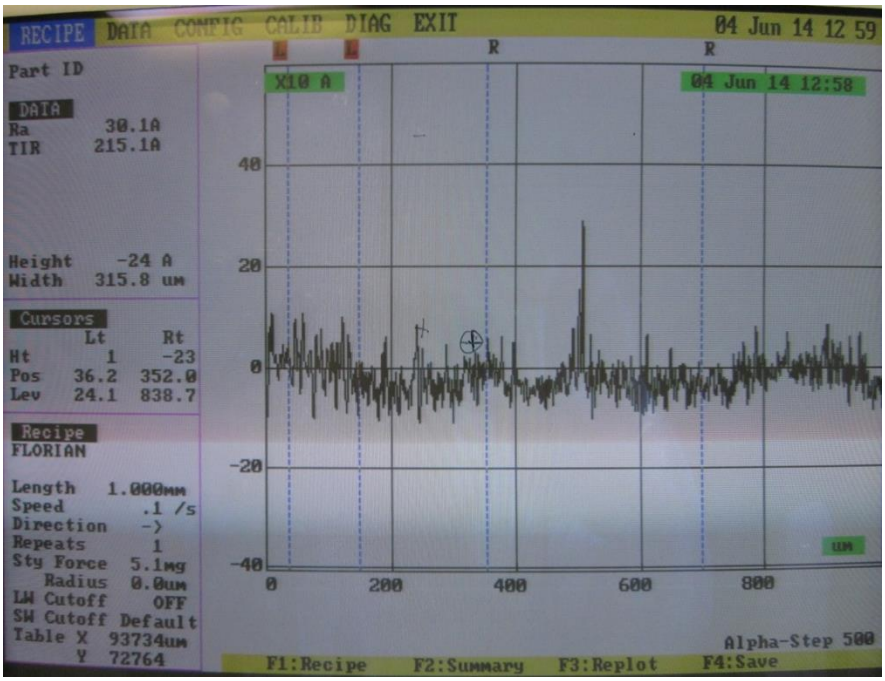

Fig 28 Top side surface roughness of LNO chip

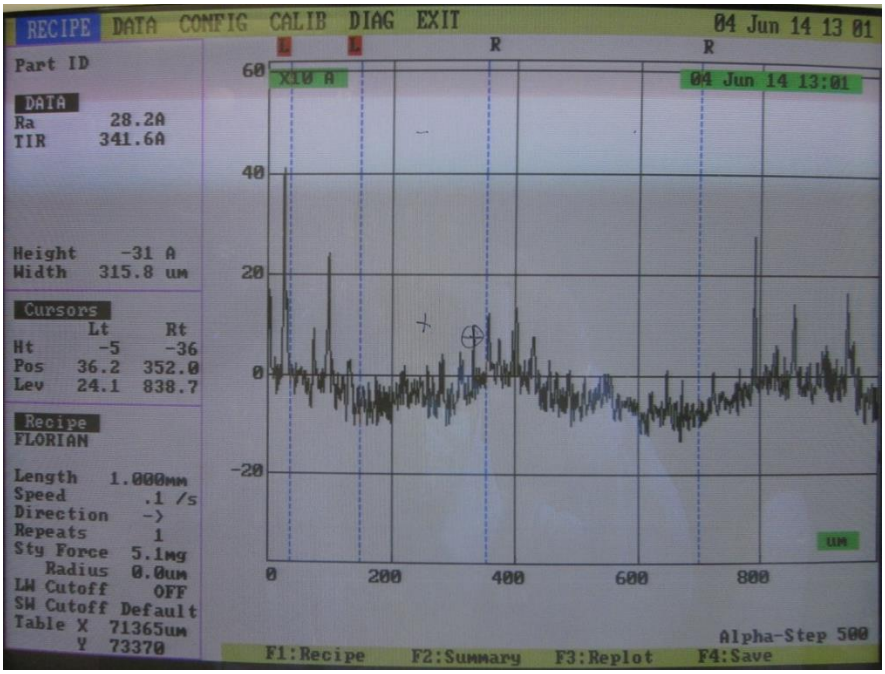

Fig 29 Bottom side surface roughness of LNO chip

Aluminum Evaporation

The results of the aluminum evaporation can be seen in Fig 30. From afar, the coating appears to be even, but at short range, it is clear that the chips were not completely cleansed of QuickStick or photoresist before the evaporation. This caused issues when the chips were placed with QuickStick back onto silicon wafers, because the backsides of the chips were clearly not uniform in height and good contact was difficult to make.

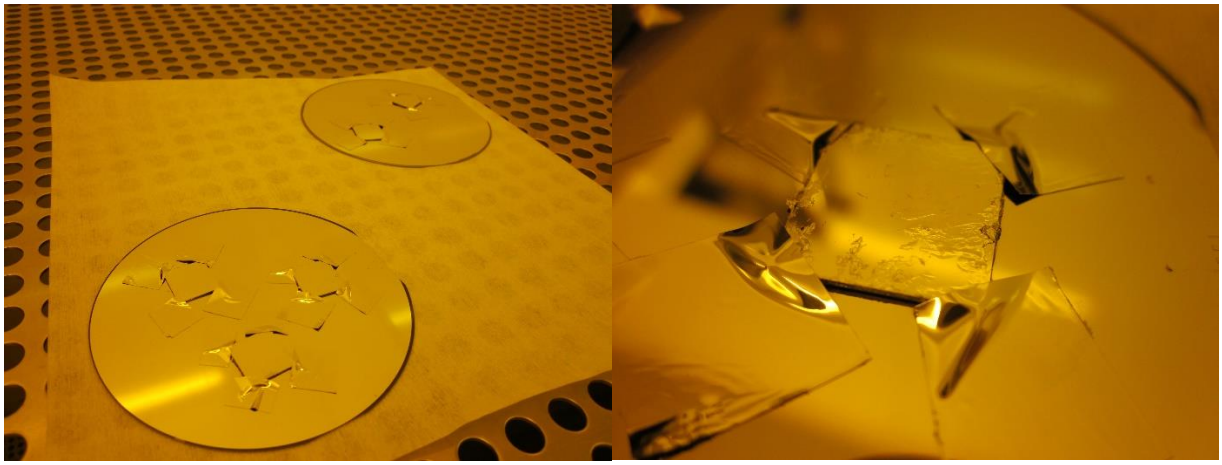

Fig 30 Aluminum evaporation of the backsides of the LNO chips and close up on one chip, left and right respectively.

When the thick photoresist was removed on the front sides of the chips, any photoresist or QuickStick residue underneath the aluminum was removed as well, lifting away the aluminum in the process. Some chips did not suffer as much, as they had been cleaner before metallization, but others lost nearly a fourth of the aluminum on the backside, as seen in Fig 31. In the future, it is clear that the backsides of the chips must be thoroughly cleaned before any metallization can be completed.

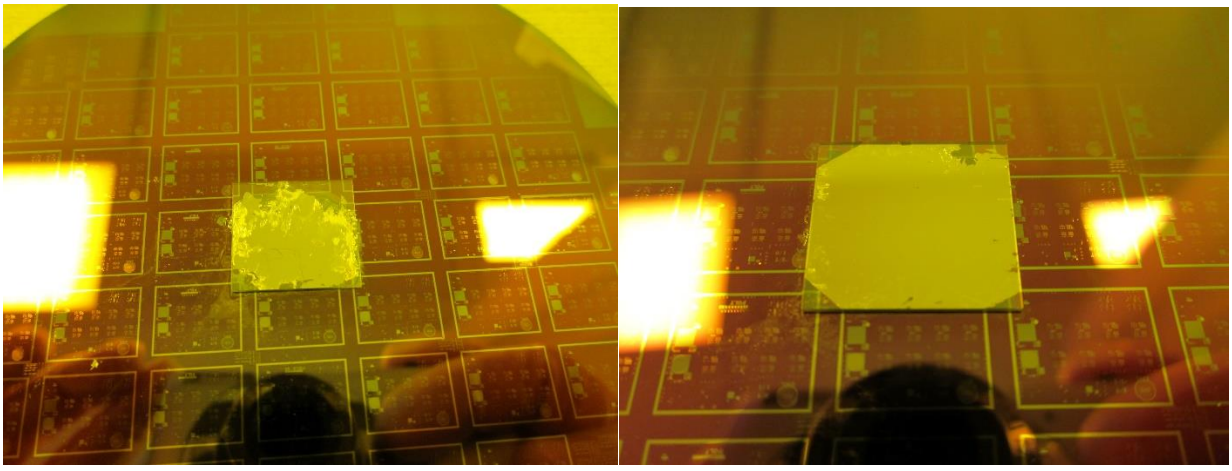

Fig 31 Poor and better quality aluminum metallization results.

Exposure Tests

During this project, three exposure tests were done, where five or six photoresist covered chips were exposed over a range of times to find the best exposure time for the best resolution of the devices. During the formation for the EVG 150, it was found that 4.8 seconds was a good exposure time. However, since the first mask was of the opposite polarity, it was found that several times needed to be tested when working with the second mask and when aluminum had been placed on the backside of the chips. The first exposure run was done to practice using the EVG 150 and MA6/BA6, as well as conclusively shown that the best exposure time for the first mask was 4.8 seconds.

First Exposure Test

Using the positive mask for metallization, six chips were exposed with a time range of 4.2, 4.4, 4.6, 4.8, 5.0 and 5.2 seconds. The overall results were studied and two IDTs were photographed using the microscope to see the differences between each exposure. Below are six images of the standard IDT for the 130° SAW device.

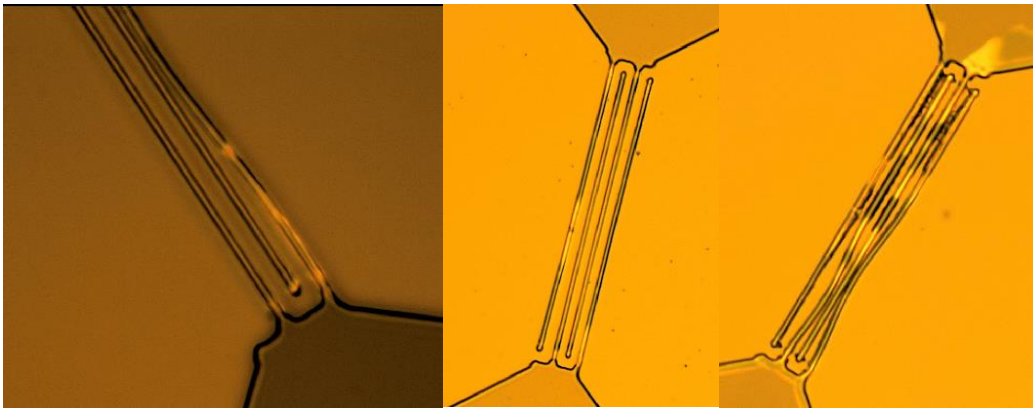

Fig 32 Standard IDT for 130° SAW device with 4.2, 4.4 and 4.6 seconds exposure, left to right respectively.

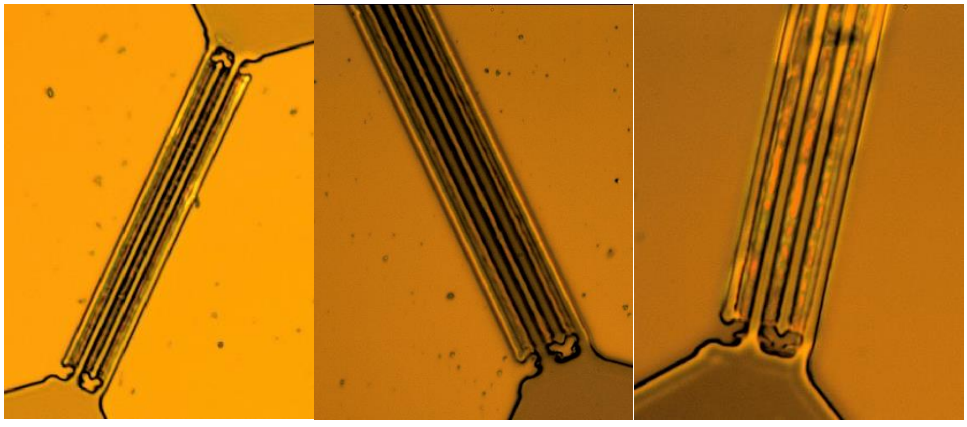

Fig 33 Standard IDT for 130° SAW device with 4.8, 5.0 and 5.2 seconds exposure, left to right respectively.

For all the IDTs in Fig 32, the fingers of the electrodes came out well, although they were thinner than the gaps in between the fingers. In Fig 33, none of the fingers were separate from each other, due to a thin layer of photoresist in between them that. Since this feature of thin photoresist was seen over much of the chips for these exposure times, the photoresist in between the fingers must have become exposed. This is most likely true because during the image reversal process, any unexposed photoresist is taken away during development. Six images for the Lewis IDT in the bottom left corner of the chips are provided in Appendix 1; in the case of the Lewis IDT, the tiny features of the IDT lead to poor development results no matter what the exposure. However, there were still better results for the shorter exposure times than the longer ones.

Second Exposure Test

This exposure run was with the negative mask for metallization, the correct mask to use for the image reversal process. Six times were tested: 4.5, 4.6, 4.7, 4.8, 4.9 and 5.0 seconds. Fig 34 and Fig 35 show a standard IDT for each exposure time. Due to the small differences between each exposure time, there are few differences between the images. One feature that can be noted is the tips of the fingers for the IDTs. The tips lose their roundness and grow darker as the exposure time increases, which may be due to photoresist staying there after development. However, this may be a good feature because the lower exposure time IDT fingers are too long, while the longer exposure times are shorter due to less rounding. There should be 2 microns between the end of the finger tips and the beginning of the opposing fingers, but this is not the case in any of the IDTs shown below or in the IDTs shown in Appendix 2.

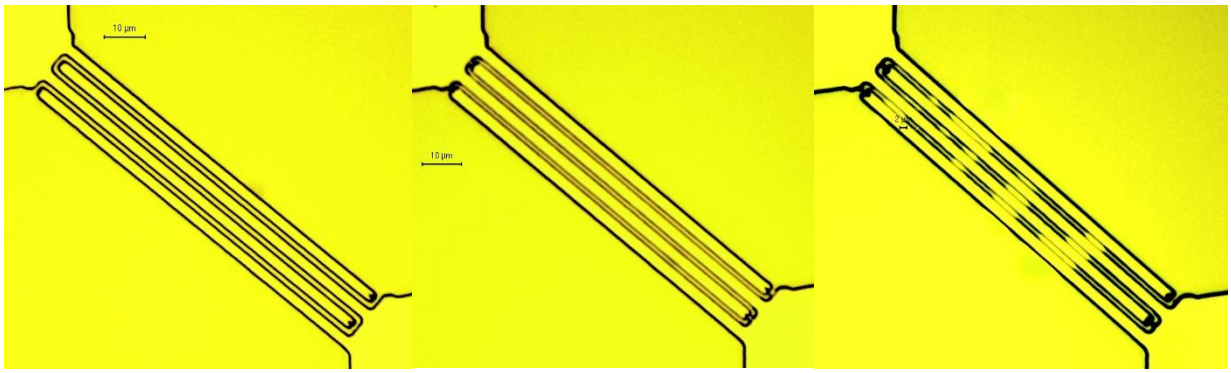

Fig 34 Standard IDT for 130° SAW device. Exposure times of 4.5, 4.6 and 4.7 seconds, left to right respectively.

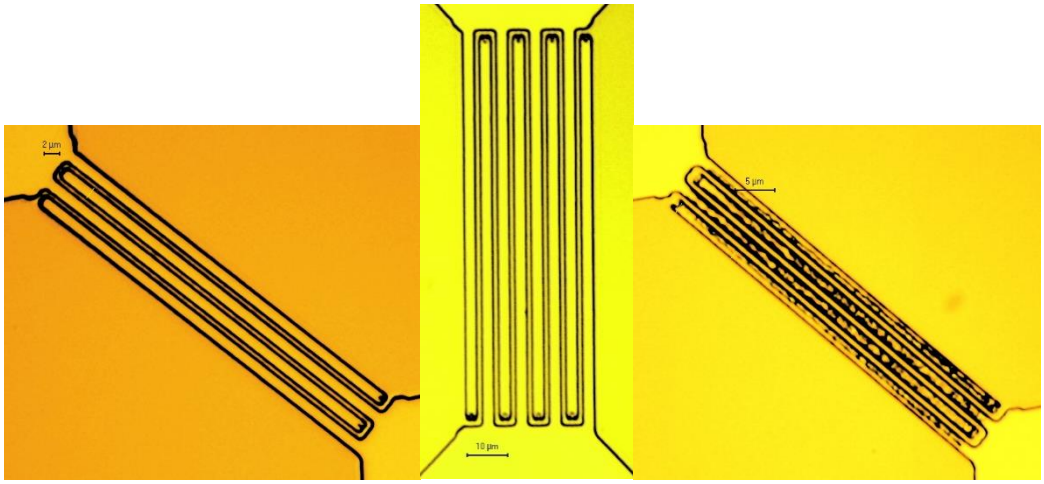

Fig 35 Standard IDT for 130° SAW device in left and right images for 4.8 and 5.0 seconds exposure time. Center image is a standard IDT for a 4 finger pair SAW device.

In Appendix 2, an example of the Hanma IDT on the chips is shown for each exposure time. The same feature of the finger tips not rounding and becoming darker is also in these IDTs. Both sets of IDTs show signs of photoresist being left after development inside the electrode openings, suggesting that overexposure occurs at 5.0 seconds and 4.9 seconds for the Hanma IDT. The features that show this are the black regions inside the electrode portions of the IDT design.

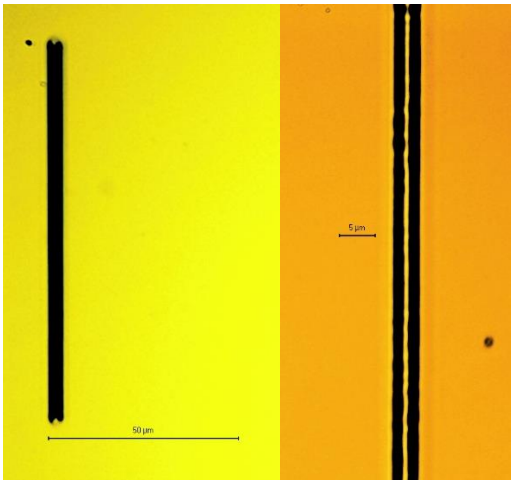

Fig 36 Examples of single reflectors for 4.7 and 5.0 seconds exposure time respectively.

Fig 36 shows some examples of what many of the reflectors look like on all the chips, no matter what the exposure time. Most are black or black with a thin bright center because photoresist is sloping down at an angle to the unexposed region in the center or closing the reflector completely with photoresist. This suggests the exposure times are always too long for the reflectors to be developed.

Third Exposure Test

This exposure test used the negative mask for metallization and chips with the poor layer of aluminum on the backsides. Five chips were exposed with exposure times of 4.5, 4.6, 4.7, 4.8 and 4.9

seconds. Due the poor aluminum layer on the backside of the chips, the results of the 4.5 second exposure were very poor, with very few structures surviving after development. However, the other four chips provided good results of the effect of the exposure time on the quality of the structures. Fig 37 gives an example of the DART SPUDT for 4.6-4.9 exposure times. As the exposure time increased, the quality of the developed design in the photoresist decreased. 4.6 seconds provides the cleanest and highest quality IDT, while for 4.7-4.9 seconds, more and more photoresist is present inside the electrodes after development, suggesting overexposure.

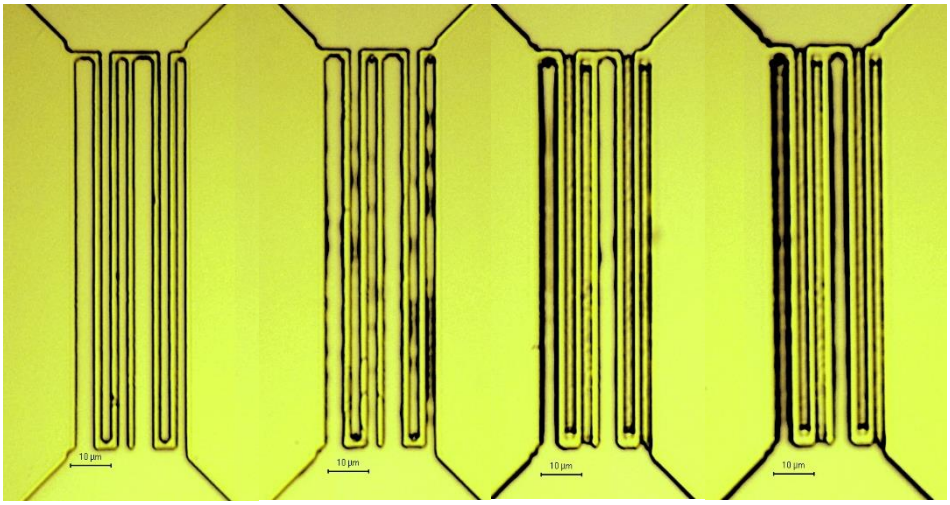

Fig 37 DART SPUDT for top left SAW device for 4.6, 4.7, 4.8 and 4.9 exposure times, left to right respectively.

The only reflectors that survived as a total array on any of the chips was in the top left corner of the 4.6 second exposure chip, shown in Fig 38. There was no aluminum underneath the array, unlike the rest of the arrays that had aluminum beneath them. It may be an outlier, but since most of the other reflector arrays looked like Fig 38, with poor slopes for the walls or the features not coming out clearly after development, it suggests that the aluminum coating did not help with the photolithography of the reflectors.

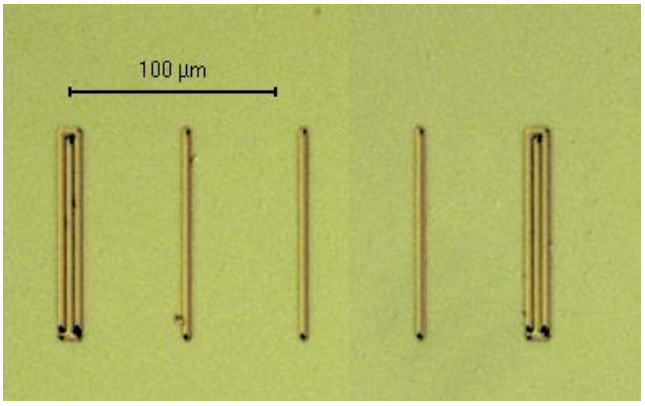

Fig 38 Only reflector array to be developed for all exposure times. In top left corner of 4.6 chip.

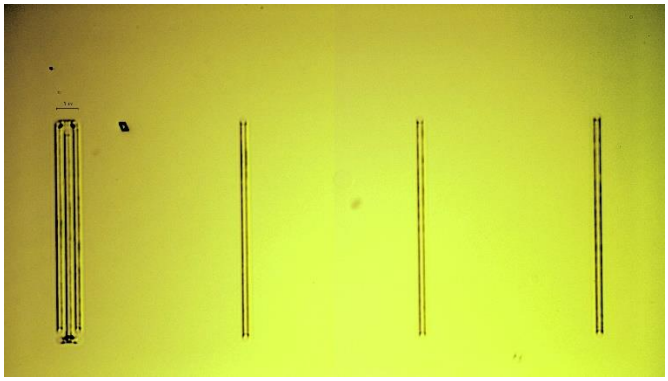

Fig 39 Best reflector array for 4.9 seconds exposed chip.

Appendix 3 includes the Yamanouchi SPUDT for the exposure times 4.6-4.9 seconds. The results for these IDTs are similar to the DART SPUDT.

Complete Fabrication

First Run

The first complete fabrication of the SAW devices was done with the positive mask for metallization, leading to metal being evaporated everywhere but the devices. This was clear before the liftoff was completed, because it was seen that photoresist still protected the devices instead of leaving them open for evaporation. Fig 40 shows the photoresist protecting the IDT fingers instead of surrounding the IDT fingers and bonding pads. After liftoff, the mistake was even clearer. In Fig 41, the results after liftoff are shown. The lighter orange area is gold, while the darker orange areas are LNO. This is the opposite of what had been desired during fabrication.

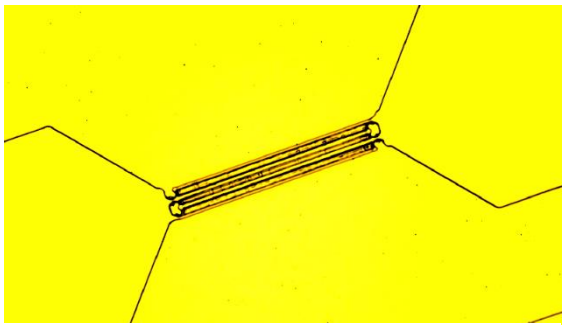

Fig 40 First metallization, before liftoff. Gold is everywhere except where photoresist is.

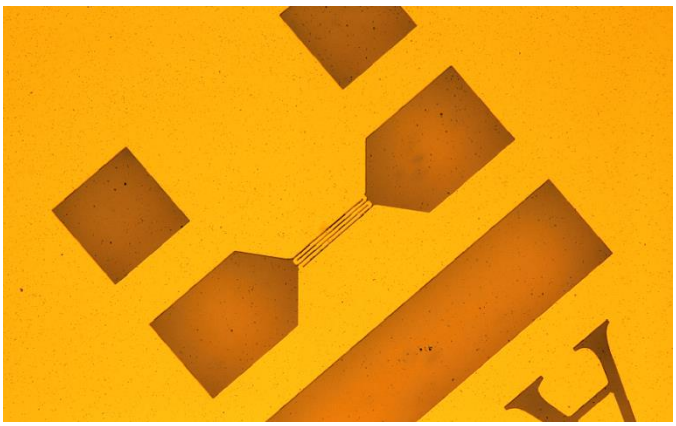

Fig 41 First metallization, after liftoff. Darker orange areas are openings empty of gold.

Second Run

In this run, the backsides of the LNO chips had been poorly metallized with aluminum and the photolithography was therefore not as good in resolution of the devices. Out of the third exposure test, the chips exposed for 4.6 and 4.7 seconds were metallized. The results of the second fabrication run were somewhat successful, at least in terms of some of the IDTs. As was seen even in the exposure test, most of the reflectors had not come out at all and did not metallize. The only array of reflectors to come out after liftoff were in the top left corner of the 4.6s chip, shown in Fig 42. There was no aluminum on the backside of the chip here. Although the gaps in-between the IDT reflectors are not the same size as the metallized lines of the IDT reflectors, the profile is still very good.

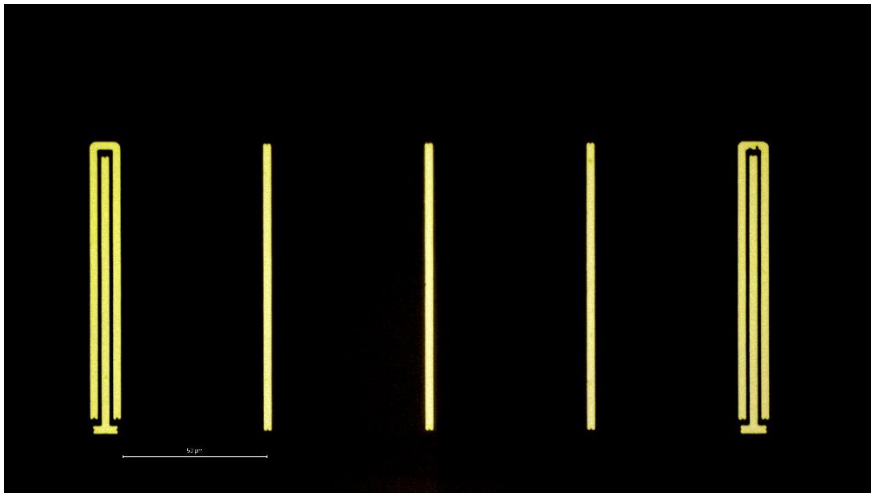

Fig 42 Array of reflectors from 4.6 seconds exposed chip.

For the 4.6 seconds exposed chip, nearly none of the reflectors came out. Most IDTs also were not present or badly metallized. Fig 43 shows the complete absence of a standard IDT and a poor Lewis IDT. The photolithography is largely to blame for the results. For example, the black line across the Lewis IDT below means that a small line of photoresist had lifted off and moved to be on top of the other photoresist lines, shielding the metal from reaching the LNO chip surface.

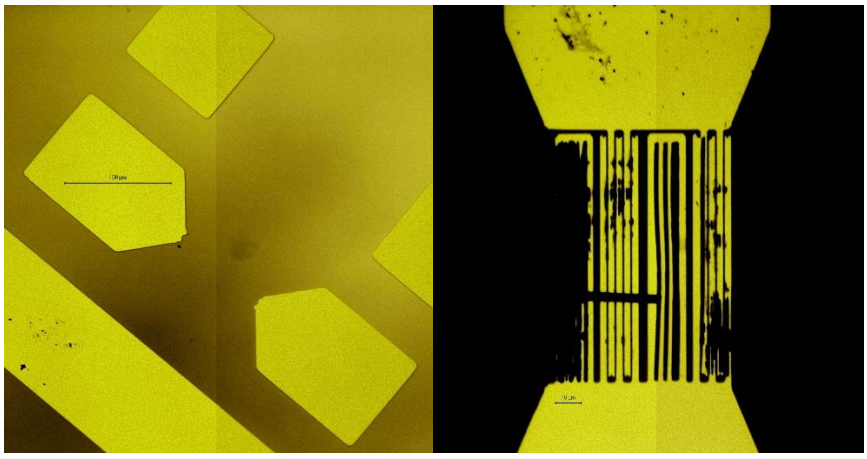

Fig 43 Absence of a standard IDT entirely and a badly metallized Lewis SPUDT, left and right respectively.

The 4.7 seconds exposed chip showed even poorer results than the other chip. The only array of reflectors that were reasonably good are shown in Fig 44. Not even the IDT reflectors came out completely and the simple reflectors are barely present. For most of the SAW devices, the reflector array is not present at all.

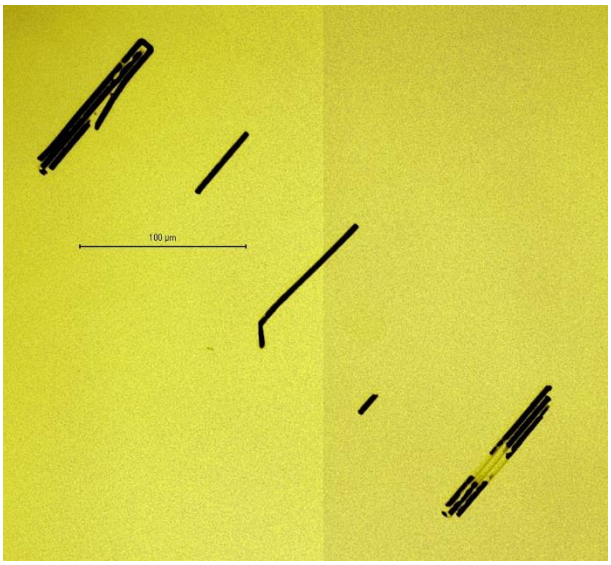

Fig 44 Best array of reflectors from 4.7 seconds exposed chip.

All of the IDTs on this chip were imperfect in some way. Most had black lines covering portions of the fingers, parts missing from the fingers or interesting black patterns across the entire IDT. The standard IDT shown in Fig 45 was one of the best IDTs on the chip, while the rest of the IDTs looked more like the Hamna SPUDT and Yamanouchi FEDUT in Fig 45. Many IDTs did not come out after the liftoff, like seen in Fig 46.

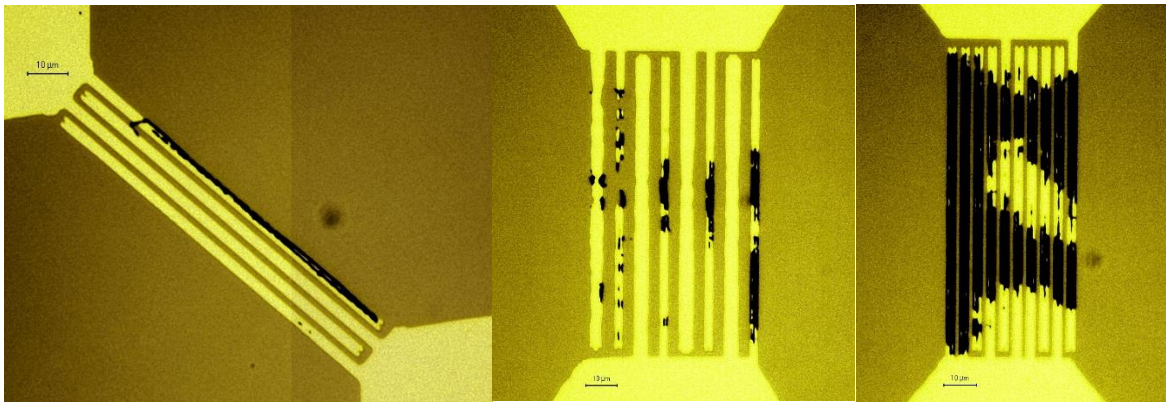

Fig 45 Examples of a standard IDT, a Hamna SPUDT and a Yamanouchi FEUDT on the 4.7 seconds exposed chip.

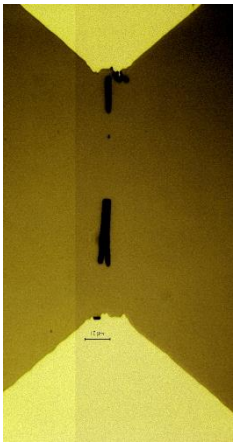

Fig 46 Standard IDT that did not come out after metallization.

Discussion

For the mask fabrication, the results show that the translation between the mask design and the final product was not perfect in terms of correctly defining the gaps between the IDTs and IDT reflectors. As seen in Fig 27, the gaps in between the electrodes were always greater than 2 µm. Therefore, because of the image reversal, our gaps in the photolithography results were always less than 2 microns. However, this may due to overexposure during the photolithography process or to optical effects in the microscopy when trying to image small features and not the mask fabrication.

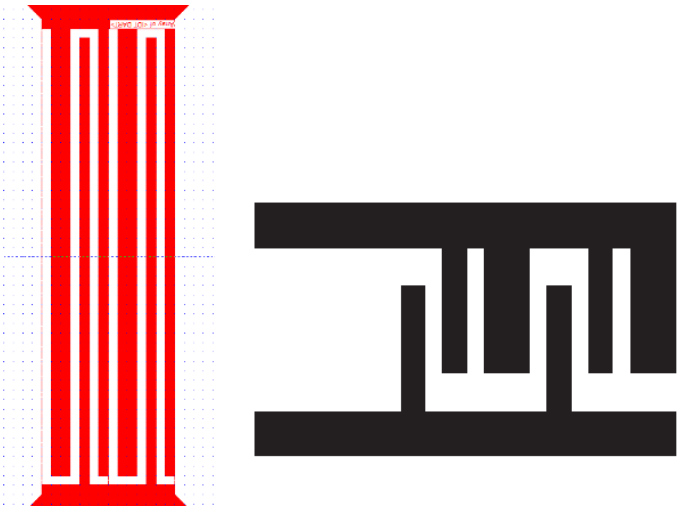

Fig 47 Comparison between mask design of DART SPUDT and design from [4] of a DART SPUDT.

The mask design also contained several errors that should be corrected if it is used to create a mask in the future, including an incorrect design of the DART SPUDT. Although the mask design may still produce a SAW wave, it will most likely behave differently than one produced by the design from literature. Since the design from literature produced good SAW results, it would be best to simply correct the mask design for the best chance of good quality SAW devices.

Based on the results of the third exposure test with the aluminum metallization on the backside of the chips, aluminum is perhaps not necessary on the backside of the chips. At the very least, it would be better to more evenly metallize the chips or provide an opaque surface on the silicon wafer. It may not

seem necessary to have an even reflective surface, but it probably would provide more consistent results with the photolithography than was seen in the exposure tests discussed in this report.

As for the exposure tests, there are many things to remark upon. Most importantly, 2 µm as a starting point of designing the electrodes was probably overambitious, due to having to deal with the transparent LNO chips, reflections, maybe poor photoresist evenness on the chip, and other issues during photolithography. Also, the poor quality of the reflectors throughout the test means that the current procedure is probably not good for fabricating them. Many times, the angles of the photoresist walls are so much that there isn't any open, unexposed area, which makes it impossible to metallize and liftoff. This means that in general, the reflectors are always over-exposed. It's possible that the fabrication of the IDTs and the reflectors must be done separately, with completely separate photolithography procedures or at least parameters that are adapted to best fabricate one or the other.

In each exposure tests, all the chips had regions of poor and good results randomly dispersed. This may be due to poor coating of the photoresist; the EVG 150 is not optimized for coating uneven surfaces such as silicon wafers with chips glued on top. The QuickStick in between the LNO chip and the silicon wafer may also be uneven, leading to an uneven photoresist coating, bad contact with the mask during exposure or changes in reflectivity in different regions of the chip.

When looking at the results of the photolithography tests with a microscope, some reoccurring features were present. One was generally poor reflectors, most likely due to over-exposure. Another was angled walls of photoresist in the IDT fingers or reflectors. These can be due to over-exposure or bad baking times for the image reversal process. Black lines in the center of IDT fingers or reflectors may be photoresist that wasn't developed enough or rinsed away after development. Finally, thin layers of photoresist at the bottom of IDT fingers or reflectors were often seen, suggesting overexposure of the photoresist so that the photoresist at the bottom of these features were exposed and therefore not taken away during the image reversal process.

Conclusion

In this project, a thorough study was made of SAW devices by researching papers and books on the subject. The theory of SAWs, piezoelectric materials, IDTs and modelling SAW devices was read in an effort to understand the mechanisms behind these devices. Although a complicated subject, enough was understood to design a mask with several different interdigital transducers, two different reflectors and a variety of adaptions to the length, aperture and angle of propagation of the SAW devices. With the help of the CMi staff, the process flow was optimized for fabricating the devices. Three exposure tests were made to optimize the photolithography portion of the fabrication. In the end, two chips were fabricated with several good quality IDTs and a few good reflector arrays.

In the future, much work could be done to improve upon the understanding of the theory, the design of the SAW devices and their fabrication. The modelling of SAW devices needs to be understood and implemented in order to have calculated results to compare to the experimental results. It is important to thoroughly go through the mask and correct any mistakes that were discovered during the fabrication portion of this project. Also, the photolithography and aluminum metallization of the backsides of the chips still needs optimization. It should be determined whether an aluminum backside is the best option for reducing reflectivity unevenness. The cleanliness of the top side of the chips before and after photolithography is an important thing to watch in the future. Should another mask be made in the future, over-etching should be kept to a minimum to have the best gap widths.

If the suggested items in the previous paragraph can be met, then a full fabrication run can be completed to try to produce good quality SAW devices for characterization. Once characterization and analysis can be made of the results, the best IDTs and SAW device parameters can be found. Then more

SAW designs with temperature sensors or ID tags could be fabricated and tested to see the quality of SAW devices as sensors. Finally, should all the above conditions be met, smaller than micron devices could be fabricated with the best quality photolithography possible or electron beam lithography. However, the surface roughness should be measured accurately to see if at any point the SAW device features will reach the same size as the surface roughness.

Several important features of the project could not be tested in the end due to lack of time, including fabricated temperature sensors and testing the quality of devices that had been isolated from each by etching away material in between them versus devices fabricated in the process described in this report. It is possible that the isolated devices will operate much better, due to not receiving stray SAWs from other devices on the same surface. Finally, it was desired to test thin film LNO chips to see if they would provide the best results for SAW devices.

I gained much experience and knowledge while working on this project. In terms of cleanroom experience, I learned how to use Clewin and all the machines necessary for the fabrication process. Not only did I learn to use them, I also learned how to deal with any problems myself instead of being assisted by a PhD student in charge of my project, instead figuring out how to get advice from cleanroom staff and other friendly cleanroom people. I learned better from whatever mistakes I made because I learned how to correct them myself, not by watching an assistant do it. I especially improved my experience with the microscope. Taking good quality, descriptive pictures is important because good documentation requires good evidence of what you've done, how you did something, and why something happened that way. The project didn't go as far as desired, but I felt that I personally grew much more confident in my abilities as a researcher and now know more of my limitations. The project was a learning experience. There was some success with the fabrication, but it was more important for me to learn all about a MEMS device than having a huge success.

I also learned how hard working in a cleanroom is. There are always complications and things that go wrong, even when you personally do everything right. Working with LNO was especially hard because it is transparent and piezoelectric. Doing the fabrication was even harder with this material than it would have been with silicon. Things always take longer than you think to get done because you couldn't book the right machines in time or something went wrong or everything went right in the fabrication but the results are poor. You can try to outline a project plan or fabrication procedure, but it almost never works out how you think it will. These were all great lessons to keep in mind for my future projects.

I want to thank Professor Guillermo Villanueva for offering this project and his patience and good advice throughout the project. Florian Bienefelt was an excellent partner to work with on this project. I also would like to thank CMi, in particular Georges-André Racine, for their assistance in the fabrication of the devices. Finally, I would like to thank LMIS1 for allowing me to conduct a semester project in their laboratory.

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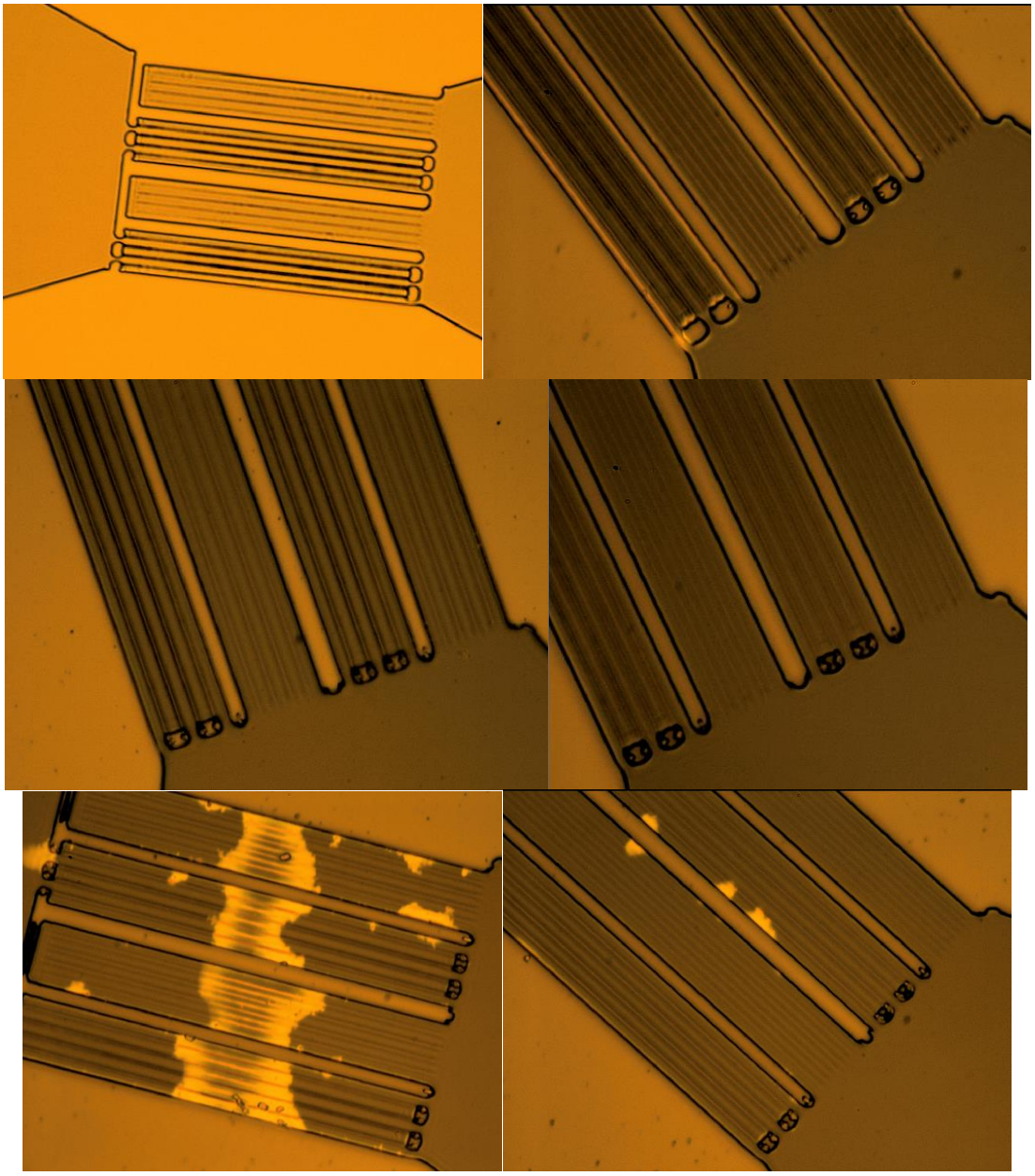
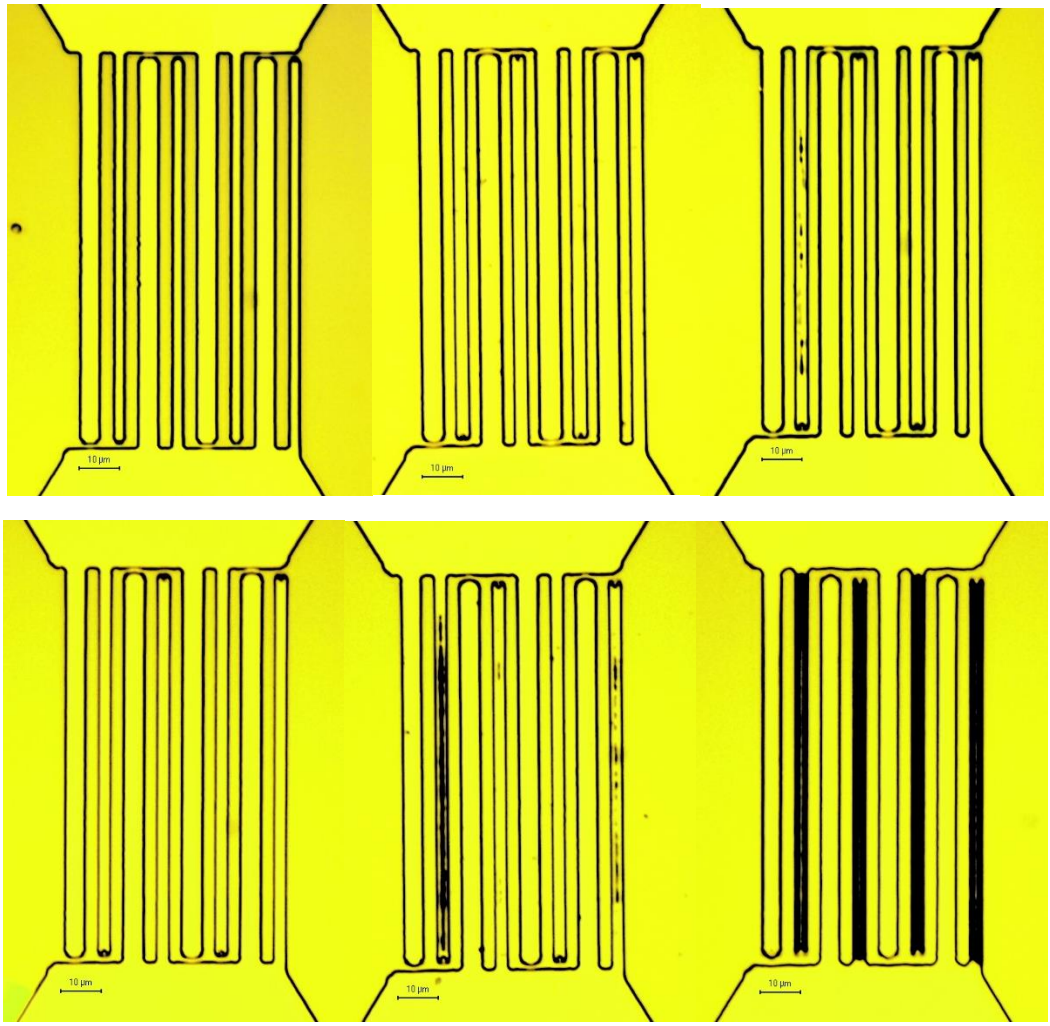
Appendix 1



Figs 1-6 First exposure test. Lewis SPUDT in bottom left corner of chips. Exposure times of 4.2 and 4.4 seconds in top row, 4.6 and 4.8 in the second row and 5.0 and 5.2 in the third row.

Appendix 2



Figs 1-6 Second exposure test. The Hanma SPUDT for the top left SAW device. Exposure times of 4.5, 4.6, and 4.7 seconds in the top row and 4.8,4.9 and 5.0 seconds in the second row.

Appendix 3

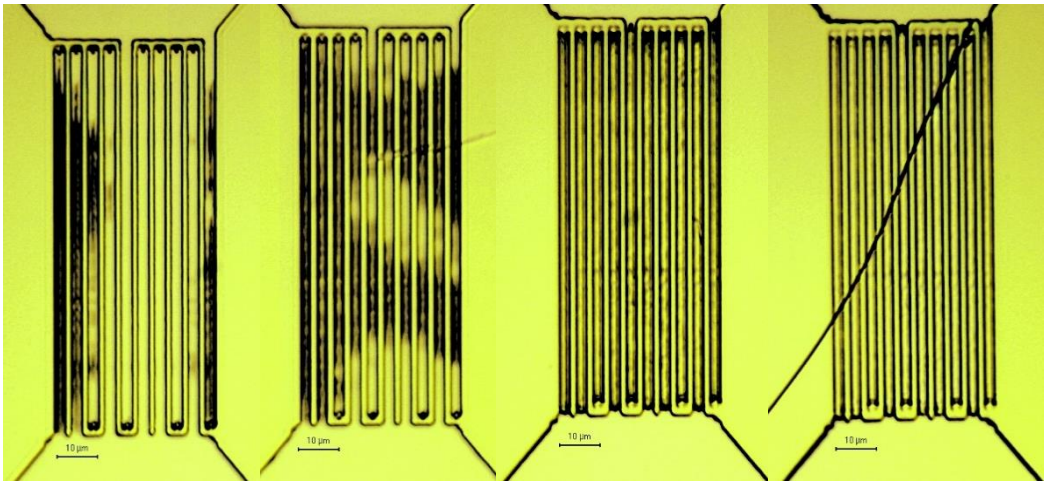


Fig 1-4 Third exposure test. The Yamanouchi SPUDT for the top left corner SAW device. Exposure times of 4.6, 4.7, 4.8 and 4.9 seconds from left to right respectively.