Enhanced Electrical Performance and Heat Dissipation in AlGaN/GaN Schottky Barrier Diodes Using Hybrid Tri-anode Structure

Jun Ma, Giovanni Santoruvo, Pulkit Tandon, and Elison Matioli

***Abstract*— Enhanced performance in AlGaN/GaN Schottky barrier diodes (SBDs) is investigated using a nanowire hybrid tri-anode structure that integrates three-dimensional Schottky junctions with tri-gate transistors. The fabricated SBDs presented an increased output current density with improved linearity, above 1 A/mm at 5 V when normalized by effective anode width, over 3 orders of magnitude lower reverse leakage current and superior heat dissipation. The sidewall Schottky contacts reduced the turn-on voltage and eliminated the non-ideality caused by the AlGaN barrier. The large surface area of tri-gate architecture greatly enhanced heat dissipation and largely reduced the average temperature as well as thermal resistance of the integrated tri-gate transistors. The trench conduction near SiO_2/GaN interface, formed under forward bias at both sidewalls and bottom of nanowire trenches, compensated part of the self-heating degradation and improved the output linearity of the device. Optimal design for the tri-anode structure, based on a model of critical filling factor, was proposed to surmount the issue of partial removal of two-dimensional electron gas (2DEG), unveiling the potential of nanostructured GaN devices to achieve comparable or even larger output current than counterpart planar devices.**

***Index Terms*— AlGaN, GaN, nanowire, tri-gate, tri-anode, self-heating, trench conduction, filling factor, Schottky diode, HEMT.**

I. Introduction

GaN is one of the most promising candidates for future power electronics. Given the large band-gap, superior breakdown field strength and excellent electron saturation velocity, GaN power devices can operate at high temperature, high voltage and high frequency, enabling efficient and compact power management as compared to the conventional Si technology [1-4]. Among GaN power devices, Schottky barrier diodes (SBDs) are an important member with wide applications in power converters. However, conventional AlGaN/GaN SBDs suffer from high turn-on voltage (V_{on}) and large reverse leakage current (I_R). A large effort has been devoted to address these challenges, but common technologies proposed to mitigate on-state (off-state) challenges tend to degrade off-state (on-state) performance [5-7]. In addition, self-heating is another major issue that hinders the performance of GaN SBDs as well as transistors [8], since high temperature degrades significantly the performance, efficiency and reliability of the devices. Engineering of heat dissipation is therefore highly desirable for miniaturization and densification of these devices.

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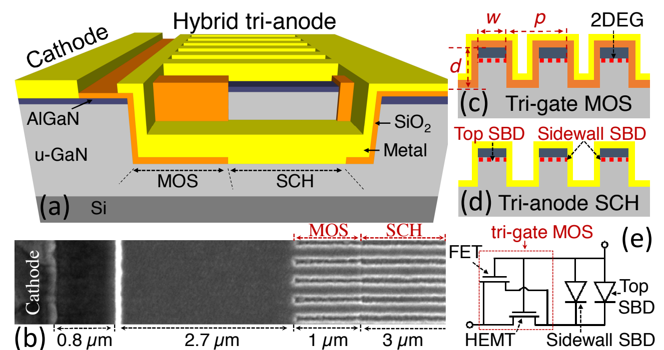

Fig. 1. (a) Schematics of the hybrid tri-anode SBD; (b) top-view SEM observation; cross-sectional schematics for (c) tri-gate MOS and (d) tri-anode Schottky (SCH) regions; (e) equivalent circuit of the hybrid tri-anode SBD.

A hybrid tri-anode structure has been recently proposed for AlGaN/GaN SBDs, resulting in reduced V_{on}, improved ideality factor and ultra-low I_R [4]. In this work we investigated the electrical enhancement in hybrid tri-anode SBDs and demonstrated further advantages in forward characteristics such as large output current density, better linearity and improved heat dissipation of this architecture. Enhanced output current density (I) with improved output linearity were achieved with a hybrid tri-anode structure due to the sidewall Schottky contact, enhanced heat dissipation and additional trench conduction channels near oxide/GaN interface. Schottky junction formed at nanowire sidewalls reduced the V_{on} and eliminated the non-ideal behavior observed in planar SBDs. The self-heating was minimized by the nanowire trenches which largely reduced the thermal resistance of the integrated tri-gate transistors as compared to the counterpart planar devices. Conduction channels at the SiO_2/GaN interfaces were found to form at not only sidewalls but also trench bottoms with increasing forward bias, which improved the output linearity of the device. This observation challenges assumptions from previous studies where only sidewall conduction is present in

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such geometry, as discussed later in this paper. Optimal tri-anode design was discussed based on a critical filling factor model, which could be generally applied to other GaN nanostructure-based approaches such as tri-gate, Ω-gate, Fin-shaped, nanochannel array and multi-mesa-channel transistors [9-14].

II. Device Structure

The AlGaN/GaN epi in this work consisted of 3.3-µm buffer, 1.2-µm un-doped GaN (u-GaN), 18-nm $Al_{0.26}Ga_{0.74}N$ barrier and 2-nm u-GaN cap layers. Schematics and scanning electron microscopy (SEM) observation of the 100-µm-wide tri-anode SBDs were shown in Fig. 1. The device fabrication started with mesa etching by Cl_2-based inductively coupled plasma (ICP), followed by metal deposition (Ti/Al/Ni/Au) and ohmic thermal annealing. The AlGaN/GaN nanowires were defined by interference lithography and ICP etching. The depth (d) of the nanowire etching was 114 nm. The width (w) of a nanowire was 135 nm and the period (p) was 300 nm, corresponding to a filling factor ($FF = w/p$) of 0.45. Then 18-nm SiO_2 was deposited by atomic layer deposition and selectively removed in Schottky and contact regions. Finally the anode was formed by deposition of Ni/Au, integrating three-dimensionally Ni/AlGaN/GaN (top SBD) and Ni/GaN (sidewall SBD) Schottky junctions as well as SiO_2/AlGaN/GaN tri-gate metal-oxide-semiconductor transistors (tri-gate MOS) to form a hybrid tri-anode. Planar AlGaN/GaN SBDs with similar dimensions based on conventional planar MOS and SCH regions were taken as reference.

III. Results and Discussion

Figure 2 shows the I and conductance (G) versus anode bias (V) of the SBDs with planar (Planar) and hybrid tri-anode (Tri-anode) structures, obtained by normalizing the current with effective anode width (w_a). The sidewall metal-to-2DEG contact in the Tri-anode was considered by defining the w_a as $n \times (w + 2b)$, where n is the number of nanowires in a given device and b represents the width of the Ni-to-2DEG sidewall modulation region (10 nm) [15]. For each of the structures, at least 12 devices were measured, and small error bars in Fig. 2 reveal little variation between devices of the same kind. The Planar exhibited a large V_{on} of 1.43 ± 0.11 V and an undesirable knee voltage. This knee voltage was eliminated in the Tri-anode, with V_{on} reduced to 0.95 ± 0.09 V. The on-resistance (R_{on}) of the Planar and Tri-anode was 3.38 ± 0.16 and 3.48 ± 0.11 ohm·mm, respectively. Furthermore, the Planar presented a resistive linear behavior under small bias, due to the AlGaN barrier, while the Tri-anode presented I-V characteristics much closer to an ideal diode (the inset of Fig. 2 (b)). The I_R was also reduced by over 3 orders of magnitude for the Tri-anode (Fig. 2 (b)). These improvements can be explained by the integrated sidewall SBDs and tri-gate MOS in the Tri-anode. As shown Fig. 1 (e), the equivalent circuit of the hybrid tri-anode consists of Top and Sidewall SBDs as well as the tri-gate MOS. The sidewall SBD has a smaller and close-to-ideal Schottky barrier due to the absence of the AlGaN barrier, which led to a smaller V_{on} and eliminated the non-ideality observed in the Planar.

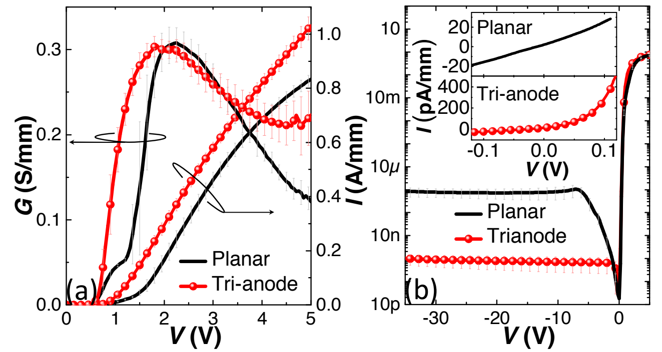

Fig. 2. (a) Forward and (b) reverse electric characteristics of the SBDs; the inset shows the I-V characteristics of the SBDs under small bias.

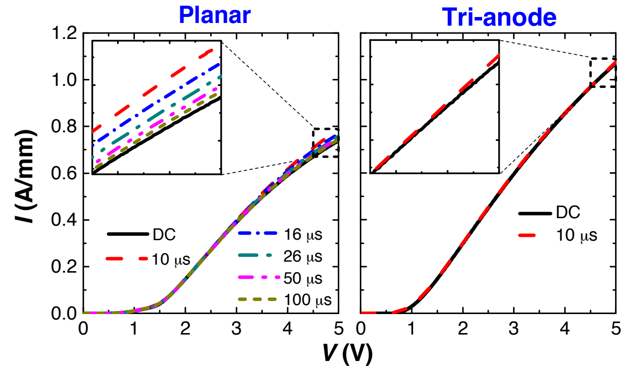

Fig. 3. DC and pulsed I-V characteristics of the SBDs with different pulse widths; the period of the pulse was kept constant as 1 s.

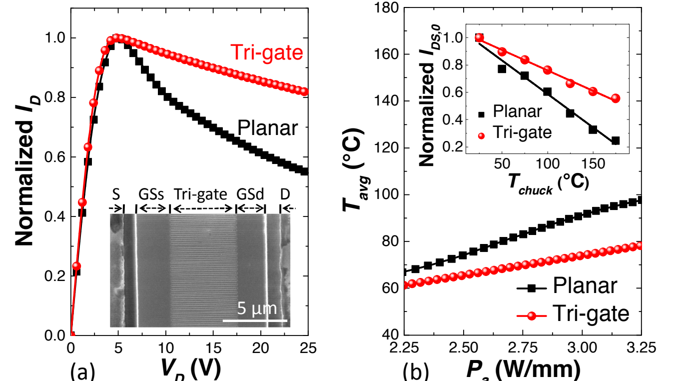

Fig. 4. (a) Normalized I_D-V_D characteristics of planar and tri-gate AlGaN/GaN MOS transistors measured with similar gate driving voltage (V_G - V_{th} = ~5 V) and (b) extracted average temperature of the 150-μm-wide transistors versus applied power normalized by device width; the insets of (a) and (b) show the SEM observation of the tri-gate transistor and the linear dependences of the extrapolated saturation drain current on the chuck temperature, respectively.

Under reverse bias, the tri-gate MOS was depleted when V was below its threshold voltage (V_{th}), largely suppressing the I_R. The reduction of I_R depends on V_{th} of the tri-gate MOS [4], which can be controlled by w and the thickness of the SiO_2 [11,16].

Fig. 2 (a) also reveals a more linear I-V characteristics with the Tri-anode. The first explanation for this is the minimized self-heating of the Tri-anode. To explore this, DC as well as pulsed I-V characteristics of the samples are compared in Fig. 3. An increase in current with reduced pulsed widths from 100 to 10 μs was observed for the Planar, indicating self-heating degradation of its DC performance. There was no obvious difference in DC and pulsed I-V characteristics for the

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Tri-anode even with a pulse width down to 10 μs (the shortest pulse width possible with our measurement equipment) and current over 1 A/mm. These results suggest a significant reduction of self-heating in the Tri-anode likely due to the improved heat dissipation from the nanowire trenches with large metal surface area, resulting in less thermal degradation in conductance of the tri-gate MOS. To verify this, AlGaN/GaN tri-gate high electron mobility transistors (HEMTs) with similar nanowires to the Tri-anode were compared with planar MOS transistors, and their normalized drain current-voltage (I_D-V_D) characteristics are shown in Fig. 4 (a). Using the technique proposed in Ref. [17], we measured the temperature dependence of the extrapolated drain saturation current ($I_{DS,0}$) and estimated the average temperature over the entire device active area (T_{avg}) as shown in Fig. 4 (b) (as justified in Ref. [18], the T_{avg} obtained by this method is close to the T_{avg} measured by micro-Raman thermography at low power levels although it may neglect the effect of traps). With the same applied power (P_a), the tri-gate HEMT exhibited a much reduced T_{avg} compared to the planar, which is comparable or greater than other technologies proposed for thermal management of GaN electronics such as graphene-graphite quilts [19], Cu-filled backside via [20], substrate transfer using h-BN [21] and nanocrystalline diamond thin film [22]. Figure 4 (b) also suggests a smaller thermal resistance (R_{TH}) for the tri-gate HEMT, which is consistent with a recent report in the literature [10]. From the slope of the linear region of the T_{avg} versus P_a curves, R_{TH} of the planar and tri-gate HEMTs were estimated to be about 34.2 and 17.0 K·mm/W, respectively, normalized by device width. The reduction in R_{TH} of about 50% in the tri-gate HEMT is very close to the reduction (55%) by replacing the Si substrate with SiC [23], indicating the great potential of the tri-gate technology in thermal engineering of GaN transistors. The reduced R_{TH} in the tri-gate HEMT can be attributed to mainly two reasons: i. the increased surface area with nanowire architecture and ii. the absence of the AlGaN barrier at the sidewalls, since AlGaN has much lower thermal conductivity with respect to GaN [24], which improves heat dissipation through the surface. The reduced T_{avg} and R_{TH} confirm the improved heat dissipation in the tri-gate HEMT, which is consistent with the results from pulsed measurements for the tri-anode SBDs.

Besides the enhanced heat dissipation, another reason for the better output linearity of the Tri-anode is the so-called sidewall conduction, which forms additional channels at sidewall SiO_2/GaN interface as a field effect transistor (FET) in parallel with the HEMT and reduces the resistance of the tri-gate MOS (Fig. 1(e)). The sidewall conduction was suggested by previous studies [25-28] but has not been investigated, in addition carrier accumulation at the oxide/GaN interface at trench bottom of the nanowires was neglected. To investigate this effect, periodically gate-recessed MOS transistors were fabricated (Fig. 5 (a) and (b)). Gate length of the transistors was 132 μm and the gate-to-source/gate-to-drain distance was 4 μm. The gate region of the transistors was periodically recessed with a depth of 114 nm and a length of 165 nm (period was 300 nm). Transfer characteristics of the fabricated transistor (Fig. 5 (c)) reveal current flows perpendicularly to the nanowires with normally-off behavior, indicating that carriers accumulated at

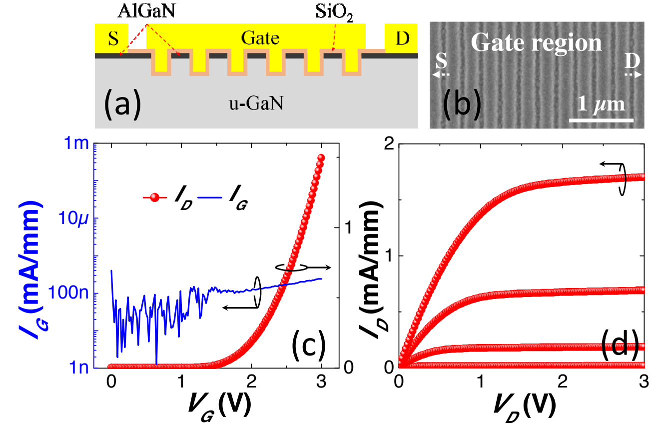

Fig. 5. (a) Cross-sectional schematic and (b) top-view SEM observations in gate region of the periodically gate-recessed transistors; (c) transfer and (d) output characteristics of the transistors.

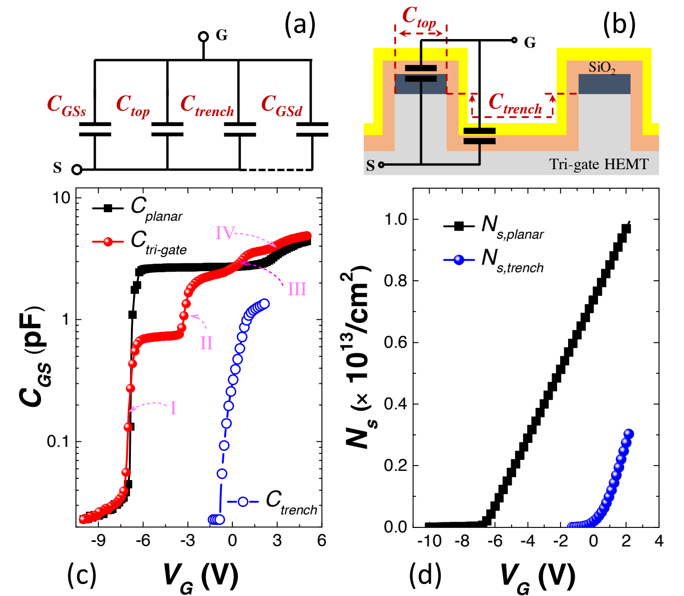

Fig. 6. (a) Equivalent circuit of C_{GS} for the tri-gate HEMT; (b) schematic of C_{top} as well as C_{trench} in the tri-gate region; (c) measured C-V characteristics of the HEMTs and extracted C_{trench}; (d) V_G-dependent sheet carrier density of the planar HEMT and the trench conduction.

the sidewalls as well as the bottom of each trench, and the two accumulation regions overlapped with each other with a threshold voltage of ~2 V. I_D-V_D plots of the transistors are presented in Fig. 5 (d), showing that accumulation-induced channels were well modulated by the gate voltage. These results clearly show that carrier accumulation at SiO_2/GaN interface forms conduction channels in the trenches and contributes to the output current of the Tri-anode. This contribution would increase with larger bias, compensating self-heat degradation and improving output linearity of the Tri-anode.

To investigate the contribution of the trench conduction, gate-source capacitance (C_{GS}) of the tri-gate and planar HEMTs were studied, denoted as $C_{tri\text{-}gate}$ and C_{planar}, respectively. The 150-μm-wide tri-gate HEMT had similar nanowires to the Tri-anode in which the direction of the current was parallel to the nanowire. Gate lengths of the HEMTs were both 10 μm (the

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inset of Fig. 4 (a)). $C_{tri\text{-}gate}$ is composed of four capacitors in parallel as shown in Fig. 6 (a). The first capacitor is the SiO_2/AlGaN/GaN top gates in the nanowire region (C_{top}), and the second is the SiO_2/GaN in nanowire trenches (C_{trench}), which acted similarly to a field effect transistor (FET), as shown in Fig. 6 (b). The other two capacitors are the SiO_2/AlGaN/GaN planar potions of the gate, one close to the source (C_{GSs}) and the other close to the drain (C_{GSd}), corresponding to the GSs and GSd regions in the inset of Fig. 4 (a). Figure. 6 (c) shows the *C-V* characteristics of the tri-gate and planar HEMTs. The steps I-IV observed for the *C-V* characteristics of the tri-gate HEMT corresponded to carrier accumulation in C_{GSs}, C_{top} + C_{GSd}, C_{trench} and at the SiO_2/AlGaN interface, respectively. C_{top} showed a less negative V_{th} with respect to C_{GSs} due to sidewall gate depletion and partial relaxation of AlGaN/GaN nanowires [29]. Before step IV, $C_{tri\text{-}gate}$ is simply the sum of C_{GSs}, $C_{top+GSd}$ and C_{trench}. Assuming that these capacitors shared similar values of capacitance in depletion, C_{trench} was extracted using $C_{trench} = C_{tri\text{-}gate} - [C_{GSs} + (C_{top} + C_{GSd})]$ when V_G was below 2 V since i. there was no spillover; ii. these capacitor were in parallel; iii $C_{GSs} + (C_{top} + C_{GSd})$ was saturated and its value was close to the value of $C_{tri\text{-}gate}$ before the V_{TH} of C_{trench}, as shown in Fig. 6 (c). Figure 6 (d) presents the comparison between the sheet carrier density of the planar HEMT ($N_{s,planar}$) and the trench ($N_{s,trench}$), extracted from the CV measurements. $N_{s,trench}$ is the equivalent carrier density obtained by normalizing the number of carriers with the product of trench length and width (not considering the four sidewalls of the trench) for a fair comparison with the planar HEMT. At a V_G of 2 V, the $N_{s,trench}$ was about 28.4% of the $N_{s,planar}$, which represents a significant portion of the carrier density and should not be neglected.

Besides the carrier density, electron mobility (μ) is another important factor that impacts the current in the trench. According to Ref [30, 31], the voltage-dependent effective mobility (μ_{eff}) of SiO_2/etched GaN channel is only about 16 $cm^2/V\cdot s$. This value is much lower than the low-field electron mobility (μ_0) and μ_{eff} of the planar HEMT equal to 1560 and 700 $cm^2/V\cdot s$ at V_G = 2 V, respectively, extracted using a mobility-degradation model [32,33]. The μ_0 was close to the Hall mobility, which was about 1660 $cm^2/V\cdot s$. Since the drain current of a transistor is proportional to the product of carrier density and μ, the drain current of the FET was about 6.5 % of the counterpart planar HEMT at $V_G = 2$ V. With increasing gate bias, this portion will further increase because of two factors: i. the slope of the $N_{s,trench}$ - V_G curve is larger with respect to the $N_{s,planar}$ - V_G curves and ii. the μ_{eff} of the FET doesn't change too much with increasing V_G [30] while that of the planar HEMT keeps degrading [34]. Consequently, the contribution of trench conduction to the output current of the Tri-anode is then estimated to be small but not negligible, which compensated partly the thermal degradation under high bias and even slightly impacted the on-resistance under low bias. Analogous to normally-off AlGaN/GaN transistors with oxide/GaN gate region, the key factor that limits the trench conduction is the low electron mobility due to the etching-induced damages at the SiO_2/GaN interface [35]. Such damages create a nitrogen-deficient surface and introduce high-concentration donor states, which greatly increase the probability of Coulomb scattering and hence degrade the electron mobility [30,36-37]. However, this mobility can be possibly enhanced by a few means. The first way is to improve the crystalline quality of GaN. For instance, 4-times higher electron mobility has been achieved for dry-etched GaN on sapphire [38] with respect to that on Si [30,31]. Secondly, optimized etching and recovery processes can also be helpful in reducing such damage. These methods would enhance the trench conduction and correspondingly that of the tri-gate HEMT or the Tri-anode. Furthermore, it should also be noted that, although the contribution of the trench conduction was small in this work, its impact can be relatively increased and possibly even dominating for other tri-gate or nanowire devices with very small *FF* or very narrow AlGaN/GaN nanowires in which the 2DEG is almost fully depleted.

The hybrid tri-anode structure improved the performance of the SBD in many aspects, but it sacrifices ~55% of the 2DEG due to the nanowire etching (*FF* = 0.45). This reduction in carriers can be compensated by increasing the *FF*. Figure 7 (a) shows the current densities I_d and I_{ed} obtained by two normalizations: i. by device width (w_d = 100 μm) and ii. by effective device width ($w_{ed} = n \times w$ for Tri-anode and w_{ed} = 100 μm for Planar). While I_{ed} was larger for the Tri-anode, the corresponding I_d became smaller than that of the Planar, because in this case the current was normalized by both widths of nanowires (with 2DEG) and trenches (without 2DEG). The absolute current of a single nanowire in Tri-anode is 9.05×10^{-5} A at V = 3 V using $I_{ed,trianode} \times w$. To achieve the same current at V = 3 V using the Planar, a width of ~197 nm (w_1) is needed, resulting in $FF_{critical} = w/w_1 = 0.69$. Assuming similar strain relaxation and heat dissipation, above such $FF_{critical}$, I_d of the Tri-anode would be larger than the Planar at this voltage. Figure 7 (b) presents the calculated $FF_{critical}$ for the Tri-anode versus V. The $FF_{critical}$ is firstly small because of the smaller V_{on} of the Tri-anode compared to the Planar, and after reaching a maximum value of ~0.73, it decreases due to the suppressed self-heating and trench conduction. Therefore, by increasing the *FF* from 0.45 to 0.73 for the Tri-anode, its absolute output current normalized by device width would exceed that of the Planar. In other words, above $FF_{critical}$ the sidewall contact, superior heat management and trench conduction overcomes

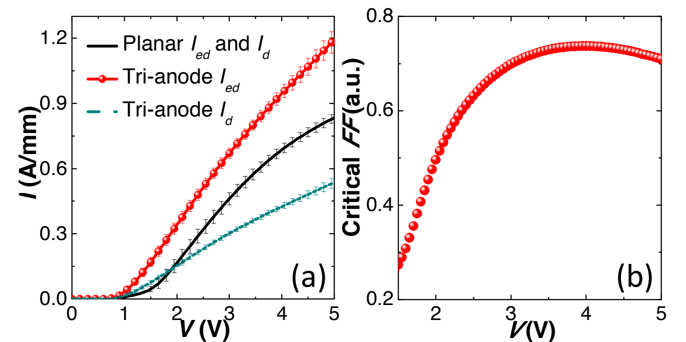

Fig. 7. (a) Current densities of the SBDs by different normalizations and (b) calculated critical *FF* versus *V* for the Tri-anode.

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the partial removal of the 2DEG. Considering that w and the length of the nanowire will impact the $FF_{critical}$, further studies of dependence of $FF_{critical}$ on w, and their impact on output and thermal characteristics of the nanowire devices will be of great importance.

IV. CONCLUSION

In conclusion, a hybrid tri-anode structure was investigated for AlGaN/GaN SBDs in this work, which resulted in a reduction of V_{on} from 1.43 V to 0.95 V and over 3 orders of magnitude lower reverse leakage current. The output current density normalized by effective anode width, and output linearity were enhanced by the integrated tri-gate transistors with trench conduction, which also largely diminished self-heating. We investigated the factors contributing to the electrical and thermal improvements in performance. Based on these results, we estimated the critical FF above which the partial removal of the 2DEG in the hybrid tri-anode can be overcome. In addition to the improved on-state performance and the significant reduction of the off-state leakage current by the nanowire geometry, this work shows the potential of future nanowire devices presenting larger absolute output current than counterpart planar devices.

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