Back-Contacted Silicon Heterojunction Solar Cells

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—per te,
che già sei qui con noi—

Abstract

Photovoltaic electricity has become competitive with traditional electricity sources in specific markets and its contribution to the global electricity supply is increasing. This has been possible in large part thanks to a simple optoelectronic device: the crystalline silicon solar cell. Despite its success, most industrial solar cells use a technology based on direct metal-silicon contacts, preventing the achievement of ultra-high conversion efficiencies. For a long time, this situation was acceptable, as the performance limitation of industrial solar cells was anyhow set by the quality of the available silicon material. Now, electronically outstanding crystalline silicon wafers are becoming affordable and available in sufficiently large quantities for photovoltaics, demanding improved device architectures to gain maximal efficiencies from such wafers.

A key to this goal is the use of carrier-selective passivating contacts, suppressing carrier recombination at the surface of the silicon absorber, and enabling open-circuit voltages and fill factors close to the theoretical limits. Combining the passivating contacts with a back-contacted solar cell architecture, in which no shadowing of contacts at the front takes place, it is possible to simultaneously maximize the short-circuit current and, thus, to aim at the maximum conversion efficiency. Recently, based on such approach, the world-record crystalline silicon device, with an efficiency of 25.6%, was demonstrated.

In this thesis, we develop original approaches to integrate passivating contacts, based on silicon heterojunctions, in back-contacted architectures. Silicon heterojunction technology uses thin films of intrinsic and doped amorphous silicon to form the passivating contacts, the so-called *"heterocontacts"*; in order to place both contact polarities at one side of the solar cell, these films require patterning. We defined a photolithography-free fabrication process using *in-situ* shadow masking, to pattern amorphous silicon thin-films, and hot melt inkjet printing to pattern the back electrodes. With this approach we demonstrated back-contacted silicon heterojunction solar cells with efficiencies above 22%.

Heterocontacts comprise also a transparent conductive oxide thin film on top of the amorphous silicon layers. To improve the heterocontacts, we optimized this transparent electrode analyzing its impact on contact passivation and transport. In addition, with the same goal, we evaluated microcrystalline doped films, as replacement of the conventional amorphous silicon films. With their use we realized heterocontacts with excellent charge-carrier transport, showing specific contact resistivity values down to $10\,\mathrm{m\Omega\,cm^2}$.

Back-contacted devices are characterized by a high fabrication complexity, which hinders

their application in industry. To solve this problem we introduce a novel and disruptive device concept, which improves and simplifies the fabrication of back-contacted devices, and where we exploit the optimum transport properties of microcrystalline-based heterocontacts. With this concept, exploiting interband tunneling effects, we made patterning of the hole collector obsolete and we demonstrate a conversion efficiency of 22.9% on a 9-cm^2 solar cell. Remarkably, as a result of the back-contacted architecture, we achieved short-circuit current densities of about $41\,\mathrm{mA\,cm^{-2}}$. Detailed device analysis quantify the remaining losses and indicate potential improvements to reach efficiencies over 24%.

Sommario

L'elettricità generata da sistemi fotovoltaici, in certi mercati, è divenuta competitiva con quella prodotta con metodi tradizionali ed il suo contributo, rispetto alla domanda globale di energia elettrica, è in crescita. Ciò è avvenuto in larga parte grazie ad un semplice dispositivo optoelettronico: la cella solare in silicio cristallino. Nonostante il suo successo, gran parte delle celle prodotte industrialmente utilizzano una tecnologia basata sul contatto diretto metallo-silicio, che ne limita le efficienze di conversione. Per lungo tempo, ciò è stato accettabile in quanto l'efficienza era limitata dalla qualità del silicio disponibile per il fotovoltaico. Ora, silicio cristallino ad alta qualità si sta rendendo disponibile nelle quantità, ed ai costi, richiesti dal fotovoltaico. Ciò richiede l'implementazione di dispositivi con architetture migliorate, in grado di sfruttare al meglio le possibilità offerte da questo materiale.

Un elemento chiave, per raggiungere le massime efficienze possibili, è l'uso di contatti passivanti. La caratteristica saliente di questa tecnologia è l'eliminazione dei processi di ricombinazione dei portatori di carica alla superficie dell'assorbitore in silicio. Ciò permette di raggiungere tensioni di circuito aperto e fattori di forma prossimi ai limiti teorici. Combinando i contatti passivanti ad un'architettura "*back-contacted*" è possibile massimizzare anche le correnti di corto circuito, e di conseguenza puntare alle massime efficienze. Recentemente, con questo approccio, è stato raggiunto il record mondiale di efficienza per una cella solare in silicio cristallino, pari al 25.6%.

In questa tesi abbiamo sviluppato un approccio originale per l'integrazione di contatti passivanti basati sulla tecnologia del silicio ad eterogiunzione, in una architettura back-contacted. La tecnologia del silicio ad eterogiunzione usa strati di silicio amorfo, intrinseco o drogato, per formare i contatti passivanti, detti "*heterocontacts*". Al fine di posizionare entrambe le polarità su di un solo lato della cella solare, questi strati devono subire un processo di "*patterning*". Senza ricorrere all'utilizzo di tecniche fotolitografiche, abbiamo definito un processo di fabbricazione basato su un sistema di maschere *in-situ*, per il patterning degli strati di silicio amorfo, e su di un processo di "*hot melt inkjet printing*" per la fabbricazione degli elettrodi posteriori. Con tale approccio, abbiamo realizzato celle solari con efficienza superiore al 22%.

Gli heterocontacts comprendono anche un film sottile di ossido trasparente e conduttivo, posto al di sopra dei layer di silicio amorfo. Con lo scopo di migliorare le proprietà degli heterocontacts, abbiamo ottimizzato questo elettrodo studiandone l'impatto sulla qualità del contatto passivante e sulle sue proprietà di trasporto. In aggiunta, con lo stesso scopo, abbiamo valutato l'uso di film drogati microcristallini come sostituti degli strati convenzionali

in silicio amorfo. Con l'uso di silicio microcristallino, abbiamo realizzato heterocontacts con eccellenti proprietà di trasporto dei portatori di carica e resistività di contatto dell'ordine dei $10\,m\Omega\,cm^2$.

Le celle solari back-contacted sono caratterizzate da un processo di fabbricazione complesso, che rende improbabile l'implementazione industriale. Per fornire una soluzione a questo problema, proponiamo un dispositivo di nuova concezione, che semplifica e migliora la fabbricazione di dispositivi back-contacted, e dove utilizziamo le ottime proprietà di trasporto degli heterocontact basati su silicio microcristallino. Con questo nuovo dispositivo, che sfrutta fenomeni di interband tunneling, e non richiede il processo di patterning del collettore per lacune, abbiamo dimostrato efficienze di conversione pari al 22.9% in una cella solare avente una superficie di 9-cm^2. I nostri dispositivi, grazie all'architettura back-contacted, hanno correnti di corto circuito prossime a $41\,mA\,cm^{-2}$. L'analisi dettagliata dei dispositivi ci permette di quantificare le restanti perdite e di indicare i miglioramenti da apportare per raggiungere efficienze superiori al 24%.

Parole chiave: eterogiunzioni al silicio, silicio amorfo, cella solare, alta efficienza, back-conatcted, IBC-SHJ, inkjet printing, contatti passivanti, ossido trasparente conduttivo, silicio microcristallino, interband tunneling.

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List of abbreviations and symbols

Solar cells

Al-BSF	Aluminium-diffused back-surface field
SE	Selective emitter
PERC	Passivated emitter and rear cell
PERL	Passivated emitter, rear locally-diffused
PERT	Passivated emitter, rear totally-diffused
SHJ	Silicon heterojunction
ARC	Anti-reflective coating
FHC SHJ	Front-hole-collecting silicon heterojunction
RHC SHJ	Rear-hole-collecting silicon heterojunction
IBC	Interdigitated back-contact
IBC-SHJ	Interdigitated back-contacted silicon heterojunction
IST	Interband silicon tunnel
IST-p	p-type film in interband silicon tunnel junction
IST-n	n-type film in interband silicon tunnel junction
tunnel-IBC-SHJ	Interdigitated back-contacted silicon heterojunction with interband tunnel junction

Semiconductors

Δn	Excess minority carrier density
τ_{eff}	Effective minority carrier lifetime
WF	Work function
N_D	Dopant atom density
E_g	Energy gap

Materials and depositions

TCO	Transparent conductive oxide
ZnO:Al	Aluminium-doped zinc oxide
ZnO:B	Boron-doped zinc oxide

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ITO	Indium tin oxide
IZO	Indium-zinc-oxide
TMO	Transition metal oxide
MoO_x	Molybdenum oxide
a-Si:H	Hydrogenated amorphous silicon
a-Si:H(i)	Intrinsic hydrogenated amorphous silicon
a-Si:H(n)	n-type phosphorous-doped hydrogenated amorphous silicon
a-Si:H(p)	p-type boron-doped hydrogenated amorphous silicon
μc-Si:H	Hydrogenated microcrystalline silicon
μc-Si:H(i)	Intrinsic hydrogenated microcrystalline silicon
μc-Si:H(n)	n-type phosphorous-doped hydrogenated microcrystalline silicon
μc-Si:H(p)	p-type boron-doped hydrogenated microcrystalline silicon
c-Si	Crystalline silicon
c-Si(n)	n-type phosphorous-doped crystalline silicon
a-SiN$_x$:H	Hydrogenated amorphous silicon nitride
a-SiO$_x$:H	Hydrogenated amorphous silicon oxide
PECVD	Plasma enhanced chemical vapor deposition
LPCVD	Low pressure chemical vapor deposition
PVD	Physical Vapor Deposition

Characterization

η	Energy conversion efficiency
FF	Fill factor
pFF	Pseudo fill factor
implied-FF	Implied fill factor
I_{sc}	Short-circuit current
J_{sc}	Short-circuit-current density
V_{oc}	Open-circuit voltage
I-V	Current-voltage measurement
mpp	Maximum power point
R_{series}	Series resistance
R_{series}^{N}	Normalized series resistance
R_c	Contact resistance
$(\rho_c)_n$	Specific contact resistivity of electron contact
$(\rho_c)_p$	Specific contact resistivity of hole contact
R_{shunt}	Shunt resistance
R^{N}_{shunt}	Normalized shunt resistance
FF_0	Ideal diode FF
FF_s	Series-resistance-affected FF
$FF_{s,sh}$	Series-and-shunt-resistance affected FF
$\Delta FF_{R_{series}}$	FF series-resistance losses

x

$\Delta FF_{R_{\text{shunt}}}$	*FF* shunt-resistance losses
$\Delta FF_{J_0(n\neq n^*)}$	*FF* recombination losses
A_{cell}	Solar cell absorbance
R_{cell}	Solar cell reflectance
T_{cell}	Solar cell transmittance
EQE	External quantum efficiency
IQE	Internal quantum efficiency
PL	Photoluminescence
LBIC	Light-beam-induced current
TLM	Transfer length method
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
HR-TEM	High resolution transmission electron microscopy

1 Introduction

This chapter introduces the general field of *Photovoltaics*, the current market and industry situation and the technological roadmap of crystalline silicon (c-Si) wafer-based solar cells. In the last sections, we give an overview of the structure of this thesis and of its main contributions to the research field of back-contacted c-Si wafer-based solar cell technologies.

1.1   The general field of *Photovoltaics*

The conversion of solar energy by means of photovoltaic (PV) technologies is by now a consolidated approach to electricity generation. The amount of PV electricity produced in the world per year supplies about 1.3 % of the global electricity demand, with an increase of about 0.3 % absolute per year. However, there are large geographical inhomogeneities in the production of solar electricity and use. In certain pioneering countries or regions, already 6 % to 8 % of the electricity demand is satisfied with PV electricity [IEA 2016]. In these countries or regions, namely Italy, Germany, California and Greece, PV is not longer a minor contributor to electricity generation with respect to conventional energy sources.

Since the early 2000s, the subsidizing policies of some European countries gave the initial impulse to the creation of the PV market and industry. PV is now moving towards a new condition of self-sustainment. The old feed-in tariffs are progressively being phased out and, especially in emerging markets, unsubsidised tenders for power purchase agreements (PPA) and net-metering schemes are the current preferred routes of PV deployment [IEA 2016]. Recent PPAs have set continuously new records for the price of PV electricity, e.g. now in Mexico at about 5 US cents/kWh, and demonstrate that photovoltaics can produce electricity at costs in line with most of the conventional energy sources. Comparing different electricity sources, the standardized metrics are the levelized cost of electricity (LCOE), expressed in $/kWh or €/kWh, which includes investment, maintenance and fuel cost, over a system's lifetime. Recent analysis attributed to non-subsidized utility-scale PV one of the lowest LCOE within all renewable and conventional electricity sources, second only to wind generation

[Lazard 2015]. At this stage it is difficult to imagine a future in which PV technologies will not play a major role in electricity generation worldwide.

With respect to the future of PV (but also of the other variable renewable energies), the central theme now is the impact of the intermittence in electricity generation. With high degrees of PV penetration, the grid needs to be strengthened, energy back-up systems are required, and electricity transmission losses increase. Recently, to account for such integration costs, a new metric, the so-called "dynamic" or "system" LCOE [Ueckerdt 2013], was introduced. System-integration challenges are assuming an increasing importance with respect to the future of PV.

Below, after giving a snapshot of the current situation of the PV market and industry, we discuss the impact of conversion efficiencies in the current context of photovoltaics and motivate the quest for higher cell and module conversion efficiencies.

In this thesis, we direct our research efforts towards the development of a PV device technology with the potential of higher conversion efficiencies, compared to the state-of-the-art of the industrial production. We develop an industrially relevant technology for back-contacted c-Si wafer-based solar cells with passivating contacts: the ultimate architecture for single-junction c-Si wafer-based devices.

1.1.1   The photovoltaic market and industry

The photovoltaic market has been constantly and considerably growing over the last 15 years; the yearly installed PV capacity has grown from 328 peak MW (MWp), in 2001, to 50 GWp in 2015 [IEA 2016], leading to a cumulative installed PV capacity of about 227 GWp. This constant growth hides big geographical differences; from a substantially European-based PV market, starting from 2012 we evolved to a more diffused market, lead by Asian countries.

Despite this continuous and progressive expansion of the global PV market, the industry has both expanded aggressively, and contracted drastically, in the last 10 years. The period 2005–2010 was characterized by an uncontrolled industrial expansion which resulted in a production overcapacity. In 2011 an industrial consolidation phase started, with hundreds of small and medium enterprises filing for insolvency and leaving the market. Few GW-sized industrial players emerged and took the lead in cell and module fabrication and technological development. Si ingot-based technologies continued to play a prominent role, whereas exotic Si substrates such as the silicon ribbon technology disappeared. High-efficiency technologies, on n-type monocrystalline Si wafers, survived with their own specific market with, as prime examples, silicon heterojunction (HIT®, Panasonic) and diffused-junction back-contacted devices (Maxeon®, SunPower®). Thin-film technologies faced hard times struggling with costs and the prices of mass-produced c-Si devices and, except for few notable cases, were pushed out of the market. Overall, strong competition between companies and different technologies shrank costs and boosted conversion efficiencies.

The result of such pressure on the industrial system: PV became cheaper but also less prone to introduce innovations. Any emerging technology, from the disruptive one to the simple process innovation, must confront a well-consolidated and optimized benchmark, moving constantly forward with respect to costs and device performances. This situation defined the current technological scenario characterized by a mainstream c-Si technology still prevalently based on the *aluminium-diffused back-surface field* solar cell architecture (see section 1.2), a technology essentially dating from the 1970's.

1.1.2 Impact of the module conversion efficiency

The current competitive cost of PV electricity comes from a reduction of the overall PV system cost ($/kWp), due to decreased module and inverter costs. As discussed above, this happened thanks to the competitive pressure on the manufacturers at each step of the PV production chain. In 2014, production costs for module manufacturers were about one fifth of what they had been in 2007 [Verlinden 2016]. Here, we argue that this decrease in module and inverter costs modified the composition of the PV system cost, augmenting the importance of the module conversion efficiency.

Low module and inverter costs increase the relative importance of the balance of systems (BOS) cost, which includes ground, mounting, structure and cabling costs. The current system cost accounts for 55 % and 11 % of module and inverter costs, respectively, whereas the remaining 34 % relates to the BOS cost [Agora 2015]. Most BOS cost components are area dependent, and hence are reduced by higher module efficiencies. Assuming, for simplicity, that the BOS cost scales linearly with the PV system area and assuming a PV system with a certain capacity (Wp), in Table 1.1 we analyse the impact of different strategies to reduce the system cost. An always-effective strategy to lower the final system cost is to increase module efficiency at a constant module unit cost (1). This decreases both BOS and module costs (less system area and less modules). Alternatively, reducing the module unit cost at a constant module efficiency is also a viable option (2). However, this will affect the final system cost only if the ratio between the total module and system cost (M) is sufficiently high. Eventually, with a high ratio between the BOS and system cost (B), increasing the module efficiency at a constant module cost per Wp becomes a third effective route towards lower system costs (3).

Importantly, in the current industrial situation, characterized by highly optimized material and processing costs for the fabrication of cells and modules, approach (3) becomes an important option. In the scenarios of Table 1.1, a 10 % higher relative module efficiency (at a fixed cost per Wp) implies a 10 % lower BOS cost, i.e. a 3.4 % lower system cost, with $B = 0.34$ [Agora 2015]. In the past, when the BOS cost component was low, this hypothetical situation would have produced a negligible reduction of the final system cost. In addition, we note that higher module efficiencies, at a fixed cost per Wp, allow for higher processing costs per unit device (cell and module) and possibly higher device complexity. Based on these arguments, several sources agreed in attributing a key role to module conversion efficiency—as a driver to BOS

Table 1.1: Strategies for PV system cost reduction. For simplicity, we assume a fixed PV system capacity and that the BOS cost scales linearly with the system area. In the current situation of high BOS cost, optimized raw-material usage and optimized low module and cell processing costs, the increase of module efficiency (η), at a fixed unit module cost, is a viable strategy to reduce the PV system cost.

Cost-reduction strategy	ΔBOS cost (%)	ΔInverter cost (%)	ΔTotal module cost (%)	Δ**System cost (%)**
(1) increase module η (+x% rel.) _at constant module cost per unit_	-x	=	-x	-x*(B-M)
(2) decrease module cost per Wp _(-x% rel.)_ at constant module η	=	=	-x	$-x \cdot M$
(3) increase module η (+x% rel.) _at constant module cost per Wp_	-x	=	=	$-x \cdot B$

ΔC (%)=ΔC/C$_{initial}$ _with_ C ($)=BOS, Inverter, Total module or System cost

System cost ($)=BOS+Inverter+Total module costs

_M_=Total module cost/System cost

_B_=BOS cost/System cost

cost reduction—in the future of PV [Agora 2015, Green 2016a, Wang 2011, MB 2014]. Again, an economical circumstance may become the motor of incoming technological changes.

1.2 Crystalline Si wafer-based solar cell technologies

Solar module conversion efficiencies are determined by solar cell efficiencies and by cell-to-module power losses. Solar cell efficiencies, in turn, depend mainly on the quality of the absorber material and on the chosen device technology. Here, we discuss this last aspect for c-Si wafer-based solar cells. We depict the current scenario of industrial production and we discuss the c-Si technological roadmap.

1.2.1 The quest for higher solar cell efficiencies

The technological roadmap towards high-efficiency c-Si solar cells was mostly defined twenty years ago. Since the 1980's, increasingly advanced and high-efficiency solar cell designs were introduced. Typically at the time of their conception, they were demonstrated as laboratory devices with improved efficiencies. Nevertheless, most of these inventions have not reached the PV industry so far. Below we give a description of the most relevant solar cell architectures, and relate them to the overall c-Si technological roadmap.
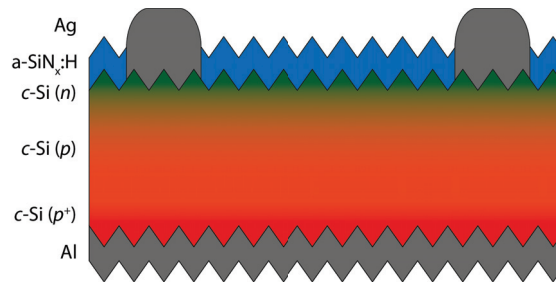
Figure 1.1: Schematic of the aluminium-diffused back-surface-field (Al-BSF) solar cell. Adapted from [De Wolf 2012b].

The aluminium-diffused back-surface-field solar cell

The aluminium-diffused back-surface-field (Al-BSF) solar cell architecture is simple, robust and industrially successful. The typical configuration is based on a monocrystalline or multicrystalline boron-doped c-Si(p) wafer as the absorber. At the front, a thin n-type phosphorous-doped diffused layer is formed and passivated with a hydrogenated amorphous silicon nitride (a-SiN$_x$:H) thin film, which acts simultaneously as an anti-reflection coating (ARC). At the back, a thick film of screen-printed aluminium, after a thermal treatment, forms a 5-μm-thick p-type Al-doped Si layer, acting as the back-surface field, and electrical back contact. The front-grid electrode is fabricated by screen-printing of a Ag paste, which, when thermally activated, etches the a-SiN$_x$:H film and contacts the underlying n-type diffused layer. Since the early 2000s, the described Al-BSF architecture was adopted as the mainstream technology by the c-Si PV industry and, over the years, has been pushed to extreme levels of optimization. Conversion efficiencies for cells based on monocrystalline Si wafers in industry are now in the range of 18.5 % to 19.5 %. A complete and detailed review of this technology can be found in Ref. [Glunz 2012]. Fig. 1.1 shows a schematic representation of the Al-BSF solar cell.

The main limitations of the Al-BSF architecture reside in the poor back-side optics and passivation. Importantly, these limitations cap the maximum achievable efficiency and become increasingly detrimental for improved quality of the Si absorber and thin Si wafers [Glunz 2012]. This led to the introduction of solar cell architectures with a passivated back side, discussed below. Another minor limitation, in the architecture of Fig. 1.1, is represented by the uniformly doped c-Si(n) layer at the front. A uniform doping causes there to be a trade-off between the electrical contact with the front-grid electrode, and Auger-recombination processes in the highly doped diffused layer. This trade-off can be overcome by means of the selective emitter (SE) concept, with different doping levels in metallized and non-metallized areas. Several approaches have been pursued to define an effective SE fabrication process [Hahn 2010]. However, their spread in industry was limited by advances in Ag paste technology, which eased the requirements to achieve a good Ag/c-Si(n) electrical contact and relaxed the trade-off mentioned above.
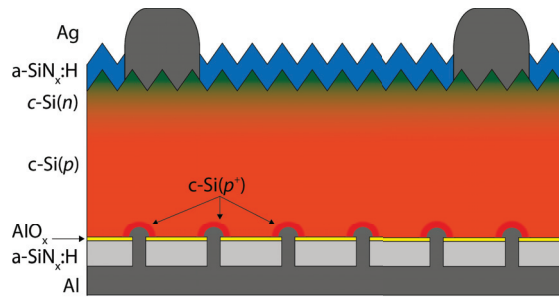
Figure 1.2: Schematic of the industrial passivated emitter, rear locally-diffused (i-PERC) solar cell.

Solar cells with passivated rear side: the PER$_x$ family

To overcome the major limitations of the Al-BSF solar cell, alternative contacting and passivation schemes for the back side were introduced. In 1989, the passivated emitter and rear cell (PERC) [Blakers 1989] was demonstrated with a conversion efficiency of 22.8 %. In this device architecture a silicon oxide passivation film at the back side is locally opened to form the back contact. A variant of this approach, which further reduces back-side carrier recombination, is the passivated emitter, rear locally-diffused (PERL) solar cell. This cell structure was proposed in 1990 [Wang 1990], with efficiencies of 24.2 %, and implements the local diffusion of boron in the back contact areas. Another derivation of the PERC approach is the passivated emitter, rear totally-diffused (PERT) solar cell that was proposed in 1992 [Wang 1992], and pushed up to an efficiency of 24.5 % in 1999 [Zhao 1999]. All these solar cell architectures can be grouped in the PER$_x$ family. They were developed in the 1980's and 1990's, on p-type substrates, thanks to the pioneering work carried out at the University of New South Wales (UNSW), Australia.

Currently, PERC technologies are progressively being introduced in industrial mass production [Metz 2014, Green 2015]. The original PERC concept [Blakers 1986] is adapted to the requirements of mass production in *industrial* passivated emitter and rear cells (i-PERC). Fig. 1.2 shows the typical scheme of an i-PERC solar cell. Modifying the device proposed by Blakers *et al.*, a stack of AlO$_x$ and a-SiN$_x$:H films is used, instead of a silicon oxide film, for back-side passivation [Hannebauer 2014, MB 2016]. The a-SiN$_x$:H capping layer is used to protect the dielectric layer underneath, so that the aluminium of the back contact can be used to form a local back-surface field and reduce carrier recombination at the contacts. Alternatively, silicon oxide can be used in place of AlO$_x$ [Cheng 2015, Tous 2012], but this solution is not expected to reach market penetration [ITRPV 2015]. Typical i-PERC conversion efficiencies are currently in the range of 20 % to 21 % on monocrystalline Si substrates. The i-PERC concept is sometimes associated with the SE technology; the additional benefits of the SE at the front allowed the current record i-PERC conversion efficiencies of 22.13 % and of 21.25 % on monocrystalline and multicrystalline Si substrates, respectively [Verlinden 2016].
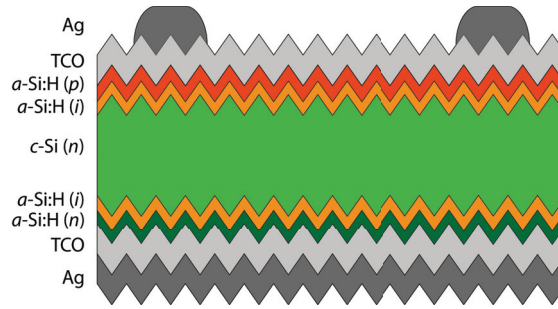
Figure 1.3: Schematic of the silicon heterojunction (SHJ) solar cell concept. The architecture reproduced in the sketch corresponds to the front-hole-collecting (FHC) architecture. Adapted from [De Wolf 2012b].

Solar cells with passivating contacts

In solar cells, to achieve ultimate open-circuit voltages (V_{oc}) and fill factors (*FF*), direct contact between the metal of the electrodes and the c-Si absorber material must be avoided. The typical approach is to use passivating carrier-selective contacts, which extract from the c-Si one specific type of carrier. Electron and hole contacts are typically based on a film stack composed of a surface passivation layer and a carrier-collecting overlayer. The latter must have the proper electronic band structure to determine the required field-effect at the c-Si surface and induce selectivity to electrons and holes, respectively.

One possible way to form passivated contacts is by means of the silicon heterojunction technology (SHJ). This approach, pioneered by Panasonic [Tanaka 1992], Japan, is based on the use of hydrogenated amorphous silicon (a-Si:H) thin films and was recently shown to allow conversion efficiencies higher than 25 % [Masuko 2014, Adachi 2015]. The passivating contacts in SHJ solar cells are formed by extremely thin intrinsic a-Si:H (a-Si:H(*i*)) films and doped a-Si:H overlayers, both deposited via plasma-enhanced chemical vapor deposition (PECVD) on the c-Si absorber surfaces. Transparent conductive oxide (TCO) overlayers transport the extracted carriers to the metal contacts. Two-side-contacted SHJ solar cells can have one of two configurations depending on the positioning of the hole- and electron-collecting side with respect to the sunlight. We can distinguish between front-hole-collecting (FHC) devices and rear-hole-collecting (RHC) devices. In Fig. 1.3 we show a cross-sectional schematic of a FHC SHJ solar cell.

Recently, in addition to the SHJ technology, other approaches to form well-optimized passivating contacts are emerging. One possibility is to combine the a-Si:H(*i*) passivating layer of SHJ devices with a high- or low-work function (WF) material other than a-Si:H. Excellent device results, with efficiencies up to 22.5 %, have been demonstrated using thin films of molybdenum oxide as the front-hole-collecting overlayer [Geissbuhler 2015b]. Importantly, with this technology, it was argued that doping in solar cells is no longer required [Bullock 2016]. An alternative approach, based on the pioneering work of [Yablonovitch 1985], is the so-called TOPCon approach. This technology combines the use of an ultrathin passivating tunneling

SiO$_2$ film (<1.5 nm) with a highly doped amorphous/crystalline silicon film deposited by PECVD. Recently, this technology was used to realize the electron contact at the back of a two-side-contacted solar cell with a conversion efficiency of 25.1 % [Glunz 2015].

Back-contacted solar cells

Back-contacted solar cells are the best candidates to reach high short-circuit current (J_{sc}) values. Their front side is devoid of any grid electrode, which avoids shadowing and maximizes the solar cell active area. The most typical back-contacted concept, conceived in 1975 [Schwartz 1975, Lammert 1977], is based on an interdigitated design for the back electrodes, the so-called interdigitated back-contacted (IBC) solar cell. Cross-sectional and bottom-view schematics of a typical IBC solar cell are shown in Fig. 1.4. IBC solar cells are industrially produced in mass production by Sunpower®, which hold the record for the highest commercial solar cell efficiency; this is thanks to the back-contacted architecture but also to the use of an unspecified passivating contact technology. Nevertheless, compared to conventional devices, they are characterized by a higher production complexity which must be compensated for by higher selling prices. The technological sophistication needed to realize both contacts at one side, is the weak point of any back-contacted technology. Smart solutions for back-contacted solar cell fabrication are still sought.

(a) Cross-sectional schematic. (b) Bottom-view schematic.
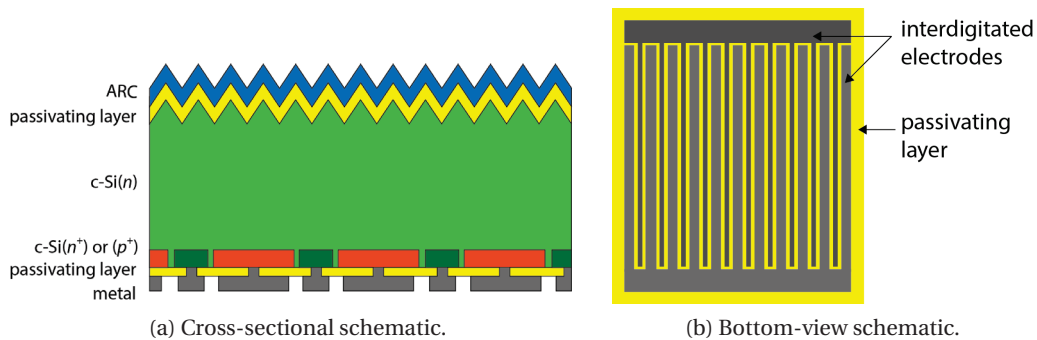
Figure 1.4: Cross-sectional and bottom-view schematics of the interdigitated (IBC) back-contacted solar cell.

Back-contacted devices other than the IBC solar cell are also possible; examples of alternatives are the emitter wrap through (EWT) [Gee 1993] and the metal wrap through (MWT) [Van Kerschaver 1998] concepts. They may present some advantages over IBC cells with respect to the fabrication process, but they do not enjoy the full J_{sc} advantage. A comprehensive review of these back-contacted solar cell concepts can be found in the work of Van Kerschaver *et al.* [Van Kerschaver 2006].

The technological roadmap of the c-Si industry

In Fig. 1.5 we summarized, schematically, the c-Si industry technological roadmap for two-side-contacted and back-contacted devices. Each technology has already been demonstrated, at least in the laboratory or in pilot production, and the corresponding record efficiencies are included in the picture. The current degree of market penetration of each technology, and its projection in ten years' time, are also indicated [ITRPV 2015]. From these data emerges the current industry position, along the technological roadmap, and the projected position for 2026. We note that, moving to high-efficiency devices, a progressive shift towards n-type substrates is also expected.

As last step, in the roadmap, we included two-terminal (2-T) and four-terminal (4-T) c-Si tandem devices. With device efficiencies approaching the limiting values predicted for c-Si absorbers, this step now seems to be the natural progression of c-Si-based device development. The most promising approach, to fabricate c-Si tandem devices, is to use a perovskite top cell [Werner 2016b, Mailoa 2015, Werner 2016a, Duong 2016]. Excluding multi-junction approaches, the ultimate architecture for c-Si wafer-based technologies integrates the passivating contact technology in a back-contacted solar cell architecture. This is the approach that produced the current 25.6 % world record conversion efficiency for single-junction c-Si devices [Masuko 2014] and also the approach followed in this thesis. Importantly, these devices have the potential to integrate the best V_{oc} and FF of passivating contact technologies and the best J_{sc} of back-contacted devices. We note that also back-contacted solar cells may be used to realize c-Si tandem devices operating in a 4-T configuration [Essig 2015].

1.3 Motivation, objective and structure of this work

1.3.1 Motivation and objective

As discussed above, the integration of passivating contacts in back-contacted solar cell architectures allows for ultimate solar cell conversion efficiencies for single-junction Si wafer-based technologies. This technological merger brings together the advantages of a shadowing-loss-free solar cell, a precondition for best-J_{sc} values, and of a recombination-free contacting system, a precondition for best-V_{oc} and -FF values. The main practical goal of this thesis is to realize such integration, effectively, for SHJ passivating contacts. From a scientific perspective, the achievement of our objective requires an in-depth understanding of the specific physical processes occurring in the fabricated back-contacted devices and the identification of the major loss mechanisms.

This thesis has been partially carried out in the framework of two research projects, funded by the *Commission pour la technologie et l'innovation* (CTI) of the Swiss Confederation. The CTI project No. 13348.1 "Development of thin high-efficiency large-area interdigitated back contact silicon heterojunction solar cells for mass production (HET-IBC)" run between 2012 and 2014; the partners involved were the PV-Lab of EPFL and Roth& Rau Switzerland SA. The
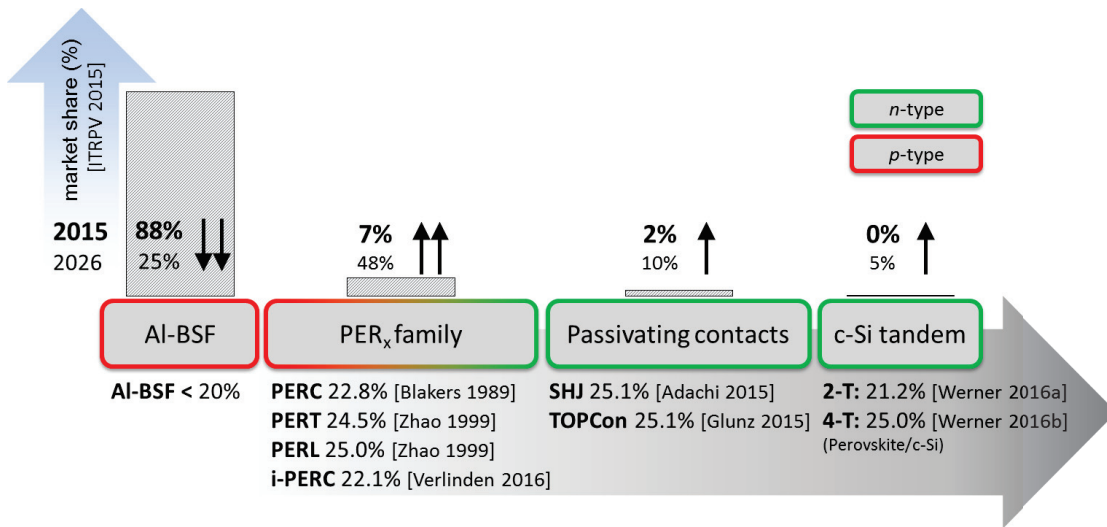
(a) Two-side-contacted solar cells.
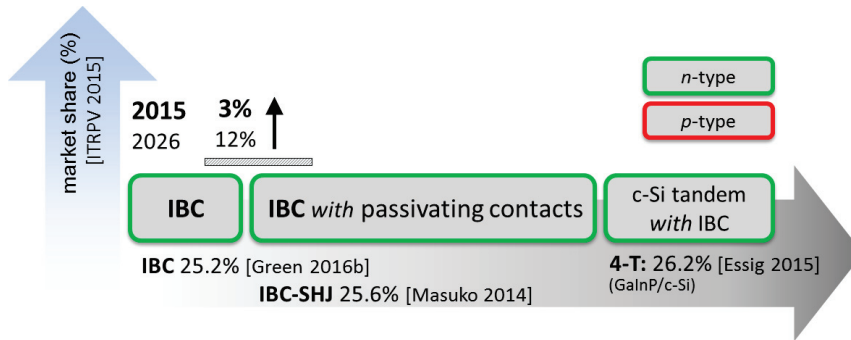
(b) Back-contacted solar cells.

Figure 1.5: Sketch of the technological roadmap for c-Si wafer-based two-side-contacted (a) and back-contacted (b) solar cells. Adapted from [Verlinden 2016].

CTI project No. 17705.1 "PUNCH: ProdUction-ready, Next-generation back-Contacted silicon Heterojunction solar cells and modules" runs between 2015 and 2017; the partners involved are the PV-Lab of EPFL, the PV-Center of the Swiss Center for Electronics and Microtechnology (CSEM) and Meyer Burger Research AG. Coherently with the scope of the project, and with the ambition of being industrially relevant, we posed some constraints to our research. In our work, we considered industrially compatible fabrication technologies and simple process flows, with a limited number of process steps.

1.3.2 Structure

The manuscript is structured as follows:

- **Chapter 2** introduces the main solar cell fabrication technologies, characterization techniques and loss-analysis methodologies used in this thesis.

- **Chapter 3** investigates possible approaches to thin-film patterning and defines a tentative processing technology for back-contacted SHJ solar cell fabrication.

- **Chapter 4** presents the development of our photolithography-free IBC-SHJ technology and highlights the major challenges in the achievement of high conversion efficiencies.

- **Chapter 5** analyses the influence of the transparent electrode material properties on SHJ contact passivation and charge-carrier transport quality.

- **Chapter 6** demonstrates a new disruptive back-contacted SHJ device concept with great promises towards industrialization.

- **Chapter 7** summarizes the major results of this thesis and presents our perspective on the future developments in the field of back-contacted solar cells.

1.4 Contribution to the research field

Part of the work presented in this thesis was carried out in collaboration with various colleagues, at **PV-Lab (EPFL)** and **PV-Center (CSEM)**, and with **Meyer Burger Research AG**. The respective contributions are acknowledged later in the thesis. The technologies proposed in this work are in part based on the baseline processes already developed for two-side-contacted SHJ devices at EPFL and CSEM.

Our research contributes to the development of back-contacted SHJ solar cell technologies. Despite the fact that devices with world-record conversion efficiencies have been recently achieved in this field, most of the technological and scientific challenges (i) overcome to reach such best devices are still veiled. In addition, it can be inferred that most of these devices were fabricated with techniques that are not viable in the PV industry such as, for instance, photolithography. In this context, high process complexity (ii) hinders the spreading of back-contacted SHJ technologies in industry. The outcomes of this thesis bring essential contributions to both theme (i) and (ii). The findings of chapters 3, 4 and 5 represent a significant advancement of the current knowledge about back-contacted SHJ devices and contribute to theme (i). The device concept of chapter 6 hints to the solution of the complexity problem usually associated with the fabrication of back-contacted devices and contributes to theme (ii). Below, we give a more detailed description of such contributions.

In this thesis, we explored thin-film patterning methodologies for back-contacted SHJ device fabrication. We defined a back-contacted SHJ photolithography-free technology [Tomasi 2014a, Tomasi 2014b], and demonstrated its potential, fabricating IBC-SHJ devices with conversion efficiencies over 22 %. This achievement was enabled by the identification and the solution of certain critical limitations to IBC-SHJ device performances. Optimized transport losses at the heterocontacts [Tomasi 2014a], a low-absorbing front passivating stack [Paviet-Salomon 2015a], efficient minority carrier collection and sharp edges for hole- and electron-collecting layers [Tomasi 2015a], were identified to be as the major challenges for

highly efficient devices. Our needs, in terms of thin-film morphology characterization, led to the development of an innovative application of Raman spectroscopy [Ledinský 2015, Ledinský 2016].

To complement our research on optimized heterocontact systems for back contacts, we investigated the role of the transparent electrode material properties. Earlier, they were shown to influence both transport and passivation properties at the heterocontacts. In our study we analysed, for different TCO materials, the impact of the film conductivity on the contact passivation quality. We found increasingly lower effective minority carrier lifetimes, at low excess carrier densities, for increasing TCO film conductivities in the hole contact [Tomasi 2015b, Tomasi 2016b]. Contextually, we found improved carrier transport, for increasing TCO film conductivities, at both the hole and electron contacts of our IBC-SHJ devices. Very importantly, we demonstrated the achievement of highly efficient charge-carrier transport in μc-Si:H-based heterocontacts [Nogay 2016]. These partially contrasting requirements make necessary a careful choice of the TCO thin-film material used in heterocontacts, and its electrical properties. The study of TCO influence on contact passivation was extended to non-conventional materials and brought interesting observations for the case of organic conductive overlayers. A manuscript, based on these findings, is in preparation [Seif 2016a].

Finally, we conceived a new device concept enabled by the innovative use of interband tunneling processes and by extremely thin doped μc-Si:H films. This solar cell architecture eliminates the need to pattern the hole-collecting layer and dramatically simplifies the challenges in back-contacted device fabrication. With this concept we demonstrated a best conversion efficiency of 22.9 %. A European patent application has been filed and a manuscript is under preparation [Tomasi 2016a].

We note that the work of this thesis contributed also to the application of Cu electroplating techniques to front-grid electrode fabrication in SHJ solar cells [Papet 2013, Geissbuhler 2014] and to the development of a 22.5 %-efficient two-side-contacted device, based on a novel passivating-contact technology [Geissbuhler 2015b].

Overall, these findings open up new perspectives with respect to the integration of passivating contact technologies in back-contacted architectures and, more generally, to the fabrication of back-contacted devices. The proposed *tunnel*-IBC-SHJ concept may realistically be the base for an industrially viable back-contacted SHJ technology.

2 Experimental details and methods

Abstract

This chapter introduces the solar cell fabrication technologies and the main characterization techniques used in this thesis. For each fabrication step, it gives credit to the partners who contributed to device processing. The experimental methods used to analyse fill factor and short-circuit current losses in our solar cells are also discussed.

Sections 2.3.1 is partially based on a paper published in IEEE Journal of Photovoltaics and adapted with permission from [Tomasi 2014a] (Copyright © 2014, IEEE). Section 2.3.2 is partially based on a paper published in IEEE Journal of Photovoltaics and adapted with permission from [Paviet-Salomon 2015a] (Copyright © 2015, IEEE).

2.1 Silicon heterojunction solar cells: fabrication technologies

The beauty of the two-side-contacted silicon heterojunction (SHJ) solar cell concept resides in its simplicity, combined with high performances. The few technologies required for its fabrication reflect this simplicity and are comprised within the following three categories:

  (i) wet-chemical processes,

 (ii) vacuum-based thin-film depositions and

(iii) metal printing techniques.

Wet-chemical processes are needed to texture and clean the crystalline silicon (c-Si) wafer surface (section 2.1.1). Thin-films are used to passivate surface defects, collect the photogenerated charge carriers in the c-Si absorber and transport them to the contacts (section 2.1.2). Eventually, metal printing techniques are required to fabricate the front-grid electrode (section 2.1.3). The back-contacted SHJ solar cells proposed in this thesis, are fabricated mostly with

the same fabrication technologies of two-side-contacted devices. Our intent was to develop a technology capable of overcoming the limits of conventional two-side-contacted SHJ solar cells while maintaining their most valuable aspect, i.e. the simplicity, untouched. The exact fabrication process is described in section 3.4 and chapter 4 for our IBC-SHJ technology, and in chapter 6 for our *tunnel*-IBC-SHJ solar cell. Compared to the case of two-side-contacted SHJ solar cells, hot melt inkjet printing is the only additional technique (section 2.1.4). It is used to structure the interdigitated metal/TCO electrodes at the back side.

In this thesis we deal exclusively with silicon heterojunction technologies based on n-type crystalline silicon (c-Si(n)) wafers. We use float-zone (FZ) silicon, with extremely high purity, which minimizes the impact of the substrate on device performance. Our 260-µm-thick n-type FZ wafers have a resistivity of about $3\,\Omega\,\text{cm}$, which corresponds to a density of phosphorous dopant atoms of $1.5\cdot10^{15}\,\text{cm}^{-3}$. Below we shortly introduce the fabrication technologies at points (i), (ii) and (iii) and inkjet printing.

2.1.1 Wet-chemical processes

Silicon wafers are sawn from ingots via multi-wire sawing and present micro-cracks in a surface layer with a depth of $10\,\mu\text{m}$ to $15\,\mu\text{m}$ [Wu 2012]. These structural defects make the wafers brittle and must be removed. This is done via wet-chemical etching in a potassium hydroxide solution. This etching step, being anisotropic, also results in an enhanced surface roughness with lower reflectivity, i.e. surface texturing. Once the saw-damage removal and the texturing process are completed, the wafers undergo additional wet-chemical cleaning steps and a final short dip, of around 60 seconds, in a diluted hydrofluoric solution.

In the case of our back-contacted SHJ devices, wet-chemical processes were also used to etch metal or transparent conductive oxide (TCO) films. In both cases we always used acidic solutions, based either on nitric or hydrochloric acid.

The wet-chemical processing for saw-damage removal and wafer texturing, was carried out at Meyer Burger Research AG and at the PV-Center of the Swiss Center for Electronics and Microtechnology (CSEM).

2.1.2 Thin-film deposition methods

a-Si:H, μc-Si:H and a-SiN$_x$:H

In SHJ technology, wafer surface passivation is obtained via an intrinsic a-Si:H layer (a-Si:H(i)). Then electron and hole collectors are formed by stacking a phosphorous-doped n-type a-Si:H (a-Si:H(n)) film and a boron-doped p-type a-Si:H (a-Si:H(p)) film on top of the intrinsic layer, respectively. All these a-Si:H films are deposited via plasma-enhanced chemical vapor deposition (PECVD). In this thesis, PECVD was used also to fabricate the a-SiN$_x$:H anti-reflection coating (ARC) at the front of our IBC-SHJ devices and the doped μc-Si:H films of chapters 5

and 6.

PECVD is a well-established technique for thin-film deposition, applied in research as well as in industry, and enables the deposition of an extremely wide range of materials. A PECVD reactor is typically composed of a heated vacuum chamber into which the desired gaseous molecules are injected and, by means of an electric discharge, decomposed into ions and radicals. Based on the type of excitation source, its frequency and the configuration of the electrodes, we can distinguish different types of PECVD processes and reactors.

In this thesis, we used parallel-plate PECVD reactors with high-frequency (13.56 MHz) or very high-frequency (40 MHz) power. The a-Si:H and μc-Si:H layers were deposited in three different PECVD reactors. A large-area PECVD reactor from TEL solar (KAI-M), a single-wafer research tool from INDEOtec (Octopus I) and a large-area system again from INDEOtec (Octopus II). Both Octopus I and Octopus II are cluster tools with several deposition chambers, which can be dedicated to a specific type of layer. The a-Si:H layers of the showcase devices IBC-SHJ[1] and IBC-SHJ[2] of chapter 4 were deposited in the KAI-M and Octopus II reactors, respectively. The a-Si:H films used in chapter 5 to study the influence of TCO on contact passivation were deposited in the KAI-M reactor. The a-Si:H layers used in the devices of chapter 6 were deposited in the Octopus II system, whereas all doped μc-Si:H films were deposited in the Octopus I reactor. The a-SiN$_x$:H film used as ARC was deposited in a different system, built in-house, operated at very high-frequency. For further details on these systems the reader can also refer to previous works [Seif 2015, Geissbuhler 2015a].

The a-Si:H layers of the Octopus II system were deposited at the PV-Center of CSEM.

Transparent conductive oxides and metals

TCO and metal thin films used in SHJ solar cells are typically deposited via sputtering. In this thesis, we relied mostly on sputtered indium tin oxide (ITO), aluminium-doped zinc oxide (ZnO:Al) and Ag thin films. Sputtering is a type of physical vapor deposition (PVD) method and is a well-established technique. In a sputtering process, a solid target, made of the material to be deposited, is bombarded by energetic ions. These collisions transfer momentum to the target atoms which, in part, are ejected from the material and are deposited onto the chamber wall and the substrate surface. The energetic ions originate from a plasma of the sputtering gas and are accelerated towards the substrate by an electric field. The sputtering gas is typically a mixture of an inert gas, such as Ar, and a dopant gas. In the case of ITO and ZnO:Al thin films, the dopant gas is oxygen. Tuning its partial pressure, it is possible to control the densities of oxygen vacancies in the deposited material and hence its conductivity. For further details on sputtered ITO and ZnO:Al thin films, please refer to [Buchanan 1980, Choi 1995] and [Minami 1984], respectively.

In this thesis, we used also boron-doped zinc oxide (ZnO:B) thin films. This TCO was deposited via low-pressure chemical vapor deposition (LPCVD), instead of sputtering. The advantage

is that LPCVD is an ultrasoft deposition technique that preserves pristine a-Si:H films. This allows contact passivation studies, such as in section 5.2, in the absence of sputter damage [Demaurex 2012]. Further details on the electrical and optical properties of ZnO:B films deposited by LPCVD can be found in [Wenas 1991]. Specific information on the deposition system and related methodology used in this thesis, can be found in [Faÿ 2005].

The deposition of the ZnO:Al thin films was performed at the PV-Center of CSEM.

2.1.3 Screen-printing of the front-grid metal contact

Screen-printing is a consolidated industrial technique which allows us to deposit thick metal layers according to a desired pattern geometry. The material to be printed must be in the form of a metal paste and is pushed through a metallic mesh onto the substrate surface. The pattern geometry is defined by an emulsion which coats the mesh in certain areas, acting as blocking layer for the metal paste. This is the standard technique used in the photovoltaic industry to fabricate the Ag front-grid electrode of solar cells. It shows technological limitations with respect to the minimum achievable finger width, and, due to the use of Ag, it contributes in large part to the solar cell fabrication costs. Nevertheless, thanks to its proven reliability and a continuous reduction in minimum achievable finger width and Ag usage, it has persisted as a mainstream technique in industry.

We note that the use of screen-printed metal combs in our back-contacted SHJ solar cells was not investigated in this thesis, but it is potentially applicable. The use of screen-printing would allow for the fabrication of bifacial back-contacted SHJ devices and thick IBC metal electrodes.

Screen-printing was performed at the PV-Center of CSEM.

2.1.4 Inkjet printing

Inkjet printing is a deposition technique used for liquid-phase materials. An inkjet printer is composed mainly of a printing head and the required mechanics for displacing it, accurately, over the substrate surface. In the printing head, the ink is filled into a chamber that contracts repeatedly in response to a voltage signal, applied to a piezoelectric element. This mechanical solicitation provokes the ejection of a liquid droplet through a nozzle and its deposition, by gravity, onto the substrate surface. There, the ink spreads and dries due to solvent evaporation. For a more in-depth analysis of the drop formation mechanisms, the interaction between the drop and the substrate, and the fluid properties and their effects on inkjet-printed patterns, please refer to [Derby 2010]. Hot melt inkjet printing, largely used in this thesis, is a variant of this technique where the material to be printed is a wax. The wax is heated inside the printing head until it becomes liquid. For a review of the various possible applications of inkjet printing, please refer to [Singh 2010]. For a recent review of possible applications in the specific field of c-Si solar cell fabrication, please refer to [Stüwe 2015].

Figure 2.1: Image of the inkjet printer "PiXDRO LP50" [MB 2013], from Meyer Burger (Netherlands) B.V., used in this thesis to fabricate the interdigitated TCO/metal electrodes of our IBC-SHJ and *tunnel*-IBC-SHJ solar cells.

The equipment we used in this thesis for inkjet printing is a "PiXDRO LP50" from Meyer Burger (Netherlands) B.V. (see Fig. 2.1). The system has the peculiarity of supporting different printing head technologies, which allows a great versatility. In our case we had two printing heads at our disposal: a "Spectra SE-128 AA" head for solvent-based inks and an "OCE CP Cobalt" head for hot melt materials. The Spectra SE-128 AA printing head, from Dimatix, is equipped with 128 nozzles of 30 pL and a diameter of 35 µm, and has a native resolution of 50 dpi. This head was used in the experiments of section 3.3.2 to print the water-solvable ink. The OCE CP Cobalt head instead has 256 nozzles of 29 pL, on two parallel rows, and a native resolution of 75 dpi. Based on the preparatory work of chapter 3, hot melt printing was chosen to be the fabrication technique for the TCO/metal electrodes of our back-contacted devices. Therefore, the OCE CP Cobalt printing head was used in the fabrication of all devices fabricated within this thesis. For further experimental details on the developed process, see also section 3.3.3. In addition, this head was also used in the experiments of section 3.3.4 to print a plating mask for the fabrication of the IBC Cu electrodes.

2.2 Characterization techniques

The key challenge of this thesis, is the fabrication of efficient back-contacted SHJ solar cells. Electrical and optical device characterization techniques, combined with loss-analysis methodologies (see section 2.3), are essential to achieve this goal.

To exploit all the characterization capabilities already available in the lab for conventional two-side-contacted SHJ devices, we designed a special contacting chuck for our back-contacted SHJ devices. The chuck is made from black-anodized aluminium and can contact 3×3 cm^2 back-contacted devices with two external bus bars (see Fig. 2.2 (a)). Each bus bar is contacted by four metal pins for current extraction (two at the bus bar ends and two close to the center) and one central pin for voltage measurement. The system is also provided with

17
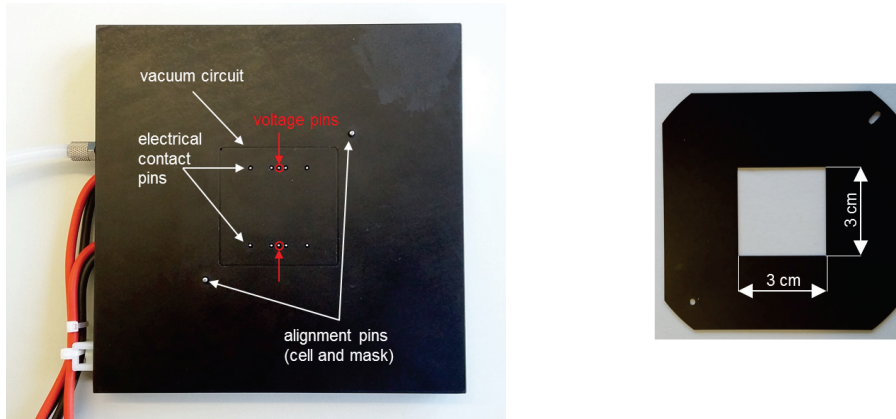
(a) Photograph of the measurement chuck for 3×3 cm^2 back-contacted solar cells with two external bus bars.

(b) Photograph of the 3×3 cm^2 mask defining the designated measurement area.

Figure 2.2: Specially developed equipment for the characterization of our 3×3 cm^2 back-contacted SHJ solar cells.

a vacuum circuit to guarantee good electrical contact, a thermocouple for monitoring the chuck temperature and alignment pins to ensure a good positioning of the solar cell. We also made a black-anodized aluminium mask to define the 3×3 cm^2 area designated for solar cell measurement (see Fig. 2.2 (b)). The shadow mask area is defined with an accuracy better than 0.05 cm^2.

Below, we give experimental details for some of the most important device characterization techniques used in this thesis, providing suitable references for more in-depth analysis. For charge-carrier lifetime and suns-V_{oc} measurements we extend the discussion to introduce some pertinent theoretical concepts. We remark that in our work, we also utilize several conventional material characterization techniques such as Hall effect measurements, spectroscopic ellipsometry, Raman spectroscopy, and confocal and electron microscopy.

Current-voltage characteristic

The measurement of the 1-sun current-voltage (I-V) characteristic of a solar cell allows us to assess its performance. From this curve we can extract important electrical parameters such as the open-circuit voltage (V_{oc}), the short-circuit current density (J_{sc}), the fill factor (*FF*) and the maximum power point (mpp) of the device. The I-V characteristics of our solar cells were measured in-house on a Wacom WXS-90S-L2 system using standard test conditions at 25 °C under 1-sun AM1.5G equivalent illumination. We defined a 3×3 cm^2 designated area using the shadow mask shown in Fig. 2.2 (b), which excludes the bus-bar area. The system is calibrated measuring a certified two-side-contacted reference solar cell. One of the back-contacted SHJ devices of chapter 6 was also certified at the qualified laboratory of CalLab (Fraunhofer ISE), confirming the accuracy of our in-house measurements. We also performed measurements of

solar cell characteristics at illumination intensities other than 1-sun and in dark conditions (dark I-V curves). Throughout the thesis, I-V curves measured with a neutral density filter that reduces J_{sc} to about 13 % of the 1-sun value, are referred as "*low-light I-V*".

Charge-carrier lifetime and suns-V_{oc}curve

In the field of c-Si wafer-based photovoltaic technologies, monitoring charge-carrier recombination processes at different steps of the device fabrication is essential and a well-established approach to device optimization. Two indispensable tools are the "Wafer-Lifetime" and the "Suns-V_{oc}" systems, from Sinton Instruments.

The "Wafer-Lifetime" tool measures, contact-less, the effective minority carrier lifetime (τ_{eff}) of a c-Si wafer over a wide range of excess minority carrier densities (Δn). This allows us to construct $\tau_{eff}(\Delta \mathbf{n})$ ***curves*** at each fabrication step, prior to metallization. The measurement is based on the quasi-steady-state photoconductance (QSSPC) method [Sinton 1996], developed by Sinton Instruments. A flash lamp is used to generate a certain Δn, in the c-Si wafer. Its evolution in time is monitored by measuring the wafer conductivity. The analysis of this photoconductance decay allows us to derive the $\tau_{eff}(\Delta n)$ curve. In this thesis, to access an extended Δn range (from $1 \cdot 10^{14}$ cm^{-3} to $1 \cdot 10^{16}$ cm^{-3}), we measured each sample in two distinct ranges (high $> 1 \cdot 10^{15}$ cm^{-3} and low $< 1 \cdot 10^{15}$ cm^{-3}), stitching together the two datasets to build the final $\tau_{eff}(\Delta n)$ curve. A certain value of wafer conductivity, or Δn value, implies a definite energy separation of the quasi-Fermi levels, for holes and electrons, within the c-Si absorber. To this energy difference corresponds a maximum attainable V_{oc}, for that specific illumination intensity, which is commonly referred to as implied-V_{oc} [Sinton 1996]. In QSSPC measurements each Δn is associated with a certain measured illumination intensity of the flash lamp; this allows us to construct suns-implied-V_{oc} plots. From this suns-implied-V_{oc} plot, by associating with each light intensity I_L (suns) and implied-V_{oc} value, a current value defined as $J = J_{sc}(1 - I_L)$, we can define implied I-V curves. The calculations and approximations required to move from one data set to the other are described in [Sinton 1996]. Applications of this procedure can be found, for instance, in section 5.2.3. The implied I-V curve is characterized by a certain implied-FF [Aberle 1993]. This parameter gives information about diode non-ideality FF losses arising only from charge-carrier recombination processes in the c-Si wafer and at its surfaces.

In ***suns*-V_{oc} *curves***, the V_{oc} of the solar cell is measured at varying illumination intensity. The light transient is generated with a flash lamp. In this case, to probe the solar cell V_{oc}, electrical contacts are required. This makes the technique applicable only to finished devices. From suns-V_{oc} curves, similarly as for the QSSPC data, associating with each light intensity I_L (suns), and the correspondent V_{oc} value, a current value $J = J_{sc}(1 - I_L)$, we can plot the so-called pseudo I-V curve [Sinton 2000]. These pseudo I-V curves are characterized by pseudo-V_{oc} and pseudo-FF (pFF) values.

In conclusion, as discussed above, both techniques allow us to derive best attainable I-V

characteristics at the specific fabrication stage of the measurement. The *potential* curves evolve over the various process steps converging towards the I-V characteristic of the final complete device. The second-to-last step is the pseudo I-V curve, which represents the final I-V characteristic measured on the full-processed device with no current flow, i.e. in absence of resistive losses. In the field of c-Si, research towards solar cell optimization is often conducted studying the evolution of these potential I-V curves. The literature covering these two techniques and their applications is wide. Their use is well-established in both academia and industry. The reader can refer to [Sinton 1996] and [Sinton 2000] for the QSSPC and the suns-V_{oc} technique, respectively.

Measurement of series and shunt resistance values [1]

A clear description and comparison of different methods to extract the series resistance (R_{series}) of a solar cell can be found in the work of Pysch *et al.* [Pysch 2007]. The R_{series} for our devices, if not specified otherwise, is extracted from the difference of the 1-sun I-V curve and the suns-V_{oc} curve at its mpp [Pysch 2007]. Another method, which we verified to be equivalent for our devices, is based on the comparison of the 1-sun I-V and dark I-V curve.

The value of shunt resistance (R_{shunt}) is extracted from the slope of a linear fit to the dark I-V characteristic, in the range (0,-100) mV.

In this thesis, resistance values normalized to the designated cell area are always indicated with the superscript N.

Quantum efficiency and other optical measurements

The external quantum efficiency (EQE) curves of the devices were measured using the IQE-SCAN system from PV-tools GmbH. The spot area is 2×2 cm^2. Solar cells were measured under a 0.5-sun light bias, at a chopping frequency of 230 Hz, unless otherwise specified. These settings ensure that there is < 2 % relative difference between the J_{sc} measured on the I-V setup and the one calculated from the EQE curve. The solar cells' reflectance (R_{cell}) and transmission (T_{cell}) spectra were measured using a Lambda950 spectrometer from PerkinElmer. The solar cell total absorbance (A_{cell}) is then calculated as $A_{cell} = 1 - (R_{cell} + T_{cell})$.

Light-beam-induced current measurements

Light-beam-induced current (LBIC) 1-D profiles were acquired with an in-house built setup. A laser beam with a diameter of about 100 µm and a wavelength $\lambda = 650$ nm is scanned over the solar cell surface, in short-circuit conditions. The stepper motor of the laser beam has a step resolution of about 8 µm. The LBIC profiles of our back-contacted SHJ devices were

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[1] Series resistance measurements extracted from fits of the I-V and dark I-V characteristic or from the slope of the I-V characteristic at voltages close to V_{oc} could give significantly different values.

taken over the entire 3-cm-wide active area, perpendicular to the hole- and electron-collecting finger and at a distance of 1 cm from the edge of the electron contact bus bar. The spatial resolution was fixed at 16 μm. For further details on the experimental setup the reader can refer to [Geissbuhler 2015a].

2.3 Experimental Methods

2.3.1 Analysis of solar cell fill-factor losses

Deviation of the 1-sun *FF* of a solar cell from its ideal value is generally the result of loss mechanisms related to charge-carrier transport as well as carrier recombination processes. Quantitative analysis of such *FF* losses is complex, and carrier-injection-level-dependent effects of these mechanisms can further complicate this type of study.

In the analysis of the solar cells presented within this thesis, we calculate *FF* series-resistance ($\Delta FF_{R_{\text{series}}}$) and shunt-resistance ($\Delta FF_{R_{\text{shunt}}}$) losses from measured R_{series} and R_{shunt} values. Then, from the difference between the measured solar cell *FF* and the series-and-shunt-resistance-affected *FF*, we estimate *FF* carrier-recombination losses ($\Delta FF_{J_0(n\neq n^*)}$). Comparing these *FF*loss term we evaluated the major loss mechanisms active in our devices and this guides our research. Their detailed calculation is described below. The solar cell *FF* measured from the I-V characteristic is retrieved by subtracting from an ideal *FF* (FF_0) value, the different losses according to:

$$FF = FF_0 - \Delta FF_{R_{\text{series}}} - \Delta FF_{R_{\text{shunt}}} - \Delta FF_{J_0(n\neq n^*)}. \tag{2.1}$$

FF_0 can be regarded as the *FF* of a single-diode I-V curve, of diode ideality factor n^*, offset by a value equal to the solar cell photogenerated current and intersecting the abscissa I = 0 A at a voltage equal to the V_{oc}. This function scales with increasing V_{oc} values and, for given temperature and n^* values, it depends only on V_{oc}. Practically, for a solar cell with a given V_{oc}, FF_0 represents the highest theoretically possible *FF*, assuming only the presence of recombination mechanisms with ideality factor n^*, where R_{series} equals zero and R_{shunt} is infinitely large. The value of FF_0 is calculated using the semi-empirical expression reported by Green *et al.* [Green 1982]:

$$FF_0 = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1}, \tag{2.2}$$

where v_{oc} is defined as $v_{oc} = V_{\text{oc}}/(n^* kT/q)$, where k is the Boltzmann's constant, T the absolute temperature and q the elementary charge. We note that FF_0 values, equivalent to those achieved with the semi-empirical expression of Green *et al.*, can be also calculated analytically, by using the Lambert W-function, or numerically [Khanna 2013].

The *FF* losses associated with R_{series} values ($\Delta FF_{R_{\text{series}}}$) can be calculated—see equations

2.3—from the ideal FF (FF_0) and the series-resistance-affected FF (FF_s), using for FF_s the semi-empirical expression reported by Green *et al.* [Green 1982]. It results:

$$\Delta FF_{R_{\text{series}}} = FF_0 - FF_s \quad with \quad FF_s = FF_0(1-1.1r_s) + \frac{r_s^2}{5.4}. \tag{2.3}$$

In this expression r_s is defined as $r_s = R_{\text{series}}/(V_{\text{oc}}/I_{\text{sc}})$, where I_{sc} is the short-circuit current of the solar cell. We remark that analogous results for $\Delta FF_{R_{\text{series}}}$ can be obtained also via analytical calculations [Khanna 2013].

Similarly as for $\Delta FF_{R_{\text{series}}}$, we can estimate the magnitude of FF losses associated with R_{shunt} by taking the difference between FF_s and the series-and-shunt-resistance-affected FF ($FF_{s,sh}$), using for $FF_{s,sh}$ the semi-empirical expression reported by Green *et al.* [Green 1982]. It results:

$$\Delta FF_{R_{\text{shunt}}} = FF_s - FF_{s,sh} \quad with \quad FF_{s,sh} = FF_s \cdot \left(1 - \frac{v_{oc}+0.7}{v_{oc}}\frac{FF_s}{r_{sh}}\right). \tag{2.4}$$

In this expression r_{sh} is defined as $r_{sh} = R_{\text{shunt}}/(V_{\text{oc}}/I_{\text{sc}})$. Alternatively, as for $\Delta FF_{R_{\text{shunt}}}$, we can use an analytical approach [Khanna 2013].

Once calculated $\Delta FF_{R_{\text{series}}}$ and $\Delta FF_{R_{\text{shunt}}}$ are calculated, we follow an approach similar to Khanna *et al.* [Khanna 2013] to estimate FF recombination losses. By considering the difference between $FF_{s,sh}$ and the measured FF (from 1-sun I-V measurements), we can calculate the FF losses due to recombination currents following ideality factors n, different from the value chosen for n^* (see Fig. 2.3 (a)). From equations 2.1, 2.3 and 2.4 it results:

$$\Delta FF_{J_0(n\neq n^*)} = FF_0 - \Delta FF_{R_{\text{series}}} - \Delta FF_{R_{\text{shunt}}} - FF = FF_s - \Delta FF_{R_{\text{shunt}}} - FF = FF_{s,sh} - FF. \tag{2.5}$$

In our FF-loss analysis, we consider the values of $\Delta FF_{R_{\text{series}}}$ and $\Delta FF_{R_{\text{shunt}}}$ calculated assuming $n^* = 1$ for FF_0 and, consequently, $\Delta FF_{J_0(n\neq1)}$. In the case of our FHC and IBC-SHJ devices, this approach is substantiated by the fact of dealing with "well-behaved" diodes with light and dark I-V characteristics that can be easily fitted with a classical two-diode model [Wolf 1963]. However, when very high-quality passivation is achieved, recombination during solar cell operation is driven mainly by radiative and Auger recombination, with the latter dominant. To account for this in the calculation of the ideal FF_0, the ideality factor should be set, in principle, to $n^* = 2/3$ [Hall 1981], yielding an increased ideal FF_0 value. We note that this increases the upper limit for the FF, but leaves the conclusions of the FF-loss analysis of our devices unchanged. From equations 2.2 and 2.4, we can also deduct the weak impact of FF_0 on $\Delta FF_{R_{\text{series}}}$ and $\Delta FF_{R_{\text{shunt}}}$. For practical V_{oc} values, assuming $n^* = 2/3$ instead of $n^* = 1$ increases the value of FF_0 of about 4 % absolute, but changes that of $\Delta FF_{R_{\text{series}}}$ by only < 5 % relative.

The overall picture, taking into account the different FF loss contributions, is schematically represented in Fig. 2.3 (a), for our FF-loss analysis, and in Fig. 2.3 (b), for the FF -loss analysis defined by Khanna *et al.* Importantly, in the representation of Fig. 2.3 (a), we see that FF_s corresponds, for a given device with a certain R_{series}, to the maximum attainable FF, for that
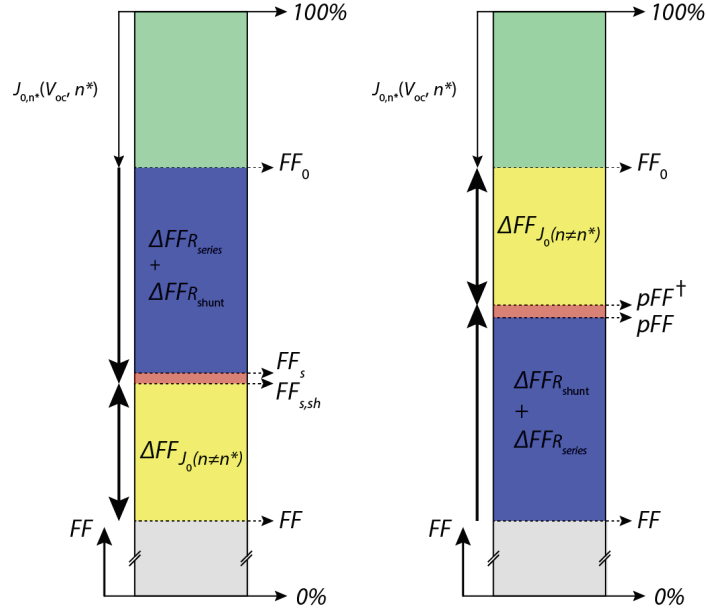
(a) Decomposition of *FF* losses in *FF* diode non-ideality losses and *FF* resistance losses as calculated in the *FF*-loss analysis of our devices. FF_s corresponds to the maximum attainable *FF*, used in chapter 4.

(b) Decomposition of *FF* losses in *FF* diode non-ideality losses and *FF* resistance losses according to the approach of Khanna *et al.* [Khanna 2013]. The value of $pFF^\dagger$, differently from *pFF*, is not lowered by the effect of R_{shunt}.

Figure 2.3: Schematic representation of different approaches to perform *FF*-loss analysis. They allow us to distinguish between diode non-ideality and carrier-transport-activated *FF* losses. The vertical arrows indicate how the calculation of the different *FF*-loss terms is performed (see also discussion in the text).

device. This concept of maximum attainable *FF* is widely used in chapter 4. In the approach of Khanna *et al*, the analytically calculated series-resistance-free *FF*, corresponds to the *pFF* value which can be obtained also from suns-V_{oc} measurements. Importantly, the $\Delta FF_{R_{series}}$ of Khanna *et al.* and that calculated as $\Delta FF_{R_{series}} = FF_0 - FF_s$ for $n^* = 1$ do not differ significantly. Typically $\Delta FF_{R_{series}}$ of Khanna *et al.* is slightly lower, but the difference is always $\leq 0.5\%$ absolute. One of the advantages of using methodologies as those described here to evaluate $\Delta FF_{R_{series}}$, with respect to looking at the difference $pFF - FF$, is the possibility to use different characterization techniques to measure R_{series}, and then estimate $\Delta FF_{R_{series}}$. We remark briefly on the fact that, in our devices, the described methodology, at 1-sun, is simplified by the negligible shunt-resistance contribution. This results in $FF_s \cong FF_{s,sh}$ and $pFF \cong pFF^\dagger$ for the case illustrated in Fig. 2.3 (a) and (b), respectively.

Eventually, we note that *FF* upper limit values can be extracted, as described in section 2.2, also from $\tau_{eff}(\Delta n)$ curves. Such implied-*FF* values, similarly to the *pFF*, do not include any transport-activated *FF* loss. However, they can be measured earlier in the processing sequence,

before contact formation, at different stages of the device fabrication process. This has the big advantage of allowing the separate evaluation of the effects of each additional processing step. Implied parameters, such as implied-*FF*, are widely used in the study of contact passivation in chapter 5. For the sake of clarity, throughout the entire thesis we explicitly use the prefix "implied-" for all quantities derived from carrier lifetime data.

Illumination-dependent *FF* measurements

An interesting approach, to widen our vision on the contribution of the different *FF* losses, is the analysis of illumination-dependent *FF* measurements. To achieve different illumination intensities in our I-V measurements, we used neutral density filters. The different *FF*-loss terms discussed above are modified by the illumination level and the corresponding photogenerated current. For each illumination level, based on the measured V_{oc} value, we can calculate FF_0. Thus, with the measured R_{series} and R_{shunt} values we can compute also FF_s and $FF_{s,sh}$. In Fig. 2.4 we report an exemplary two-side-contacted SHJ solar cell fabricated in our laboratory. At low illumination intensities, $\Delta FF_{J_0(n \neq n^*)}$ and, to a minor extent, $\Delta FF_{R_{shunt}}$ are the highest *FF* losses. Oppositely, at high illumination, $\Delta FF_{R_{series}}$ is the dominant *FF* loss. The competition between these different *FF*-loss contributions determine a maximum in the measured *FF*. Interestingly the illumination level at which this maximum occurs, higher or lower than 1-sun, can be taken as a first indicator of the dominant loss mechanism limiting the device 1-sun *FF*. The analysis of our solar cells using illumination-dependent *FF* measurements can be found in chapter 6.

2.3.2 Calculation of solar cell short-circuit current losses

To facilitate the discussion, in our J_{sc} loss analysis we distinguish between *internal* and *external* J_{sc} losses, as also proposed in [Holman 2013a], [Holman 2012] and [Wong 2015]. *Internal* losses result from light that is absorbed in the device, but is then either lost due to internal parasitic absorption (e.g. in the a-Si:H or the TCO layers), or whose generated carriers are lost due to imperfect collection. In contrast, *external* losses are optical losses that result from light that is not absorbed in the device (e.g. due to reflection or transmission losses), and thus does not generate any carrier. Below we report a discussion of each contribution to J_{sc} losses. For the sake of clarity, all these loss sources are also depicted in Fig. 2.5 and the corresponding formulas are reported in appendix B.

We calculated the *internal* J_{sc} losses in our SHJ solar cells by integrating the area between the EQE and the total absorbance curves (A_{cell}) over the AM1.5G solar spectrum. A_{cell} is calculated as $A_{cell} = 1 - (R_{cell} + T_{cell})$, where R_{cell} and T_{cell} are experimentally measured. The general expression for the calculation of the internal J_{sc} losses (J_{loss}) has the following form:

$$J_{loss} = \frac{q}{hc} \int_{\lambda_1}^{\lambda_2} \lambda \cdot \phi(\lambda) \cdot [A_{cell}(\lambda) - EQE(\lambda)] \cdot d\lambda \qquad (2.6)$$
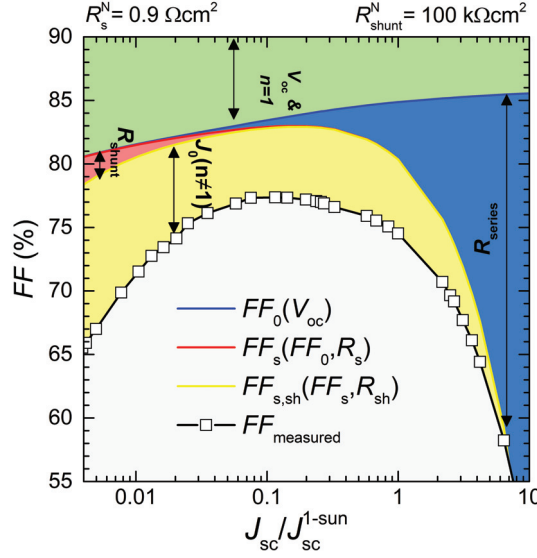
Figure 2.4: Illumination-dependent *FF* measurements ($FF_{measured}$) for an exemplary two-side-contacted SHJ device, fabricated in our laboratory. The terms of our *FF*-loss analysis are calculated for the different illumination levels, and indicated by coloured areas. The illumination level at which the maximum *FF* occurs, higher or lower than 1-sun, may be taken as an indicator about the prevalence of $\Delta FF_{R_{series}}$ or $\Delta FF_{J_0(n \neq n^*)}$ losses in the 1-sun characteristic of the measured device.

In equation 2.6, q is the elementary charge, h Planck's constant, c the speed of the light, λ the photon wavelength, and $\phi(\lambda)$ the AM1.5G solar spectrum. λ_1 and λ_2 are the outer bounds of the range for which the J_{loss} calculation is performed. The values of λ_1 and λ_2 are reported in appendix B. *Internal* losses can be broken down according to the specific region in which they occur. In our analysis, we discerned between short wavelength current losses, corresponding to the wavelength integration range between 350 and 600 nm (J_{short}), medium wavelength losses in the range 600 to 1000 nm (J_{medium}), and long wavelength losses in the range 1000 to 1200 nm (J_{long}). J_{short} hence accounts for the losses occurring in the ultraviolet and the blue part of the spectrum, J_{medium} in the visible range, and J_{long} in the infrared region.

Regarding *external* losses, we distinguish three different mechanisms. At the device front, part of the light is lost due to external reflection ($J_{reflection}$, commonly referred also as *primary reflection*). At the back side of the device, part of the long wavelength light is lost by transmission through the gaps between the back electrodes (escape light at the back, $J_{escape,back}$), whereas another part is internally reflected towards the front side, where part of it further escapes (escape light at the front $J_{escape,front}$, commonly referred also as *secondary reflection*). We used the OPAL software [Baker-Finch 2010] to calculate the theoretical reflectance (R_{OPAL}) and absorbance ($A_{OPAL} = 1 - R_{OPAL}$), for the front a-Si:H and ARC layer used in our devices. The refractive-index and absorption-coefficient spectra of our layers required for these simulations were acquired using a Horiba UVISEL ellipsometer. As OPAL assumes semi-infinite substrates, the simulated R_{OPAL} spectrum does not account for long wavelength light internally reflected
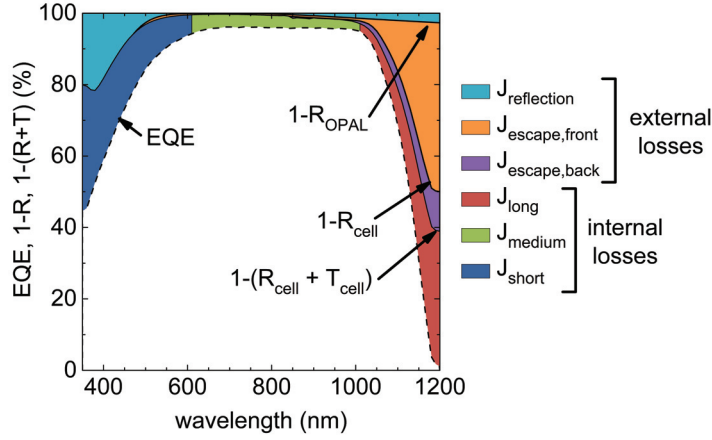
Figure 2.5: Illustrative example of J_{sc} loss sources in our IBC-SHJ solar cell. Reproduced with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE.

at the rear side of the wafer. Integrating the simulated R_{OPAL} we can thus calculate $J_{reflection}$. The comparison of R_{OPAL} to R_{cell} (see Fig. 2.5) allows now to separate the reflection losses due merely to the front stack from those due to the long wavelength light internally reflected at the back. In the case of the IBC-SHJ devices processed in our laboratory, the R_{OPAL} and R_{cell} spectra usually start to differ from 850 nm on. $J_{escape,front}$ is calculated by simply integrating the area between the R_{cell} and the R_{OPAL} curves at wavelengths > 850 nm. Subsequently, $J_{escape,back}$ is calculated by integrating the transmission curve of the cell. In the case of conventional two-side-contacted devices, an additional J_{sc} loss associated with front metal-grid shadowing must be considered ($J_{shadowing}$). This loss can be calculated from the difference between the J_{sc} value calculated by integrating the EQE curve, measured on an electrode-free device, and the 1-sun J_{sc}, measured on the actual device.

The integration of the AM1.5G spectrum over the range 350-1200 nm gives the total available photocurrent J_{ph}, which equals 45.9 mA cm^{-2}. This value represents the current that could be extracted from an infinitely thick device in the hypothesis that each photon in this spectral range generates one electron-hole pair that is successfully separated and collected. Subtracting the sum of all J_{sc} losses from J_{ph} we can retrieve the actual J_{sc} of our devices. Importantly, J_{ph} should not be considered as a maximum value for the achievable J_{sc} of practical devices. Detailed analysis of the theoretical limits of J_{sc} in solar cells can be found elsewhere [McIntosh 2014, Richter 2013].

3 Thin-film patterning and fabrication of interdigitated back-contacted silicon heterojunction solar cells

Abstract

This chapter presents experiments on thin-film patterning methods. We found that *in-situ* shadow masking is a suitable technique to pattern hydrogenated amorphous silicon thin-films and that with hot melt inkjet printing and wet-chemical etching is possible to fabricate accurate interdigitated electrodes. In the last part, we describe our original IBC-SHJ technology, providing experimental details on the fabrication process and the alignment methodologies.

3.1 Introduction and motivation

High-efficiency silicon solar cell architectures may feature one or more elements that do not uniformly occupy the entire device area. The realization of these elements requires the use of patterning techniques, which adds complexity to the fabrication process. Unfortunately, complexity often limits the appeal of technologies to industry. In this sense, the development of smart, robust and low-cost ways of patterning could be decisive in the evolution of mainstream silicon industrial technology. In the discussion below, we make references to solar cell architectures and technologies described in section 1.2. The typical "patterning problems", in solar cell fabrication, concern:

1. the fabrication of metal-grid electrodes,

2. the structuring of diffused layers and

3. the patterning of thin films.

A metal-grid electrode is used in any conventional two-side-contacted device and is fabricated, most typically, by screen-printing of a metal paste. Structured diffused layers are needed in two-side-contacted devices that employ optimized electron or hole collectors, such as selective emitters, and in back-contacted diffused-junction devices. The patterning of high-temperature diffused layers is not trivial. Typical approaches are based on the use of thin-film masks during the diffusion process, etch-back processes, ion implantation, localized dopant sources or laser-induced thermal processes. The last category includes various patterning problems. A typical problem arises with the use of dielectric passivating layers, which require openings for contact formation, as for instance in the PERC technology (see section 1.2). Importantly, this category comprises all patterning problems that can be encountered in the fabrication of back-contacted SHJ devices.

In the field of c-Si solar cells, the best-performing device architectures were already identified more than 25 years ago [Schwartz 1975, Lammert 1977, Swanson 1984, Blakers 1989, Wang 1990] (see discussion in section 1.2). However, the aluminium-diffused back-surface-field (Al-BSF) solar cell has always been the mainstream industrial technology. Only in the last few years have we witnessed a progressive shift to more advanced architectures using selective emitters [Hahn 2010] or, even more recently, the PERC concept [Green 2015]. This is mostly the consequence of a lack of cost-effective solutions for their fabrication. Importantly, for both selective-emitter- and PERC-based technologies, the development of a viable cost-effective industrial process depends on the solution of a patterning problem. In principle, however patterning is not a limitation. As briefly introduced already in section 1.2, even the mainstream Al-BSF c-Si solar cell incorporates a patterning process. The metal front-grid electrode contacts the diffused c-Si wafer surface, locally, through a dielectric passivation layer. The metal paste contains etching materials that, when thermally activated, open the dielectric layer and form the contact. This solution has become practically the only one adopted in the solar cell industry, and demonstrates that well-designed patterning processes are viable for industrial production. We can conclude that, from an industrial perspective, the way in which a certain advanced solar cell architecture can be fabricated is at least as important as its technological advances.

The case of back-contacted diffused-junction c-Si devices using IBC, MWT or EWT architectures (see section 1.2) is quite emblematic in this respect. The back-contacted architecture represents technologically the ultimate device concept for single-junction c-Si wafer-based devices. The gain in short-circuit current, brought by the absence of a front electrode, determines its fundamental superiority with respect to conventional two-side-contacted devices. However, the fabrication of these cells involves several complex patterning problems and only SunPower, CA, USA, following an industrial strategy different from all other photovoltaic manufacturers, has been able to develop the know-how needed to mass-produce them. Importantly, despite having one of the best products on the market, SunPower is evaluating different technologies for future capacity expansions. The implementation of back-contacted SHJ devices is an

opportunity to exploit, in a different manner, the technological advantage of back-contacted architectures. The whole patterning problem is reduced to thin-film patterning, which still is an added complexity, compared to planar devices, but it could possibly lead to smart and innovative processing solutions. The thin films to be patterned are doped a-Si:H, transparent conductive oxides (TCO) and metal films. As a starting point to define our own solution, in the next section, we revise some basic concepts for thin-film patterning.

In this context, it is worth mentioning that the integration of emerging passivating contacts [Battaglia 2014a, Bullock 2014, Feldmann 2014a, Geissbuhler 2015b] in back-contacted devices will pose very similar problems to the case of IBC-SHJ devices. Thin-film patterning will be again the main patterning problem and could open the path towards the definition of innovative and smart processing sequences for back-contacted devices.

3.2   Thin-film patterning concepts

We give here a quick non-exhaustive overview of thin-film patterning methods. It is restricted to those methods that have been considered, at least to some extent, within this thesis work. Except for the case of *in-situ* shadow masking, all of them can be implemented via inkjet printing or screen-printing techniques.

With respect to the target layer, i.e. the material layer that requires patterning, we can distinguish between *subtractive* and *additive* patterning methods. *Subtractive* methods consist in the full-area deposition of the target layer over the substrate and its subsequent selective removal. In contrast, *additive* methods are based on the direct printing, or deposition, of the target layer onto the substrate surface in the required pattern. Examples of *additive* methods are *in-situ* shadow masking, electroplating and target layer lift-off. An example of the *subtractive* method is etch resist printing and target layer wet-chemical etching.

In-situ shadow masking

This patterning method consists in interposing a shadow mask in between the deposition source and the substrate surface. This type of shadow mask is normally referred as an *in-situ* shadow mask. The deposition techniques and regime, the material of the mask, the mask thickness, the distance between the mask and the substrate surface and the distance between the deposition source and the masked substrate are all critical parameters of the process. They determine the target layer morphology and the overall patterning quality. Several problems can arise with the use of an *in-situ* shadow mask for thin-film patterning. These include thermal deformation of the mask, possible deposition under the mask, mask degradation and cleanliness after re-use, mask and substrate handling, physical contact mask-substrate and mask alignment to the substrate. Nevertheless, the approach is made strong by its simplicity and by the possibility to maintain a pristine interface between the target layer and the layer beneath.

Target layer lift-off

Figure 3.1: Schematic representation of the thin-film patterning method based on the use of a solvable material and target layer lift-off.

Target layer lift-off

This method consists of placing a solvable material directly on the substrate surface prior to deposition of the target layer. After deposition of the target layer, the sample must be immersed in a solvent that dissolves the solvable material and selective lift-off of the target layer. The phases of this patterning approach are presented in Fig. 3.1. The choice of the solvable material, and its chemical composition, are critical. The solvable material must be resistant to the temperature and pressure used for the deposition of the target layer. In addition, the morphology of the material deposited on the sample surface must guarantee an effective lift-off. "Mushroom"-shaped features help the solvent-agent to contact the solvable material and lift-off the target layer. The solvent-agent must be not harmful for the target layer itself and the layers beneath, if present.

Etch resist and target layer wet-chemical etching

This approach is based on the use of an etch resist material, which is deposited over the target layer according to the desired pattern. Via wet-chemical etching the target layer is then removed in the exposed areas that are not covered by the etch resist (see Fig. 3.2). The etching solution must be chosen from among those which the etch resist material can withstand. In addition, it must have a good etching selectivity between the target layer and the layers beneath, if present. Etch resists can be printed via hot melt inkjet printing or screen-printing. These techniques are commonly used in the printed circuit board (PCB) industry, and several products are commercially available. Most frequently, the etch resist materials must be removed from the final device. This requires a stripping procedure for the etch resist, which consists of sample immersion in a specific solvent. Possible harmful effects of the stripping solution on the various exposed materials must be considered.

Sacrificial-layer-based methods

Sacrificial-layer-based methods use a film of sacrificial material similarly to an etching resist or to a solvable material in lift-off processes (see Fig. 3.3). The sacrificial layer can be patterned with any method on top of the target layer and be used subsequently as a *hard mask* for wet-chemical etching, or it can be deposited and patterned directly on the substrate, before target layer deposition, and be used as a lift-off material. In Fig. 3.3, the sacrificial layer is

Etch resist and wet-chemical etching
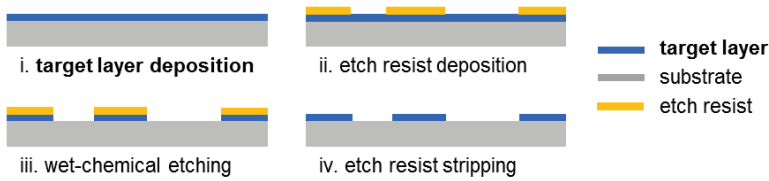
Figure 3.2: Schematic representation of the thin-film patterning method based on the use of an etch resist and target layer wet-chemical etching.
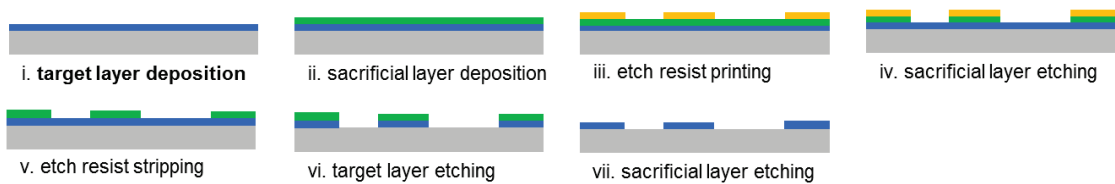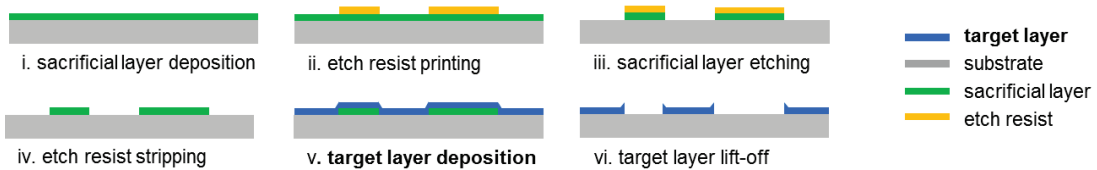
Figure 3.3: Schematic representation of sacrificial-layer-based patterning methods: hard mask and target layer wet-chemical etching (a) and target layer lift-off (b).

patterned via etch resist printing and wet-chemical etching. Most importantly, in the hard mask approach, the etching solution must etch selectively only the target layer material. Conversely, in the lift-off approach, it must etch selectively only the sacrificial layer material. Both approaches are more complex than the other patterning methods described above. Nevertheless, they have the advantage of being cleaner. The sacrificial layer may protect the target layer from contaminations or damages induced by direct patterning. In addition, in lift-off processes, hard mask materials may better withstand temperature and pressure conditions for target layer deposition.

Electroplating

Generally speaking, metals can be plated onto a conductive electrode via electro-induced plating metallization. Electroplating is an industrial technique that produces very high-quality materials and electrodes. Importantly, it can work as an effective self-aligned patterning method when a conductive material is surrounded by a non-conductive material. The ap-

proach is commonly exploited in the fabrication of metal electrodes for conventional diffused silicon solar cells, which employ dielectric passivation layers.

3.2.1 Applications to c-Si solar cell fabrication

Most of the described thin-film patterning concepts have been already applied, to some extent, to solar cell fabrication. The combination of hot melt inkjet printing with wet-chemical etching was shown to allow for high-quality electrical separation between patterned metal stripes, as those required in interdigitated back contacts. Over minimum distances of > 50 µm, the electrical resistance was measured to be >1 MΩ [Mingirulli 2009]. A hot melt inkjet printing and metal lift-off process was also tested, unsuccessfully, with the same purpose [Mingirulli 2009]. The etch resist and target layer wet-chemical etching approach was also applied to selective-emitter fabrication, via emitter etch-back, using both screen-printed [Song 2012, Haverkamp 2008] and inkjet-printed [Lauermann 2009] etch resists. The use of a sacrificial layer as a hard mask for wet-chemical etching was introduced in patterning for IBC-SHJ devices as a solution to the detrimental effects brought by direct patterning methods. The approach worked effectively [De Vecchi 2012a], in combination with laser ablation, and with etch resist screen-printing and wet-chemical etching, for patterning of the sacrificial layer itself. Cu electroplating has been used to fabricate solar cell front electrodes on large-area devices [Tous 2012]. For application to SHJ devices, certain difficulties must still be overcome but the applicability is proven [Hernandez 2013, Geissbuhler 2014, Papet 2013]. *In-situ* shadow masking was investigated as a technique to pattern hole- and electron-collecting layer stacks, or metal films, in IBC-SHJ devices [Spee 2008]. The technique was employed in device fabrication but, at the time of starting this thesis, with relatively moderate efficiencies up to a maximum of 15.7 % [Desrues 2011].

3.3 Experiments on selected thin-film patterning techniques

Our experimental work started with the investigation of a few selected thin-film patterning methodologies. Below we collect the most significant findings. Importantly, this preliminary investigation is the basis for the development of our original back-contacted *n*-type SHJ technology, of which main experimental details are presented in section 3.4. For further details on the exact equipment and printing head technologies used in inkjet printing applications, please refer also to section 2.1.4.

3.3.1 *In-situ* shadow masking

The use of *in-situ* shadow masks, in principle, permits patterning of any kind of film deposited via PECVD or PVD. However, the quality in structuring may vary strongly with the deposition technique, the deposition regime and the pattern geometry. Films deposited through an *in-situ* shadow mask slit do not present perfectly sharp edges [Spee 2008]. At the center of

Figure 3.4: Profilometer measurement of the a-Si:H(p) layer used in the device IBC-SHJ[1] (see section 4.5), deposited on a polished c-Si surface through a 1590-μm-wide mask slit. The orange areas represent the *in-situ* shadow mask, and the green area indicates the portion of the a-Si:H(p) layer with a thickness exceeding 80 % of the maximum thickness. The position of the 0 value on the x-axis is arbitrary.

the slit, the film deposition rate can be higher than it is close to the edges and, in addition, under-deposition "tails" in the masked areas may also be present. Hereafter we refer to these effects on the film morphology as *tapering* and *tailing* effects, respectively. Tapering is the result of shielding effects due to the proximity of the mask edges; part of the plasma radicals, which do not move perpendicularly to the substrate surface, cannot reach the deposition area and the film growth rate is reduced. Tailing effects instead are associated with radicals penetrating the space between mask and substrate surface; the type of substrate surface, polished or textured, and the adhesion between mask and substrate may play a role in this respect.

In the case of our *in-situ* shadow-mask-patterned a-Si:H, TCO and metal films, we can observe both tapering and tailing effects. An explicative thickness profile, for the a-Si:H(p) film used in the device IBC-SHJ[1] (see section 4.5), deposited on a c-Si polished surface through a mask slit 1590 µm wide, is given in Fig. 3.4. In this illustration we compare the width of the mask slit, measured by an optical microscope, with the morphology of the deposited film and distinguish tailing effects of about 100 µm at each side, and tapering effects extending few hundreds of microns away from the mask edges. Below, we present a detailed analysis of the morphology of a-Si:H films deposited through *in-situ* shadow mask slits of different widths on polished and textured c-Si surfaces. The textured surface required the development of a specially developed characterization technique, based on Raman-scattering measurements [Ledinský 2016].

Importantly, the patterns achievable with *in-situ* shadow masking are limited by the mask mechanical strength and by the mask fabrication process. For the fabrication of our masks we laser-cut masks from 250-μm-thick double-side-polished c-Si wafers. Based on the equipment at our disposal, we can consider, as the practical minimum limit, a 0.5-mm-wide slit.
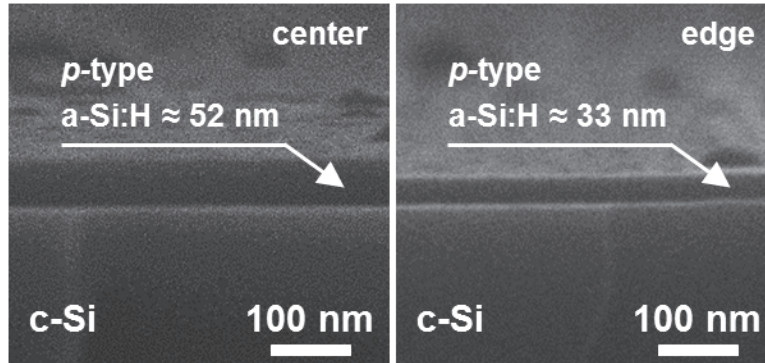
Figure 3.5: SEM cross sections of a thick a-Si:H(*p*) layer on a polished c-Si wafer, patterned via *in-situ* masking, close to the center (left image) and edge (right image) of the deposited layer, respectively. Reproduced with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

In-situ shadow-mask-patterned a-Si:H layers on polished c-Si surfaces

The characterization of a-Si:H thin-film morphologies, resulting from the use of *in-situ* shadow masks, is not trivial. We need high resolution in height but position measurements over wide distances. By SEM cross-sectional observations, see Fig. 3.5, we first observed a different a-Si:H(*p*) film thickness at different positions in respect to the mask edges. Then, by means of high-resolution profilometry measurements we proceeded to a more systematic and quantitative analysis.

In this experiment, we considered mask slit widths (w) in the range of 0.8 mm to 2.2 mm, the a-Si:H(*p*) layer used in the device IBC-SHJ[1] and a c-Si substrate with a polished surface. We measured the resulting thickness profiles for an a-Si:H(*p*) layer deposited, simultaneously, through all the slit widths. For each profile we evaluated the maximum film thickness, as well as tapering and tailing effects. The maximum film thickness was extracted from the acquired height profile smoothed by an adjacent-averaging algorithm. Tapering and tailing effects were quantitatively assessed measuring the width of the film portions exceeding 80 % (w_{80}) and 5 % (w_5) of the maximum film thickness, respectively. The maximum film thickness occurs close to the center of the mask slit and appears to diminish with decreasing w (Fig. 3.6 (a)). Practically, going from a 2-mm- to a 0.8-mm-wide slit means halving the film deposition rate. Conversely, the shape of the height profiles looks to be independent of w. The quantity $(w-w_{80})/2$, which can be taken as an indication for the extent of film tapering effects, increases from 100 μm to about 250 μm for wider slits, i.e. higher w, but the relative difference $(w-w_{80})/2 \cdot 1/w$ is roughly constant, between 10 % and 15 % (see Fig. 3.6 (b)). This indicates that a broad portion of the deposited film, of about 10 % to 15 %, around the edges of the pattern is significantly thinner than in the rest of the deposited surface. The width of the under-deposition tails, evaluated as $(w_5-w)/2$, is independent of w (see again Fig. 3.6 (b)). This implies that their width relative to w, i.e. $(w_5-w)/2 \cdot 1/w$, increases from 4 % to 12 % for narrower slits.

In section 4.4 we will discuss the most important implications of these observations with
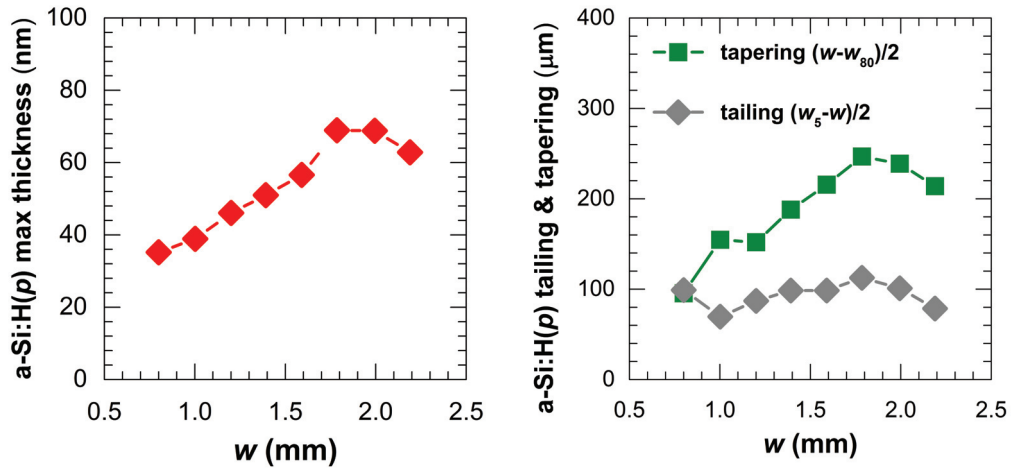
(a) Maximum a-Si:H(p) film thickness measured for different mask slit widths (w).

(b) Tapering and tailing effects as function of mask slit width (w). The metrics are based on the width of the a-Si:H(p) film portions exceeding 80% (w_{80}) and 5% (w_5) of the maximum film thickness, respectively.

Figure 3.6: Analysis of film morphologies for a-Si:H(p) deposited on a c-Si substrate with a polished surface through *in-situ* shadow mask slits of widths ranging from 0.8 mm to 2.2 mm. Thickness profiles are measured by a high-resolution profilometer.

respect to our IBC-SHJ solar cells.

In-situ shadow-mask-patterned a-Si:H layers on textured c-Si surfaces

The extension of the experiment discussed above to textured c-Si surfaces is relevant to device applications. Unfortunately, due to the textured surface roughness, this is not possible to measure by means of profilometry measurements. To circumvent this problem, a new method for thin-film profiling on rough surfaces, based on Raman micro-spectroscopy measurements [Ledinský 2016], was developed. This approach evaluates the Raman scattering intensity of the silicon wafer substrate c-Si peak, attenuated by the absorption of the excitation laser (λ = 442 nm) and the back-scattered Raman photons in the a-Si:H film only. A detection limit below 1 nm, for the a-Si:H film thickness, and a lateral resolution of about 500 nm could be demonstrated. In Fig. 3.7 we report the a-Si:H thickness map measured by "Raman profilometry" on a textured wafer, for a test a-Si:H(p) layer deposited through the series of mask slit widths from 0.8 mm to 2.2 mm. By means of this technique we repeated the previous experiment on a textured c-Si surface. Again the overall a-Si:H(p) deposition rate, at the center of the mask slit, is lower for the narrower slits, whereas tapering effects interest a fixed fraction of the mask slit width.

Importantly, the developed Raman-based technique can be applied also to non-absorbing materials, as for instance MoO$_x$, exploiting differences in optical reflection. Interestingly,
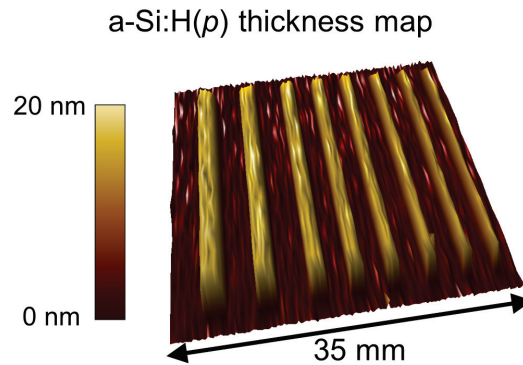
Figure 3.7: "Raman profilometry" maps of a-Si:H thin-film thickness, measured on a textured c-Si wafer. The a-Si:H thin-film was deposited via PECVD and patterned with the use of *in-situ* shadow masking. Reproduced with permission from [Ledinský 2016].

for the case of an efficient hole-collecting MoO_x layer [Geissbuhler 2015b] patterned via *in-situ* shadow masking, we were able to detect much sharper edges than for the case of our a-Si:H(p) layers. This is most likely the result of using thermal evaporation, rather than PECVD, as the deposition technique. This finding is valuable with respect to the integration of emerging passivating contact technologies, based on layers deposited via thermal evaporation [Battaglia 2014a, Bullock 2014, Geissbuhler 2015b], in next-generation back-contacted architectures.

In-situ shadow masking of TCO and metal films

In the case of TCOs and metals, we also observed imperfect film morphologies when patterning via *in-situ* shadow masking. For the case of a 100-nm-thick ITO layer, we can easily observe, with an optical microscope, changes in color 200 µm to 300 µm from the edges of the patterned area. This variation of color, determined by optical interference effects, is a direct indication of a changing ITO thickness.

We did not proceed further in the investigation of this approach. The reasons are multiple: first we were able to develop an effective alternative TCO/metal patterning technique based on hot melt inkjet printing (see section 3.3.3). Secondly, repeated PVD processes result in mask warping, which prevents mask re-use. Thirdly the realization of the full TCO/metal electrode poses practical problems due to the pattern geometry. The metallization mask, with both *p-* and *n*-combs, is very fragile and patterning one comb per deposition would require 4 deposition steps for the fabrication of the back electrode alone. Our use of *in-situ* shadow masks for patterning TCO films is limited to specific experiments in which we wanted to differentiate the TCO materials used for hole and electron contacts (see section 5.3.2 and section 5.3.3).

3.3.2   Inkjet printing and lift-off

Here we report on the use of inkjet printing to lift off different types of target layer. We chose a water-solvable ink, motivated by the potential advantages of a mild water-based lift-off process. At first, an effort was required to gain control over the morphology of the printed features and improve ink printability. Subsequently, we attempted layer lift-off of hydrogenated amorphous silicon nitride (a-SiN$_x$:H), ITO and ITO/Ag target layers. The 40-nm-thick a-SiN$_x$:H film was included in this investigation as candidate sacrificial layer for a-Si:H patterning. The ITO/Ag layer stack is that typically used in SHJ back electrodes. We considered both textured and polished c-Si substrates.

In inkjet printing the water-solvable ink, we experienced delays in jet start-up and frequent nozzle clogging problems. In addition, we observed a strong accumulation of the ink on the sides of the printed lines, the so-called coffee-ring effect [Deegan 1997]. Such coffee-ring effects are produced by differences in the evaporation rate (between sides and center of a printed drop) and capillary flow and are a known problem for solvent-based inks. As shown in case **(i)** of Fig. 3.8, the printed lines were depleted in the center resulting in almost no ink coverage at all. For lift-off processes, an uniform ink layer, ideally mushroom shaped, is desirable. Thus ink morphologies that result from strong coffee-ring effects, are inappropriate for application in lift-off processes. Fortunately, different ink solid contents, substrate temperatures, printing strategies or solvent compositions can mitigate coffee-ring effects [Kim 2006, Soltman 2008, Tekin 2004, Smith 2006]. By increasing the substrate temperature [Soltman 2008] and adding (1,2)-propandiol, an high-boiling-point solvent, to the ink chemistry [Kim 2006], we were able to suppress coffee-ring effects and improve the ink printability. With the adapted ink formulation we achieved the ink lines shown in case **(ii)** of Fig. 3.8, and we attempted thin-film patterning.

Lift-off of a-SiN$_x$:H thin films

We examined the case of an a-SiN$_x$:H layer with the aim to probe it as candidate sacrificial layer and to gain insights into the feasibility of direct inkjet lift-off processes for PECVD layers. a-SiN$_x$:H is a good sacrificial layer candidate as it can be easily etched in HF, differently from a-Si:H. Importantly, similar conditions (pressure and temperature) are used for the deposition of a-SiN$_x$:H and a-Si:H layers. This allows us to extend some of our findings for a-SiN$_x$:H to a-Si:H layers.

We inkjet printed thick ink layers on both polished and textured c-Si substrate surfaces, on top of which we deposited a 40-nm-thick a-SiN$_x$:H film via PECVD. By microscope inspection we observed cracks in the ink layer after a-SiN$_x$:H film deposition. Poor ink thermal resistance was the most likely cause of this phenomenon. As a result, after immersion of both textured and polished samples in water and ink dissolution, we achieved poor-quality a-SiN$_x$:H layer lift-off. The edges of the lift-off area were not sharp and the target layer removal was incomplete. We found remaining stripes of material in the lift-off area. The measured thickness, on the

(a) Optical microscope images of inkjet-printed lines.

(b) Profilometer measurements of inkjet-printed line cross-sections.
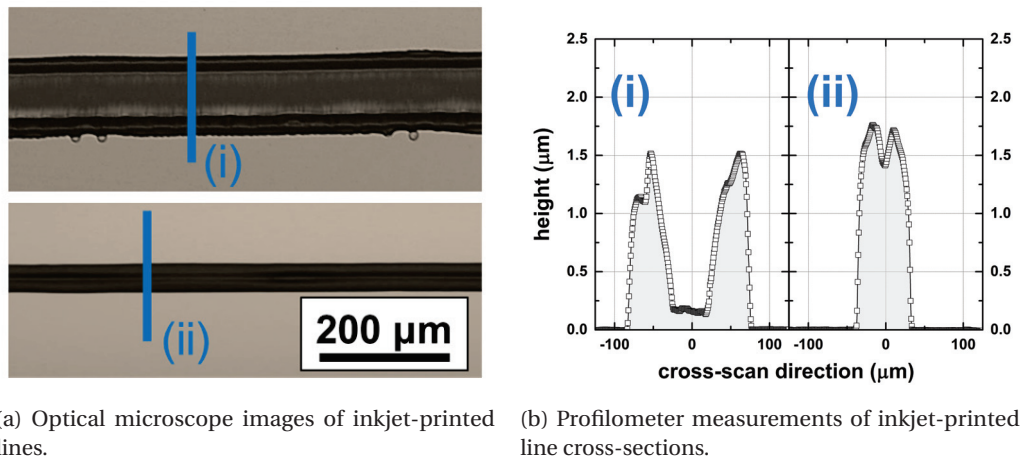
Figure 3.8: Characterization of inkjet-printed lines for different substrate temperatures, print parameters and ink chemistries. In case **(i)** the ink line presents coffee-ring effects [Deegan 1997]. In case **(ii)** the coffee-ring effects are almost totally suppressed and a minimum ink layer thickness of ≥ 1.5 μm is achieved for an ink line width of about 60 μm.

polished samples, was equal to the a-SiN$_x$:H film thickness, indicating that the ink cracks form at the beginning of the deposition process and that a-SiN$_x$:H is deposited, through the cracks, directly onto the substrate surface. The overall problem of a-SiN$_x$:H patterning is visualized in Fig. 3.9.

Despite the potential simplicity of this approach, based on these preliminary results, we judged it to be inappropriate for application to a-Si:H or for sacrificial layer patterning and we disregarded it for integration in our IBC-SHJ technology. The validity of this conclusion is limited to the specific ink formulation we used in our experiments.

Lift-off of ITO/Ag film stacks

We approached the problem of TCO and metal thin-film patterning considering the electrode used at the back of our front-hole-collecting (FHC) SHJ solar cells, which consists of a 200-nm-thick ITO film capped by a 300-nm-thick Ag film [Holman 2013b]. Lift-off patterning was attempted first on each layer separately and then on the full layer stack. In contrast to a-SiN$_x$:H, here we did not observe stripes of the target layer remaining after lift-off. Clean lift-off and effective electrical separation between the patterned ITO/Ag lines was achieved on both polished and textured samples. As shown in Fig. 3.10 (a), ink cracks are visible at the end of the deposition process. However, they form a network of unopened cracks, which avoids the direct deposition of the target layer on the c-Si surface. Our hypothesis is that the ink cracks develop at a later stage of the deposition process and therefore do not compromise the entire process. We fabricated full 3×3 cm^2 IBC electrodes with ITO (see Fig. 3.10 (c)), and ITO/Ag layers (see Fig. 3.10 (d)). The preliminary IBC geometry shown here has an

(a) Optical microscope image of a uniform ink layer after inkjet printing on a polished c-Si surface.

(b) Optical microscope image of the ink layer cracks after a-SiN$_x$:H deposition.

(c) Optical microscope image of the polished c-Si surface after ink dissolution and a-SiN$_x$:H lift-off.

(d) Profilometer measurement of a remaining a-SiN$_x$:H stripe after lift-off. The measurement was taken along the blue line of (c).
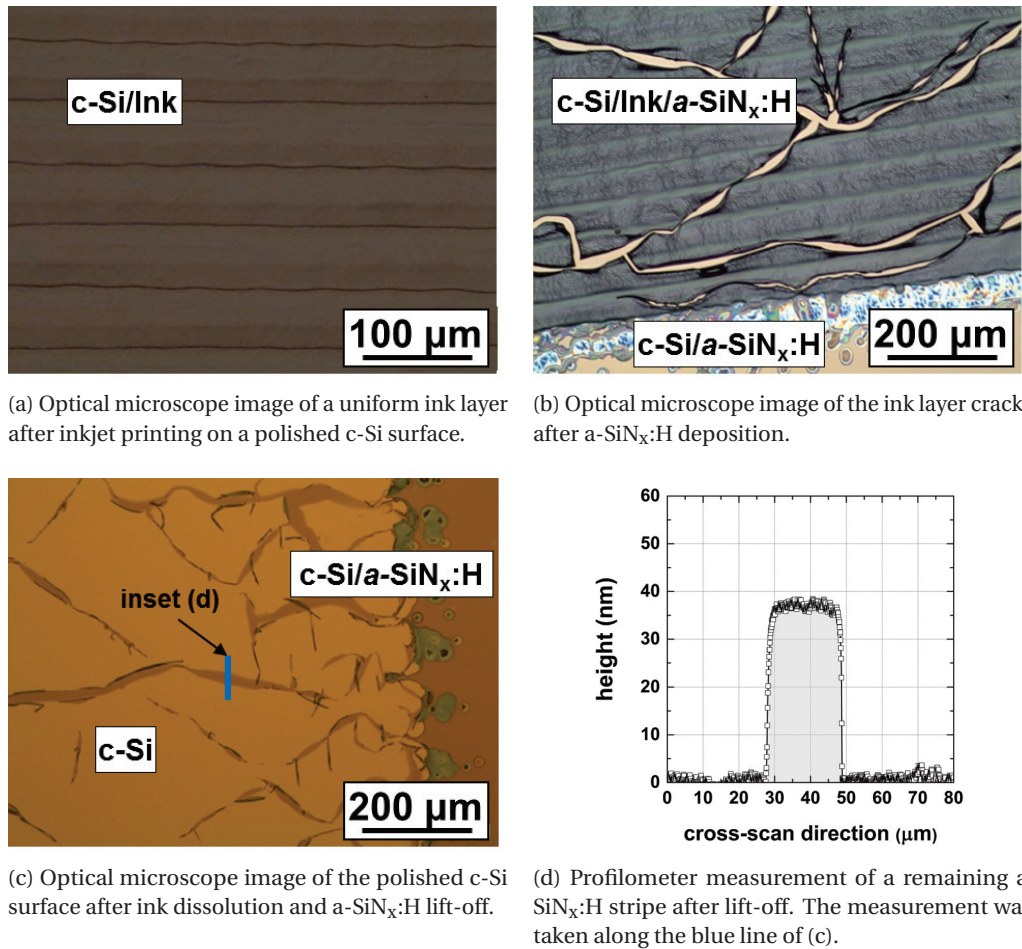
Figure 3.9: Optical microscope images (a)-(c) and profilometer measurements (d), showing the problems encountered in patterning a 40-nm-thick a-SiN$_x$:H film via inkjet printing and target layer lift-off.

IBC-pitch of 3.49 mm and the gap between the two interdigitated electrodes is around 400 µm. Macroscopic results are relatively good but, under a more careful examination, the edges of the back electrode are poorly defined (see Fig. 3.10 (b)). This is due to ink spreading effects, which in addition limit the minimum distance between the two electrodes. Ink spreading depends mainly on the substrate roughness but it can be reduced by using a different printing head technology with smaller nozzle volumes.

The limitations attributed to ink spreading and poorly defined edges, combined with an overall process quality that is sensitive to changes in the ITO and Ag layer thickness, or substrate surface roughness, brought us to conclude that this approach was not suitable for integration in our IBC-SHJ technology. As a result, the back electrodes of only the first few IBC-SHJ devices, which showed conversion efficiencies of about 10 %, were processed in this way.
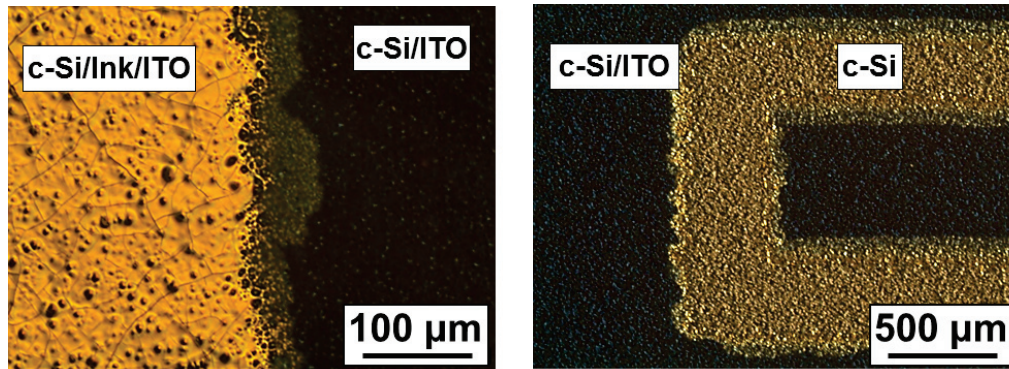
(a) Optical microscope image of the ink layer after ITO deposition on a textured c-Si surface.

(b) Optical microscope image of an ITO back electrode patterned via inkjet printing and lift-off on a textured c-Si surface.
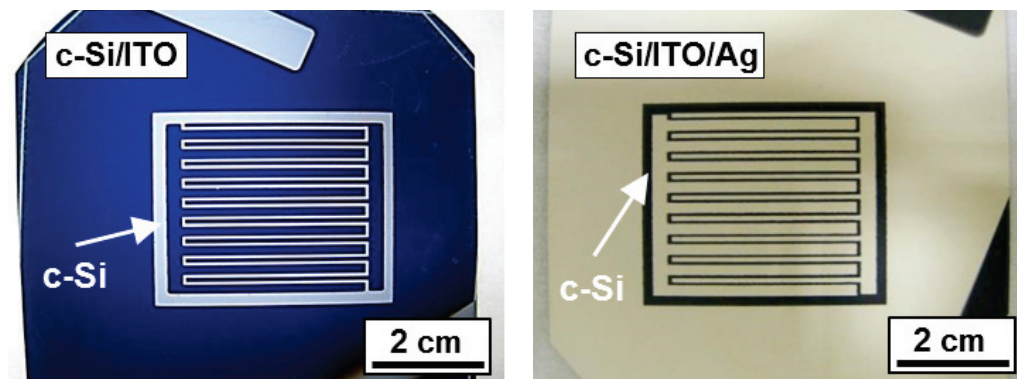
(c) Photograph of 3×3 cm^2 ITO electrodes for IBC-SHJ devices, patterned on a 4-inch textured c-Si wafer.

(d) Photograph of 3×3 cm^2 ITO/Ag electrodes for IBC-SHJ devices, patterned on a 6-inch textured c-Si wafer.

Figure 3.10: Optical microscope images (a)-(b) and photographs (c)-(d) illustrating the fabrication of IBC-SHJ back electrodes via inkjet printing and ITO/Ag lift-off.

3.3.3 Hot melt inkjet printing and wet-chemical etching

Here we report about the use of hot melt inkjet printing, combined with wet-chemical etching, for patterning various type of target layers. As for the case of inkjet printing and lift-off, we consider TCO/metal stacks and candidate sacrificial layers. Again we consider both polished and textured c-Si surfaces.

For hot melt printing we used an OCE CP Cobalt printing head which technology is very special. The printing head has 256 nozzles, each with a capacity of 29 pL, and is equipped with a control mechanism that independently probes the status of each nozzle. This dramatically increases the system reliability and makes it suitable for industrial processes [Hermans 2012]. Hot melt materials, at room temperature, are in the form of a wax. Once heated they become liquid and can be inkjet printed. In our case, the head operating temperature is higher than 95 °C and the jetting frequency is over 10 kHz. A whole 6-in wafer can be printed in few

(a) Optical microscope image of the *wet-on-wet* hot melt inkjet-printed etch resist.

(b) Profilometer measurement of the *wet-on-wet* hot melt inkjet printed etch resist of (a), along the blue line.

(c) Optical microscope image of a 22-μm-wide line opening, in a *wet-on-wet* hot melt inkjet-printed etch resist.
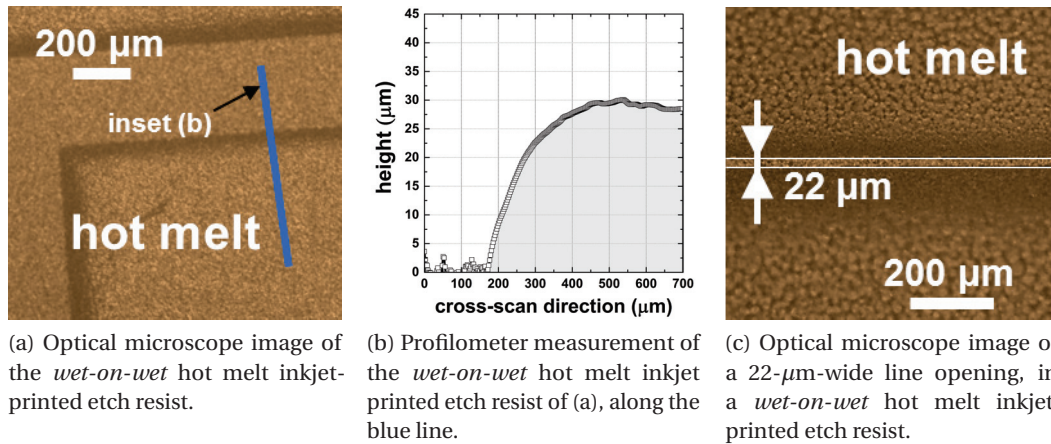
Figure 3.11: Optical microscope images (a) and (c), and profilometer measurement of an etch resist printed via *wet-on-wet* hot melt inkjet printing, on top of a textured c-Si wafer coated by a TCO/metal layer stack.

seconds. The hot melt material we used is a commercial product which resists acids such as HF, HNO_3 and HCl. To strip it, after use, it is sufficient to immerse of the sample for few minutes in a hot solvent such as isopropyl alcohol or acetone. The compatibility of the hot melt and the stripping procedure, with passivating a-Si:H layers, was preliminary assessed by performing hot melt inkjet printing, HF dipping and solvent stripping on a passivated polished c-Si wafer and taking photoluminescence (PL) images at each step. These images showed detrimental effects that were considered not critical. In hot melt inkjet printing, the jetted material solidifies very rapidly in contact with the substrate surface at room temperature (or below). This fast solidification minimizes the spreading of the material and print deformation effects.

To achieve an effective, uniformly thick etch resist via hot melt inkjet printing, it is necessary to use a so-called *wet-on-wet* printing strategy. Adjacent drops in the print must reach the substrate surface within a time interval shorter than the time for solidification. In this way they constitute a unique liquid media that solidifies as one and forms a uniform etch resist. This is obtained by rotating the printing head so that the projection of the nozzle positions on one axis matches the print resolution on the same axis. In this way, as shown in Fig. 3.11 (a) and (b), the hot melt forms a flat layer 30 to 40 μm thick. With our system, using a *wet-on-wet* printing strategy, we can achieve printed features with a minimum size ≥ 35 μm. As shown in Fig. 3.11 (c), this translates into minimum opening sizes in the hot melt etch resist as small as 20 μm [Hermans 2013].

Wet-chemical etching of TCO/metal film stacks

We defined a *wet-on-wet* printing strategy for interdigitated electrodes with a separation of about 300 μm and printed the etch resist on top of an ITO/Ag layer stack. In the case of both

(a) Hot melt inkjet-printed etch resist on top of a textured c-Si(n) wafer coated by a thin a-Si:H film and a TCO/metal layer stack.

(b) Hot melt inkjet-printed etch resist, on top of a textured c-Si(n) wafer coated by a thin a-Si:H film and a TCO/metal layer stack, after wet-chemical etching of the TCO and metal layers.

(c) Interdigitated TCO/metal back electrodes used in our IBC-SHJ devices.
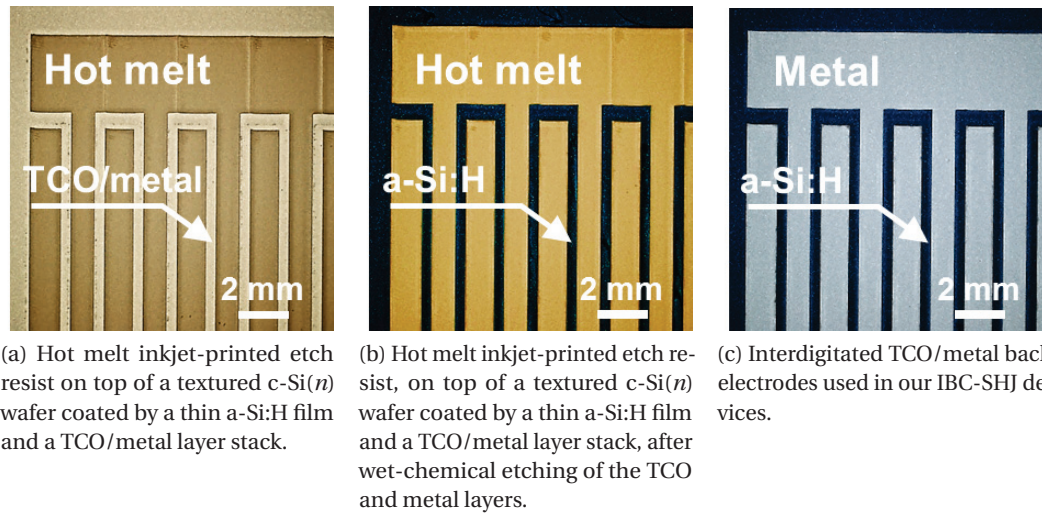
Figure 3.12: Optical microscope images (a)-(c) illustrating the fabrication process of the TCO/metal back electrodes of our IBC-SHJ devices via hot melt inkjet printing and wet-chemical etching.

polished and textured c-Si surfaces we obtained excellent print quality and definition. Thus we applied a two-step etching process; a few seconds in diluted HNO_3, sufficient to remove the Ag layer and expose the ITO film beneath, and about 3 minutes in diluted HCl to remove the ITO film. The hot melt was then dissolved in a hot solvent, leaving no residuals on the substrate surface. Under-etching of the ITO layer was sometimes present, and was, suppressed by optimizing the etchant chemical concentrations and etching times. The fabricated electrodes were of good quality, with sharp and clean edges. The overall process was judged to be very promising for IBC-SHJ solar cell back-electrode fabrication. Most of the devices presented in this thesis, if not specified otherwise, make use of back electrodes fabricated via hot melt inkjet printing and wet-chemical etching, as described here. The overall fabrication process is visualized in Fig. 3.12.

To implement TCOs and metals other than ITO and Ag, we developed few additional etching procedures. The use of Zn-based TCOs and Ag as the metal layer is particularly convenient, as a single quick etching step in diluted HNO_3 is sufficient to pattern the electrodes. In general, such TCOs are easily etched in acidic solutions, and a single-step process is also possible when they are combined with other metal layers, such as Al.

Geometrical accuracy, in the fabrication of IBC-SHJ back electrodes is very important. We identified systematic errors, accumulating along the different process steps. We compensated for these errors redefining the geometry of the initial print. Such errors arise for example in the digitalization of the back-electrode design, which is made necessary by the use of inkjet printing. These errors cannot be larger than the print resolution, which is typically around 900 dpi, i.e. $\leq 20\,\mu m$. Of the same magnitude is the error caused by hot melt spreading, which tends

to reduce the size of the etch resist openings. Conversely, under-etching counterbalances this effect increasing the size of the etched features. These effects vary according to the specific TCO/metal stack used. However, they can be normally reduced to values $\leq 15\,\mu m$. Considering all these major sources of errors, we achieved a good control in the fabrication process of interdigitated back electrodes to an overall precision in the range of $10\,\mu m$ to $20\,\mu m$.

Wet-chemical etching of a-SiO$_x$:H and a-SiN$_x$:H layers

Unlike a-Si:H, a-SiN$_x$:H and hydrogenated amorphous silicon oxide (a-SiO$_x$:H) can be easily etched in HF, and both can resist KOH etching much better than a-Si:H. Such properties make them good candidates as sacrificial layers for a-Si:H lift-off and as hard masks for a-Si:H etching. With these final applications in mind, we addressed the problem of their patterning with hot melt inkjet printing and wet-chemical etching. We printed an etch resist with line openings of 1 mm, mimicking the electron-collecting comb of our back electrodes. a-SiO$_x$:H or a-SiN$_x$:H films etched with this geometry could be used to lift-off the a-Si:H(n) layer, in the area where the a-Si:H(p) has to be placed, or, alternatively, as a hard mask for removing the a-Si:H(p) layer in the area where the a-Si:H(n) has to be placed.

We consider a 300-nm-thick a-SiO$_x$:H layer and an a-SiO$_x$:H/a-SiN$_x$:H stack in which the film thicknesses were 300 nm and 80 nm, respectively. For lift-off, the edges of the patterned sacrificial layer should be as steep as possible to facilitate dissolution of the sacrificial layer and detachment of the target layer from the substrate. The a-SiO$_x$:H/a-SiN$_x$:H stack aimed at an increased edge steepness, compared to the case of a single-layer stack, exploiting the different etch rates of a-SiN$_x$:H and a-SiO$_x$:H in HF [Desrues 2009]. The hot melt etch resist showed a good resistance to HF and we achieved well-defined geometries, on both textured and polished c-Si surfaces. We observed the desired increases in edge steepness for the a-SiO$_x$:H/a-SiN$_x$:H film stack (see Fig. 3.13 (c)). Average slopes of 0.50° and 1.02° were measured for the a-SiO$_x$:H and the a-SiO$_x$:H/a-SiN$_x$:H layers, respectively. Unfortunately, after PECVD of one of our standard a-Si:H doped layers on top of the patterned a-SiO$_x$:H and a-SiO$_x$:H/a-SiN$_x$:H film stacks, and subsequent sample immersion in HF for a long time, no signs of lift-off were observed for the a-Si:H layers. Apparently, the conformal deposition of the PECVD a-Si:H layer constitutes an effective barrier and the HF solution cannot penetrate and dissolve the sacrificial layer underneath.

With sacrificial-layer-based lift-off patterning techniques, the condition of the substrate surface after the lift-off process is critical. This is especially important if the lift-off area will be occupied, in the final device, by a certain functional layer, as for instance a hole- or electron-collecting layer. To test the use of a-SiO$_x$:H and a-SiN$_x$:H films as potential sacrificial layers, we conducted an experiment on conventional two-side-contacted FHC SHJ solar cells. Instead of depositing, on the two wafer sides, the usual a-Si:H(ip) and a-Si:H(in) film stacks, we deposited only one of the two, on one side, and only an a-Si:H(i) layer on the opposite side. On top of the a-Si:H(i) film we then deposited either an a-SiO$_x$:H or an a-SiN$_x$:H layer, always via PECVD, which we subsequently etched away in HF. At this point we deposited the missing

(a) Photograph of a patterned a-SiO$_x$:H/a-SiN$_x$:H layer stack on a polished c-Si wafer surface.

(b) SEM cross-sectional view of an a-SiO$_x$:H/a-SiN$_x$:H film, patterned via hot melt inkjet printing and wet-chemical etching.

(c) Profilometry measurements of the edges of an a-SiO$_x$:H film and an a-SiO$_x$:H/a-SiN$_x$:H layer stack, patterned via hot melt inkjet printing and wet-chemical etching.
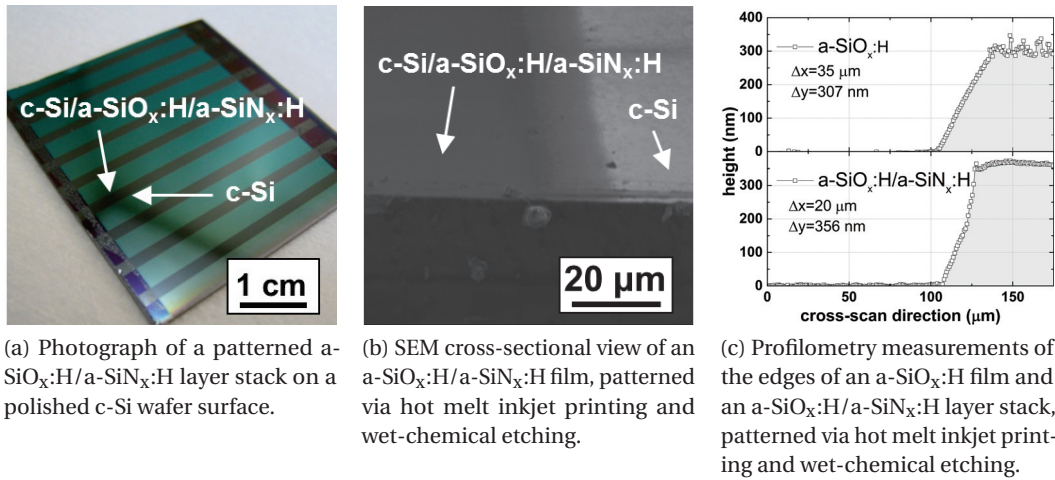
Figure 3.13: Images and measurements illustrating a-SiO$_x$:H films and a-SiO$_x$:H/a-SiN$_x$:H film stacks, patterned via hot melt inkjet printing and wet-chemical etching.

a-Si:H doped layer, always on this side, and completed the devices with a back electrode and a front TCO and metal grid. In the end, we had a group of FHC SHJ devices whose electron contact was built on the a-Si:H(i) film that saw a-SiO$_x$:H, or a-SiN$_x$:H, deposition and etching, and a group of FHC devices whose hole contact was built on such an interface. The device electrical parameters show the negative impact of the additional processes; importantly they are much more detrimental on the hole-collecting side. In both cases we observed, similarly for a-SiO$_x$:H and a-SiN$_x$:H, a *FF* drop which was of about 2 % absolute, for the case of the electron collector, and up to about 7 %, for the case of the hole collector. In addition, in the latter case we also observed a V_{oc} drop ≥ 30 mV, which we did not observe in the case of the electron collector. The experiment was conducted for 50-nm-thick as well as for 300-nm-thick a-SiO$_x$:H and a-SiN$_x$:H films. Based on this result we conclude that for an efficient patterning based on sacrificial-layer-based methods, the condition of the a-Si:H(i) layer interface, after lift-off, should be carefully investigated.

Based on these preliminary results we did not proceed further with respect to the integration of sacrificial-layer-based lift-off techniques into IBC-SHJ device fabrication. Nevertheless, the use of these dielectric films as hard masks could still be a viable and interesting option. In fabrication sequences such as that developed by Sharp, Japan [Nakamura 2014], for instance, the dielectric films could be used to replace photolithographic techniques. In the framework of the research project in which this thesis was carried out, a full wet-chemical-etching-based IBC-SHJ processing technology was not considered to be of interest. For this reason also we did not proceed further.

3.3.4 Hot melt inkjet printing for Cu electroplating

As briefly mentioned in sections 3.2 and 3.2.1, electroplating can be a valuable self-aligned patterning technique. It finds its most straightforward application in the fabrication of metal front-grid electrodes for conventional diffused-junction solar cells (see for instance [Tous 2012]). The replacement of screen-printed Ag with a low-cost material, such as Cu, and the reduced finger widths in the grid electrode are the main motivations. The case of SHJ solar cells is unfortunate in this respect; the presence of a TCO film, in place of a dielectric passivating layer, makes masking of the device surface necessary. However, the reasons that make electroplating attractive remain and the use of hot melt inkjet printing for masking may be a practical solution. We note that in the specific case of IBC-SHJ devices, where low-conductivity μm-thick back metal fingers are required to transport charge carriers towards the interconnections, Cu electroplating represents a practical fabrication tool to avoid long sputtering depositions.

We performed a series of experiments to evaluate the size of the minimum opening achievable in the hot melt resist. Decreasing the substrate temperatures slightly below room temperature we were able to target finger widths of 30 μm to 35 μm. Once we re-optimized the front-grid layout for 2×2 cm^2 solar cells for this metal finger width, we could fabricate, via hot melt inkjet printing masking of the front TCO film, conventional FHC SHJ devices with Cu grid electrodes (see Fig. 3.14 (a)) and efficiencies over 20 %. The Cu electroplating process is discussed in detail elsewhere [Geissbuhler 2014, Geissbuhler 2015a]. Importantly, this hot-melt-based patterning approach was also scaled up to industrially relevant full 6-in SHJ devices, demonstrating improved conversion efficiencies with respect to conventional screen-printed SHJ solar cells [Papet 2013].

In the case of IBC-SHJ devices, we applied hot melt inkjet printing and wet-chemical etching, similarly as described in section 3.3.3, to fabricate TCO/Cu electrodes. A copper seed layer was first evaporated, on top of the TCO film, over the full back surface of the wafer. Thus, a thick metal layer was grown on it, by Cu electroplating, and the hot melt etch resist was inkjet printed on top. The final TCO/Cu back electrodes were achieved via chemical etching. We demonstrate finished IBC-SHJ devices using a Cu back electrode, several tens of μm thick. They featured only moderate conversion efficiencies, of around 18 %, but for reasons independent of the metallization process. Further details on these devices can be found elsewhere [Geissbuhler 2015a].

3.4 The definition of our IBC-SHJ solar cell technology

A priority of our work has been, from the beginning, the establishment of a full process for n-type IBC-SHJ devices. From our perspective, some specific patterning problems are better investigated in a complete device, using its performance as a diagnostic tool. In addition, a prerequisite to address the technological and scientific challenges underlying the IBC-SHJ solar cell was the definition of a baseline IBC-SHJ processing technology. Consequently, we limited the exploration of patterning techniques and moved quickly into device fabrication.
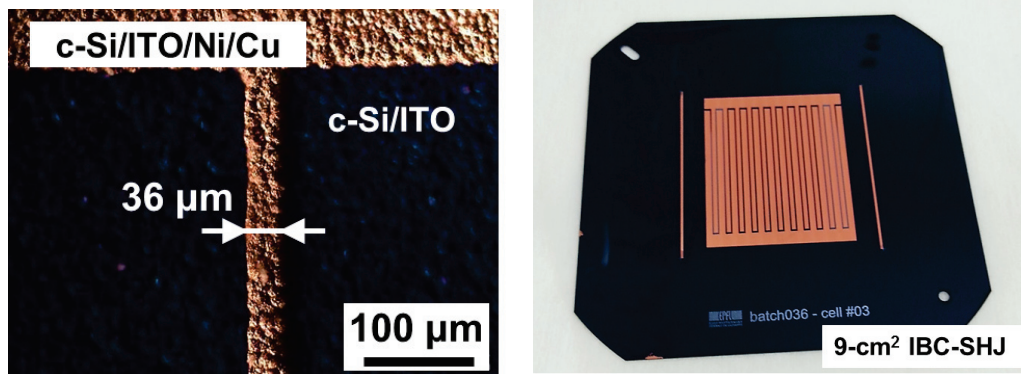
(a) Optical microscope image of a Cu-plated front-grid electrode fabricated via hot melt inkjet masking of the TCO.

(b) Photograph of an interdigitated TCO/Cu back electrode fabricated via hot melt inkjet printing and wet-chemical etching.

Figure 3.14: Examples of applications of hot melt inkjet printing and Cu electroplating in SHJ solar cells.

Based mainly on the results of this chapter, we defined a tentative IBC-SHJ solar cell technology. Our decisions were not based exclusively on technical evaluations. Aiming at the definition of a manufacturable solar cell technology, we considered inputs from the industrial partners of the research project in which the thesis has been carried out. With respect to the fabrication process, we came to the following conclusions.

(i) **The fabrication process should not rely on patterning of a-Si:H, TCO or metal films via inkjet printing and lift-off of such layers.** Despite the simplicity of this approach and the demonstrated fabrication of back electrodes for IBC-SHJ devices, the quality and reliability of the process, at least for the printing technologies and materials at our disposal, were judged to be insufficient.

(ii) **It should not rely on *in-situ* shadow masking for the fabrication of the TCO/metal electrodes.** This approach was judged to be impractical, due to the several steps needed for the realization of the full TCO/metal electrode design, and due to problems with mask re-use. It was restricted to studies where it was necessary to differentiate the TCO materials in the hole and electron contacts.

(iii) **The fabrication process should rely on *in-situ* shadow masking for patterning the doped a-Si:H films of electron and hole collectors.** This technique does not provide perfectly homogeneous films, as discussed in section 3.3.1, but has the advantage of maintaining pristine a-Si:H(*i*)/a-Si:H(*ip*) and /a-Si:H(*n*) interfaces.

(iv) **It should rely on hot melt inkjet printing of an etch resist and wet-chemical etching for the fabrication of the TCO/metal electrodes.** This process was shown to be robust, reliable and with a high patterning quality and accuracy. For quick fabrication of
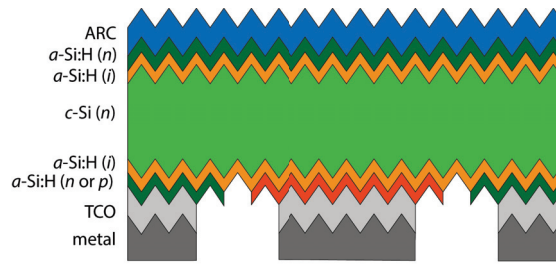
Figure 3.15: Cross-sectional schematic of the proposed IBC-SHJ solar cell architecture: **IBC-SHJ Type I**. Note **(1)** the gap between the a-Si:H(*p*) and a-Si:H(*n*) layers and **(2)** the "pyramidal scheme" for stacking doped a-Si:H layers and TCO/metal electrodes.

thick metal layers, Cu electroplating and screen-printing are viable alternatives to film deposition by sputtering.

3.4.1 Solar cell design and fabrication process

In this work, IBC-SHJ solar cells with a 9-cm^2 active cell area were fabricated on 250-μm-thick, *n*-type, 4-in float-zone (FZ) wafers, with a nominal resistivity of 3 Ω cm. Wafer texturing was performed in a potassium hydroxide solution. Following wet-chemical cleaning of the surfaces and a short dip in a diluted hydrofluoric solution, an a-Si:H(*i*) layer and a thin a-Si:H(*in*) layer stack were deposited on the back side and on the front side of the wafer, respectively. The thickness of the front a-Si:H(*i*) and thin a-Si:H(*n*) layers, measured by spectroscopic ellipsometry on a planar glass substrate, is in the range of 10 nm. The *n*- and *p*-type a-Si:H combs on the back side, needed for respectively electron and hole collection, were fabricated via *in-situ* shadow masks. All a-Si:H layers were deposited by PECVD; details can be found elsewhere [Descoeudres 2011]. For the back electrodes, a thick TCO/metal stack was deposited on the full back surface of the cell precursor, typically via PVD. During TCO deposition, we co-deposited films on a bare glass witness sample in order to measure TCO properties (thickness, resistivity, carrier density, carrier mobility). The film thickness was assessed by a stylus profilometer, its resistivity by four-point–probe measurements and the carrier density and mobility by Hall effect measurements. For an anti-reflection coating (ARC) on the front side, a 75-nm-thick a-SiN$_x$:H layer was deposited by PECVD, at sufficiently low temperature (< 200 °C) to avoid annealing-induced degradation of the a-Si:H layers [De Wolf 2009]. The TCO/metal stack was then patterned into two interdigitated combs by hot melt inkjet printing of an etch resist that was well aligned with the *p*- and *n*-type regions underneath, followed by wet etching of the exposed areas. Hot melt inkjet printing was performed by the commercial system LP50 from Meyer Burger B.V., mounting an OCE CP Cobalt printing head for hot melt materials. To heal potentially present sputter-induced damage of the a-Si:H layers [Demaurex 2012], and to activate the TCO properties, a final curing step, at a temperature below 200 °C, was performed in a belt furnace. The cross-sectional schematic of the resulting cell architecture is represented in Fig. 3.15.

1	Wafer texturing			1	Wafer texturing	
2-3	Back a-Si:H (*in*)	2x PECVD		2	Back a-Si:H (*i*)	PECVD
4-5	Front a-Si:H(*ip*)	2x PECVD		3-4	Front a-Si:H(*in*)	2x PECVD
6	Front TCO	PVD		5-6	Back a-Si:H(*n*)-(*p*) combs	2x PECVD
7-8	Back TCO/metal	2x PVD		7-8	Back TCO/metal	2x PVD
9	Front metal-grid	SCREEN-PRINTING		9	Front a-SiN$_x$:H (ARC)	PECVD
10	Curing			10	Hot melt resist	INKJET
				11	Wet etching TCO/metal	
				12	Hot melt resist stripping	
				13	Curing	
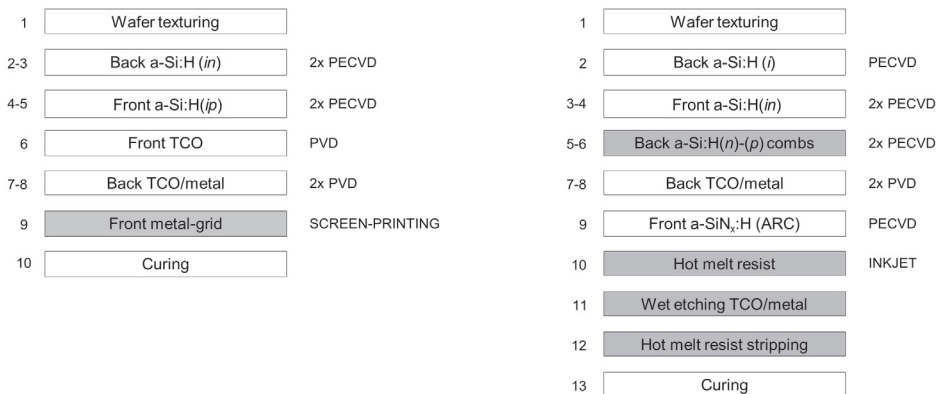
(a) Typical process flow for two-side-contacted SHJ devices (the patterning step is highlighted with a gray background). This is a FHC SHJ device.

(b) Proposed IBC-SHJ process flow (patterning steps are highlighted with a gray background). Reproduced with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

Figure 3.16: Comparison of two-side-contacted and IBC-SHJ device processing sequences.

The overall cell fabrication process relies in total on six PECVD and two PVD process steps, some of these without vacuum break, in the same reactor. Counting wafer texturing, hot melt inkjet printing, TCO/metal etching, hot melt stripping and curing, we end up with only 13 steps for our IBC-SHJ processing sequence, to be compared with a total of 10 steps required for typical two-side-contacted SHJ devices (wafer texturing, four PECVD and three PVD layers plus metal front-grid printing and curing). Fig. 3.16 shows, in details, the overall process flow of our IBC-SHJ devices, put in comparison with the process flow of a two-side-contacted FHC SHJ solar cell.

Fig. 3.17 shows the simplified fabrication process for our IBC-SHJ solar cells. In this representation, we grouped the process steps that can be done consecutively, in the same deposition system, and possibly without vacuum brake. Overall, the processing sequence is composed by six process steps.

3.4.2 Patterning techniques and alignment methodologies

The IBC-SHJ architecture requires patterning of the back n- and p-type a-Si:H layers, of the back TCO/metal stack and the relative alignment of the patterned structures. The patterning of the doped a-Si:H PECVD layers is critical due to the high-purity requirements of wafer surfaces during PECVD passivation processes and the need to strictly preserve the high quality of the a-Si:H(*i*)/a-Si:H(*p*) and a-Si:H(*i*)/a-Si:H(*n*) interfaces [Zhang 2012]. For patterning the doped a-Si:H PECVD layers we laser cut masks from double-side-polished c-Si wafers. Alignment between the mask and substrate in the PECVD deposition chamber was achieved by means of a specially designed substrate holder and metal pins. Holes to accommodate the metal pins

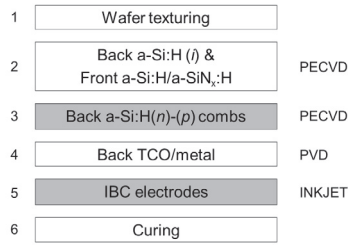| 1 | Wafer texturing | |
2	Back a-Si:H (*i*) & Front a-Si:H/a-SiN$_x$:H	PECVD
3	Back a-Si:H(*n*)-(*p*) combs	PECVD
4	Back TCO/metal	PVD
5	IBC electrodes	INKJET
6	Curing	

Figure 3.17: Simplified fabrication process for our IBC-SHJ solar cells (patterning steps are highlighted with a gray background). In this representation we grouped the process steps which can be performed consecutively in the same deposition system, and possibly without vacuum brake.

can be seen passing through the c-Si substrate in the photograph in Fig. 3.18 (b). Importantly, for process scale-up, this approach could be replaced by a mechanical edge alignment method, which would be more compatible with a full-wafer industrial device. As discussed in section 3.3.1, the deposition rate of a-Si:H through the mask slits was found to be lower, compared to full-area PECVD a-Si:H deposition. In addition, tapering of the a-Si:H layer thickness towards the edge of the deposited feature was also present. Section 4.4 discusses the impact of tapering on IBC-SHJ devices. For patterning the TCO/metal stack we used hot melt inkjet printing combined with wet-chemical etching. The alignment of the hot melt inkjet print over the patterned doped a-Si:H layers was achieved by fiducials laser marked on the wafer. These fiducials were performed simultaneously with the wafer holes used to position the *in-situ* shadow masks for the p- and n-type a-Si:H combs. In this way the relative alignment of hole- and electron-collecting layers and TCO/metal electrodes was guaranteed. With a-Si:H doped layers, this alignment method may be replaced by a wafer-edge-based system. An automatic optical recognition system of the substrate edges is normally implemented on most inkjet printers such as ours.

We estimate an overall accuracy of $\pm$ 15 µm for the positioning of the TCO/metal combs over the mask-patterned a-Si:H layers. The main error sources are linked to laser distortion in marking and mask fabrication, and mask positioning during PECVD processes. In designing the hot melt inkjet etch resist, under-etching effects were also considered for accurate patterning. To account for these positioning errors, the width of the TCO/metal comb fingers in our cell was kept narrower than the width of the doped a-Si:H comb fingers underneath. In our initial IBC-SHJ design, as schematically reproduced in Fig. 3.15, we kept nominally a 100 µm distance between the TCO/metal and doped a-Si:H layer edges, with a 100-µm-wide gap between the a-Si:H(*n*) and a-Si:H(*p*) layers. In this IBC design, the TCO/metal electrodes cover the *p*- and *n*-type a-Si:H layers by nominally ∼ 86 % and ∼ 80 %, respectively. The alignment quality can be assessed in Fig. 3.18 (a), where both a *p*-type a-Si:H layer and a TCO/metal electrode are visible (an *n*-type a-Si:H layer is weakly visible). Fig. 3.18 (b) shows a photograph of the back side of a full-processed IBC-SHJ device.
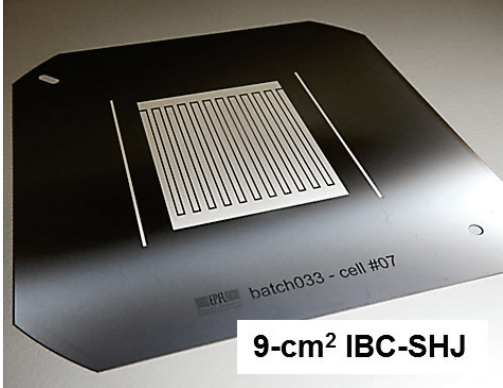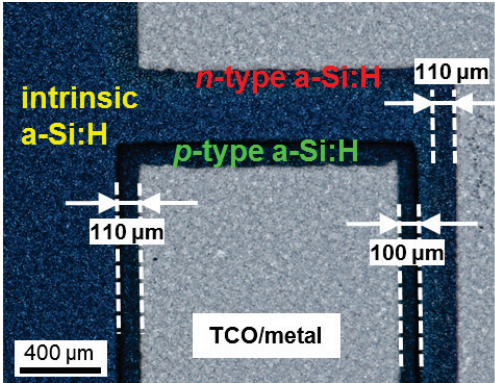
(a) Optical microscope image showing the alignment quality of the doped a-Si:H layers and the TCO/metal electrodes for use in our IBC-SHJ solar cells. In the area between the doped a-Si:H layers, the textured c-Si surface is covered only by an intrinsic a-Si:H layer. Reproduced with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

(b) Photograph of the back side of a full-processed IBC-SHJ device. The two metal lines, outside the solar cell area, serve only as a post-processing alignment check; they end on the laser-marked fiducials used for hot melt inkjet printing.

Figure 3.18: Images of the back side of our full-processed IBC-SHJ solar cells.

4 Interdigitated back-contacted silicon heterojunction solar cells with conversion efficiency >22%

Abstract

This chapter presents the step-by-step development of our original photolithography-free *n*-type interdigitated back-contacted silicon heterojunction (IBC-SHJ) technology. It discusses, in detail, three major topics of IBC-SHJ devices: **(i) hole and electron contact fabrication**, **(ii) losses due to charge-carrier transport** and **(iii) device optics**. An improved back-contacted architecture, the reduction of the losses due to charge-carrier transport at the heterocontacts and the redesign of the front stack for improved transparency, led to improved fill factors (*FF*) and short-circuit current densities (J_{sc}) in our IBC-SHJ solar cells. With *FF* above 75% and J_{sc} approaching $41\,\mathrm{mA\,cm^{-2}}$, we demonstrated device conversion efficiencies >22%.

This chapter is partially based on a paper published in IEEE Journal of Photovoltaics and reproduced with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.[1]. Section 4.6 is partially based on a paper published in IEEE Journal of Photovoltaics and reproduced with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE. Sections taken from this paper are marked by the symbol †.

4.1 Introduction

Our IBC-SHJ technology developed progressively over the years. The preparatory experiments described in chapter 3 formed the basis of the tentative IBC-SHJ process flow used for the fabrication of our first devices. Subsequent improvements were the joint results of experimental work and a deeper understanding of the device limiting factors. These improvements consist of modifications to the materials, the device architecture and the fabrication methodology. They concern, respectively, optimization of:

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[1]The results presented here were obtained with the help of B. Paviet-Salomon, D. Lachenal, S.M. de Nicolas, A. Descoeudres, J. Geissbuhler, S. De Wolf and C. Ballif. Contributions are gratefully acknowledged.

  (i) the back-contacted architecture (section 4.4),

 (ii) the charge-carrier transport properties of the heterocontacts (section 4.5) and

(iii) the device optics (section 4.6).

By combining the benefits of such technology advances, we were able to fabricate original 3×3 cm^2 n-type IBC-SHJ devices with conversion efficiencies well above 22 %. Importantly, the developed IBC-SHJ technology relies on a photolithography-free process which is in principle cost-compatible with mass production and scalable to industrially relevant full 6-in devices.

4.2 Motivation

Silicon heterojunction technology is of high interest for application in solar cells. Thanks to the excellent c-Si surface passivation properties of hydrogenated amorphous silicon (a-Si:H), it is one of the most likely candidates to achieve high conversion efficiencies at competitive costs [De Wolf 2012b, Louwen 2016]. The promise of this technology was recently further substantiated by Kaneka, Japan, who reported conversion efficiencies as high as 25.1%, within the highest to date ever reached for c-Si-based solar cells of practical size [Adachi 2015]. However, standard two-side-contacted front-hole-colecting (FHC) and rear-hole-collecting (RHC) SHJ solar cells are limited by front metal-grid shadowing and parasitic absorption of light, either in the a-Si:H or the transparent conductive oxide (TCO) films. These J_{sc} losses are linked to the modest short-wavelength response of SHJ devices [Holman 2012]. Contrastingly, in the long-wavelength part of the spectrum, well-engineered SHJ devices can outperform the best reported homojunction solar cells [Holman 2013a].

A straightforward step towards higher J_{sc} values and higher conversion efficiencies in SHJ devices consists of the back-contacted architecture, featuring both electron- and hole-collecting contacts at the back of the solar cell. This cell concept—industrially proven by SunPower, USA, for homojunction devices with conversion efficiencies of up to 25.2% [Green 2016b]—has the advantage of eliminating front-electrode shadowing. Moreover, in the case of SHJ devices, it brings additional benefits by minimizing or even eliminating parasitic absorption. In back-contacted SHJ solar cells a front TCO layer is no longer required and the front a-Si:H layers can be tuned, irrespective of their carrier transport properties, solely in regard to their transparency and passivation properties. Actually, substitution of the complete a-Si:H/TCO stack with wider band-gap passivating dielectrics, such as a-SiN$_x$:H, a-SiO$_x$:H or Al$_2$O$_3$, for improved transparency becomes possible. The potential of back-contacted architectures using SHJ contacts was recently convincingly, and conclusively, pointed out by Panasonic, Japan, reporting the world's highest energy conversion efficiency of 25.6 % for c-Si-based solar cells under 1-sun illumination [Masuko 2014]. This record device exhibits an area of 143.7 cm^2 and demonstrates, in addition to the potential of the technology, its scalability to devices of practical size. Based on this new exciting result, back-contacted SHJ solar cells are arguably the ultimate device architecture for single-junction silicon-wafer-based solar cells.

Despite this great result, the implementation of back-contacted architectures adds complexity to the overall fabrication process. It requires adequate patterning technologies and accurate alignment techniques. In our work we aimed at high-efficiency IBC-SHJ device fabrication via simple processing technologies and a minimal number of processing steps, comparable to those required for the fabrication of FHC or RHC SHJ devices.

4.3 State-of-the-art of IBC-SHJ devices

Besides the extraordinary result of Panasonic, Japan [Masuko 2014], several other notable back-contacted SHJ record devices have been demonstrated in the last few years. Table 4.1 summarizes the current state-of-the-art of back-contacted SHJ solar cells with a conversion efficiency higher than 20.0 %. Along the same lines as Panasonic, Sharp, Japan, with its so-called rear heterojunction emitter plus antireflective passivation layers (RHEA) concept demonstrated recently a conversion efficiency of 25.1 %, on a cell area < 4 cm^2 [Nakamura 2014]. Just below these two outstanding devices, we find the best *tunnel*-IBC-SHJ solar cell fabricated in this thesis work, with a conversion efficiency of 22.9 %, which will be presented in chapter 6. A conversion efficiency of 20.5 % was also reached by LG, Korea [Lee 2014], on a cell area of 221 cm^2. Using an industrially feasible laser-based approach, CEA-INES, France, recently reported a conversion efficiency of 20.3 % [Aguila 2015]. Conversely, both Helmholtz-Zentrum Berlin, Germany [Mingirulli 2011], and the University of Delaware, USA [Zhang 2015], reported a conversion efficiency of 20.2 % using photolithographic techniques. Some other groups have also presented back-contacted SHJ solar cells but with conversion efficiencies in the range 15–20% [Chowdhury 2012, Tucci 2008] (not included in Table 4.1). Interestingly, all mentioned back-contacted SHJ devices exploit an interdigitated design for the back contact. Back-contacted SHJ devices using alternative contacting schemes have also been proposed [Chen 2013, De Vecchi 2012b, Stangl 2009], but so far with a maximum conversion efficiency of only 17.1 % [Haschke 2012]. The use of *in-situ* shadow masks to structure a-Si:H layers in back-contacted SHJ devices, as proposed in the present work, is an approach previously demonstrated; however, at the time of starting this thesis, only relatively modest device performances were achieved [Tucci 2007, Desrues 2008, Scherff 2011, Ohdaira 2006].

Surprisingly, several of the back-contacted devices listed in Table 4.1 feature J_{sc} values of about 40.0 mA cm^{-2}, as Kaneka's top-J_{sc} two-side-contacted SHJ solar cell [Hernandez 2013]. From this observation we infer that proper optimization of sunlight absorption and carrier collection in back-contacted SHJ solar cells may not be so straightforward. The device optics (point iii in the list of section 4.1) will be extensively discussed in section 4.6 of this chapter.

Generally speaking, in IBC-SHJ devices aiming at top efficiencies, the achievement of good *FF*s seems to be the major difficulty. Excluding the two devices of Panasonic and Sharp, all listed back-contacted devices in Table 4.1 show *FF* ≤ 77 %, which is a value routinely surpassed in conventional two-side-contacted SHJ devices. In our IBC-SHJ technology we also encountered this problem, on which we focused most of our research efforts. The most

important *FF* increments resulted from the optimization of the back-contacted architecture and of the heterocontact transport properties (points (i) and (ii) in the list of section 4.1). In sections 4.4 and 4.5, and in chapter 5, we present most of our findings in this regard.

Table 4.1: State-of-the-art of back-contacted SHJ solar cells with η >20 %, sorted by decreasing η. Adapted with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE.

Affiliation	Year	Area (cm^2)	J_{sc} (mA cm^{-2})	V_{oc} (mV)	*FF* (%)	η (%)
Panasonic, Japan [Masuko 2014]	2014	143.7 (da)	41.8	740	82.7	25.6
Sharp, Japan [Nakamura 2014]	2014	3.72 (ap)	41.7	736	81.9	25.1
EPFL-CSEM (chapter 6 of this thesis)	2016	9.0 (da)	40.8	728	77.1	22.9
LG, Korea [Lee 2014]	2014	221 (ta)	37.5	716	76.4	20.5
CEA-INES, France [Aguila 2015]	2015	22.1 (da)	40.1	705	71.9	20.3
HZB-ISFH, Germany [Mingirulli 2011]	2011	1 (da)	39.7	673	75.7	20.2
University of Delaware, USA [Zhang 2015]	2015	1 (da)	38.1	697	76.0	20.2

ap: aperture area; da: designated area; ta: total area (see [Green 2013])

4.4 Optimization of hole and electron contact architectures (I)

4.4.1 Introduction

In our *n*-type IBC-SHJ technology, the doped a-Si:H films forming the hole and electron collectors, patterned via *in-situ* shadow masking, present an imperfect morphology. As shown in section 3.3.1, we found that patterned a-Si:H films are not homogeneously thick but show a reduced thickness (*tapering*) towards the edges of the deposition area, compared to the center. In addition some under-deposition tails (*tailing*), around the edges, are also present. This has relevant implications with respect to the design of an optimized back contact. In the experiments presented below, we dealt with this imperfect morphology and modified the initial IBC-SHJ device architecture, proposed in section 3.4, to circumvent the associated device performance limitations. The main "variables" of this optimization are the thickness of the doped a-Si:H layers and the geometry of the doped a-Si:H combs and of the TCO/metal electrodes.

4.4.2   Experimental details

The IBC-SHJ solar cells presented in this section integrate the best ZnO:Al material (see section 4.5.3) and the doped a-Si:H films either of IBC-SHJ[1], in sections 4.4.3 and 4.4.4, or of IBC-SHJ[2], in sections 4.4.5 and 4.4.6. For the presentation of IBC-SHJ[1] and IBC-SHJ[2], please refer to section 4.5.4. The reference device is that delineated in Fig. 3.15. Its fabrication process and the used front-side stack are described in section 3.4. In IBC-SHJ devices with this baseline architecture, we show and discuss the effect of doped a-Si:H film thickness, the distance between the edge of the TCO/metal electrode and the p-type a-Si:H (a-Si:H(p)) layer ("d" in the schematic of Fig. 4.4 (a)) and eliminating the gap between the doped a-Si:H layers. The thickness of the standard a-Si:H layers used in SHJ heterocontacts, measured by spectroscopic ellipsometry on a planar glass substrate, are typically in the range of 10 nm.

4.4.3   The impact of the a-Si:H(p) film thickness

In FHC SHJ devices, the planar a-Si:H(p) layer used in the front stack is the origin of important parasitic absorption losses of light [Holman 2012]. Practically, these losses are reduced as much as possible, by thinning the a-Si:H(p) layer until the device V_{oc} and FF start to degrade [Fujiwara 2007]. Such an optimized a-Si:H(p) layer cannot be directly employed in IBC-SHJ devices as it results in low V_{oc} and FF values.

In this section we first consider the case of FHC SHJ devices and discuss the origin of V_{oc} and FF losses for mask-less depositions of thin a-Si:H(p) films. Thus we address the problem of a-Si:H(p) thickness optimization in our IBC-SHJ solar cells and give our interpretation of the observed results.

Unpatterned a-Si:H(p) films for FHC SHJ devices

The physical origin of V_{oc} and FF losses for thin a-Si:H(p) films is twofold. The insertion of a sufficiently thick doped a-Si:H layer between the TCO and the a-Si:H(i) passivating film, is required to protect the latter from irreversible sputter damage **(1)**. At the same time, the a-Si:H(p) layer must be thick enough to generate the required built-in potential [Fujiwara 2007] and, simultaneously, to preserve such built-in potential from the detrimental effect of the lower bare TCO work function (WF) [Centurioni 2003, Kanevce 2009] **(2)**.

Considering the effect **(1)**, in Fig. 4.1, we report on the evolution of effective lifetime curves ($\tau_{eff}(\Delta n)$) for symmetric lifetime samples featuring a hole collector with a *standard* a-Si:H(p) layer thickness, and with a thin a-Si:H(p) layer (1/3 of the *standard* a-Si:H(p) thickness), respectively. After a-Si:H(p) deposition and TCO sputtering, the two samples show only slightly different carrier lifetimes. However, this difference augments significantly after post-deposition annealing in air at 200 °C. The sputter damage [Demaurex 2012], reversible for the standard a-Si:H(p) film, turns out to be irreversible for the thin film. After TCO etch-off, the initial passivation level is totally recovered for the standard a-Si:H(p) film only. For the thin a-Si:H(p)
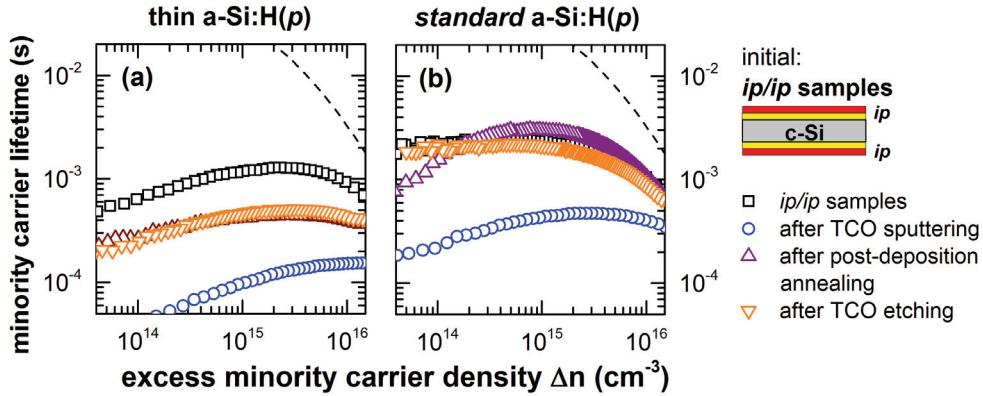
Figure 4.1: $\tau_{eff}(\Delta n)$ measurements on an n-type c-Si absorber featuring a bifacial hole collector (*ip/ip* samples) formed by a thin (a) and a standard (b) a-Si:H(*p*) layer. $\tau_{eff}(\Delta n)$ is monitored at different process steps: initially with only the a-Si:H layers, after TCO sputtering, after post-deposition annealing at 200 °C for 20 minutes and after TCO removal by chemical etching. The combined Auger and radiative limit is indicated by the dashed line [Richter 2012].

film, from the measured $\tau_{eff}(\Delta n)$ we can calculate losses of up to 40 mV in implied-V_{oc} and to 5 % absolute in implied-*FF*. We note that, for the standard a-Si:H(*p*) film, we observe a lower τ_{eff} at low Δn in the presence of the TCO overlayer. This effect is discussed in section 5.2.

The limiting situation is when no a-Si:H(*p*) layer is present. In this case, the device resembles a metal-insulator-semiconductor solar cell [Pulfrey 1978], whose I-V characteristic depends on the bare TCO WF but, more importantly, on the resulting a-Si:H(*i*)/TCO interfacial WF. The bare TCO WF, being normally higher than the c-Si(*n*) substrate, makes the TCO (despite being *n*-type) act as a hole collector. However, its moderately high value combined with Fermi-level pinning effects [Schroder 2006, Robertson 2013]—highly conceivable for an a-Si:H(*i*)/sputtered-TCO interface [Ritzau 2014, Wronski 1977])—will result in an a-Si:H(*i*)/TCO interfacial WF insufficiently high to guarantee good V_{oc} and *FF* values. As an example we refer to the case of the ITO films of section 5.2.4 that, without an a-Si:H(*p*) film, result in V_{oc}s in the range of 350 mV to 550 mV [Tomasi 2016b].

Patterned a-Si:H(*p*) films for IBC-SHJ devices

In Fig. 4.2, we report on the results of a simple experiment in which we modify the deposition time, i.e. film thickness, for the a-Si:H(*p*) layer used in the hole contact of our IBC-SHJ devices. We chose a minimum deposition time, t_{std}, equal to the one used for the optimized a-Si:H(*p*) layer of the front stack of our high-efficiency FHC SHJ devices.

Insufficiently thick a-Si:H(*p*) layers provoke V_{oc} and *FF* losses, including in IBC-SHJ devices, but the optimum a-Si:H(*p*) layer deposition time is very far from that of conventional FHC SHJ devices. We think that this is peculiar to the *in-situ* shadow masks technology. As observed
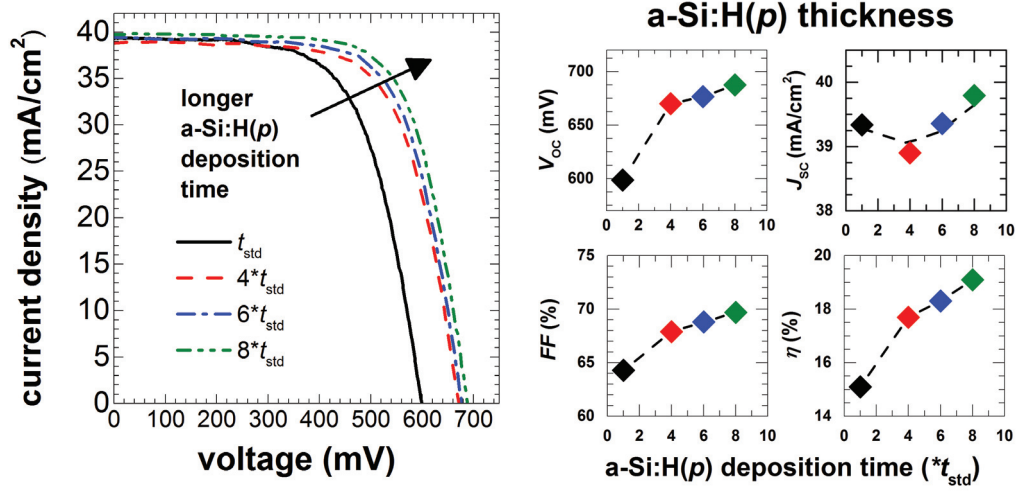
(a) 1-sun I-V characteristics of IBC-SHJ devices using, in the hole contact, a-Si:H(p) films of different thickness.

(b) IBC-SHJ solar cell electrical parameters extracted from the 1-sun I-V characteristics of (a).

Figure 4.2: 1-sun I-V characteristics, and electrical parameters, of IBC-SHJ devices using a-Si:H(p) films of different thicknesses in the hole contact. The deposition times for the a-Si:H(p) layers were chosen as multiples of the minimum deposition time t_{std}, corresponding to the deposition time used for the optimized front-side a-Si:H(p) layer of our high-efficiency FHC SHJ devices.

in the experiment of section 3.3.1, this technology reduces the a-Si:H film growth rate, when depositing through slits smaller than ∼ 2 mm, and to thickness *tapering* close to the film edges. For the specific case of a 1.4-mm-wide mask slit (as used for our hole-collecting fingers), we detected a reduction in the maximum a-Si:H(p) layer thickness of about 25 %, with respect to a mask-less deposition. This value indicates the reduction in the a-Si:H(p) deposition rate only near the center of the mask slit; however, the film thickness is lower everywhere else. This phenomenon is likely to play a role in our devices and may explain the need for much longer a-Si:H(p) depositions times for IBC-SHJ devices compared to FHC SHJ devices.

When the portion of the thinner a-Si:H(p) film act as part of the hole collector, contacted by the TCO/metal electrode, it determines, due to the effect **(2)**, a locally "bad" diode I-V characteristic featuring low V_{oc}, and *FF*. Such a "bad" diode would be connected in parallel, through the TCO and metal films of the back electrode, to the "good" diode with the sufficiently thick a-Si:H(p) layer. The effect on the overall I-V characteristic can be simulated by considering the equivalent circuit reported in the inset of Fig. 4.3 (a). The voltage across the two diodes must be the same, whereas the photo-generated currents add. By means of a MATLAB script we studied the impact of varying the ratio between the area of the "bad" diode (A_{bad}), i.e. the portion of thin a-Si:H(p) layer, and that of the "good" diode (A_{good}), i.e. the portion of sufficiently thick a-Si:H(p) layer, for a fixed total area $A_{tot} = A_{bad} + A_{good}$. For simplicity, we assumed a single-diode I-V characteristic for both diodes, and higher J_0 and n
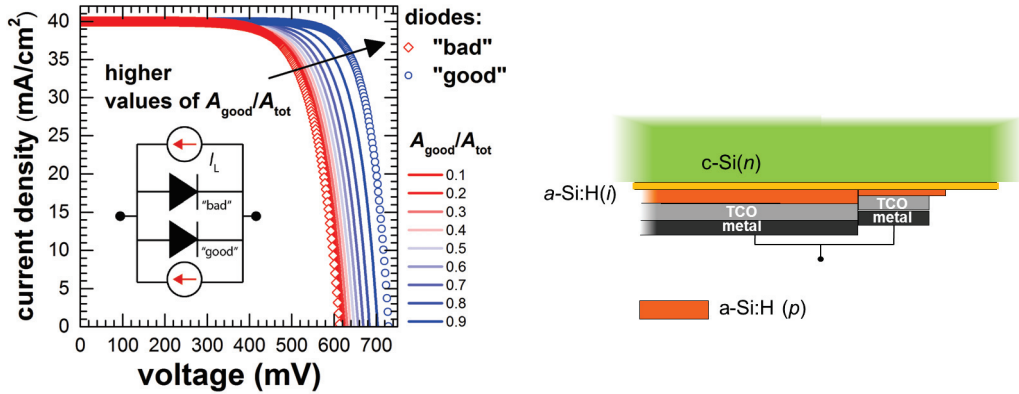
(a) Simulated 1-sun I-V characteristics of an IBC-SHJ device in parallel with a "bad" diode, for different area fractions ($A_{\text{good}} / A_{\text{tot}}$).

(b) Cross-sectional schematic of the back hole contact. The effect of the a-Si:H(p) thickness *tapering* can be schematically reproduced with the equivalent circuit represented in the inset of Fig. (a), where the parallel-connected diodes correspond to area of different a-Si:H(p) thicknesses.

Figure 4.3: Simulated 1-sun I-V characteristics of IBC-SHJ devices connected in parallel with a "bad" diode of different areas. The trends in the device electrical parameters mirror the results of the experiment of Fig. 4.2.

values for the "bad" diode. Fig. 4.3 shows the I-V characteristics and the respective electrical parameters. They reproduce trends which could explain those observed in the experiment of Fig. 4.2. Importantly, similar trends can be achieved (a) with a fixed A_{good}, while increasing A_{bad} and A_{tot}, or (b) with fixed A_{bad} and A_{good} but degrading J_0 and n of the "bad"-diode. Situation (a) corresponds to the case of varying the TCO/a-Si:H(p) contact fraction, including a wider or narrower portion of the thinner a-Si:H(p) film, and supports our interpretation of the experimental results presented in section 4.4.4.

To conclude this discussion about the effects of thin a-Si:H(p) films, we note that in our process the TCO/metal layer stack is sputtered on the whole back surface. A locally thin a-Si:H(p) film, along the edges of the p-type comb, enlarges the portion of the unprotected a-Si:H(i) layer and may contribute to increased V_{oc} and *FF* losses also via the irreversible passivation degradation effect **(1)**.

4.4.4 The impact of the TCO/a-Si:H(p) contact fraction

In IBC-SHJ devices, at the back side, some of the layers may be stacked according to a "pyramidal scheme". Bottom (wider) and upper (narrower) patterned fingers are piled up with a certain distance between their edge positions. This structure helps to prevent detrimental effects of an imperfect alignment and gives robustness to the device technology.

Using the hot-melt-based patterning process of section 3.3.3, TCO and metal films can be

structured simultaneously, maintaining the same pattern geometry. Conversely, to accurately position the TCO/metal electrodes on top of the doped a-Si:H layers, which are patterned and aligned to the substrate differently, we need to use such a "pyramidal scheme". This leads to an incomplete coverage of the charge-carrier collectors, i.e. TCO/a-Si:H(p) and TCO/a-Si:H(n) contact fractions < 100 %. For the hole contacts, TCO/a-Si:H(p) contact fractions < 100 % have been shown to be a source of J_{sc} and FF losses in earlier experiments and simulations [Desrues 2010, Desrues 2011, Desrues 2014, Haschke 2013]. TCO/a-Si:H(p) contact fractions of 64 and 93 %, were found to yield IBC-SHJ FF values of 53 % and 73 %, respectively. Contextually, J_{sc} values increased from about 28 mA cm^{-2} to above 33 mA cm^{-2} and V_{oc} values were in the range of 600 mV to 650 mV [Desrues 2014]. The phenomenon was explained by distributed series-resistance effects, which are associated to the portions of the uncovered a-Si:H(p) layer. Charge carriers may, or may not, be collected through these high-resistance paths that become areas of enhanced carrier recombination. For increasing forward bias, a smaller amount of these carriers experience a sufficient lateral electric field, in the not-contacted hole-collecting region, to reach the TCO/metal electrode. This generates a stronger "shunted-like" behavior of the I-V characteristic in IBC-SHJ devices with larger not-contacted hole-collecting regions, which in turn determines lower FFs and J_{sc} values.

To study the impact of the TCO/a-Si:H(p) contact fraction in our IBC-SHJ solar cells, we fabricated a series of identical devices but with different portions of the uncovered a-Si:H(p) layer. We varied the distance (d) between the edge of the TCO/metal electrode and the edge of the a-Si:H(p) fingers, as illustrated in Fig. 4.4 (a). The device results of this experiment are presented in Fig. 4.4 (b) and (c). We observed decreasing V_{oc} and FF, but increasing J_{sc}, for higher hole collector contact fractions, with the former dominating and determining the overall trend of device conversion efficiencies. The d values of 300 μm, 200 μm and 100 μm correspond to TCO/a-Si:H(p) contact fractions of about 57 %, 71 % and 86 %, respectively. Comparing our experimental results with those of Desrues *et al.*, we can find a correspondence only for the J_{sc} trend. However, for a similar range of TCO/a-Si:H(p) contact fractions, in our case the overall difference in J_{sc} is much lower, about 1 mA cm^{-2}.

V_{oc}, FF and TCO/a-Si:H(p) contact fraction

As discussed in section 4.4.3, for SHJ solar cells, an insufficiently thick a-Si:H(p) layer detrimentally affects mainly V_{oc} and FF, and not J_{sc}, in conventional two-side-contacted and back-contacted devices. From this perspective, the lower V_{oc} and FF values observed for higher TCO/a-Si:H(p) contact fractions in IBC-SHJ devices can be explained by an increasingly wide portion of the hole contact characterized by an insufficiently thick a-Si:H(p) layer. By means of the same MATLAB script used for the simulations of the section 4.4.3, we could obtain increasing V_{oc} and FF losses for a fixed A_{good} but higher A_{bad} and A_{tot} values. The experimental results of this and the previous section are very much in line. Overall, lower V_{oc} and FF are achieved for shorter a-Si:H(p) layer deposition times and a fixed TCO/a-Si:H(p) contact fraction, or for wider TCO/metal electrodes at the hole contact and a fixed a-Si:H(p)
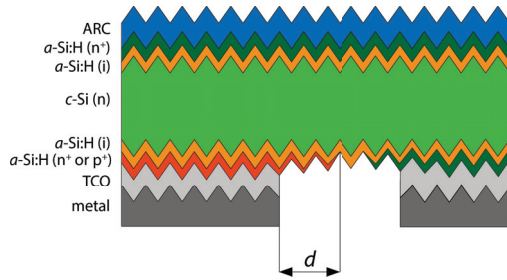
(a) Schematic of the IBC-SHJ solar cell architecture of this experiment. The parameter d indicates the portion of the uncovered a-Si:H(p) layer.
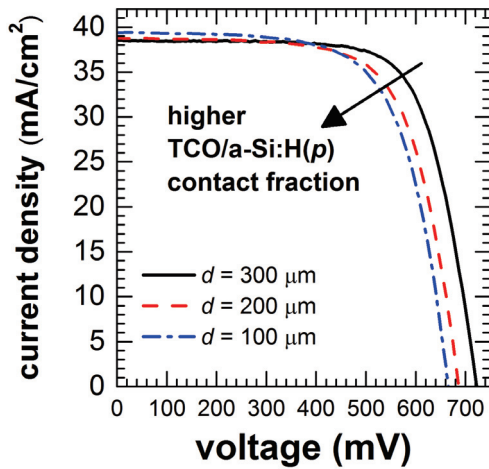
(b) 1-sun I-V characteristics of IBC-SHJ devices with a variable TCO/a-Si:H(p) contact fraction. For clarity, the I-V curve of one device is not shown.
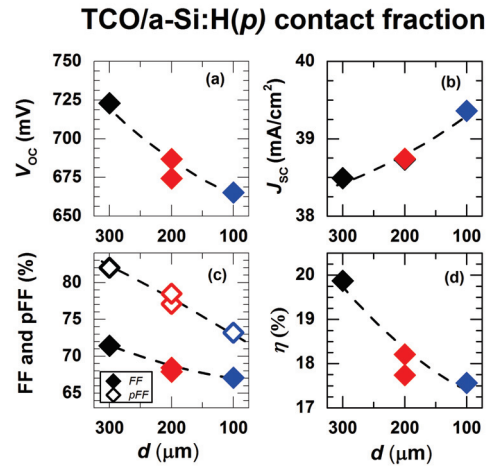
(c) IBC-SHJ solar cell electrical parameters extracted from the 1-sun I-V characteristics of (a).

Figure 4.4: 1-sun I-V characteristics, and electrical parameters, of IBC-SHJ devices in which the TCO/metal electrode contacts different fractions of the hole collector. d values of 300 μm, 200 μm and 100 μm correspond to a-Si:H(p) contact fractions of 57 %, 71 % and 86 %, respectively.

deposition time. In both situations, a larger portion of the hole contact is characterized by an insufficiently thick a-Si:H(p) layer, which explains the V_{oc} and FF loss.

J_{sc} and TCO/a-Si:H(p) contact fraction

The experiment reveals increasing J_{sc} with increasing contact fractions. To understand the physical effects causing the J_{sc} variation, we performed EQE/IQE measurements and applied the J_{sc}-loss analysis method of section 2.3.2. The different sources of J_{sc} losses, and reference values for relevant IBC-SHJ devices, are discussed in section 4.6.

In Fig. 4.5, we report EQE, reflectance (R_{cell}), transmission (T_{cell}) and total absorbance (A_{cell}) curves measured on the three IBC-SHJ devices of Fig. 4.4 (b) and (c). From the J_{sc}-loss analysis
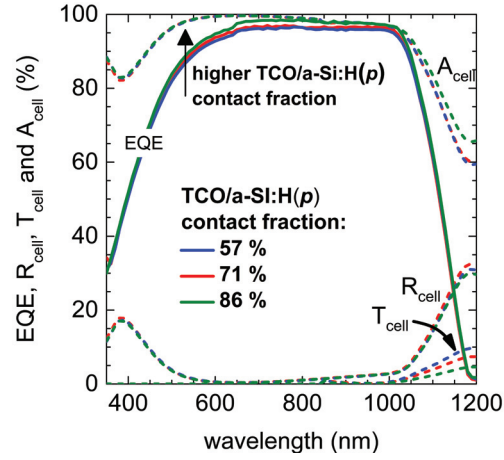
Figure 4.5: Influence of the TCO/a-Si:H(p) contact fraction on EQE, reflection, transmission and absorbance curves. 1-sun I-V characteristics and respective electrical parameters of these IBC-SHJ devices are presented in Fig. 4.4.

it emerges that the main contribution, to the J_{sc} variation, comes primary from J_{medium} and then from J_{short}. In the IBC-SHJ device with the highest TCO/a-Si:H(p) contact fraction, J_{medium} and J_{short} are reduced by about 0.5 mA cm^{-2} and 0.3 mA cm^{-2}, respectively, compared to the IBC-SHJ device with the lowest contact fraction. The reduction of J_{medium} and J_{short} may be explained either by a decreased distributed series-resistance effect, as a result of the higher a-Si:H(p) contact fraction [Desrues 2010, Desrues 2011, Desrues 2014, Haschke 2013], or by decreased electrical-shading losses. The higher a-Si:H(p) contact fraction is achieved by moving the edges of the TCO/metal electrode of the hole contact closer to the electron contact, thus shortening the diffusion path for minority carrier (hole) collection. For a more detailed discussion of electrical-shading losses in our IBC-SHJ devices, please refer to section 4.6.5. Discerning unambiguously between these two possible loss mechanisms will require further investigations. However, in the data shown in Fig. 4.23 (b), we measured, at each step, a relative loss of about 8 % in the normalized LBIC signal moving to a position 100 μm, 200 μm and 300 μm far from the edge of the front TCO pad. Since a portion of 100 μm at each side of the hole-collecting fingers corresponds to roughly 15 % of the whole hole contact area, we can expect a relative loss in J_{sc} of about 1.2 %, i.e. 0.5 mA cm^{-2}, each time we move the edge of the TCO electrode 100 μm backward in respect to its original position. Hence, this effect alone seems to explicate the J_{sc} trend observed in the experiment of Fig. 4.4 (c).

4.4.5 The electron contact architecture

In FHC SHJ devices, the planar a-Si:H(n) layer forming the electron collector is typically thicker than its p-type counterpart at the front. This difference originates from optical reasons as the n-type layer, placed at the back side, does not contribute critically to the parasitic absorption of short-wavelength photons. However, as was true for the a-Si:H(p) layer, its optimum deposition time in IBC-SHJ devices, compared to FHC SHJ devices, increases as
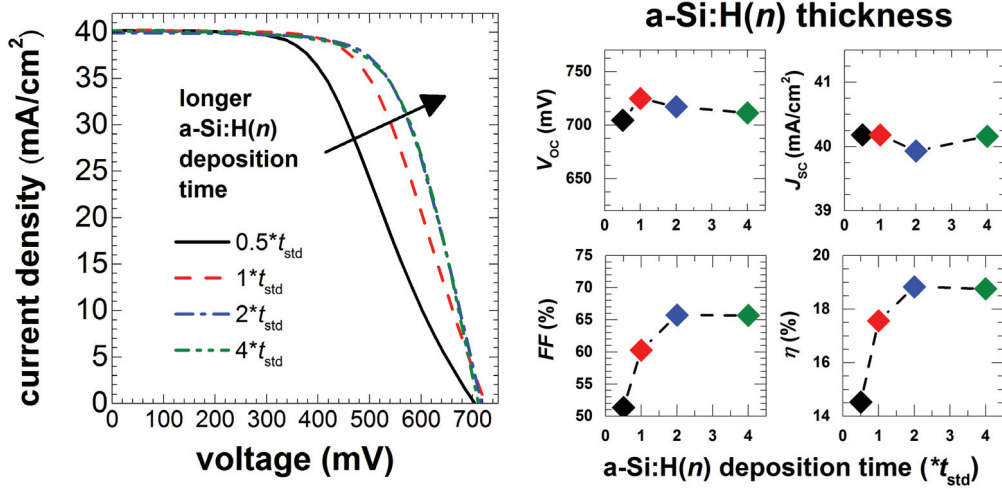
(a) 1-sun I-V characteristics of IBC-SHJ devices using in the hole contact a-Si:H(n) films of different thicknesses.

(b) IBC-SHJ solar cell electrical parameters extracted from the 1-sun I-V characteristics of (a).

Figure 4.6: 1-sun I-V characteristics, and related electrical parameters, of IBC-SHJ devices using a-Si:H(n) films of different thicknesses in the electron contact. The deposition times for the a-Si:H(n) layers were chosen as multiples of the *standard* deposition time t_{std}, corresponding to the deposition time used for the optimized back a-Si:H(n) layer of our high-efficiency FHC SHJ devices.

well.

In the results of the experiment shown in Fig. 4.6, we observe *FF* and efficiency losses for thinner a-Si:H(n) layers. Importantly, in contrast with the a-Si:H(p) film, there are almost no V_{oc} losses for thin a-Si:H(n) films. This is explained by the fact that the electron contact does not contribute to determine the built-in voltage of the solar cell. However, its thickness may still affect the device V_{oc} via the passivation degradation effect **(1)**, discussed in section 4.4.3. Based on the results of this experiment, for a-Si:H(n) films thicker than half of the standard thickness, this seems to be only a minor effect. We note also that, in the electron contact, the portion of the a-Si:H(n) layer that is not covered by the TCO/metal electrode does not dictate any J_{sc} loss. This is documented and discussed, based on experimental results, in section 4.6.5. Overall, the fabrication of well-performing a-Si:H-based electron-collecting contacts results less critical.

4.4.6 The impact of the gap between the doped a-Si:H layers

The $\tau_{eff}(\Delta n)$ data reported in Fig. 4.1, indicates that sputtering a TCO film on top of a thin doped a-Si:H layer or, worse, directly on top of an a-Si:H(i) layer may have strongly detrimental effects on passivation. In this respect, the initial IBC-SHJ architecture of section 3.4 exhibits a critical shortcoming: the 100-μm-wide gap in between the doped a-Si:H layers, where

the TCO electrode is locally sputtered directly on the a-Si:H(i) passivating film. This area corresponds to about ~8 % of the overall device area, which is not negligible. As a result, our IBC-SHJ devices may suffer of irreversible sputter damage. This 100-μm-wide gap is inherited from conventional diffused-junction IBC devices, to avoid shunts between electron and hole contacts, but it may not be strictly required in IBC-SHJ devices. The resistivity of the thin doped a-Si:H layers indeed is very high (>$1 \cdot 10^3$ Ω cm for a-Si:H(n); >$1 \cdot 10^5$ Ω cm for a-Si:H(p)), and their physical contact should not hinder the achievement of sufficiently high R_{shunt} values. Importantly, in the specific case of our IBC-SHJ technology, the elimination of the gap may bring additional benefits, besides the suppression of sputter damage. Its removal can be used to help the problems presented in sections 4.4.3 and 4.4.4. Without modifying the design of the electron collector, we enlarged by 100 μm, at each side, the hole-collecting fingers to close the gap. In this way, a-Si:H(p) *tapering*-induced effects on the device parameters are weakened by the increased distance from the metal/TCO to the a-Si:H(p) edges. We note that this increased distance is not achieved by moving the edges of the hole contact TCO/metal electrode backwards. This has the advantage of avoiding the J_{sc} detrimental effects of Fig. 4.4 and maintaining unchanged the overall hole contact surface (see section 4.5).

In Fig. 4.7, we compare two IBC-SHJ devices with the electrode design of Fig. 3.15 and Fig. 4.8. These devices integrate in their contacts the best thick doped a-Si:H layers of IBC-SHJ[2] and our best performing ZnO:Al material (see section 4.5). Thanks to this improved IBC-SHJ design we reached higher V_{oc} and higher *FF*, together with a J_{sc} value of about 40.0 mA cm^{-2}, which increased the conversion efficiency to > 21 %.

4.4.7   Conclusion (I)

Based on the experiments discussed in this section, we defined a new IBC-SHJ architecture which minimizes the identified device limitations. This improved IBC-SHJ solar cell is schematically represented in Fig. 4.8. In the new design, the thickness of the doped a-Si:H layers is increased. Additionally, by widening the fingers of the a-Si:H(p) comb with respect to its respective TCO/metal electrode, we mitigated the detrimental effects of a-Si:H(p) thickness *tapering*, caused by *in-situ* shadow masking. Importantly, this was achieved without displacing the edge of the TCO/metal electrode with respect to the electron-collecting fingers, which avoids unwanted J_{sc} losses and maintains unchanged the hole contact area. Additionally, by widening the hole-collecting fingers and closing the gap between the doped a-Si:H layers, we avoided sputter damage of the a-Si:H(i) layer and reached a conversion efficiency above 21 %.

4.5   Losses due to charge-carrier transport in IBC-SHJ solar cells (II)

4.5.1   Introduction

As briefly noted in section 4.3, one of the major problems in obtaining high-efficiency devices is the achievement of good *FF* values. In this respect, *FF* losses due to charge-carrier transport
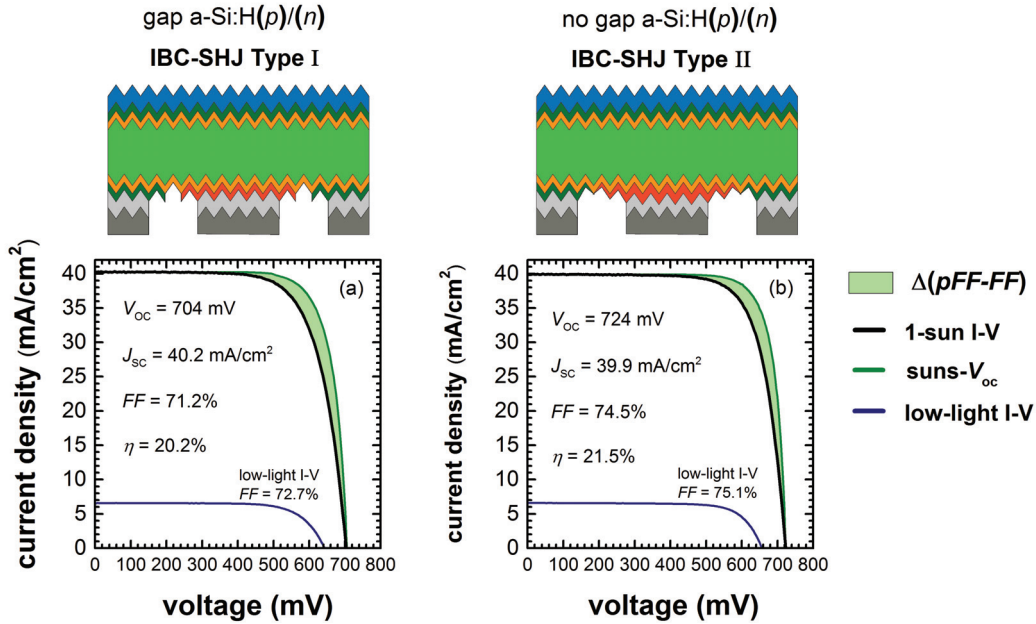
Figure 4.7: Pseudo I-V, 1-sun I-V and low light I-V characteristics of IBC-SHJ devices with and without a 100-μm-wide gap between the doped a-Si:H layers. The IBC-SHJ device architecture with a gap is depicted in Fig. 3.15, and the one without in Fig. 4.8. Both devices integrate the best ZnO:Al of section 4.5.3 and the best a-Si:H(p) of section 4.5.4. The device without a gap is IBC-SHJ[2] of section 4.5.4. The light green areas, between pseudo I-V and 1-sun I-V curves, indicate the *FF* losses due to charge-carrier transport.

can play an important role. In our first IBC-SHJ devices the measured device *FF*s were as low as 55 % despite high implied-*FF* and *pFF* values. In addition, the *FF* strongly recovered under low illumination. These are signatures of high *FF* losses due to charge-carrier transport, and of high device R_{series}, which in section 4.5.6 we attribute to carrier transport through the hole and electron contacts. In this context, the improved *FF*s we eventually achieved in the thesis, result primarily from efforts directed at the optimization of the heterocontact transport properties.

Here, we present showcase IBC-SHJ solar cells with developments that reduce charge-carrier transport losses. These results unambiguously demonstrate the importance of heterocontacts in high-efficiency IBC-SHJ devices. More specifically, they show the huge impact of the materials used as the electron and hole contacts on the overall device R_{series} and the associated *FF* losses. The contacting properties of TCO films (section 4.5.3) and doped a-Si:H layers (section 4.5.4), more than in the case of FHC and RHC SHJ devices, are crucial in achieving good device *FF*s.

It is worth specifying here, with respect to the SHJ solar cell *FF*-loss analysis presented in section 4.5.3, 4.5.4 and 4.5.5, that R_{shunt}s provide negligible contributions. In our devices, the R_{shunt} values were extracted from the slope of a linear fit to the dark I-V characteristic, in the

(a) Cross-sectional schematic of the solar cell architecture **IBC-SHJ Type II**. There is **(1)** no gap between the a-Si:H(*p*) and a-Si:H(*n*) layers, **(2)** an increased distance between the TCO/metal edge and a-Si:H(*p*) edge and **(3)** an increased thickness of the doped a-Si:H layers, in respect to the architecture IBC-SHJ Type I, of Fig. 3.15.

(b) Bottom-view schematic of the improved IBC-SHJ solar cell architecture of (a). For clarity, the TCO and metal electrodes are omitted. Note the absence of a gap in between the a-Si:H(*p*) and a-Si:H(*n*) fingers.
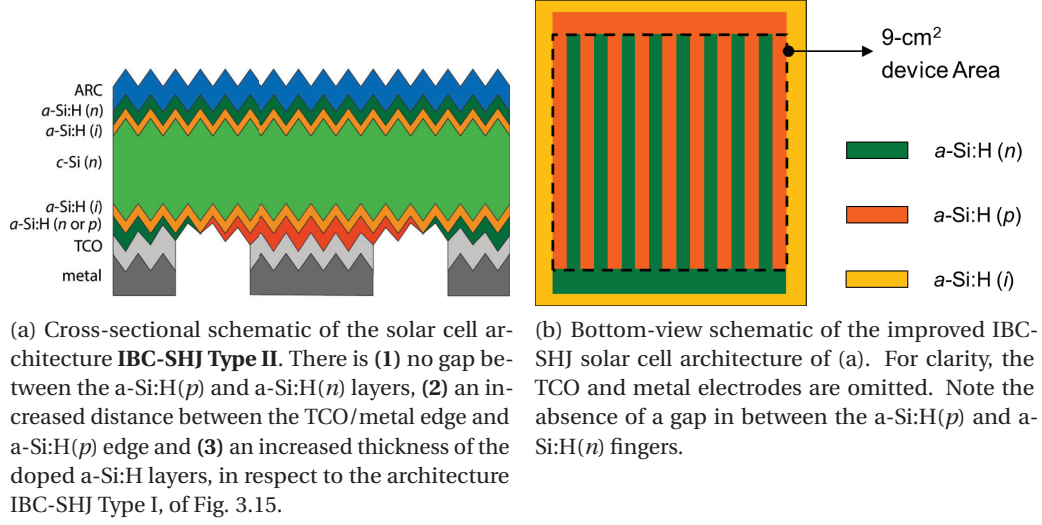
Figure 4.8: Cross-sectional and bottom-view schematics of the improved IBC-SHJ solar cell architecture: **IBC-SHJ Type II**.

range (-100,0) mV. In general, we measured high R_{shunt} values, i.e. $R^{\text{N}}_{\text{shunt}} \geqslant 50\,k\Omega\,\text{cm}^2$, both for IBC-SHJ and conventional two-side-contacted SHJ architectures. Based on the method of section 2.3.1, we find that $\Delta FF_{R_{\text{shunt}}} = FF_s - FF_{s,sh} < 0.1\,\%$. We conclude that shunt-related effects on *FF* are negligible for both of our IBC-SHJ and conventional two-side-contacted SHJ solar cells.

The overall R_{series} of a SHJ device results from the addition of several different series-resistance contributions. With the aid of a basic model of the different series-resistance contributions in our IBC-SHJ devices, we were able to interpret our experimental results and analyse, quantitatively, the dominant role played by the heterocontacts. This model and its major outcomes are described in section 4.5.6. A comparison with FHC SHJ devices is didactic and helps to guide the IBC-SHJ development.

4.5.2 Experimental details

The IBC-SHJ solar cells presented in this section integrate the best hole-collecting electrode of section 4.4. The device structure is depicted in Fig. 4.8. Its fabrication process and the front-side stack are described in section 3.4. In IBC-SHJ devices with this baseline architecture, we show the effects of using different TCOs (section 4.5.3) and different doped a-Si:H films (section 4.5.4) in the back contact. Importantly, the devices presented in section 4.5.3 use the best doped a-Si:H layers of section 4.5.4, whereas the devices presented in section 4.5.4 use the best TCO material of section 4.5.3. Indium tin oxide (ITO) films were sputtered from an In_2O_3-SnO_2 target [Buchanan 1980], nominally at room temperature, whereas aluminium-doped zinc oxide (ZnO:Al) films were sputtered at a temperature of 60 °C. Boron-doped zinc oxide (ZnO:B) layers were deposited by low-pressure chemical vapor deposition (LPCVD)

[Wenas 1991] at a temperature of around 175 °C. Further details on the deposition system and related methodology can be found elsewhere [Faÿ 2005].

Our best certified 4-cm^2 FHC SHJ device with a Ag screen-printed grid at the front [Descoeudres 2013], features a-Si:H(*ip*) and a-Si:H(*in*) layer stacks that, apart from the deposition time, were deposited with the same plasma conditions as were used for IBC-SHJ[1] of section 4.5.4. As contact layers this best FHC SHJ solar cell features a highly transparent IO:H/ITO stack, at the front, and a full-area ITO/Ag electrode at the back side. We remark that this FHC SHJ device [Descoeudres 2013] will be used as reference two-side-contacted SHJ solar cell throughout the entire thesis; from now on it will be referred as the **"reference FHC SHJ"** solar cell.

4.5.3   The impact of TCO materials

Hole and electron contacts in SHJ solar cells consist of a-Si:H(*ip*) and a-Si:H(*in*) layer stacks, respectively, deposited on the c-Si wafer surface and capped by a *n*-type TCO film. The TCO overlayer is needed primarily for carrier extraction and is in direct contact with the metal electrode, which eventually transports the collected carriers to the external circuit. Importantly, the TCO film should be considered as an integral part of the hole and electron contacts. For c-Si(*n*) SHJ-based devices, the TCO material properties were shown to influence both hole and electron contact transport properties [Bivour 2014b, Kirner 2015] and hole contact passivation [Tomasi 2016b, Favre 2013, Macco 2014, Demaurex 2014, Rößler 2013]. The challenge of defining the optimum TCO film properties, for simultaneous good charge-carrier transport and passivation at the contacts, is not trivial and will be addressed in chapter 5.

In Fig. 4.9, we report on identical IBC-SHJ solar cells using different TCO materials in both the electron and hole contacts. Importantly, these same TCO films are used in our laboratory for back-contact fabrication in conventional high-efficiency two-side-contacted FHC and RHC SHJ devices, with minor variations in terms of device electrical parameters. The TCO film properties are reported in Table 4.2. We note that the wet-chemical-etching procedure for back-electrode fabrication had to be adapted to the different TCO materials, as described in section 3.3.3, and that the a-Si:H layers used in these devices are the same as those used in IBC-SHJ[2] (see section 4.5.4).

The 1-sun I-V characteristics of the IBC-SHJ solar cells using ITO and ZnO:B are characterized by significantly lower *FF* values, with respect to the cell using ZnO:Al. Conversely, all three cells show similarly high *pFF*s and low-light *FF*s values, which indicate that such low *FF*s, in the case of ITO and ZnO:B, are determined by carrier transport losses. A quantitative assessment of these losses is possible by comparing the R_{series}^{N} values and the associated $\Delta FF_{R_{series}}$ values. The device electrical parameters are summarized in Table 4.3. $\Delta FF_{R_{series}}$ values are calculated using the semi-empirical equations of Green *et al.* [Green 1982], as described in section 2.3.1. Interestingly, indications of improved charge-carrier transport properties for ZnO:Al-based electron contacts, were reported also by Tatsuro *et al.* [Tatsuro 2015]. It is worth noting that, the use of different TCO materials in hole and electron contacts leads to different $\Delta FF_{R_{series}}$,

Table 4.2: TCO films used in the back electrode of the IBC-SHJ solar cells in Fig. 4.9.

Material	Thickness (nm)	Carrier density (cm^{-3})	Hall mobility ($cm^2 V^{-1} s^{-1}$)	ρ_{TCO} ($\Omega\,cm$)
ITO	154	$3.3 \cdot 10^{19}$	26.9	$7.0 \cdot 10^{-3}$
ZnO:B	184	$1.2 \cdot 10^{20}$	8.7	$6.1 \cdot 10^{-3}$
ZnO:Al	118	$3.6 \cdot 10^{20}$	14.9	$1.2 \cdot 10^{-3}$

Figure 4.9: Pseudo I-V, 1-sun I-V and low-light I-V characteristics of IBC-SHJ devices using the TCO films of Table 4.2 in both electron and hole contacts. The electrical parameters extracted from these curves are summarized in Table 4.3. The light green area indicates losses due to charge-carrier transport.

but similar $\Delta FF_{J_0(n \neq 1)}$ losses.

We shortly remark on the fact that the differences in J_{sc} for these cells are due to parasitic absorption losses in the long wavelength region, i.e. the J_{sc}-loss term J_{long} in the analysis of section 4.6. The IBC-SHJ with ZnO:Al in the back contact shows a J_{long} that is about $1\,mA\,cm^{-2}$ higher than in the cell with ZnO:B.

4.5.4 The impact of a-Si:H films

Charge-carrier transport at electron and hole contacts, beside the impact of TCO materials, is strongly influenced by the properties of a-Si:H(in) and a-Si:H(ip) film stacks.

In Fig. 4.10, we show two classes of IBC-SHJ solar cells with different a-Si:H film stacks in their heterocontacts. We chose two representative devices, **IBC-SHJ**[1] and **IBC-SHJ**[2], making use of an ZnO:Al film as described in Table 4.2. The a-Si:H layers of IBC-SHJ[1], apart from the deposition time, are deposited with the same plasma conditions as in our reference FHC SHJ device [Descoeudres 2013] (see also section 4.5.5). The IBC-SHJ[2] device instead belongs to an entire class of devices fabricated in a different PECVD reactor, and with a-Si:H layers in which plasma conditions were specifically tuned for improved carrier transport at the two

Table 4.3: Electrical parameters and *FF* losses of IBC-SHJ devices using the TCO films of Table 4.2 in both electron and hole contacts.

Parameter	IBC-SHJ with ITO	IBC-SHJ with ZnO:B	IBC-SHJ with ZnO:Al
V_{oc} (mV)	720	715	719
J_{sc} (mA/cm^2)	38.4	39.8	38.7
η (%)	19.2	17.0	21.0
FF (%)	69.5	60.0	75.4
R_{series}^{N} ($\Omega\,cm^2$)	2.4	4.3	1.4
pFF (%)	80.9	82.0	81.8
$\Delta FF_{R_{series}}$ (%)	11.7	21.3	6.9
$\Delta FF_{J_0(n\neq 1)}$ (%)	3.6	3.5	2.5

heterocontacts [Descoeudres 2015]. IBC-SHJ[1] and IBC-SHJ[2] show similar V_{oc} and J_{sc} values, of about 725 mV and in the range 39.5 mA cm^{-2} to 40.0 mA cm^{-2}, respectively, but different *FF*s. The higher *FF* of IBC-SHJ[2], which is approaching 75 %, resulted from a decrease in series resistance and is representative of a general *FF* increase, in our IBC-SHJ devices, which allowed for a significant efficiency enhancement. The electrical parameters of these devices are summarized in Table 4.4. [2]

The normalized series resistance of IBC-SHJ[1] equals R_{series}^{N} = 2.1 Ω cm^2, which determines $\Delta FF_{R_{series}}$ losses greater than 10 % absolute. For IBC-SHJ[2] results R_{series}^{N} = 1.3 Ω cm^2 and $\Delta FF_{R_{series}}$ = 6.6 %. Thus, from IBC-SHJ[1] to IBC-SHJ[2], *FF* losses due to carrier transport are reduced by roughly 4 % absolute. However, $\Delta FF_{J_0(n\neq 1)}$ is large for IBC-SHJ[2], accounting for a 3.8 % absolute *FF* loss, compared to 1.6 % for IBC-SHJ[1]. For clarity, in Fig. 4.11, we represent the different contributions to the overall *FF* loss in IBC-SHJ[1] and IBC-SHJ[2].

The increased value of $\Delta FF_{J_0(n\neq 1)}$ for IBC-SHJ[2] can be clearly linked with a lack of passivation in the excess minority carrier injection range $< 3 \cdot 10^{15}$ cm^{-3}. By calculating the implied-*FF* value of the injection-level-dependent lifetime data of the IBC-SHJ[2] cell precursor, after the deposition of the intrinsic and doped a-Si:H layers, we extract a value that is around 2 % lower than that of IBC-SHJ[1]. This value is in agreement with the observed variation of $\Delta FF_{J_0(n\neq 1)}$.

Our experimental results indicate again, as in section 4.5.3, the importance of electron and hole contact stacks in determining the *FF* of IBC-SHJ devices. However, in contrast to the impact of the TCO materials, the a-Si:H film properties impact both transport and diode non-ideality *FF* losses, i.e. losses due to increased recombination with $n \neq 1$. The reduction of $\Delta FF_{R_{series}}$ in IBC-SHJ[2] is achieved at the expenses of increased $\Delta FF_{J_0(n\neq 1)}$ losses, compared to IBC-SHJ[1]. This is clearly illustrated in Fig. 4.11 and suggests that the contact passivation and carrier transport properties of SHJ heterocontacts are entangled and difficult to be independently
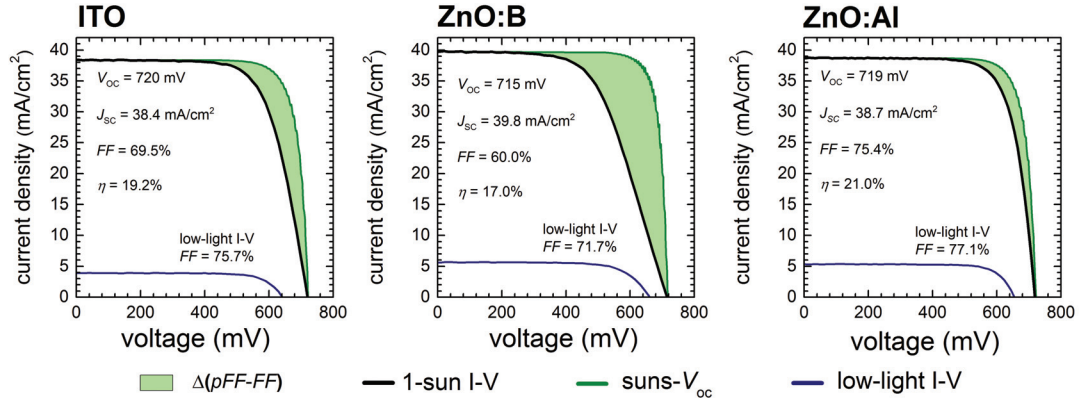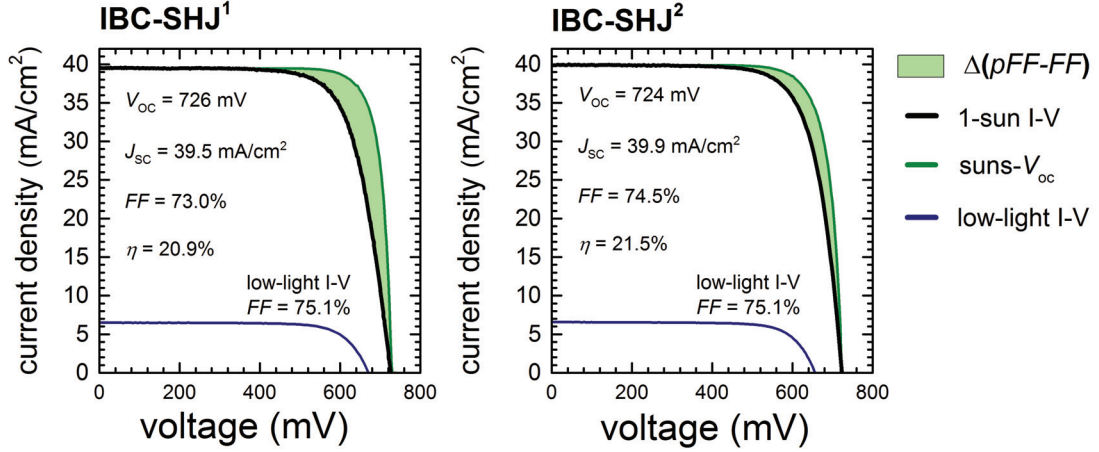
Figure 4.10: Pseudo I-V, 1-sun I-V and low-light I-V characteristics of IBC-SHJ devices using different doped a-Si:H films in electron and hole contacts. The a-Si:H layers used in the heterocontacts of IBC-SHJ[1] are those of our reference FHC SHJ device [Descoeudres 2013]. The electrical parameters extracted from these curves are summarized in Table 4.4. The light green area indicates losses due to charge-carrier transport.

optimized. This is not exclusive to SHJ contacts, but concerns passivating contact technologies in general.

4.5.5 Comparison of IBC-SHJ and reference FHC SHJ solar cells

Here we compare our reference FHC SHJ solar cell [Descoeudres 2013] with IBC-SHJ[1] and IBC-SHJ[2] (see Table 4.4 and Fig. 4.13), with the aim of identifying the main differences in term of FF limiting mechanisms.

The V_{oc} of the reference FHC SHJ solar cell (727 mV) is only 1 mV higher than that of IBC-SHJ[1], which demonstrates the compatibility of our IBC-SHJ processing sequence with high-quality a-Si:H passivation layers. The measured J_{sc} of 38.9 mA cm^{-2}, as expected, is lower than for the IBC-SHJ devices. The J_{sc} difference remains ≤ 1 mA cm^{-2}, which is still a modest gain for the back-contacted architecture (see discussion in section 4.6). Conversely, the FF of 78.4 % is significantly higher which results from $R_{series}^{N} = 1.1\,\Omega$ cm, $\Delta FF_{R_{series}} = 5.2$ % and $\Delta FF_{J_0(n\neq1)}$ = 1.4 %. The total FF loss equals $\Delta FF_{total} = \Delta FF_{R_{series}} + \Delta FF_{J_0(n\neq1)} = 6.6$ %, which is about 6 % and 4 % absolute lower than for IBC-SHJ[1] and IBC-SHJ[2], respectively. This is in line with the observed differences in final device FFs. This reference FHC solar cell, which uses the a-Si:H layer stacks of IBC-SHJ[1], shows the same low FF recombination losses of IBC-SHJ[1] but lower FF carrier transport losses, on the same level of IBC-SHJ[2]. This is in line with the simulation results of section 4.5.6, where by assuming fixed heterocontact properties in an IBC-SHJ device we forecast higher carrier transport losses, compared to a conventional FHC SHJ device. Re-optimizing the heterocontact properties for the IBC-SHJ device architecture, in IBC-SHJ[2] we were able to reduce $\Delta FF_{R_{series}}$, but we paid in terms of passivation quality and
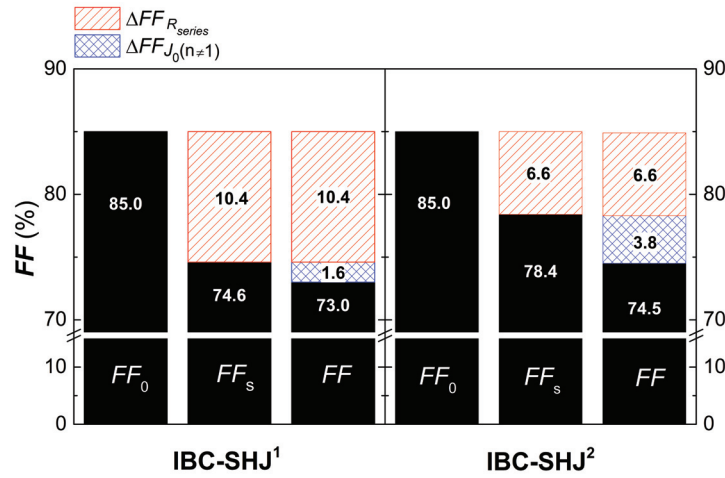
Figure 4.11: Breakdown of *FF* losses in IBC-SHJ devices using different a-Si:H films in both electron and hole contacts. The correspondent solar cell I-V curves and electrical parameters are shown in Fig. 4.10 and summarized in Table 4.4, respectively. The a-Si:H layers used in the heterocontacts of IBC-SHJ[1] are those of our reference FHC SHJ device [Descoeudres 2013]. Adapted with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

$\Delta FF_{J_0(n \neq 1)}$ losses. This emerges clearly in Fig. 4.12, which compares the injection-dependent lifetime curves of the reference FHC SHJ, IBC-SHJ[1] and IBC-SHJ[2] cell precursors. The first two curves coincide, whereas the latter one is increasingly lower for decreasing Δn values, which translates into lower implied-*FF* values.

Despite the fact that $\Delta FF_{R_{series}}$ in IBC-SHJ[2] is still a major contributor to *FF* losses, its value is close to that of an optimized FHC SHJ device. From this we can appreciate the results of our efforts towards minimization of carrier transport losses in IBC-SHJ devices. Since our very first devices, in which transport losses accounted for 10 % to 20 % absolute *FF* losses, by choosing appropriate TCO materials and a-Si:H layer stacks, we reduced $\Delta FF_{R_{series}}$ to values of about 6 %, similar to those of FHC SHJ devices.

In this comparison IBC-SHJ[1] and IBC-SHJ[2] are both emblematic. They show that our IBC-SHJ technology can attain, at least separately, similar levels of *FF* carrier transport losses and excellent passivation quality as in our reference FHC SHJ device.

4.5.6 Series-resistance components in IBC-SHJ and FHC SHJ solar cells

The case of IBC-SHJ devices

As series-resistance losses are an important *FF* limiting factor in IBC-SHJ devices, here we analyse in detail the different resistance components that contribute to the device overall R_{series}. In general, these can be divided into three classes:
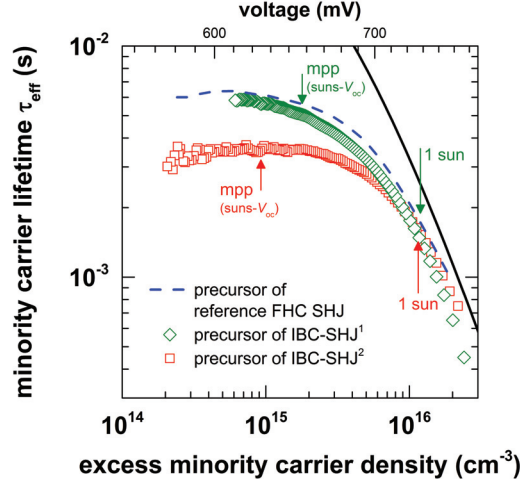
Figure 4.12: Minority carrier effective lifetimes of the IBC-SHJ[1] and IBC-SHJ[2] solar cell precursors after deposition of all intrinsic and doped a-Si:H layers (no further contacting layers are present). Corresponding implied-V_{oc} values, assuming a wafer resistivity of $3\,\Omega\,cm$ (N_D $= 1.4 \cdot 10^{15}\,cm^{-3}$), are reported on the top axis. The injection levels corresponding to 1-sun illumination and the maximum power point (mpp) in suns-V_{oc} measurements of finished devices are marked by solid arrows. The combined Auger and radiative limit is indicated by the solid line [Richter 2012]. For comparison, the dashed blue line shows also the lifetime curve associated with the solar cell precursor of the reference FHC SHJ device presented in section 4.5.5. Adapted with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

1. bulk resistance (R_{bulk}) of the wafer,

2. finger (R_{finger}) and bus bar (R_{bb}) grid resistances, and

3. hole and electron contact resistances ($R_{contact}$).

R_{bulk} is linked to lateral charge-carrier transport in the bulk of the wafer between the two comb electrodes. R_{finger} and R_{bb} are associated with electrical conduction into the TCO/metal back contact; $R_{finger,p}$ and $R_{bb,p}$ refer to the hole collecting comb and $R_{finger,n}$ and $R_{bb,n}$ refer to the electron collecting comb. $R_{contact,p}$ and $R_{contact,n}$ are linked, respectively, to transport through the hole contact (c-Si(n)/a-Si:H(i)/a-Si:H(p)/TCO) and through the electron contact (c-Si(n)/a-Si:H(i)/a-Si:H(n)/TCO). Note that both stacks feature several interfaces, with each possibly affecting $R_{contact}$ and consequently R_{series}.

The several orders of magnitude difference between the metal and TCO layer resistivities causes the latter to act in principle as a resistive buffer layer for transverse carrier extraction. However, as a result of typical TCO resistivity ($1 \cdot 10^{-3}\,\Omega\,cm$ to $2 \cdot 10^{-3}\,\Omega\,cm$), TCO thickness ($\leq 100\,nm$), and TCO/metal specific contact resistivity ($< 1 \cdot 10^{-3}\,\Omega\,cm^2$), series-resistance contributions linked with transport through the TCO layer to the metal layer, perpendicular to the wafer, are negligible ($< 1 \cdot 10^{-2}\,\Omega\,cm^2$). Due to the difference in the metal and TCO layer resistivity, the TCO does not contribute to lateral carrier conduction into the back contact.

Table 4.4: Electrical parameters and *FF* losses of our reference FHC SHJ device [Descoeudres 2013] and IBC-SHJ devices using different doped a-Si:H films in electron and hole contacts. The a-Si:H layers used in the heterocontacts of IBC-SHJ[1] are those of the reference FHC SHJ device. Adapted with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

Parameter	IBC-SHJ[1] [Tomasi 2014a]	IBC-SHJ[2] [Tomasi 2014a]	Ref. FHC SHJ [Descoeudres 2013]
V_{oc} (mV)	726	724	727
J_{sc} (mA/cm^2)	39.5	39.9	38.9
η (%)	20.9	21.5	22.1
FF (%)	73.0	74.5	78.4
R^N_{series} ($\Omega\,cm^2$)	2.1	1.3	1.1
pFF (%)	83.0	80.6	84.4
$\Delta FF_{R_{series}}$ (%)	10.4	6.6	5.2
$\Delta FF_{J_0(n\neq1)}$ (%)	1.6	3.8	1.4

The R_{finger} and R_{bb} values can thus be considered as merely metal line resistances. The typical values indicated above are those of the layers employed in our IBC-SHJ devices; TCO resistivity was measured by Hall effect measurements, TCO thickness by means of a stylus profiler and TCO/metal specific contact resistivity by means of the transfer length method [Berger 1972]. The precise derivation of the series-resistance components specific to our IBC-SHJ solar cell design is given in the appendix A.1. The normalized cell series resistance $\left(R^N_{series}\right)$ equals

$$R^N_{series} = R^N_{bulk} + \left(R^N_{finger} + R^N_{bb} + R^N_{contact}\right)_n + \left(R^N_{finger} + R^N_{bb} + R^N_{contact}\right)_p. \tag{4.1}$$

Based on equation 4.1, we now evaluate the magnitude of the different series-resistance components and their associated *FF* losses. For this, we take experimental values, from our IBC-SHJ solar cells, for the wafer and TCO/metal stack properties, the back-contact geometry and the excess minority carrier density at the mpp.

We find that transport losses at the heterocontacts have a dominating role in the determination of the total device R^N_{series} and the associated $\Delta FF_{R_{series}}$. In the range of specific contact resistivity values $0.1\,\Omega\,cm^2$ to $0.5\,\Omega\,cm^2$, for both hole $(\rho_c)_p$ and electron $(\rho_c)_n$ heterocontacts, the *FF* loss associated with only the contact resistance component goes from a minimum of 2.7 % absolute to 13.8 % absolute, which is indeed a significant loss. The range of $0.1\,\Omega\,cm^2$ to $0.5\,\Omega\,cm^2$ covers most of the values reported in the literature for the specific contact resistivity of optimized SHJ heterocontacts [Lee 2014, Haschke 2013, Gogolin 2014]. On the other hand, the *FF* loss associated with lateral conduction in the bulk of the wafer accounts for slightly more than 1.5 % absolute, and the overall *FF* loss associated with the different grid resistance components is about 1.7 % absolute.
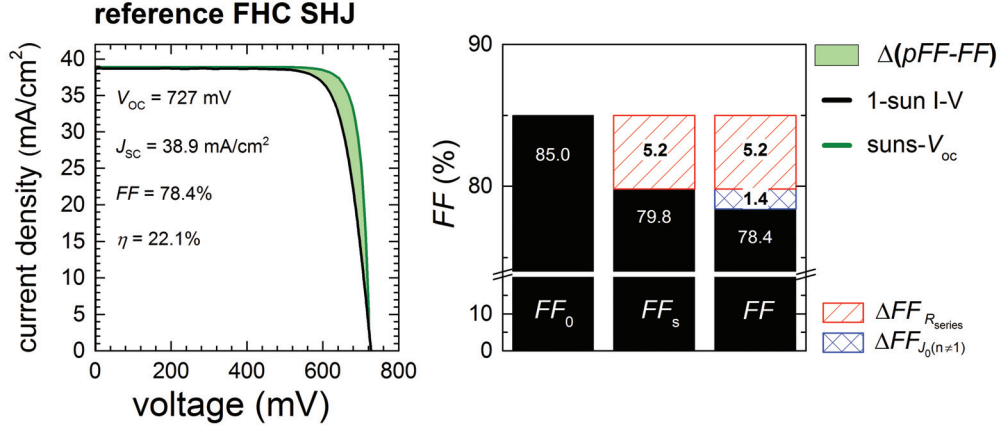
Figure 4.13: Pseudo I-V and 1-sun certified I-V of our reference FHC SHJ device [Descoeudres 2013]. The electrical parameters extracted from these curves are summarized in Table 4.4. The light green area indicates losses due to charge-carrier transport.

For a certain value of $R_{\text{series}}^{\text{N}}$, via the calculation of the correspondent $\Delta FF_{R_{\text{series}}}$, we can calculate a maximum attainable FF with the hypothesis that only recombination mechanisms with $n = 1$ and such FF carrier transport losses are present. This maximum attainable FF corresponds to FF_s, as defined in section 2.3.1 and Fig. 2.3 (a). Thus, based on the calculation of the different series-resistance components, we can model FF_s as a function of the variables of interest. In Fig. 4.14, for our IBC-SHJ device, we give calculated values of $R_{\text{series}}^{\text{N}}$ and the maximum attainable FF as a function of $(\rho_c)_p$ and $(\rho_c)_n$. This contour plot shows the effect of hole and electron contact transport properties on the FF of back-contacted devices.

For the sake of completeness, we briefly note the care to be taken when considering the maximum attainable FF value, i.e. FF_s, based on the assumption of $n = 1$. Considering fully-optimized IBC-SHJ devices, as those of Panasonic [Masuko 2014] and Sharp [Nakamura 2014], this assumption is not valid and n should be set equal to 2/3 (see the discussion in section 2.3.1). This results in similar $\Delta FF_{R_{\text{series}}}$ but higher FF_0 values which allow for the high FF values of these devices, of about 82 %, that otherwise according to Fig. 4.14 could hardly be explained.

The case of FHC SHJ devices

With the aim of comparing IBC-SHJ devices with conventional two-side-contacted SHJ devices, here we extend the analysis of series-resistance components to the case of FHC SHJ solar cells.

In FHC SHJ devices we can distinguish R_{bulk}, R_{contact}, R_{finger} and R_{bb} as in IBC-SHJ devices. However, this time R_{finger} and R_{bb} refer to the front-grid electrode only, which is in contact with the p-type a-Si:H hole collector. For the sake of clarity, we add the superscript p. In addition, two more series-resistance components must be included in the analysis:

1. lateral resistance of the front TCO film ($R_{\text{lateral,TCO}}$), and
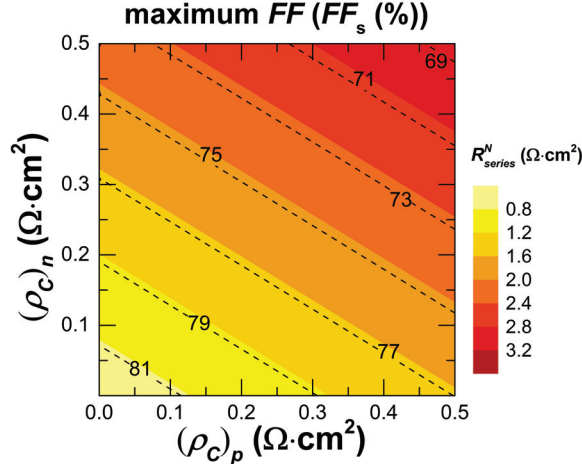
Figure 4.14: Simulated normalized series resistance $\left(R_{\text{series}}^{\text{N}}(\Omega\,\text{cm}^2)\right)$ in our IBC-SHJ device and the associated maximum attainable *FF* ($FF_s(\%)$), as a function of heterocontact specific contact resistivity $(\rho_c)_p$ and $(\rho_c)_n$. Contact fractions, in our back-contacted design, correspond to about ~ 45 % and ~ 30 % of the back-surface of the cell (excluding the bus bar area), for the hole and electron contacts, respectively; the pitch is of 2.6 mm. FF_s is calculated assuming a single diode with $n = 1$ and carrier transport losses according to $R_{\text{series}}^{\text{N}}$. Dashed contour lines delimit regions of FF_s values, whereas the color map represents $R_{\text{series}}^{\text{N}}$ values. Adapted with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

2. contact resistance between metal front-grid electrode and TCO film ($R_{\text{TCO/Metal,p}}$).

$R_{\text{lateral,TCO}}$ originates from the charge-carriers extracted by the front hole collector which travel laterally, in the TCO film, to the metal front-grid electrode. The contact resistance between the TCO and metal, for contacts with a full metal coverage, can be neglected (as in FHC SHJ or IBC-SHJ back contacts). However, this is not the case for front-grid electrodes, whose contact area is minimized to reduce shadowing losses. The precise derivation of the different series-resistance components in FHC SHJ devices is given in the appendix A.2. Thus, the normalized cell series resistance equals

$$R_{\text{series}}^{\text{N}} = R_{\text{bulk}}^{\text{N}} + \left(R_{\text{contact}}^{\text{N}}\right)_n + \left(R_{\text{contact}}^{\text{N}}\right)_p + R_{\text{lateral,TCO}}^{\text{N}} + R_{\text{TCO/Metal,p}}^{\text{N}} + R_{\text{finger,p}}^{\text{N}} + R_{\text{bb,p}}^{\text{N}}. \quad (4.2)$$

Based on equation 4.2, we now evaluate the magnitude of the different series-resistance components and their associated *FF* losses. For this, we take experimental values from our FHC SHJ solar cells for the wafer and TCO properties, the front-grid electrode geometry, the TCO/metal grid contact and the minority carrier injection level at the mpp.

We find that transport losses at the heterocontacts have a reduced impact on the overall device $R_{\text{series}}^{\text{N}}$, compared to IBC-SHJ devices. In Fig. 4.15 (a), similarly as in Fig. 4.14, we report the maximum attainable *FF* and $R_{\text{series}}^{\text{N}}$ values for our FHJ SHJ devices. Here, in the range of specific contact resistivity values of $0.1\,\Omega\,\text{cm}^2$ to $0.5\,\Omega\,\text{cm}^2$, for both hole $(\rho_c)_p$ and electron
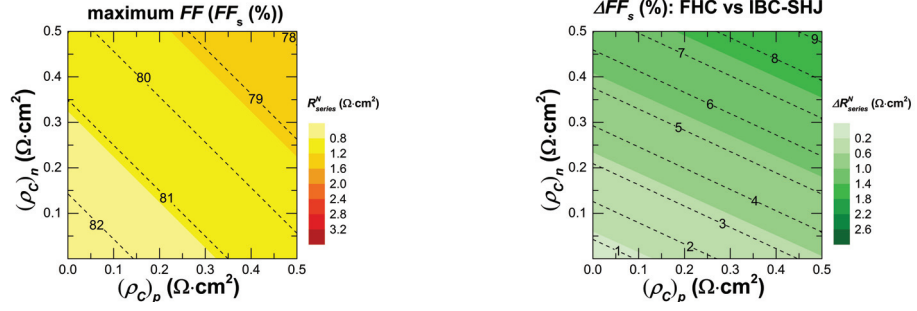
(a) Simulated normalized series resistance $\left(R^{\mathrm{N}}_{\mathrm{series}}\left(\Omega cm^2\right)\right)$ and maximum attainable FF (FF_s(%)), of our FHC SHJ device as a function of heterocontact specific contact resistivity. Both hole and electron contact fractions equal 100 % of the cell surface. Dashed contour lines delimit regions of FF_s values, whereas the color map is used to represent $R^{\mathrm{N}}_{\mathrm{series}}$ values.

(b) Simulated normalized series resistance difference $\left(\Delta R^{\mathrm{N}}_{\mathrm{series}}\left(\Omega cm^2\right)\right)$ and absolute gain in maximum attainable FF (ΔFF_s(%)) for FHC SHJ vs IBC-SHJ devices. Dashed contour lines delimit regions of ΔFF_s (%) gain values, whereas the color map is used to represent $\Delta R^{\mathrm{N}}_{\mathrm{series}}$ values.

Figure 4.15: Simulated impact of heterocontact transport properties on the normalized series resistance ($R^{\mathrm{N}}_{\mathrm{series}}$) and the maximum attainable FF (FF_s) of FHC SHJ solar cells and compared to IBC-SHJ devices.

$\left(\rho_c\right)_n$ heterocontacts, the FF loss associated with only the contact resistance component goes from a minimum of 1 % absolute to 5 % absolute. This is evidence of the reduced impact of heterocontacts on $R^{\mathrm{N}}_{\mathrm{series}}$. To highlight the difference with IBC-SHJ devices, we subtracted from Fig. 4.15 (a), the maximum attainable FF and $R^{\mathrm{N}}_{\mathrm{series}}$ values for our IBC-SHJ devices (Fig. 4.14). The result is plotted in Fig. 4.15 (b), and represents the absolute gain in maximum attainable FF, for certain hole and electron contact transport properties, in FHC vs IBC-SHJ devices. In the same contour plot, the variation in overall $R^{\mathrm{N}}_{\mathrm{series}}$, which causes such differences in FF_s, is also reported. In contrast, the FF losses associated with transport in the bulk of the wafer and through the TCO/metal interface are almost negligible, about 0.2 % and 0.3 %, respectively. Conversely, lateral conduction in the TCO and in the front-grid electrode accounts for almost 2.0 %.

Matching experimental and simulation results

The results presented and discussed in sections 4.5.3 and 4.5.4 indicate the importance of contact optimization in IBC-SHJ devices with respect to overall $\Delta FF_{R_{\mathrm{series}}}$ losses. They can be reproduced in simulations assuming different ρ_c values for the different contacting solutions, i.e. different TCO materials or a-Si:H films.

We note that the problem of measuring ρ_c values for SHJ hole and electron contacts is not trivial. In our analysis we made a limited use of absolute ρ_c values, relying instead on ranges of ρ_c, inclusive of all previously reported values [Lee 2014, Haschke 2013, Gogolin 2014, Tatsuro 2015]. The discrimination of the different factors determining ρ_c for a SHJ contact is

also challenging and triggers further discussion in chapter 5.

Importantly, the same layers that allow $\eta > 22\,\%$ and $FF > 78\,\%$ in a FHC solar cell, generate a $\Delta FF_{R_{\text{series}}}$ loss over 10 % in back-contacted device, which is not compatible with high-efficiency devices. Similarly, TCO materials that perform well in conventional two-side-contacted SHJ devices are unsuitable for IBC-SHJ devices. These observations coincide with the outcomes of our series-resistance models which indicate increasingly high FF differences, for two-side-contacted SHJ vs IBC-SHJ technologies, for increasing ρ_{c} values.

To define guidelines for further device optimization, we attempt a qualitative assessment of the importance of each series-resistance contribution in our IBC-SHJ solar cells, matching our simulation and experimental results. We associated fixed values of $(\rho_c)_p$ and $(\rho_c)_n$ to the contacts used in IBC-SHJ[1] and IBC-SHJ[2], so that the resulting $R_{\text{series}}^{\text{N}}$ simulated values correspond to the measured values for these two devices. Based also on previously reported results [Lee 2014, Haschke 2013, Gogolin 2014, Tatsuro 2015], we presumed $(\rho_c)_p = 0.45\,\Omega\,\text{cm}^2$ and $(\rho_c)_p = 0.2\,\Omega\,\text{cm}^2$ for IBC-SHJ[1] and IBC-SHJ[2] hole contacts, respectively, and $(\rho_c)_n = 0.2\,\Omega\,\text{cm}^2$ and $(\rho_c)_n = 0.1\,\Omega\,\text{cm}^2$ for IBC-SHJ[1] and IBC-SHJ[2] electron contacts, respectively. These values reproduce not only the measured $R_{\text{series}}^{\text{N}}$ values for the device IBC-SHJ[1] and IBC-SHJ[2], but also those of conventional two-side-contacted FHC SHJ devices fabricated with the respective a-Si:H layers. Assuming the $(\rho_c)_p$ and $(\rho_c)_n$ values of IBC-SHJ[1], in a FHC SHJ device, we achieve $R_{\text{series}}^{\text{N}} = 1.1\,\Omega\,\text{cm}^2$, which is much lower than $R_{\text{series}}^{\text{N}} = 2.1\,\Omega\,\text{cm}^2$ and equals the measured series resistance of the reference FHC SHJ device [Descoeudres 2013], presented in section 4.5.5 and fabricated with the same a-Si:H layers used in IBC-SHJ[1]. Differently, with the heterocontact properties of IBC-SHJ[2], in a conventional two-side-contacted FHC SHJ device, we achieve more similar $R_{\text{series}}^{\text{N}}$ values, which reflect well those measured for the best FHC SHJ devices fabricated at CSEM, Switzerland [Descoeudres 2015], with the same a-Si:H layers used in the fabrication of IBC-SHJ[2].

In the models, we can now analyse the importance of the different series-resistance components for the different specific devices and architectures (see Fig. 4.16). The series-resistance component associated with the heterocontacts is always important, particularly with back-contacted architectures. From the comparison of the results for IBC-SHJ[1] and IBC-SHJ[2], we can appreciate the results of our effort with respect to contact optimization and the increased relevance of all other series-resistance components. As a consequence, further device series-resistance optimizations will need to start by considering also contributions other than those associated with the heterocontacts.

4.5.7   Conclusion (II)

Losses due to charge-carrier transport are an important limiting mechanism for the FF of IBC-SHJ devices. In this section we presented the main milestones in the achievement of $\Delta FF_{R_{\text{series}}}$ on a level similar to that of optimized FHC SHJ devices. The actions taken to reduce $\Delta FF_{R_{\text{series}}}$ concerns components of the heterocontacts, either the TCO or the a-Si:H layers.
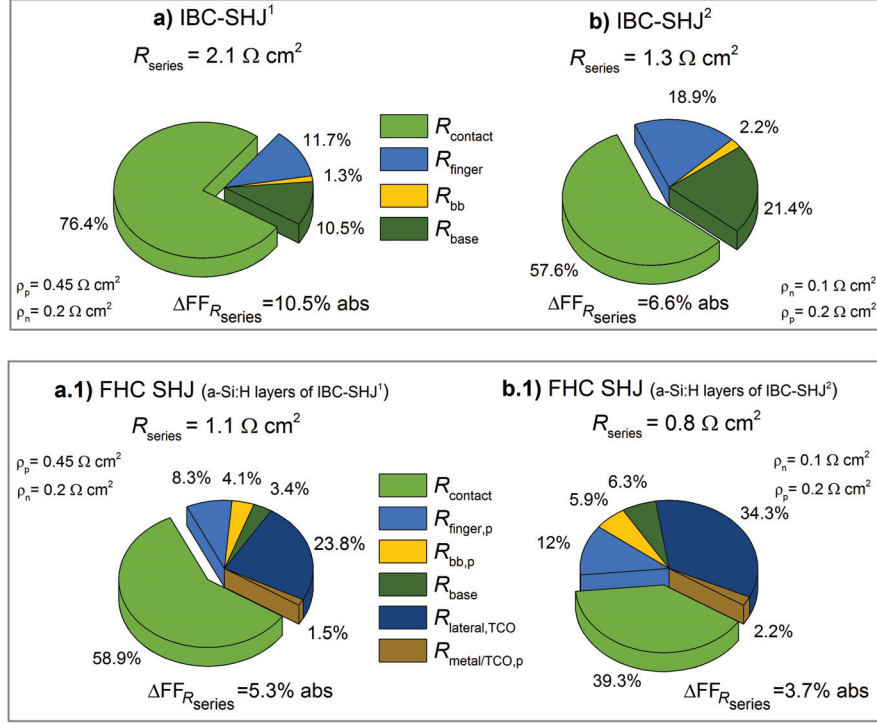
Figure 4.16: Simulated series-resistance contributions for IBC-SHJ devices with $R_{\text{series}}^{\text{N}}$ equal to that measured for our IBC-SHJ[1] (a) and IBC-SHJ[2] (b) solar cells. To match the measured $R_{\text{series}}^{\text{N}}$ values only $(\rho_c)_p$ and $(\rho_c)_n$ were varied, to account for the different a-Si:H-based contact stacks. All other simulation input parameters were based on values measured on the specific devices. In the inset (a.1) and (b.1) we report on conventional two-side-contacted FHC SHJ devices assuming the same $(\rho_c)_n$ and $(\rho_c)_p$ values as for IBC-SHJ[1] and IBC-SHJ[2].

This observation pairs with the results of our R_{series} simulations. This indicates that, compared to FHC SHJ devices, our IBC-SHJ devices exhibit (1) greater *FF* losses due to carrier transport through the heterocontacts, and (2) an increased dependency of *FF* losses due to carrier transport through the heterocontacts from contact resistivities values. This results in diverging FF_s values, for IBC-SHJ and FHC SHJ solar cells, at increasing values of $(\rho_c)_n$ and $(\rho_c)_p$, which explains why different heterocontacts giving similar performances in FHC SHJ solar cells could drastically affect the *FF* of IBC-SHJ devices. We remark that, overall, series-resistance losses now are at a tolerable level in our optimized devices and further device optimizations will need to target other losses, such as those determining $\Delta FF_{J_0(n\neq 1)}$ and implied-*FF*.

We observe that carrier transport losses are relevant with respect to the definition of the optimum back-contacted design. As we will see in the next section, carrier collection benefit from narrower electron-collecting fingers. However, smaller electron contact areas may degrade device *FF*s if $(\rho_c)_n$ values are not sufficiently low. Contextually, also R_{bulk} would suffer from narrower electron-collecting fingers, assuming a fixed half-pitch for the IBC geometry. From this perspective, the ultimate solution is perfect passivation. Longer effective hole

diffusion length (L_h) will decrease electrical-shading losses, reducing size constraints on the electron-collecting finger width, and allow higher excess minority carrier densities at mpp, decreasing R_{bulk} and reducing the importance of having small-pitch IBC geometry.

Evaluating the impact of different a-Si:H layers, we observed variations in both *FF* transport and recombination losses. This is not surprising as doped a-Si:H layers are themselves strongly involved in determining the level of c-Si surface passivation, mainly via field-effects [Tomasi 2016b]. Conversely, looking at the impact of different TCO materials, we identified mainly variations in transport losses. However, as it will be shown in chapter 5, minor TCO influences on contact passivation are also possible and may still play a role.

4.6 Optical-loss analysis and mitigation in IBC-SHJ solar cells (III)

4.6.1 Introduction

In section 4.3 we observed that, so far, top-J_{sc} values have been shown only by the outstanding devices of Panasonic, Japan [Masuko 2014] and Sharp, Japan [Nakamura 2014]. The reasons are not easily identifiable as several mechanisms may limit solar cell J_{sc} values. As a first step towards higher J_{sc}, we conducted an in-depth analysis of the J_{sc} losses in our IBC-SHJ devices. In this loss analysis we applied the method described in section 2.3.2. Here, we present the resulting J_{sc} loss breakdown for IBC-SHJ[2], the device discussed in section 4.5, compared to the reference FHC SHJ device [Descoeudres 2013]. Based on this analysis, we focused on the reduction of the reflection and parasitic absorption losses, at the front side of our back-contacted SHJ devices. Doing so, we obtained a J_{sc} gain of $1.0\,\text{mA}\,\text{cm}^{-2}$ compared to IBC-SHJ[2]. This enabled a highest-J_{sc} device with $J_{sc}= 40.9\,\text{mA}\,\text{cm}^{-2}$, yielding a conversion efficiency of 22.0 %.

4.6.2 Experimental details

The IBC-SHJ solar cells presented in this section combines the best hole-collecting electrode of section 4.4 and the best combination of TCO and a-Si:H materials of section 4.5. The device structure is depicted in Fig. 4.8, and the fabrication process is described in section 3.4. On this baseline architecture we evaluated four different thicknesses for the front side a-Si:H(n) layer, namely 12 nm, 6 nm, 1 nm and 0 nm (i.e. no front a-Si:H(n) at all), and a double-layer ARC (DARC) that consists of a 62-nm-thick layer of a-SiN$_x$:Hcapped with a 88-nm-thick a-SiO$_x$:H layer. The refractive index of these layers is 1.87 and 1.46 at a wavelength of 630 nm, respectively. Our reference FHC SHJ device [Descoeudres 2013], at the front side, features a thin a-Si:H(ip) layer stack, a highly-transparent IO:H/ITO stack, and a screen-printed metal grid with 4 % metallized area fraction. On the back side, it uses a full-area ITO/Ag electrode.
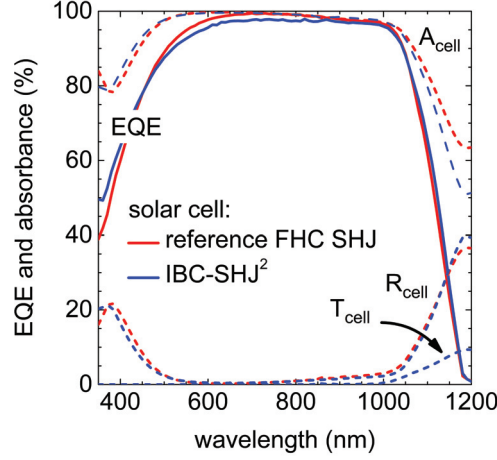
Figure 4.17: EQE, reflection, transmission and absorbance curves of the reference FHC SHJ and the IBC-SHJ^2 solar cells processed in our laboratory. Notice that the EQE curve for the FHC SHJ device does not account for the shadowing losses, as it is measured on a front-electrode-free device, as explained in section 2.3.2. Reproduced with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE.

4.6.3 Short-circuit current losses: FHC and IBC-SHJ solar cells [†]

For this comparison we consider our reference FHC SHJ device and IBC-SHJ^2, whose electrical parameters are summarized in Table 4.4. Their EQE, R_{cell}, T_{cell}, and A_{cell} curves are shown in Fig. 4.17. Note that the EQE of the FHC SHJ device is measured on a front-electrode-free device and it does not suffer from $J_{shadowing}$ losses. In addition, T_{cell} of the same device is zero as it features a fully metallized back side. As seen from Fig. 4.17, the EQE curves of the two solar cells are quite similar. Conversely, their absorbance curves differ in the long-wavelength region. This difference is related to the part of the long-wavelength light, that is transmitted through IBC-SHJ devices.

Using the method described in section 2.3.2, we calculated the J_{sc} losses of both solar cells; the results are presented in Fig. 4.18. The total J_{sc} loss for the FHC SHJ solar cell amounts to 6.9 mA cm^{-2}, compared to 5.9 mA cm^{-2} for the IBC-SHJ^2 solar cell, giving thus a 1.0 mA cm^{-2} loss difference between the two architectures. This is consistent with the difference in 1-sun J_{sc} experimentally measured on the two devices. Having a closer look at the J_{sc} loss breakdown in Fig. 4.18, we can see that some losses are common to the two solar cells and some are architecture-specific. First of all there is no front electrode shadowing loss for the IBC-SHJ solar cell. This alone represents a potential gain of about 1.3 mA cm^{-2} for back-contacted devices. In contrast, $J_{escape,back}$ is a peculiar feature of the IBC-SHJ device. This loss is caused by light escaping through the gap between the fingers of the back electrodes. This phenomenon is not present in the FHC SHJ solar cell as its back side is fully metallized. However, this does not mean that the FHC SHJ solar cell makes better use of this part of the spectrum:
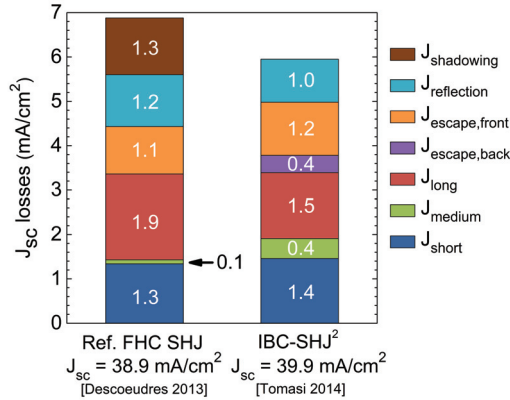
Figure 4.18: Comparison of short-circuit current losses in the reference FHC SHJ and IBC-SHJ solar cells processed in our laboratory, calculated with respect to the available photocurrent $J_{ph} = 45.9 \, \text{mA cm}^{-2}$. Reproduced with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE.

a significant amount of it can be lost within the TCO/metal back stack due to plasmonic absorption, in case of a suboptimal optical design, and thus contributes to long-wavelength parasitic absorption [Holman 2013a, Holman 2012]. Interestingly, the sum of $J_{escape,back}$ and J_{long} in IBC-SHJ^2 equals J_{long} of the reference FHC SHJ device. This brings us to the conclusion that $J_{escape,back}$ in IBC-SHJ^2 is mostly not an additional loss, but rather the consequence of a reduced absorption loss. Importantly, this light could possibly be recycled at the module level, e.g. by using a white back sheet. An important observation is the increased optical loss in the medium part of the spectrum for IBC-SHJ^2. This increase accounts for a J_{medium} loss that is $0.3 \, \text{mA cm}^{-2}$ higher in IBC-SHJ^2. This augmented loss appears to be decisive in limiting the J_{sc} gain brought by the back-contacted architecture to only $1.0 \, \text{mA cm}^{-2}$, compared to the potential gain of $1.3 \, \text{mA cm}^{-2}$ offered by the suppression of front-grid shadowing losses. This difference in J_{medium} may be attributed to electrical-shading losses, occurring above the electron-collecting regions in back-contacted devices [Lu 2011, Reichel 2011, Hermle 2008]. This type of carrier collection loss is discussed further in section 4.6.5. All the remaining J_{sc} loss terms are present in both solar cells and are found to be rather similar.

In conclusion, this comparison indicates that, in our actual IBC-SHJ devices, the potential gain in J_{sc} of the back-contacted architecture is only partially exploited. The potential gain brought by the absence of the front-grid electrode is partially compromised by an increased J_{medium} loss, which is most likely associated with electrical-shading losses. Such effects will be discussed in section 4.6.5. In addition, parasitic absorption of light in the front layers, which mostly determines J_{short}, is equivalent to our optimized FHC SHJ device. This equality demonstrates that further expected J_{sc} advantages of the back-contacted architecture, brought by the partial decoupling of the optical and electrical functions at the front side, have not been fully exploited. J_{short} and $J_{reflection}$ account for a loss of $1.4 \, \text{mA cm}^{-2}$ and $1.0 \, \text{mA cm}^{-2}$, respectively. Therefore, we can envisage J_{sc} gains from the optimization of our front-side
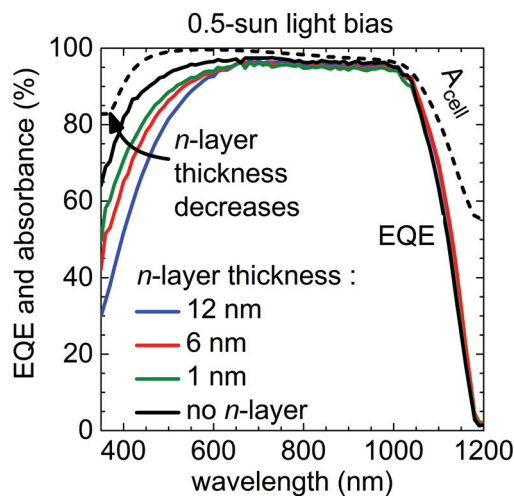
Figure 4.19: EQE curves of IBC-SHJ devices with various thicknesses (0, 1, 6 and 12 nm) of the a-Si:H(n) layer at the front , under a light bias of 0.5 sun. We also reported the measured absorbance curve (identical for all the solar cells within this batch). Adapted with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE.

passivating and anti-reflection film stack.

4.6.4 Mitigation of short-circuit current losses at the front-side of IBC-SHJ devices [†]

Aiming for improved J_{sc}, we tackled the J_{sc} losses occurring at the front side of our IBC-SHJ devices. We fabricated a series of IBC-SHJ devices with different thicknesses of the front a-Si:H(n) layer. The EQE curves measured on these devices (Fig. 4.19) show a clear trend of better device response, at short wavelength, for thinner a-Si:H(n) layers. This clearly results from reduced parasitic absorption in the thinner a-Si:H stack at the front. From these curves we calculated J_{short} which varied from a maximum of $2.5\,\mathrm{mA\,cm^{-2}}$ for the thicker a-Si:H(n) layer to a minimum of $0.6\,\mathrm{mA\,cm^{-2}}$ for the device with no a-Si:H(n) layer. From these data, for a device with no front a-Si:H(n) layer, we can envisage a potential J_{sc} gain of ~$1.0\,\mathrm{mA\,cm^{-2}}$ compared to our previous IBC-SHJ devices, such as IBC-SHJ[2], which has a 6-nm-thick front a-Si:H(n) layer.

The application of the DARC (as defined in section 4.6.2) on top of the front passivating layers helps further to reduce J_{sc} losses. In the case of our IBC-SHJ devices, comparing cells featuring either the standard ARC or the DARC scheme, we observed a reduction of the overall contribution $\left(J_{\mathrm{reflection}} + J_{\mathrm{escape,front}}\right)$ of about $0.2\,\mathrm{mA\,cm^{-2}}$. More specifically, this reduction resulted from a decrease of $J_{\mathrm{reflection}}$ of $0.4\,\mathrm{mA\,cm^{-2}}$ and an increase of $J_{\mathrm{escape,front}}$ of $0.2\,\mathrm{mA\,cm^{-2}}$. The latter may be explained by the overall increase in the light coupled into the wafer.
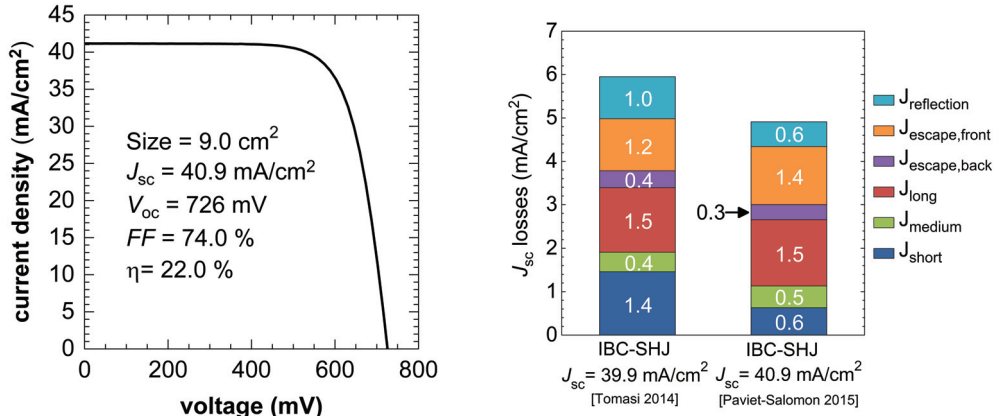
(a) 1-sun I-V characteristic of our J_{sc}-optimized IBC-SHJ device. Reproduced with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE.

(b) J_{sc} loss breakdown for IBC-SHJ[2] ($J_{sc} = 39.9$ mA cm^{-2}, see section 4.5) [Tomasi 2014a], and our new J_{sc}-optimized device, featuring a J_{sc} of 40.9 mA cm^{-2}. Reproduced with permission from [Paviet-Salomon 2015a]. Copyright © 2015, IEEE.

Figure 4.20: 1-sun I-V characteristic and J_{sc}-loss breakdown of an J_{sc}-optimized IBC-SHJ device featuring no front a-Si:H(n) layer and a DARC scheme at the front-side.

By applying this DARC scheme at the front of an IBC-SHJ device featuring only an a-Si:H(i) passivating layer, we could fabricate a J_{sc}-optimized device, whose J_{sc} reached almost 41 mA cm^{-2}, yielding a conversion efficiency of 22.0 %. In Fig. 4.20, we show the 1-sun I-V characteristic of this device and its J_{sc} loss breakdown compared to that of IBC-SHJ[2]. The removal of the a-Si:H(n) layer at the front reduces J_{short} by 0.8 mA cm^{-2}, whereas the DARC scheme decreases $J_{reflection}$ by 0.4 mA cm^{-2}. The overall J_{sc} gain is 1.0 mA cm^{-2}, instead of 1.2 mA cm^{-2}, due to an increase of 0.2 mA cm^{-2} in $J_{escape,front}$. Importantly, this J_{sc} improvement seen in Fig. 4.20 is not achieved at expense of other electrical parameters, which are very similar to those of IBC-SHJ[2]. This indicates that the field-effect passivation of the a-Si:H(n) layer at the front may not be imperative for high-efficiency IBC-SHJ devices.

4.6.5 J_{sc} losses and electrical-shading

As mentioned in section 4.6.3, comparing J_{sc} losses in FHC and IBC-SHJ devices, the latter suffer from higher J_{medium} values. We believe that this J_{sc} loss term is associated with electrical-shading losses [Lu 2011, Reichel 2011, Hermle 2008]. In n-type IBC devices, the minority carriers (holes) generated above the electron-collecting fingers must diffuse laterally to reach the closest hole-collecting region (see schematic of Fig. 4.21). In this process some of the holes recombine and are lost, lowering the final device J_{sc}. This distance is directly linked to the design of the interdigitated electrodes which, for this reason, typically present narrow electron-collecting fingers.

Comparing the half-pitch of an interdigitated back contact to the minority carrier diffusion
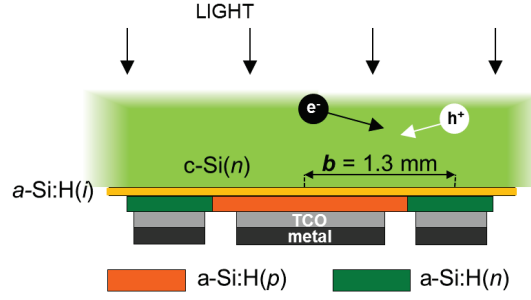
Figure 4.21: Cross-sectional schematic of the back contact used in our IBC-SHJ devices. Minority carriers (holes) generated above the electron contacts must diffuse laterally to reach the hole contact. Consequently, minority carrier recombination losses may affect the final 1-sun solar cell J_{sc}. The phenomenon is commonly referred as electrical shading [Lu 2011, Reichel 2011, Hermle 2008]. The half-pitch $b = 1.3$ mm of the back-contacted geometry used in the devices of this chapter is shown.

lengths measured on the solar cell precursor, after deposition of all a-Si:H layers, we can assess the presence of electrical-shading losses. τ_{eff} should be evaluated at Δn values close (as much as possible), to J_{sc} conditions, i.e. $\Delta n \approx 1 \cdot 10^{13}$ cm^{-3}. For all IBC-SHJ devices presented in this chapter the half-pitch of the back-contact is 1.3 mm. A hole diffusion length (L_h) equal to this distance, assuming an n-type c-Si wafer of resistivity $3\,\Omega$ cm as the substrate, implies $\tau_{eff} = L_h^2/D_h = 1.4$ ms. These values do not exclude the possibility of having a certain amount of electrical-shading losses in our IBC-SHJ devices. As confirmation, in our IBC-SHJ devices we observed strong detrimental effects on the final 1-sun solar cell J_{sc} for low values of τ_{eff} (data not shown). For reference, a clear example of such a relation between J_{sc} and τ_{eff} can be found in Fig. 6.8. The overall result is that electrical-shading losses make the J_{sc} of back-contacted devices much more sensitive to the level of surface passivation, compared to the case of two-side-contacted devices.

To unambiguously point at electrical-shading losses to explain the J_{sc}-τ_{eff} relation, we performed light-beam-induced current (LBIC) characterizations on two IBC-SHJ cells characterized by *high*- and *low*-passivation qualities (and J_{sc}), respectively. The τ_{eff} values, measured at Δn of $5 \cdot 10^{14}$ cm^{-3}, on the respective solar cell precursors were higher and lower than 1.4 ms, respectively. In Fig. 4.22, we show the LBIC cross-sectional profiles of such showcase devices. We scanned the entire 30-mm-wide active area of the solar cell, perpendicularly to the hole- and electron-collecting fingers, at a distance of 1 cm from the bus bar of the electron contact. For the IBC-SHJ with low-quality passivation we observed a significant drop in the LBIC signal, over the electron-collecting fingers, which explains the lower overall J_{sc}. For the IBC-SHJ with high-quality passivation, this drop is significantly smaller, despite being still present. These observations clearly confirm the hypothesis that electrical-shading losses grow in our back-contacted devices with decreasing passivation quality. In addition, we note that IQE/EQE curves measured on such devices showed increased J_{medium} losses, which strongly motivates the association of this J_{sc} loss term with electrical-shading.
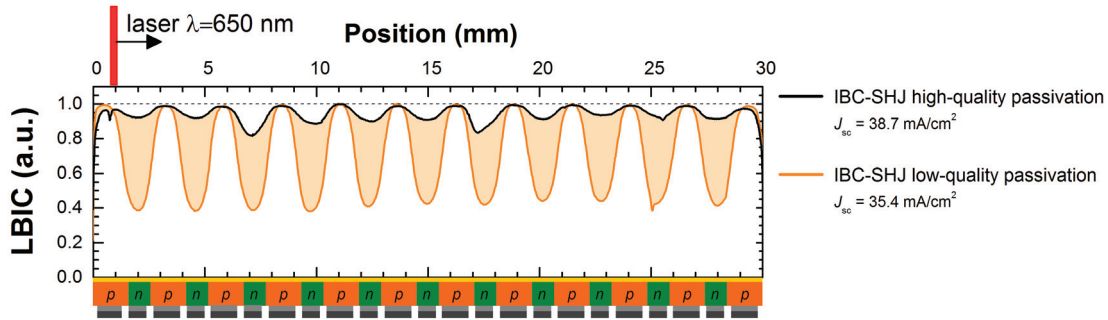
Figure 4.22: 30-mm-long LBIC cross-sectional profiles in the dark of IBC-SHJ devices with high-quality (black line) and low-quality (orange line) passivation. The two LBIC profiles correspond to J_{sc} values of 38.7 mA cm^{-2} and 35.4 mA cm^{-2}, respectively. The filled area between the two LBIC profiles represents the amount of charge carriers lost due to the reduced value of L_h for the low-passivation-quality IBC-SHJ device.

Electrical-shading and back-electrode design

Electrical-shading losses are relevant with respect to the design of the back contacts. Generally speaking, what matters is the distance that holes must diffuse to reach the respective electrode. From this perspective, it is important to have narrow electron-collecting fingers and, simultaneously, to reduce as much as possible the distance between the electron contact and the edge of the hole electrode, i.e. minimizing for instance the portion of the a-Si:H(p) film uncovered by the TCO/metal stack. Here we report two LBIC measurements that are explanatory with respect to the present discussion of electrical-shading losses.

We measured LBIC profiles, in the dark, on two test SHJ solar cells, with FHC and RHC configurations and with a fully metallized back side. For the RHC device, we observe that the LBIC signal suffers a minor loss in intensity when the excitation laser exits the front TCO pad, but then it remains constant. This loss occurs only for the change in the front-side reflection, outside the TCO pad. Conversely, for the FHC solar cell, we observe an exponential decay of the LBIC signal after the excitation source exits the front TCO pad. Explanatory schematics for the observed effects and the LBIC profiles are reported in Fig. 4.23. We remark that in practical devices this effect will be modified by the higher excess minority carrier density present under 1-sun conditions. This observation agrees with the device results discussed in section 4.4.4 and, more specifically, explains the J_{sc} increase observed for the reduced distance between the edges of the TCO/metal electrode and the hole-collecting area. We note that the LBIC signal decay measured on the FHC SHJ device, outside the TCO pad, is perfectly fitted with an exponential curve in the form $I(x) = I_0 e^{-x/L_h}$, with L_h equal to the effective hole diffusion length in the bulk of the c-Si(n) wafer. Thus, we could extract $L_h = 1.8$ mm from which we calculated $\tau_{eff} = 2.8$ ms; this value corresponds to the typical τ_{eff} values measured on our solar cell precursors and can be taken as proof of the connection between recombination and the LBIC signal decay far from the hole contact.

test-FHC solar cell

test-RHC solar cell

a-Si:H(p)   a-Si:H(n)   a-Si:H(i)
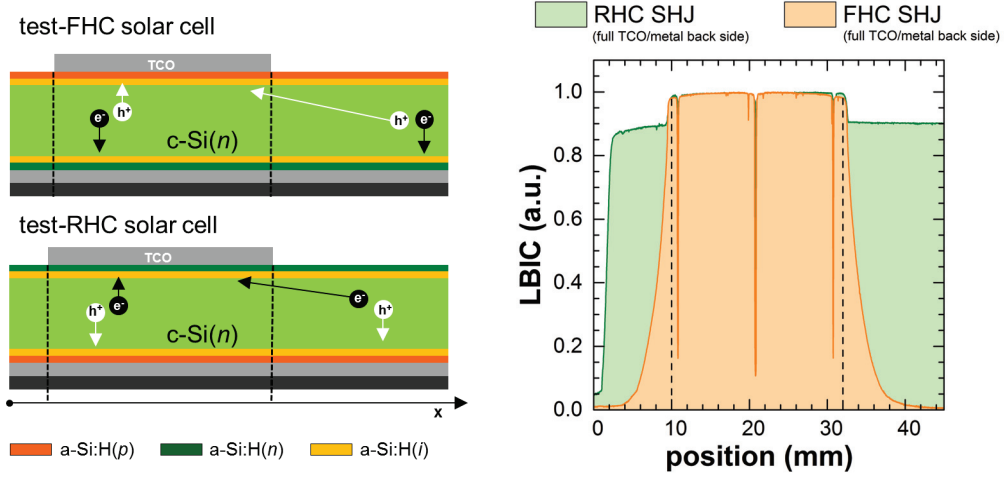
(a) Cross-sectional schematic of n-type FHC and RHC SHJ test solar cells with a fully metallized back side. The path that minority (holes) and majority (electrons) carriers have to travel in order to be collected is also represented (drawings not in scale).

(b) 45-mm-long LBIC cross-sectional profiles of 2×2 cm^2 two-side-contacted n-type FHC and RHC SHJ solar cells. The back side of these test SHJ solar cells is fully covered by a TCO/metal layer stack. For clarity, LBIC profiles are normalized.

Figure 4.23: LBIC profiles in n-type FHC and RHC test SHJ solar cells with fully metallized back side and respective carrier collection paths. The three severe drops in the LBIC signals are caused by the presence of the finger of the front-grid electrode.

4.6.6 Conclusion (III)

In this section, we benchmarked the optics of our non-J_{sc}-optimized back-contacted devices against our reference FHC SHJ device. We found that the J_{sc} gain of about 1 mA cm^{-2} in IBC-SHJ devices is due mainly to the absence of front-grid shadowing. Thus, we analysed the different sources of J_{sc} losses and identified possible routes towards higher J_{sc}. We tackled parasitic absorption and reflection losses at the front side, thinning the a-Si:H(n) layer and implementing a DARC scheme. We found that, without a front a-Si:H(n) layer, our IBC-SHJ device performs better it does with an a-Si:H(n) layer, and has reduced parasitic absorption losses. Combining the DARC scheme with a simple a-Si:H(i) passivating layer at the front of an IBC-SHJ device, we achieved a J_{sc}-optimized solar cell with a J_{sc} of 40.9 mA cm^{-2}, yielding a conversion efficiency of 22 %. In this device we realized a J_{sc} gain of about 1 mA cm^{-2}, compared to our previous IBC-SHJ devices, and of about 2 mA cm^{-2}, compared to our reference FHC SHJ device [Descoeudres 2013].

Further major J_{sc} improvements may be obtained by suppressing electrical-shading losses (J_{medium}), by using highly-transparent passivating layers, such as a-SiO$_x$:H, Al$_2$O$_3$ or high-temperature a-SiN$_x$:H, at the front (J_{short}) and, by reducing infrared light absorption in the back electrode (J_{long}).

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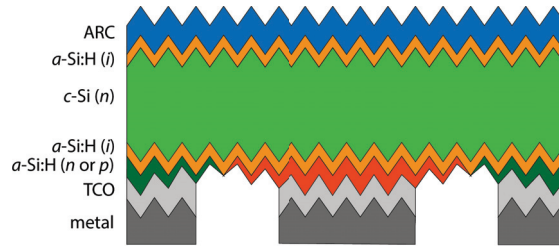
Figure 4.24: Cross-sectional schematic of the improved IBC-SHJ solar cell architecture (**IBC-SHJ Type III**). In the sketch we can notice the absence of the front *n*-type a-Si:H layer, compared to the case of **IBC-SHJ Type II** (see Fig. 4.8).

4.7 Industrially relevant IBC-SHJ solar cells with efficiency >22 %

Bringing together, in the same IBC-SHJ device architecture, the lessons learned in the three main sections of this chapter we fabricated devices with conversion efficiencies higher than 22.0 %. Based on the results of section 4.4, this new device has no gap between the doped a-Si:H layers. Both doped a-Si:H layers are increased in thickness with respect to conventional high-efficiency SHJ devices. In addition, portions of the a-Si:H(p) and a-Si:H(n) layers that are 200 µm long and 100 µm long, respectively, are not covered by the TCO/metal electrodes. A highly doped ZnO:Al film is included in both electron and hole contacts for optimized carrier extraction from the a-Si:H-based collectors (see sections 4.5.3 and 5.3). These a-Si:H-based collectors are purposely designed for improved carrier transport through the heterocontacts (see section 4.5.4). No a-Si:H(n) layer is present at the front side. The resulting IBC-SHJ device architecture is shown in Fig. 4.24.

In Fig. 4.25, we report the I-V characteristic of a solar cell representative of this new class of IBC-SHJ device. The V_{oc} of this device is aligned with the best values presented so far. The J_{sc} benefits from the absence of the a-Si:H(n) layer in the front stack and approaches the value achieved in our highest-J_{sc} device of section 4.6. The *FF* is among the highest presented so far. Such *FF*s, exceeding 75 %, were achieved exclusively combining our best a-Si:H and ZnO:Al films. An analogous result was presented in section 4.5.3, where the device performances were instead compromised by the lower J_{sc} due mainly to the higher parasitic absorption in the front-side stack.

These device results demonstrate the feasibility of IBC-SHJ devices exceeding 22 % conversion efficiencies by means of our original fabrication process. Importantly, the developed IBC-SHJ technology, being photolithography-free and scalable to larger device sizes, is industrially relevant.
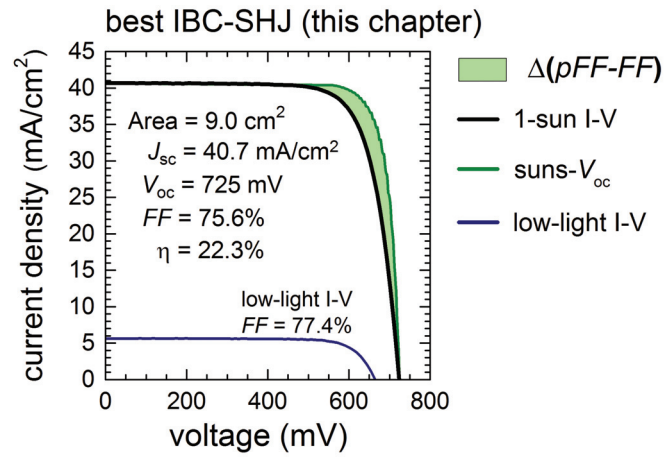
Figure 4.25: Pseudo I-V, 1-sun I-V and low-light I-V characteristics of a fabricated IBC-SHJ device with conversion efficiency exceeding 22 %. This device is representative of the improved class of devices represented in Fig. 4.24, which incorporate all the major improvements presented in this chapter. The light green area indicates losses due to charge-carrier transport.

5 Transparent electrodes in silicon heterojunction solar cells: influence on contact passivation and charge-carrier transport

Abstract

This chapter address the optimization of hole and electron passivating contacts. In experiments, the influence of the transparent conductive oxide (TCO) electrical properties both on contact passivation and charge-carrier transport were investigated. At the hole contact, higher TCO conductivities were found to detrimentally affect the minority carrier lifetime at low excess minority carrier densities, and, consequently, the solar cell operating voltage. Conversely, efficient transverse carrier extraction from electron and hole collectors was shown to require, in the case of aluminium-doped zinc oxide as TCO, high TCO doping. Along similar lines, the use of microcrystalline-based films in carrier-selective passivating contacts is shown to provide improved charge-carrier transport properties, with specific contact resistivity values $\leq 0.02\,\Omega\,\mathrm{cm}^2$. These experiments contribute to define a tentative picture of the silicon heterojunction contacts, which is presented in the conclusive part of the chapter.

Section 5.2 of this chapter is based on a paper published in IEEE Journal of Photovoltaics and reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE [1].

5.1 Introduction and motivation

Charge-carrier collection in silicon heterojunction solar cells occurs via intrinsic/doped a-Si:H layer stacks deposited on the crystalline silicon wafer surfaces. Usually, both the electron- and hole-collecting stacks are externally capped by an *n*-type transparent conductive oxide (TCO), primarily needed for carrier extraction and transport. Importantly, throughout the whole chapter we refer to TCOs meaning standard *n*-type TCO materials.

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[1]The results presented here were obtained with the help of F. Sahli, J.P. Seif, L. Fanni, S.M. de Nicolas Agut, J. Geissbuhler, B. Paviet-Salomon, S. Nicolay, L. Barraud, B. Niesen, S. De Wolf and C. Ballif. Contributions are gratefully acknowledged.

Chapter 5. Transparent electrodes in silicon heterojunction solar cells: influence on contact passivation and charge-carrier transport

Transparent conductive oxides play an important role in silicon heterojunction (SHJ) solar cells. Two obvious tasks that these layers need to fulfill are efficient light coupling into the silicon wafer and conduction of electrical current to the front metal grid [Holman 2013b]. In addition, they also should guarantee efficient transverse carrier extraction from the electron and hole collectors of the device. For such transverse carrier extraction to be efficient, at least two requirements need to be fulfilled. Firstly, the TCOs should yield minimal contact resistivity needed for efficient carrier transport. Secondly, the TCOs (and their deposition methods), should not degrade the surface passivation properties of the underlying layers. The more these two requirements are fulfilled, the higher the "carrier selectivity" of the contact will be, collecting one carrier type while repelling the other. In practice, these two requirements critically depend on the energetic line-up of the TCO with the silicon layers underneath, but so far it remains elusive to what extent these phenomena are interlinked.

In the case of front contacts, or more generally in contacts which are not fully metallized, the need to conduct electrical current laterally to the metal grid dominates and dictates the required TCO film electrical properties. For a fixed TCO thickness, insufficiently-high TCO film conductivities, i.e. carrier densities and/or mobilities, detrimentally impact the device series-resistance, its *FF* and its conversion efficiency. In this case, the optimum TCO electrical properties are easily individuated lowering the film carrier density, thus maximizing its transparency, until *FF* losses starts to occur. Conversely, in fully metallized contacts, the TCO electrical properties are free from this constraint and may be differently optimized to reach best contact "carrier selectivity". Unfortunately, the requirements on TCO properties for efficient carrier transverse extraction are still partially unclear. On the one hand several authors claimed that high TCO bare *work functions* (WF) are required to contact effectively the a-Si:H(p) layer [Centurioni 2003, Bivour 2014a, Bivour 2013, Ritzau 2014], avoiding detrimental "Schottky-contact" effects and carrier transport losses, on the other hand it was observed that to contact both a-Si:H(p) and a-Si:H(n) layers *highly doped TCOs,* i.e. lower TCO bare WFs, are beneficial [Bivour 2014a, Bivour 2014b, Kirner 2015].

Fully metallized contacts are present at the back of conventional two-side-contacted front-hole-collecting (FHC) and rear-hole-collecting (RHC) SHJ devices, and also in IBC-SHJ devices. The optimization of the heterocontact properties in our **IBC-SHJ devices** is the real motivation behind the investigations presented in this chapter. We aim to the identification of the TCO film properties for simultaneous best contact passivation and charge-carrier transport. Thus, to gain better insights on the factors determining the TCO quality as contact layer, we address first the impact of the TCO electrical properties on contact passivation, and then in electron and hole contacts of full-processed IBC-SHJ devices.

We note that the high impact of an excellent surface passivation quality, over the whole excess carrier density range of solar cell operation, was very recently substantiated by Kaneka, Japan, which demonstrated a SHJ device with conversion efficiency and *FF* of 25.1 % and 83.5 %, respectively. This outstanding solar cell is the result of reduced recombination at the a-Si:H/c-Si interface and improved τ_{eff} at mpp [Adachi 2015]. The combined Auger and

radiative recombination limit (for our 3 Ω cm, 250-μm-thick n-type c-Si wafers at 300 K) define a $\tau_{\text{eff}}(\Delta n)$ curve with a maximum theoretical FF of about 88 %. Aiming to best FF values, any possible detrimental effect on τ_{eff}, at low Δn, cannot be neglected and the investigation of the TCO influences on contact passivation gains importance.

Summary

Earlier, it has been demonstrated that the mere presence of a TCO material on top of the hole-collecting a-Si:H(p) film can affect the carrier recombination in the crystalline silicon absorber [Demaurex 2014, Rößler 2013, Favre 2013, Macco 2014]. In section 5.2, we study the dependence of this phenomenon from the TCO conductivity and we present a detailed investigation of the impact on both the electron- and hole-collecting sides, including its consequences for the operating voltages of silicon heterojunction solar cells.

Transverse charge-carrier extraction from hole- and electron-collecting a-Si:H layers, was shown to depend on the TCO film electrical properties [Bivour 2014a, Bivour 2014b, Kirner 2015]. In section 5.3, we present a study on the charge-carrier transport properties of the fully-metallized SHJ contacts of our IBC-SHJ solar cells, considering the impact of the TCO film conductivity.

In section 5.4.1, we extend our analysis of charge-carrier transport in heterocontacts to μc-Si:H-based electron contacts.

Finally, based also on the findings of this chapter, in section 5.4.2, we propose a tentative picture of the hole and electron contacts in high-efficiency SHJ solar cells.

5.2 Transparent electrodes in SHJ solar cells: influence on contact passivation

5.2.1 Introduction

In this section, we aim at identifying the conditions for best contact passivation in SHJ solar cells. By carrier lifetime measurements, we first probe the influence on passivation of the doped a-Si:H film thickness in SHJ charge-carrier collectors, yet uncapped by TCOs. Then, we investigate how the doping of TCO films affects the passivation of underlying a-Si:H layer stacks. We pay specific attention to both electron and hole contacts, defined as a-Si:H(i)/a-Si:H(n) (hereafter abbreviated as "in") and a-Si:H(i)/a-Si:H(p) (hereafter abbreviated as "ip") stacks, respectively, capped by TCOs.

Next, we report on illumination intensity vs open-circuit voltage measurements (i.e. suns-Voc curves [Sinton 2000]) of SHJ devices, featuring TCO films with a variety of electrical properties. The V_{oc} at low illumination intensity (<1 suns) is directly affected by surface passivation. Conversely, tracking the V_{oc} of SHJ devices under very high illumination intensities (>10 suns) has

been argued to give insight in the carrier extraction properties of the involved contacts, especially at the a-Si:H(p)/TCO interface [Bivour 2012, Bivour 2014a]. Here, to identify possible correlations between the TCO impact on surface passivation and on carrier extraction, we study V_{oc} at high and low illumination intensities, respectively. The presented methodology can easily be extended to other solar cell concepts employing passivating contacts [Battaglia 2014b, Battaglia 2014a, Bullock 2014, Feldmann 2014a, Feldmann 2014b, Geissbuhler 2015b].

To conclude, we analyse the implications of our findings on the design of high-efficiency SHJ solar cells and discuss possible routes towards optimum contact passivation. [2]

5.2.2   Experimental details

Crystalline Si wafers (4-in float-zone, n-type, nominal resistivity of $3\,\Omega\,cm$) were textured and cleaned by a wet-chemical process. Subsequently they were dipped in a diluted hydrofluoric solution to strip off the chemical oxide. Thin blanket intrinsic/doped a-Si:H layer stacks were deposited on both wafer surfaces in a PECVD reactor, at $200\,°C$. More details on our a-Si:H stacks for hole and electron collection can be found elsewhere [Descoeudres 2011]. The thickness of the standard a-Si:H layers, measured by spectroscopic ellipsometry on a planar glass substrate, are typically in the range of $10\,nm$. Indium tin oxide (ITO) films were sputtered from an In_2O_3-SnO_2 target [Buchanan 1980], nominally at room temperature. Boron-doped zinc oxide (ZnO:B) layers were deposited by low-pressure chemical vapor deposition (LPCVD) [Wenas 1991] at a temperature of around $175\,°C$. Further details on the used deposition system and related methodology can be found elsewhere [Faÿ 2005]. The wafer edges were protected during TCO depositions and remained uncoated. During each TCO deposition, we co-deposited films on a bare glass witness sample in order to measure TCO properties (thickness, resistivity, carrier density, carrier mobility). The film thickness was assessed by a stylus profilometer, its resistivity by four-point–probe measurements and the carrier density and mobility by Hall effect measurements. TCO layer thicknesses, measured on glass, range between $180\,nm$ to $250\,nm$, which are typical TCO thicknesses used in our SHJ device back contacts [Holman 2013b, Tomasi 2014a]. In the case of the least doped ZnO:B film, the carrier density and mobility values, extracted from Hall measurements, are not considered reliable, due to the excessively high film resistivity.

The effective minority carrier lifetime of the passivated c-Si wafers, τ_{eff}, was assessed in the excess minority charge-carrier density (Δn) range $10^{14}\,cm^{-3}$ to $10^{16}\,cm^{-3}$, by transient photoconductance decay measurements [Sinton 1996]. To cover the entire device-relevant Δn range, each sample was measured in two distinct ranges (high>$10^{15}\,cm^{-3}$ and low<$10^{15}\,cm^{-3}$). Subsequently, the two datasets were stitched together to build the final $\tau_{eff}(\Delta n)$ curve. Suns-V_{oc} measurements were acquired with a standard suns-V_{oc} set-up [Sinton 2000]. Similarly as for τ_{eff} measurements, suns-V_{oc} measurements were taken at high (5–200 suns) and low (<5

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[2]This work was done in collaboration with F. Sahli. N. Holm is acknowledged for help in PECVD layer depositions.

suns) illumination intensities and then merged in final high-low suns-V_{oc} curves.

5.2.3 Effects on effective minority carrier lifetime

Photoconductance decay lifetime measurements yield τ_{eff} vs Δn curves. The characteristic shape of these data reveals direct information about the nature of the sample's surface passivation (chemical or field effect). In the case of a-Si:H(i) passivating films, the passivation is mainly chemical, resulting in low a-Si:H/c-Si interface defect densities [De Wolf 2012a]. Despite this, for the case of a-Si:H-based charge-carrier collectors important differences in τ_{eff} values at Δn values lower than $\sim 10^{15}$ cm^{-3} can be observed and are associated to field-effect passivation (or the lack thereof) [Leendertz 2011, Olibet 2007].

To quantitatively assess the impact of such Δn dependencies on device performance, we chose as metrics the implied fill factor (implied-FF) [Aberle 1993] and the implied open-circuit voltage (implied-V_{oc}) [Sinton 1996]. Throughout this entire work, we explicitly use the prefix "implied-" for all quantities derived from carrier lifetime data. In the following, we stepwise build up our hole and electron contacts and systematically verify the impact of each layer on their passivation properties.

Impact of doped a-Si:H layers [3]

To simplify the interpretation of our results, we study n-type c-Si wafers featuring either symmetric in or ip stacks (hereafter referred to as "in/in samples" and "ip/ip samples", respectively). The thickness of the doped a-Si:H layers was varied between one third to twice their standard thickness, as typically used in our devices [Descoeudres 2013] (see also section 5.2.2). Fig. 5.1 gives measured $\tau_{eff}(\Delta n)$ data for both types of charge-carrier collectors under study, not yet capped by any TCO. In either case we witness lower τ_{eff} for thinner doped a-Si:H layers. This loss seems particularly important at low Δn which especially impacts implied-FF values. Implied-V_{oc} values increase slightly with increasing doped a-Si:H layer thicknesses; the overall variation is <10 mV and <20 mV in the case of the a-Si:H(p) and a-Si:H(n) layer thickness series, respectively. Implied-FF values vary more significantly. However, one can obtain values ≥84 % for sufficiently thick a-Si:H(p) layers and ≥86 % for sufficiently thick a-Si:H(n) layers (see Fig. 5.2). Such thickness dependency may be the outcome of two competing mechanisms. On the one hand, the presence of the defective (doped) a-Si:H overlayers may lead to recombination of carriers tunneling through the thin a-Si:H(i) layers [De Wolf 2006]. On the other hand, their recombination is conditioned by surface field effects, as those discussed in more details below, which gain in importance with doped layer thickness.

Remarkably, very similar implied-FF trends were observed also by external corona charging of test structures featuring a simple a-Si:H(i)/n-type c-Si wafer structure [Reusch 2013]. To enable

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[3]For this experiment the a-Si:H layer stacks were deposited in a different PECVD reactor, compared to all other a-Si:H layers reported in section 5.2.

corona charging, these samples were capped by a 1-μm-thick silicon oxide dielectric film. The extremely good correspondence of the results achieved in these two different experiments highlights the prime importance of field effects on the overall surface passivation associated to state-of-the-art a-Si:H-based carrier collectors. From this perspective, the layer-thickness dependencies observed in Fig. 5.1 (a) and (b), and in Fig. 5.2 are driven mainly by the WF of the different n- and p-type doped a-Si:H layer, yielding field effects inside the wafer, also needed for (selective) charge collection. For the electron collector, the a-Si:H(n) layer introduces a downward band bending inside the wafer (electron accumulation, hole depletion). Conversely, for the hole collector, the presence of the a-Si:H(p) layer results in a strong upwards band bending inside the wafer that can result in surface inversion (hole accumulation, electron depletion) [Maslova 2010]. In our experiment, different asymptotic implied-FF values ($\sim 86\,\%$ and $\sim 84\,\%$ for increasingly thick a-Si:H(n) and a-Si:H(p) films, respectively) are attributed to these two opposite situations. Intriguingly, these asymptotic values also match very closely those determined in the corona charging experiment by Reusch *et al.* [Reusch 2013]. They can be explained by larger interface defect capture cross-sections for electrons vs holes, similarly to the case of thermal silicon oxide passivated surfaces [Glunz 1999]. Noteworthy, our typical a-Si:H(i) film provides better surface passivation, and better implied-FF values, without than with the thin doped a-Si:H overlayers. This latter observation can be put in relation with the amphoteric nature of Si dangling bonds at the interface a-Si:H(i)/c-Si, which determines a carrier recombination minimum in case of comparable free hole and electron densities, i.e. low band bending at c-Si surface [Olibet 2007]. The variations observed for the $\tau_{\mathrm{eff}}(\Delta n)$ data, for changing doped layer thicknesses, are most likely a distinctive sign of efficient hole and electron collectors. They demonstrate the capability of the doped a-Si:H layers to induce a certain electrical field, in the proximity of the c-Si wafer surface, despite the presence of the a-Si:H(i) passivating film.

Impact of transparent conductive oxides

The next step in contact fabrication consists in the deposition of a TCO on the doped a-Si:H films. Earlier, it was already established that deposition of TCOs on *ip* stacks (i.e. hole collectors) can result in additional Δn-dependencies of the wafer surface passivation [Rößler 2013, Favre 2013, Demaurex 2014, Macco 2014], leading to a reduction in τ_{eff} values at low Δn values ($\Delta n<10^{15}\,\mathrm{cm}^{-3}$). This was reported for a variety of TCOs, including aluminum doped zinc oxide (ZnO:Al) [Rößler 2013, Demaurex 2014, Macco 2014] and ITO films [Favre 2013, Demaurex 2014]. Numerical simulations suggested that the τ_{eff} variation at low Δn is caused by the presumed existence of an ultrathin highly defective (recombination-active) layer in-between the a-Si:H(p) layer and ITO [Favre 2013]. However, although some TCO deposition methods can cause damage to underlying films [Demaurex 2012], the described τ_{eff} variations were also observed using ultra-soft deposition techniques such as atomic layer deposition [Demaurex 2014, Macco 2014], and vanished after TCO removal via chemical etching [Rößler 2013, Macco 2014]. Therefore, the most accepted physical interpretation associates this phenomenon rather to the WF of the bare TCO film, being lower than the one of the
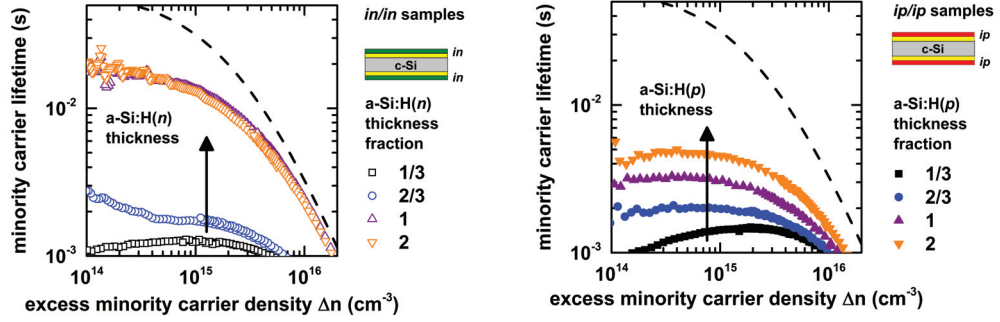
(a) Measurements of $\tau_{\text{eff}}(\Delta n)$ on n-type c-Si absorbers, featuring a symmetric electron collector (*in/in* samples), of which the a-Si:H(n) layer thickness was varied from one third to twice its standard thickness. The combined Auger and radiative limit is indicated by the dashed line [Richter 2012]

(b) Measurements of $\tau_{\text{eff}}(\Delta n)$ on n-type c-Si absorbers, featuring a symmetric hole collector (*ip/ip* samples), of which the a-Si:H(p) layer thickness was varied from one third to twice its standard thickness. The combined Auger and radiative limit is indicated by the dashed line [Richter 2012]

Figure 5.1: Effects on $\tau_{\text{eff}}(\Delta n)$ of different a-Si:H doped film thicknesses. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

a-Si:H(p) layer. This energetic mismatch may deteriorate the field effect of the *ip* stack, reducing the band bending—and thus hole accumulation— at the n-type c-Si wafer surface. In support of this, the presence of a ZnO:Al layer capping an *ip* layer stack was observed, by surface photovoltage measurements, to result in band bending modifications at the n-type c-Si wafer surface [Rößler 2013]. For a schematic representation of the TCO-induced effects on c-Si band bending, at the hole contact, the reader can refer to [Demaurex 2014] or to our sketch in Fig. 5.15 (a). According to this interpretation, it is reasonable to expect variations in τ_{eff}, at low Δn, with changing TCO electrical properties such as the TCO carrier density and WF. To clarify further the implications of the TCO layer on the passivation properties of the substrate underneath, we now present a more detailed study, starting with ITO, being one of the most commonly used TCO material in high-efficiency SHJ devices [De Wolf 2012b].

Sputtered indium tin oxide

In this study we again fabricated symmetric *in/in* and *ip/ip* samples, this time using a-Si:H doped layers with device-relevant thicknesses but adding ITO films with a variety of electrical properties to both wafer surfaces. We then track the effect of these different films on the $\tau_{\text{eff}}(\Delta n)$ data. It is well known that oxygen vacancies in ITO dictate material carrier density and mobility [Choi 1995]. Hence, by varying solely the oxygen partial pressure during ITO deposition, we achieved ITO film carrier densities in the range of 10^{19}–10^{20} cm^{-3}, yielding resistivities comprised between 10^{-2} and 10^{-4} Ω cm (see Table 5.1). The recorded mobility increase, in ITO films with higher carrier densities, is most likely related to grain barrier-limited carrier transport [Ellmer 2008]. This range of materials also includes the ITO films we use in our state-of-the-art n-type FHC SHJ devices.
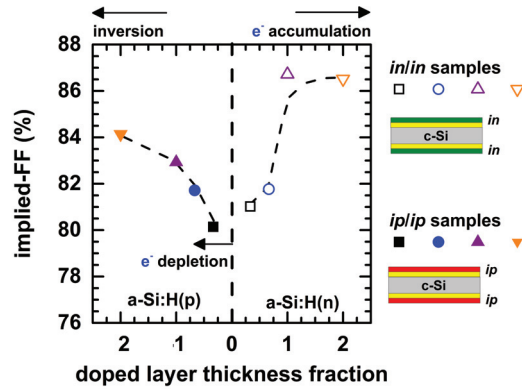
Figure 5.2: Implied-*FF* values extracted from $\tau_{\text{eff}}(\Delta n)$ curves measured on *n*-type c-Si absorbers featuring symmetric electron (*in/in* samples) and hole (*ip/ip* samples) collectors, for varying doped a-Si:H layer thickness fractions (see Fig. 5.1). Regions corresponding to electron (e⁻) accumulation, depletion and inversion conditions at the c-Si wafer surface are also indicated. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

As already reported earlier [Demaurex 2014, Demaurex 2012], following ITO sputtering, an overall degradation of the measured $\tau_{\text{eff}}(\Delta n)$ curve is seen. Succeeding ITO deposition, the samples were annealed for 20 minutes at 200 °C. This treatment recovers passivation, but not for low Δn values, which is linked again to field effects further discussed below. Fig. 5.3 shows the $\tau_{\text{eff}}(\Delta n)$ data, after deposition of solely the a-Si:H layers and after ITO sputtering followed by post-deposition annealing.

In the case of the *in/in* samples, we observed only a slight increase in τ_{eff}, which is comparable for all the ITO films tested here, at least for Δn down to ~$5 \cdot 10^{14}$ cm⁻³. Implied-V_{oc} values are all comprised in the range 732–735 mV and implied-*FF* in the range 83.2–83.8%.

In contrast, for the *ip/ip* samples, the measured $\tau_{\text{eff}}(\Delta n)$ data shows a stronger decrease for increasing ITO conductivity and carrier density. Implied-V_{oc} values, extracted from the $\tau_{\text{eff}}(\Delta n)$ curves reported in Fig. 5.3, range from 736 mV (layer ITO_1) to 726 mV (layer ITO_3), whereas implied-*FF* values decrease from 83.8 % (layer ITO_1) to 81.8 % (layer ITO_3). Noteworthy, the relative variation in measured implied-*FF* values is higher than that in implied-V_{oc} values. Considering the data shown in Fig. 5.3, converted to a suns-implied-V_{oc} plot [Sinton 1996] given in Fig. 5.4, we can directly visualize the expected impact of the observed phenomena also on the V_{oc} of SHJ devices (see section 5.2.4).

Low-pressure chemical vapor deposition boron-doped zinc oxide

To further investigate the nature of the effects observed for the sputtered ITO films, we now extend our analysis to ZnO:B layers deposited via LPCVD, an ultra-soft deposition technique that preserves pristine a-Si:H films. ZnO:B deposited via LPCVD is widely used in thin-film solar cells [Faÿ 2005], and has found applications also in SHJ photovoltaic devices
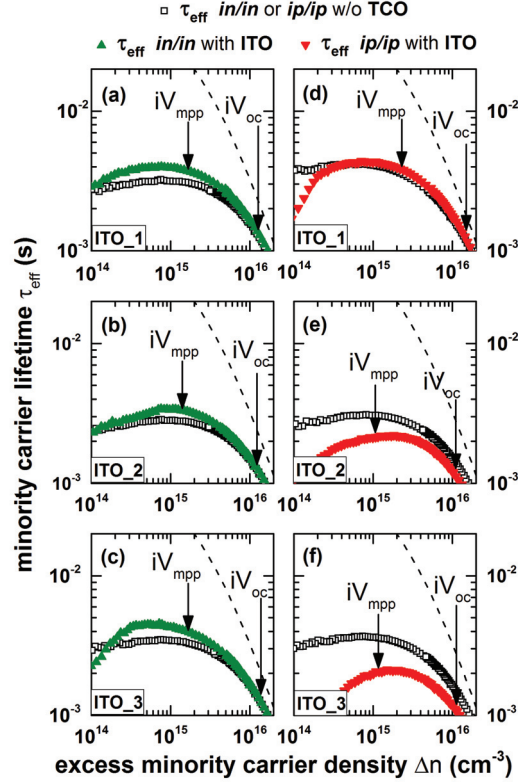
Figure 5.3: Measurements of $\tau_{\mathrm{eff}}(\Delta n)$ on *n*-type c-Si absorbers featuring either a symmetrically co-deposited (a)–(c) electron collector (*in/in* samples) or (d)–(f) hole collector (*ip/ip* samples), before and after deposition, on both sides, of ITO films of different resistivity and subsequent annealing at 200 °C (see Table 5.1). Δn corresponding to implied-V_{oc} and implied maximum power-point voltage (here referred as iV$_{\mathrm{oc}}$ and iV$_{\mathrm{mpp}}$, respectively) are identified by arrows for the $\tau_{\mathrm{eff}}(\Delta n)$ curves measured after deposition of the ITO layers. The combined Auger and radiative limit is indicated in each graph, for comparison, by a dashed line [Richter 2012]. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

[Favier 2011, Choong 2010]. Using these films has two advantages: (1) a wide range of carrier densities is accessible, aiding the identification of physical trends and (2) sputter-damage is completely avoided, enabling unambiguous proof of the "electrical field" origin of the observed phenomena.

In this experiment, we co-deposited ZnO:B layers with four different resistivities (see Table 5.2) on both surfaces of *in/in* and *ip/ip* samples. The electrical properties of ZnO:B are tuned by varying the flow ratio of the precursor-dopant gas (diborane, B_2H_6) and the zinc-precursor gas [diethyl zinc, $(C_2H_5)_2Zn$)]. As for ITO, also in ZnO:B films higher carrier mobilities correspond to higher carrier densities [Steinhauser 2007]. We measured $\tau_{\mathrm{eff}}(\Delta n)$ curves before and after deposition of the different ZnO:B layers. For the *in/in* samples we observed a slight increase in τ_{eff} for all samples after the deposition of the ZnO:B layers, similar to what we observed with ITO films (Fig. 5.3 (a), (b) and (c)). The strongest increase is obtained for the sample
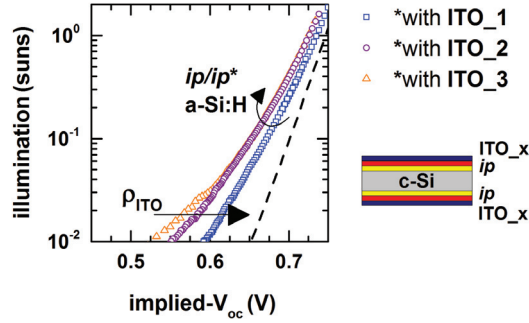
Figure 5.4: Implied-V_{oc} *vs* illumination intensity values of the photoconductance decay lifetime measurements which $\tau_{eff}(\Delta n)$ data are given in Fig. 5.3 (d), (e) and (f). The combined Auger and radiative limit is indicated, for comparison, by the dashed line [Richter 2012]. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

Table 5.1: Electrical parameters of ITO layers

Layer	Carrier density (cm^{-3})	Hall Mobility (cm^{2}V^{-1}s^{-1})	ρ_{ITO} (Ω cm)
ITO_1	$4.0 \cdot 10^{19}$	14.2	$1.1 \cdot 10^{-2}$
ITO_2	$1.0 \cdot 10^{20}$	18.0	$3.4 \cdot 10^{-3}$
ITO_3	$5.9 \cdot 10^{20}$	28.8	$3.7 \cdot 10^{-4}$

The values are measured after postdeposition annealing for 20 min at 200 °C (coherently with reported $\tau_{eff}(\Delta n)$ measurements).

featuring the most conductive ZnO:B layer (see Fig. 5.5 (left)). Conversely, for the *ip/ip* samples, we observed a stronger decrease in τ_{eff} at low Δn values for samples featuring increasingly conductive ZnO:B films (see Fig. 5.5 (right)), confirming the trend observed for sputtered ITO films. In addition to these effects, during ZnO:B deposition, our samples also undergo *in-situ* annealing at a temperature below 200 °C for about 5 minutes. This annealing could be sufficient to explain a slight improvement in passivation [De Wolf 2008], as witnessed for the lowly doped ZnO:B layers in both the *in/in* sample series (layer ZnO:B_1, ZnO:B_2 and ZnO:B_3 in Fig. 5.5 (left)) and the *ip/ip* sample series (layer ZnO:B_1 and ZnO:B_2 in Fig. 5.5 (right)).

Compared to the case of *ip/ip* samples with sputtered ITO films, implied-V_{oc} values do not reveal any obvious trend here (see Fig. 5.6 (a)). The implied-*FF* values vary significantly for samples exhibiting the most conductive ZnO:B film that yields the highest and the lowest implied-*FF* values for the *in/in* and *ip/ip* passivated sample, respectively (see Fig. 5.6 (b)).

Summary on carrier lifetime effects

Therefore, our tentative conclusions are the following: doped a-Si:H overlayers have a clear and strong impact on the surface passivation, especially at low Δn. This results from the

Table 5.2: Electrical parameters of ZnO:B layers

Layer	Carrier density (cm^{-3})	Hall Mobility $(\text{cm}^2\text{V}^{-1}\text{s}^{-1})$	$\rho_{\textbf{ZnO:B}}$ $(\Omega\,\text{cm})$
ZnO:B_1	-	-	105
ZnO:B_2	$1.0\cdot 10^{19}$	0.3	2.5
ZnO:B_3	$6.1\cdot 10^{19}$	3.9	$2.6\cdot 10^{-2}$
ZnO:B_4	$1.4\cdot 10^{20}$	13.0	$3.5\cdot 10^{-3}$

band bending they induce at the c-Si wafer surface (i.e. surface field effect or lack thereof). The presence of TCOs on such overlayers can further affect the low-Δn passivation, again modifying the band bending in the c-Si wafer. Only from a passivation perspective, the presence of a highly doped (n-type) TCO can be beneficial when capping *in* stacks, but is detrimental for *ip* stacks. These two opposite observations are coherent with a reduced and augmented, TCO/a-Si:H(n/p) WF mismatch, respectively [Centurioni 2003], as result of TCO doping and bare TCO WF variations. Visual representations of these effects are given in Fig. 5.15. We note that these phenomena may directly impact the fill factor's upper limits, for the different SHJ device architectures (see section 5.2.5).

In the following section we now evaluate the described effects and their impact on the voltage of our devices and its illumination dependency.

5.2.4 Effects on operating voltage

High-low suns-V_{oc} curves of SHJ devices

The V_{oc} of a solar cell, obtained from the 1-sun current-voltage characteristics, is a first indication of the recombination losses occurring in the device. However, this parameter also contains important information about the quality of contacts and carrier collectors [Pysch 2011]. Our aim here is to verify to what extent the TCO-induced effects on $\tau_{\text{eff}}(\Delta n)$, described in section 5.2.3, also hold relevance for the V_{oc} and especially for its illumination (i.e. Δn) dependency.

As a starting point for our discussion we plot in Fig. 5.7 (a) a typical *high-low* suns-V_{oc} curve measured for one of our FHC SHJ devices (conversion efficiency >20 % and V_{oc}>720 mV). In Fig. 5.7 (b), for the same typical suns-V_{oc} curve the local ideality factor n was also derived, defined as $n = q/kT(d(ln(I))/dV_oc)^{(-1)}$, where k is the Boltzmann's constant, T the absolute temperature, q the elementary charge and I the illumination intensity. In the same graphs, we also show the upper limit of implied-V_{oc}, and the relative n, for our c-Si substrates (see dashed lines in Fig. 5.7). This implied-V_{oc}-limit is dictated exclusively by the c-Si wafer properties (thickness and doping) and the intrinsic recombination processes in the wafer (Auger and radiative, described in Ref. [Richter 2012]). For the precise conversion from Δn-dependent lifetime to suns-implied-V_{oc} data, we followed the procedure outlined in [Sinton 1996].
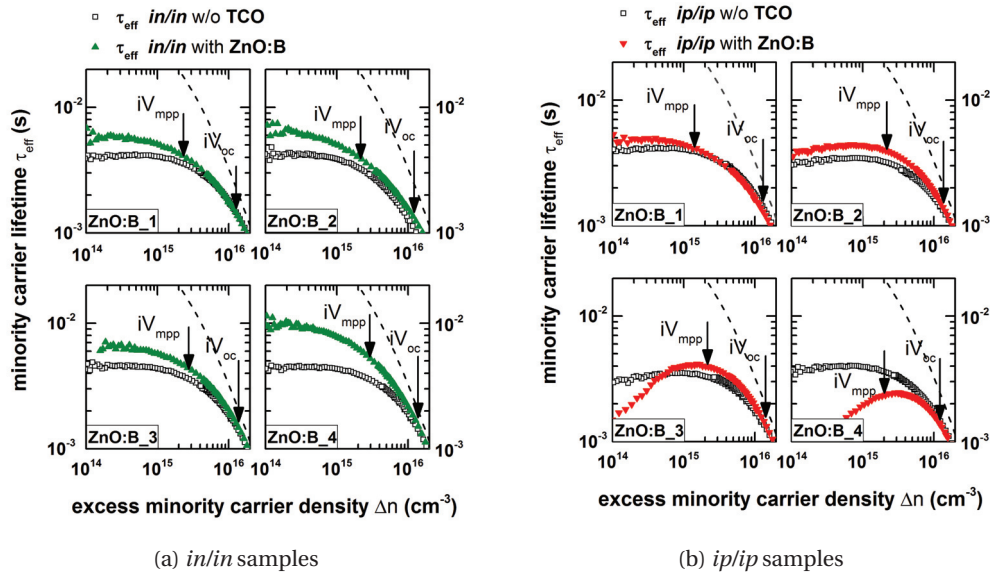
(a) *in/in* samples

(b) *ip/ip* samples

Figure 5.5: Measurements of $\tau_{\text{eff}}(\Delta n)$ on *n*-type c-Si absorbers featuring either a symmetrically co-deposited electron collector (*in/in* samples) or hole collector (*ip/ip* samples), before and after deposition, on both sides, of ZnO:B films. In the bottom left corner of each graph the type of ZnO:B layer to which the data refer is identified (for the layer electrical properties see Table 5.2). Δn corresponding to implied-V_{oc} and implied maximum power-point voltage (here referred as iV_{oc} and iV_{mpp}, respectively) are identified by arrows for the $\tau_{\text{eff}}(\Delta n)$ curves measured after deposition of the ZnO:B layers. The combined Auger and radiative limit is indicated in each graph, for comparison, by a dashed line [Richter 2012]. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

Earlier, the *high*-illumination suns-V_{oc} data was argued to be a useful diagnostic tool to characterize back-contacts in diffused homojunction c-Si devices [Glunz 2007]. Later on, as already mentioned in section 5.2.1, the same approach was also applied for the characterization of the a-Si:H(*p*)/TCO interface in SHJ devices [Bivour 2012, Bivour 2014a]. For such samples, a lowering of the measured V_{oc} at high illumination intensities was sometimes observed. This evidence supports the belief that the WF of the *n*-type TCO, being lower than the one of a-Si:H(*p*), may result rather in a Schottky than an ohmic contact, causing a V_{oc} drop and resistive losses under solar cell operation conditions [Centurioni 2003, Bivour 2013]. The value of *n* at 100 suns (n_{100}) was proposed as indicator for the strength of this effect [Bivour 2014a].

The *low*-illumination suns-V_{oc} data instead give direct information about the performance of the device under the excess minority carrier density levels occurring during actual operation. From the V_{oc} data in the illumination range ~0.04–1 suns, the so-called pseudo-*FF* can be extracted [Sinton 2000], which represents the upper *FF* limit imposed by carrier recombination processes only (assuming thus zero resistive losses in the device). Higher *n* at low illumination imply lower pseudo-*FF*s. Importantly, if the TCO-related effects acting on the illumination dependency of the implied-V_{oc} (Fig. 5.4) equally affect also the V_{oc}, the calculated pseudo-*FF*
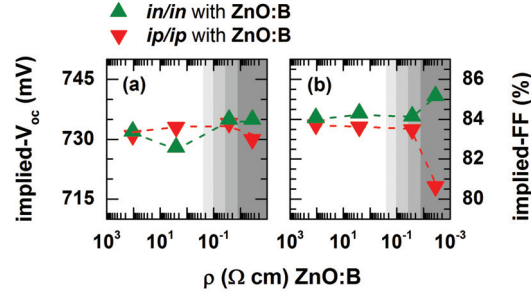
Figure 5.6: Implied-V_{oc} and implied-FF values extracted from the $\tau_{eff}(\Delta n)$ curves given in Fig. 5.5 (left and right panel). The grey background indicates the range of TCO resistivities more relevant respect to applications in SHJ devices. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

value would be consequently affected.

Comparing the illumination-dependent V_{oc} (from suns-V_{oc} measurements) in our FHC SHJ device to the theoretical implied-V_{oc}-limit we observe the following:

1. A moderate deviation of the *high*-illumination V_{oc}, resulting in $0.5 < n_{100} < 2/3$ (see Fig. 5.7 (b)). This value is slightly lower than the one of the implied-V_{oc}-limit but is still far above zero, indicating *high*-illumination V_{oc} "pinning" rather than "bending", using the terminology of Ref. [Gunawan 2014].

2. V_{oc} values closely approaching the limit in the illumination range 1–10 suns, indicating a high level of surface passivation.

3. Increasing deviation of the measured V_{oc} for lower illumination (<1 suns). This deviation accounts mainly for suboptimal field effect passivation provided by a-Si:H-based hole and electron contacts.

Impact of indium tin oxide electrical properties

Following the description of suns-V_{oc} data of typical SHJ devices, we now discuss the impact of varying ITO electrical properties at the front of such solar cells, on such curves. The test structures are fabricated on *n*-type c-Si wafers featuring full-area *ip* and *in* stacks at front and back side, respectively. The back contact is completed by a full-area ITO/metal stack, as in our FHC SHJ devices, whereas at the front we deposited 1-cm^2 ITO pads connected to a small silver dot to allow for a good electrical contact. The properties of the ITO films used at the front are identical to those given in Table 5.1.

The *high-low* suns-V_{oc} curves measured on these samples are plotted in Fig. 5.8. Focusing on the low-illumination data, a weaker V_{oc} decrease is observed for the ITO films with higher

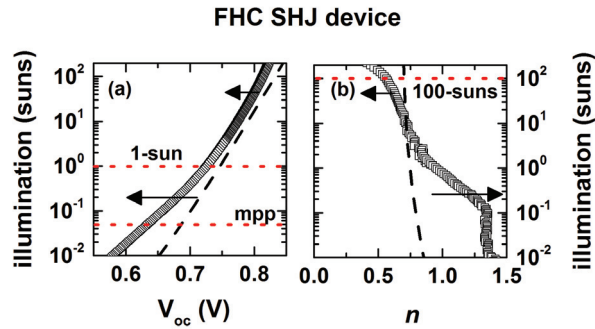Figure 5.7: Typical *high-low* suns-V_{oc} curve (a) measured on one of our FHC SHJ devices and (b) the respective local ideality factor *n*. For comparison the combined Auger and radiative implied-V_{oc}-limit (for our $3\,\Omega$ cm, 250-μm-thick *n*-typec-Si wafers at 300 K) is indicated by the dashed lines [Richter 2012]. The deviations of the measured V_{oc} from this limit, at high and low illuminations, are highlighted by arrows. The illumination levels corresponding to 1-sun and maximum power point (mpp) conditions, and to 100-suns conditions, are denoted by horizontal dotted lines in panel (a) and (b), respectively. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

resistivity and lower carrier density. Here, the overall influence of varying the TCO properties is moderate. The change in ITO-induced band bending at the c-Si surface results in suns-V_{oc} curves differing only at low illumination. In this regard, the a-Si:H(*p*) layer reveals itself as crucial in dampening the ITO influence on surface field effects The trend observed for the *high-low* suns-V_{oc} curves is consistent with the suns-implied-V_{oc} plot of Fig. 5.4, where the data were extracted directly from the $\tau_{eff}(\Delta n)$ curves. This result confirms that the TCO-induced change in τ_{eff} at low Δn can indeed affect the operating voltage of our devices at low illuminations. As such, it proves that the carrier recombination effects studied here are relevant towards pseudo-*FF* values, in addition to implied-*FF* values (as already extensively shown in section 5.2.3), and can impact high-efficiency SHJ devices.

For these samples, in Fig. 5.8, the absence of variations in the high-illumination suns-V_{oc} data is also remarkable. The perfect superposition of all the curves shown here, and the coincidence of their n_{100} values, indicates that—within the explored carrier density range—the ITO properties do not impact those of the presumed "Schottky-contact" [Centurioni 2003, Bivour 2013].

5.2.5   Outlook on transparent electrodes for best-passivated high-efficiency SHJ solar cells

As discussed elsewhere [Holman 2013b], the electrical and optical properties of optimized front and back TCO layers for high-efficiency SHJ devices differ significantly. For instance, in our FHC SHJ devices the front ITO layers have typically a resistivity in the order of $\sim 10^{-4}\,\Omega$ cm and a carrier density in the range of $2\cdot 10^{20}$ cm^{-3} to $3\cdot 10^{20}$ cm^{-3}. In contrast, at the back, ITO
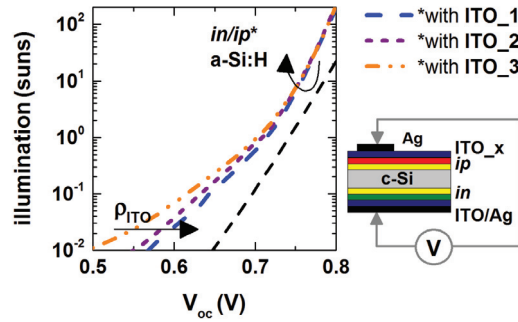
Figure 5.8: Suns-V_{oc} measurements of 1-cm^2 test devices featuring "a-Si:H(i)/a-Si:H(p)/ITO/metal" and "a-Si:H(i)/a-Si:H(n)/ITO/metal" as front and back contacts, respectively (*in/ip* a-Si:H samples). The ITO films used in the front contact are layer ITO$_1$, ITO$_2$ and ITO$_3$ of Table 5.1. Reproduced with permission from [Tomasi 2016b]. Copyright © 2016, IEEE.

films have usually a slightly higher resistivity in the range of $10^{-3}\,\Omega\,\text{cm}$ to $10^{-2}\,\Omega\,\text{cm}$ and a carrier density in the range of $1\cdot10^{19}\,\text{cm}^{-3}$ to $9\cdot10^{19}\,\text{cm}^{-3}$. Higher resistivities can be tolerated at the back thanks to the absence of lateral transport requirements in the TCO, when coated by a metallic layer. This allows the use of films with lower carrier densities, resulting in more transparent layers and improved short-circuit current values [Holman 2013b].

In this context, based on the experimental results discussed above, we concluded that from a surface passivation perspective, the presence of highly doped TCOs is not detrimental if contacting *in* stacks (i.e. electron collectors), whereas this may be when contacting *ip* stacks (i.e. hole collectors). Therefore, it would be preferable to avoid contacting the *ip* stack by a highly doped standard TCO at the front. This requirement is fulfilled by RHC SHJ devices. In this case, the front TCO is in contact with the *in* stack. In addition, without any optical penalty, the back a-Si:H(p) layer could be thickened, thereby improving the screening of the c-Si wafer against the TCO. Notably, this architecture, exploiting better the substrate conductivity, relaxes the requirement for the front TCO lateral conductivity and a highly conductive TCO is no longer required [Bivour 2014c].

Finally, in all SHJ device architectures electrical screening of the c-Si wafer surfaces could be further improved by implementing p-type hydrogenated microcrystalline silicon layers (μc-Si:H), exploiting their much better dopability compared to a-Si:H [Hiroshi 1984]. Along similar lines, an improved a-Si:H(i) passivating layer, reducing the density of available defect states at the c-Si wafer surface, would also diminish the detrimental impact that field effects–such as those induced by TCOs–can have on surface passivation [Leendertz 2011].

5.2.6 Conclusion

In this section we demonstrated how the electrical properties of TCO layers can affect the surface passivation of SHJ contacts. A shift in the bare TCO WF, as result of changing TCO

doping, affects the doped a-Si:H/TCO interfacial WF and the corresponding band bending in c-Si. In the case of the hole contact, higher TCO doping (lower bare TCO WF) tends to diminish the interfacial WF, opposing the field generated by the a-Si:H(p) layer at the c-Si surface. Conversely, at the electron contact a diminished interfacial WF reinforces the field effect generated by the a-Si:H(n) layer at the c-Si surface. These variations of field-effect passivation are detectable in $\tau_{\text{eff}}(\Delta n)$ curves, at low Δn. Next, we showed that the effects observed, for the hole contact, in $\tau_{\text{eff}}(\Delta n)$ measurements at low Δn fully correspond to those observed when measuring the V_{oc} at low illumination intensities. Based on our observations, we concluded that from a surface passivation perspective highly doped TCOs should be avoided to contact hole collectors in n-type SHJ devices. This would lead to the best contact passivation and to the highest device FF's upper limits, which are imposed by carrier recombination. As front TCO layers in FHC SHJ devices are constrained by lateral conductivity requirements, our findings suggest increased design freedom and efficiency benefits for RHC and back-contacted SHJ device architectures.

5.3 Transparent electrodes in SHJ solar cells: influence on charge-carrier transport

5.3.1 Introduction

Regarding the ideal properties of TCO as contact layer for high-efficiency SHJ devices, the effects on carrier recombination, examined in the previous section, represent only half of the wider and more complex problem of passivating-contact optimization. As argued in section 5.1, the latter must address the minimization of charge-carrier recombination, but also of transport-activated losses (while preserving simultaneously also broadband transparency), as both contribute to determine the final solar cell FF.

In this section we address the effects of TCO film properties on transport-activated losses in hole and electron contacts. As case study we consider our IBC-SHJ devices, which are extremely well-suited for this kind of investigation. The TCOs films, in both hole and electron contacts, are fully covered by a thick metal layer and do not contribute to lateral carrier transport in our devices. Thus, from the electrical perspective, the sole function of the TCO films in the IBC-SHJ heterocontacts is the transverse extraction of carriers from the hole and electron-collecting a-Si:H doped layers to the thick metal electrodes. In addition, as extensively discussed in section 4.5, IBC-SHJ devices are intrinsically highly-sensitive to variations in heterocontact transport properties. To better delineate the heterocontact characteristics we used transfer-length-method (TLM) contact pad arrays. Possible limitations of this approach are discussed in the appendix C.

5.3.2 Experimental details

The IBC-SHJ solar cells presented below integrates the best hole-collecting electrode of section 4.4, the best a-Si:H materials of section 4.5.4 and no a-Si:H(n) layer in the front-side stack. The device structure is that one depicted in the schematic of Fig. 4.24. To allow the integration of differently-doped ZnO:Al layers in hole and electron contacts, the fabrication process described in section 3.4 was modified as follows. The TCO films are deposited in two distinct steps on the hole- and electron-collecting comb, respectively, through *in-situ* shadow masks having a geometry identical to the doped a-Si:H layers. So doing, they coat the entire cell area without leaving any uncovered gap in between the combs. Subsequently, the thick metal layer is deposited on the full back-side surface and hot melt inkjet printing and wet-chemical etching are performed as usual. In this last step both the metal and the TCO are etched and the conventional TCO/metal electrode geometry is eventually defined.

TLM contact pad arrays are fabricated on the same textured n-type c-Si wafers as used in our IBC-SHJ devices. These samples feature one wafer side passivated by a thin a-Si:H(i) layer and, at the opposite side, a full-area electron contact with the following structure "c-Si(n)/a-Si:H(i)/a-Si:H(n)/TCO/metal", which mimics the one used in our IBC-SHJ devices. Either by hot melt inkjet printing and wet-chemical etching, or *in-situ* shadow masking during sputtering, the TCO/metal layer is then structured to form the TLM contact pad array. Eventually, to avoid lateral current flows in the c-Si substrate, the wafer is laser cut in stripes of width w_{TLM}, with the same size of the TCO/metal contact pads (see cross-sectional and top-view of the TLM sample in Fig. 5.9). We chose $w_{TLM} = 0.6$ cm and a contact pad width w_{pad} of 2 mm. The pad spacing values (d) are 0.05, 0.1, 0.2, 0.4 and 0.8 cm, respectively. Before the electrical characterization the samples are annealed for 20 minutes at 200 °C. The I-V characteristics are thus measured in dark and at a temperature of 25 °C.

During each TCO deposition we co-deposited films on a bare glass witness sample in order to measure TCO properties. Aluminium-doped zinc oxide (ZnO:Al) films were sputtered at a temperature of 60 °C and variations in film conductivity were achieved varying the oxygen partial pressure during deposition.

5.3.3 Effects of ZnO:Al film electrical properties in IBC-SHJ devices

To asses the impact of different ZnO:Al film electrical properties, in hole and electron contacts of IBC-SHJ devices, we design the experiment summarized in Fig. 5.10. Reference electrical properties, for the ZnO:Al films, are shown in Table 5.3.[4] In overall we fabricated 4 devices with the film ZnO:Al_2 at the hole contact but varying ZnO:Al at the electron contact, and 3 devices with the film ZnO:Al_2 at the electron contact but varying ZnO:Al at the hole contact. An IBC-SHJ device using the highly doped film ZnO:Al_4, at both contacts, was also fabricated. This solar cell, even if it uses the same TCO film in both contacts, underwent the TCO *in-situ*

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[4]ZnO:Al films were developed at the PV-Center of CSEM. The results presented here were obtained with the help of G. Christmann and S. Nicolay.

(a) Cross-sectional schematic of our TLM structure.   (b) Top-view schematic of our TLM structure.
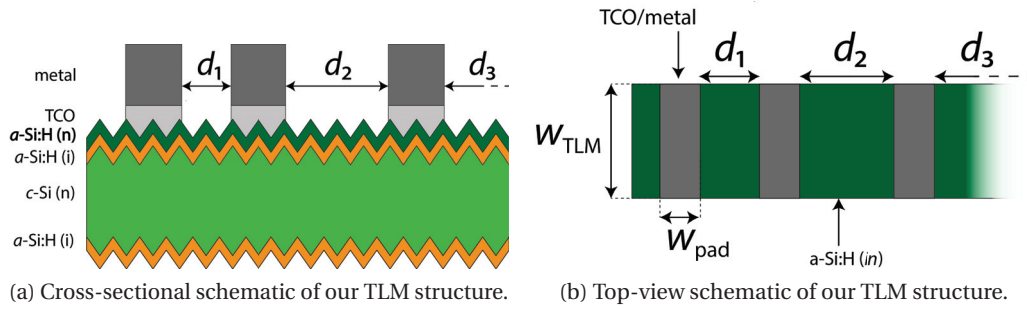
Figure 5.9: Cross-sectional (left) and top-view (right) schematics of the TLM structure used for passivating-contact characterization.

Figure 5.10: Structure of the design of experiment done to probe the ZnO:Al film of Table 5.3 in the contacts of our IBC-SHJ devices. We fabricated two series of devices varying the TCO properties in the hole (series h_*) or in the electron (series e_*) contact, respectively. In each series, we named the solar cell with the number of ZnO:Al film present in the contact with varying TCO.

masking steps. It serves as reference for the *non-standard* process flow used in this experiment. The exact electrical parameters of the ZnO:Al films of each device were also measured and do not differ significantly from those of Table 5.3.

Up to now ZnO:Al is the best performing TCO material in our IBC-SHJ devices (see section 4.5.3). The purpose of this experiment is twofold; (1) on the one hand it verifies if the independent optimization of ZnO:Al in hole and electron contacts can bring further improvements to our best devices, and (2) on the other hand it investigates the requirements, in terms of TCO contact film properties, for optimized carrier transport at the SHJ heterocontacts.

IBC-SHJ solar cell results

The measured electrical parameters, summarized in Table 5.4, show clear trends. Both in the hole, or electron contact, higher ZnO:Al doping leads to better solar cell performances. The 1-sun I-V characteristic of most devices, as can be seen in Fig. 5.11, present a characteristic shape, so-called "S-shape", which compromises the solar cell performances determining poor FFs. Strongly S-shaped I-V curves may also show low J_{sc} and, to a less extent, low V_{oc}

Table 5.3: Reference electrical parameters for the ZnO:Al layers used in the experiment of Fig. 5.10.

Layer	Carrier density (cm^{-3})	Hall Mobility (cm^{2}V^{-1}s^{-1})	$\rho_{\text{ZnO:Al}}$ (Ω cm)	Thickness (nm)
ZnO:Al_1	$3.8 \cdot 10^{19}$	1.6	0.1	139
ZnO:Al_2	$1.4 \cdot 10^{20}$	5.1	$8.6 \cdot 10^{-3}$	150
ZnO:Al_3	$1.8 \cdot 10^{20}$	7.5	$4.8 \cdot 10^{-3}$	144
ZnO:Al_4	$3.5 \cdot 10^{20}$	14.0	$1.3 \cdot 10^{-3}$	151

The values are measured after postdeposition annealing for 20 min at 200 °C.

values. The strength of such effect, decreasing for higher ZnO:Al doping, determines the trends observed in the electrical parameters. We note that the TCO doping, at the hole contact, seems more critical in this respect. The device with by far the highest *FF* and V_{oc} is h_4, the sole using the film ZnO:Al_4 in the hole contact. Its I-V characteristic is the only one where, the presence of a S-shape behaviour, can be totally excluded.

S-shaped I-V curves are associated to problems in charge-carrier transport. In the field of silicon heterojunction they were shown as result of various problems. For instance, at the hole contact, they were shown to relate with the valence band alignment at the a-Si:H(*i*)/ and a-SiO$_x$:H/c-Si(*n*) interfaces [Mews 2015] but also with the band alignment at the TCO/a-Si:H(*p*) interface [Kirner 2015, Kanevce 2009]. In our experiment, the link with carrier transport is evident in the measured low-illumination I-V characteristics (see again Fig. 5.11); at lower current densities they recover progressively the shape of a well-behaved I-V characteristic. Coherently, for all devices, the *pFF* measured in suns-V_{oc} measurements are above 80 %. Our results demonstrate the importance of the TCO film as contact layer, and that S-shaped I-V characteristics can be originated, simply by the TCO film properties, both at the hole or electron contact.

Importantly, the device eh_4 performs similarly to the devices presented in chapter 4. This validates the results of the experiment and exclude important artefacts due to the *non-standard* process flow.

Probing the I-V characteristic of the electron contact in TLM contact pad arrays

To unambiguously link our results to the impact of the ZnO:Al films on the heterocontact transport properties, we integrated the electron contacts of the experiment in TLM contact pad arrays. The I-V characteristics measured in between the TLM contact pads, for different ZnO:Al films, are compared in Fig. 5.12. With ZnO:Al_1 and ZnO:Al_2 we measured the characteristic I-V curve generated by two opposing diodes. Differently, for ZnO:Al_3 we observed linear I-V characteristics, up to currents of about 100 mA, on which we performed the TLM analysis. The extracted $(\rho_c)_{\text{n}}$ is equal to 0.238 Ω cm^2. However, this value should be handled with the cares detailed in the appendix C.

Table 5.4: Electrical parameters of IBC-SHJ devices using different ZnO:Al films of Table 5.3 in electron and hole contacts. The experiment is summarized in Fig. 5.10.

Parameter	h_1	h_2	h_4	e_1	e_2	e_3	e_4	eh_4
V_{oc} (V)	0.693	0.710	0.723	0.706	0.715	0.709	0.691	0.719
J_{sc} (mA/cm^2)	28.4	28.2	41.1	33.9	40.3	40.9	40.3	40.7
η (%)	2.8	3.2	19.2	3.5	6.8	12.1	14.9	21.6
FF (%)	14.1	16.1	64.7	14.6	23.6	41.6	53.3	73.8
R_{series}^{N} ($\Omega\,cm^2$)	>10	>10	3.3	>10	>10	8.8	5.5	1.3
pFF (%)	82.6	82.8	81.2	80.9	83.0	80.9	78.1	80.1
Low Light I-V FF (%)	32.5	39.8	73.4	35.1	53.0	61.1	62.7	73.4

The I-V characteristics measured in these TLM structures demonstrate that the electron contact, for low TCO doping, develops a rectifying characteristic. This rectifying characteristic can be directly linked with the outbreak of S-shape effects in the 1-sun I-V characteristic of SHJ solar cells (see the series of IBC-SHJ devices e_*).

5.3.4   Transport and recombination at the SHJ hole contact

As shortly mentioned in section 5.1, the presumed TCO requirements for optimal transverse carrier extraction and contact passivation are in some aspects controversial. Our results confirm previous observations that *highly doped TCO* are beneficial to carrier transport to contact both a-Si:H(*n*) and a-Si:H(*p*) layers [Bivour 2014a, Bivour 2014b, Kirner 2015]. However, for the hole contact this does not fit the requirement of a *higher WF*, to mitigate possible detrimental "Schottky-contact" effects, as argued in other earlier works [Centurioni 2003, Bivour 2014a, Bivour 2013, Ritzau 2014]. This apparent contradiction evokes additional determining factors for the quality of carrier transport across the hole contact, which occurs via thermionic emission, across the c-Si/a-Si:H(*i*) interface, and band-to-band tunneling, at the a-Si:H(*p*)/TCO interface [Kanevce 2009]. Looking into the requirements for efficient band-to-band tunneling, the *FF* loss observed with insufficiently doped TCOs was recently explained–treating the TCO-contact film as a semiconductor material–with inefficient carrier tunneling through a wider space charge region at the a-Si:H(*p*)/TCO interface [Kirner 2015] (see also the discussion in section 5.4.2 and Fig. 5.15 (a)). For this, it can be understood that high TCO conductivities are needed for low contact resistivities. In contrast, as argued in section 5.2, from surface passivation perspective, it would be rather beneficial to have a lowly doped TCO at the surface with the *p*-type a-Si:H film, in case a thin *p*-type film is used. These seemingly competing requirements may have both implications towards the *FF* of high-efficiency SHJ devices. At the hole contact, differently than for the electron contact, optimum TCO film properties would then result from a trade-off of contact passivation and charge-carrier transport.
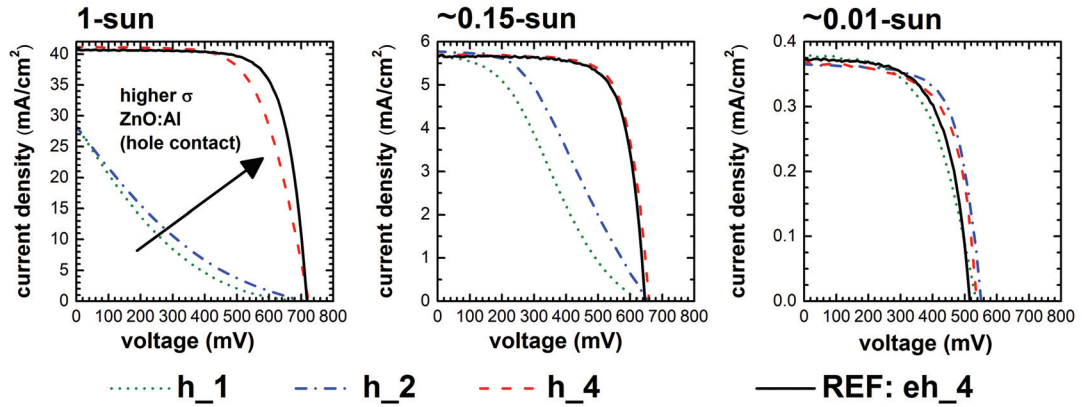
(a) Series of IBC-SHJ devices with different ZnO:Al films in the hole contact.
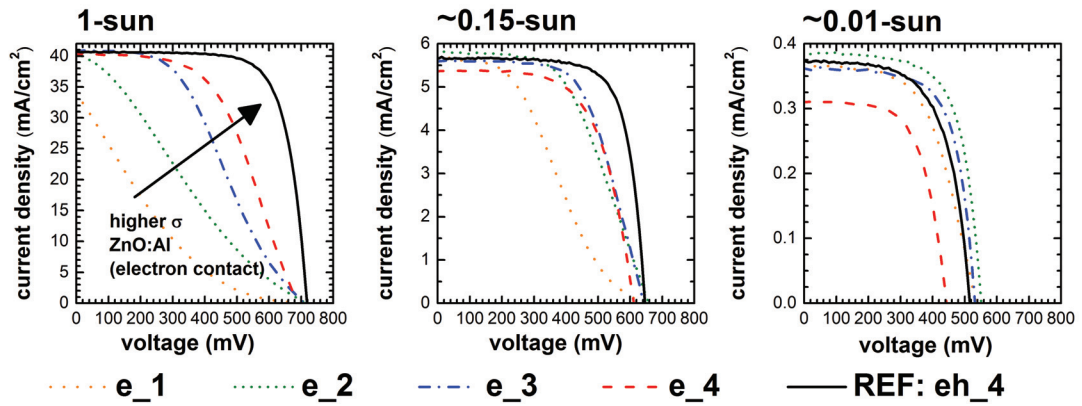
(b) Series of IBC-SHJ devices with different ZnO:Al films in the electron contact.

Figure 5.11: Illumination dependent I-V characteristics of IBC-SHJ devices using different combinations of the ZnO:Al films of Table 5.3 in electron and hole contacts. The experiment is summarized in Fig. 5.10 and the electrical parameters extracted from these curves are recapitulated in Table 5.4.

5.3.5 Conclusion

Based on the results of section 5.3.3, we conclude that for ZnO:Al as TCO film, at both electron and hole contacts, high TCO doping are beneficial to charge-carrier transport. As a consequence, in our IBC-SHJ technology, optimized charge-carrier transport is achieved without the need to differentiate the TCO film properties for hole and electron contacts. This simplify importantly the fabrication process of our solar cells. However, it should be kept in mind that this finding may be not of general validity for any TCO material.

measured I-V characteristics (a-Si:H(*n*)/ZnO:Al)
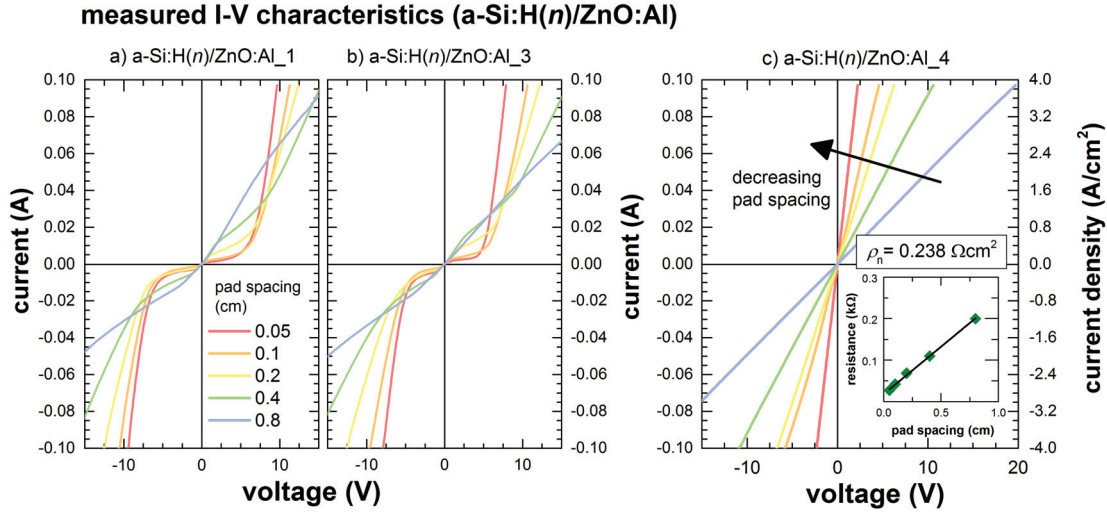
Figure 5.12: Measured I-V characteristics in TLM contact pad arrays integrating different electron contacts. The graph (a), (b) and (c) refer to electron contacts including the films ZnO:Al_1, ZnO:Al_3 and ZnO:Al_4, respectively. These electron contacts are those used in the devices e_1, e_3 and e_4 . The current densities values, calculated for the transfer length value of $L_t = 418\,\mu$m, are shown on the right axis of graph (c).

5.4 Outlook on the SHJ contacts

5.4.1 An improved electron contact based on doped μc-Si:H

Here, we apply TLM measurements to characterize μc-Si:H-based electron contacts, in which the a-Si:H(*n*) film is replaced by a μc-Si:H(*n*) film. These μc-Si:H layers were deposited by PECVD, at higher powers and pressures than conventional a-Si:H layers. Further details on their fabrication can be found in[Seif 2015, Seif 2016b, Nogay 2016]. In the TLM measurements, the I-V characteristics are linear over a 200 mA current range ($> 20\,\mathrm{A\,cm^{-2}}$) and the extracted values of R_c are much lower, compared to conventional a-Si:H-based electron contacts. Typically, in our μc-Si:H-based electron contacts, we measured $(\rho_c)_n$ values in the range of $0.01\,\Omega\,\mathrm{cm^2}$ to $0.02\,\Omega\,\mathrm{cm^2}$. This is one order of magnitude lower than in our best a-Si:H-based electron contact, showing $(\rho_c)_n \approx 0.2\,\Omega\,\mathrm{cm^2}$. In Fig. 5.13 we show a TLM measurement for a μc-Si:H(*n*)- based electron contact. This difference in $(\rho_c)_n$ confirms some earlier results [Lee 2014, Tatsuro 2015]. In the work of [Kanicki 1988], $(\rho_c)_n$ was shown to strongly depend on the *n*-type layer bulk conductivity. Our μc-Si:H(*n*) layers, being more conductive than our a-Si:H layers, are in line with these earlier findings.

We note that the conductance of the μc-Si:H(*n*) layer is still sufficiently low to avoid alterations of the current flow in the TLM structures. The R_{sheet} value of about $130\,\Omega/\square$, extracted from the TLM measurements, indicates that the μc-Si:H(*n*) film does not contribute significantly to the lateral transport of the carriers and assures that the current flow crosses twice the entire electron contact. It should be kept in mind that the low $(\rho_c)_n$ of μc-Si:H-based electron

measured I-V characteristics (μc-Si:H(*n*)/TCO)
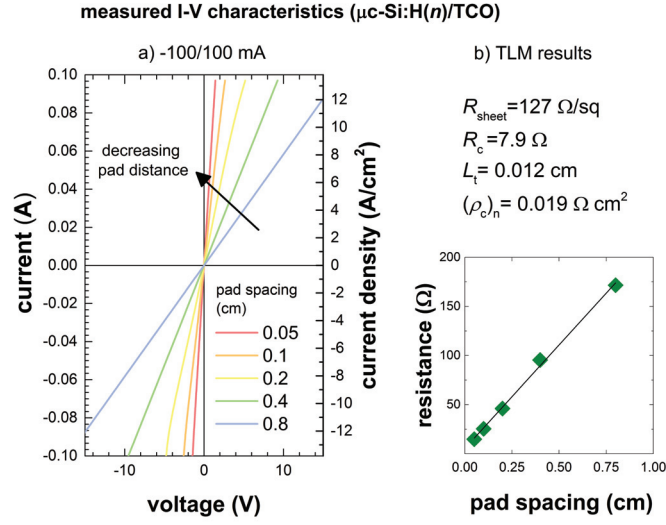
Figure 5.13: Measured I-V characteristics, over an extended current range, in a TLM contact pad array integrating a μc-Si:H-based electron contact. The parameter resulting from the TLM anaylsis are shown in the inset (b).

contacts may be also artefact by "*hidden*" non-linear effects in the measured I-V characteristics (see the discussion in the appendix C). Nevertheless, this can hardly justify the differences observed in the TLM measurements for the a-Si:H- and μc-Si:H-based contacts. The very low values measured for $(\rho_c)_n$ prove optimal charge-carrier transport in the μc-Si:H-based electron contacts.

A further demonstration of the improved charge-carrier transport properties of μc-Si:H-based heterocontacts are the beneficial effects observed with their integration in devices. Improved solar cell performance were achieved both in two-side-contacted SHJ architectures [Seif 2015, Seif 2016b, Nogay 2016] and in the *tunnel*-IBC-SHJ architecture of chapter 6.

A possible interpretation for the improved carrier transport in μc-Si:H-based electron contacts, is that, for high doping of the *n*-type layer, a narrower barrier width is formed at the interface μc-Si:H(*n*)/ TCO. Therefore, tunnelling transport mechanisms are facilitated and the overall charge-carrier transport properties of the contact are improved. This effect is discussed further in section 5.4.2 and is schematically represented in Fig. 5.14 (b).

5.4.2   A tentative picture for the heterocontacts

In metal-semiconductor or semiconductor-semiconductor contacts, the WFs of the two distinct materials are often the starting point to determine the energy-band lineup. However, when considering absolute WF values in practical contacting problems extreme care should be taken. When bringing two material in intimate contact, indeed the resulting interfacial WF is mostly determined by Fermi-level pinning effects [Robertson 2013, Schroder 2006]. These ef-

fects, dependent on energy and density of interface electronic states, may be in turn influenced by the employed material deposition techniques or surface preparation methods. So, in most practical metal-semiconductor contacts, Fermi-level pinning effects lead to the formation of a depletion contact, with a barrier height (ϕ_B) largely independent from the metal WF. However, the width of this barrier is reduced by higher material doping; this explains why, to have well-optimized Ohmic contacts, highly doped semiconductors are needed [Schroder 2006]. In most common n-type and p-type semiconductors, such as Ge, Si, GaAs and other III-V materials, it results $\phi_B \approx 2/3E_g$ and $\phi_B \approx 1/3E_g$, respectively, where E_g is the energy band gap of the material [Mead 1969]. Based on earlier findings [Ritzau 2014, Wronski 1977], analogous Fermi-level pinning effects are expected also at the interface of a doped a-Si:H thin-film with the sputtered-TCO. Hence, we draw our schematic of the SHJ contacts under this assumption. This is also in line with our observation of improved transport with highly doped TCO films (see discussion in section 5.3.4), and with highly doped μc-Si:H thin-films (see discussion in section 5.4.1). With these arguments and the help of AFORS-HET [Froitzheim 2003] simulations, we drew a tentative picture for hole and electron SHJ contacts. We remark that these illustrations should be intended as a base for further discussions rather than a complete representation of the exact band structure and working principles of the heterocontacts.

In the SHJ hole contact (Fig. 5.14 (a) and Fig. 5.15 (a)), the presence of the a-Si:H(p) film leads to an upward band bending at the c-Si(n) wafer surface. This is due to the higher WF of the a-Si:H(p) layer, compared to the c-Si(n) wafer. Oppositely, in the SHJ electron contact (Fig. 5.14 (b) and Fig. 5.15 (b)), the presence of the a-Si:H(n) film, with WF lower than the c-Si(n) wafer, leads to a downward band bending at the c-Si(n) wafer surface.

At the a-Si:H(p)/ and a-Si:H(n)/TCO interfaces, due to Fermi-level pinning, we have the formation of a depletion contact with barrier height (ϕ_B) independent from the WF of the TCO overlayers. The a-Si:H(p)/TCO interface is a recombination interface and transport occurs via hole-electron recombination processes, which are impeded by the depletion of holes. However, with higher a-Si:H(p) doping levels, the depletion width at the interface is reduced and holes can approach more closely the TCO, which helps hole-electron recombination processes. This provides improved charge-carrier transport properties for higher a-Si:H(p) doping and also in μc-Si:H-based hole contacts. Similarly, at the a-Si:H(n)/TCO interface, we have a barrier for electron transport which becomes narrower for higher a-Si:H(n) doping, or with μc-Si:H(n) layers. We remark that narrower barrier widths, improve charge-carrier transport promoting tunnelling transport mechanisms, with respect to thermionic emission. These effects may explain our findings of section 5.4.1.

The given interpretation finds confirmation also in temperature-dependent contact-resistance measurements. Charge-carrier transport dominated by tunneling processes, rather than thermionic emission, is largely independent from the temperature. Oppositely, thermionic emission processes are promoted by higher temperatures [Schroder 2006]. For a-Si:H-based hole and electron contacts we measured decreasing $(\rho_c)_n$ values for higher temperature, whereas for μc-Si:H(n)-based electron contacts, instead, we measured almost unchanged

(a) Sketch of the SHJ hole contact (blue solid line) and effect of the higher a-Si:H(*p*) doping (green solid line).

(b) Sketch of the SHJ electron contact (blue solid line) and effect of the higher a-Si:H(*n*) doping (green solid line).

Figure 5.14: Artistic representations of the energetic band line-up in a SHJ hole (a) and electron (b) contact. The effect of an higher a-Si:H(*p*) and a-Si:H(*n*) doping is highlighted, in the respective image, with coloured lines and arrows.

$(\rho_c)_n$ values up to 80 °C [Nogay 2016].

According to [Kirner 2015], analogous effects are produced, in highly doped TCO, at the interface with the a-Si:H(*p*) layer (see Fig. 5.15 (a)). This improves the charge-carrier transport properties of hole contacts using highly doped TCO. Our findings of section 5.3.3, are in line with this interpretation. For higher TCO doping in the SHJ electron contact we can imagine the situation represented in Fig. 5.15 (b). In this case it is not clear if transport properties would be modified, or not, by the different TCO dopings. Further investigations are needed to match this picture with the improved transport, for high TCO doping, observed in experiments.

Finally, with higher TCO doping, i.e. lower bare TCO WF, and for the hole contact, we expect a reduction in the band bending at the c-Si surface. This explains the degradation in contact passivation, for highly doped TCO films, observed in section 5.2. Oppositely, we expect an increase in the band bending at the c-Si surface for the electron contact, which may lead to a reinforcement of the surface passivation. This effects are represented in Fig. 5.15 (a) and (b) and can be easily reproduced in AFORS-HET, omitting Fermi-level pinning effects. Further investigations are needed to verify if these are still realistic representation in the hypothesis of fully Fermi-level pinned TCO/a-Si:H(*p*) and a-Si:H(*n*) interfaces.

(a) Sketch of the SHJ hole contact (blue solid line) and effect of the higher TCO doping (red solid line).

(b) Sketch of the SHJ electron contact (blue solid line) and effect of the higher TCO doping (red solid line).
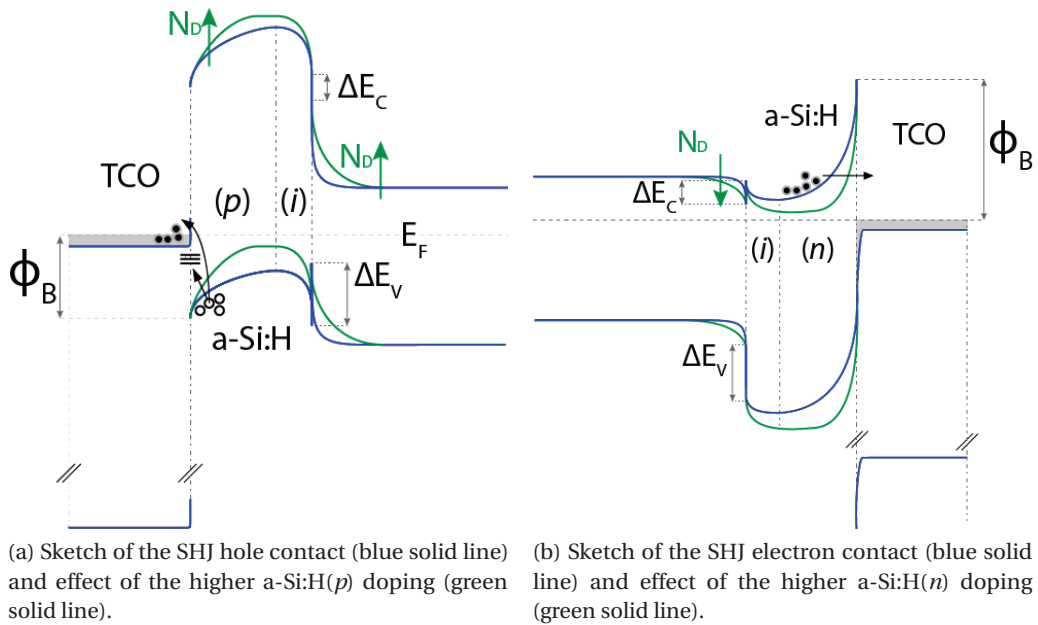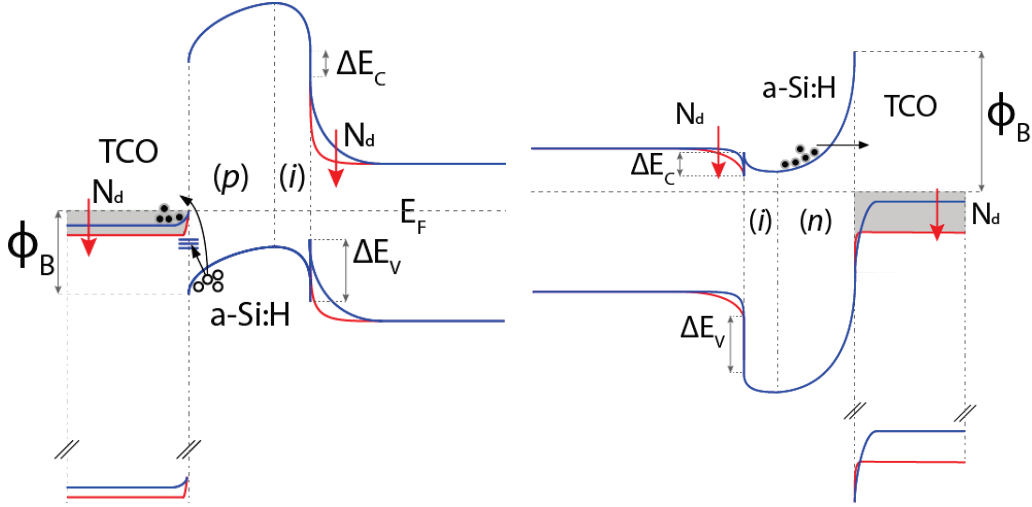
Figure 5.15: Artistic representations of the energetic band line-up in a SHJ hole (a) and electron (b) contact. The effect of an higher TCO doping is highlighted with coloured lines and arrows.

6 22.9% back-contacted silicon heterojunction solar cell enabled by an interband silicon tunnel junction

Abstract

Back-contacted solar cells, thanks to the lack of any front electrode, are fundamentally superior to conventional two-side-contacted devices. However, the technological sophistication needed to realize both contact polarities at one device side may limit their appeal and restrict their spreading in industry. In this chapter we demonstrate the feasibility of a novel and disruptive interdigitated back-contacted device concept exploiting an interband silicon tunnel junction. Our approach employs the silicon heterojunction technology and has the beauty of dramatically simplifying the back-contacted architecture and its fabrication process, solving simultaneously specific weaknesses of back-contacted silicon heterojunction devices. Applying the proposed device concept we fabricated a 9-cm^2 back-contacted SHJ device with a conversion efficiency of 22.9 % and a open-circuit voltage of 728 mV.

The contents of this chapter are still unpublished, but a manuscript is in preparation. A patent application protecting certain features of the device concept presented in this chapter has been filed in November 2015 [Paviet-Salomon 2015b]. Contributions are acknowledged in the text as footnotes.

6.1 Introduction and motivation

In the recent years, single-junction silicon wafer-based solar cells with conversion efficiencies overcoming the "psychological" barrier of 25 % have been achieved using few different distinctive technologies [Masuko 2014, Nakamura 2014, Smith 2014, Glunz 2015, Adachi 2015]. Notably, within these top-efficiency devices, the highest conversion efficiency of 25.6 % was reached by means of a back-contacted architecture [Masuko 2014]. This arguably reflects the superiority of this class of devices which active area is not reduced by front electrode shadowing and allows ultimate J_{sc} values.

To fully realize the efficiency potential of back-contacted architectures, hole and electron

contacts must be fabricated avoiding any direct contact between the metal electrode and the absorber material. The fulfilment of this condition is a prerequisite to allow ultimate minority carrier effective lifetimes over the entire excess minority carrier density range of solar cell operation. This makes possible top-V_{oc} and *FF* values, but requires the use of a passivating contact technology. A possible choice for this is to use silicon heterojunction contacts. The potential of this approach was already conclusively demonstrated in IBC-SHJ devices with world-record conversion efficiencies [Masuko 2014, Nakamura 2014]. However, with regard to industrialization, the key challenge remains the reduction of the complexity associated with their fabrication.

In the previous chapters we addressed this problem by developing an original photolithography-free technology, based on *in-situ* shadow masking and inkjet printing. In this way we pushed conversion efficiencies up to about 22% [Tomasi 2014a, Tomasi 2014b, Paviet-Salomon 2015a, Tomasi 2015a]. Here, we present an alternative strongly simplified and innovative device concept, hereafter referred as *tunnel*-IBC-SHJ solar cell, employing an interband silicon tunnel (IST) junction [Esaki 1958]. Importantly, with such disruptive approach we could already achieve conversion efficiencies close to 23 %. Our proposal brings along a viable solution to the general problem of simplification of the back-contact fabrication. In addition, as discussed more extensively ahead in the chapter, it presents also strong assets with regard to the general problem of carrier transport optimization in passivating contacts of back-contacted devices (section 4.5), and to specific limitations of *in-situ* shadow mask-based patterning technologies (section 4.4).

6.2   Experimental

In this chapter, two-side-contacted front-hole-collecting (FHC) SHJ solar cells and *tunnel*-IBC-SHJ devices were fabricated on *n*-type, 250-μm-thick 4-inch float-zone c-Si wafers with nominal resistivity of 3 Ω cm. The device active area is either 4-cm^2 or 9-cm^2, excluding the bus bar region, in FHC and *tunnel*-IBC-SHJ solar cells, respectively. Wafers were textured in a potassium hydroxide solution and cleaned by a wet-chemical process. Following a short dip in a diluted hydrofluoric solution, a thin a-Si:H(*i*) film was deposited on both entire wafer surfaces as passivating layer. In some cases, specified in the text, also an a-Si:H(*n*) film was deposited at the front side, as in the architectures IBC-SHJ Type I and II. Doped a-Si:H and hydrogenated microcrystalline silicon (μc-Si:H) materials were both used in our hole and electron collecting contacts. All a-Si:H and μc-Si:H films were deposited by PECVD; further details on our a-Si:H and μc-Si:H layers and their fabrication can be found in [Descoeudres 2011] and in [Seif 2015, Seif 2016b, Nogay 2016], respectively.

In the case of FHC devices, full-area doped layers were deposited on the front and back wafer surfaces, respectively. The back electron contact was thus completed by a full-area TCO/metal stack whereas the front hole contact was finished by a TCO film and a screen-printed Ag grid. The front TCO layer was patterned, by deposition through a shadow mask, to define three

(a) Cross-sectional schematic of the best-performing IBC-SHJ solar cell architecture of chapter 4 (**IBC-SHJ Type III**).

(b) Cross-sectional schematic of the ***tunnel*-IBC-SHJ** solar cell architecture. At the back, we can notice the full-area *p*-type layer.
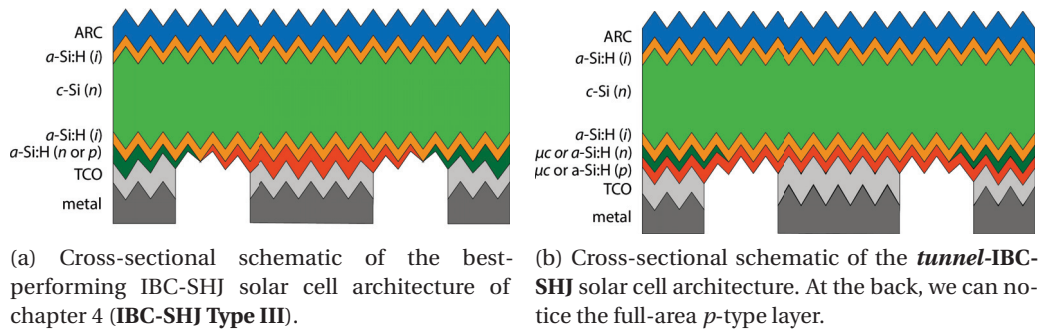
Figure 6.1: Comparison of cross-sectional schematics for the best-performing IBC-SHJ architecture and the *tunnel*-IBC-SHJ concept. We can notice the absence of the front *n*-type a-Si:H layers, in both devices.

different 4-cm^2 cell areas on the wafer. For further details on our FHC solar cells, and the relative processing sequence, please refer also to [Descoeudres 2013]. The two-side-contacted devices of this chapter were fabricated to assess different IST junctions, in the back electron contact. The resulting *test*-FHC device structure is depicted in Fig. 6.2 (b).

The *n*-type a-Si:H or μc-Si:H "comb" of our *tunnel*-IBC-SHJ, needed for electron collection, was fabricated first via an *in-situ* shadow mask, during PECVD. Then, full-area deposition of a *p*-type a- or μc-Si:H film was performed to act as IST junction, all over the electron collecting region, and as hole collector, everywhere else (see also Fig. 6.1). Hole and electron collecting contacts were completed by the addition of a TCO film and a thick metal layer. These were sputtered on the full back surface and patterned in two interdigitated combs via hot-melt inkjet printing and wet-chemical etching [Tomasi 2014a, Tomasi 2014b]. As antireflection coating, at the front side, an a-SiN$_x$:H layer was deposited by PECVD, at sufficiently low temperature (< 200°C) to avoid annealing induced degradation of the a-Si:H layers [De Wolf 2009].

In this chapter, TLM contact pad arrays, integrating electron contacts with an embedded IST junction, have been also fabricated and characterized. Such test structures were realized as described in section 5.3.2.

6.3 The *tunnel*-IBC-SHJ solar cell concept

In Fig. 6.1, our *tunnel*-IBC-SHJ solar cell concept is compared to our best-performing IBC-SHJ architecture of chapter 4. The proposed device design presents several very unique features. Most importantly, the hole collecting *p*-type doped a-Si:H or μc-Si:H layer does not have to be patterned, nor aligned, in any way to the other previously or subsequently deposited functional layers. This brings a drastic reduction of the fabrication complexity as well as a drastic increase of the process robustness and yield. In addition, the doped a-Si:H or μc-Si:H/TCO contacting problem is reduced to one unique doping type of a- or μc-Si:H, simplifying the optimization of the hole and electron contact properties.

Chapter 6. 22.9% back-contacted silicon heterojunction solar cell enabled by an interband silicon tunnel junction

The key to enable the *tunnel*-IBC-SHJ technology is the fabrication of an effective IST junction at the interface of hole and electron collecting layers. Thanks to internal field emission current transport, well-engineered tunnel junctions are characterized by anomalous I-V characteristics which allow, up to a certain peak current density, an extremely low electrical resistance in both forward and reverse direction. Under solar cell operation this guarantee a low voltage loss across the electron contact and prevent detrimental effects on the device *FF*s. Since their early discover by Esaki in 1958 [Esaki 1958], interband tunnel junctions were successfully exploited in various microelectronic and photovoltaic devices. Practically, interband tunnel junctions are formed at the interface of highly doped *p*-/*n*-type materials, whose high doping levels guarantee extremely narrow depletion widths. For this reason, highly-doped μc-Si:H materials are better candidates than a-Si:H to form an effective IST junction in our *tunnel*-IBC-SHJ concept.

6.3.1 Interband tunneling in photovoltaic technologies

In the field of photovoltaics, the spreading of interband tunnel junctions relates with the implementation of the multi-junction solar cell concept. Such type of device in its monolithic implementation, theorized already in 1960 [Wolf 1960], rely on interband tunnel junctions to serially connect the different sub-cells with a low electrical resistance and low optical losses.

Tunnel junctions were successfully implemented in high-efficiency III-V compound multi-junction solar cells [Amano 1987] and tandem a-Si:H/a-Si:H thin-film devices [Yoshida 1987]. Later, based on the developed experience, their use was also extended to "micromorph" solar cells [Meier 1995], and even to triple- and quadruple-junction thin-film silicon based devices [Schüttauf 2014, Schüttauf 2015]. The case of multiple-junction thin-film silicon solar cell is most interesting with respect to our *tunnel*-IBC-SHJ concept. Processing technologies and materials, in this application, are very similar to those used for SHJ device fabrication. State-of-the-art tandem a-Si:H/a-Si:H devices typically make use of an IST junction based on doped μc-Si:H films, deposited via PECVD. Optimized results were shown to critically depend on the insertion either of a thin silicon oxide, or of a thin intrinsic μc-Si:H layer, in between the two doped μc-Si:H films [Rath 1998, Rath 2000, Rubinelli 2001]. Recently, well-optimized interband tunnel junctions are gaining, again, some attention; the mature stage of development reached by c-Si based devices, triggered research efforts towards new c-Si tandem devices combining c-Si with III-V compounds [Derendorf 2013, Takashi 2005, Hamon 2015] or more exotic materials, as for instance perovskites [Mailoa 2015, Werner 2016b].

We note that in several photovoltaic devices, as for instance SHJ solar cells and thin-film silicon devices, carrier transport from the *p*-type doped layers to the TCO electrode occurs via hole-electron recombination processes [Kanevce 2009], similarly as in an interband tunnel junction. Despite the presence of such recombinating-interface, these devices did not fail in achieving the absorber potentialities.

Based on the fact that all such diverse technologies make an effective use of a tunnelling

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junction without suffering any performance limitation, fostered our belief on the feasibility of the *tunnel*-IBC-SHJ concept. We remark that the application of an IST junction in an efficient c-Si wafer-based back-contacted device was envisaged [Spee 2008, Herasimenka 2014] but, to our knowledge, never demonstrated before.

6.3.2 Requirements for an effective IST junction in *tunnel*-IBC-SHJ solar cells

Compared to the cases mentioned in section 6.3.1, the IST junction required for efficient *tunnel*-IBC-SHJ solar cells must solve some additional challenges. Here, we give a description of such specificities and present the methodology of our research (section 6.3.3). The IST junction of our *tunnel*-IBC-SHJ devices must comply with the following requirements:

(i) The *n*-type doped film at one side of the IST junction (hereafter referred as "IST-*n*" film) is deposited through an *in-situ* shadow mask. Conversely, the *p*-type doped film of the IST junction (hereafter referred as "IST-*p*" film) is deposited over the wafer full-area and must form an efficient IST junction in contact with the IST-*n* film, while acting as well-optimized hole collector outside the IST junction area.

(ii) The presence of a thin film material on top of a c-Si wafer can modify the electrical field at its surface. In the case of a stack of sufficiently-thin layers, such surface field effect may be influenced also by the electronic band structure of the overlying film, which is not directly in contact with the c-Si surface. Such interference of field effects is routinely exploited in passivated-contact technologies, where an extremely thin passivating layer, on the wafer surface, is coated by a high- or low-WF material to form an efficient selective hole or electron contact, respectively [Tomasi 2016b, Geissbuhler 2015b, Bullock 2016]. Importantly, field-interference effects were observed also for three-layer stacks as in the case of TCO layers on top of SHJ hole or electron collectors [Tomasi 2016b, Rößler 2013, Macco 2014, Favre 2013, Demaurex 2014]. Thus the electron collecting stack in our *tunnel*-IBC-SHJs must be engineered in such a way to be opaque to the electronic band structure of the IST-*p* overlayer.

(iii) The IST junction of our *tunnel*-IBC-SHJ solar cells should feature a sufficiently-high peak current density. Compared to the case of tandem thin-film silicon devices, the current density through our IST junction will be significantly higher due to: (1) the use of a non-tandem architecture and (2) a reduced contact-fraction < 0.5 as result of the back-contact architecture and of narrow electron collecting fingers to control electrical-shading losses (see section 4.6.5). We can estimate current density multiplication factors of 2 and 3 due to effect (1) and (2), respectively. Practically, we expect current densities of about $240\,\mathrm{mA\,cm^{-2}}$ going through our IST junction.

(iv) It is well known that a-Si:H layer stacks may suffer of annealing induced degradation at temperature higher than $200\,^{\circ}\mathrm{C}$ [De Wolf 2009]. To prevent such effects the fabrication of our IST junction should rely exclusively on low-temperature processes.

(v) Eventually, the IST-*p* and IST-*n* films, despite being sufficiently doped to guarantee efficient carrier tunnelling, must feature a sufficiently-low lateral conductance to prevent short-circuiting the *tunnel*-IBC-SHJ device.

6.3.3   Our research methodology

In our research, we considered a wide spectrum of materials and deposition regimes to find the best candidates as IST-*p* and IST-*n* films. As a consequence of the experience matured in the field of multi-junction thin-film silicon devices, we included μc-Si:H doped materials, beside the conventional a-Si:H films used in heterocontacts. We studied the impact of embedding different IST junctions in:

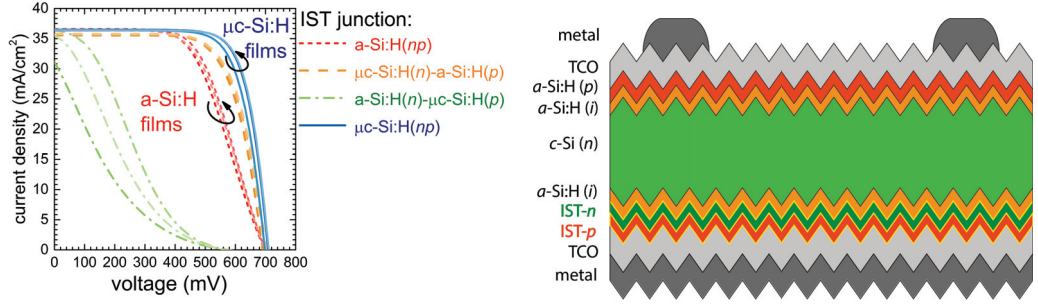(i) the back electron contact of *test*-FHC devices (see section 6.4),

(ii) the electron contacts of TLM structures (section 6.5) and,

(iii) in *tunnel*-IBC-SHJ devices (section 6.6).

6.4   IST junctions in *test*-FHC solar cells

Making use of the *test*-FHC solar cell structure of Fig. 6.2 (b), we screened several combinations of IST-*n* and IST-*p* films.[1] We note that the operating conditions for such embedded IST junction resembles very much those that would be encountered in the *tunnel*-IBC-SHJ concept.

In Fig. 6.2 (a), we summarized the 1-sun I-V characteristic of the most relevant *test*-FHC solar cells. For each layer combination we fabricate three solar cells and the electrical parameters of the best one, for each group, are reported in Table 6.1. For the case in which only doped a-Si:H films are used, we achieve a maximum conversion efficiency of 15 % due to a poor V_{oc} of roughly 700 mV and *FF* not exceeding 60 %. The I-V characteristic of such solar cells are slightly S-shaped. Replacing the a-Si:H(*n*) layer with a μc-Si:H(*n*) layer the I-V characteristic is not S-shaped anymore and the FF increases to values around 70 %. Losses due to charge-carrier transport are still limiting the device, but less severely. Eventually replacing also the a-Si:H(*p*) layer with a μc-Si:H(*p*) layer we reached conversion efficiencies up to 20 %, thanks to improved $V_{oc} > 700mV$ and *FF* in the range 76 % to 77 %. Most importantly, such electrical parameters are aligned with those routinely achieved in FHC solar cells, *without* IST junction, when employing doped a-Si:H films of the PECVD reactor used in this experiment. Concurrent reference cells with a-Si:H(*in*) and μc-Si:H(*in*) electron collector showed V_{oc} of about 715 mV, J_{sc} of 37.0 mAcm^{-2}, *FF* of 76 % and conversion efficiency slightly above 20.0 %. The best-performing doped μc-Si:H material, which allowed the results presented here, was deposited at higher powers and pressures than standard a-Si:H [Seif 2015, Seif 2016b, Nogay 2016]. The

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[1]This work was done in collaboration with M.J. Lehmann, during his Master's thesis.

(a) 1-sun I-V characteristics of *test-FHC* solar cells using different back electron contacts with embedded IST junction. The electrical parameter of the best solar cell, for each type of electron contact, are reported in Table 6.1.

(b) Cross-sectional schematic of the *test*-FHC solar cell. The device structure is the same of a conventional FHC device with the addition of the IST-*p* film in between the electron collector and the TCO. Adapted from [De Wolf 2012b].

Figure 6.2: Schematic of the *test*-FHC solar cell and measured 1-sun I-V characteristics for different IST junctions. The films varied in the experiment are highlighted with a thicker yellow border in the sketch of (b).

correspondence of the electrical parameters achieved for the *test*-FHC solar cell, embedding the "all μc-Si:H-based" IST junction, with those of our typical FHC SHJ devices, indicates a properly engineered back electron contact and IST junction. We note that using μc-Si:H(*p*) as IST-*p* films in combination to a-Si:H(*n*) as IST-*n* film, we observed severe detrimental effects on the device characteristics. We may attribute this effect to the interference of the highly doped μc-Si:H(*p*) layer on the relatively weak surface field effect induced by the a-Si:H(*n*) layer within the c-Si absorber. This compromises the electron collecting character of the whole contact stack, degrading the overall device performances.

Table 6.1: Best electrical parameters of *test-FHC* solar cells using different electron contacts with embedded IST junction. The exact composition of the back electron contact is "a-Si:H(*i*)/IST-*n*/IST-*p*/TCO/metal". At the front these devices feature the a-Si:H(*ip*) hole collecting stack of conventional FHC SHJ solar cells.

IST-*n*	IST-*p*	J_{sc} (mA cm^{-2})	V_{oc} (mV)	*FF* (%)	η (%)
a-Si:H(*n*)	a-Si:H(*p*)	37.2	0.698	61.0	15.9
μc-Si:H(*n*)	a-Si:H(*p*)	36.5	0.703	69.5	17.8
a-Si:H(*n*)	μc-Si:H(*p*)	37.5	0.574	24.1	5.2
μc-Si:H(*n*)	μc-Si:H(*p*)	37.5	0.710	75.7	20.2

6.5 IST junctions in TLM contact pad arrays

The results achieved in the experiment of section 6.4 were confirmed in TLM contact pad arrays. These were fabricated as in chapter 5 (for a detailed description see section 5.3.2), depositing the full-area doped a-Si:H or μc-Si:H layers on one surface of both-side a-Si:H(*i*)-passivated *n*-type c-Si textured wafers. The TLM pads are formed by a TCO and a thick metal
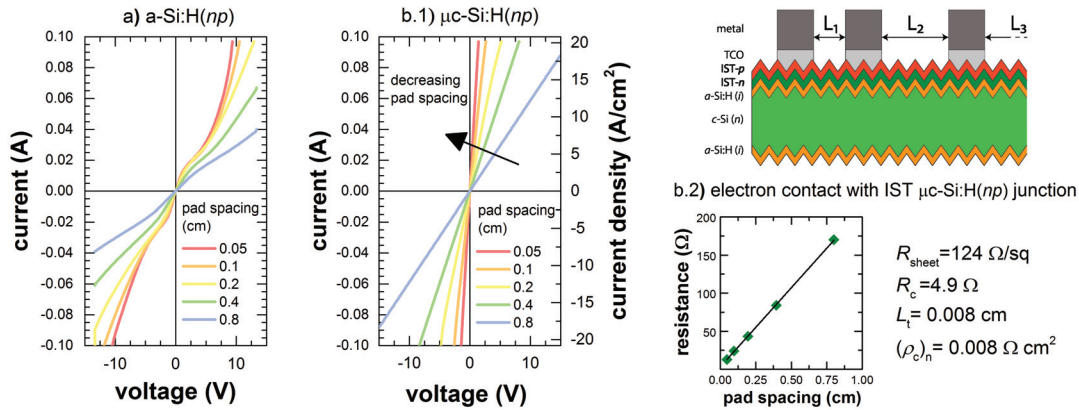
Figure 6.3: I-V characteristics measured between contact pads of TLM structures integrating electron contacts with a-Si:H(n)/a-Si:H(p) (a) and μc-Si:H(n)/μc-Si:H(p) (b) IST junctions, respectively. In the right inset, we report the cross-sectional schematic of the used TLM structure.

overlayer, patterned via *in-situ* shadow masking during sputtering, and the test structures are eventually laser-cut in stripes, wide as the TLM pads, to suppress lateral current flows. A schematic of the resulting structure is reported in the inset of Fig. 6.3, together with the I-V curve measured in between the TLM contact pads, for samples integrating the "all a-Si:H-based" and the "all μc-Si:H-based" IST junctions, respectively.

In the case of the "all a-Si:H-based" IST junction we do not observe a linear characteristic, which is consistent with the slightly S-shaped I-V measured in the *test*-FHC solar cell. For the case of the "all μc-Si:H-based" IST junction we observe instead a very linear behaviour consistent, again, with the results achieved in the previous device-related experiment. Performing a TLM analysis, we extracted, for several different samples, a R_{sheet} of about $130\,\Omega/\square$, specific contact resistivity values $\leq 0.01\,\Omega\,\text{cm}^2$ and $L_t \leq 100\,\mu\text{m}$. Comparing the measured I-V curves and the extracted contact resistance parameters with the results of section 5.3, we conclude that the developed IST junction works effectively and should not impede the successful implementation of the *tunnel*-IBC-SHJ concept.

6.6 *Tunnel*-IBC-SHJ solar cells: results and discussion

Based on the results of section 6.4 and 6.5, we started confidently our research efforts to demonstrate the *tunnel*-IBC-SHJ concept. In a first stage, in section 6.6.1, we probed selected IST junctions in *tunnel*-IBC-SHJ devices. So doing, we could already achieve encouraging device results demonstrating the feasibility of the *tunnel*-IBC-SHJ concept and the superiority of μc-Si:H materials with regard to our application. In a second stage we focused on the optimization of the "all μc-Si:H-based" *tunnel*-IBC-SHJ device taking in consideration the following aspects:

(i) the role of the back a-Si:H(*i*) film (section 6.6.2),

(ii) the re-optimization of the TCO/metal electrode geometry for the case of a uniformly-thick μc-Si:H(*p*) layer (section 6.6.3) and

(iii) the interfaces of the μc-Si:H(*p*) layer with the passivating a-Si:H(*i*) film and the μc-Si:H(*n*) layer in the hole and electron contact areas, respectively (section 6.6.4).

6.6.1 IST junctions in *tunnel*-IBC-SHJ solar cells

The integration of a-Si:H- and μc-Si:H-based IST junctions in *tunnel*-IBC-SHJ solar cells gave results in line with our expectations. The use of only a-Si:H-based layers resulted always in *tunnel*-IBC-SHJ devices with I-V characteristics that at least were slightly S-shaped, whereas the use of μc-Si:H-based materials allowed the achievement of *tunnel*-IBC-SHJ solar cells with well-behaved I-V curves.

Using the same doped layers of section 6.5 in *tunnel*-IBC-SHJ devices we reached the best efficiencies reported in Table 6.2. The "all a-Si:H-based" IST junction showed a maximum efficiency of about 16 % limited by *FF* values < 60 %. The "all μc-Si:H-based" IST junction instead allowed efficiencies and *FF* close to 20 % and 70 %, respectively. With respect to the experiment of section 6.4, in which we performed only planar depositions, and similarly as for the doped a-Si:H layers in our IBC-SHJ technology (section 4.4) the deposition time for the IST-*n* film had to be adapted.

Table 6.2: Electrical parameters of *tunnel*-IBC-SHJ solar cells with an "all a-Si:H-based" and an "all μc-Si:H-based" IST junction. The exact layer composition of the electron contact is "a-Si:H(*i*)/IST-*n*/IST-*p*/TCO/metal" whereas, in the case of the hole contact, is "a-Si:H(*i*)/IST-*p*/TCO/metal". For reasons of experimental simplicity, at the front side these devices feature an a-Si:H(*in*)/ITO stack.

IST-*n*	IST-*p*	J_{sc} (mA cm^{-2})	V_{oc} (mV)	*FF* (%)	η (%)
a-Si:H(*n*)	a-Si:H(*p*)	38.6	0.713	58.7	16.2
μc-Si:H(*n*)	μc-Si:H(*p*)	38.8	0.714	69.6	19.3

6.6.2 On the role of the back intrinsic a-Si:H layer

Based on the clear outcomes of the previous sections, from now on the use of doped a-Si:H was abandoned. Here we discuss effects linked to the back a-Si:H(*i*) layer, in "all μc-Si:H-based" *tunnel*-IBC-SHJ devices. The back a-Si:H(*i*) passivating layer happened to be a critical factor in achieving high *tunnel*-IBC-SHJ device performances, and more specifically simultaneous high *FF* and J_{sc} values.

Table 6.3 and Fig. 6.4 present the impact of two selected a-Si:H(*i*) layer types, in two showcase

tunnel-IBC-SHJ solar cells.[2] We remark on the fact that, for reasons of experimental simplicity, at the front side these devices presents an a-Si:H(*in*)/ITO stack. Each device belongs to an entire class of devices fabricated with one of these two different a-Si:H layers, which are characterized by a comparable thickness, of about 10 nm on flat glass substrates, but different plasma deposition regimes. The plasma excitation frequency was 13 MHz and 40 MHz for the case of a-Si:H(i)[A] and a-Si:H(i)[B], respectively. In the case of a-Si:H(i)[A], the respective *tunnel*-IBC-SHJ devices show J_{sc} values in line with those of our IBC-SHJ devices but lower *FF*, whereas, in the case of a-Si:H(i)[B], they show low J_{sc} but high *FF* values, close to the highest ever reached, including also our IBC-SHJ technology. The two *tunnel*-IBC-SHJ solar cells are named after the a-Si:H(i) layer type used in their contacts, as *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B], respectively. To point out the causes of such a clear distinction in the final electrical parameters, these two solar cells underwent further characterization.

Table 6.3: Electrical parameters of *tunnel*-IBC-SHJ solar cells with an "all µc-Si:H-based" IST junction but different back-side a-Si:H(i) films. The exact composition of the electron and hole contacts are "a-Si:H(i)/IST-*n*/IST-*p*/TCO/metal" and "a-Si:H(i)/IST-*p*/TCO/metal", respectively, where the a-Si:H(i) layer is of type A (13 MHz) or of type B (40 MHz). The two *tunnel*-IBC-SHJ solar cells are named as *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B], respectively. For reasons of experimental simplicity, at the front side these devices feature an a-Si:H(*in*)/ITO stack.

Name	**a-Si:H(i)**	IST	J_{sc} (mA cm^{-2})	V_{oc} (mV)	*FF* (%)	η (%)
tunnel-IBC-SHJ[A]	a-Si:H(i)[A]	µc-Si:H(*np*)	**39.1**	0.711	**67.7**	18.8
tunnel-IBC-SHJ[B]	a-Si:H(i)[B]	µc-Si:H(*np*)	**35.7**	0.709	**75.8**	19.2

$\tau_{eff}(\Delta n)$, electrical-shading losses and J_{sc} values

The low J_{sc} of *tunnel*-IBC-SHJ[B] is a very distinctive feature. In our research on back-contacted SHJ devices we encountered very rarely such low J_{sc} values. Tracking $\tau_{eff}(\Delta n)$ during the various processing steps, a pronounced difference in its evolution was observed, comparing *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B]. As shown in Fig. 6.5, in the case of the *tunnel*-IBC-SHJ[B] precursor the $\tau_{eff}(\Delta n)$ curve degrades importantly after the full-area deposition of the µc-Si:H(*p*) layer; this degradation being stronger at low Δn values. Low τ_{eff} at low Δn results in low J_{sc} values for this class of devices, hinting at enhanced electrical-shading losses (see also section 4.6.5).

To confirm our hypothesis we did LBIC cross-sectional measurements. In Fig. 6.6, we report the LBIC profiles measured for the *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B] solar cells and for the IBC-SHJ device with high-quality passivation of section 4.6.5 and Fig. 4.22. The

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[2]The a-Si:H(i) layers type A and B were developed at the PV-Center of CSEM. The results presented were obtained with the help of B. Paviet-Salomon, A. Descoeudres, L. Barraud and M. Despeisse. Contributions are gratefully acknowledged.
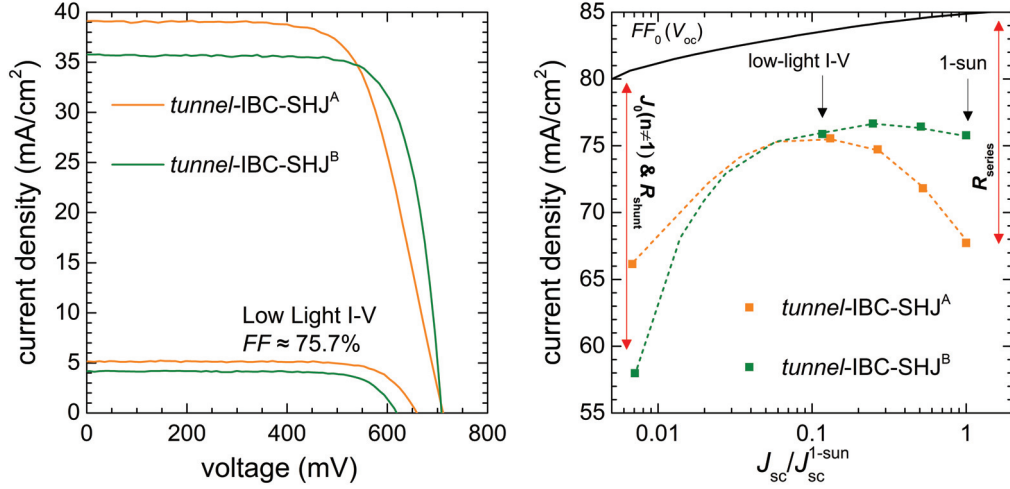
(a) 1-sun I-V characteristics of the devices *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B]. The electrical parameters extracted from these curves are summarized in Table 6.3.

(b) Illumination-dependent *FF* measurements for the devices *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B]. The low R_{series}^{N} characterizing *tunnel*-IBC-SHJ[B] translates in almost constant *FF*s for illumination intensities down to about 0.1 suns.

Figure 6.4: Electrical characterization of the devices *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B] of Table 6.3.

electrical parameters of such IBC-SHJ device are reported in Table 6.4. From now on we refer to this device as **well-passivated IBC-SHJ** solar cell. We scanned the entire 3-cm-wide active area of the solar cell, perpendicularly to the collecting fingers, at a distance of 1 cm from the bus bar of the electron contact. The LBIC signal measured on *tunnel*-IBC-SHJ[A] follows closely that of the well-passivated IBC-SHJ device, whereas, that of *tunnel*-IBC-SHJ[B] drops importantly whenever scanning the electron collecting fingers. In overall, we established a perfect correspondence between *tunnel*-IBC-SHJ devices with degraded $\tau_{eff}(\Delta n)$ curves, low J_{sc} values and electrical-shading losses, which confirm our initial hypothesis.

We note that the locally-lower LBIC signal, impact also the overall IQE/EQE curves measured on these devices. As already suggested in section 4.6.5, electrical-shading losses in back-contacted devices result in an increment of the J_{sc}-loss term, J_{medium}. In Fig. 6.7 we can observe the EQE curves of *tunnel*-IBC-SHJ[A], *tunnel*-IBC-SHJ[B] and the well-passivated IBC-SHJ solar cell, of which LBIC profiles were already shown in Fig. 6.6. J_{medium} for the three cells equals $0.3\,\mathrm{mA\,cm^{-2}}$, $2.5\,\mathrm{mA\,cm^{-2}}$ and $0.6\,\mathrm{mA\,cm^{-2}}$, respectively. The remaining difference in J_{sc} for *tunnel*-IBC-SHJ[B] compared to *tunnel*-IBC-SHJ[A], or the well-passivated IBC-SHJ devices, comes mainly from higher J_{short} losses which can also be attributed to increased electrical-shading losses.

In overall, we found that the deposition of μc-Si:H(p) layers in our *tunnel*-IBC-SHJ concept, depending on the type of passivating a-Si:H(i) layer, may bring to a degradation of the $\tau_{eff}(\Delta n)$ curve and more remarkably at low Δn. Such degradation, which origin is still under investiga-
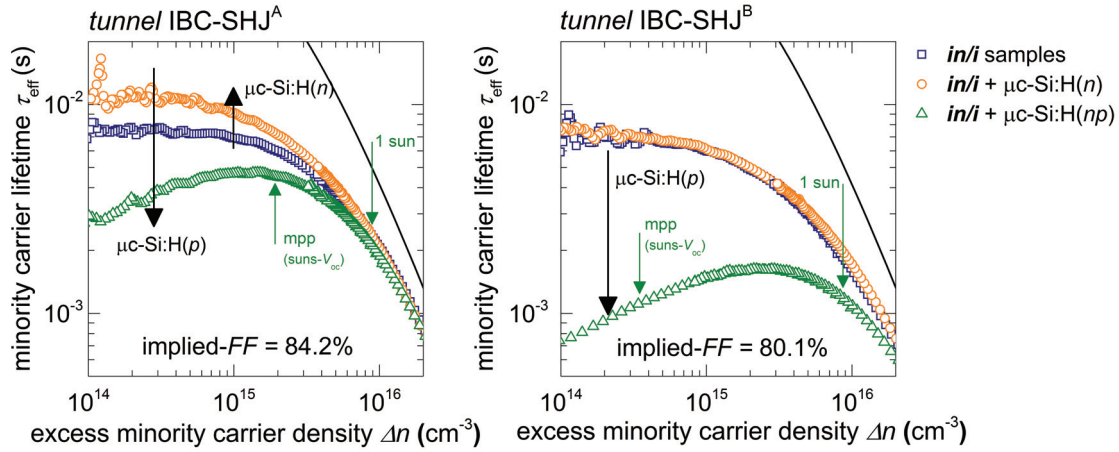
Figure 6.5: Measurements of $\tau_{\text{eff}}(\Delta n)$ on the n-type cell precursors of the device *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B], at different steps throughout the fabrication process. These samples feature initially an a-Si:H(in) stack at the front and an a-Si:H(i) layer at the back ("in/i samples"). Afterwards a μc-Si:H(n) layer, patterned via *in-situ* shadow masking to form the n-type comb of the IBC design, is deposited on the back-side. Eventually a full-area μc-Si:H(p) layer is deposited on top of the patterned μc-Si:H(n) layer. The injection levels corresponding to 1-sun illumination and the maximum power point (mpp) in suns-V_{oc} measurements of finished devices are marked by solid arrows. The combined Auger and radiative limit is indicated by the solid line [Richter 2012].

tion, provokes enhanced electrical-shading losses resulting in low J_{sc} values. The enhanced losses are detectable from increasingly lower LBIC signal intensities away from the hole collecting fingers. Conversely, due to the strong dependency of τ_{eff} from Δn in the degraded curves, i.e. sufficiently-high τ_{eff} values at high Δn, the V_{oc} of the same devices are practically unaffected. These findings allow to explain the different J_{sc} values in the devices *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B].

In a different experiment (data not shown), we experienced improved final $\tau_{\text{eff}}(\Delta n)$ curves, after the μc-Si:H(p) blanket deposition, for thicker back-side a-Si:H(i)[B] films. We found that the thicker the a-Si:H(i)[B] film is, the weakest are the $\tau_{\text{eff}}(\Delta n)$ degradation and the associated electrical-shading losses. All the experimental observations discussed above on the causes of low J_{sc} for the case of *tunnel*-IBC-SHJ[B]($\tau_{\text{eff}}(\Delta n)$, LBIC and EQE measurements), are confirmed also for the case of the *tunnel*-IBC-SHJ devices of this experiment.

The wide range of τ_{eff} values explored in optimization experiments dealing with the type of a-Si:H(i) film and its thickness created an extended data set of $\tau_{\text{eff}}(\Delta n)$ curves and J_{sc} values for *tunnel*-IBC-SHJ devices. Plotting J_{sc} values as a function of τ_{eff} makes clear the strong sensitivity of the J_{sc} of our back-contacted devices from the level of passivation. In Fig. 6.8, J_{sc} losses up to $4\,\text{mA}\,\text{cm}^{-2}$ can be attributed to low τ_{eff} and poor carrier collection. We remark on the fact that the data points reported in this figure, for reasons independent from our investigation, are not homogeneous with respect to the employed front-side stack. The group
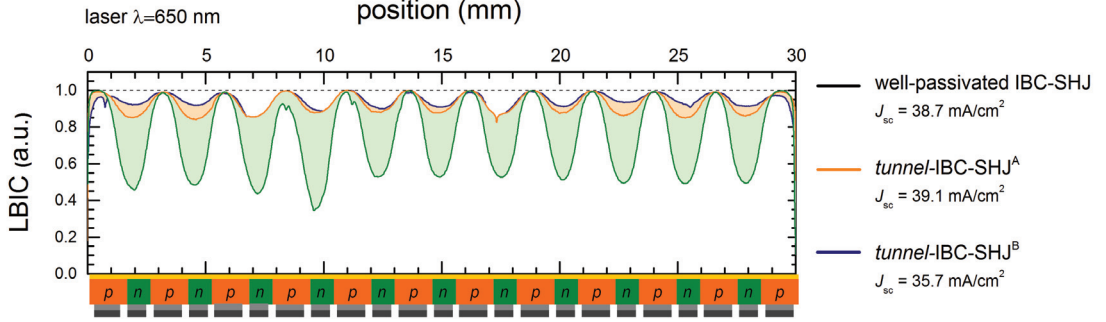
Figure 6.6: LBIC cross-sectional profiles in dark of the devices *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B], employing a back-side a-Si:H passivating layer deposited at 13 MHz and 40 MHz, respectively. The LBIC cross-sectional profile of the well-passivated IBC-SHJ device, presented in Fig. 4.22, is also reported as reference. *Tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B] are characterized by a J_{sc} of 39.1 mA cm^{-2} and 35.7 mA cm^{-2}, respectively, as results of different electrical-shading losses. The filled area in between the LBIC profiles represent the amount of charge carriers lost due to electrical-shading losses.

of devices indicated with the empty symbols feature at the front a lowly-doped TCO film as ARC and the "old" a-Si:H(*in*) stack used in the architectures IBC-SHJ type I and II (chapter 3 and 4). Thus, their J_{sc} suffer from higher absorption losses and reach, for sufficiently-high τ_{eff}, maximum values only 2 mA cm^{-2} lower than the other group of devices employing the J_{sc}-optimized front stack of the architecture IBC-SHJ type III. In Fig. 6.8 we also indicate with special symbols the data points corresponding to device *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B] which belong to the high and low τ_{eff} group, respectively.

$\tau_{eff}(\Delta n)$, transport losses and *FF* values

The case of *tunnel*-IBC-SHJ[B] is representative of a general improved *FF* in *tunnel*-IBC-SHJ devices, thank to the use of a-Si:H(*i*)[B] as back-side passivating layer. The *FF* loss terms calculated in Table 6.4 show low losses due to carrier transport for *tunnel*-IBC-SHJ[B]. The extracted R^{N}_{series} and the correspondent $\Delta FF_{R_{series}}$ value are significantly lower than for the optimized IBC-SHJ devices of chapter 4, as for instance IBC-SHJ[2], and even for the reference FHC SHJ device [Descoeudres 2013]. Simultaneously, as we could expect from the $\tau_{eff}(\Delta n)$ curve reported in the right graph of Fig. 6.5, $\Delta FF_{J_0(n\neq 1)}$ results strongly enhanced and corresponds to a low *pFF* value. This reduction in series resistance losses is the result of using μc-Si:H-based contacts with improved transport properties, with respect to a-Si:H-based contacts. To support this argument we remind of the characterization results of Fig. 6.3, which attribute highly-optimized transport properties to the μc-Si:H-based electron contact with embedded IST junction. Such low R^{N}_{series} values and low $\Delta FF_{R_{series}}$ losses, were confirmed in all *tunnel*-IBC-SHJ devices combining a-Si:H(*i*)[B] and doped μc-Si:H layers in their heterocontacts, independently from the final $\tau_{eff}(\Delta n)$ curves. Reduced losses due to carrier transport for the film a-Si:H(*i*)[B] are proved
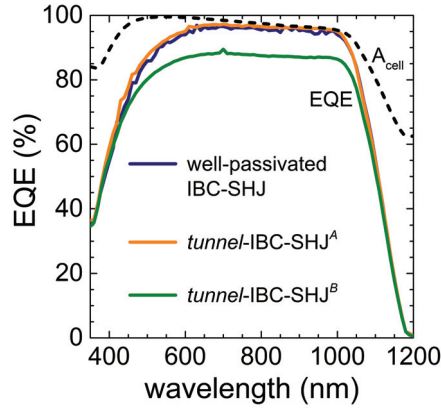
Figure 6.7: EQE curves of *tunnel*-IBC-SHJ[A], *tunnel*-IBC-SHJ[B] and the well-passivated IBC-SHJ solar cell. We reported also the measured absorbance curve (identical for all the three solar cells)

also by illumination dependent *FF*s measurements. In the case of *tunnel*-IBC-SHJ[B] we observe an almost constant *FF* for I-V characteristics measured at low illumination intensities down to about 0.1 sun (see Fig. 6.4 (b)). This differs from the case of our IBC-SHJ devices and of the device *tunnel*-IBC-SHJ[A], showing increasingly-high *FF*s down to about 0.1 suns, and indicates low losses due to carrier transport for the device *tunnel*-IBC-SHJ[B].

We remark on the fact that for the devices of Table 6.4 , R_{series}^{N} values were extracted from the comparison of dark I-V and 1-sun I-V characteristics [Pysch 2007]. Typically this method is perfectly equivalent to that based on the comparison of 1-sun I-V characteristic and suns-V_{oc} curves; however, in the case of the class of device defined by *tunnel*-IBC-SHJ[B] we could not extract reasonable R_{series}^{N} values. The voltages measured on these devices drops significantly at low illumination intensities and the resulting pseudo I-V curves almost superimpose to the 1-sun I-V characteristics.

In general, our *tunnel*-IBC-SHJ devices show lower R_{shunt} values, compared to conventional two-side-contacted SHJ devices and IBC-SHJ devices (always $\geq 50 k\Omega\,cm^2$). *Tunnel*-IBC-SHJ R_{shunt} values cover an extremely wide range from about 50 k$\Omega\,cm^2$ down to 5 k $\Omega\,cm^2$. However, these values are sufficiently-high to determine still negligible effects on the 1-sun I-V characteristic and $\Delta FF_{R_{shunt}} < 0.3\,\%$. We remind that R_{shunt} values are extracted from the slope of a linear fit to the dark I-V characteristic in the range (0,-100) mV. R_{shunt} values of 5 k$\Omega\,cm^2$ are totally unusual for SHJ devices and will associate to lower performances at low illumination intensities. Nevertheless, R_{shunt} in this range are typical in conventional diffused solar cells [Khanna 2013] and still acceptable for a photovoltaic technology.

With respect to the improved *FF* of the *tunnel*-IBC-SHJ[B] device it should also be noted the following. Electrical-shading losses depend on the minority carrier diffusion length (L_h), which is defined for specific values of Δn. Due to the measured dependency of the τ_{eff}, and the associated L_h, from Δn (see also Fig. 6.5), we can expect a reduction of electrical-shading losses
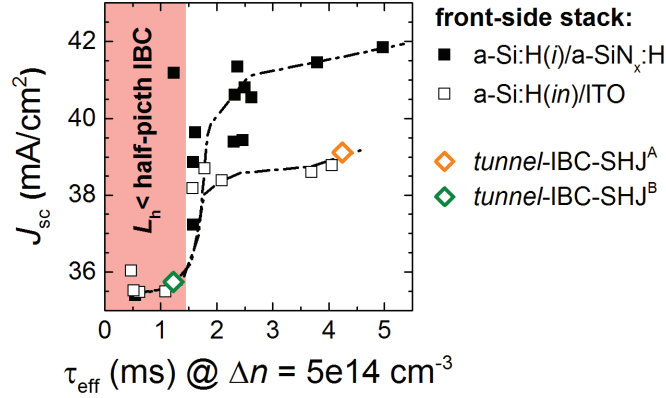
Figure 6.8: Measured τ_{eff} on the solar cell precursor, after the deposition of all a-Si:H and μc-Si:H layers, and measured 1-sun J_{sc} value after completion of the *tunnel*-IBC-SHJ device (on the respective cell precursor). The data points corresponding to the devices *tunnel*-IBC-SHJ^A and *tunnel*-IBC-SHJ^B are indicated with special symbols. The τ_{eff} values are measured at an excess minority carrier density $\Delta n = 5 \cdot 10^{14}$ cm^{-3}. We remark that most of the *tunnel*-IBC-SHJ devices with the a-Si:H(i)/a-SiN$_x$:H front stack and $\tau_{eff} > 2$ ms, show conversion efficiencies $\geq 22\%$.

for increasing voltage values, i.e. Δn, moving from J_{sc} conditions towards mpp conditions. This phenomenon may have effects on the shape of the final I-V characteristic and increase the measured *tunnel*-IBC-SHJ^B *FF* value. In this hypothesis, the higher *FF*, compared to *tunnel*-IBC-SHJ^A, may deteriorate once electrical-shading losses are resolved. However, we think that such possible *FF* artefact, if present, is a minor effect. Our arguments are the following: (1) with the use of a-Si:H(i)^B in the back-contacts we could improve $\tau_{eff}(\Delta n)$ curves and J_{sc} values maintaining *FF*s of about 76 %; (2) comparing the 1-sun I-V characteristics measured in Fig. 6.4 (a) for the devices *tunnel*-IBC-SHJ^A and *tunnel*-IBC-SHJ^B we can attribute the *FF* difference mainly to the slope of the curve close to open-circuit conditions, which relates to the device series resistance. This last observation is confirmed by the evidence of higher transport losses in the case of *tunnel*-IBC-SHJ^A compared to *tunnel*-IBC-SHJ^B, as already discussed above.

In conclusion, we could link the observed low J_{sc} and high *FF*, for different a-Si:H(i) film types, to degraded $\tau_{eff}(\Delta n)$ curves, with a strong Δn dependency, and reduced carrier transport losses, respectively. Based on the electrical parameters of *tunnel*-IBC-SHJ^B, solving the degradation of $\tau_{eff}(\Delta n)$ while maintaining *FF* unchanged, we see already the potential for conversion efficiencies over 22.0 %. In addition to the strong electrical-shading losses, the J_{sc} of *tunnel*-IBC-SHJ^B was penalized by the not-optimized front-stack accounting for a loss of almost 2 mA cm^{-2}. With an optimized front-stack *tunnel*-IBC-SHJ^B would have already overcome a conversion efficiency of 20.0 %. Then, eliminating the J_{sc} loss compared to *tunnel*-IBC-SHJ^A, the conversion efficiency would reach a value > 22 %. Similar efficiencies results were reached already in the experiment of the next section, where we could benefit again of the optimized

Table 6.4: Electrical parameters and *FF* losses of the well-passivated IBC SHJ device and of the devices *tunnel*-IBC-SHJ[A] and *tunnel*-IBC-SHJ[B].

Parameter	well-passivated IBC-SHJ	*tunnel*-IBC-SHJ[A]	*tunnel*-IBC-SHJ[B]
V_{oc} (V)	0.719	0.711	0.709
J_{sc} (mA/cm^2)	38.7	39.1	35.7
η (%)	21.0	18.8	19.2
FF (%)	75.4	67.7	75.8
R^{N}_{series} ($\Omega\,cm^2$)	1.3	3.0	0.73
pFF (%)	81.8	84.7	76.8
$\Delta FF_{R_{series}}$ (%)	6.5	15.4	3.4
$\Delta FF_{J_0(n\neq1)}$ (%)	3.0	1.7	5.5

front-stack developed in chapter 4, and in most of the devices populating the upper branch of the graph of Fig. 6.8.

6.6.3   The impact of a homogeneously-thick hole collector

The μc-Si:H(p) hole collecting film, in *tunnel*-IBC-SHJ devices, is fabricated with a mask-less planar deposition, exactly as in a conventional two-side-contacted device. This is a strong favourable point for such back-contacted technology which, compared to the case of our IBC-SHJ solar cells, presents the great advantage of a homogeneously-thick hole collecting layer. The performance losses discussed in section 4.4, occurring when contacting portion of insufficiently-thick doped a-Si:H layers with the TCO/metal electrodes, should be avoided.

The experiment presented in section 4.4.4, for the case of IBC-SHJ devices, was repeated for the specific case of *tunnel*-IBC-SHJ solar cells. This time, the parameter d represent the distance between the TCO/metal electrode of the hole contact and the edge of the electron collecting finger (see Fig. 6.9 (a)) and was set equal to 200 µm, 150 µm, 100 µm and 50 µm. Looking at the V_{oc} and FF of the *tunnel*-IBC-SHJ devices in their electrode design (Fig. 6.9 (c)), we observed decreased values only for $d = 50$µm. This is quite different from what was found for the case of IBC-SHJ devices and confirms the presumed advantages of a non-patterned hole collecting layer. The performance for the smallest d is most likely an effect of misalignment problems rather than p-type film thickness tapering. For smaller d values, the J_{sc}s of these devices benefit of an improved carrier collection for shorter minority carrier diffusion paths. This without incurring in V_{oc} and FF losses.

We note that in the case of the *tunnel*-IBC-SHJ cell with $d = 200$µm, the detrimental effect of electrical-shading losses on J_{sc} are enhanced by a low τ_{eff}. In the inset (b) of Fig. 6.9 (b) we report the respective τ_{eff} values, measured at $\Delta n = 5\cdot10^{14}$ cm^{-3} on the solar cell precursors after deposition of all a-Si:H and μc-Si:H layers, to account for this effect.

In overall in the *tunnel*-IBC-SHJ back-contact we can allow wider TCO/metal electrodes

TCO/μc-Si:H(*p*) contact fraction
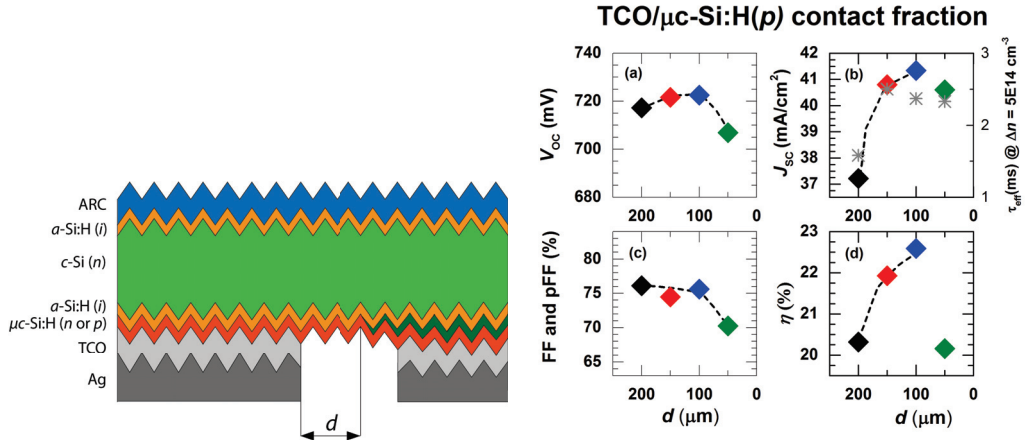
(a) Schematic of the *tunnel*-IBC-SHJ solar cell architecture of this experiment. The parameters *d* indicates the distance between the edge of the TCO/metal electrode of the hole contact and the edge of the μc-Si:H(*n*) electron collector.

(b) Electrical parameters of *tunnel*-IBC-SHJ devices for different values of the parameter *d*. In the right axes of graph (b) we report τ_{eff} values for the respective solar cell precursors after deposition of all a-Si:H and μc-Si:H thin films.

Figure 6.9: Experiment with *tunnel*-IBC-SHJ devices with different widths of the TCO/metal electrode of the hole contact. *d* values of 200 μm, 150 μm, 100 μm and 50 μm correspond to TCO/a-Si:H(*p*) contact fractions of 75 %, 81 %, 88 % and 94 %, respectively.

on the hole contact, without compromising V_{oc} and *FF* values. This is advantageous with respect to the minimization of electrical-shading losses, i.e. the reduction of J_{medium}, and the achievement of best J_{sc} and efficiencies values.

6.6.4   Structural characterization of *tunnel*-IBC-SHJ heterocontacts

Transmission electron microscopy (TEM) was used to assess the microstructure of both a-Si:H(i)^B/μc-Si:H(p)/TCO and a-Si:H(i)^B/μc-Si:H(n)/μc-Si:H(p)/TCO stacks, which were deposited onto mirror-polished c-Si wafers. These samples reproduced the exact structure of hole and electron contacts of our best performing tunnel-IBC-SHJ devices. Using a probe and image and Cs-corrected FEI Titan Themis microscope operated at 200 kV, high-resolution TEM images and scanning TEM (STEM) micrographs obtained using either the high-angle annular dark-field (HAADF) or the annular dark field (DF) detector were acquired to study the microstructure and crystallography of the layers. In addition energy-dispersive X-ray spectroscopy was performed in combination with STEM to provide a chemical analysis of the contact structures. TEM samples were prepared using the conventional focused ion beam (FIB) lift-out technique in a Zeiss NVision 40 microscope. [3]

High-resolution TEM (HRTEM) micrographs and corresponding Fourier transforms and in-

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[3] The structural characterization was done with the help of Q. Jeangros and A. Hessler. Transmission electron microscopy images were taken at the Interdisciplinary Centre for Electron Microscopy (CIME) by Q. Jeangros.
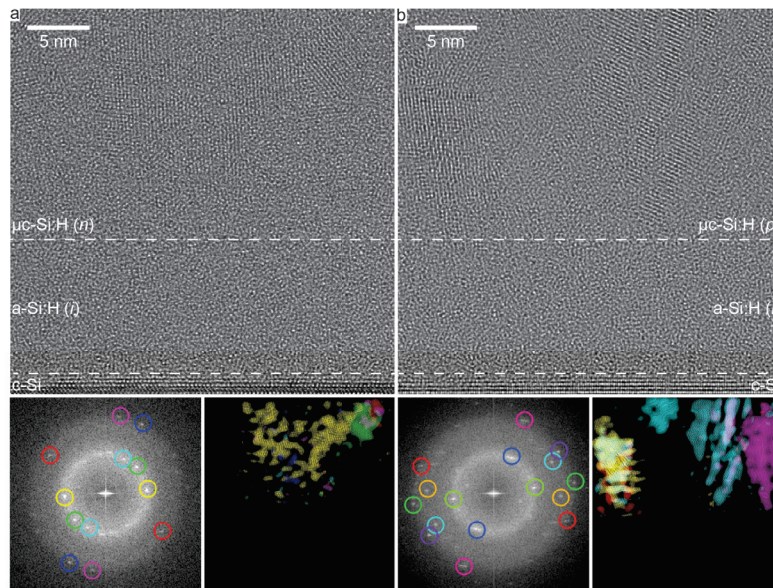
Figure 6.10: High-resolution TEM (HRTEM) micrographs along with corresponding Fourier transforms and colored inverse Fourier transforms of selected reflections of (a) μc-Si:H(n) and (b) μc-Si:H(p) films deposited on a-Si:H(i)^B, itself deposited on mirror-polished c-Si wafers. Reproduced with permission from [Nogay 2016]. Copyright © 2016, IEEE.

verse Fourier transforms of selected reflections shown in Fig. 6.10 demonstrate that both μc-Si:H(n) and μc-Si:H(p) deposited on a-Si:H contain crystallites in an amorphous matrix. In both cases, crystallites exhibit a characteristic conical shape as observed in the virtual dark-field inverse Fourier transform images, with the crystalline fraction increasing along the growth direction (i.e. away from the interface with a-Si:H). Overall, these results confirm the microcrystalline nature of the films, which is achieved despite the extremely small thicknesses (≤ 20 nm). Indeed, inducing crystallinity at these length scales is not trivial. Further insights into strategies for μc-Si:H thin-film growth can be found in [Seif 2016b, Seif 2015, Nogay 2016].

STEM EDX performed on the electron contact of the *tunnel*-IBC-SHJ highlights the concentration profile of Si, P, O and Zn (see Fig. 6.11). P is confined in the 15-nm-thick μc-Si:H(n) electron collecting layer. In addition, O rich regions are observed at every interface of the contact structure, which results from vacuum-break between the deposition of the a-Si:H(i), the μc-Si:H(n) and the μc-Si:H(p) layers. In that regard, the presence of an oxygen-rich layer at the interface of μc-Si:H-based IST junctions, in tandem thin-film silicon solar cells, was actually argued to prove beneficial to carrier transport properties [Rath 1998, Rath 2000]. Its effect of enhancing hole-electron recombination processes may also be beneficial here. Interestingly, and as expected, the concentration of O at the interface between the two μc-Si:H layers is
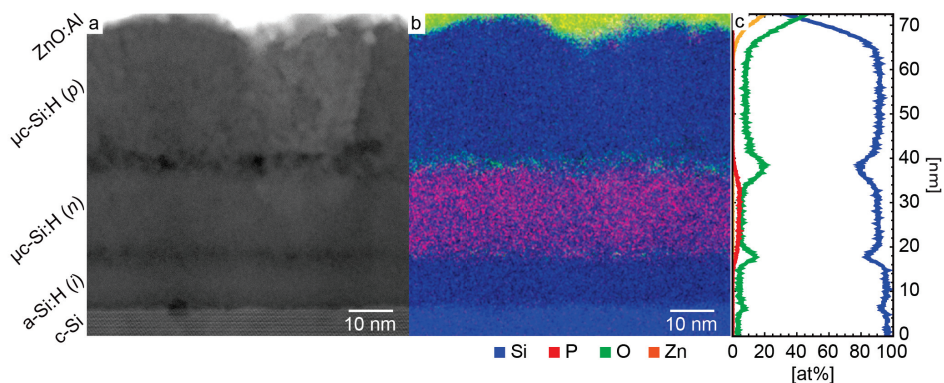
Figure 6.11: (a) STEM HAADF image of the electron contact structure and (b) corresponding EDX map, with (c) the concentration profile of Si, P, O and Zn given in at% . Quantification was performed using the Cliff-Lorimer method [Cliff 1975].

measured to be higher than at the μc-Si:H(n)/a-Si:H(i)^B interface.

A detailed analysis of the crystallography by high resolution STEM micrographs reveals that μc-Si:H(p) grows differently when deposited on a-Si:H(i) film when compared to μc-Si:H(n) (Fig. 6.12). Low magnification STEM DF images reveal that crystallographic features span across the μc-Si:H(p)/μc-Si:H(n) interface (Fig. Fig. 6.12 (a)). At higher magnification, STEM HAADF micrographs acquired with atomic resolution of the μc-Si:H(p)/μc-Si:H(n)/a-Si:H(i) stacks demonstrate that these are crystalline regions that show an epitaxy between the crystals in the μc-Si:H(p) and μc-Si:H(n) below (Fig. 6.12 (b-d)). The μc-Si:H(n) layer hence acts as a nucleation layer for the overlaying μc-Si:H(p). In turn, crystals forming during deposition of μc-Si:H(p), grow directly with a larger cross section, the crystalline cross section that was reached at the end of the μc-Si:H(n). Interestingly, the presence of O at this interface did not prevent this epitaxy. On the other hand, μc-Si:H(p) grown directly onto a-Si:H(i) exhibits characteristic conical shaped crystals originating from, this time, nucleation seeds (Fig. 6.12 (e-g)). Contrary to the case of the μc-Si:H(p) layer grown on μc-Si:H(n), here an extremely thin (< 5 nm) a-Si:H nucleation region is still present.

In conclusion, we argue that the not-homogeneous back-surface resulting from the blanket a-Si:H(i) layer deposition and the patterned μc-Si:H(n) comb can be exploited to achieve a differential growth of the μc-Si:H(p) layer on top of the hole-collecting and IST junction areas. We argue that this structural differences may essentially contribute in forming, simultaneously and by means of the same thin-film material, an efficient hole collector and IST tunnel junction, respectively, without inducing excessive lateral shunts.
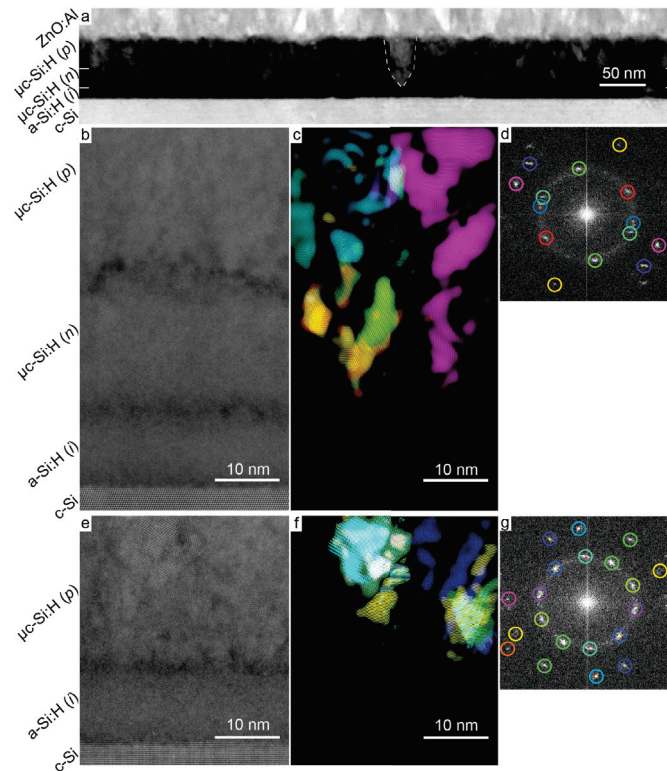
Figure 6.12: (a) STEM DF image of the μc-Si:H(p)/μc-Si:H(n)/a-Si:H(i) electron contact structure highlighting the presence of crystallographic features spanning across the μc-Si:H(p)/μc-Si:H(n)interface; (b) High-resolution STEM HAADF image of the μc-Si:H(p)/ μc-Si:H(n)/a-Si:H(i) structure and (c) corresponding colored inverse Fourier transform obtained from (d) the Fourier transform (computed from (b) excluding the c-Si wafer); (e) High-resolution STEM HAADF image of the μc-Si:H(p)/a-Si:H structure along with (f) colored inverse Fourier transform obtained from (g) the Fourier transform (computed from (e) excluding the c-Si wafer).

6.6.5   Certified *tunnel*-IBC-SHJ device

To validate the excellent device performances achieved with our innovative back-contacted technology we took the opportunity to certify, in an external qualified laboratory, one of our *tunnel*-IBC-SHJ devices. The 1-sun I-V characteristic measured at the CalLab of Fraunhofer ISE in Freiburg, Germany, confirmed our internal measurements. Comparing the parameters measured on our set-up, before shipping, and the certified results we could notice only a small discrepancy in the J_{sc} current values ($< 2\%$). However, this difference is comprised in the measurement uncertainty given by the certification laboratory. In Fig. 6.13 we report the certified 1-sun I-V characteristic and the extracted electrical parameters.
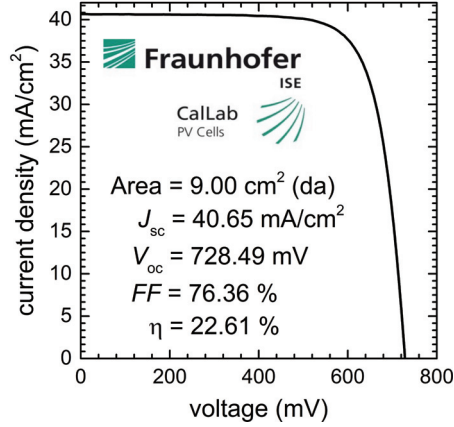
Figure 6.13: 1-sun I-V characteristic of the *tunnel*-IBC-SHJ devices, certified at the qualified laboratory CalLab, Fraunhofer ISE, Freiburg, Germany.

6.6.6 Best *tunnel*-IBC-SHJ device

Combining in an optimized *tunnel*-IBC-SHJ device the findings of section 6.6.2, 6.6.3 and the layer/interfaces observed in section 6.6.4, we achieved a best-device conversion efficiency of 22.9 %. This best device includes the a-Si:H(i)^B film of section 6.6.2 in its heterocontacts and the developed "all μc-Si:H-based" IST junction of section 6.6.1. This heterocontact configuration allows to limit R^N_{series} losses and achieve improved *FF* values. At the front, low parasitic absorption losses were set employing the J_{sc}-optimized a-Si:H(i)/a-SiN$_x$:H film stack. Finally, electrical-shading losses were inhibited by sufficiently-high τ_{eff}, after the blanket μc-Si:H(p) deposition, and a wide TCO/metal electrode at the hole contact. The control over the degradation of the $\tau_{eff}(\Delta n)$ curves, after μc-Si:H(p) deposition, is essential to reach high conversion efficiencies. Based on our experiments in *tunnel*-IBC-SHJ devices, we individuate two important factors influencing the entity of such degradation: (1) the quality of the initial passivation, before μc-Si:H layer depositions, and (2) the a-Si:H(i)^B film thickness. Further investigations, to understand the nature of this effect are still ongoing. In Fig. 6.14 (a) we report 1-sun I-V characteristic, suns-V_{oc} curve and low-light I-V characteristic measured on this best cell. The cell show a V_{oc} of 728 mV, a J_{sc} of 40.8 mA cm^{-2} and a *FF* of 77.1 %. This best *FF* value results mainly from a low series resistance $R^N_{series} = 1.05\,\Omega\,cm^2$, which determines $\Delta FF_{R_{series}} = 5.4$ %, and $\Delta FF_{J_0(n\neq1)} = 2.4$ %; the measured *pFF* values is of 82.0 %.

As a result of the low $\Delta FF_{R_{series}}$ loss, in this best cell the 1-sun *FF* is higher than the *FF* extracted from the low-light I-V characteristic. For lower illuminations, i.e. lower current densities, the *FF* do not benefit of the reduced series resistance loss. The prevailing effects are instead the reduction of FF_0, due to the lower V_{oc}, and the higher shunt-resistance and recombination losses. In the graph of Fig. 6.14 (b), we report illumination dependent *FF* values measured for this best *tunnel*-IBC-SHJ and the device IBC-SHJ[1] and IBC-SHJ[2] of chapter 4. The lower series resistances of IBC-SHJ[2] compared to IBC-SHJ[1], and of the best *tunnel*-IBC-SHJ compared to IBC-SHJ[2], move the maximum of the $FF(J_{sc}/J_{sc}^{1\text{-}sun})$ curves closer to 1-sun.
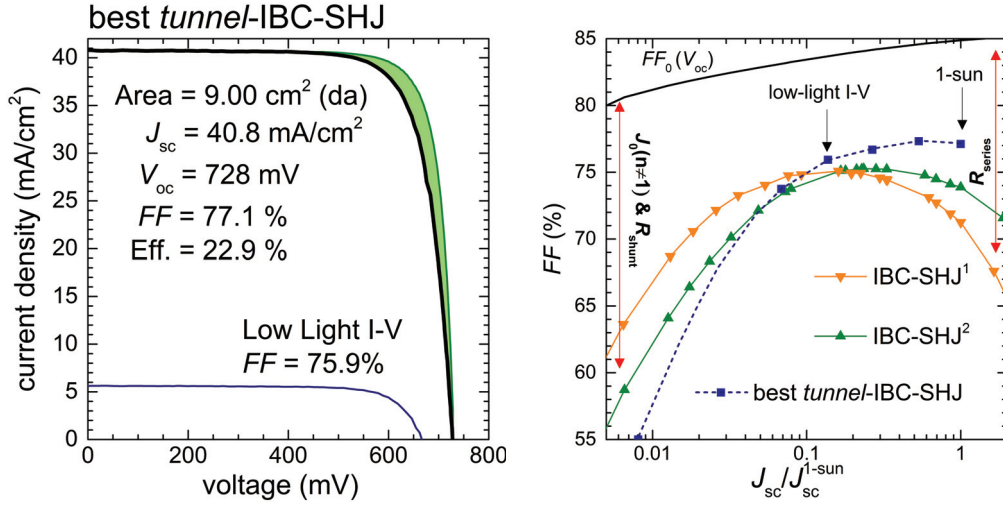
(a) Best *tunnel*-IBC-SHJ pseudo I-V, 1-sun I-V and low-light I-V characteristics indicated by the green, black and blue solid lines, respectively. The electrical parameters extracted from the 1-sun I-V characteristic and the low-light I-V *FF* are reported in the graph. The light green area indicates the amount of *FF* losses due to charge-carrier transport. The *pFF* value measured for this best *tunnel*-IBC-SHJ is of 82% .

(b) Illumination-dependent *FF* measurements for the best *tunnel*-IBC-SHJ, IBC-SHJ[1] and IBC-SHJ[2] solar cells. The low $R^{\mathrm{N}}_{\mathrm{series}}$ value of this best device, achieved thanks to the use of μc-Si:H-based heterocontacts, translates in decreasing *FF* for illumination intensities down to about 0.1 suns. The FF_0 limit, calculated for $n = 1$ and the V_{oc} values of IBC-SHJ[2], is indicated for comparison with a solid black line.

Figure 6.14: Electrical characterization results for our best *tunnel*-IBC-SHJ device.

6.6.7 Series resistance losses in the *tunnel*-IBC-SHJ device

Similarly as in section 4.5.6, we now assess the importance of each series resistance contributor in our *tunnel*-IBC-SHJ solar cells. Again, based on the model discussed in chapter 4, we can match our simulation and experimental results choosing appropriate values for $(\rho_c)_n$ and $(\rho_c)_p$. We consider here the case of our lowest-$R^{\mathrm{N}}_{\mathrm{series}}$ *tunnel*-IBC-SHJ device, with $R^{\mathrm{N}}_{\mathrm{series}} = 0.75\,\Omega\,\mathrm{cm}^2$. The model input parameters are set for this specific solar cell, which is the device of the experiment of section 6.6.3, with $d = 100\,\mu\mathrm{m}$. We note that the value of $(\rho_c)_n$, for *tunnel*-IBC-SHJ devices, refers to the whole electron contact with embedded IST junction and was measured in the experiment of Fig. 6.3. With $(\rho_c)_n = 0.008\,\Omega\,\mathrm{cm}^2$ and assuming $(\rho_c)_p = 0.100\,\Omega\,\mathrm{cm}^2$ we computed, with our model, a series resistance $R^{\mathrm{N}}_{\mathrm{series}} = 0.75\,\Omega\,\mathrm{cm}^2$.

In Fig. 6.15, we show the simulated series resistance components for this lowest-$R^{\mathrm{N}}_{\mathrm{series}}$ *tunnel*-IBC-SHJ device compared to the case of IBC-SHJ[2]. The contribution associated with transport at the heterocontacts is practically halved and $\Delta FF_{R_{\mathrm{series}}}$ accounts for only a 4 % *FF* absolute loss. This value is finally in line with the case of the two-side-contacted FHC SHJ devices discussed in chapter 4.

We remark on the fact that for very low ρ_c values, the series resistance model used to describe our IBC-SHJ devices should be corrected as follows. Extremely low ρ_c values associates to
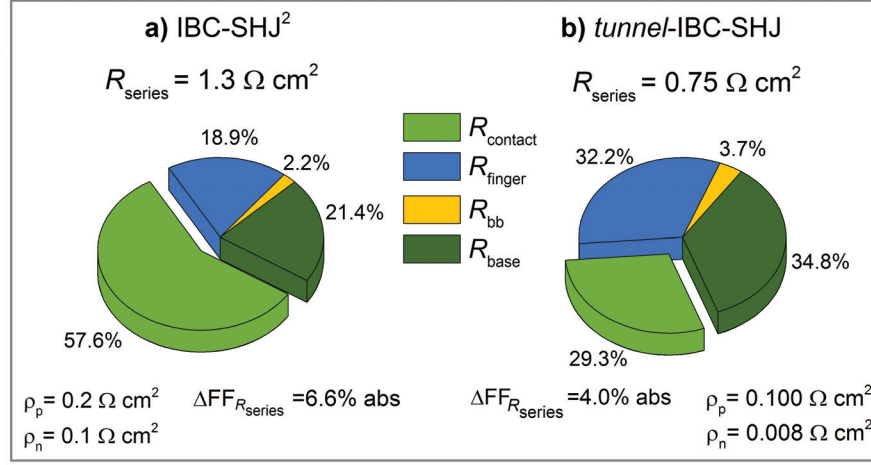
Figure 6.15: Simulated series-resistance contributions for an IBC-SHJ devices with R_{series}^N equal to that measured for our IBC-SHJ[2], or the well-passivated IBC-SHJ device of Table 6.4, (a) and for the case of our lowest-R_{series}^N *tunnel*-IBC-SHJ solar cell.

transfer lengths (L_t) lower than half of the hole and electron contact finger widths. In this case the series resistance components $\left(R_{contact}^N\right)_p$ and $\left(R_{contact}^N\right)_n$ should not be calculated considering the whole hole and electron contact areas—see equations A.4—but rather the portion defined by $L_t\left(\rho_c\right)$. It becomes:

$$\left(R_{contact}^N\right)_p = \frac{\left(\rho_c\right)_p}{2\left(L_t\right)_p na} \cdot A_d \quad and \quad \left(R_{contact}^N\right)_n = \frac{\left(\rho_c\right)_n}{2\left(L_t\right)_n na} \cdot A_d, \tag{6.1}$$

where n is the number of fingers, of length a, in the hole or electron comb, respectively. A_d is the designated area of 9 cm^2, $\left(L_t\right)_p = \sqrt{\left(\rho_c\right)_p/R_{sheet}^{wafer}}$ and $\left(L_t\right)_n = \sqrt{\left(\rho_c\right)_n/R_{sheet}^{wafer}}$, with R_{sheet}^{wafer} equal to the wafer sheet resistance. Similarly as in equation A.1, we include photoconductance effects, in the calculation of R_{sheet}^{wafer}, with the expression $R_{sheet}^{wafer} \cong (\rho_w N_D)/(N_D+\Delta_n) \cdot 1/t$, where ρ_w is the wafer resistivity in the dark, t its thickness and N_D the donor-dopant density. The excess minority carrier density Δ_n at mpp, is calculated as described in the appendix A.1. With these new expression we can correct our model for low ρ_c values. The correction is applied only for $\left(L_t\right)_n \le 0.04$ cm—i.e. $\left(\rho_c\right)_n \le 0.11\,\Omega\,\mathrm{cm}^2$—and $\left(L_t\right)_p \le 0.07$ cm—i.e. $\left(\rho_c\right)_p \le 0.34\,\Omega\,\mathrm{cm}^2$—which correspond to diffusion lengths smaller than half of the electron and hole contact finger widths (namely w_n and w_p in the appendix A.1), respectively.

In Fig. 6.16, for this lowest-R_{series}^N *tunnel*-IBC-SHJ device considered in Fig. 6.15, we give the corrected (simulated) values of R_{series}^N and maximum attainable *FF*, as a function of $\left(\rho_c\right)_p$ and $\left(\rho_c\right)_n$. For $\left(\rho_c\right)_p > 0.34\,\Omega\,\mathrm{cm}^2$ and $\left(\rho_c\right)_n > 0.11\,\Omega\,\mathrm{cm}^2$ we used the equations A.4, as the whole contact area again contribute to carrier transport. This contour plot, compared to Fig. 4.14, shows the effect of lower L_t values at low ρ_c, which inhibit the reduction in R_{series}^N.

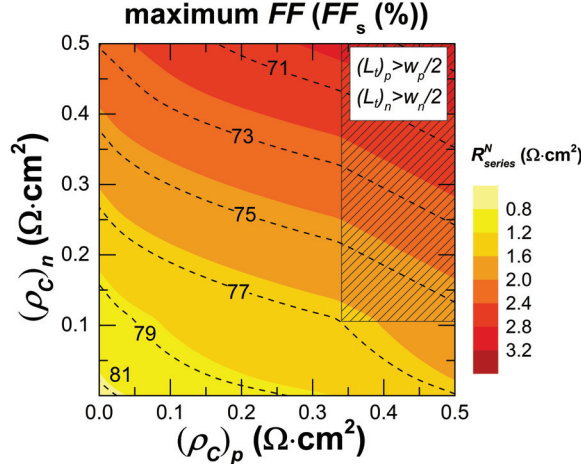With this upgraded model we can now examine the limiting case of a device with nearly-perfect

Figure 6.16: Simulated normalized series resistance $\left(R_{\text{series}}^{\text{N}}(\Omega\,\text{cm}^2)\right)$ in our lowest-$R_{\text{series}}^{\text{N}}$ *tunnel*-IBC-SHJ device and associated maximum attainable *FF* ($FF_s(\%)$), as a function of heterocontact specific contact resistivity $(\rho_c)_p$ and $(\rho_c)_n$. Differently from the case of Fig. 4.14, the model used here account for carrier collection, below the contacts, over a region wide as the transfer length L_t. The patterned area indicates the region where $(\rho_c)_p \geq 0.11\,\Omega\,\text{cm}^2$ and $(\rho_c)_n \geq 0.34\,\Omega\,\text{cm}^2$. For these values, the respective L_t are larger than half of the hole and electron contact finger widths, respectively, and equations A.4 are again valid. The area occupied by the contacts, in this back-contact design, correspond to about $\sim 55\%$ and $\sim 30\%$ of the cell back-surface (excluding the bus bar area), for the case of the hole and electron contacts, respectively; the pitch is of 2.6 mm. FF_s is calculated in the hypothesis of a single diode with $n = 1$ and *FF* losses due to carrier transport as from $R_{\text{series}}^{\text{N}}$ values. Dashed contour lines delimitate regions of FF_s values, whereas the color map is used to represent $R_{\text{series}}^{\text{N}}$ values.

heterocontacs. Assuming, for instance, $(\rho_c)_n \cong (\rho_c)_p \cong 1 \cdot 10^{-3}\,\Omega\,\text{cm}^2$ we predict $R_{\text{series}}^{\text{N}} = 0.60\,\Omega\,\text{cm}^2$, in the case in which L_t is taken into account. Without considering L_t, we would have found $R_{\text{series}}^{\text{N}} = 0.54\,\Omega\,\text{cm}^2$, which is underestimated by about 10 %. Hence, the effect of L_t on the overall device $R_{\text{series}}^{\text{N}}$ is not a major effect. However, this effect implies that further improvements of the heterocontact transport properties will be dampened by lower L_t. To increase further the *FF* of our devices we should now consider also other losses than those due to carrier transport at the heterocontacts. In section 7.2, we discuss the developments which may contribute to further enhance the *FF*s of our *tunnel*-IBC-SHJ solar cells.

6.7 Conclusion

In this chapter we unveiled the development of a simple and innovative back-contacted solar cell concept, up to efficiencies of almost 23%. The proposed technology, the so-called *tunnel*-IBC-SHJ technology, suppresses the need to pattern one of the carrier collecting layer which led to a strong process simplification and devices with a robust architecture. In addition, with respect to the problems individuated in our IBC-SHJ solar cells of chapter 4, it has the following

advantages: (1) a homogeneously-thick hole collecting layer and (2) optimized μc-Si:H- based heterocontacts, with low losses due to carrier transport. The enabling factor for such solar cell concept has been the development of a suitable IST junction. Eventually, this brought us to the demonstration of a best *tunnel*-IBC-SHJ device with a certified conversion efficiency of 22.9%, a J_{sc} of 40.8 mA cm^{-2} and a V_{oc} of 728 mV. We believe that the presented *tunnel*-IBC-SHJ concept represents a big step forwards for the solution of the typical complexity linked with back-contacted device fabrication.

7 | Summary and perspectives

This chapter discusses the best back-contacted silicon heterojunction solar cells achieved in this thesis, compared to other record c-Si devices, and delineates future developments of the *tunnel*-IBC-SHJ technology.

7.1 Summary of back-contacted SHJ solar cell results

In this thesis we demonstrate that high-efficiency back-contacted silicon heterojunction solar cells can be fabricated by means of unsophisticated patterning processes. With only two patterning steps and avoiding the use of photolithography, which is not a viable technique in the photovoltaic industry, we were able to fabricate back-contacted solar cells with a conversion efficiency of almost 23 %. These solar cells demonstrate conclusively the potential of the back-contacted architecture, which leads to high J_{sc} values.

The back-contacted solar cell architectures developed in this thesis are the IBC-SHJ architecture (chapters 3,4, 5 and Fig. 7.1 (a)) and the *tunnel*-IBC-SHJ architecture (chapter 6 and Fig. 7.1 (b)). Below, we list the salient points of these technologies.

- **IBC-SHJ** architecture (Fig. 7.1 (a))

  ⬦ Transparent a-Si:H(*i*)/a-SiN$_x$:H front stack with excellent surface passivation and low reflectance.

  ⬦ Interdigitated electron and hole-collecting a-Si:H combs, with no gap in between, patterned via *in-situ* shadow masking.

  ⬦ Interdigitated TCO/metal electrodes patterned via hot melt inkjet printing.

- ***tunnel*-IBC-SHJ** architecture (Fig. 7.1 (b))

  ⬦ Transparent a-Si:H(*i*)/a-SiN$_x$:H front stack with excellent surface passivation and low reflectance.

Table 7.1: Best-performing back-contacted SHJ solar cells fabricated in the framework of this thesis and of the collaboration between EPFL and CSEM.

Back-contacted SHJ devices (EPFL-CSEM)				
Solar cell	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
IBC-SHJ (this work) *in-situ* shadow masking and inkjet printing	725	40.7	75.6	22.3
tunnel-IBC-SHJ [Tomasi 2016a] μc-Si:H-based heterocontacts and IST junction	728	40.8	77.1	22.9

⬦ Electron-collecting μc-Si:H(n) comb patterned via *in-situ* shadow masking.

⬦ Blanket μc-Si:H(p) thin-film forming, simultaneously, a hole-collecting comb on top of the a-Si:H(i) film and an IST junction on top of the electron-collecting μc-Si:H(n) comb.

⬦ Interdigitated TCO/metal electrodes patterned via hot melt inkjet printing.

7.1.1 Best-performing certified SHJ devices at EPFL and CSEM

Here, we propose a fair technological comparison, considering only certified solar cell results, obtained within the collaboration between EPFL and CSEM. We included the certified *tunnel*-IBC-SHJ device of chapter 6, the reference FHC SHJ solar cell [Descoeudres 2013], the best FHC SHJ solar cell with a Cu-plated front grid and indium-zinc-oxide (IZO) as front TCO [Geissbuhler 2015a] and the best MoO$_x$-based FHC SHJ solar cell [Geissbuhler 2015b]. For reference, the cross-sectional schematics of these device architectures are shown in Fig. 7.1 (b) and (c).

The V_{oc} of all these solar cells is very similar, in the narrow range of 725 mV to 729 mV. This is due to analogous level of passivation and similar wafer thicknesses of about 250 µm.

The FF of the certified *tunnel*-IBC-SHJ is more than 1 % lower, compared to the two-side-contacted devices. This despite the use of the best contacting materials and the advanced μc-Si:H-based heterocontacts. This remaining difference is due to an higher FF recombination loss, which caps the value of pFF of our best back-contacted solar cells to about 82 %. Interestingly, the solar cell with by far the highest FF, of 80.4 %, is that using the novel MoO$_x$-based SHJ hole contact. In this technology the a-Si:H(p) layer, on top of the a-Si:H(i) film, is replaced by a thin-film of MoO$_x$.

The J_{sc} of the *tunnel*-IBC-SHJ device surpasses those of the two-side-contacted devices by more than 1 mA cm^{-2}. Overall, this J_{sc} gain offsets the lower FF and leads to a slightly higher efficiency. The use of a Cu-plated grid and a highly-transparent TCO material, at the front of a two-side-contacted solar cell, reduces shadowing and parasitic absorption losses by roughly 0.5 mA cm^{-2}. However, this is not sufficient to equal the J_{sc} of a back-contacted device, with

Table 7.2: Best certified two-side-contacted and back-contacted SHJ solar cells fabricated in the framework of the collaboration between EPFL and CSEM.

Best-certified SHJ devices (EPFL-CSEM)				
Solar cell	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
two-side-contacted				
FHC SHJ* [Descoeudres 2013] Ag screen-printed front grid	727	38.9	78.4	22.1
FHC SHJ* [Geissbuhler 2015a] Cu-plated front grid and IZO	727	39.4	77.9	22.3
MoO$_x$-based FHC SHJ* [Geissbuhler 2015b] Cu-plated front grid	725	38.6	80.4	22.5
back-side-contacted				
tunnel-IBC-SHJ * [Tomasi 2016a] μc-Si:H-based heterocontacts and IST junction	729	40.7	76.4	22.6

* Certified by CalLab of Fraunhofer ISE

no front grid and an highly-transparent front stack. For the MoO$_x$-based FHC SHJ solar cell, the interaction TCO-MoOx and parasitic absorption in the blue part of the spectrum may be the causes of the moderate J_{sc} value [Geissbuhler 2015b].

We remark on the fact that, the certified two-side-contacted devices shown in Table 7.2, are not the best current solar cells achieved in the collaboration between EPFL and CSEM. Yet, they are significant with respect to our technological analysis. Current record two-side-contacted 4-cm^2 devices fabricated at CSEM reach the efficiency of 22.9%, with $V_{oc} = 729$ mV, $J_{sc} = 38.4$ mA cm^{-2} and $FF = 81.6$ %. On the 6-in format, and with a 150-um-thick wafer, the record efficiency is of 22.8%, with $V_{oc} = 736$ mV, $J_{sc} = 38.8$ mA cm^{-2} and $FF = 79.8$ %, measured with GridTouch®.
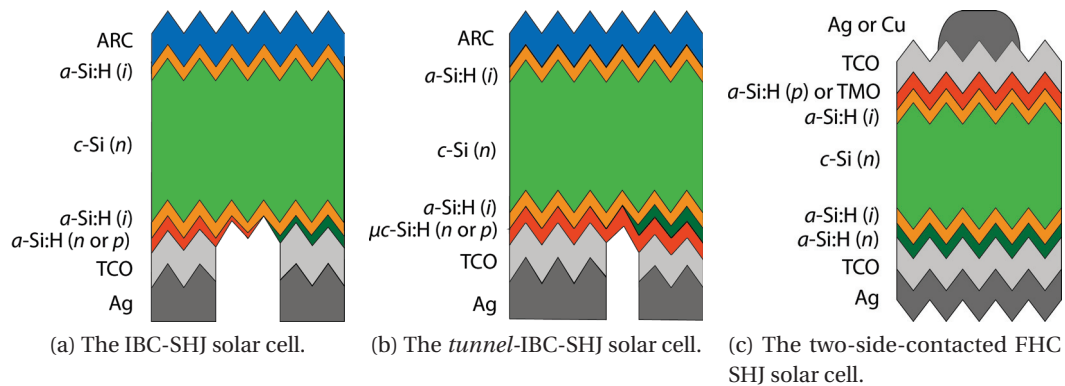

(a) The IBC-SHJ solar cell. (b) The *tunnel*-IBC-SHJ solar cell. (c) The two-side-contacted FHC SHJ solar cell.

Figure 7.1: Cross-sectional schematics for the SHJ solar cells considered in the discussion.

Table 7.3: Best-reported two-side-contacted and back-contacted SHJ solar cells. The result of [Masuko 2014] is the current world-record conversion efficiency for c-Si wafer-based single-junction devices.

Best-reported SHJ solar cells				
Solar cell	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
two-side-contacted SHJ* [Adachi 2015]	738	40.8	83.5	25.1
IBC-SHJ^T [Masuko 2014]	740	41.8	82.7	25.6

* Certified by CalLab of Fraunhofer ISE, ^{T} Certified by AIST

World-record c-Si devices

We now look in Table 7.3 at the world-record large-area c-Si single-junction solar cells with a back-contacted and a two-side-contacted architecture, respectively. Interestingly, both solar cells make use of the SHJ technology and mirror the differences observed in our comparison of Table 7.2. The two record devices show similar V_{oc} values, indicating similar passivation quality and similar wafer thicknesses of 160 μm [Adachi 2015] and 150 μm [Masuko 2014]. The higher J_{sc} of the back-contacted device offsets the lower FF and leads to an higher efficiency. The J_{sc} difference demonstrates, again, the fundamental superiority of the back-contacted architecture. The two-side-contacted device, despite the Cu-plated front grid, shows a J_{sc} which is $1\,\mathrm{mA\,cm^{-2}}$ lower than in the device of [Masuko 2014]. This J_{sc} loss of $1\,\mathrm{mA\,cm^{-2}}$ corresponds to about 2.5 % of the total J_{sc}. Front grids featuring a smaller area fraction are difficult to fabricate and the *handicap* of the lower J_{sc}, in the two-side-contacted device, is likely to remain also in the future.

7.2   Perspectives

Among the two back-contacted SHJ architectures developed in this thesis, we believe that the *tunnel*-IBC-SHJ architecture is by far the most interesting and promising. Here, we chose to discuss the future developments of this technology. Overall, we believe that its potential has not been fully expressed yet and that further work will bring soon to higher efficiencies.

7.2.1   Limitations and possible improvements of the *tunnel*-IBC-SHJ solar cell

The *FF* of our best *tunnel*-IBC-SHJ solar cells is moderate and its improvement should be still the prime objective. **FF losses** due to **charge-carrier transport** were dominant, over *FF* recombination losses, in our first back-contacted solar cells. They accounted for a *FF* loss up to 10 % absolute. This was mostly due to transport losses caused by high contact resistance at the heterocontacts (see IBC-SHJ[1] in Fig. 4.16 (a)). By heterocontact engineering these losses were reduced. Now, in our lowest-R_{series} *tunnel*-IBC-SHJ solar cell, the series resistance is equally distributed between **contact resistance**, resistance in the **TCO/metal electrode** and in the bulk of the **wafer** (see Fig. 6.15 (b)). Overall, it accounts for only a 4 % absolute *FF* loss.

A further improvement of the contact resistance at the heterocontacts is possible, but it is most likely a tough challenge.

The implementation of thicker metal electrodes looks urgent. In back-contacted SHJ devices overcoming the limit of 25 % [Masuko 2014, Nakamura 2014], special cares are taken to eliminate charge-carrier transport losses in the electrodes. The device of [Masuko 2014] uses a Cu-plated electrode, thick several tens of µm, and the one of [Nakamura 2014] is coupled with a printed circuit board when measuring the I-V characteristic. We carried out preliminary experiments to develop thick Ag screen-printed IBC electrodes with encouraging results. A Cu-plated IBC electrode, as shown in section 3.3.4, is also a viable option.

Eventually, a modified IBC design, with a reduced pitch, is a possible way to reduce the series-resistance component due to the lateral conduction in the wafer. However, it should be noted that a reduction in IBC pitch leads to an increase of the edge-to-area ratio for the carrier-collecting combs. This, in case of imperfect edges, may detrimentally affect the *FF* and offset the benefit of a lower IBC pitch. This problem, eliminated for the blanket μc-Si:H(p) film, may still play a role for the μc-Si:H(n) layer. In the development of our *tunnel*-IBC-SHJ technology we fabricated *tunnel*-IBC-SHJ devices with a pitch of 3.5 mm, 2.6 mm and 1.4 mm. The highest *FF* was achieved with the pitch of 2.6 mm and in a fair comparison we detected a 1.5 % absolute lower *FF* for the solar cell with pitch of 1.4 mm. We note that the sharpness of the μc-Si:H(n) thin-film edges may be improved choosing different masks (thickness and material) or PECVD deposition regimes. Alternatively, the μc-Si:H(n) film may be replaced by a transition metal oxide (TMO) film with sharper edges (see discussion in section 7.2.2).

Finally, a reduction of series resistance in the bulk of the wafer is possible also via the improvement of the passsivation quality, i.e. increasing the excess minority carrier density at mpp, or with wafers of lower resistivities.

In our best *tunnel*-IBC-SHJ solar cells the remaining *FF* difference with two-side-contacted SHJ solar cells is due to higher **FF recombination losses**. Our high-efficiency devices show *pFF* values rarely overcoming the limit of 82 %, whereas in two-side-contacted devices they can be, routinely, over 84 %. We note that this does not looks a fundamental problem of our back-contacted SHJ technology. High *pFF* were achieved also in certain back-contacted SHJ devices, as for instance IBC-SHJ[1] in section 4.5.4 or *tunnel*-IBC-SHJ[A] in section 6.6.2, but were always coupled with high *FF* losses due to carrier-transport, which led to lower final *FF*. This reminds of the complexity associated with carrier-selective passivating contact technologies, in which passivation and charge-carrier transport properties are fundamentally entangled.

Finally, to increase further *FF* values at the record level of 83 %, the theme of achieving high passivation at mpp, recently raised by [Adachi 2015], is decisive. However, this is a theme that concerns the SHJ technology in general, including our two-side-contacted devices. Recent improvements of *FF* obtained by CSEM, could contribute to such improvements.

The **J_{sc}** of our back-contacted SHJ solar cells is about 1 mA cm^{-2} lower than for the record

device of [Masuko 2014]. We believe that a first step to fill this gap is the elimination of the **electrical-shading loss** (see the discussion in section 4.6). In our analysis this loss is associated to the J_{sc}-loss term J_{medium}, which was found to account for a loss of $0.5\,\mathrm{mA\,cm^{-2}}$ in our highest-J_{sc} IBC-SHJ solar cell. A way to reduce J_{medium}, is by reducing the pitch of the IBC design, with the problems discussed above. Alternatively, a reduction can be achieved by moving the edge of the a-Si:H(p)/TCO electrode closer to edge of the electron-collecting contact or by reducing the width of the fingers of the electron-contact. The first option, pursued in section 6.6.3, requires a perfectly flat hole-collecting film and optimum alignment capabilities. The second option requires an highly optimized electron contact, to prevent losses due to carrier transport through the reduced contact area. We note that an improved passivation level would also reduce electrical-shading losses. With respect to the **parasitic absorption loss** in the front stack the use of a passivating dielectric layer, such as a-SiN$_x$:H, a-SiO$_x$:H, Al$_2$O$_3$ or an hybrid solution as that proposed by [Wan 2015], would be beneficial. Finally, with respect to the J_{sc} loss in the long wavelength region, highly-transparent TCOs with low free-carrier absorption, may bring an interesting contribution. We note that comparing TCO films in the back electrode of our IBC-SHJ devices (see section 4.5.3), the J_{sc}-loss term J_{long} varied of more than $1\,\mathrm{mA\,cm^{-2}}$. The best device was that with ZnO:Al in the back-contact, because of the higher *FF*, but higher J_{sc} were achieved for ZnO:B. Combining a good TCO contact layer with the optical properties of ZnO:B would already improve our device.

7.2.2   The opportunity of TMO-based carrier-selective passivating contacts

Recently, transition metal oxides (TMO) emerged as promising high- and low-WF materials to form hole- and electron-collecting contacts. A possible approach, is to combined them with a passivating a-Si:H(i) thin film to form a TMO-based SHJ contact. This class of novel carrier-selective passivating contacts, is highly interesting with respect to applications in back-contacted SHJ architectures. The motivations are specified below.

- TMO thin-films may be promising candidate materials to replace one or both the doped μc-Si:H layers in the *tunnel*-IBC-SHJ architecture.

- TMOs are typically easily etched, compared to a-Si:H thin films. This may help the development of etching solutions with high selectivity between the TMO and the a-Si:H.

- TMO thin-films deposited by thermal evaporation and *in-situ* shadow masking may show sharper edged than a-Si:H thin-films deposited via PECVD.

In an earlier work, it was found that a TiO$_x$ thin film, interposed between the a-Si:H(p) and the a-Si:H(n) layer of an a-Si:H/a-Si:H tandem thin-film device, provides beneficial effects on the solar cell performance [Sakai 1988]. This is promising with respect to the possibility to form efficient tunnel junction with TMO materials.

The sharpness of an evaporated MoO$_x$ thin-films, patterned via *in-situ* shadow masking, was already verified by Raman profilometry measurements (see the discussion in 3.3.1 [Ledinský 2016]). We found sharper edges compared to a-Si:H or μc-Si:H PECVD thin-films.

Overall, a TMO-based electron collector looks to be a good candidate to replace the patterned μc-Si:H(n) thin-film in our *tunnel*-IBC-SHJ. It could be patterned either by hot melt inkjet printing and wet-chemical etching or still by *in-situ* shadow masking, offering improved edge sharpness. This may allow to decrease the pitch of our IBC design, reducing electrical shading losses and the series resistance contribution of the wafer. In preliminary experiments, we already fabricated MoO$_x$-based back-contacted SHJ devices, by means of original and practical fabrication processes, and with encouraging results.

7.2.3   The fabrication process of *tunnel*-IBC-SHJ solar cells

Hot melt inkjet printing combined with wet-chemical etching, was recognized as an excellent technique for the fabrication of interdigitated electrodes. This approach is fast, accurate, reliable and can easily be adapted to realize different IBC designs. In addition, if an IBC design with smaller features will be required, it won't be a limitation. Industrial equipments, based on the same inkjet technology used in the thesis, are commercially available and hot melt inkjet printing patterning, in mass-production, looks a viable option.

In-situ shadow masking of a-Si:H thin-film depositions was shown to be a suitable technique for device fabrication, despite being characterized by certain limitations. Thin-film patterned with this approach show imperfect edges and not uniform thicknesses. If an IBC design with smaller features will be required, the imperfections at the edges of the patterned fingers may become important and block further device improvements. The use of *in-situ* shadow masking in industrial manufacturing seems feasible but might require hardware modifications to the current PECVD equipments.

The *tunnel*-IBC-SHJ makes the overall approach realistic for industrial production. Yet, the individuation of an alternative approach to pattern the μc-Si:H(n) layer could be beneficial for the technology. The unexplored possibilities offered by TMO-based SHJ contacts, with respect to this last problem, look promising.

A Series-resistance components of IBC-SHJ and FHC SHJ devices

A.1 IBC-SHJ devices

The interdigitated back contact consists of two combs, each with n fingers of length a and width w, which half-pitch is indicated with the parameter b. In the text below, when present, subscripts n and p specify, respectively, the n-type and the p-type comb (see Fig. A.1). The designated cell area—see equations A.2, A.3 and A.4—is indicated with the parameter A_d. Series resistance contributions are normalized to the designated area $A_d = 9 \text{ cm}^2$.

Equation A.1 for the normalized series resistance bulk component is taken from [Verlinden 2012]. For substrate we assume an n-type c-Si wafer of thickness t, resistivity ρ_w and with a donor-dopant density equal to N_D. The solar cell injection level at mpp (Δn) is calculated from V_{mpp} of the resistance-free I-V curve, measured by suns-V_{oc}, according to [Sinton 1996]. The pre-factor $(\rho_w N_D)/(N_D + \Delta n)$ in A.1 accounts for photo-conductance effects in the wafer.

$$R_{bulk}^N \cong \frac{\rho_w N_D}{N_D + \Delta n} \left(\frac{b \cdot \left(b - \frac{w_n}{2} \right)}{3t} \right) \tag{A.1}$$

The expressions for the normalized metal grid series resistance component—see equations A.2 and A.3—of each comb are derived as reported in [Meier 1984]; the calculated expression for the power loss is divided by the square of the light-generated current $I_L^2 = (J_L \cdot A_d)^2$ and then multiplied by the normalization area A_d. The TCO/metal stack is considered as a sole conduction medium whose sheet resistance equals the measured value $R_{\text{sheet}}^{\text{metal/TCO}} = 0.02 \Omega/\square$. The pre-factor in A.3 accounts for three current-extraction points along each bus bar (of width w'), as in our measurement setup.

$$R_{finger}^N = \frac{4}{3} a^3 b^2 n \left(\frac{R_{\text{sheet}}^{\text{metal/TCO}}}{w} \right) \cdot \frac{1}{A_d} \tag{A.2}$$
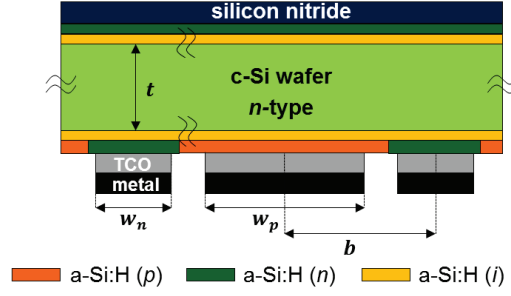
Figure A.1: Geometry of the back contact: side view. Adapted with permission from [Tomasi 2014a]. Copyright © 2014, IEEE.

$$R_{bb}^{N} = \frac{2}{27} a^2 n^3 b^3 \left(\frac{R_{\text{sheet}}^{\text{metal/TCO}}}{w'} \right) \cdot \frac{1}{A_d} \tag{A.3}$$

The normalized resistance components associated with the heterocontacts are calculated according to A.4. Modifying A.4 to account for carrier collection, below the contacts, over a region wide as the transfer length $L_t(\rho_c)$, our conclusions of chapters 4 and 6 remain unchanged. For a more detailed discussion on the contribution of L_t see also 6.6.7.

$$\left(R_{contact}^{N} \right)_p = \frac{(\rho_c)_p}{w_p na} \cdot A_d \quad ; \quad \left(R_{contact}^{N} \right)_n = \frac{(\rho_c)_n}{w_n na} \cdot A_d. \tag{A.4}$$

For the IBC-SHJ solar cell, the normalized total series resistance $\left(R_{\text{series}}^{\text{N}} \right)$ is calculated according to:

$$R_{\text{series}}^{\text{N}}(\text{IBC-SHJ}) = R_{\text{bulk}}^{\text{N}} + \left(R_{\text{finger}}^{\text{N}} + R_{\text{bb}}^{\text{N}} + R_{\text{contact}}^{\text{N}} \right)_n + \left(R_{\text{finger}}^{\text{N}} + R_{\text{bb}}^{\text{N}} + R_{\text{contact}}^{\text{N}} \right)_p. \tag{A.5}$$

A.2   FHC SHJ devices

In our FHC SHJ solar cells, the metal front-grid electrode consist of n metal fingers of resistivity ρ_f, width w_f, thickness t_f and length a, departing from both sides of a single central bus bar (see also Fig. A.2). The grid half-pitch is indicated as b and the bus bar width and thickness are indicated as w' and t', respectively. Series resistance contributions are normalized to the designated area $A_d = 4 \text{ cm}^2$.

Equation A.6 for the normalized series resistance bulk component is taken from [Meier 1984] and adapted including substrate photo-conductivity effects, similarly as in [Verlinden 2012].
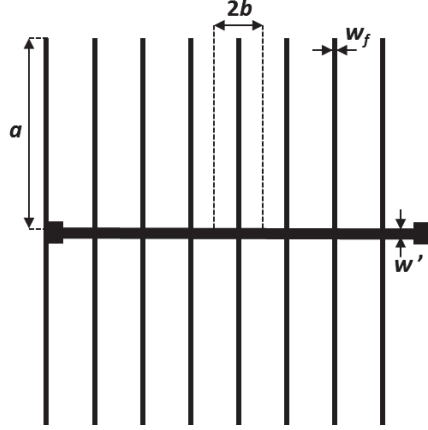
Figure A.2: Metal front-grid electrode: top view.

As substrate we assume a n-type c-Si wafer of thickness t and resistivity ρ_w, with a donor-dopant density equal to N_D. The solar cell injection level at mpp (Δn) is calculated from V_{mpp} of the resistance-free I-V curve, measured by suns-V_{oc}, according to [Sinton 1996].

$$R_{bulk}^N \cong \frac{\rho_w N_D}{N_D + \Delta n} t \tag{A.6}$$

The expressions for the normalized grid series resistance component—see equation A.7 and A.8—are derived as reported in [Meier 1984] and expressed, in analogy with the case of the IBC-SHJ device, as a function of the designated cell area A_d. The subscript p, in the case of R_{finger}, R_{bb} and $R_{TCO/metal}^N$ specify their association to the front-grid electrode, in contact with the p-type a-Si:H layer. Equation A.8 is derived for the case of two lateral current extraction points at each side of the central bus bar, as in our measurement set-up.

$$R_{finger,p}^N = \frac{8}{3} a^3 b^2 n \left(\frac{\rho_f}{w_f t_f} \right) \cdot \frac{1}{A_d} \tag{A.7}$$

$$R_{bb,p}^N = \frac{8}{3} a^2 n^3 b^3 \left(\frac{\rho_f}{w' t'} \right) \cdot \frac{1}{A_d} \tag{A.8}$$

The normalized resistance component associated with the contact between TCO and metal front-grid is calculated as in equation A.9. We note that equivalent results can be obtained, taking into account of the TCO/metal contact transfer length L_t as in [Meier 1984].

$$R_{TCO/metal,p}^N = \frac{(\rho_c)_{TCO/metal}}{(2 a w_f n + 2 b n w')} \cdot A_d \tag{A.9}$$

The normalized series resistance component associated with lateral transport of carrier

through the front TCO films is calculated as in equation A.10. We note that this expression gives an overestimation of the real resistance values. As it has been show elsewhere [Geissbuhler 2014], lateral transport in the front TCO is not the only current path followed by the collected charge carriers.

$$R^N_{lateral,TCO} = \frac{1}{3} b^2 R^{TCO}_{sheet} \tag{A.10}$$

Eventually, the normalized resistance components associated with the hole and electron contacts simply equal the respective specific contact resistivity values $(\rho_c)_p$ and $(\rho_c)_n$—as expressed in A.11—due to the coincidence of heterocontact and designated areas.

$$\left(R^N_{contact}\right)_p = (\rho_c)_p \quad ; \quad \left(R^N_{contact}\right)_n = (\rho_c)_n. \tag{A.11}$$

For the FHC SHJ solar cell, the normalized total series resistance $\left(R^N_{series}\right)$ is calculated according to:

$$R^N_{series}(\text{FHC}) = R^N_{bulk} + \left(R^N_{contact}\right)_n + \left(R^N_{contact}\right)_p + R^N_{lateral,TCO} + R^N_{TCO/Metal,p} + R^N_{finger,p} + R^N_{bb,p}. \tag{A.12}$$

B | Short-circuit current losses of IBC-SHJ devices

Table B.1: Formulas used to calculate the short-circuit current losses of SHJ devices using their EQE, reflectance, trasmittance and absorbance curves. Reproduced with permission from [Paviet-Salomon 2015a]. Copyright 2015, AIP Publishing LLC.

J_{sc} loss formulas

$$J_{\text{reflection}} = \frac{q}{hc} \int_{350\,\text{nm}}^{1200\,\text{nm}} \lambda \cdot \phi(\lambda) \cdot R_{\text{OPAL}}(\lambda) \cdot d\lambda$$

$$J_{\text{escape,front}} = \frac{q}{hc} \int_{850\,\text{nm}}^{1200\,\text{nm}} \lambda \cdot \phi(\lambda) \cdot [R_{\text{cell}}(\lambda) - R_{\text{OPAL}}(\lambda)] \cdot d\lambda$$

$$J_{\text{escape,back}} = \frac{q}{hc} \int_{850\,\text{nm}}^{1200\,\text{nm}} \lambda \cdot \phi(\lambda) \cdot T_{\text{cell}}(\lambda) \cdot d\lambda$$

$$J_{\text{short}} = \frac{q}{hc} \int_{350\,\text{nm}}^{600\,\text{nm}} \lambda \cdot \phi(\lambda) \cdot [1 - R_{\text{cell}}(\lambda) - T_{\text{cell}}(\lambda) - EQE(\lambda)] \cdot d\lambda$$

$$J_{\text{medium}} = \frac{q}{hc} \int_{600\,\text{nm}}^{1000\,\text{nm}} \lambda \cdot \phi(\lambda) \cdot [1 - R_{\text{cell}}(\lambda) - T_{\text{cell}}(\lambda) - EQE(\lambda)] \cdot d\lambda$$

$$J_{\text{long}} = \frac{q}{hc} \int_{1000\,\text{nm}}^{1200\,\text{nm}} \lambda \cdot \phi(\lambda) \cdot [1 - R_{\text{cell}}(\lambda) - T_{\text{cell}}(\lambda) - EQE(\lambda)] \cdot d\lambda$$

q is the elementary charge, h Planck's constant, c the speed of the light, λ the photon wavelength and $\phi(\lambda)$ the AM1.5G solar spectrum (all other symbols are defined in the text).

C On the use of the transfer-length-method to characterize heterocontacts

In this appendix, we comment on the care to be taken when applying the conventional transfer-length-method (TLM) [Berger 1972] to SHJ contact characterization. Here, we consider the case of TLM contact pad arrays with an a-Si:H-based passivating electron contact. However, our analysis may be extended to the more general case of carrier-selective passivating contacts, which I-V characteristic present some non-linear effects.

The I-V characteristic measured between the contact pads of a TLM test sample may show strong non-linear effects (see for instance Fig. 5.12). In this case the TLM analysis simply cannot be applied. However, depending on the considered current range, non-linear effects may appear, or not, and the applicability of the TLM analysis results unclear. In Fig. C.1, we consider the exemplary case of a not-optimized SHJ electron contact, which serves well the scope of our discussion. In the graphs (a) and (b) of this figure, for the same TLM measurement, we visualize a current range of 200 mA and of 10 mA, respectively. It can be observed as the non-linear effects, evident in graph (a), are not visible in graph (b). Considering the I-V characteristics of graph (b), we may extract resistance values, for each pad spacing, which are perfectly suited for a TLM analysis. Importantly, the current range considered in graph (b) fully comprises the J_{sc} values of 1-sun SHJ solar cell operation. Either considering the entire contact pad area, or that defined by the TLM-sample width (w_{TLM}) and the transfer length (L_t), current density values exceed abundantly $40 \, \mathrm{mA \, cm^{-2}}$. For reference, the TLM contact pad array geometry can be found in Fig. 5.9.

Non-linear effects, as those of Fig. 5.12 and C.1, indicate a rectifying characteristic of the electron contact. The contact is probed twice, once in forward and once in reverse bias conditions, which generates such characteristic symmetric "opposite-diode" I-V curve. To study the impact of such non-linear effects on the parameters extracted via a TLM analysis, we performed simulations. In a MATLAB script we computed the I-V characteristic of two opposite diodes and one resistor connected in series (see Fig. C.2). At first the script builds the I-V characteristic of each element separately. Then it constructs the overall I-V characteristic calculating, for a defined array of current values, the voltage drops at each circuit element

Appendix C. On the use of the transfer-length-method to characterize heterocontacts
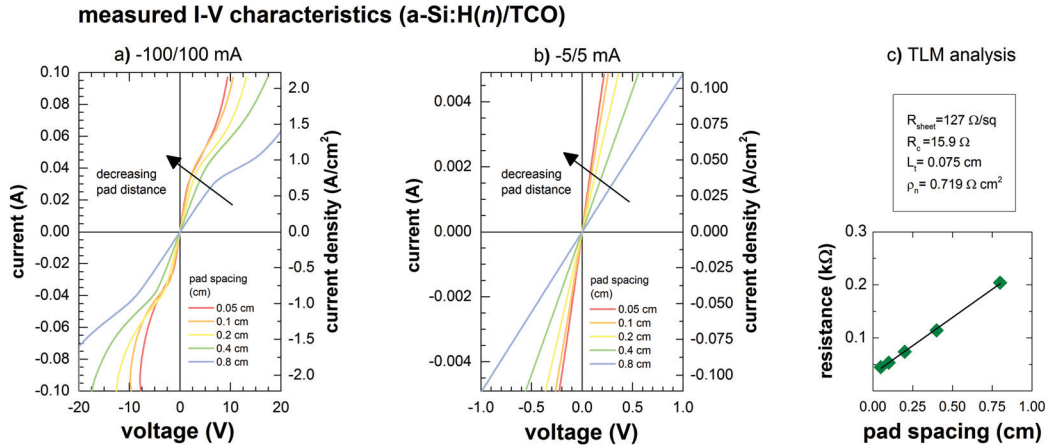
measured I-V characteristics (a-Si:H(n)/TCO)

Figure C.1: Measured I-V characteristics for the TLM contact pad array with the exemplary SHJ electron contact. The data are shown in two different current ranges: -100/100 mA in graph (a) and -5/5 mA in graph (b). The results of the TLM analysis, performed on the resistance values extracted from the data shown in graph (b), are reported in the inset (c). Based on the calculated transfer length (L_t), the current density values are indicated on the right axis of graph (b).

and the total voltage difference between the two circuit ends. The diode characteristic follows the equation $I(V) = I_0 \cdot (\exp(qV/nkT) - 1) + V/R_{shunt}$, where V is the applied voltage, I_0 the inverse saturation current, q the elementary charge, n the diode ideality factor, k the Boltzmann's constant, T the absolute temperature and R_{shunt} the shunt resistance associated with each diode.

In our simulations, we defined a series of values for R^*, assuming a fixed contact resistance (R_c) and adding the variable resistor (R_{var}). R_{var} values represent the c-Si wafer resistance in between each couple of TLM contact pads, and were calculated for the wafer and the TLM structure used in our experiments. Simply assuming $R_c = 10\Omega$ and choosing suitable values for n, R_{shunt} and I_0 in the diode equations, we simulated the I-V curves of Fig. C.3, which mimic well the experimental results of Fig. C.1. Considering only the simulated data in
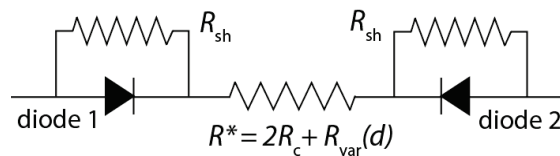
Figure C.2: The equivalent circuit simulating a TLM measurement, in the dark. The resistor R^* accounts for twice the electron-contact resistance R_c and the variable wafer resistance (R_{var}), between each couple of TLM contact pads. The latter is calculated as $R_{var} = R_{sheet} \cdot d / w_{TLM}$, where $R_{sheet} = 130\,\Omega/sq$, d is the pad spacing and w_{TLM} the width of the TLM-sample (for clarity see also Fig. 5.9). In our case $w_{TLM} = 0.6$ cm and d assumes the values: 0.05, 0.1, 0.2, 0.4 and 0.8 cm.

simulated I-V characteristics (a-Si:H(*n*)/TCO)

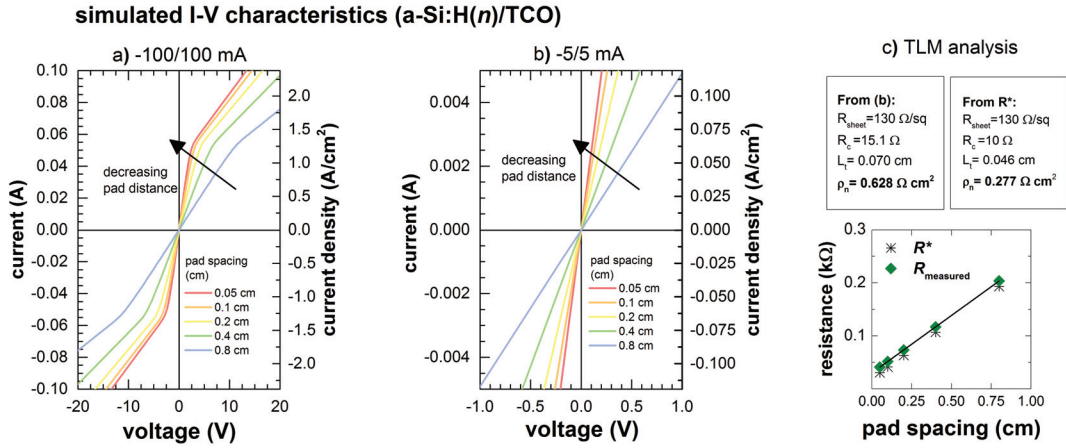Figure C.3: Simulated I-V characteristics for the circuit of Fig. C.2. In analogy with Fig. C.1, we show the simulated curves in two different current ranges. In graph (c) we compare the resulting resistance values for the simulated I-V curves in graph (b) (R_{measured}) and the set of resistance values (R^*) used in the simulation. From the TLM experiment we extract $R_c = 15.1\,\Omega$, when in the circuit of Fig. C.2 was set $R_c = 10\,\Omega$. The extracted R_c values are influenced by the non-linear component of the electron contact characteristic.

the 10 mA current range, as in the real TLM experiment, we extracted the resistance values R_{measured} and performed the TLM analysis. The values of R_{measured}, compared to R^*, are higher. This means that the diode I-V characteristics contribute significantly to the overall I-V curve, even if in the considered current range it appears totally linear. As a consequence, the TLM analysis overestimates the value of R_c. The value of R_{measured}, extrapolated for $d = 0$, does not correspond to $2 \cdot R_c$, but includes the additional contribution of the diode characteristics. In this exemplary case, the extracted $(\rho_c)_n$ is 2 times higher than that calculated from R_c. This difference is by far higher than what we expect (from simulations) for SHJ electron contacts with low measured $(\rho_c)_n$. However, this exemplary case clarifies the problem encountered in any TLM analysis of contacts with non-linear I-V characteristics.

The inclusion of non-linear effects in a contact resistance measurement, is not a problem as far as these effects are those encountered in the contact, under operating conditions. However, in the TLM measurement the non-linear effects are generated by diodes which are oppositely biased. Then, in our I-V measurement, we include the reverse characteristic of one of the diodes, which is excluded in device operating conditions. In addition, we observed that these non-linear effects vary with the contact pad array geometry and under illumination.

To conclude, care must be taken when applying TLM to the characterization of SHJ contacts. The values of contact resistance achieved with this method may be considered as upper bounds rather than exact absolute values. Nevertheless, the method remains useful in the context of device optimization. It helps the evaluation of passivating-contact properties and the identification of best-performing a-Si:H and TCO layers. Notable examples are the ZnO:Al layers studied in section 5.3.3 or of the μc-Si:H(*n*) layer of section 5.4.1.

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Oral presentations as first or presenting author

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1 M. Pesce, M. Maugeri, M. Marsili, M. Zarcone, D. Tonini, C. Bottosso, M. Galiazzo, and A. Tomasi (**P**), *"Technological and economic assessment of two-steps printing processes in a mc-Si solar cells production environment"*, presented at Third Metallization Workshop on Metallization for Crystalline Silicon Solar Cells, Charleroi, Belgium, 2011.

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- B. Paviet-Salomon, A. Tomasi, M. Despeisse, C. Ballif, EUROPEAN PATENT APPLICATION, EP15192655.7 (2015)
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