Improved electrical and thermal performances in nanostructured GaN devices

(Invited Paper)

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***Abstract*—Electrical and thermal performances were enhanced for AlGaN/GaN Schottky barrier diodes (SBDs) using a nanostructured anode technology. The fabricated SBDs presented small turn-on voltage of 0.95 V, large output current density over 1 A/mm, low reverse leakage current below 1 nA/mm and diminished self-heating. Additionally, the nanostructured electrode greatly reduced the thermal resistance of the device by about 50% and hence improved the thermal performance of GaN SBDs as well as transistors. Furthermore, geometry of the nanostructured electrode had a large impact on device performance, which was presented and analyzed in this work.**

Keywords— GaN; nanostructure; Schottky diode; HEMT; heat dissipation

I. Introduction

The efficiency of power management systems have shown impressive improvements with silicon technology, which is however asymptotically approaching its limits. For future compact and efficient power electronics, GaN is highly desirable since it offers superior material properties such as large band-gap, high electron saturation velocity and high breakdown field strength [1,2]. Furthermore, GaN heterostructures present high-density two-dimensional electron gas (2DEG) with mobility over 2000 $cm^2/V{\cdot}s$, which enables power electronics with simultaneously fast switching, high blocking voltage and large power density.

GaN SBDs are an important component in several topologies of power converters. In this case, small turn-on voltage (V_{on}), small reverse leakage current (I_R) as well as small series inductance are required for the SBD to reduce operating loss. AlGaN/GaN lateral SBDs are therefore very promising since it can be easily monolithically integrated with AlGaN/GaN HEMTs and greatly reduces the series inductance. However, conventional AlGaN/GaN lateral SBDs suffer from large V_{on} and I_R. Besides that, thermal management is another important issue for power devices. The relatively poor thermal conductivity of GaN causes issues like self-heating and thermal instabilities, which greatly degrade the performance, efficiency and reliability of the device. To pave the path for future high-efficiency and compact GaN-based power devices, both enhancement in electrical and thermal performances of the devices are necessary.

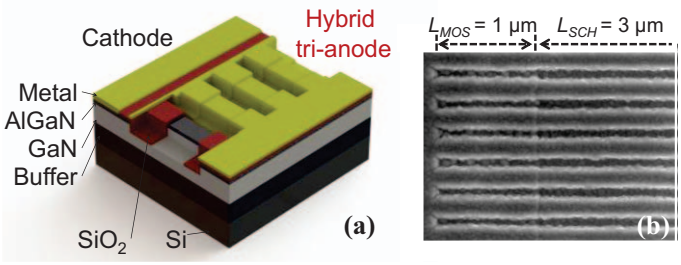

Fig. 1. (a) The schematic of AlGaN/GaN hybrid tri-anode SBDs and (b) top-view SEM observation of the hybrid tri-anode.

Great effort has been devoted to overcome these challenges but simultaneous improvement in both electrical and thermal performance of the devices are rare. Recently nanostructured electrode technology has been demonstrated in AlGaN/GaN SBDs with a hybrid tri-anode structure for minimized V_{on}, suppressed I_R as well as improved ideality [3], which is very promising. In this work, we explored the improved electrical performance in such nanostructured SBDs, revealed their significant potential for heat dissipation, and investigated the impact of the geometry of such nanostructure on device performance.

II. Device Fabrication

SBDs in this work were fabricated using commercial AlGaN/GaN HEMT epi on 4-inch Si substrate. Thickness and Al composition of the AlGaN barrier was 18 nm and 26%, respectively. The schematic of the 100-μm-wide tri-anode SBDs is shown in Fig. 1 (a), in which part of the anode metal is not presented for better observation. Device isolation was firstly done by Cl_2-based inductively coupled plasma (ICP) etching. After that ohmic metal stack of Ti/Al/Ni/Au was deposited by e-beam evaporation followed by rapid thermal annealing of 30 seconds in N_2 atmosphere. Then AlGaN/GaN nanowires in tri-anode region were fabricated by combining conventional lithography, interference lithography as well as ICP etching. The interference lithography enables faster and cheaper fabrication of periodic nanostructures with respect to conventional e-beam or deep/extreme ultra-violet lithography, and thus can be more suitable for mass production. The height (h) of the nanowire was measured to be about 114 nm using

atomic force microscopy. The width (w) and period (p) of a nanowire was 135 nm and 300 nm, respectively, corresponding to a filling factor ($FF = w/p$) of about 45%. After nanowire etching, 18-nm SiO_2 was deposited by atomic layer deposition and then selectively removed in Schottky and ohmic contact areas. Finally Ni/Au was deposited as the anode. Figure 1 (b) shows top-view SEM observation of the hybrid tri-anode after fabrication, which consisted of a tri-gate metal-oxide-semicondutor (MOS) high electron mobility transistor (HEMT) in series with a tri-anode Schottky regions. The length of the tri-gate HEMT (L_{MOS}) and Schottky regions (L_{SCH}) were 1 and 3 µm, respectively. Planar AlGaN/GaN SBDs (Planar) with similar dimensions were taken as reference.

III. Results and Discussion

Current-voltage (I-V) characteristics of the fabricated SBDs were plotted in Fig. 2. Under forward bias, the Planar exhibited a large V_{on} of 1.43 ± 0.11 V and an undesirable knee voltage. This knee voltage was eliminated in the Tri-anode, with V_{on} reduced to 0.95 ± 0.09 V. With reverse bias, I_R was reduced by over 3 orders of magnitude with the hybrid tri-anode. These improvements can be explained by the integrated sidewall SBDs and tri-gate HEMTs in the Tri-anode. Due to the absence of the AlGaN barrier, the sidewall Ni-to-2DEG Schottky contact has a smaller and close-to-ideal Schottky barrier, which led to a smaller V_{on} and eliminated the non-ideality observed in the Planar. Under reverse bias, the integrated tri-gate HEMT was depleted and hence I_R was significantly reduced. DC and pulsed I-V characteristics of the SBDs are also compared in Fig. 2 (a), which suggests much less self-heating degradation for the Tri-anode with respect to the Planar. This is likely attributed to the improved heat dissipation by the nanowire trenches that results in less thermal degradation in conductance of the integrated tri-gate HEMTs. To verify this, separate AlGaN/GaN tri-gate HEMTs with similar nanowires to the Tri-anode were fabricated (the inset of Fig. 3) and compared with planar HEMTs. The gate length for the 150-µm-wide HEMTs was 10 µm, with gate-to-source/drain separations of 1 µm. Drain current (I_D) of the HEMTs were plotted as a function of dissipated power (P_d) in

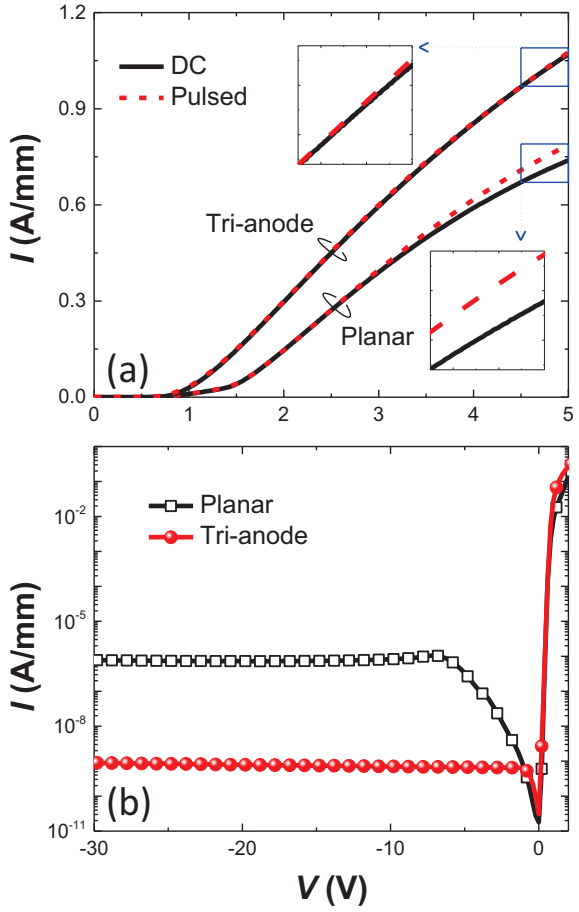

Fig. 2. (a) Forward and (b) reverse I-V characteristics of the SBDs normalized by width of un-etched area and sidewall contact (10 nm/sidewall).

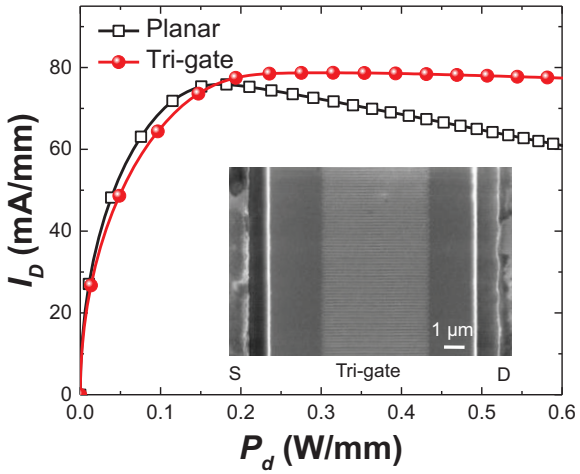

Fig. 3. Drain current versus dissipated power of the planar and tri-gate HEMTs measured at similar gate driving voltage (V_G - V_{TH}) and normalized by device width (150 µm); the inset shows the schematic of the fabricated tri-gate HEMTs.

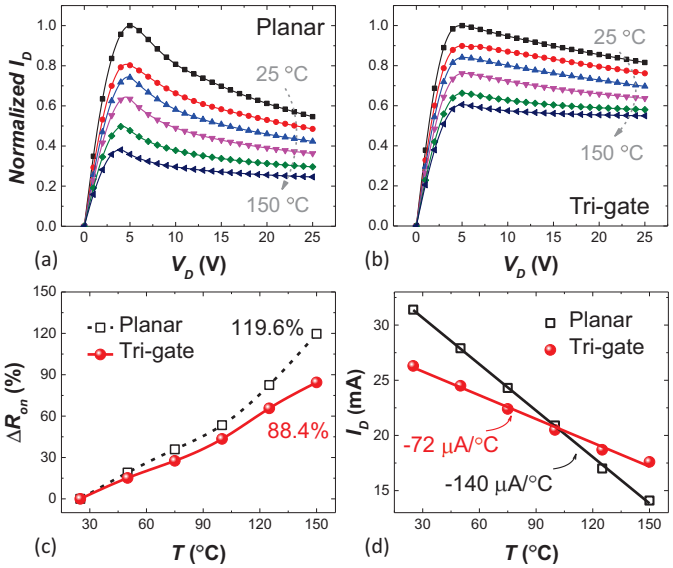

Fig. 4. Temperature-dependent I_D-V_D characteristics of the (a) planar and (b) tri-gate HEMTs under similar gate driving voltage; (c) degradation in on-resistance (ΔR_{on}) versus temperature; (d) I_D of the HEMTs versus temperature at V_D = 25 V.

Fig. 3. With increasing P_d, I_D of the planar HEMT reduced due to the self-heating effect while that of the tri-gate HEMT was almost constant. Figure. 4 (a) and (b) present the normalized temperature-dependent I_D-V_D curves of the HEMTs. With increasing temperature, the degradation in maximum I_D was over 60% and below 40% for the planar and tri-gate HEMTs, respectively. This suggests much better thermal stability for the tri-gate HEMTs. Temperature-dependent degradation of on-resistance (ΔR_{on}) was then extracted and plotted Fig. 4 (c). The ΔR_{on} of the tri-gate HEMT was over 25% smaller that of the planar at a temperature of 150 ºC. Furthermore, the tri-gate HEMT presented larger absolute I_D at V_D = 25 V than the Planar when T was above 100 ºC, although the nanowire etching removed 55% of the 2DEG in the tri-gate region, as shown in Fig. 4 (d). These results indicate enhanced thermal performance in tri-gate HEMTs, and reveals the great potential of the tri-gate architecture for GaN high-temperature electronics.

To further investigate the enhanced thermal performance in Tri-anode and tri-gate HEMTs, we measured the temperature dependence of the extrapolated drain saturation current ($I_{DS,0}$) of the HEMTs and then extracted their average temperature over the entire device active area (T_{avg}) (Fig. 5) [4, 5]. With the same P_d, the tri-gate HEMT exhibited a smaller T_{avg} as compared to the planar. Such reduction of T_{avg} is comparable or greater than other technologies proposed for improve the heat dissipation of GaN electronics such as graphene-graphite quilts [6], Cu-filled backside via [7], substrate transfer using h-BN [8], and nanocrystalline diamond thin film [9]. Figure 4 (b) also reveals a smaller thermal resistance (R_{TH}) for the tri-gate HEMT. From the slope of the linear region of the T_{avg}-P_d curves, R_{TH} of the planar and tri-gate HEMTs were estimated to be about 34.2 and 17.0 K·mm/W, respectively, normalized by device width. The reduction in R_{TH} of about 50% with the tri-gate architecture is very close to the reduction (55%) by replacing Si substrates with expensive SiC substrates [10], indicating the significant potential of the tri-gate technology in thermal engineering of GaN transistors. The reduced R_{TH} in the tri-gate HEMT is likely due to the increased surface area from the nanowire architecture and the partial removal of AlGaN which has smaller thermal conductivity than GaN. The reduced T_{avg} and R_{TH} confirm the improved heat dissipation in the tri-gate HEMT, which is consistent with the results from pulsed measurements for the tri-anode SBDs.

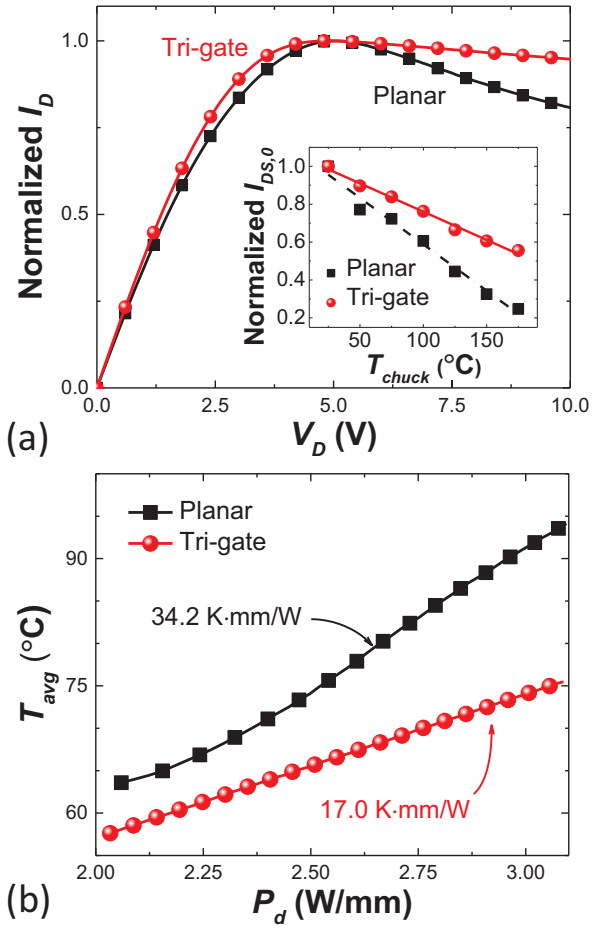

Fig. 5. (a) Normalized I_D-V_D characteristics of planar and tri-gate HEMTs measured with similar gate driving voltage (~5 V) and (b) extracted average temperature of the 150-µm-wide HEMTs versus dissipated power normalized by device width; the inset show the linear dependences of the extrapolated saturation drain current on the chuck temperature.

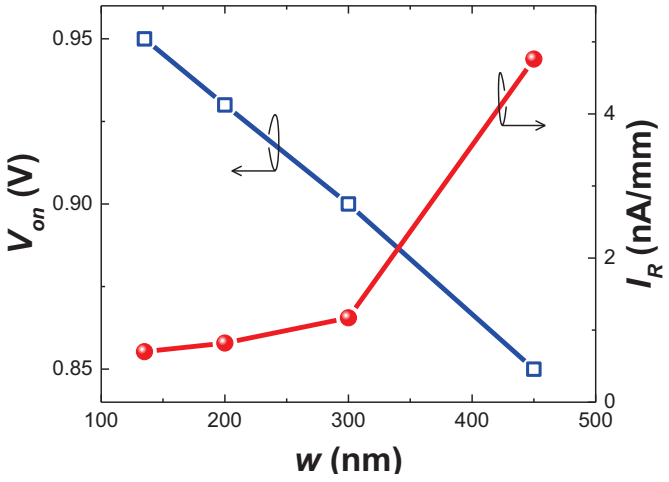

Fig. 6. V_{on} and I_R at -10 V of hybrid tri-anode SBDs with different w.

As discussed above, both electrical and thermal performances of the SBD were improved with the hybrid tri-anode structure. Yet the dimension of such nanostructured electrode has a significant impact upon device performance, which needs to be carefully determined based on the requirements of a given application. To study this impact, we fabricated hybrid tri-anode SBDs with different w. As shown in Fig. 6, I_R reduced and V_{on} increased with decreasing w. The reduction in I_R was attributed to the enhanced gate control for the integrated tri-gate HEMT in the hybrid tri-anode. Smaller w reduced the separation between the 2DEG channel and the sidewall gates, resulting in better gate control and hence smaller leakage current. To justify this explanation, we fabricated discrete tri-gate HEMTs with different w and their transfer characteristics were plotted in Fig. 7. The off-state leakage current and subthreshold slope of tri-gate HEMTs

decreased with reducing w. This indicates better control with narrower nanowire and agrees well with previous assumptions.

Another interesting phenomenon revealed in Fig. 6 is that the V_{on} of the Tri-anode increases with decreasing w. This can be explained by the w-dependent reduction of 2DEG in AlGaN/GaN nanowires which reduces the Schottky barrier height. To investigate this, we fabricated MOS capacitors consisted of various AlGaN/GaN nanowires and explored the 2DEG concentration in these nanowires. As shown in Fig. 8, the 2DEG density (N_s) reduced with shrinking w. Compared to the N_s of 7.4 × 10^{12} /cm^2 for planar AlGaN/GaN heterostructure (extracted from planar MOS capacitors), the N_s became very small when the nanowire was as narrow as about 80 nm. Such reduction of 2DEG in AlGaN/GaN nanowires is due to the partial relaxation of the AlGaN barrier caused by the nanowire etching. The etching reduced tensile stress from the buffer layers as well as substrates and increased the elastic deformation of GaN channel due to the lattice-induced compressive stress from the AlGaN. This reduced the effective lattice mismatch between the AlGaN layer and the GaN channel, resulting in the less-strained AlGaN and hence degraded 2DEG density for in the nanowire.

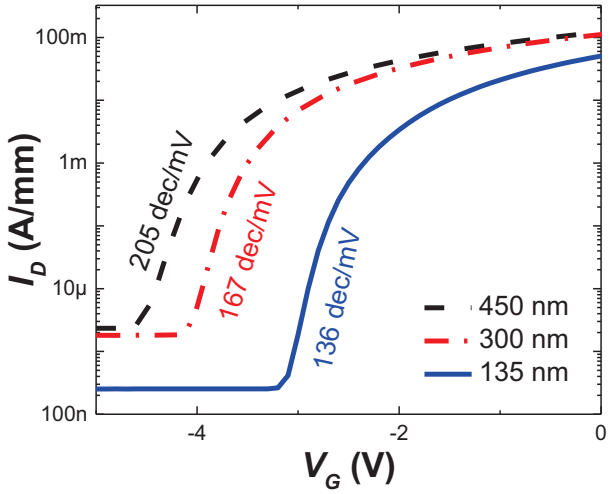

Fig. 7. Transfer characteristics of GaN tri-gate HEMTs with nanowire width from 135 nm to 450 nm; gate and tri-gate region lengths were 8 and 5 μm, respectively, and gate-to-drain separation was 11 μm.

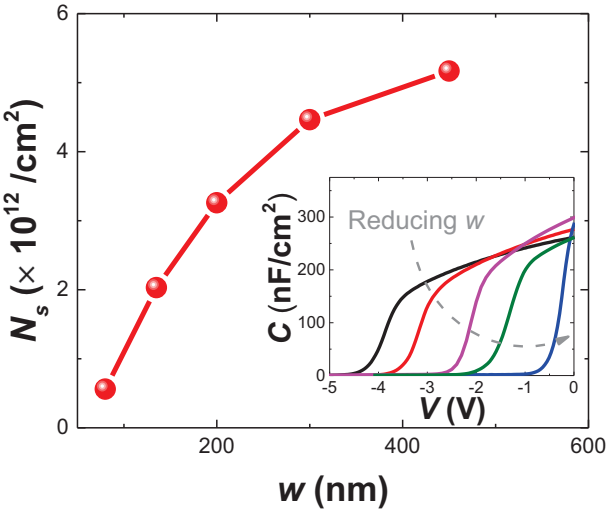

Fig. 8. Width-dependent 2DEG density (N_s) extracted from C-V characteristics of SiO_2/AlGaN/GaN nanowire MOS capacitors with nanowire widths from 450 to 80 nm; the inset shows the C-V plots of the capacitors.

IV. Conclusion

In this work we presented high-performance AlGaN/GaN SBDs with nanostructured anode (hybrid tri-anode). This technique minimized the V_{on} from 1.43 V to 0.95 V and significantly reduced the reverse leakage current by over 3 orders of magnitude. The nanostructured anode also reduced the R_{TH} of the integrated HEMTs by about 50% and hence led to largely diminished self-heating as well as enhanced thermal stability of the device. The geometry of the nanostructured anode had a large impact on device performance due to the w-dependent gate control and reduction of 2DEG, which can be carefully designed based on different applications.

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