

# **Modulation, Coding, and Receiver Design for Gigabit mmWave Communication**

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*Lausanne, 20th July 2016*

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# Abstract

While wireless communication has become an ubiquitous part of our daily life and the world around us, it has not been able yet to deliver the multi-gigabit throughput required for applications like high-definition video transmission or cellular backhaul communication. The throughput limitation of current wireless systems is mainly the result of a shortage of spectrum and the problem of congestion.

Recent advancements in circuit design allow the realization of analog frontends for mmWave frequencies between 30GHz and 300GHz, making abundant unused spectrum accessible. However, the transition to mmWave carrier frequencies and GHz bandwidths comes with new challenges for wireless receiver design. Large variations of the channel conditions and high symbol rates require flexible but power-efficient architectures. This thesis investigates receiver algorithms and architectures that enable multi-gigabit mmWave communication. Using a system-level approach, the design options between low-power time-domain and power-hungry frequency-domain signal processing are explored. The system discussion is started with an analysis of the problem of parameter synchronization in mmWave systems and its impact on system design. The proposed synchronization architecture extends known synchronization techniques to provide greater flexibility regarding the operating environments and for system efficiency optimization.

For frequency-selective environments, versatile single-carrier frequency domain equalization (SC-FDE) offers not only excellent channel equalization, but also the possibility to integrate additional baseband tasks without overhead. Hence, the high initial complexity of SC-FDE needs to be put in perspective to the complexity savings in the other parts of the baseband. Furthermore, an extension to the SC-FDE architecture is proposed that allows an adaptation of the equalization complexity by switching between a cyclic-prefix mode and a reduced block length overlap-save mode based on the delay spread. Approaching the problem of complexity adaptation from the time-domain, a high-speed hardware architecture for the delayed decision feedback sequence estimation (DDFSE) algorithm is presented. DDFSE uses decision feedback to reduce the complexity of the sequence estimation and allows to set the system performance between the performance of full maximum-likelihood detection and pure decision feedback equalization. An implementation of the DDFSE architecture is demonstrated as part of an all-digital IEEE 802.11ad baseband ASIC manufactured in 40nm CMOS.

A flexible architecture for wideband mmWave receivers based on complex sub-sampling is presented. Complex sub-sampling combines the design advantages of sub-sampling receivers

## Acknowledgements

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with the flexibility of direct-conversion receivers using a single passive component and a digital compensation scheme. Feasibility of the architecture is proven with a 16Gb/s hardware demonstrator. The demonstrator is used to explore the potential gain of non-equidistant constellations for high-throughput mmWave links. Specifically crafted amplitude phase-shift keying (APSK) modulation achieve 1dB average mutual information (AMI) advantage over quadrature amplitude modulation (QAM) in simulation and on the testbed hardware. The AMI advantage of APSK can be leveraged for a practical transmission using Polar codes which are trained specifically for the constellation.

Key words: millimeter wave communication, digital communication, mmWave, digital signal processing, baseband algorithms, VLSI systems, signal sampling, sub-sampling, digital modulation, amplitude phase-shift keying modulation, channel coding, polar codes

# Zusammenfassung

Während Funksysteme zu einem allgegenwärtigen Teil unseres täglichen Lebens und der Welt um uns herum geworden sind, haben sie es noch nicht geschafft die Multi-Gigabit Datenraten zu liefern, welche für Anwendungen wie die Übertragung von hochauflösenden Videodaten oder den Rücktransport moderner Mobilfunknetze nötig wären. Die Durchsatzbegrenzung aktueller Funksysteme liegt im Wesentlichen im Mangel an Spektrum und Überlastung.

Jüngste Entwicklungen im Bereich der Schaltungsentwicklung erlauben die Realisierung von analogen Schaltungen für Millimeterwellen im Frequenzbereich von 30GHz bis 300GHz, und machen damit reichlich ungenutztes Spektrum zugänglich. Der Umstieg auf mmWellen Trägerfrequenzen und GHz Kanalbandbreiten bringt neue Herausforderungen für die Entwicklung von Funkempfängern mit sich. Grosse Variationen in den Kanalbedingungen sowie hohe Symbolraten bedingen flexible und gleichzeitig energie-effiziente Empfängersysteme. Diese Arbeit untersucht Algorithmen und Architekturen für Empfänger, welche Multi-Gigabit mmWellen Kommunikation ermöglichen. Basierend auf einem Systemansatz werden Optionen zwischen Energie-sparender Zeitbereichs- und Energie-hungriger Frequenzbereichs-Signalverarbeitung untersucht. Die Systemdiskussion startet mit einer Analyse des Problems der Parameter Synchronisierung für mmWellen Systeme und dessen Einfluss auf die Systementwicklung. Die vorgeschlagene flexible Architektur für die Synchronisierung erweitert bestehende Synchronisierungstechniken, um mehr Designflexibilität im Bezug auf die Kanalbedingungen und eine höhere Systemeffizienz zu erhalten.

In Frequenz-selektiven Umgebungen, bietet die vielseitige Einträger Frequenzbereichs Entzerrung (EFE) nicht nur ausgezeichnete Kanal-Entzerrung sondern auch die Möglichkeit weitere Basisband Signalverarbeitungsaufgaben zu integrieren. Deshalb muss der hohe initiale Aufwand von EFE immer ins Verhältnis zu den Einsparungen in anderen Bereichen des Basisbandempfängers gestellt werden. Ferner wird eine Erweiterung von EFE vorgeschlagen, welche eine Anpassung des Entzerrungsaufwands an die Kanalbedingungen durch Umschalten des Entzerrungsmodus erreicht. Um das Problem der Aufwandsanpassung aus dem Zeitbereich zu beleuchten, wird eine Hochgeschwindigkeits-Architektur für den "delayed decision feedback sequence estimation" (DDFSE) Algorithmus vorgestellt. DDFSE nutzt Entscheidungsrückkopplung um den Aufwand für die Bestimmung der wahrscheinlichsten Sequenz zu reduzieren, was es erlaubt die Leistungsfähigkeit des Systems zwischen einer optimalen Detektierung und einer puren Entscheidungsrückkopplung einzustellen. Eine Implementierung der DDFSE Architektur wird als Teil eines voll-digitalen IEEE 802.11ad Basisband integriertem Schaltkreis in 40nm CMOS vorgeführt.

## Acknowledgements

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Eine flexible Architektur für breitbandige mmWellen Empfänger basierend auf komplexer Unterabtastung wird vorgestellt. Komplexe Unterabtastung kombiniert die Systemvorteile von real-wertigen Unterabtastungsempfängern mit der Flexibilität von Direktmischempfängern mittels eines einzelnen passiven Bauelements sowie einer digitalen Korrekturmaßnahme. Die Realisierbarkeit der Architektur wird anhand eines 16Gb/s Vorführsystems bewiesen. Das Vorführsystem wird zur Sondierung möglicher Vorteile von nicht-äquidistantem Konstellationen für mmWellen Verbindungen mit hohem Durchsatz genutzt. Speziell strukturierte Phasen- und Amplituden-Modulation (PuAM) erzielt einen 1dB Vorsprung in Bezug auf die mittlere-gegenseitige Information (MGI) im Vergleich zu Quadraturamplitudenmodulation in der Simulation und auf dem Vorführsystem. Der MGI Vorsprung von PuAM kann für praktische Datenübertragung genutzt werden unter Zuhilfenahme von polaren Codes welche speziell für die Konstellation trainiert wurden.

Stichwörter: Millimeterwellenkommunikation, digitale Kommunikation, mmWave, digitale Signalverarbeitung, Basisbandalgorithmen, hochintegrierte Systeme, Signalabtastung, Unterabtastung, Amplituden- und Phasenmodulation, Kanalkodierung, polare Codes

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# 1 Introduction

Only few other technologies have had a more transformational impact on our daily lives than wireless communication. Within the last 20 years cellphones have replaced landline phones for the majority of the global population as the principal means of personal communication. In most western countries there are now more cellphones registered than inhabitants, while the number of landlines is not even half [1]. However, personal communication is only one part of the wireless revolution, the communication with and between devices is the second driver of wireless innovation. After the emergence of cheap microcontroller a first wave of “*smart*” products covered nearly all aspects of our daily life, now in a second step everything is becoming wireless. Wireless devices range from rather trivial low-rate applications, like the Bluetooth-enabled egg tray “Egg Minder” [2], which keeps you updated about the expiration dates of your eggs, over critical life saving medical devices like wireless-enabled pacemakers, that allow remote monitoring and reprogramming [3], to devices that stream high-quality audio on demand [4]. Wireless communication is either replacing existing cables for convenience and cost-saving, or even extending capabilities by providing connectivity for devices where a connection has not been practical so far. However, wireless proliferation has been restricted to low- and medium-throughput applications in the past. For multi-gigabit throughput applications cables are still the preferred solution.

The most salient example of machine-to-machine communication, for which wireless solutions have not prevailed yet, is the transportation of raw video data. Raw high-definition video connections between devices still rely mostly on physical cables. Today, in a typical home environment as shown in Fig. 1.1 the consumer uses Bluetooth devices like a remote control or a headset to interact with the home entertainment system which connects to the long term evolution (LTE)-based router using Wi-Fi, nevertheless the high definition multimedia interface (HDMI) cable to the TV is the last wired data connection. While the motivation to replace video cables at home may be mainly driven by convenience, the technical difficulty to stream video data affects also other areas. Problems when interfacing the video projector in a conference room or lecture hall are arguably the single most common reason for delays at the start of a presentation. Often, long cable connections with analog signaling are used to

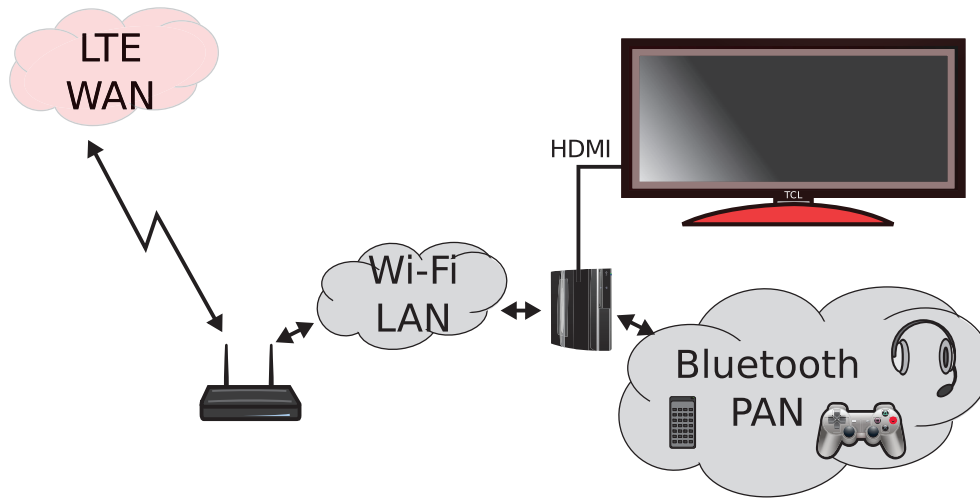


Figure 1.1 – Typical consumer home entertainment system based on different wireless technologies to provide connectivity to accessories and the internet, while still requiring a cable-based link for the video data connection to the TV.

connect the computer to the video projector, to ensure maximum compatibility.

The undesirable situation is the result of the fact that wireless data rates are not even near the throughput required to stream raw high-definition video. In Fig. 1.2 the development of data rates of recent IEEE 802.11 Wi-Fi standards and HDMI cable specifications are compared. The comparison shows that video data rates outgrow the throughput development of wireless LAN, mainly due to the increase in resolution and the uptake of new technologies e.g. 3D video. It becomes evident that the data rates of current Wi-Fi standards are far from being able to replace cable based connections.

The biggest limitations of current Wi-Fi technologies are:

- **Limited available spectrum:** For technical reasons most terrestrial communication is performed below 6 GHz<sup>1</sup>. Up to 6 GHz the design of receivers is comparatively easy and simple antenna setups can still achieve decent ranges. However, the usable spectrum is segmented in many sub-bands so that it can be shared between many different users and applications. The most commonly used band for Wi-Fi is the unlicensed industrial, scientific, and medical (ISM) band at 2.4 GHz which provides only a mere 100 MHz of continuous spectrum. In total 455 MHz of spectrum are available for Wi-Fi above 5 GHz, but because of possible conflicts with legacy primary users, the spectrum is not only non-continuous, but is regulated for indoor use only [5].
- **Congestion:** Because of the unlicensed nature of the bands, there is no inherent control of the number of users or any coordination of the occupied bandwidth. As a result the achievable throughput for each user is not guaranteed and can vary significantly over

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<sup>1</sup>The term sub-6 GHz systems will be used to describe this class of systems.

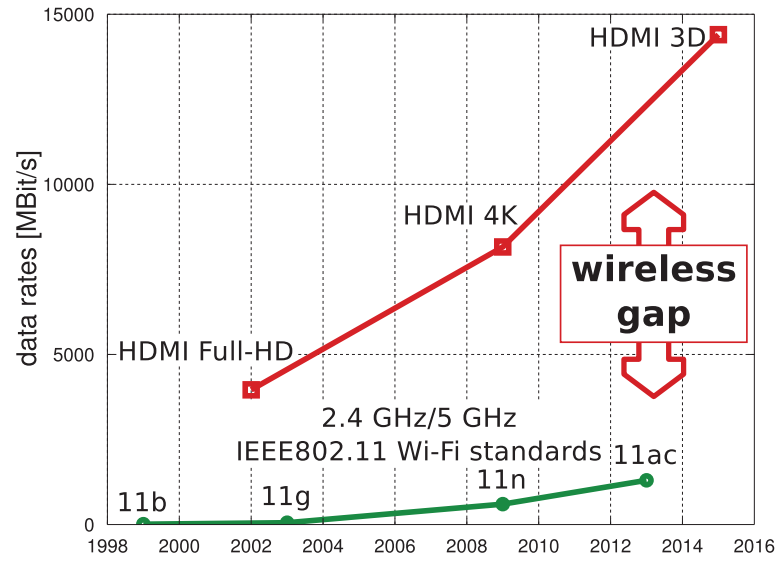


Figure 1.2 – Comparison of the data rate development of the sub-6GHz IEEE 802.11 Wi-Fi and HDMI video cable standards over the years from 1998 to 2016.

time. Quality of service (QoS) schemes, that prioritize certain data, have been suggested with limited success. While the congestion problem exists in principle also in wired networks, there congestion can usually be avoided by over-provisioning the network capacity. A technique that is not possible in wireless networks because of the limited available spectrum.

Different strategies have been suggested to mitigate these two problems and increase the capacity. Besides application layer solutions like data compression, the capacity of wireless systems can be improved by increasing either the spectral efficiency or operating with a higher bandwidth. An increase in spectral efficiency can be achieved by operating at a higher signal-to-noise ratio (SNR) level or using multiple-input multiple-output (MIMO) techniques to exploit multiple spatial streams. Both solutions have the disadvantage that the required complexity grows rapidly with the increase in capacity. Increasing the bandwidth increases capacity and complexity approximately linearly, but again suffers from the aforementioned problem that spectrum is scarce at low GHz frequencies.

Another urgent application for which the increasing throughput demand outgrows the capabilities of wireless connections is the backhaul of cellular wireless networks. The need for interconnection capacity grows not only because of the general increase in user numbers and data rates, but also because upcoming MIMO techniques like coordinated multi-point (COMP) in LTE [6] lead to increased synchronization traffic between basestations. Currently the high throughput demand of backhaul connections is satisfied with high-capacity fiber connections, leveraging the throughput advantage of cable-based links. However, with continuously shrinking cell sizes, cellular networks require more and more backhaul interconnect

and render cable based solutions uneconomic [7].

The situation is even more difficult for developing countries that can not gradually extend an existing backhaul infrastructure. These countries are looking for more cost-effective solutions to supply wideband data services to densely populated urban areas. A high-capacity wireless backhaul network could not only provide the capacity to serve high-speed next generation cellular networks for many user, but also allow high-speed mmWave connections to the homes. Such a technology would allow a transformation out of the current low-rate cellular networks to cellular wireless broadband services and leapfrog classical wired broadband access.

And while raw video transmission and cellular broadband network interconnects are very different in their practical application, they share a common need for multi-gigabit wireless communication.

### 1.1 mmWave Wireless Communication

The need for more bandwidth has lead to increased research interest in the bands above 6 GHz for wireless communication. Increasing the carrier frequency makes significant amounts of spectrum available. Especially the band at 60 GHz became interesting after the feasibility of integrated front-end circuits was demonstrated in SiGE [8][9][10][11] and CMOS [12][13] processes. In the 60 GHz band a continuous 9 GHz spectrum from 57 GHz to 66 GHz is available for unlicensed wideband data transmission systems in Switzerland and the European Union [5]. Hence, the 60 GHz band provides multiple times the spectrum of all other unlicensed bands combined.

The fact that such a big chunk of spectrum was made available at 60 GHz can be explained by the reduced commercial interest for this frequency range. The 60 GHz band coincides with the resonance frequency of oxygen [14] as shown in Fig. 1.3, which makes the band especially suitable for indoor local area network (LAN) and personal area network (PAN) applications. Because of its unlicensed nature the 60 GHz band is ideal for experimental study of very large throughput mmWave systems. Nevertheless, most of the presented research can also be applied to other high frequency bands of current commercial interest, e.g., at 28 GHz<sup>2</sup>, 38 GHz, 77 GHz, or 110 GHz with adjusted assumptions for the attenuation. All these bands promise above GHz channel bandwidths and require new architectures for baseband processing.

The most common objection to the use of frequencies above 10 GHz is the elevated path loss of such systems. And while it is true that mmWave systems suffer from a high path loss, care must be taken to attribute the different components of the path loss correctly. The word path loss is to a certain extent misleading, as most of the energy is not lost but only spread over more dimensions. Depending on the point of view, this can be considered an advantage, as it also increases the spatial selectivity. So path loss is in fact less about reduced range than about the challenge to build steerable high-gain antennas, as will be shown in Chapter 2 in

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<sup>2</sup>The 28 GHz band is strictly speaking [15] not a mmWave band, but bears many technical similarities.

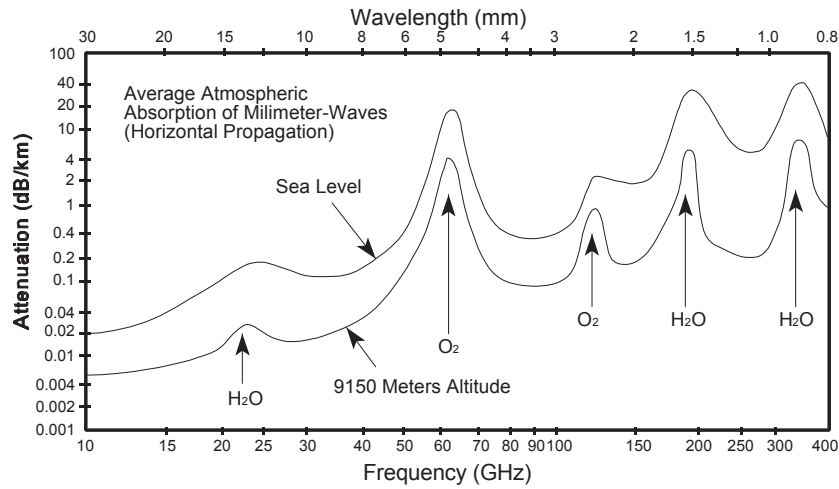


Figure 1.3 – Attenuation of mmWave radio waves due to atmospheric absorption (Figure taken from public domain publication [14] p.146)

more detail.

## 1.2 mmWave Usage Scenarios

Because of the challenge to build high gain antennas, at the beginning mmWave systems were considered mainly for short range, high-throughput scenarios. Envisioned applications include:

- **On-chip and chip-to-chip communication** [16][17][18] in which wireless links replace current high-speed serial links on and between chips of the same system. Wireless links provide a higher level of flexibility for the interconnect.
- **Wireless personal area network (WPAN)** [19] based on mmWave would allow high throughput connections between personal devices for distances below 3 m. The possibility to stream raw video data is especially interesting for the emerging class of augmented and virtual reality devices. Such devices can profit by offloading computationally heavy graphics processing to existing personal devices and thereby reduce cost and size. WPANs with 60 GHz have been standardized as IEEE 802.15.3c [20].
- **Wireless Displays** were initially the main driver for commercial 60 GHz development. High throughput short range wireless mmWave links can replace video cables between home entertainment devices or the feed to video projectors. WirelessHD (sometimes also called UltraGig) was the first commercial standard [21] that used 60 GHz to replace high-resolution HDMI connections. Despite the availability of commercial products the standard never gained traction.

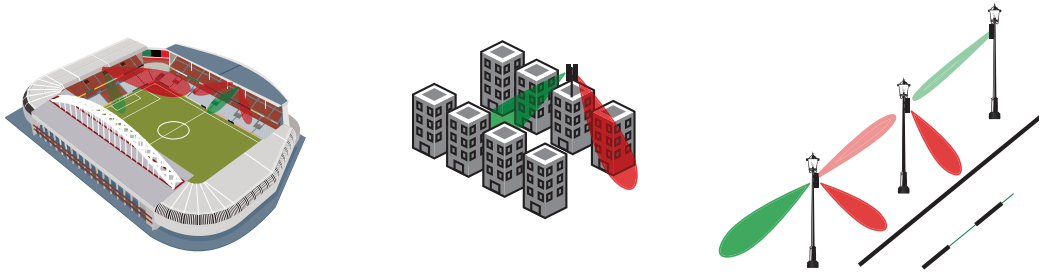


Figure 1.4 – Envisioned urban high-density mmWave applications in future cellular networks include sport stadiums, urban canyons and dense micro-cell networks.

- **Wireless LAN** in the mmWave band (sometimes also called WiGig) merges the initial wireless display and WPAN efforts into a standard for general high-speed data transfers within rooms. With beam-forming on transmitter and receiver side the operating range is extended beyond 10 m. Applications cover raw video streaming, high-speed internet connections, device synchronization and more. In an industry-lead effort of the "Wireless Gigabit Alliance" [22], the IEEE 802.15.3c standard was stripped down and made compatible to IP-based networks resulting in the IEEE 802.11ad [23] 60 GHz extension of the existing IEEE 802.11 Wi-Fi standard. In 2016 the first devices with IEEE 802.11ad support have appeared in retail stores.

With the progress on mmWave circuits and more confidence in the feasibility of high-gain antennas, mmWave frequencies are also considered for next-generation cellular applications. Especially the 28 GHz and 38 GHz bands are considered [24] for cellular application. The use of mmWave technologies is considered for different cellular scenarios (cf. Fig. 1.4):

- **High density cells** realized with mmWave technology can achieve a high network capacity. Festivals, sport stadiums, or crowded shopping streets are a challenge for current cellular networks because of a high density of active users. Such high user densities can be served by a small-meshed network of mmWave basestations that reuse existing infrastructure, e.g., crowded downtown streets could be served by basestations which are mounted on every other lamppost. With the basestations moving closer together, at some point the network capacity becomes limited by interference. The high spatial selectivity of mmWave systems promises reduced inter cell interference and therefore, allows smaller cells.
- **Heterogeneous networks (HetNets)** of future 5G networks are expected to have a mmWave component for opportunistic high-data rate bursts. A mobile handset stays connected to a conventional non-mmWave cellular network with broad coverage. On demand, the basestation can use an additional mmWave link to transmit high-speed data bursts to the handset and thereby save capacity of the conventional network. This operating mode has the advantage that the power-hungry mmWave baseband needs

to run for the duration of the actual data transmission only. Additionally, the reliable low-frequency link can be used to exchange sector information and thereby speed up the expensive and complex beam-forming (BF) establishment.

- **Backhaul connections** for future cellular networks will require high throughputs, that could be provided by directional mmWave links. The data rate requirements of such backhaul connections are expected to grow even faster than the increase in down-link speeds and soon reach 100 Gb/s and more [25]. Not only does each cell try to increase spatial reuse, distributed MIMO techniques, e.g., coordinated multi-point (CoMP) multiply the required backhaul capacity. Shrinking cell sizes make wired backhaul connections less and less cost-effective compared to wireless solutions. Because of the low rank of mmWave MIMO channel matrices [26] such wireless backhaul connections would be most likely realized with multiple parallel and highly directional links using high modulation orders to maximize the spectral efficiency.
- **Fronthaul connections** are an alternative approach of using mmWave links to deal with the increasing density of cellular networks. Low-complexity radio front-ends, placed at strategic locations to maximize coverage, connect to a central baseband processing unit using mmWave links. The central processing locations are chosen, based on the availability of space, power, and network connectivity. With fronthauling much of the coordination between antennas can be performed within the processing unit.

### 1.3 Overview mmWave Research Challenges

The use of mmWave for wireless communication comes with a cornucopia of novel research and engineering challenges that needs to be mastered:

- **Flexible equalization architectures** are required for robust and energy-efficient operation. Unlike classical serial link receivers which operate at similar symbol rates wireless mmWave receivers are challenged by vastly varying operating conditions in different environments. Because of the large signal bandwidth, the typical mmWave propagation characteristics, and the use of beam-forming, the delay spread can range from a single tap to multiple clusters of energy that are spaced dozens of symbol periods apart. Hitherto, mmWave research focused solely on either of the two channel condition regimes. Hence, the receiver designs proposed so far are either low-power architectures for no or short delay spreads that would have difficulties in most mmWave channel scenarios or systems that can deal with very frequency selective channels, but can not adapt their complexity and therefore, can not take advantage from beneficial channel conditions. Not much research has been performed on architectures that combine the two characteristics.
- **Low-complexity high-speed VLSI implementations** of signal processing algorithms are needed for mmWave receivers. Shrinking CMOS transistor sizes allow the imple-



mentation of advanced algorithms even at giga-symbol per second (GSPS) speeds. With continuously faster transistors and growing design areas the delay of the interconnect becomes more critical and the actual physical implementation is a crucial factor for successful semi-custom design. Very large scale integration (VLSI) architectures for mmWave need to be designed to take placement and resulting interconnect from the beginning into account.

- **Smart antennas and even smarter tracking algorithms** are key to leverage the inherent physical advantages of mmWave frequencies. The small wavelength of mmWave allows the integration of a large number of antenna elements in small and portable devices. Such high gain antennas increase not only the operating range significantly, they also allow a higher spatial reuse. However, effective beam-forming requires establishing and tracking the spatial antenna parameters on the transmit and receive side. This has significant implication for the receiver design, as the baseband processing needs not only efficient algorithms for tracking, but also they need to be able to deal temporarily with non-ideal beam-forming conditions.
- **Analog/digital co-design** can bring significant advantages for wireless baseband implementations especially in mmWave systems. For most wireless baseband problems exist solutions in analog and digital domain. Wireless system designers tend to stay in their respective domains and confirm the old proverb “if all you have is a hammer, everything looks like a nail”. Analog designers try to solve all baseband signal processing problems with analog circuitry and advocate the low power consumption, while digital designers assume that for every problem there is an appropriate universal digital filter that will profit over time from technology-scaling. Little effort is taken in current mmWave literature to draw a system level picture of how digital and analog design can profit from each other. A notable exception is [27] where a mixed-signal design approach was proposed to reduce the analog-to-digital converter (ADC) complexity.
- **Flexible receiver architectures** for global multi-band operation are the biggest challenge for modern transceiver design. The need for cellular capacity has lead to a significant fragmentation of the band plan. Currently, the LTE standard specifies [28] more than 45 different frequency bands below 6 GHz, which makes the design more and more difficult. Current cellular transceivers approach this problem by continuously adding receive and transmit chains to the transceiver. Adding mmWave bands to cellular networks will worsen the situation even further and make new approaches to flexible low-power receiver design necessary. The desired reuse of analog front-end resources for different frequency bands makes matching of components more challenging and will put an emphasis on impairment compensation.



## 1.4 Contributions

In this dissertation several of the aforementioned challenges of mmWave receiver design are addressed and novel approaches are proposed which contribute to their solution.

- A **high-speed reduced state sequence estimation (RSSE)** architecture based on the delayed decision feedback sequence estimation (DDFSE) algorithm for giga-sample per second (Gbps) mmWave systems is demonstrated. A VLSI architecture is presented that uses intelligent operation reordering and intermediate result precalculation to enable approximate maximum-likelihood (ML) sequence estimation at mmWave throughput rates. The detector is the first mmWave RSSE receiver design and thereby opens a new corner for the design space of mmWave systems.
- An **IEEE 802.11ad baseband implementation** manufactured in 40 nm CMOS is presented and analyzed. A system-level architecture for parallel processing of the pilot-based block frame format of IEEE 802.11ad at 1.76 GHz symbol rate is presented. The physical layer (PHY) is built around the aforementioned DDFSE detector and features synchronization, channel estimation, detection and low-density parity check (LDPC) error decoding. The implementation supports binary phase-shift keying (BPSK) and quadrature phase-shift keying (QPSK) modulation and all code-rates as specified in the standard. The design demonstrates the integration of the DDFSE detector in a system architecture and the resulting implementation numbers.
- An **improved single-carrier baseband architecture** for robust and flexible mmWave baseband signal processing is presented. The architecture combines time-domain (TD) and frequency-domain (FD) processing to maximize flexibility and efficiency. The efficiency of the fast Fourier transform (FFT) is leveraged to perform some of the complex baseband operations more efficiently in frequency-domain. System efficiency can be maximized by choosing for each operation the more suitable domain. The architecture can be extended to include additional compensation of the receiver non-idealities with minimal overhead.
- **Energy-proportional frequency-domain equalization (FDE)** is proposed to close the gap between energy-scaling time-domain equalization schemes and power-hungry frequency domain equalization. A transparent scheme that combines cyclic prefix (CP) FDE and overlap-save (OS) FDE allows the adjustment of equalizer complexity based on the delay-spread. It further offers a practical adjustment parameter which provides a powerful complexity-performance trade-off that can be used to adjust the power-consumption based on the current environment conditions.
- A **novel complex sub-sampling architecture** for wideband mmWave receivers unites the advantages of a sub-sampling receiver with the flexibility of direct-conversion architectures. Complex sub-sampling lifts the biggest limitation of current sub-sampling receivers by allowing free placement of the passband signal. A digital compensation

scheme is proposed to reduce the precision requirements on the analog components making the architecture suitable for applications with high linearity requirements. The compensation scheme can be integrated in the existing signal-processing architecture with minimal overhead. The feasibility of the sub-sampling architecture and the calibration scheme is demonstrated with a versatile mmWave hardware testbed. The flexibility of complex sub-sampling enables new low-power receiver architectures.

- **Information-driven waveform design** improves the spectral-efficiency for high modulation order directional mmWave links. Shaped constellations offer a significant performance improvement over the currently used equidistant modulations. It is demonstrated in simulation and on real-world hardware that amplitude phase-shift keying (APSK) modulations can achieve significantly higher mutual information values compared to square quadrature amplitude modulation (QAM) over mmWave transmissions. The mutual information advantage of APSK can be transformed with a bit (-interleaved) coded modulation (B[I]CM)<sup>3</sup> scheme using Polar codes into a bit error rate (BER) and a packet error rate (PER) advantage. It is shown, that the best coding performance is achieved with Polar codes that are constructed specifically for APSK constellations.

### 1.5 Outline of the Thesis

In Chapter 2, the use of mmWave for high-speed wireless local area networks (WLAN) is investigated. Propagation conditions and possible application scenarios are presented and their implications for the baseband design are discussed. Afterwards, 60 GHz-specific details of the IEEE 802.11ad single-carrier PHY definition are outlined. Performance and implementation differences of time-domain and frequency-domain baseband processing are analyzed. Based on the discussion two very different equalizer architectures are presented. A versatile frequency-domain equalization based architecture is compared to a power-adaptive time-domain DDFSE architecture. Based on the DDFSE algorithm a time-domain IEEE 802.11ad baseband application-specific integrated circuit (ASIC) implementation is presented and manufacturing results are given.

A new IF architecture for wideband mmWave receivers based on complex sub-sampling is proposed in Chapter 3. First, the basic idea of the architecture is presented assuming ideal components. Afterwards, a low-complexity compensation method is presented that allows the use of non-ideal components and makes the architecture feasible for practical receivers.

In Chapter 4, a 60 GHz hardware testbed based on the proposed complex sub-sampling architecture is described. The signal quality of the testbed and the influence of non-ideal components are characterized and discussed. Afterwards, a practical calibration scheme to measure and correct the influence of non-idealities is proposed and its effectiveness demonstrated. The trade-offs related to the sub-sampling and the necessary impairment compensation scheme

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<sup>3</sup>B[I]CM is used in a general sense for systems in which the channel code operates on bits with or without an explicit interleaver.

are analyzed and put into a system context.

The following Chapter 5 discusses the penalty in spectral efficiency of current wireless systems, as a result of suboptimal equidistant modulation. The theoretical results for shaped constellations are applied to practical bit-coded systems and the achievable gain in numerical simulations and on the testbed hardware is evaluated. Based on this work the use of polar codes, a novel class of error correction codes, for such shaped mmWave modulations is analyzed. A method on how to integrate polar codes in practical high order modulated communication systems is proposed and its effectiveness demonstrated.

Finally in Chapter 6 the findings of the different topics covered in this thesis are summarized and conclusions are drawn.

## 1.6 Third-Party Contributions

At the beginning, I would like to address the different contributions from other people to this work in more detail.

For the work on parameter synchronization algorithms and phase noise my student Radoslav Pantic contributed simulations and algorithmic improvements. My student Sara Rodriguez-Erea performed many simulations showing the feasibility and possible savings of the energy-proportional FDE. She has also developed the various ways to graphically depict the savings, which I have gladly adopted.

The presented IEEE 802.11ad baseband was designed in a collaboration between myself, Alessandro Cevrero from LSM at EPFL and Paul Wei-Chang from the group of Prof. Jou at NCTU. The group at NCTU contributed not only the digital synchronization code of the baseband, but also the physical implementation flow. Alexios Balatsoukas-Stimmig and Christian Senning further contributed register transfer level (RTL) code to the baseband design.

My student Lorenz Koestler programmed significant parts of the MATLAB code especially for the hardware interface of the mmWave testbed presented in Chapter 4. He also performed many measurements and characterizations which contributed to the foundations of the testbed. The development of the testbed profited also from the work of my student Abbass Hammoud who significantly contributed to the initial bring-up and first trials of the transceiver boards.

Many of the graphical depictions would have overburdened my artistic skills and have been designed using elements from [OpenClipArt.org](https://openclipart.org) under a public-domain license [29].

### 1.7 Notation

Throughout this work, vectors and matrices are designated with boldface lower- and boldface uppercase letters, respectively. The  $i$ -th element of a vector  $\mathbf{h} = [h_0 \dots h_{N-1}]$  is denoted  $h_i$  and  $\mathbf{h}^T$  its transpose. We write the  $N \times N$  identity matrix as  $\mathbf{I}_N$ , while  $\mathcal{F}$  denotes the Fourier transform in general,  $\mathcal{F}_N$  is used for the discrete Fourier transform (DFT) matrix of size  $N \times N$ .

A complex number  $x \in \mathbb{C}$  is defined as  $x = a + jb$  with  $a, b \in \mathbb{R}$  and  $j^2 = -1$ , while its complex conjugate is denoted with an overline, e.g.,  $\bar{x} = a - jb$ . Consequently,  $\Re\{x\} = a$  and  $\Im\{x\} = b$  are real and imaginary parts of  $x$ , respectively. The set of complex integers  $\mathbb{C}\mathbb{Z}$  is defined as  $a + jb$  with  $a, b \in \mathbb{Z}$ .

For the discussion of signals, the following notation will be used. Time-domain signals are denoted with a lower case and frequency-domain signals with an upper-case designator. Continuous-time signals are written with parentheses while discrete-time signals have brackets surrounding the time index. Hence, the discrete-time samples  $x[n]$  of the continuous-time signal  $x(t)$  are found as  $x[n] = x(n/f_s)$  with  $f_s$  being the sampling rate. To avoid confusion, the subscript  $c$  can be added to a frequency-domain signal to emphasize that the signal is the Fourier transform of a continuous time-domain signal. For the Fourier transform  $X_c$  of a  $\omega_l$  bandlimited signal holds that  $X_c(f) = 0, |f| \geq \omega_l/2$ . The  $2\pi$ -periodic expansion of a  $-\pi < \omega < \pi$  band-limited signal  $X(\omega)$  is denoted with a tilde as  $\tilde{X}(e^{j\omega}) = \sum_{i=-\infty}^{\infty} X(\omega - 2\pi i)$ .

In general,  $\log_b$  denotes the logarithm to the base  $b$ , if no explicit base is given it is assumed that  $\log = \log_2$  and  $\ln = \log_e$ . Hexadecimal numbers are formatted with the prefix 0x in pairs of two, e.g., decimal 43 corresponds to 0x2B.

## 2 mmWave Wireless LAN Receiver

Of all the applications envisioned for mmWave, high-speed Wi-Fi in the 60 GHz band is the one where development has progressed the most. One of the principal system decisions is whether future mmWave Wi-Fi systems should be based on single- or multi-carrier transmission. The various 60 GHz standards specify single carrier (SC) and orthogonal frequency-division multiplexing (OFDM) operating modes and the first 60 GHz Wi-Fi and HDMI streaming devices have been OFDM-based. However, these early OFDM-based mmWave designs commonly suffered from high power consumption [30].

Therefore, current development focuses more on SC transmission mode, which promises more degrees of design freedom for low power receivers. SC transmission has seen a remarkable revival in recent years not only for mmWave systems, but also for wireless communication in the sub-6 GHz spectrum. The current LTE standard uses a variation of single-carrier transmission called single carrier frequency-division multiple access (SC-FDMA) for a flexible and power-efficient uplink [6]. FDE allows SC systems to operate under similar delay spread conditions as OFDM systems with only a small penalty in ergodic capacity [31]. The performance disadvantage to OFDM is outweighed by the fact that SC systems have a well-controlled time-domain waveform with a lower peak-to-average power ratio (PAPR) which requires less power amplifier (PA) back-off and allows more power-efficient analog frontends. It was shown by Tubbax et al. [32] for Wi-Fi systems that SC transmission results in more power-efficient receiver designs compared to OFDM-based systems, as the overall power consumption is dominated by the analog frontend.

Because of the time-domain representation of the information, SC transmission systems offer also a higher flexibility for the baseband receiver design. The minimal required complexity for demodulation of SC transmission is significantly lower compared to OFDM which always entails the overhead of the FFT. Under frequency flat channel conditions, when no or little equalization is required, SC receivers<sup>1</sup> can reduce the filter length of the equalizer to save power. Hence, SC offers the potential for energy-proportional operation, which means that the

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<sup>1</sup>This applies not to SC-FDMA receivers.

Table 2.1 – Attenuation of radio waves in dB due to absorption for 2.4 GHz, 28 GHz, and 60 GHz.

|         | gases     |            | atmosphere   |             | foliage   |           |
|---------|-----------|------------|--------------|-------------|-----------|-----------|
|         | $O^2$ /km | $H^2O$ /km | sea level/km | 4km alt./km | 10m dist. | 50m dist. |
| 2.4 GHz | 6E-3      | -          | <0.02        | <0.005      | 8.2       | 21.6      |
| 28 GHz  | 1.75E-2   | 8.5E-2     | 0.15         | 0.015       | 17.1      | 45.1      |
| 60 GHz  | 15        | 1.75E-1    | 15           | 5           | 21.6      | 56.7      |

receiver can adapt its power consumption to the channel complexity, and therefore, always operates close to a pareto optimum between equalization performance and energy efficiency.

This chapter starts with a discussion of the established propagation characteristics and the channel models for 60 GHz wireless communications. Afterwards, details of the frame format and modulation defined in the IEEE 802.11ad standard are given as reference and its implications for receiver design are discussed. The following section provides an overview of the different receiver designs proposed for mmWave, outlining in particular the differences between receivers which are based on time-domain and receivers based on frequency-domain signal processing. First an analysis of a FDE architecture and its integration in the mmWave baseband processing is given. Subsequently, a time-domain reduced state sequence estimator based on the DDFSE algorithm is discussed and a suitable VLSI architecture is proposed. Finally, implementation results for a complete IEEE 802.11ad CMOS baseband design based on the aforementioned DDFSE detector are presented.

## 2.1 mmWave Environment & Standards

The transition of wireless communication from sub-6 GHz to mmWave frequencies brings an increase in carrier frequency and channel bandwidth by more than an order of magnitude. Hence, at mmWave channel conditions and propagation characteristics are drastically different from conventional sub-6 GHz systems. In particular, the propagation characteristics at mmWave frequencies have a significant influence on signal attenuation and delay spread in different usage scenarios and the system design of mmWave receivers.

### 2.1.1 Free Space Path Loss and Array Gain

Analysis of the path loss behaviour of mmWave transmissions requires the differentiation between an attenuation of mmWave frequencies by the environment and the frequency-dependency of the free-space path loss (FSPL). Higher attenuation of mmWave signals is caused by increased absorption of radio waves by the atmosphere, rain, foliage, and buildings. Absorbed energy is lost and therefore, fundamentally limits the achievable range. The different attenuation values for different frequencies due to absorption according to [33] are listed in Tbl. 2.1. It can be seen that 60 GHz communication faces a significant attenuation by the

Table 2.2 – Attenuation of radio waves in dB/km due to rain for 2.4 GHz, 28 GHz, and 60 GHz.

|         | 1.25 mm/h | 5 mm/h | 50 mm/h | 100mm/h |
|---------|-----------|--------|---------|---------|
| 2.4 GHz | -         | -      | -       | 0.02    |
| 28 GHz  | 0.2       | 1      | 10      | 19      |
| 60 GHz  | 0.8       | 3      | 16      | 35      |

atmosphere. However, the 15 dB/km of attenuation are not relevant for applications below 100 m. Foliage on the other hand can have a significant influence on the propagation and shows a strong frequency-dependency. Blockage by foliage over a distance of 10 m, which is equivalent to one big tree, will cause a 13.4 dB higher attenuation at 60 GHz compared to 2.4 GHz. Rain can also be a significant factor for propagation in outdoor environments. In Tbl. 2.2 the attenuation per km for different rain strengths are listed according to [33]. Rain has a significant influence on the propagation, though fatal attenuation due to torrential rains would be rare in most parts of the world. Hence, Wi-Fi coverage using mmWave technologies is not a recommended solution for parks and forests, but propagation characteristics indicate it is suitable for large indoor spaces and unobstructed outdoor areas.

The FSPL describes not the absorption of energy, but its distribution in space from an antenna perspective. The FSPL is given by Friis transmission equation [34] for a signal with wavelength  $\lambda$  that is transmitted over a distance  $R$  as

$$\frac{P_r}{P_t} = G_t G_r \left( \frac{\lambda}{4\pi R} \right)^2 \quad (2.1)$$

with  $\frac{P_r}{P_t}$  being the path loss defined as ratio between received and transmitted power.  $G_t$  and  $G_r$  are the transmit (TX) and receive (RX) antenna gain relative to an isotropic antenna with unit gain. It is important to note that the path loss in this case is logically defined as a gain.

Evaluating (2.1) for two systems operating at 2.4 GHz band and at 60 GHz with otherwise identical parameters gives a constant factor

$$\Psi = \left( \frac{2.4 \text{ GHz}}{60 \text{ GHz}} \right)^2 = 0.0016 = -29.7 \text{ dB}, \quad (2.2)$$

between the FSPLs. This calculation suggests that a 60 GHz system will face nearly 30 dB more FSPL. The pitfall of this factor  $F$  is that it assumes that the antenna gains  $G_t$  and  $G_r$  remain constant as the frequency is increased.

As was pointed out in [35] (2.1) can be split into an effective RX antenna aperture area and an energy density part as

$$\frac{P_r}{P_t} = G_t \underbrace{\left( \frac{\lambda^2}{4\pi} \right)}_{\text{effective area}} G_r \underbrace{\left( \frac{1}{4\pi R^2} \right)}_{\text{spherical surface}}. \quad (2.3)$$



In fact, not the propagation of the transmitted signal is frequency dependent, but only the effective antenna area of a unit-gain RX antenna. The electromagnetic energy of an isotropic radiator distributes evenly on the surface of the sphere independent of its actual frequency. The difference is that at 60 GHz an antenna of a similar complexity would only capture a smaller area out of this sphere (i.e., has a smaller aperture), but such an antenna would also be physically smaller in size. The total effective antenna area and therefore, the RX antenna gain can be increased by using multiple antennas and coherent combining.

From a system level perspective, a mmWave receiver can achieve the same effective area by using an RX antenna array and beam-forming (BF). Such an antenna array would capture the same amount of energy and require similar physical dimensions, compared to a single antenna at 2.4 GHz. Further, the antenna array would exhibit a higher antenna gain and therefore, show more directivity. In fact the effective area argument can be extended to the TX side, since a mmWave transmit antenna array of the same effective area can also accommodate significantly more TX antennas. Therefore, a mmWave system can leverage the large number of transmit antennas in order to perform TX BF and profit from an additional TX antenna array gain of the same magnitude as the RX antenna array gain [35]. Assuming a constant effective aperture on TX and RX side a mmWave system would have in fact a lower free-space path loss compared to a sub-6 GHz system due to an effectively higher  $G_t$  and  $G_r$ .

The use of TX and RX BF results in high spatial selectivity and high spatial reuse for mmWave systems. Simulations presented in [36] suggest that in indoor cubicle office-scenarios a single channel can accommodate up to seven concurrent mmWave Wi-Fi connections when  $6 \times 6$  antenna arrays are used on TX and RX side, offering a capacity gain through space-division multiple access (SDMA).

Unfortunately, any BF gain does not come for free. Finding the appropriate set of antenna parameters is a complex problem, especially when BF is applied on both sides. Today's BF systems typically offer a predefined subset of antenna patterns, from which all combinations on TX and RX side need to be tried in order to determine the optimal setting. However, not only the initial establishment of a link is challenging, but also the continuous tracking of the optimal BF parameters is not trivial. In the case of varying channel conditions, continuous training can consume a significant portion of the link resources. Though recent research [37] suggests that the antenna parameters are correlated and this correlation can help in predicting suitable antenna patterns.

### 2.1.2 60 GHz Indoor Channel Models

Different channel models have been specified for 60 GHz indoor applications. The TG3c taskgroup in charge of the IEEE 802.15.3c standardization effort has published an initial set of channel models [38][39] for various 60 GHz scenarios. The TG3c channel model specifies the following scenarios:



- Residential
- Office
- Library
- Desktop
- Kiosk

The channel model of the TGad taskgroup[40] for the IEEE 802.11ad standard is technically similar to the one of the TG3c, but more focused on beam-forming and typical mmWave Wi-Fi environments. The IEEE 802.11ad channel model specifies the following scenarios:

- Living Room (LR)
- Cubicle Office (CB)
- Conference Room (CR)

The IEEE 802.11ad channel model will be used throughout this work. All channel models can be configured with or without a direct path from TX to RX, leading to a line-of-sight (LOS) or non line-of-sight (NLOS) situation. The presence of a LOS path has significant impact on the channel characteristics, as it leads to a nearly frequency flat channel spectrum.

The IEEE 802.11ad channel model is implemented using statistical ray tracing in time-domain. The channel model rounds the randomly generated arrival times of the incident rays to the next time instance on the discrete time grid. Hence, even for symbol-spaced systems, the channel realizations need to be generated with over-sampling in order to get sufficient temporal resolution. For the simulations in this thesis an over-sampling factor of 10 is used for channel generation. After the RX pulse shape filter is applied, the channel realization is decimated to the symbol-spaced signal.

The TGad channel model includes also a path loss component, but for the simulations performed in this work the channel energy is always normalized to unity. This is justified as it is assumed that sufficient antenna gain is achieved by the antenna frontend and allows algorithms to be evaluated as a function of the SNR rather than the link distance. Otherwise performance could only be indicated as a function of the distance between transmitter and receiver and a comparison between channel models would be complicated.

The use of BF has implications for the baseband design. In Fig. 2.1 a comparison of ten randomly drawn channel realizations from the TGad LR NLOS channel model are shown with and without BF. In both scenarios, the channel impulse responses are normalized to unit energy and aligned to the strongest component. The channel realizations provide an intuition of the implication of BF on the delay spread. The observed excess delay spread

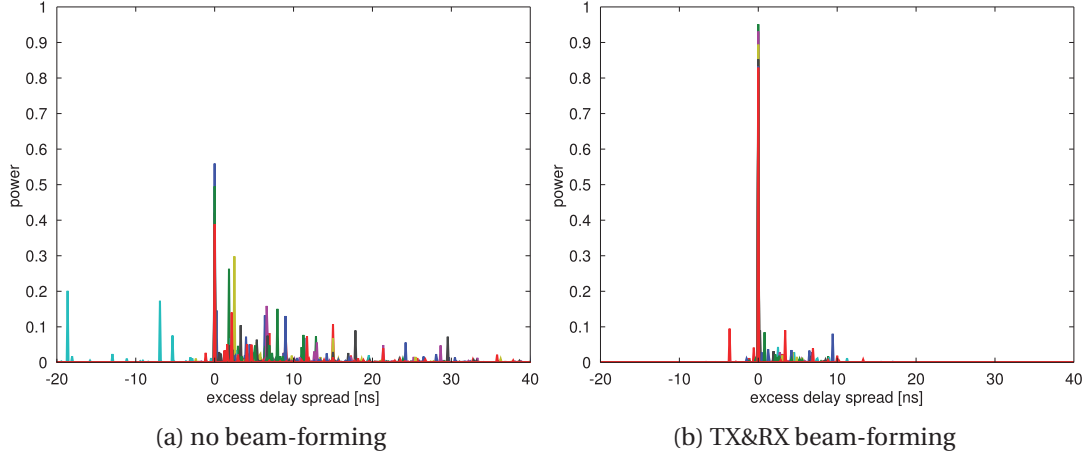


Figure 2.1 – Comparison of ten random LR NLOS channel realizations with and without BF

varies significantly between ten and forty nano-seconds depending on whether or not beam-forming is used. In mmWave receivers the establishment of the optimal BF pattern is not expected to be instantaneous, but an iterative process. Hence, an implementation needs to face a range of intermediate conditions. A smooth user experience will depend on the capability of the receiver to operate under all conditions.

### 2.1.3 60 GHz Wireless Communication Standards

Several standards have been defined for wireless local area network (WLAN) communication in the 60 GHz band. Due to the abundance of spectrum in the mmWave bands, initial 60 GHz standards combine large bandwidths with low modulation orders in order to achieve the required throughput. This is very different to the evolution of Wi-Fi in the traditional 2.4 GHz and 5 GHz bands, e.g., IEEE 802.11ac [41], which focuses on increasing the spectral efficiency with high order modulation and MIMO techniques, since the available bandwidth is severely limited.

WirelessHD [21] was the first commercial standard based on OFDM and was targeted at wireless HDMI video-cable replacement. Hardware supporting the WirelessHD standard is commercially available [30]. While the competing ECMA-387 [42] standard also provides an HDMI cable replacement mode, it never found adoption. The mmWave extension of the WPAN standard IEEE 802.15.3c [20] resonated well with the scientific community, but was not developed into products. An industry-driven development led to the creation of the IEEE 802.11ad [23] standard, a mmWave extension of the widely adopted IEEE 802.11 Wi-Fi standard.

The system parameters and channel models of the IEEE 802.11ad standard will be used for the system design and the simulations in this work. A comparison of the IEEE 802.11ad standard with IEEE 802.15.3c shows many similarities between the two. Both standards have

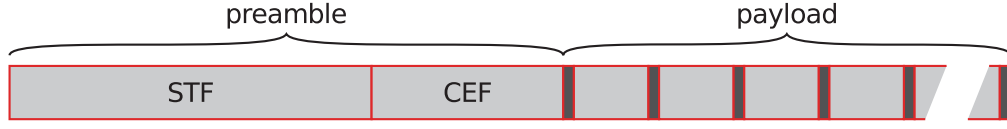


Figure 2.2 – Considered frame format according to the IEEE 802.11ad standard.

a harmonized channel structure with a symbol rate  $f_{\text{symbol}}$  of 1.76 giga-symbol per second (Gs/s) for the SC mode. The signal is centered in one of four channels with a bandwidth of 2.16 GHz each.

Similar synchronization and channel estimation strategies of the two standards have led to designs that support the characteristics of both standards [43][44][45][46][47], though the IEEE 802.11ad standard is leaner and more focused on simple implementation. Many configuration options available in IEEE 802.15.3c were dropped for the IEEE 802.11ad standard, e.g., the use of different error correction schemes or the optional support for non-quadrature modulation. Furthermore, the use of beam-forming for increased link reliability and throughput was assumed from the beginning of the standardization process of IEEE 802.11ad [48].

#### 2.1.4 IEEE 802.11ad Single-Carrier Frame Format

The basic single-carrier frame format considered in this work is shown in Fig. 2.2, it consists of an initial preamble used for parameter synchronization, followed by the payload body. The frame format matches the one defined in the IEEE 802.11ad standard, except for the header field which is not explicitly considered. The header field, specified in the standard, is omitted as it exhibits the same basic structure as the payload field with the only difference that it is always modulated in BPSK.

##### Preamble

The preamble at the beginning of each frame comprises a short training field (STF) and a channel estimation field (CEF). The STF (cf. Fig. 2.3a) consists of 16 repetitions of the 128 symbol long  $G_{b_{128}}$  Golay sequence, terminated by a  $-G_{b_{128}}$  sequence. The STF provides a periodic structure of 2048 symbols length at the beginning of the frame for blind synchronization.

The CEF shown in Fig. 2.3b consists of a pair of complementary Golay sequences  $G_{v_{512}}$  and  $G_{u_{512}}$ , which are terminated with a  $-G_{b_{128}}$  sequence. Because of the recursive construction scheme of Golay sequence pairs the two complementary sequences  $G_{v_{512}}$  and  $G_{u_{512}}$  can be

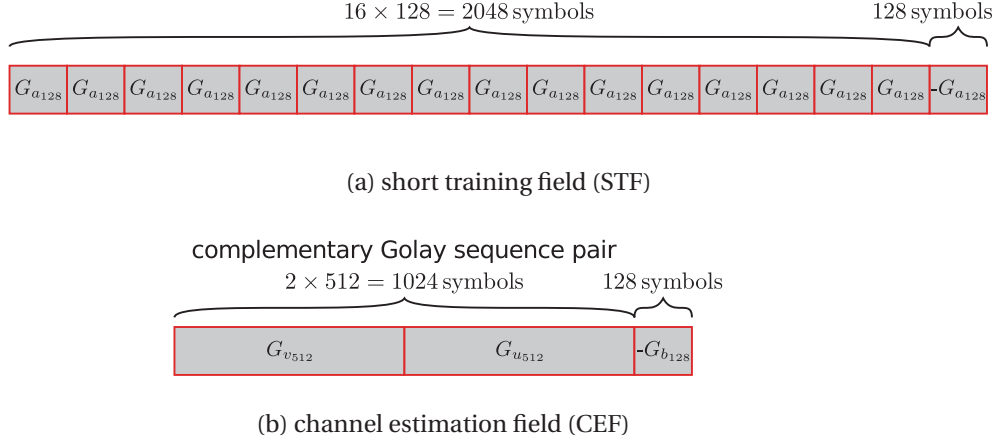


Figure 2.3 – The short training field (STF) and the channel estimation field (CEF) of the IEEE 802.11ad single-carrier preamble.

disassembled into a sequence of shorter complementary Golay sequences of length 128 as

$$G_{v_{512}} = [-G_{b_{128}} \ G_{a_{128}} \ -G_{b_{128}} \ -G_{a_{128}}] \quad \text{and} \quad (2.4)$$

$$G_{u_{512}} = [-G_{b_{128}} \ -G_{a_{128}} \ G_{b_{128}} \ -G_{a_{128}}]. \quad (2.5)$$

Hence, channel estimation can be performed using a Golay correlator for the shorter sequence pair  $G_{a_{128}}/G_{b_{128}}$ . The termination at the end of the CEF ensures that both fields are periodic.

### Payload

The payload field of the frame format exhibits a distinct block structure. The data symbols of the payload are segmented into blocks by periodically inserted pilot words. Each pilot word consists of the same BPSK modulated binary Golay sequence of length 64.

The payload field is started by an initial pilot word, afterwards the data symbols are grouped into blocks of 448 data symbols followed by a pilot word. The pilot word acts as guard interval to avoid inter-symbol interference (ISI) spill from one block into another. This can be helpful for equalizers that suffer from error propagation, as with the beginning of every block detection can be restarted. Independent of the receiver architecture, the guard interval allows independent processing of the blocks. High-throughput baseband architectures can make use of this property by parallelizing the block processing. The guard interval also serves as a cyclic prefix for single carrier frequency-domain equalization (SC-FDE), as it ensures a cyclic convolution of the data symbols with the channel. The use of a pilot word, sometimes also called unique word, for the guard interval has the advantage that it can be used for data-aided synchronization [49].

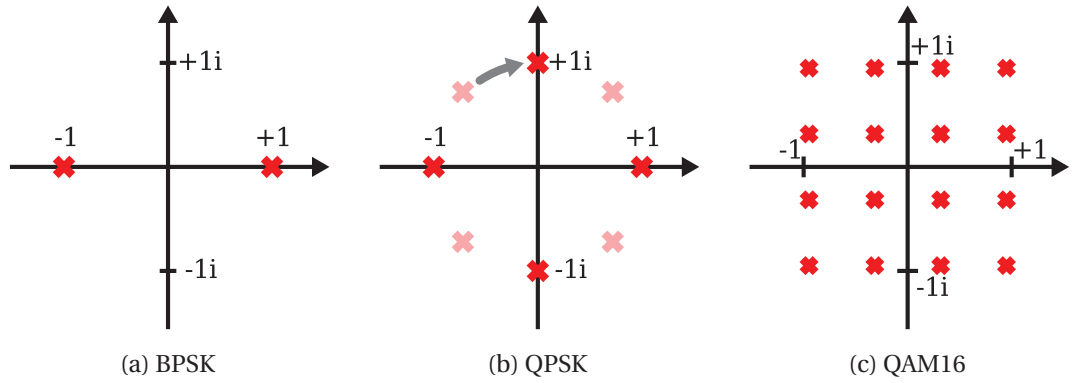


Figure 2.4 – BPSK-/QPSK-/QAM16-Constellations of the IEEE 802.11ad standard.

### $\pi/2$ -Rotating Modulation

The IEEE 802.11ad standard specifies BPSK, QPSK, and QAM16 modulation for the single-carrier mode. The different constellations are shown in Fig. 2.4. The QPSK constellation, shown in Fig. 2.4b, shows a  $45^\circ$  angular offset compared to conventional QPSK constellations. Because of this change, the BPSK constellation points are a subset of the QPSK alphabet, which simplifies the receiver design.

In addition to the fixed angular rotation of the QPSK constellation, the standard specifies a continuous  $\frac{\pi}{2}$  rotation for all modulations. The constellations of successive symbols are rotated by  $\frac{\pi}{2}$  relative to each other. Consequently, the modulations are called  $\frac{\pi}{2}$ -BPSK,  $\frac{\pi}{2}$ -QPSK and  $\frac{\pi}{2}$ -QAM16 in the standard.

The rotation ensures that real-valued BPSK symbols are spread over both dimensions of the complex constellation plane and thereby improves the spectral properties of the transmitted signal. The  $\frac{\pi}{2}$ -rotation can be applied and removed completely agnostic to the actual modulation and demodulation. The already modulated discrete symbols at rate  $f_{\text{symbol}}$  can be multiplied at the output of the frame assembly with a  $\frac{f_{\text{symbol}}}{4}$ -carrier. On the downside, the agnostic approach implies that the higher modulation orders have to be rotated, despite not profiting from a rotation.

The decision to describe the  $\frac{\pi}{2}$ -rotation as part of the modulation is somewhat unfortunate as it suggests a time-dependency of the modulation. In particular, for the initial synchronization this poses the question how a receiver should synchronize to this rotation. In practice, the time dependency is not problematic, as all fields of the frame have lengths that are a multiple of 4. Hence, the rotation logically “restarts” with every field and is agnostic to the modulation order used. Assuming a common phase rotation offset that is absorbed by the estimated channel impulse response, the received symbols can be rotated in the opposite direction with an arbitrary starting phase. With this scheme, the rotation is reverted before channel estimation and equalization is performed and therefore, no special provisions in the equalization and detection architecture are necessary. Yet, special care must be taken in receivers based on

fractionally-spaced samples.

### Error Correction Coding

The IEEE 802.11ad standard specifies LDPC codes [50] for error correction. The LDPC codes are defined for a single code-word size of 672 bits and four different rates ( $\frac{1}{2}/\frac{5}{8}/\frac{3}{4}/\frac{13}{16}$ ). Each code is defined by a parity check matrix with a quasi-cyclic structure [51], that facilitates high-speed decoder implementations. The code-word size of the IEEE 802.11ad LDPC codes are short compared to LDPC codes defined in other wireless communication standards like IEEE 802.11n [52] or DVB-S2X [53]. The short code length allows low-latency, high-throughput decoder implementations, but becomes problematic with high-order modulations [54].

## 2.2 Algorithms and Implementations

Algorithm design for 60 GHz receivers needs to take the specific characteristics of mmWave systems into account. Baseband receivers need to adapt to the wide range of channel conditions, while their corresponding architectures need to process Gsps rates at low complexity. Algorithms which rely on simple arithmetic operations and require minimal buffering are thus advantageous. Precalculation of intermediate values can help to reduce the system complexity, as the large frame size renders the cost of any one-time calculations negligible compared to the cost of operations that need to be applied to each symbol.

Feedback loops should be avoided as they significantly limit the implementation design space. In feed-forward structures the introduction of pipeline registers reduces the critical path with a moderate complexity increase. Feedback paths prevent pipelining and require either algorithmic transformations or re-synthesis of parts of the netlist to reduce the critical path. Both approaches reduce the critical path at the cost of a significant increase in hardware complexity. In small technology sizes such an increase in complexity and area, comes with a notable increase in interconnection delay, which reduces the effectiveness of any optimization.

### 2.2.1 Time-Domain vs. Frequency-Domain Architectures

Previously proposed 60 GHz single-carrier baseband designs can be categorized in two classes, based on whether the equalizer is realized in TD or FD. Both classes of designs have their distinct advantages. TD receivers can in general better adapt their complexity to the channel conditions, in particular the excess delay spread. The length of the equalization filter can be adjusted to the instantaneous delay spread length by disabling parts of the circuit in order to realize power savings. The capability to adapt receiver complexity to the length of the delay spread is called energy-proportional operation and is crucial for energy efficient receiver operation under varying channel conditions. FD based receiver designs can usually not adapt their complexity. However, FD receivers can better handle long delay spreads that would be

computationally infeasible for TD receivers. As a result, FD receiver operate in more scenarios and show a better link reliability, in return for a higher average power consumption.

The ability to adjust the number of filter elements (or taps) and the possibility to integrate analog signal processing, allows TD implementations with very low power consumption. Many of the proposed time-domain receiver architectures are based on short linear time-domain filters which are combined with a low-complexity decision feedback equalizer (DFE). Such designs are inspired by low-power design techniques known from wired high-speed serial links, which operate at similar symbol rates. Hence, most receiver designs assume channel characteristics similar to the ones observed in serial link environments, which may not be a valid assumption for some mmWave scenarios.

In [55], Marcu et al. have demonstrated a 60 GHz receiver with a single tap phase rotator and a 5 tap mixed-signal DFE. A factor of two oversampled receiver design based on a phase rotator and an analog 16 tap DFE was shown by Sobel and Brodersen in [56]. The potential for energy-proportional operation of TD receivers has been demonstrated by Park et al. [27] with a design based on a digital linear equalizer and mixed-signal DFE. For frequency-flat channels this receiver can reduce power consumption below 10 mW. However, the design can operate only on a limited set of NLOS channels. Another low-complexity time-domain scheme was presented by Liu et al. [44] as multi-path interference cancellation (MPIC). MPIC is essentially a linear equalization scheme based on the assumption that many mmWave channels are dominated by a strong LOS path and a significantly weaker subsequent path. The use of long analog filters to overcome the length limitation of digital TD filter implementations was proposed by Thakkar et al. in several publications. First, a design composed of a single phase rotator and a 40 tap DFE was shown in [57], later a 32 tap analog feed forward equalizer combined with a 100 tap DFE was presented in [58].

Frequency-domain based equalization has been suggested by Daniels et al.[59] as a powerful technique to deal with the long delay spread in mmWave systems. The feasibility of single carrier frequency-domain equalization (SC-FDE) for IEEE 802.15.3c has been analyzed by Lei et al. in [60] and [61] using numerical simulations. Implementations of SC-FDE for mmWave have been demonstrated using field-programmable gate arrays (FPGAs) in [62] and with a reduced rate in [63]. An ASIC implementation of an SC-FDE based receiver has been shown by Hsiao et al. [64]. This design performs a 512 point FFT for the transformation from-and-to frequency-domain as well as the MMSE criterion for the equalization filter. An adaptive SC-FDE equalization scheme was proposed by Yeh et al. [43]. Another frequency-domain based baseband architecture for IEEE 802.11ad was presented by Saito et al.[65]. The authors suggest a 128-point overlap-save frequency-domain equalizer in order to achieve a complexity reduction compared to a full 512-point FFT. The reduced length frequency-domain equalizer also includes low-pass filtering and decimation.

A conclusive comparison of time-domain and frequency-domain approaches requires a system perspective on the receiver. A baseband receiver does not only perform channel equalization,

synchronization and error decoding are also an integral part of the baseband signal processing. The merger of operations and the reuse of hardware resources has the potential to increase the system efficiency and is not captured by a mere comparison of equalizer complexities. While SC-FDE requires a significant overhead for the necessary Fourier transform, the obtained frequency-domain samples allow additional baseband signal processing with reduced complexity.

### 2.2.2 Synchronization

Correct synchronization under all operating conditions is crucial for the reliable operation of a wireless receiver. Discussion of the parameter synchronization is also a helpful introduction to the system level challenges of mmWave receiver design. Synchronization establishes a common time and frequency reference between transmitter and receiver at the beginning of each transmission to allow coherent communication. The quality of the initial parameter estimation has significant impact on the overall performance.

Different digital synchronization architectures have been proposed for 60 GHz. In [66] and [67] architectures based on Frank-Zadoff sequences for channel estimation with and without over-sampling are suggested for SC-FDE receivers. A symbol-spaced multi-standard synchronization design in [46] proposes a reduced length correlation for frame synchronization and interpolation for sampling-point correction.

The process of synchronization is divided into the following main tasks,

- **Packet detection** determines the presence of the periodic zone of the STF in the received sample stream.
- **Sampling phase alignment** determines the optimal sampling phase which maximizes the effective SNR and reduces the delay spread of the effective channel.
- **Frequency synchronization** estimates the frequency offset between the clocks in the transmitter and in the receiver.
- **Frame synchronization** determines the start of the CEF within the preamble.
- **Channel estimation and alignment** acquires a precise estimation of the channel impulse response  $h$ , which is used to determine a synchronization point.
- **Phase-noise (PN) tracking** estimates the instantaneous phase deviation due to phase noise and a residual frequency offset.

While the different tasks are logically distinct, an implementation can perform multiple steps in parallel.



### System Model

The  $N$  transmitted symbols  $\mathbf{x} = [x_0, \dots, x_{N-1}]$  experience a frequency-selective channel with a time-domain impulse response  $\mathbf{h} = [h_0, \dots, h_{L-1}]$  of length  $L$ . Without loss of generality it can be assumed that the power of each realization of  $\mathbf{h}$  is normalized to unity.

Initially, synchronization is considered for a symbol-space sampled design where the sampling rate  $f_s$  equals the symbol rate  $f_{\text{symbol}}$ . For such a design the received samples are given as

$$r_k = \left( \sum_{i=0}^{L-1} x_{k-i} \cdot h_i \right) e^{j(2\pi k f_{\text{offset}}/f_s + \phi_k)} + w_k \quad (2.6)$$

$$= \hat{r}_k e^{j(2\pi k f_{\text{offset}}/f_s + \phi_k)} + w_k, \quad (2.7)$$

where  $w_k$  is white Gaussian noise with zero mean and variance  $\sigma_w^2$ ,  $f_{\text{offset}}$  is the carrier frequency offset (CFO) and  $\phi_k$  is the time-varying phase deviation due to phase noise. During the discussion of the synchronization, the impact of a sampling frequency offset on the received samples is omitted from the equations in order to keep the notation simple. The sampling frequency offset becomes critical when samples are related to each other over distances significantly longer than the preamble. It is further assumed that the coherence time of the phase-noise is significantly longer than the delay spread which allows to consider phase-noise on the receiver side only. For selected parts of the synchronization, also the situation of an oversampling factor  $R^{\text{OS}} = \frac{f_s}{f_{\text{symbol}}}$  larger than 1 is discussed.

### Packet Detection

The repetition of the  $G_{b_{128}}$  sequence at the beginning of the STF results in a periodic structure with a period of  $D = 128$ . This periodic property can be detected by performing an autocorrelation of the received samples at a distance  $D$ . The auto-correlation  $P_k$  is calculated over a window of length  $D$  as

$$P_k = \sum_{i=0}^{D-1} r_{k+i} \overline{r_{k+D+i}}. \quad (2.8)$$

For a simplified system model without frequency offset or phase noise (2.6) reduces to

$$r_k = \sum_{i=0}^{L-1} x_{k-i} \cdot h_i + w_k \quad (2.9)$$

$$= \hat{r}_k + w_k \quad (2.10)$$

and the windowed autocorrelation in the periodic zone  $P_{k|\text{in}}$  becomes

$$P_{k|\text{in}} = \sum_{i=k}^{k+D-1} |\hat{r}_i|^2 + (\hat{r}_i \overline{w_{i+D}} + \overline{\hat{r}_i} w_i) + (w_i \overline{w_{i+D}}). \quad (2.11)$$

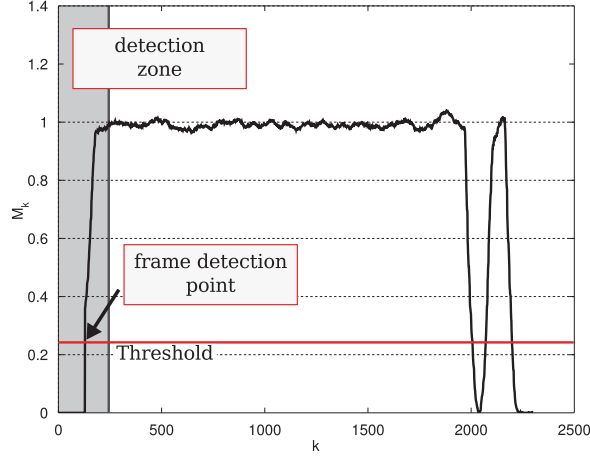


Figure 2.5 – Windowed and squared normalized autocorrelation signal  $M_k$  at distance  $L = 128$  of the received STF with the threshold for detection.

The signal energy terms  $|\hat{r}_i|^2$  add up coherently over the autocorrelation window and the presence of a frame in the received sample stream can be detected based on the magnitude of  $P_k$ , which is insensitive to the yet unknown  $\mathbf{h}$ . Variations of the signal strength are taken into account, by performing the detection on the squared normalized autocorrelation  $M_k$  as

$$M_k = \frac{|P_k|^2}{|R_k|^2}. \quad (2.12)$$

The signal energy  $R_k = \sum_{i=0}^{D-1} r_{k+D+i} \overline{r_{k+D+i}}$  is calculated as the windowed autocorrelation of the received signal at distance 0.

The squared normalized auto-correlation  $M_k$  approaches 1 within the periodic zone of the preamble in a high SNR regime as illustrated in Fig. 2.5. Using the squared normalization in (2.12) was suggested in [68] in order to replace the computationally expensive step of calculating the magnitude of a complex number with a significantly cheaper complex multiplication.

Setting the detection threshold requires a trade-off between the probability for a false-positive detection outside the periodic zone and a false-negative (miss) detection error during the STF. For a single value of  $M_k$  the combined detection error probability can be found as a function of the threshold and the SNR using the approximation provided in [69]. The detection failure-rate as a function of the threshold is shown in Fig. 2.6 for different values of the SNR. These probabilities are calculated for a single value of  $M_k$  and are not system miss rates. Because of the length of the periodic zone, a single  $M_k$  value below the threshold at the beginning is in most cases not fatal for packet detection, but the detection will trigger at a later point of the periodic zone. The detection error probability serves as a starting point for finding the threshold, a value of 0.25 has been found to provide robust detection results and is assumed

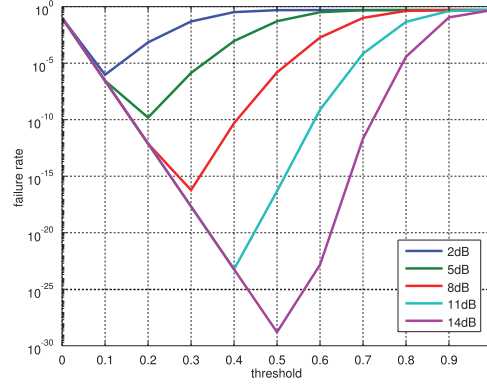


Figure 2.6 – Detection error probability for the normalized auto-correlation value  $M_k$  as a function of the threshold evaluated at different SNR.

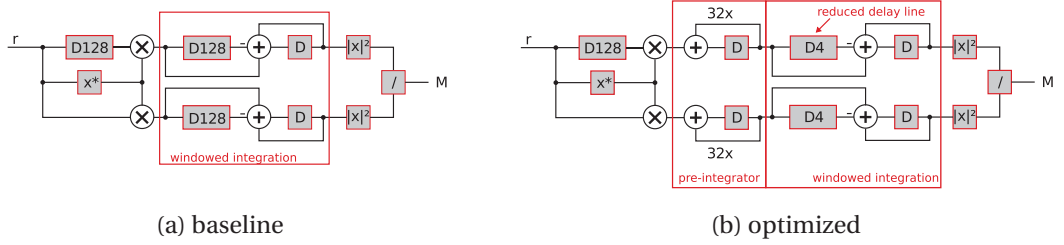


Figure 2.7 – Baseline and optimized architectures for auto-correlation based packet detection.

throughout this paper.

Auto-correlation based packet detection is based on simple arithmetic operations and allows low-complexity, high-speed VLSI implementations. The basic architecture of the correlator is shown in Fig. 2.7a. The architecture can be easily reconfigured to a varying degree of parallelism. Implementations can save significant amounts of power using the fact that successive values of  $M_k$  are highly correlated. Because of the high correlation, not every value of  $M_k$  needs to be evaluated. Instead it is suggested that  $M_k$  can be subsampled and only every 32nd value is calculated in our implementation. This reduction allows the optimized architecture shown in Fig. 2.7b which reduces the amount of active register by more than 40% during idle periods without noticeable performance loss compared to the baseline architecture. The interval can be even further increased if a detection penalty can be accepted.

The proposed packet detection scheme can also be used in oversampled systems, as the periodicity of the received signal is independent of the sampling rate. For fractionally-sampled systems the implementation is significantly simplified when the periodicity is aligned with the grid of the discrete samples meaning that the periodicity is an integer multiple of the sampling frequency. If synchronization is performed before the matched filter (MF), power can be saved by deactivating the MF during idle periods at the cost of a reduced SNR due to the noise in the excess bandwidth. For an over-sampling factor  $R^{OS} = 2$  this can result in an SNR degradation

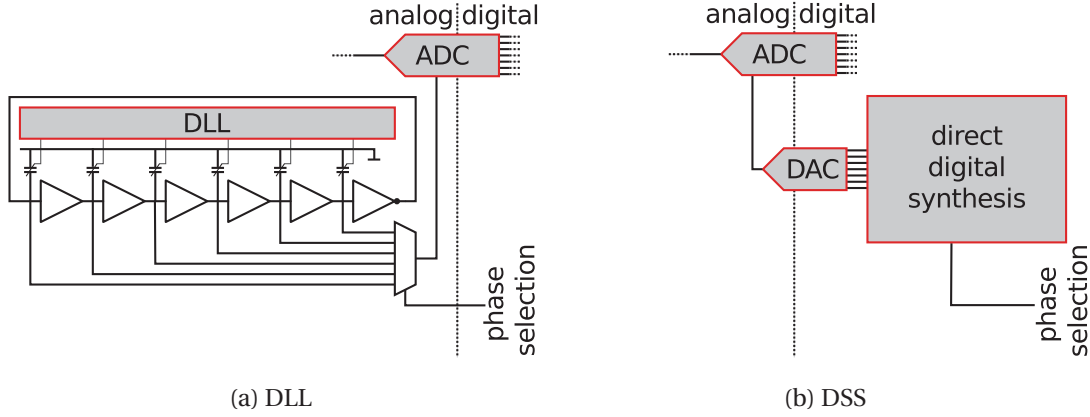


Figure 2.8 – Analog and digital sampling phase alignment using a DLL or a DSS.

of up to 3 dB, for a typical fractional over-sampling factor  $R^{\text{OS}} = 1.25$  the SNR reduction is less than 1 dB.

### Sampling Phase Alignment

The alignment of the sampling phase has a significant impact on the overall system performance in symbol-spaced systems. In fact, choosing the optimal sampling phase can not only maximize the observed SNR, but also reduces the length of the observed ISI. Especially for short-length time-domain equalizer and detector the length of the delay spread can have significant influence on the system performance.

For a frequency-flat channel, the optimal sampling point can be derived from the slope of the phase response. However, in a frequency-selective environment a full channel estimation including the excess bandwidth is necessary to determine an optimal sampling point. Unfortunately, even with knowledge of the channel estimation finding the optimal sampling point remains a challenging problem. In this section, an alternative based on a low-complexity search strategy is proposed. The optimal sampling point is approximated by evaluating a discrete set of sampling phases. After the evaluation period, the sampling phase which has led to the maximal useful signal energy is selected for the sampling of the rest of the frame.

After the initial packet detection has been established the synchronization module continues the calculation of the values for  $P_k$  and  $R_k$ . A single auto-correlation window is calculated with each of the possible sampling phases. The corresponding value of  $R_k$  is used as measure of the signal power associated to this sampling phase. Hence, instead of a sliding window, non over-lapping windows of the auto-correlation are calculated with the different sampling phases. After cycling through all phase settings the phase with the highest  $R_k$  value is used for subsequent sampling.

Adjusting the sampling clock phase to set the sampling point is the only way to maximize

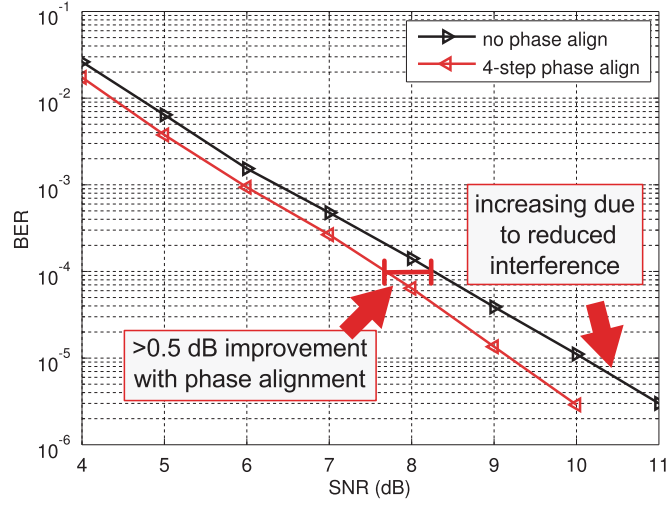


Figure 2.9 – A four step phase alignment shows a gain of more than 0.5 dB in BER system performance compared to the same system without phase alignment.

the SNR in symbol-spaced systems. Interpolation-based mechanisms suffer from an inherent degradation of performance because of the uncontrolled excess bandwidth. Different approaches have been proposed in order to adjust the phase of the sampling clock. Sampling clock adjustment using a delay-locked loop (DLL) (cf. Fig. 2.8a) was proposed in [70]. The sampling phase is changed by connecting the clock input of the ADC to the different phase outputs of the DLL. Alternatively, a direct digital synthesis (DDS) based frequency synthesizer can be used for generation of the sampling clock. DDS promises not only precise control about the phase, but can also be used to adjust the sampling frequency in very fine grained steps.

Adjusting the sampling clock improves the performance of symbol-spaced receivers in general, but can be especially helpful for time-domain receivers. A BER comparison of a finite-length time-domain receiver using decision feedback with and without sampling adjustment is shown in Fig. 2.9. The sampling phase is adjusted in only four coarse  $\frac{\pi}{2}$  steps, nevertheless a performance improvement of more than 0.5 dB can be obtained. The BER gap increases for higher SNR as not only the sampled signal energy is increased, but also ISI is reduced.

As mentioned before, sampling phase alignment is critical in systems with symbol-spaced sampling, as the sampling phase influences received SNR and delay spread. In over-sampled architectures, the sampling point adjustment can be performed after the physical sampling and before decimation in the digital signal processing and merged with the matched filter. Analog to the sampling phase optimization scheme, a discrete set of matched filters can be evaluated to determine the filter that results in the maximum signal energy for the symbol-spaced signal.

### Frequency Synchronization

The frequency-offset (FO) between transmitter and receiver is estimated indirectly via the CFO. From the CFO estimation, a common reference oscillator FO can be derived due to the fixed relationship of generated clocks in the transmitter, which is mandated by the standard [23]. The standard limits the reference oscillator deviation to below  $\pm 40$  ppm, resulting in maximum CFO of approximately  $\pm 2.5$  MHz.

For the estimation of the CFO the windowed auto-correlation signal  $P_{k|\text{in}}$  can be repurposed. The phase deviation due to PN can be assumed constant over the short correlation distance of  $D = 128$ , therefore, the phase noise term  $\phi_k$  is assumed zero for the discussion of the frequency offset such that (2.7) becomes

$$r_k = \hat{r}_k e^{-j2\pi k f_{\text{offset}} / f_s} + w_k. \quad (2.13)$$

The  $e^{-j2\pi k f_{\text{offset}} / f_s}$  term leads to a complex rotation of the received symbols over time. For a BPSK constellation, a rotation becomes disruptive as soon as the magnitude of the phase deviation  $\Phi_k = 2\pi k \frac{f_{\text{offset}}}{f_s}$  caused by the frequency offset approaches  $\frac{\pi}{2}$ . Assuming a maximal possible CFO of 2.5 MHz such an event can occur within 180 symbols. Hence, reliable detection of data is not possible without prior compensation of the CFO [71].

The CFO causes a rotation of  $P_{k|\text{in}}$  in the complex plane, but does not affect its magnitude, as (2.8) transforms into

$$P_{k|\text{in}} = \sum_{i=k}^{k+D-1} |\hat{r}_i|^2 e^{-j\Phi_D} + \hat{r}_i e^{-j\Phi_i} \overline{w_{i+D}} + \overline{\hat{r}_{i+D}} e^{-j\Phi_{i+D}} w_i + w_i \overline{w_{i+D}}. \quad (2.14)$$

The statistics of the noise terms do not change due to the circular symmetry of  $w_k$ . An estimate of  $f_{\text{CFO}}$  can be derived from the phase of  $P_{k|\text{in}}$  as

$$\hat{f}_{\text{CFO}} = \frac{\angle(P_{k|\text{in}}) f_s}{2\pi D}. \quad (2.15)$$

The influence of the noise term  $w_k$  can be further suppressed by using multiple instances of  $P_{k|\text{in}}$ . Because successive values of  $P_{k|\text{in}}$  are highly correlated, only auto-correlation values from non-overlapping windows are used for the frequency estimation. Due to the non-overlapping window, the sampling phase can change between each window and (2.14) still holds. Hence, phase alignment and frequency estimation can be performed jointly, while being in the periodic zone. The quality of the frequency offset estimation depends on the number of valid and uncorrelated  $P_{k|\text{in}}$  values calculated before the coarse frame synchronization starts.

An FO estimation error results consequently in a residual CFO term, which has a significantly smaller magnitude than the original FO, but might still lead to data corruption at some point later in the frame. This residual CFO can be tracked as part of the phase noise of the system.

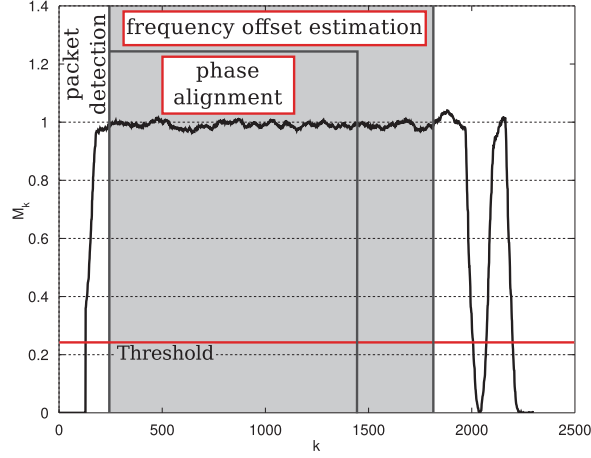


Figure 2.10 – Phase alignment and frequency estimation are performed in parallel in the periodic zone of the STF after packet detection.

Obviously, any offset between the reference oscillators in the transmitter and the receiver will not only affect the carrier- but also the sampling-frequency. Fortunately, the impact of the sampling frequency offset (SFO) is less severe compared to the CFO due to its lower frequency. In fact, the SFO is assumed to be negligible during processing of the STF field. Nevertheless, due to the accumulation of sampling offsets the sampling frequency offset (SFO) will degrade the performance of long frames. Therefore, the SFO is compensated before the channel estimation by adjusting the sampling frequency in the DDS. Residual SFO can be estimated by derivation and filtering of the phase-noise tracking signal.

In over-sampled systems, frequency offset estimation can be performed in the same way as for symbol-spaced systems. Analog to the packet detection, the implementation becomes much simpler when the STF period is an integer multiple of the sampling period. Any SFO can be digitally compensated with a phase rotation of the matched filter (see Subsection 2.3.2 for details of an FD implementation).

### Frame Synchronization

While the packet detection algorithm only identifies the presence of the periodic zone, it does not provide the location of the boundaries of the preamble fields. A more precise time reference is required to determine the start of the CEF which allows coherent detection of the frame. The normalized separated maximum correlation (NSMC) method for frame synchronization proposed in [68] is restricted to conditions in which the delay spread does not exceed the correlation sequence length of 32. This delay spread limitation is significantly stricter than what the equalization stage of various proposed FD receivers [61][43][72] can operate with and hence imposes for such receivers an artificial restriction on the operating conditions of the complete receiver.

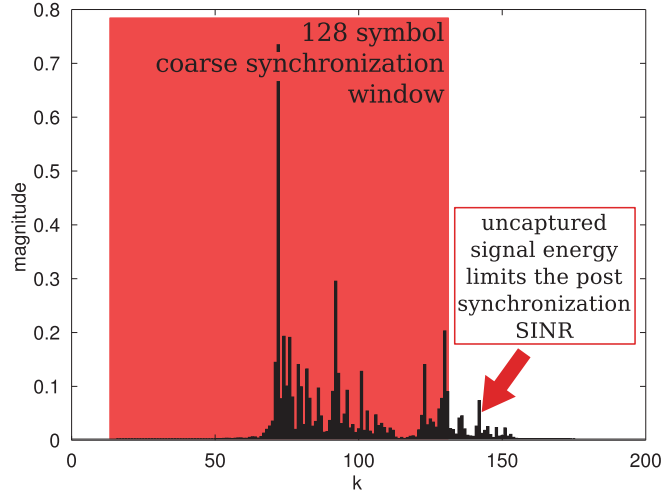


Figure 2.11 – Example of 60 GHz CIR drawn from the TGad LR NLOS channel model with coarse synchronization channel estimation window.

For a receiver that should support all possible delay spread scenarios, a more flexible approach to frame synchronization is required. Traditionally, the quality of synchronization is quantified by the offset between the estimated frame start and an ideal synchronization point. It was already observed in [66] that in scenarios with a large spread of channel energy the strongest channel tap is not always the ideal synchronization point. Instead, the optimal synchronization point strongly depends on the used receiver architecture, especially, if non-linear decision feedback equalization techniques are used.

Hence, a more general two step process for synchronization is proposed. An initial coarse frame synchronization step establishes a window for channel estimation which confines most of the channel energy. The subsequent fine frame synchronization step determines a synchronization point based on a channel impulse response (CIR) estimation and knowledge of the receiver architecture. An example of an NLOS CIR with strong delay spread is depicted in Fig. 2.11, the corresponding 128 symbol window found by coarse synchronization is marked in red and contains most of the channel energy. Signal energy, which does not fall into the estimation window, will subsequently appear as interference and limit the signal-to-interference-and-noise ratio (SINR).

The coarse frame synchronization window is established with the help of the same normalized auto-correlation signal  $M_k$  that was already used for frame detection. The example for  $M_k$  in Fig. 2.12 shows that at the end of the periodic zone the magnitude of the auto-correlation drops close to zero before rising again towards one. This drop is due to the inverted  $G_{b_{128}}$  sequence at the end of the STF and can be used to derive the coarse synchronization within the frame.

Unfortunately, the slopes of the autocorrelation depend on the delay spread and the noise



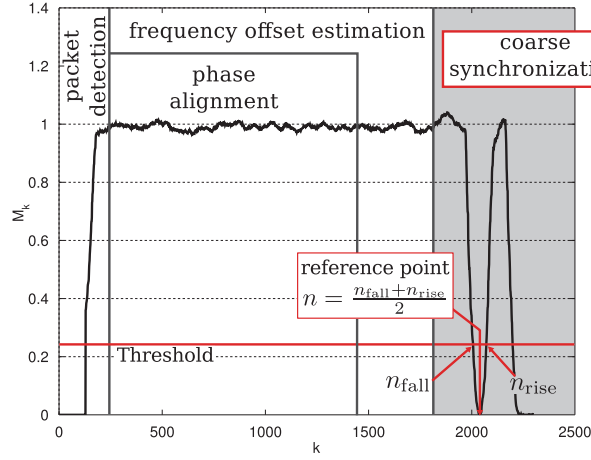


Figure 2.12 – Coarse synchronization is performed using the falling and rising slope of the auto-correlation signal at the end of the STF.

level, and are therefore neither symmetric nor at a fixed distance from the start of the CEF. By applying the threshold used during frame detection on the falling and the rising slope two reference points  $n_{\text{fall}}$  and  $n_{\text{rise}}$  can be established. The arithmetic mean

$$n = \frac{n_{\text{fall}} + n_{\text{rise}}}{2}$$

of the two reference time indices  $n_{\text{fall}}$  and  $n_{\text{rise}}$  can be easily calculated and used to determine a coarse synchronization window. This point is sufficiently robust against noise and delay spread such that a fixed offset can be used to find the start of the estimation window. The fixed offset is set such that on average the signal energy is centered in the coarse synchronization window. Consequently, the effectiveness of the coarse frame synchronization is determined based on how much of the signal energy falls within the window of the channel estimation. As mentioned before, energy which falls outside the capture window as shown in Fig. 2.11 limits the achievable SINR of the system. The limitation of the SINR is a function of the window size and the excess delay spread as the alignment of the signal energy in the capture window gets more challenging with increasing excess delay spread or reduced window size. The simulation results in Fig. 2.13 show that for a 128 symbol estimation window and excess delay spread below 64 symbol periods the average SINR limit lies above 36 dB and therefore, will not noticeably impact the quality of the transmission.

### Channel Estimation and Alignment

After coarse synchronization, a channel estimation can be performed over the established window using the CEF. The complementary Golay sequence pairs used in the CEF have the special property that the sum of their cyclic auto-correlations exhibits a perfect auto-

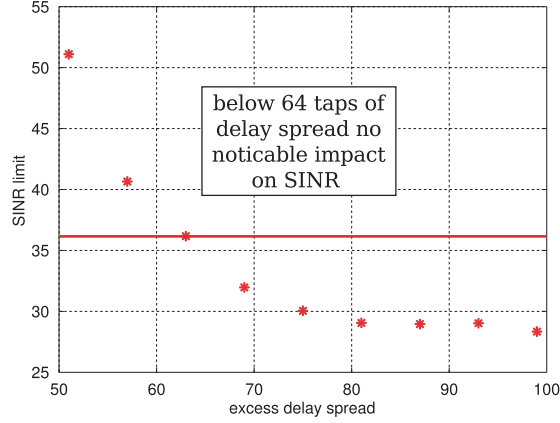


Figure 2.13 – SINR limitation due to misalignment of the 128 symbol long coarse frame synchronization window as a function of the excess delay spread.

correlation property. This property means that the combined auto-correlation exhibits a non-zero magnitude only at time zero. The use of complementary sequences for channel estimation was already proposed in [73]. While a similar property can also be achieved with Chu-Zadoff sequences, Golay sequences have the advantage that they do not require complex waveforms but are based on binary signaling, which simplifies the correlator architecture. A simple time-domain correlator architecture solely based on adders and registers, called efficient Golay correlator (EGC), has been proposed by Popovic in [74] for complementary Golay sequences. The EGC has the helpful property that it correlates the two sequences of the complementary sequence pair at the same time. Hence, EGCs allow low-complexity time-domain channel estimator implementations with a small memory footprint ideally suited for mmWave application [75].

The low-complexity of the channel estimation lends itself to the two step synchronization procedure described before. The channel estimation window can be significantly longer than the expected CIR. After performing channel estimation over the coarse synchronization window, the fine frame synchronization step can be performed. The distribution of the energy within the estimated window is analyzed and the best synchronization point is set. This best fine synchronization point depends heavily on the used receiver architecture. Assuming a SC-FDE based receiver with a IEEE 802.11ad frame format, the equalization performance is optimal when the cyclic prefix spans the maximal amount of CIR energy. Hence, the fine synchronization determines the 64 symbol window that comprises the maximum amount of channel energy. Coming back to the example CIR from Fig. 2.11, the optimal cyclic prefix window for SC-FDE and the corresponding fine synchronization point are shown in Fig. 2.14. For a SC-FDE equalizer it is irrelevant whether interference appears before or after the equalization window, for a short linear time-domain receiver which relies heavily on decision feedback as in [27], precursor interference could be way more problematic. In such a situation a more complex optimization criterion needs to be defined. After determining the fine synchronization point, the CIR and the data stream are aligned accordingly and forwarded to the equalizer.

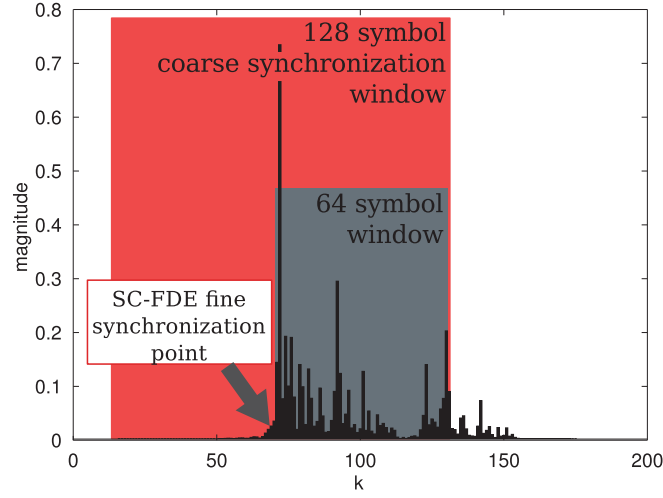


Figure 2.14 – Fine synchronization point chosen for a SC-FDE based receiver architectures with a cyclic prefix length of 64 symbols.

### Phase Noise Tracking

While absolute phase noise levels are higher in mmWave systems compared to sub-6 GHz systems, phase noise is usually not a significantly more severe concern [76] because of the higher channel bandwidth of mmWave systems. Hence, tracking of phase noise can be performed by techniques known from sub-6 GHz systems. In systems with equalizer and pilot words a good phase-noise estimate can be found by cross-correlating the equalized pilot word with the ideal pilot word.

An auto-correlation based alternative, which does not require equalized symbols, is proposed for mmWave systems that do not have equalized symbols available. The proposed phase-noise estimation algorithm is useful in systems that do not feature a channel equalizer, e.g., sequence estimation based receiver. In such systems the phase-noise estimation can be obtained by low complexity auto-correlation of the pilot words.

The influence of PN can strongly vary within a frame, hence, it is usually not helpful to evaluate the effect of phase noise averaged over a complete frame. Instead the impact of PN is averaged over a shorter window and the observed worst-case value is used as metric. The metric is based on the high level assumption that a frame that has at some point faced fatal distortion needs to be discarded as a whole anyway. The window size is set to a length of 672 symbols, which corresponds to the length of a BPSK-modulated LDPC code-word. It is assumed that a following error correction code can correct errors within such a window. The worst-case EVM metric is a monotonic function of the time.

In a system without phase-noise, this metric rises very slowly over time due to non-ideal averaging of the finite length block. In a system with phase noise the error due to phase

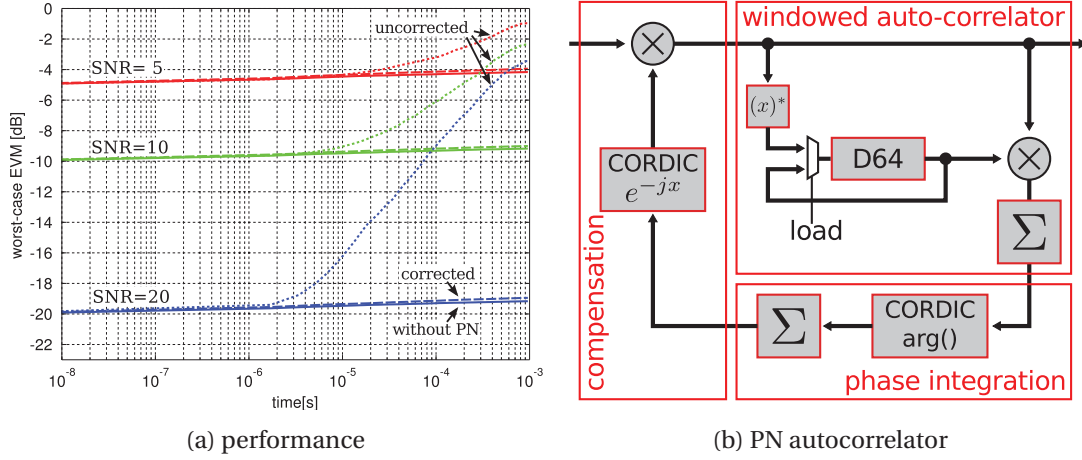


Figure 2.15 – Performance and architecture of the auto-correlation PN-tracking algorithm.

deviation is expected to become quickly the dominating source of error. A worst-case EVM comparison of a system without PN, a system with uncorrected PN and a system with corrected PN is shown in Fig. 2.15a for different SNR values. It can be seen that the phase noise becomes the dominant error source within several micro-seconds depending on the SNR. Application of the proposed estimation algorithms and compensation cancels the phase-noise nearly perfectly and reduces the worst-case EVM level close to the one of a system without phase-noise. The architecture shown in Fig. 2.15b implements the PN algorithm with the same basic elements already used for the other synchronization tasks, therefore, implementations can profit from resource sharing. For the calculation of the phase CORDIC [77] algorithms are used.

### Combined Synchronization Architecture

The proposed synchronization module for symbol-spaced sampled mmWave receivers is based around a central auto-correlation unit. The correlation unit features a reconfigurable moving window of which the length can be adjusted depending on the current phase of the synchronization. The architecture of the synchronization unit is shown in Fig. 2.16. The squared and normalized value is compared to a threshold for packet detection, the same value is also used in a later stage for the coarse frame synchronization. Intermediate values of the autocorrelation and the signal power are used to determine the sampling phase which maximizes the SNR and to estimate the frequency offset. The very regular feed-forward structure of the architecture allows high-speed VLSI implementations based on registers. The proposed synchronization algorithm is used in the baseband receiver signal processing of the Testbed described in Chapter 4.

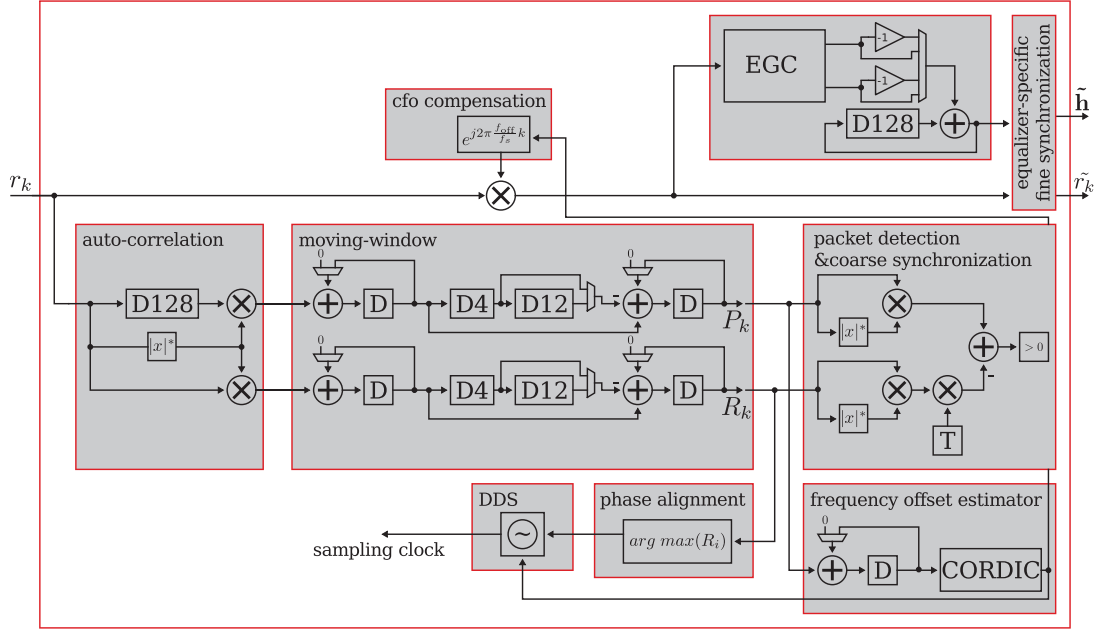


Figure 2.16 – Synchronization module for a symbol-spaced sampling IEEE 802.11ad receiver with packet detection, sampling phase alignment, frequency synchronization, coarse and fine time synchronization and channel estimation.

## 2.3 Single-Carrier Frequency-Domain Equalization

Single-carrier frequency-domain equalization (SC-FDE) is the most versatile equalization architecture for mmWave systems. SC-FDE[78] shares many similarities with OFDM regarding the required signal processing. A comparison of the signal processing architectures of SC-FDE and OFDM receivers in Fig. 2.17 shows that the two share the same basic operations with two notable differences.

First, in SC-FDE systems all FFT operations are performed on the receiver side, which effectively reduces power consumption of the transmitter. Second, in the SC-FDE architecture the transmitted symbols are directly modulated in time-domain and therefore the transmitted waveform is very well controlled, resulting in a better PAPR. Interestingly, both points lead to a power reduction in the transmitter which makes the SC-FDE especially interesting for asymmetric applications, in which the receiver has a higher power budget compared to the transmitter e.g., streaming of video data from a mobile to a stationary device.

### 2.3.1 Cyclic-Prefix SC-FDE

While different schemes have been proposed [78] for SC-FDE, the most common scheme uses a CP to make the convolution with the channel block-wise circular. The IEEE 802.11ad frame format described in Section 2.1.4 uses periodic pilot words as CP between blocks of data (cf.

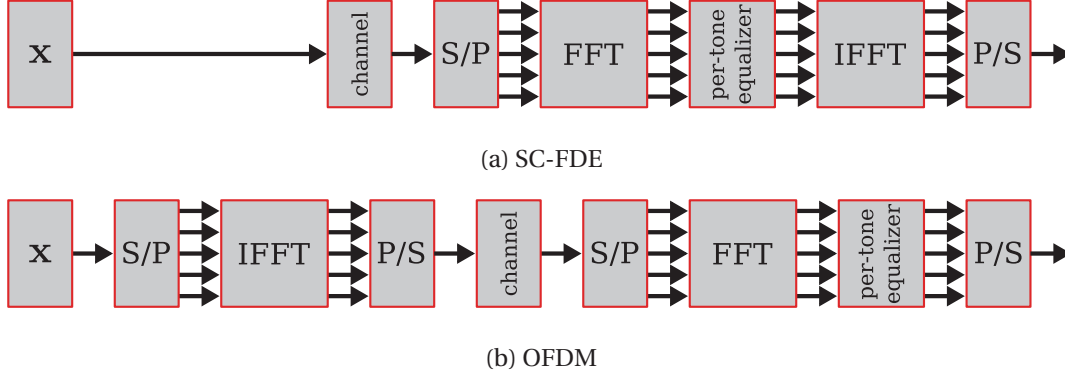


Figure 2.17 – Comparison of the signal processing architecture of SC-FDE and OFDM.

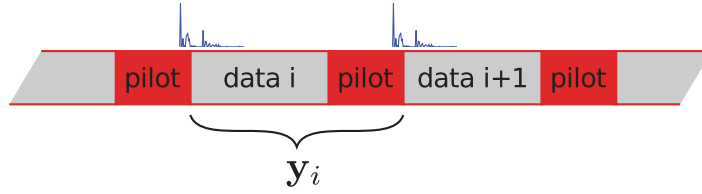


Figure 2.18 – Periodic pilot structure of frame format allows blockwise circulant processing.

Fig. 2.18). The pilot word is part of the equalized block in the order to function as CP.

If the length  $G$  of the pilot word equals or exceeds the length  $L$  of the delay spread, the convolution of each block with the CIR  $\mathbf{h}$  becomes circular. The  $i$ -th block of length  $N$  comprises the  $B = N - G$  data symbols  $\mathbf{d}_i = [d_{i,0}, \dots, d_{i,B-1}]$  and the  $G$  pilot symbols  $\mathbf{g} = [g_0, \dots, g_{G-1}]$ . The received vector  $\mathbf{r}_i = [r_0, \dots, r_{N-1}]^T$  of the  $i$ -th block can be written as

$$\mathbf{r}_i = \tilde{\mathbf{H}}\mathbf{x}_i, \quad (2.16)$$

where  $\mathbf{x}_i = [d_{i,0}, \dots, d_{i,B-1}, g_0, \dots, g_{G-1}]^T$  is the vector of transmitted symbols and  $\tilde{\mathbf{H}}$  is a  $N \times N$  circular channel matrix. The circular nature of the channel matrix  $\tilde{\mathbf{H}}$  implies that its singular value decomposition (SVD) is of the form,

$$\tilde{\mathbf{H}} = \mathcal{F}_N^{-1} \Lambda \mathcal{F}_N, \quad (2.17)$$

where  $\mathcal{F}_N$  is the  $N \times N$  DFT matrix and  $\Lambda$  a diagonal matrix of the singular values. Using (2.17) it is clear that the knowledge of  $\Lambda$  allows to reconstruct (or equalize)  $\mathbf{x}_i$  perfectly<sup>2</sup> as

$$\hat{\mathbf{x}}_i^{\text{ZF}} = \mathcal{F}_N^{-1} \Lambda^{-1} \mathcal{F}_N \mathbf{r}_i \quad (2.18)$$

$$= \mathbf{x}_i. \quad (2.19)$$

<sup>2</sup>Assuming a full rank of  $\mathbf{H}$ .

### 2.3. Single-Carrier Frequency-Domain Equalization

This channel inversion corresponds to the zero-forcing (ZF) equalizer with an equalization block length (EBL) of  $N$ . Fortunately, the singular values can be calculated from the time-domain CIR  $\mathbf{h}$  as,

$$\Lambda = \text{diag}(\mathcal{F}_N \mathbf{h}). \quad (2.20)$$

It is (for a SC system) remarkable that SC-FDE can not only perfectly revert the effect of the channel, but also allows the use of the highly efficient FFT for the convolution. Interestingly, for this type of SC-FDE the complexity of the equalization does not directly depend on the length of the channel impulse response but only on the EBL.

Adding the effect of thermal noise transforms (2.16) into

$$\mathbf{r}_i = \tilde{\mathbf{H}} \mathbf{x}_i + \mathbf{w}_i, \quad (2.21)$$

where  $\mathbf{w}$  is a vector of white Gaussian noise with variance  $\sigma_w^2$ . Inverting the channel affects also the noise vector such that (2.18) becomes

$$\hat{\mathbf{x}}_i^{\text{ZF}} = \mathcal{F}_N^{-1} \Lambda^{-1} \mathcal{F}_N \mathbf{y}_i \quad (2.22)$$

$$= \mathbf{x}_i + \mathcal{F}_N^{-1} \Lambda^{-1} \mathcal{F}_N \mathbf{w}_i \quad (2.23)$$

$$= \mathbf{x}_i + \tilde{\mathbf{H}}^{-1} \mathbf{w}_i. \quad (2.24)$$

It is clear that channel inversion also affects the noise vector and can lead to the problem of noise amplification.

Instead of the ZF criterion, the minimum mean-square error (MMSE) criterion can be used to limit the impact of noise amplification. The MMSE criterion trades noise amplification for interference suppression to minimize the total resulting error. The MMSE estimation matrix is calculated as

$$\tilde{\mathbf{H}}^{\text{MMSE}} = \frac{\tilde{\mathbf{H}}^H}{\tilde{\mathbf{H}}^H \tilde{\mathbf{H}} + \sigma_w^2 \mathbf{I}_N} \quad (2.25)$$

assuming that the transmitted symbols have unit variance. The MMSE criterion makes system integration more complicated as it requires an estimation of the noise variance. In the presence of noise, the fundamental difference between OFDM and SC-FDE becomes apparent. While OFDM allows low-complexity ML estimation of each sub-carrier, SC-FDE still performs only a sub-optimal linear-equalization.

Similar to OFDM, alternative methods are available to ensure a circular convolution. Instead of a known pilot word, the tail of the data symbols can be copied in front as CP. This data CP structure has the advantage that the FFT operations do not need to include the cyclic prefix. Instead, the FFT is performed over the data block only and therefore, shorter block sizes are required. As a result the SC-FDE receiver becomes more efficient. On the downside, the transmitter design becomes more complicated as a whole block needs to be buffered in order

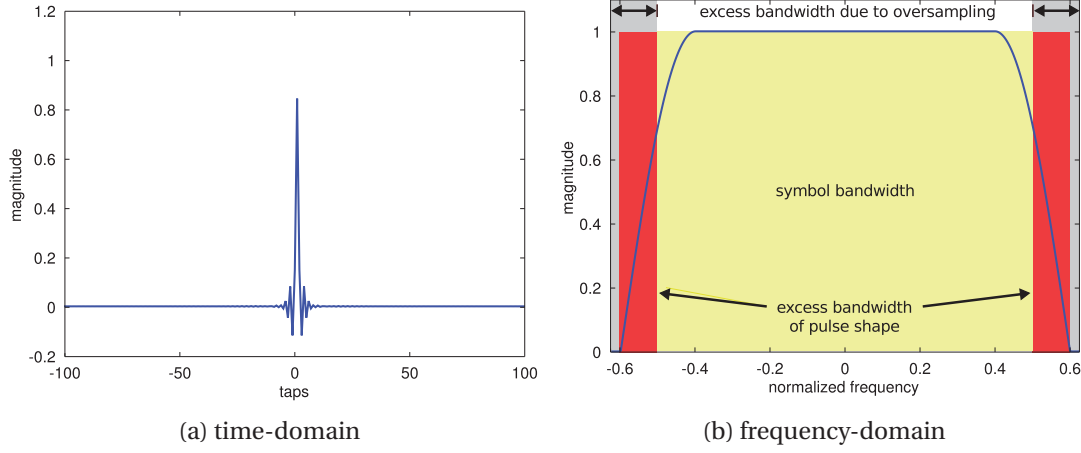


Figure 2.19 – Root raised cosine (RRC) filter with a roll-off of 0.2 and an over-sampling factor of 1.25 in time- and frequency-domain.

to extract the CP. Even more problematic is, that the CP itself cannot be used for data-aided synchronization [49].

### 2.3.2 Extension of SC-FDE

SC-FDE always requires the full transformation of a block from time-domain to frequency-domain and back. This necessity entails a complexity overhead, which makes SC-FDE appear unfavorable in complexity comparisons between different equalization architectures. However, it is often overlooked that frequency-domain processing offers efficient integration of additional baseband signal processing. Hence, a comparison of the efficiency of different receiver strategies is only useful, if all aspects of the baseband processing are considered.

FDE offers a flexible and low-complexity way to filter and resample the received signal. All-digital baseband receiver require over-sampling to perform correct frequency synchronization and maximize the SNR. With a sampling bandwidth larger than the excess bandwidth of the pulse shape filter, the matched filter can be integrated in digital-domain. Unfortunately the over-sampled signal is not suitable for low-complexity detection. Hence, decimation of the received signal before detection is required, which usually entails an additional decimation filter that contributes significantly to the overall power consumption of the receiver [65].

Frequency-domain signal processing provides a flexible way to perform filtering and decimation on signals with fractional over-sampling factors.



### Frequency-Domain Matched Filter

FD processing allows the simple integration of a matched filter in the baseband processing. Figure 2.19 shows the commonly used RRC pulse shape in time- and frequency-domain with a roll-off factor of 0.2. The pulse shape was generated with an over-sampling factor of 1.25. The frequency-domain representation in Fig. 2.19b shows the symbol bandwidth in yellow, the excess bandwidth of the pulse-shape filter in red and the excess bandwidth of the over-sampling in grey. Synchronization can be performed in digital domain as long as the sampling bandwidth is equal or larger than the excess bandwidth of the pulse. Additional sampling bandwidth can be required to compensate non-ideal filters in the analog frontend. Hence, the exact amount of over-sampling depends heavily on the characteristics of the analog frontend and the required selectivity. From a power-efficiency perspective it is desirable to use the minimal over-sampling rate which fulfills the performance requirements, in order to have the least amount of samples to process. TD receivers [79][72][80] often implement an integer (or half-integer) over-sampling factors to simplify the filter design. SC-FDE architectures allow a very fine-grained selection of the fractional over-sampling as the only requirement for efficient sampling is that the block size

$$N^{\text{OS}} = R^{\text{OS}} \cdot N \quad (2.26)$$

of the over-sampled signal is again integer. This condition implies that the sampling bandwidth can be adjusted in steps of  $f_{\text{spacing}} = \frac{f_{\text{sym}}}{N}$  where  $f_{\text{symbol}}$  is the symbol rate. For an IEEE 802.11ad system,  $f_{\text{spacing}}$  evaluates to 3.4375 MHz. A comparison to the commonly used step size of  $0.5f_{\text{sym}} = 880\text{MHz}$  underlines the high flexibility of frequency-domain based filtering.

Another advantage of frequency-domain filtering is the possibility to integrate sampling delays. The sampling point alignment proposed in Section 2.2.2 for optimization of SNR and delay spread can be easily integrated into the matched filter. Fractional shifts of the sampling point can be performed in FD by a frequency dependent phase rotation of the pulse shape coefficients. This can not only be used to establish the optimal initial sampling phase, but also for SFO compensation.

### Frequency-Domain Decimation

A fractionally-sampled received signal allows flexible filtering but is not suitable for symbol detection. Decimation is required to transform the over-sampled received signal into a symbol spaced sequence. In FD the signal can be decimated by circular folding of the excess bandwidth onto the signal, a technique which is also sometimes called spectral over-lapping [63]. Circular folding is demonstrated for a discrete raised cosine pulse shape in Fig. 2.20. Decimation can be implemented as simple addition of the frequency components. The implementation of the folding operation can take advantage of knowledge about the shape of any preceding pulse filter. Sub-carriers for which the corresponding filter coefficients

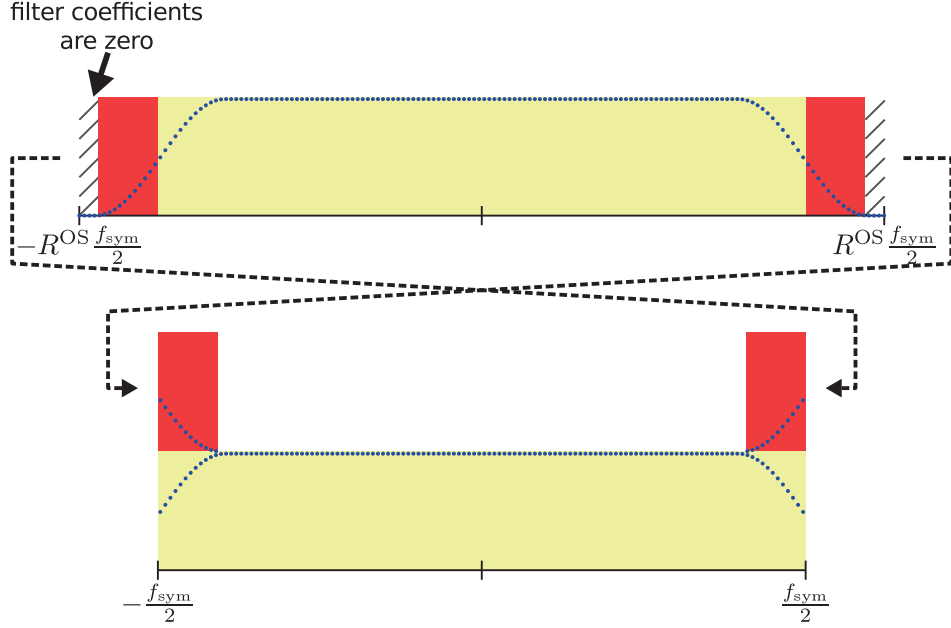


Figure 2.20 – Folding of the excess bandwidth of a raised cosine (RC) pulse to symbol-spaced sampling.

are zero can be directly omitted from the folding.

Sampling rate decimation in FD implies that FFT and IFFT operate on different block sizes<sup>3</sup>. This property can be undesirable in narrowband systems where FFT and IFFT operations share the same physical hardware. In the wideband mmWave systems it is usually not a problem as dedicated hardware is required for FFT and IFFT in order to achieve the necessary throughput.

### $\pi/2$ -rotation Modulation

In FDE-based equalization architectures, the  $\pi/2$ -rotation Modulation described in Section 2.1.4 can be seen as a cyclic shift in frequency-domain. Hence, the  $\pi/2$ -rotation can be reverted after decimation by reordering the frequency bins before back transformation to time-domain. The DFT transform pair,

$$x_n e^{j2\pi nl/N} \longleftrightarrow X_{k-l}, \quad (2.27)$$

for a complex rotation of the sequence  $x_n, n = 1, \dots, N-1$  and the effect on its DFT  $X_k, k = 1, \dots, N-1$  can be used for the  $\pi/2$  rotation of the modulation in time-domain. The  $\pi/2$  rotation

<sup>3</sup>Several algorithms are known which allow the hardware implementation of non-power-of-two FFTs [81], an implementation of a non-power-of-two FFT was shown in [63].

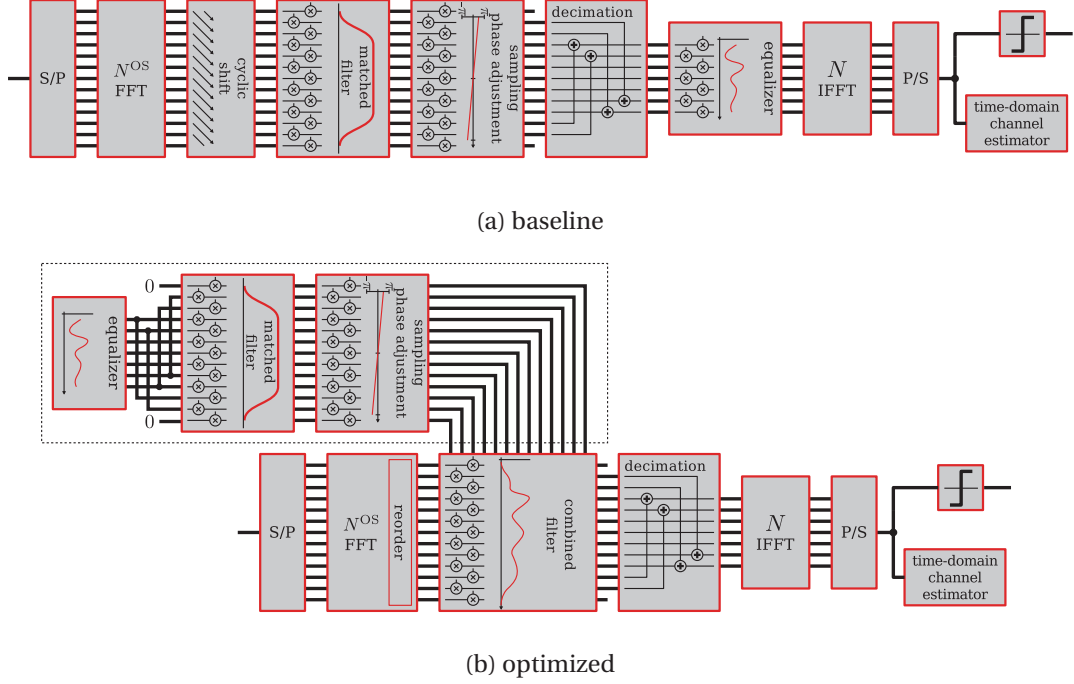


Figure 2.21 – SC-FDE based baseband signal processing architectures.

corresponds to a circular shift of the frequency-domain vector by

$$l = \frac{N}{4}, \quad (2.28)$$

where  $N$  is the length of the DFT vector. The multiplication in TD transforms into a simple memory operation in FD, which can be absorbed in the reordering operations necessary for the decimation and therefore comes with no additional overhead.

#### 2.3.3 SC-FDE Baseband Architecture

Implementation of the frequency-domain signal processing is straight forward. A baseline architecture for the implementation of the different steps is shown in Fig. 2.21a. The order of equalization and decimation is a system design decision. In frequency selective environments performing equalization before decimation can result in a higher SNR, but complicates the overall system design. Hence, for mmWave systems an equalization-after-decimation strategy is proposed which allows the use of low-complexity symbol-spaced time-domain channel estimation. The performance penalty can be mitigated by a sampling point adjustment as proposed in Section 2.2.2.

Complexity of the SC-FDE architecture can be quantified based on the number of complex multiplications, using the assumption that a single FFT with a block size  $N$  requires  $N \cdot \log(N)$

complex operations. The proposed baseline architecture requires

$$C^{\text{base}} = N^{\text{OS}} \log(N^{\text{OS}}) + N \log(N) + 1.5N^{\text{OS}} + N \quad (2.29)$$

$$= N^{\text{OS}}(\log(N^{\text{OS}}) + 1.5) + N(\log(N) + 1) \quad (2.30)$$

complex multiplications in order to process  $N$  symbols.

The number of required complex multiplications can be significantly reduced, when operations are merged. It is obvious that the coefficients of the pulse shape filter and the phase adjustment can be multiplied once at the beginning in order to obtain a single filter coefficient. Using the distributive law, also the coefficients of the equalization can be merged into the joint filter. The joint filter coefficients need to be calculated only once at the beginning of the frame which makes the complexity of this operation from a system power perspective negligible for long frames. The optimized architecture based on a single joint filter is shown in Fig. 2.21b. Because of the optimization the architecture requires only

$$C^{\text{opt}} = N^{\text{OS}}(\log(N^{\text{OS}}) + 1) + N \cdot \log(N) \quad (2.31)$$

complex multiplications for a block of  $N$  symbols. The complexity of the SC-FDE baseband architecture depends heavily on the chosen block size  $N$ .

It is important to note that  $C^{\text{opt}}$  is the complexity of one block and the  $N$  block symbols include  $P$  pilot symbols. Hence, the complexity per data symbol  $\hat{C}^{\text{opt}}$  is a function of the block size and the pilot word length as

$$\hat{C}^{\text{opt}} = \frac{C^{\text{opt}}}{N - P}. \quad (2.32)$$

The length of the pilot word needs to exceed the delay spread, which makes the optimal block size effectively a function of the delay spread. If the transmitter has channel state information (CSI) he can adjust pilot word and block length in order to minimize the receiver complexity. The IEEE 802.15.3c standard [20] for WPAN supports different pilot-/block-length configurations, which allows a system to adapt to the system conditions. In the IEEE 802.11ad standard, only a single pilot word and block length combination is specified. For such a standard the SC-FDE baseband receivers entail a constant complexity independent of the actual delay spread.

### 2.3.4 Energy Proportional Frequency-Domain Equalization

While the single-carrier equalization capabilities of SC-FDE receivers are unmatched for long delay spreads, time-domain linear equalizers (TD-LEs) can deliver a similar performance for no or very short delay spreads with a significantly lower complexity. It was shown in Section 2.1.2 that the excess delay spread of wideband mmWave systems varies heavily with the degree of beam-forming used, even in the same usage scenario. Hence, mmWave system

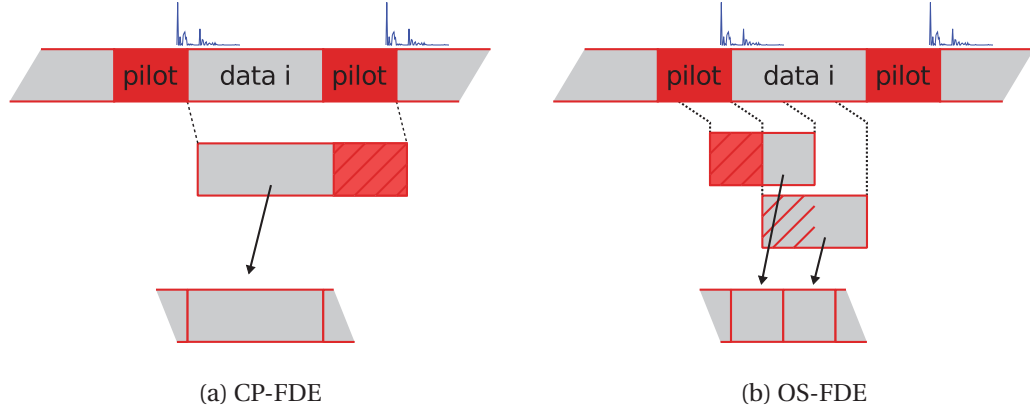


Figure 2.22 – Comparison of data processing in cyclic-prefix (CP) and overlap-save (OS) frequency-domain equalization (FDE) modes.

designs need to choose between high link reliability and energy-efficient operation. In this section an energy-proportional frequency-domain equalization (EP-FDE) scheme is proposed that offers not only the channel equalization properties of cyclic-prefix based SC-FDE in very frequency-selective environments but also the reduction of the equalizer complexity in frequency-flat or weak frequency-selective channel conditions.

#### Overlap-save frequency-domain equalization (OS-FDE)

Overlap-save frequency-domain equalization (OS-FDE) is an alternative algorithm that uses the efficiency of the FFT to perform equalization dating back to the 70s [82][83]. The advantage of OS-FDE is that it does not require a circular channel matrix. OS-FDE uses the effect that corruption due to non-circular channel convolution is concentrated on the beginning of the equalized block. The use of the FFT to approximate the convolution is a commonly proposed [84][85][86] method for filtering in various contexts.

Similar to the CP-FDE algorithm, the FFT is used for efficient conversion between frequency and time-domain, but corruption due to the lack of a cyclic prefix is mitigated by discarding the initial segment of the equalized block. Because of the discarded initial segment, the OS-FDE equalizer needs to operate on overlapping segments of the received symbol stream as shown in Fig. 2.22b. It is reported [78] that an overlap of 50% results in a good balance between block length and equalization performance. Because of the overlap, each received symbol is processed more than once by the equalizer, which makes OS-FDE less efficient compared to CP-FDE for the same EBL. However, OS-FDE can be more efficient than CP-FDE, if a smaller EBL is used.

Unlike for CP-FDE, during OS-FDE, perfect channel inversion cannot be guaranteed and there is residual interference. Nevertheless, the use of overlap-save FDE for mmWave receivers was proposed in [65] with a fixed block length.

Table 2.3 – Equalization complexity for a frame block of 512 symbols.

| EBL    | 8    | 16   | 32   | 64   | 512  |
|--------|------|------|------|------|------|
| OS-FDE | 1344 | 2016 | 2800 | 3640 | 7184 |
| CP-FDE | -    | -    | -    | -    | 3592 |

### Dual-Mode FDE

EP-FDE is based on a reconfigurable FDE module which can switch between a conventional CP-FDE and an OS-FDE mode. The different data processing schemes of the two modes are compared in Fig. 2.22.

The hybrid receiver chooses between OS-FDE with various block lengths and CP-FDE based on the channel conditions. While for the same equalization block length OS-FDE is more complex compared to CP-FDE, OS-FDE can adapt its equalization block length independently of the structure of the frame. For a short excess delay spread, performing OS-FDE with a small EBL can provide sufficient equalization with less computational complexity than CP-FDE. The ability to switch between CP-FDE and OS-FDE operation allows to operate the receiver with the configuration that exhibits the lowest complexity, while still providing sufficient equalization performance. In particular, the receiver does not sacrifice its worst-case equalization capabilities.

The hardware area overhead of a dual-mode frequency-domain receiver compared to a conventional CP-FDE receiver is negligible as the OS-FDE and CP-FDE algorithms require essentially the same basic receiver architecture. Nevertheless, there are differences in the resource usage, hence, the computational complexity of each operation mode is used as an indicator of the expected power consumption. Complexity for the different operation modes is quantified by the number of required non-trivial complex multiplications, which is a common measure for the complexity of FFTs. The number of complex multiplications required to equalize the data symbols of a block of 512 symbols using the CP-FDE and OS-FDE algorithm with different EBLs is given in Tbl. 2.3. It can be seen that the OS-FDE with an EBL below 64 reduces the complexity compared to CP-FDE. Per channel selection of the optimal configuration promises a reduction of the overall complexity, but it is not obvious how the optimal block size shall be determined.

### FDE Block Size Selection

The optimal selection of the equalization block length is the central challenge for the effectiveness of EP-FDE. Two strategies for the choice of the EBL are presented. The first genie-aided approach assumes perfect knowledge of all possible outcomes and hence, establishes a lower bound for the complexity. The second strategy suggests a sub-optimal method which determines the EBL on the fly in the receiver.

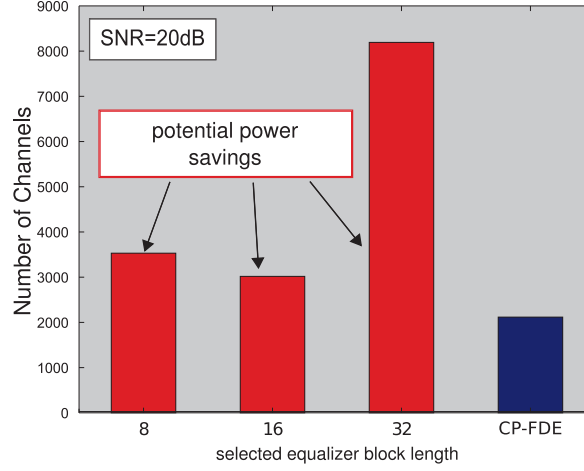


Figure 2.23 – Example distribution of selected equalizer block length for statistically generated channel realizations at 20 dB using the genie-aided algorithm.

For the genie-aided receiver, perfect knowledge of the resulting BER is assumed for all eligible configurations in advance. Based on this knowledge, the configuration with the lowest complexity which still achieves the minimum number of bit errors is chosen for equalization. It is clear that such a genie-aided hybrid scheme will always achieve at least the performance of the CP-FDE only receiver. In the case that for some of the channel realizations an OS-FDE can be chosen, the hybrid scheme achieves a reduction of the average equalization complexity compared to a pure CP-FDE receiver. For statistically generated NLOS channel realizations, the distribution of selected EBL in Fig. 2.23 shows that for the majority of channel realizations a smaller EBL can be chosen.

The genie-aided approach is obviously not suitable for receiver implementations. Therefore, a practical algorithm which approximates the optimal configuration choice is proposed. Our practical algorithm is sufficiently low in complexity so that it can be performed during the reception of a frame.

As criterion for the choice of the appropriate EBL, the minimal post-equalization signal-to-interference ratio ( $\text{SIR}^{\text{POST}}$ ) is proposed. An estimate of the resulting SIR is calculated for each equalization block length from the residual post-equalization channel impulse response (CIR). The residual post-equalization CIR  $\tilde{\mathbf{h}}$  is obtained from the convolution of the estimated CIR  $\hat{\mathbf{h}}$  with the time-domain response of the equalizer<sup>4</sup> as

$$\tilde{\mathbf{h}} = \hat{\mathbf{h}} * \left( (\mathcal{F}^N)^{-1} [\mathcal{F}^N [\hat{\mathbf{h}}]^N]^{-1} \right), \quad (2.33)$$

where  $\mathcal{F}^N$  is the  $N \times N$  DFT matrix and  $[\cdot]^N$  is truncation or zero-padding of a vector to length  $N$  and  $[\cdot]^{-1}$  the element-wise inversion. The post-equalization  $\text{SIR}^{\text{POST}}$  is consequently

<sup>4</sup>In this example the ZF criterion is used, the receiver can also be implemented using the MMSE criterion.

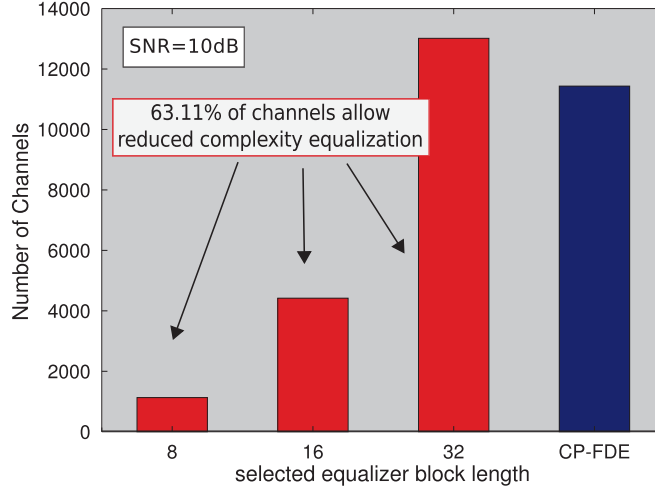


Figure 2.24 – Distribution of selected equalizer block lengths for statistically generated channel realizations at 10 dB using the practical SIR based algorithm.

calculated as

$$\text{SIR}^{\text{POST}} = \frac{|\tilde{h}_0|^2}{\sum_{i=1}^{N-1} |\tilde{h}_i|^2}. \quad (2.34)$$

Although the SIR calculation is only an approximation of the final SIR, it provides a sufficiently good criterion to judge the quality of equalization. An example of the EBL distribution using the SIR criterion allows a complexity reduction for 63% of the channel realizations as shown in Fig. 2.24. The exact value depends on the used channel scenario, the operating SNR and the target  $\text{SIR}^{\text{POST}}$ .

The SIR requirement can be defined as a function of the current SNR with a back-off parameter  $b$  (in dB) as margin in the following way,

$$\text{SIR}^{\text{POST}}|_{\text{dB}} = \text{SNR}|_{\text{dB}} + b. \quad (2.35)$$

The parameter  $b$  offers a performance-complexity trade-off that can be adjusted based on high level considerations as the currently available power budget for the receiver. A small value for  $b$  allows a larger amount of interference and, hence, is more easily satisfied by a shorter equalization block length.

The proposed procedure to determine the SIR is simple enough such that a receiver can try all candidate EBL at the beginning of each frame. In order to avoid costly buffering of received symbols, a mmWave receiver implementing EP-FDE already begins equalization using the CP-FDE algorithm while in parallel determining the appropriate reduced complexity block size. Because of the very long frame size of mmWave systems, this initial increase in complexity will not affect the overall complexity reduction.



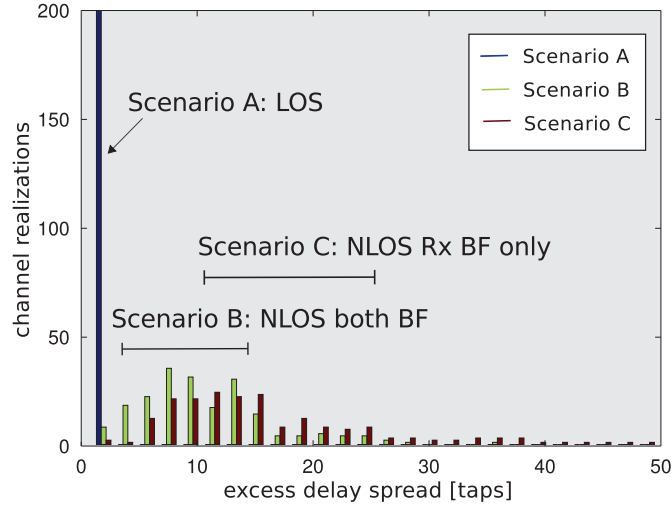


Figure 2.25 – Distribution of excess delay spread for the three defined scenarios.

#### Results

For the evaluation of the energy scaling capabilities, three representative mmWave scenarios have been defined:

- **Scenario A** is under LOS conditions. The path between the two antennas is not obstructed.
- **Scenario B** is under NLOS conditions, with the path between the two antennas obstructed, while beam-forming is employed on both the TX and RX side.
- **Scenario C** is under NLOS conditions, with the path between the two antennas obstructed, while beam-forming is only employed on the RX side.

The scenarios are chosen in such a way that a receiver could face all three of them in the same environment. The distribution of the excess delay spread of 200 channel realizations generated for the three different proposed scenarios is shown in Fig. 2.25. The excess delay spread is measured as the smallest window which comprises more than 90% of the channel energy. It can be seen that for the different scenarios there are huge variations in the distribution of the delay spread, which varies between a single tap and dozens of symbol periods. Especially, if there is no beam-forming on the transmitter side the excess delay spread can grow significantly beyond 25 taps.

The results shown in Fig. 2.23 and Fig. 2.24 are evaluated for a single SNR point only. In order to quantify the achievable complexity savings an average complexity is calculated for each scenario based on the EBL distribution and the equalization complexity for each EBL. The complexity is measured using the number of complex multiplications required on average to equalize a channel realization. Figure 2.26 shows the average complexity of the EP-FDE

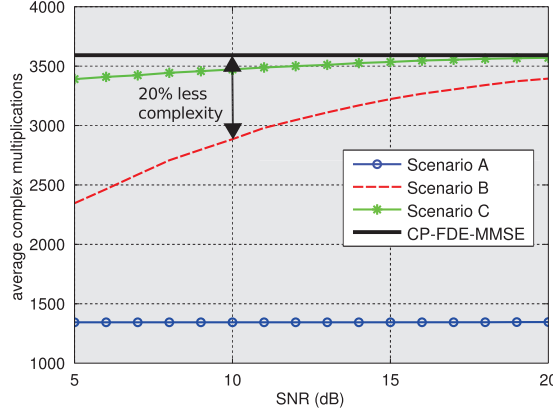


Figure 2.26 – Average complexity for the three defined scenarios for the practical block length selection scheme with a backoff parameter  $b = 6$ .

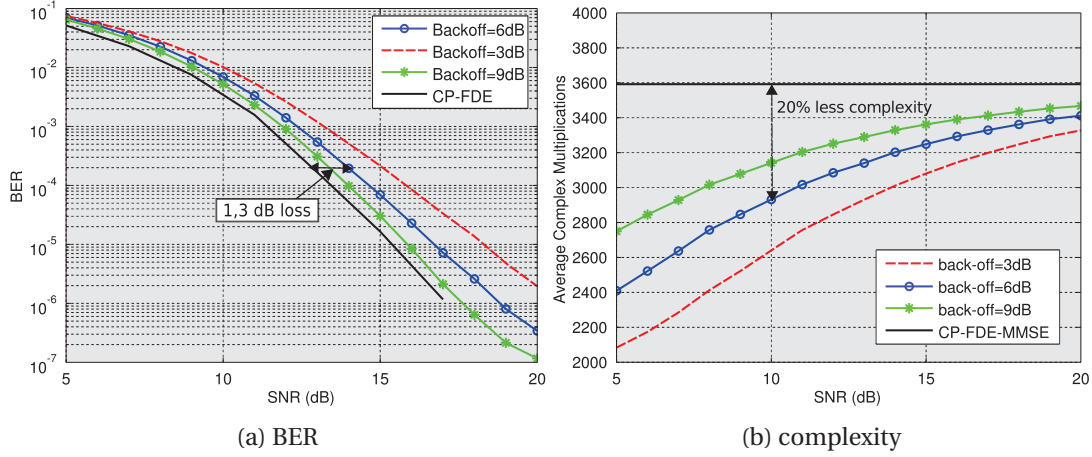


Figure 2.27 – Complexity and BER performance for different values of the back-off parameter.

receiver using the practical block selection algorithm with a backoff parameter  $b = 6$  for the three defined scenarios and the standard CP-FDE receiver. The CP-FDE receiver exhibits the same complexity independent of the SNR and the usage scenario. It can be seen that for scenario A, due to the strong LOS path always the minimal EBL can be used and a significant reduction is achieved compared to the CP-FDE receiver. In scenario B, the practical algorithm chooses in the low SNR regime frequently the overlap save mode with small EBL, which tolerates a bigger amount of interference. Towards the higher SNR regime, the CP-FDE needs to be used more often and the complexity converges towards the one of the CP-FDE receiver. This is an expected behaviour, because the SIR criterion of the practical receiver is defined in such a way, that it strives for better equalization at higher SNR levels.

The target  $\text{SIR}^{\text{POST}}$  is determined in (2.35) from the current SNR level and the back-off parameter  $b$ . Changing the back-off parameter provides a possibility to trade equalization quality for complexity. In Fig. 2.27, the complexity and BER performance are shown for different values of

*b.* With increasing back-off the BER performance of the practical receiver converges towards the performance of the CP-FDE receiver, but in return also the possible complexity savings reduce. Hence, the back-off parameter can be used to trade power reduction for performance.

As mentioned before, a mmWave receiver could face all three defined scenarios at different SNR levels in the same environment. For the traditional mmWave receiver paradigm, the designer of the receiver architecture has either the choice between a CP-FDE receiver that operates reliable in all three scenarios, but always uses maximum complexity or a short time-domain receiver that operates very efficient in scenario A, but shows a high outage probability in scenario B and C. EP-FDE allows to unite the two concepts with an emphasis on the link reliability, as it is usually the more crucial virtue. On the downside, the absolute complexity of EP-FDE even for beneficial channels might be higher compared to power optimized analog time-domain receivers.

It was demonstrated in [65] that also reduced-length FDE architectures and therefore also EP-FDE can incorporate some of the equalization extensions described in Section 2.3.2. Further study is needed to show how reducing the block rate impacts the ability to integrate additional baseband signal processing in the FDE.

## 2.4 Soft-Output Delayed Decision Feedback Sequence Estimation

Maximum-likelihood sequence estimation (MLSE) is the holy grail of SC receiver design. Unlike equalization and demodulation based receivers, which are inherently sub-optimal in frequency-selective conditions [87], MLSE determines the most-likely transmitted sequence (also called ML solution) from the received samples. Unfortunately, performing MLSE for channels with long delay spreads becomes quickly prohibitive in terms of required area and power, since the number of (channel) states grows exponentially with the ISI length. Several methods have been proposed [88][89][90] to approximate the ML solution and reduce the complexity of the sequence estimation. These approximations reduce the complexity by skipping or merging parts of the state space and are therefore usually summarized as reduced state sequence estimation (RSSE) methods. A possible way to reduce the number of states by using decision feedback has been described by Duel-Hallen and Heegard [90] as delayed decision feedback sequence estimation (DDFSE). The DDFSE algorithm has been implemented for narrowband cellular application in [91].

In this section, the architecture of a soft-output DDFSE detector for mmWave with support for BPSK and QPSK modulation is presented. First, an algorithmic description of full MLSE using the Viterbi algorithm (VA) is provided. Afterwards, it is outlined how the DDFSE algorithm reduces the required state-space to reduce the receiver complexity. A high-speed VLSI architecture will be presented which allows the use of the DDFSE algorithm in mmWave systems with GHz symbol rates.

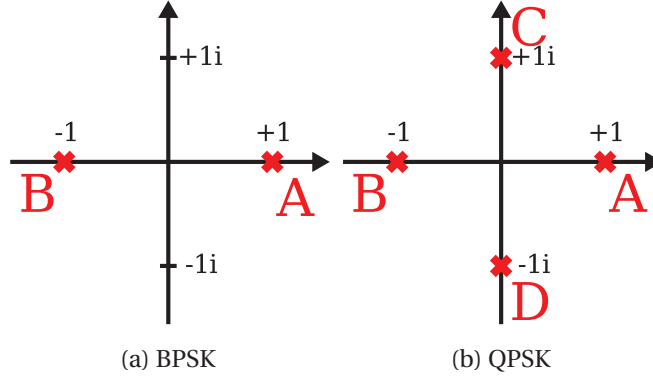


Figure 2.28 – BPSK-/QPSK-constellation labeling for the DDFSE algorithm.

### 2.4.1 System Model

For the algorithmic description of the DDFSE algorithm, it is assumed that a digital bit stream  $\mathbf{b} = [b_0, \dots, b_{J-1}]$  of length  $J$  is mapped to a vector  $\mathbf{x} = [x_0, \dots, x_{K-1}]$  of  $K$  symbols according to a constellation alphabet  $\mathcal{M}$  with cardinality  $M$ . The  $L$  symbol-spaced taps of the CIR are denoted  $\mathbf{h} = [h_0, \dots, h_{L-1}]$ . The corresponding input-output relationship is given by

$$r_k = \sum_{i=0}^{L-1} x_{k-i} \cdot h_i + w_k,$$

where  $r_k$  denotes the  $k$ -th received baseband sample and  $w_k$  is its additive white Gaussian noise component.

For the examples in this section, we assume either BPSK modulation with  $M = 2$  or QPSK modulation with  $M = 4$ . For the sake of convenience, the elements of the BPSK and QPSK constellations are labeled alphabetically  $A, B, C, D$  (cf. Fig. 2.28) and the BPSK constellation is treated as a subset of QPSK.

### 2.4.2 Algorithm

#### Maximum Likelihood Sequence Estimation

Detection based on the ML criterion is optimal in the sense that it determines the most likely transmitted signal  $\mathbf{x}$  out of all possible sequences of length  $K$  based on the received vector  $\mathbf{r}$ , as

$$\hat{\mathbf{x}} = \arg \max_{\mathbf{x} \in \mathcal{M}^K} (p(\mathbf{r}|\mathbf{x})). \quad (2.36)$$

Under the assumption of additive white Gaussian noise, the ML solution (2.36) for a transmitted sequence of length  $K$  and a CIR of length  $L$  can be found by minimizing the squared

euclidean distance from a candidate sequence  $\tilde{\mathbf{x}}$  as

$$\hat{\mathbf{x}} = \arg \min_{\tilde{\mathbf{x}} \in \mathcal{M}^K} \left( \sum_{k=0}^{K+L-2} \left| r_k - \sum_{i=0}^{L-1} \tilde{x}_{k-i} \cdot h_i \right|^2 \right). \quad (2.37)$$

The optimal sequence can be found by comparing the received vector with all possible transmit combinations, but the required effort grows exponentially with  $K$ . Hence, for a reasonable number of transmitted symbols the complexity very quickly exceeds all practical limits. A more efficient method to find the ML solution is the Viterbi algorithm (VA)[92], which is based on a concept also known as dynamic programming.

The VA uses the insight that each received symbol is only influenced by  $L$  preceeding transmitted symbols. Hence, the detector needs to deal only with the probabilities of  $M^L$  possible candidate sequences of length  $L$  simultaneously.

The VA keeps the complexity constant by continuously discarding intermediate probabilities of combinations which cannot lead to the optimal solution anymore. Thus the complexity of the VA algorithm grows “only” exponentially with the channel length  $L$  and not the sequence length. During each step, the algorithm adds a new symbol to the candidate sequence and makes a decision in each state about the earliest symbol of the candidate sequence. Therefore, only the probabilities for a set  $\mathcal{S}_k$  of  $Z = M^{L-1}$  intermediate states need to be stored. Each element of  $\mathcal{S}_k$  corresponds to a vector  $\bar{\mathbf{s}}_k^i = [\bar{s}_k, \bar{s}_{k-1}, \dots, \bar{s}_{k-L+2}]$  of  $L-1$  symbols  $\bar{s} \in \mathcal{M}$ . This vector is given by the  $L-1$  newest symbols of the evaluated candidate sequence.

States from  $\mathcal{S}_{k-1}$  which have a transition to a state  $\bar{\mathbf{s}}_k^i$  form a set of source states  $\mathcal{X}(\bar{\mathbf{s}}_k^i)$ . Possible transitions between states can be visualized by a trellis as shown in Fig. 2.29. The probability of a state  $\bar{\mathbf{s}}_k^i$  is fully determined by the received symbol  $r_k$  and the probabilities of  $\mathcal{X}(\bar{\mathbf{s}}_k^i)$ . The probability of state  $\bar{\mathbf{s}}_k^i$  is stored as the state metric  $A(\bar{\mathbf{s}}_k)$  along with a vector of all previously taken decisions  $G_i(\bar{\mathbf{s}}_k)$ ,  $i = k-L+1, \dots, 0$  which constitute the most likely path leading to this state.

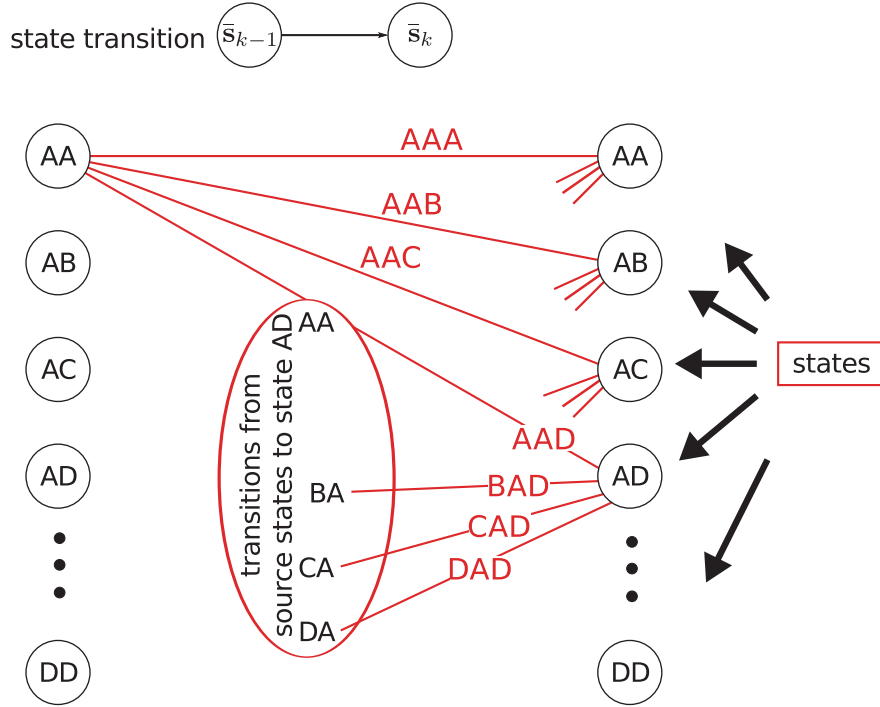
The weight of the transition between a state  $\bar{\mathbf{s}}_k$  and a valid source state  $\bar{\mathbf{s}}_{k-1} \in \mathcal{X}(\bar{\mathbf{s}}_k)$  is referred to as branch metric  $\Gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k)$  and is given by the distance between the received symbol  $r_k$  and an ideal noise-free signal given by the candidate sequence as

$$\Gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k) = \left( \left( \sum_{i=0}^{L-1} \bar{s}_{k-i} \hat{h}_i \right) - r_k \right)^2. \quad (2.38)$$

The path metric  $\gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k)$  can be calculated in a recursive manner from the joint probability of the transition  $\Gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k)$  and the state metric  $A(\bar{\mathbf{s}}_{k-1})$  of the source state. If the calculation is performed in the logarithmic domain, the path metric calculation simplifies to

$$\gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k) = \Gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k) + A_{k-1}(\bar{\mathbf{s}}_{k-1}). \quad (2.39)$$

For each state, the path can originate only from  $M$  different source states, which reduces the


 Figure 2.29 – Trellis diagram of possible state transitions for QPSK and a channel length  $D = 3$ .

number of candidates for each local ML function significantly.

The source state

$$\bar{\bar{s}}_{k-1} = \arg \min_{\bar{s}_{k-1} \in \mathcal{X}(\bar{s}_k)} (\gamma(\bar{s}_{k-1}, \bar{s}_k)), \quad (2.40)$$

which corresponds to the surviving path fully defines the new path history  $\mathbf{G}(\bar{s}_k)$ . The decision leading to the surviving path together with the decision history of its source state form the decision history of the winning state as

$$G_i(\bar{s}_k) = \begin{cases} \bar{\bar{s}}_{k-L-2} & , i = k - D + 1, \\ G_i(\bar{\bar{s}}_{k-1}) & , i = 0, \dots, K - D. \end{cases} \quad (2.41)$$

The weight of the winning path is stored as the new state metric

$$A(\bar{s}_k) = \gamma(\bar{\bar{s}}_{k-1}, \bar{s}_k). \quad (2.42)$$

Instead of finding the minimum of  $\mathcal{M}^K$  possible solutions the VA needs to find  $(K + L) \cdot M^{L-1}$  times the minimum between  $M$  possible solutions. Yet, the number of states  $Z$  of the trellis grows exponentially with the channel length  $L$  as  $Z = M^{L-1}$ .

### State Reduction

The DDFSE algorithm applies the VA with a truncated constraint length. Only  $D$  taps of the CIR are considered for expansion in the trellis. The inter-symbol-interference terms from the remaining  $V = L - D$  symbols are canceled by means of a decision feedback equalizer. This state reduction is motivated by the insight that in the CIR the signal power is not evenly distributed over all taps. Hence, while not all channel taps contribute the same to the signal energy, they all lead to the same complexity increase of the Viterbi decoder. By reducing the constraint length, less relevant dimensions of the state space are removed for the sequence estimation.

With the number of taps in the trellis fixed to  $D$ , the number of states is limited to  $Z = M^{D-1}$ . Hence, the complexity of the DDFSE is decoupled from the length of the channel impulse response  $L$ .

For the VA branch metric (2.38), only the received sample  $r_k$  has a time dependency. DDFSE introduces a per state, time variant feedback in addition to the time invariant reference signal part. This feedback term

$$f(\bar{\mathbf{s}}_k) = \sum_{i=D}^{L-1} G_{k-i}(\bar{\mathbf{s}}_k) \cdot \hat{h}_i \quad (2.43)$$

is based on the decision history of each state. To ease notation, the time-invariant reference signal part is labeled  $e_{\bar{\mathbf{b}}}$ , where  $\bar{\mathbf{b}}$  is a unique identifier of a transition between  $\bar{\mathbf{s}}_k$  and  $\bar{\mathbf{s}}_{k-1} \in \mathcal{X}(\bar{\mathbf{s}}_k)$  (also called branch).

$$e_{\bar{\mathbf{b}}} = \sum_{i=0}^{D-1} \bar{s}_{k-i} \hat{h}_i \quad (2.44)$$

The calculation of the branch metric in (2.38) can now be written as

$$\Gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k) = r_k - f_{k-1}(\bar{\mathbf{s}}_{k-1}) - e_{\bar{\mathbf{b}}}. \quad (2.45)$$

It can be seen that the feedback term is only dependent on the source state of the branch. Unfortunately, the feedback term  $f_{k-1}$  needs to be recalculated in every cycle for each state. However, the complexity to calculate this term grows linearly with the number of trellis states and the number of feedback taps. Hence, the DDFSE algorithm leads to a significant reduction of the overall complexity if  $D$  is chosen such that  $D \ll L$ .

The complexity of the feedback calculation can further be reduced if we take advantage of the fact that multiple states can inherit the same decision history  $\mathbf{G}$  from a source state. The paths to different states merge after some steps and share a common initial path segment. While it is not guaranteed that all the different surviving paths merge, it can be shown that in practical situations a merge happens after only a few steps with very high probability. Under the assumption that after  $I$  steps the decision history of all states has merged with high

probability, the decision history can be split into two parts. The first  $I - 1$  decisions, which need to be stored per state, are combined in the individual state history (ISH). The remaining  $Q = V - I$  converged decisions from the common history (CH) need to be stored only once for all states.

To this end the feedback term is segmented into two components, a state-specific feedback term  $f^{\text{ISH}}(\bar{\mathbf{s}}_k)$  based on the ISH of the source state and a feedback signal  $f_k^{\text{CH}}$  based on the CH of all states.

$$f(\bar{\mathbf{s}}_k) = f_k^{\text{CH}} + f^{\text{ISH}}(\bar{\mathbf{s}}_k) \quad (2.46)$$

Substituting (2.46) in (2.45) we can write the calculation of the branch metric as

$$\Gamma(\bar{\mathbf{s}}_{k-1}, \bar{\mathbf{s}}_k) = r_k - f_{k-1}^{\text{CH}} - f^{\text{ISH}}(\bar{\mathbf{s}}_{k-1}) - e_{\bar{\mathbf{b}}}. \quad (2.47)$$

A common problem of all receivers using decision feedback is the presence of error propagation. A wrongly detected symbol lowers the detection probability of successive symbols significantly. While it is difficult to analytically derive the impact of error propagation, it is obvious that it leads to monotonous increase of the symbol error probability during the detection of successive symbols. The problem is mitigated in our setup by the pilot words described in Section 2.1.3, which periodically reset the decision history of the DDFSE receiver to correct values.

The choice of  $D$  is crucial for the performance of the DDFSE algorithm. If  $D$  equals  $L$ , DDFSE transforms into MLSE. On the other extreme, if  $D$  is restricted to a single tap the DDFSE receiver becomes a conventional DFE with demodulator. Hence, the DDFSE algorithm provides a gradual performance-complexity tradeoff between the optimal ML solution and a highly suboptimal detection scheme.

### Modified Soft-Output Extension

MLSE results in the most likely sequence of symbols, but it does not provide any information about the confidence of the estimation. An extension to the VA called soft-output Viterbi algorithm (SOVA) [93] provides soft-information for the bits of each detected symbol.

The soft-information is represented by means of log-likelihood ratios (LLRs)<sup>5</sup>. In this context, the LLR  $L_{k,i}$  of the  $i$ -th bit in the  $k$ -th symbol is defined as,

$$L_{k,i} = \ln \left( \frac{p(b_{k,i} = 1 | \mathbf{r})}{p(b_{k,i} = 0 | \mathbf{r})} \right). \quad (2.48)$$

In the context of the DDFSE, the sign of the output LLR coincides with the output of a hard-

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<sup>5</sup>Details about the derivation of LLRs can be found in Appendix A.3.



## 2.4. Soft-Output Delayed Decision Feedback Sequence Estimation

decision DDFSE, the magnitude corresponds to the reliability with which this decision was taken.

As it is a-priori not clear which path will end up winning, non-final initial LLR values need to be calculated in all states for all bits. An initial set of estimations for  $L_{k,i}$  can be obtained by dividing  $\mathcal{X}_i(\bar{\mathbf{s}}_k)$  into two disjoint subset. The subset  $\tilde{\mathcal{X}}_i(\bar{\mathbf{s}}_k)$  contains all source states from which a transition would lead to a bit decision of  $b_{k,i} = 1$  and  $\hat{\mathcal{X}}_i(\bar{\mathbf{s}}_k)$  for the remaining source states.

The difference between the joint probability of all path metrics originating from the elements of  $\tilde{\mathcal{X}}_i(\bar{\mathbf{s}}_k)$  and the joint probability of all path metrics originating from the elements of  $\hat{\mathcal{X}}_i(\bar{\mathbf{s}}_k)$  gives an initial estimate  $L_i^1(\bar{\mathbf{s}}_k)$  of the final  $L_i(\bar{\mathbf{s}}_k)$  as

$$L_i^1(\bar{\mathbf{s}}_k) = \ln \left( \prod_{\hat{\mathbf{s}} \in \tilde{\mathcal{X}}(\bar{\mathbf{s}}_k)} e^{\gamma(\hat{\mathbf{s}}, \bar{\mathbf{s}}_k)} \right) - \ln \left( \prod_{\hat{\mathbf{s}} \in \hat{\mathcal{X}}(\bar{\mathbf{s}}_k)} e^{\gamma(\hat{\mathbf{s}}, \bar{\mathbf{s}}_k)} \right). \quad (2.49)$$

This calculation needs to be performed per bit and state.

The complexity of the initial estimation can be significantly reduced by performing a max-log approximation (see Appendix A.4) on the incoming paths. Instead of taking the probability of all paths into account the initial  $L_i^1(\bar{\mathbf{s}}_k)$  is calculated by the difference between the surviving path metric and the smallest non-surviving path metric which would have lead to an opposite decision as

$$L_i^1(\bar{\mathbf{s}}_k) = \min_{\hat{\mathbf{s}} \in \tilde{\mathcal{X}}(\bar{\mathbf{s}}_k)} \gamma(\hat{\mathbf{s}}, \bar{\mathbf{s}}_k) - \min_{\hat{\mathbf{s}} \in \hat{\mathcal{X}}(\bar{\mathbf{s}}_k)} \gamma(\hat{\mathbf{s}}, \bar{\mathbf{s}}_k). \quad (2.50)$$

The calculation in (2.50) takes only the reliability of the initial surviving path decision into account. However, reliability of the final decision for a certain symbol  $s_k$  and therefore its bits does also depend on  $I - 1$  successive decisions, because of the transitions of the path history. In order to achieve full max-log performance, an addition to the SOVA is proposed in [94] as modified SOVA (mSOVA). The mSOVA algorithm calculates the final LLR value in multiple steps following the transitions of the history vector.

An initial value is calculated for each LLR and state, based on the winning path transitions as described in (2.50), the magnitude is then updated with each decision as long as not all paths have merged yet. Every time a state history is replaced in the decision history because of a current state decision (see (2.41)) the reliability value of the history itself is lower-bound by the reliability of the decision which lead to this transition. The mSOVA algorithm is equivalent to a full max-log soft-decision [94].

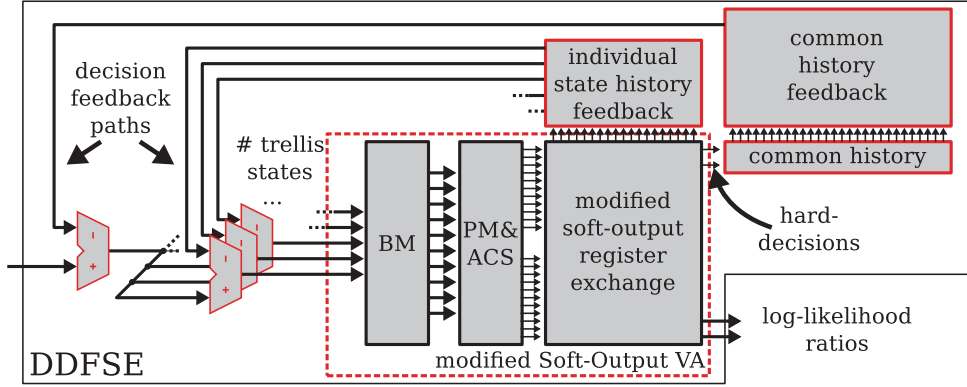


Figure 2.30 – Overview of the DDFSE baseline architecture.

### 2.4.3 Baseline Architecture

The soft-output DDFSE algorithm is essentially a classical soft-output VA with an additional decision feedback stage, hence, the DDFSE architecture shares many components with a classical Viterbi architecture. A straightforward translation of the DDFSE algorithm into a VLSI architecture is depicted in Fig. 2.30. This architecture will be referred to as DDFSE baseline architecture. It consists of a branch metric (BM), a path metric (PM), an add-compare-select (ACS) unit, and the modified soft-output register exchange.

The baseline architecture implements the DDFSE algorithm with the minimal amount of operations, but is not very suitable for high-speed implementation. The additional DFE adds feedback paths with different timing requirements from the output of the Viterbi decoder to its input. In particular, also first order feedback loops are added, which feature a feedback term, which is directly in the following cycle required. In the baseline architecture, the path of a first order feedback loop traverses through all stages of the Viterbi decoder and the decision feedback calculation and becomes the critical path. This critical path is shown in the detailed overview of the baseline architecture in Fig. 2.31. The feedback loop makes the insertion of pipeline registers impossible and therefore, the baseline architecture is unsuitable for the high processing speeds required for mmWave applications.

### 2.4.4 Optimized Architecture

The critical path can be significantly reduced by sacrificing the minimum number of operations property. The order of operations is changed in such a way that as few operations as possible are part of the first order feedback loops. An overview of the optimized architecture with the operation reordering is shown in Fig. 2.32. It can be easily seen that the reordering comes with an increase in the total number of operations required.

A first delay optimization can be achieved by exploiting the fact that the calculation of the history feedback requires only hard-decisions and not soft information. Hence, the complexity

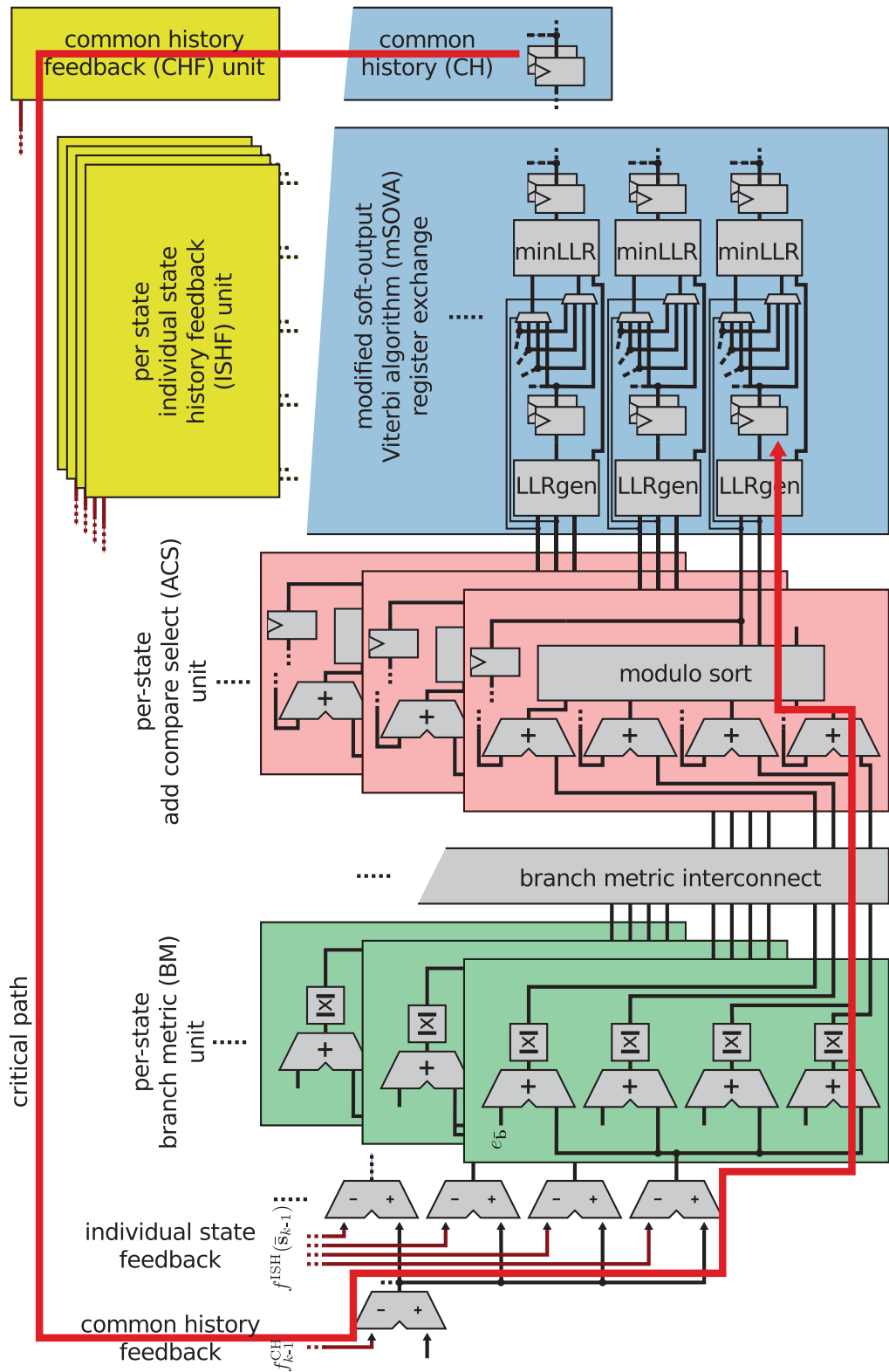


Figure 2.31 – Detailed overview of the DDFSE baseline architecture with the critical path marked in red.

of the LLR calculation can be taken out of the critical path. This optimization comes at the cost of a second register exchange module which stores only (hard) decision histories of all states. After the duplication, the timing of the soft-output generation can be relaxed by inserting a pipeline register at the beginning. The overhead of the register exchange duplication is minor, as the hard-decision register exchange has significantly lower complexity compared to the soft-decision version.

The operations of (2.47) can now be reordered according to their data dependencies, e.g., the reference signal  $e_b$  only depends on the CIR  $\mathbf{h}$  and is time-invariant during the processing of a frame. It can be subtracted without any feedback dependency and therefore moved further to the beginning of the arithmetic operations. Another reordering can be performed for the common history feedback (CHF). In the common history, which is essentially a shift register, only the first register depends on the decision taken in the ACS. Hence, the feedback from all but the first register can be effectively retimed and removed from the critical path. Consequently the CHF is split into two parts, a primary common history feedback which consists only of the feedback of the first decision and a secondary common history feedback for all remaining decisions. The secondary CHF can now be retimed and applied before all other operations.

### Speculative ISH Feedback Calculation

In a classical register exchange the decisions of the ACS unit are not only used to determine the transitions between states, but also become the most recent value of the respective state. As a consequence all possible history vectors for a state at time  $k$  can be predicted using the histories of its source states at time  $k - 1$ . Interestingly, the decision value and therefore the complete predicted history vector only depends on the source state. As a result, there is only one speculative feedback value per state which is identical for all its destination states.

This knowledge can be used to calculate for each state a speculative feedback value in preparation for the case in which this state would be chosen as source state. This allows to break the critical path of the baseline architecture. Due to the speculation, the arithmetic operations of (2.47) do not depend on the decision of the previous cycle. Instead, potential branch metric values are calculated for all possible feedback values from a specific state already before the decision is taken.

The BM unit is split into two parts, a preBM unit, which speculatively calculates all possible branch metric values and a postBM unit, which selects the applicable value and calculates the norm. By inserting a pipeline stage between the preBM and postBM unit, the calculation of the norm and the operations in the ACS unit are removed from the critical path. Practically, this halves the complexity of the critical path and allows a significant increase of the clock speed.

## 2.4. Soft-Output Delayed Decision Feedback Sequence Estimation

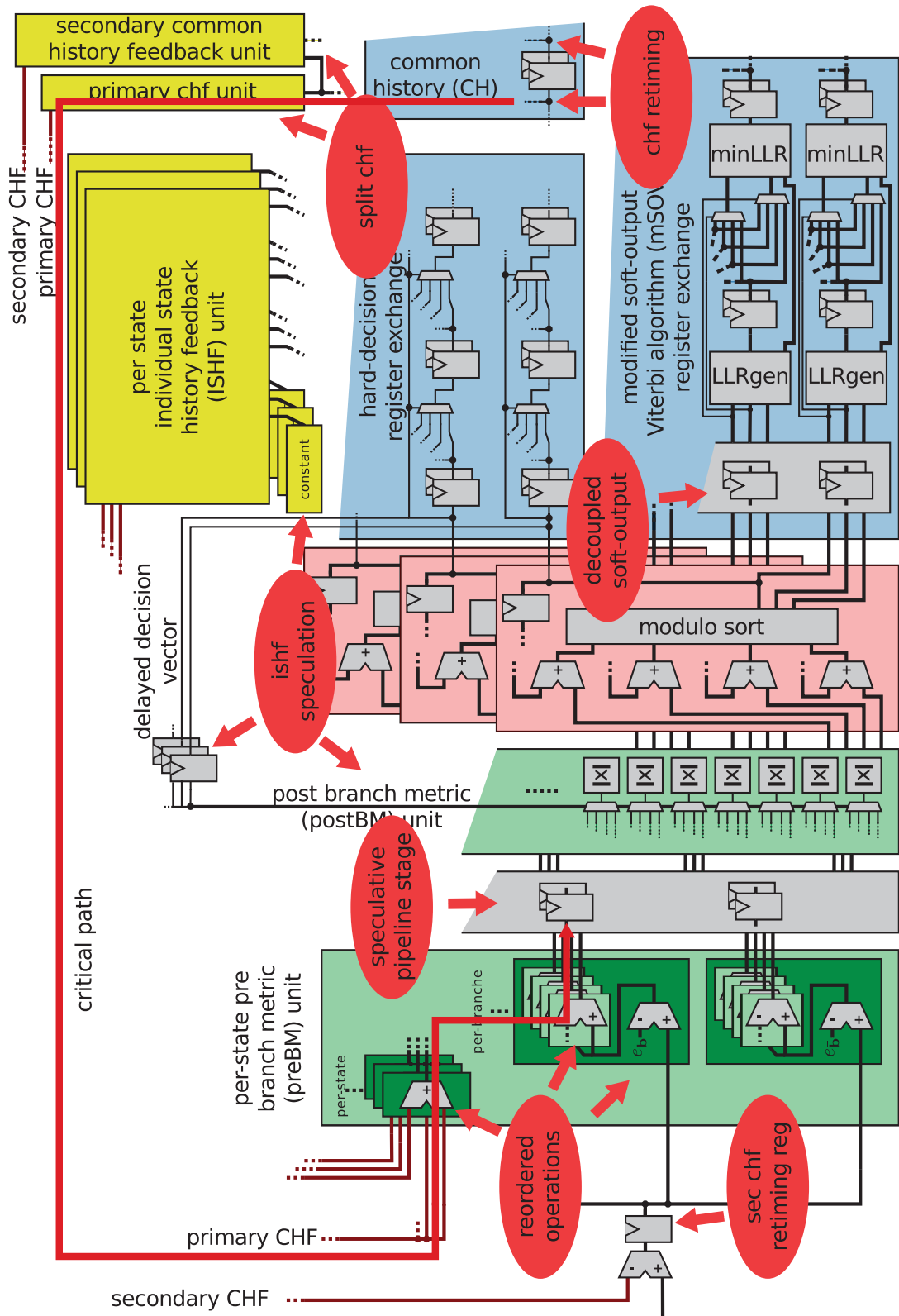


Figure 2.32 – Detailed overview of the optimized DDFSE architecture with a reduced critical path.

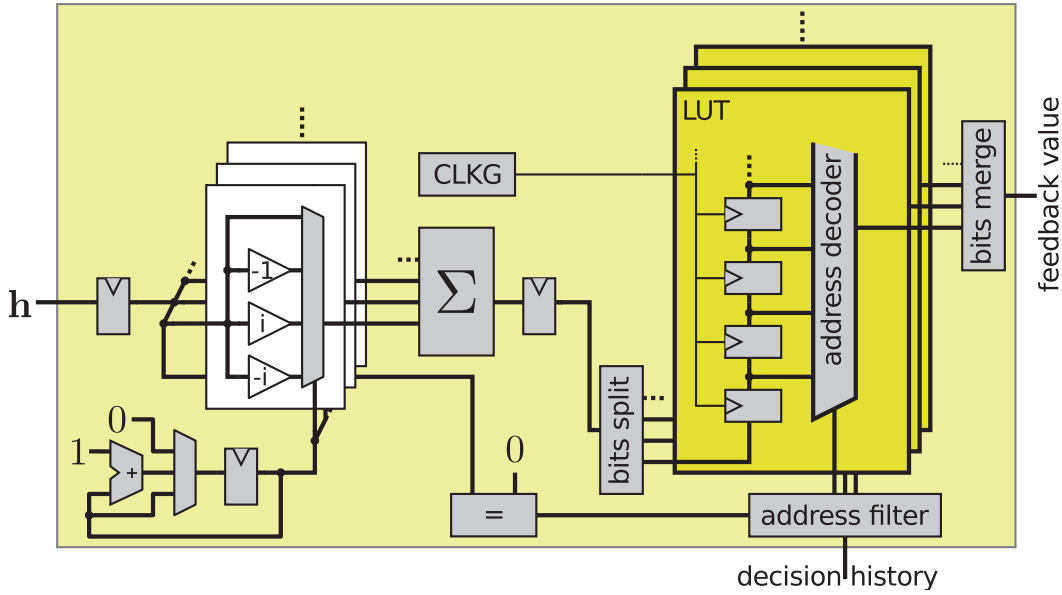


Figure 2.33 – LUT architecture with serial write and parallel read scheme.

### Pre-calculated Look-Up Tables

The calculation of the feedback and the reference values  $e_b$  is performed using look-up tables (LUTs). All possible output values are pre-calculated at the beginning of a frame and stored in a memory. The decision vector input of the feedback unit is used as address for the feedback value storage.

The register-based LUT is implemented in a *serial-in, parallel-out* fashion. The possible feedback words are serially calculated by convolution of the relevant part of the CIR with the output of a counter. Afterwards the feedback value is written to the last entry of the LUT. During the write phase the registers are configured as a shift register and the values are clocked into their respective position. After all values are clocked in the LUT, the clock of the registers can be gated during the actual detection (between the first and the last data symbol of the frame) to reduce the power consumption.

The parallel output of the LUT registers is connected to an address decoder multiplexer. The address decoder selects the correct LUT value based on the input decision vector. For large feedback word widths routing of the address decoder can be problematic during the backend design due to congestion. To address this problem, the LUT can be split into multiple slices of which each stores only some of the bits of the final feedback value. The number of bits per slice is variable to match the requirements of the physical implementation.

The same basic LUT design is used for the generation of the ISHF, the CHF, and the reference values  $e_b$ . The difference between the LUTs is in the number of address inputs and generated output signals. The register based design allows a variable number of address inputs and

## 2.4. Soft-Output Delayed Decision Feedback Sequence Estimation

feedback output ports. While the primary and secondary CHF's generate only a single feedback value each, the individual state history feedback (ISHF) generates one output per state and the LUT for the reference values has each entry hard-wired as a separate output.

The basic feedback unit allows to deactivate parts of the address input, if the corresponding channel coefficient is zero. A zero channel coefficient implies that the associated decision will not affect the feedback. Nevertheless, on any input change the feedback unit will still apply a different address vector to the LUT and cause activity in the address decoder logic. As the main power consumption of the LUT-based feedback calculation comes from switching in the logic tree of the address decoder, a receiver cannot profit from zero channel coefficients and therefore will not exhibit an energy-proportional behaviour. Deactivation of the corresponding address inputs allows the feedback unit to reduce the power consumption with the number of channel coefficients that are zero (energy-proportional operation).

### mSOVA Unit

The mSOVA register exchange (RE) unit calculates the initial LLR values based on a sorted list of PMs and the associated decisions from the ACS. Unlike in a traditional register exchange, the mSOVA RE keeps not only track of the decision of the most likely path, but uses the sorted PMs to evaluate the probability of each decision. Because the reliability is calculated separately for the bits of each symbol, the mSOVA RE always evaluates the decision reliability relative to the next most likely transition which would have led to a different bit decision. In a QPSK scenario it is given that if the first and the second path lead to the same bit decision, the decision associated with the third path must differ in this bit. Hence, the LLRgen unit shown in Fig. 2.34 always calculates the difference between the smallest PM and the two following PMs. Based on the decisions associated with the two winning PMs, the correct value for the reliability is selected. In the case that the first two path metrics would lead to a different bit decision, their difference becomes the reliability, otherwise the PM difference of the first and the third path becomes the reliability of the LLR. The decision of the winning path metric provides the sign for the LLR. The LLR values inside the mSOVA unit are stored and processed in a sign-magnitude format and only converted at the output into a two's complement representation.

After initial calculation, the LLRs enter a soft-information register exchange. While a hard-decision register exchanges swaps only decision histories between states, the soft-decision extension additionally calculates for each transition an upper limit of the LLR magnitudes based on the reliability of this decision. The minLLR unit shown in Fig. 2.35 updates the reliability of the LLR. Similar to the calculation of the initial LLR values, the minLLR unit takes the reliability of the decision and the LLR reliability values of the two most-likely paths into account. In case the bit decisions of the two paths differ, the reliability of the LLR is upper-bound by the reliability of the decision of the swap. If the two bit decisions do not differ, then the LLR is updated using the minimum between the reliability values of the winning path and the sum of the reliability values of the decision and the second path.

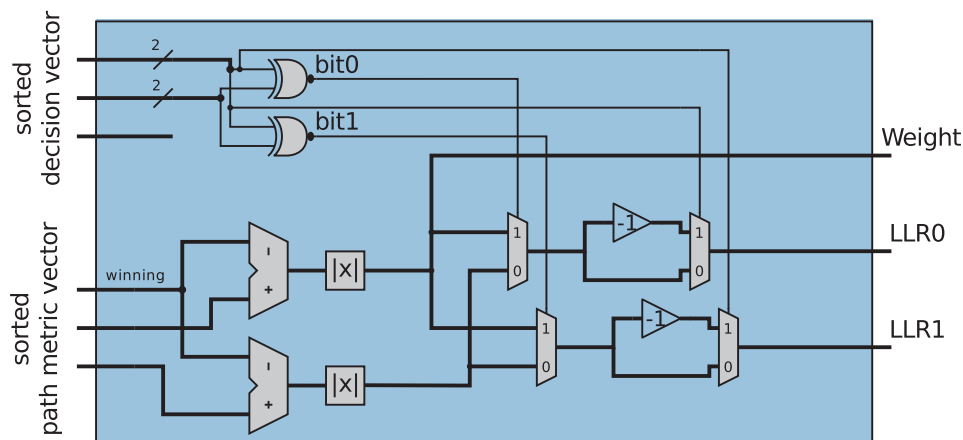


Figure 2.34 – Initial LLR generation unit for modified soft-output register exchange.

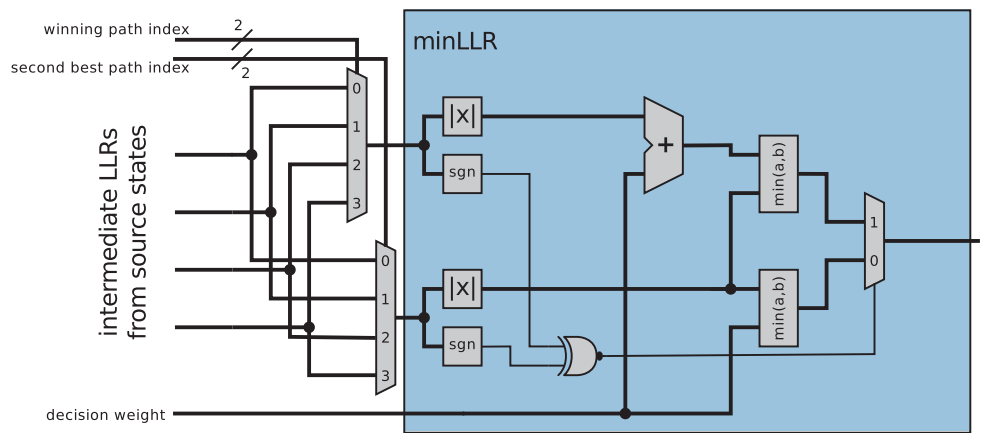


Figure 2.35 – Minimum LLR unit with preceding muxes for path selection.



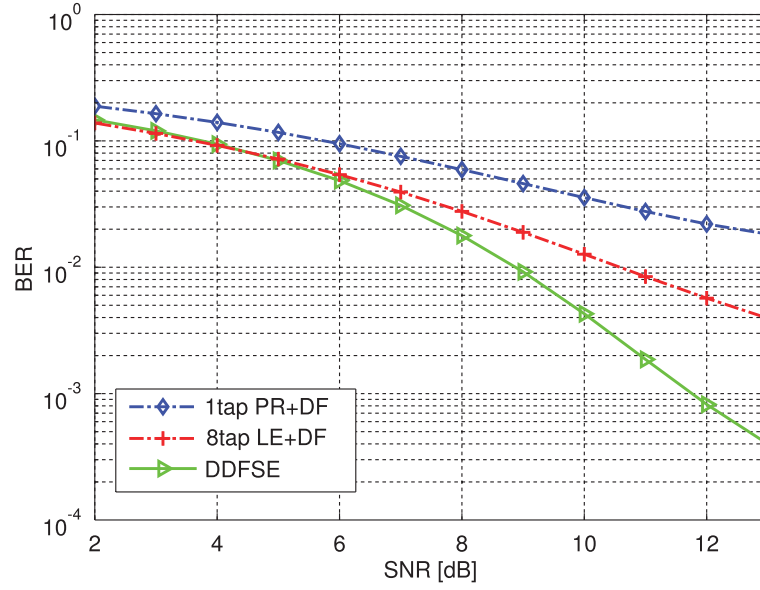


Figure 2.36 – BER performance comparison of single tap phase rotator with decision feedback, 8 taps MMMSE TD-LE and DDFSE receiver in 11ad CB near location scenario.

### 2.4.5 Results

The DDFSE algorithm operates best, if most of the channel energy falls into the trellis window. This is given when the channel exhibits a minimum phase impulse response. In general, a physical channel will not exhibit a minimum-phase characteristic [95], but linear phase-equalization can be used to transform the CIR into an minimum phase equivalent. Such a prefilter was used in [96] to maximize the effectiveness of the DDFSE estimator.

Without the use of a minimum-phase prefilter, the DDFSE requires very specific channel propagation conditions to be effective. However, careful analysis of the 60 GHz channel model shows that there are scenarios in which the DDFSE can leverage its advantage. In the near-location cubicle office (CB) scenario of the IEEE 802.11ad channel model, the DDFSE algorithm can demonstrate its strength. In this scenario, the LOS path is immediately succeeded by strong reflections arising from the compact geometries. The simulations show that the DDFSE with a trellis length,  $D = 3$ , cannot only exploit the energy of the LOS path but also the energy of subsequent reflections. Hence, the DDFSE provides significantly better BER performance compared to a 1-tap phase rotator with DFE as well as an 8-tap MMSE linear equalizer with DFE.

A standalone synthesis and place&route of the DDFSE detector was performed in a 40 nm CMOS process. The resulting floorplan is depicted in Fig. 2.37. The post-layout implementation occupies a cell area of  $0.589 \text{ mm}^2$  and achieves a clock speed of 1.1 GHz in the typical corner (tc) corner. A complete overview of the implementation results is given in Tbl. 2.4.

Dynamic power simulations have been performed with the placed design. The power con-

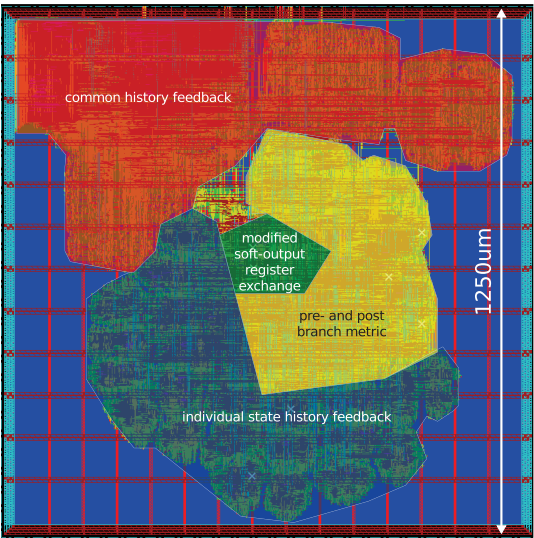


Figure 2.37 – Floorplan of standalone implementation of the DDFSE detector in 40 nm CMOS.

Table 2.4 – Implementation parameters and results for the standalone DDFSE detector.

| Parameters         |           | Results          |                       |
|--------------------|-----------|------------------|-----------------------|
| Trellis length (D) | 3         | Clock speed (tc) | 1.1 GHz               |
| ISH length (I)     | 4         | Instances        | 229854                |
| CHF length (Q)     | 22        | Logic            | 187424                |
| Technology         | 40nm CMOS | Registers        | 42430                 |
|                    |           | Cell area        | 0.589 mm <sup>2</sup> |
|                    |           | Complexity       | 656kGE                |

## 2.5. 11ad Baseband Implementation in 40nm CMOS

Table 2.5 – Power consumption (in mW) of a DDFSE detector core at 880 MHz (half-rate) for the three different operation modes.

| Power [mW]    | LUT Init | Pilot | Data |
|---------------|----------|-------|------|
| Internal      | 157      | 111   | 129  |
| Switching     | 59       | 103   | 125  |
| Leakage       | 10       | 10    | 10   |
| <b>Total:</b> | 216      | 224   | 264  |

sumption of the DDFSE depends heavily on the current operation, hence power consumption is evaluated for three different operation phases. The power numbers for the three different operation phases at a clock speed of 880 MHz are shown in Tbl. 2.5. The first phase is the initialization of the LUTs with values, in this phase the power consumption is dominated by the internal power of the registers. The DDFSE detector consumes 216 mW during the LUT initialization phase. Afterwards, the payload symbols are processed by the DDFSE core. Power consumption is evaluated separately for processing data symbols and the known pilot words, consuming 224 mW and 264 mW power respectively.

## 2.5 11ad Baseband Implementation in 40nm CMOS

Based on the DDFSE algorithm described in Section 2.4, a full baseband chip for mmWave communication is demonstrated. To the best of the authors knowledge, the design is the first ASIC implementation of a sequence-estimation based detector for mmWave communication. The DDFSE baseband supports the IEEE 802.11ad frame structure, described in Section 2.1.3, with preamble, single-carrier block structure and standard-compliant error decoding. In particular the baseband implements

- Time & frequency synchronization
- Channel estimation
- Channel impulse response alignment
- Soft-output sequence estimation
- Deframing
- Error decoding

for a sample rate of 1.76 Gsps and channel impulse responses of up to 29 taps length. A detailed overview of the supported features is provided in Tbl. 2.6.

Table 2.6 – IEEE 802.11ad single-carrier baseband feature overview

|        |                             |   |
|--------|-----------------------------|---|
| Common |                             |   |
|        | Symbol rate                 | 1.76 Gbps   |
|        | Target clock speed          | 880 MHz   |
|        | Parallelism                 | 2×  |
| SYNC   |                             |   |
|        | Frequency Offset Estimation | auto-correlation based                                    |
|        | CFO compensation            | rotator   |
|        | SFO compensation            | interpolator  |
| CE     |                             |   |
|        | Type                        | Time-Domain   |
|        | Algorithm                   | efficient Golay correlator (EGC)                          |
| DDFSE  |                             |   |
|        | Modulation                  | BPSK/QPSK   |
|        | Trellis Length              | 3   |
|        | Individual State Feedback   | 4   |
|        | Common History Feedback     | 22  |
|        | 11ad pilot support          | yes   |
| LDPC   |                             |   |
|        | Schedule                    | Layered   |
|        | Code-word Size              | 672   |
|        | code-rate                   | $\frac{1}{2} / \frac{5}{8} / \frac{3}{4} / \frac{13}{16}$ |

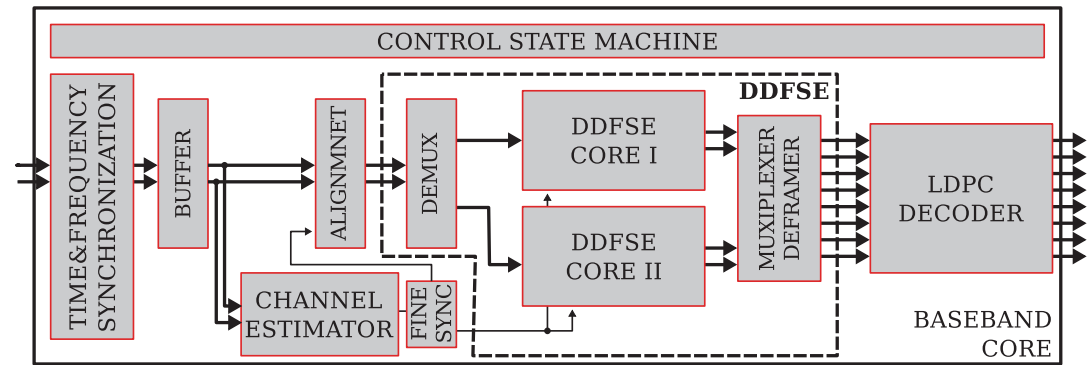


Figure 2.38 – Block diagram of the proposed 60 GHz baseband based on reduced state sequence estimation.

### **2.5.1 Architecture**

The top-level block diagram of the IEEE 802.11ad baseband is shown in Fig. 2.38. The implemented features are summarized in Tbl. 2.6. The baseband implements a data-flow based control model, which achieves synchronization between blocks with hand-shaking on all interfaces. A detailed description of the methodology is given in [97]. A minimal central state machine controls the overall behaviour by sending high-level commands to the different modules. Every command leads to a deterministic amount of data being read and processed by a module. Each module incorporates a state machine on its own, which keeps track of the number of processed samples. Using handshaking and small intermediate buffers between modules provides a high degree of flexibility regarding the implementation of each module.

#### **Synchronization**

The auto-correlation based synchronization module uses the STF of the preamble for time synchronization and FO estimation. A complex rotator and an interpolator, implemented as feed forward filter, correct carrier and sampling frequency offset. A subsequent channel estimation (CE) unit performs time-domain estimation of the CIR. The CIR is estimated over a 64 coefficients window, which is significantly longer than what is used for detection. An intermediate alignment stage adjusts the starting point of CIR and data symbols, as described in Section 2.2.2, in order to maximize the performance of the subsequent detector module.

#### **Detection**

Detection of the BPSK or QPSK data symbols of the payload is performed using the delayed decision feedback sequence estimation (DDFSE) algorithm described in Section 2.4. As the targeted symbol rates for the proposed mmWave system exceed the clock frequencies for which the DDFSE algorithm can be implemented in a power efficient way, the design requires some parallelization of the detection. A two way parallelism with a target clock speed of 880 MHz was chosen for the implementation. Because of the operation principle of the Viterbi algorithm, a DDFSE detector needs to operate on a continuous sequence of symbols. Hence, unlike other receiver circuits, the DDFSE circuit cannot be parallelized on a per symbol base. In order to operate two DDFSE detector cores in parallel, the block structure of the IEEE 802.11ad payload field is exploited to segment the data without performance penalty. As mentioned before, the pilot words decouple the dependencies between symbols of different payload blocks and allow to perform independent sequence estimation on a single payload block. In order to satisfy the required throughput, two DDFSE detector cores operating at 880 MHz are instantiated. A detailed overview of the two-core DDFSE architecture is shown in Fig. 2.39. Subsequent blocks of the payload field are buffered by first-in first-out (FIFO) memories and processed on one of the two soft-output Radix-2 DDFSE cores operating at half the symbol rate. The two resulting LLR streams are again buffered and multiplexed in the correct order. After the pilot data is removed, the LLR stream is segmented in chunks of code-words and

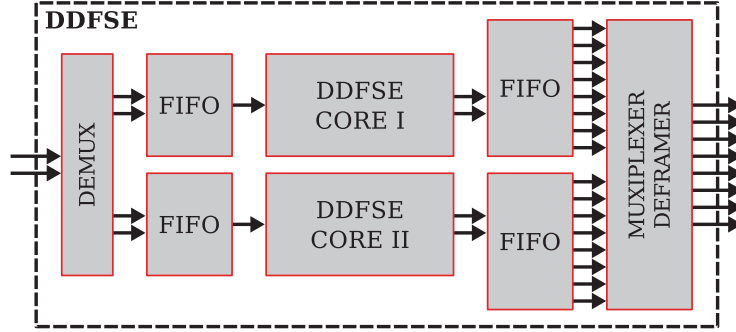


Figure 2.39 – Architecture of the DDFSE module with two instantiated detector cores.

forwarded to the subsequent LDPC channel decoder.

### Error Decoding

As can be seen in Fig. 2.38, the interface between the DDFSE mux and the LDPC decoder is eight LLRs wide, instead of four LLRs required for a half-rate architecture. This over-provisioning of the bus allows to write the LDPC decoder memories at twice the speed, and therefore allows to use the output FIFO of the DDFSE module as buffer for read and write operations on the shadow memory in the LDPC decoder. With only little additional overhead for the interface, the LLR buffering requirements of the LDPC decoder are reduced by a third.

The LDPC decoder itself is implemented as doubly parallel offset min-sum (OMS) decoder with a layered schedule. The decoder exploits not only the quasi-cyclic structure of the LDPC code in order to parallelize the processing, it also operates on two distinct set of columns in parallel. The layered schedule with a variable number of iterations is governed by a control sequences, that is rate dependent. A code-word size of 672 and all four rates specified by the IEEE 802.11ad standard are implemented. Early termination can be enabled to save power in high SNR operating regimes. A detailed description of the architecture can be found in [98].

### 2.5.2 Implementation

The proposed 11ad baseband design was fabricated in 40nm CMOS technology. A micrograph of the fabricated chip is shown in Fig. 2.40. The available core area is  $2.7 \text{ mm}^2$  and the design was placed with a core utilization of 67 %. The core area contains also an internal clock generation unit and dedicated test structures. Details on the complexity of the different modules are listed in Tbl. 2.7.

The test structures comprise a command buffer and a memory for test vectors. The test

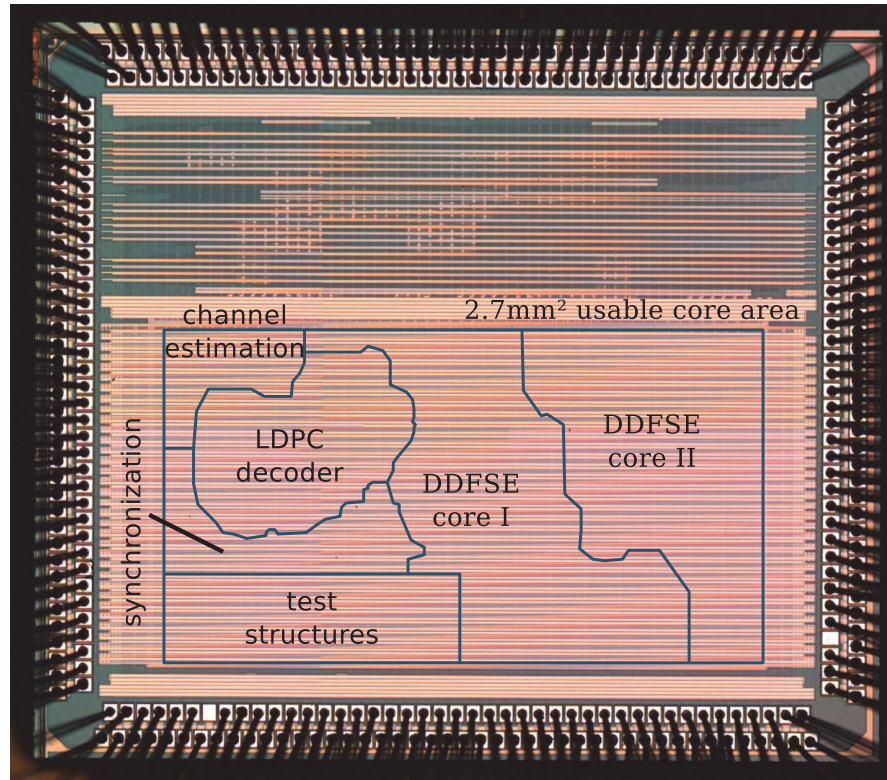


Figure 2.40 – Micrograph of the 11ad baseband manufactured in 40 nm CMOS. The chip accommodates two independent designs in a single pad frame.

Table 2.7 – Key facts of 11ad baseband VLSI implementation.

|                 |                   |  |
|-----------------|-------------------|--|
| CMOS Technology |                   | 40 nm                                  |
| Core Area       |                   | 2.7 mm <sup>2</sup> (Utilization: 67%) |
| Measured Clock  |                   | 940 MHz                                |
| Gate Count      | Synchronization   | 139 kGE                                |
|                 | Channel Estimator | 64 kGE                                 |
|                 | DDFSE core I+II   | 1443 kGE                               |
|                 | LDPC Decoder      | 363 kGE                                |
|                 | Clock Tree        | 75 kGE                                 |
|                 | Reset Tree        | 25 kGE                                 |
|                 | Control&Buffer    | 97 kGE                                 |
|                 | Test Structures   | 457 kGE                                |
|                 | <b>Total</b>      | <b>2563 kGE</b>                        |



Table 2.8 – Comparison of mmWave SC receivers

|      | [27]                 | [99]                  | [65]                   | [100]                 | This Work              |
|------|----------------------|-----------------------|------------------------|-----------------------|------------------------|
|      | BPSK                 | BPSK<br>QPSK<br>QAM16 | BPSK<br>QPSK           | BPSK<br>QPSK<br>QAM16 | BPSK<br>QPSK           |
| Sync | no                   | yes                   | yes                    | yes                   | yes                    |
| CE   | yes                  | no                    | yes                    | yes                   | yes                    |
| EQ   | LE                   | 1-tap                 | OS-FDE                 | RLS                   | DDFSE                  |
| DF   | yes                  | no                    | no                     | no                    | yes                    |
| Code | no                   | LDPC                  | LDPC                   | LDPC                  | LDPC                   |
| CMOS | 65 nm                | 40nm                  | 40 nm                  | 65 nm                 | 40 nm                  |
| Core | 2.34 mm <sup>2</sup> | 1.15 mm <sup>2</sup>  | 46.62 mm <sup>2a</sup> | 16 mm <sup>2b</sup>   | 2.7 mm <sup>2</sup>    |
| Rate | 2 Gb/s               | 6.3 Gb/s              | 1.8 Gb/s               | 4.6 Gb/s              | 3.52 Gb/s <sup>c</sup> |

<sup>a</sup>including ADC/DAC,TX,MAC

<sup>b</sup>including ADC/DAC,TX,uP

<sup>c</sup>at 1.15 V core supply

memory can be loaded and unloaded at a reduced clock speed to overcome limitations of the I/O interface. The memory is not only used for the input samples of the baseband, but also stores the output of the channel decoder.

## Results

Measurements of the fabricated chip were performed in order to verify its correct operation. The required throughput could be achieved with a core supply voltage of 1.15 V. The number constitutes an upper bound, as due to limitations of the measurement setup not all IR-drop on the test setup could be accounted for. The given throughput values specify the raw throughput. The net data rate depends on the used pilot word scheme and code-rate. The comparison of the results in Tbl. 2.8 shows that the proposed DDFSE does not support as high modulation orders as proposed linear equalizer-based basebands, nevertheless, for low modulation orders DDFSE can achieve better performance with little additional complexity overhead.

## 2.6 Summary

The analysis of the mmWave propagation characteristics shows the potential of 60 GHz for high speed Wi-Fi applications, but also indicates implications on the mmWave receiver design. The large variations in excess delay spread lead to algorithmic trade-offs between flexibility and complexity. Hence, the design of mmWave receivers is very much influenced by the usage scenarios, leading to the two distinct architecture choices of implementing mmWave receiver either based on equalization in TD or in FD.



The intended usage scenario has not only implications for the equalizer choice, but also on other parts of the receiver design. A set of improvements to previously proposed time-domain parameter synchronization algorithms extend the range of possible operation regimes for IEEE 802.11ad baseband receivers and maximize system performance.

Successful synchronization in frequency-selective environments is a prerequisite for powerful frequency-domain baseband equalization. SC-FDE leverages the efficiency of the FFT to operate single-carrier systems with reasonable complexity in delay spread environments that used to be reserved for OFDM systems. While SC-FDE is significantly more complex than traditional TD-LE, the overhead of SC-FDE is put in relation, when the baseband signal processing is considered as a whole. SC-FDE architectures allow a low-complexity integration of synchronization and decimation filters improving the over-all system efficiency. With EP-FDE some energy-adaption can be added to the conventional SC-FDE allowing to reduce the receiver complexity in short delay spread environments achieving energy-proportional operation.

On the contrary, DDFSE is a special-purpose time-domain algorithm approximating the ML solution for channels with a certain time-domain characteristic. State space reduction is achieved using decision feedback. Reordering, precalculation and speculation enable an optimized DDFSE architecture which can process Gsps. The DDFSE implementation as part of a time-domain IEEE 802.11ad baseband proves the feasibility of sequence estimation for mmWave systems. The complete baseband was implemented and manufactured in 40 nm CMOS with a complexity of 2.6 MGE.



### 3 Complex Sub-Sampling Receiver

Today the most common topology for wireless receiver front-ends is the direct-conversion (DC) (sometimes also called Zero-IF) receiver shown in Fig. 3.1a. The desired signal with a bandwidth  $W$  is directly down-converted from radio frequency (RF) to a complex baseband signal by means of two quadrature mixers. The resulting baseband signal is sampled with two ADCs with a sampling rate  $f_s = W$ . DC receivers are popular because they require few (but precise) components. For good performance the two down conversion stages need to be closely matched and components need to operate over a wide frequency range extending down to zero.

In case direct conversion is technically not feasible, a heterodyne architecture can be used, in which the RF signal is first down-converted by a single mixer to an intermediate frequency (IF) signal. The IF signal is filtered and amplified and afterwards either down-converted by a quadrature mixer to baseband (cf. Fig. 3.1b) or to another IF. While the heterodyne architecture requires more components compared to a DC receiver, it is usually easier to realize due to the relaxed requirements on oscillators and mixers. Consistent with [101] the term *heterodyne* receiver will be used in the following synonymous with *super-heterodyne* receiver for any receiver which has multiple conversion stages.

A possible way to reduce the complexity of the heterodyne receiver is direct sampling of the IF signal. The real IF signal is then digitally down-converted and filtered to obtain a complex-valued baseband signal. Such a digital-IF architecture (cf. Fig. 3.1c) offers not only many of the advantages of analog heterodyne receivers, but also avoids the problem of imbalance and offsets in the quadrature mixing stage. The downside of this receiver architecture are the stringent requirements on analog bandwidth and sampling rate of the ADC. In order to satisfy the Nyquist rate, the sampling frequency needs to be larger than twice the IF frequency  $f_{\text{IF}}$  plus half the signal bandwidth ( $f_s \geq 2f_{\text{IF}} + W$ ). The high sampling rate is a significant problem for system integration not only because of the increased requirements on the ADC, but also because of the significantly increased number of samples that need to be processed in the digital domain.

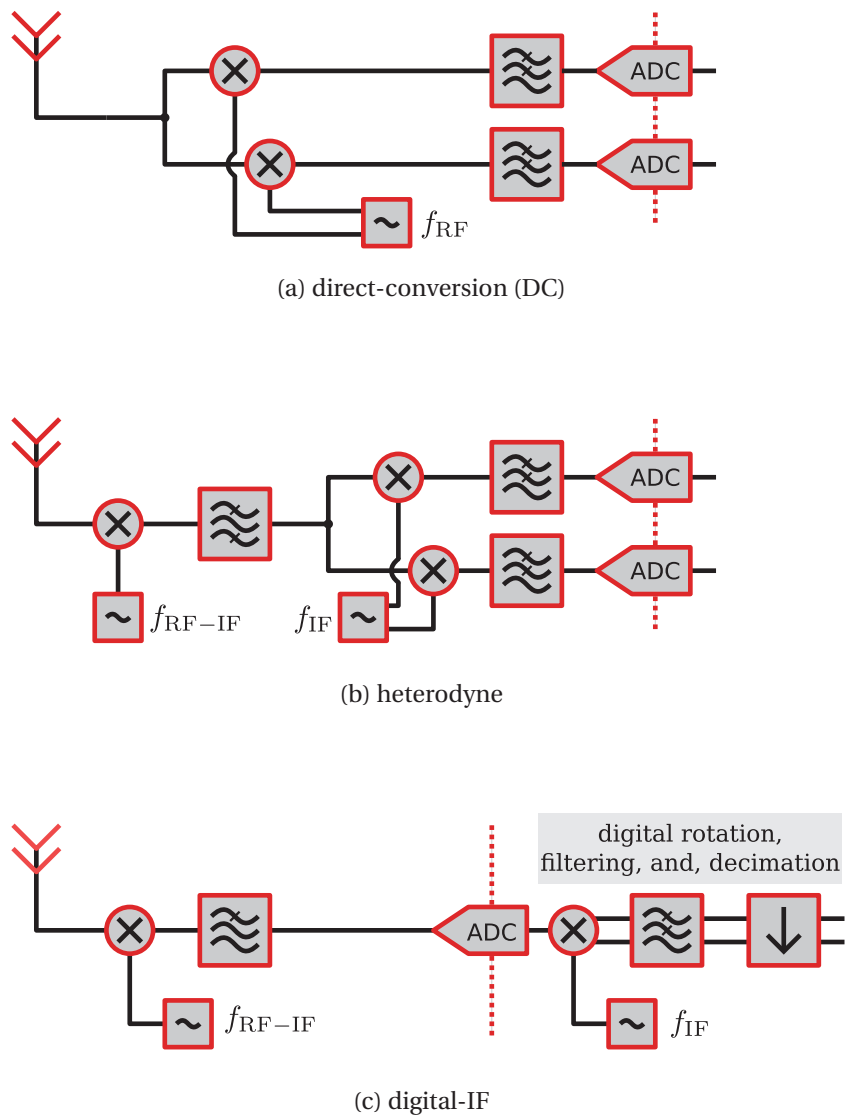


Figure 3.1 – The most common RF front-end architectures for wireless receivers.

The required sampling rate renders digital-IF architectures currently close to impossible for mmWave systems. The necessary ADCs would be at the edge of what is currently economically feasible and the large number of samples to process would imply very power hungry baseband circuits. However, the required sampling rate can be significantly reduced, if knowledge about the structure of the sampled IF signal is leveraged [102]. Under certain conditions the IF signal can be fully recovered despite being sampled below the Nyquist rate (sub-Nyquist sampling). Hence, sub-sampling (sometimes also called under-sampling or bandpass-sampling) has been suggested [103] for low power designs of narrow band communication systems. Sub-sampling the IF signal combines the analog design advantages of heterodyne receivers with the low analog part count and low digital complexity of DC receivers.

The idea of sub-sampling the IF signal for a low-complexity 60 GHz receiver was proposed in [104] and later outlined in more detail [105]. The authors propose an architecture based on delayed sampling clocks and charge domain subsamplers for QPSK. The architecture demonstrates that sub-sampling mmWave receivers can be realized with very small analog frontends, but the proposed solution requires four-way oversampling of the signal bandwidth, and thereby puts a significant burden on the digital baseband part. The necessary oversampling renders this type of sub-sampling architecture unappealing for 60 GHz applications.

An alternative sub-sampling architecture that combines a small analog footprint with efficient digital baseband processing is presented in this chapter. First, the general theory of sub-sampling receivers and their practical limitations are discussed. Afterwards, the general concept of complex sub-sampling is presented and it is shown that it provides significantly more flexibility compared to real-valued sub-sampling. A possible implementation of complex sub-sampling using a passive hybrid coupler is presented and the implication of component non-idealities on the signal quality is discussed. Finally, a way how to compensate analog non-idealities of the complex sampling chain in the digital domain is proposed and an architecture how such a compensation can be integrated in the baseband digital signal processing chain is presented.

## 3.1 Sub-Sampling Receiver

The aliasing theorem generalizes the Nyquist-Shannon sampling theorem to the case where the sampled signal,  $x(t)$ , is not bandlimited to  $\frac{f_s}{2}$  [106]. The spectrum of a sampled signal,  $x[n]$ , is

$$X(e^{j\omega}) = f_s \sum_{k=-\infty}^{\infty} X_c(j\omega f_s - j2\pi f_s k), \quad -\pi \leq \omega < \pi. \quad (3.1)$$

The spectrum becomes periodic by accumulating shifted copies of the spectrum  $X_c$  of the continuous signal  $x(t)$ .

It can be easily verified that this theorem is a generalization of the Nyquist-Shannon sampling

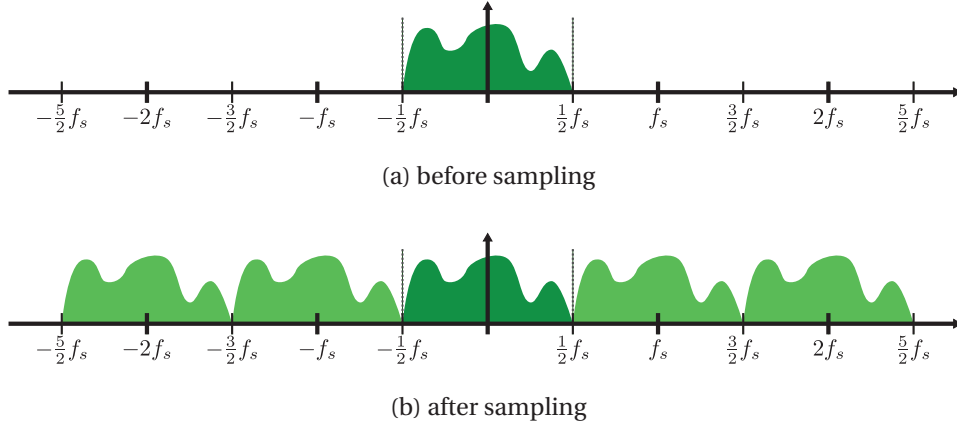


Figure 3.2 – Spectrum of bandlimited signal before (Fig. 3.2a) and after (Fig. 3.2b) sampling

theorem, by considering the case of a bandlimited signal  $x(t)$  (cf. Fig. 3.2a) where

$$X_c(j\omega) = 0, \quad \omega \geq \frac{f_s}{2}. \quad (3.2)$$

In this case the formula reduces to the well-known sampling theorem (cf. Fig. 3.2b)

$$X(e^{j\omega}) = f_s X_c(j\omega f_s). \quad (3.3)$$

Simply speaking, the sampling theorem states that all the information of the spectrum of the continuous signal is preserved in the spectrum of the sampled sequence when  $f_s$  is larger than twice the highest non-zero frequency component of the sampled signal.

The special case when the sampling frequency is exactly twice the highest frequency component of the sampled signal is denoted critical sampling, and the sampling frequency is termed the Nyquist rate. From an information theoretic perspective, critical sampling is the most efficient way to digitize a bandlimited signal, as it uses the minimal number of samples required for perfect reconstruction.

Examining the graphical representation of the aliasing effect in Fig. 3.2b, it is clear that there exist non-baseband signal configurations which preserve the complete spectrum of the continuous signal after sampling. For example, the spectrum of the real passband signal shown in Fig. 3.4a is fully preserved after sampling (cf. Fig. 3.4b) as no frequency components fold on top of each other. The corresponding architecture for sub-sampling is shown in Fig. 3.3. As a difference to Fig. 3.1c a filter is required which ensures the passband nature of the sampled signal. It is important to note that because of the single sampling dimension, the resulting sub-sampled signal needs to be sampled at twice the frequency of an equivalent complex baseband signal.

Unfortunately, spectrum preserving sub-sampling is only possible for a very limited set of sig-

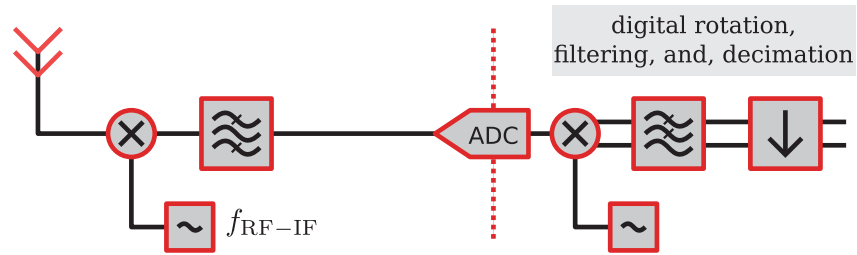


Figure 3.3 – IF sub-sampling receiver architecture using passband filter to avoid aliasing.

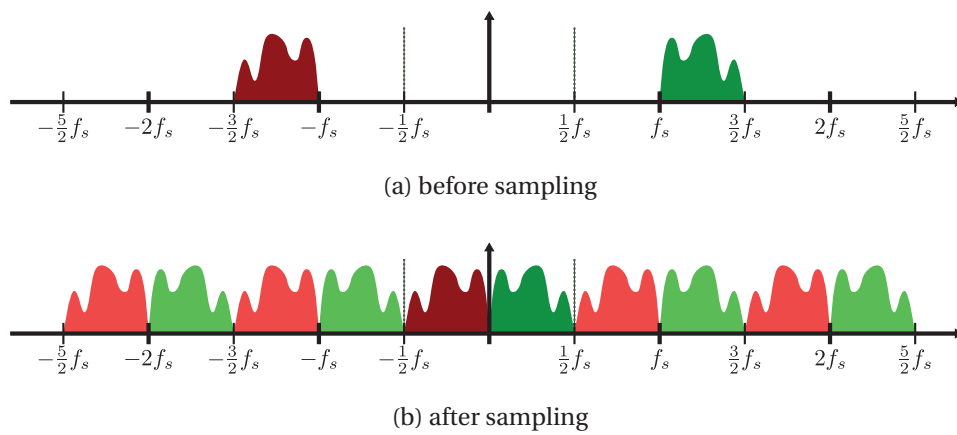


Figure 3.4 – Real passband signal with bandwidth equal or below half the sampling bandwidth.

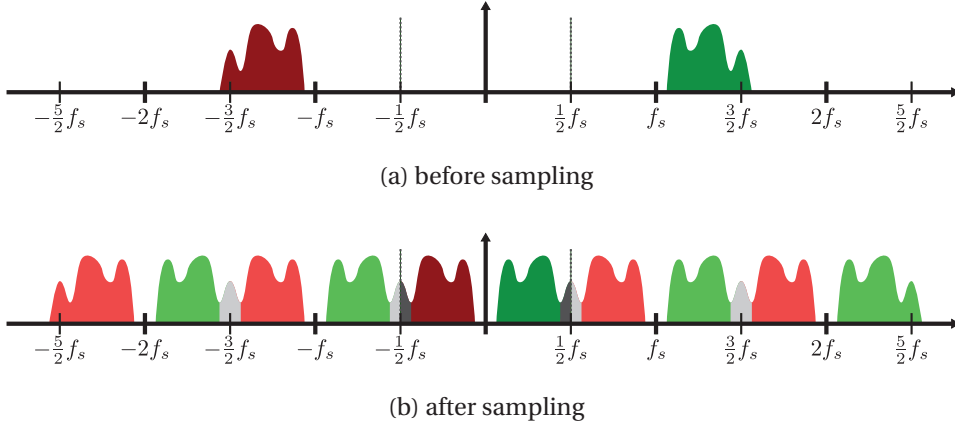


Figure 3.5 – Shifted real passband signal with bandwidth equal or below half the sampling bandwidth which is NOT confined to a Nyquist zone.

nal configurations. Figure 3.5a shows a slightly shifted version of Fig. 3.4a, which is corrupted at the edges after sub-sampling (cf. Fig. 3.4b) due to aliasing. In general, no corruption occurs only if the signal falls completely within a frequency region given by a set of boundary points  $b_k$ ,  $k \in \mathbb{Z}$ . The boundary points can be found as a function of the sampling frequency as

$$b_k = k \frac{f_s}{2}. \quad (3.4)$$

In the ADC terminology these regions are usually called Nyquist zones [107] and are enumerated for the positive frequency axis. Hence, the condition for the placement of the carrier frequency  $f_c$  for a signal with bandwidth  $W$  as a function of the Nyquist zone  $k$  and the sampling rate  $f_s$  can be expressed as

$$\frac{1}{2} ((k-1)f_s + W) \leq f_c \leq \frac{1}{2} (kf_s - W). \quad (3.5)$$

Normalized with the signal bandwidth  $W$  this formula can be rewritten

$$\frac{1}{2} \left( (k-1) \frac{f_s}{W} + 1 \right) \leq \frac{f_c}{W} \leq \frac{1}{2} \left( k \frac{f_s}{W} - 1 \right). \quad (3.6)$$

The normalized formula allows the very intuitive graphical depiction of the constraint introduced by sub-sampling shown in Fig. 3.6. The admissible regions for the normalized carrier frequency  $\frac{f_c}{W}$  as function of the normalized sampling rate  $\frac{f_s}{W}$  are colored in green. Each admissible region corresponds to a Nyquist zone  $k$ . It is observed from Fig. 3.6, that IF placement flexibility can only be obtained at the cost of increasing the sampling rate. For the desirable case of critical sampling, which corresponds to a normalized sampling rate of  $f_s/W = 2$ , the IF



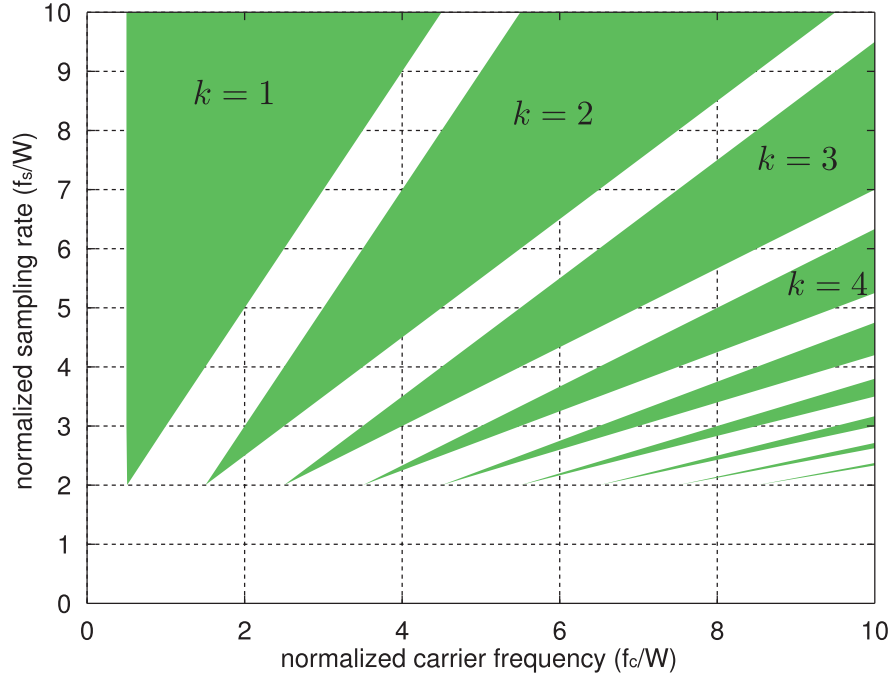


Figure 3.6 – Admissible placement regions (green) of the normalized carrier frequency for the Nyquist zones  $k$  in a real sub-sampling receiver.

signal can only be placed on a discrete set of frequencies

$$f_{c,k} = \frac{f_s}{4} + k \frac{f_s}{2}, \quad k \in \mathbb{Z}. \quad (3.7)$$

The set of usable center frequencies is further reduced by the requirement that the desired signal has to fall within the analog bandwidth of the ADC. These constraints are especially severe for systems with a high symbol rate as the analog bandwidth requirement becomes quickly prohibitive. The lack of flexibility of sub-sampling receivers is cited to be the biggest obstacle for their adoption despite the numerous advantages [102].

### 3.2 Complex Sub-Sampling

Complex sub-sampling is an alternative method to digitize a passband signal at sub-Nyquist rate while providing a significantly higher flexibility for frequency planning. Instead of directly sampling the real passband signal, an analytic version is created in the analog domain and sampled with two ADCs.

The analytic representation of a real-valued signal,  $x(t)$ , is a complex-valued signal,  $\hat{x}(t)$ , with

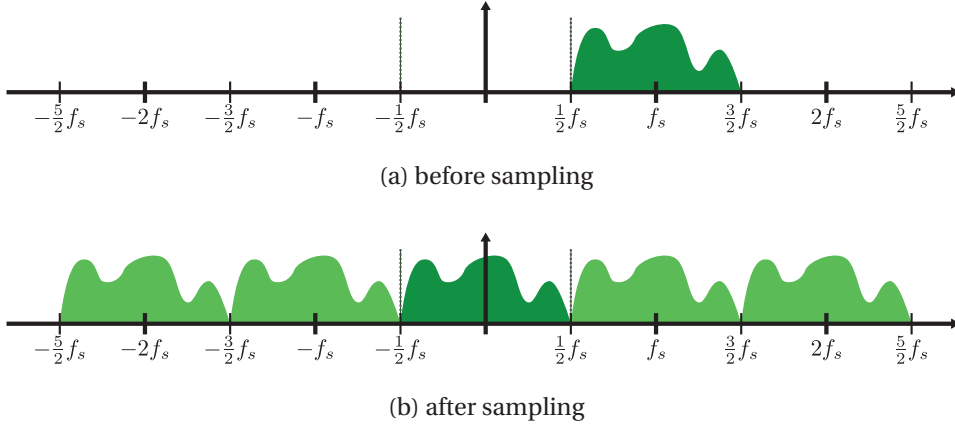


Figure 3.7 – Analytic complex passband signal with bandwidth equal or below half the sampling bandwidth

the following property in the frequency-domain

$$\hat{X}(f) = \begin{cases} 2X(f) & , f > 0 \\ X(f) & , f = 0 \\ 0 & , f < 0. \end{cases} \quad (3.8)$$

The analytic representation exhibits a scaled version of the original spectrum for all positive frequencies, while having no negative frequency components (cf. Fig. 3.7a).

$\hat{X}$  can be created with the help of the Hilbert transform ( $\mathcal{H}$ ) as

$$\hat{X} = \frac{1}{2} (X(f) + j\mathcal{H}(f)X(f)). \quad (3.9)$$

In frequency-domain, the Hilbert transform is defined as

$$\mathcal{H}(f) = \begin{cases} -j & , f > 0 \\ 1 & , f = 0 \\ j & , f < 0. \end{cases} \quad (3.10)$$

It is obvious that the transformation between real and analytic representation is loss-less and therefore reversible.

Because of the lack of any negative frequency components an analytic signal is not corrupted by sub-sampling as long as the sampling bandwidth is larger than the signal bandwidth (cf. Fig. 3.7b). In particular, the center frequency can be arbitrarily placed, relative to the Nyquist zones of the ADCs. The architecture of a complex sub-sampling receiver is shown in Fig. 3.8. While complex sub-sampling requires two ADCs, the sampling rate is only half of the *real*

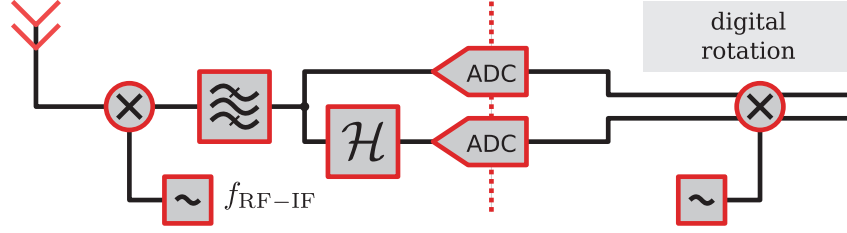


Figure 3.8 – Complex sub-sampling with two ADCs.

sub-sampling case, and therefore the total number of required samples remains unchanged.

A possible method to create a complex IF signal is the use of IQ mixers, as proposed in [108] for fiber-optics systems. Unfortunately, this method requires two matched and very wide-band mixers, very similar to a DC architecture. An even bigger disadvantage of this method for wireless systems is that the resulting system is only analytic if there is no energy at the image frequency of the mixer. This requires either a high IF which makes the sub-sampling challenging or steep pre-selection filters at RF which are difficult to realize.

### 3.2.1 Non-Ideal Complex Sub-Sampling

A complex IF signal can also be generated from a real IF signal. The analog device that performs the Hilbert transform is the  $90^\circ$  hybrid directional coupler. A directional coupler (also just called coupler) is a passive microwave device featuring four ports (cf. Fig. 3.9a) divided in two groups of two ports (Port 1&4/Port 2&3<sup>1</sup>). The  $90^\circ$  hybrid coupler is highly symmetrical as any input in one of the ports is outputted on both opposing ports with a  $90^\circ$  phase difference and 3 dB attenuation, while the fourth port remains isolated (cf. Fig. 3.9b). The signal outputted on the  $90^\circ$  shifted port three can be considered the Hilbert transformation of the signal out of port two.

For the generation of the analytic signal in a complex sub-sampling receiver, ports two and three are connected to two ADCs as shown in Fig. 3.9c. The real IF signal  $s(t)$  is fed into port 1, such that port 2 and 3 provide the real and the imaginary part of the analytic version  $\tilde{s}(t)$ . The remaining fourth port is terminated with a matched  $50\ \Omega$  load to absorb any unwanted reflections.

In practice,  $90^\circ$  hybrid coupler provide the Hilbert transform only within a certain precision and only over a limited frequency band. The  $90^\circ$  separation between the two coupler output ports is only given within some degree precision and the magnitude of the branches can further vary significantly over the bandwidth of the signal. The wider the frequency band, the more challenging it becomes to match the two outputs.

<sup>1</sup>Enumeration is not consistent in literature, here the enumeration shown in Fig. 3.9a is used.

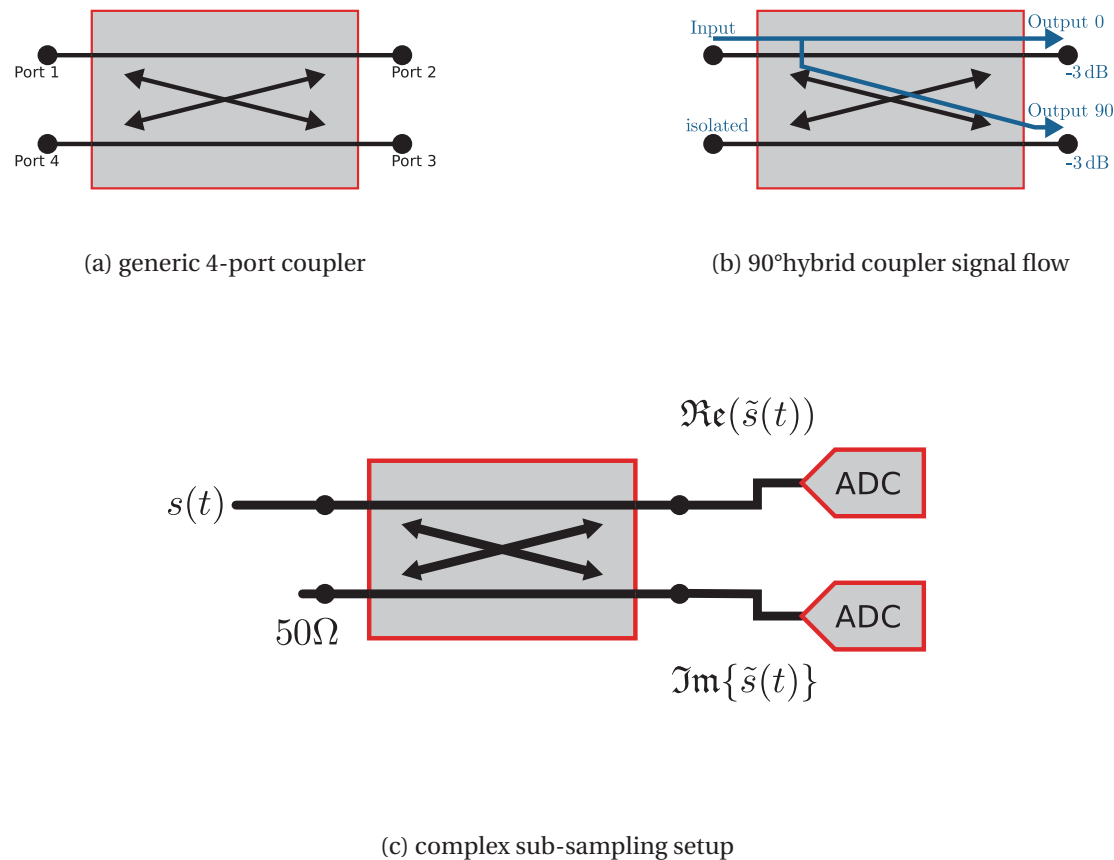


Figure 3.9 – Overview of a generic 4-port coupler device, the signal flow in the used 90° hybrid coupler and the use of the coupler in the sub-sampling setup.

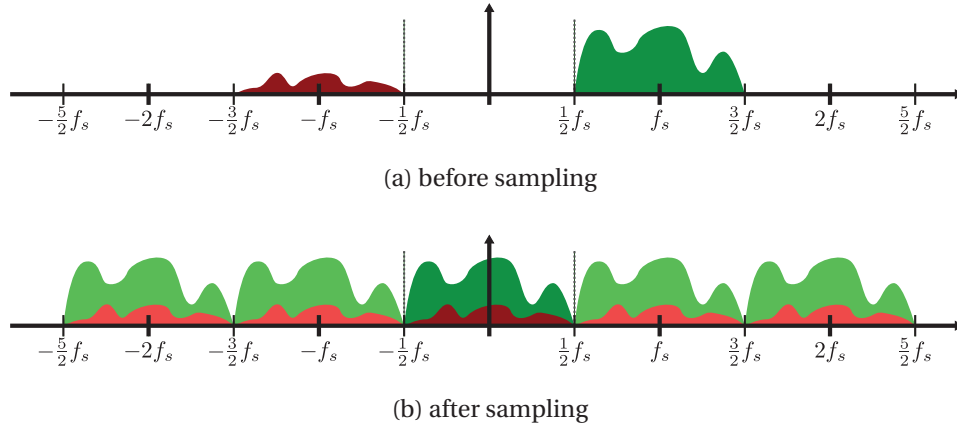


Figure 3.10 – Non-ideal analytic complex passband signal with bandwidth equal or below half the sampling bandwidth

Any imbalance in the coupler branches results in an imperfect analytic output signal with residual negative frequency components (cf. Fig. 3.10a). During sub-sampling, the residual negative frequency components will fold on top of the desired positive signal and consequently appear as interference (cf. Fig. 3.10b). This interference is highly correlated with the actual signal and therefore causes strong geometric distortion in the recovered constellation<sup>2</sup>. Without compensation, coupler imbalance greatly limits the signal quality of complex sub-sampling receivers.

### 3.2.2 Non-Ideal Coupler Compensation

Fortunately, compensation of the coupler imbalance is possible. In particular, it is not only feasible in analog domain before the sampling, but also after sampling in digital domain. The latter is especially interesting as no additional analog components are required and the receiver can take full advantage of digital VLSI scaling effects. In this case digital compensation can be performed after sub-sampling of the IF signal has already occurred and after the negative interference was already folded on top of the useful signal.

The non-ideal coupler can be seen as a linear time-invariant (LTI) system (cf. Fig. 3.11) in which the in-phase and the 90°-shifted signal go through independent linear filters  $h_{\Re}$  and  $h_{\Im}$ . We define the real input signal of the coupler  $y(t)$  and its Fourier transform as  $Y(j\omega)$ . Hence the (continuous) output of the coupler in frequency-domain is the pair

$$\hat{Y}_{\Re}(j\omega) = H_{\Re}(j\omega)Y(j\omega) \quad (3.11)$$

<sup>2</sup>An example of such a distortion can be found in Fig. 4.12 of Section 4.2.1.

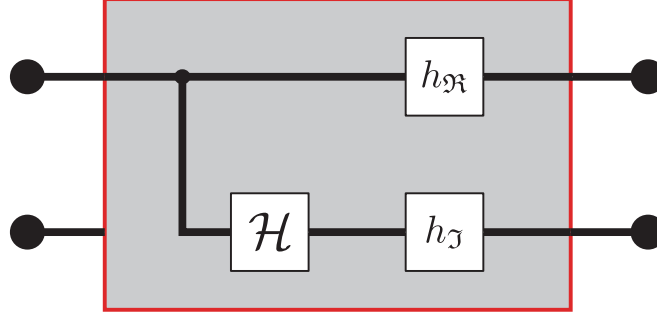


Figure 3.11 – Signal flow view of the 90° hybrid coupler as LTI system.

and

$$\hat{Y}_{\Im}(j\omega) = \mathcal{H}(j\omega) H_{\Im}(j\omega) Y(j\omega). \quad (3.12)$$

After sub-sampling using (3.1) results in the periodic spectra

$$\tilde{Y}_{\Re}(e^{j\omega}) = f_s \sum_{k=-\infty}^{\infty} \hat{Y}_{\Re}(j\omega f_s - j2\pi f_s k) \quad (3.13)$$

$$\tilde{Y}_{\Im}(e^{j\omega}) = f_s \sum_{k=-\infty}^{\infty} \hat{Y}_{\Im}(j\omega f_s - j2\pi f_s k) \quad (3.14)$$

defined for  $|\omega| \leq \pi$ . Assuming now that  $Y(j\omega)$  is a real passband version of a  $\frac{f_s}{2}$  band-limited baseband signal  $X(j\omega)$ , the spectrum of  $Y(j\omega)$  can be expressed by

$$Y(j\omega) = X(j(\omega - 2\pi k' f_s)) + \overline{X(-j(\omega + 2\pi k' f_s))}. \quad (3.15)$$

In this special case, the passband signal is centered at multiples of the sampling frequency  $f_s$  as also shown in Fig. 3.10a. Such an assumption simplifies the notation significantly and thereby facilitates the understanding, nevertheless, the proposed compensation scheme is not limited to this special case. The formulas (3.13) and (3.14) simplify to

$$\tilde{Y}_{\Re}(e^{j\omega}) = H_{\Re}(j(\omega + 2\pi k' f_s)) X(j\omega) + \overline{H_{\Re}(-j(\omega + 2\pi k' f_s)) X(-j\omega)} \quad \text{and} \quad (3.16)$$

$$\tilde{Y}_{\Im}(e^{j\omega}) = -j H_{\Im}(j(\omega + 2\pi k' f_s)) X(j\omega) + j \overline{H_{\Im}(-j(\omega + 2\pi k' f_s)) X(-j\omega)}, \quad (3.17)$$

which is defined for  $-\pi \leq \omega < \pi$ . By defining a pair of equivalent baseband filters as

$$K_{\Re}(e^{j\omega}) = H_{\Re}(j(\omega + 2\pi k' f_s)) \quad \text{and} \quad (3.18)$$

$$K_{\Im}(e^{j\omega}) = H_{\Im}(j(\omega + 2\pi k' f_s)), \quad (3.19)$$

for the passband transfer function  $H_{\Re}$  and  $H_{\Im}$  the equations (3.16) and (3.17) can be further simplified to

$$\tilde{Y}_{\Re}(e^{j\omega}) = K_{\Re}(e^{j\omega})X(j\omega) + \overline{K_{\Re}(e^{-j\omega})X(-j\omega)} \quad \text{and} \quad (3.20)$$

$$\tilde{Y}_{\Im}(e^{j\omega}) = -jK_{\Im}(e^{j\omega})X(j\omega) + \overline{jK_{\Im}(e^{-j\omega})X(-j\omega)}. \quad (3.21)$$

Considering the two sampled coupler outputs as real and imaginary parts of the desired analytic signal

$$\tilde{Y}(e^{j\omega}) = \tilde{Y}_{\Re}(e^{j\omega}) + j\tilde{Y}_{\Im}(e^{j\omega}) \quad (3.22)$$

$$= \left( K_{\Re}(e^{j\omega}) + K_{\Im}(e^{j\omega}) \right) X(j\omega) + \left( \overline{K_{\Re}(e^{-j\omega}) - K_{\Im}(e^{-j\omega})} \right) \overline{X(-j\omega)}, \quad (3.23)$$

leads to a residual negative frequency term  $X(-j\omega)$ .

In the case of a perfectly balanced coupler it holds that  $H_{\Re} = H_{\Im}$  and therefore also  $K_{\Re} = K_{\Im}$  so that

$$\tilde{Y}(e^{j\omega}) = \left( K_{\Re}(e^{j\omega}) + K_{\Re}(e^{j\omega}) \right) X(j\omega) + \left( \overline{K_{\Re}(e^{-j\omega}) - K_{\Re}(e^{-j\omega})} \right) \overline{X(-j\omega)} \quad (3.24)$$

$$= 2K_{\Re}(e^{j\omega})X(j\omega), \quad (3.25)$$

in which the negative frequency term  $X(-j\omega)$  cancels out and the received signal is a frequency-selective scaled version of  $X(j\omega)$ .

In the case of unbalanced coupler outputs with  $H_{\Re} \neq H_{\Im}$ , the  $X(-j\omega)$  component will not disappear. However, a dimension-wise equalization can make the negative frequency components cancel each other. An obvious choice for the equalization filters would be the inverted and frequency-reversed transfer functions of the coupler branches  $\overline{K_{\Re}^{-1}(e^{-j\omega})}$  and  $\overline{K_{\Im}^{-1}(e^{-j\omega})}$ . This filter choice ensures that the negative frequency components cancel each other, because

$$\tilde{Y}(e^{j\omega}) = \overline{K_{\Re}^{-1}(e^{-j\omega})} \tilde{Y}_{\Re}(e^{j\omega}) + \overline{K_{\Im}^{-1}(e^{-j\omega})} \tilde{Y}_{\Im}(e^{j\omega}) \quad (3.26)$$

$$= \left( \overline{K_{\Re}^{-1}(e^{-j\omega})} K_{\Re}(e^{j\omega}) + \overline{K_{\Im}^{-1}(e^{-j\omega})} K_{\Im}(e^{j\omega}) \right) X(j\omega) \quad (3.27)$$

$$+ \left( \overline{K_{\Re}^{-1}(e^{-j\omega})} K_{\Re}(e^{-j\omega}) - \overline{K_{\Im}^{-1}(e^{-j\omega})} K_{\Im}(e^{-j\omega}) \right) X(-j\omega) \quad (3.28)$$

$$= \left( \overline{K_{\Re}^{-1}(e^{-j\omega})} K_{\Re}(e^{j\omega}) + \overline{K_{\Im}^{-1}(e^{-j\omega})} K_{\Im}(e^{j\omega}) \right) X(j\omega). \quad (3.29)$$

Despite the unbalanced coupler transfer functions, only the positive frequency components remain. Nevertheless, except for the unlikely special case that both transfer functions are perfectly symmetric, such a compensation introduces new frequency selectivity on the desired signal. Frequency selectivity introduced in the receiver chain needs to be considered separately. Unlike the frequency selectivity of a channel, frequency selectivity introduced by the coupler and its compensation influences the noise statistic of the received signal. This noise coloring can be avoided by using the fact that the negative frequency components do not need to be equalized in the strict sense. For compensation to work, the two outputs just need to be filtered

in such a way that the negative frequency components of real and imaginary part match. A flat frequency spectrum of the two signals is not crucial. Hence, a white noise statistic in the compensated signal can be attained by using a normalized compensation filter pair

$$E_{\Re}(e^{-j\omega}) = \frac{1}{\left( \overline{K_{\Re}^{-1}(e^{-j\omega})K_{\Re}(e^{j\omega})} + \overline{K_{\Im}^{-1}(e^{-j\omega})K_{\Im}(e^{j\omega})} \right)} \overline{K_{\Re}^{-1}(e^{-j\omega})} \quad \text{and} \quad (3.30)$$

$$E_{\Im}(e^{-j\omega}) = \frac{1}{\left( \overline{K_{\Re}^{-1}(e^{-j\omega})K_{\Re}(e^{j\omega})} + \overline{K_{\Im}^{-1}(e^{-j\omega})K_{\Im}(e^{j\omega})} \right)} \overline{K_{\Im}^{-1}(e^{-j\omega})}. \quad (3.31)$$

Using these filters will result in a compensated signal

$$\tilde{Y}(e^{j\omega}) = E_{\Re}(e^{-j\omega}) \tilde{Y}_{\Re}(e^{j\omega}) + j E_{\Im}(e^{-j\omega}) \tilde{Y}_{\Im}(e^{j\omega}), \quad (3.32)$$

$$= X(j\omega), \quad (3.33)$$

which does not exhibit any additional frequency selectivity for the positive frequency components.

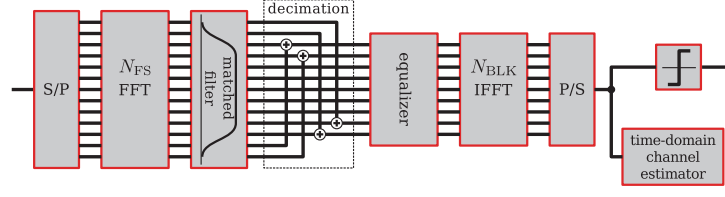
### 3.3 DSP for Complex Sub-Sampling

It has been shown that complex sub-sampling offers significant advantages at the cost of only little additional complexity. Nevertheless, for the usefulness in practical mmWave receiver also the digital signal processing overhead to perform the imbalance compensation needs to be considered. In the most simple architecture, the coupler impairment compensation is implemented with a pair of linear time-domain FIR filters directly after the ADCs. From a system perspective, the two compensated sequences are merged to complex samples which appear as if they were produced by an ideal complex sub-sampling setup with some additional delay. With such dedicated compensation filters, the baseband processing is completely decoupled from the front-end architecture.

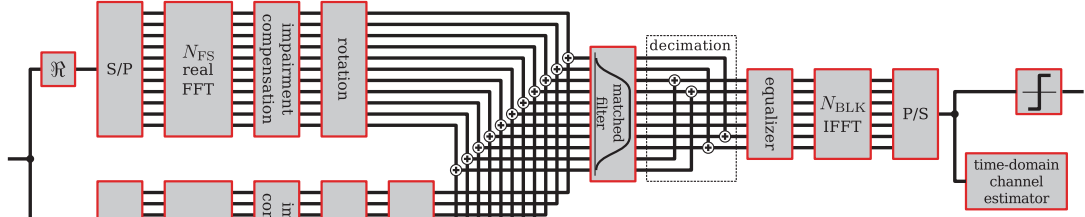
However, dedicated time-domain filters do not come for free. The spectrum of the compensation filter is not Hermitian and therefore the coefficients of each of the two filters as well as the compensated signal are complex. The exact length of the required FIR filter depends on the level of coupler imbalance but can easily span dozens of filter taps. Adding two complex-valued digital FIR filters significantly impacts the over-all complexity of a mmWave receiver. The increase in complexity renders an architecture based on dedicated compensation filters only interesting for special purpose receivers, which are not constrained by power budgets.

Fortunately, the typical block-based SC-FDE receiver architecture described in Section 2.3 can be extended with very little overhead to also incorporate coupler impairment compensation. The baseline DSP architecture for an SC-FDE receiver is shown in Fig. 3.12a. The one-dimensional equalization of the two coupler branches can be achieved by splitting the

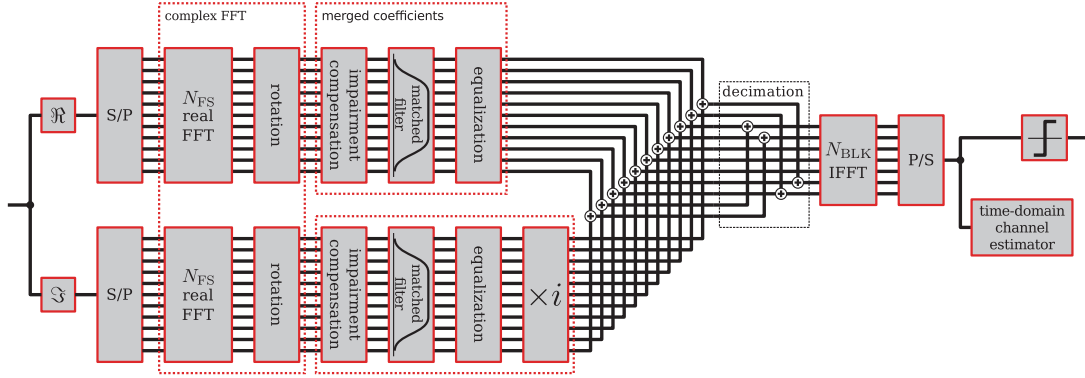




(a) baseline architecture (see Section 2.3)



(b) including coupler impairment compensation



(c) optimized impairment compensation architecture

Figure 3.12 – DSP architectures for block-based SC-FDE receiver

complex-valued FFT into two real-valued<sup>3</sup> FFTs (cf. Fig. 3.12b). After both branches are independently converted to frequency-domain, compensation can be applied using (3.30) and (3.31). The FFT bins of the compensated signal can now be reordered to perform a rotation of the signal in frequency. The compensated frequency-domain signals are merged and processed analog to the baseline DSP architecture.

At first glance such a compensation scheme entails the overhead of an additional FFT and  $2N_{\text{FS}}$  additional complex multiplications. A closer examination reveals that the impairment compensation comes with significantly less overhead, because the complexity of a real-valued DFT is significantly lower than that of a complex-valued DFT. In fact the two DFTs of the real vector  $\mathbf{x}, \mathbf{y} \in \mathbb{R}$  of size  $N$

$$\mathbf{X} = \mathcal{F}_N \mathbf{x} \quad \text{and} \quad (3.34)$$

$$\mathbf{Y} = \mathcal{F}_N \mathbf{y} \quad (3.35)$$

can be reconstructed from  $\mathbf{C} = \mathcal{F}_N (\mathbf{x} + j\mathbf{y})$  as

$$X_k = \frac{1}{2} (C_k + \overline{C_{N-k}}) \quad \text{and} \quad (3.36)$$

$$Y_k = \frac{1}{2j} (C_k - \overline{C_{N-k}}), \quad (3.37)$$

for  $k = 0, 1, \dots, N-1$ . Essentially a single complex-valued FFT can be used to calculate two real-valued FFTs [106]. The calculation of (3.36) and (3.37) can be conveniently used to reorder the bins and thereby perform any necessary frequency rotation without additional overhead.

Using the distributive property of the applied operations, the matched filter and the channel equalization can be moved before the decimation. Now, impairment compensation, matched filtering and, channel equalization can be merged into a single combined set of coefficients. This set of coefficients needs to be calculated only once at the beginning of the frame after the channel estimation. Considering the large number of blocks in a typical mmWave frame, the complexity of the initial coefficient calculation becomes negligible. Hence, the optimized architecture in Fig. 3.12c requires only a single additional set of complex multiplications per block for integration of the impairment compensation.

Using the system parameters of the IEEE 802.11ad SC-FDE receiver architecture discussed in Section 2.1.3 as baseline, the necessary overhead can be quantified. For the comparison of the different architectures the number of required complex multiplications per data symbol (CMPS) is used as a complexity metric<sup>4</sup>. For the calculation a frame block size of  $N_{\text{BLK}} = 512$  and an oversampling factor  $R^{\text{OS}} = 1.125$  is assumed. Table 3.1 provides a comparison of the required CMPS of the receiver with and without compensation. The baseline architecture as shown in Fig. 3.12a is used as a reference for normalization. To provide a fair comparison,

<sup>3</sup>In this context real-valued and complex-valued refers to the input signal of the FFT, which is somewhat imprecise as the operations in the FFT and its output signal are in most cases still complex.

<sup>4</sup>The number of required complex multiplications is a common complexity metric for FFTs.

### 3.4. Noise Characterization in Sub-Sampling Receiver

Table 3.1 – Number of required complex multiplications per data symbol (CMPS).

| baseline |      | baseline opt |       | compensation |        | compensation opt |        |
|----------|------|--------------|-------|--------------|--------|------------------|--------|
| #CMPS    | %    | #CMPS        | %     | #CMPS        | %      | #CMPS            | %      |
| 17.7     | 100% | 16.6         | 93.6% | 27.2         | 153.3% | 17.9             | 100.8% |

an optimized version of the baseline architecture is added to the comparison lineup. In the optimized architecture the matched filter is merged with the channel equalizer. Additionally the complexity metrics of the unoptimized compensation architecture in Fig. 3.12b and the optimized architecture in Fig. 3.12c are provided. Comparing the two optimized architectures shows that coupler impairment compensation requires only 7% more complex multiplications per data symbol, if existing system resources are reused. Additionally this 7% increase is only relative to the complexity of the frequency-domain equalization, considering the overall receiver complexity the overhead becomes even less significant.

### 3.4 Noise Characterization in Sub-Sampling Receiver

Until now we have only considered the correct reconstruction of the signal in the complex sub-sampling receiver. However, the impact of the complex sub-sampling receiver on the noise is similarly important for a successful data transmission.

Thermal noise is in general considered to have a constant noise spectrum over the frequency range interesting for communication purposes [109]. As a result the thermal noise can be modeled as a white noise source that depends on the sampling bandwidth only. Due to the proposed normalization of the compensation coefficients (see (3.30)) the thermal noise is not affected by the complex sub-sampling architecture.

Another source of noise affected by the receiver architecture is sampling jitter introduced by phase noise on the sampling clock. In time-domain, sampling jitter leads to samples being taken at time instances with a slight offset. Consequently the sampling error is proportional to the rate of change of the sampled signal during the time offset. By looking at the two sinusoids with different frequencies in Fig. 3.13, it becomes intuitive that the rate of change is related to the frequency components of a signal. Signals with higher frequency components will be more affected by sampling jitter compared to signals with lower frequency components. Hence IF sampling and especially the proposed sub-sampling receiver will suffer more from sampling jitter compared to receivers that sample a baseband signal [110].

In the literature [111][112] the limiting effect of sampling jitter on the SINR is reported as

$$\text{SINR}_{\text{jitter}} = -20 \log_{10}(2\pi f \tau), \quad (3.38)$$

for a signal with frequency  $f$  and an root mean-square (RMS) sampling jitter  $\tau$ . Applying

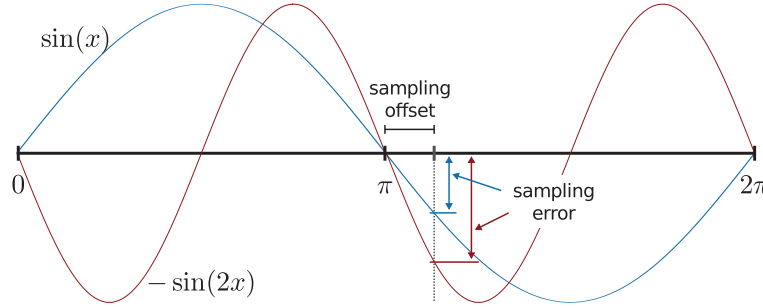


Figure 3.13 – Impact of sampling jitter on the sampling error of sines with different frequencies.

this to all frequency component of the signal we can conclude that a doubling the carrier frequency of the IF-Signal reduces the  $\text{SINR}_{\text{jitter}}$  by 6 dB. In return this means that the local oscillator would need to exhibit half the effective jitter in order to deliver the same  $\text{SINR}_{\text{jitter}}$  performance.

More subtle is the relation between complex sub-sampling and the quantization noise of the ADCs. The complex sub-sampling itself might be advantageous for the dynamic range of the receiver as the split into two branches with 3 dB less power and potentially uncorrelated quantization noise. In practice this advantage can be outweighed by the loss of dynamic range due to need for compensation of non-flat frequency responses of the analog components. While the normalization proposed in (3.30) and (3.31) ensures a white noise statistic of any incident thermal noise it does not guarantee a constant spectrum of the quantization noise. Because the quantization noise is introduced between the coupler and the coupler compensation, the proposed impairment compensation will color the quantization noise. As a result the dynamic range requirements for the ADCs increase. The amount of additional required dynamic range is directly related to the mismatch between the two branches.

For completeness, flicker noise is occasionally mentioned as a noise source affected by the receiver architecture. Flicker noise, represents thermal noise components whose spectrum decays with  $\frac{1}{f}$  [113]. In general, complex sub-sampling is similar to real sub-sampling inherently less affected by flicker noise because of the filtered low frequency components. In the pass-band of the IF signal, the flicker noise has already dropped well below the level of the thermal noise. Although flicker noise can be a significant at very low frequencies, the overall impact for mmWave systems is due to the large bandwidth negligible. For narrowband applications of complex sub-sampling the lack of flicker noise can bring a noticeable difference.

### 3.5 Single Oscillator Receiver

It is a common optimization method for heterodyne receivers to place the IF in such a way that the second local oscillator clock can be derived from the first local oscillator. Such an

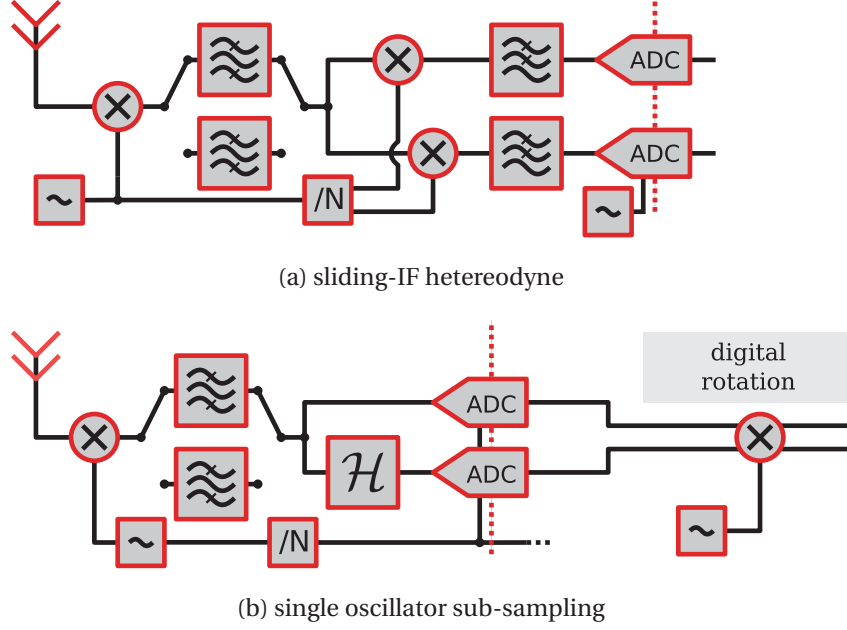


Figure 3.14 – Evolution from low-power sliding-IF receiver to true single oscillator architecture.

architecture is called sliding-IF [101] receiver and shown in Fig. 3.14a. Sliding-IF receiver allow to replace a second local oscillator with a simple divider, leading to

$$f_{\text{IF}} = \frac{f_{\text{RF}} - f_{\text{IF}}}{N}. \quad (3.39)$$

This can be rewritten to the following relation

$$f_{\text{IF}} = \frac{f_{\text{RF}}}{N + 1} \quad (3.40)$$

between IF and RF IN such an architecture  $f_{\text{IF}}$  becomes a function of  $f_{\text{RF}}$  which means that the IF changes with the selected channel, lending the name sliding-IF to this architecture. Sliding-IF architecture have been proposed [114][115] in mmWave receiver for complexity and power reduction.

However, even with a sliding-IF receiver at least one additional oscillator is required for generation of the sampling frequency and and the digital baseband clock. The flexibility of the complex sub-sampling receiver to arbitrarily place the IF allows to overcome this limitation and implement a true single oscillator design. It is evident that IF sub-sampling architectures in general do not require a second local oscillator. Using complex sub-sampling,  $f_{\text{IF}}$  can now be chosen such that the first local oscillator clock  $f_{\text{RF-IF}}$  is a multiple of the sampling clock  $f_s$ . Consequently it holds that

$$f_{\text{RF}} - f_{\text{IF}} = M \cdot f_s. \quad (3.41)$$

This allows to derive the clocks for the ADCs and the digital baseband from the first local oscillator by division.

In a typical wireless receiver design  $f_s$  would be fix and  $f_{RF}$  would depend on the used channel, so that the IF changes with the selected channel. Similar as in a traditional sliding-IF architecture, the IF filter needs to be either sufficiently wideband or reconfigurable. It should also be noted that the coefficients of the coupler compensation need to be adjusted to the used IF frequency. Nevertheless especially for mmWave systems this does not entail much overhead, because of the low number of channels. Using the local oscillator to derive the sampling clock has the additional benefit that phase noise and sampling jitter become correlated. This allows baseband architecture to compensate sampling jitter based on phase noise estimates.

### 3.6 Summary

The proposed complex sub-sampling architecture is a promising candidate for low-power wireless receiver designs with very wide bandwidths. Complex sub-sampling combines the complexity advantages of sub-sampling with the flexibility and system efficiency of conventional down-conversion. The strength of complex sub-sampling results from the large flexibility for placing the IF and thereby removing the biggest obstacle of conventional real sub-sampling receivers. Complex sub-sampling achieves its advantages at the cost of only a single passive component and therefore still offers a very low complexity analog front-end. Further it was shown that no specifically precise components are required as an impairment compensation can be performed in digital domain. The compensation can be integrated into the existing baseband equalization with a complexity overhead of less then 10 %. The achieved frequency agility does not only facilitate the receiver design, it also enables completely new receiver architectures supporting multi-channel/-band operation with only a single oscillator for the analog and digital domain. Such an architecture promises to offer significantly reduced power consumption for mmWave receivers. An implementation of a complex sub-sampling receiver for 60 GHz is shown in Chapter 4.

## 4 Testbed for High-Rate mmWave Communication

Today the exploration of new wireless technologies is mostly based on numerical simulation. These numerical simulations are based on models which require the confidence that they represent the hardware correctly. There is a significant risk that research solely based on simulations transforms to a self-fulfilling prophecy in which the models are adjusted to the proposed solution in order to justify results. Obviously such bias nullifies any value of the research as means of acquiring insight and will not lead to solutions that help solve real-world engineering challenges.

Hardware testbeds therefore play a crucial role in the development of wireless systems. Testbeds are not only useful for the characterization of parameters which are a prerequisite to meaningful simulation models, they also provide insight in the dominant limitations of a system. Finally only testbed transmission can provide confidence in the end-to-end effectiveness of proposed baseband algorithms.

A high-rate 60 GHz hardware testbed for research on next-generation cellular backhaul networks is presented. Such backhaul links are characterized by a large bandwidth significantly above 1 GHz and a high spectral efficiency. The low rank of the backhaul channels[26] suggests that MIMO will not be effective in such a scenario and high spectral efficiency can only be achieved with the use of high modulation orders. Hence, the testbed is focused on high linearity with a receiver EVM of down to -30 dB with a bandwidth beyond 1.5 GHz.

In this chapter, the setup of the testbed and the characteristics of the different components are described. A link budget analysis is performed to identify the correct operation regimes for the link components. Afterwards the effect of receive chain non-idealities on the signal is investigated. First, the impact of the non-ideal coupler on the suppression of the negative frequency components is analyzed. A calibration scheme is described which allows to determine the necessary filter responses for the digital impairment compensation. Subsequently the influence of compression and frequency selectivity on the signal is discussed. At the end general measurement considerations are given and the achievable receiver performance is demonstrated.

### 4.1 Architecture

The testbed adopts a *hardware in the loop (HIL)/simulation* co-design approach. An overview of the testbed architecture is shown in Fig. 4.1. The testbed is built around a central host which runs the signal processing framework based on MATLAB and connects to the different parts of the hardware link. The framework implements the baseband signal processing of the transmitter and receiver as well as software interfaces to integrate the testbed hardware in the signal flow. It also provides a set of numerical models for hardware impairment and channel conditions. The modular structure allows to seamlessly switch between numerical models and real hardware and thereby provides a simple way to debug the setup and verify existing simulation models against the real-world transmission setup.

The framework also allows the combination of numerical impairment models and hardware effects, which is interesting for all effects where a single hardware setup can not appropriately model the spread between devices. A good example for such an effect is the carrier frequency offset resulting from device-variations of the reference frequency oscillator. This effect can not be properly modeled in the hardware testbed which only has a fixed pair of reference oscillators. Fortunately a frequency offset can be artificially introduced in MATLAB on the transmitter side to mimic such an effect.

The different hardware components of TX and RX are controlled directly from the MATLAB-based framework. The hardware-specific connectors [116] provide an interface to the testbed hardware in MATLAB such that measurements can be performed fully automated. The different components of the testbed are connected with Ethernet-based IP links to the central host.

Implementation of the 60 GHz transmitter and receiver are based on commercial off-the-shelf (COTS) components. The use of COTS components accelerates not only the overall development process, it also enables an end-to-end driven development cycle, where initial results can be obtained very quickly. The following improvement steps of the setup are applied iteratively to an already working link, which allows the immediate observation of the effect on the final output. The practical challenge of the testbed setup is to operate all components in a regime that maximizes the signal quality by balancing the different noise and interference sources. Another challenge arises from the fact that with system bandwidths beyond GHz the components can not be considered frequency-flat anymore.

#### 4.1.1 60 GHz RF Frontends

The mmWave link is built around a pair of integrated Sivers IMA FC1005V00 [117] V-band converter boards. The boards feature mixers for the up- and down-conversion from an intermediate frequency (IF) to the target 60 GHz band and amplifiers for the RF and IF signal. Each FC1005V00 contains independent converter circuits for transmitter and receiver with dedicated local oscillators and a common reference oscillator. Nevertheless in the testbed,



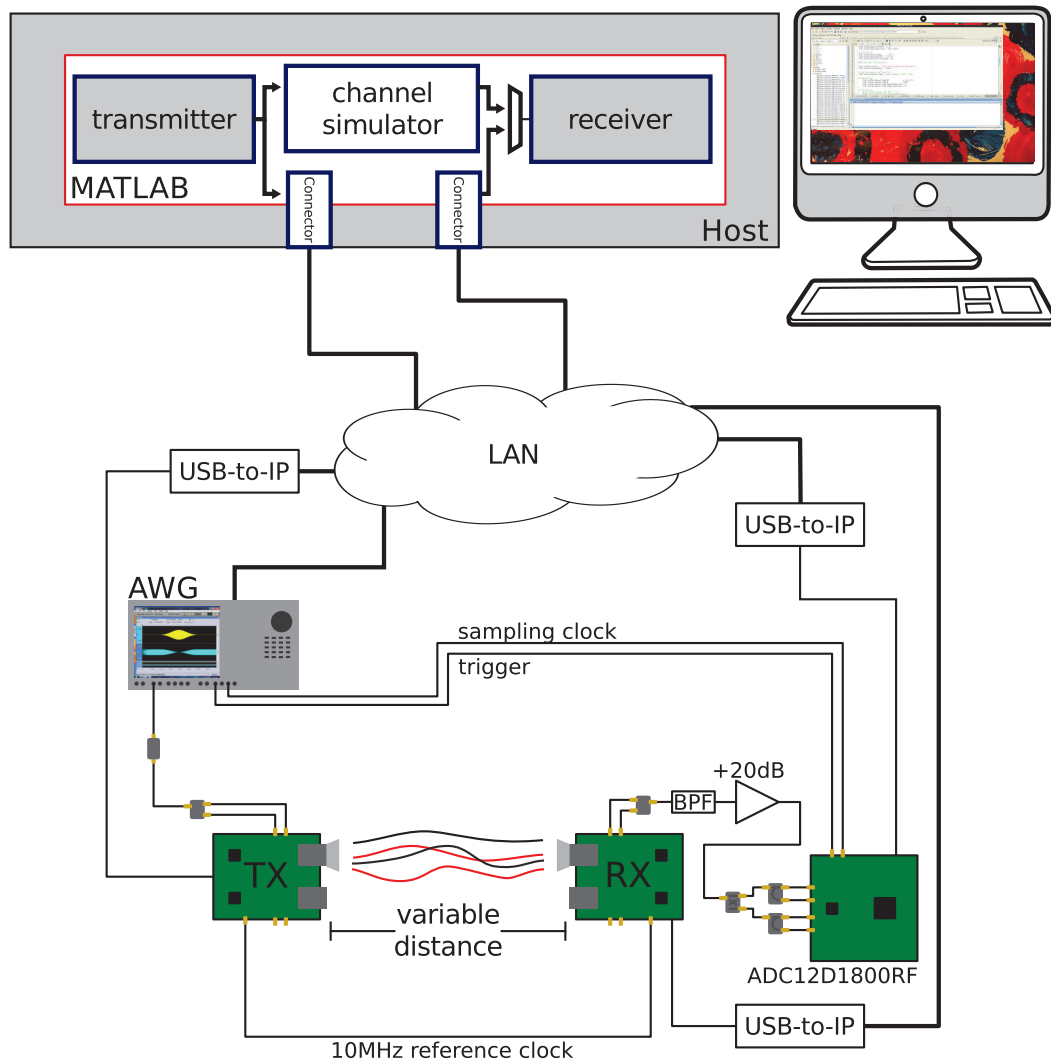


Figure 4.1 – Overview of the 60 GHz demonstration testbed architecture.

transmit and receive converter of two separate FC1005V00 converter boards with independent power supplies are used to provide a higher flexibility for placement of the nodes and reduce correlation between noise sources.

The FC1005V00 implements a low-IF architecture, in which the supported IF frequency range of 1-5 GHz is low compared to the supported RF bandwidth ranging 58-66 GHz. As a result with such a frequency plan the RF image frequency of the mixer falls in or nearby the RF band. Without any provisions such an architecture would need steep pre-selection filters at RF to avoid aliasing of the image frequency. Instead an image-rejection mixer architecture [101] with an external coupler on the IF side is used to achieve sufficient RF image suppression. The converter board feature double SMA connectors for the IF connection to the coupler, while the 60 GHz signal is provided over a WR-15 waveguide interface. The clock modules of the TX and RX converters are connected with a coaxial cable which allows on demand synchronization of the reference oscillator in order to remove frequency offsets.

A USB interface allows control of the oscillators and the power settings of the converter board. Because of the limited flexibility of USB connections a Raspberry Pi [118] is used as a USB-to-IP gateway. The gateway allows access to the converter boards from MATLAB with a simple transmission control protocol (TCP) connection.

### Transmitter

The transmitter is implemented using a Tektronix AWG7122C [119] arbitrary waveform generator (AWG). This AWG supports a vector length of 32 MS with a precision of up to 10 bit and is programmed directly from MATLAB. With a sampling rate of up to 12 Gsps the AWG directly synthesizes the digitally up-converted TX IF signal. Digital synthesis with over-sampling provides the most flexible way to create a high quality IF signal. In particular, the AWG allows to place the IF signal with arbitrary pulse shape in the whole IF range. A high signal quality is ensured by the lack of transmit IQ imbalance or IF oscillator phase-noise. To match the setup on the RX side, the IF signal is synthesized around a center frequency  $f_{IFc}^{TX} = 1.8 \text{ GHz}$  with a sampling rate of 10.8 GHz. While the precise sampling rate is not critical for the actual IF signal, choosing 10.8 GHz facilitates the generation of a 1.8 GHz sampling clock for the RX ADC. An integer over-sampling factor allows to use the digital marker outputs of the AWG to generate a square clock signal that is phase-aligned to the TX IF signal. A sampling rate of 10.8 GHz allows to generate sequences of up to 3 ms duration with 32 MS.

The AWG has only very little built-in suppression of the high frequency components due to artifacts from the installed wideband option. An external bandpass filter suppresses these high frequency components and low-frequency out of band spurs. The filtered signal is attenuated by 16 dB to ensure the correct input power level for the FC1005V boards. The transmitter IF spectrum for a single carrier signal with 1.6 GS/s and a root-raised cosine pulse shape with 0.125 roll-off factor, is shown in Fig. 4.2.

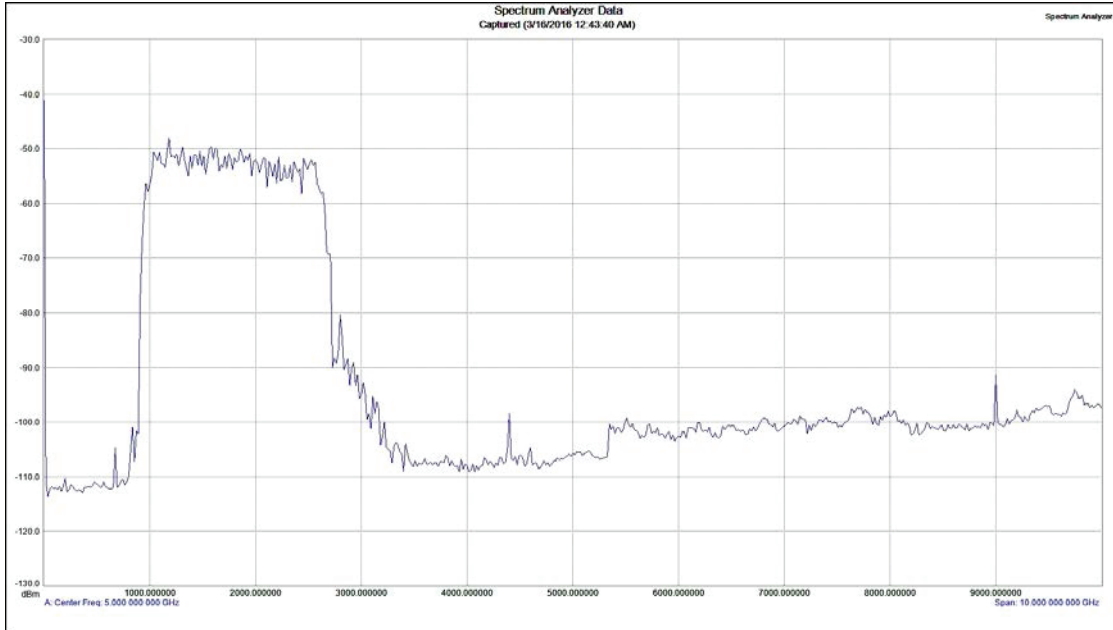


Figure 4.2 – TX output spectrum of a 1.6 GS/s signal using the 7122C with a sample rate of 10.8 GSPS.

The output power of the FC1005V boards can be adjusted by the transmit power setting (TXPS) using the control interface of the converter boards. The TXPS controls the bias voltage of the PA and can take values from 0x00 to 0xFF covering approximately 20 dB of variable gain range.

The AWG also generates a 1.8 GHz clock signal using the digital marker output. The clock signal is used as offset and phase-noise free sampling clock for the receiver. A second digital marker output provides a trigger signal to start sampling on the ADC board.

### Receiver

The IF to baseband conversion in the receiver is performed using a complex sub-sampling architecture as presented in Chapter 3. The RX IF signal centered at 1.8 GHz is initially amplified with a Minicircuits ZX60-V63+ and filtering with a Minicircuits BHP-1000+ band-pass filter (BPF). The filtered signal is converted to an analytic signal using a MECA 705S-3.000 90° hybrid coupler [120] with a nominal frequency range of 2-4 GHz. The used coupler is at the time of writing the one with the widest specified bandwidth which is commercially available. Unfortunately its nominal frequency does not match fully our targeted IF signal range and even for the nominal frequency matching of the output ports is only given within a  $\pm 0.4$  dB band for the magnitude and  $90 \pm 2^\circ$  for the phase.

The real and imaginary output signals of the coupler are conditioned for the ADCs with two TI ADC-LD-BB [121] balun boards. The balun boards with a nominal operating frequency range of 0.4-3 GHz transform the single-ended 50  $\Omega$  signals in differential signal with 100  $\Omega$

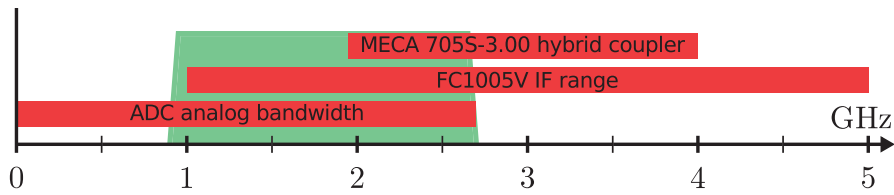


Figure 4.3 – Placement of the IF signal (green) relative to the optimal operating ranges of ADC, converter boards, and hybrid coupler of the testbed.

impedance.

The ADCs are operated in AC-coupled mode therefore direct-current-blocks are required for correct operation. Consequently all four inputs of the ADCs are equipped with Minicircuits BLK-98-S+ [122] broadband direct-current-blocks. The two branches are sub-sampled using a Texas Instruments ADC12D1800RF dual-ADC [123] with 12 bit resolution. The ADC offers a sampling rate of 1.8 Gsps on both channels or an interleaved mode with 3.6 Gsps on a single channel. This particular ADC is optimized for sub-sampling and its analog bandwidth, defined by the 3 dB attenuation point, extends significantly beyond the first Nyquist zone up to 2.7 GHz. The ADC chip is mounted on a Texas Instruments ADC12D1800RFRB reference board, that features an FPGA to sample the ADC output and a USB 2.0 interface. The USB interface allows the download of sampled sequences of up to 32768 samples length, which gives a window of  $18.2 \mu\text{s}$  at 1.8 GHz sampling rate.

The analog bandwidth limitation of the ADC and the IF range of the 60 GHz converter boards dictate the frequency planning (cf. Fig. 4.3) of the receiver. Because of the steep low-pass characteristic of the ADCs the IF signal needs to be placed below its 2.7 GHz corner frequency. The lower IF signal limitation is given by the 1-5 GHz range of the IF circuit in the converter boards. Hence the RX IF signal is centered around 1.8 GHz, such that for the maximum sampling rate of 1.8 GHz it extends from 0.9 GHz to 2.7 GHz. With this configuration the IF signal extends slightly below the specified IF frequency range of the Sivers converter boards. Experiments have shown that operating the mmWave converter boards slightly out of the specification is less critical compared to exceeding the analog bandwidth of the ADCs.

### 4.1.2 Link Budget Analysis

For the link budget calculation the effect of all processing gains and losses on the signal and noise are added to get an SNR estimate. The link budget calculation is not precise as it is mostly based on the datasheet specifications of the different components. It further neglects the loss in cabling and connectors and mild frequency selectivity of the components. Nevertheless, a link budget calculation can provide an initial estimate of the feasibility of a receiver design for a certain scenario. Often the link budget is used to determine the maximal achievable operating distance of the link. As the required antenna technique (see Section 2.1.1) is not our

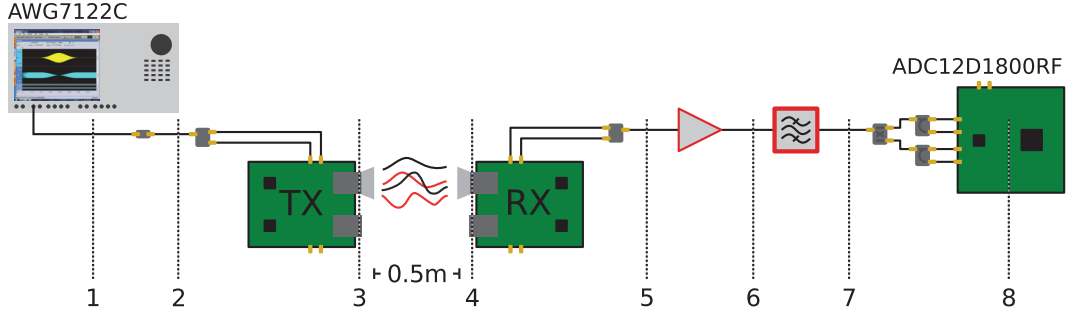


Figure 4.4 – Probing points for the link budget analysis of the 60 GHz testbed.

| Stage                        | 1   | 2   | 3      | 4     | 5     | 6     | 7     | 8     |
|------------------------------|-----|-----|--------|-------|-------|-------|-------|-------|
| Gain [dB]                    | 0   | -20 | 30     | -42   | 15    | 20    | -0.5  | 0     |
| Signal level [dBm]           | -4  | -24 | 6      | -36   | -21   | -1    | -1.5  | -1.5  |
| TX quantization noise [dBm]  | -47 | -67 | -37    | -79   | -64   | -44   | -44.5 | -46.5 |
| TX thermal noise level [dBm] |     |     | -32    | -74   | -59   | -39   | -39.5 | -39.5 |
| RX thermal noise level [dBm] |     |     |        |       | -56   | -36   | -36.5 | -36.5 |
| RX IF amp noise [dBm]        |     |     |        |       |       | -77.2 | -77.7 | -77.7 |
| RX quantization noise [dBm]  |     |     |        |       |       |       |       | -50   |
| Total noise [dBm]            | -47 | -67 | -30.81 | -72.8 | -53.8 | -33.8 | -34.3 | -34.2 |
| SNR [dB]                     | 43  | 43  | 36.8   | 36.8  | 32.8  | 32.8  | 32.8  | 32.7  |

Table 4.1 – Link budget calculations for the 60 GHz testbeds showing a final achievable SNR of 36 dB, column numbers correspond to the different measurement points shown in Fig. 4.4.

main focus, we will set an arbitrary operating distance of 0.5 m and assume that for the final application antennas with sufficient gain are available. In the context of the testbed the link budget serves mainly to ensure that all components in the transmission chain are used within their optimal operating range limits.

The thermal noise floor of the system is assumed to be white with an available thermal noise power per Hertz of  $kT = -174\text{dBm/Hz}$  at  $T = 300\text{K}(26.84^\circ\text{C})$ [109]. For the 1.8 GHz bandwidth of interest this gives an absolute thermal noise power level of -81 dBm. This is the unalterable lower limit, the minimal distance of the signal power level to the thermal noise floor at any point in the link determines the upper-limit for the achievable SNR of the system.

The maximum output power of the AWG in single-ended configuration is given by the output amplitude of  $0.5 V_{pp}$  over  $50\Omega$  as  $P_{\max} = \frac{(0.25V)^2}{50\Omega} = 1.3\text{mW} \approx 1\text{dBm}$ . To account for the PAPR of the intended high-order single-carrier modulation we assume a necessary back-off of 5 dB resulting in -4 dBm output signal power. For the estimation of the quantization noise we can apply a common rule of thumb [106] of 6 dB of dynamic range per bit resolution. Hence, the 8 bit sample resolution provides approximately 48 dB of dynamic range and results in a quantization noise level of -47 dBm.

## Chapter 4. Testbed for High-Rate mmWave Communication

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The AWG is equipped with a wideband analog front-end option, which significantly reduces the available output power settings. Hence, an additional 20 dB attenuator, assembled from Minicircuits VAT components, is used to match the signal power level to the operating range of the Sivers IMA converter boards.

Adjusting the incident IF-signal is crucial for maintaining signal-integrity of the transmit chain in the FC1005V00 board. Overdriving the initial transmitter IF amplifier introduces significant non-linear components independent of the power setting, which limits the transmit EVM. An adjustable output amplifier delivers a gain between 20-38 dB. The output noise density of the transmitter module is specified as -120 dBm/MHz resulting in an additional -32 dBm noise for the used bandwidth. Output PA saturation is reached at 15 dBm. A 9 dB PA backoff is assumed to avoid significant PA compression.

Directional 10 dBi horn antennas are mounted on the waveguide interfaces of the mmWave converter boards on both sides. A transmission distance of 0.45 m between transmitter and receiver results in a free-space path-loss (see Section 2.1.1) of 62 dB assuming unit-gain antennas. Including the directional gain of the antennas the transmitted signal is attenuated by 42 dB at the waveguide input of the receive converter board.

The receive converter board is specified with a noise figure (NF) of 10 dB and a fixed RF-to-IF gain with a very wide spread of 8-20 dB. This results in a RX thermal noise power level between -54 dBm and -66 dBm at the IF output.

The IF signal is amplified by a Minicircuits ZX60-V63+ amplifier with a gain of 19-21 dB and a NF of 3.8 dB in the frequency band of interest. The amplifier is characterized by a good gain flatness over the required frequency range and a high 1 dB-compression point. After amplification the signal is filtered by a Minicircuits BHP-1000+ bandpass filter with a 0.5 dB in-band insertion loss.

The filtered IF signal is transformed to a complex signal using a MECA 705S-3.000 90° hybrid coupler and sampled by the TI ADC12D1800RF dual ADC. The ADC has a nominal resolution of 12 bit with an effective number of bits (ENOB) of 9.3 bits for a voltage input of  $0.8 V_{pp}$  over  $50 \Omega$ . This results in a maximal acceptable peak input power of 5 dBm and with again 5 dB of backoff an maximal average input power of 0 dBm and a receive quantization noise level of -50 dBm.

The different signal and noise power levels can be calculated after every component of the testbed in order to track which component limits the achievable SNR. In Tbl. 4.1 we observe that for these gain settings an SNR of approximately 35 dB can be achieved. In general, the link budget calculation shows the high output noise level of the transmit converter board at -32 dBm is limiting the performance. Considering an output saturation level of 15 dBm the transmitter can under no circumstances achieve a transmit EVM below -47 dB. In practice the achievable EVM is even lower due to compression by the transmit PA and due to the PAPR of the transmitted signal which requires a back-off of 10 dB or more. The link budget is largely

independent from the used complex sub-sampling architecture and provides an upper limit for the achievable performance.

## **4.2 Testbed Characterization**

Based on the link budget a hardware demonstrator is assembled and characterized. Hardware impairments which are not included in the link budget can be analyzed and their impact on the signal quality can be assessed. The main effects not covered by the link budget are:

- Coupler Impairment
- Compression
- Frequency Selectivity

The achievable operating range of the complex sub-sampling scheme is the main concern that needs to be verified on the testbed. The precision of the proposed coupler impairment compensation and the resulting residual interference can limit the signal quality and thereby reduce the upper limit on the operable SNR range below the limit calculated in the link budget. Also the compression of various amplifiers in the transmission chain is not captured in the link budget. Therefore, the influence of compression needs to be measured on the actual hardware in order to ensure that non-linear products do not become the dominant noise source in the system. Finally the frequency selectivity of the different components of the receiver chain influences the required dynamic range of the ADC.

### **4.2.1 Coupler Compensation Calibration**

The parameters required to compensate the frequency selectivity of the 90° hybrid coupler are found in a two step process. First, a characterization of the frequency response of the coupler is performed outside of the testbed. This characterization can be used to determine an initial set of compensation parameters. In a second step, a fine calibration is performed on the assembled complex sub-sampling part.

#### **Coarse Compensation**

The frequency response of the coupler can be characterized with a vector network analyzer. The network analyzer provides a set of S-parameters for all possible input-output combinations of the device under test (DUT). The parameter  $S_{yx}$  corresponds to the positive part of the transfer function from input  $x$  to output  $y$ .<sup>1</sup> The parameter  $S_{21}$  describes the transfer function for the real branch, while  $S_{31}$  describes the transfer function of the imaginary 90° shifted

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<sup>1</sup> Because of the real nature of the input and the output signal, the positive frequency range fully characterizes the complete transfer function.

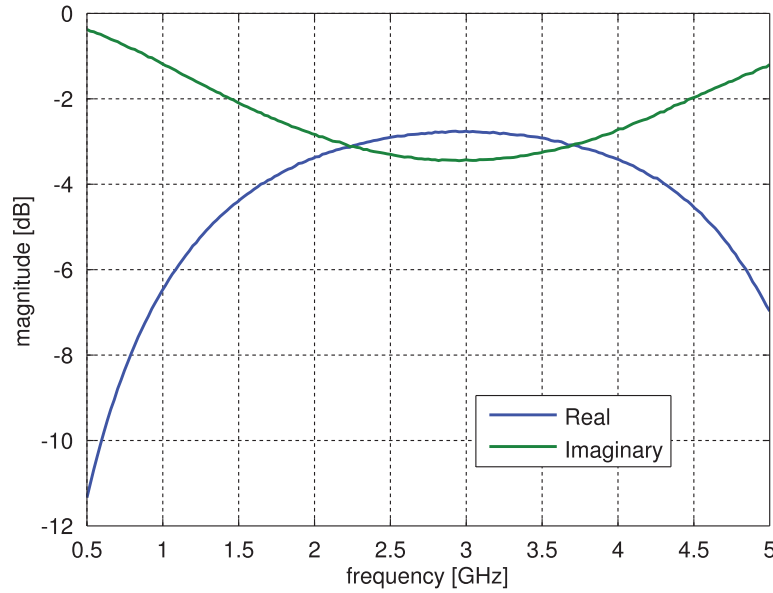


Figure 4.5 – Transfer function of the real and the imaginary branch of the MECA 705S-3.000 90° hybrid coupler used in the complex sub-sampling receiver.

branch. The measured magnitudes of the real and the imaginary branches of the MECA 705S-3.000 are shown in Fig. 4.5. The characterization confirms that the transfer characteristics of the two outputs match for a compact 2 GHz band between 2-4 GHz within 0.5 dB. Using (3.30) and (3.31), the frequency characterization can be transformed to a set of frequency-domain compensation parameters.

An external characterization reflects the main imbalance of the two coupler outputs, but does not address the imbalance introduced by the cabling and mismatch of the two ADCs. In particular phase variations, due to different electrical lengths of the connection between the coupler and the ADCs, lead to a significant impairment of the complex sub-sampling receiver performance. The coarse calibration ensures correct thermal noise statistics in the received signal, but can not provide sufficient residual cancellation.

### Fine Calibration

The set of compensation parameters can be refined by an additional in-system calibration step. Figure 4.6 shows the used measurement setup, with the coupler connected to the two ADCs. The test signal from the AWG is directly converted to an analytic signal by a coupler.

Fine calibration uses the complex sub-sampling receiver to measure a narrowband signal with a significantly larger sampling bandwidth. This configuration can cause some confusion regarding the terminology. An over-sampling is performed regarding the relation between the signal bandwidth and the sampling bandwidth. Nevertheless the narrowband signal still resides in a higher Nyquist zone above the Nyquist rate and is therefore sub-sampled. Unlike



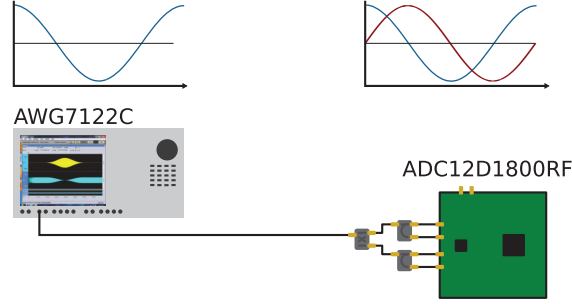


Figure 4.6 – Hardware setup for the fine calibration of the imbalance compensation. The setup allows calibration of the complex sampling chain including imbalance introduced by cables and ADCs.

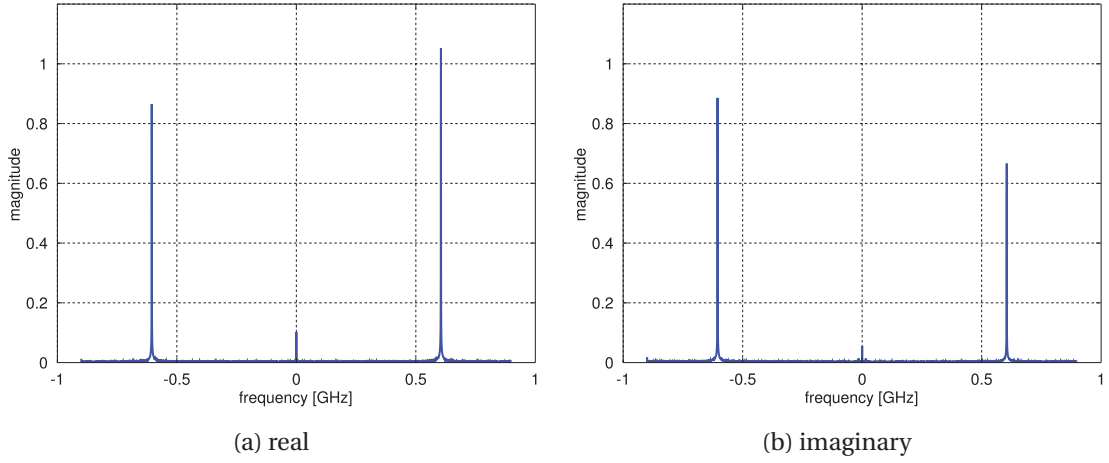


Figure 4.7 – Spectrum of a sub-sampled 2405 MHz sine test signal after the initial coarse compensation.

the critically sub-sampled signal, in the narrowband scenario the negative and positive components do not fold on top of each other in the sub-sampled spectrum. Hence, the negative frequency components in the real and imaginary part can still be observed independently. With an ideal coupler, or a perfect compensation in place, the negative frequency component of the real and the imaginary part would be identical except of a  $e^{j\pi/2}$  phase difference in frequency-domain. As such they cancel each other when combined to a real and imaginary part of a complex number. Imperfect compensation results in a magnitude and/or phase mismatch between the negative components of the two branches.

The fine calibration procedure is then executed in the following way. A cosine wave is fed as a test signal to the complex sub-sampling receiver. For a cosine wave as input the output of an ideal coupler would be a cosine and a sine with a common phase offset. Considering the in-phase output as real part  $s_R(t)$  and the quadrature output as imaginary part  $s_I(t)$  of a

complex signal  $s(t)$  leads to Euler's identity

$$s(t) = s_R(t) + j s_I(t) \quad (4.1)$$

$$= \cos(\omega t + \phi) + j \sin(\omega t + \phi) \quad (4.2)$$

$$= e^{j(\omega t + \phi)}. \quad (4.3)$$

The resulting complex exponential has no negative frequency components. Applying the coarse impairment compensation to the sampled sequences  $s_R[t]$  and  $s_I[t]$  should lead to the same result with a non-ideal coupler. In practice due to imprecision of the compensation parameters the negative frequency component is not fully canceled, but the mismatch can be measured.

The procedure to determine the mismatch of the coarse impairment compensation is described for a single frequency. A cosine with a frequency of  $f_t = 2405\text{MHz}$  is fed to the complex sub-sampling receiver. The two sampled sequences  $s_R[t]$  and  $s_I[t]$  are transformed each to their frequency-domain representations  $S_R[f]$  and  $S_I[f]$  using the DFT and corrected with the compensation parameters obtained from the first coarse compensation step. The magnitude of the corrected spectra of the real and imaginary part of the sampled signal are shown Fig. 4.7a and Fig. 4.7b. In both spectra the positive frequency components of the sine wave have folded to  $f_p = 2405\text{MHz} - 1800\text{MHz} = 605\text{MHz}$  and the negative are found at  $f_n = -2405\text{MHz} + 1800\text{MHz} = -605\text{MHz}$ . As expected due to the coarse compensation the two negative frequency components approximately match in magnitude, while the positive frequency components are not matched at all. The spectrum of the combined (complex) signal in Fig. 4.8a shows that the negative frequency components mostly cancel each other. Nevertheless mismatch leads to a noticeable residual negative interference component which limits the receive performance. Sweeping the test signal and comparing the energy of the positive frequency component and the negative frequency residual allows to determine the signal-to-interference ratio (SIR) as a function of the frequency. The plot of such an SIR spectrum in Fig. 4.8b shows that the level of negative frequency suppression depends on the frequency.

The fine calibration step now uses the information about the mismatch to compute an additional compensation filter, that can be merged in the coarse compensation filter. This filter further reduces the level of the residual negative interference. As we have seen in the ideal case the two negative frequency components match and cancel each other. Hence the fine calibration factor for the frequency  $f_n$  can be calculated from the mismatch of the negative components in  $S_R$  and  $S_I$  as

$$H_{\text{cal}}[f_n] = \frac{S_R[f_n]}{-j S_I[f_n]}. \quad (4.4)$$

For a full fine calibration spectrum a frequency sweep is performed through the band of interest. The sweep is repeated 20 times to reduce the impact of noise on the calibration data. The fine calibration profile obtained from the hardware setup is shown in Fig. 4.9.

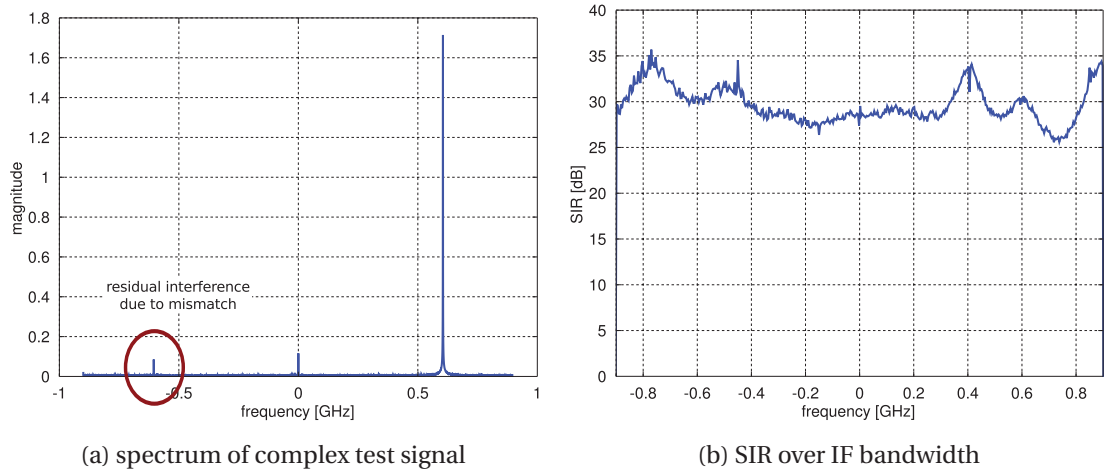


Figure 4.8 – Residual interference in coarse compensated signal due to compensation parameter imprecision. In Fig. 4.8a the effect is shown in frequency-domain for a single test frequency, while Fig. 4.8b shows the condensed effect after a test signal sweep.

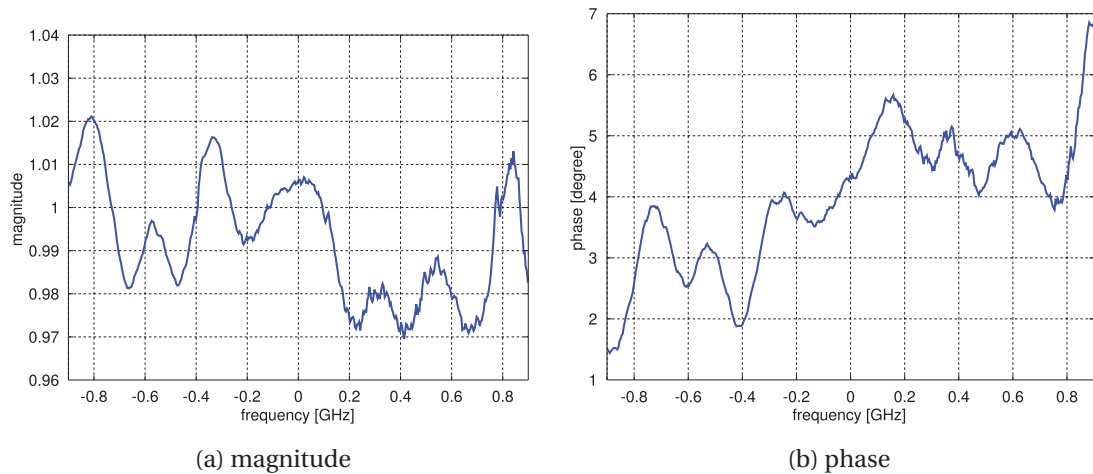


Figure 4.9 – Spectrum of the fine calibration parameters obtained after 20 fine calibration sweep measurements.

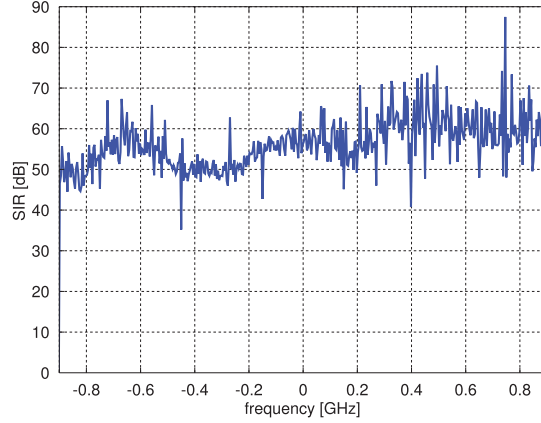


Figure 4.10 – SIR level of signal after applying fine calibration

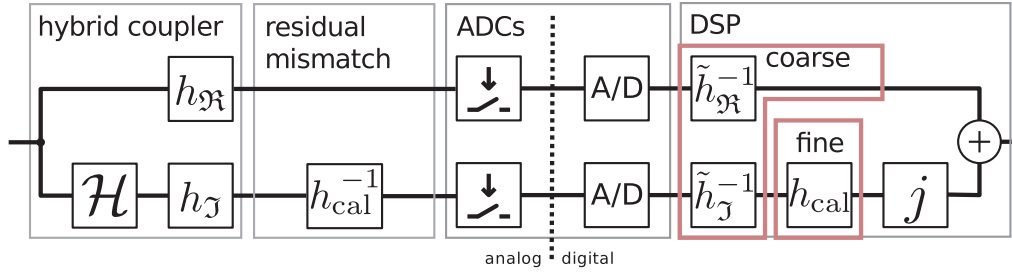


Figure 4.11 – Signal flow of the impairment compensation in the complex sub-sampling receiver.

As the fine calibration filter is determined solely from the difference of the two outputs it has only a single dimension and can therefore not be normalized as described in (3.30) and (3.31). This is the principal reason why an initial coarse compensation step is needed. The SIR after application of fine compensation parameters is shown in Fig. 4.10. It can be seen that the SIR is significantly improved compared to Fig. 4.8b.

### Compensation Results

Including the fine calibration filter on the imaginary branch we can model the signal flow as shown in Fig. 4.11. Imbalance introduced by the cabling, the ADCs, and the imprecision of the coarse coupler characterization are merged to form a combined residual mismatch component. As the fine calibration procedure determines a combined effect only, it is not suitable to separate the different components of the mismatch.

The SIR measurements indicate a significant improvement in the signal quality because of the fine calibration step. However, due to the special nature of the test signal the value can not necessarily be translated to the RX signal quality. A modulated signal is used to assess the effect of the different compensation schemes on the signal quality. Figure 4.12 shows the

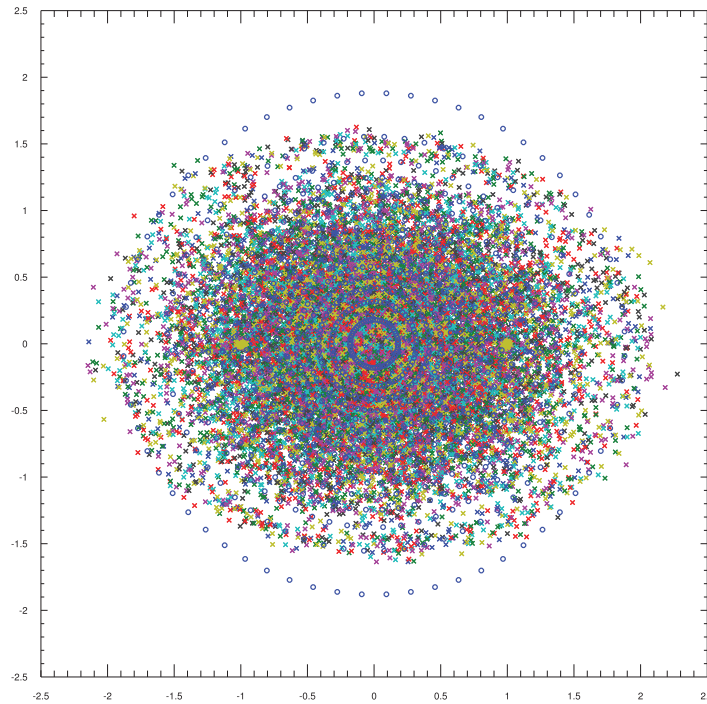
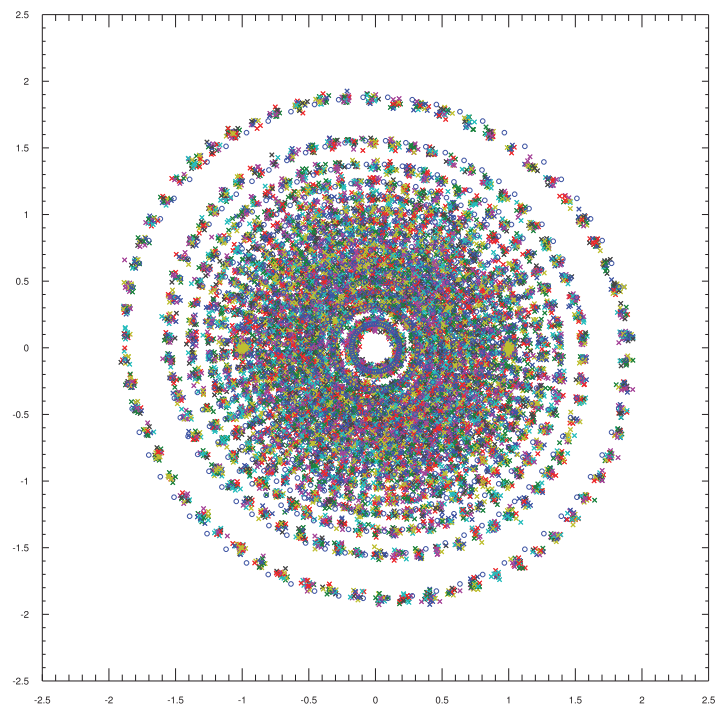


Figure 4.12 – Measured APSK1024 constellations received by a complex sub-sampling receiver without any impairment compensation. Blue circles mark the perfect constellation points.

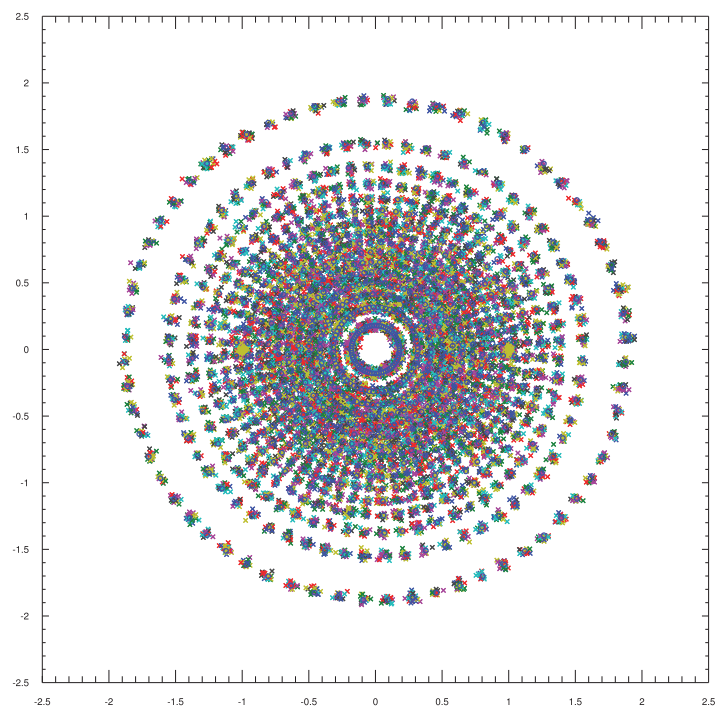
received constellation of an APSK1024 modulated signal before applying any compensation. The strong geometric distortion introduced by the coupler imbalance can be clearly observed. Nevertheless the basic constellation structure is still visible and even without compensation EVM levels of around -12 dB can be achieved. While this is obviously not sufficient to operate high-order modulations in an efficient code rate regime, lower order modulation schemes can be used even without any compensation.

Applying the compensation in the baseband signal processing improves the received signal quality significantly. The constellation after applying the coarse compensation filter is shown in Fig. 4.13a. The geometric distortion is visibly reduced and the receive EVM is improved to -24 dB. Nevertheless, careful observation shows that there is still some distortion present in the constellation. Finally applying the compensation filter obtained from the fine calibration procedure leads to the constellation shown in Fig. 4.13b. The constellations shows no visible geometric distortions and the EVM is improved further to below -30 dB. An EVM of -30 dB is considered sufficient for the targeted backhaul application. It further matches the expected operating regime of future directional mmWave links [124].

Comparing the signal EVM of -30 dB to the estimated SIR (cf. Fig. 4.10) obtained during the fine calibration shows a significant difference. The gap might be explained by limitations of the fine calibration scheme and suggests that a higher precision may be obtained when applying more advanced calibration techniques.



(a) coarse (-24 dB EVM)



(b) fine (<-30 dB EVM)

Figure 4.13 – Measured APSK1024 constellation of complex sub-sampling receiver after coarse compensation and after fine calibration.

### Impact on the Dynamic Range

The loss of dynamic range due to the impairment compensation scheme can be determined from the spectrum of the noise floor of the ADC after compensation. To perform this measurement the input of the hybrid coupler is terminated with  $50\ \Omega$ . In this case the error floor is dominated by the noise floor of the ADCs. A measurement is taken and coarse and fine compensation are applied to the sampled “empty” sequence. The spectrum of the compensated signal is a simple experimental measure, how the noise floor is affected by the compensation. In Fig. 4.14a the power spectral density of the uncorrected signal calculated using Welch’s method [125] is shown. After applying coupler impairment compensation it can be seen that the noise floor is slightly raised above 0.7 GHz. The increase in frequency sensitivity of the compensated noise floor is approximately 2-3 dB, this is also the additional amount of dynamic range required to ensure correct coupler impairment compensation. Nevertheless, Fig. 4.14c shows the noise floor spectrum, after compensating for the coupler impairment and the general frequency selectivity of the RX chain. We can conclude that in the testbed considered the loss of dynamic range due to coupler compensation is insignificant compared to the loss from a common frequency selectivity of the components. This result may not be generalized as a fully integrated 60 GHz transceiver might exhibit significantly less frequency selectivity.

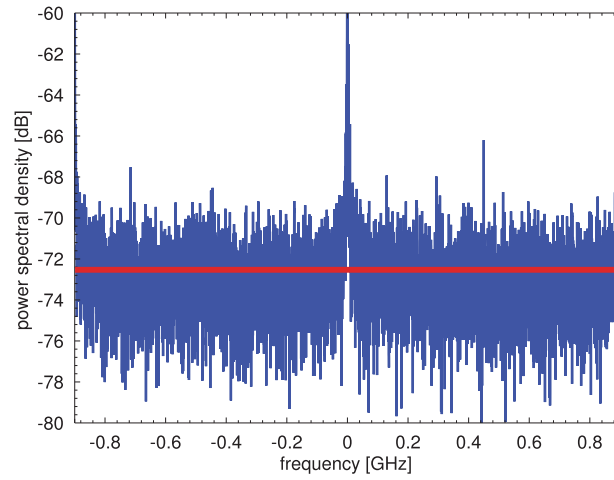
#### 4.2.2 Compression

A crucial step in the engineering of a testbed is to ensure that all components are operated in their linear regions. The signal processing theory of wireless communications heavily relies on the assumption of linear behaviour. Non-linearities introduced in the transmission chain propagate and limit the final performance of the system. The difference between linear and non-linear impairments is the difficulty to track and compensate the non-linear effects at a later stage. It is usually beneficial to avoid non-linearities in the first place.

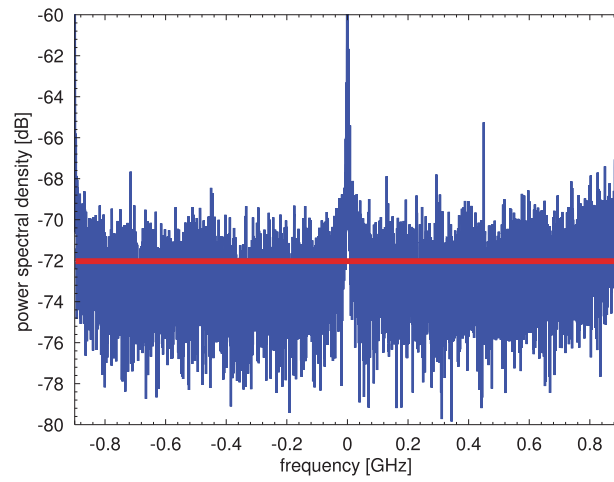
The two-tone test is a common method to determine the level of non-linearity introduced in the system by intermodulation. A test signal consisting of two sinusoids with equal energy and spaced  $\Delta f$  apart, is injected in the system and the output spectrum is observed. In the spectrum of the two tone test the intermodulation products can be easily identified, as they appear at multiples of  $\Delta f$  away from the test signal.

Figure 4.15a shows the spectrum of the two-tone test signal generated by the AWG. The first non-linear components can be seen at approximately 40 dB below the test tones. Transmitting the signal over the 60 GHz link does not contribute any further significant non-linear components, as can be seen from the two-tone spectrum after transmission shown in Fig. 4.15b. The results of the two-tone test are used to adjust the operation points found during the link budget calculation. Especially the input power level of the transmit IF port, which is crucial for maximizing the link performance. The input power level, the initial fixed gain amplifier and the variable gain PA need to be carefully balanced to maximize the link EVM.

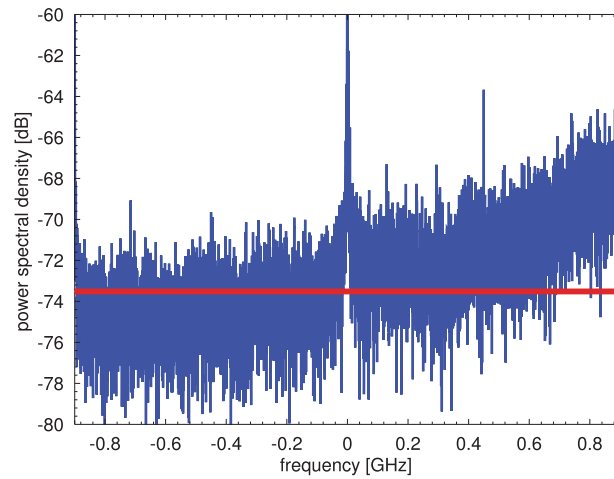




(a) uncorrected



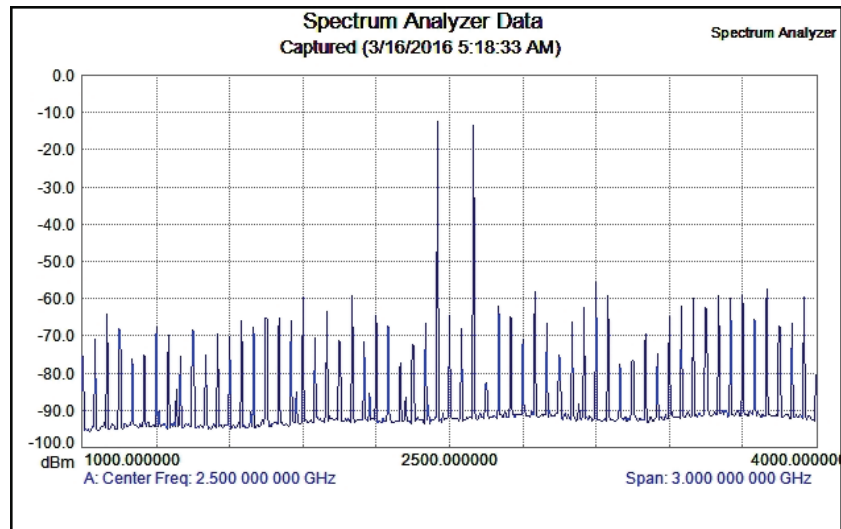
(b) coupler impairment corrected



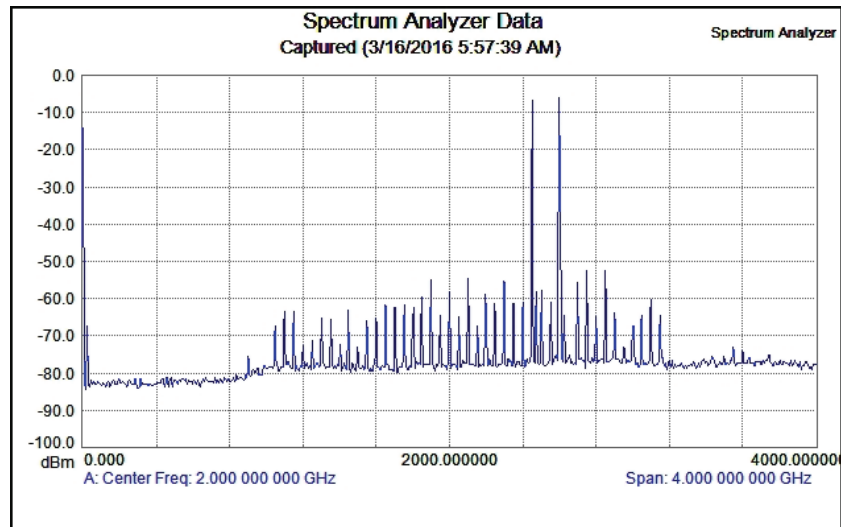
(c) full frequency-selectivity corrected

Figure 4.14 – Walsh’s power spectral density of the ADC noise floor with different levels of compensation applied, illustrating the loss of dynamic range.





(a) At the output of the AWG.



(b) At the IF signal of the RX with a TXPS of C4.

Figure 4.15 – Spectrum of a two-tone test signal directly out of the AWG and of the IF signal after the 60 GHz transmission.

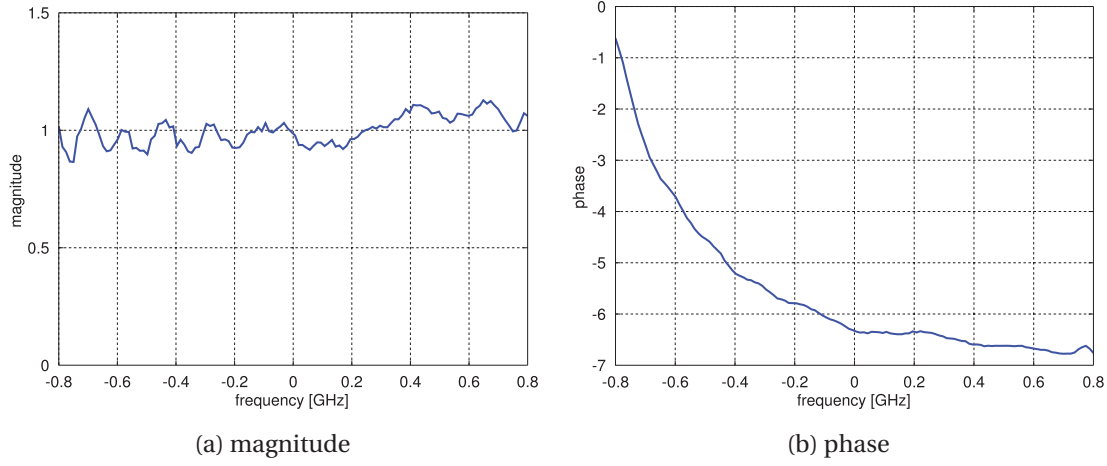


Figure 4.16 – Frequency response of an example measurement taken on the testbed with a LOS connection with coupler-impairment and common frequency selectivity compensation already applied.

### 4.2.3 Common Frequency Selectivity

The frequency selectivity of the components especially the cabling and the ADCs can have a significant impact on the signal. This frequency selectivity often exhibits a low-pass characteristics due to the wide channel bandwidth. Unlike the coupler mismatch this impairment does not cause the introduction of non-linear interference, but is linear in nature. It appears in the receiver signal processing as part of the channel impulse response and can be measured by a linear channel estimator. Nevertheless, the receive chain induced frequency selectivity must be addressed independently of the actual channel frequency selectivity because it has different noise statistics. The frequency-domain of a compensated channel impulse response for a LOS channel is shown in Fig. 4.16. It can be seen that the frequency compensation achieves a flat channel impulse response. Nevertheless there is a strong phase selectivity, that causes a significant time-domain dispersion as shown in Fig. 4.17. While phase-selectivity does not impact the theoretical capacity of the channel it imposes practical constraints on the receiver architecture. Significant amounts of the channel energy spread over more than 15 taps, which is especially challenging for a time-domain receiver. The sequence estimation or equalization architecture of such a receiver needs to be able to cope with this delay spread.

## 4.3 Measurement Considerations

The capture of a single measurement on the testbed involves several time intensive steps. Initially the frame needs to be generated, resampled to the TX sampling rate, and digitally upconverted to the IF. The frame with the corrected sampling rate is uploaded over Ethernet to the AWG and the output run engine is activated. The run engine outputs the programmed sequences on the analog output in a continuous loop. Afterwards the trigger of the ADC board

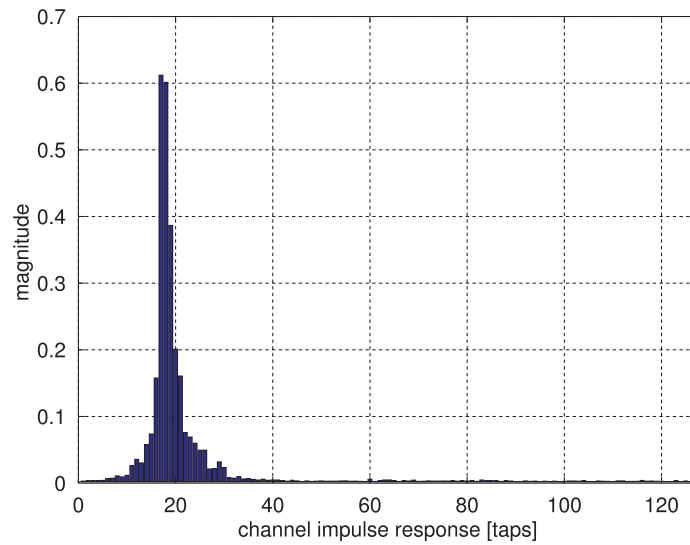


Figure 4.17 – Magnitude of the channel impulse response taps of the example measurement from Fig. 4.16b in time-domain.

Table 4.2 – Testbed measurement round-trip time in single frame mode and RX-block mode with 10 frames.

| frame | code-words       | raw symbols | 1 frame     | 10 frames | avg./frame  | reduction |
|-------|------------------|-------------|-------------|-----------|-------------|-----------|
| Short | $7 \times 8192$  | 8192        | <b>39 s</b> | 143 s     | <b>14 s</b> | 64%       |
| Long  | $18 \times 8192$ | 21504       | <b>72 s</b> | 240 s     | <b>24 s</b> | 67%       |

can be armed and with the next iteration of the AWG the data acquisition is started. The acquired data is downloaded to the host PC and parsed in MATLAB for RX baseband signal processing.

An overview of the times required to transmit and receive a frame is listed in Tbl. 4.2. The total round-trip time for a single data acquisition of a long frame of 14745 data symbols is 72 s. The measurement can be optimized by performing multiple data captures of the same programmed frame data. The AWG is programmed in such a way that it outputs the TX frame in a continuous loop. This allows several receive data acquisitions to be obtained, while requiring only once the overhead to generate a frame and program the AWG. This operation mode is subsequently called block-RX and reduces the average acquisition time for a frame significantly. When a TX frame is used for ten receive measurements the average time required for a single frame reduces to 24 s. For a short frame of 5734 data symbols the average time per frame reduces from 39 s to 14 s when block-RX is used. On the downside the use of block-RX obviously reduces the entropy in the measurements, hence it must be ensured that sufficiently many independent measurements are taken. In order to keep the correlation between results low, a maximum of 10 captures per transmit frame is performed.

Despite the use of the RX-block mode, the acquisition of sufficient measurement points takes several hours. As the measurement environment is not a perfectly isolated system, measurements spread over multiple days bear the risk that changing conditions bias the measurement results. In order to ensure comparable data sets, the measurements are conducted in campaigns. During a campaign, measurements with different configurations and power settings are interleaved to ensure that results can be compared. While interleaving cannot avoid changing environment conditions, it can ensure that all measurements are influenced in a similar fashion.

### 4.4 Summary

The testbed setup shows that a high-rate mmWave link can be realized using COTS components. The resulting link is well suited for research on high order modulation backhaul links. The testbed implements the complex sub-sampling receiver architecture proposed in Chapter 3 and shows its suitability for wideband mmWave receivers. The non-ideality of practical couplers limits the receiver performance significantly and allows the operation with low-order modulation schemes because of interference. An RX EVM of -14 dB can be achieved without coupler impairment compensation. A practical two step procedure characterizes the hybrid coupler impairment and any mismatch between the two branches of the sampling chain. Based on the characterization data a coupler compensation scheme allows 26 dB reduction of the interference from the non-ideal coupler.

The impairment compensation of the sub-sampling architecture has an impact on noise and dynamic range of the receiver. Impairment compensation is achieved at the cost of dynamic range of the ADCs. Nevertheless in the described setup the loss of dynamic range is negligible compared to the dynamic range loss induced by the overall frequency selectivity of the RX chain.

With compensation the complex sub-sampling receiver achieves excellent RX linearity with an EVM below -30 dB at a sampling bandwidth of 1.8 Gsps. Such performance figures allow modulations with a cardinality of 1024 and higher, and thus meets the expected hardware capabilities of next-generation mmWave backhaul links. The comparison with previous 60 GHz demonstration setups in Tbl. 4.3 shows that the proposed setup stands out with its combination of bandwidth and high order modulation.

Table 4.3 – Comparison of digital radio testbeds for 60 GHz demonstration.

|                  | [126]   | [62]    | [127]        | This Work |
|------------------|---------|---------|--------------|-----------|
| Transmission     | SC/OFDM | OFDM    | OFDM         | SC        |
| Bandwidth        | 75 MHz  | 500 MHz | 250 MHz      | 1800 MHz  |
| Modulation       | QAM     | QAM     | QAM          | QAM,APSK  |
| Modulation order | 4-16    | 2-64    | 4-64         | 2-1024    |
| MIMO             | -       | -       | $2 \times 2$ | -         |



## 5 Information-Driven Modulation and Coding

High order modulated mmWave links combine high spectral efficiency with a large available bandwidth. They are a promising candidate to satisfy the requirements of future cellular backhaul networks. Unlike mobile terminals, such stationary devices are more focused on throughput and less constrained by stringent power budgets or compatibility requirements. In this scenario, spectral efficiency is more relevant and therefore more advanced modulation and coding techniques need to be considered.

For the purpose of this discussion we adopt the definition of Massey [128] and draw the line between modulation and coding by whether [or not] memory is involved. According to this definition, modulation is a memory-less mapping of data words to constellation symbols, while coding is the mapping of a sequence of information bits to one or multiple data words. In practice multiple different codes can be concatenated to create the data words for the modulation.

It is known that with increasing SNR alternative modulation schemes promise significant theoretical improvements over the equidistant modulation schemes currently used for mmWave systems. Nevertheless most discussions about the spectral efficiency of modulation address only the theoretical aspects. Little is known about how much of the theoretical gain can be leveraged in a practical system.

In this chapter, the construction of constellations that are optimized for spectral efficiency is discussed and their feasibility for implementation is demonstrated. Further real-world measurements of the achievable gains of shaped amplitude phase shift keying modulations are shown. In the second part of this chapter, the construction of error correction codes for such modulations is discussed.

### 5.1 Information-Driven Modulation

For the majority of wireless systems the choice of modulation is motivated by implementation considerations and not the amount of transferred information. QAM is the most commonly

used modulation scheme today. QAM allows to break the complexity of modulation and demodulation down into two orthogonal dimensions. It is important to note that occasionally (e.g. in [129]) the term QAM is used in a wider sense for any kind of quadrature modulation based on orthogonal base pulses. We will use QAM for what Forney [130] describes as "narrow sense QAM", a quadrature modulation as a symmetric two-dimensional pulse amplitude modulation (PAM) in which both dimensions have the same modulation order. The resulting constellation schemes are characterized by their equidistant constellation points, the square shape and the uniform probability of the constellation points. Square QAM is found in nearly all modern communication standards from cellular applications like LTE [6] to IEEE 802.11 ad [23] wireless LAN. Due to its widespread use, QAM is very well understood and offers proven low-complexity soft-demapping schemes suitable for hardware implementation [131]. Besides the limitation that square QAM constellations require an even modulation order, it is well known that QAM schemes are not optimal in an information theoretic sense.

In [130] Forney outlines two fundamental problems:

1. The square envelope shape of the constellation diagram entails an inherent power penalty, as constellation points can be rearranged from the corners to the sides to get a more round shaped constellation. Such a modified constellation will offer the same distances between the points and therefore the same symbol error probabilities, but requires less energy. As a side effect such an optimized constellation will also offer a lower PAPR which reduces the backoff requirement and thereby improves system efficiency [32].
2. The second problem is related to the equidistant spacing of the symbols. Traditionally constellations are constructed to maximize the minimal distance between constellation points, therefore the symbols of the two PAM modulated dimensions are equidistantly placed on the axis. Because of the equidistant property of QAM, the uncoded error probability quickly converges toward zero for high SNR. As a practical consequence QAM links can be operated with very high code-rates or even completely without coding for a sufficiently high operating SNR. While this property seems to be appealing at the first glance, it was already shown in [130] that such an uncoded operation regime is far away from the channel capacity and exhibits a very low spectral efficiency. Hence, the behavior in the high-SNR/high-rate regime is of little interest for choosing a suitable modulation. Instead it was shown that always a combination of modulation and coding is required to close the gap to the theoretical channel capacity. Further it was noted in [128] that "that the coding and modulation system together should deliver "information bits" ".

Many alternatives to square QAM constellation schemes have been proposed, often based on alternative envelopes. Most of the alternatives are motivated either by reducing the PAPR in the context of PA non-linearity [132][133] or by supporting odd modulation orders [134][88][135][136]. These alternative constellations are designed with the symbol error



probability in mind and therefore try to maximize the distance between constellation points. Without additional measures an equiprobable input to such a constellation leads to an approximately uniform<sup>1</sup> distribution of the modulated symbols. From Shannon we know that a Gaussian symbol distribution is required to maximize the entropy and it was shown in [137] that for high SNR, uniform equiprobable signaling entails a gap of 1.53 dB in capacity.

Hence, two strategies have emerged to get rid of this discrepancy and approximate the Gaussian distribution. The first is based on combining an equidistant constellation with a pre-coding scheme [138][139][140]. The pre-coding ensures a non-equiprobable distribution of the data words used for the modulation resulting in a shaped symbol distribution. While it was shown that such methods can leverage a shaping gain, they are usually not very suitable for hardware implementations. They are based on variable length words which is especially undesirable in high speed application because it requires irregular signal processing.

The second approach to achieve a Gaussian symbol distribution drops the minimum distance criterion and shapes the distribution of the constellation points. With a shaped constellation the channel capacity can be achieved even with equiprobable signaling [137] and the signal processing can be realized with a regular constant rate architecture. In the step towards capacity achieving modulations, [137] and [141] have shown non-uniform constellations for a single dimension. Two-dimensional APSK constellations that approximate the Gaussian distribution have been suggested in [142]. Several square but non-uniformly distributed constellations to increase the bit-coded capacity are suggested in [143]. Finally Meric showed in [144] a method to construct arbitrary-order APSK constellations that asymptotically result in a Gaussian distribution and hence can asymptotically achieve capacity. An example for a constellation according to Meric is shown in Fig. 5.1<sup>2</sup>. The ideas of non-uniform constellations and non-equiprobable symbols have been combined in [145] with only little additional gain.

One drawback of shaped constellations is that the use of a soft decision demodulator as originally proposed in [146] and [147] becomes mandatory. Hard decision demodulation will not provide good results as a significant part of the information is irretrievably lost. With some constellation points falling virtually on top of each other the shaped constellations exhibit a distinct error floor in uncoded operation. Although the practical implication of this is limited, as hard decision demodulators are according to Massey “about the worst possible answer” [128] to the problem of demodulation, independent of the constellation. Nevertheless the problem of efficient soft-decision demodulation of non-uniform shaped constellations is not trivial and needs to be addressed.

## 5.2 Amplitude Phase Shift Keying (APSK)

While QAM is still the predominant modulation for most wireless systems, APSK has occupied a niche in the area of satellite communication. APSK was shown to be beneficial for the

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<sup>1</sup>Uniform in an asymptotic sense, for modulation orders going towards infinity.

<sup>2</sup>Constellations will always be plotted in the complex plane with the x-axis corresponding to the real part.

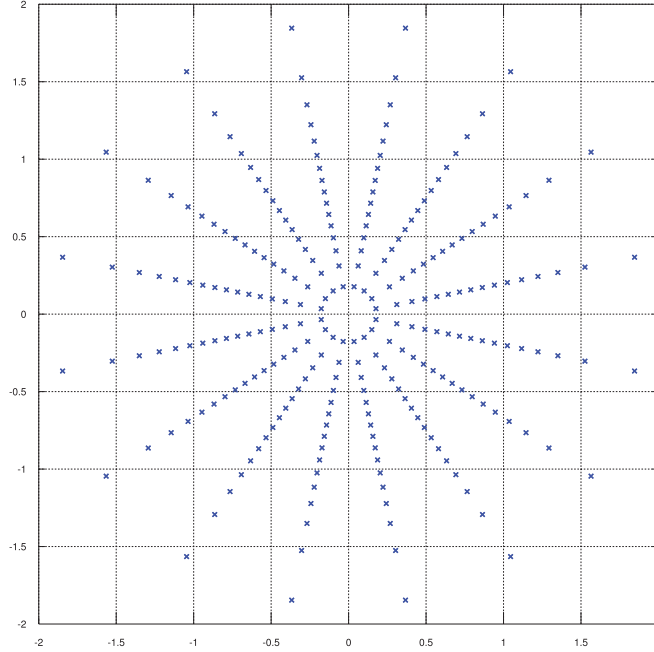


Figure 5.1 – 256-ary APSK constellation generated according to Meric [144].

highly non-linear traveling wave tube (TWT) amplifiers used in satellites [148]. The DVB-S2X standard [53] specifies different APSK constellations with cardinality up to 256. For the 256-ary modulation two basic types with minor variations each are specified. The first type shows a very regular structure, while the second type exhibits some anomalies in the center.

For the regular type, the symbols are allocated on 24 axial rays with and a phase-independent set of 8 radii. The codes are similar to the constellation shown in Fig. 5.1. While the phases follow a fix uniformly-distributed pattern, the radii are specific to the rate of the used channel code.

The second more irregular type specifies two variants for the constellation points for different code-rates. The two variants are shown in Fig. 5.2. While the irregular constellations exhibit also a fair amount of circular symmetry for the outer symbols, they feature a more rectangular structure in the center. In order to analyze the two irregular constellations in more detail a probability distribution is derived based on the constellation points. The real and imaginary values of the constellation points are sorted in 21 uniformly spaced bins spanning from  $-2$  to  $2$ . The resulting discrete probability density functions are shown in Fig. 5.3 and provide some insight about the constellations. The mismatch between the two axis, especially around the center is clearly visible from the distribution. An identical discretized and correctly scaled normal distribution with  $\sigma^2 = 0.5$  is added for reference (in green). It can be seen that both types approximate the normal distribution well for the intermediate section and then diverge again for the tails. It is also interesting to note that all specified constellations put an emphasis

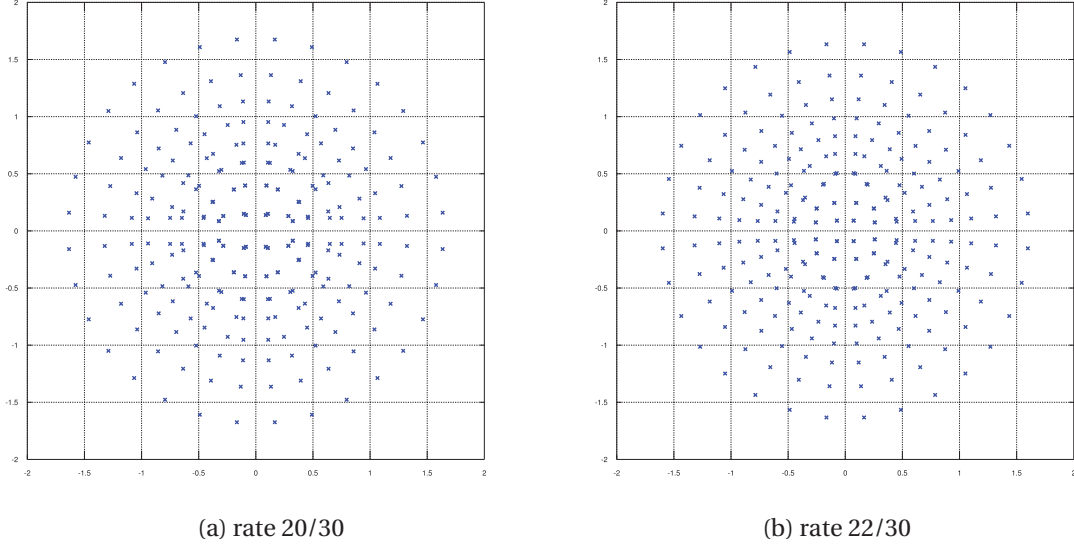


Figure 5.2 – 256-ary APSK modulation according to the DVB-S2X standard [53].

on the number of rays compared to the number of rings.

The APSK constellations of the DVB-S2X standard are based on several different not publicly known construction methods and specify only constellations up to 256-ary modulation. As the Gaussian distribution can only be asymptotically achieved it is of great interest to further increase the alphabet sizes towards the capacity. Hence, the lack of a systematic construction method makes the APSK constellations of the DVB-S2X standard less suitable as a base for APSK research.

### 5.2.1 Meric APSK constellations

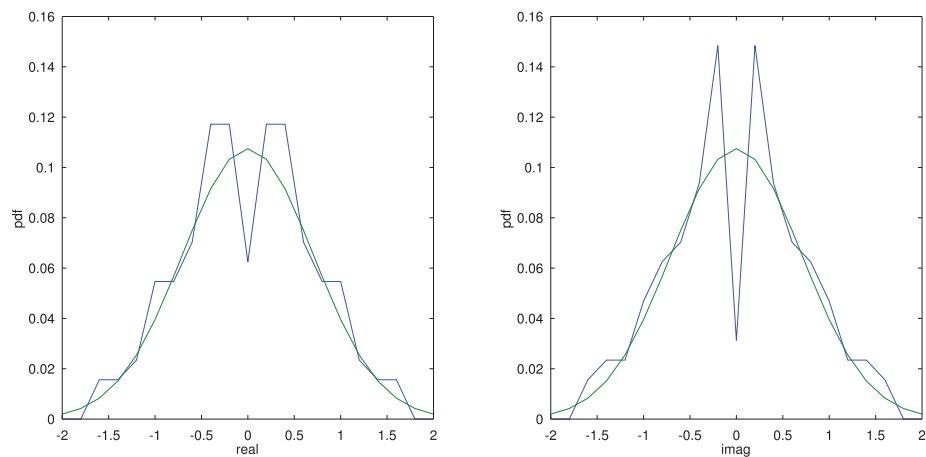
The family of APSK constellations proposed by Meric [144] has a very regular construction method which can be shown to asymptotically approach the Gaussian distribution as the modulation order increases. Like the more regular APSK256 constellation type of the DVB-S2X standard the constellation points are distributed on rays with a uniformly spaced phase and phase-independent radii.

Meric uses a theorem presented by Box-Muller in [149] to show that his proposed construction method leads asymptotically to a Gaussian distribution of the symbols. Let  $U$  and  $V$  be random variables uniformly distributed over the interval  $[0, 1)$ . It can be shown that

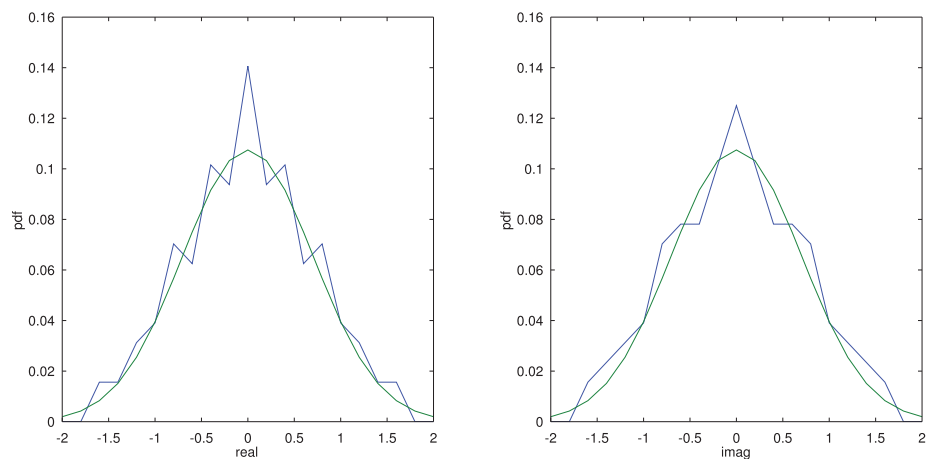
$$X = \sqrt{-2 \ln U} \cos(2\pi V) \quad (5.1)$$

and

$$Y = \sqrt{-2 \ln U} \sin(2\pi V) \quad (5.2)$$



(a) type 20/30



(b) type 22/30

Figure 5.3 – Distribution of the constellation points of the two APSK256 constellations of DVB-S2X. The discretized normal distribution with  $\sigma^2 = 0.5$  is shown in green for reference.

are independent random variables with a Gaussian distribution, zero mean, and variance one.

The constellations are constructed orthogonal, such that the  $M$  symbols of the constellation are distributed on  $M_a$  circles with  $M_p$  symbols each and  $M_a \times M_p = M$ . The symbols are created from the tuple  $(a, p)$  as

$$s_{a,p} = A_a e^{j\phi_p} \quad (5.3)$$

with

$$\phi_p = 2\pi \frac{p-0.5}{M_p}, \quad p = 1, \dots, M_p \quad (5.4)$$

$$A_a = \sqrt{-\ln\left(\frac{a-0.5}{M_a}\right)}, \quad a = 1, \dots, M_a. \quad (5.5)$$

All possible symbols  $s_{a,p}$  form the set  $\mathcal{S}$ . It is obvious that (5.1) and (5.2) correspond to the real and imaginary part of (5.3) with

$$U = \frac{a-0.5}{M_a} \quad (5.6)$$

and

$$V = \frac{p-0.5}{M_p}. \quad (5.7)$$

The assignment of both elements of the tuple to an equidistant grid between 0 and 1 converges weakly to a uniformly distributed random variable if the modulation order goes to infinity. An additional scaling factor of  $\frac{1}{\sqrt{2}}$  ensures that each dimension has a variance of  $\frac{1}{2}$  and therefore the resulting complex symbols have a total variance of one. For the 256-ary Meric constellation shown in Fig. 5.1 the corresponding distribution is depicted in Fig. 5.4. It can be seen that unlike for the irregular distributions shown before the distribution is identical along the real and the imaginary axis.

### 5.2.2 Asymmetrical Meric APSK

One advantage of APSK compared to QAM is, that the radial and the angular dimensions do not need to be of the same order to achieve circular symmetric constellations. In the original paper Meric assumes symmetric dimensions, meaning that  $M_a = M_p = \frac{M}{2}$ , in order to ensure that for  $M \rightarrow \infty$  both  $M_a$  and  $M_p$  also go towards infinity. But he also noted that such a configuration might be not optimal for practical systems. With an increasing  $M_a$  the minimum value of the term  $\frac{a-0.5}{M_a}$  will become smaller and therefore the maximum value for the amplitude  $A_a$  will increase. Hence, the radius of the constellation envelope will increase. As the constellation is normalized to unit energy the increasing radius leads to a higher PAPR of the system. This leads to the fundamental insight that capacity achieving modulation is

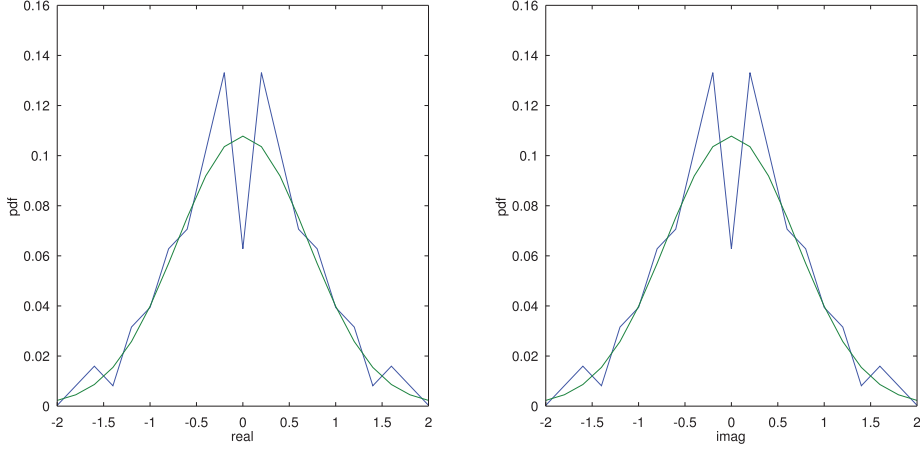


Figure 5.4 – Distribution of the constellation points of a APSK256 according to Meric [144].

not feasible, as it would require infinite dynamic range in transmitter and receiver. However, even for moderate modulation orders the PAPR of Meric APSK constellation becomes quickly impractical. Fortunately the problem can be partly mitigated by letting  $M_a$  and  $M_p$  increase at different rates. It has already been noted in [144], that APSK with asymmetric dimensions can under certain conditions still achieve Gaussian capacity.

Independent from the PAPR problem is the question of how quickly a constellation converges towards the Gaussian capacity with increasing modulation order. In [144] only the asymptotic behavior is analyzed, while it is not clear “per se” what configuration achieves the highest information rate for a finite constellation size. The evaluations in [142] indicate that an asymmetric weighting of dimensions is beneficial not only for the PAPR but also increases the average mutual information (AMI). Hence, we suggest the following asymmetric scheme

$$m, \text{ even} \begin{cases} m_A = \frac{m}{2} - 1 \\ m_B = \frac{m}{2} + 1 \end{cases} \quad (5.8)$$

$$m, \text{ odd} \begin{cases} m_A = \lfloor \frac{m}{2} \rfloor \\ m_B = \lceil \frac{m}{2} \rceil \end{cases} \quad (5.9)$$

for setting the order of each dimension with a slight bias to the phase. A 256-ary constellation generated according to (5.8) is shown in Fig. 5.5. In comparison to the symmetric Meric constellation from Fig. 5.1 the emphasis on the phase can be clearly seen. The resulting distribution of the constellation points of the asymmetric scheme is shown in Fig. 5.5.

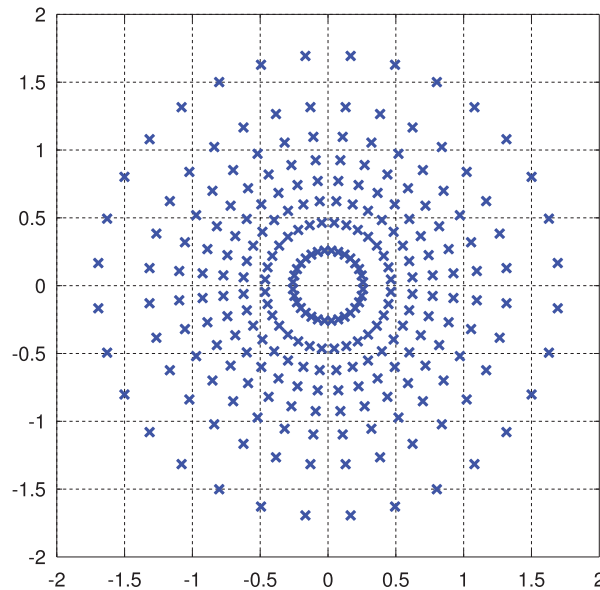


Figure 5.5 – The constellation points of a APSK256 according to a modified Meric scheme with asymmetric weighted dimensions.

### 5.2.3 Symbol Mapping & Demapping

While Meric shows that his APSK constellations can asymptotically achieve capacity, his proof is based on the distribution of the symbols only. It is not shown how an APSK constellation can leverage its theoretical advantage in a practical wireless system.

Due to its inherent symbol error floor, shaped constellations are only meaningful in combination with error correction coding. In [128] it is stated that an optimal demodulator is one that does not provide a decision but instead provides a vector with probabilities for each possible constellation point. A coding scheme that directly operates on such a vector of symbol probabilities is possible, but brings many problems for implementations. The size of the interface between demodulation and decoding would grow exponentially with the modulation order, making it increasingly difficult to implement for higher modulation orders. Additionally the architecture of the decoder itself would be highly dependent on the employed modulation order.

The standard way to overcome these problems is to abstract the interface between demodulation and decoding and to represent the probability of the symbols with its associated bits. Hence, the demodulator passes bit probabilities instead of symbol probabilities to the decoder. While bit probabilities provide a handy means of dealing with demodulation probabilities and thereby simplify the signal processing significantly, they do not remove the dependency between the modulation and the coding. In Section 5.3 this aspect is discussed in more detail.

### Mapping

In order to use the APSK constellation in a bit-coded system, a bit-mapping for all  $M$  symbols needs to be defined. Unlike with irregular constellations the orthogonality of phase and amplitude of the Meric constellations allows a very systematic mapping of the symbols to bits. The two components of the tuple  $(a, p)$  can be independently mapped to bits. Such an orthogonal mapping of the bits to the radial and phase component of the APSK codes was discussed before [142][150][151] and is sometimes referred to as “product-APSK” or “product-constellation-APSK”. The  $m = \log_2(M)$  bits of a symbol are split in  $m_A$  bits for the amplitude and  $m_P$  bits for the phase such that  $m_A + m_P = m$ . A regular Gray-mapping [152]  $\mathcal{G}()$  is used to independently map the bits to the indices in the two dimension. This mapping ensures that along each dimension neighboring symbols differ only in a single bit.

The mapping is performed as follows. A bit vector  $\mathbf{b} = [b_0, \dots, b_{m-1}]$  is separated into two vectors  $\mathbf{b}_A = [b_0, \dots, b_{m_A-1}]$  and  $\mathbf{b}_P = [b_{m_A}, \dots, b_{m-1}]$  for the two dimensions. The symbol  $s$  is then formed using (5.3) with

$$a = \mathcal{G}(\mathbf{b}_A) \quad \text{and} \quad (5.10)$$

$$p = \mathcal{G}(\mathbf{b}_P). \quad (5.11)$$

A 256-ary asymmetric APSK constellation with the associated bit labeling is shown in Fig. 5.6. Because of the small distance between the center points the uncoded bit error rate of this constellation is expected to converge only slowly to zero. And in fact the comparison of QAM and APSK in Fig. 5.7a shows that APSK exhibits a significantly higher uncoded BER for high SNR. This is because of the very small distances between symbols in the center of the APSK constellation, which cause symbol errors even at high SNR. Nevertheless with a  $R = \frac{1}{2}$  LDPC code the same APSK constellation can show a lower coded BER as shown in Fig. 5.7b. This leads to the conclusion that the uncoded BER is a nearly useless measure for the quality of a modulation scheme at high SNR.

### Soft-Decision Demapping

For the soft-decision demapping the demodulator calculates for each bit of the transmitted symbol a probability in the form of a LLR<sup>3</sup>. For the targeted 256-ary and higher constellations exact LLR calculation is not feasible in a practical receiver. Hence, we will only consider the max-log approximation (see Appendix A.4) for the LLR calculation.

The demodulated LLRs allow to compare different modulations beyond the analysis of their distributions. A significant difference between APSK and QAM can already be seen in the shapes of the distribution of demapped LLRs given in Fig. 5.8. The LLRs of the APSK modulation in Fig. 5.8b exhibit overall a significantly smoother distribution compared to the step-like structure in Fig. 5.8a. Further it is interesting to note that the APSK LLR distribution peaks at

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<sup>3</sup>A detailed discussion of the calculation of LLRs is given in Appendix A.3



## 5.2. Amplitude Phase Shift Keying (APSK)

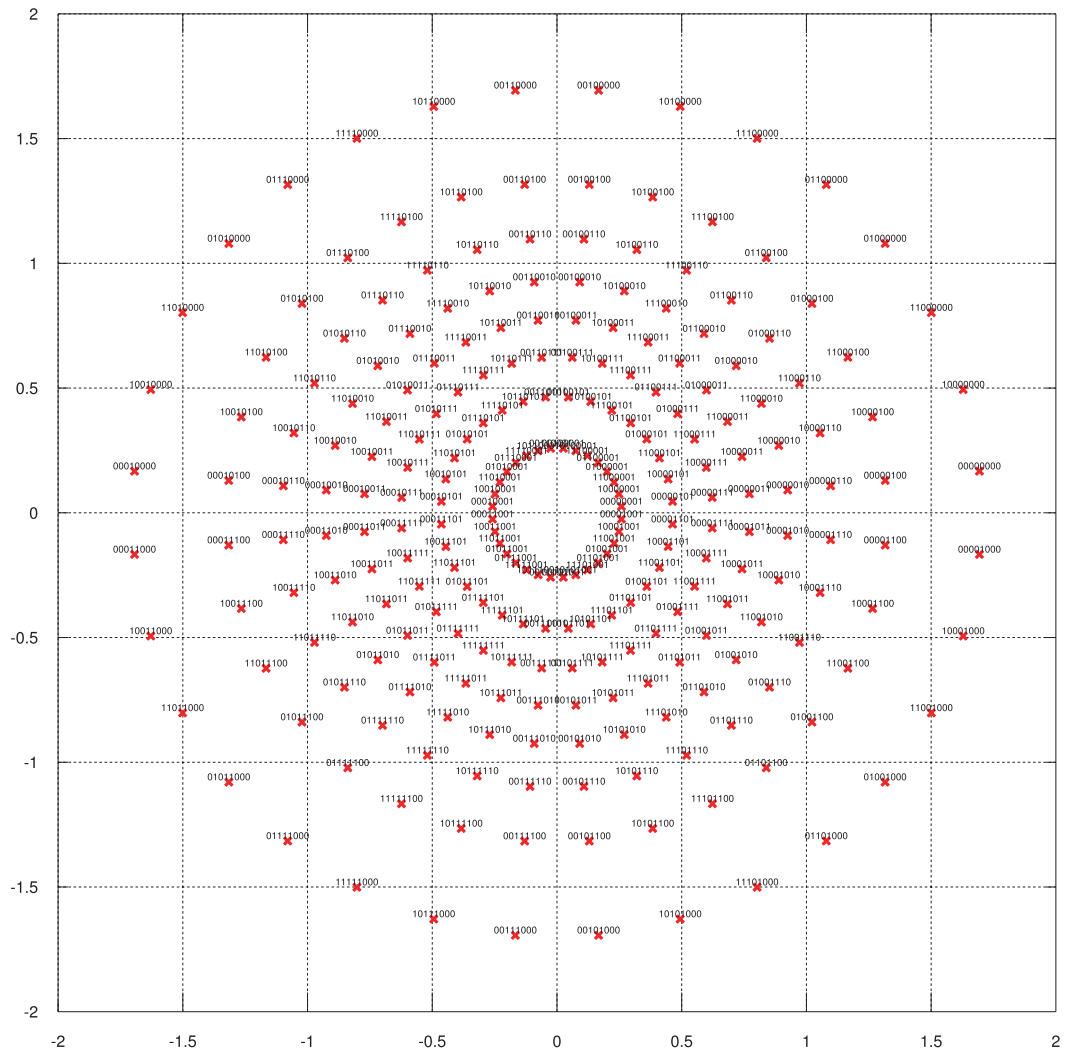
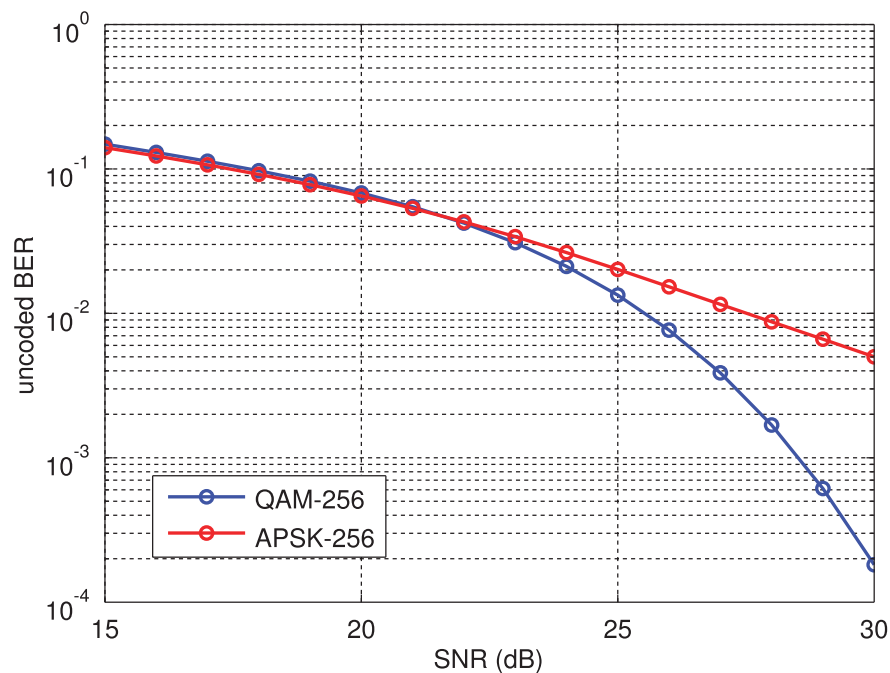
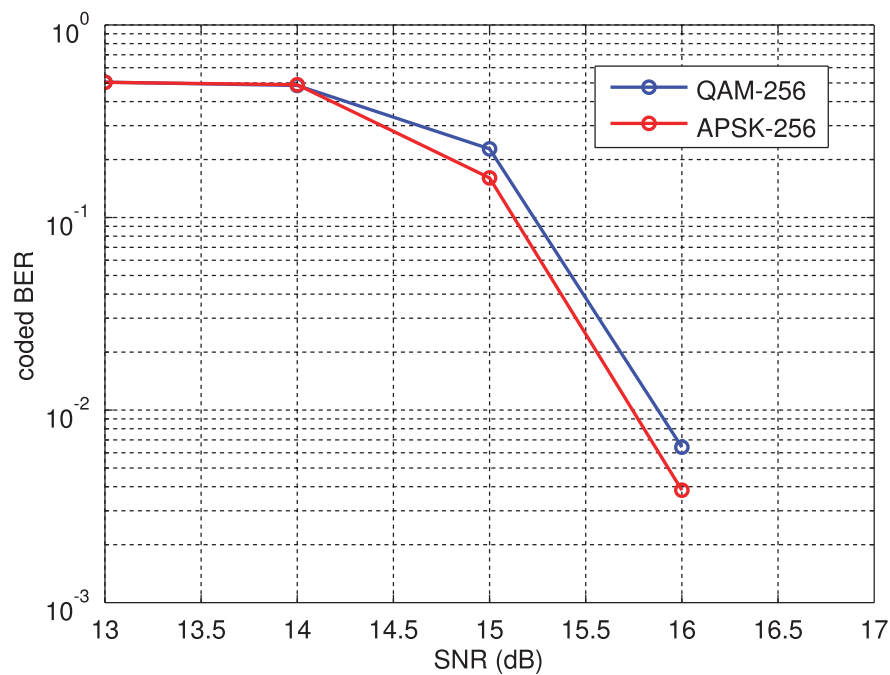


Figure 5.6 – Asymmetric Merit APSK256 constellation with the associated bit labels.



(a) uncoded bit error rate



(b) coded bit error rate

Figure 5.7 – Comparison of uncoded and LDPC-coded bit error rate for QAM and APSK modulation.

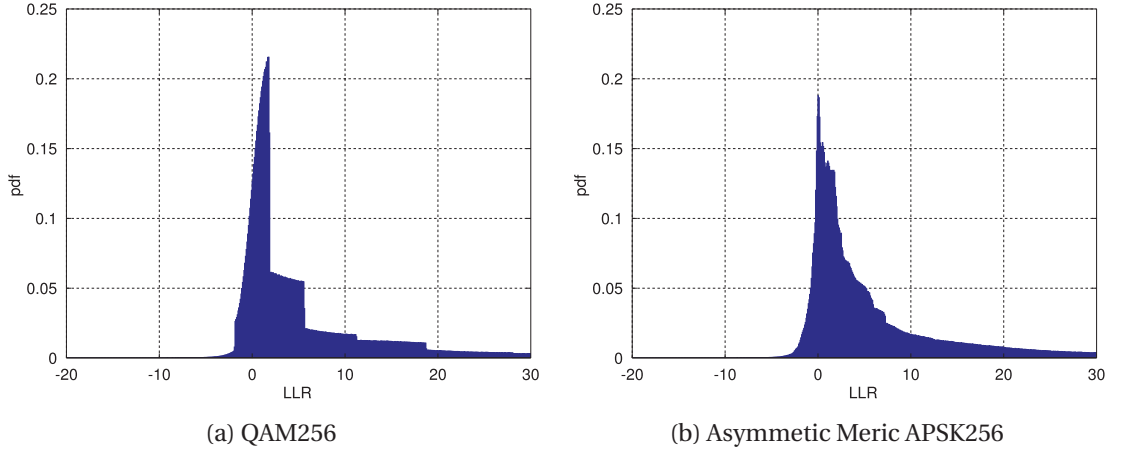


Figure 5.8 – Distribution of demodulated LLRs of 256-ary constellations at SNR = 16dB.

zero while for the QAM LLR distribution the peak is at approximately 1.8. The shown probability mass functions have been experimentally derived from  $1.024 \cdot 10^6$  randomly generated symbols using a max-log demodulator. The resulting LLRs have been normalized by their respective bit value, such that a positive LLR value always corresponds to a correct hard-decision. The symbols were generated using an AWGN channel at SNR = 16dB.

The shape of the distribution might already be an indicator for the larger amount of entropy in the demapped LLRs of the APSK constellations, but for a dependable result a quantifiable metric is required. To this end, the LLR distribution is used to calculate the AMI between the transmitted bits and the received LLR<sup>4</sup>. The AMI provides a powerful measure of the amount of information contained on average in each of the demapped LLRs.

The advantage of the AMI as a measure for the quality of the modulation is its independence from a specific coding scheme. In general the AMI is expressed per bit<sup>5</sup> and allows the comparison of different constellations of the same size. By normalizing it with the modulation order it can be transformed to an AMI per symbol (subsequently called symbol-AMI). Calculating the AMI per symbol offers a comparison of the performance of modulations with different constellation sizes.

Another advantage of the AMI is that it provides some form of end-to-end quality measure for modulation. It can transparently include various non-ideal effects such as the max-log approximation of the demodulator or the channel. For the BER simulations shown in Fig. 5.7 the AMI is plotted in Fig. 5.9. The AMI plot shows a 1 dB advantage of APSK over QAM in the waterfall region. The AMI comparison therefore predicts that the APSK constellation exhibits a better coded BER despite showing an equal or even worse uncoded BER than QAM. In fact the AMI gap suggests an even bigger advantage for APSK compared to what can be observed

<sup>4</sup>A description on how the AMI is calculated can be found in Appendix A.5.

<sup>5</sup>In case of possible confusion, we will refer to this as LLR-AMI.

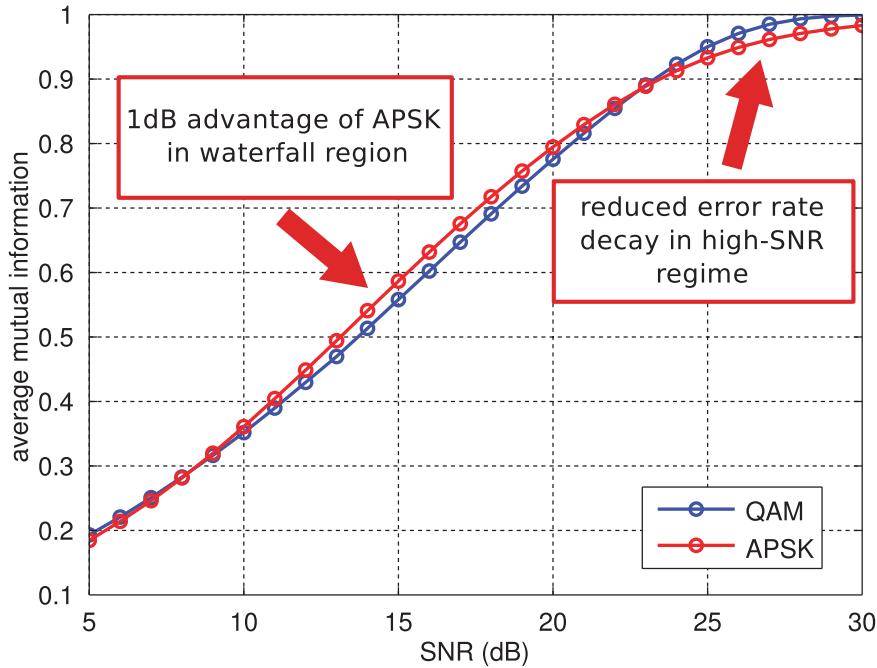


Figure 5.9 – Comparison of the AMI of 256-ary QAM and APSK after max-log demodulation.

in the coded BER. This points to another important factor of the discussion. The aptitude of the code for the used modulation is important for the final outcome. Hence, the AMI can be used to determine the effectiveness of the coding. The dependency between modulation and coding is discussed in more detail in Section 5.3.

### VLSI Implementation

The hardware implementation of the soft-decision demodulation is usually considered to be the biggest obstacle for the adoption of alternatives to QAM. In fact APSK modulation requires a significantly more complex demodulator, mainly because the modulation dimensions do not coincide with the Cartesian coordinates. Sub-optimal schemes have been suggested for a complexity reduction of the demodulation [150][151] based on approximations of the decision regions. Nevertheless what is usually not considered is the demodulation complexity relative to the total required baseband complexity.

Considering the amount of baseband processing required for a high-rate backhaul link, we show that soft-decision demodulation with a simple look-up table (LUT) is feasible and the overhead is low compared to the total receiver complexity. In a LUT based demodulator the equalized symbols serve as address input to a memory of precalculated LLR table. The contents of the LUT are in principal SNR dependent, but when the max-log approximation is used for the LLR calculation a single LUT can be used independent of the noise variance. At the output of the LUT the pre-calculated values are scaled according to the given SNR. It will

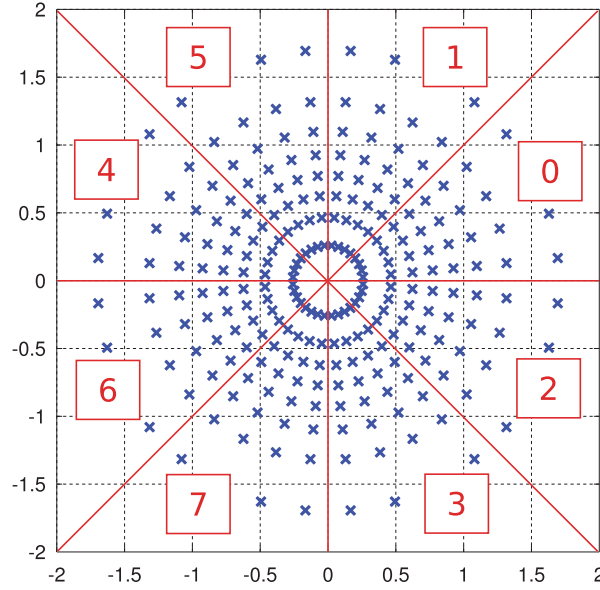


Figure 5.10 – Symmetric demodulation sectors of the modified Meric APSK256 constellation.

be shown that the LUT approach comes with a moderate implementation complexity.

A high degree of symmetry in constellation and bit mapping can be leveraged for a significant complexity reduction of the demodulator. Hence, the proposed bit-labeled Meric APSK code can be demodulated very efficiently. The constellation can be split into eight symmetrical sectors as shown in Fig. 5.10. A comparison with Fig. 5.6 shows that the sectors are not only symmetric in the placement of the constellation points but also exhibit a regularity regarding the labeling of the bits. The borders of the sectors are further chosen such that they can be determined with simple arithmetic operations. The zone index  $i$  can be calculated based on the signs and a comparison of the absolute values of the of the real and imaginary part of the received symbol  $y$  as

$$i = (\Re(y) < 0) \cdot 2^2 + (\Im(y) < 0) \cdot 2^1 + (|\Re(y)| < |\Im(y)|) \cdot 2^0. \quad (5.12)$$

Due to the symmetry of the Gray coding only the LUT values for one sector need to be stored. Based on the sector index the output of the reduced-size LUT is transformed by inversion and swaps into the correct set of LLRs. The schematic of the optimized LUT with the post-processing is shown in Fig. 5.11. With the optimized architecture the number of LUT entries can be significantly reduced. Asymptotically only  $\frac{1}{8}$  of the values are required, which corresponds to a size reduction of 87.5% compared to a full LUT. For practical implementations the size reduction depends on the bit resolution of the input samples. To ease of notation we assume the complex input symbols  $\mathbf{y}$  to have integer values with a magnitude smaller or equal

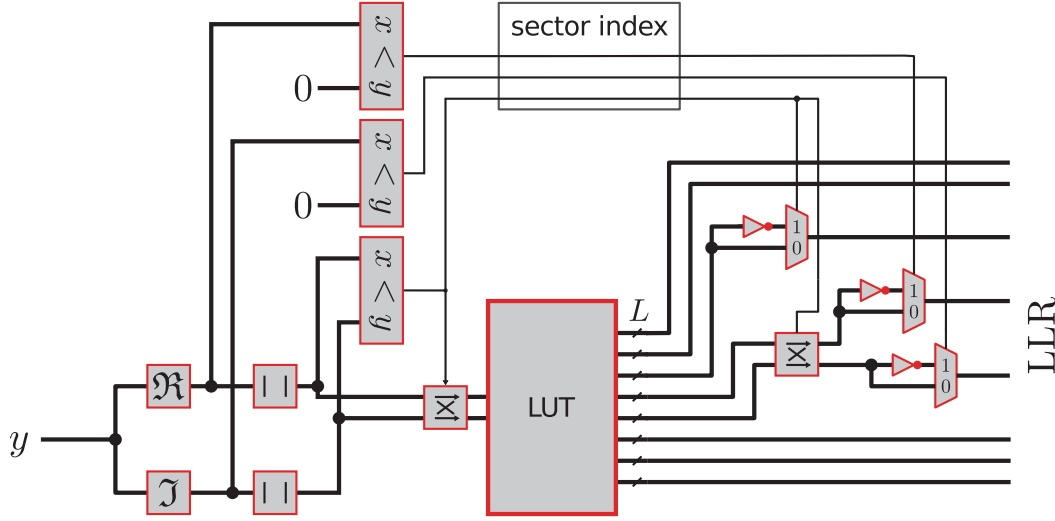


Figure 5.11 – LUT-based soft-decision demodulator optimized for the Meric APSK256 constellation.

to  $D$  in each dimension such that,

$$y \in \{\mathbb{CZ} | (|\Re\{y\}| \leq D) \wedge (|\Im\{y\}| \leq D)\}. \quad (5.13)$$

With such input symbols a full LUT would require  $(2D + 1)^2$  entries. The optimized LUT stores only the values for which holds that,

$$y \in \{\mathbb{CZ} | (0 \leq \Re\{y\} \leq D) \wedge (0 \leq \Im\{y\} \leq \Re\{y\})\}, \quad (5.14)$$

which results in  $\frac{1}{2}((D + 1)^2 + D + 1)$  entries. Unlike other proposed simplified APSK soft-decision demodulator this scheme provides the full max-log performance and does not entail any additional approximation loss.

There are two options for implementing the LUT, either using an static random access memory (SRAM) macro or with hard-wired combinatorial logic. While the use of SRAM allows reconfiguration for different constellations it has the inherent disadvantage that the address range is not continuous because of the limitation that  $0 \leq \Im\{y\} \leq \Re\{y\}$ . Accordingly, an SRAM needs either to be over-provisioned to  $(R + 1)^2$  entries to allow the use of the absolute values of real and imaginary part as addresses or needs an additional address encoder. On the other hand with a combinatorial described LUT the unused entries can be designated “don’t care”. Consequently the synthesis tool can leverage the gaps in the address range for optimization and it can also take advantage of redundancy in the output values, as often multiple input values lead to same LLR output. A combinatorial solution is further beneficial for the generally challenging physical implementation of high-speed mmWave systems. Pipelining allows nearly arbitrary clock speeds and the increased placement flexibility reduces critical interconnect overhead.

| Input | Full-LUT | Reduced-LUT | Reduction |
|-------|----------|-------------|-----------|
| 10bit | 15932 GE | 3830 GE     | 76%       |
| 12bit | 42927 GE | 11032 GE    | 74%       |

Table 5.1 – Complexity comparison of LUT-based soft-decision demodulator for APSK256 with and without symmetry optimization synthesized in 40 nm CMOS at 1 GHz clock speed.

Because of these advantages a combinatorial solution was chosen.

For comparison two soft-decision demodulator designs, one with a full and one with the proposed optimized LUT are implemented in hardware description language (HDL). Both design are synthesized for a typical mmWave scenario in a 40 nm CMOS process with a target clock frequency of 1 GHz, which matches the synthesis requirements for the IEEE 802.11ad baseband design presented in Section 2.5. The high clock speed ensures that the increased critical path of the optimized LUT design is correctly taken into account. A problem of the LUT based approach is that the actual size grows exponentially with the precision of the input samples. Hence, the synthesis was performed for 10 bit and 12 bit input sizes and a typical LLR size of 6 Bit. The results of the synthesis are provided in Tbl. 5.1. The optimized LUT achieves an area reduction of around 75 % compared to a full LUT implementation. The absolute complexity requirements of 3.8 kGE for 10 bit and 11 kGE for 12 bit are reasonable compared to the typical area requirements of mmWave baseband such as the one discussed in Section 2.5.

The performance of the proposed soft-decision demodulator might even be improved beyond max-log performance. Leveraging the flexibility of the value pre-calculation the look-up table can be populated with a linearized version of the exact LLR values, which further reduces the performance gap to exact LLRs.

### 5.3 Polar Coding for APSK

The discussion of information-driven modulation is directly related to the discussion of error correction coding. The suggested AMI measure reports the amount of conveyed information in an abstract way only. For practical communication purposes the partly erroneous LLR sequence needs to be transformed into an error-free bit sequence (with a reduced length).

Error correction coding (also called channel coding) is used in addition to the modulation to provide error free end-to-end data transfer. As discussed in Section 2.1.3 the IEEE 802.11ad standard relies on LDPC codes with very short code-words. For high-modulation order back-haul links more powerful codes are required to leverage the full potential of APSK. In this work the recently emerged class of Polar codes is investigated for coding. The good error correction capabilities and a fine-grained selection of the rate make polar codes an interesting candidate for applications that try to maximize the throughput. Additionally polar codes have interesting rate adaption properties that make them especially suitable for efficient performance

evaluations in experimental setups.

### 5.3.1 Optimal Code-Rate

The introduction of coding in the system brings the fundamental question at what code-rate  $R$  a system should be operated. It is obvious that the code-rate needs to be equal or smaller than the AMI of the LLRs. It can only be extracted as much error-free data from the demodulated LLR as information is contained in them.

There exist infinite many different combinations of modulation order and code-rate which result in the same net throughput. This poses the question which configuration achieves the maximal throughput. In theory, asymptotically capacity achieving modulations, such as the one from Meric, should be operated at a very high modulation order with a very low rate code and very long code-words in order to maximize the throughput. Obviously with increasing modulation order also the necessary baseband complexity also rises and therefore there is a practical implementation limit on the usable modulation order. Additionally there is the previously discussed PAPR problem that implies that infinitely high modulation orders also require infinite dynamic range.

The aforementioned AMI per symbol can be used to provide insight into the optimal operation point for practical modulation orders at each SNR point. Figure 5.12 shows the AMI per symbol for different modulation orders. A pareto-optimal operating system would need to select the modulation order with the highest AMI per symbol for each SNR point and adjust the coding rate accordingly. From the comparison of QAM modulations in Fig. 5.12a it can be seen that at around 17 dB SNR such an optimal system would switch between QAM64 and QAM256 at an effective spectral efficiency of 5.2 bits/symbol. This corresponds to a coding rate of  $\frac{5.2}{6} = 0.86$  for QAM64 and  $\frac{5.2}{8} = 0.65$  for QAM256. The optimal switching point between QAM256 and QAM1024 is around 23.5 dB with rates of  $\frac{7.3}{8} = 0.91$  and  $\frac{7.3}{10} = 0.73$  respectively. So the optimal coding rate regime for QAM systems would be roughly between  $\frac{2}{3}$  and  $\frac{9}{10}$ .

The symbol-AMI of APSK modulation shown in Fig. 5.12b suggests that its thresholds are at distinctively lower SNR. An optimal APSK system would switch between the modulations already at 14.9 dB and 20.6 dB with corresponding lower coding rates. The optimal coding rate regime for APSK seems to be more situated between  $\frac{6}{10}$  and  $\frac{8}{10}$ . This confirms the initial assumption that shaped constellation rely more on the interaction with coding compared to classical equi-distant constellations.

### 5.3.2 Introduction to Polar Codes

Polar Codes are a relatively new coding scheme proposed by Arikan [153] based on an effect called channel polarization. Arikan observed that with increasing block sizes bits undergoing polar coding can be partitioned into two sets. While one set is becoming completely corrupted by the noise of the channel, the other set is completely noise-free. This effect can be used



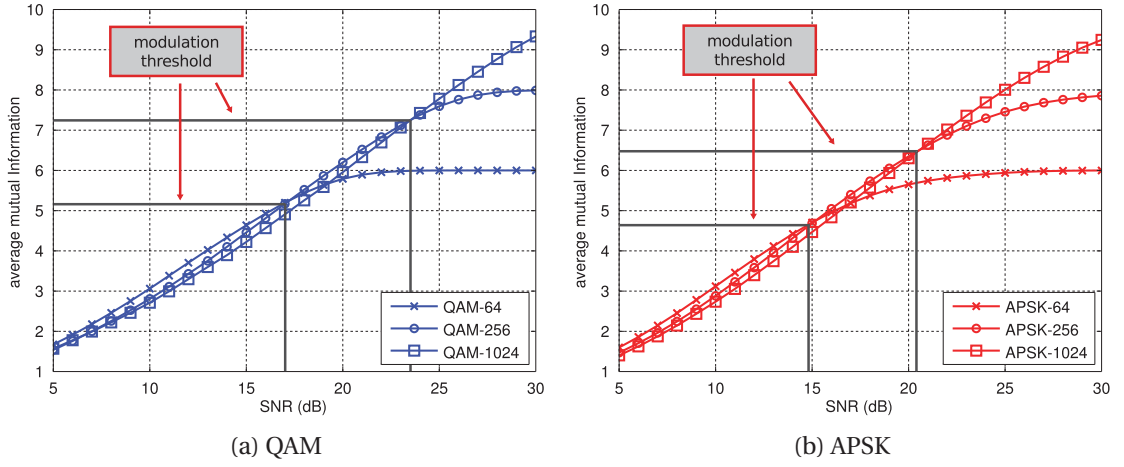


Figure 5.12 – Comparison of the average mutual information per symbol for different modulation orders with the switching thresholds for pareto-optimal operation indicated in grey.

for channel coding in the following way. The information is assigned to the noise-free bit positions, all other bits are fixed. In most cases the fixed bits, which are also called frozen bits, are set to zero, but in general they can be set to any value, the only condition is that their values are known at the receiver. The bit vector is encoded to a code-word using a generic polar encoder and passed through a channel. The corrupted code-word is afterwards reconstructed by the polar decoder. Because of the polarization feature the bit positions which carry the information are perfectly reconstructed, while the complementary bit positions are completely distorted. Polar codes have been proven to be asymptotically capacity achieving for some channel models assuming infinitely large block sizes.

For finite length block sizes the polarization effect can still be used for channel coding. In order to determine which bits should carry the information reliability value, the Bhattacharyya parameter, is calculated for each bit position. The frozen bits are determined based on the rate and their associated reliability values. For a code with rate  $R$  and code-word size  $N$  the frozen set is chosen to be the  $(1 - R)N$  least reliable output bits. The reliability order of the bits can be determined either analytically from the channel statistics or empirically by Monte-Carlo simulations. A polar code is fully defined by the reliability order of the bits and the code-rate.

For symmetrical binary channels the scheme shown in Fig. 5.13 can be used to determine the order of reliability values. The all zero code-word is BPSK modulated and transmitted through the channel for which the code should be trained for. Afterwards the symbols are demodulated and the resulting LLRs are passed to a polar decoder in which all bits are known to the receiver. The LLR outputs of the decoder are accumulated over multiple simulations and sorted to determine the order of the bits.

While the order of bits is independent of the used rate it is sensitive to the channel conditions. Hence, the precise order of the bits is dependent on the SNR and a code is always generated for a specific SNR point only. This poses the interesting question, namely what SNR point a

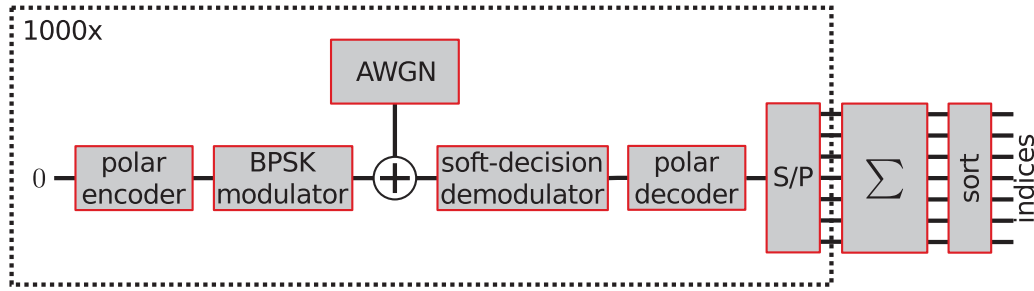


Figure 5.13 – Experimental method to derive reliability order of bit positions using Monte-Carlo simulations

code should be designed or whether the system should use different codes in different SNR regimes. Nevertheless in practical systems this is usually not a problem because reliability values of bits are not decreasing. This happens because, a bit which is good at a low SNR will not accumulate more noise at a higher SNR, just some other bits might become even better. As a result practical polar codes are trained for the waterfall region of the target rate. Consequently polar codes are indirectly again depending on the code-rate.

### 5.3.3 High-Modulation Order Trained Polar Codes

In the analysis of typical polar codes it is assumed that all input LLRs exhibit the same distribution. This is obviously not correct for LLRs which are demodulated from high-order constellations with  $M > 2$ . Depending on the bit position within each symbol the demodulated LLRs have a very different reliability. One solution which was suggested in [154] is to use  $M$  parallel code-words each specifically adapted to the position within the symbol. While such a procedure is helpful for theoretical analysis, it is not very suitable for high-speed implementation. Parallel code-words either require the buffering of the  $M$  code-words or a modulation dependent number of parallel en- and decoders. Both solutions lead to a significant increase in latency.

The possibility of adapting the code structure to the different LLR distributions in order to get a decoding improvement was already shown for irregular LDPC codes in [155]. However, with LDPC only a very limited set of degrees of freedom could be used for the adaptation to the modulation. Polar codes have the interesting property that the frozen set can be determined empirically. Hence, a very structured and powerful method is available to find a suitable code for a specific modulation. We propose a method to derive polar codes for the suggested APSK constellations based on Monte-Carlo simulations. The scheme described in Subsection 5.3.2 can be extended to work with high-modulation orders that exhibit demodulated LLRs with very different reliability distributions as depicted in Fig. 5.14. The all zero code-word used in the original scheme is scrambled using a random sequence and afterwards mapped to the high-order APSK symbols. The scrambling ensures that all-zero code-word maps to all

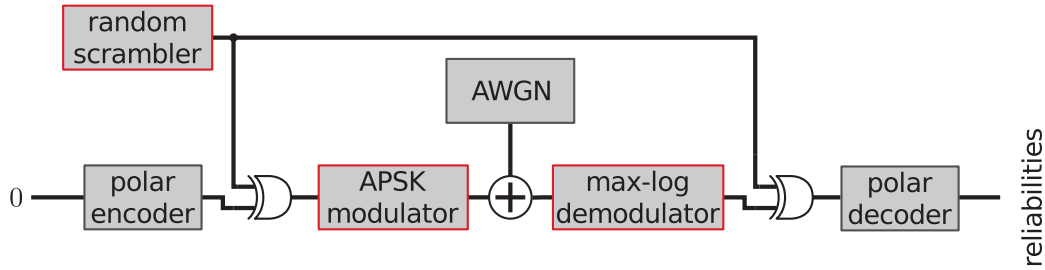


Figure 5.14 – Setup for high modulation order training of APSK codes with random scrambling.

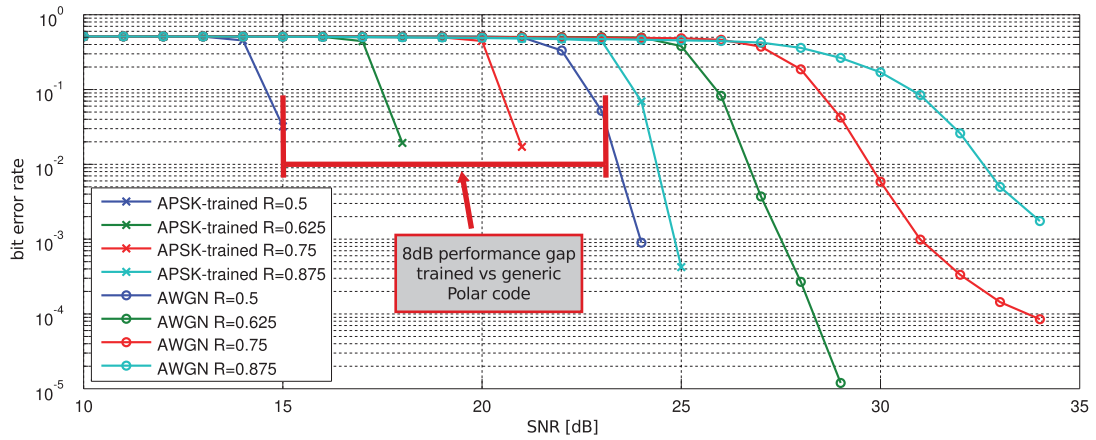


Figure 5.15 – Comparison BER of polar codes specifically trained for APSK256 constellation and polar codes trained for a generic AWGN channel at different coding rates.

possible symbols and hence, the LLRs exhibit a specific distribution based on what position it is within a symbol. After noise is added to the symbols a max-log soft-decision demodulator calculates LLRs which are unscrambled by the same random sequence. The unscrambled sequence is used in a polar decoder to generate bit reliability values in the same way as in the scheme for binary AWGN channels.

Special care has to be taken when polar codes trained for high-modulation order are used in a frame compiled of multiple code-words. In general it is not guaranteed that the code-word boundaries will align with the symbol boundaries. The relative assignment of bits in the code-word to bits in the symbol can change, and therefore its distribution. In such a case random bit padding is added to the end of each code-word to ensure that the following code-word starts with a new symbol.

Polar codes trained specifically for a modulation scheme achieve a significantly better performance compared to polar codes that were designed for the generic AWGN channel with equal reliability of the individual bits in a constellation. Figure 5.15 shows a performance comparison between polar codes trained for the specific constellation and polar codes which

have been trained for a generic AWGN channel. Both type of codes shown in Fig. 5.15 have been evaluated at the rates  $\frac{1}{2}$ ,  $\frac{5}{8}$ ,  $\frac{3}{4}$  and  $\frac{7}{8}$ . Training the polar codes for the specific constellation achieves approximately 8 dB better BER performance. It can be further seen that the training is especially crucial for higher rates, as in this regime the generic polar codes exhibit a significantly slower BER decay.

### 5.3.4 Multi-Rate Polar Code Evaluation

The way how polar codes work provides an interesting property, which allows to speed up experimental testbed measurements significantly. Experimental measurements are compared to numerical simulations rather slow due to the reprogramming of the testbed hardware requires significantly more time, then the baseband signal processing operations. Another problem is that the experiment can not be easily parallelized. Hence, it is always beneficial when acquired measurement data can be used in multiple different contexts.

Polar codes allow transmission to be performed without the need to set the rate beforehand. For a code-word size  $N$  every random generated sequence of  $N$  bits is a valid code-word for an arbitrary rate given that the values of the frozen set can be arbitrarily chosen. This allows the evaluation of arbitrary many data rates using a single acquired data sample set. A precondition for this scheme is that transmitter and receiver have a sidechannel to communicate the values of the frozen bits. While this is not a viable strategy for a real communication scenario it does speed up experimental measurements significantly and is in terms of coding performance equivalent to a frozen bit set which is fixed to zero.

The successive interference cancellation based decoder described in [156] can be readily extended to accept a frozen bit set with arbitrary fixed value. Hence, for the multi-rate measurement procedure a frame of multiple code-words is transmitted. Each code-word is a sequence of random bits of length  $N$  that is known at the receiver. Initially the receiver demodulates the frame to a series of LLRs completely agnostic to the intended rate. The same sequence of LLRs can now be evaluated multiple times with different rates in the polar decoder. For each rate the framework provides the polar decoder with the indices and values of the frozen set at the target rate. The non-frozen bits are then used to evaluate the resulting bit-error-rate after decoding.

As outlined before the set of frozen bits should not be a function of the current SNR, but only of the code-rate. Hence, choosing the best frozen bits set for each rate is an optimization problem, which could be solved for each target rate on it own. For each rate the waterfall region is iteratively determined. The polar code is trained based on an initial assumption of the position of the waterfall region, afterwards the code is used for BER simulation. If the waterfall of the simulated BER is different from the initially assumed waterfall region, the code is regenerated according to the new assumption. This procedure is repeated until the waterfall region stops moving to a lower SNR. Unfortunately such a procedure significantly impairs the flexibility of the polar codes in our research environment, as the process needs to be performed

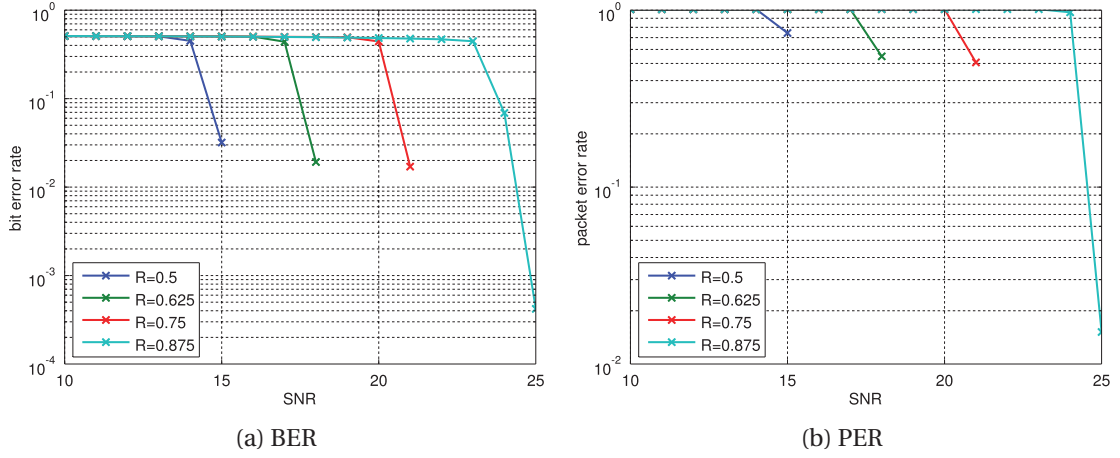


Figure 5.16 – Numerical multi-rate simulation of an APSK256 constellation in a mmWave LOS channel with polar coding based on 2000 simulated frames. The code-rates have been chosen to always result in integer bits for the spectral efficiency.

for each used rate. Hence, a more flexible simplified scheme is used for the simulations. The frozen bit sets are pre-generated for a regular grid of SNR points. From rate and the modulation order a target spectral efficiency is calculated. Based on the spectral efficiency the minimal required SNR can be calculated from the Shannon Capacity (see Appendix A.1). This allows to set choose a frozen bit set purely from the rate and the modulation order. The results of a numerical multi-rate simulation of an APSK trained polar code are shown in Fig. 5.16. The packet error rate results confirm the very steep error rate decay of polar codes in this environment. Despite the fact that 2000 frames have been simulated per SNR point nearly no data points below  $0.5 \cdot 10^{-1}$  are captured. The problem of this simulation is that the SNR grid that was necessary to perform the simulation over a wide SNR range was too coarse to properly capture the steep slope of the packet error rate. This finding underlines the importance to precisely adjust the rate to the operating conditions in polar coded systems.

In the testbed the multi-rate approach significantly reduces the time required for a BER and PER measurements. The time required for a single complete measurement and for a block-RX measurement with 10 frames are listed in Tbl. 5.2. When comparing the results with the single rate measurement times in Tbl. 4.2 we can see that the average time for the measurement of one frame with one rate can be reduced from 14 s to 5 s seconds for a short frame and from 24 s to 8 s seconds for a long frame. Hence combining block-RX mode and multi-rate code evaluation reduces the average time required to evaluate one frame at a single rate from 72 s to only 8 s.

Multi-rate simulations allow BER and PER results for multiple configurations (with different spectral efficiency) to be generated with a single set of measurements. Hence, this technique is well suited for comparisons between different modulation orders. In Fig. 5.17 the BER and PER of different APSK256 and APSK1024 configurations with the same spectral efficiency are

| Frame | single rate       |                     |  | multi rate         |                      |  | Reduction |
|-------|-------------------|---------------------|--|--------------------|----------------------|--|-----------|
|       | 1 frame<br>1 rate | 10 frames<br>1 rate | $\frac{\text{time}}{(\text{frame} \cdot \text{rate})}$ | 1 frame<br>4 rates | 10 frames<br>4 rates | $\frac{\text{time}}{(\text{frame} \cdot \text{rate})}$ |           |
| Short | 46 s              | 143 s               | <b>14 s</b>  | 46 s               | 178 s                | <b>5 s</b>   | 64%       |
| Long  | 72 s              | 240 s               | <b>24 s</b>  | 81 s               | 334 s                | <b>8 s</b>   | 66%       |

Table 5.2 – Multi-rate testbed measurements for single and block-RX mode with 4 rates. (The frame parameters are identical to the one used for Tbl. 4.2)

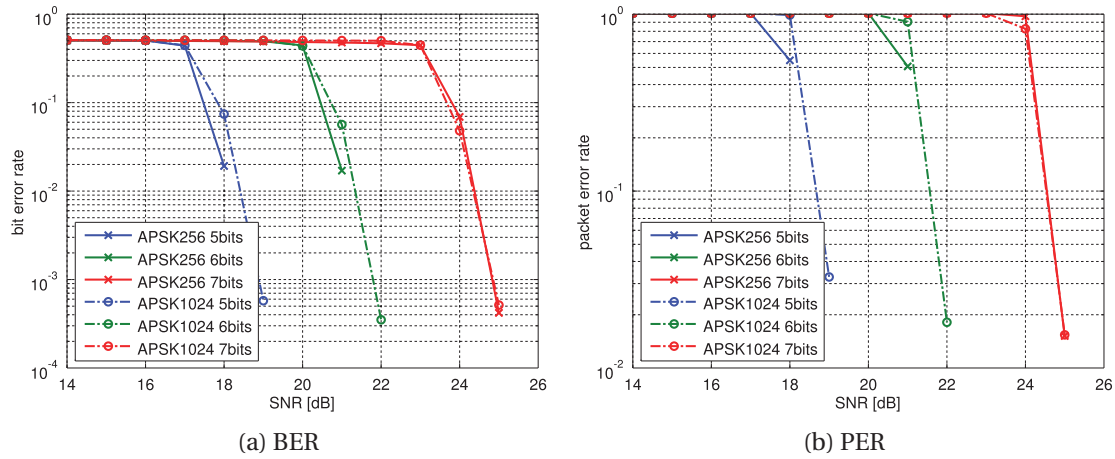


Figure 5.17 – Comparison of APSK256 and APSK1024 configurations with the same spectral efficiency.

compared. Using multi-rate simulation such a comparison requires only a single simulation run per modulation. For a spectral efficiency of 5-6 bits/symbol the APSK256 has small but visible advantage, while for 7 bits/symbol APSK1024 seems to perform slightly better. This is consistent with the modulation thresholds derived from the MI in Fig. 5.12.

## 5.4 APSK-Polar Codes Testbed Measurements

The numerical simulations show a clear advantage for APSK modulation compared to more traditional QAM. However, numerical simulations have the problem that they can not perfectly emulate all non-ideal effects of a real transceiver chain. Usually this problem is mitigated by using the link only in such a regime that the influence of all effects are not modeled are negligible in the final results. The measurements are taken in a directed LOS link setup as it would be expected for such a high-rate application. For the measurement the distance between the TX and RX was about 0.5 m because of constraints of the facilities. This distance is significantly less than in the expected scenario, nevertheless the required adjustment to the output power and antenna gains are not expected to substantially change the behavior of the link.

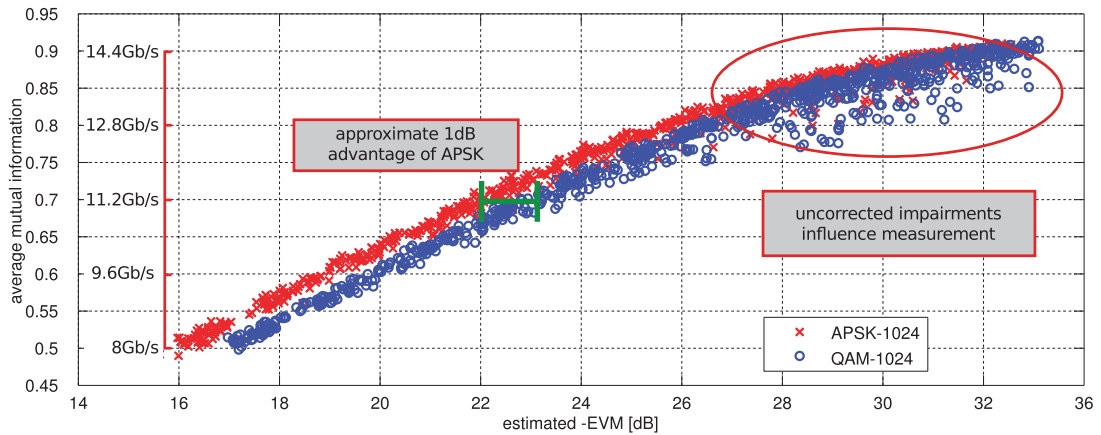


Figure 5.18 – AMI comparison between APSK1024 and QAM1024 modulations on the hardware testbed with a symbol rate of 1.6 GHz.

### 5.4.1 Average Mutual Information on the Testbed

AMI measurements of 1024-ary modulations on the testbed are shown in Fig. 5.18. Each point is the average mutual information per LLR of a transmitted frame as a function of the estimated signal quality. As explained in Appendix A.2 we reserve the use of the term SNR exclusively for the ratio between signal energy and a clearly defined thermal noise. In order to allow easy comparison with the results from the numerical simulations we define here the term of negative error vector magnitude (-EVM), which can be used in the same way as the SNR but indicates that various other impairments can be included. The absolute value of the estimated negative EVM is derived from the statistics of the raw samples, adjusted by an empirically derived offset that corrects the effect of impairment compensation. The precise value of the offset is not of significance as long as the same value is used for all measurements in the same measurement campaign and a comparison is only made between measurement of the same campaign. An additional scale on the left side translates the AMI to the net achievable throughput based on the modulation order and the symbol rate of 1.6 GHz, e.g. an AMI of 0.6 would translate to a spectral efficiency of 6 bits/s and results in a achievable net throughput of 9.6 Gb/s.

The AMI comparison in Fig. 5.18 shows that the testbed measurements confirm the results of the simulation and APSK modulation offers a clear AMI advantage to QAM. The spread for different measurements at the same -EVM point are low, showing not only that the testbed delivers very reproducible results but also that the transmitted frames are sufficiently long to reliably calculate the AMI. For SNR above 28 dB we can see that the variations between measurements increase. While the majority of measurements follow the predicted curve, there are some outliers which exhibit a significantly lower AMI then expected. This can be explained with transmission impairments which are either not captured or not fully corrected by the baseband signal processing. In fact closer analysis indicates that this error term is dominated by secondary effects introduced by the phase noise.



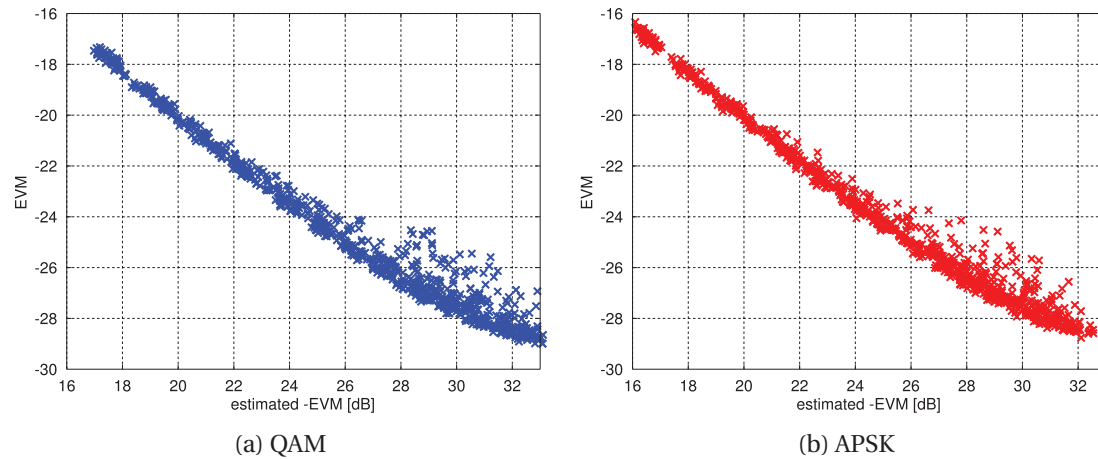


Figure 5.19 – Comparison of estimated -EVM and measured post-equalization EVM.

In order to demonstrate that the AMI advantage of APSK results from the inner structure of the modulation, the quality of the received signal can be analyzed. Based on the received symbols an RX post-equalization EVM is calculated and put into relation to the estimated -EVM. It is important to note the difference between the two quantities, the estimated -EVM is blindly calculated from the statistics of the ADC samples, while the EVM is calculated from the equalized symbols after the complete baseband signal processing and with knowledge of the transmitted data. In an ideal system with thermal noise only, the relation between the two quantities would be perfectly inverse and independent of the modulation. A difference between APSK and QAM modulation would indicate that the modulations are affected differently by the signal processing. The comparison in Fig. 5.19 shows that both modulations exhibit the same post-equalization EVM and any advantage results from the statistic of the modulation itself.

The data points of Fig. 5.18 can be used to fit AMI curves for the two modulations. A comparison of the fitted AMI curves is depicted in Fig. 5.20. The comparison shows that APSK modulation exhibits a consistent advantage of 1 dB to QAM over most of the operational range. At an operating -EVM of 21 dB this would translate to a theoretical 7% increase in the net throughput for APSK.

### 5.4.2 Error Rate Measurements on the Testbed

The 1 dB advantage for the AMI can not be directly translated into an equivalent advantage for BER and PER because of the fluctuations in code quality and the different averaging. The AMI is calculated from the statistics of a complete frame while the coding requires the same or a higher AMI averaged over the distance of a code-word. Due to the code-word being significantly smaller than the frame length, error rates are sensitive to variations within the frame. A single failed code-word will impact significantly the overall error rate of the frame. It was discussed before that the quality of the used code can vary depending on the code-word



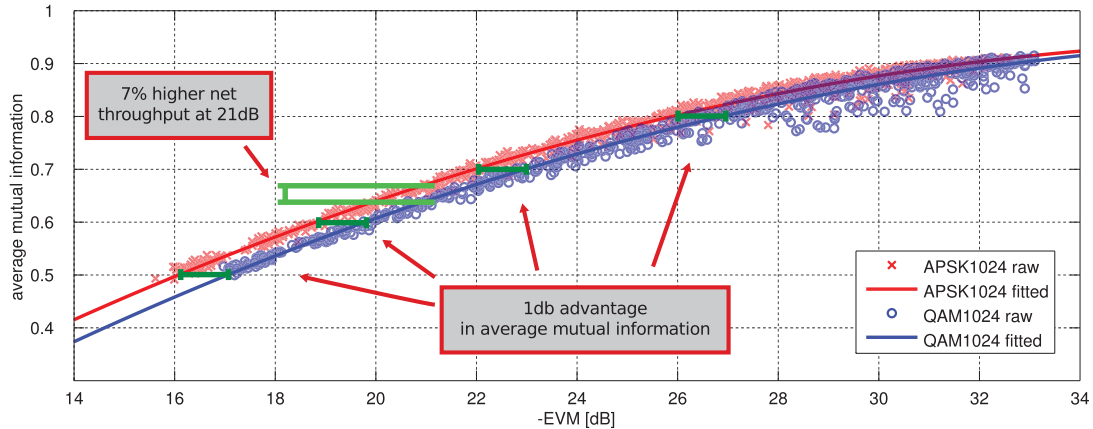


Figure 5.20 – Testbed AMI comparison between APSK1024 and QAM1024 modulations with fitted curves.

size, the rate and the modulation for which it was generated.

For the multi-rate BER comparisons of APSK and QAM shown in Fig. 5.21a the advantage of APSK can still be observed. For a spectral efficiency of 5-7 bits/symbol the APSK modulation exhibits a similar 1 dB advantage over QAM. For higher rates the testbed operates at the edge of its operation regime and results are already affected by impairments.

The plot of the corresponding PER comparison in Fig. 5.21b is not very conclusive as not enough measurements are available. In order to get a reliable PER comparison a new measurement campaign is performed over a reduced power range for a single rate only. This campaign with APSK1024 and a  $R = \frac{1}{2}$  polar code has measure 4000 frames and hence allows significantly more measurement points for every -EVM point. Hence, the BER and PER comparison in Fig. 5.22 show a noticable smoother behaviour. The more detailed PER curve shows the expected 1 dB advantage of APSK modulation.

## 5.5 Summary

Most current wireless systems accept a significant performance penalty due to the choice of highly-unoptimal QAM modulation. While alternatives to QAM have long been known only recently have shaped constellation been considered for practical systems e.g., for satellite communication. The class of APSK constellations suggested by Meric was shown to achieve asymptotic capacity. Though the capacity-achieving property was shown purely based on the distribution of an infinite sized constellation, it was not shown how much gain could be achieved in a practical system.

Numerical simulations show that also LLR-mapped Meric constellations with finite alphabet size can perform significantly better than QAM. To measure the effectiveness of modulation

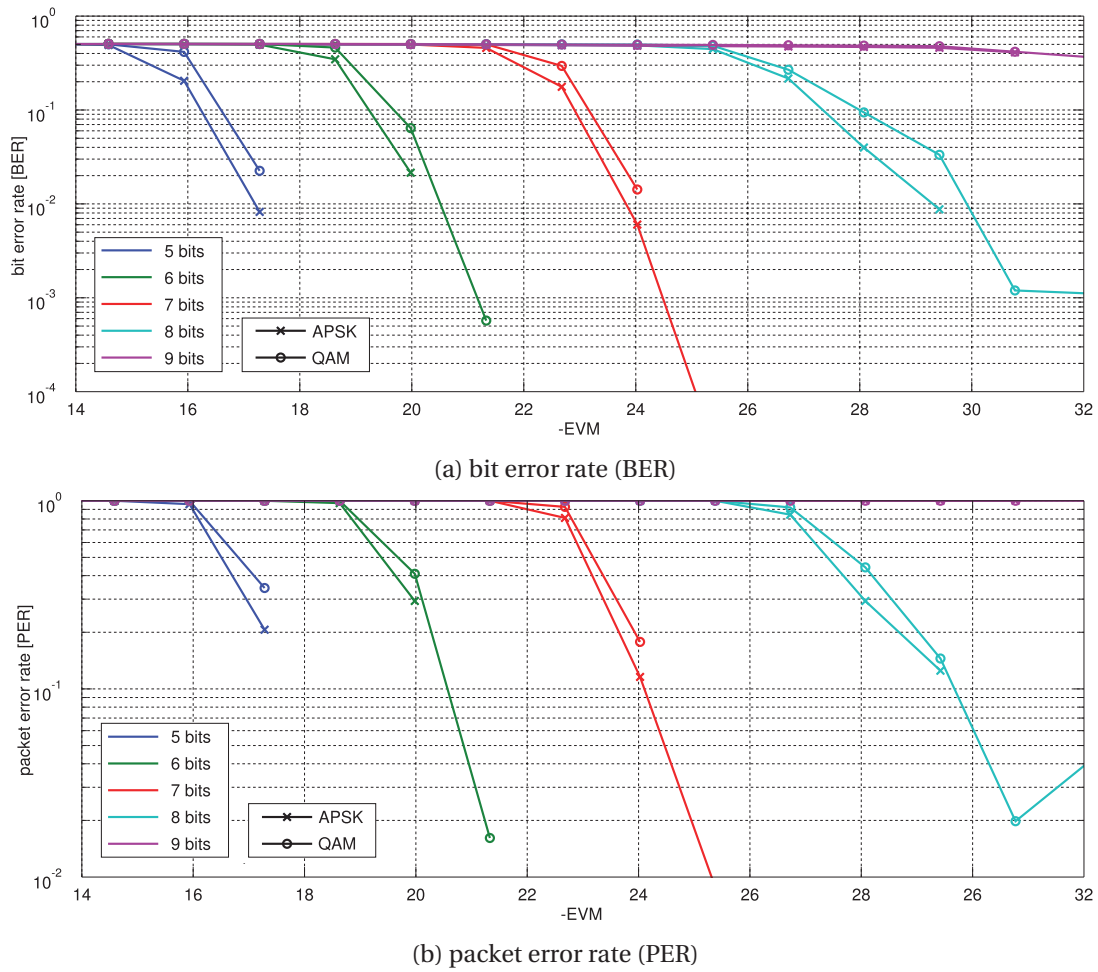


Figure 5.21 – BER and PER multirate testbed measurements of APSK1024 and QAM1024 modulation with polar codes for 1500 measurement points per modulation.

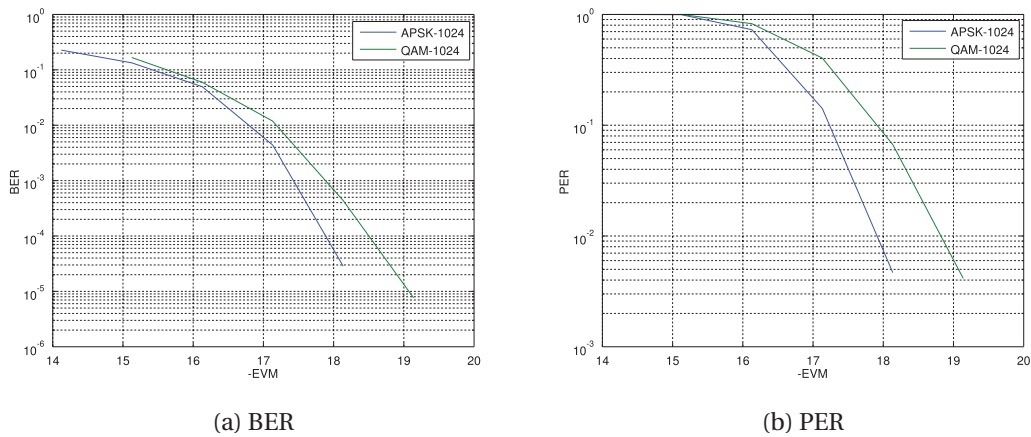


Figure 5.22 – Measurement over a reduced power range with APSK1024 and a  $R = \frac{1}{2}$  polar code.

without requiring any assumptions about the coding, the average mutual information is suggested as a measure of the received signal quality. AMI simulations show that APSK, even with finite constellation sizes, can leverage approximately 1 dB of the possible 1.53 dB gain compared to equidistant modulations without increasing the PAPR.

Soft-decision demodulation complexity is often the biggest concern about the use of non standard modulation schemes. Implementation results show that LUT-based implementations allow soft-decision demodulation with 16-42 kGE complexity, which is modest compared to the overall system complexity. The complexity can be further reduced to 4-11 kGE when the constellation exhibits some symmetry.

The use of polar codes to exploit the AMI advantage of APSK modulations is investigated. Polar codes are especially appealing for testbed measurement campaigns, as the rate can be chosen on the receiver side after the transmission. This property allows efficient multi-rate evaluation which can reduce the required time per measurement significantly.

It is a specialty of polar codes, that their structure heavily depends on the channel, therefore they need to be especially crafted for the used modulation. Using such trained polar codes with high order APSK modulations allows to translate the 1 dB AMI advantage also in an BER and PER advantage. This advantage can not only be demonstrated in numerical simulations but is also observed in testbed measurements. It could be demonstrated that shaped modulations are not only technical feasible for receiver implementations, but also provide a significant gain in spectral efficiency.

More research is needed to identify the impact of LLR quantization on the decoding performance. Another interesting question for future research is whether hardware impairments have an influence on optimal code construction and whether a gain can be achieved by training the polar codes with testbed data.



## 6 Summary and Conclusions

In this thesis the challenges and opportunities of mmWave receiver and system design have been investigated. The large channel bandwidths and the high carrier frequencies of mmWave systems require new ways to think about the design space of receiver architectures. The high symbol rate leads not only to extremely varying excess delay spread due to multipath, it also entails strong frequency-selectivity and non-idealities in the analog receiver chain. Signal processing architectures for mmWave need to cope with worst-case conditions for reliable operations, while at the same time energy efficiency is key for the use in battery-limited mobile applications.

Single-carrier mmWave transmission offers a wide range of design options from low-power, short delay spread time-domain (TD) to powerful but power-expensive frequency-domain (FD) processing. Starting from the intended usage scenario, mmWave design needs to take all parts of the PHY layer into account, from parameter synchronization to channel coding.

The synchronization scheme proposed in this thesis adapts known synchronization techniques to the specific requirements of mmWave communication. The higher flexibility allows to operate under more channel conditions and to improve the overall system efficiency. A reconfigurable packet detection offers the possibility to trade synchronization performance for receiver power consumption, the register activity can be reduced by 40 % and more. System efficiency is maximized by putting emphasis on the synchronization methods which can be efficiently implemented for a mmWave receiver. A discrete step sampling phase optimization is a technique that allows to improve the system performance of symbol-spaced receivers by more than 0.5 dB with little additional complexity. The challenging problem of precise time synchronization is addressed with a flexible two-step synchronization strategy, that can trade initial time synchronization precision for the computationally cheaper channel estimation. Knowledge about the equalization architecture in the synchronization unit is used to maximize the overall system performance.

It is shown, that single carrier frequency-domain equalization (SC-FDE) provides not only very good equalization but also allows efficient integration of additional baseband signal

processing. SC-FDE-based baseband architectures can choose for each baseband task the more suitable domain. In the presented architecture digital sampling frequency offset compensation, sample point alignment, matched filtering, and decimation can be efficiently performed as part of the frequency domain processing, while time and frequency estimation, phase noise compensation, and channel estimation are more efficiently performed in the TD. This flexibility combined with excellent equalization capabilities make SC-FDE a versatile and efficient all-digital baseband architecture, which is especially suited for applications that require a high level of flexibility, e.g., SDR, Testbeds, etc. Nevertheless, conventional SC-FDE suffers from the disadvantage that its complexity is constant and can not adapt to the channel conditions.

Energy proportional frequency domain equalization (EP-FDE) is proposed as a novel extension to SC-FDE and makes a first step towards a combination of powerful FD and energy-proportional TD equalization capabilities. EP-FDE uses a dual mode frequency domain equalization structure that can switch between a perfectly circular cyclic-prefix and a sub-optimal overlap-save frequency domain equalization mode in order to reduce the equalization block length and therefore the complexity per symbol. The architecture provides a way to achieve excellent equalization capabilities under frequency-selective channel conditions, while still allowing complexity reduction in benign channel conditions with short delay spread.

Reduced state sequence estimation (RSSE) algorithms offer the capability to set the performance of a TD receiver between optimal maximum likelihood (ML) performance and low-complexity decision feedback equalization to find a trade-off between complexity and performance. A high-speed RSSE architecture for mmWave based on the delayed decision feedback sequences estimation (DDFSE) algorithm is presented. DDFSE achieves state reduction by truncating the CIR used for sequence estimation, the remaining inter-symbol interference is canceled by a decision feedback equalizer. Operation reordering, speculative calculation and retiming allow to achieve the necessary clock speeds despite the decision feedback constraint. The proposed DDFSE architecture operates on a trellis of three channel taps combined with a 26 taps decision feedback equalizer (DFE), which allows selective deactivation of taps for power saving based on the delay spread. The detector requires 656 kGE for a synthesis clock speed of 1.1 GHz.

A dual DDFSE core is used as detector in an IEEE 802.11ad all-digital baseband ASIC design which includes synchronization, channel estimation, DDFSE detection and LDPC error decoding. The 2.6 MGE design was fabricated in 40 nm CMOS and processes a IEEE 802.11ad compliant frame structure with a symbol rate of 1.76 Gs/s. The system complexity is dominated by the DDFSE detectors which consume 68 % of the baseband complexity, the LDPC decoder uses 17 % and synchronization 10 %. The remainder of the complexity is required for control logic, clock- and reset-trees and interface buffering. The design demonstrates the feasibility of sequence estimation for mmWave systems.

A new proposed receiver architecture based on complex sub-sampling offers a low-complexity

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alternative to the commonly used heterodyne architecture for wideband mmWave receivers. Complex sub-sampling overcomes the strict frequency-planning constraints of real-valued sub-sampling receivers and combines the design advantages of heterodyne receivers with the low-complexity of direction-conversion receivers. The advantages of complex sub-sampling come at the cost of a single additional passive 3 dB hybrid coupler. The coupler is used to generate an analytic signal in the analog domain, which allows an arbitrary placement of the IF. Without further measures the performance of complex sub-sampling receivers depends strongly on the precision of the employed coupler. For a demonstrated hardware setup it is shown that non-idealities of the couplers limit the received EVM of the complex sub-sampling receiver to -12 dB. With digital equalization the complex sub-sampling receiver achieves a high linearity better than -30 dB EVM. Furthermore, the coupler compensation can be integrated into the existing frequency-domain baseband signal processing with a complexity overhead of less than 10 %.

New modulation schemes can improve the spectral efficiency of high-throughput mmWave links, making them a promising technology for next-generation cellular front- and backhaul-applications. Amplitude phase shift keying (APSK) allows to construct constellations that are asymptotically capacity achieving, contrary to traditional rectangular and equidistant quadrature amplitude modulation (QAM). Using the average mutual information (AMI) as metric APSK constellations can achieve approximately 1 dB of gain compared to QAM constellations. This gain can not only be shown in numerical simulations, but also on the testbed hardware for real-world transmissions. For practical systems, the AMI advantage can only be exploited using soft-information from the demodulator and a suitable coding scheme.

The novel class of polar codes can be used to transform the demodulated soft information into an error free data stream. Polar codes have the special property that their construction depends heavily on the characteristics of the transmission channel. In order to take full advantage of the increased AMI of APSK constellation, the polar codes are trained for a specific modulation constellation alphabet. This training allows the 1 dB AMI advantage of APSK over QAM to be reflected in lower bit-error rate and packet-error rate after decoding. Additionally polar codes provide a convenient way to select the code-rate after the transmission, if side channel communication is available. This property allows significant time savings in experimental testbed setups, as every physical transmission can be evaluated for many different rates.

In order to demonstrate the feasibility of the complex sub-sampling architecture for high-throughput mmWave applications an FPGA-based 60 GHz testbed based on commercially available components was engineered. The testbed was used to verify the proposed baseband algorithms for synchronization and SC-FDE equalization, as well as the mutual information optimized APSK modulation schemes. The testbed operates with 1024-ary modulation and symbol rates of up to 1.6 GS/s, resulting in an uncoded throughput of 16 Gb/s.





# A Appendix

## A.1 Gaussian Channel Capacity

Assuming a signal with power  $S$  affected by white Gaussian noise with noise spectral density  $\frac{N_0}{2}$ . For a bandwidth  $B$  the Gaussian channel capacity, also known as the Shannon-Hartley theorem, is stated [157] as

$$C = B \log_2 \left( 1 + \frac{S}{BN_0} \right) \quad (\text{A.1})$$

and given in bits per second. The important insight of this formula is that the capacity of the channel grows linearly with the bandwidth but only logarithmically with the SNR for high SNR.

The Gaussian channel capacity formula can be used to calculate the minimal possible SNR as a function of the spectral efficiency  $b = C/B$  as

$$\text{SNR}[b] = 2^b - 1. \quad (\text{A.2})$$

The required SNR in decibel for those integer values of  $b$  which are of practical use in our environment are:

| bits/symbol | SNR [dB] |
|-------------|----------|
| 1           | 0        |
| 2           | 4.77     |
| 3           | 8.45     |
| 4           | 11.76    |
| 5           | 14.91    |
| 6           | 18.00    |
| 7           | 21.04    |
| 8           | 24.07    |
| 9           | 27.08    |

## A.2 SNR and EVM Definition

The signal-noise-ratio (SNR) is used in this work exclusively to express the relation between the power of the signal and the thermal noise. Hence we assume that noise is always a white Gaussian random process for the bandwidth of interest. Assuming a signal with power  $S = \text{Var}(\mathbf{s})$  affected by noise with noise spectral density  $\frac{N_0}{2}$  and bandwidth  $B$ . The noise energy  $\sigma_n^2$  is given as  $\sigma_n^2 = \text{Var}(\mathbf{n}) = 2B \frac{N_0}{2}$ . The SNR is then defined as

$$\text{SNR} = \frac{S}{2B \cdot N_0/2} \quad (\text{A.3})$$

$$= \frac{S}{\sigma_n^2} \quad (\text{A.4})$$

$$= \frac{\text{Var}(\mathbf{s})}{\text{Var}(\mathbf{w})} \quad (\text{A.5})$$

and expressed in decibel

$$\text{SNR}_{\text{dB}} = 10 \log_{10} \text{SNR}. \quad (\text{A.6})$$

In most cases out side of simulation environments the received signal is affected by more then just thermal noise. This effects are often covered by extension of the SNR term to e.g. signal-to-interference-and-noise ration (SINR) or signal-to-jitter-noise ratio (SJNR). Such a naming scheme allows only to cover a limited number of effects and gets very quickly unhandy.

The EVM is introduced to quantize the ratio between the total deviation of the received symbol from its ideal position and the average power. Such a measure is calculated from the power of the error between the equalized symbols  $\hat{\mathbf{s}}$  and the transmitted signal  $\mathbf{s}$  as

$$\text{EVM}_{\text{dB}} = 10 \log_{10} \left( \frac{\sum_{k=0}^{N-1} |\hat{s}_k - s_k|^2}{N \cdot \text{Var}(\mathbf{s})} \right), \quad (\text{A.7})$$

which sums up all impairment effects without the need to identify every single one.

The relation between the EVM and the SNR is inverse. In a pure thermal noise scenario it holds that

$$\text{EVM}_{\text{dB}} = -\text{SNR}_{\text{dB}}. \quad (\text{A.8})$$

## A.3 Log-Likelihood Ratio (LLR)

The log-likelihood ratio is a measure for the probability of a certain bit in the transmitted symbol. For a modulation order  $m$  a bit vector  $\mathbf{b} = [b_0, \dots, b_{m-1}]$  is mapped to a symbol  $s$  from the constellation alphabet  $\mathcal{S}$  with cardinality  $M = 2^m$ . The transmitted symbol  $s$  is affected by

a noise term  $n$  such that only the corrupted version

$$r = s + n \quad (\text{A.9})$$

can be observed. A soft-decision demodulator uses  $r$  to perform probability estimates for  $\mathbf{b}$ . Then the LLR of the  $i$ -th bit  $b_i$  of  $s$  is calculated as

$$L_i = \ln \left( \frac{p(b_i = 1|r)}{p(b_i = 0|r)} \right) \quad (\text{A.10})$$

$$= \ln(p(b_i = 1|r)) - \ln(p(b_i = 0|r)). \quad (\text{A.11})$$

From the set of all symbols  $\mathcal{S}$  we define the two mutual exclusive subsets  $\mathcal{S}_i^{(1)}$  and  $\mathcal{S}_i^{(0)}$  of all those symbols for which the  $i$ -th bit is 1 and 0 respectively. Assuming equiprobable symbols and applying Bayes' theorem the two probabilities required for the LLR can be calculated as

$$p(b_i = 1|r) = \sum_{\hat{s} \in \mathcal{S}_i^{(1)}} p(r|s = \hat{s}) \quad (\text{A.12})$$

and

$$p(b_i = 0|r) = \sum_{\hat{s} \in \mathcal{S}_i^{(0)}} p(r|s = \hat{s}). \quad (\text{A.13})$$

The calculation of  $p(r|s)$  requires assumption about the statistic of the noise component  $n$ .

In the case of the noise being white and normally distributed with variance  $\sigma_w^2$  the probability can be found as

$$p(r|s = \hat{s}) = \frac{-1}{\sigma_w^2 \pi} e^{\frac{-1}{\sigma_w^2} |r - \hat{s}|^2}. \quad (\text{A.14})$$

The exact value of  $L_i$  is calculated as

$$L_i = \ln \left( \frac{1}{\sigma_w^2 \pi} \sum_{\hat{s} \in \mathcal{S}_i^{(1)}} \left( e^{\frac{-1}{\sigma_w^2} |r - \hat{s}|^2} \right) \right) - \ln \left( \frac{1}{\sigma_w^2 \pi} \sum_{\hat{s} \in \mathcal{S}_i^{(0)}} \left( e^{\frac{-1}{\sigma_w^2} |r - \hat{s}|^2} \right) \right) \quad (\text{A.15})$$

$$= \ln \left( \sum_{\hat{s} \in \mathcal{S}_i^{(1)}} e^{\frac{-1}{\sigma_w^2} |r - \hat{s}|^2} \right) - \ln \left( \sum_{\hat{s} \in \mathcal{S}_i^{(0)}} e^{\frac{-1}{\sigma_w^2} |r - \hat{s}|^2} \right). \quad (\text{A.16})$$

This calculation entails a high computational complexity because it requires the calculation of all distances from the received symbol to every constellation point. This means the complexity is exponentially increasing with the modulation order. Hence online computation of exact LLR values is usually infeasible for high modulation orders.

Using precalculated values is also problematic due to the noise dependency  $\frac{-1}{\sigma_w^2}$  of the exponent. Correct calculation would require a set of values for each possible SNR point.

## A.4 Max-Log Log-Likelihood Ratio (max-log LLR)

The exact LLR calculation is relaxed using the “max-log” approximation which brings a significant reduction in complexity and entails only a small penalty in performance. The approximation is based on the observation that the sum of exponentials is dominated by the largest exponent or

$$\sum_i e^{x_i} \approx e^{\max_i(x_i)}. \quad (\text{A.17})$$

With this approximation the LLR of the  $i$ -th bit is calculated based on the two closest symbols for which the bit of interest has opposing values.

This approximation simplifies (A.16) into

$$L_i = \ln \left( e^{\frac{-1}{\sigma_w^2} \min_{\hat{s} \in \mathcal{S}_i^{(1)}} (|r - \hat{s}|)^2} \right) - \ln \left( e^{\frac{-1}{\sigma_w^2} \min_{\hat{s} \in \mathcal{S}_i^{(0)}} (|r - \hat{s}|)^2} \right) \quad (\text{A.18})$$

$$= \frac{-1}{\sigma_w^2} \left( \min_{\hat{s} \in \mathcal{S}_i^{(1)}} (|r - \hat{s}|)^2 - \min_{\hat{s} \in \mathcal{S}_i^{(0)}} (|r - \hat{s}|)^2 \right). \quad (\text{A.19})$$

The max-log LLR approximations comes with two significant advantages compared to the exact LLR calculation. First of all, the number of required distance calculations is reduced to two independent of the used modulation order. Second the LLR is linear with the noise variance allowing to pre-calculate an SNR independent value that can be adjusted to the current noise condition if required.

## A.5 Average Mutual Information (AMI)

The mutual information for two random variables  $X$  and  $Y$  is according to [157] defined as

$$I(X; Y) = \sum_{x,y} p(x, y) \log_2 \frac{p(x, y)}{p(x)p(y)} \quad (\text{A.20})$$

$$= - \sum_{x,y} p(x, y) \log_2 p(x) + \sum_{x,y} p(x, y) \log_2 p(x|y) \quad (\text{A.21})$$

$$= - \sum_x p(x) \log_2 p(x) - \left( - \sum_{x,y} p(x, y) \log_2 p(x|y) \right) \quad (\text{A.22})$$

$$= H(X) - H(X|Y). \quad (\text{A.23})$$

with  $H(X)$  being the entropy defined as

$$H(X) = - \sum_x p(x) \log_2 p(x). \quad (\text{A.24})$$

Hence the mutual information is defined as the reduction in entropy of the variable  $X$  due to the observation of  $Y$ .

The average mutual information (AMI) is calculated per sequence of the bits from the distribution of the resulting LLRs. A bit vector  $\mathbf{b} = [b_0, \dots, b_{N-1}]$  of length  $N$  is modulated and soft demodulated to an LLR vector  $\mathbf{L} = [L_0, \dots, L_{N-1}]$ . Each LLR  $L_i$  is assigned to one of two mutual exclusive sets  $\mathcal{L}^{(0)}$  and  $\mathcal{L}^{(1)}$  based on whether its corresponding bit  $b_i$  equals 0 or 1. Two discrete distributions  $p_{L0}[k]$  and  $p_{L1}[k]$  for  $k = 0, \dots, K-1$  are obtained for each of the two sets by sorting the LLRs in  $K$  equally spaced bins and normalization with the number of elements of the set. With  $p_b(b=0)$  being the probability that  $b=0$  the AMI can be calculated as

$$I(\mathbf{b}, \mathbf{L}) = \sum_{k=0, \dots, K-1} p_b(b=0) p_{L0}[k] \log_2 \frac{p_{L0}[k]}{p_b(b=0) p_{L0}[k] + p_b(b=1) p_{L1}[k]} \quad (\text{A.25})$$

$$+ \sum_{k=0, \dots, K-1} p_b(b=1) p_{L1}[k] \log_2 \frac{p_{L1}[k]}{p_b(b=0) p_{L0}[k] + p_b(b=1) p_{L1}[k]}. \quad (\text{A.26})$$

In MATLAB code the mutual information can be calculated as follows:

```

1 function [ I ] = ami(LLR, bits)
2
3 Kbins = 100;
4 maxval = max(abs(LLR));
5 range = linspace(-maxval, maxval, Kbins);
6
7 L1 = LLR( logical(bits));
8 L0 = LLR(~logical(bits));
9
10 dist1 = hist(L1, range);
11 dist0 = hist(L0, range);
12
13 p1 = dist1/length(L1);
14 p0 = dist0/length(L0);
15
16 b1 = length(L1) / length(LLR);
17 b0 = length(L0) / length(LLR);
18
19 psum1 = b1 * p1 .* log2 ( p1 ./ (b0*p0 + b1*p1) );
20 psum1(p1 == 0) = 0;
21
22 psum0 = b0 * p0 .* log2 ( p0 ./ (b0*p0 + b1*p1) );
23 psum0(p0 == 0) = 0;
24
25 I = sum ( psum0 ) + sum ( psum1 ) ;
26
27 end

```



# Acronyms

## A

**ACS** add-compare-select.

**ADC** analog-to-digital converter.

**AMI** average mutual information.

**APSK** amplitude phase-shift keying.

**ASIC** application-specific integrated circuit.

**AWG** arbitrary waveform generator.

## B

**B[I]CM** bit (-interleaved) coded modulation.

**BER** bit error rate.

**BF** beam-forming.

**BM** branch metric.

**BPF** band-pass filter.

**BPSK** binary phase-shift keying.

## C

**CB** cubicle office.

**CE** channel estimation.

**CEF** channel estimation field.

**CFO** carrier frequency offset.

**CH** common history.

## Acronyms

---

**CHF** common history feedback.

**CIR** channel impulse response.

**CMPS** complex multiplications per data symbol.

**COMP** coordinated multi-point.

**COTS** commercial off-the-shelf.

**CP** cyclic prefix.

**CSI** channel state information.

### D

**DC** direct-conversion.

**DDFSE** delayed decision feedback sequence estimation.

**DDS** direct digital synthesis.

**DFE** decision feedback equalizer.

**DFT** discrete Fourier transform.

**DLL** delay-locked loop.

**DUT** device under test.

### E

**EBL** equalization block length.

**ENOB** effective number of bits.

**EP-FDE** energy-proportional frequency-domain equalization.

**-EVM** negative error vector magnitude.

### F

**FD** frequency-domain.

**FDE** frequency-domain equalization.

**FFT** fast Fourier transform.

**FIFO** first-in first-out.

**FO** frequency-offset.



**FPGA** field-programmable gate array.

**FSPL** free-space path loss.

## **G**

**Gs/s** giga-symbol per second.

**Gsps** giga-sample per second.

## **H**

**HDL** hardware description language.

**HDMI** high definition multimedia interface.

**HIL** hardware in the loop.

## **I**

**IF** intermediate frequency.

**ISH** individual state history.

**ISHF** individual state history feedback.

**ISI** inter-symbol interference.

**ISM** industrial, scientific, and medical.

## **L**

**LAN** local area network.

**LDPC** low-density parity check.

**LLR** log-likelihood ratio.

**LOS** line-of-sight.

**LTE** long term evolution.

**LTI** linear time-invariant.

**LUT** look-up table.

## **M**

**MF** matched filter.

**MIMO** multiple-input multiple-output.

## Acronyms

---

**ML** maximum-likelihood.

**MLSE** maximum-likelihood sequence estimation.

**MMSE** minimum mean-square error.

**MPIC** multi-path interference cancellation.

### N

**NF** noise figure.

**NLOS** non line-of-sight.

**NSMC** normalized separated maximum correlation.

### O

**OFDM** orthogonal frequency-division multiplexing.

**OS** overlap-save.

**OS-FDE** overlap-save frequency-domain equalization.

### P

**PA** power amplifier.

**PAM** pulse amplitude modulation.

**PAN** personal area network.

**PAPR** peak-to-average power ratio.

**PER** packet error rate.

**PHY** physical layer.

**PM** path metric.

**PN** phase-noise.

### Q

**QAM** quadrature amplitude modulation.

**QoS** quality of service.

**QPSK** quadrature phase-shift keying.

### R

**RC** raised cosine.

**RE** register exchange.

**RF** radio frequency.

**RMS** root mean-square.

**RRC** root raised cosine.

**RSSE** reduced state sequence estimation.

**RTL** register transfer level.

**RX** receive.

### S

**SC** single carrier.

**SC-FDE** single carrier frequency-domain equalization.

**SC-FDMA** single carrier frequency-division multiple access.

**SDMA** space-division multiple access.

**SFO** sampling frequency offset.

**SINR** signal-to-interference-and-noise ratio.

**SIR** signal-to-interference ratio.

**SNR** signal-to-noise ratio.

**SOVA** soft-output Viterbi algorithm.

**SRAM** static random access memory.

**STF** short training field.

**SVD** singular value decomposition.

### T

**tc** typical corner.

**TCP** transmission control protocol.

**TD** time-domain.

**TD-LE** time-domain linear equalizer.

## Acronyms

---

**TWT** traveling wave tube.

**TX** transmit.

**TXPS** transmit power setting.

### V

**VA** Viterbi algorithm.

**VLSI** very large scale integration.

### W

**WLAN** wireless local area network.

**WPAN** wireless personal area network.

### Z

**ZF** zero-forcing.

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## Publications

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Preyss, N., and Burg, A., "*Experimental Signal-Quality Characterization of a High-Capacity mmWave Link for Backhaul Applications*", IEEE Workshop on Sensor Array and Multichannel Signal Processing (SAM), Rio de Janeiro, 2016

Preyss, N., and Burg, A., "*Digital Synchronization for Symbol-Spaced IEEE 802.11ad Giga-bit mmWave Systems*", IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Cairo, 2015

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## Appendix A. Curriculum Vitae

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Preyss, N., Koestler, L., and Burg, A., "*Fractionally Spaced Complex Sub-Nyquist Sampling for Multi-Gigabit 60 GHz Wireless Communication*", IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS), Fort Collins, 2015 (2nd place, best student paper)

Preyss, N., Pantic, R. D., and Burg, A., "*Correlation Based Phase Noise Compensation in 60 GHz Wireless Systems*", IEEE 28th Convention of Electrical & Electronics Engineers in Israel (IEEEI), Eilat, 2014

Preyss, N., Studer, C., and Burg, A., "*Layered Detection and Decoding in MIMO Wireless Systems*", Conference on Design and Architectures for Signal and Image Processing (DASIP), Karlsruhe, 2012

### Co-authored publications

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Kail, G., Maechler, P., Preyss, N., and Burg, A., "*Robust Asynchronous Indoor Localization using LED Lighting*", IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), Florence, 2014

Constantin, J., Houlmann, R., Preyss, N., Walenta, N., Zbinden, H., and Burg, A., "*An FPGA-based secret key distillation engine for quantum key distribution systems*", The Journal of Signal Processing Systems, 2015, Springer

Balatsoukas-Stimming, A., Preyss, N., Cevrero, A., Burg, A., and Roth, C., "*A parallelized layered QC-LDPC decoder for IEEE 802.11ad*", IEEE 11th International New Circuits and Systems Conference (NEWCAS), Paris, 2013

Studer, C., Preyss, N., Roth, C., and Burg, A., "*Configurable High-Throughput Decoder Architecture for Quasi-Cyclic LDPC Codes*," Proceedings of the 42th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, Oct. 2008

