# Ultra Low-Power Frequency Synthesizers for Duty Cycled IoT radios

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ÉCOLE POLYTECHNIQUE
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குருவே சிவமெனக் கூறினன் நந்தி
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श्री गुरुणा पालितोऽस्मि ।
गुरुगुहादन्यं न जानेऽहं ।
श्री गुरुगुह मूर्ते शिष्य जनावन कीर्ते सुमुहूर्ते ।
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नो चेत् चिद्गुरुगुह एवाहम् ॥

*To the Eternal Teacher...*

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*Neuchâtel, December 2015* Raghavasimhan T

# Abstract

Internet of Things (IoT), which is one of the main talking points in the electronics industry today, consists of a number of highly miniaturized sensors and actuators which sense the physical environment around us and communicate that information to a central information hub for further processing. This agglomeration of miniaturized sensors helps the system to be deployed in previously impossible arenas such as healthcare (Body Area Networks - BAN), industrial automation, real-time monitoring environmental parameters and so on; thereby greatly improving the quality of life. Since the IoT devices are usually untethered, their energy sources are limited (typically battery powered or energy scavenging) and hence have to consume very low power. Today's IoT systems employ radios that use communication protocols like Bluetooth Smart; which means that they communicate at data rates of a few hundred kb/s to a few Mb/s while consuming around a few mW power. Even though the power dissipation of these radios have been decreasing steadily over the years, they seem to have reached a lower limit in the recent times. Hence, there is a need to explore other avenues to further reduce this dissipation so as to further improve the energy autonomy of the IoT node.

Duty cycling has emerged as a promising alternative in this sense since it involves radios transmitting very short bursts of data at high rates and being asleep the rest of the time. In addition, high data rates proffer the added advantage of reducing network congestion which has become a major problem in IoT owing to the increase in the number of sensor nodes as well as the volume of data they send. But, as the average power (energy) dissipated decreases due to duty cycling, the energy overhead associated with the start-up phase of the radio becomes comparable with the former. Therefore, in order to take full advantage of duty cycling, the radio should be capable of being turned ON/OFF almost instantaneously. Furthermore, the radio of the future should also be able to support easy frequency hopping to improve the system efficiency from an interference point of view. In other words, in addition to high data rate capability, the next generation radios must also be highly agile and have a low energy overhead. All these factors viz. data rate, agility and overhead are mainly dependent on the radio's frequency synthesizer and therefore emphasis needs to be laid on developing new synthesizer architectures which are also amenable to technology scaling. This thesis deals with the evolution of such a frequency synthesizer; with each step dealing with one of the aforementioned issues, the culmination of which is a Phase Domain Direct Digital Synthesizer.

The start-up overhead in a loop based synthesizer has two sources viz. start-up of the crystal oscillator (XO) reference and the loop settling time. The latter depends on the bandwidth of the loop which, ultimately is constrained by the Quantization Noise (QN) of the $\Sigma\Delta$

Modulator (SDM). This noise also leads to higher in-band PLL noise due to noise folding within the loop bandwidth as a result of charge pump nonlinearities. Addressing this issue of QN noise, a Phase Switching Divider (PSD) with a division ratio step of 0.2 is implemented in a PLL prototype. This five-fold reduction in the division ratio step size (Multi-modulus dividers usually have a step size of 1) leads to a reduction in the QN which is measured to be 14 dB.

While the SDM QN reduction improves the synthesizer settling, the large energy overhead due to the XO wake up still persists. Therefore, there is a need to find a high-Q alternative to the XO with a much faster wake up. Film Bulk Acoustic Wave Resonators (FBAR), a class of high-Q MEMS resonators, satisfy this criteria. Their intrinsic Q-factors range from 500-2000 and the oscillators using them can wake up in a few $\mu s$. They are high frequency references (1 - 7 GHz) and thus can be used to build loop-free frequency synthesizers. But due to the frequency stability of the temperature compensated FBAR, wide frequency tuning of the synthesizer is extremely difficult. To circumvent the issue, the stable FBAR local oscillator (LO) signal is divided using the aforementioned PSD (division ratio step of 0.2) to produce an Intermediate Frequency (IF) signal. This IF signal is then upconverted to RF by the LO signal using a Gilbert cell mixer. The use of the PSD makes the synthesizer capable of generating frequencies from 2.36 to 2.5 GHz. Integrated along with a linearized class-C PA in a Transmitter (TX), this synthesizer supports FSK at data rates as high as 16 Mb/s as well as QPSK at 1.2 Mb/s. Thanks to the near instantaneous start up of the synthesizer at 5 $\mu s$, the TX gains a 34 fold reduction in the energy overhead as compared to a State-of-the-Art TX with a XO reference. Furthermore, the frequency agility of the synthesizer permits channel switching within just 3 $\mu s$.

Even though the above synthesizer has very low overhead and can achieve high data rates, the presence of an analog mixer makes it somewhat inimical to technology scaling. Scaling friendly Direct Digital Synthesizers (DDS) have been demonstrated in the literature to be extremely frequency agile, but at the cost of high power consumption. Yet, the principle of DDS can be modified to use the information about the phase instead of the amplitude information to build the desired RF signal. In combination with the fast start up of the FBAR, such a synthesizer could potentially satisfy all the criteria needed to be used in next generation radios; in terms of energy overhead, data rate, agility, scaling and power. The principle of the proposed synthesizer involves generating various phases of an LO signal from an FBAR oscillator by injection locking it to a ring oscillator and combining these phases based on the outputs of a $\Sigma\Delta$ Modulator (SDM) to get the desired output frequency. Direct modulation can then be performed on this synthesizer by varying the SDM input. A prototype of this synthesizer has been integrated within a TX system which outputs up to 3 dBm power. Measurement results show that the synthesizer has a rapid start up of about 1.5 $\mu s$ (subsequently low energy overhead) as expected thanks to the FBAR. The TX supports a peak data rate of 51.4 Mb/s which is the highest reported for narrowband synthesizers, with a potential to increase as high as 80 Mb/s. In addition, its frequency agility and fully digital nature makes it an ideal candidate to be used in next generation radios for IoT applications.

Key words: ULP; IoT; WMNs; Duty cycling; Quantization Noise; MEMS; FBAR; fast start up; frequency agility; Loop-free Synthesizers; Phase Domain DDS.

# Résumé

Aujourd'hui, l'internet des objets (IoT) constitue un tournant dans l'univers de l'industrie électronique. Il se compose d'un réseau de nombreux capteurs et actionneurs miniatures détectant les paramètres physiques de notre entourage et communiquant ces informations à des centres d'informations pour des traitements intelligents. Cet ensemble de capteurs miniatures a permis d'intégrer l'IoT dans des environnements où cela était jusqu'à présent impossible, dans l'ultime but d'améliorer la qualité de vie, comme dans le domaine du réseau personnel de la santé (BAN), l'automatisme industriel, contrôle en temps réel des paramètres d'environnement, etc. Etant donné que les composants de l'IoT sont généralement des objets connectés sans fil, ils doivent répondre à des exigences strictes en termes de consommation énergétique, à cause de leurs sources de puissance constituées principalement de piles ou de systèmes de captage d'énergie. Les objets IoT utilisent aujourd'hui des systèmes radio fondés sur des protocoles à faible consommation comme « Bluetooth Smart ». Cela signifie qu'ils communiquent à des débits de l'ordre de quelques centaines de kb/s à quelques Mb/s tout en consommant quelques mW de puissance. La consommation des systèmes radio a remarquablement diminué ces dernières années. Toutefois cette diminution semble avoir ralenti récemment. Il est donc nécessaire de réduire encore cette consommation afin d'améliorer l'autonomie énergétique des nœuds IoT.

L'introduction d'un rapport cyclique dans les radios apparaît comme une alternative prometteuse. Cela implique la transmission de paquets (*bursts*) de données à haut débit sur des laps de temps courts (mode actif) et le passage en veille le reste du temps. La congestion des réseaux IoT est devenue aussi un problème majeur à cause de la multiplication des capteurs augmentant significativement le volume des données communiquées. Le haut débit dans cette technique a aussi l'avantage de permettre une réduction de la congestion des réseaux IoT. Malgré ces avantages, la technique du rapport cyclique peut devenir non pertinente dans le cas d'un fonctionnement à très haut débit où l'énergie dissipée pour passer entre le mode actif et le mode veille devient comparable à l'énergie nécessaire pour la transmission des données. Il est alors nécessaire d'établir le passage entre les deux modes de façon instantanée pour profiter de cette technique. En outre, les systèmes radio du futur doivent permettre des sauts de fréquence instantanés pour une meilleure immunité contre les interférences. En d'autres termes, les systèmes radio doivent être agiles lors des sauts de fréquence en dissipant un minimum d'énergie lors du redémarrage tout en assurant des hauts débits. L'ensemble de ces éléments, à savoir, le haut débit, l'agilité, et l'énergie dissipée lors des redémarrages, dépend principalement du synthétiseur de fréquence de la radio. Par conséquent, les efforts

doivent être concentrés sur le développement de nouvelles architectures pour les synthétiseurs, qui doivent, entre autres, être compatibles avec la miniaturisation technologique. Cette thèse est consacrée à l'étude de synthétiseurs répondant aux critères précédemment cités afin d'aboutir à un synthétiseur numérique dans le domaine de phase (*Phase Domain Direct Digital Synthesizer*).

L'énergie dissipée lors du démarrage de la boucle PLL a deux origines : la première est l'allumage de l'oscillateur à cristal (XO) et la deuxième, la stabilisation de la boucle PLL. Cette dernière dépend de la bande passante de la boucle contrainte par le bruit de quantification du modulateur ΣΔ modulateur (SDM). Ce bruit est par ailleurs replié sur la bande passante de la PLL à cause de la non-linéarité de la pompe de charge. Afin de traiter ce problème de bruit de quantification, un diviseur à commutation de phase (PSD) doté d'un pas de division de 0,2 est implémenté dans un prototype de PLL. Cette diminution par 5 du pas du diviseur de la PLL (par rapport au pas usuel de 1) conduit à la réduction du bruit de quantification par 14 dB.

Alors que la réduction du bruit de quantification améliore la stabilisation du synthétiseur, l'énergie dissipée durant le démarrage de l'oscillateur à cristal demeure considérable. Il faut donc trouver une alternative à haut facteur de qualité et à démarrage rapide pour remplacer l'oscillateur à cristal. Les résonateurs à onde acoustique de volume (FBAR), connu pour leur haut facteur de qualité, répondent à ce critère. Leur facteur de qualité varie entre 500 et 2000 et les oscillateurs disposés sur ces éléments peuvent s'allumer en moins d'une µs. Ces oscillateurs constituent des références pour hautes fréquences (1-7 GHz) et peuvent donc être utilisés pour concevoir des synthétiseurs sans boucle. Toutefois, ces oscillateurs montrent une stabilité fréquentielle importante, après compensation thermique, rendant la variation de fréquence très difficile. Afin de contourner ce problème, l'oscillateur local (LO) disposé sur le FBAR stable est utilisé avec le PSD mentionné précédemment dont le pas de division est de 0,2, pour générer la fréquence intermédiaire (IF). Ce signal est ensuite converti en RF par le biais du LO. L'utilisation de la PSD permet au synthétiseur de générer des fréquences entre 2,36 et 2,5 GHz. Ce synthétiseur a été intégré, avec un amplificateur de puissance linéarisé de classe C (PA), dans le transmetteur (TX). Ce synthétiseur supporte une modulation FSK jusqu'à un débit de 16 Mo/s, et une modulation QPSK s'élevant à 1,2 Mo/s. Grâce au démarrage presque instantané du synthétiseur autour de 5 µs, l'énergie dissipée lors de cette phase est réduite d'un facteur 34, en comparaison avec l'état de l'art des TX avec une référence XO. En outre, la souplesse fréquentielle de ce synthétiseur permet le changement de la chaîne fréquentielle en moins de 3 µs.

Malgré le démarrage rapide de ce synthétiseur et le fait qu'il permette d'atteindre des hauts débits, la présence du mixeur analogique présente un obstacle pour la miniaturisation technologique. Des synthétiseurs numériques (DDS), compatibles avec la miniaturisation technologique, ont fait leurs preuves dans la littérature technique. Ils présentent une bonne agilité fréquentielle, mais au prix d'une consommation énergétique importante. Toutefois, le principe du DDS peut être modifié en utilisant la phase au lieu de l'amplitude afin de générer le signal RF souhaité. En combinant ceci avec le démarrage rapide du FBAR, ce synthétiseur peut potentiellement satisfaire à tous les critères des radios futures pour : l'énergie dissipée lors de l'établissement, le débit, la souplesse fréquentielle, la miniaturisation et la consommation

de puissance. Le principe du synthétiseur proposé est fondé sur la génération de différentes phases du signal LO généré par le FBAR en le verrouillant par injection dans un oscillateur en anneau. Ensuite les phases sont combinées par l'intermédiaire d'un SDM pour obtenir la fréquence désirée. La modulation peut alors être implémentée par la variation de l'entrée du SDM. Un prototype de ce synthétiseur a été intégré dans un système TX émettant jusqu'à 3 dBm de puissance. Les mesures ont démontré la rapidité de son démarrage : moins de 1,5 µs (par conséquent, moins d'énergie dissipée lors du démarrage) grâce au FBAR, comme prévu. Le TX permet de monter jusqu'à 51,4 Mo/s de débit. Ce résultat devance tous les synthétiseurs à bande étroite présentés jusqu'à présent, avec en plus un potentiel d'augmentation jusqu'à 80 Mo/s. En plus, sa souplesse fréquentielle et son intégration numérique font de lui un candidat idéal pour les radios de génération future utilisées dans les applications IoT.

Mots clefs : ULP ; IoT ; WMNs ; Rapport cyclique ; Bruit de quantification ; MEMS ; FBAR ; Demarrage rapide ; Agilité de fréquence ; Synthétiseur sans boucle ; Synthétiseur numerique en Domaine de phase.

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# 1 Introduction

## 1.1 Motivation – Improving the energy autonomy of IoT nodes

There has been an explosion of connected devices in the past decade, with the number of these devices even surpassing the human population. The growth rate of these devices is expected to increase exponentially with about 50 billion devices expected to be deployed globally by the year 2020 as shown in figure 1.1 [1]. Looking at the breakdown of these connected devices, it can be seen from figure 1.2 [2] that indeed Internet of Things (IoT) is expected to be the major contributor to the expected exponential rise in the number of devices. The IoT consists of a number of miniature actuators and sensors that are capable of monitoring various aspects of the physical environment around us such as humidity, temperature etc. The information about these physical parameters are then communicated to a central information hub where further processing takes place. Since these IoT nodes are typically untethered, energy autonomy is one of the major requirements due to the energy sources being restricted to batteries or energy scavenging. Indeed, the IoT as well as Wearables for Wireless Body Area Networks (WBAN) are the major driving forces of the need for Ultra Low Power connected devices. Similar to IoTs, the WBAN also consists of a number of small, intelligent devices attached on or implanted in the body which are capable of establishing a wireless communication link. These devices provide continuous health monitoring and real-time feedback to the user or medical personnel [3] (Fig. 1.3 [4]). Like the IoT, there has been a rapid proliferation of the WBAN with almost 19 million of these units being sold worldwide in 2012. This figure is projected to go up further (Figure 1.4 [5]) with the WBANs becoming more and more ubiquitous due to the fact that they provide a low cost solution to continuous real time monitoring of the physiological parameters of patients. In essence, WBANs serve to alleviate the pressure on the already under-staffed healthcare systems [6] which are struggling to deal with an increase in the incidence of Non communicable diseases (NCD) [7] and an ageing global population [8].

In addition to the aforementioned requirements of Ultra Low Power and a high degree of miniaturization which are similar to IoT nodes, due to the implantable nature of devices, the WBAN also has an unique set of requirements which are summarized below:

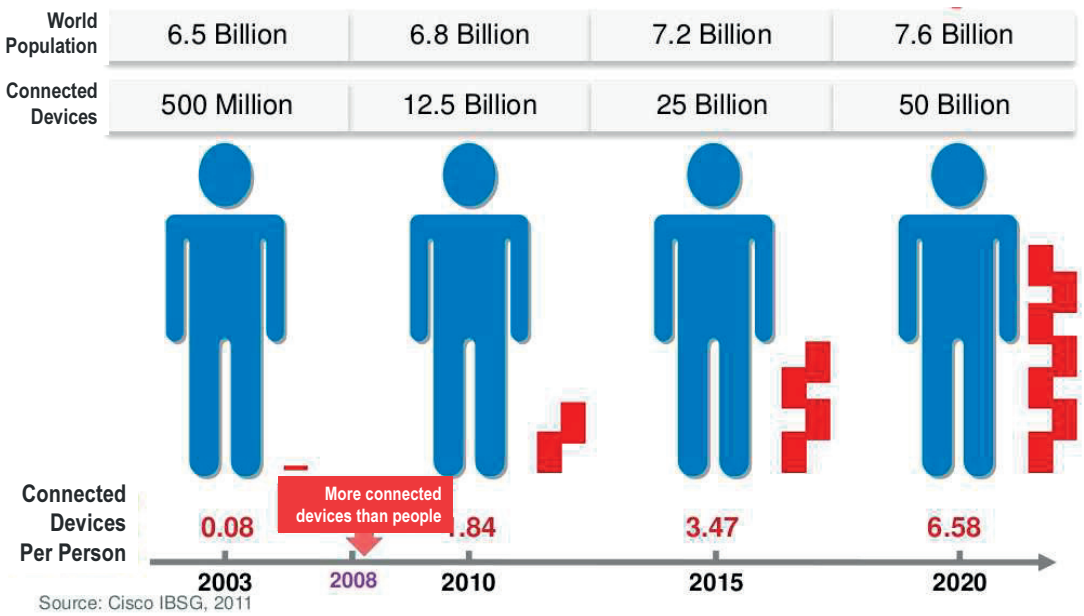


Figure 1.1 – Global Proliferation of Connected Devices

- They should have low output power to avoid any potential health concerns.
- The communication in some of these nodes which involve implantable devices occur through the human body which is a lossy medium which should be taken into consideration. Moreover, the fact that the human body may be in motion should also be taken into account.
- Finally, strict security mechanisms are needed to ensure confidentiality of the patient's data.

## 1.2 Reduction of energy dissipation - Duty cycling

Keeping in line with the limited availability of energy sources, reducing the power consumption of the nodes, be it IoT or WBAN, is paramount. In these systems, the main power sink is the radio which is required to communicate with the data collection hub. Typically, these radios use the traditional low power communication protocols like Bluetooth Smart wherein they communicate at data rates of a few hundred kb/s to a few Mb/s. These protocols are ill suited for duty cycled systems due to their long in-built latency and thus specific protocols such as WiseMAC need to be used [9]. In addition, the radios using the traditional protocols consume a few mW of power for operation. But even these power dissipation figures are very high for a battery powered IoT node. To illustrate this point, let a hypothetical ultra low powered radio that requires only 10 µW for nominal operation be utilized by the IoT node. If such a radio uses a CR2032 button cell battery (20 mm diameter and 3.2 mm thickness which amounts to around 1 $cm^3$) providing 225 mAh as an energy source, the battery life time can be calculated

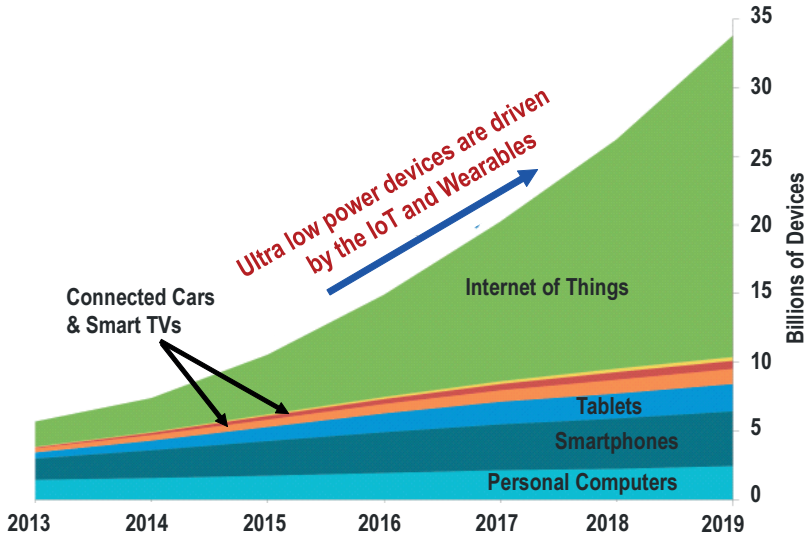


Figure 1.2 – Breakdown of Connected devices - Data and Projection

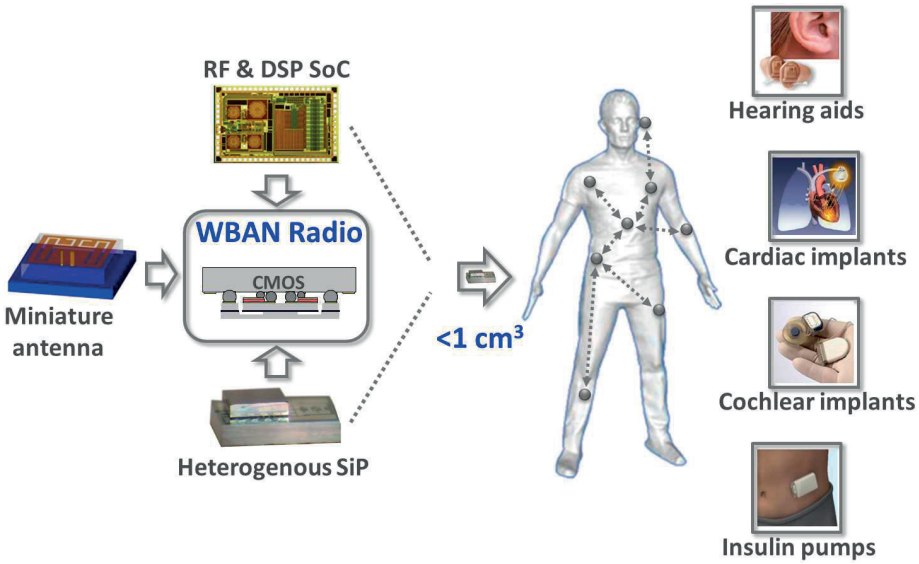


Figure 1.3 – A typical WBAN system [4]

to be around 2.5 years. In case of further miniaturization of the battery, this lifetime will decrease even further as in the case when a V335 battery providing 5 mAh is used for the same radio. This battery is expected to last only 20 days with the radio consuming 10 µW of power. On top of this, the power dissipation of the conventional radios used in the IoT nodes has saturated over the recent years. This is illustrated in figure 1.5 which shows that the power consumption figures of a the Bluetooth Smart radios published in the past few years in the literature are around 5 mW [10], [11], [12], [13], [14], [15], [16], [17].

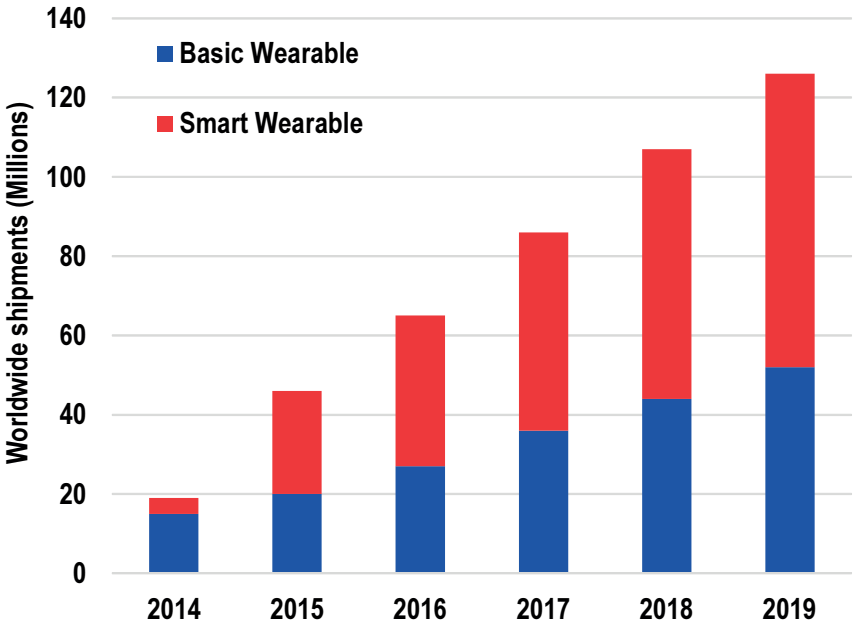


Figure 1.4 – Projection of Global Health WBAN Shipments [5]

In search for methods to reduce the power / energy dissipation, duty cycling of the radio has emerged as one of the most appealing alternatives in protocols like WiseMAC. Duty cycling involves data transfer via radios capable of achieving high peak data rates so that they communicate short bursts of data at this high rate and are asleep the rest of the time. Any increase in the data rate capability of these radios serves to reduce the time for which they are active, thus leading to lower duty cycle ratios and subsequently lower average energy dissipation.

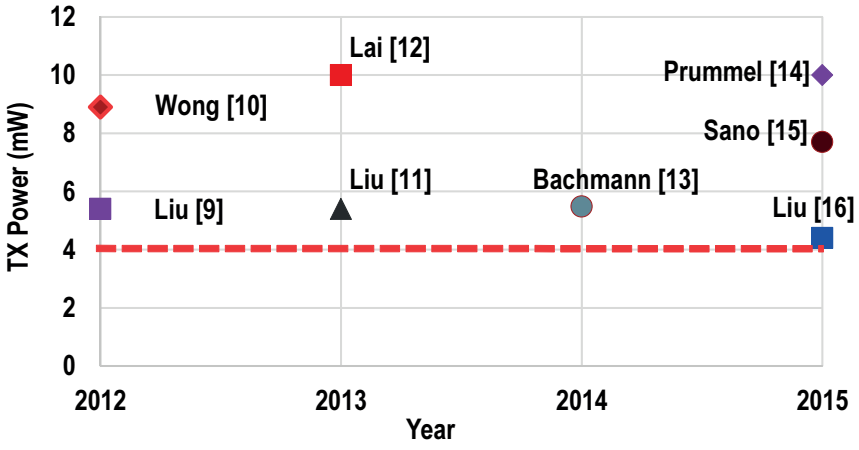


Figure 1.5 – Evolution of power dissipation of Bluetooth Smart Radios over the recent years

In addition to lowering the average power / energy dissipation, duty cycling also serves to reduce network congestion in Wireless Mesh Networks (WMNs) that form the backbone of IoTs. These networks usually employ access mechanisms like TDMA to enable interference free communication [18]. As the number of nodes in the mesh increases the time-slot available for each unique communication decreases. Coupled with each sensor node sending more data, this leads to severe network congestion. An increase in the data rate of the radio would lead to a reduction in the time slot required to communicate a given data packet and thereby ease the load on the network.

But any such data rate increase poses many design challenges, especially in the frequency synthesizer part due to the fact that the energy overhead becomes comparable to the energy that is spent to communicate useful information. For instance, in the case of conventional Phase Locked Loop (PLL) based synthesizers, the settling time is inversely proportional to the loop bandwidth. This settling time, along with the constant energy overhead due to the long wake up of the crystal oscillator (XO) reference negates any advantage gained by increasing the radio data rate (increased rate of duty cycling) aimed at reducing the average energy dissipation of the system. Therefore, in order to reduce the energy overhead, the PLL settling time as well as the XO wake up time have to be reduced. To improve the PLL settling time, the loop bandwidth can be increased. But this will lead to an increase in the Quantization Noise (QN) due to the Sigma-Delta modulator (SDM) appearing at the PLL output [19]. Many techniques have been suggested in the literature to reduce the impact of the SDM QN at the output of the PLL [20], [21]. But all such techniques either increase circuit complexity or consume a significant amount of power. In addition, for PLLs employing single point modulation, the data rate is also directly proportional to the loop bandwidth. In such cases, any increase in data rate will therefore also require an increase of the loop bandwidth. To summarize, the average energy dissipation of a duty cycled radio is linked mainly to its frequency synthesizer. Moreover, the radios should be able to support multi-hop communication to achieve robust performance against interferers. Therefore, frequency agility of the radio (also dependent on the frequency synthesizer) also becomes important. In a nutshell, for enabling effective duty-cycling of a futuristic radio that can be used in IoT nodes, it is imperative to evolve synthesizer architectures that can address all the aforementioned constraints of data rate, overhead and frequency agility.

But before going into the step by step evolution of such a synthesizer, it is necessary to define a Figure-of-Merit (FoM) that accurately reflects the effect of the energy overhead on the system energy autonomy. Indeed, the Energy per Bit FoM that has been traditionally used for quantifying the energy efficiency of the radio fails to take into account the energy overhead and is hence of little use in duty-cycled systems. Therefore, a new FoM has to be defined to better benchmark duty-cycled systems (radios in particular). This is done in the next section.

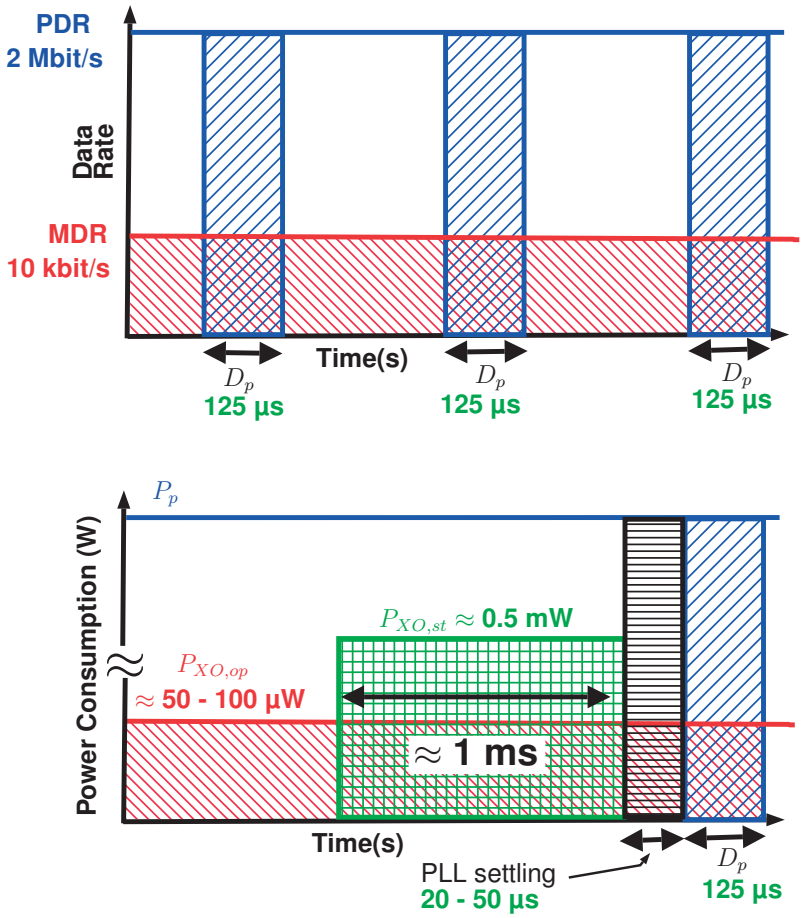


Figure 1.6 – PLL-based Transmitter duty cycling showing the various sources of energy dissipation in a duty cycled system - Multi-packet communication (top) and Single packet communication with crystal oscillator startup overhead (bottom)

## 1.3 Metrics and Figures of merit for Duty-cycled ULP radios

The derivation of the energy metric in this paper follows the work of [22] by assuming an ULP system which has to maintain a mean data rate of $MDR(bps)$. Let the time taken for this system to communicate $K$ bits of data be $T_d(s) = K/MDR$. If the system employs a transmitter capable of a peak data rate of $PDR(bps)$, then it can be duty cycled with a ratio $DC = MDR/PDR$. The packet rate of the system is given by $R_p(packets/s) = MDR/L$ where $L$ is the length of each packet. The duration of each packet is then $D_p(s) = L/PDR$. If this radio consumes a peak power of $P_p(W)$ while in operation, then the energy spent for communicating $K$ bits of data is given by $E_c(J) = T_d \times R_p \times D_p \times P_p$ (communication energy). In addition, the static energy overhead in the radio is denoted as $E_{oh}(J)$. If the radio dissipates a power of $P_{wu}(W)$ during wake-up, the overhead energy spent during each wake-up cycle will be $E_{oh}(J) = P_{wu} \times T_{wu}$, where $T_{wu}(s)$ is the wake-up time of the radio (which is usually dominated

by the frequency synthesizer wake up time). Subsequently, the energy wasted as overhead during the transmission of $K$ data bits is $E_{oh,tot}(J) = T_d \times R_p \times E_{oh}$. Then, the overall energy spent by the system for transmitting $K$ bits of raw data is $E_{p,tot}(J) = E_c + E_{oh,tot}$, which is the new FoM for duty cycled radios.

To illustrate the effectiveness of this $E_{p,tot}$ FoM in reflecting the true energy dissipation in a duty cycled systems, let a ULP radio communicating 10 kb/s on average be assumed. Now let the radio used in the system utilize the State-Of-The-Art (SOTA) transmitters given by [12], [11] which have a peak operational power dissipation ($P_p$) of 5.4 mW and are capable of a peak data rate (PDR) of 2 Mb/s. To achieve the MDR of 10 kb/s, the system can be duty cycled with a ratio of $DC = 0.5\%$. If the packet length is fixed to be $L$=32 bytes, then the packet rate is calculated as $R_p$=40 packets/s and the duration of each packet is $D_p$=125 µs. If the data transmitted by the system is assumed to be $K = 10$ kb, then $T_d = 1$ s and the mean energy dissipated for communication is $E_c$=47 µJ. If such an BAN employs a PLL-based radio for its radio, then the system will have a long wake up time owing to the XO (typically $T_w$=1 ms) and a high start up power dissipation ($P_{st}$) of around 1 mW which worsens the $E_{p,tot}$ FoM. Coming to the energy overhead, due to its long startup time, the XO is usually left permanently ON during which time it consumes 50-100 µW of power. Therefore the energy overhead for the transmission of 10 kb of data is $E_{oh,tot}$ = 50-100 µJ which is higher than the energy spent to communicate. Even if duty cycling of the XO along with the TX is pursued, based on the 1 ms startup time and 0.5 mW power, the energy overhead is 20 µJ (40 packets/s). In addition to this, assuming a best case PLL settling time of around 20 µs, the energy overhead due to the PLL will be around 4.3 µJ. This is shown in Figure 1.6 which graphically explains the aforementioned energy dissipation calculations. Thus, the total energy dissipated in the best case is then $E_{p,tot} = 51.3$ µJ. If the system uses a CR2032 button cell battery (225 mAh) as its power source, this energy dissipation translates to a battery lifetime of 200 days or about 4.4 days when a V335 (5 mAh) battery is used. This very small lifetime deters the use of button cell powered autonomous wearable/implantable nodes. An important conclusion that can be drawn from the figures presented above is that the energy wasted as overhead during each transmit cycle is almost equal to the communication energy. As the data rate of the transmitter is increased further, the communication energy keeps decreasing and at a certain point, the overhead takes over as the dominant energy sink of the system. This crossover point (called Useful Energy Threshold or $UET$) shown in Figure 1.7 represents an important point for duty cycled applications. This is due to the fact that any data rate increase which brings $E_c$ below this $UET$ has a limited impact on the system efficiency due to the larger energy overhead. Therefore, in order to increase the $UET$, there is a need to reduce the energy overhead of the system by means of reducing its start-up time.

## 1.4 Dissertation outline

Leading from the discussion of the previous sections, the solution to the conundrum of designing a truly Ultra-Low Power radio involves the following requirements

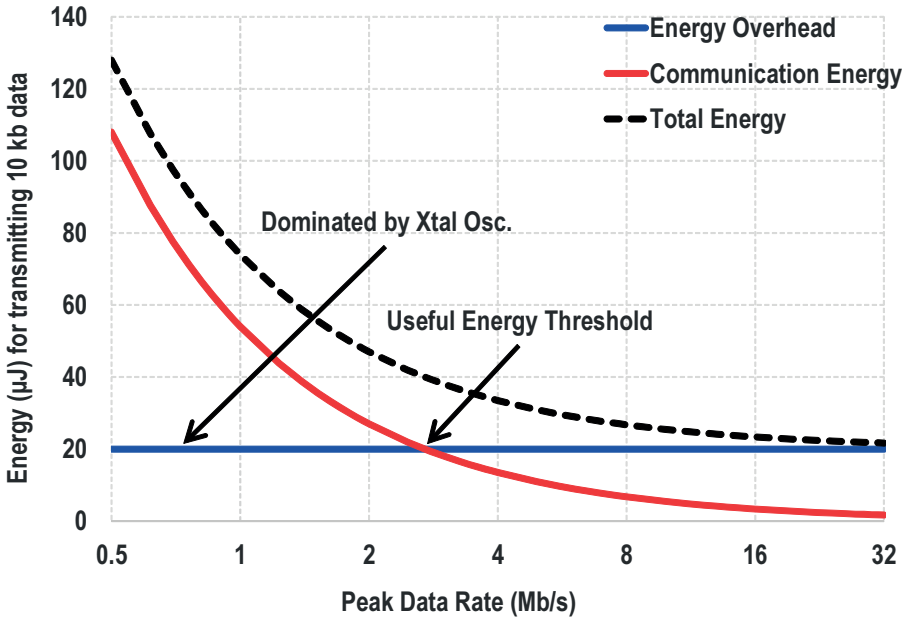


Figure 1.7 – Energy dissipation break-up of a 10 kbit/s ULP system using the TX in [12]

- Reducing the synthesizer energy overhead.
- Increasing the maximum data rate capability.
- Improving the frequency agility.
- Making the system digital to be conducive to technology scaling.

In the case of Fractional-N PLLs (loop based synthesizers in general) the maximum data rate increase (in case of frequency modulation) can be addressed by adopting a multi-point modulation scheme or increasing the loop bandwidth. But this increase in the bandwidth will allow more Quantization Noise(QN) of ΣΔ Modulator (SDM) to appear at the output and hence a data rate increase will mean reducing the QN. The loop bandwidth also determines the loop settling time and subsequently the SDM QN also has an impact on the radio's energy overhead as mentioned previously. This dependency is explained in detail in the first section of Chapter 2. Thus the reduction of the SDM QN has a two fold impact in reducing the synthesizer overhead as well as increasing the data rate. As Chapter 2 illustrates, one of the ways to reduce the Quantization Noise (QN) is by the use of division ratio step size. A detailed discussion on different circuit designs of a latch based low-power Phase Switching Divider (PSD) for this purpose is given in that chapter followed by measurement results of a PLL with this PSD. Finally, the chapter also includes a comparison of the proposed PSD with other similar architectures from the literature.

The next step in the evolution of the new frequency synthesizer is aimed at exploring ways of dealing with the energy overhead due to the crystal oscillator frequency reference. Apart from this overhead problem, the quartz crystal remains one of the bulkiest components (after the battery) for applications requiring ultra miniaturized radio like cochlear implants. Therefore, there is a need to find an alternative to the crystal which not only can wake-up fast and support high data rates, but also is small so that it can be used in miniaturized systems. Film Bulk Acoustic Resonators (FBARs) are a class of MEMS resonators which fit this criteria and Chapter 3 is dedicated to the design of frequency synthesizers based on FBARs. With the FBARs being RF frequency references, they can be used to design loop-free frequency synthesizers. But the price paid for these advantages is the necessity of an off-chip filter to remove all the spurious components that lie outside the band of interest. This chapter starts off by introducing the FBAR resonators a is ndfollowed by an outline of the synthesizer architecture. This is followed by an overview of the State-of-the-Art (SOTA) in synthesizers using FBAR resonators. The next step is the circuit design of the various building blocks of this synthesizer including the DCO, mixer and adapting the PSD. The chapter also includes the details of the design of a Transmitter (TX) including this synthesizer. The Power Amplifier (PA) of this TX also includes a linearization block which enables it to be used with standard protocols like IEEE 802.15.6. Finally, the measurement results of this TX are presented along with a comparison with the SOTA synthesizers.

Though the above mentioned frequency synthesizer satisfies the first three requirements of the future IoT radios, it has an analog mixer which is not conducive to technology scaling from the point of view of area, mismatch etc. Direct Digital synthesizers (DDS) are a potential solution to this scaling issue as they have high frequency agility. These synthesizers make use of a look up table to map an input code to the stored amplitude value of the required output signal. But the main drawback of such DDS is that their active power consumption is very high and they are restricted in their output frequency range. Yet, the principle of DDS can be modified to map the input code to the zero crossing times (instantaneous frequency information) of the output signal to achieve the desired output frequency. In order to avoid spurs and to have low close-in noise, this idea of using the zero crossings can be combined with a $\Sigma\Delta$ Modulator which performs noise shaping. Based on this idea, the fourth chapter of the thesis involves the design of a Phase Domain Direct Digital Synthesizer (PDDDS) that is based on an FBAR frequency reference. This synthesizer satisfies all the IoT requirements mentioned previously. Chapter 4 begins by explaining the architecture of this synthesizer along with its principle of operation. This is succeeded by the design of the core circuit blocks namely the retimer circuit (which is essential for proper operation), range extension circuit and the $\Sigma\Delta$ modulator. The SDM section deals with the bus-splitting technique used for high speed operation. Also given under the banner of the SDM is the design methodology of Hybrid Requantizers (HRQ) which can reduce the level of the spurious components in the output spectrum that arise from the non-linear nature of the frequency synthesizer. Finally, Chapter 4 ends by presenting the measurement results of a TX which includes this all-digital frequency synthesizer.

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# 2 ΣΔ Quantization Noise reduction in fractional-N PLLs

ΣΔ modulator (SDM) Quantization Noise (QN) is one of the main issues that prevents the reduction in the energy dissipation of systems using fractional-N loop based synthesizers like Phase Locked Loops (PLLs) and Delay Locked Loops (DLLs). Indeed, as mentioned in the introduction, the QN is related to the bandwidth of the loop, which in turn affects the loop settling time and in turn the energy overhead. In addition, the bandwidth of the system also determines the maximum data rate in case of a single point modulation. This restriction can be circumvented using two point modulation, but at the cost of high circuit complexity. Therefore for the purpose of QN reduction, many circuit techniques have been proposed in the literature such as using a Digital to Analog Converter (DAC) to convert the quantization error into analog current and using it for cancellation at the output of the charge-pump [1]. While this technique is effective in cancelling the QN, it results in the doubling of the noise that is folded down due to charge pump non-linearities [2]. Others have utilized Finite Impulse Response (FIR) filters at the output of the SDM to custom-shape the QN spectrum [3]. But the disadvantage of these techniques are increased circuit complexity and accuracy requirements. By far, the simplest technique to reduce the QN that appears at the PLL output is to reduce the division ratio step size of the Multi-Modulus Divider (MMD) that follows the SDM. For this purpose, a low-power solution that manages to reduce the division ratio step by a factor of 5 to 0.2 is proposed in this chapter, and thereby achieving a 14 $dB$ reduction in QN. The organization of this chapter is as follows: this chapter begins by listing the inter-dependence of the various parameters of a fractional-N PLL. This gives way to the principle of the Phase Switching Divider (PSD) to reduce the QN and the State of the Art in PSDs. Then comes the design of the PSD with a division ratio step size of 0.2 with the measurement results and a summary of the same bringing up the rear of the chapter.

## 2.1 An overview of fractional-N PLLs

Fractional-N Phase Locked Loops (PLLs) are ubiquitous in wireless radios mainly due to their capability of achieving high frequency resolution unlike their integer-N counterparts, whose resolution is dependent on the reference frequency, $f_{ref}$. The delinking of the resolution and

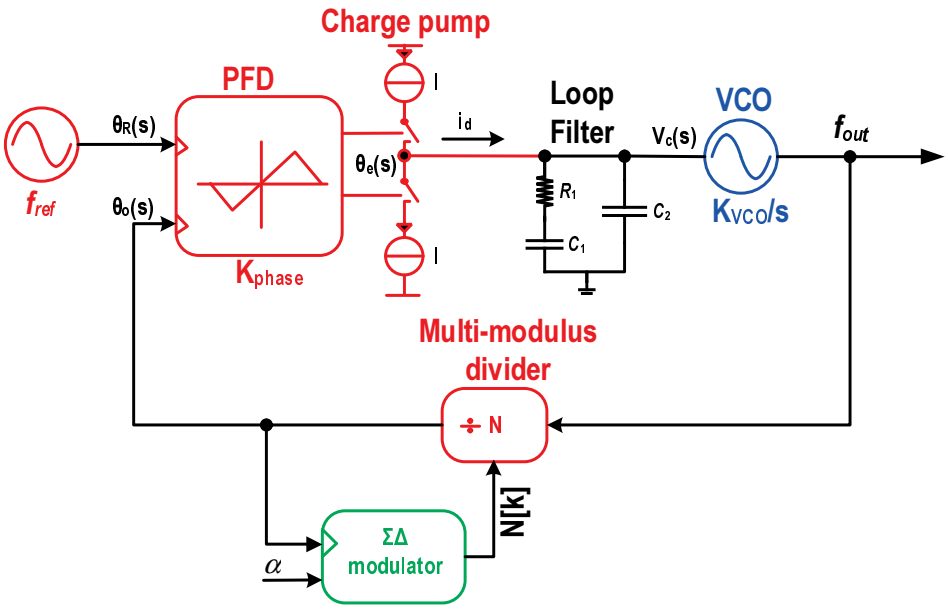



Figure 2.1 – Block Diagram of a PLL

$f_{ref}$ has a significant impact on the synthesizer settling time and the noise performance of the system. This can be explained by the following rationale: In an integer-N PLL, a finer resolution entails a lower reference frequency. Low reference frequency requires low loop bandwidth to ensure the stability of the loop. But a low loop bandwidth leads to a large settling time for the PLL and thereby increases the energy overhead of the system [4]. To explain this concept further the transfer function of the PLL is derived using figure 2.1 (This block diagram represents a fractional-N PLL. The integer-N PLL lacks the ΣΔ modulator and the Multi-modulus divider is replaced by a simple integer divider). This closed loop transfer function is given by

$$\frac{\theta_0}{\theta_R} = \frac{K_{VCO}K_{phase}(1+sRC_1)}{s^2N(C_1+C_2)(1+sRC_s)+K_{VCO}K_{phase}(1+sRC_1)} \tag{2.1}$$

where $K_{VCO}$ and $K_{phase}$ are the gains of the VCO and the PFD respectively, $C_s$ represents the series combination of $C_1$ and $C_2$. Ignoring the effect of $C_2$ which is just a capacitor to suppress high frequency ripple on the VCO control line, the criterion for loop stability can be written as

$$\omega_n \leq \frac{\omega_{ref}}{2\pi\zeta}, \tag{2.2}$$

where $\omega_n$ is the natural frequency of the loop (it is a second order system), $\zeta$ is the damping constant and $\omega_{ref}$ is the reference frequency of the system. For the sake of completeness, the expressions for the $\zeta$ and $\omega_n$ are given below in equation 2.3.

$$\omega_n = \sqrt{\frac{IK_{VCO}}{2\pi \cdot NC_1}} \tag{2.3a}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{IK_{VCO}C_1}{2\pi \cdot N}} \tag{2.3b}$$

which has been obtained by substituting for $K_{phase}$ in equation 2.1 with $I/2\pi\,(R+1/sC_1)$ representing the charge pump transfer function. The natural frequency of the loop is related to the loop bandwidth by the following formula

$$\omega_{3dB} = \omega_n\sqrt{1+2\zeta^2+\sqrt{4\zeta^4+4\zeta^2+2}} \tag{2.4}$$

Assuming the system is critically damped ($\zeta = 1$), this equation reduces to

$$\omega_{3dB} = \left(1+\zeta\sqrt{2}\right)\omega_n \tag{2.5}$$

Substituting equation 2.5 in equation 2.2 yields the relation between the loop bandwidth and the reference frequency as

$$\omega_{3dB} \leq \frac{\omega_{ref}}{2\pi\zeta}\left(1+\zeta\sqrt{2}\right) \tag{2.6}$$

Now, looking at the settling time of the PLL, it is noted that for an input frequency step the evolution of the phase error with time is given by

$$\theta_e(t) = \frac{\Delta\omega}{\omega_n}\left[\frac{\sinh\,\omega_n\sqrt{\zeta^2-1}\,t}{\sqrt{\zeta^2-1}}\right]e^{-\zeta\omega_n t} \qquad \zeta > 1 \tag{2.7a}$$

$$\theta_e(t) = \frac{\Delta\omega}{\omega_n}\omega_n t\cdot e^{-\omega_n t} \qquad \zeta = 1 \tag{2.7b}$$

$$\theta_e(t) = \frac{\Delta\omega}{\omega_n}\left[\frac{\sin\,\omega_n\sqrt{\zeta^2-1}\,t}{\sqrt{\zeta^2-1}}\right]e^{-\zeta\omega_n t} \qquad \zeta < 1 \tag{2.7c}$$

Now if the reference frequency of the system is made smaller to enhance the frequency resolution, then the natural frequency of the system and subsequently the loop bandwidth becomes smaller and it means that the phase error takes longer to approach its final value of zero. This means the loop will take longer to settle during which time no communication is possible.

The impact of the loop bandwidth on the phase noise of the system can also easily be derived by finding the transfer function of the various noise sources given in figure 2.2. Out of these different noise PSDs, the one of the VCO is of particular interest for this discussion. The VCO phase noise has a -30 $dBc/Hz$ per decade rolloff close to the carrier due to flicker noise and

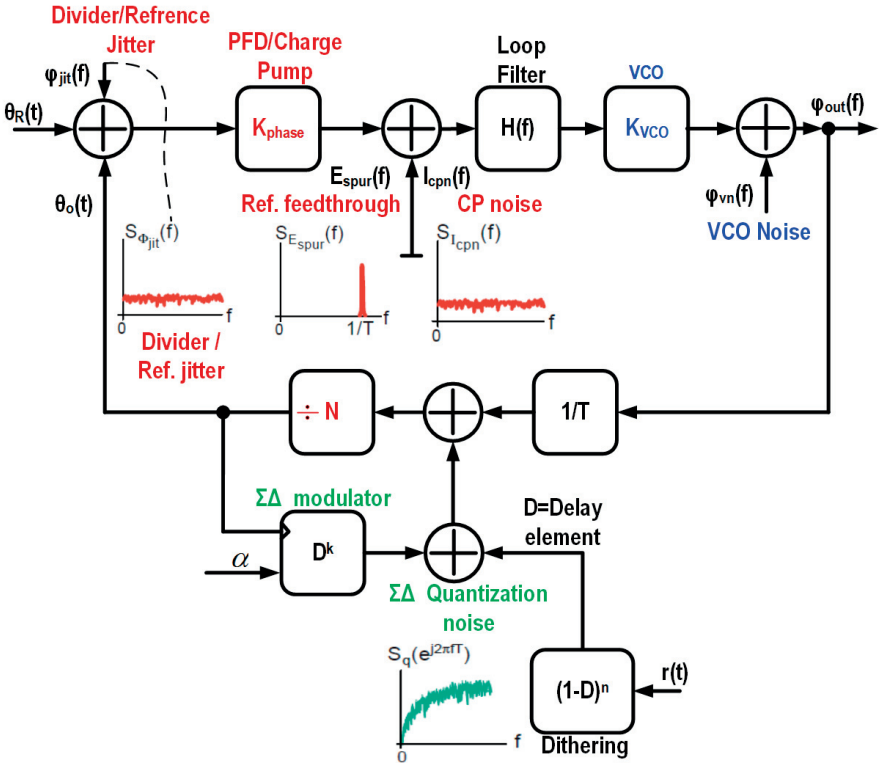



Figure 2.2 – The various noise sources in a PLL [5]

from slightly higher offsets, the thermal noise takes over and hence it exhibits a -20 $dBc/Hz$ per decade slope. Now, the transfer function of this noise ($S_{\phi_{vn}}(f)$ in figure 2.2) to the output is calculated as

$$\frac{\phi_{out}}{\phi_{vn}} = \frac{s^2}{s^2 + \frac{K_{phase}K_{VCO}}{N}sR + \frac{K_{phase}K_{VCO}}{NC_1}}. \tag{2.8}$$

This has been calculated by replacing $H(f)$ with the impedance of the loop filter ($R + 1/sC_1$) in figure 2.2. From equation 2.8, it can be ascertained that the transfer function is of high-pass nature. Therefore, as the loop bandwidth is decreased to ensure stability, more and more of the VCO noise is passed unfiltered to the output, thereby degrading the noise performance of the synthesizer.

A Fractional-N PLL overcomes the dependence of the synthesizer performance on the frequency of the reference. The simplest fractional-N PLL can be built by using a look-up table that toggles the division ratio of a multi-modulus divider so that the average frequency at the output of the divider equals the reference frequency. The problem with this method is that the division ratios are periodic (periodic dither) and hence will result in spurious tones at low frequency offsets. The bandwidth of the PLL must be reduced to get rid of these tones, which in effect nullifies the fractional-N approach. A solution to this problem is to use a ΣΔ

modulator (SDM) with randomized dithering. The ΣΔ converts the spurious tones in the output spectrum into noise (called Quantization Noise) that is shaped so that most of its energy lies at high frequency offsets from the carrier. By using a sufficiently high order for the SDM, this technique eliminates most of the spurious tones. Further discussion on the SDM Quantization Noise (QN) and its effect on the PLL performance is detailed in the following section.

## 2.2 PLL QN vs data-rate tradeoff

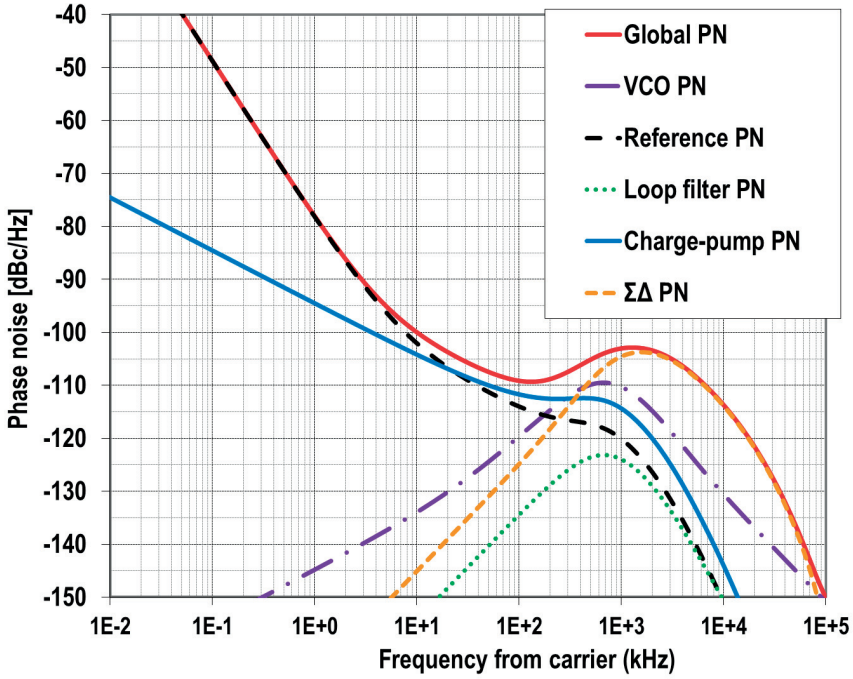



Figure 2.3 – Simulated Phase noise of various PLL components

The randomization action of the SDM gives rise to phase noise whose value can be determined by the following rationale [4]: Assuming that the output levels of the SDM are uniformly distributed with a step size of Δ, the 1-bit quantization noise power is $\Delta^2/12$. This noise power is spread over the sampling bandwidth which is equal to the frequency of the divider output. Since in a PLL, the divider signal frequency is ideally equal to the reference frequency, the sampling bandwidth can be approximated with $f_{ref}$. For a SDM of order $m$, the noise transfer function of the dither is $(1-z^{-1})^m$. Therefore the frequency noise PSD ($S_{qf}(z)$) due to the SDM is given by [4]

$$S_{qf}(z) = \frac{\Delta^2}{12 f_{ref}} \left| \left(1-z^{-1}\right)^m f_{ref} \right|^2 = \frac{\Delta^2}{12} \left(1-z^{-1}\right)^{2m} f_{ref}. \tag{2.9}$$

Now, to obtain the phase noise expression, the derivative of this noise should be calculated i.e.

$$2\pi f = \frac{d\phi(t)}{dt} = \frac{\phi(z)(1-z^{-1})}{T_s} \tag{2.10}$$

Converting the frequency noise in equation 2.9 into phase noise gives

$$S_\phi(z) = \frac{\Delta^2}{12} \cdot \frac{4\pi^2}{f_{ref}} \left(1-z^{-1}\right)^{2(m-1)} \tag{2.11}$$

This equation can be simplified by observing that

$$\left(1-z^{-1}\right) = \left|1-e^{-j2\pi f_{off} T_s}\right| \approx 2sin\left(\frac{\pi f_{off}}{f_{ref}}\right) \tag{2.12}$$

where $f_{off}$ represents the offset frequency at which the phase noise is measured. Therefore, the phase noise is calculated as

$$PN_{\phi_{qn}}(f) = 10\log\left[\frac{\Delta^2}{12} \cdot \frac{4\pi^2}{f_{ref}} \left[2\sin\left(\frac{\pi f_{off}}{f_{ref}}\right)\right]^{2(m-1)}\right] dBc/Hz. \tag{2.13}$$

This quantization noise while passing through the loop acquires a transfer function given by (the conventions used are given in figure 2.2)

$$G(s) = \frac{K_{phase} H(s) K_{VCO}/N}{s + K_{phase} H(s) K_{VCO}/N}. \tag{2.14}$$

This is a low pass transfer function. Therefore, the SDM QN only starts becoming important when the loop bandwidth is increased to accommodate higher data rates. This is shown in the phase noise spectrum (Figure 2.3) at the output of the PLL with a loop bandwidth of around 1.5 MHz. There are three distinct regions that can be observed from this figure *viz.* (1) at low frequency offsets the noise of the system is dominated by the reference oscillator flicker noise (2) at the intermediate frequency offsets (in the vicinity of 10 kHz to 100 kHz) the charge pump noise becomes the highest contributor and (3) at high frequency offsets (above 1 MHz) the noise of the SDM is the dominant factor causing the PLL global phase noise to have a bump instead of a smooth roll off. A higher order of SDM will entail low close-in noise but will translate to higher out-of band noise. This is due to the fact that since the noise of the random dither is constant, a lower close-in noise should be compensated by a higher noise elsewhere. In addition to this, the non-linearities in the PLL such as charge pump current mismatch (both static and dynamic) and the various delays in the dividers and the Phase Frequency Detectors (PFD) cause the SDM QN to fold back within the bandwidth of the PLL, thereby increasing the noise. But before going into the details of this non-linearity induced noise folding, the connection between the PLL bandwidth and the data rate in the case of single point modulation is shown in the next section which closely follows the work of [6] and [5].

## 2.3 Relation between PLL bandwidth and Data rate

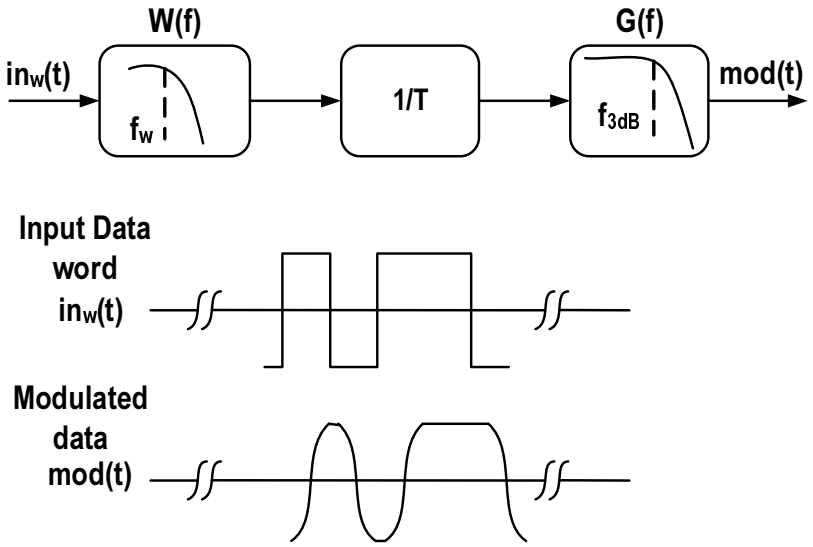



Figure 2.4 – Data path for GFSK modulation

Two point modulation schemes for PLLs have been proposed in the literature with the aim of circumventing the issue of loop bandwidth dependency of the data rate. In such schemes, modulation data is applied both at the ΣΔ input (which has a low pass transfer function) as well as the VCO node (high pass characteristic), thereby removing the dependency of the data rate on the PLL bandwidth. But unfortunately, such schemes need precise gain matching at these two nodes as well as phase matching, lest it will degrade the Error Vector Magnitude (EVM) of the transmitted signal. To ensure such matching, calibration circuits have to be designed which greatly increases circuit complexity. Therefore, extending the PLL bandwidth still is important for high data rate capable PLLs. To study this interdependence, let a PLL with a closed loop transfer function of $G(f)$ be assumed to support GFSK modulation. In this case, the data passes through the discrete time Gaussian transmit filter followed by the PLL transfer function in continuous time as shown in figure 2.4. The total transfer function that the data to be communicated must go through is [6]

$$H(f) = \frac{1}{T} W(f) G(f). \tag{2.15}$$

Here, the transmit filter has a bandwidth of $f_w$, the PLL has a loop bandwidth of $\omega_{3dB}/2\pi$. Then, the total transfer function $H(f)$ can be thought of representing one filter with a bandwidth of $B$. An important parameter of the GFSK modulation is the product of the Gaussian filter bandwidth times symbol time, $T_d$ (Data rate, $DR = 1/T_d$). This value determines the spectral occupancy of the Gaussian filter. A small value of the $f_w T_d$ product will lead to small spectral occupancy and this means that the impulse response will spread over adjacent symbols leading to increased Intersymbol Interference (ISI) [7]. On the other hand, a high value of the $f_w T_d$ product is spectrally inefficient. Therefore, the established guideline for GFSK is to have

the $f_w T_d$ product to be 0.5. Ideally, the bandwidth of the PLL can be chosen to coincide with that of the Gaussian filter. But the low pass filter established by the PLL is analog in nature and the non-linearities in the loop may not allow ideal Gaussian shaping to be achieved. So by setting $f_w$ to be less than $\omega_{3dB}/2\pi$, it is ensured that the modulation data is always shaped by the discrete time Gaussian filter. To summarize, the lower bound on the PLL loop bandwidth is set by the Gaussian filter and subsequently by the maximum data rate (since $f_w/DR = 0.5$). As with the Gaussian filter, as the loop bandwidth of the PLL approaches the value of $f_w$, intersymbol interference will increase due to the PLL non-linearities. A typical rule of thumb on the PLL bandwidth for GFSK modulation is given in [6] to be $\omega_{3dB} T_d = 2\pi \cdot 0.7$.

## 2.4 ΣΔ Noise Folding due to PLL non-linearities

The noise at the output of a PLL due to a ΣΔ modulator of order $m$ is given in equation 2.13. But this has been derived using a Linear Time Invariant (LTI) analysis. Thus, it fails to capture the effect of the various PLL non-linearities like Charge Pump (CP) gain mismatch, charge pump current slew, reset delay mismatch in the PFD, etc. All these non-linearities in effect increase the noise floor of the PLL inside the loop bandwidth and hence it is difficult to filter out. This is explained in this section which presents a brief overview of these noise mechanisms [8].

Let a multi-modulus divider with a nominal division ratio of $N$ be assumed. If the divider is controlled by a SDM, then the instantaneous division ratio $N[k]$ can be expressed as $N + \Gamma[k]$, where $\Gamma[k]$ is the instantaneous deviation from the nominal division ratio. With $\alpha$ being the fractional part of the SDM input, the reference frequency is expressed as

$$f_{ref} = \frac{f_{out}}{N + \alpha}. \tag{2.16}$$

Now the Phase Frequency Detector (PFD) compares the reference clock edge with the output of the divider and produces a pulse. The duration of the pulse can be expressed as

$$\begin{aligned} \delta_k &= t_{div}[k] - t_{ref}[k] \\ &= t_{div}[k-1] + N[k] - t_{ref}[k-1] - (N+\alpha) T_{VCO}. \end{aligned} \tag{2.17}$$

Due to its recursive nature, the above equation can be written as

$$\delta_k = \delta_{k-1} + (\Gamma[k] - \alpha) T_{VCO}. \tag{2.18}$$

Now, the average of $\Gamma[k]$ can be expressed as the sum of $\alpha$ and the quantization error $E_q$ multiplied by the Noise Transfer Function ($NTF$) of the SDM. In frequency domain, this can be written as

$$\Gamma(z) = E_q \cdot NTF(z) + \alpha. \tag{2.19}$$

Substituting this in equation 2.18 yields

$$\delta_k(z) = \frac{E_q \cdot NTF(z)}{1 - z^{-1}} T_{VCO}. \tag{2.20}$$

The pulses of width $\delta_k$ produced by the PFD are converted into current pulses (up or down depending on whether the divider output leads or lags the reference) by the Charge Pump. The effect of the CP action is that there is a net charge delivered to the loop filter in each reference clock cycle. The amount of charge delivered to the loop filter is $I_{CP}\delta_k$. Therefore, if the CP were to be ideal, the equivalent current delivered by the CP is given by

$$i_k = \frac{I_{CP}\delta_k}{T_{ref}}. \tag{2.21}$$

In order to ensure that the CP currents have enough time to settle, i.e. to minimize the dead zone in the PFD, both the UP and the DOWN currents are turned on together for a non-zero amount of time. For example, when the reference signal leads the divider output signal, the UP current is turned on with the reference edge, followed by the DOWN current at the divider output edge. Then after a delay for a period called $T_d$, both of the currents are turned off. This procedure ensures that the charge pump currents have settled properly, thereby eliminating one of the major sources of CP non-linearity [9].

Assuming a mismatch of $\epsilon$, the CP currents can be written as

$$I_{up} = I_{CP}(1 + \epsilon/2) \qquad I_{dn} = I_{CP}(1 - \epsilon/2). \tag{2.22}$$

With this knowledge, the net charge dumped on the loop filter is determined by

$$Q_k = \begin{cases} I_{up}\delta_k + \epsilon I_{CP} T_d, & \text{if } \delta_k > 0, \\ I_{dn}\delta_k + \epsilon I_{CP} T_d, & \text{if } \delta_k < 0. \end{cases} \tag{2.23}$$

Substituting equation 2.22 in equation 2.23 yields

$$Q_k = I_{CP}\delta_k + \frac{\epsilon}{2} I_{CP} |\delta_k| + \epsilon I_{CP} T_d. \tag{2.24}$$

The third term in the above equation is a constant since $T_d$ and $I_{CP}$ are constant and this term causes a static offset charge in the loop filter. The first term represents the ideal CP behaviour. The second mismatch term which is dependent on $\delta_k$ is responsible for the SDM noise folding and results in the increase of the noise floor. Writing in terms of currents, we get

$$I_k = I_{ideal} + I_{error} + I_{static}, \qquad \text{where}$$

$$I_{ideal} = \frac{I_{CP}}{T_{ref}}\delta_k, \tag{2.25a}$$

$$I_{error} = \frac{I_{CP}}{T_{ref}} \frac{\epsilon}{2} |\delta_k|, \tag{2.25b}$$

$$I_{static} = \frac{I_{CP}}{T_{ref}} \epsilon T_d. \tag{2.25c}$$

Substituting for $\delta_k$ from equation 2.20 results in the ideal CP current being given by

$$I_{ideal} = \frac{T_{VCO}}{T_{ref}} \frac{E_q \cdot NTF(z)}{1 - z^{-1}} I_{CP}. \tag{2.26}$$

Using equation 2.11 and equation 2.12 in conjunction with the above equation produces the ideal CP current noise PSD as

$$S_{i,ideal}(f_{off}) = \frac{T_{VCO}^2}{T_{ref}^2} \frac{\Delta^2}{12} \frac{I_{CP}^2 4\pi^2}{f_{ref}} \left[ 2 \sin\left( \frac{\pi f_{off}}{f_{ref}} \right) \right]^{2(m-1)} \qquad (A^2/Hz). \tag{2.27}$$

Assuming that the CP error current noise is essentially white, the noise PSD due to the error current can be expressed as

$$S_{i,error}(f_{off}) = \frac{\epsilon^2}{4} \frac{I_{CP}^2}{T_{ref}^2} \cdot \overline{\sigma^2_{|\delta_k|}} \qquad (A^2/Hz). \tag{2.28}$$

This PSD due to the CP gain mismatch error represents the noise that is folded back thus increasing the noise floor of the system. Now if the assumption that $\delta_k$ is Gaussian in nature and the division ratio step size being $\Delta$, then the variance $\overline{\sigma^2_{|\delta_k|}}$ can be written as

$$\sigma^2_{|\delta_k|} = \Delta^2 \sigma^2_{\delta_k} \left( 1 - \frac{2}{\pi} \right). \tag{2.29}$$

Substituting equation 2.29 in equation 2.28 and equating this noise PSD with the ideal CP current noise PSD of 2.27 gives the expression of the gain mismatch corner frequency as [8]

$$\frac{f_c}{f_{ref}} = \frac{1}{4\pi^2} \left[ \epsilon \cdot \frac{\sigma_{\delta_k}}{T_{VCO}} \sqrt{3\left( 1 - \frac{2}{\pi} \right)} \right]^{\frac{1}{m-1}}. \tag{2.30}$$

This corner frequency represents the crossover point between the folded noise and the actual ΣΔ noise. This is shown in figure 2.5. From equation 2.30, it can be ascertained that as the magnitude of the current mismatch in the CP increases, the noise corner frequency also increases. It also increases with the variance of the phase error. This means that higher order SDMs, in spite of having lower close-in QN, cause more noise to fold back due to the CP current mismatch, thereby negating the increase in the order. Finally, the noise PSD due to

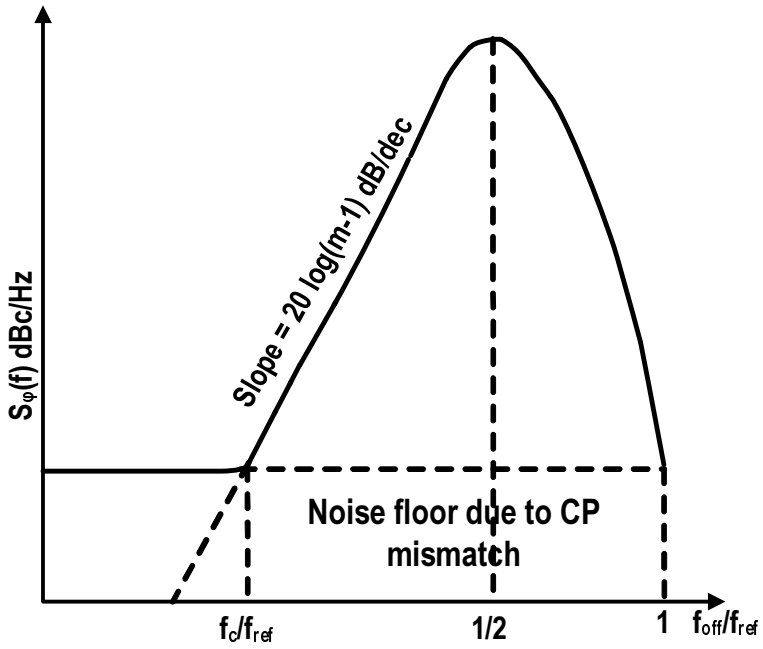



Figure 2.5 – CP current mismatch noise corner frequency [8]

the error current can be referred to the output of the PLL which is given by [2]

$$S_{i,error,out}(f_{off}) = \left(\frac{\epsilon}{2T_{ref}}\right)^2 \cdot \frac{\overline{\sigma^2_{|\delta_k|}}}{f_{ref}} \cdot 2\pi N^2 \left(\frac{A}{1+A}\right)^2 \qquad (rad^2/Hz) \tag{2.31}$$

where $A$ is the open loop transfer function of the PLL. The effect of the noise folding on the output phase noise of the PLL can be seen clearly in the plot of figure 2.6, which depicts the simulation of the noise contribution to the PLL output noise with a CP having a 10% mismatch in its UP and DOWN currents. On the overall phase noise plot, the aforementioned noise folding will show up at the intermediate frequency range (10 kHz to 500 kHz) where the CP noise is dominant. From looking at equation 2.13, it can be noted that the QN is dependent on the square of the division ratio step size. Therefore, a reduction in the step size by a factor '**k**' can bring about a lowering of the QN by **20*log(k)**. Furthermore, in the noise PSD of equation 2.31, the SDM comes into the picture via $\overline{\sigma^2_{|\delta_k|}}$ i.e. the variance of the timing error between the divider and the reference signals. Here too, reducing the divider step size will be great assistance, since the timing error $\delta_k$ is reduced as the PLL can more closely align its divider output edge with the reference edge. This results in smaller charge pump pulses and subsequently lower mismatch currents. Simply put, with a smaller division ratio step, the SDM QN is reduced and subsequently there is less noise folding. Looking at this from another point of view, the PFD/charge-pump needs to operate linearly over a smaller range, leading to reduced noise folding.

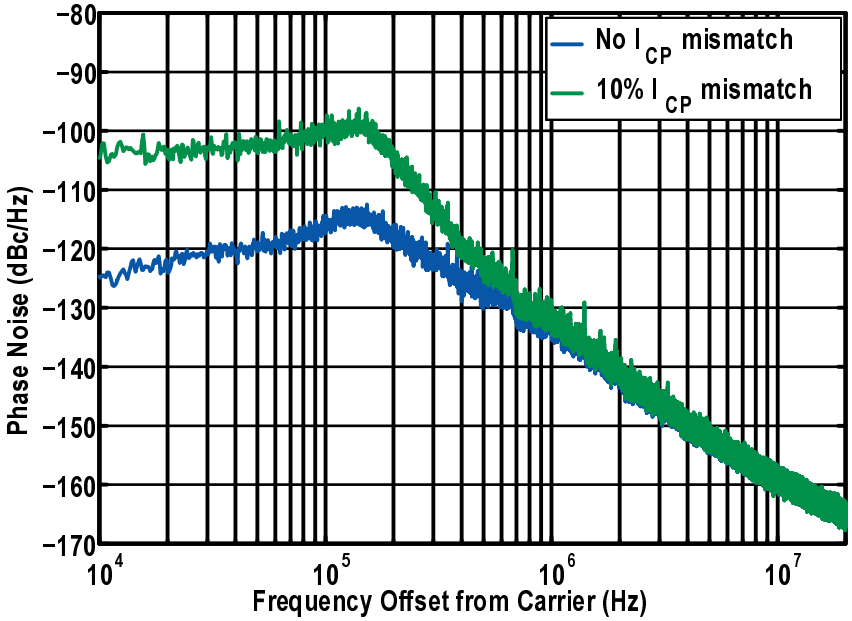



Figure 2.6 – Noise floor increase because of the Sigma Delta noise folding due to charge pump mismatch

## 2.5 State of the Art

Phase Switching Dividers have been reported in the literature [10], [11], [12], [13], [14] to reduce the division ratio step and subsequently the SDM QN and the CP noise folding. This section gives a short overview of the circuit architectures employed in these dividers and their drawbacks.

- One of the most widely cited PSDs found in the literature is [10]. Even though the PSD in this paper was used to achieve integer division steps for high speed applications, the principle can be extended to achieve sub-unity division step. This PSD divides the VCO signal by 2 and produces 4 phases that are separated by 90°. These phases are retimed and fed to a multiplexer whose control signals choose the phase which needs to be passed on to the output. The retiming circuit involves the resynchronization of both the control signal and the phase using latches. Although this serves the purpose of achieving glitch free operation, high speed phase retiming leads to a large power dissipation and places a large strain on the layout to ensure equitable delays on the retimed phases.
- The PSD of [11] utilizes the four phases of the VCO signal divided by 2 and builds a divide by 1/1.5 circuit. This is followed by a cascade of divide by 2/3 stages which gives the desired division ratios with a step size of 0.5. The disadvantage of such a divider is two-fold *viz.* 1) It suffers from potential race-conditions due to the fact that the input signal is used to clock the D-flip flops (DFFs) as well as the multiplexers that follow the DFF in the divide by 1/1.5 cell. 2) To build the flip-flops and other sequential logic,

Current-mode Logic (CML) latches are used which results in a large power consumption.

- The PSD in [12] shifts the retiming problem to the analog domain. In this circuit, the glitches are avoided by making sure the transitions of the control signals of the multiplexer are gradual i.e. they have a large slew so that the phase of the net output exhibits a smooth interpolation. The issue with this PSD is that it requires the presence of a limiter at the output of the multiplexer to correct for amplitude reduction of 3 dB that occurs due to the slewing property of the control signals. In addition, the divider is susceptible to mismatches in the analog domain and thereby to unwanted spurs.

- [13] utilizes a divide by 4/4.5 cell which is built using both positive and negative edge triggered flip flops. By appropriately choosing which of the flip-flops are on at a given instant, the division ratio step size of 0.5 is achieved. The problem with this circuit is that the complexity of the circuit exponentially increases if the division ratio step is envisaged to be further lowered. In addition, the minimum division ratio is dictated by the division ratio step (for eg. if such a circuit is designed for a division ratio step size of 0.25, the minimum division ratio will be 8).

- The circuit of [14] utilizes minimum reversed state transitions to avoid glitches and builds a divide by 0.5/1/1.5/2 cell based on this principle. Essentially, this means that the divide by 1.5 and 2 operations are performed by cascading three or four VCO cycles with $0.5T$ (where $T$ is the time period of one VCO cycle). From a system perspective, this would restrict the minimum division ratio to 4. This minimum division ratio will prevent higher reference frequencies in the system, thereby reducing the maximum data rate that can be achieved.

In all of the above references, the division ratio step size is restricted to 0.5 due to the fact that the multiple phases are derived by dividing the VCO signal by 2 to get quadrature phases and building the dividers from these phases. This in turn provides a reduction in the division step size by a factor of 2 (i.e. step size, $\Delta = 0.5$) which in turn leads to a 6 dB noise reduction. With this background, this chapter aims to improve upon these dividers and provide a generalized concept of PSD design which can achieve very small fractional division ratio. As a proof of concept, a fully CMOS logic PSD with a division ratio step size of 0.2 has been designed and measurement results of the same show a 14 dB decrease of SDM QN [15] and a consequent reduction in the SDM noise folding.

## 2.6 Architecture of an Injection Locked PSD

The principle of Injection Locking enables the designer to generate multiple phases of any given signal without having to worry about additional phase noise. Contrary to PSDs employing frequency division by 2 (or any integer for that matter) that can only reduce the division ratio step by 2 (i.e. division ratio step = 0.5 due to the fact that division operates only on the two edges of the input clock), injection locking can be used to reduce the division ratio step

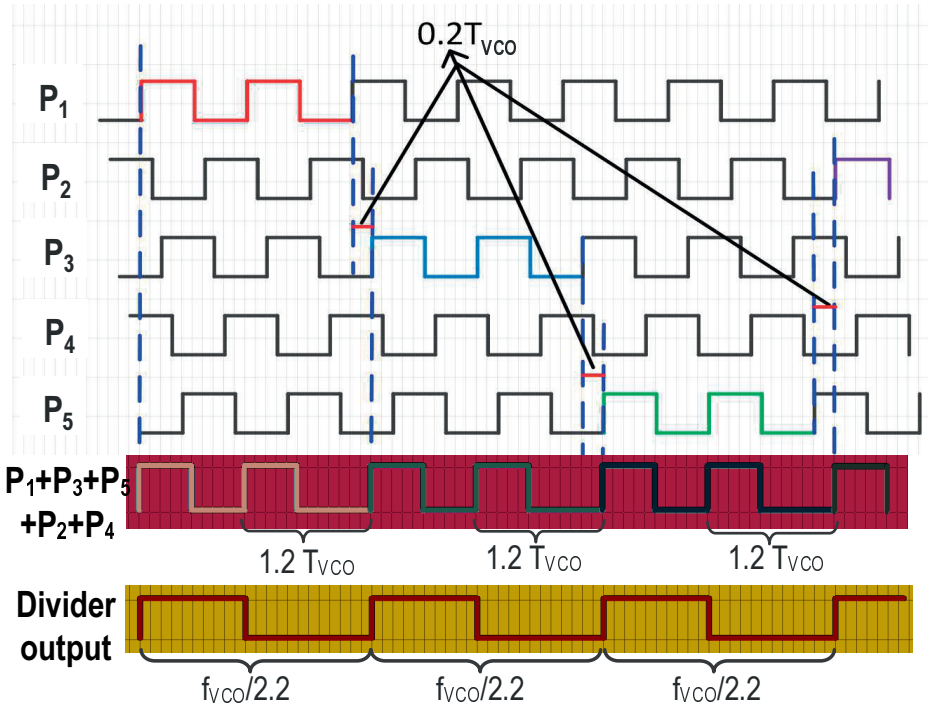



Figure 2.7 – Operation of the divider - Example : Divide by 2.2

by any arbitrary factor (subject to circuit speed limitations). Using this principle of injection locking, the proposed PSD first produces $k$ phases of the VCO signal. Then these phases are added at opportune moments to achieve a signal which has time periods that are fractional multiples of the VCO time period $T_{VCO}$. This principle is explained by the figure 2.7, where $P_1$, $P_2$, $P_3$, $P_4$, $P_5$ represent the various phases of the VCO signal which are spaced $0.2T_{VCO}$ apart. Now if it is required to divide by $N+0.2$, then $P_1$ is selected for 'N' clock cycles after which $P_3$ is selected for 'N' cycles, then $P_5$ and so on after which the selected signals are added together. This summed signal then consists of $N-1$ pulses of width $T_{VCO}$ and one pulse of width $1.2T_{VCO}$. In other words, $N$ cycles of this signal take $(N+0.2)T_{VCO}$ seconds to complete. The summed signal is then fed to an integer divider set to divide by $N$ and the output of the divider is the input signal divided by $N+0.2$. The case shown in figure 2.7 is for a division ratio of 2.2. In the case of division by $N+0.4$, the order to the phase selection goes as follows: $P_1 \rightarrow P_5 \rightarrow P_4 \rightarrow P_3 \rightarrow P_2 \rightarrow P_1$. Other cases like divide by $N+0.6$ and $N+0.8$ are similar. For division by an integer $N$, the status quo is maintained and there is no change in the choice of the phase that is selected.

The block diagram of the proposed PSD is shown in Figure 2.8. It consists of a phase generator which is basically an injection locked ring oscillator (multi-phase injection locking is used in this case) to generate the various phases of the VCO signal. At the same time, a Finite State Machine (FSM) produces the different select signals (each select signal corresponds to a phase) after which the select signals are multiplied with their corresponding phase and the

resulting signals are summed in a Phase Combiner (PC). Before phase combining, the select signals are resynchronized by the phases themselves to avoid glitches. This Phase-Combined Signal (PCS) is then fed to a dynamic integer divider set to the nearest rounded integer value. The output of this integer divider is the required output signal which is also fed back to the system to clock the FSM.

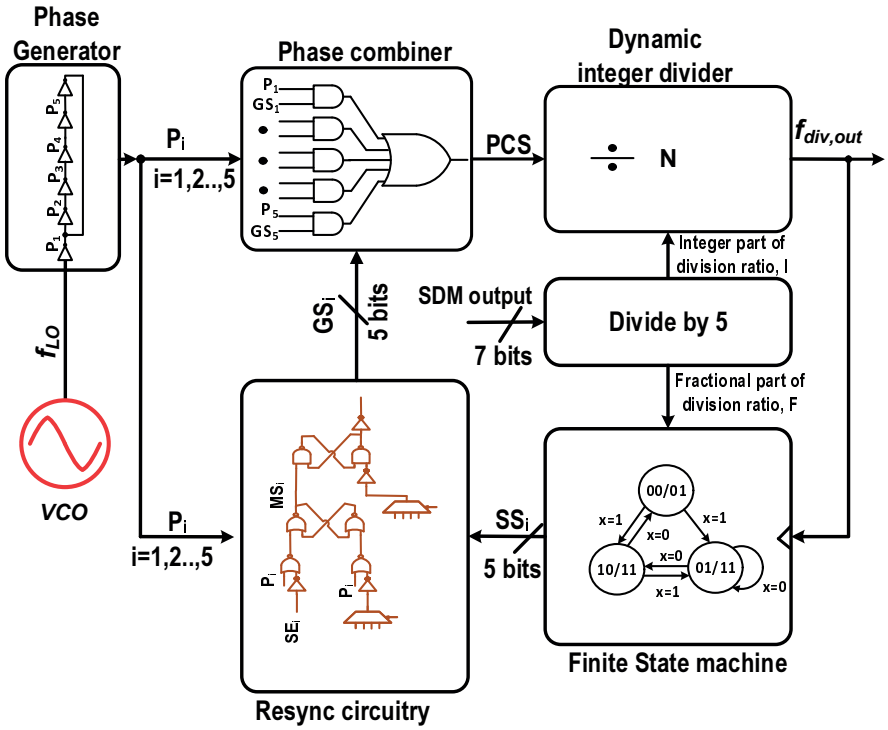



Figure 2.8 – Block diagram of the phase switching fractional-N divider

### 2.6.1 Phase generator

There are various ways to generate multiple phases of a given signal, of which injection locking offers many advantages as discussed previously. But the problem with single phase injection locking is that the node at which the locking signal is injected suffers from more capacitance (due to the extra inverter load) and consequently all the phases are not symmetrical. This asymmetry leads to spurs in the divider output spectrum. To circumvent this issue, multi-phase injection locking (where the first ring locked to the VCO uses all its phases to injection lock a second ring oscillator) is employed herein [16]. This multi-phase locking also has an advantage in that it increases the locking range and ensures that the lock is maintained in spite of the PVT variations. Since multi-phase injection locking is a basic recurring theme in this thesis, it is imperative to discuss the theory involved before progressing with the circuit description. This is done in the next section with a focus on the lock range extension of the multi-phase injection locking.

### Theory of multi-phase injection locking

Following the work of [17] and [18], let a ring oscillator with $N$ stages be assumed (where $N$ is odd). In this case, to maintain the Barkhausen criteria of $2k\pi$ (where $k$ is even) phase shift around the loop, each inverter contributes a phase shift of $\pi$ and the load at the output node of each inverter contributes a phase shift of $\pi/N$ as shown in figure 2.9 which also depicts the corresponding phasor diagram. Since the load consists of a parallel RC network, the phase shift introduced by the load shown in figure 2.9 can be written as

$$\pi/N = \tan^{-1}(\omega_0 R_L C_L). \tag{2.32}$$

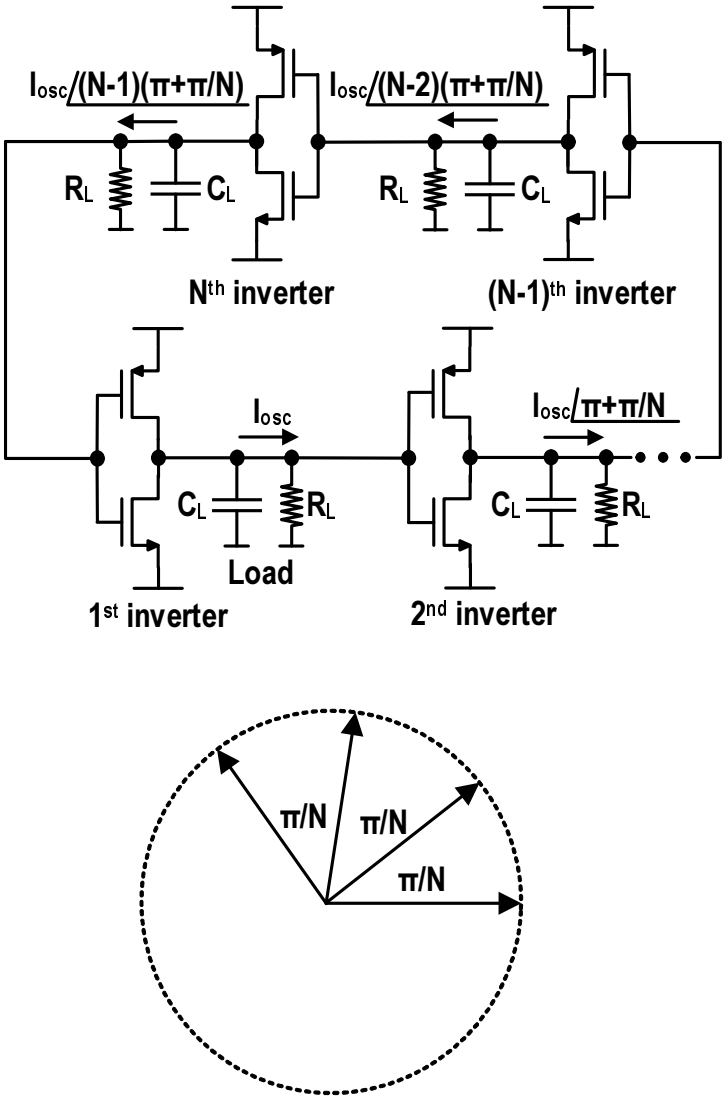



Figure 2.9 – Free running N-stage ring oscillator

Now, if an external signal is injected at one of the nodes producing a phase shift of $\phi$ at that node, then the load associated with the rest of the nodes should contribute an additional phase shift of $\theta$. Now to maintain the Barkhausen criterion, the phase equation around the loop becomes

$$\left(\pi + \frac{\pi}{N} + \theta\right) N + \phi = 2k\pi, \tag{2.33}$$

from which $\theta$ can be calculated as

$$\theta = -\frac{1}{N}\phi \tag{2.34}$$

In addition to causing an extra phase shift in the load, the injected signal also shifts the frequency of the oscillator from $\omega_0$ to $\omega$. Expressing the phase shifts in terms of circuit components gives

$$\frac{\pi}{N} + \theta = \tan^{-1}(\omega R_L C_L). \tag{2.35}$$

Rearranging this equation and expanding the right hand side using Taylor series in the vicinity of the natural oscillating frequency of the circuit $\omega_0$, the expression for $\theta$ can be deduced as shown in the following equation as

$$\theta \approx \frac{\omega_0 / R_L C_L}{1 + (\omega_0 / R_L C_L)^2} \frac{\Delta\omega}{\omega_0} \tag{2.36}$$

Substituting from equation 2.32 produces

$$\theta \approx \frac{\tan \pi / N}{1 + \left(\tan^2 \pi / N\right)} \frac{\Delta\omega}{\omega_0} \tag{2.37}$$

This phase shift can also be expressed in terms of the current phasors which are given in 2.10. With $I_{inj}$ being the injected current, $I_{osc}$ being the current phasor representing the oscillator and $I_T$ being the resultant phasor, it can be written with the aid of the figure that

$$\sin\phi = \frac{\left|I_{inj}\right|}{|I_T|} \sin(\alpha). \tag{2.38}$$

Writing the expression for the resultant renders the above equation as follows:

$$\sin\phi = \frac{\left|I_{inj}\right| \sin\alpha}{\sqrt{I_{osc}^2 + I_{inj}^2 + 2 I_{inj} I_{osc} cos\alpha}}. \tag{2.39}$$

The maximum of this injected phase corresponds to the edge of the locking range. This can be found by equating the derivative of equation 2.39 to zero which gives

$$\sin\phi_{max} = \frac{I_{inj}}{I_{osc}} \qquad \text{under the condition} \qquad \cos\alpha = -\frac{I_{inj}}{I_{osc}}. \tag{2.40}$$

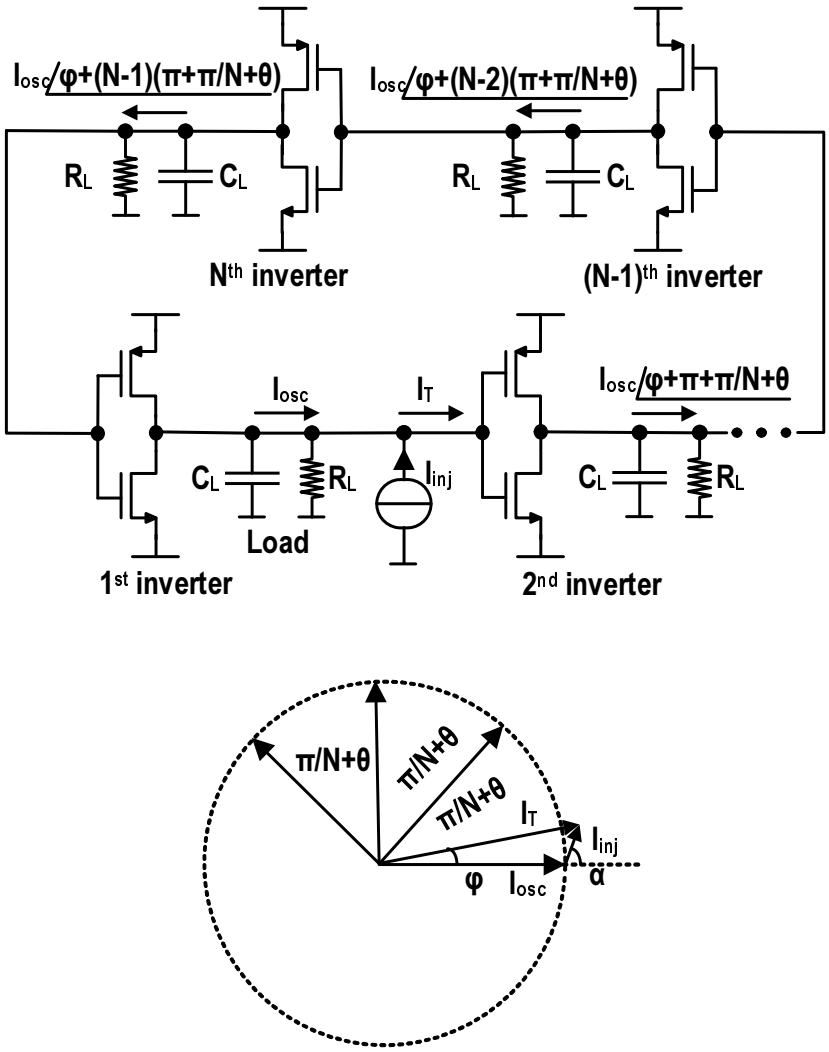



Figure 2.10 – N-stage ring oscillator with single-phase Injection Locking

From this, the inference can be made that at edge of the locking range, the phase difference between the load phasor and the phasor of the injected current is 90°. The phase shift of the tank in the vicinity of the resonance at the edge of the locking range is $tan\phi_{max}$. Assuming small signal injection, the phase shift of the tank is given by

$$\phi_{max} = \frac{I_{inj}}{I_T} = \frac{|I_{inj}|}{\sqrt{|I_{osc}|^2 - |I_{inj}|^2}} \tag{2.41}$$

Substituting equation 2.41 and equation 2.37 into equation 2.34 gives the expression of locking

range to be

$$\left.\frac{\Delta\omega}{\omega_0}\right|_{multi-phase} \leq \frac{1}{N}\cdot\frac{1+\left(\tan^2\pi/N\right)}{\tan\pi/N}\cdot\frac{\left|I_{inj}\right|}{\sqrt{|I_{osc}|^2-\left|I_{inj}\right|^2}} \tag{2.42}$$

This equation tells the reader that the locking range of the ring oscillator is heavily dependent on the number of stages $N$ and with higher number of stages, the locking range diminishes. Intuitively it can be argued that the phase shift produced by the injected signal compensates the phase shift of the load belonging to all the $N$ stages so that the total phase shift around the loop still remains $2\pi$.

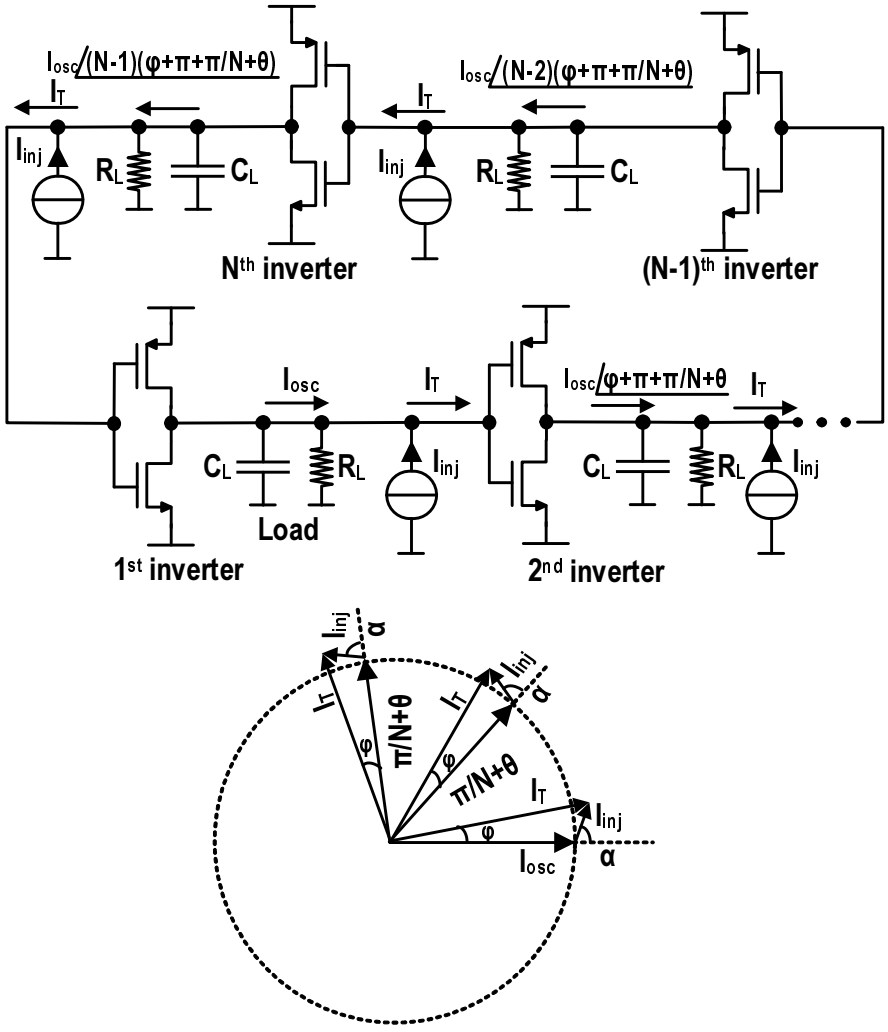



Figure 2.11 – N-stage ring oscillator with multi-phase Injection Locking

Now for the same $N$ stage ring oscillator, let $M$ nodes be injected with currents with progressive phases as shown in figure 2.11. Then, the phase shift contributed by the injected currents is

$M\phi$. The relationship between $\theta$ and $\phi$ is now

$$\theta = -\frac{M}{N}\phi. \tag{2.43}$$

Using the methodology previously followed, the locking range of the multi-phase injection locking can be calculated as

$$\left.\frac{\Delta\omega}{\omega_0}\right|_{multi-phase} \leq \frac{M}{N}\cdot\frac{1+\left(\tan^2\pi/N\right)}{\tan\pi/N}\cdot\frac{\left|I_{inj}\right|}{\sqrt{|I_{osc}|^2-\left|I_{inj}\right|^2}}. \tag{2.44}$$

For the special case where $M = N$, i.e. when the number of locking phases is the same as that of the number of stages of the ring oscillator, the dependency of the locking range on the number of stages $N$ is greatly reduced. With sufficiently large $N$, the maximum possible locking range becomes dependent only on the amplitude of the injected signal as shown by the following equation

$$\left.\frac{\Delta\omega}{\omega_0}\right|_{multi-phase;M=N} \approx \frac{\left|I_{inj}\right|}{\sqrt{|I_{osc}|^2-\left|I_{inj}\right|^2}}. \tag{2.45}$$

In other words, the phase shift of each of the inverter load can more easily compensated by the multiple phases so as to satisfy the Barkhausen criterion. In other words, the ring can tolerate a larger phase shift and consequently a larger locking range. One thing to be noted in the above discussion is that the order of the injected phases plays an important role in determining the lock range of the circuit and hence sufficient simulations need to be performed by the designer to ensure that the maximum lock range is obtained.

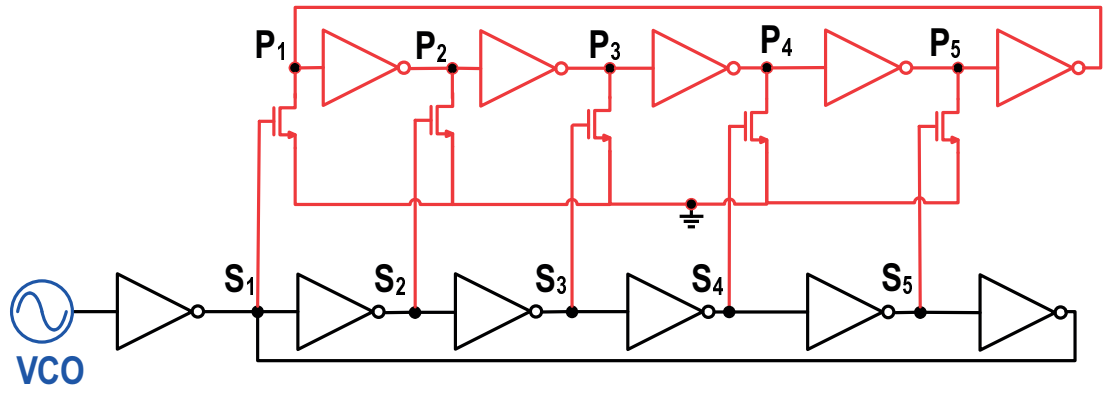



Figure 2.12 – Injection Locked Ring Oscillator

Coming to the PSD described herein, the VCO injection locks a 5 stage ring oscillator using standard CMOS logic inverters to produce phases that are separated by $0.2/f_{VCO}$. This is followed by another 5 stage ring oscillator that is injection locked to the first ring as shown in 2.12, whereby any phase asymmetries are removed. In theory, the second ring oscillator

could have any multiple of the number of stages in the first ring. For instance, in this case, the second ring can have 5,10,15 stages and so on. This modularity of multi-phase injection locking to produce the phases makes this circuit quite attractive to further QN reduction without having to worry about power hungry buffers after the VCO to ensure sufficient signal strength to maintain lock over PVT variations.

### 2.6.2 Finite State machine and phase combiner

The Finite State Machine (FSM) operates based on the state equations given in Figure 2.13. A sample state transition graph is provided in figure 2.14. The inputs to the FSM are the outputs of the SDM which sets the momentary division ratio and a clock which is obtained from the output of the divider itself ($f_{out}$ in Figure 2.8). The outputs of the SDM are divided by 5 and the quotient (which is the integer part $I$ of the division ratio) is fed to the dynamic divider while the reminder (corresponding to the fractional part, $F$) goes to the FSM. The FSM outputs select signals each of which corresponds to selecting a particular phase from the phase generator. This phase selection is performed by ANDing the select signals with their respective phases and the resulting signals are ORed and this signal called $S_{sum}$ is fed as an input to the succeeding divider chain set to the desired integer. In the case of the division ratio being just an integer, the fractional bits are set to '0' and the state machine retains its current state, thereby implying there is no phase switching.

### 2.6.3 Dynamic Integer divider

The starting point of the design of the dynamic divider is the fact that a D-Flip flop (DFF) whose output is inverted and looped on itself serves as a frequency divider by 2. If the flip-flop is constructed using True Single Phase Clocked (TSPC) latches, then with slight modifications to the circuit, it could also be made to divide the frequency of the input signal by 3. Figure 2.15 shows the TSPC divider for divide by 2 operation along with the chronogram. The structure of the circuit is slightly different as compared to a TSPC DFF by adding an extra PMOS $M_2$ on top of the second latch. By adding an NMOS $M_{10}$ to the first latch and a PMOS $M_3$ to the third latch transforms this circuit into a divide by 3 stage (2.16). In this configuration, the internal nodes **a**,**b** and **c** can never be logic '0' or logic '1' simultaneously. Therefore a divider that can divide by 2 or 3 can be constructed from figure 2.16 by adding switches in parallel with $M_3$ and $M_{10}$ respectively. By turning on these switches, the aforementioned transistors are effectively shorted leading to a divide by 2 operation. The modified divide by 2/3 circuit is shown in figure 2.17. In this circuit the control signal $div_{val}$ allows the switching of the division ratios. The circuit operation in its default case of divide by 3 is as follows: Let the initial state of node **b** be '0'. Now when the input clock goes low, then node **b** will rise to '1' since both the PMOS $M_2$ and $M_5$ are $ON$ and their corresponding NMOS are $OFF$. Similarly, when the input clock goes high next, node **c** will become '0' and the cycle continues. In the divide by 2 mode, the switches $M_{s1}$ and $M_{s2}$ are turned on, which ensure that one clock cycle is swallowed (corresponding to the shaded region in 2.16). Care should be taken that the $div_{val}$ signals do not change during

N0 = C1 C2 F0' F1 F2 + C1' C2 F0 F1' F2' + C1 C2' F0' F1' F2 + C0 F0' F1' F2' + C0' C1' C2' F0' F1 F2' + C0 F0 F1 + C0 F0 F2

N1 = C1 C2 F1 F2' + C1' C2' F0 F1' F2' + C0 F0' F1 F2' + C1' C2 F0' F2 + C0' C1' F0' F1' F2 + C1 F0 F1 + C1 F0 F2 + C1 F0' F1' F2' + C1 C2' F1 F2

N2 = C1 C2 F1' F2' + C2 F0 F2 + C1' C2 F0' F1' + C0 F0' F1 F2' + C0 F0' F1' F2 + C1 C2' F0' F1 + C0' C1' C2' F0 F1' F2' + C0' C2' F0' F1 F2 + C2 F0 F1

Legend: C2 C1 C0 → Three bit representation of current state

N2 N1 N0 → Three bit representation of next state

For any phase P*i*, the binary representation of '*i*' is coded by the state variable.

For e.g. Phase 1, P1 → the state representation corresponding to selecting this phase is 001

F2 F1 F0 → Fractional part of the input division ratio

F2 F1 F0 = 000 → Fractional part = 0 i.e. integer division ratio

001 → Fractional part = 0.2

010 → Fractional part = 0.4

011 → Fractional part = 0.6

100 → Fractional part = 0.8

Figure 2.13 – State equations of the FSM

this cycle swallow phase lest glitches and instability in the divider will follow. By cascading a number of these divide by 2/3 stages, a dynamic divider chain with arbitrary division ratio can be built [19], [20].

At this point, it can be noted that this divider behaves as a ring oscillator that is injection locked to the third harmonic of the output signal. Therefore, the circuit exhibits a frequency locking range of the input signal whose upper limit is set by three times the self oscillation frequency of the ring oscillator formed by the three inverters. The main advantage of this circuit is that it is capable of high speed operation due to the dynamic TSPC latches which form the basis of this divider. An important effect to note is the charge sharing from the output nodes to the intermediate nodes. This is exacerbated in this case due to the dynamic nature of the circuit as well as the high frequency of operation. For instance, charge sharing between nodes **p**, **q**, **r** and **s**, **t**, **u** respectively in figure 2.17 causes the output node voltage to decay with time. This is shown in figure 2.18 (adopted from [19])which depicts the case of the a dynamic half latch with significant parasitic at the intermediate node. For instance, when the input clock is low and there is a low to high transition at the input of the inverter, ideally the output signal $V_{out}$ should remain unaffected. But due to the parasitic capacitance at the intermediate node $s$, there is a charge sharing effect (since $M_7$ is ON) and the $V_{out}$ degrades and the voltage

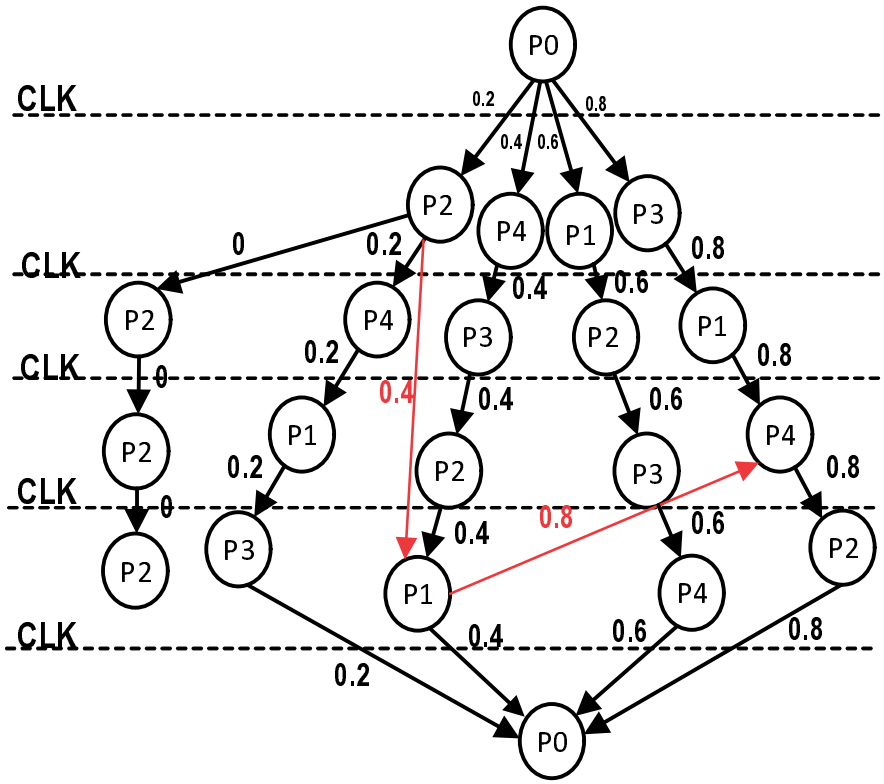



Figure 2.14 – State transition graph of the state machine

at $s$ increases. If this parasitic capacitance is of the same order of magnitude as that of the output node, then $V_{out}$ degrades to half the supply voltage which may not be sufficient to drive the next stage. Therefore, care should be taken in sizing these transistors to minimize this effect. Further, careful post layout simulations need to be performed to ensure that this charge sharing effect is minimal for high speed clock inputs.

### Constructing the dynamic divider chain

The programmable divider chain circuit is based on the recursion method introduced in [21] and is shown in figure 2.20. The main advantage of this idea is that it prevents 2/3 division ratio control signals from switching at inappropriate times as well as ensuring glitch free operation when the division ratios are changed. Starting from the last stage, this divider chain generates validation signals denoted by $M_i$ (corresponding to the $mod_{in}$/ $mod_{out}$ signals of each slice) which control when the divider slice is to divide by 2 instead of dividing by 3. This is shown in figure 2.19 which depicts the recursive validation signals for the maximum division ratio 15 that is possible for the divider chain of figure 2.20.

The circuit level implementation of this idea is shown in 2.21. At each dual modulus divider slice, a $mod_{out}$ signal is generated from the nodes **a & c**, a $mod_{in}$ signal (which corresponds to the $mod_{out}$ signal from the succeeding slice) and the binary input bit of the division ratio,

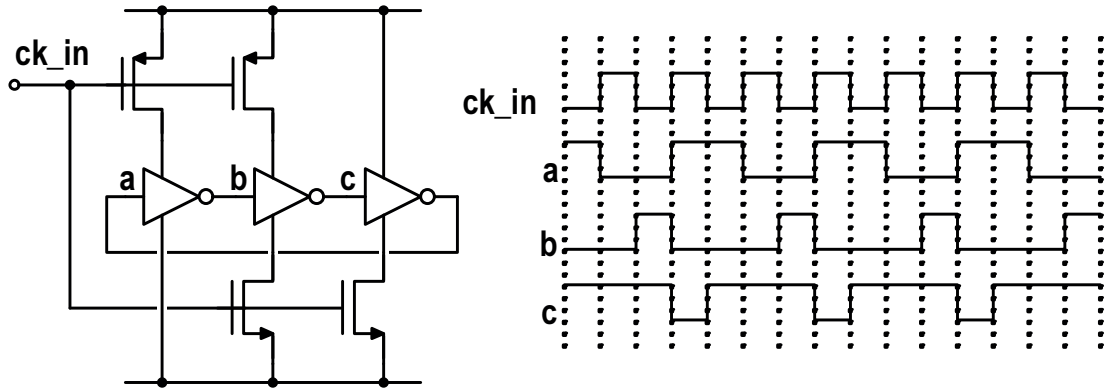



Figure 2.15 – Divide by 2 timing diagrams

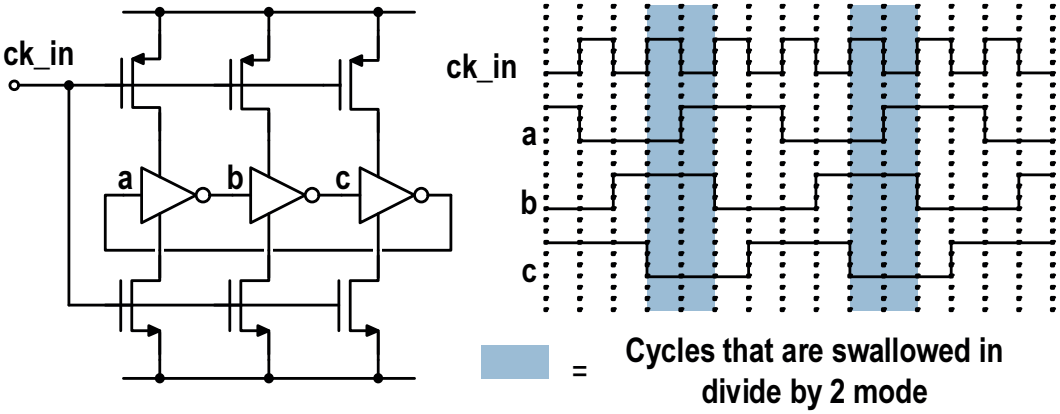



Figure 2.16 – Divide by 3 timing diagrams

$p$. This signal is resynchronized by the falling edge of the input clock by a simple dynamic latch and fed to the previous stage. The resynchronization helps to reduce the accumulated jitter along the chain so that when the $mod_{out}$ signal of the first stage is taken as the divided output clock signal, it is free of jitter. The $mod_{in}$ signal of each stage also controls whether the dual modulus divider divides by 2 or 3. Furthermore, the signal at node **a** (which serves as the input to the next stage) is clock gated and controlled by the signal $ppp$ so that the succeeding divider stages are enabled or disabled according to the division ratio. Signal $pp$ also assists in enabling / disabling the stages based on the division ratio. As shown in figure 2.23, the $pp$ signal of the last stage is the MSB of the division ratio. The $ppp$ signal is set to $'0'$ and so is the $mod_{in}$ for this last stage. The maximum division ratio possible with this divider is $2^{N+1}-1$ where $N$ is the number of divider slices.

The main issue with this implementation of [19] is the duty cycle of the output clock is inversely proportional to the division ratio. This can be clearly seen in figure 2.19, where the $mod_{out}$ signal of the first stage, $M_0$, which is the output clock of the system has a very low duty cycle. In combination with the fractional nature of the divider output signal, this leads to large far offset spurious spectral content. This is usually not a problem for the operation of PLLs per se,

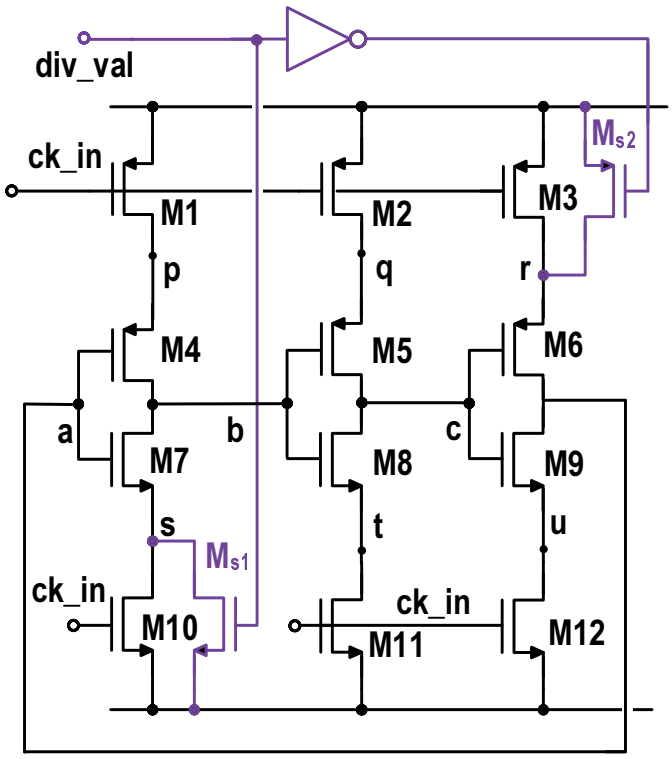



Figure 2.17 – Basic Dynamic divider slice

since the PFDs use only the rising (or falling) edge of the divider. But in reality, the spectral content may couple through the supply and cause unwanted spurs. Therefore, it requires the layout to be carefully planned to avoid such coupling. Furthermore, the lower the duty cycle, the larger the buffer needed to achieve reliable drive strength for clocking the SDM and hence leading to larger power dissipation. Therefore, to solve this problem, another signal which has near 50% duty cycle can be recursively generated from the internal signals of the divider as shown in figure 2.22. This is the $mod\_valid$ signal which is recursively modified by the successive stages and resynchronized to the input clock of each stage. The $mod\_valid\_out$ signal of the first stage after resynchronization by the input signal of the dynamic divider (this signal is the output of the PC) gives the output clock as depicted in figure 2.23. The duty cycle $D$ of this modified output signal is then given by

$$cD = \frac{2^{(L-1)} + K \, mod \, 2^{(L-1)}}{K} \tag{2.46}$$

$$\text{with} L = floor\,(log_2(K)) \tag{2.47}$$

and $K$ being the division ratio. The duty cycle thus obtained varies between 33% and 66% with division by powers of 2 yielding 50% duty cycle. This formula is true only if the PSD is set to divide by an integer. If the PSD divides by a fraction, then the duty cycle varies between 30%

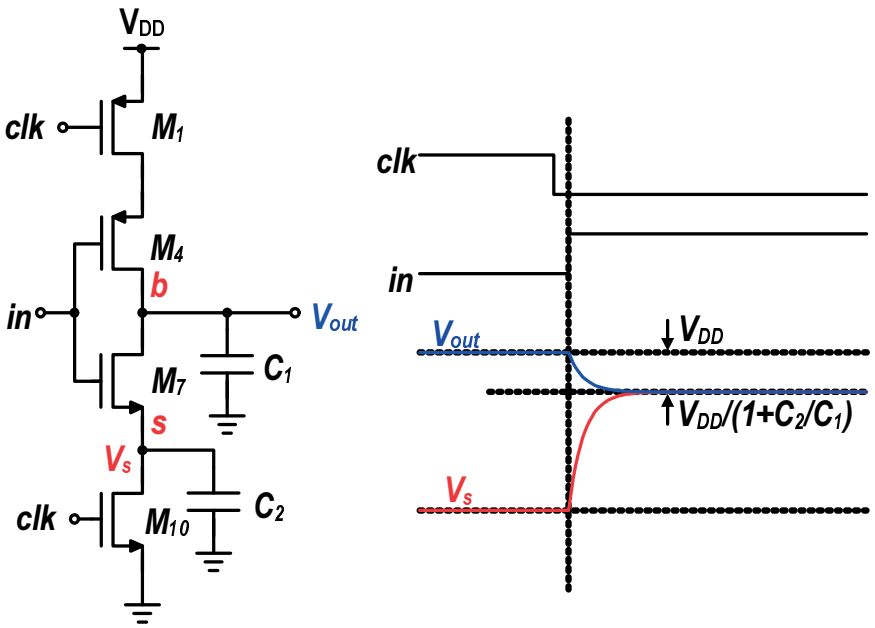



Figure 2.18 – Charge sharing in the dynamic latch due to parasitics

and 70%. The block diagram of the total divider chain is given in figure 2.23 for the reader's reference.

### 2.6.4 Resynchronization circuit

The select signals produced by the FSM must be resynchronized with respect to their corresponding phases so as to avoid glitches in the divider output. This is essential since the select signals may experience relative difference in interconnect delays as well as mismatches and PVT variations, all of which affect their transition times. This issue is dealt with by the Resynchronization block which retimes the select signal with its phase and makes sure that there are no dead times between the select signals (i.e. during the time when no select signal is $high$). Ideally, the select signals corresponding to each phase must go low immediately after the previous select signal becomes high to avoid glitches in the output and subsequently wrong output frequency. But this usually is not the case since different interconnect parasitics delay each select signal differently. To study the effects of these unequal delays, the division ratios are grouped into two categories *viz.* a) $F < 0.5$ and b) $F > 0.5$ ($F$ being the fractional part of the desired division ratio). The case where $F = 0$ is trivial since it does not involve any select signal transition. But, before going into the timing analysis, the terminology used for studying the glitches needs to be explained:

- A phase signal is called a ***Current Phase*** ($P_i$) when the select signal (SS) corresponding to that phase undergoes a 'high' to 'low' transition in any particular observation interval and that SS itself is called the ***Current Select Signal***, $SS_i$.

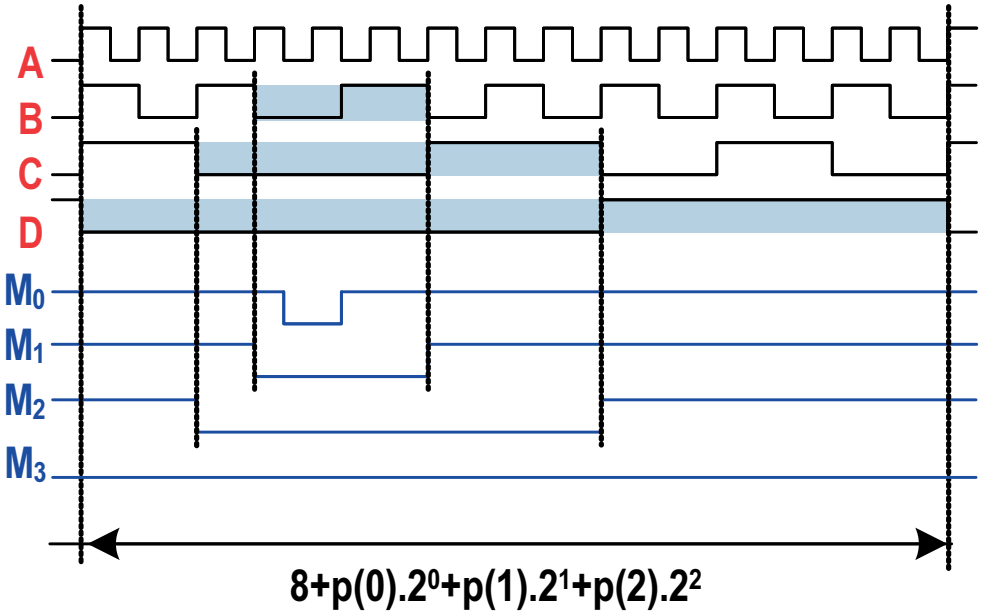



Figure 2.19 – Chronogram of the internal signals of the divider chain of figure 2.20

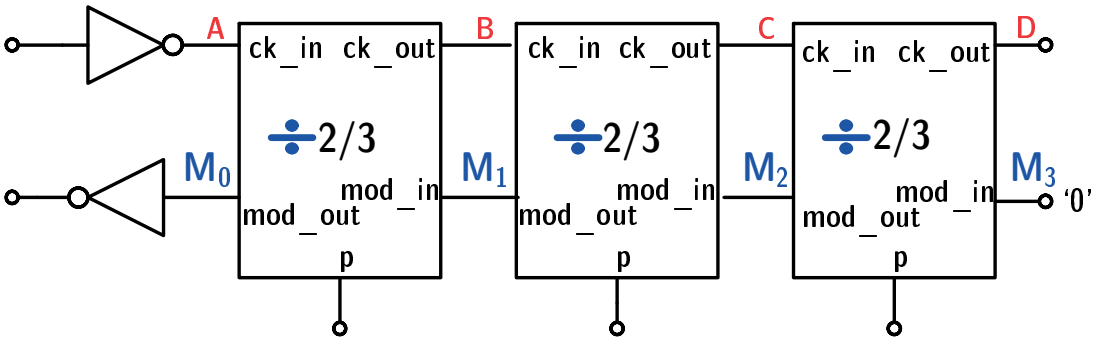



Figure 2.20 – Dynamic divider chain - Basic block diagram

- A phase signal is called a ***Next Phase*** ($P_{i+1}$) only when its corresponding select signal undergoes a 'low' to 'high' transition in the same observation interval and this SS is denoted as the ***Next Select Signal***, $SS_{i+1}$.
- The cycle of the phases when the transitions happen is called the ***current cycle*** and the cycle just before the transition is called the ***previous cycle***.

Fig. 2.24 further shows these terminologies graphically. Now, within the current cycle, one can identify four regions during which the select signal transitions from the state machine can take place *viz.*

1. when both phases are high.
2. when the current phase ($P_i$) is low and next phase ($P_{i+1}$) is high.

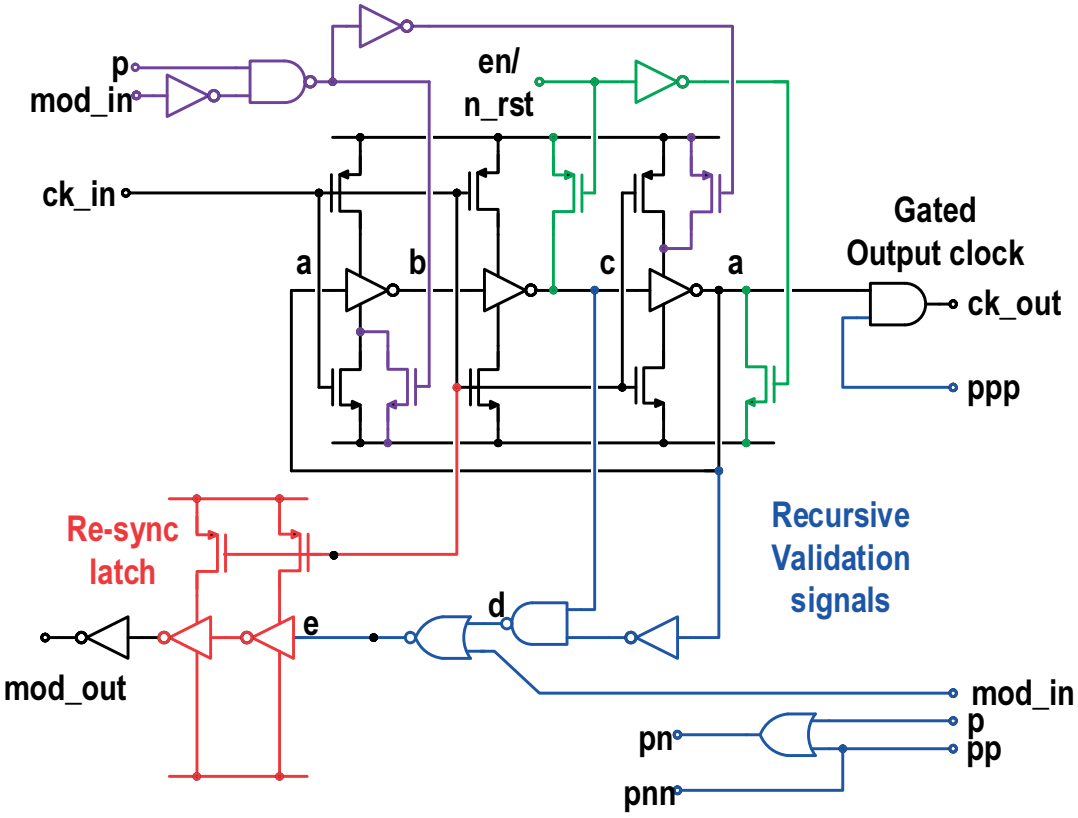



Figure 2.21 – Dynamic Divider slice with recursive feedback gates

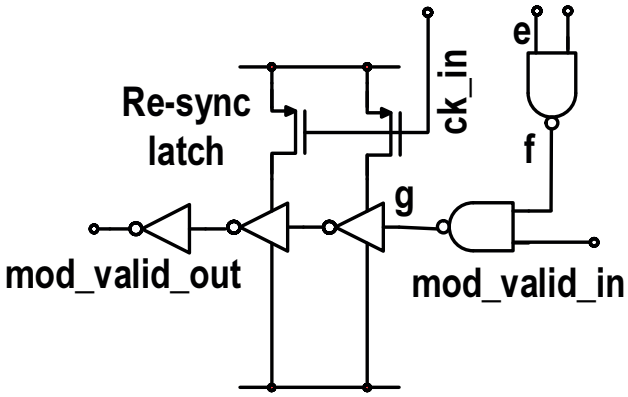



Figure 2.22 – Duty cycle correction circuit for the dynamic divider slice

3. when both phases are low.

4. when $P_i$ is high and $P_{i+1}$ is low.

This is shown in Fig. 2.25, for both cases *i.e.* $F < 0.5$ and $F > 0.5$.

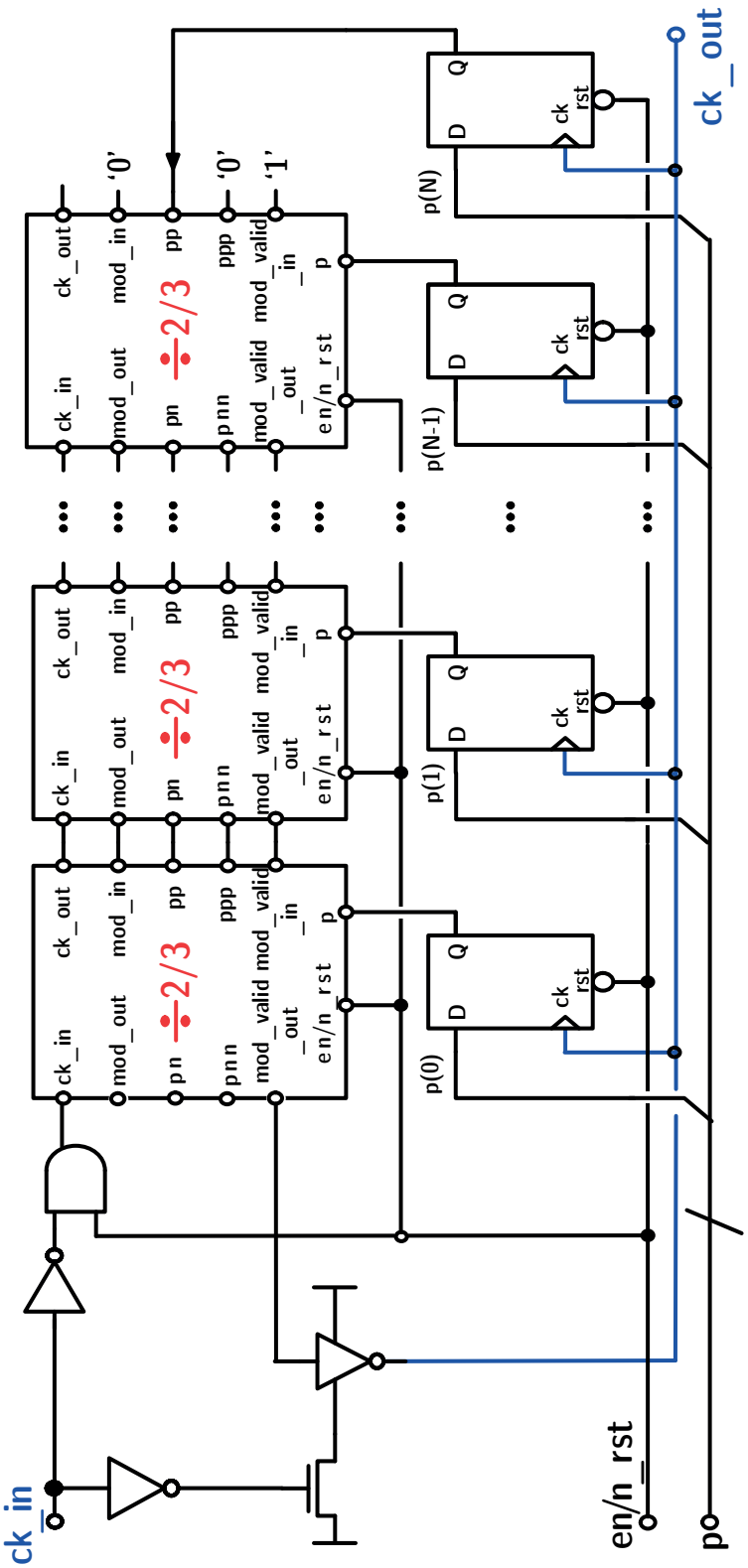



Figure 2.23 – Dynamic divider chain - synoptic view

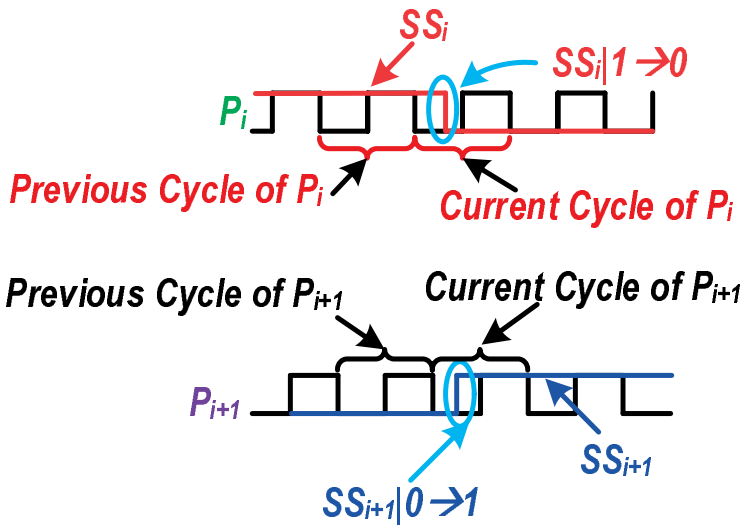



Figure 2.24 – Terminology used for select signals and phases

Now, to ensure a that glitch-free operation, the following conditions must be ensured:
Current select signal ($SS_i$) transition from high to low ($SS_i|high \rightarrow low$) should occur

(i) Case: when $F < 0.5$

1. when $P_i$ is low in its **current cycle**, provided $SS_{i+1}|low \rightarrow high$ occurs when $P_{i+1}$ = high / low in its current cycle or
2. when $P_i$ is high in its **current cycle**, provided $SS_{i+1}|low \rightarrow high$ occurs when $P_{i+1}$ = low in its current cycle or
3. when $P_i$ is high in its **previous cycle**, provided $SS_{i+1}|low \rightarrow high$ occurs when $P_{i+1}$ = low / high in its current cycle.

(ii) Case: when $F > 0.5$

1. when $P_i$ = low / high in its **current cycle**, provided $SS_{i+1}|low \rightarrow high$ occurs when $P_{i+1}$ = high / low in its current cycle or $P_{i+1}$ = high in its previous cycle or
2. when $P_i$ = high in its **previous cycle**, provided $SS_{i+1}|low \rightarrow high$ occurs when $P_{i+1}$ = low in its current cycle.

In reality, due to the difference in interconnect capacitances, these transitions arrive at inopportune or different times, the result of which are glitches in the PCS that propagate to the divider chain, leading to an erroneous division ratio. To illustrate this, figure 2.26 shows two different instances of SS transitions in the case when $F = 0.4$. Here, if the select signal transition occurs in either region 2 or 4, any slight mismatch in the delay of the present and

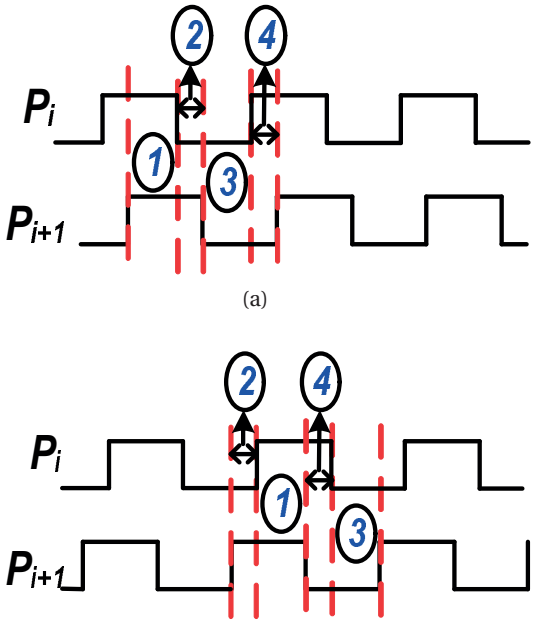


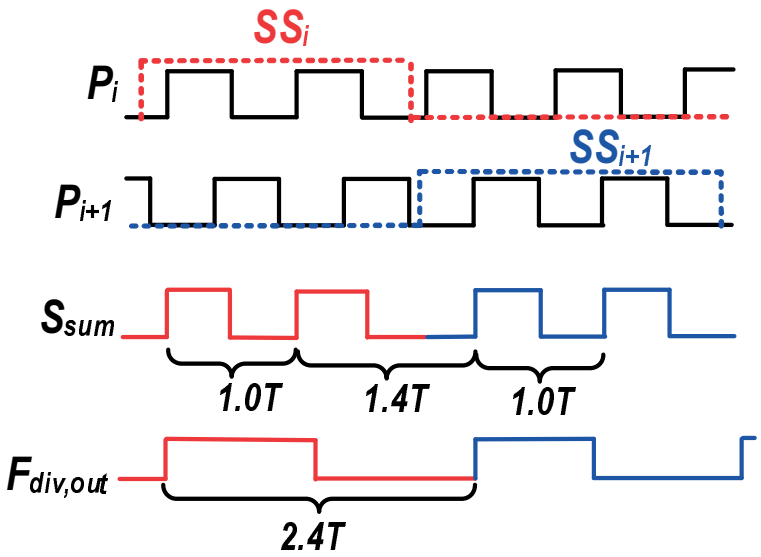

Figure 2.25 – Possible Time intervals (regions) for select signal transitions (a) $F < 0.5$ (b) $F > 0.5$

the next SS will result in glitches at the output, while the glitches are absent if the transitions are in regions 1 and 3.

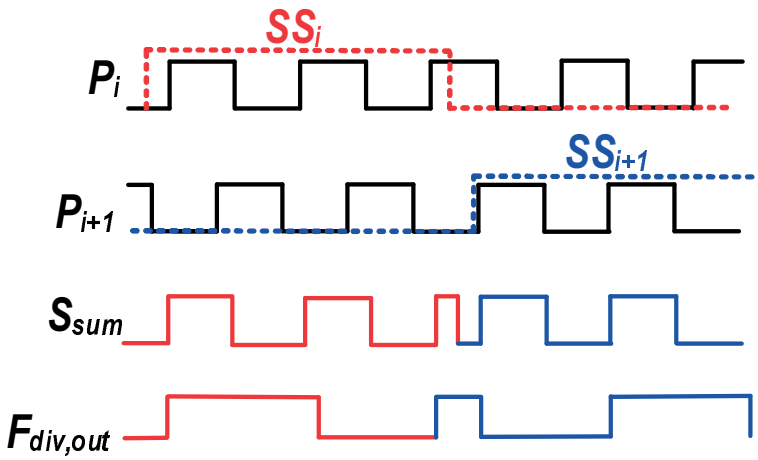
For $F = 0.8$ ($F > 0.5$ case), these transitions are shown in Figure 2.27. In this case, the select signal transitions in regions 3 and 4 result in correct division ratio. But if the transitions occur in regions 1 and 2, then the PCS will have more than the intended $0.8T$ in that cycle and less than the intended $1.0T$ in the next cycle. Therefore, when passed through the divider chain, this incorrect $S_{sum}$ will lead to a temporarily incorrect division ratio, but on average a correct division ratio will result, as seen in figure 2.27b. Here the output of the divider chain will have successive time periods of $1.9T$ and $1.9T$, leading to an elapsed time period of $3.8T$ which is the same if the division ratio was 1.8 and 2.0 in the two cycles under observation.

The importance of proper layout cannot be stressed enough for avoiding glitches. Bad layout may cause large delays between select signals, making it very difficult to design the retiming circuit. For instance, if the $SS_i|low \rightarrow high$ transition is late by one time period of $P_i$, then the resulting $S_{sum}$ signal will skip one cycle of $P_i$, resulting in a wrong output frequency. Further, the rise and fall times of these signals (which are dependent upon voltage and other ambient conditions) can be expected to further degrade the accuracy of the output frequency and hence they should also be taken into account when designing the retimer.

Coming to circuit design, among the previously mentioned conditions for glitch-free operation, the first condition for both cases ($F < 0.5$ and $F > 0.5$) can be satisfied by using flip-flops which are clocked by the corresponding phases themselves. In the case of $F < 0.5$ each of the



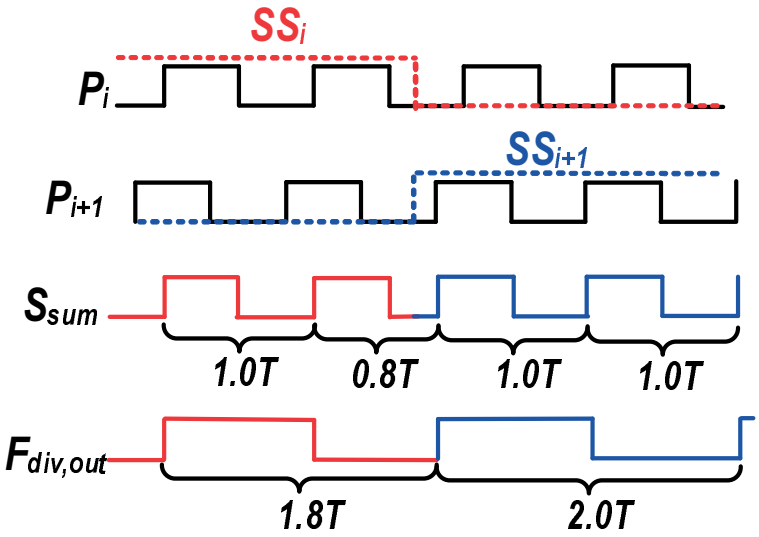

(a) Transition in region 3 : Glitch free operation



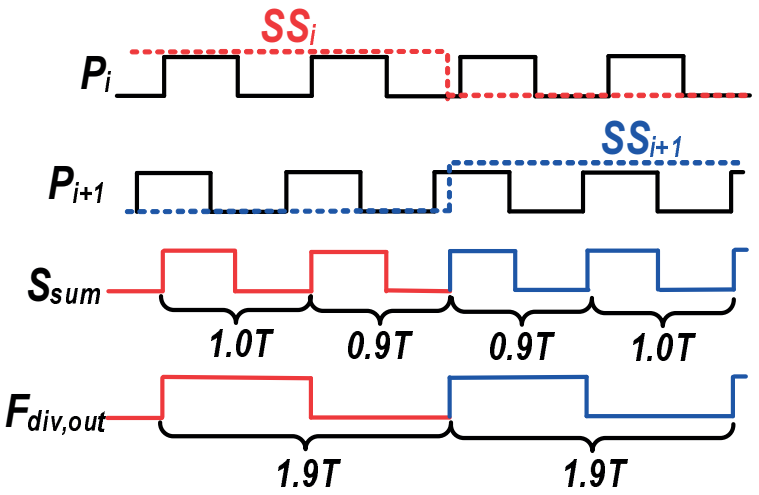

(b) Transition in region 4 : Glitch and Incorrect division ratio

Figure 2.26 – Select Signal Transition diagrams for $F = 0.4$ case

incoming select signal from the state machine must pass through a positive edge triggered flip-flop followed by a negative edge triggered flip-flop clocked by its own phase. The flip-flop order is reversed in the case of $F > 0.5$. Thus this approach uses 4 flip-flops, two each of which trigger on the opposite clock edge. These flip-flops could be combined into 2 double edge triggered flip-flops or using only 2 flip-flops and 6 AND gates and 3 OR gates, as shown in figure 2.28. The problem of using flip-flops is that the setup time becomes a major issue. Even though this can be solved by using low threshold transistors, the leakage and the power consumption will go up in this case. Therefore, there is a need to find a much easier solution for resynchronization.




(a) Transition in region 3 : Correct operation




(b) Transition in region 2 : Incorrect momentary division ratio

Figure 2.27 – Select Signal Transition diagrams for $F = 0.8$ case

To achieve low power resynchronization, a latch-based resynchronization block is implemented for each select signal. In order to design such a circuit, it is observed from the aforementioned conditions for glitch free output that there exists one common condition pertaining to both $F < 0.5$ as well as $F > 0.5$. Therefore, a single resynchronization block would suffice to eliminate glitches. The condition for this can be summarized as: Both $SS_i$ and $SS_{i+1}$ should transition when their respective phases $P_i$ and $P_{i+1}$ are at logic low in the current cycle. Moreover, the transition of $SS_{i+1}$ can happen $P_{i+1}$ only after the transition in $SS_i$ has occurred. This will ensure that there is no dead time between the select signals which may potentially

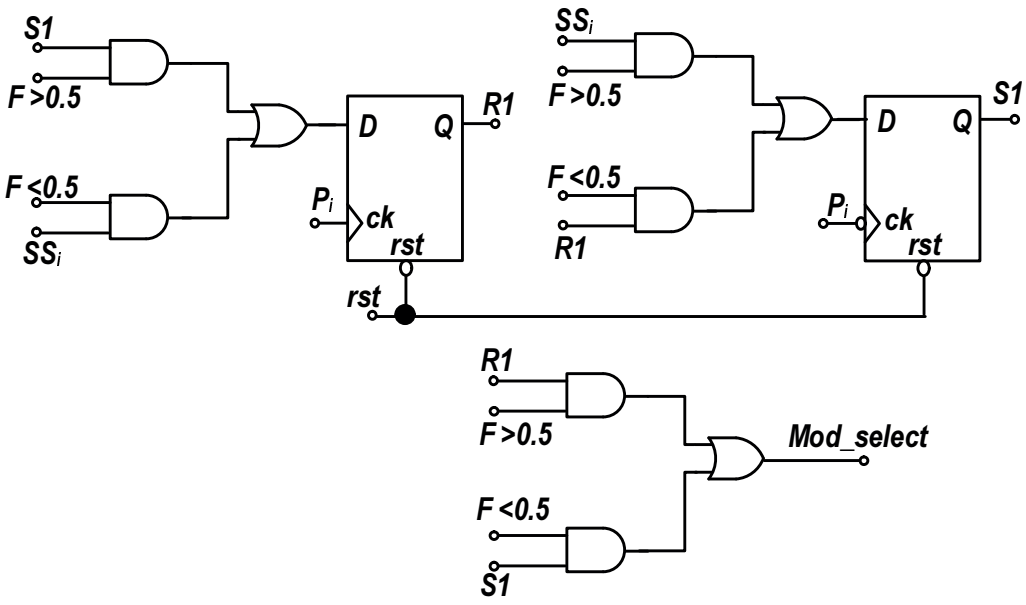



Figure 2.28 – Flip-flop based approach for resynchronization

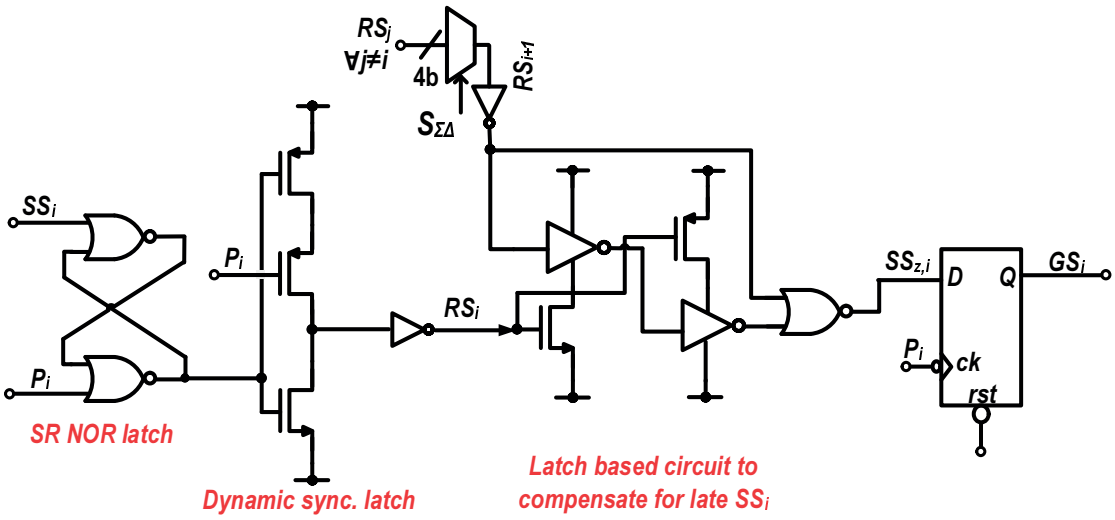



Figure 2.29 – Latch based low power resynchronization circuit

cause cycle skipping and therefore erroneous division ratio. To begin with, the transitions in both $SS_i$ and $SS_{i+1}$ are aligned to the 'logic low' period of their respective phases by using an SR NOR latch followed by a dynamic synchronization latch to produce a signal $RS_i$, as shown in figure 2.29. But this alignment does not ensure that the transitions happen in the current cycle of the respective phases i.e. cycles will not be skipped if $SS_{i+1}$ is late or if the select signal violates the setup time of the latch, as shown in the chronogram of figure 2.30. Hence, to solve this, the signal $RS_i$ in combination with the $RS_{i+1}$ signal corresponding to the next phase is used to produce a signal $SS_{z,i}$ which satisfies the condition of glitch free switching. The signal

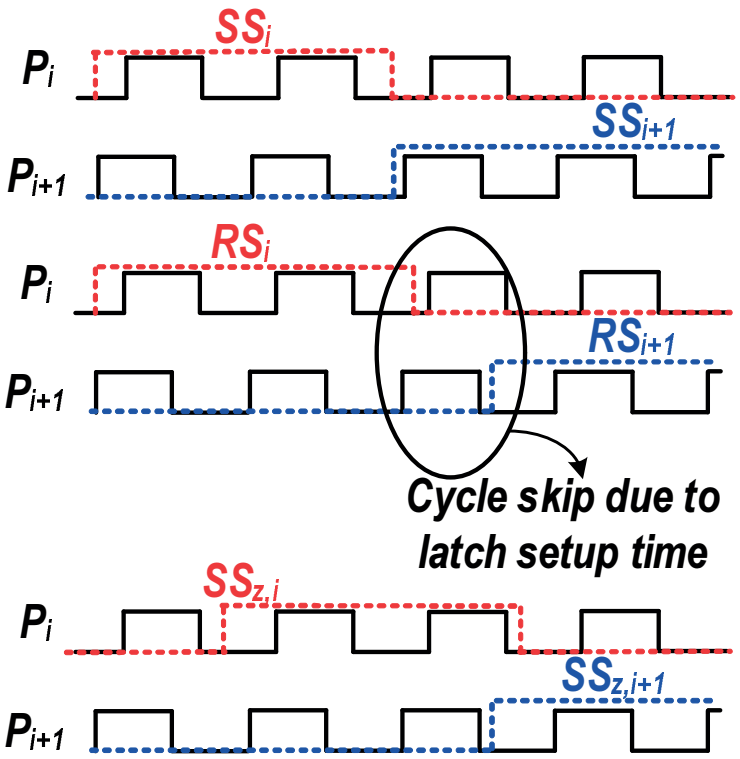



Figure 2.30 – Intermediate signals of the resynchronization circuit

$SS_{z,i}$ is passed through a negative edge triggered flip flop to neutralize the delay accrued while passing through the latches thereby producing the resynchronized signal $GS_i$ which is then passed on to the Phase Combiner. Compared to the resynchronization circuit used in [10], the employed circuit avoids any retiming of the phases themselves thus reducing the power dissipation to a great extent.

At this moment, it is imperative to state an important fact about the flip-flop design which has an impact on the phase combiner. As discussed previously, the division by a fraction greater than 0.5 involves phase switching in a retrograde order. This results in a very short $low$ / $high$ period of the pulse which may result in cycle skipping if the logic in the Phase Combiner is not fast enough. For example, in the case of a division ratio of 2.6, two cycles of the Phase Combined signal should have $1.0T$ each and the third cycle will have $0.6T$. But $0.6T$ means that the cycle will have $0.5T$ high period and just $0.1T$ low period. This low period amounts to just 40 $ps$ at 2.5 GHz, which is a very short time period for the phase combiner gates to operate with. Therefore, this part of the cycle will be skipped, leading to erroneous division. To solve this issue, the flip-flop has been modified to purposefully introduce a dead time of $1.0T$ between the select signals for $F > 0.5$ case, due to which if the PSD is set to divide by 2.6, it would do so by 3.6 instead. The inputs to the PSD are adjusted to deal with this change and thereby to get a correct division ratio.

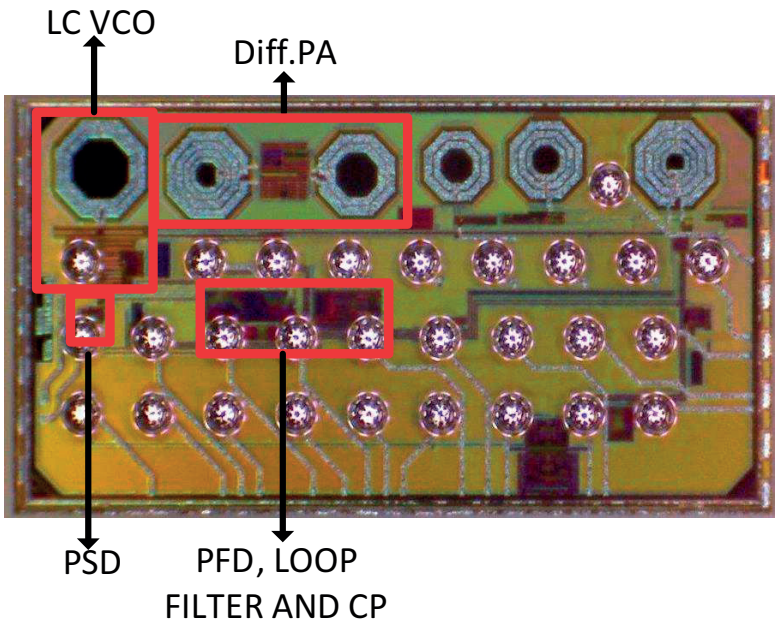



Figure 2.31 – Microphotograph of the chip showing the PSD and the PLL

## 2.7 Measurements

The proposed PSD along with a fractional-N PLL with an output frequency of 2.44 GHz have been integrated in CMOS 65 nm technology (chip microphotograph shown in figure 2.31). The PSD has a division ratio ranging from 4 to 31.8. In order to ensure that the amplitude of the VCO signal is sufficient to lock the ring oscillator of the phase generator at all PVT conditions, a simple push-pull buffer has also been implemented as a fail-safe mechanism. The reference frequency of the PLL was chosen to be 128 MHz which can be produced by either the third overtone of a crystal oscillator or dividing down the output of an FBAR. Such a high reference frequency was aimed towards high data rate applications for making the system attractive for duty cycling. The locking range of the ring oscillator was measured to be 2.16 GHz (from 1.44 GHz to 3.6 GHz) thanks to multi-phase locking. This is illustrated in figure 2.32 which shows the variation of the strength of the injected signal to lock the ring oscillator versus its frequency. Since the ring was designed to operate at a frequency of 2.4 GHz, the further the frequency of the locking signal is from this, the more the signal strength should be to establish lock. Another issue that needs to be taken care of is the supply voltage sensitivity of the ring oscillator. The ring oscillator in this design exhibited a sensitivity of 2.2 GHz/V as shown in figure 2.33. This high supply sensitivity means that unwanted spurious signals may potentially couple through the supply node and corrupt the output spectrum. Therefore, care should be taken to avoid this by implementing a voltage regulator to improve the Power Supply Rejection Ratio (PSRR) of the circuit.

Coming to the operation of the divider, figure 2.34 shows the divider output spectrum when

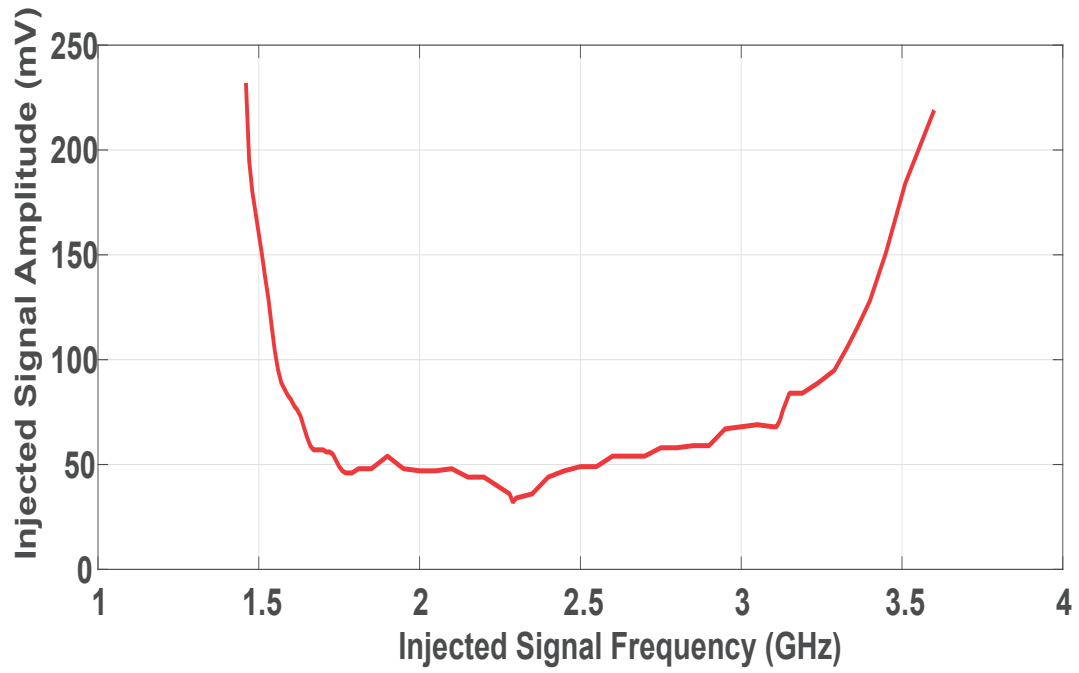



Figure 2.32 – Variation of the amplitude of the injected signal with its frequency

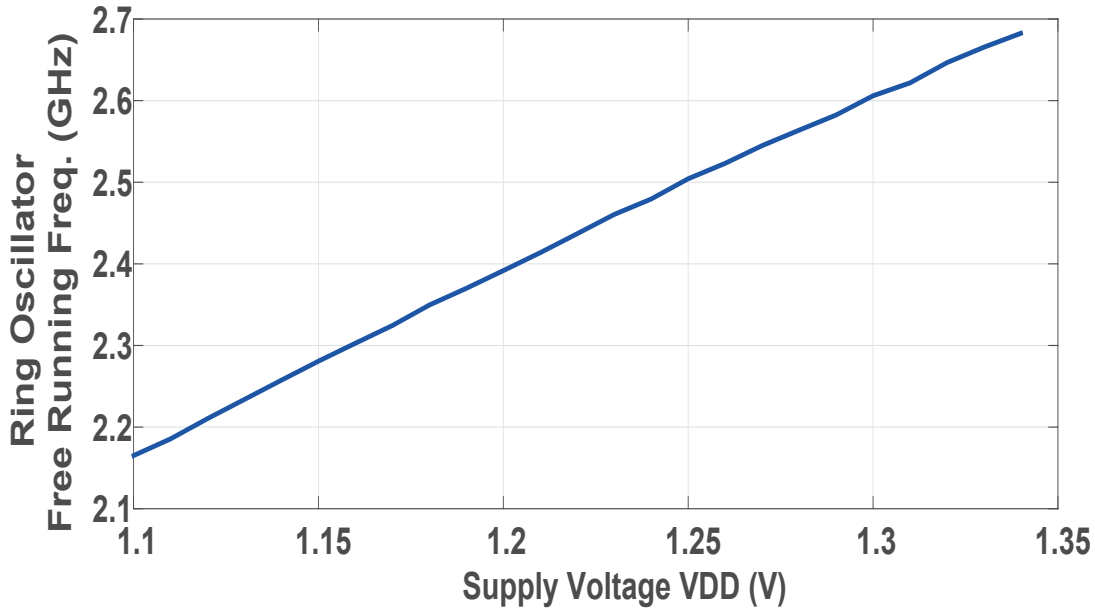



Figure 2.33 – Variation of the ring oscillator frequency with the supply voltage

the division ratio (DR) is varied from 24.6 - 25.6 for a 2.5 GHz input signal. As the division ratio step size is 0.2, one would expect to see fractional spurs at multiples of 0.2 times the output frequency, ($k * 0.2 * f_{out}$ where $k = \pm 1, \pm 2, ...$) as shown in figure 2.35. But since these

spurs are nearly 45 $dB$ below the wanted signal, they are usually filtered out by the PLL. In addition to this, the averaging performed by the SDM randomizes these spurs so that they are invisible in the divider output spectrum. For the division ratio 25, there are no spurs observed in the output spectrum due to the absence of phase switching. The time domain waveforms corresponding to the aforementioned division ratios are shown in figure 2.36. These waveforms clearly show that the duty cycle of the divider output in these cases is around 66% which is within the range mentioned earlier.

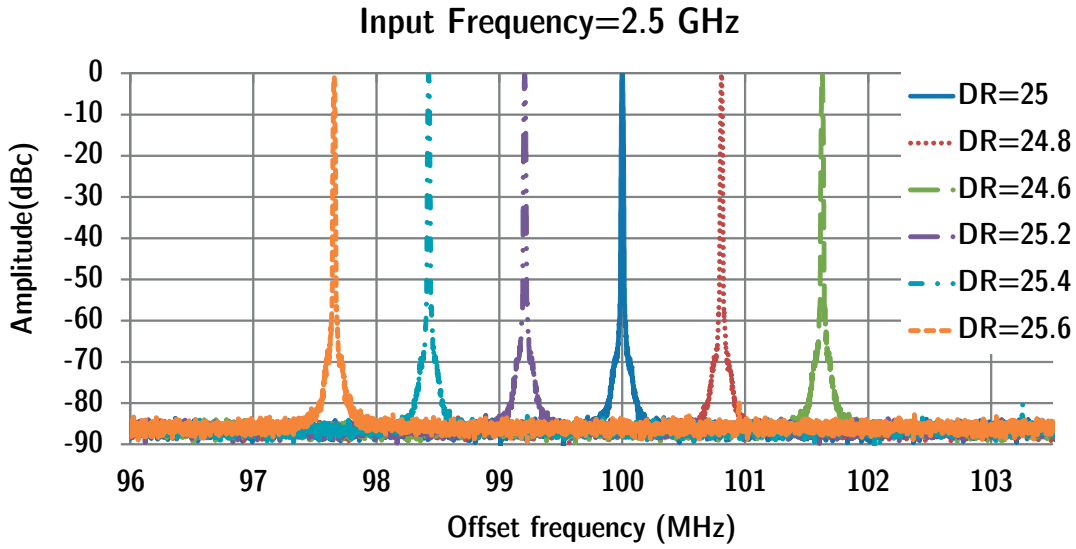



Figure 2.34 – PSD output - Division ratios 24.6 to 25.6 - close-in view

To evaluate the noise performance, this PLL was compared with a similar PLL (same architecture and same technology node) which utilized a conventional Integer Multi-modulus Divider (IMMD). Figure 2.37 shows the phase noise at the output of the divider in the case of both a PLL with a IMMD and a PLL with a PSD. The noise at this divider node is identical to the noise at the PLL output except that it is scaled down by a factor $20logN$, $N$ being the division ratio. Referring to the phase noise plot, it can be observed that the phase noise follows the noise of the reference in the low frequency range (<10 kHz) as expected. The slight difference in the noise of the two PLLs in this region is due to the difference in the flicker noise of the FBAR oscillator architecture used as the reference. At high frequency offsets (>1 MHz), the SDM QN becomes the dominant contributor to the PLL noise. In this region the measured noise in the case of the PSD shows a close match with that of the theoretical prediction by gaining 14 dB over the IMMD PLL corresponding to a reduction in the division step by a factor 5. At intermediate frequency offsets (10 kHz - 1 MHz) too, the PSD performs better by folding less noise as compared to the IMMD case thanks to the SDM QN reduction as discussed previously.

The proposed divider consumes 850 $\mu A$ at 1.1 V supply. The break-up of the consumption is as follows:

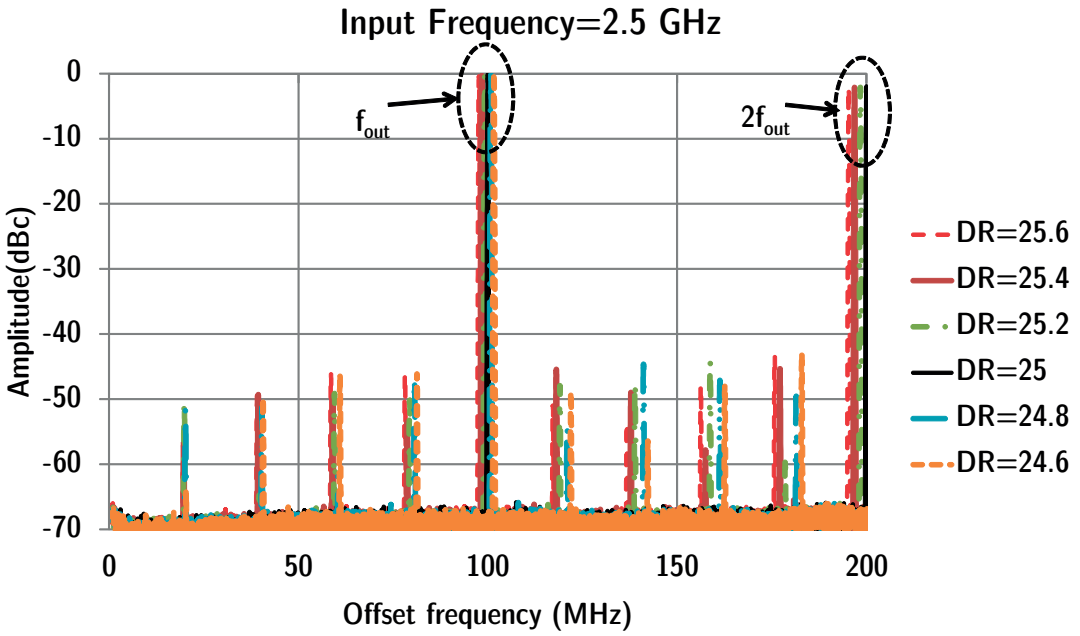



Figure 2.35 – Division ratios 24.6 to 25.6 showing spurs at multiples of 0.2 $f_{out}$

- Phase generator → 550 $\mu A$,
- Phase combiner and Dynamic Integer Divider → 220 $\mu A$,
- FSM → 30 $\mu A$.

Thus, one can see that the phase generator is the major power drain in the circuit. This is entirely expected since the high frequency phase generator outputs drive the combined load of the resynchronization circuit and the phase combiner.

Table I gives a comparison of the performance of the presented PSD with that of other PSDs in the literature. It can be established from the table that due to the fully CMOS nature of this synthesizer, this PSD consumes far less power as compared to this counterparts while also achieving a greater QN reduction. It should be noted at this stage that due to the digital nature of this PSD, it is greatly amenable to technology scaling, thereby enabling to further reduce the division ratio step (by increasing the number of stages in the ring oscillator of the phase generator) and consequently a greater QN reduction.

## 2.8 Summary and Prospective work

This chapter dealt with reduction in the Quantization Noise of the ΣΔ Modulator in fractional-N PLLs. Starting out by elaborating the effect of the SDM QN on the loop bandwidth and subsequently the data rate (in the case of single point modulation), the discussion then

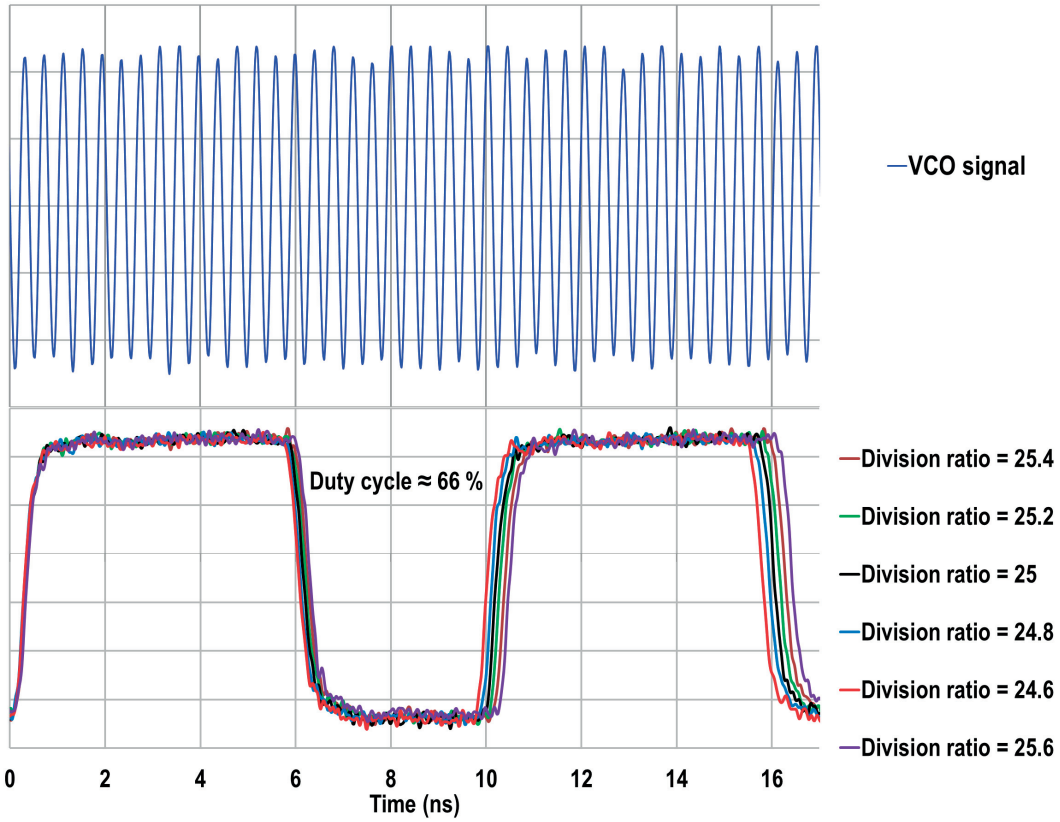



Figure 2.36 – Divider output waveforms showing division ratios 24.6 to 25.6

| Parameter | [14] | [13] | **This work** |
|---|---|---|---|
| PLL Frequency range | 0.8-3.8 GHz | 0.97-1.96 GHz | 2-2.6 GHz |
| Division ratio range | 30.5-510.5 | 36-83.5 | 8-31.4 |
| Division ratio step | 0.5 | 0.5 | 0.2 |
| QN reduction achieved | 6 dB | 6 dB | 14 dB |
| Power dissipation | 5 mA@1.8 V | 14 mA@1.8 V | 0.85 mA@1.1 V |
| Technology | 180 nm | 180 nm | 65 nm |

Table 2.1 – Performance comparison of the proposed PSD with prior literature

focussed on the phenomenon of noise folding due to charge pump mismatches that increases the noise floor within the loop bandwidth. This was followed by the section on the design of a Phase Switching Divider that has a division ratio step size of 0.2. The theory of multi-phase injection locking to remove asymmetries in the ring oscillator output as well as improve the locking range was also discussed. Following this, a low-power select signal resynchronization circuit was explained, which helps to avoid glitches and subsequently erroneous division ratios. The measurement results show that this divider is successful in reducing the QN by 14 dB as compared to a simple multi-modulus divider with a division ratio step of 1, as well as

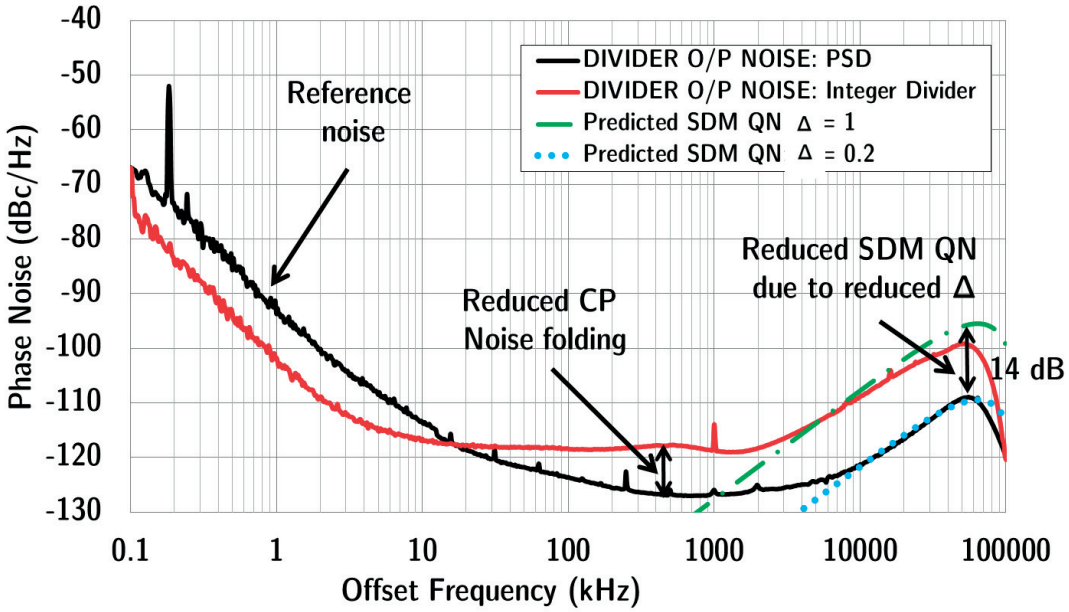



Figure 2.37 – Phase noise at the output of the divider

bringing about a significant reduction in the noise floor increase due to QN folding.

The prospective work needs to be focussed on further reduction of the PSD division ratio step size. It can be easily achieved by simply extending the number of stages of the second ring oscillator in phase generator. This would also involve improving the resynchronization circuit to further reduce the power consumption. Another area of focus that can be improved in the PSD is to reduce the effect of the supply voltage noise on the phase generator circuit. Apart from designing a Low Drop-out (LDO) regulator, current starved inverters can be used in the ring oscillator for better supply noise immunity.

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# 3 FBAR based Transmitters: Reducing the wake up energy overhead

A significant energy overhead due to the long wake up of the frequency reference is the major bottleneck in the use of conventional loop based synthesizers (like DPLLs [1] and MDLLs [2]) for duty-cycled ULP systems. Indeed, as discussed in the Introduction of this thesis, these frequency references usually consist of a quartz crystal possessing a wake up time of 0.5 $ms$ while consuming 1 $mW$ of power. The crystal oscillator (XO) startup overhead therefore reduces the impact of any increase in data rate for reducing power consumption by increasing the rate of duty cycling in ULP systems. Therefore it is necessary to look for an architecture that circumvents this energy overhead of the frequency synthesizer, thereby making a migration to higher peak data rates more effective. An interesting option to do so would be to eliminate the synthesizer loop itself, which in-turn eliminates the crystal based reference oscillator. Such an architecture would also avoid the settling time latency of the PLL, thereby greatly aiding the reduction of the energy overhead. Taking a closer look at the XO, it can be noticed that apart from the wake up time, another important parameter is the Q of the crystal reference which determines the phase noise performance of the synthesizer at low frequency offsets, i.e. the higher the crystal Q, the lower its phase noise. Therefore, there is a need to find a high-Q alternative which can wake up much faster than a crystal. Bulk Acoustic Wave Resonators (BAW) which are a class of high-Q MEMS resonators, satisfy this criteria. Their instrinsic-Q factors range from 500-2000 and the oscillators using these resonators can wake up in a few $\mu s$. They are high frequency references (1 - 7 GHz) and thus can be used to build loop-free frequency synthesizers.

Using the BAW resonators, a transmitter that can wake up in 5 $\mu s$ employing loop-free synthesizers is proposed in this chapter. This transmitter possesses a very low energy overhead thanks to the fast wake up of the BAW resonator. In addition, this synthesizer is capable of supporting peak data rates of upto 16 Mb/s, thereby reducing the energy dissipated for communicating the actual data. The organization of this chapter is as follows: First a brief overview of BAW resonators is presented followed by the State-of-the-Art in MEMS resonator based synthesizers. This is followed by the architectural description of the MEMS based Transmitter after which the circuit design of each TX block is described. The final section consists of the

measurement results and the summary of the chapter.

## 3.1 MEMS resonators - An alternative to bulky crystals

MEMS resonators are an attractive alternative to the bulky quartz crystals due to their extremely small size with about 100 times smaller form factor. Among these micromachined resonators, a class of resonators called Bulk Acoustic Wave (BAW) resonators are of particular interest at RF since they provide a stable frequency reference in the GHz range. Using such resonators, the loop-based synthesizer (PLL) employing the crystal can be replaced by a loop-free synthesizer which not only can startup in $\mu s$, but also avoid the latency due to the settling of the PLL. In addition, the high $Q$ of BAW resonators also makes them suitable for bandpass filters at RF with sharp roll off characteristics.

### 3.1.1 BAW resonators

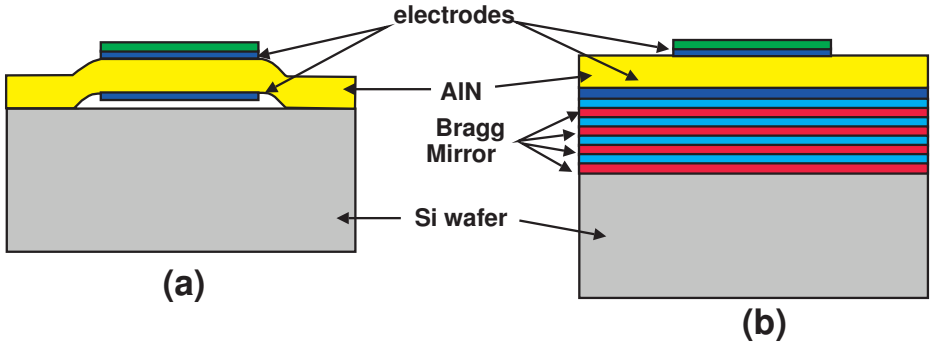



Figure 3.1 – Cross section of BAW resonators: (a) FBAR, (b) SMR

Bulk Acoustic Wave (BAW) resonators have found widespread use in duplexers due to their small size, high rejection and low insertion loss [3]. They consist of a piezoelectric material (typically AlN) sandwiched between two electrodes as shown in figure 3.1. When an electric field is applied between these electrodes, it causes mechanical deformation of the piezoelectric material. This results in an acoustic wave that travels in the direction of the thickness of the piezoelectric film for a particular orientation of electric field. The acoustic wave is reflected back at the film interface with the acoustic insulation layer due to impedance mismatch. When the thickness of the film equals an integer multiple of half wavelength, a standing wave is created by the forward travelling wave and the reflected wave. This acoustic wave in turn modifies the electric field distribution inside the piezoelectric film which changes the electrical impedance of the device. Thus the electrical impedance of the resonator changes with frequency [4]. Based on the nature of the acoustic insulator, BAW resonators are classified into a) Thin-Film Bulk Acoustic Resonators (FBAR) and b) Solidly Mounted Resonators (SMR). While in an FBAR, the air interface serves as the acoustic insulator, the SMR employs Bragg

mirrors made up of alternating layers of high and low acoustic impedance. The acoustic impedance layers must be designed with specified thickness such that there is a complete reflection of the acoustic waves into the device. Even though either of FBAR or SMR can be utilized in the design of the radio, the work presented in this chapter is based on FBAR and both the terms FBAR and BAW resonator will be used interchangeably henceforth in this chapter. The electrical equivalent of the BAW resonator is given by the Butterworth-Van Dyke model (figure 3.2) and is similar to that of a quartz crystal [5]. It consists of a series RLC network (called the motional branch) along with a parallel capacitance (called the parallel branch). In addition there are parasitic resistances and inductances associated with the access connections. The intrinsic resonator thus has two resonance frequencies, one corresponding to the series RLC branch (series resonance) and the other corresponding to the total resonator itself (parallel or anti-resonance). The relation between these frequencies is given by

$$\omega_s = \frac{1}{\sqrt{L_m C_m}} \tag{3.1a}$$

$$\omega_p = \omega_s \sqrt{1 + \frac{C_m}{C_p}}. \tag{3.1b}$$

This is shown in figure 3.3 which depicts the real and imaginary part of the FBAR impedance

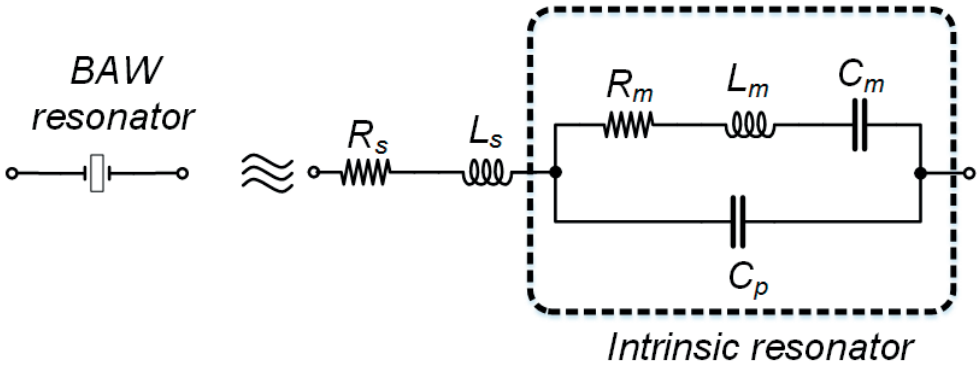



Figure 3.2 – Butterworh-Van Dyke equivalent circuit of the FBAR

near the resonance frequencies. As expected, the real part of the impedance at the resonance frequency due to the series RLC network is zero (in the ideal case, but in the real case is equal to the loss resistance) while the impedance at the antiresonance point is infinity. The imaginary part of the impedance on the other hand varies as follows : Between dc and the series resonance frequency, the FBAR behaves as a capacitor having negative imaginary impedance reaching zero at the series resonance. Then, the impedance turns inductive and increases, before falling and reaching zero at anti-resonance again following which the imaginary part of the impedance is capacitive again.

Consequent of two resonances, the FBAR also possesses two quality factors relating to the motional and the parallel branch. The motional Q-factor $Q_m$ ( which specifies the energy

loss in the resonator material) is of particular importance as a performance parameter of the resonator and is given by the following equation as

$$Q_m = \frac{\omega_m L_m}{R_m} = \frac{1}{\omega_m R_m C_m} \tag{3.2}$$

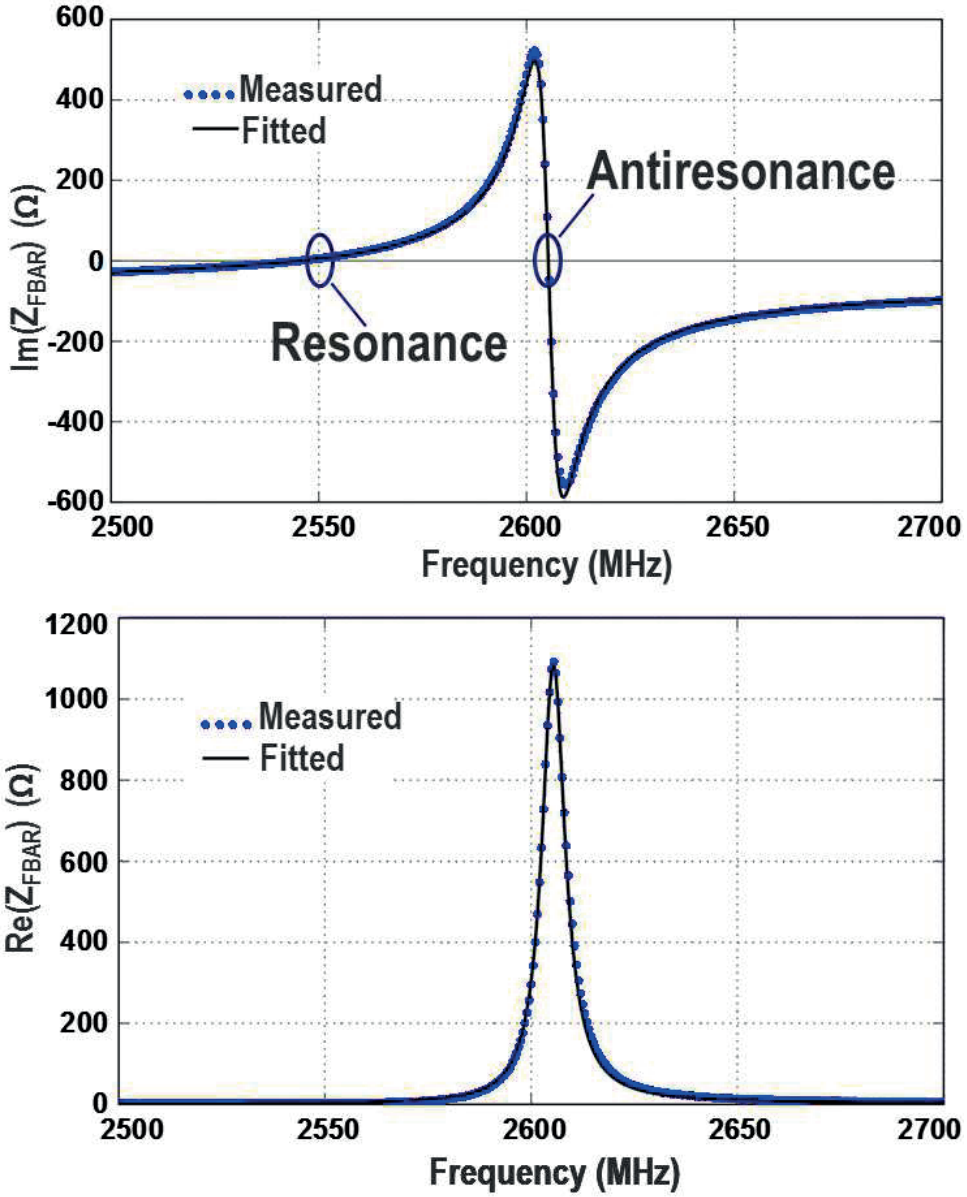



Figure 3.3 – Real and imaginary parts of the impedance of the FBAR showing resonance and anti-resonanace

In addition, the effective electromechanical coupling coefficient $k_{eff}$ also is an important

factor that needs to be considered for an FBAR. The coupling coefficient determines the energy conversion efficiency between acoustic and electrical energies or in other words is the ratio of the current in the motional branch to the parallel branch. The higher this coupling factor, the larger the tunability of a VCO or the bandwidth of a filter. The relationship between this coupling coefficient and the resonance frequencies is given by [4]

$$k_{eff}^2 = \frac{\pi^2}{8}\left(\frac{C_m}{C_m + C_p}\right). \tag{3.3}$$

By substituting for $C_m/C_p$ from equation 3.1b, the above equation can be reduced to

$$k_{eff}^2 = \frac{\pi^2}{8}\left(\frac{\omega_p^2 - \omega_s^2}{\omega_p^2}\right). \tag{3.4}$$

Since $\omega_p^2 - \omega_s^2 \approx 2\omega_p(\omega_p - \omega_s)$, this gives the coupling factor as

$$k_{eff}^2 \approx \frac{\pi^2}{4}\left(\frac{\omega_p - \omega_s}{\omega_p}\right). \tag{3.5}$$

Thus, the coupling coefficient determines the interval of the resonance frequencies and therefore the tunability of the FBAR. Typical values of the coupling coefficient for an FBAR is about a few % and typical values of $Q$ are in the range of 500-1000, as depicted in table 3.1. Thus, the product $M = K \cdot Q_m$ ($K$ is the ratio of the motional and the parallel capacitances i.e. $C_m/C_p$) is the Figure of Merit of an FBAR which needs to be maximized to improve its performance.

Table 3.1 – Parameters of a typical FBAR

| Parameter | Unloaded resonator | Loaded resonator |
|---|---|---|
| Coupling coefficient K | 5.04 % | 5.13 % |
| Intrinsic series resonance $f_m$ | 2552 MHz | 2469 MHz |
| Parallel resonance $f_p$ | 2605 MHz | 2522 MHz |
| Series Q-factor $Q_m$ | 487 | 332 |
| Parallel Q-factor $Q_p$ | 381 | 288 |
| Figure of Merit $M$ | 24.5 | 17.03 |
| Motional inductance $L_m$ | 104.62 nH | 110.37 nH |
| Motional capacitance $C_m$ | 37.19 fF | 37.66 fF |
| Motional resistance $R_m$ | 3.44 Ω | 5.16 Ω |
| Parallel capacitance $C_p$ | 872.68 fF | 867.46 fF |
| Parallel resistance $R_p$ | 1.06 Ω | 0.92 Ω |
| Parasitic series resistance $R_s$ | 1.01 Ω | 1.05 Ω |
| Parasitic series inductance $L_s$ | 0.46 nH | 0.47 nH |

## 3.2 Reducing the synthesizer start-up energy overhead

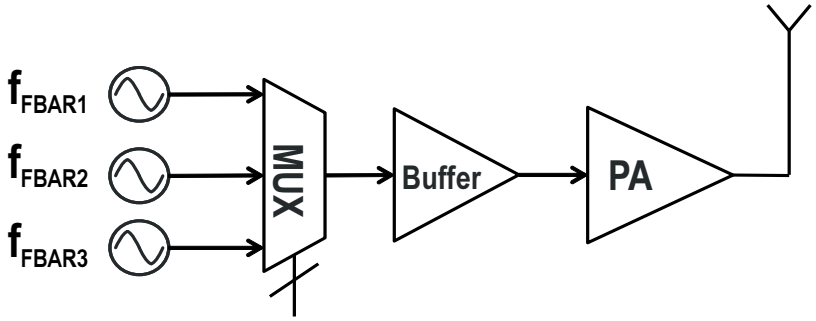
### 3.2.1 FBAR based TX : State of the Art

In order to reduce the synthesizer start-up energy overhead $E_{oh}$, an alternative method of frequency synthesis based on an FBAR was proposed in [6], [7], [8] and [9]. This idea takes advantage of the fact that the FBAR based oscillators have a very small start-up time (a few $\mu s$) and hence less energy is wasted during each wake-up sequence. This section summarizes each of these architectures and along with their pros and cons.

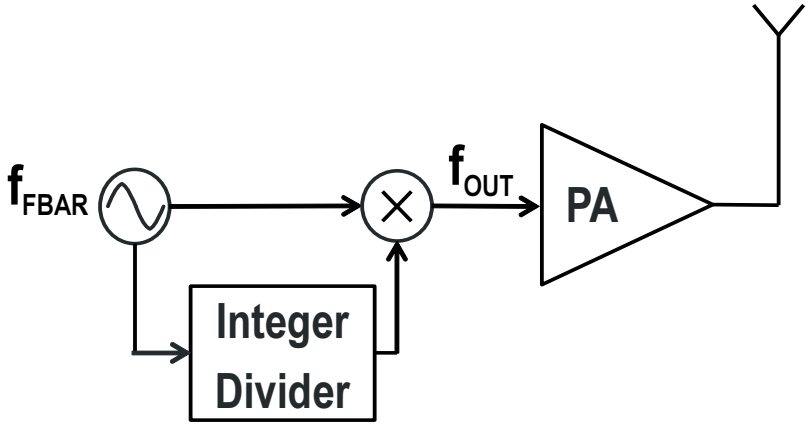
- One of the earliest works of designing a radio based on an FBAR was done by Flatscher *et.al.* for Tire Pressure Monitoring System (TPMS) [6]. The problem with this system was that it was limited to address a single channel and was very limited in the data rate it could achieve i.e. 50 kb/s owing to very small tuning range that was left for modulation after compensating for the temperature dependent frequency drift.
- The radio of [7] uses three FBAR to address an increased number of channels as compared to the previous design (3.4a). While this design is scalable and covers a larger frequency range, it also means the addition of more off-chip components (namely the FBARs). Even though the FBARs are not as bulky as the quartz crystals, packaging multiple instances of them along with the integrated chip can be unattractive. Furthermore, this solution also does not cover a wide frequency range and is limited to addressing a few channels only.
- To circumvent the FBAR tuning issue, a solution was proposed in [8], [9]. This involves generating an Intermediate Frequency (IF) by dividing down the FBAR DCO Local Oscillator (LO) signal ($f_{LO}$) using an integer divider. The LO and the IF can then be up-converted ($f_{RF} = f_{LO} + f_{IF}$) to get the desired carrier frequency which is then power amplified and transmitted (3.4b). Even this method of mixing does not enable this architecture to cover all the frequencies in a band like the 2.4 GHz ISM.

### 3.2.2 FBAR based TX : Architecture

As mentioned in the previous subsection, the fast start up property of the FBAR is very attractive for decreasing the energy overhead of the radio. In addition, the excellent frequency stability of the FBAR lends itself to very low phase noise. The modulation in such a system is performed by simply varying the FBAR Digitally Controlled Oscillator (DCO) frequency (Frequency Shift Keying - FSK). The clock for the digital modulator can also be derived from the FBAR by division. In order to improve upon the frequency tuning limitation which has been the main drawback with the previous designs, this thesis proposes to reduce the division ratio step size of the divider generating the IF. This in turn leads to a decreased tuning required on the FBAR to cover all channels in the band of interest. This minimum tuning required on the FBAR to enable all channel coverage within a given band be calculated as follows: Let a




(a)




(b) Spur due to IF second harmonic out of band

Figure 3.4 – (a)Loop free TX architecture using 3 FBARs (b)1+1/N architecture

divider with a division ratio step size of $\Delta$ be assumed to generate the IF signal. Let a desired frequency in the given band be addressed by generating an IF by dividing the LO signal with a nominal division ratio of $N$. Then the frequency of this nominal RF signal output by this synthesizer is given by

$$f_{RF} = f_{LO}\left(\frac{1}{N}+1\right). \tag{3.6}$$

The frequency of the RF signal can be adjusted slightly by tuning the FBAR keeping the division ratio $N$ constant. Therefore, for a given $N$, the minimum frequency that can be generated is

$$f_{RF,min}|_N = \left(f_{LO} - \Delta f_t\right)\left(\frac{1}{N}+1\right) \tag{3.7}$$

where $\Delta f_t$ is the tuning imposed on the FBAR. For a contiguous frequency coverage, this minimum frequency that can be generated with the division ratio fixed at $N$ should be equal to the nominal frequency that can be generated with the next division ratio which is $N+\Delta$. By substituting this condition, the tuning range required on the FBAR for covering all the

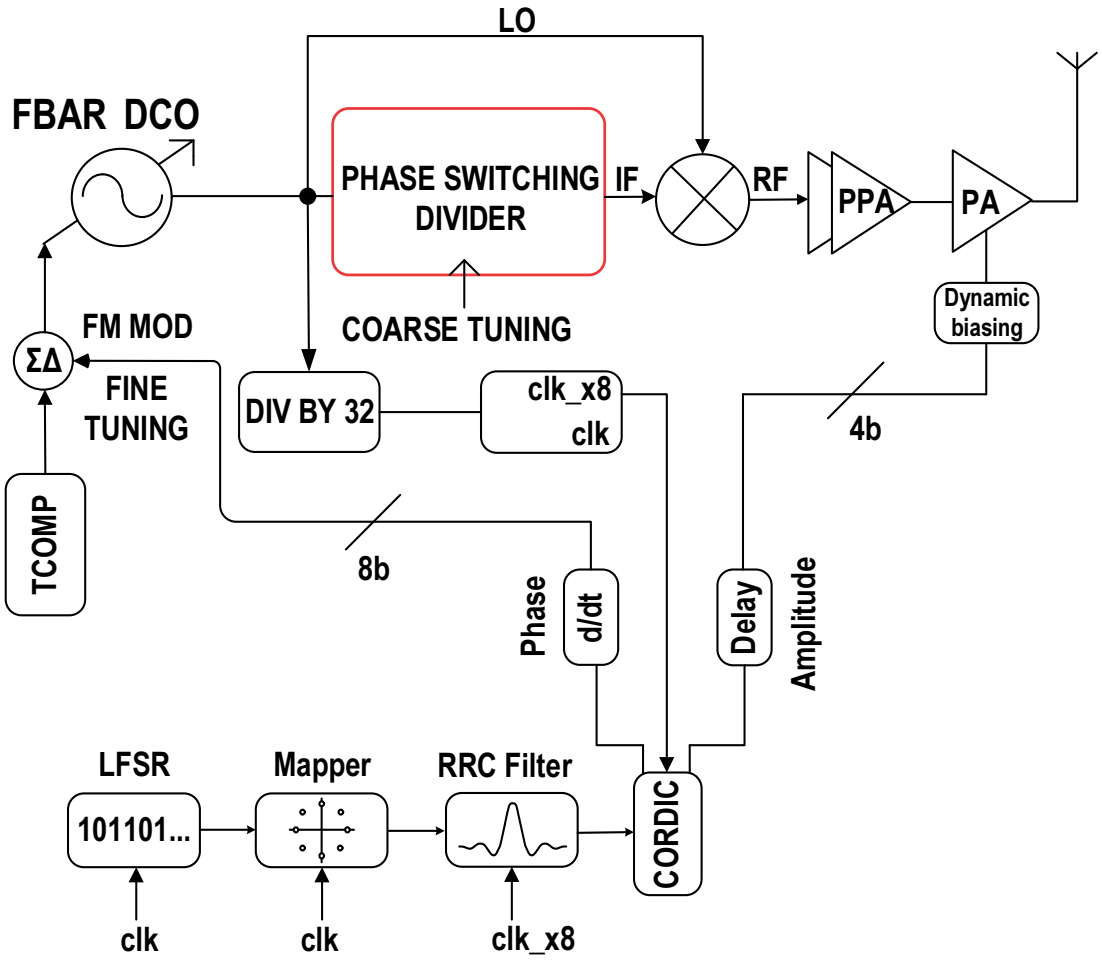



Figure 3.5 – PLL-free up-conversion TX architecture

frequencies within a given band can be given by

$$\Delta f_t = \frac{\Delta \cdot f_{LO}}{N_L^2 + (\Delta + 1) N_L + \Delta} \tag{3.8}$$

where $N_L$ is the lowest division ratio required for IF generation (which corresponds to the highest IF, provided low-side injection is used.

This FBAR tuning along with the Modulation Index (MI) required on the transmit side for a successful demodulation by the receiver also sets the limit on the Maximum Achievable Data Rate (MADR) of the system (irrespective of single or multi-channel addressing). If the condition of all channel addressing is imposed on this, and if the maximum tuning range of the FBAR is given as $TR$ (in‰) and the tuning required to compensate for the Process and Voltage variations is $PV$ (in ‰) ($\simeq$ 1‰ [10]), the tuning remaining for modulation after accounting for

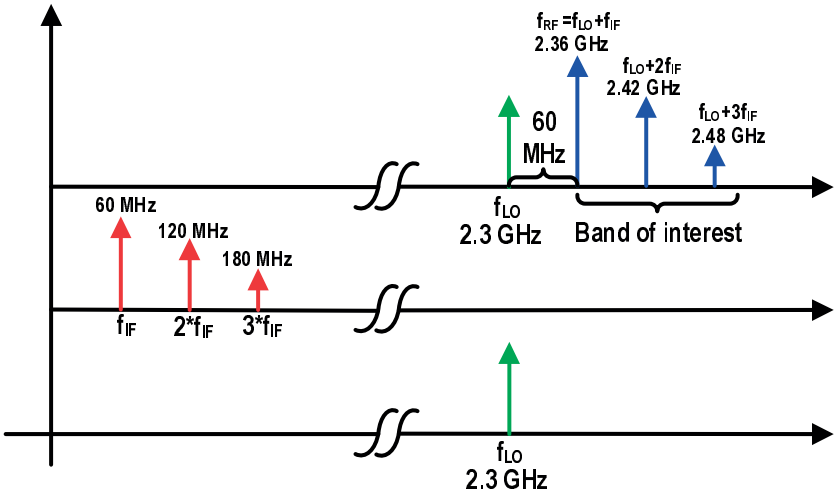
$\Delta f_t$ is

$$\Delta f_m = (TR - PV) * f_{LO} - \Delta f_t. \tag{3.9}$$

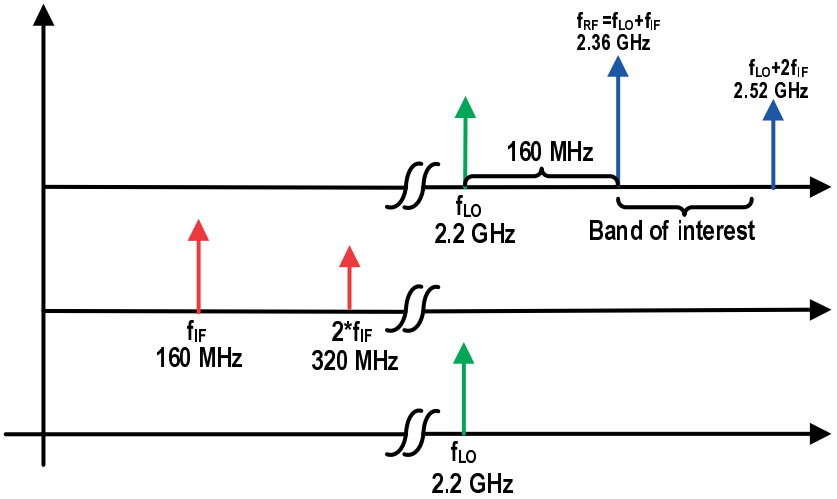
Then the MADR with All Channel coverage (MADR-ACC) is given by

$$MADR - ACC = \frac{\Delta f_m}{MI} \tag{3.10}$$

Any attempt to achieve data rates above this limit will see that the communication is restricted to a few channels.




(a) Spur due to IF second harmonic in band




(b) Spur due to IF second harmonic out of band

Figure 3.6 – Constraints on the choice of the LO frequency

Figure 3.5 shows the proposed PLL-free up-conversion transmitter architecture. It consists of an FBAR DCO generating the LO signal, which is then divided by a Phase-Switching Divider (PSD) to produce the desired IF signal i.e. $f_{IF} = f_{LO}/N$ . The centre frequency of the FBAR is chosen such that the spurs due to IF harmonics fall outside the band of interest while also being able to address all the channels in the given band. For instance, with the band of interest in this case being $f_{RF}$ = 2.36-2.5 GHz and the channel to be addressed is at 2.36 GHz, if $f_{LO}$ is chosen to be greater than or equal to 2.22 GHz, the second harmonic IF spur will be located at frequencies ≤ 2.5 GHz which is within the ISM band as shown in figure 3.6a. Therefore the constraint on the LO is given by $f_{LO} < 2.21$ GHz. The other extreme is having an LO frequency far away from the wanted band. The drawback of this is as follows: greater the frequency difference between the LO and the wanted band, the higher the frequency of the IF signal will be. The IF is produced by the PSD which utilizes the IF itself as a clock (asynchronous feedback) for its FSM. Therefore, a high IF would result in more power dissipation in the PSD. Based on these constraints, a frequency of 2.2 GHz was chosen for the FBAR DCO as shown in figure 3.6b. With the $f_{LO}$ being 2.2 GHz and with the given band of interest, the lowest division ratio $N_L$ is 7.33 for addressing a channel at $f_{RF}$=2.5 GHz ($f_{IF}$=300 MHz). If a divider with a step size $\Delta = 1$ is used, the tuning range required to address all the channels according to (equation 3.8) is $\Delta f_t$ = 31.6 MHz or $\Delta f_t / f_{LO}$ = 14.4‰. This is impossible to achieve for an FBAR thus making this architecture unsuitable for multi-channel communication [6]. To circumvent this problem, the PSD with $\Delta = 0.2$ is used which decreases the tuning range needed to a more relaxed value of $\Delta f_t$ = 7 MHz or $\Delta f_t / f_{LO}$ = 3.18‰, which is about the nominal value of the tuning range of an FBAR.

The LO and the IF are then fed to a mixer which up-converts these signals ($f_{RF} = f_{LO} + f_{IF}$). The mixer is followed by a single-ended class-C PA doing the final amplification. The PA supports complex modulation which is accomplished by tuning the bias of the cascode transistor. The cascode bias is set by a 4-bit digitized value of the AM input which controls a dynamic biasing circuit. The dynamic biasing circuit aids in achieving a highly linear PA characteristic that satisfies the IEEE 802.15.6 standard in terms of Adjacent Channel Power Ratio (ACPR). The following subsections give a brief description of each of the building blocks of the transmitter.

### 3.2.3 FBAR DCO

As explained in the previous section, temperature compensated FBAR DCO is the starting point of frequency synthesis. These DCOs achieve an excellent phase noise performance along with low power consumption [11], which is the main reason for choosing them for this TX architecture. Since the FBAR has two resonant frequencies, two possible differential oscillators can be designed [4]. Amongst these two possibilities, the parallel resonance oscillator first proposed in [12] has better performance in terms of noise and power and hence it is chosen in this case. As shown inf figure 3.7, it consists of a cross coupled pair ($M_1$ and $M_2$) that provides negative conductance to compensate for the resonator losses. There are two feedback transistors at the bottom ($M_3$ and $M_4$) which set the common-mode voltage. Since the FBAR

is essentially an open circuit at DC, in order to avoid latching, a DC decoupling capacitor $C_s$ is present at the source of the common mode feedback transistors. The value of $C_s$ is determined by the onset of relaxation oscillation which occurs due to the energy transfer between this capacitance and the parallel capacitance seen at the output nodes of the DCO (a combination of the FBAR parallel capacitance and the output load capacitance). Therefore, the condition on $C_s$ to avoid relaxation oscillations is given by

$$C_s < \frac{n}{2}\left(C_p + C_L\right), \tag{3.11}$$

where $n$ is the subthreshold slope factor of the differential pair transistors.

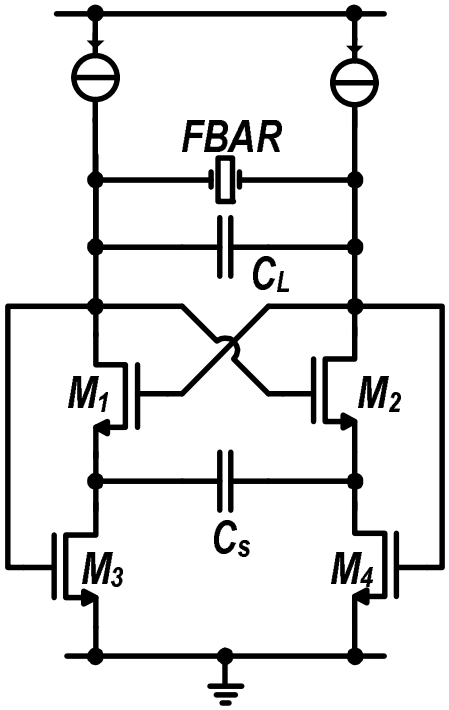



Figure 3.7 – NMOS cross-coupled FBAR oscillator

The series impedance of the FBAR, ignoring the contact resistance and the inductance, is given by

$$Z_{m,FBAR} = R_m + sL_m + \frac{1}{C_m}. \tag{3.12}$$

The parallel component of the resonator impedance is absorbed into the impedance of the active part of the circuit and this impedance is given by

$$Z_c = \frac{nG_m + 2sC_s}{s\left(-G_mC_s + nG_mC_l + 2sC_sC_L\right)}. \tag{3.13}$$

The real and imaginary parts of the equation are then

$$\Re(Z_c) = \frac{-G_m}{n^2 G_m^2 + 2\omega^2 C_L^2} \qquad \text{and} \tag{3.14a}$$

$$\Im(Z_c) = \frac{-1}{\omega C_L}. \tag{3.14b}$$

At the frequency of oscillation this real part of the impedance compensates for $R_m$, from which the critical transconductance required for oscillation can be found to be

$$G_{m,crit} = 2\omega^2 R_m C_L^2. \tag{3.15}$$

This is the minimum transconductance needed for sustaining oscillations. This equation is derived based on the assumption that for low values of transconductance, the $n^2 G_m^2$ in equation 3.14a can be neglected. Looking at the analysis from another point of view, figure 3.8 which plots in frequency domain, the variation of the impedance locus with various values of current. Ideally, the relation between the real and the imaginary parts of the circuit impedance is bilinear which translates into a circular plot. The plot of the motional impedance of the resonator is a straight line. The stable oscillation point is the intersection of this straight line with the circle as shown in figure 3.8. As the current flowing through the circuit is increased (to increase the amplitude of the signal by decreasing the ON resistance of the top current sources), the transconductance ($G_m$) of the cross coupled transistors increases and the $n^2 G_m^2$ term of equation 3.14a becomes non negligible and even starts dominating which leads to the real impedance seen by the resonator becoming less negative. In addition, the output conductance of the cross coupled pairs also contribute to the non-linearity, leading to the loci of the resonator impedance and the circuit impedance no longer intersecting at very high currents and hence oscillation is no longer possible. This is shown in figure 3.8 which plots the real versus the imaginary part of the impedance seen by the resonator at increasing values of bias current (corresponding to increasing non-linearity related losses). This can also been seen in the figure 3.9 which shows the oscillator output amplitude with varying current. Indeed, the output signal amplitude starts to rise gradually after the critical current value growing till a point where the circuit becomes very non-linear (due to the transistors spending more and more time in triode region) after which the output signal abruptly goes to zero. Readers are requested to refer to [4] (pages 55-58) for further explanation regarding the effects of the transistor nonlinearities on the impedance loci plots.

Coming to the phase noise of the circuit, the thermal noise component is given by

$$\mathscr{L}(\Delta\omega) = \frac{2kT\omega^2}{G_{m,crit} V_{osc}^2 (\Delta\omega)^2 Q_m^2} \left(1 + \frac{\gamma_{a1} G_m + \gamma_{a2} G_L}{G_{m,crit}}\right), \tag{3.16}$$

where $k$ is the Boltzmann's constant, $V_{osc}$ is the amplitude of the output signal, $\Delta\omega$ is the frequency offset at which the phase noise is measured, $G_m$ is the transconductance of the

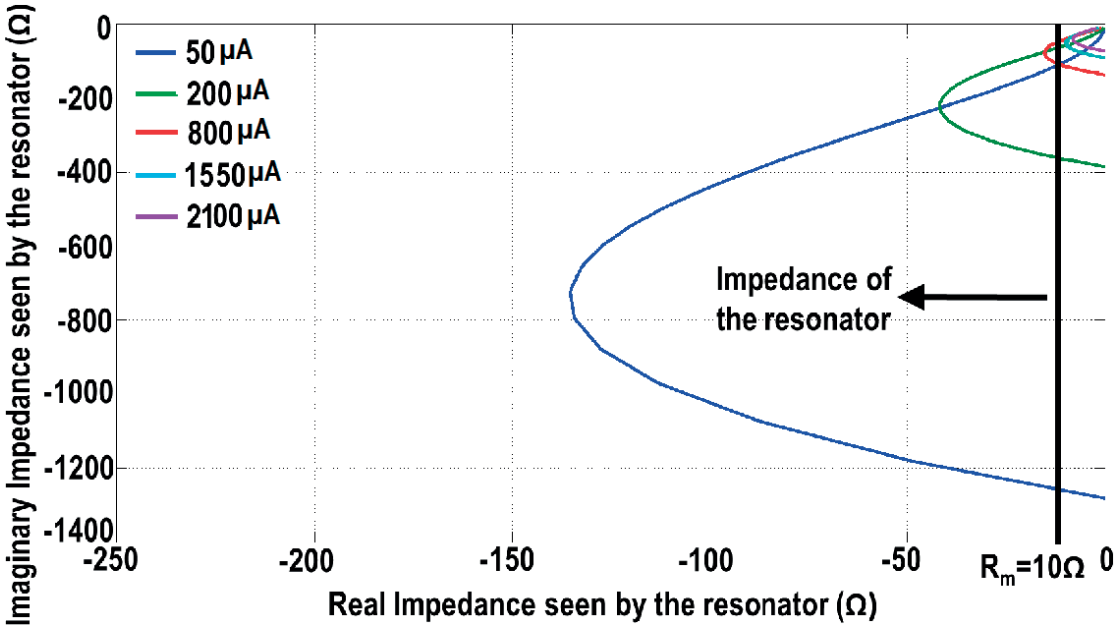



Figure 3.8 – Impedance locus variation with bias current (increasing the bias current leads to increasing losses and nonlinearity associated with the cross-coupled pair)

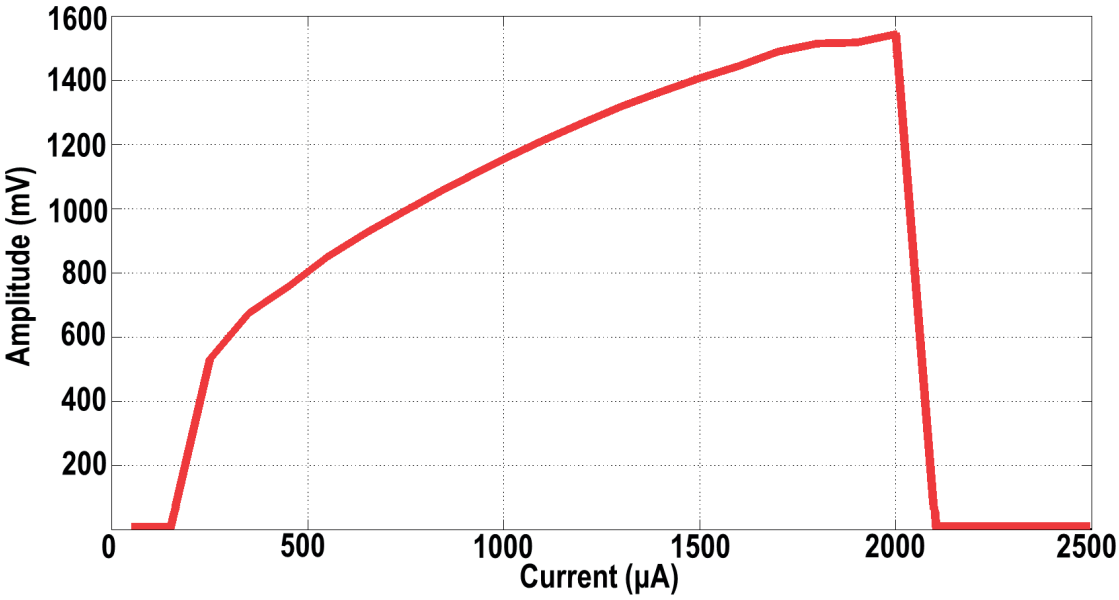



Figure 3.9 – Variation of output signal amplitude vs current

cross-coupled transistors, $G_L$ is the conductance representing the top biasing current sources and $\gamma_{a1}$, $\gamma_{a2}$ are the noise excess factors of the cross-coupled pair and the bias transistors respectively. It can be seen from this equation that the noise of the FBAR DCO is dependent on the motional Q-factor of the resonator and the amplitude of the output signal. Indeed, this is intuitive since the Q-factor denotes how effective the resonator can filter frequencies

other than the resonance frequency. Further, the higher the output amplitude, the lower the susceptibility of the output signal to the injection of noise.

In order to halve the power dissipation of the DCO and reduce the flicker noise upconversion, the DCO implemented in this work uses a complementary cross coupled structure as shown in figure 3.11 [13]. The critical transconductance of this circuit is half as that given in equation 3.15. In order to avoid the latch-up of the circuit at start-up, the PMOS cross-coupled pair should also be AC coupled at their sources. The biasing point of the PMOS cross-coupled pair is set by an external voltage $V_b$. To control the amplitude of the circuit while also ensuring a fast and reliable start up, an amplitude regulation loop ($M_5$-$M_7$) has been implemented. This amplitude regulation loop is based on the concept of a Proportional-To-Absolute-Temperature (PTAT) current reference [14]. The variation of the output signal amplitude with that of current in each limb of the cross-coupled pair (assuming the transistors are biased in weak inversion) is

$$I_0 = \frac{nU_T}{R}\left(ln\left(\frac{K}{I_{B0}(x)}\right)\right), \tag{3.17}$$

where, $I_{B0}(x)$ is the modified Bessel function of the zeroth order, $x$ is the amplitude of the output signal normalized to $nU_T$ i.e. $x = V_{out}/(nU_T)$ and K is the ratio of sizes of transistors in figure 3.11, $K = \frac{(W/L)_{M7}}{(W/L)_{M6}} = \frac{(W/L)_{M7}}{(W/L)_{M5}}$. The amplitude of the output signal can be varied by changing the factor $K$ or the resistance $R$.

If all the transistors $M_5$, $M_6$ and $M_7$ are in weak inversion, the relation between the amplitude of the output signal and the current in the transistor $M_7$ is given as [15]

$$I_7 = \frac{\pi}{8}\left(xG_{m,crit}\cdot nU_T\right). \tag{3.18}$$

The intersection of the currents given by the equations 3.17 and 3.18 gives the operating point of the oscillator as shown in figure 3.10.

Coarse tuning of the DCO is enabled by a bank of 31 pairs of depletion/inversion MOS capacitors ($C_L$). The coarse tuning is also accomplished by changing the division ratio of the PSD. The amount of frequency tuning that can be achieved by changing the load capacitance is given by [16]

$$\frac{d\omega}{\omega} = \left(\frac{C_m}{C_p}\frac{C_L}{C_p}\left(1+\frac{C_L}{C_p}\right)^{-2}\right)\cdot\frac{\Delta C_L}{2C_L}. \tag{3.19}$$

The maximum of this frequency tuning is achieved when $C_L$ equals the parallel capacitance of the resonator, $C_p$. This value is given by,

$$\left.\frac{d\omega}{\omega}\right|_{max} = \frac{K}{4}\cdot\frac{\Delta C_L}{2C_L}. \tag{3.20}$$

The DCO also has three other MOS capacitances driven by the output of a 7-bit $2^{nd}-$order

ΔΣ modulator enabling fine tuning (higher resolution). The DCO in the prototype has been designed to achieve a tuning resolution of around 0.9 ppm.

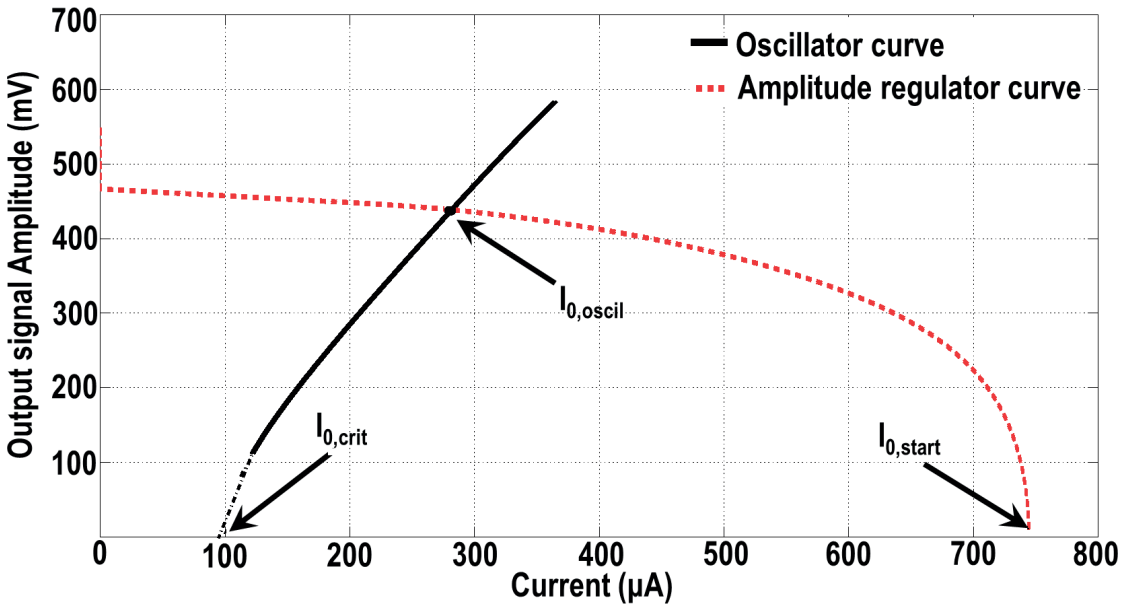



Figure 3.10 – V-I characteristics of the amplitude regulator

### 3.2.4 Phase Switching Divider

The PSD implemented here is similar to the one described in detail in the previous chapter to reduce the quantization noise at the output of a fractional-N PLL [17]. But the main difference between the two cases is that the division ratio of the PSD is firmly fixed in this case for a particular channel unlike the case of a fractional-N PLL where the modulation is performed by changing the division ratio. This leads to a simplification of the resynchronization circuitry where the latches $L_3$ and $L_4$ can be replaced by a single combinational logic gate. In addition, since the range of IF that is needed is limited, the division ratio is bounded and hence the integer divider can be simplified. For instance, the first divider stage can omit the $mod_{out}$ circuit and the clock output of this stage need not be gated. All these small modifications help to reduce the power consumption since some of this circuitry (like the latches) operate at the LO frequency.

### 3.2.5 Mixer, Pre Power Amplifier and Digital Baseband

The mixer which performs the IF up-conversion is implemented as a single-balanced Gilbert cell with resonant load at 2.44 GHz as shown in figure 3.12. This is followed by a push-pull preamplifier-buffer (PPA) which performs differential to single-ended conversion as shown in figure 3.13. The input resonance tank of the PA is also included in this figure for the sake of continuity. The integrated digital baseband contains a high data rate capable FSK modulator

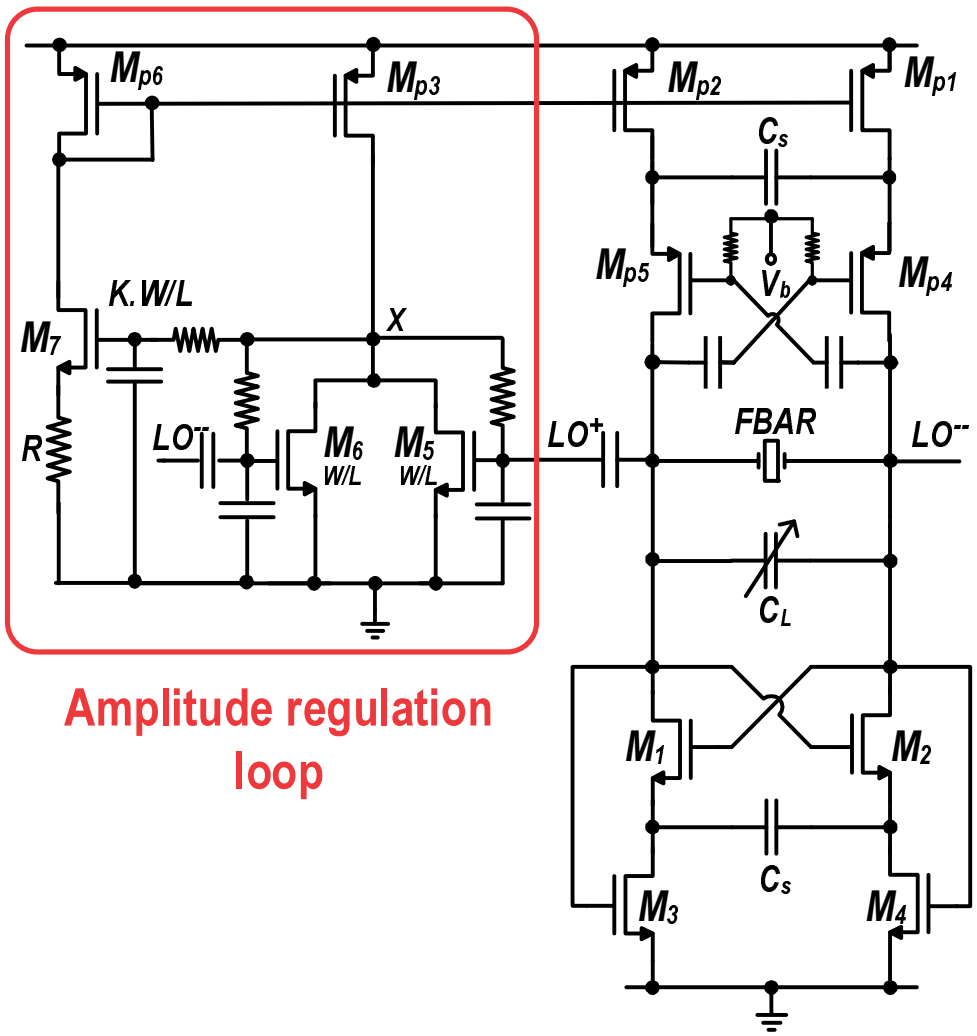



Figure 3.11 – Schematic of the FBAR DCO

with programmable pulse shape and modulation index, datarate selection, Manchester coding along with a high speed SPI interface. The clock for this DBB is obtained by dividing the FBAR output signal by 32. The input to the FSK modulator is the desired TX data pattern that is programmable via an SPI interface and can be set to a random sequence for the purpose of modulation analysis. The polar modulator necessary for IEEE 802.15.6 standard is implemented on an FPGA which is also clocked by the 64 MHz signal. A sequence of pseudo-random bits, generated by a linear feedback shift register (LFSR) are mapped onto constellation points. A root raised cosine filter with an oversampling factor of 8 is used for pulse shaping. A computationally efficient CORDIC algorithm transforms the modulation data in Cartesian to polar coordinates; thereafter the phase part is fed to the DCO tuning and the amplitude part goes to the PA. Since the amplitude and the phase path experience different delays (with the phase path lagging as compared to the amplitude path), a programmable delay is added to the amplitude path to compensate for this.

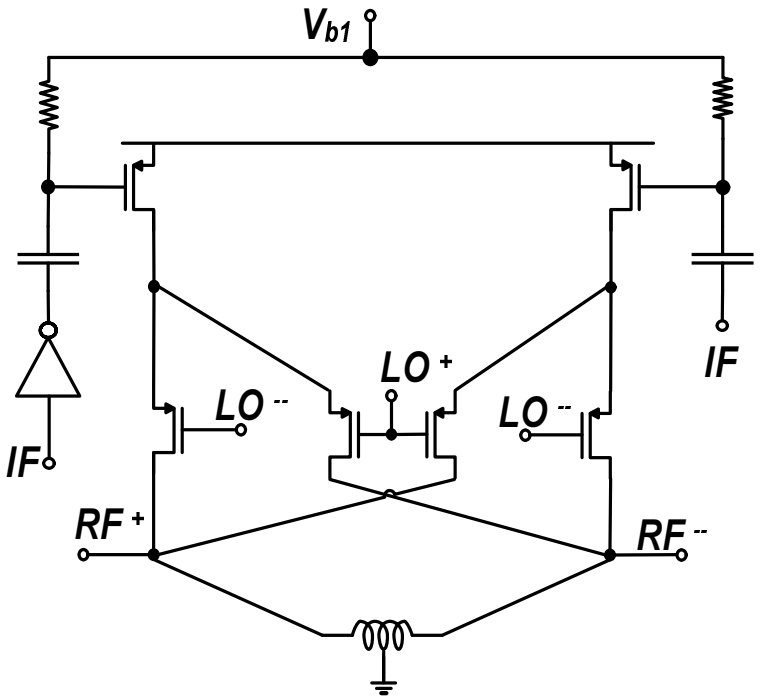



Figure 3.12 – RF frontend: Gilbert cell Mixer

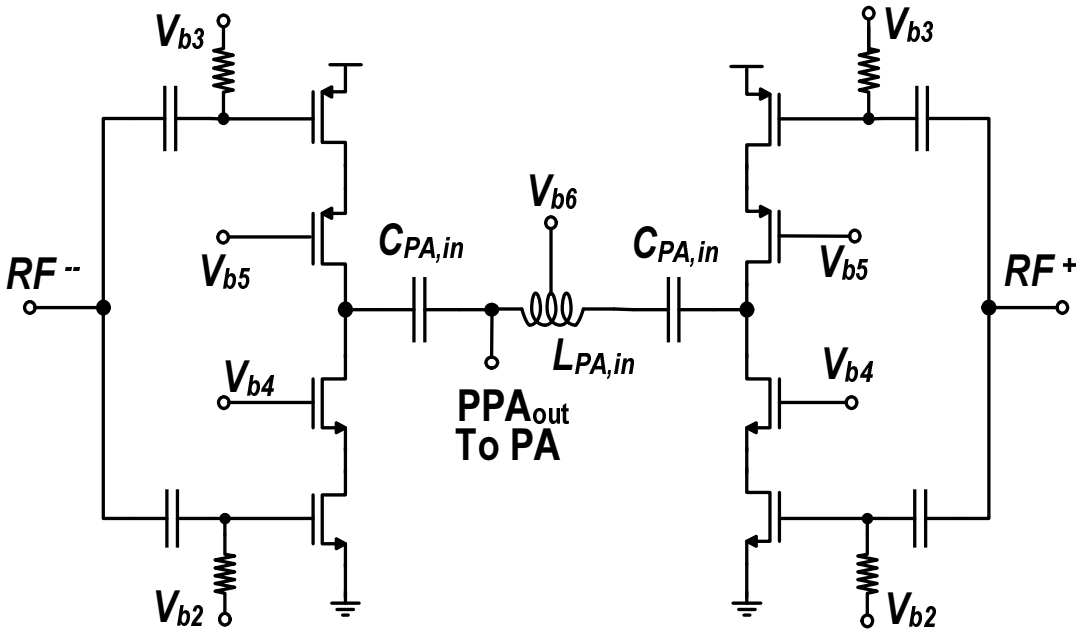



Figure 3.13 – RF frontend: Pre-Power Amplifier

### 3.2.6 Class-C PA with dynamic biasing for amplitude modulation

The power amplifier stage is implemented as a class-C circuit, with the RF signal from the PPA being AC-coupled to the gate of the Common Source transistor ($M_{PA1}$). The DC bias of this

transistor is set via an inductor which helps to nullify the effect of any input capacitance by creating a resonance at the frequency of interest. The cascode transistor ($M_{PA2}$) is biased using a dynamic biasing circuit (figure 3.14). High voltage swing at the output of the preamplifier causes the transistor ($M_{PA1}$) to behave like a switch effectively shorting the cascode transistor $M_{PA2}$ to ground when conducting. Setting the bias voltage of the cascode transistor therefore determines the amplitude of the current pulse generated at the PA output. This bias voltage can be varied according to a given digital pattern; whereby amplitude modulation can be performed. Compared to supply voltage modulation techniques to perform AM which are complex [18], acting upon the bias of the cascode requires little circuit overhead. In addition, supply voltage modulation requires extensive care in terms of spurious injections via the supply; the cascode bias modulation is free of such issues.

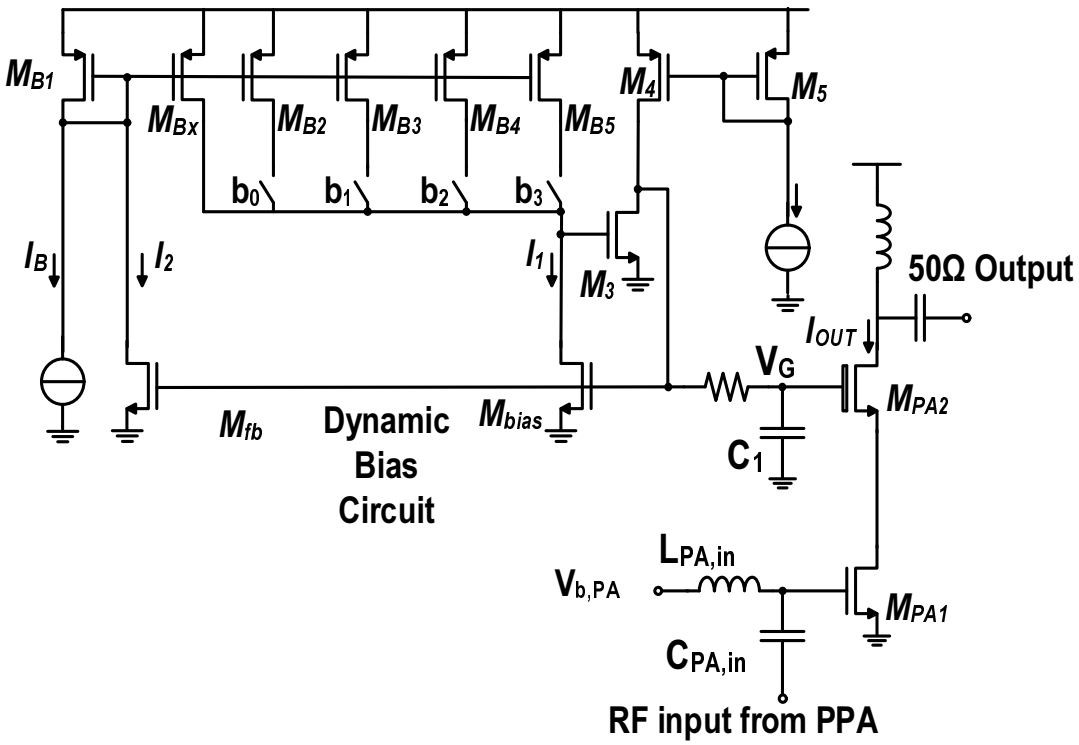



Figure 3.14 – Circuit implementation of the PA and the bias circuit

The dynamic biasing circuit in this case is essentially a Digital to Analog Converter (DAC) which converts the digitized version of the Amplitude of the baseband signal into voltage [19]. This voltage then modulates the envelope of the output RF signal. The most important parameter of the DAC is the number of bits, which has a direct impact on the output spectrum. Reducing the number of bits has the direct effect of increasing the Error Vector Magnitude (EVM) of the output signal. This is seen from figure 3.15 which plots the variation of the EVM with the number of bits controlling the dynamic biasing DAC. It can be observed that the EVM is highly dependent on the number of DAC bits initially, but as soon reaches a floor where

other non-linear effects in the circuit become the dominant sources of distortion. The EVM figure ascribed by the IEEE 802.15.6 standard is pretty relaxed (17.2 % which can be satisfied with even a single bit in the DAC). Therefore, the initial tendency is to choose the least number of bits for performing the AM. But, in reality, the output spectrum is also dependent on the number of bits in the DAC and hence it also should be made sure that the output satisfies the spectral mask of the standard before settling upon the number of DAC bits.

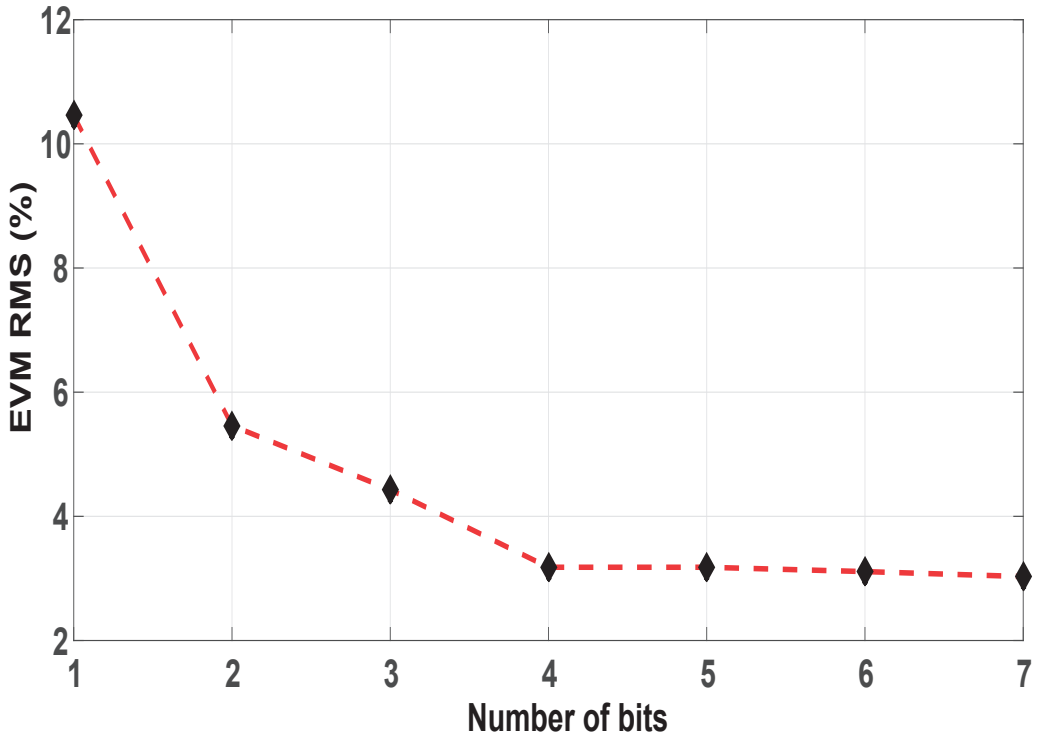



Figure 3.15 – Variation of the output RMS Error Vector Magnitude with number of DAC bits

Figure 3.16 shows the evolution of the output spectrum with the number of DAC bits. From the figure it is clear that 2 DAC bits would be sufficient for the output spectrum to satisfy the mask. But in order to keep sufficient margin to ensure that the spectrum does not violate the mask under all conditions, a compromise is made to choose the number of DAC bits to be 4. The simulation shows that with 4 DAC bits, there is a 20 dB margin between the output spectrum and the standard mask.

The sizing of the PA transistors should be made after careful consideration the of output power, efficiency and distortion due to AM-AM and AM-PM conversions. First, the drain efficiency of the PA can be calculated using the following formula:

$$\eta = \frac{P_{RF,out}}{P_{DC}} = \frac{P_{RF,out}}{P_{PPA} + P_{PA}}, \tag{3.21}$$

where $P_{RF,out}$ is the power in the fundamental of the RF output, $P_{PPA}$ and $P_{PA}$ denote the DC

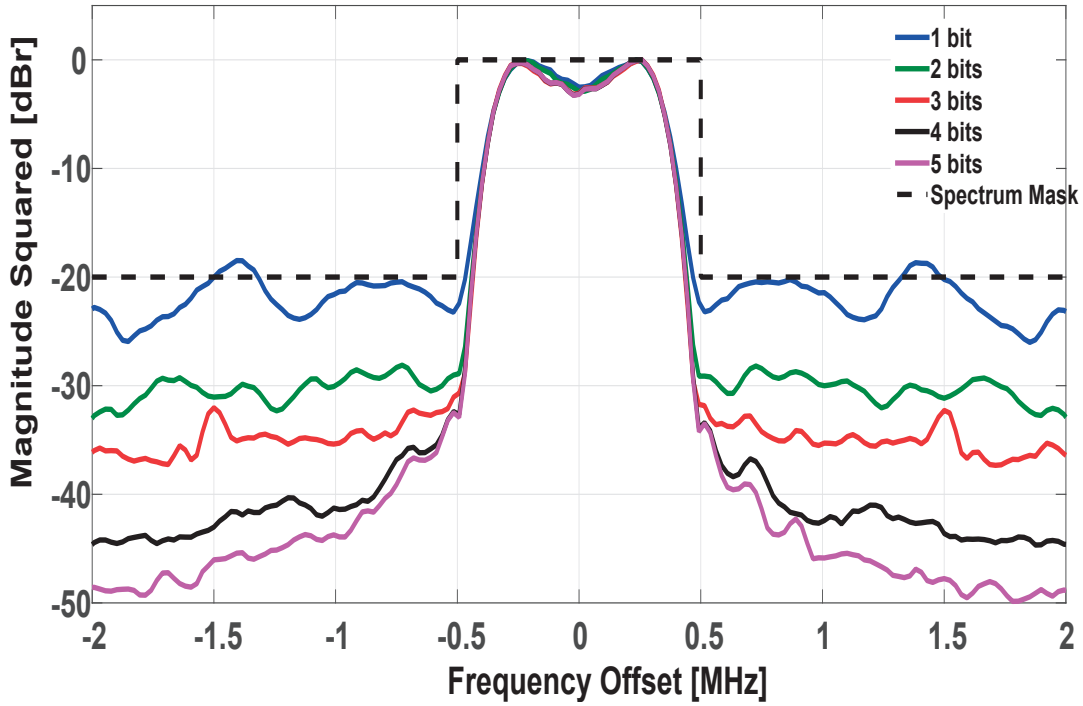



Figure 3.16 – Variation of the output spectrum with number of DAC bits

power consumption in the Pre-Power Amplifier and the PA respectively. Figure 3.17 shows the variation of the efficiency with the bias voltage of the cascode for a given size of the $M_{PA1}$ and $M_{PA2}$ transistors. From the figure, it can be seen that the maximum efficiency occurs when the bias voltage is equal to $V_{DD}$, which would correspond to higher output power. For an output power of around 0 dBm as required for our application, the simulated efficiency for this PA topology is around 18 % as can be seen from figure 3.18. In order to calculate the average efficiency, the Probability Density Function (PDF) of the possible values that the bias voltage can take is calculated based on the prospective Amplitude Modulation data. Then the area under the curve formed by plotting the PDF at different values of $V_G$ against the efficiency of the PA at these $V_G$ points gives the average PA efficiency. In this thesis, the efficiency figures mentioned are the drain efficiency unless specifically mentioned.

Another factor that influences the output spectrum is the output phase. For a large output power or a signal with a large Peak to Average Power Ratio (PAPR), the output signal phase varies a lot with the cascode bias. Therefore, there is a need to compensate for the phase distortion. But, in the case of this design, since the target power is 0 dBm, the PAPR is small and hence the phase distortion is negligible. This can be seen from the figure 3.19 which shows that the phase is nearly constant over a range of bias voltages from 0.8 V to 1.2 V and hence there is no need for phase compensation if the PA is operating in this region.

Coming to the design of the bias circuit, this circuit converts the input digital envelope signal

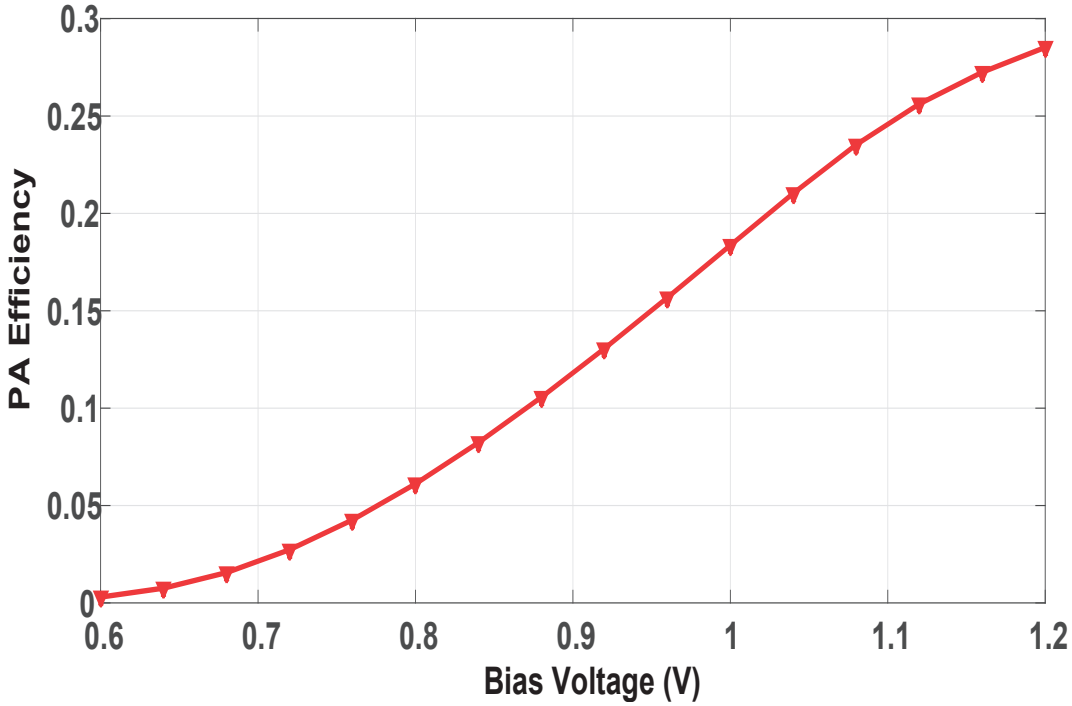



Figure 3.17 – Variation of the output efficiency with cascode bias voltage

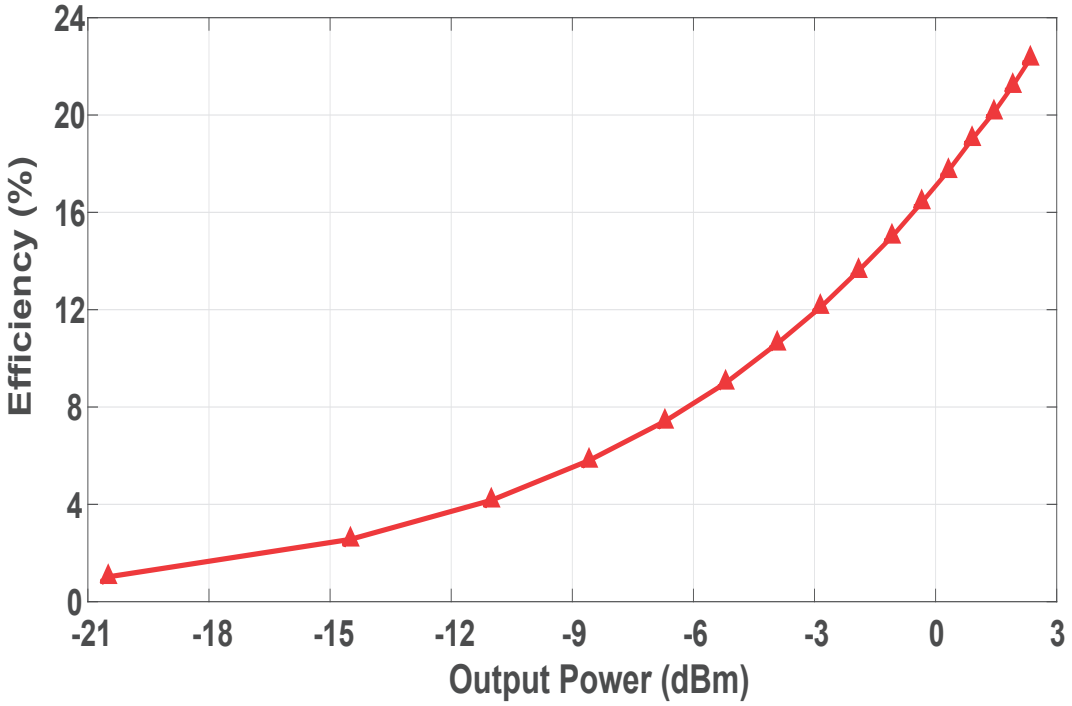



Figure 3.18 – Output Power versus PA Efficiency

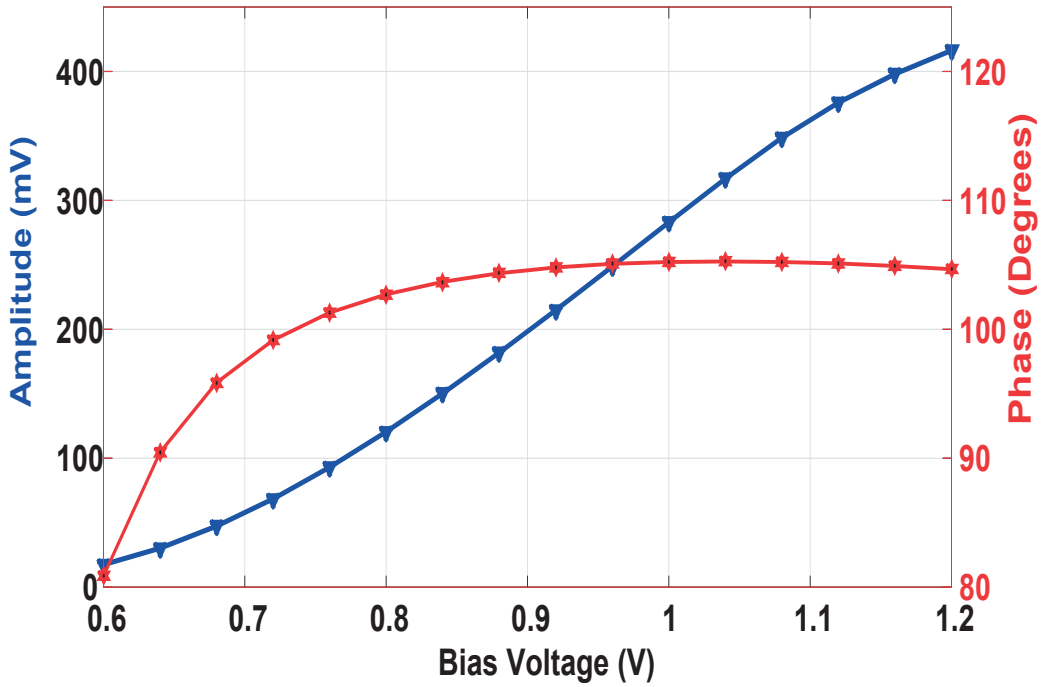



Figure 3.19 – Output amplitude and phase characteristic of the PA with varying cascode bias voltage

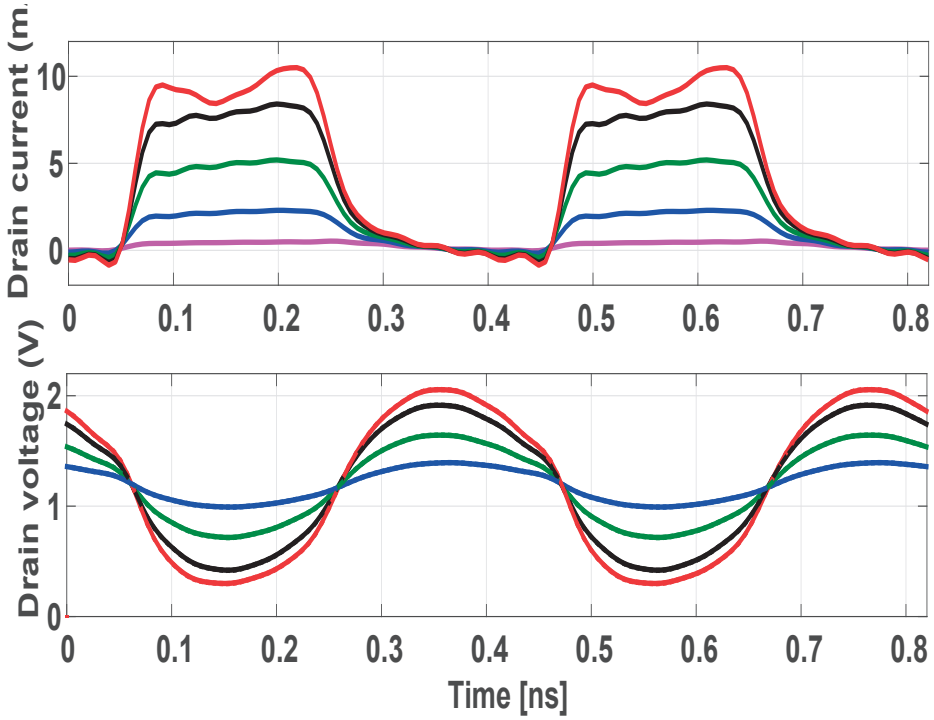



Figure 3.20 – Output current and voltage waveforms with varying cascode bias voltage

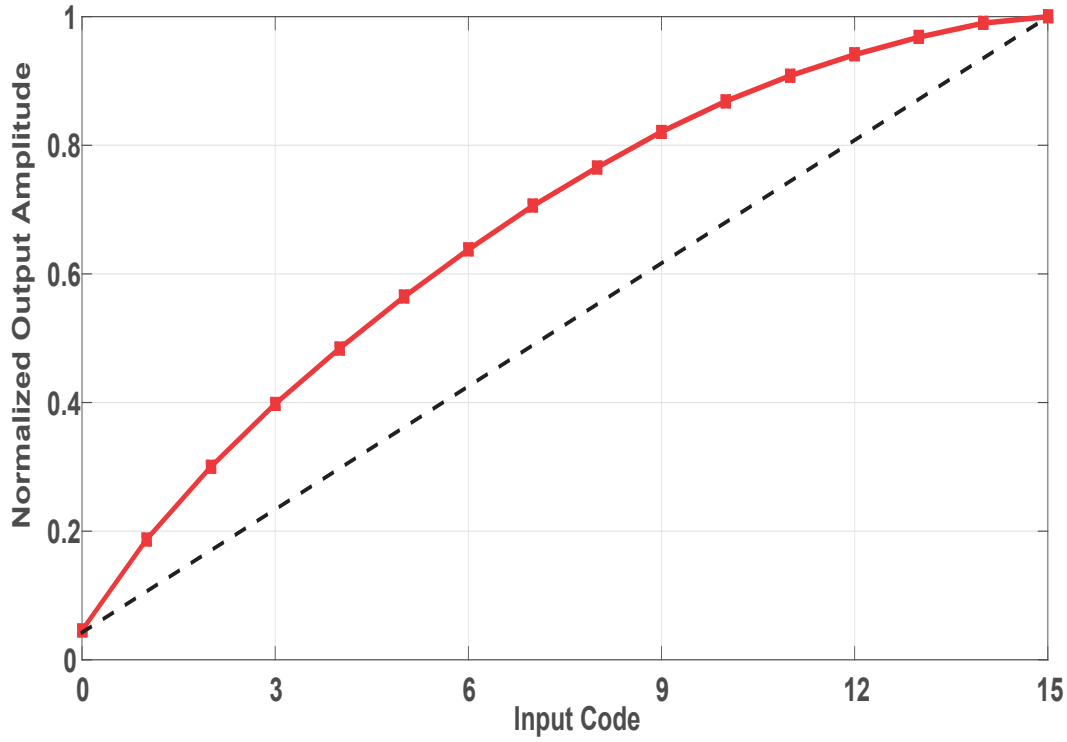



Figure 3.21 – Simulated non-linear behaviour of the PA with varying input code

into the bias voltage $V_G$ of the cascode transistor. The schematic of this circuit is presented in 3.14. As discussed previously, the DAC is chosen to have 4 bits as a tradeoff between circuit complexity and linearity of the PA. The transistors $M_{Bx}$, $M_{B2}$,..., $M_{B5}$ are current mirrors with each successive transistor having twice the current capability of the previous. These transistors are controlled by the switches $b0, b1, b2, b3$ which are turned ON according to the input binary code which corresponds to the AM data. Therefore, the drain current $I_1$ and consequently gate voltage $V_G$ will be determined by the input codeword. The range of the bias voltage is determined by the drain current $I_1$ and the size of $M_1$. When the bias voltage approaches $V_{DD}$ , the current mirror saturates and there is no longer a linear relation between $I_1$ and the input code. So in order to preserve the linearity, the current mirror is adapted by introducing a level shifter made up of transistors $M_3, M_4 \& M_5$. Due to this modification, the $V_{DS}$ of $M_{bias}$ will be less than $V_G$ by $V_{GS3}$. This allows us to keep transistors $MB2$-$MB5$ in saturation across the entire range of $V_G$. It is imperative to mention here that, for this to work ($M_{bias}$ to be in saturation), $M_3$ should be kept in weak inversion. The decoupling capacitor $C_1$ causes the $V_G$ to slew when the input code changes. Therefore, the transistors $M_4$ and $M_3$ must have enough current sourcing and sinking capability to avoid slewing. Since the capacitor $C_1$ is large so as to keep $V_G$ steady, the current of $M_4$ should also be large and hence will dominate the power dissipation in the biasing circuit.

Now when the bottom transistor of the PA $M_{PA1}$ is on, the cascode transistor and the biasing

transistor $M_{bias}$ form a current mirror and hence the output current ideally should have a linear relation with the current $I_1$. But as the biasing voltage increases, the output current exhibits a non-linear behaviour, where the drain current stops being a square wave as the amplitude of the drain voltage increases. This is due to the fact that the cascode transistor enters the linear region and hence the gain of the transistor is less compared to when it is in saturation. The non-linearity effect can be seen in the figures 3.20 and 3.21. The reason for this non-linearity is twofold. First is the voltage drop at the output of the cascode transistor which leads to a lower current. Second is the fact that the cascode transistor is minimum sized and hence short channel effects profoundly affect the linearity of the device.

Taking into account both of these factors, the drain current of $M_{PA2}$ can be written as

$$I_{OUT} = \frac{\beta_0}{2n}(V_G - V_T)^2\left(1 - \lambda\left(V_{DD} - I_{OUT}R_{eq}\right)\right), \tag{3.22}$$

where $\lambda$ is the channel length modulation parameter and $R_{EQ}$ is an empirical parameter that is used for curve fitting and is related to the equivalent resistance seen from the drain of the cascode transistor. Now, since $M_{bias}$ is a significantly longer device, the current of the transistor is void of significant short channel effects and can be given as

$$I_1 = \frac{\beta_1}{2n}(V_G - V_T)^2. \tag{3.23}$$

In addition to this, in order to compensate for the non-linearity between the currents $I_B$ and $I_1$, feedback was introduced by adding the transistor $M_{fb}$. The size ratio between $M_{fb}$ and $M_{bias}$ is denoted by $M$ and the ratio of the currents $I_B$ and $I_1$ is given by $N$. With this, writing the feedback equation gives

$$I_1 = \frac{N}{1 - MN} I_B. \tag{3.24}$$

Combining the equations 3.22, 3.23 and 3.24 gives

$$I_{OUT} = \frac{\beta_0}{\beta_1}(1 + \lambda V_{DD})\, I_B N \frac{1}{1 - MN + \frac{\beta_0}{\beta_1} I_B \lambda N R_{EQ}}. \tag{3.25}$$

The last fractional term on the right hand side can be made equal to 1 by setting the feedback factor $M$ suitably which results in the output current being linearly dependent on the reference current, $I_B$. This is given as

$$I_{OUT} = \frac{\beta_0}{\beta_1}(1 + \lambda V_{DD})\, I_B N. \tag{3.26}$$

Compared to digital predistortion, this approach used is less complex and can be easily implemented without any great area overhead.

## 3.3 Measurement Results

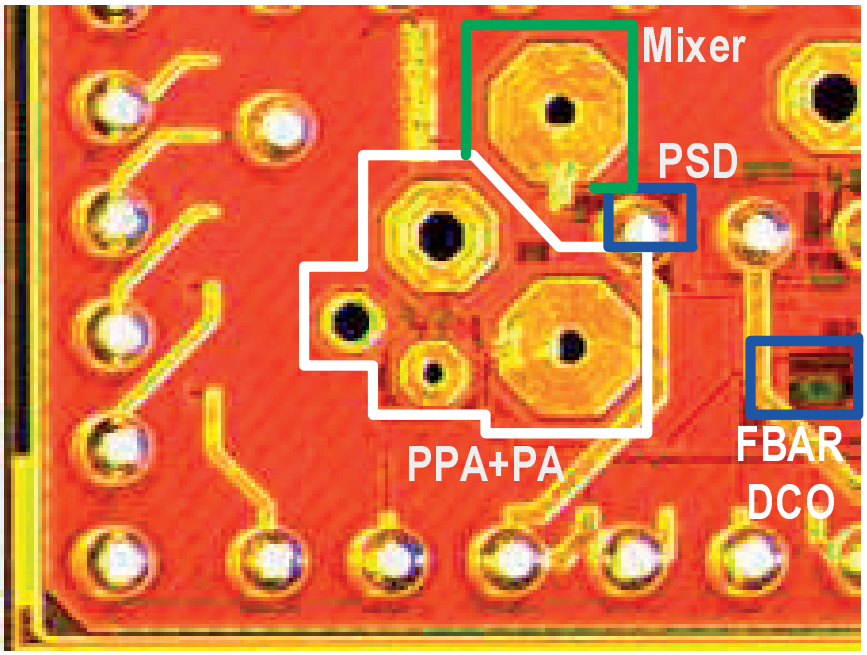



Figure 3.22 – FBAR based Transmitter Chip microphotograph

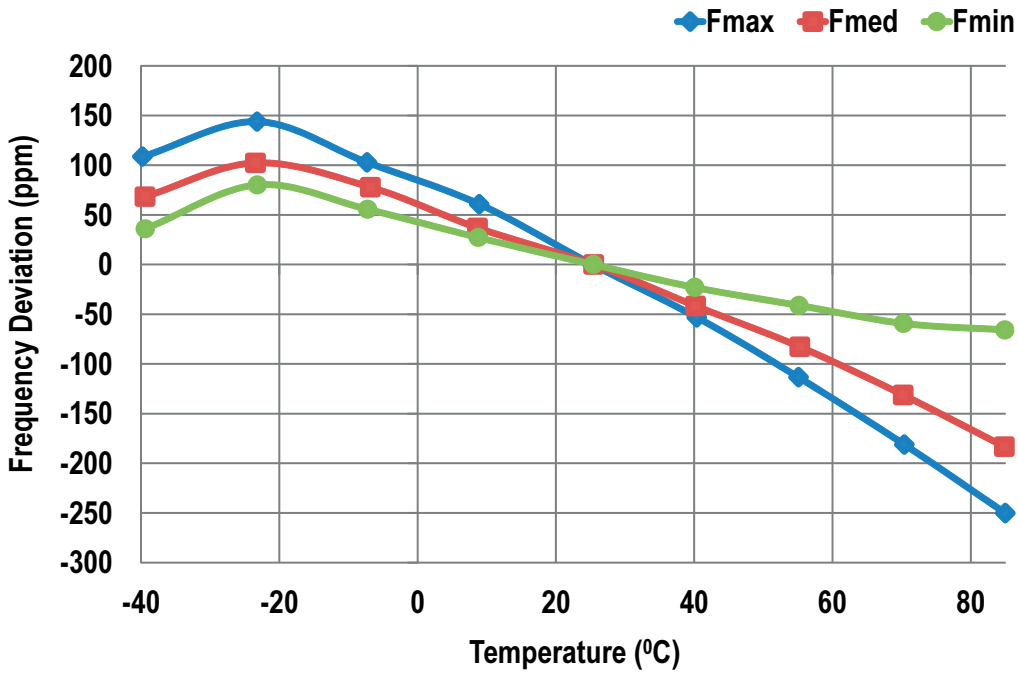



Figure 3.23 – Variation of structurally compensated FBAR DCO frequency vs. temperature

The TX was implemented in a 65 nm CMOS technology and the chip microphotograph is

given in 3.22. The FBAR used in this TX had an anti-resonance at 2.2 GHz. To compensate the frequency variation with temperature, the resonator is structurally compensated for frequency drift. The thermal compensation is achieved at the device level by balancing the negative Thermal Coefficient of Stiffness (TCE) of the thin films used in the resonator like $AlN$, $Si$ and electrodes with negative TCEs with $SiO_2$ which has a positive TCE). Further details about the $SiO_2$ compensation of the FBAR and its packaging can be found in [20]. After this compensation, the frequency sensitivity of the FBAR was measured to be -6.5 ppm/°C or 814 ppm over the temperature range -40 to 85°C as shown in figure 3.23 which depicts the frequency variation of the FBAR DCO at maximum, nominal and minimum tuning. In order to further improve the frequency stability, a 3-points calibration scheme was employed [21]. This scheme employs curve fitting to estimate the polynomial relation between the frequency and the tuning word at 7 different temperature values (figure 3.24). Then the inverse of the polynomials are calculated; and from this the tripartite relation between frequency, tuning word and the frequency is found. Based on this relation, a certain amount of tuning is applied at each of the 7 temperature values which effecively nulls the frequency dependence on temperature at 3 of the 7 temperatures values between -40 to 85°C. This also makes sure that the frequency deviation with temperature is confined within certain bound over the entire range. As a result of this open-loop calibration scheme, the temperature dependent frequency drift was measured to be ± 20 ppm in this case as shown in figure 3.25. Compared with a loop based implementation of the temperature compensation, this 3-point open-loop scheme is very simple to implement and can be readily synthesized into hardware using RTL.

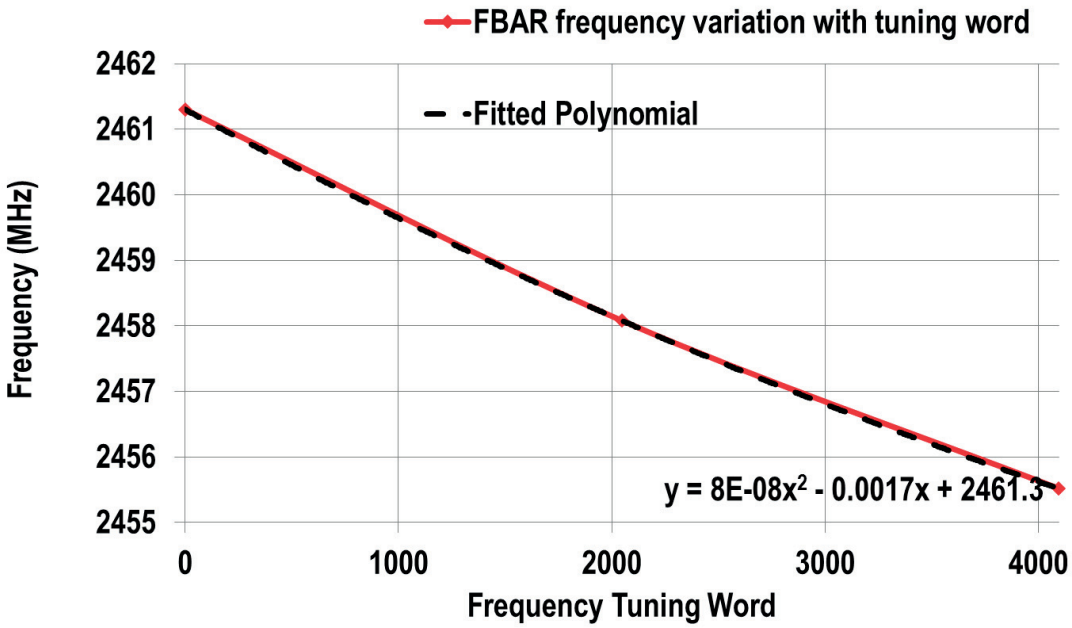



Figure 3.24 – Curve fitting : Polynomial relation between FBAR DCO frequency and tuning word

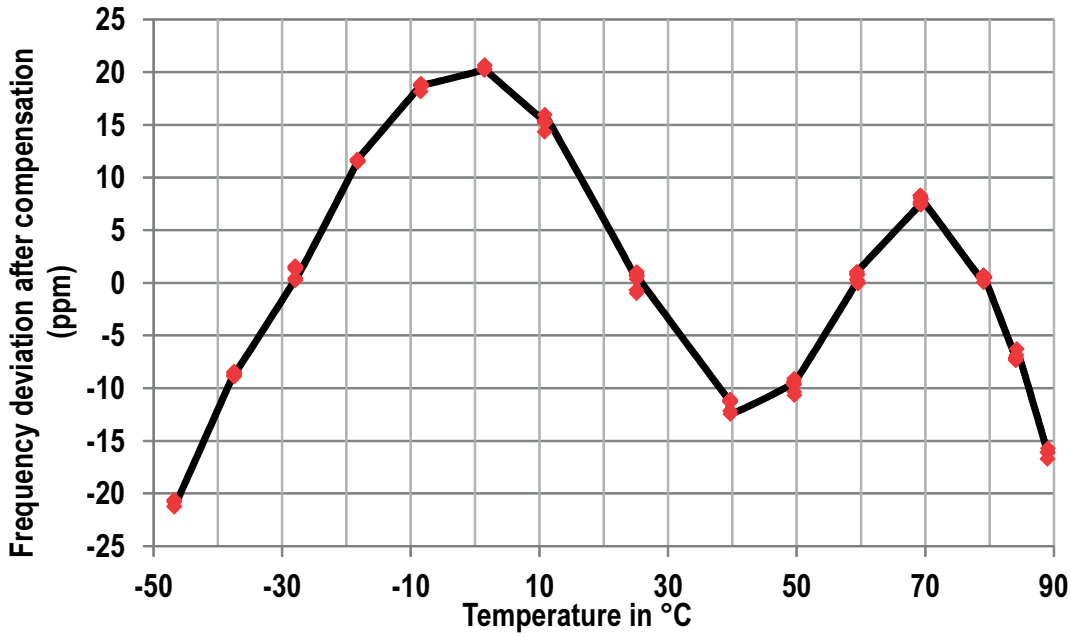



Figure 3.25 – Measured FBAR DCO frequency stability vs. temperature

The maximum tuning of the FBAR DCO was measured to be 4.9 ‰. Out of this available tuning, approximately 1‰ is spent to adjust for FBAR PV variations as well as temperature compensation [10]. Then, to cover all the frequencies in the given band, the tuning required was calculated previously to be $\Delta f_t / f_{LO}$ = 3.18 ‰ which leaves 0.72 ‰ for performing frequency modulation (FSK). From equation 3.10 this translates to MADR-ACC of 3 Mbit/s at a MI of 0.5 in the range of 2.36-2.5 GHz. But if the focus is only on the 2.4-2.48 GHz ISM band, then the FBAR frequency $f_{LO}$ frequency can be chosen to be 2.3 GHz so that the spur due to the IF $2^{nd}$ harmonic is outside the band. In this case the tuning range required for addressing reduces to 0.99 ‰ leaving 2.9 ‰ for modulation. This translates into an MADR-CC of 12 Mb/s. Now, if the user wishes to address only particular channels with the same modulation index, then the data rate can be even higher. For this, the digital baseband of the implemented TX supports data rate up to 16 Mbit/s (4 FSK with 8 MS/s) with a modulation index of 0.5 and the eye diagrams corresponding to the different data rates are given in figure 3.27, which show a trend of decreasing modulation accuracy with increasing data rates. Therefore, while the theoretical maximum of the data rate that this synthesizer can achieve is set by the switching speed of the DCO varactors, the practical upper limit is set by the modulation index and the tuning available for modulation. Finally, the phase noise of the DCO shown in figure 3.26 gives the value of -128 dBc/Hz at a frequency offset of 100 kHz and a flicker to thermal noise corner frequency of 5 kHz. It is to be noted here that the FBAR DCO was designed such that it can oscillate irrespective of the quality factor of the FBAR and as such was not optimized in terms of flicker noise. Moreover, since the output RF signal of the synthesizer is formed by mixing the LO signal with a divided version of itself, the phase noise of the RF signal is the same as

that of the LO (since the noise of a divided signal is less than the noise of the original signal by a factor $20logN$).

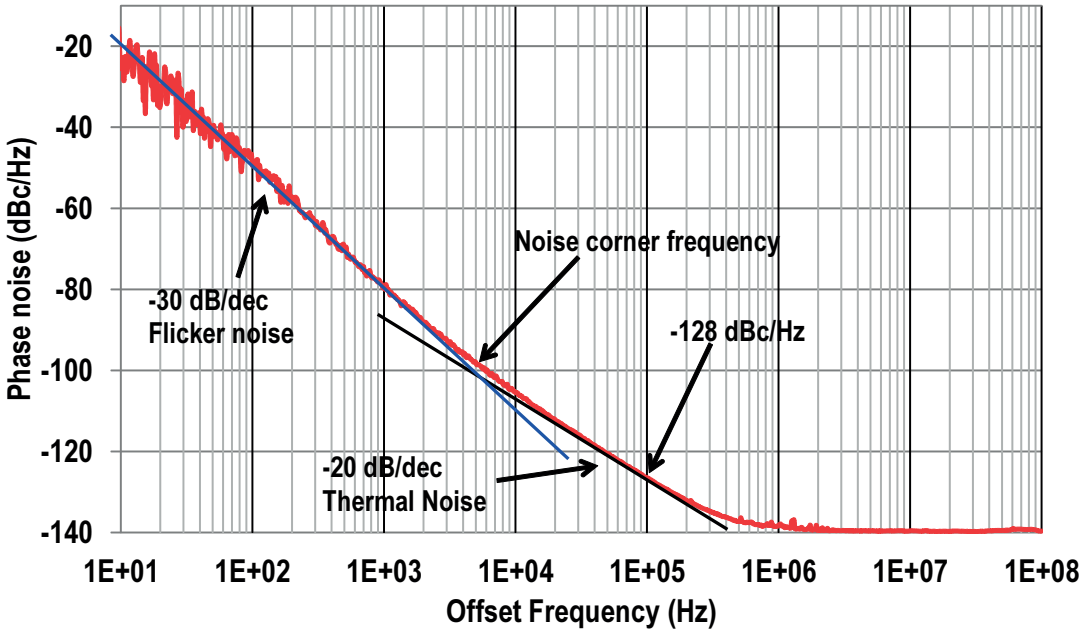



Figure 3.26 – Measured Phase noise of the FBAR DCO showing the flicker and the thermal noise regions

The output power of the transmitter is 0 dBm. The close in spectrum of the TX output is shown in figure 3.28. It shows both FSK as well as GFSK modulation at 1 Mbps data rate and a modulation index of 0.5. Even though the TX was designed for a custom communication protocol, it also satisfies the requirements of Bluetooth Smart (formerly Bluetooth Low Energy) protocol as shown in the figure. A wideband view of the TX output spectrum spread over 800 MHz is depicted in figure 3.29. This shows the spurious emissions of the transmitter. The spurs mainly occur due to four mechanisms. First is due to the fractional division step of the PSD (=0.2) which causes spurs at multiples of $0.2 * f_{IF}$ offset from the carrier. These spurs are at least 47 dB below the carrier. The second spur mechanism is due to clock feedthrough. The source of this is the digital baseband clock which is derived from the FBAR itself after division by 32. These spurs located at multiples of $f_{LO}/32$ offset and have a strength of -70 dBc. The third spur mechanism is due to the LO feedthrough through the mixer and the final one is the second harmonic of the IF. While both these spurs are significant in strength at about -29 dBc, they are far away from the frequency band of interest. Thus, to avoid any potential issues regarding the spurious emission violating FCC/ETSI regulations, a simple bandpass filter can be inserted at the output of the PA.

In order to view the frequency agility of the transmitter and subsequently the frequency synthesizer, the current profile of the TX is viewed as the TX starts communicating. This is shown in figure 3.30 where the bottom plot shows the current consumption of the TX and the

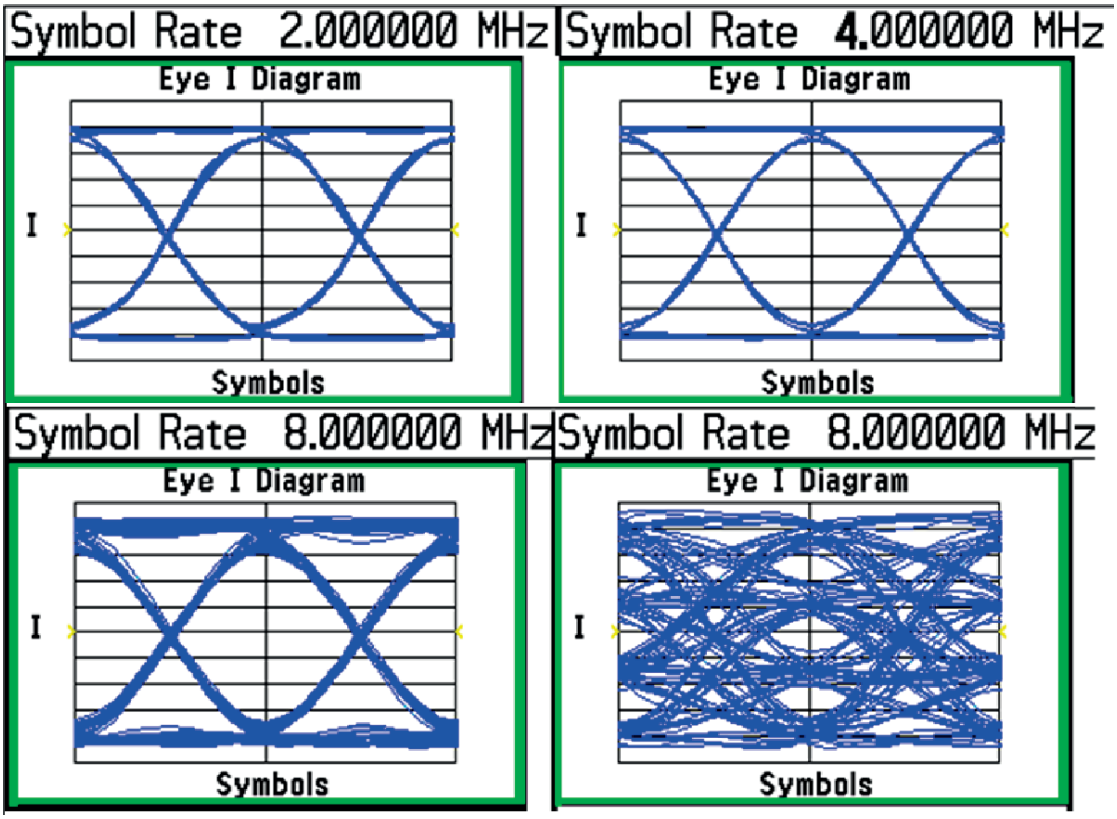



Figure 3.27 – Eye diagrams for GFSK at various data rates *viz.* (a) 1 Mbit/s (b) 2 Mbit/s (c) 8 Mbit/s (d) 16 Mbit/s (8 MSps - 4FSK)

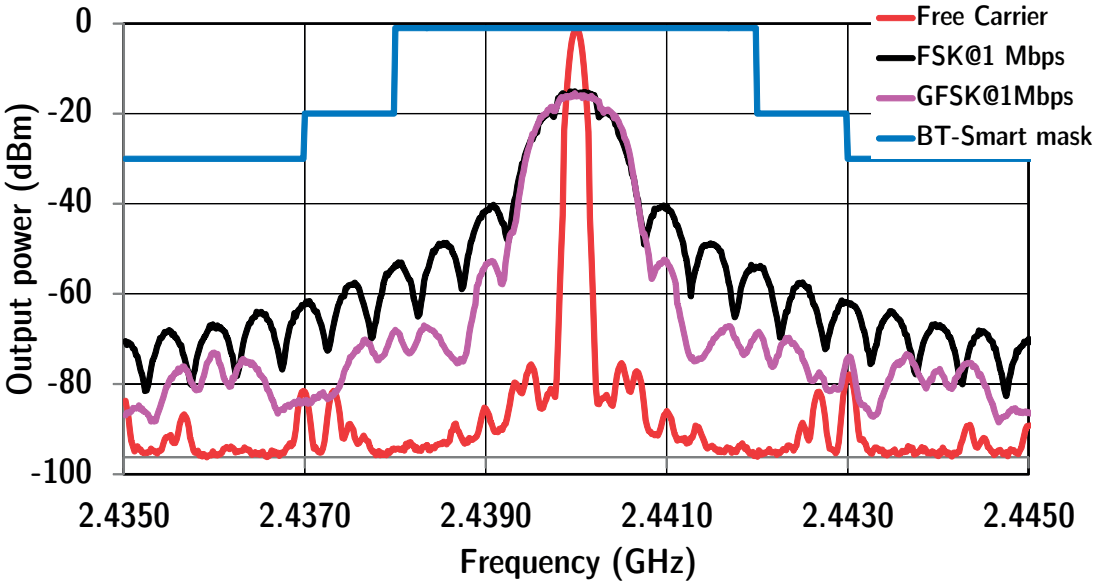



Figure 3.28 – Close-in spectrum showing free carrier, FSK and GFSK

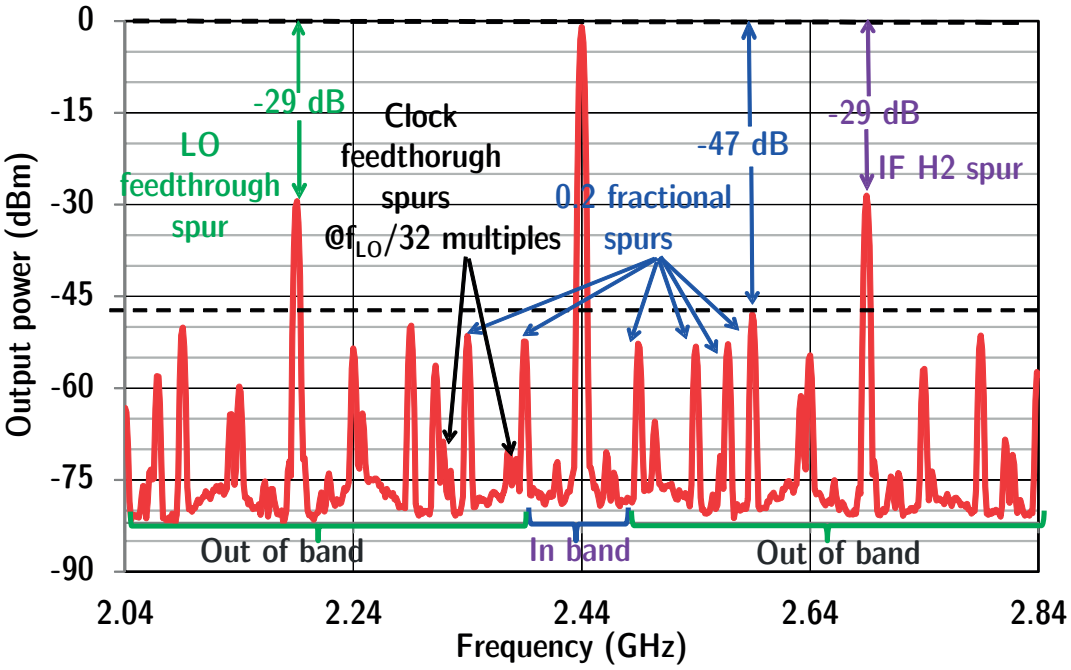



Figure 3.29 – Wide-band spectrum showing the spurious characteristics

top plot shows the variation of frequency with time. This test is performed with a 1 Mbit/s FSK with a modulation index of 0.5. From the current profile, it can be observed that the TX start-up can be decomposed into two distinct regions. Initially, the FBAR DCO starts-up in 2 $\mu s$ followed by the Power-Amplifier which takes 2 $\mu s$. The digital modulator requires 3 $\mu s$ to start-up and is turned on at the same time as the PA. Therefore, the total start up phase of the TX takes only 5 $\mu s$ after which the sample data pattern "0110 1010" can be seen on the frequency vs. time plot. This a factor 200 improvement compared with around 1 $ms$ that is required for a PLL based TX (XO start up and loop settling phase); the result of which is a massive reduction in the energy overhead as explained in the subsequent discussions in this section. Ideally, all the three, viz. the FBAR DCO, the PA and the modulator can be started at the same time using dedicated hardware to further reduce the wake up time of the TX. The turn off of the TX occurs in 3 $\mu s$ while channel switching also can be performed in just 3 $\mu s$. This frequency agility is one of the main advantages of this TX since it allows us to perform frequency hopping to any channel within the band in a span of 3 $\mu s$, while still being a narrow-band system.

The TX consumes 8.7 mA from a 1.2 V supply with the power breakdown shown in figure 3.31. The power consumption during the 5 $\mu s$ startup phase takes the following trajectory: Initially, the FBAR DCO current starts increasing and shoots past the critical current before the amplitude regulation loop takes over and the current comes down and stabilizes to a value of 1.8 $mA$. For the purpose of evaluation of the energy spent, the average current consumption is taken to be 2.5 $mA$ during this phase. This is followed by a ramping up of the current due to

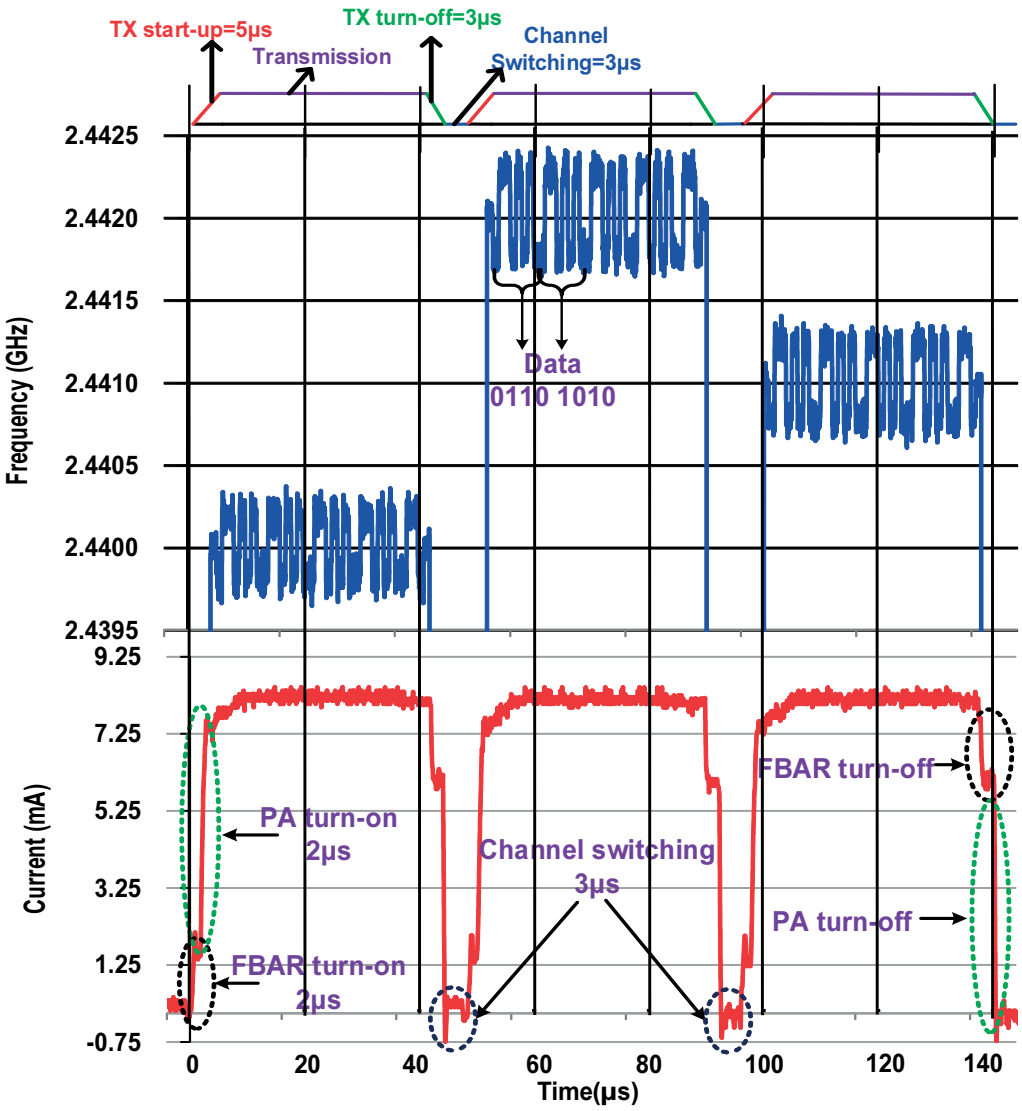



Figure 3.30 – Frequency agility of the TX showing FSK data (top) and TX current profile (bottom) showing the start-up / channel switching times

the PA startup during the next 3 $\mu s$ till the peak current is reached. To find an approximation for the startup energy overhead, the area under the current profile (figure 3.30) for this initial 5 $\mu s$ is calculated and multiplied with the supply voltage to give the energy dissipation as $E_{oh}$ = 18 $nJ$. At this juncture, it is imperative to note that this synthesizer does not suffer from the settling time that plagues the PLL-based synthesizer. Now, if this TX is implemented in a 10 kbit/s WBAN system described in the Introduction chapter with a packet length of 32 bytes needing to transmit 10 kb of data, at a peak data rate of 16 Mbit/s, this results in a packet duration of 16 $\mu s$. Then, the energy overhead for communicating 40 packets is then $E_{oh,tot}$ = 0.72 $\mu J$. In addition, the higher data rate results in the energy dissipated for communication to be $E_c$ = 7 $\mu J$. Therefore, the total energy FoM is $E_{p,tot}$ = 7.72 $\mu J$. A comparison of this TX

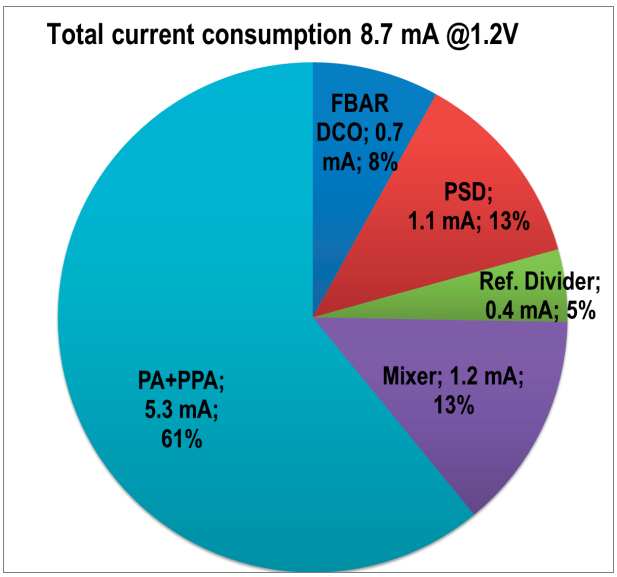



Figure 3.31 – TX power consumption breakdown

with the PLL-based SOTA TX given in the introduction at different peak data rates can be seen in figure 3.32 from which the following conclusions can be drawn:

- The FBAR based TX shows a 34x reduction in the startup energy overhead figures due to the very fast startup of the FBAR DCO and the absence of the synthesizer settling time.
- Due to this small startup overhead, the Useful Energy Threshold of the FBAR based TX is 187.5 Mbit/s as opposed to 2.8 Mbit/s for PLL-based transmitter.
- The PLL-based TX performs slightly better at lower peak data rates due to the fact that the energy spent for communication is much higher than the energy overhead at these data rates. Since the PLL-based TX has lower peak power dissipation, this is an expected result.
- At higher peak data rates the longevity of the FBAR based TX operating from a fixed power source such as a CR2032 battery is much more (figures 3.33a and 3.33b) than that of the PLL-based TX due to its reduced overhead $E_{oh,tot}$. For instance, if under the assumption that the SOTA TX can be extended to operate at 16 Mbit/s peak data rate with the same power (5.4 $\mu W$), the FBAR based TX outperforms the PLL-based SOTA TX by having a three times longer (1254 days vs 400 days) battery life. But if the transmitters are operated at their maximum capable peak data rates (16 Mbit/s for FBAR TX and 2 Mbit/s for PLL TX), then the FBAR based TX outperforms the PLL-based TX by a factor 7 in battery lifetime.

In order to measure the polar modulation capability of the transmitter, the associated digital baseband was coded in an FPGA. The clock of the FPGA based modulator was derived by the

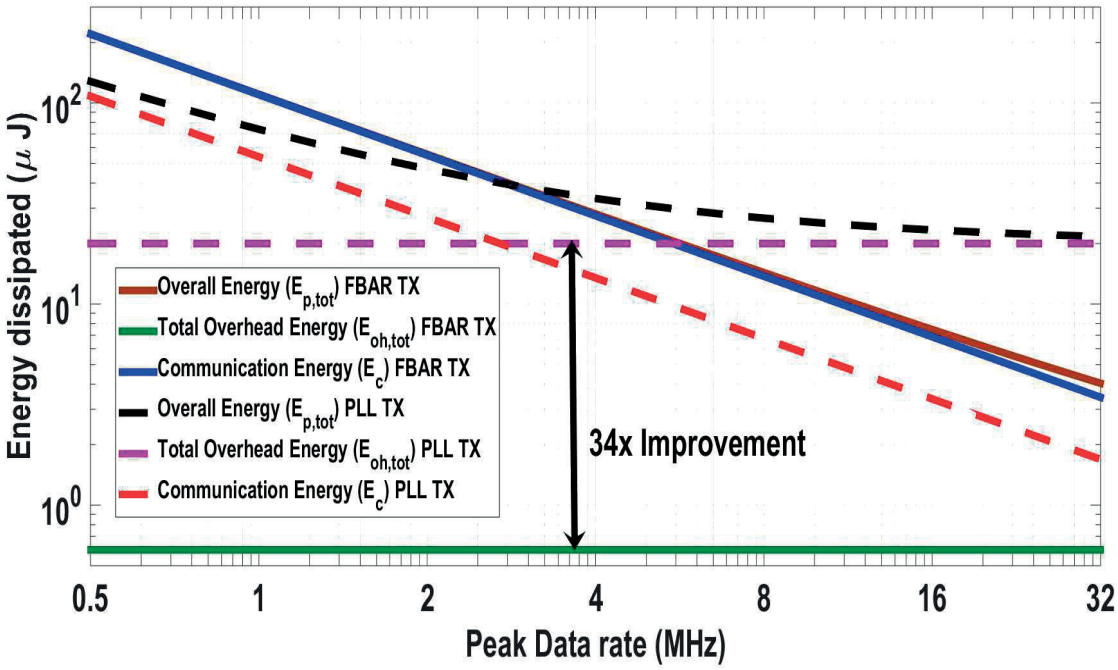


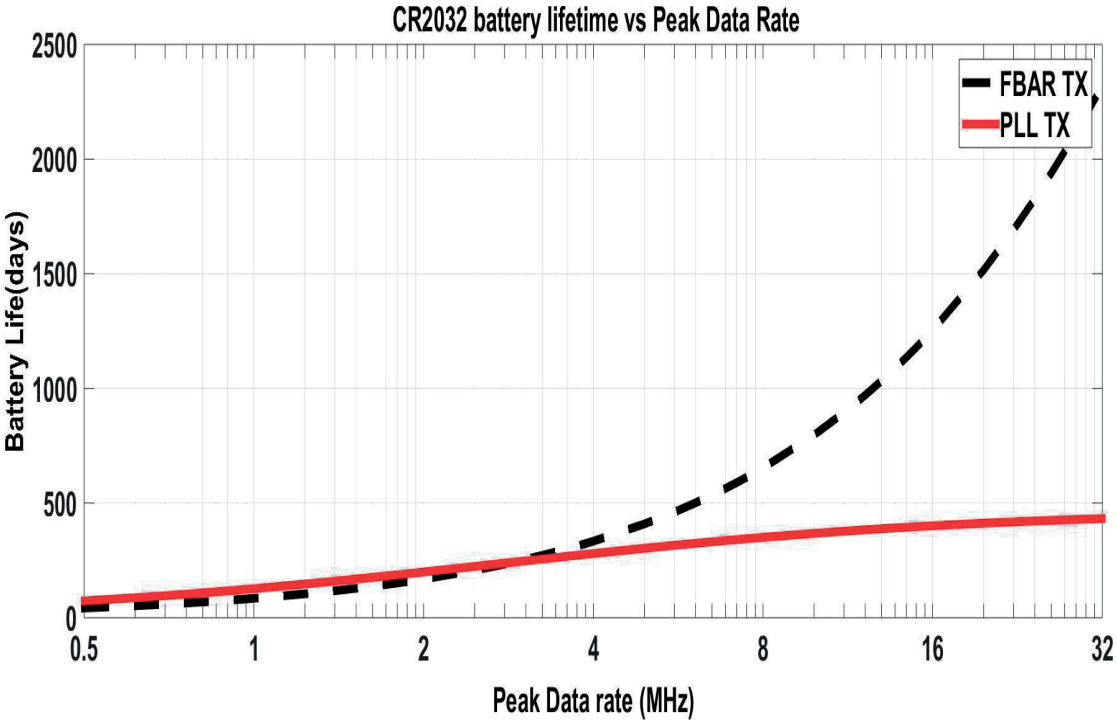

Figure 3.32 – Variation of the energy dissipation with Peak Data Rate in PLL-based SOTA TX and FBAR TX

division of the FBAR frequency by 32. Figure 3.33 shows the measured variation of the output amplitude with input code and compares it with the values obtained in simulations. Since the measured output power was approximately 1.0 dB lower than simulated, normalized curves are presented here, in order to emphasize the shape of the curves rather than the absolute values of the output voltage.

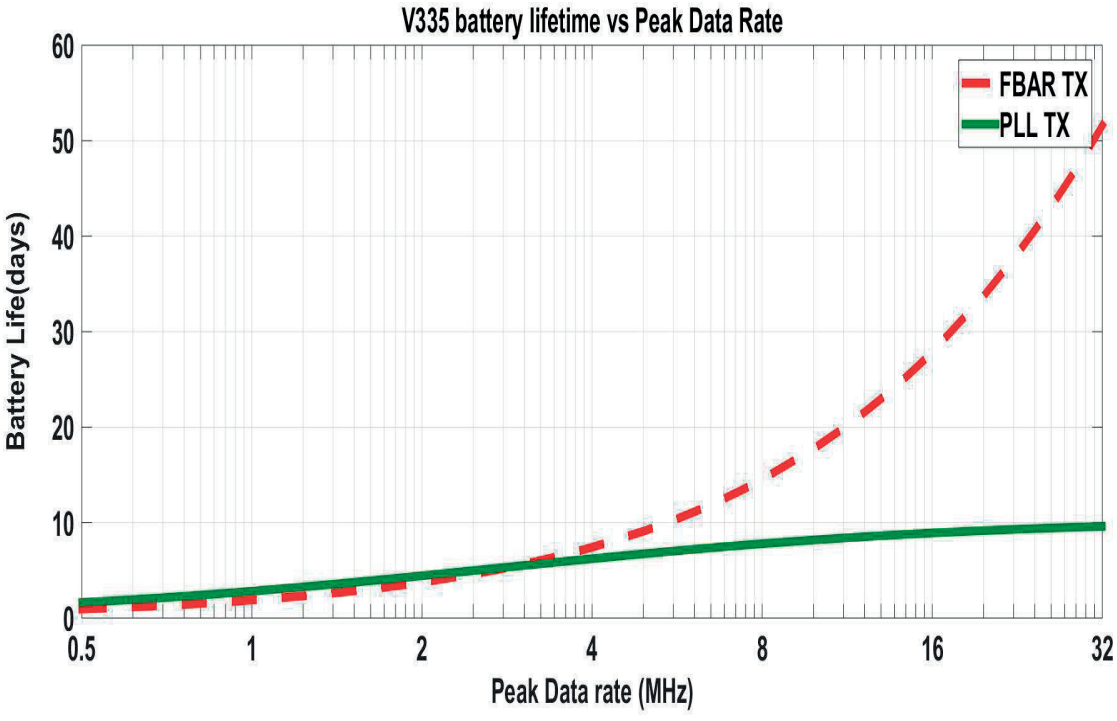
The polar modulation measurements were conducted at 600 kS/s at carrier frequency of 2.4 GHz. The measured spectrum is compared to the spectrum resulting from high level Matlab simulations in figure 3.34. Compared to simulated results, measured spectrum shows only a minor increase of signal level outside of the desired channel. Nevertheless, ACPR remains below -34.3 dB, well within the standard specifications.

Figure 3.35 illustrates the impact of the transmitter linearity on the output spectrum. The spectral regrowth in the output depends on the feedback factor which affects the transmitter linearity. The more the feedback factor deviates from the optimum, the more the spectral regrowth will be. One such example, where the feedback factor value is lower than optimum, is shown in figure 3.35. The worst case where there is no feedback (a constant envelope signal) is also shown in the figure; with this spectrum clearly violating the spectral mask of IEEE 802.15.6 as expected.

Another factor that determines whether the signal spectrum falls within the defined mask is the differential delay between the amplitude and the phase signal. A small delay will only cause




(a) Variation of lifetime of CR2032 battery with increasing data rate




(b) Variation of lifetime of V335 battery with increasing data rate

a minor asymmetry in the spectrum (typical for polar transmitters [22]). Larger differential delay may cause significant spectral regrowth and eventually violation of the spectrum mask

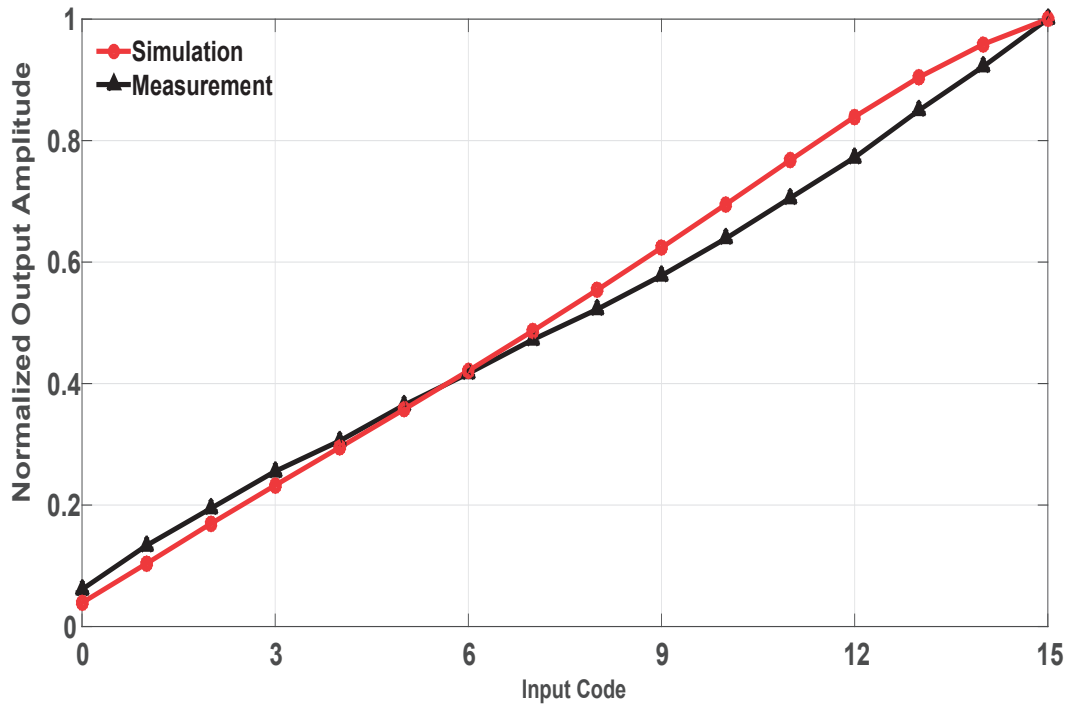



Figure 3.33 – Comparison of simulated and measured normalized output voltage as a function of input code word

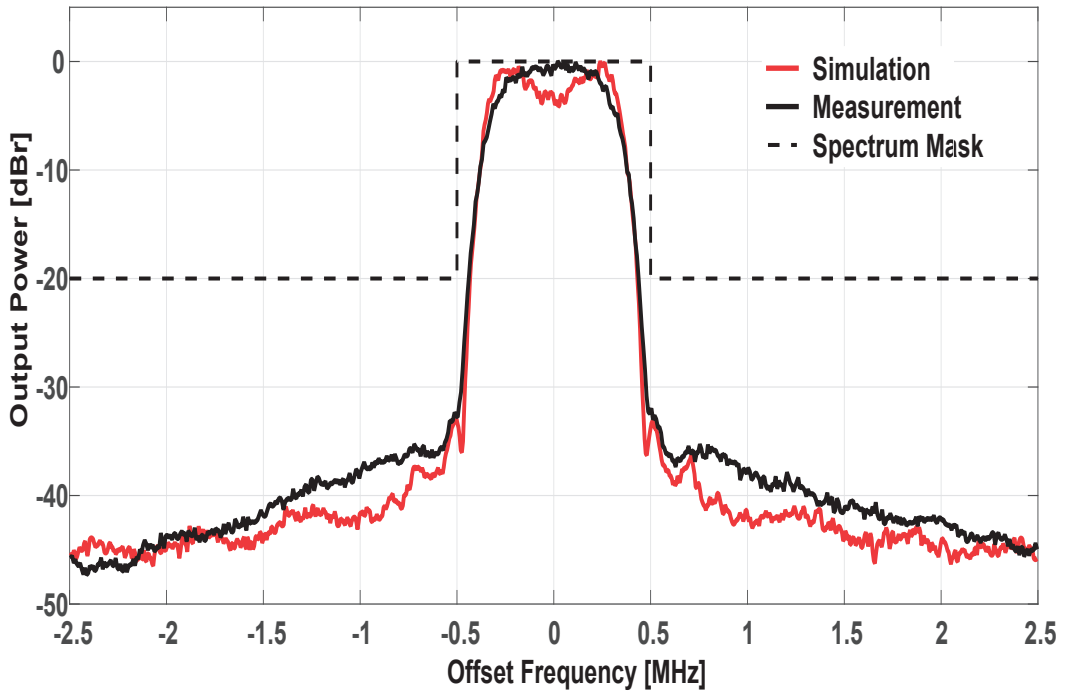



Figure 3.34 – Comparison of measured and simulated output spectrum

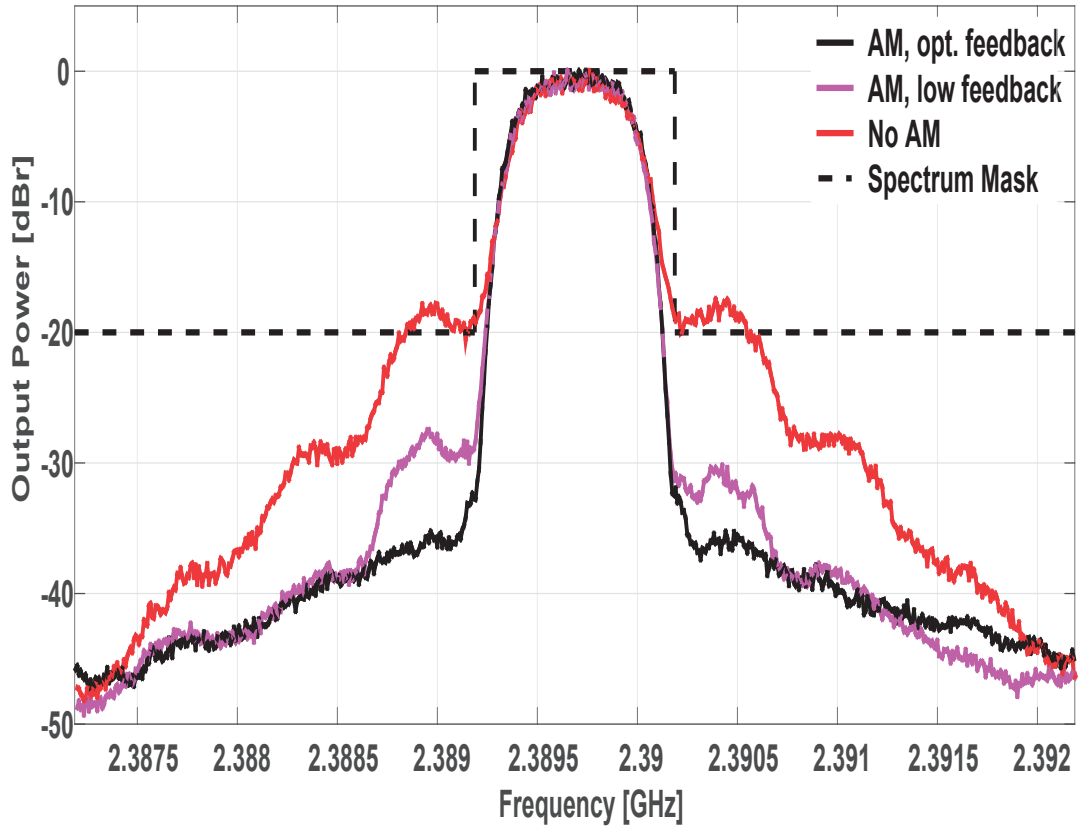
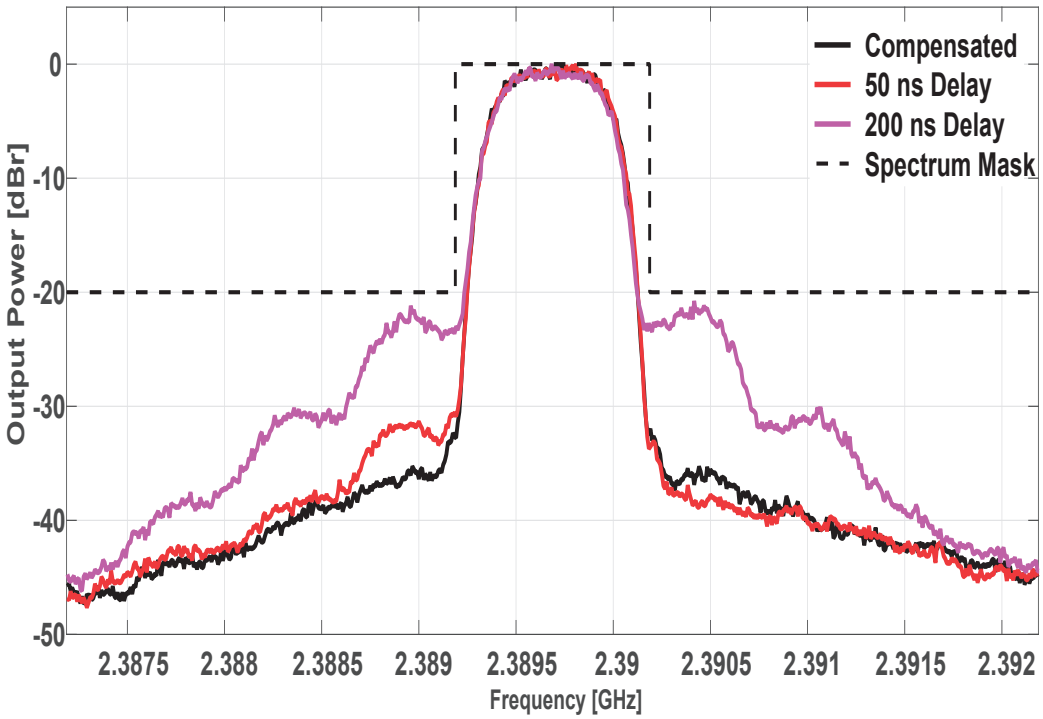



Figure 3.35 – Comparison of measured output spectrum with and without amplitude modulation

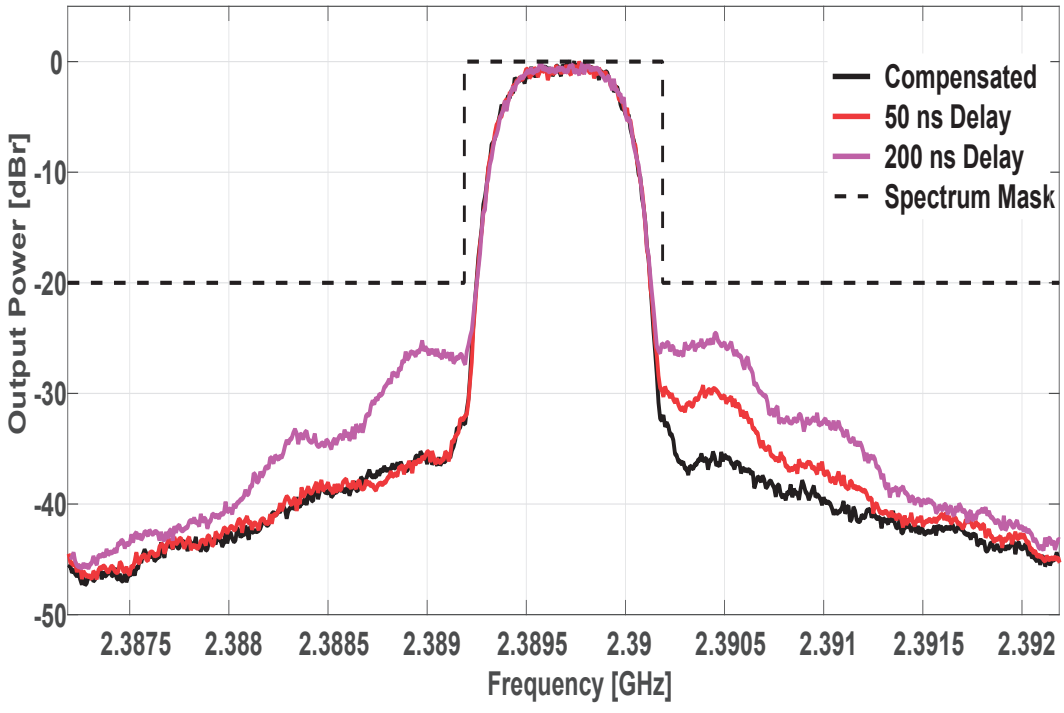
as shown in figures 3.36a and 3.36b. However, due to the loose constraints of the IEEE 802.15.6 standard, a delay up to 200 ns, or approximately one-eighth of the symbol time, can be tolerated.

At the maximum output power level of 0 dBm, the efficiency of the PA, including the power consumption of the pre-amplifier and the bias circuit, is 16% as shown in figure 3.37.

The eye diagrams for $\pi/2$-DBPSK and $\pi/4$-DQPSK is shown in figure 3.38. The measured EVM RMS is 5.11% for $\pi/2$-DBPSK and 6% for $\pi/4$-DQPSK. Both these values are within the limits defined by the standard (17% for $\pi/4$-DQPSK). The performance comparison of this transmitter with other low power transmitters in literature is shown in Table 3.2. Amongst the transmitters in the table, [7] and [23] seem to achieve better Energy/bit figures than this work. But they have serious shortcomings as in [7] is restricted to 3 channels and uses 3 FBAR to generate 3 separate LO signals. This not only severely hampers the scope of this work for deployment in IoT, it also makes packaging of the system, a very difficult proposition. Whereas the TX of [23] is designed for frequencies around 400 MHz. By contrast, the proposed work can cover all the channels over a wide range of frequencies while using a single FBAR. In addition, both these transmitters output much less power compared to the TX proposed in this work




(a)




(b)

Figure 3.36 – Measured output spectrum for different values of (a)amplitude delay (b) phase signal delay

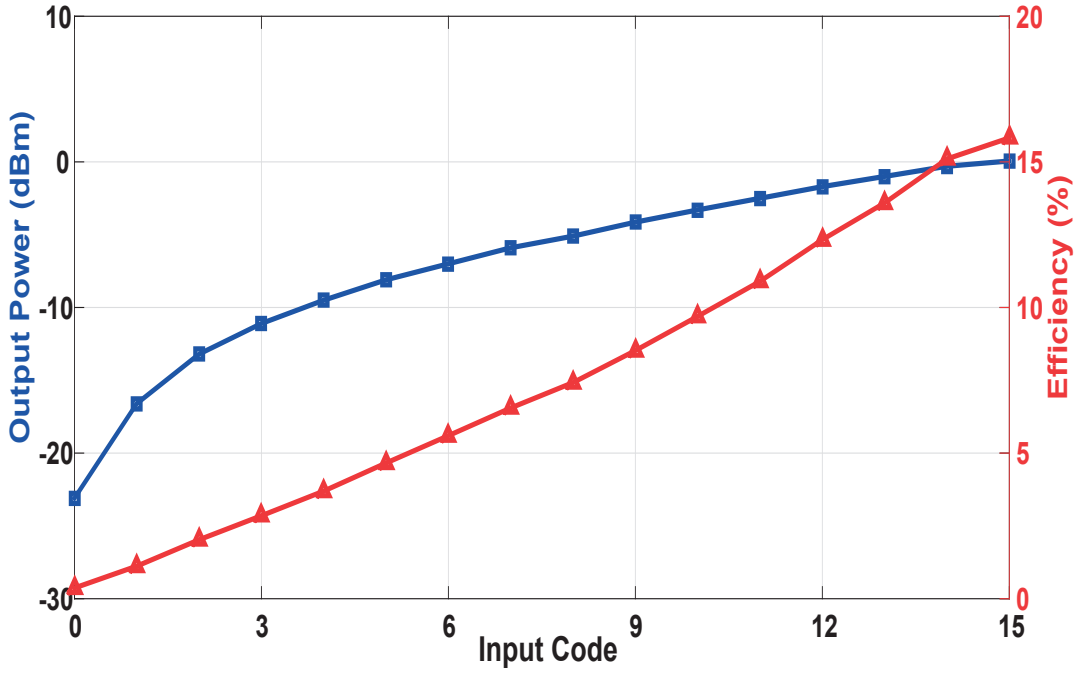
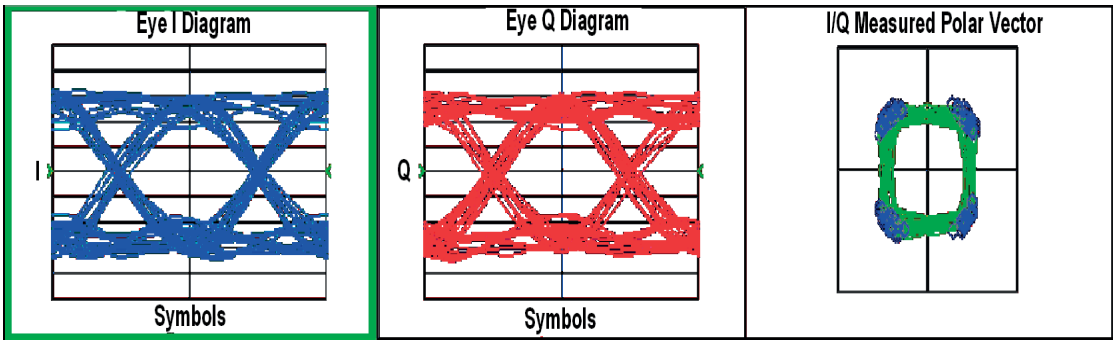
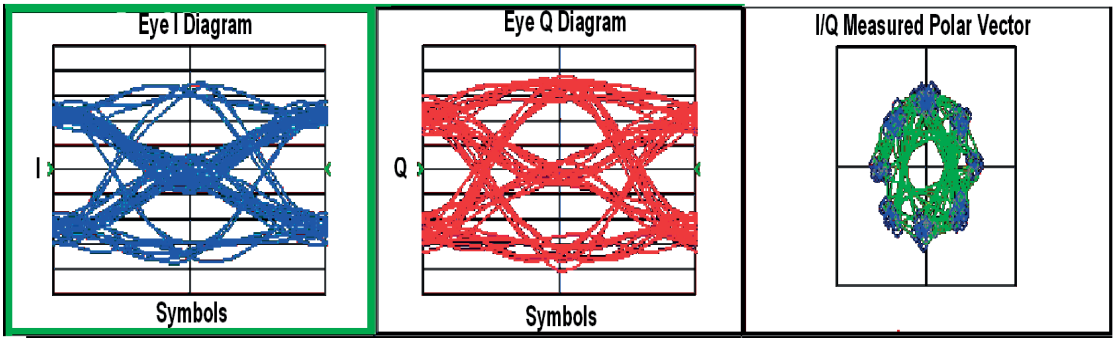



Figure 3.37 – Output power and drain efficiency as functions of input code word




(a)




(b)

Figure 3.38 – (a)Eye diagram of $\pi/2$-DBPSK modulation (b)Eye diagram of $\pi/4$-DQPSK modulation

and do not support as high a data rate. Although fast settling PLLs have been designed with a settling time of a few $\mu s$, the XO start up still remains as discussed previously; which is one of the areas where this synthesizer outperforms the conventional PLLs. For example, the PLL presented in [24] has a settling time of 40 $\mu s$, which allows fast channel switching, however full wake-up time is not reported; yet it can be expected to be in the order of hundreds of $\mu s$.

Table 3.2 – Performance comparison of the FBAR based Transmitter with prior literature

| Parameter | [25] | [24] | [23] | [6] | [7] | **This work** |
|---|---|---|---|---|---|---|
| Architecture | PLL based | PLL based | DLL based | FBAR based | FBAR based | FBAR and Mixer based |
| Frequency | 2.4 GHz | 2.4 GHz | 400 MHz | 2.4 GHz | 2.4 GHz | 2.4 GHz |
| Peak FSK Data rate | 2 Mb/s | 1 Mb/s | 5 Mb/s | 50 kb/s | 1 Mb/s | 16 Mb/s |
| Power Consumption | 5.4 mW | 8.9 mW | 2.2 mW | 10.8 mW | 0.53 mW | 10.4 mW |
| TX output power | -10 dBm | 0 dBm | -8 dBm | 1 dBm | -12.5 dBm | 0 dBm |
| Start up time | 40 $\mu s$ | N/A | N/A | 2 $\mu s$ | 4 $\mu s$ | 5 $\mu s$ |
| Channels switching | Yes | Yes | Yes | No | Restricted to 3 | Yes |
| DCO PN (dBc/Hz) | -112 @ 1 MHz | -87 @ 130 kHz | -107 @ 1 MHz | -126 @ 1 MHz | -132 @ 1 MHz | -128 @ 100 kHz |
| Energy Efficiency | 2.7 nJ/b | 6.5 nJ/b | 0.11 nJ/b | 144 nJ/b | 0.53 nJ/b | 0.7 nJ/b |
| $E_{st,tot}$ FoM | 67 $\mu J$ | 89 $\mu J$ | N/A | N/A | N/A | 7.5 $\mu J$ |
| Polar modulation data rate | 1.2 Mb/s | 1.2 Mb/s | 0.8 Mb/s | N/A | 1 Mb/s | 1.2 Mb/s |
| EVM RMS(%) | 7.3 | 10 | 2 | N/A | 6 | 6 |
| ACPR (dB) | -32 | -26 | N/A | N/A | N/A | -34.4 |
| PA Efficiency (%) | 3.4 | 20.3 | N/A | N/A | 33 (PA only) | 16 |
| Technology | 90 nm | 130 nm | 65 nm | 130 nm | 65 nm | 65 nm |

## 3.4 Summary and Prospective work

A high data rate capable transmitter employing a frequency synthesizer based on an FBAR as a frequency reference enables fast start up of 5 $\mu s$ has been presented in this chapter. The FBAR DCO has been implemented using a complementary cross coupled structure in order to halve the power consumption. By using a Phase Switching Divider, this synthesizer was able to overcome the limited tuning range of the FBAR to cover a wide frequency range, as well as to support data rates of up to 16 Mb/s. The high data rate enables a higher rate of duty cycling. This, in turn reduces the energy overhead of the system by 34x as compared to a PLL based system with a crystal oscillator as the reference; which makes this transmitter adept to be employed in Ultra Low Powered systems like IoT, WBAN etc. In addition to this, a dynamic biasing circuit that enables a linear PA operation was also presented; which makes the TX capable to handle standards that require polar modulation such as IEEE 802.15.6.

Concerning the prospective work, there is a scope for improvement on compensating for the FBAR frequency drift with temperature. Even after employing the open loop compensation scheme, the temperature dependent frequency drift of the FBAR DCO was measured to be around 25 ppm. Temperature compensated crystal oscillators have much better frequency stability as their frequency deviation is around 1 ppm over a large temperature range [26]. Therefore, there is a need to improve the FBAR temperature behaviour and this requires improvement on both the FBAR design procedure as well as from the circuit perspective. While the FBAR design itself is out of the purview of this work, the open loop temperature compensation scheme describe herein can be improved by increasing the polynomial order for better curve fitting and proceeding to compensate for the frequency variations.

Another point on which work has to be done is the packaging of the FBAR resonators together with the CMOS ICs so that the entire radio remains miniature. Indeed, this was one of the main advantages of choosing FBAR over the bulky quartz crystals. One solution for low-cost packaging was described in [27] wherein the CMOS IC forms a part of the lid of a hermetic package that contains the FBAR, while the interfacing between the resonator and the IC can be provided by a gold-tin eutectic bond.

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# 4 FBAR based Transmitters: Evolving from Analog to Digital Synthesizers

The rapid proliferation of Internet of Things (IoT) in recent years imposes many constraints on the radios employed in these IoT nodes, the primary of which is to reduce the power dissipation so as to improve the energy autonomy. Conventional radios that communicate continuously are ill suited for such autonomous nodes since the power dissipation in such cases is dominated by the Power Amplifier irrespective of technology scaling. Indeed, as shown in the Introduction, the power dissipation of the State-of-the-Art (SoTA) radios has remained more or less constant over the recent years (figure 1.5). In order to overcome this minimum energy barrier, duty cycling has emerged as one of the preferred methods for communication. To obtain maximum mileage out of duty cycling, both the active energy dissipation and the energy overhead of the radio has to be minimized [1], as demonstrated in the previous chapter. In addition, the synthesizer employed in the radio must be frequency agile, in order to achieve robust performance in the presence of interferers. The reduction of the energy overhead was discussed in the chapters 2 and 3 of this thesis. Whilst the former showed the ways to increase the bandwidth of a loop based synthesizer without compromising its noise performance so as to minimize the energy overhead due to the synthesizer settling, a PLL-free, FBAR based synthesizer (TX) was introduced in the latter. This FBAR based synthesizer had the advantages of having a very rapid wake up, being frequency agile and supporting moderately high data rates [2]. But the main issue with such a synthesizer is that the frequency range trades off with the maximum data rate (a few Mbps with a given modulation index) and both of these parameters are constrained solely by the FBAR tuning which is in the order of a few MHz. This can be seen from equation 3.9 which shows that the wider the frequency range of the synthesizer is, the lower the maximum data rate that can be achieved and vice versa. Moreover, the synthesizer employs an active analog mixer to generated the wanted output frequency from the FBAR LO signal and its divided version. The use of such an analog synthesizer is not favourable to technology scaling in terms of area (since the mixer uses an inductor to reduce the loading by the input capacitance of the succeeding PA stage), mismatch, etc. Therefore there is a need to find a completely digital solution that would the incorporate features such as frequency agility, low overhead and high data rate capability. Such a synthesizer could potentially become the mainstay of the future IoT radios. Is such a synthesizer possible?

In terms of frequency agility and being conducive to technology scaling, Direct Digital Synthesizers (DDS) have proven to be an effective solution [3], [4], [5]. These synthesizers map an input word which represents the wanted output frequency to the stored time dependent amplitude information to build the desired signal. Figure 4.1 shows the block diagram of the DDS. The system consists of a frequency control register that stores an input Frequency Control Word (FCW) whose value is proportional to the desired frequency. This is followed by a Numerical Controlled Oscillator (NCO) which accumulates the FCW and produces a sampled output at the reference clock rate($f_{ref}$). Finally this sampled value is mapped to the stored amplitude values and fed to a DAC sampled at $f_{ref}$. This is followed by a smoothing Low Pass Filter to remove the frequency aliases. The direct mapping of the FCW directly to the output signal without any loop helps the system immensely to achieve high frequency agility. While the DDS is very versatile due to the fact that it can produce any shape of output waveform, it suffers from two major problems. First is that the maximum clock frequency of the system is limited to half the reference frequency due to the need to satisfy Nyquist's criterion. Second is the extremely high active power consumption of the system. For instance, the SoTA DDS designed in 28 nm technology [6] consumes 68 mW to generate frequencies in the vicinity of 1 GHz.

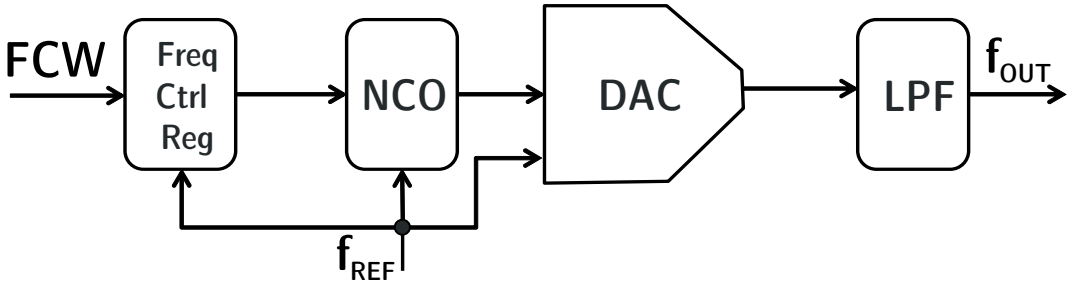



Figure 4.1 – Block Diagram of a Direct Digital Synthesizer

An alternative to the time domain DDS is to move to the phase domain where information about the zero crossings could be used to build the desired frequency signal albeit with a fixed amplitude. Combined with a ΣΔ modulator to perform noise shaping as well as an FBAR for rapid wake up, this synthesizer could achieve very low energy overhead and be frequency agile. Furthermore, such a synthesizer could support data rates of up to tens/hundreds of Mbps since the data rate depends only on the speed of the ΣΔ which is technology dependent. This chapter describes the design of one such Phase Domain Direct Digital Synthesizer (PDDDS), while also including the persisting design challenges and prospectives for future improvements. The organization of this chapter is as follows: First, the principle of the PDDDS is shown, followed by the design of the various circuit blocks. Special emphasis is given to the design of the ΣΔ modulator which is one of the most important circuit blocks. This section includes the design of a Hybrid Requantizer (HRQ) to reduce the impact of the level of the spurs that arise due to the nonlinearity of the frequency synthesizer. Finally, the measurements of a prototype PDDDS based TX are provided, followed by recommendations for future work.

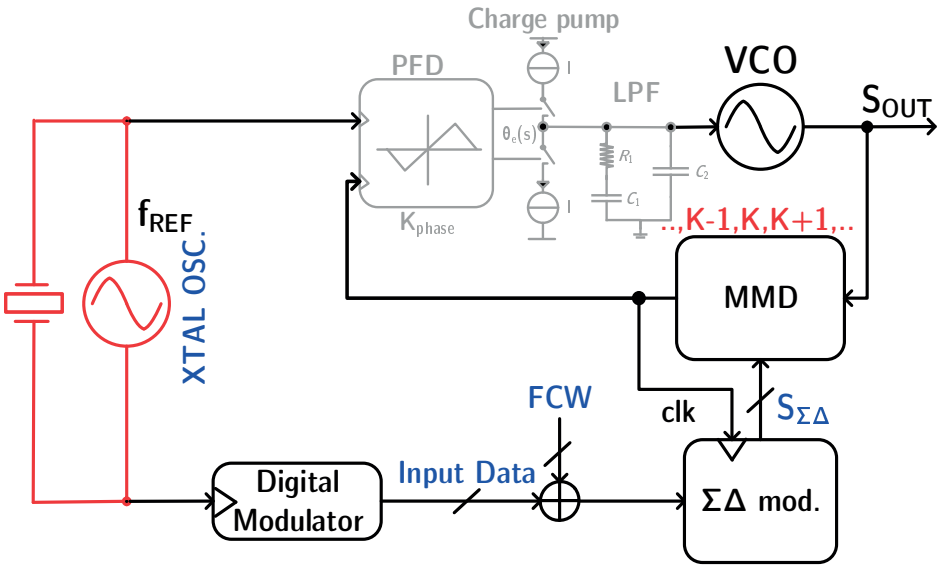



Figure 4.2 – Block Diagram of Fractional-N frequency synthesizer

## 4.1 Phase Domain Direct Digital Synthesizer: Principle

The idea behind the PDDDS is the traditional fractional-N frequency synthesizer whose block diagram has been reproduced in figure 4.2. The Multi-modulus Divider (MMD) of the synthesizer divides the output frequency based on the output of a ΣΔ modulator which dithers the division ratio between different values $(..., K-1, K, K+1, ..)$ so that the average divided output frequency is equal to the reference frequency. The data to be modulated is directly fed to the ΣΔ with the digital modulator being clocked by the reference frequency itself.

By slightly modifying the fractional-N synthesizer, the basic circuit for a PDDDS can be obtained, as shown in figure 4.3. The first modification is to replace the reference crystal oscillator with an FBAR DCO which serves as the high frequency reference. Then the PSD, charge pump and the LPF are removed. The VCO is replaced by a frequency multiplier by $K$ and is then fed to the MMD. Thus, by dithering the division ratios, various frequencies in the vicinity of $f_{REF}$ can be synthesized. Therefore, the desired output signal is simply the output of the MMD. This output signal also clocks the ΣΔ modulator. But since this output signal is at RF, it is difficult if not impossible to design the ΣΔ for operating at such high frequencies. Therefore, a $divide-by-N$ circuit is implemented, the output of which serves as the clock to the ΣΔ [7].

The major issue with such a setup is that the high frequency reference signal is multiplied by $K$ and hence the MMD working at this frequency $(Kf_{REF})$ would result in a huge power dissipation. Therefore, there is a need to virtually synthesize a $Kf_{REF}$ signal to be fed to the MMD which would lead to the same desired functionality without increased power. This can be achieved by using a $K$-stage ring oscillator injection locked to the reference oscillator. The ring oscillator produces multiple edges whose frequency is $Kf_{REF}$. By manipulating these

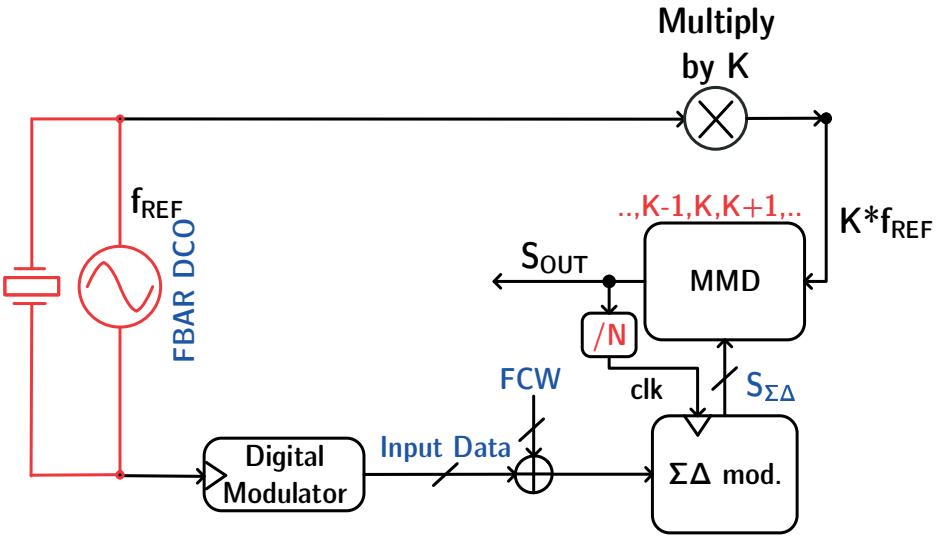



Figure 4.3 – Basic principle of Phase Domain DDS

edges appropriately and dividing the resultant, the desired output frequency can be produced. Since the MMD cannot deal with the virtual LO, a specialized circuit is needed for this purpose. This is depicted in figure 4.4 which shows the block diagram of the implemented PDDDS.

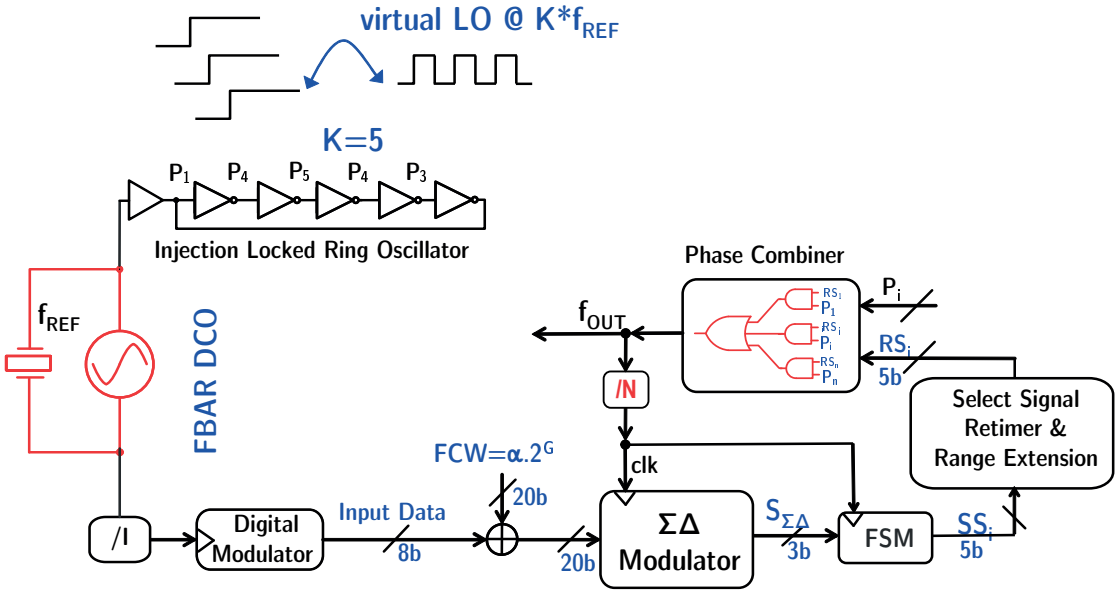



Figure 4.4 – All Digital Open-Loop Synthesizer : Block Diagram

As mentioned previously, the frequency synthesis starts with the FBAR DCO which generates a stable high frequency reference signal. This reference signal injection locks a ring oscillator thereby producing multiple phases at the reference frequency. As explained in chapter 2, the

multi-phase injection locking is employed here which serves to reduce phase imbalances due to slightly different load at one of the inverter stages. Then, by linear combination of these various phases of the LO signal based on the outputs of a ΣΔ modulator, an RF signal is produced, whose average frequency is equal to the desired output frequency. Going back to the block diagram, in parallel to the $K$ phases being produced by an Injection Locked Ring Oscillator, the Select Signals (SS signals in figure 4.4) are produced by a Finite State Machine (FSM) based on the output bits ($S_{\Sigma\Delta}$) of the ΣΔ modulator. These SS signals are resynchronized to their corresponding phases in a retimer block to yield the RS signals. The process of resynchronization is critical to this synthesizer to avoid momentary glitches and cycle skipping in the output signal which will translate to erroneous output frequencies and will also show up as noise in the output spectrum. The RS signals are then multiplied with the phases using AND gates and the resultant signals are then summed to produce the required output RF signal $S_{OUT}$. To extend the frequency range of this synthesizer, the Retimer circuit also includes a Range Extend block (RE). Frequency modulation can be performed in this circuit by adding the output of a digital modulator directly to the input of the ΣΔ. The digital baseband which includes the modulator is clocked by the FBAR reference frequency divided by an integer $I$. Both the ΣΔ modulator and the FSM are clocked by a divided version of the output signal itself; $f_{CLK} = f_{OUT}/N$, with $N$ being an integer and $f_{OUT}$ being the frequency of $S_{OUT}$.

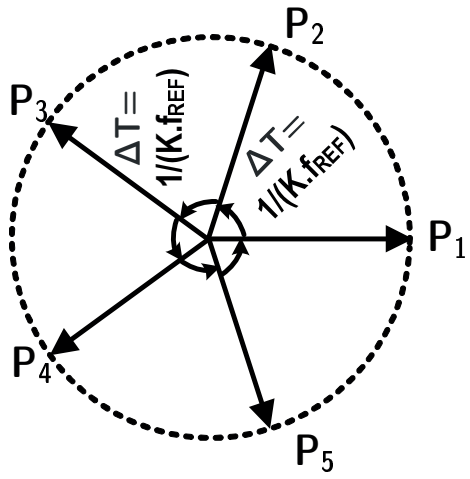



Figure 4.5 – Time separation of the phases of the ring oscillator

The input to the ΣΔ is the FCW which can be written as $\alpha \cdot 2^G$, where $G$ is the ΣΔ bit width. Denoting the FBAR output signal as $f_{REF}$, a $K$ stage ring oscillator which is injection locked to this reference signal produces $K$ phases. The delay between these phases is then $1/(Kf_{REF})$ as shown in figure 4.5. From here on, the phases combination process produces the output signal whose frequency, for each ΣΔ clock cycle (= N cycles of the output), deviates from the reference frequency for only one cycle i.e. $(N-1)$ cycles of the output have a time period of $1/f_{REF}$ and one cycle has a duration given by $(K+S_{\Sigma\Delta})/(Kf_{REF})$, where $S_{\Sigma\Delta}$ is an integer and

is the momentary output of the ΣΔ modulator. This is illustrated in the timing diagram of figure 4.6 which shows the sequential signal generation process for an example with N=4 and K=5. As expected, the instantaneous frequency of the output signal is $f_{REF}$ for 3 cycles and $5f_{REF}/(S_{\Sigma\Delta}+5)$ for one cycle. The average output time period per each ΣΔ clock cycle of this approach is given by

$$T_{OUT,ave,CLK} = \frac{(N-1)+\frac{K+S_{\Sigma\Delta}}{K}}{N} T_{REF}. \tag{4.1}$$

The corresponding frequency is obtained after simplification is

$$f_{OUT,ave,CLK} = \left(\frac{1}{1+\frac{S_{\Sigma\Delta}}{KN}}\right) f_{REF}. \tag{4.2}$$

The average output frequency after the ΣΔ has cycled through all its $2^G$ states is then

$$f_{OUT,ave} = \left(\frac{1}{1+\frac{\alpha}{KN}}\right) f_{REF}, \tag{4.3}$$

where $\alpha$ is the average of the ΣΔ modulator output.

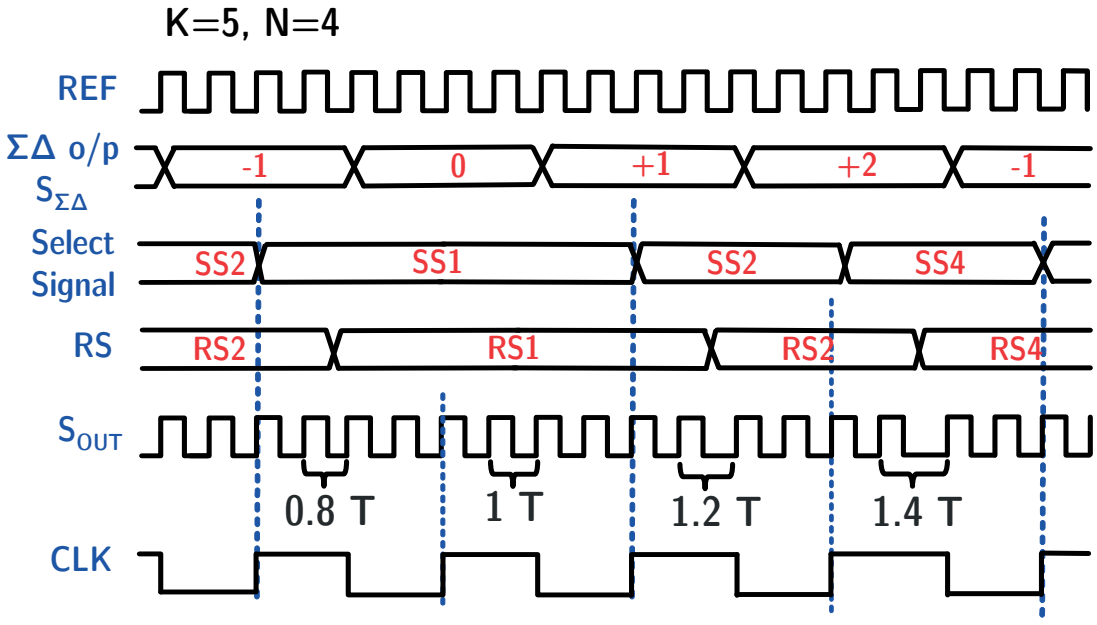



Figure 4.6 – All Digital Open-Loop Synthesizer : Signal Diagrams

The conversion of the ΣΔ output into the desired signal in this synthesizer is similar in principle to the conventional DDS [8]; but instead of the instantaneous amplitude, the FCW is mapped to the instantaneous frequency of the signal $f_{OUT}$. In effect, the injection locked ring oscillator, the FSM, the phase combiner and the associated circuitry serve as a DAC which converts the FCW to the desired frequency output. At this point, it is imperative to note that this loop-free

direct digital frequency synthesis is made possible only thanks to the very high frequency stability of the FBAR. Therefore it is necessary to compensate for the frequency variations of the FBAR with respect to temperature as explained in chapter 3.

The maximum frequency that can be synthesized by this process is the same as that of the FBAR frequency $f_{REF}$. The minimum frequency synthesizable can be calculated as follows: Since the maximum value of the FCW input for a ΣΔ of bit width $G$ is $2^G - 1$, the maximum value of $\alpha$ is $\left(2^G - 1\right)/2^G$. Now, substituting for $\alpha$ in equation 4.3, which yields the minimum frequency as

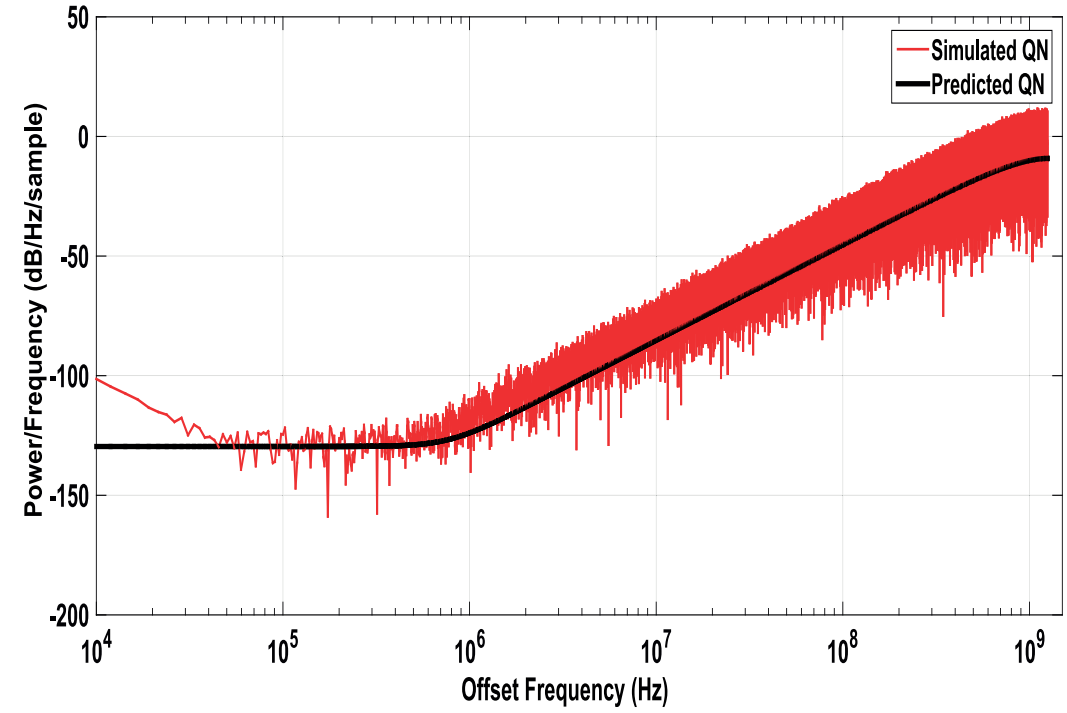
$$f_{OUT,min} = \left(\frac{1}{1 + \frac{2^G - 1}{2^G KN}}\right) f_{REF} \approx \left(\frac{1}{1 + \frac{1}{KN}}\right) f_{REF}. \tag{4.4}$$

Thus, for large values of $G$, the frequency range of this system is solely dependent on the parameters $K$, the number of stages in the ring oscillator and $N$, the frequency of the ΣΔ modulator by inverse proportionality. Therefore, one way to increase the frequency range of this system is to increase the speed of the ΣΔ as well as the number of stages of the ring oscillator, both of which come at the cost of increased power consumption.

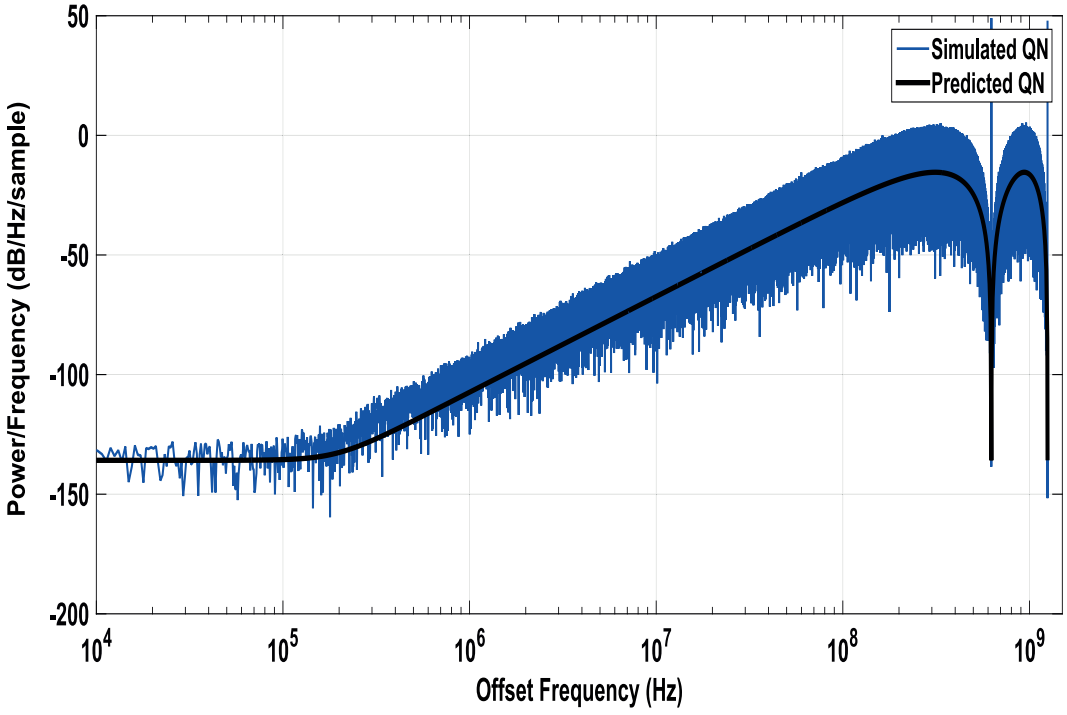
The parameters $N$ and $K$ also determine the Quantization Noise (QN) of the ΣΔ modulator. This in-turn affects the noise performance of the synthesizer since the QN of the ΣΔ dominates the output synthesizer noise at high frequency offsets. Also, as it is shown later, the ΣΔ also determines the close-in noise due to noise folding. An increase in $K$ reduces the time difference between two phases of the ring oscillator which also means a reduced quantization step size for the ΣΔ and hence the noise is expected to decrease proportionally. In addition, since the ΣΔ operates at $N$ times lower frequency as compared to that of the output signal, the QN at the output can be expected to be compressed in the frequency domain by a factor $N$. For example, the QN in the case where the ΣΔ is implemented as a MASH modulator reaches its maximum at an offset frequency of $(f_{REF}/2N)$ instead of $f_{REF}/2$. This can be seen from the figure 4.7. The quantization noise of a MASH modulator of order $m$ is shown in equation 4.5.

$$S_{\phi_{out}q}(f_{off}) = \frac{1}{12K^2} \cdot \frac{4\pi^2}{f_{REF}} \left(2sin\left(\frac{\pi N f_{off}}{f_{REF}}\right)\right)^{2(m-1)}, \tag{4.5}$$

where $f_{off}$ is the frequency offset at which the phase noise is measured. Thus an increase of $K$ and a reduction in $N$ both will lead to a decrease in QN. Ideally, one would like $N$ to be '1' to push the QN as far away as possible. But, this is impossible to do since synthesizing the MASH at RF (around 2.4 GHz) is extremely difficult and consumes a large amount of power. In addition, increasing $K$ means increasing the number of stages of the ring oscillator. This, in turn increases the number of Select Signals which corresponds to an increase in the hardware of FSM as well as the retimer block, invariably leading to an increase in the circuit power consumption. Moreover, the number of stages in the ring oscillator also cannot be arbitrarily increased for a particular technology node lest the oscillator will not lock to the desired frequency. Finally, increasing $K$ to reduce noise decreases the frequency range of this




(a)




(b)

Figure 4.7 – Simulated and predicted QN for different values of N (a) $N = 1$ (b) $N = 4$

synthesizer, thus exhibiting a tradeoff between noise and frequency range. In summary, the frequency range vs noise vs power tradeoff of this synthesizer is dictated by parameters $K$ (the number of ring oscillator stages) and $N$ (clock frequency of the $\Sigma\Delta$) both of which are technology dependent. At this juncture, the reader's attention is drawn to the fact that this synthesizer lacks the inherent low-pass filtering mechanism of a PLL and thus a reduction in the QN becomes imperative. Even then, an off-chip BAW or a SAW filter may be required to mitigate the effect of this far away noise. This is the inevitable price to be paid for a loop-free synthesizer architecture. But a positive aspect of this tradeoff is that both the parameters $K$ and $N$ are technology dependent, and therefore a significant improvement can be expected at smaller technology nodes.

The clock frequency of the $\Sigma\Delta$ ($f_{CLK}$) also determines the ideal maximum data rate $DR_{max}$ of this synthesizer which is given by

$$DR_{max} = f_{CLK}/OSR, \tag{4.6}$$

where $OSR$ is the oversampling ratio used in the digital baseband. Here again, lower $N$ leads to a higher $\Sigma\Delta$ frequency and subsequently a higher maximum data rate for this synthesizer. Ddue to noise concerns, the aim is to run the $\Sigma\Delta$ modulator at as high a frequency as possible; as a by-product, this synthesizer can support data rates upto a few hundred Mb/s for a given modulation index as we approach the ideal value of $N = 1$. Imperative to note here is that as explained previously, since the $f_{OUT}$ and subsequently $f_{REF}$ are not momentarily varying, the practical maximum data rate should have to be less than the one specified by equation 4.6. Thus, as a rule of thumb, a safe value of the highest data rate for such a system would be $f_{CLK}/(2 * OSR)$.

The frequency resolution of this synthesizer is determined by the input FCW of this synthesizer. Rewriting equation 4.3 gives

$$f_{OUT,ave} = \left(\frac{1}{1+\frac{FCW}{2^G \cdot KN}}\right) f_{REF}. \tag{4.7}$$

Now, the resolution due to decrementing the FCW by unity gives the expression for the frequency resolution as

$$\Delta f_{Resol} = \left(\frac{1}{1+\frac{FCW-1}{2^G \cdot KN}} - \frac{1}{1+\frac{FCW}{2^G \cdot KN}}\right) f_{REF} \approx \frac{2^G \cdot KN}{\left(2^G \cdot KN + FCW\right)^2} \cdot f_{REF}. \tag{4.8}$$

The minimum resolution of this synthesizer is obtained when the $FCW$ is zero, which is given by

$$\Delta f_{Resol,min} \approx \frac{1}{\left(2^G \cdot KN\right)} \cdot f_{REF}. \tag{4.9}$$

The maximum is when $FCW$ is at its maximum $2^G - 1$, which can be then approximated to be

$$\Delta f_{Resol,max} \approx \frac{2^G \cdot KN}{\left(2^G \cdot (KN+1)\right)^2} \cdot f_{REF}. \tag{4.10}$$

The variation of frequency resolution with FCW for the example with $N = 4$ and $K = 5$ is shown in figure 4.8.

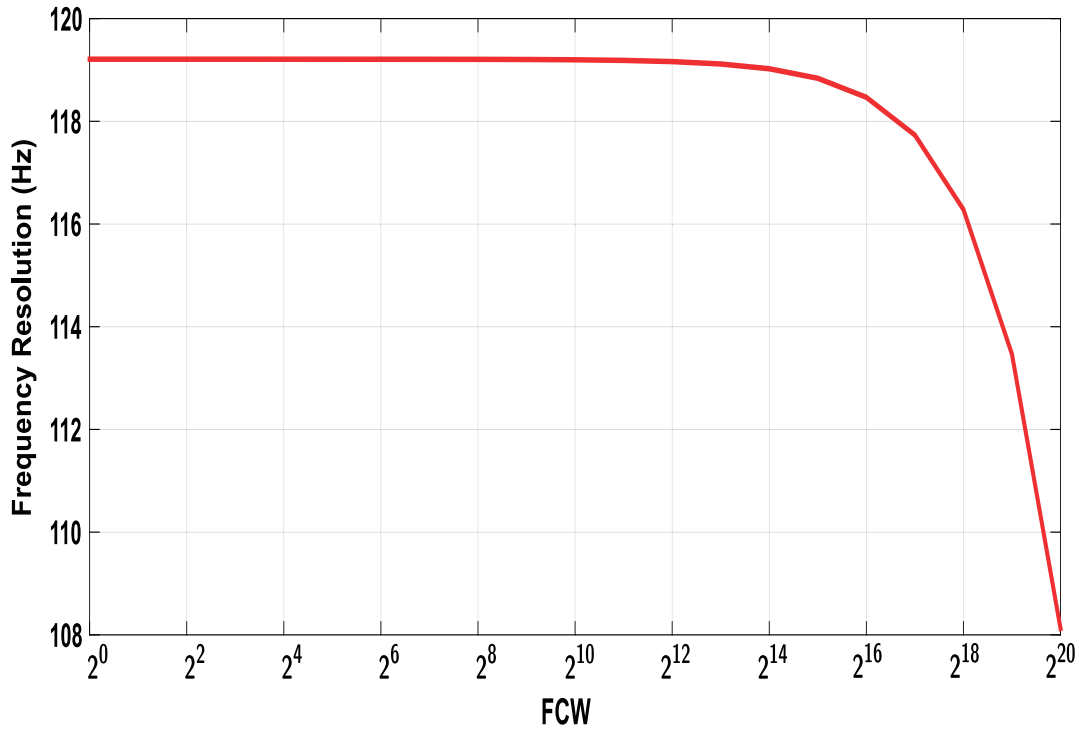



Figure 4.8 – Variation of PDDDS resolution with Frequency Control Word

At this juncture, it is worth mentioning that an alternative method of mapping the ΣΔ was also investigated, in which for a given ΣΔ clock cycle, all the $N$ cycles of the output have a duration $(K + S_{\Sigma\Delta})/(Kf_{REF})$, as shown in figure 4.9. The advantage of this approach over the adopted approach is that it has a better frequency range, with the minimum frequency given as

$$f_{OUT,min,app-II} \approx \left(\frac{1}{1+\frac{1}{K}}\right) f_{REF}, \tag{4.11}$$

which is always lower than the one of the first approach that is given in equation 4.4. But, on the other hand, this approach has more average power dissipation than the adopted approach since the FSM, retimer and the phase combiner have to deal with $N$ times more transitions, thereby increasing the dynamic power dissipation. Furthermore, the QN in the output signal of this approach is also higher than the first as noted from the figure 4.10.

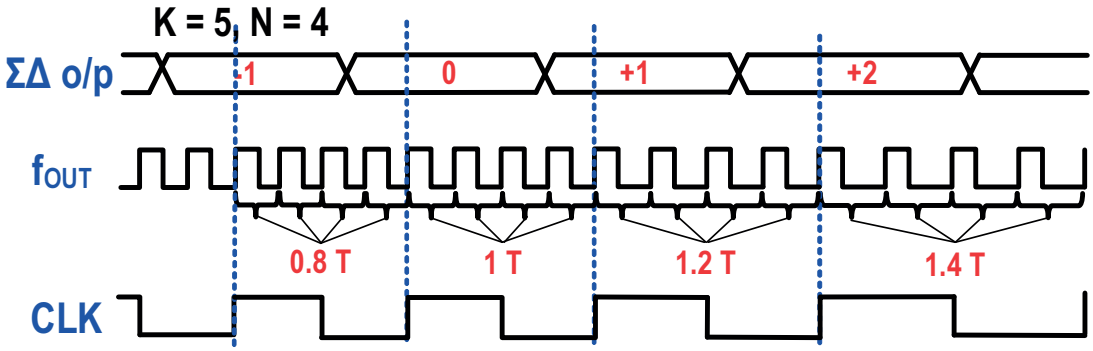



Figure 4.9 – Chronogram of the alternative PDDDS approach

Having discussed the principle of the PDDDS in detail, the following section gives a description of the circuit blocks of the synthesizer.

## 4.2 Synthesizer Blocks

### 4.2.1 FBAR DCO

The FBAR DCO used in this synthesizer is the same as that described in the previous chapter but without the frequency tuning varactors since there is no need to tune the FBAR.

### 4.2.2 Select-signal Retimer

The select signal retimer in this case is built on the same principle as described previously but with a few subtle yet major differences. First, in the case of the resynchronization circuit described in Chapter 2 of this thesis, there was no concern about the duty cycle of the signal at the output of the phase combiner since this signal was fed to an integer divider which operated only on signal edges. But in the case of this synthesizer, since the output of the Phase combiner is the wanted signal itself, care should be taken to avoid any surprising spurious content in the output spectrum. Figure 4.11 depicts the circuit diagram of the proposed retimer circuit. The SR-NOR latch and the dynamic resynchronization latch perform the function of aligning the select signals with the low periods of their respective phases. Readers are requested to refer to Chapter II for the timing diagrams related to these two latches. The output of the dynamic synchronization latch is the signal $L$. This signal is passed through two further dynamic latches $Latch-I$ and $Latch-II$ which are triggered on the rising and the falling edges of the current phase signal $P_i$ respectively. The output of the first latch is the signal $HS_i$ and the second latch is the signal $DS_i$. The other control signal of both these latches is the $HS$ signal (denoted by $HS_{i+1}$) corresponding to the next selected phase. Both the $HS_i$ and the $DS_i$ signals serve as an input to an unconventional Dynamic Flip flop, which then produces the desired output signal. In addition, two latches *viz.* $Latch-III$ and $Latch-IV$, which act on the $HS_i$ and $DS_i$

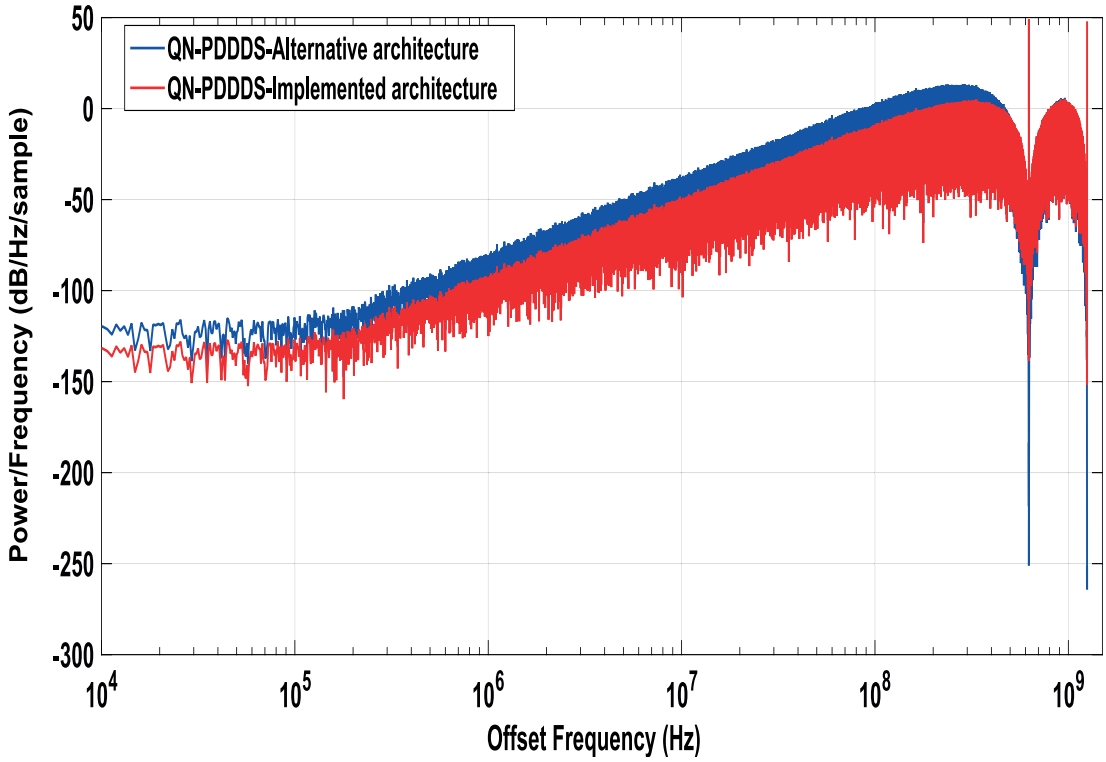



Figure 4.10 – Comparison of Quantization noise in $f_{OUT}$ of the two different PDDDS approaches

signals respectively, are required for correct operation as explained in the following paragraph. In addition, these latches ensure that the logic high portion of the output signal is always at $0.5T_{REF}$.

The functioning of this circuit can be explained using the chronogram given in 4.12. Recalling from Chapter II, for proper glitch-free signal generation, the next select signal $SS_{i+1}$ should transition from logic $low$ to $high$ only when **its corresponding phase,** $P_{i+1}$ **is logic** $low$ **in its current cycle, if and only if the current select signal** $SS_i$ **has transitioned from logic** $high$ **to** $low$ **within the current cycle of** $P_i$. The SR NOR latch and the dynamic synchronization latch take the current select signal and the current phase which is supposed to be selected as input. These latches align the select signal with the logic $low$ portion of the phase signal (signal $L_i$ which is inverted as compared to the $SS_i$). Ideally, if the select signals from the FSM arrive at the same time, then this simple retiming would suffice. But, owing to difference in interconnect parasitics, this is not often the case as a result of which there may be an overlap between the current and the next $L$ signals or there may be a cycle skip as evinced in the chronogram. This will inevitably result in a very slight deviation in frequency. For instance if the system uses a 20 bit ΣΔ modulator with dithering, then the maximum period of such a modulator is $2^{20}$ clock cycles. In addition, with the decimation factor being 4 ($N = 4$), the ΣΔ modulator will repeat for every $2^{22}$ cycles of the output signal. With such a long averaging sequence, missing one cycle will not have a large impact on the output frequency. But this

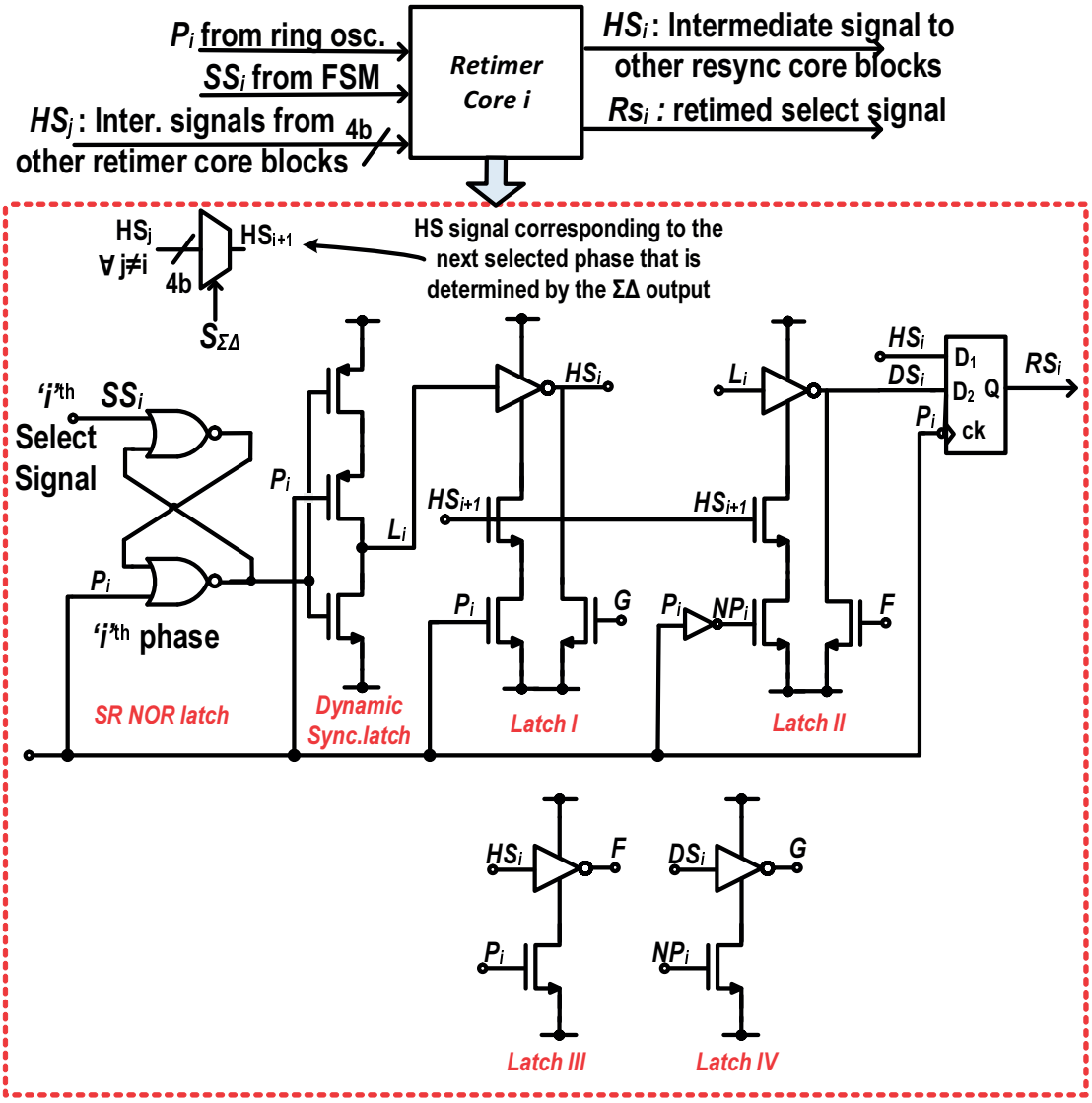



Figure 4.11 – Latch based low power select signal retimer

missed cycle will give rise to spurious components which may mix with the reference frequency and give rise to further spurs. Since this synthesizer lacks any natural filtering ability, any mechanism that gives rise to additional spurs is of great concern.

In order to avoid this cycle skipping and select signal overlap, the signal $L_i$ is passed through a latch ($Latch-I$ in the figure 4.11) whose output is $HS_i$ which is a realigned version of $L_i$. This latch makes sure that the $HS_i$ goes $low$ only when the next realigned select signal $HS_{i+1}$ has transitioned to logic $high$. In order to avoid overlap of the $HS$ signals, one additional latch ($Latch-II$ - output $DS_i$) which operates with the same inputs as $Latch-I$ albeit clocked on the falling edge of $P_i$ is implemented. Two further latches ($Latch-III$ & $Latch-IV$) serve to avoid any race conditions in the circuit. Finally, the $HS_i$ and the $DS_i$ signals serve

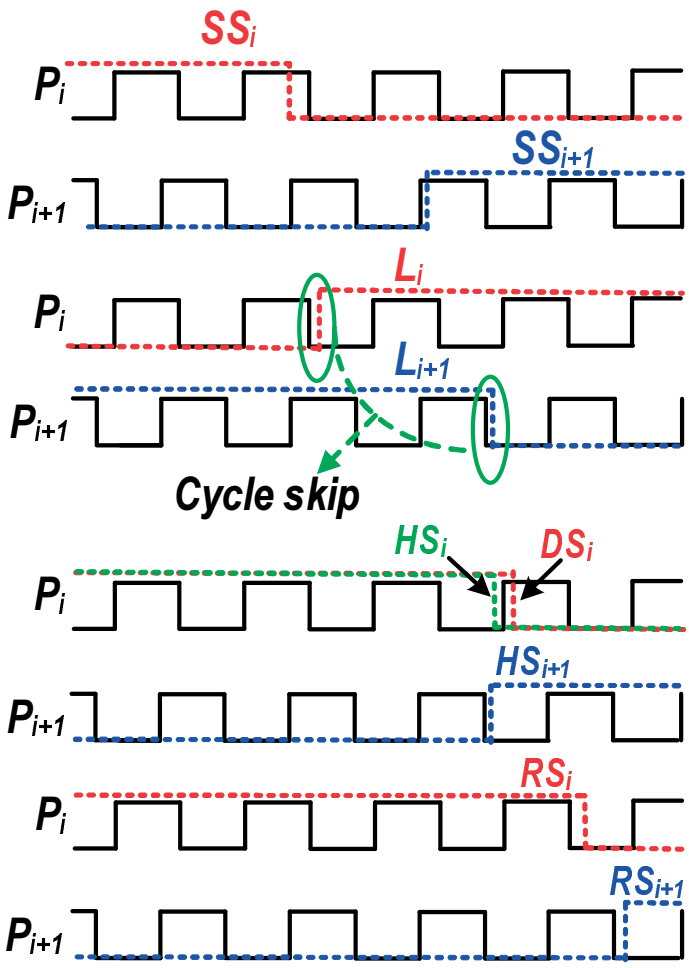



Figure 4.12 – Intermediate signals of the retimer

as inputs to the dynamic flip flop whose circuit diagram is given in figure 4.13. The flip flop is designed using True Single Phase Clocked (TSPC) latches albeit with a small difference. Instead of having a single data input, the flip-flop in this case has two D inputs, namely the $HS$ and $DS$ signals. This makes sure that the resulting retimed select signal ($RS_i$) has no overlap with the next signal $RS_{i+1}$ as well as its transition being aligned with the $low$ period of the phase signal $P_i$. It is important to note here that the clock of this flip-flop is $P_i$, which is at the RF reference frequency $f_{REF}$. In addition, with the $DS_i$ signal aligned to the $high$ period of $P_i$, this negative edge triggered flip flop has essentially less than $T_{REF}/2$ in which to operate. In the worst case of slow corners, this available time can be as small as $T_{REF}/4$, which translates to about 100 ps with a 2.5 GHz reference. Therefore, in order to enable high speed operation, the circuit has been designed using transistors with low threshold voltages. Moreover, the $M_{Pi}$ transistors should be designed to minimize the gate capacitance that can load the phase signal so as to minimize power consumption but at the same time should be designed to be fast enough to handle such a high frequency. The Dynamic flip-flop also includes a Range

Extension circuit which is described in detail in the next section.

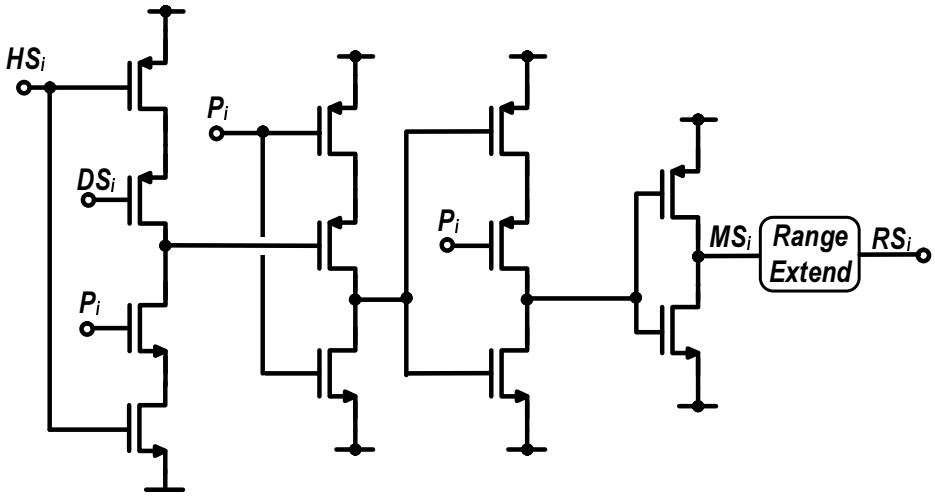



Figure 4.13 – Dual Input Flip Flop used in the retimer

### 4.2.3 Frequency Range Extension

The minimum frequency that this PDDDS can synthesize is given in equation 4.4. Assuming a case of $f_{REF}$=2.47 GHz, K=5, N=4 and a $2^{nd}$ order MASH ΣΔ modulator, the lowest synthesizable frequency is 2.35 GHz. This is a very limited frequency range and is of the similar order as that of the FBAR based analog synthesizer described in the previous chapter. Therefore, in order to improve the frequency range, it is noted that the second order MASH modulator output is bounded between -1 and +2. But, on the other hand there are 5 stages in the ring oscillator i.e. $K = 5$ and thus the FSM can handle inputs ranging from $-\lfloor K/2 \rfloor$ to $+\lfloor K/2 \rfloor$. In this case, this translates to -2 to +2. Therefore, in order to extend the frequency range, the output of the ΣΔ can be decremented by 1 and fed to the FSM. But the problem with this approach is as follows: An input of $-2$ to the FSM corresponds to one cycle of the output signal being $0.6T_{REF}$. This cycle will be logic $high$ for $0.5T_{REF}$ and logic $low$ for $0.1T_{REF}$. With a reference frequency of 2.47 GHz, the logic low period will be around 40 ps. This is a very short duration for the gates of the phase combiner with the given technology node (65 nm) to handle without resulting in one $low$ period being swallowed and subsequently an erroneous output. This is illustrated in figure 4.14. One way to circumvent this restriction is to shift the output of the ΣΔ in the positive direction before it is fed to the FSM. For this, a few Range Extension (RE) bits are added to the output of the ΣΔ. For instance if two range extension bits are added, the output range of the ΣΔ increases to -1,....,+5. But due to the cyclical nature of the phases, any value of $S_{\Sigma\Delta}$ greater than $+K/2$ maps to $(S_{\Sigma\Delta} \bmod K - K)$. Thus +3 will map to -2, +4 will map to -1 and so on, thereby returning to the cycle swallow problem.

To this effect, a slight modification is made to the ΣΔ modulator so that it produces a control signal, $RE_{Ctrl}$ which is logic $high$ for all values of $S_{\Sigma\Delta}$ greater than $+\lfloor K/2 \rfloor$. This control signal is resynchronized and fed to the Range Extension (RE) block that is added after the Dynamic

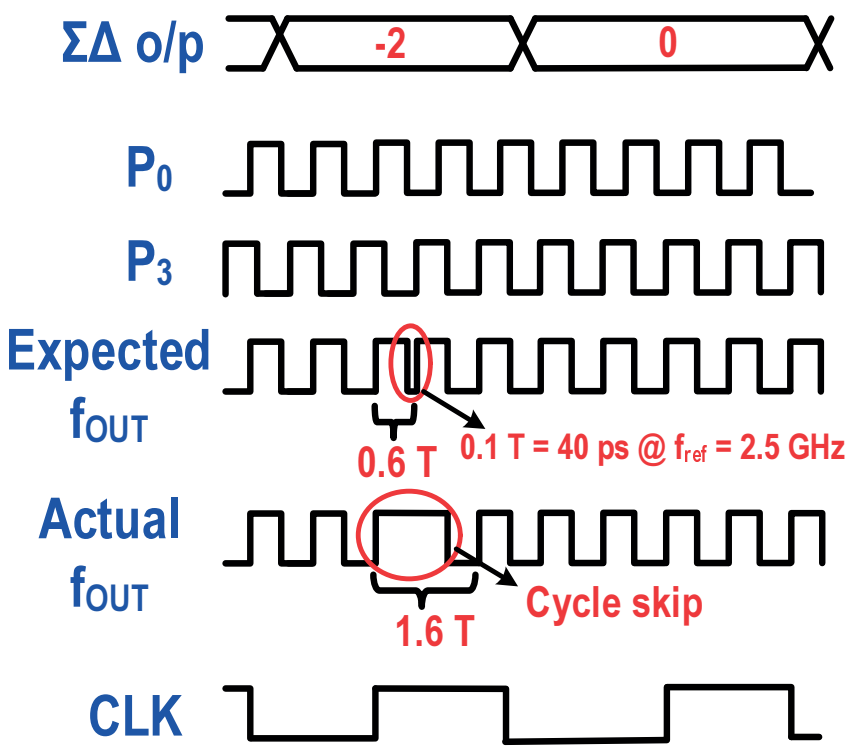



Figure 4.14 – Cycle swallow for $S_{\Sigma\Delta} = -2$ due to short low period

flip flop of the retimer circuit. This RE block modifies the retimed select signal $QS_i$ such that whenever the $RE_{Ctrl}$ signal is high, the logic $low$ to $high$ transition of $MS_i$ is shifted by one clock cycle of the phase signal $P_i$. This introduces a dead time of one clock cycle in the output signal when its instantaneous frequency deviates from $f_{REF}$. Thus, the instantaneous frequency of $f_{OUT}$ will be proportional to $S_{\Sigma\Delta}$. This is illustrated well in the figure 4.16. In the chronogram, the RE bits of value 2 are added to $S_{\Sigma\Delta}$. For the values of $RE + S_{\Sigma\Delta}$ greater than 2 (with $K$ being 5 in this case), the $RE_{Ctrl}$ is high. This causes one cycle dead time in the $RS$ signals where none of the select signals are ON. This results in one cycle of the output signal being swallowed, which yields a time period of $1.6T_{REF}$ corresponding to $S_{\Sigma\Delta}$ of +3, $1.8T_{REF}$ for +4 and so on. Figure 4.15 shows the circuit diagram of this Range Extension block. It consists of an $N-latch$ followed by a $P-latch$ both of which are clocked by the Current Phase $P_i$. These two latches act only on the rising edge of the flip flop's output signal $MS_i$. The latches are enabled / disabled by a retimed version of the $RE_{Ctrl}$ signal. In principle, this Range Extension process can be infinitely extended by cascading multiple Range Extension blocks, which would enable the synthesizer to generate any frequency from DC to $f_{REF}$. But, with the addition of each RE block, the duty cycle of the output signal will get smaller and smaller, causing the spurs due to both the odd and the even harmonics, to grow rapidly. Once again, the inherent lack of filtering would result in significant power to be present in other frequency bands - a rather unpleasant scenario.

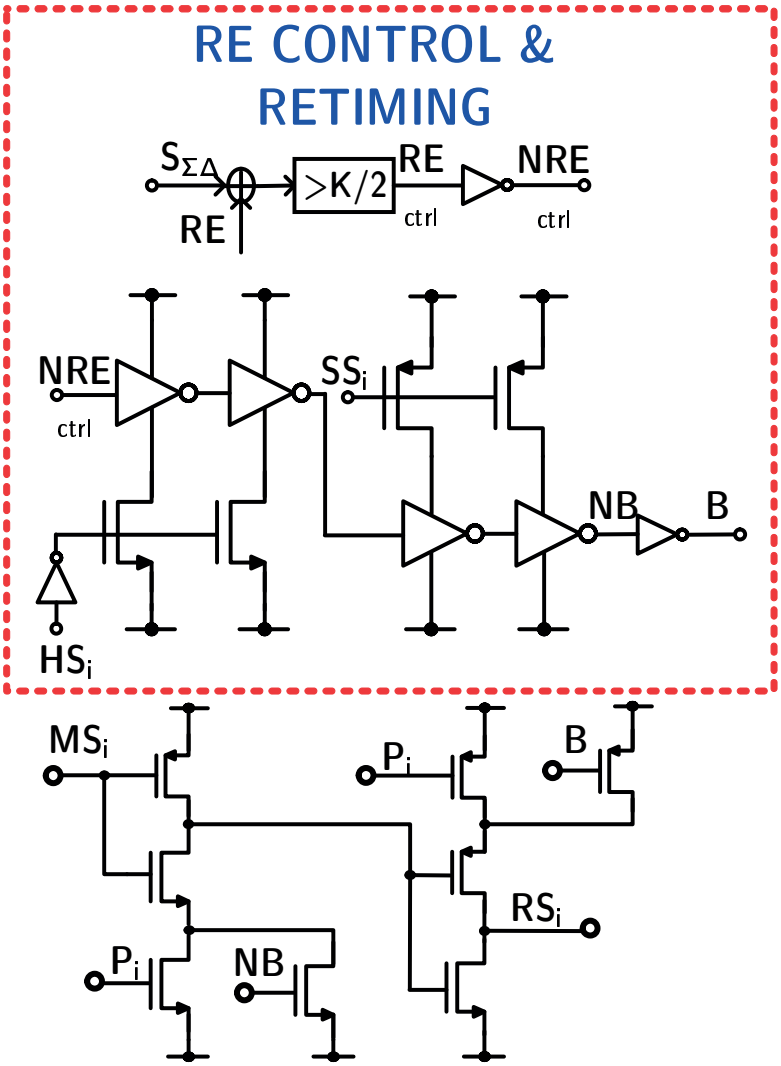



Figure 4.15 – Range Extension Circuit

The lowest frequency that can be synthesized by the PDDDS after the addition of the RE block can be calculated using the following rationale: The addition of one RE bit is akin to virtually extending the bit width of the ΣΔ modulator by '1'. The maximum value of the FCW that can be applied to the ΣΔ is $2^{(G+RE)}-1$. Rewriting equation 4.4 with this new maximum of the FCW gives

$$f_{OUT,min,RE} = \left(\frac{1}{1+\frac{2^{G+RE}-1}{2^G KN}}\right) f_{REF} \approx \left(\frac{1}{1+\frac{2^{RE}}{KN}}\right) f_{REF}. \tag{4.12}$$

The ratio of this new minimum frequency to that of equation 4.4 is

$$\frac{f_{OUT,min,RE}}{f_{OUT,min}} = \frac{KN+1}{KN+2^{RE}}. \tag{4.13}$$

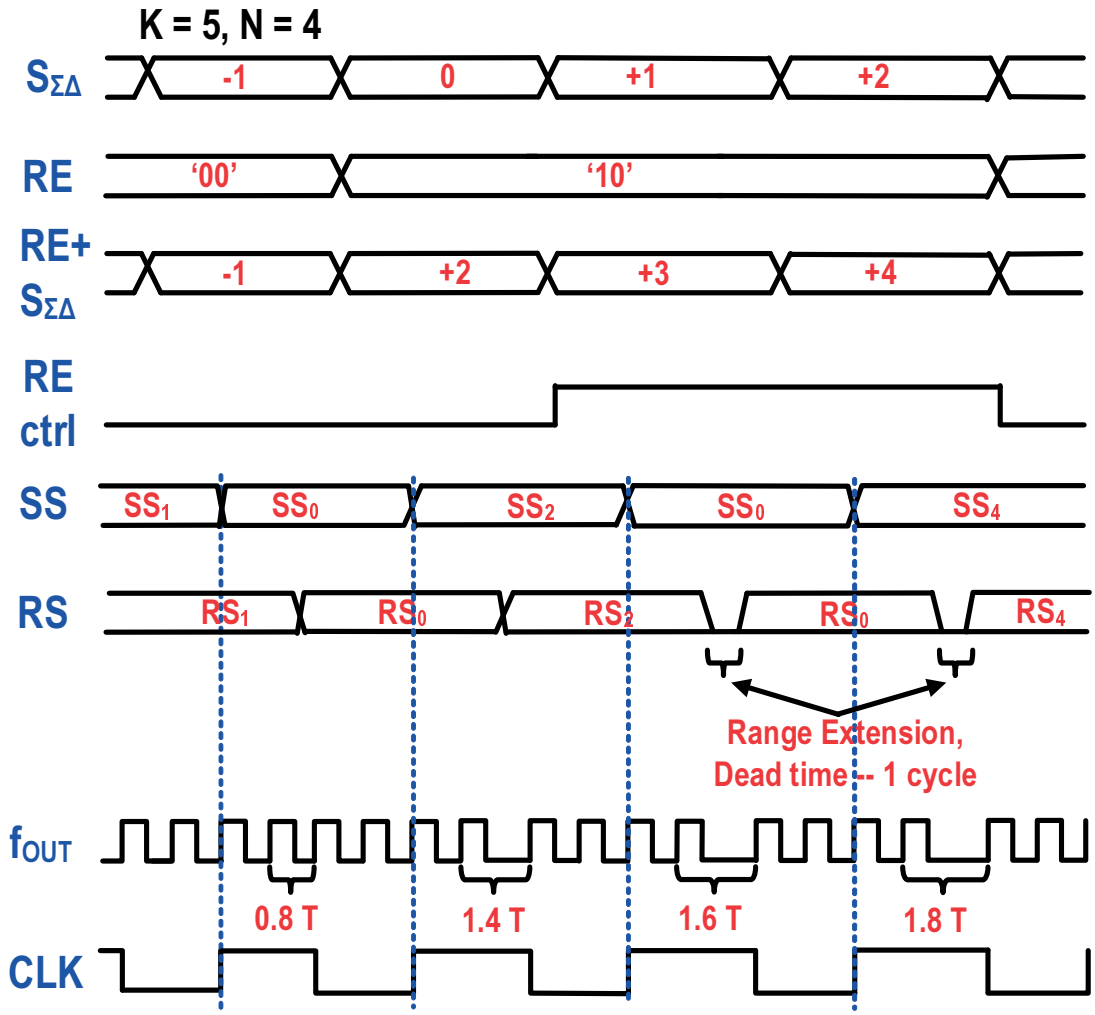
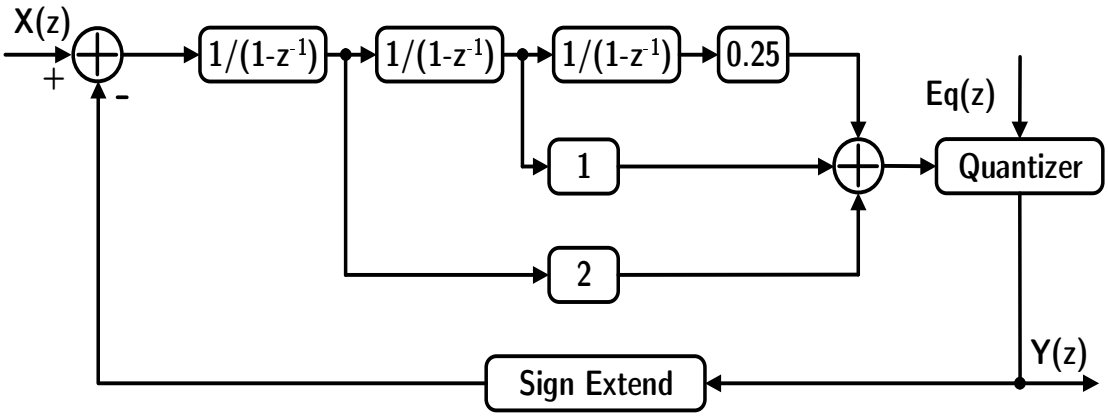



Figure 4.16 – Chronogram after Range Extension

Since the second term in the denominator of the above equation is always greater than or equal to 1, the minimum frequency that can be synthesized with the addition of RE bits is smaller, leading to a larger frequency range. In the aforementioned example, the addition of two RE bits to $S_{\Sigma\Delta}$ reduces the minimum synthesizable frequency from 2.35 GHz to 2.05 GHz.

### 4.2.4 ΣΔ modulator

One of the most important blocks of the PDDDS is the ΣΔ modulator. As mentioned previously, the ΣΔ determines the total noise performance of the system. Recalling from equation 4.8, the bit width of the ΣΔ determines the resolution of the synthesizer. This, in turn affects the noise of the modulated data. In addition, the type of the ΣΔ also impacts the noise shaping and in turn the noise performance of the system.

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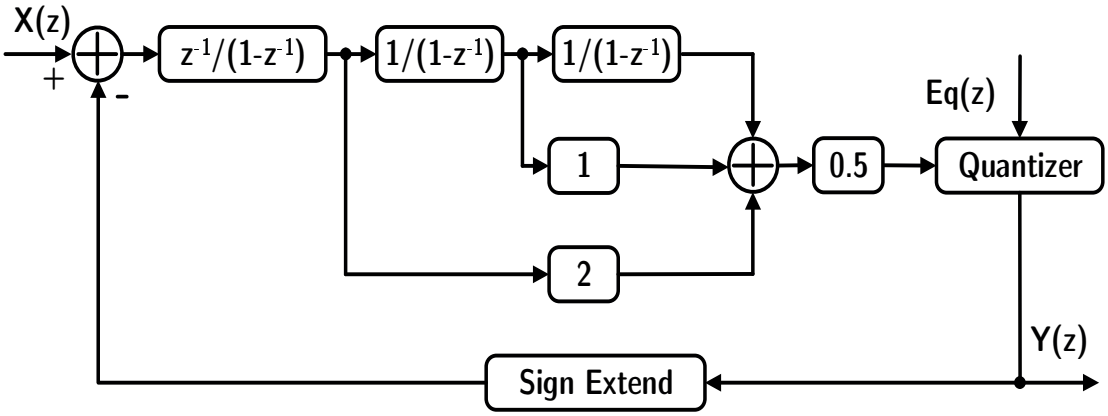


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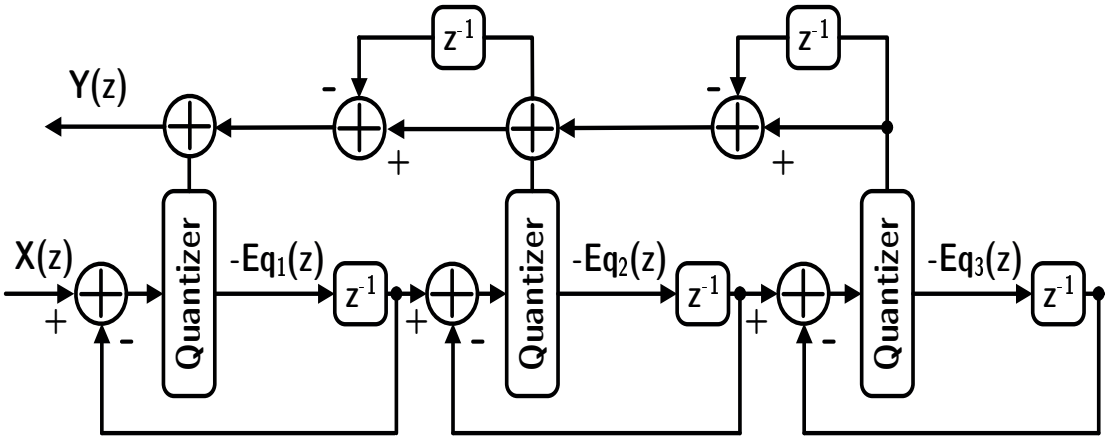


(c)

Figure 4.17 – Different topologies of ΣΔ modulator (a) Single Stage Modulator - I (b) Single Stage Modulator - II (c) MASH modulator

Figure 4.17 gives the block diagrams of three commonly used ΣΔ architectures viz. the Single Stage Modulator - I [9], the Single Stage Modulator - II [10] and the MASH modulator. While the MASH modulator is a feedback architecture, the Single Stage Modulators are feedforward in nature. Each of these modulators is advantageous from the perspective of different performance parameters as explained below.

Out of all these topologies, the MASH modulator has the lowest close in QN while the far away QN is unsuppressed. To illustrate this the Noise Transfer Function (NTF) of the three different topologies are given in the following equations.

$$NTF_{SSM-I} = \frac{\left(1-z^{-1}\right)^3}{4.25-8z^{-1}+5z^{-2}-z^{-3}}. \tag{4.14}$$

$$NTF_{SSM-II} = \frac{\left(1-z^{-1}\right)^3}{1-z^{-1}+0.5z^{-2}}. \tag{4.15}$$

$$NTF_{MASH} = \left(1-z^{-1}\right)^3. \tag{4.16}$$

Figure 4.18 plots the magnitude of the NTF of these three topologies [11] over the various offset frequencies. In the inset figure, a zoom of the close in QN is also given for easy comparison.

Another major factor which is of concern is the stability of the modulator. In general, multi-loop modulators are unconditionally stable as opposed to Single Stage Modulators. Therefore, out of the three topologies presented, the MASH modulator is always stable. In addition, the MASH modulator does not have any scaling factors in its data path unlike the Single Stage Modulators and therefore the MASH modulator has the lowest hardware overhead and also consumes the lowest power. Taking into account all these criteria, the MASH ΣΔ modulator was used in the first prototype of the PDDDS.

The next natural question would be to determine the order of the MASH modulator. The higher the order of the MASH, the lower the near QN but the far away QN is proportionally higher, since the integrated noise power is constant. Since this PDDDS has no inherent filtering mechanism, it is in the best interest of the designers to keep the far offset QN as low as possible which means using a lower order MASH modulator. In addition, due to the non-linear nature of this frequency generation operation (phase combining is essentially non-linear), the noise of the ΣΔ modulator folds back and causes the close-in noise to be dependent on the QN instead of following the reference noise as it would be expected from an injection locked system. The noise folding thus entails careful simulation of the close-in noise to determine the order of the ΣΔ modulator. This is shown in figure 4.19 which is the phase noise simulation of the output for two MASH modulators of order 2 and 3 respectively. It is clear from the figure that the higher order modulators cause a higher in band noise as well as a large excursion of

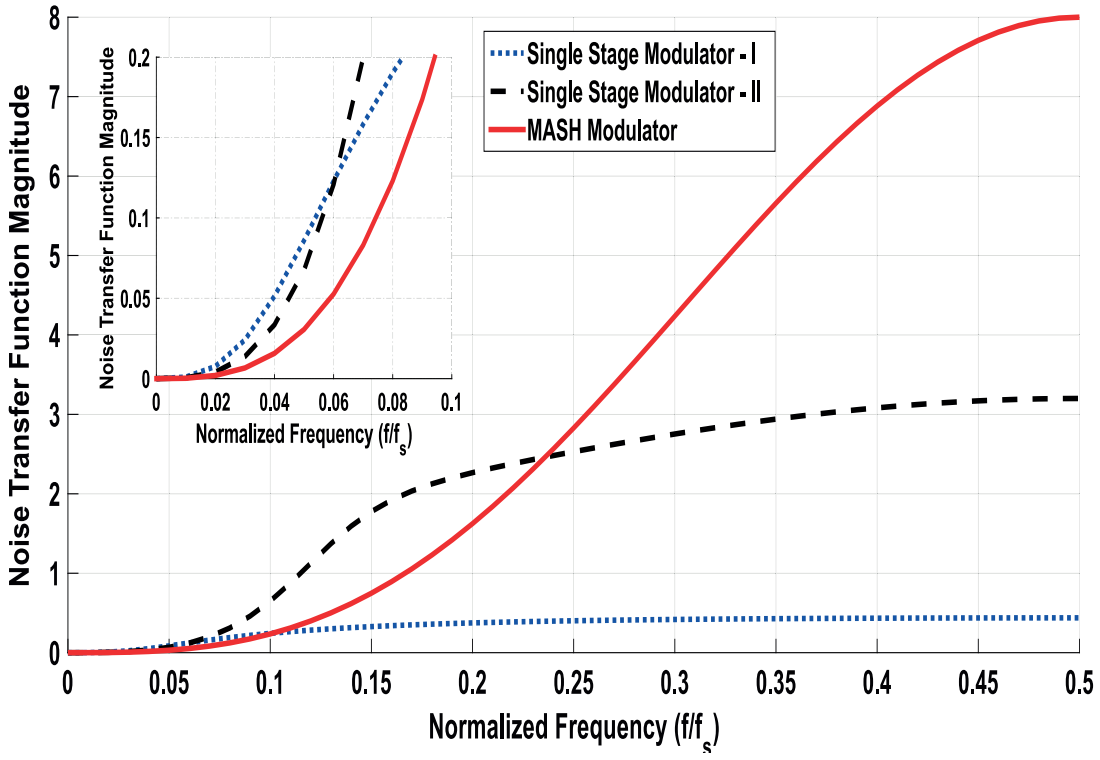


Figure 4.18 – Magnitude of Noise Transfer Function of various ΣΔ modulator architectures

output. Thus from a close-in phase noise perspective, the lowest order of the ΣΔ that ensures spur-free operation would be the correct choice, which is order 2 for a MASH.

In addition to this background, the MASH modulator also has to operate at very high frequencies. For example with $N = 3$ or 4 and the nominal frequency being $f_{REF}$, which is around 2.5 GHz, means that the clock frequency of the MASH will be around 833 or 625 MHz. This operating frequency can momentarily go as high as 1 GHz in the case of the former (750 MHz for the latter) due the maximum momentary frequency of the output signal being around 3 GHz. Moreover, as seen previously, it is of great interest in terms of noise, frequency range etc. to push this clock to even higher frequencies, ideally working at the output frequency itself $f_{OUT}$. All these factors make it very difficult to design a MASH modulator while also minimizing power consumption.

One way reduce to power and hardware of the MASH modulator is to implement what is described as bus-splitting as introduced by Fitzgibbon *et.al.* in [12]. The principle behind this technique is the fact that the contribution of the LSBs to the output spectrum is less than that of the MSBs in a multi-bit noise shaper. Therefore, the LSBs can be quantized by a lesser order ΣΔ and combined with the MSBs following which the sum is quantized again by a higher order modulator as shown in figure 4.20. The procedure of allotting the number of bits to be sent to the lower / higher order modulator is reproduced here from [12] for the sake of completeness.

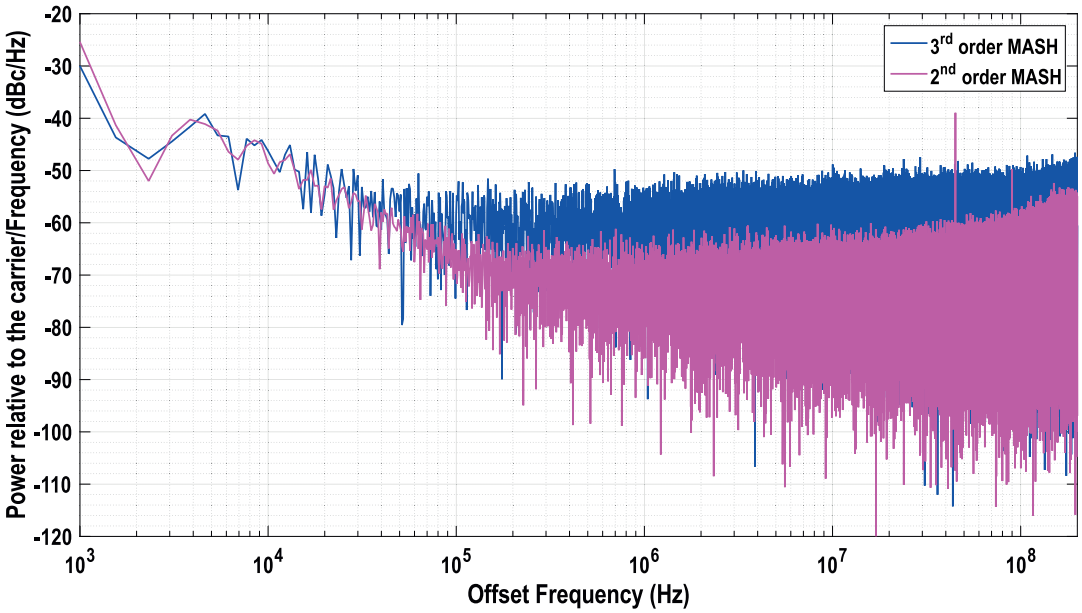


Figure 4.19 – Simulation of the close in phase noise of PDDDS with second and third order MASH

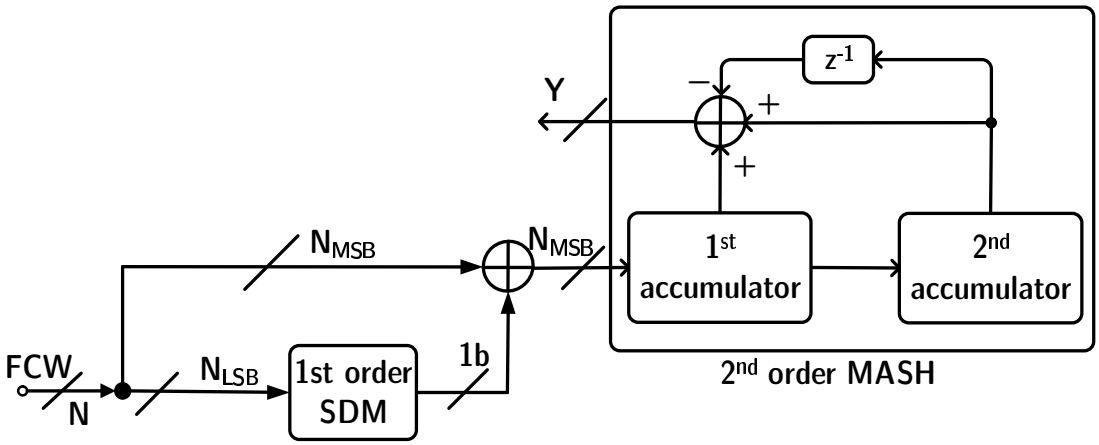


Figure 4.20 – Bus-split MASH ΣΔ modulator

Given an $N$ bit input $X_{in}$ to the MASH modulator, the first $N_{LSB}$ bits are quantized by a first order modulator whose output is summed with the $N_{MSB}$ bits and passed through a second order modulator. The instantaneous output of the MASH modulator $Y$ can be expressed as a sum of the input $X_{in}$ scaled by $2^G$ ($G$ being the bit width of the modulator) and the Quantization noise arising from the first and second order modulators scaled appropriately. Writing this relationship in the z-domain gives

$$Y(z) = \frac{X_{in}(z)}{2^N} + \left(1 - z^{-1}\right) \frac{Eq1(z)}{2^{N_{LSB}} 2^{N_{MSB}}} + \left(1 - z^{-1}\right)^3 \frac{Eq2(z)}{2^{N_{MSB}}}, \tag{4.17}$$

where $Eq1(z)$ and $Eq2(z)$ are the z-transforms of the QN of the first and the second order modulators respectively. The idea is to mask the noise of the first order below that of the second order modulator by an appropriate choice of $N_{MSB}$ and $N_{LSB}$. At this juncture, it is noted that the spectrum of the first order modulator is made up of spurs at multiples of $f_{CLK}/2^{N_{LSB}}$. The noise spectrum of the second order modulator has a 20 dB/dec slope. So, in order to achieve a spur free noise shaping, it is imperative to ensure that the first spur of the first order modulator remains below the second order modulator noise which will ensure that all the other spurs remain hidden, given the 20 dB/decade slope (increasing nature) of the second order modulator noise.

The cycle lengths of the first and the second order modulators are $2^{N_{LSB}}$ and $2^{N}$ respectively. For a constant input to the modulator without dithering, the noise power spectra of the first and the second order MASH modulator is given by

$$S_1(f) = \frac{1}{12L_{s1}} \frac{1}{(2^{N_{MSB}})^2} \left(1 - z^{-1}\right)^2, \tag{4.18}$$

$$S_2(f) = \frac{1}{12L_{s2}} \left(1 - z^{-1}\right)^2 \Big|^2. \tag{4.19}$$

Then the condition for the spur free bus splitting is given as

$$S_1 < S_2 @ f = f_{CLK}/2^{N_{LSB}}. \tag{4.20}$$

Since

$$\left|\left(1 - z^{-1}\right)\right| = 2sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s} \qquad \text{for} \quad f << f_s, \tag{4.21}$$

the noise power spectra can be rewritten as

$$S_1(f[k]) = \frac{4}{12 \cdot 2^{N_{LSB}}} \frac{1}{(2^{N_{MSB}})^2} \left(\frac{\pi f}{f_s}\right)^2, \tag{4.22}$$

$$S_2(f[k]) = \frac{16}{12 \cdot 2^{N_{LSB}+N_{MSB}}} \left(\frac{\pi f}{f_s}\right)^4. \tag{4.23}$$

To satisfy the condition given in equation 4.20, the requirements on the bit width of the first and second order modulators is given by

$$2N - 3N_{MSB} < 5.3. \tag{4.24}$$

If dither component is added, the equations become slightly different. Due to the presence of dither, the output is essentially spur-free. Therefore, the equations have to be solved at the

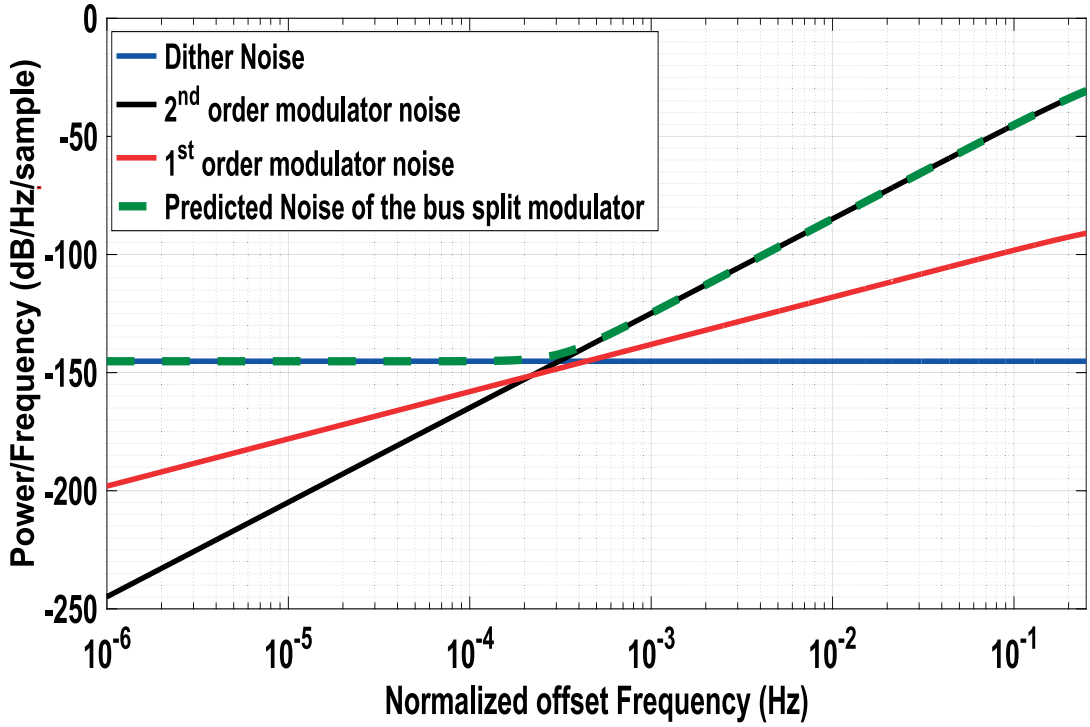


Figure 4.21 – Masking (dashed), second order, first order and dither noise spectrum

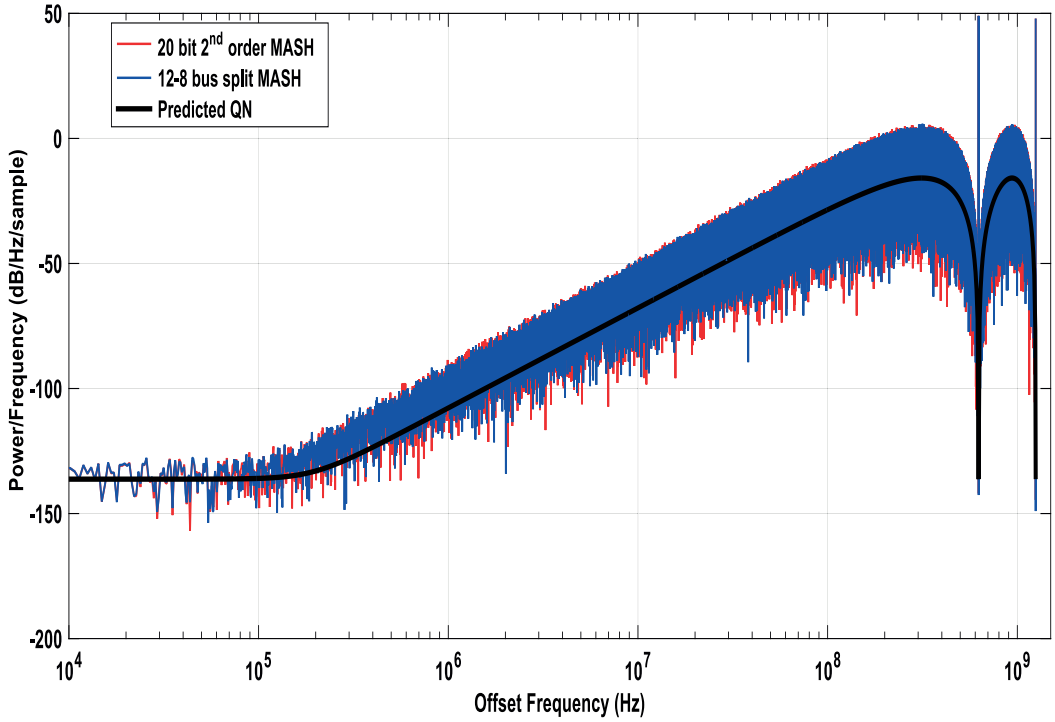


Figure 4.22 – Noise comparison between 20 bit MASH modulator and the bus split modulator

frequency where the ΣΔ noise takes over from the dither noise floor. If a zero order dither is employed, this noise floor is given by

$$\mathscr{L}_{nf}(f) = \frac{1}{12 \cdot \left(2^N\right)^2}. \tag{4.25}$$

The noise floor is illustrated in figure 4.21 which also shows the predicted first and second order modulator noise spectra along with that of the bus split MASH. This noise floor is the dominant component of the QN till the frequency which is derived by equating equations 4.25 and 4.23 as

$$f = \frac{f_s}{2\pi \cdot 2^{N/2}}. \tag{4.26}$$

At this frequency, equating the noise from the first and the second order modulator gives the condition on the bus splitting as

$$N_{MSB} > \frac{N}{2}. \tag{4.27}$$

For example, to design a 20-bit second order MASH, taking into account both the cases of with and without dither, the bus splitting technique leads to $N_{MSB} = 12$ and $N_{LSB} = 8$. The output noise power of this modulator is shown in figure 4.22 which shows that the noise of the bus split modulator and the normal 20 bit modulator are virtually identical and closely follow the predicted noise. Coming to the hardware perspective, for this 20 bit modulator, the use of bus splitting helps to reduce the number of full adders and flip-flops required by 20%, thus helping to reduce the power consumption.

### 4.2.5 Hybrid requantizers for spurious level reduction

One of the main issues with the use of the SDM are the spurs which appear due to the non-linearity of the frequency synthesizer [13]. This is similar to a PLL, where the nonlinearity of the charge pump combined with the pseudo-random nature of the traditional ΣΔ (MASH) output results in near-integer spurs. The appearance of these spurs can be verified by plotting the PSD of the higher powers of the MASH output as shown in figure 4.23. These spurs may be particularly annoying in the case of the PDDDS since the synthesizer lacks the inherent filtering mechanism of the PLL. These spurs may fall in the cellular bands and violate the spectral requirements. In order to mitigate these spurs, Shaped Requantizers (SRQ) have been designed in the literature [14]. These ΣΔ modulators trade-off spurs for in-band noise and hence could be used in applications where the presence of the spurs is the major mitigating factor that deters the use of PDDDS. The major problem with the SRQ is the high power consumption and hardware count at the clock frequencies that the ΣΔ of the PDDDS is supposed to operate. Hence, in order to reduce the same, a Hybrid Requantizer (HRQ) based on the combination of the traditional MASH and the SRQ has been developed. Before going

into the evolution of the HRQ, a rudimentary background of the SRQ is provided herein for the benefit of the readers.

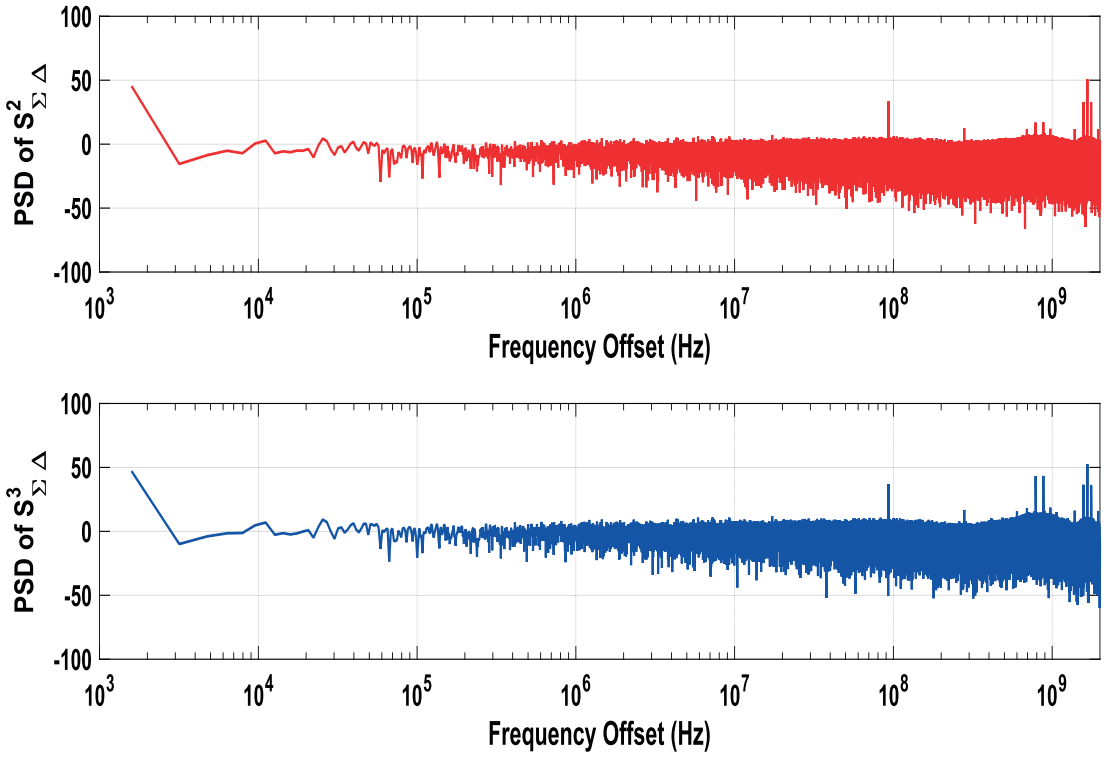


Figure 4.23 – PSD of the output of the ΣΔ raised to higher powers

The Shaped Requantizer is a class of DC-free quantizer which quantizes the Frequency Control Word (FCW). The SRQ consists of a cascade of $K$ 1-bit quantizers whose block diagram is shown in figure 4.24. The output of each of these quantization blocks is based on the output of its previous block and a random number generator. The quantizer block inspects its input and a random number is added to it based on certain conditions to be described shortly and the resultant is passed on to the divide by 2 sub-block which gives the output. The mean of the random number sequence that is added to the input of the SRQ block needs to be zero. Thus, the output of each SRQ block can be written as

$$x_{d+1}[n] = \frac{1}{2}(x_d[n] + s_d[n]), \tag{4.28}$$

where $s_d[n]$ is generated based on the parity of the input ($o_d[n]$), the running sum of $s_d[n]$ and the output from a random number generator. The combinational logic (given in figure 4.25) makes sure that $s_d[n]$ has the same parity of the input $x_d[n]$. This makes sure that the sum of the input and $s_d[n]$ is divisible by 2 i.e. the output has one bit less than the input [15].

The running sum of $s_d[n]$ is denoted by $t_d[n]$ written mathematically as

$$t_d[n] = \sum_{k=0}^{n} s_d[k]. \tag{4.29}$$

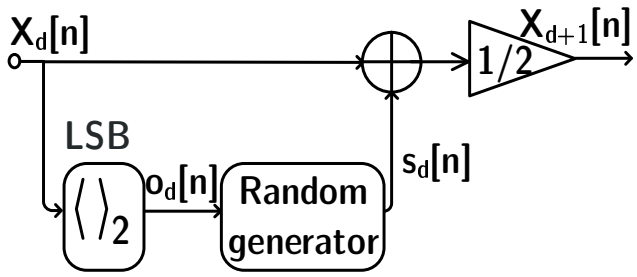


Figure 4.24 – Block Diagram of the individual Shaped requantizer unit

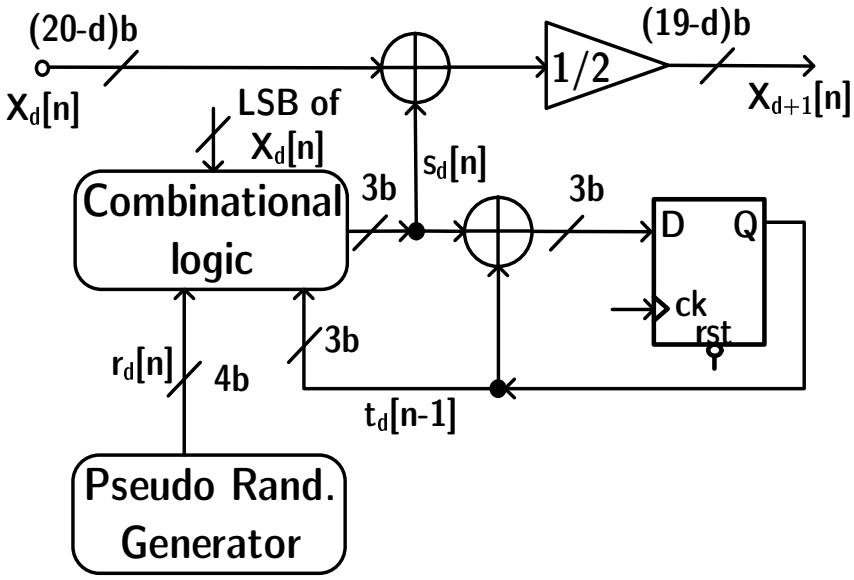


Figure 4.25 – Schematic of the SRQ unit

Based on the span of the random number sequence that is used to determine $s_d[n]$, which in turn means the upper bound on the values that $|t_d[n]|$ (this upper bound is denoted by $N_t$) can take, the output sequence of the SRQ presents immunity up to certain orders of non-linearity and subsequently have less power in the spurious tones. The determination of $s_d[n]$ based on $r_d[n]$, $o_d[n]$ and $t_d[n-1]$ for $N_t = 1$ and $N_t = 2$ is given in tables 4.1 and 4.2 respectively. The first is immune to spurs upto order 1 nonlinearity while the latter is immune to spurious tones up to a nonlinearity of order 3. This can be verified from the simulations of the figure 4.29 which show the $\Sigma\Delta$ output raised to the power 3 as well as the PSD of the $s_d[n]$ raised to power 3 and the running sum of the same raised to the power 5 [16]. At this juncture, it is important to note that the random number streams used in each SRQ block should be uncorrelated from

| $o_d[n]=0$ | | | | $o_d[n]=1$ | | |
|---|---|---|---|---|---|---|
| $t_d[n-1]$ | $r_d[n]$ | $s_d[n]$ | | $t_d[n-1]$ | $r_d[n]$ | $s_d[n]$ |
| 1 | -1 or 0 | 0 | | 1 | -1 or 0 | -1 |
| 0 | -1 or 0 | 0 | | 0 | -1 | -1 |
| | | | | 0 | 0 | 1 |
| -1 | -1 or 0 | 0 | | -1 | -1 or 0 | 1 |

Table 4.1 – $s_d[n]$ Combinatorial decision table for $N_t$ = 1 and $r_d[n]$ = -1,0

| $o_d[n]=0$ | | | | $o_d[n]=1$ | | |
|---|---|---|---|---|---|---|
| $t_d[n-1]$ | $r_d[n]$ | $s_d[n]$ | | $t_d[n-1]$ | $r_d[n]$ | $s_d[n]$ |
| 2 | ≥ 0 and ≤ 3 | 0 | | 2 | ≤ -1 or ≥ 4 | -1 |
| 2 | ≤ -1 or ≥ 4 | -2 | | 2 | ≥ 0 and ≤ 3 | -3 |
| 1 | ≤ -1 or ≥ 6 | 0 | | 1 | ≥ 1 and ≤ 3 | 1 |
| 1 | ≥ 0 and ≤ 5 | -2 | | 1 | ≤ -1 or ≥ 4 | -1 |
| | | | | 1 | 0 | -3 |
| 0 | 0 or 1 | 2 | | 0 | ≥ 0 | 1 |
| 0 | ≤ -1 or ≥ 4 | 0 | | 0 | ≤ -1 | -1 |
| 0 | 2 or 3 | -2 | | | | |
| -1 | ≤ -1 or ≥ 6 | 0 | | -1 | ≥ 1 and ≤ 3 | -1 |
| -1 | ≥ 0 and ≤ 5 | 2 | | -1 | ≤ -1 or ≥ 4 | 1 |
| | | | | -1 | 0 | 3 |
| -2 | ≥ 0 and ≤ 3 | 0 | | -2 | ≤ -1 or ≥ 4 | 1 |
| -2 | ≤ -1 or ≥ 4 | 2 | | -2 | ≥ 0 and ≤ 3 | 3 |

Table 4.2 – $s_d[n]$ Combinatorial decision table for $N_t$ = 2 and $r_d[n]$ = -8,...,7

each other lest it results in spurs, as seen in figure 4.27. Thus, to summarize, since only higher order non-linearities contribute to spurs, the spurious levels of the output of the transmitter can be expected to be lower with an SRQ than when a MASH modulator is used.

The QN of this SRQ is essentially first order in nature, rising with a slope of 20 dB/dec. Compared with the MASH, the noise of the SRQ is higher as the total integrated noise in both cases are the same and the spurious tones in the case of the former are traded off for the latter. As mentioned previously, the problem with the SRQ is the high hardware count and consequently the higher power consumption. For instance a 20 bit SRQ would require 245 1-bit adders, 120 flip-flops and 1105 gates. By contrast, a simple third order MASH modulator would require just 60 1-bit adders and 60 flip-flops. At low reference frequencies, the power consumption of the SRQ may be negligible compared to the whole transmitter and hence this large hardware and subsequently power overhead can be tolerated. But in the case of a PDDDS with the ΣΔ operating at hundreds of MHz, the power consumption of the ΣΔ becomes dominant.

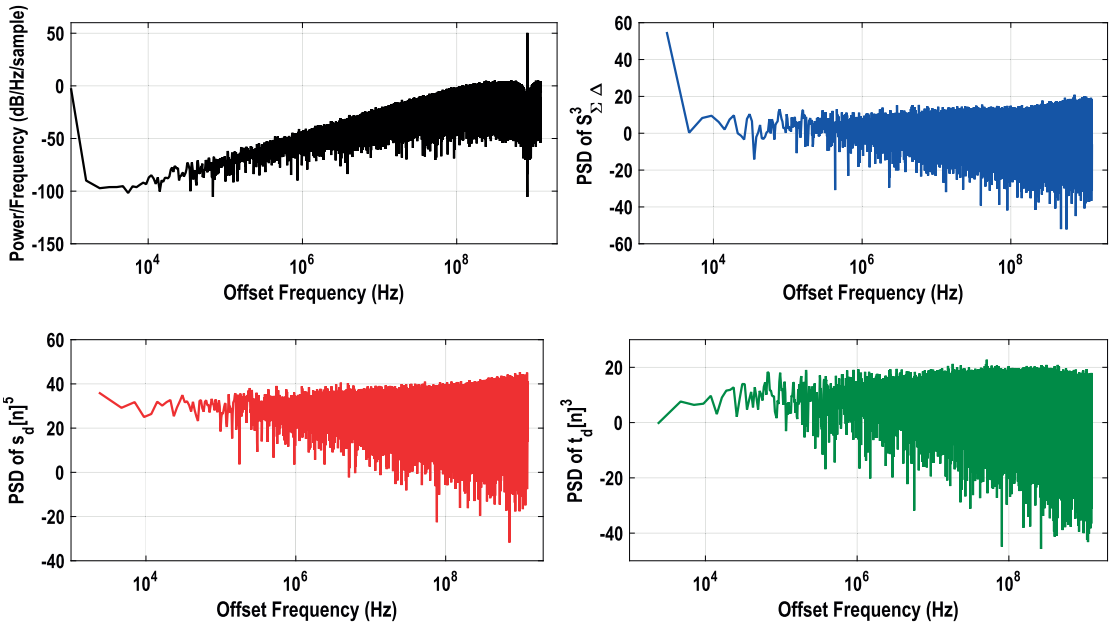


Figure 4.26 – PSD of various HRQ signals a) output ($S_{\Sigma\Delta}$ (top left) b) HRQ - $S^3_{\Sigma\Delta}$ (top right) c) HRQ - $s_d[n]^5$ (bottom left) d) HRQ - $t_d[n]^3$ (bottom right)

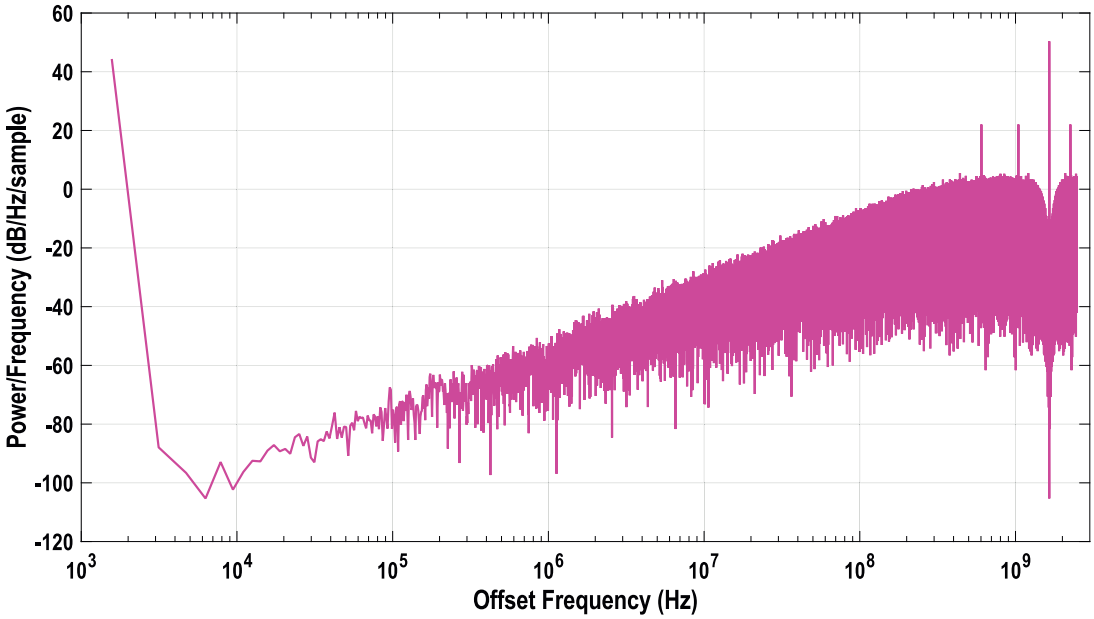


Figure 4.27 – PSD of the SRQ with correlated random number generators

Furthermore, at very high frequencies, it may not be possible to synthesize the ΣΔ if the circuit is hardware intensive like the SRQ. Therefore, there is a need to find a solution which preserves not only the noise shaping of the SRQ but also greatly reduces the hardware.

To this end, a comparison of the PSD of the outputs of the MASH and the SRQ is shown in figure 4.28. The QN of the SRQ is substantially higher than that of the MASH and therefore it is possible to perform bus splitting by hybridizing the less hardware intensive MASH with the SRQ. Thus, the $M$ LSBs of the input $N$-bit FCW are quantized using a conventional MASH modulator and the results are summed to the remaining $N-M$ MSBs and passed through a shaped requantizer. The noise spectrum of this resultant Hybrid Requantizer (HRQ) is identical to that of the SRQ. For example, a 20 bit FCW can be split into 16 LSBs quantized by the MASH and the remaining MSBs quantized by the SRQ. Now the question arises about the order of the MASH used to quantize the LSBs. For this purpose, different 20 bit HRQs have been synthesized with different orders of MASH modulator at 100 MHz frequency and the results shown in the table of figure 4.29. It can be seen from the table that the use of a second order MASH in the HRQ consumes the least power and occupies the least area. The block diagram of the resulting HRQ is shown in figure 4.30. In addition, to reduce the hardware due to uncorrelated random number generators, it is noted that since a LFSR involves a recursive XOR function, it is possible to predict the future outputs. By combining bits from the different registers of the LFSR by pre-prediction, sufficiently uncorrelated random number sequences can be generated from a single LFSR, thereby greatly reducing the hardware.

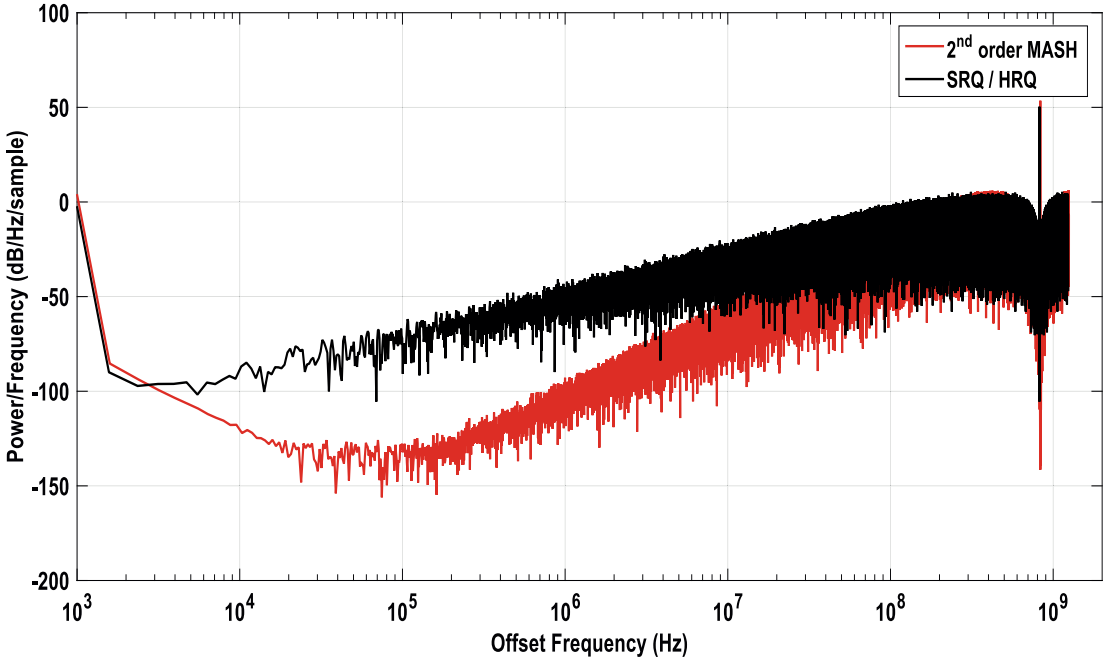


Figure 4.28 – Comparison PSD of the output of a MASH and a SRQ

## 4.3 Transmitter Design

With the PDDDS described in the previous sections, a transmitter prototype whose block diagram is given in figure 4.32 is developed. The PDDDS used in this TX prototype consists

| | Area ($\mu m^2$) in 65 nm CMOS | Power ($\mu W$) @100 MHz | No. of Gates | No. of FFs | No. of 1-b adders |
|---|---|---|---|---|---|
| Simple SRQ | N/A | N/A | 1105 | 120 | 245 |
| 1st order MASH+SRQ | 3770 | 345 | 408 | 65 | 74 |
| 2nd order MASH+SRQ | 2041 | 255.4 | 188 | 62 | 40 |
| 3rd order MASH+SRQ | 2088 | 329.2 | 135 | 76 | 48 |

Figure 4.29 – Comparison of a 20 bit HRQ implemented with various orders of MASH

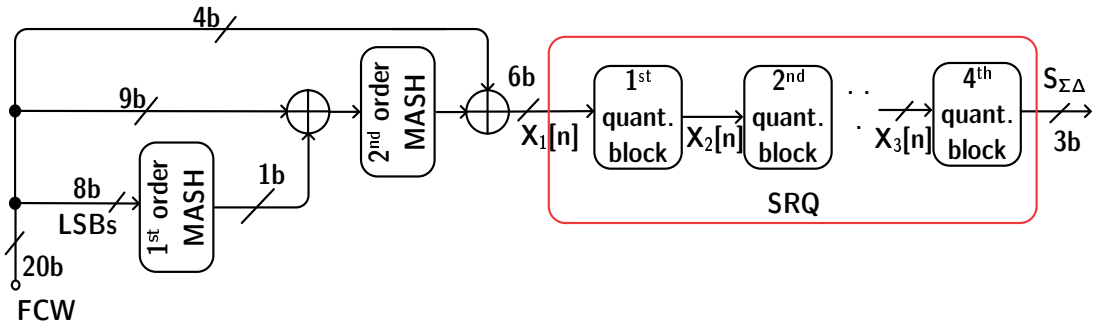


Figure 4.30 – Block Diagram of the Hybrid Requantizer

of a 5 stage ring oscillator which injection locks a 10-stage pseudo differential ring oscillator, thus providing $K = 10$. The digital baseband is clocked by the divided versions of the FBAR DCO signal. The output of a multi-modulus divider with moduli of 6 or 8 followed by two divide by 2 circuits are multiplexed to provide the desired clocks.

Since the output of the frequency synthesizer is driven by logic gates, the voltage swing is rail to rail and hence simple inverters can be used as pre-power amplifiers. To this end, a series of inverters of increasing sizes drive a switching PA [17]. Moreover, the PA is implemented with multiple slices (16 in this case, refer figure 4.31) to enable output power control. Care should be taken in designing this PA since the instantaneous duty cycle of the synthesizer output varies greatly. For instantaneous frequencies greater than $f_{ref}$, the duty cycle of the synthesizer output is below 50 % and hence the PA transistor spends more time in the off state which may result in a drop in output power. Accounting for this in the design process is therefore mandatory, the result of which is a slightly increased power consumption than if the PA was driven by a signal with nearly 50 % duty cycle.

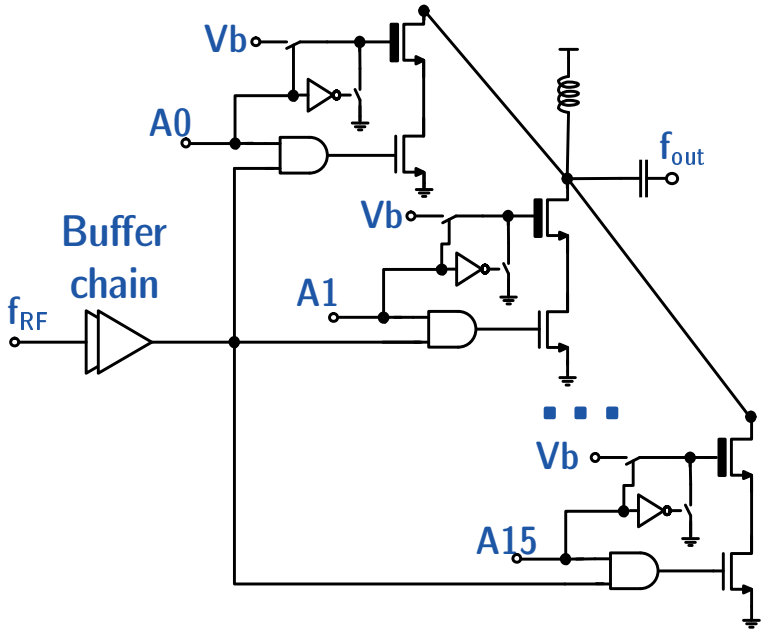


Figure 4.31 – Schematic of the sliced Power Amplifier

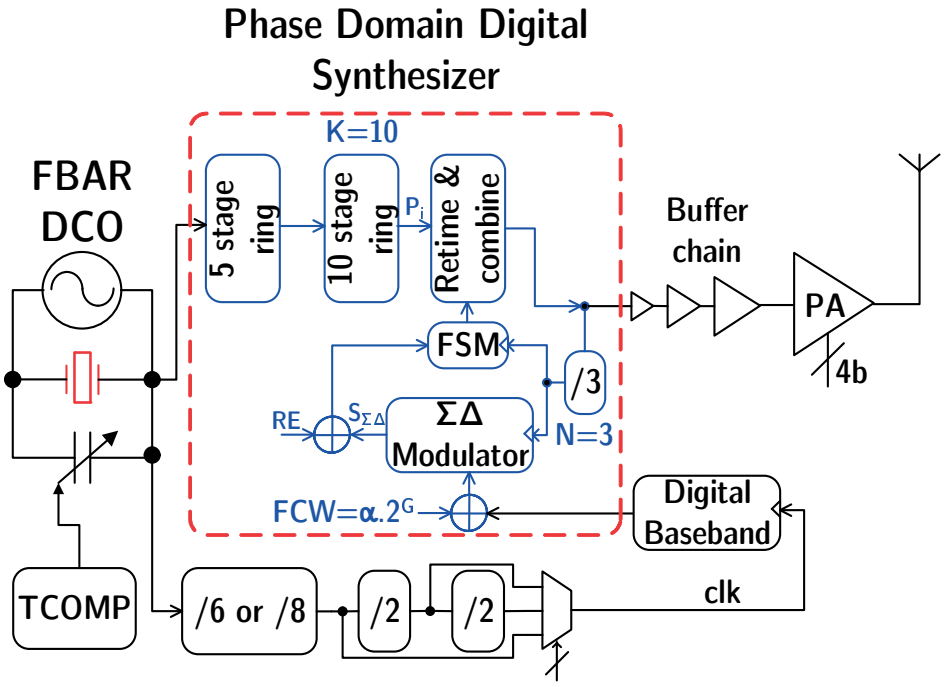


Figure 4.32 – Schematic of the PDDDS based TX

## 4.4 Measurement Results

This transmitter has been integrated in a 65 nm CMOS process (chip photograph shown in Fig.4.33). Thanks to the fully digital architecture of the PDDDS, the synthesizer occupies

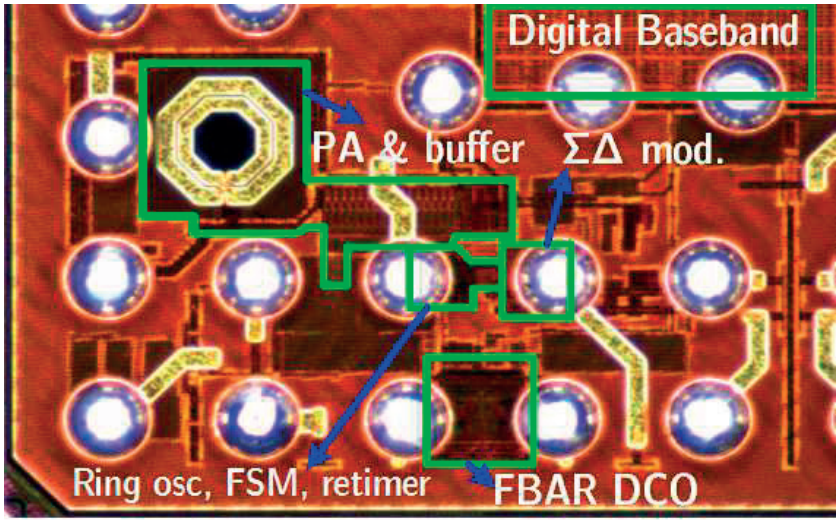


Figure 4.33 – Chip microphotograph

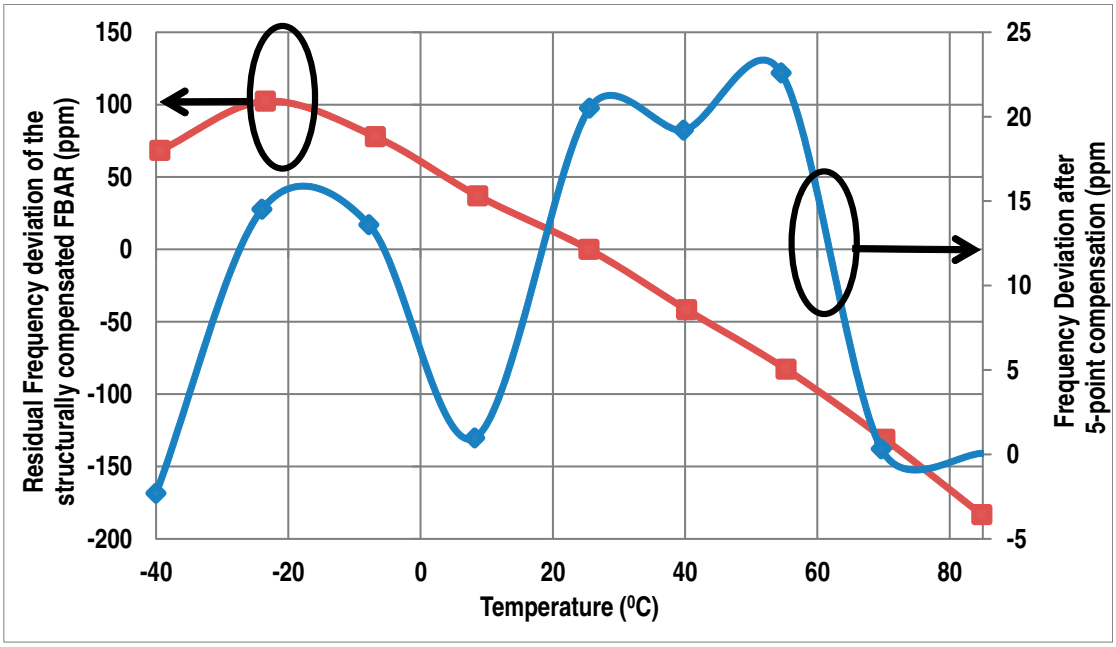


Figure 4.34 – Frequency variation of an FBAR before and after a 5-point temperature compensation scheme

an area of only 0.035 $mm^2$. The FBAR that was chosen had a resonance frequency of 2.47 GHz ($f_{LO}$) and a frequency-sensitivity of 280 ppm over the temperature range −40 to 85°C. To improve the frequency stability, a 5-point open-loop calibration scheme similar to the 3-point scheme described in the previous chapter was used. This process of temperature compensation reduced the large FBAR deviation to 25 ppm over the entire range as shown in Fig.4.34.

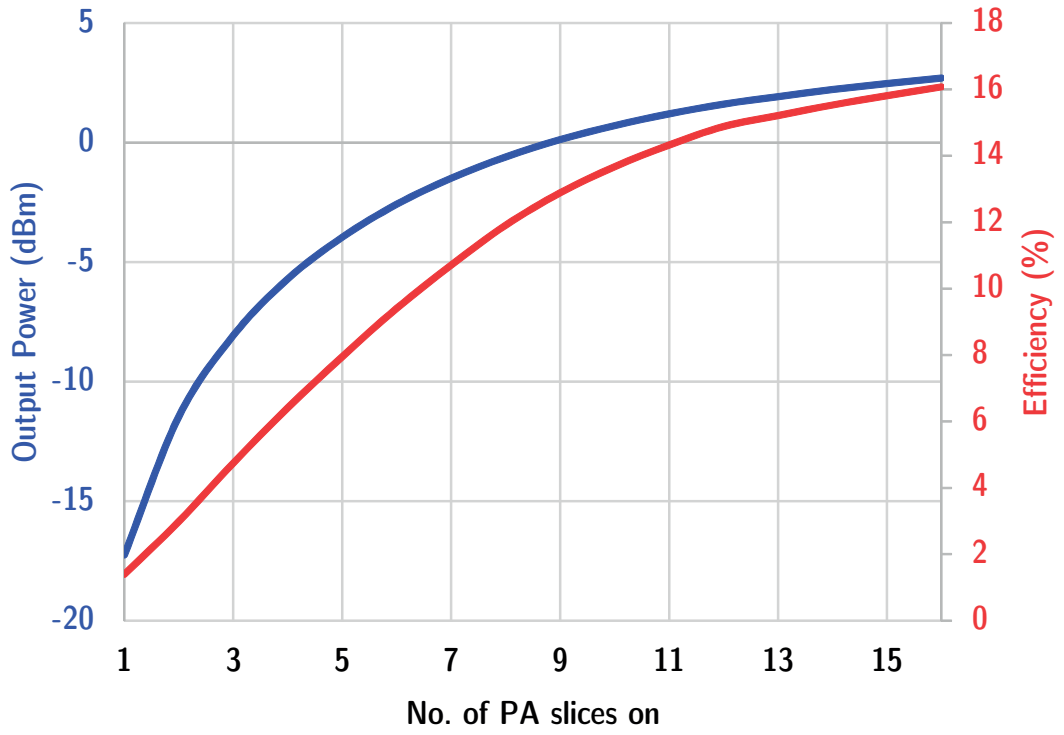


Figure 4.35 – Variation of the output power and the efficiency of the PA with the number of slices ON

The transmitter can output a maximum of 3 dBm output power at a power supply of 1.08 V. The pre-amplifier buffer chain can operate at a lower supply voltage of 0.9 V to reduce power consumption. The biasing voltage of the cascode $V_b$ is held at 0.9 V. The variation of the output power as well as the total drain efficiency of the PA including the buffer chain with the number of the PA slices turned ON is shown in Fig. 4.35. The peak efficiency is around 16 % which is slightly less than the SOTA [18] due the aforementioned issue of duty cycle variation.

For the purpose of comparison, the frequency synthesizer was integrated with a $2^{nd}$ order MASH and HRQ with both $N_t$ = 1 and 2. The wideband spectrum of the TX is shown in Fig. 4.36. The measurement was performed with a resolution bandwidth of 100 kHz. As expected, the in band noise of the MASH is better than that of both versions of the HRQ. The spurious tones on the other hand are the highest in the case of the MASH with the HRQ with $N_t = 1$ performing only slightly better. On the other hand, the HRQ with $N_t = 2$ is much superior with the spurs being significantly lower. While the largest spur in the case of a MASH is -35 dB below the carrier, for the HRQ the spur level is -46 dBc. The close in phase noise spectrum of the FBAR DCO standalone, transmitter with the MASH and HRQ is shown in Fig. 4.37. The DCO phase noise is around -128 dBc/Hz at 1 MHz offset. While the close in phase noise of the TX is expected to follow the DCO phase noise due to injection locking, the non-linearity of the frequency generation process folds the SDM noise leading to an increased in-band noise.

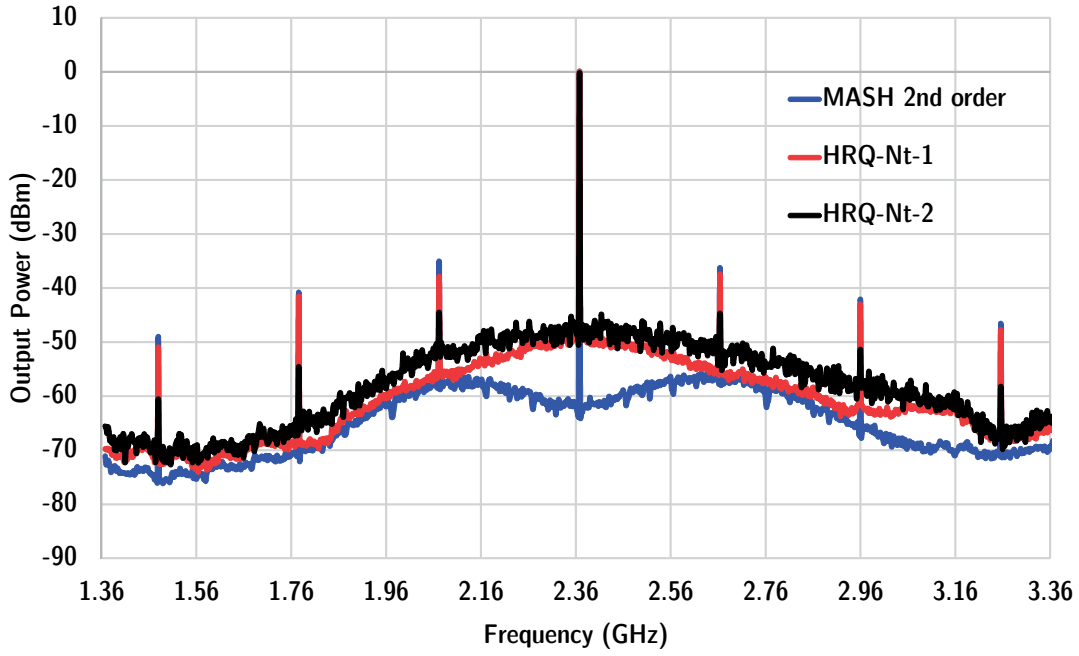


Figure 4.36 – Wideband output spectrum of the TX

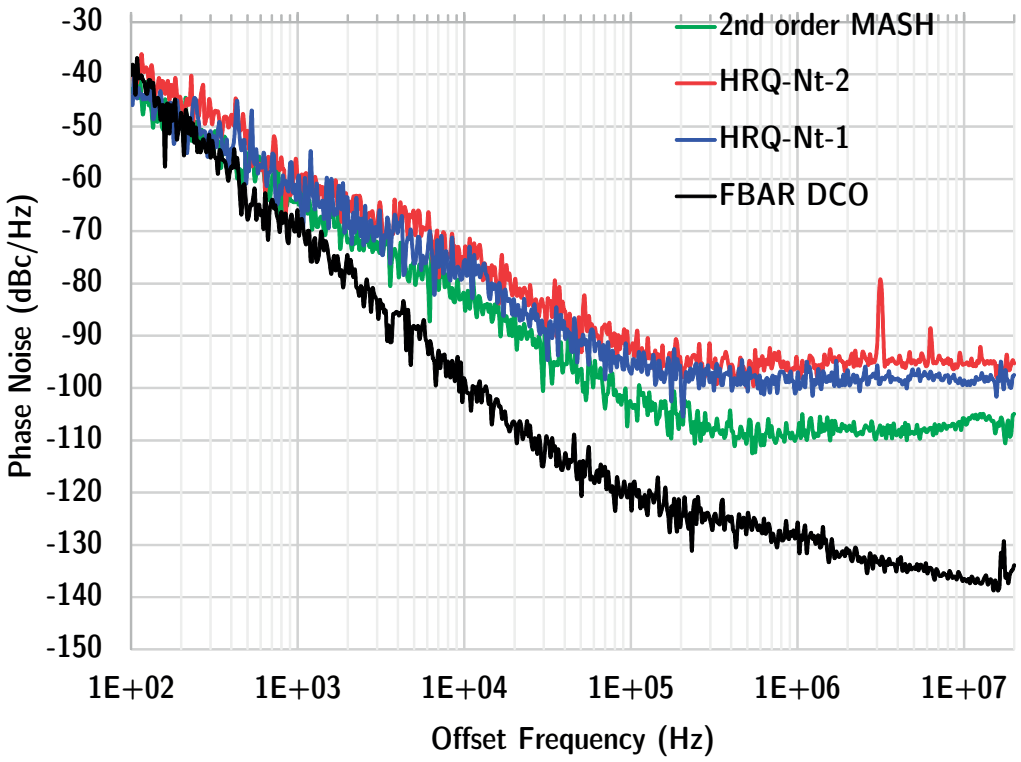


Figure 4.37 – Phase noise of the TX

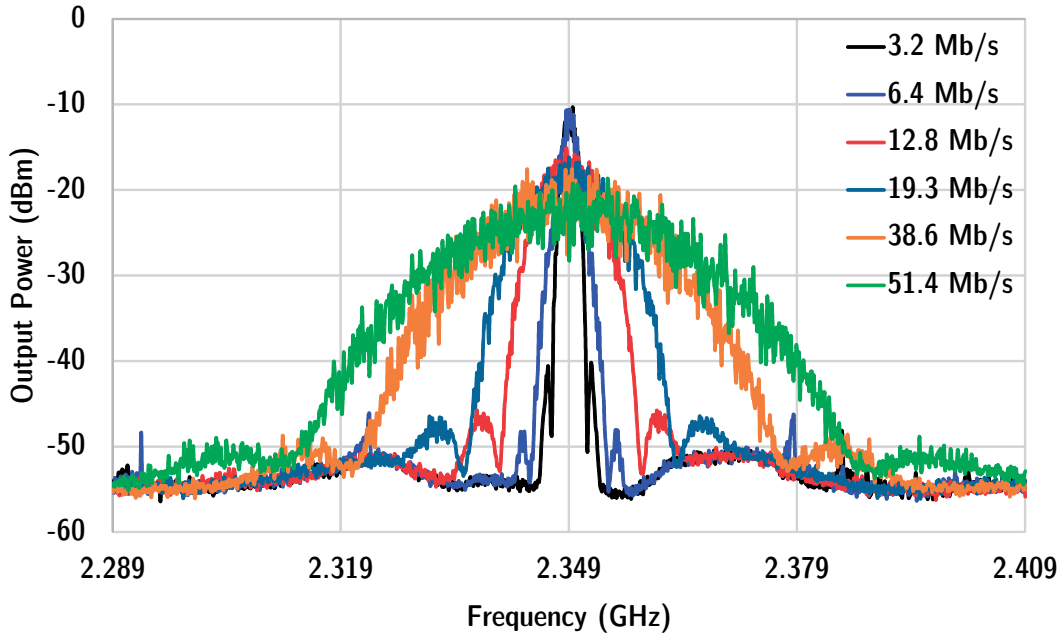


Figure 4.38 – Output spectrum of the Transmitter at various data rates

The fact that this indeed is the case is borne out by the fact that TX employing the HRQ shows higher phase noise due to the fact that the HRQ has a higher QN. The phase noise levels at 1 MHz offset are -110 dBc/Hz, -97 dBc/Hz and -100 dBc/Hz for the MASH, HRQ $N_t = 1$ and HRQ $N_t = 2$ respectively. To summarize the above measurement results, the HRQ provides the designer another degree of freedom to deal with the spurious tones in the synthesizer.

The transmitter supports FSK data rates of upto 51.4 Mb/s with modulation index of 0.5 which is the highest achieved so far for such a system. This is evinced by the modulated spectrum shown in Fig. 4.38 as well as the eye diagrams for various data rates shown in Fig. 4.39. This data rate of the TX depends on the clock frequency of the DBB which subsequently affects the power consumption. This is shown in the plot of Fig. 4.40 which depicts the DBB power versus increasing data rate. An almost exponential increase in the power consumption can be seen with increasing data rates. The DBB power at 51.4 Mb/s is 5.47 mW. The power consumption of the rest of the circuit blocks in given in Table 4.3. The overall power consumption of the TX at 6.5 Mb/s data rate and 0 dBm output power is 15.4 mW.

As mentioned previously, the FBAR aids the fast startup of this transmitter as shown in the plot of frequency and current profile vs time which was measured with E5052B signal source analyzer along with the current profile in figure 4.41. As shown, the latency of this TX is just 1.5 µs and the $T_{TO}$ is just 1 µs. To change channels, this TX needs just 5 µs (SPI limited, can be improved by dedicated on chip circuits) which is a great advantage for multi-hop networks. A comparison of this transmitter with other State of the Art Transmitters in the literature in

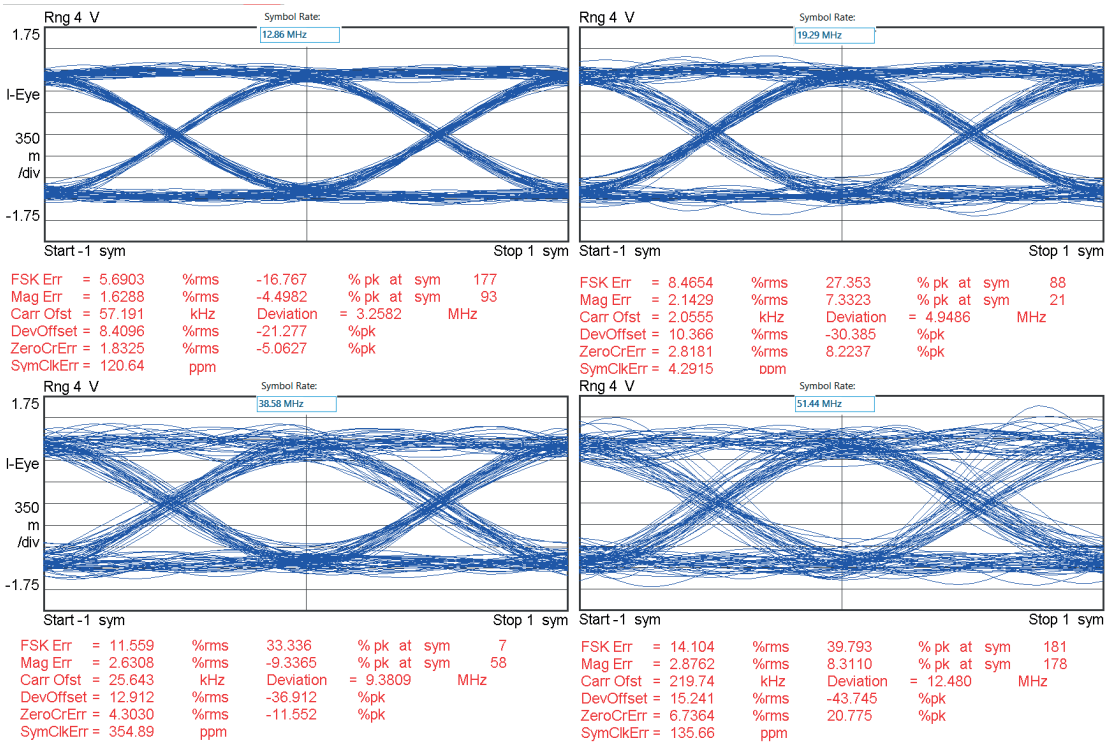


Figure 4.39 – Eye diagrams at various data rates: 12.8 Mb/s (top left), 19.3 Mb/s (top right), 38.6 Mb/s (bottom left), 51.4 Mb/s (bottom right)

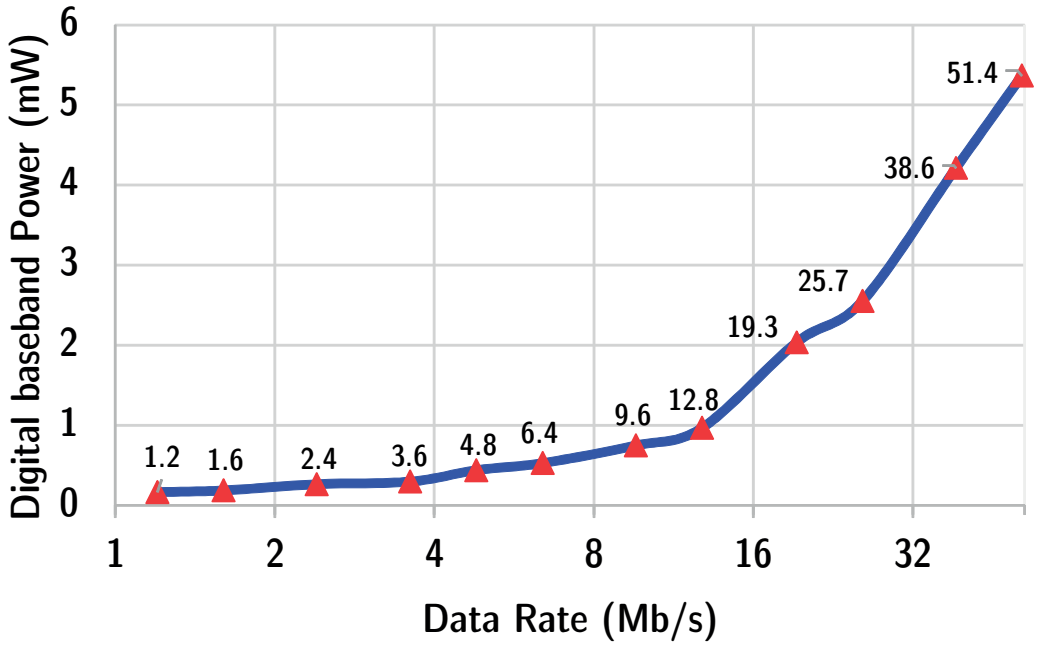


Figure 4.40 – Power consumption of the DBB with increasing data rates

Table 4.3 – Power consumption of the TX at 0 dBm output power

| Transmitter block | Power consumption |
|---|---|
| FBAR DCO and clock dividers | 638 µW (/8) |
| | 858 µW (/6) |
| ΣΔ modulator | 4.257 mW |
| Phase Domain Digital Synthesizer | 2.13 mW |
| Buffer chain | 1.29 mW |
| Power Amplifier | 6.7 mW |

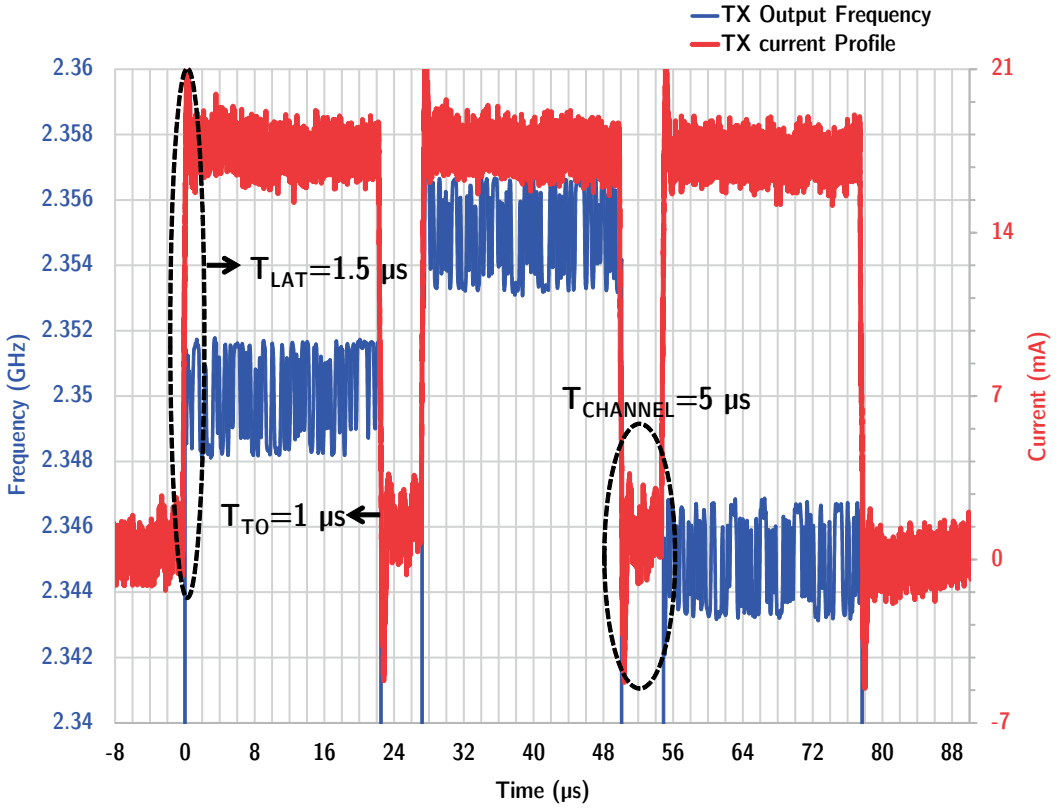


Figure 4.41 – Current profile and output frequency of the TX vs Time

terms of various performance parameters is given in Table 4.4.

### 4.4.1 Duty cycling Energy Efficiency

As described in the introduction, the total energy overhead is determined by the wake up time of the transmitter $T_{wu}$, the power dissipated during this wake up phase $P_{wu}$, the amount of

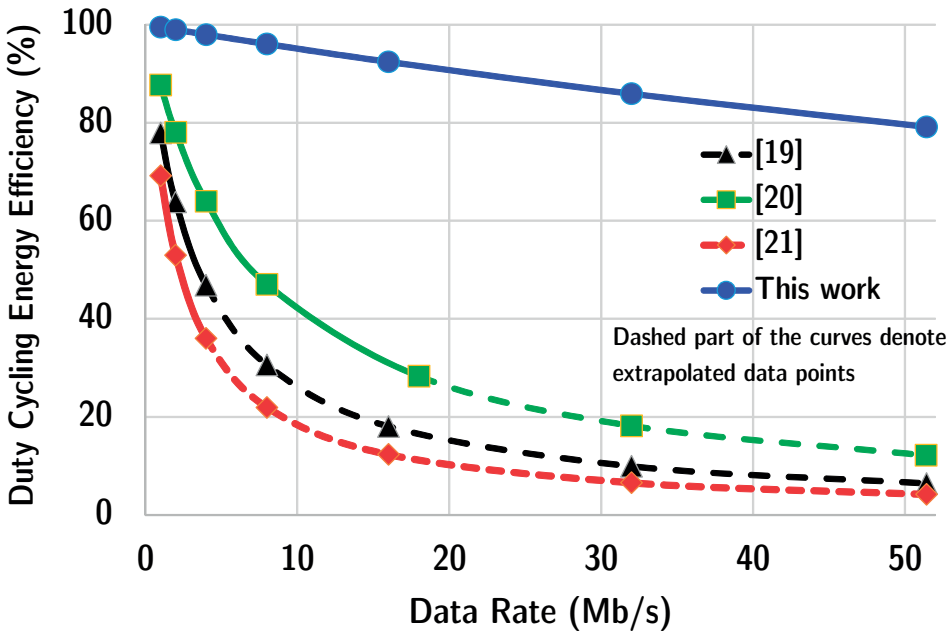


Figure 4.42 – Duty cycling Energy Efficiency comparison of the PDDDS based TX with other State of the Art Transmitters for communicating 32 byte data packets at various data rates

data to be communicated $K$ as well as the length of the packet to be communicated $L$ i.e.

$$E_{oh,tot} = T_{wu} \times \frac{K}{L} \times P_{wu}. \tag{4.30}$$

The energy spent during the active communication phase depends on the power dissipation during this phase $P_p$, the amount of data and the Data Rate ($PDR$) at which the communication takes place i.e.

$$E_c = \frac{K}{PDR} \times P_p. \tag{4.31}$$

Using this information, a comparison metric called the duty cycling energy efficiency ($\eta_{EDC}$) can be defined as

$$\eta_{EDC} = \frac{E_c}{E_c + E_{oh,tot}} \tag{4.32a}$$

$$\eta_{EDC} = \frac{\frac{P_p}{PDR}}{\frac{P_p}{PDR} + \frac{P_{wu}T_{wu}}{L}}. \tag{4.32b}$$

By looking at the above equation, the following observations can be made:

- The $\eta_{EDC}$ does not depend on the amount of data to be communicated and thus can be a global comparison metric.
- $\eta_{EDC}$ tells the designer how efficiently the system uses the available energy for active

Table 4.4 – Performance comparison with prior literature

| Parameter | [18] | [19] | [20] | **This work** |
|---|---|---|---|---|
| Frequency (GHz) | 2.4 | 2.2-2.48 | 2.4 | 2.17-2.47 |
| **Start up Latency** | N/A | 8 µs + XO | 7 µs + XO | **1.5 µs** |
| Phase Noise (dBc/Hz) @ 100 kHz | -86 | -97.6 | -91 | -104 |
| **Data Rate (Mb/s)** | 1.2 | 1 | 18 | **51.4** |
| Power diss. of core TX (mW) | 12.3 @ 1.5 V | 7.0 @ 1.0 V | 11.6 @ 1.8 V | 15.0 @ 1.08 V |
| Output Power (dBm) | 3 | -4.4 | 0 | 3 |
| PA Efficiency | 20.3 % | 5.1 % | 16.7 % | 16 % |
| Process (nm) | 130 | 130 | 180 | 65 |

communication.

- At low $PDR$, $E_c$ is the dominant energy sink and as data rate increases, with all the power consumption figures remaining constant (a hypothetical case since the digital baseband power will be significant at high data rates), $\eta_{EDC}$ drops rapidly as shown in figure 4.42. This is due to the fact that $E_{oh,tot}$ becoming comparable with $E_c$. The same effect is observed if $P_p$ is scaled down without any regard for $E_{oh,tot}$, which is the current scenario in modern ULP radios like [19], [20], [21]. This degradation of $\eta_{EDC}$ can be clearly evinced from figure 4.42 which has been plotted for a packet length of 32 bytes. Readers are requested to note that as a rule of thumb, $P_{wu}$ for the conventional PLL based TX is taken to be 1 mW and the $T_{wu}$ is taken to be 0.5 ms. Another important thing to note is that the work presented in [19] had a maximum output power of -4.4 dBm and hence has a slightly better $\eta_{EDC}$ in the figure (than the hypothetical case if it outputs 0 dBm).
- Thus, the only way to have a linear scaling of $\eta_{EDC}$ is to greatly reduce $T_{wu}$ which was achieved using the PDDDS based TX presented in this thesis. The energy efficiency plot of this work is also shown in figure 4.42 for comparison.

## 4.5 Summary and Prospective work

This chapter presented a Transmitter utilizing a Phase Domain Direct Digital Frequency Synthesizer with an FSK data rate capability of 51.4 Mb/s. The FBAR helps to greatly reduce the start up latency of the synthesizer to just 1.5 µs. The synthesizer is based on the principle of the traditional ΣΔ based frequency synthesis and utilizes an FBAR DCO as the frequency reference. By digitally manipulating multiple time-shifted copies of an FBAR DCO signal, this synthesizer is able to generate a wide range of frequencies from 2.17 GHz to 2.47 GHz. Moreover, a Hybrid Requantizer circuit which allows a tradeoff between the spurious levels

and the phase noise depending upon the application has also been presented in this chapter. The transmitter also employs a sliced PA which helps in power control. The maximum output power of the transmitter is 3 dBm and the Power amplifier achieves a total efficiency of 16 % at 0 dBm output power. Furthermore, the synthesizer occupies an extremely small area of 0.035 $mm^2$ due to its all-digital nature which also makes it an attractive proposition for scaling towards smaller technology nodes. The very high data rate coupled with low latency of this TX greatly improves the duty cycling energy efficiency which, along with very fast channel switching time of just 5 µs, makes this TX ideal for duty cycled networks.

Concerning the prospective work, the following points provide a few pointers to the same.

- The number of stages of the ring oscillator could be increased so as to reduce the Quantization Noise. With an optimal design, a 20 stage ring oscillator locked to a 2.5 GHz signal is feasible within the limits of the 65 nm CMOS process adapted herein.
- A Hybrid requantizer with second order noise shaping and beyond can be envisaged to reduce the in-band noise and make this a suitable replacement for a traditional $\Sigma\Delta$ modulator under all circumstances.
- The Hybrid Requantizer could be implemented in a traditional fractional-N PLL where the PLL, provided a suitable bandwidth could filter out the close-in noise of the HRQ.
- The mathematical model of the noise transfer function of the HRQ needs to be derived to better optimize the tradeoff between the MASH and the SRQ stages.
- There is further scope for optimizing the design of the PA from a power dissipation point of view so as to improve upon its efficiency.
- There is a potential to carry out Digital pre-distortion so as to compensate for the PA non-linearity and make the transmitter suitable for more complex modulation types.

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# 5 Conclusion

In order to reduce the wasted energy overhead to ensure efficient duty cycling of radios, several innovations at the circuit as well as architectural levels have been introduced in this thesis and these innovations have been validated by simulation and measurements.

## 5.1 Innovations

### 5.1.1 ΣΔ Quantization Noise Reduction in Fractional-N PLLs

In order to reduce the Quantization Noise of the ΣΔ modulator used in a fractional-N PLL, thereby enabling an increase of the PLL bandwith and subsequently a reduction in the PLL settling time, this thesis proposed a multi-modulus frequency divider with a division ratio step size of 0.2. Such a reduced division ratio step helps to reduce the Quantization Noise at the output of the PLL by 14 dB. Moreover, the division ratio step size reduction also provides for the decrease of the noise floor increase that occurs due to the folding of the QN passing via the non-linearity of the Charge Pump Transfer function.

From a circuit perspective, the multi-modulus divider was designed using injection locking and the design methodology of a simple and low power retiming circuit based on latches was proposed. This retiming circuit offers the advantage of greatly reducing the power dissipation, unlike similar dividers with reduced step size [1], [2], [3], [4], [5].

### 5.1.2 FBAR based Analog Transmitter

In the chapter 3, the architecture of a PLL-free, FBAR based Analog Transmitter was proposed. In order to cover a wide frequency range, the circuit used a Phase Switching Divider. The utilization of the FBAR helps to significantly reduce the wake up latency, thereby greatly improving the battery life provided the radio is used in duty-cycled energy autonomous systems. To the best of our knowledge, this is the first FBAR based analog TX architecture to support high data rates as well as have a very small energy overhead.

From a circuit perspective, an open loop linearization circuit for the PA was introduced. Compared to complex PA linearization techniques [6], the proposed circuit is a simple feedback that modulates the bias voltage of the PA cascode, thereby aiding in easy polar modulation.

### 5.1.3 FBAR based Transmitter with Phase Domain Direct Digital Synthesizer

In the chapter 4, the architecture of a Phase Domain Digital Synthesizer was presented along with a Transmitter derived from the same. The TX has a wake up time of just 1.5 µs and a sleep time of 1 µs and can support very high data rates, thus achieving very high duty cycling energy efficiency. Furthermore, it can be noted that the denominator of the equation 4.32b has the units of J/b and denotes the energy spent per bit communicated akin to the conventional Energy/bit FoM albeit with the advantage of including the energy overhead. Thus, it provides another metric to compare different transmitters ([7], [8], [9], [10], [11], [12], [13], [14]) as shown in figure 5.1). From the figure, it is clear that the proposed TX with a duty cycling Energy/bit off 500 pJ/b performs better that the other State of the Art Transmitters.

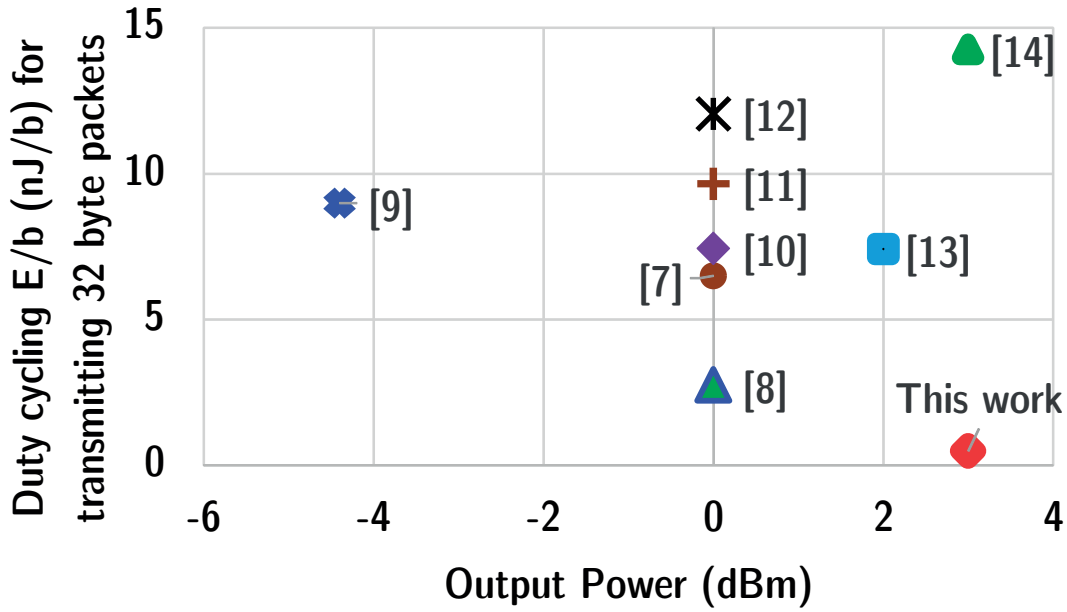


Figure 5.1 – Duty cycling Energy/bit including the energy overhead comparison of the PDDDS based TX with other State of the Art Transmitters for communicating 32 byte data packets

From the circuit perspective, a Hybrid Requantizer (HRQ) which combines the traditional MASH SDM with a shaped requantizer was proposed. This HRQ helps to trade off the in-band noise with the levels of the spurious tones that appear due to non-linearity of the phase domain frequency synthesis. The combination of the traditional MASH with the SRQ helps to reduce power consumption as opposed to a SDM incorporating only SRQ stages. The same technique can be applied to a PLL-based system to trade-off the near integer spurs with the Quantization Noise.

## 5.2 Summary

To summarize, this thesis proposed various methods to reduce the wake up latency and the associated energy overhead and to increase the data rate of radios in order to improve the energy autonomy of battery powered IoT nodes. All of these methods were verified by measuring the Integrated circuits that included innovations in both circuit and architectural levels as mentioned previously. Moreover, a few new metrics that accurately reflect the impact of energy wasted as overhead on the lifetime have been proposed herein to compare the efficiency of various radio architectures employed in duty cycled systems.

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# Curriculum Vitae

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