Enabling High Frequency Reconfigurable Functions with Graphene

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PAR

Clara Fausta MOLDOVAN

acceptée sur proposition du jury:

Prof. J. Brugger, président du jury
Prof. M. A. Ionescu, directeur de thèse
Prof. M. Östling, rapporteur
Prof. J. Robertson, rapporteur
Prof. H. Shea, rapporteur

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE
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There cannot be a greater mistake than that of looking superciliously upon the practical applications of science. The life and soul of science is its practical application.

— William Thomson, 1st Baron Kelvin

To my parents

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Lausanne, March 2016

Abstract

As the scaling of complementary metal-oxide-semiconductor (CMOS) technology is reaching fundamental limitations, novel device concepts and materials have started to be investigated to overcome the scaling challenges for integrated circuits. Graphene has been considered one of the most promising alternatives for the future due to its plethora of superlative properties that are not found in any other material or material system, and consequently, outstanding potential applications in various fields have arisen from this material. However, the high frequency applications of graphene have not seen much progress, with the notable exception of field effect transistors.

The objective of this work is to experimentally investigate graphene's potential for high frequency reconfigurable functions. We propose and demonstrate two novel types of variable capacitors based on graphene for digital and analog radio-frequency (RF) applications, and, finally, place the cornerstone for far and mid-infrared graphene-based technology through a framework that we have developed for applications such as isolators and reflect arrays.

This thesis proposes technology approaches that enable the integration of graphene into high frequency reconfigurable functions and provides a design and optimisation pathway towards competitive performance relative to alternative technologies and unique functionality not matched by traditional counterparts.

First, we demonstrated and fully characterise graphene nano-electromechanical (NEM) capacitive switches and varactors for digital and analog applications at RF frequencies. We empirically investigate several fabrication routes to find the most suitable to obtain a high yield of suspended graphene membranes. We then focus on opportunities for mass production of graphene-based RF NEM switches, examine and compare several approaches with potential for mass production, and further assess the potential for phase shifters working at 2.4 GHz, by calibrated simulations.

The second type of variable capacitor, is a quantum capacitor exploiting graphene in a planar configuration and it is suitable for analog applications. We report the first investigations of graphene quantum capacitors at RF frequencies and demonstrate excellent performance.

Moreover, we propose a novel design optimization strategy leading to a performance superior to alternative technologies at frequencies higher than 2.1 GHz and we showcase it in the development of a phase shifter RFID applications working at 5.8 GHz. The experimental results recommend this graphene-based technology as promising for reconfigurable RF analog functions, without the technological and reliability challenges of NEMS.

Finally, we describe a graphene stacking technology on transparent and reflective substrates at mid and far-IR, with excellent performance in THz devices such as modulators and isolators, and make a systematic investigation of graphene properties at THz and IR.

Keywords: CVD graphene, exfoliated graphene, RF NEMS shunt capacitive switches, tunable capacitors, varactors, quantum capacitance, reconfigurable electronics, THz modulator, THz isolator, graphene stacks, IR complex graphene conductivity.

Sommario

Avvicinandosi ai limiti fondamentali del processo di miniaturizzazione della tecnologia *complementary metal-oxide semiconductor* (CMOS), diviene sempre più importante studiare nuovi materiali o proporre nuove idee per dispositivi in grado di sostenere il progresso richiesto dall'industria elettronica. Il grafene è considerato uno dei materiali più promettenti per il futuro grazie ad una pletora di proprietà eccezionali, superiori a tecnologie alternative. Tali proprietà hanno dato origine ad applicazioni potenzialmente rivoluzionarie nei campi pi disparati. Tuttavia, con l'eccezione dei transistor a effetto di campo, il potenziale del grafene per dispositivi ad alta frequenza è rimasto in gran parte inesplorato.

L'obiettivo principale di questa tesi consiste in un accurato studio sperimentale delle potenzialità del grafene per dispositivi riconfigurabili ad alta frequenza. A tal scopo, in primo luogo abbiamo proposto e dimostrato due nuovi tipi di condensatori variabili basati sul grafene, adatti per applicazioni in radiofrequenza (RF) riconfigurabili in modo analogico o digitale. In secondo luogo, abbiamo sviluppato una tecnologia per massimizzare il potenziale del grafene nel medio e lontano infrarosso (IR), ideale per svariate applicazioni, tra cui isolatori e reflectarray per onde terahertz (THz).

In questa tesi proponiamo sviluppi tecnologici in grado di integrare il grafene in sistemi RF riconfigurabili, progettiamo e realizziamo diversi dispositivi e forniamo linee guida per la loro ottimizzazione, in grado di sovrastare tecnologie alternative in termini di prestazioni o funzionalità.

Inizialmente eseguiamo una caratterizzazione approfondita di interruttori capacitivi nanoelettromeccanici a radiofrequenza (RF NEM) basati sul grafene, e condensatori variabili per applicazioni RF riconfigurabili in modo analogico o digitale. Studiamo sperimentalmente diverse opzioni per sospendere membrane in grafene, con l'obiettivo di individuare la più adatta per massimizzare le probabilità di successo del processo. Di seguito, ci concentriamo su diverse possibilità per la produzione di massa di interruttori RF NEM basati sul grafene, esaminando e confrontando diversi approcci, di cui dimostriamo il potenziale per sfasatori a 2.4 GHz attraverso simulazioni calibrate su esperimenti.

Il secondo tipo di condensatore variabile sviluppato in questa tesi è il condensatore basato sulla capacit quantistica del grafene, realizzato in una tecnologia planare e adatto per applicazioni a riconfigurabilità analogica. Effettuiamo per primi una caratterizzazione dei condensatori quantistici in grafene a radiofrequenza, e riportiamo dispositivi dalle prestazioni eccellenti. Inoltre, proponiamo una nuova strategia per ottimizzare questi dispositivi e garantire prestazioni superiori a quelle di tecnologie alternative oltre 2.1 GHz, e ne dimostriamo il potenziale sviluppando sfasatori per identificazione a radiofrequenza (RFID) a 5.8 GHz. I risultati sperimentali suggeriscono che questa tecnologia basata sul grafene sia molto promettente per sistemi riconfigurabili a radiofrequenza, offrendo prestazioni superiori o comparabili a quelle dei NEMS, oltre ad essere privi dei loro problemi in termini di fabbricazione ed affidabilità.

Successivamente proponiamo una tecnica per impilare diversi strati di grafene, separati da strati dielettrici, su substrati trasparenti o riflettenti nel medio e lontano infrarosso, in grado di permettere prestazioni eccellenti per modulatori e isolatori a onde terahertz. Infine, studiamo in modo sistematico le proprietà del grafene in bande THz e IR.

Parole chiave: grafene CVD, grafene esfoliato, RF NEMS shunt capacitive switches, condensatori variabili, capacità quantistica, elettronica riconfigurabile, modulatore THz, isolatore THz, pile di grafene, conduttività complessa del grafene in banda infrarossa.

Contents

1. Introduction

In the last decades, micro- and nanotechnology have become of tremendous importance for the modern world, enabling a wide range of applications. The aspiration towards faster and smaller computers, ultrasensitive sensors, better medication and, overall, a new generation of products that are lighter, stronger and more efficient, spearheaded the research for new technologies. Research, discovery and innovation are moving forward at a rapid pace, driven by miniaturization. Currently, most devices are based on silicon technology, and improvements are driven by miniaturization and design optimization. However, silicon technology is approaching its fundamental limits, when structures reach the dimensions of single atoms or molecules [1]. International Technology Roadmap for Semiconductors (ITRS) states that a likely solution to the scaling challenge will be based on nonclassical materials for integrated circuit production beyond 2017 [2]. Various material systems have been considered for integration with current silicon technology including semiconducting nanowires, III-V materials, germanium, carbon nanotubes, and most notable, graphene. Graphene is a good candidate to become the next disruptive technology, offering dramatic improvements over the state of the art, due to its extensive combination of superlative properties and its versatility. The 2010 Nobel Prize in Physics acknowledged the striking novelty of the physical properties that can be observed in graphene: different physics principles apply compared with bulk materials and common semiconductors. But what makes graphene extraordinary is that such a combination of superlative properties cannot be found in any other material or material system. Consequently, an abundance of outstanding applications in various fields have arisen from this material. The main applications target a vast number of fields and a few examples are: channel in RF transistors, transparent conducting electrodes, sensors, photodetectors, printable inks, and nanoelectromechanical systems (NEMS). The wide spectra shows graphenes potential as a universal technology, predicting a broad base success.

Fundamental properties of graphene and potential applications are summarized later in this chapter.

1.1 Graphene—The Wonder Material?

Graphene is a one-atom thick planar sheet of carbon atoms packed in a honeycomb crystal lattice, and it is a fundamentally new type of electronic material with electrons strictly confined to a two-dimensional plane, exhibiting properties similar to relativistic particles. Investigations

on graphene started long before the present hype, in the mid 1990s and the evolution of graphene research is depicted in Figure 1.1. The term "graphene" was first officially defined in 1994 as "the individual carbon layers in graphite intercalation compounds" [3]. But long before the nomenclature was made official, graphene was been studied theoretically in band structure calculations as a single layer of graphite used to extrapolate the properties of graphite [4, 5]. Although it was shown that graphite is technically composed of individual monolayers of hexagonally-arranged carbon atoms, it was widely believed that the isolation of such a 2D crystal would be thermodynamically unstable [6] and therefore impossible to perform in an experimental setting.

It was only after 2004, when researchers at the University of Manchester became the first to successfully isolate monolayers of graphite through a mechanical exfoliation/cleaving method [9], that research started developing at a fast pace, promising to completely revolutionize the field of electronics both within and beyond complementary metal oxide semiconductors (CMOS). This seminal work later earned the Manchester group leaders, Andre Geim and Konstantin Novoselov, the 2010 Nobel Prize in Physics, and it represents the starting point of an intense period of research into graphene electronics and beyond.

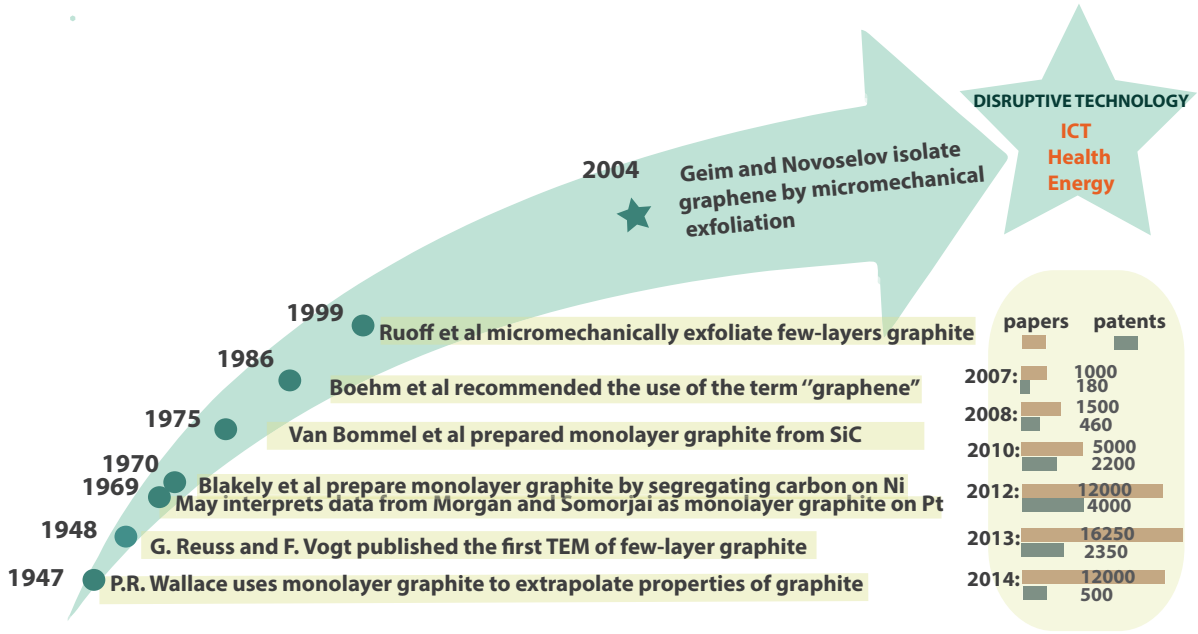


Figure 1.1: Development of the graphene research from the early days until the present. Data from the plot was summarized from [4, 7, 8]. Source for number of papers ISI Web of Science (search: Graphene)

1.2 Structure and Properties

The unique superlative properties of graphene make it a promising candidate to start a paradigm shift in science and technology, from basic physics to industry. It constitutes an interesting two-dimensional electron system for a physicist, a two-dimensional organic macromolecule consisting of benzene rings for a chemist and a material with immense possibilities for an engineer due to its excellent electrical, mechanical, optical and thermal properties. Due to its 2D structure it has significantly different properties from the bulk material due to increased relative surface area, which can change or enhance chemical reactivity [10] and quantum effects that, in turn, can affect the materials optical, magnetic and electrical properties [11]. Whereas carbon is a poor conductor of electricity and not particularly strong, the two-dimensional carbon is a semimetal that exhibits high charge carrier mobility and obeys the laws of relativistic rather than regular quantum mechanics, and has a mechanical strength two orders of magnitude higher than steel.

1.2.1 Structure

Carbon atoms are arranged in a hexagonal structure in graphene, as illustrated in Figure 1.2, and the lattice unit cell is fully described by the vectors $\vec{a_1}$ and $\vec{a_2}$:

$$\vec{a}_1 = \left(\frac{\sqrt{3}}{2}a, \frac{a}{2}\right); \vec{a}_2 = \left(\frac{\sqrt{3}}{2}a, -\frac{a}{2}\right) \tag{1.1}$$

where $a = |\vec{a}_1| = |\vec{a}_2| = \sqrt{3}a_{\mathrm{C-C}} = 0.246\,\mathrm{nm}$ is the lattice constant of the graphene sheet resulting from the distance between two neighbor carbon atoms $a_{\mathrm{C-C}} = 0.142\,\mathrm{nm}$.

The $\vec{k}$ vectors constitute the ensemble of electronic momenta. K and K' have the following coordinates in the momentum space:

$$K = \frac{2\pi}{3a}\left(1, \frac{1}{\sqrt{3}}\right) \tag{1.2}$$

$$K' = \frac{2\pi}{3a}\left(1, \frac{-1}{\sqrt{3}}\right) \tag{1.3}$$

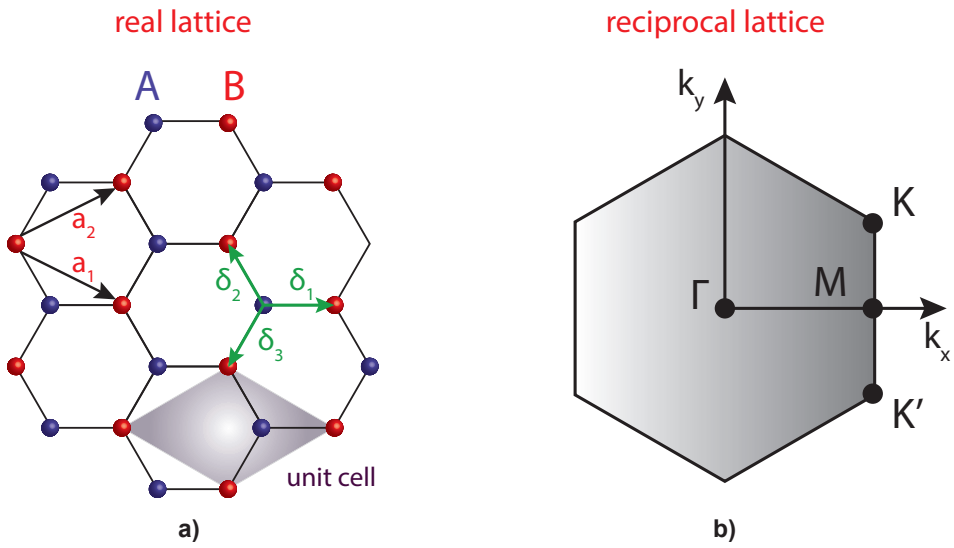


Figure 1.2: Graphene honeycomb lattice. The vectors δ_1, δ_2 and δ_3 connect the next neighboring carbon atoms separated by a distance of 0.142 nm. The two primitive translation vectors are noted by $\vec{a_1}$ and $\vec{a_2}$. b) The first Brillouin zone in the reciprocal lattice. The vertices of the hexagon are called K and K' points and its center, Γ, stands for a zero-wave K vector. The reciprocal lattice vectors are denoted by $\vec{k_x}$ and $\vec{k_y}$.

1.2.2 Electrical Properties

Graphenes unique electronic properties are mostly due to its low-energy electronic structure. The energy dispersion of graphene is given by:

$$E_{g2D}(k_x, k_y) = \pm t \left[1 + 4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right) + 4\cos^2\left(\frac{k_y a}{2}\right) \right]^{1/2} \tag{1.4}$$

Where t is the nearest neighbour hopping energy and a is the distance between two neighbouring carbon atoms. The positive part of the energy dispersion describes the π^* anti-bonding energy band and the negative part is the π bonding energy band. Interestingly, the π^* anti-bonding and π bonding bands are degenerate at the points through which the Fermi energy passes. The first significant feature arising from this fact is that, since the energy band is exactly symmetric around the point E = $E_{2p} = 0$ and this condition is met at the Dirac point (Figure 1.3.a). This means that for a half filling of the band the density of states at the Fermi level is exactly zero and undoped graphene is a perfect semimetal. At zero doping, the lower half of the band is filled exactly up to the Dirac point. A comparison with the band structures of metals and semiconductors is depicted in Figure 1.3.b.

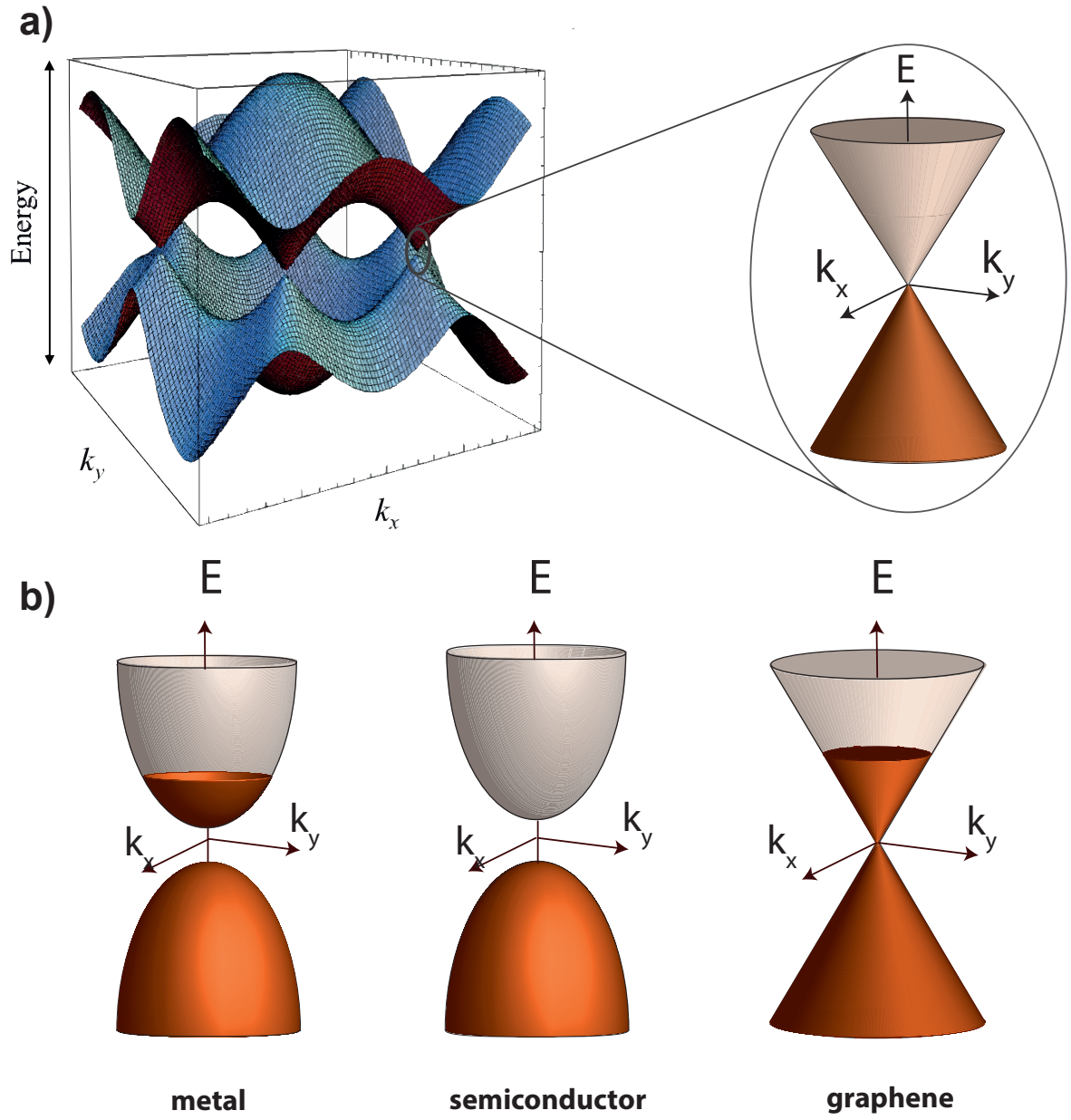


Figure 1.3: a) Energy dispersion relations in graphene. Inset shows the energy dispersion along the high symmetry axes near the Diarc point b) Comparison of the energy dispersion of metals, conventional semiconductors (parabolic shape with a band gap)and graphene.

The density of states is:

$$D(E) = \frac{g_s g_v |E|}{2\pi\hbar^2 v^2} \tag{1.5}$$

where $g_s = 2$ is the spin degeneracy and $g_v = 2$ is the valley degeneracy, i.e., the degrees of

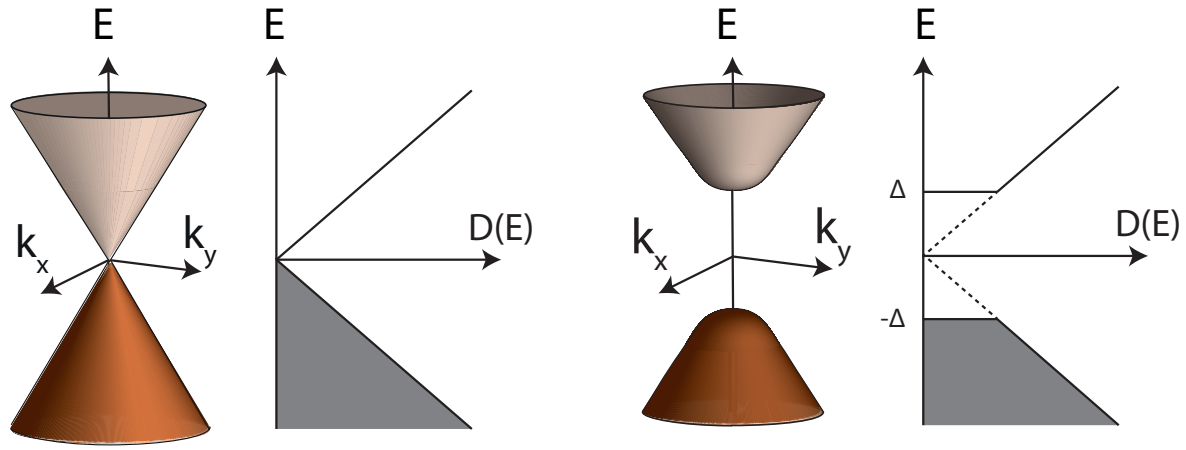


Figure 1.4: Energy dispersion relations in single and bi-layer graphene and the DOS.

freedom for the K and K' points. The energy bands and the density of states in the low energy region of graphene are plotted in Figure 1.4.

The electron or hole concentration at zero temperature is:

$$n_s = \mathrm{sgn}(E)\frac{g_s g_v E^2}{4\pi\hbar^2 v^2} \tag{1.6}$$

$$\mathrm{sgn}(x) = \begin{cases} +1, & (x > 0) \\ 0, & (x = 0) \\ -1 & (x > 0) \end{cases}$$

Owing to its unique band structure, graphene exhibits novel transport effects such as ambipolar field effect and minimum conductivity which are absent in most conventional materials [12]. The unusual electronic behaviour is summarized in Table 1.1.

Transport

Ambipolar Field Effect

By applying a gate voltage to the graphene, relative to the substrate, we induce a nonzero charge, this is equivalent to injecting a number of electrons in the upper half or holes in the lower half of the Dirac cones. This effect is known as the field effect (Figure 1.5).

Table 1.1: Comparison of graphene to traditional semiconductors.

Graphene	**Traditional Semiconductors**
nominal 0 band gap	finite bandgap
the Fermi level in graphene is always within the conduction or valence band	the Fermi level often falls within the bandgap when pinned by impurity states
linear dispersion relation	quadratic dispersion relation
one atom thick $\sim 3\,\text{Å}$ (twice the carbon-carbon bond length)	traditional 2DEG in a quantum well or heterostructure tend to have an effective thickness around 5 to 50 nm
has a finite minimum conductivity [13] $\Rightarrow$ low on/off current ratio	no minimum conductivity high on-off current ratio

Graphene exhibits an ambipolar electric field effect, which means that charge carriers can be tuned continuously between electrons and holes. A single layer graphene on top of an insulating SiO_2 layer constitutes a basic FET structure, and a back-gate voltage can be applied to vary carrier concentration (Figure 1.5). The gate voltage induces a surface charge density $n = \varepsilon_0 \varepsilon V_g / te$ where ε_0 is the the permittivity of SiO_2, e is the electron charge, and t is the thickness of the SiO_2 layer. This charge density is tuned according to the Fermi level

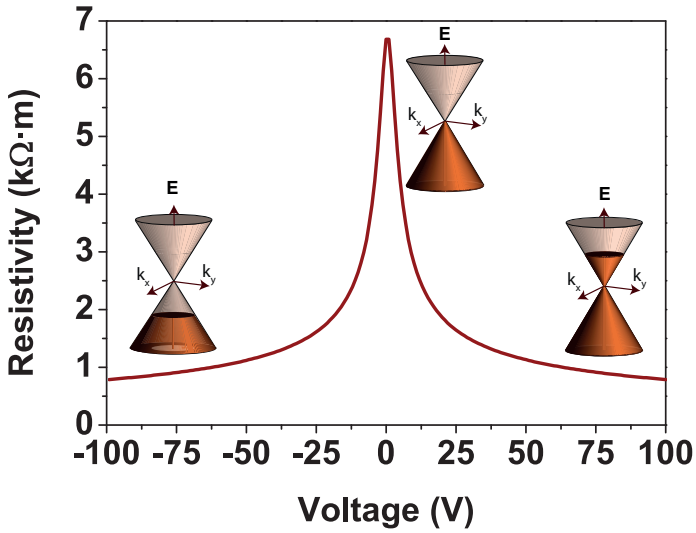


Figure 1.5: Positive (negative) V_g induce electrons (holes) for field-effect devices with a 300 nm SiO_2 layer used as a dielectric and considering a charge injection from $n = \pm 3.6 \times 10^{12}\,\text{cm}^{-2}$. Conical low energy spectrum $E(k)$ indicating changes in the position of the Fermi energy E_F with changing gate voltage V_g.

position (E_{F}) in the band structure (see the insets in Figure 1.5). At the Dirac point, n should theoretically vanish, but thermally generated carriers [14] and electrostatic spatial inhomogeneity [15] limit the minimum charge density. Early graphene FET devices based on exfoliated graphene demonstrated by Novoselov exhibited dopant concentrations as high as $10^{13}\,\mathrm{cm}^{-2}$ and achieved a mobility exceeding $10.000\,\mathrm{cm\,V}^{-2}\,\mathrm{s}^{-1}$ [16], which translates into ballistic transport on submicron scales.

Transport Regimes

Electrons in graphene behave like massless relativistic particles, which govern most of the electronic properties. One of the most important consequences of such a dispersion relation is the observation of half-integer Quantum Hall Effect and the absence of localization, which can be very important for graphene-based field effect transistors [17].

Theoretically there are two transport regimes depending on the mean free path length l and the graphene length L. When $l > L$, the transport is considered ballistic since carriers can travel at the Fermi velocity (ν_{F}) from one electrode to the other without scattering. In this regime, transport is described by the Landauer formalism [18] and the conductivity is expressed as:

$$\sigma_{ball} = \frac{L}{W}\frac{4e^2}{h}\sum_{n=1}^{\infty} T_{\mathrm{n}} \tag{1.7}$$

where the sum is over all available transport modes of transmission probability T_{n}. For ballistic transport mediated by evanescent modes, this theory predicts that at the Dirac point, the minimum conductivity is:

$$\sigma_{min} = \frac{4e^2}{\pi h} = 4.92 \times 10^{-5}\Omega^{-1} \tag{1.8}$$

On the other hand, when $l < L$, carriers undergo elastic and inelastic collisions and transport enters the diffusive regime. This regime prevails when the carrier density n is much larger than the impurity density n_i. In that case, transport is often described by the semiclassical Boltzmann transport theory [15], and at very low temperature, carrier mobility can be expressed in terms of the total relaxation time τ as

$$\sigma_{sc} = \frac{e^2\nu_f\tau}{\hbar}\sqrt{\frac{n}{\pi}} \tag{1.9}$$

Graphene has exceptional transport properties in comparison to common semiconductors, as

can be seen in Table 1.2. The energy band gap (E_g), electron effective mass (m^*/m_e), electron mobility (μ_e), and electron saturation velocity (ν_{sat}) of graphene are compared to those of conventional semiconductors, GaAs and 2DEG [19].

Table 1.2: Comparison between the electronic properties of graphene and common bulk semiconductors.

Property	**Si**	**Ge**	**GaAs**	**2DEG**	**Graphene**
$\mathbf{E_g}$ **@ 300 K (eV)**	1.1	0.67	1.43	3.3	0
$\boldsymbol{m^*/m_e}$	1.08	0.55	0.067	0.19	0
$\boldsymbol{\mu_e}$ **@ 300 K** ($\mathbf{cm^2V^{-1}s^{-1}}$)	1350	3900	4600	1500-2000	$\sim 2 \times 10^5$
$\boldsymbol{\nu_{sat}}$($\mathbf{10^7 cm/s}$)	1	0.6	2	3	~ 4

Frequency Dependence of Graphene Conductivity

Graphene conductivity is frequency dependent, showing a different behaviour at various frequency bands. It is influenced by the surface carriers density n, which depends on the Fermi level μ_c (also referred to as chemical potential). For low value of the carrier density, the thermal carriers are significant, and hence also the temperature T affects the conductivity. Finally, the mean free time between carriers collisions (i.e. carriers' scattering time τ) has an important impact on the conductivity, as it directly related to the carrier mobility μ.

These effects can be modelled using Kubo formula, which provides an excellent numerical approximation of graphene conductivity up to visible light frequencies. The formula is based on the electronic band structure of graphene (discussed in the previous section). The conductivity is given by:

$$\sigma(\omega, \mu_c, \tau, T) = \frac{jq_e^2\left(\omega - j\tau^{-1}\right)}{\pi\hbar^2}\left[\frac{1}{\left(\omega - j\tau^{-1}\right)^2}\int_0^\infty E\left(\frac{\partial f_d(E)}{\partial E} - \frac{\partial f_d(-E)}{\partial E}\right)\partial E - \int_0^\infty \frac{f_d(-E) - f_d(E)}{\left(\omega - j\tau^{-1}\right)^2 - 4(E/\hbar)^2}\right] \quad (1.10)$$

where $\omega = 2\pi f$ is the angular frequency, q_e is the elementary charge, $\hbar$ is the reduced Planck constant and $f_d(E)$ is the Fermi distribution given by:

$$f_d(E) = \left(1 + e^{\frac{E-\mu_c}{k_B T}}\right)^{-1} \quad (1.11)$$

where K_{B} is Boltzmann's constant.

The first integral is referred to as *intra-band conductivity*, and it refers to dynamical phenomena in which carriers remain in the same electronic band. The second one is the *inter-band conductivity* and it takes into account the absorption of photons in graphene due to the interband transitions of carrier from the upper Dirac cone to the lower or vice versa.

While the inter-band integral cannot in general be solved analytically (i.e. requires numerical integration), the intra-band allows a closed-form expression:

$$\sigma\left(\omega, \mu_{\mathrm{c}}, \tau, T\right) = \sigma_{intra} + \sigma_{inter} \tag{1.12}$$

$$\sigma_{intra} = \frac{-jq_e^2 k_B T}{\pi\hbar^2\left(\omega - j\tau^{-1}\right)}\left(\frac{\mu_{\mathrm{c}}}{k_B T} + 2\ln\left(1 + e^{\frac{\mu_{\mathrm{c}}}{k_B T}}\right)\right) \tag{1.13}$$

$$\sigma_{inter} = \frac{jq_e^2\left(\omega - j\tau^{-1}\right)}{\pi\hbar^2}\int_0^{\infty}\frac{f_d(-E) - f_d(E)}{\left(\omega - j\tau^{-1}\right)^2 - 4(E/\hbar)^2} \tag{1.14}$$

The Dirac cone approximation gives mobility μ and carrier density n as function of μ_{c} and τ :

$$\mu = \frac{\tau q_e v_f^2}{\mu_{\mathrm{c}}} \tag{1.15}$$

$$n = \frac{\mu_{\mathrm{c}}^2}{\pi\hbar^2 v_f^2} \tag{1.16}$$

Figure 1.6 shows an example of conductivity numerical computation for typical CVD graphene parameters. Three regions can be clearly identified. For frequencies much lower than τ^{-1} the conductivity is essentially real, namely graphene behaves as a resistor. This range, of *ohmic conductivity*, extends from DC to microwaves.

At terahertz and far-infrared frequencies, the imaginary part of the conductivity becomes significant and dominates in the near infrared. Graphene shows an inductive behaviour which allows the formation of surface plasmon-polaritons.

For frequencies where $\hbar\omega > 2\mu_{\mathrm{c}}$, the conductivity is dominated by the inter-band contribution, and it takes the constant value of $q_e^2\hbar^{-1} \simeq 61\,\mu\mathrm{S}$, known as the universal dynamic conductivity.

Figure 1.7 illustrates the dependence of the complex conductivity on the Fermi level. An increased Fermi level leads to higher carrier density (and hence higher ohmic conductivity) and to a larger transition frequency between plasmonic behaviour and inter-band behaviour.

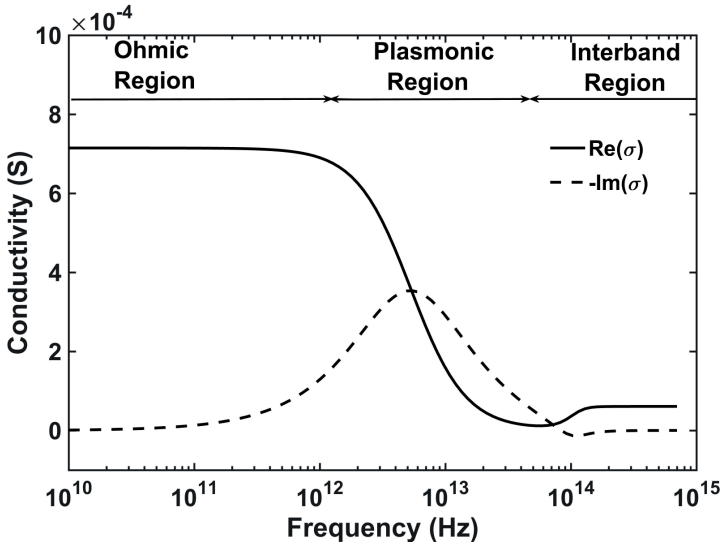


Figure 1.6: Numerical evaluation of graphene complex conductivity using Kubo formula. The parameters τ=30 fs and μ_c=0.2 eV. The imaginary part has a reverse sign to allow better comparison with the real part.

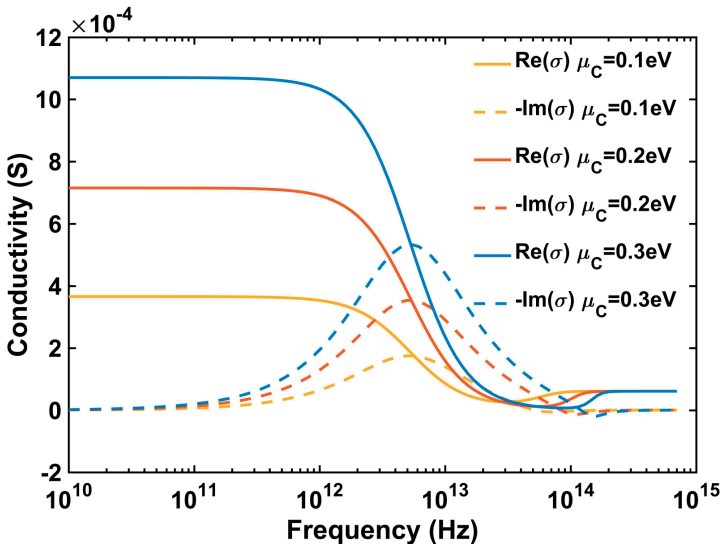


Figure 1.7: Numerical evaluation of graphene complex conductivity using Kubo formula. Various values of Fermi level are used.

Figure 1.8 illustrates the dependence of the conductivity on the carrier scattering time. Larger τ implies higher mobility and DC conductivity, and a lower transition frequency to the plasmonic region.

Finally, if a magneto-static field is applied orthogonally to graphene, the conductivity is given

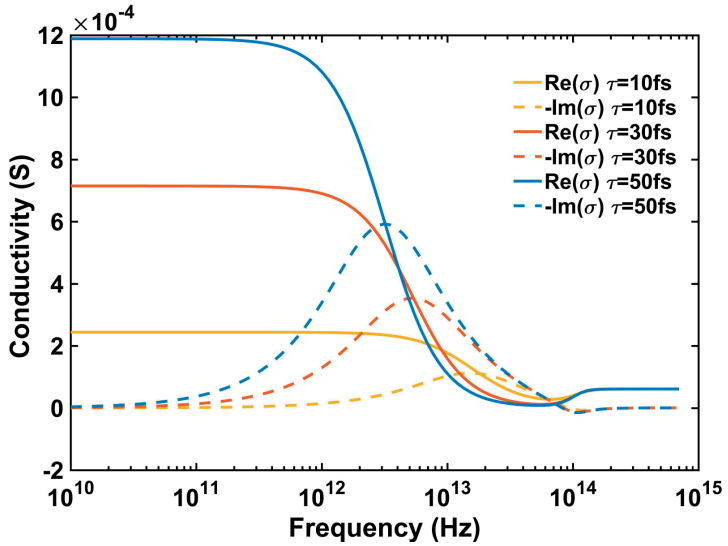


Figure 1.8: Numerical evaluation of graphene complex conductivity using Kubo formula. Various values of τ are used.

by eq. 1.17 and the Kubo formalism gives a discrete summation of terms detailed in [20].

$$\mathbf{J} = \bar{\bar{\sigma}}\mathbf{E} \qquad \bar{\bar{\sigma}} = \begin{pmatrix} \sigma_d & \sigma_o \\ -\sigma_o & \sigma_d \end{pmatrix} \tag{1.17}$$

1.2.3 Mechanical Properties

Graphene exhibits an extremely interesting combination of mechanic properties. The strength of the 0.142 nm long carbon bonds, makes graphene the strongest material ever discovered, with a measured tensile strength, ε, up to 130 GPa [21].It was experimentally demonstrated [21] that suspended graphene shows both non-linear elastic behaviour and brittle fracture. The elastic response of graphene to tensile load is described as: $\sigma = \varepsilon E + \varepsilon^2 D$, where σ is the applied stress, ε is the elastic strain, E is the Young modulus and D is the third order elastic stiffness. Graphene has a Young modulus of 1 TPa. What makes graphene very interesting is that it is not only extraordinarily strong but also very light with 0.77 mg per square metre. Additionally, it has good elastic properties, being able to recover its initial size after strain. In [22] atomic force microscopy (AFM) tests were carried out on suspended graphene sheets of 2 to 8 nm thickness, obtaining spring constants in the range of 1-5 N/m and a Youngs modulus of 0.5 TPa. It exhibits a remarkable response to deformation, being able to withstand up to 20 % tensile strain before fracture [23], superior to hard materials which fail at around 1 %. However, these ideal values are severely influenced by defects in graphene like vacancies [24], Stone-Wales defects [24], dislocations [25] and grain boundaries [26], which degrade its mechanical properties.

1.2.4 Thermal Properties

The thermal properties of a material are essential to ensure small and efficient electronic devices, where thermal management is one of the key factors for better performance and reliability. A considerable amount of heat generated during the device operation needs to be dissipated. Carbon allotropes such as graphite, diamond, and carbon nanotubes have shown high thermal conductivity due to strong C-C covalent bonds and phonon scattering. From the kinetic theory of gases, the thermal conductivity due to phonons is given by $\kappa \approx c_{\mathrm{ph}} CV(T)\lambda$, where $CV(T)$ is the specific heat per unit volume and λ is the phonon mean free path. This implies that since c_{ph} is very large in graphene, a large thermal conductivity can be expected. This was validated for exfoliated graphene flakes by experiments at near room temperature, performed using a Raman spectrometer as an optical "thermometer". A $\kappa \sim 3080 - 5150\,\mathrm{W/m\,K}$ and a phonon mean free path of $\lambda \sim 775\,\mathrm{nm}$ [27] were obtained. These values are, again, among the largest ever measured from any material. However, they highly depend on the configuration, environment and defects such as defects edge scattering [28] and isotopic doping [29]. These factors are generally detrimental to the conductivity due to phonon scattering at defect and phonons modes localization due to the doping. For instance, for supported graphene as well as for nanoribbons, the values for the thermal conductivity were found to be smaller [30,31]. Also, different experiments have found smaller values even for suspended graphene ranging between 600 and 3000 watt/mK [32, 33]. The thermal properties of graphene described in different works, obtained by different methods and types of samples, are summarized in Table 1.3

Table 1.3: Thermal properties of graphene and graphene oxide based materials.

Method	**Material**	**Thermal conductivity (W/mK)@ RT**	**Ref.**
Confocal micro-Raman spectroscopy	Single layer graphene	4840 - 5300	[27]
Confocal micro-Raman spectroscopy	Suspended graphene flake	4100-4800	[34]
Thermal measurement method	Single layer (suspended)	3000 - 5000	[31]
Thermal measurement method	Single layer (on SiO2)	600	[31]
Electrical four-point measurement	Reduced GO flake	0.14 - 0.87	[35]

1.3 Applications

Due to its wide range of outstanding properties, graphene was explored for a large variety of applications in very diverse fields. A high-level overview of the wide range of applications envisaged for graphene films and the properties that enable them is presented in Figure 1.9.

Graphene transistors have been extensively investigated since the material isolation, but a drawback in their implementation in the current semiconductor technology is the lack of a band gap in graphene, resulting in a low ratio between currents in ON and OFF states in graphene-based field-effect transistors [17, 36]. However, graphene transistors may be used in devices which do not require high ON/OFF ratios, but rather high-frequency operation, such as transistors for RF [37, 38] or teraherz (THz) radiation emission and/or detection [39, 40]. The high graphene mobility would favor the high frequency performance. Such devices are exhibiting a cutoff frequency of 100 GHz for a device of gate length of 240 nm and using a source-drain voltage of 2.5 V [41]. Promising current-voltage characteristics of semiconductor-insulator-graphene tunnel diodes as hot-electron injection units in graphene base transistors (GBTs) have also been demonstrated in [42]. Graphene hot-electrons transistors are considered a promising solution to push the limits of electronics to the so-called THz gap [43,44]. On top of its electronic properties, its thermal properties also indicate that graphene is a good candidate for electronic devices, since a high thermal conductivity facilitates the diffusion of heat to the contacts, enabling more compact circuits. Graphene was successfully employed in thermal management applications: graphene-containing metal, ceramic and polymer matrix composites could provide thermal interface materials and heat spreaders [45, 46].

Graphene has also been employed for numerous optoelectronic and photonic devices like light-emitting diodes [47], photodetectors [48], touch screens, smart windows, photovoltaics, quantum dots, saturable absorbers, and optical limiters [49, 50]. Its elastic properties and high strength enable flexible optoelectronic applications such as OLEDs [51], displays and touch screens.

Its unique mechanic properties combined with its low mass make graphene an extremely interesting candidate for NEMS applications such as resonators [52–54] and switches [55]. Its mechanical properties have also been exploited for bioapplications for example in tissue engineering and regenerative medicine [56]. Also nanopores in graphene could enable DNA sequencing [57]. The combination of mechanical properties, conductivity and ultimate thinness make a perfect candidate as a support for imaging in transmission electron microscopy (TEM).

Its high intrinsic capacitance and conductivity combined with its high surface area and an accessible and defined pore structure, good resistance to oxidative processes and high temperature stability make it interesting for batteries, supercapacitors as well as for corrosion barriers

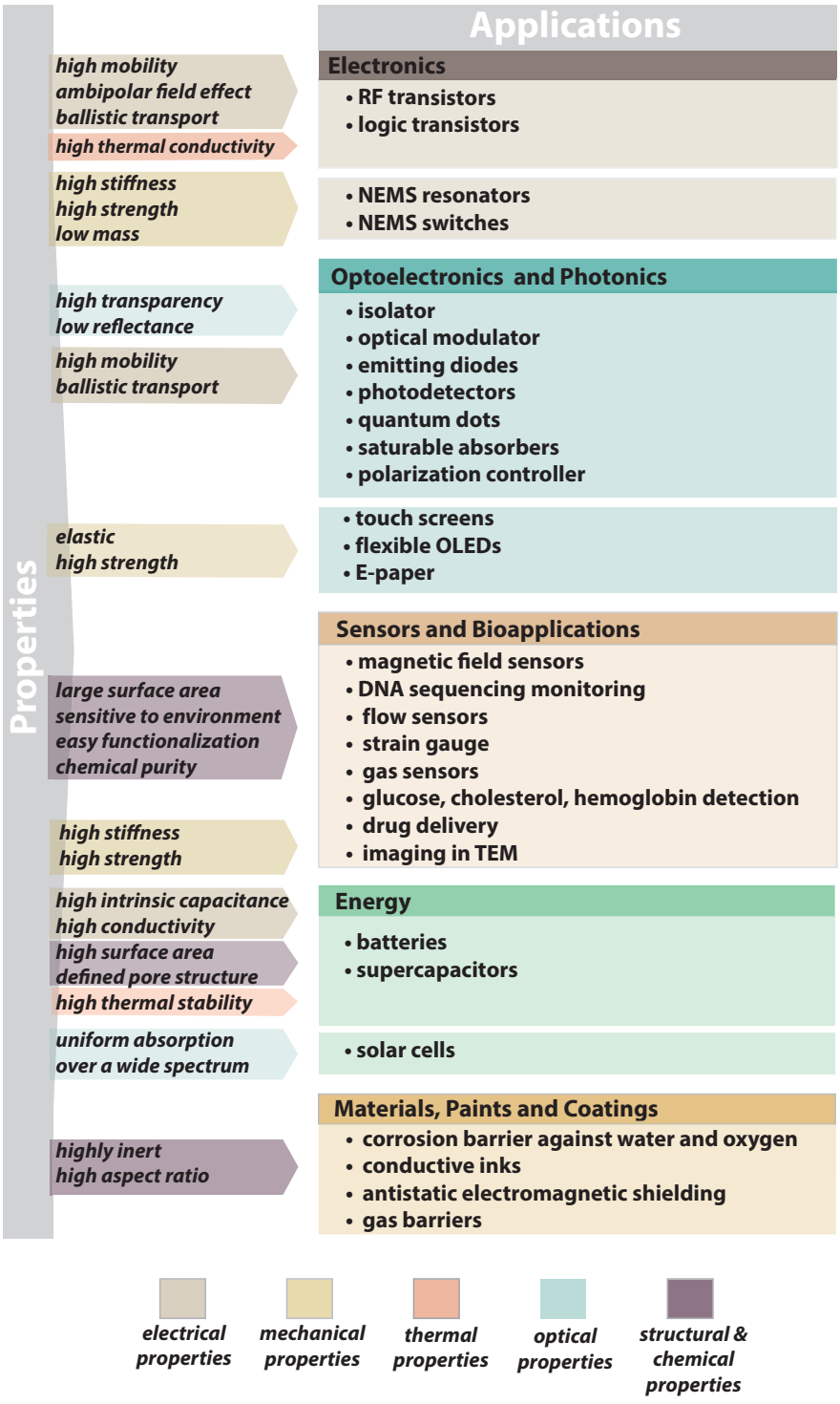


Figure 1.9: Graphene properties and enabled application.

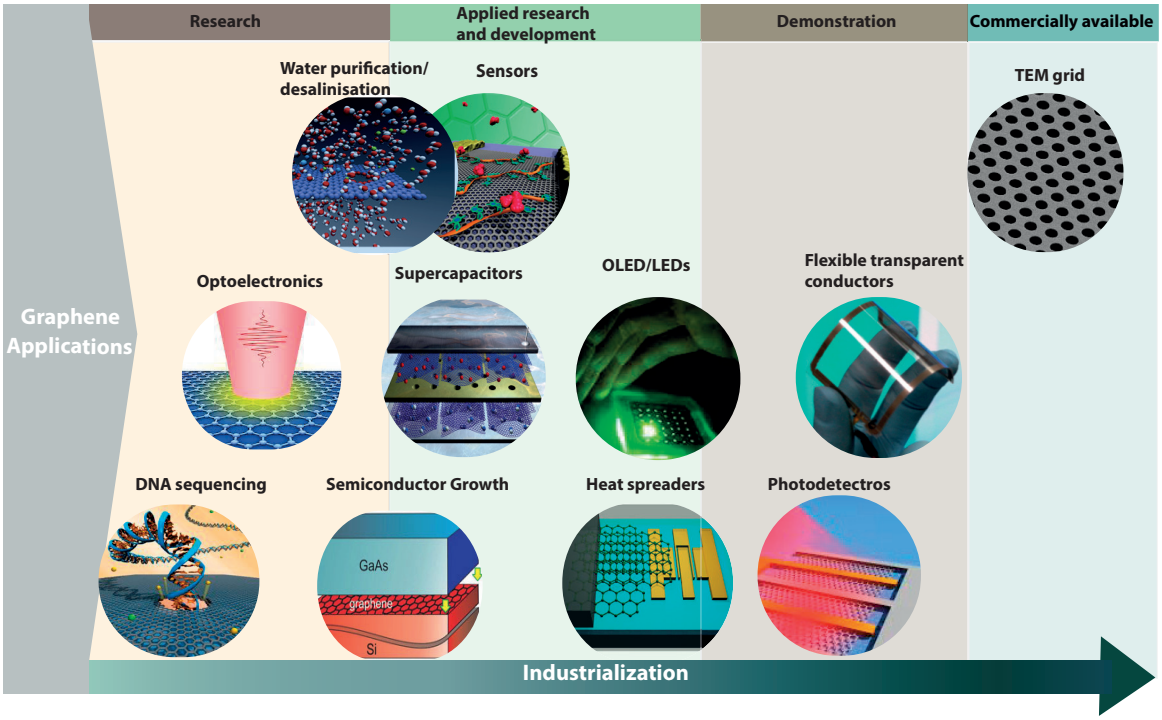


Figure 1.10: Main graphene applications and their development stage.

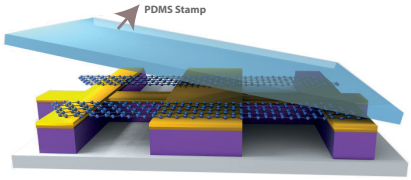
against water and oxygen diffusion etc. Another application is as a substrate for growing high-quality semiconductor materials such as gallium nitride (GaN) [58].

In order to assess the potential of graphene to revolutionize the various fields of science and technology and eventually impose as a technological standard, as well as to have a good indication of the advancements in the specific fields, the development stage for a few applications identified as most promising is depicted in Figure 1.10.

The vast combination of unique properties and the wide spectra of applications recommend graphene as a potential universal technology, pushing further the limits of science and technology.

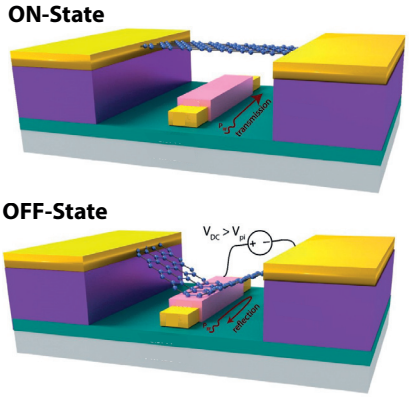
1.4 Thesis Outline

Chapter 2: Synthesis, Transfer and Characterization



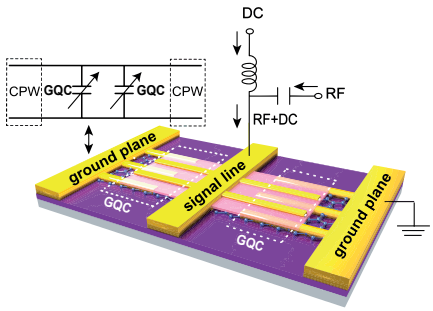
This chapter presents a comprehensive overview of the current state of graphene technology, looking at synthesis and transfer, and emphasizing the methods employed in this thesis. The various transfer strategies adopted both for supported and suspended graphene samples are discussed and characterized. The ability to suspend graphene membranes reliably, with a higher yield than previously reported, is instrumental for the work presented in Chapter 3. Supported and suspended graphene structures are characterized by several nano- and macro-scale methods, to assess their potential for the applications further developed in this thesis.

Chapter 3: Graphene NEMS Switches for Reconfigurable RF Applications



This chapter demonstrates the development of graphene NEMS variable capacitors comparing several strategies to suspend the graphene membranes, and reports a detailed characterization of the devices at radio-frequency. The design optimization and the performance trade-offs specific to graphene in NEMS are discussed in a systematic manner. A proof-of-concept device based on exfoliated graphene and a large scale processes using CVD graphene were developed and characterized. Equivalent electric models have been proposed and validated leading to accurate projections of the potential of graphene for RF NEMS variable capacitors, compared to alternative technologies. The applications of the devices are discussed and their use for phase shifters is investigated by calibrated simulations.

Chapter 4: Graphene Quantum Capacitors for Reconfigurable RF Applications

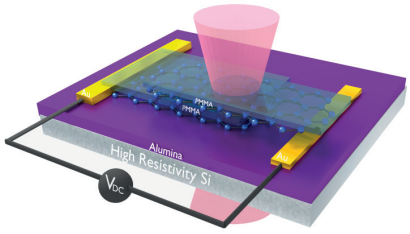


This chapter illustrates and validates an alternative variable capacitor based on graphene for radio-frequency applications, complementary to the graphene NEMS. Graphene's quantum capacitance is exploited to obtain high frequency reconfigurable functions. A route for design optimization and performance boost is devised, leading to performance superior to any available alternatives at frequencies higher

than 2.1 GHz. The applications of the devices are discussed and their use for phase shifters is also investigated.

Chapter 5: Technology Platforms for Mid- and Far-Infrared Applications

Test structures for graphenes characterization at THz and IR frequencies are fabricated and characterized. Basic structures enabling a wide range of applications were demonstrated for the first time, demonstrating viable strategies for integrating graphene in a series of devices like THz modulators and isolators, enabling an unprecedented performance.



Chapter 6: Conclusions and Perspectives

To conclude the thesis, we reiterate through its scientific contributions, highlighting the original achievements in the frame of current technology, and we present an outlook of the necessary technological advancements of graphene processing in the broader context of reconfigurable electronics. The perspectives enabled by these advancements are also discussed based on recent developments in the graphene research.

2. Synthesis, Transfer and Characterization

In this chapter we give a general overview of the main synthesis and transfer methods, compare their potential for graphene integration into electronic devices and their influence on graphene's electrical properties. We first look at the synthesis and transfer methods used later in this thesis, then evaluate and compare several strategies to suspend graphene by transfer on cavities, and finally experimentally examine the spatial distribution and the large-scale average of the electrical properties of supported and suspended graphene, using Kelvin force probe microscopy and Fourier transform infrared spectroscopy, respectively.

2.1 Synthesis

2.1.1 Overview

There has been tremendous progress in the development of graphene manufacturing methods and there is a variety of methods to produce graphene, including mechanical exfoliation of highly-oriented pyrolitic graphite onto oxidized silicon (SiO_2/Si) substrates, chemical vapor deposition (CVD) on metallic thin films, chemical reduction of graphene oxide or graphite, and by the sublimation of silicon atoms from single-crystal silicon carbide (SiC) and by growth on SiC by molecular beam epitaxy (MBE).

As it was discussed in the previous chapter, graphene devices and applications are steadily moving toward industrialization which creates a demand for quality, quantity, reliability and lower cost, in graphene production leading to standardization and industrialization in manufacturing methods. The main quality demands from graphene synthesis methods are:

- controlling the mass production techniques to produce uniform graphene sheets
- realizing direct growth of large-area, uniform, defect-free, few-layer graphene films on arbitrary substrates at low temperatures
- methods for modification, functionalization, and stable doping are also required to achieve the desired properties and enable more extensive use

Figure 2.1 gives an overview of the scaling potential of the main manufacturing methods, while considering the cost and performance, and the main application they are promising for. Exfoliated graphene (ExG) is the most common and least expensive method of graphene

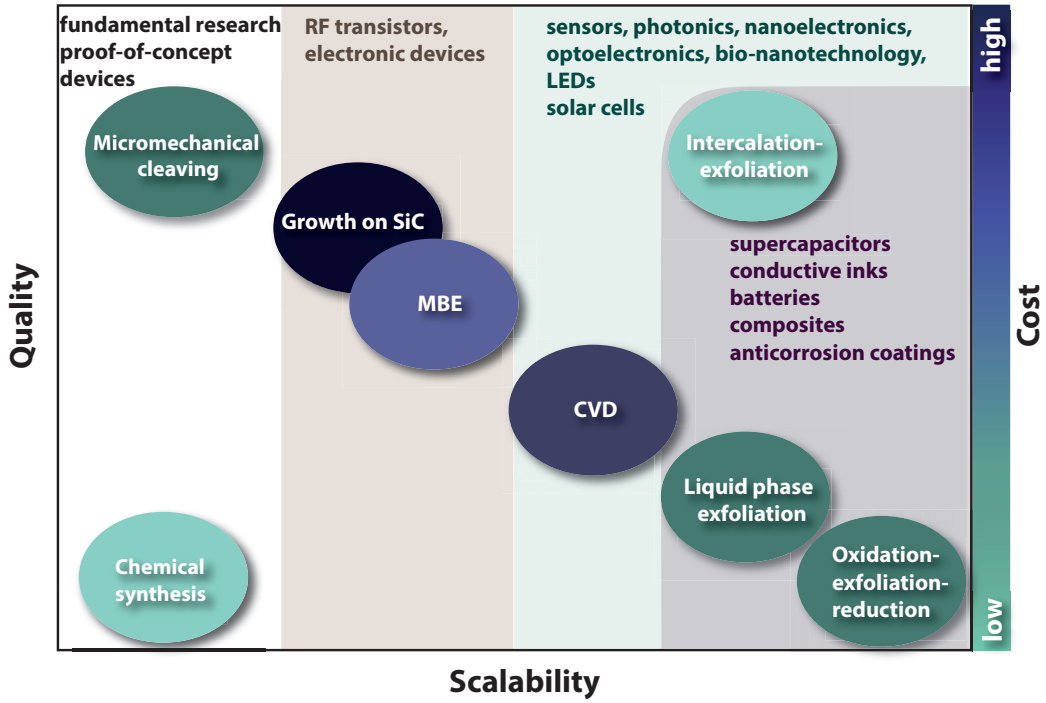


Figure 2.1: Comparison of graphene synthesis methods in terms of quality, scalability and cost.

production, but the exfoliation process and subsequent manual identification of single layer and bilayer graphene regions make this method not suited for mass production. Both CVD growth and graphene oxide reduction require graphene to be transferred to alternate substrates, usually SiO_2/Si, which also limits the quality of the material and the throughput of such methods. In contrast, the sublimation method from SiC, which produces epitaxial graphene (EG), represents a promising route to large-scale manufacturing, but is limited to the SiC substrates and cannot be integrated with CMOS compatible electronics. Next, the main methods are discussed briefly.

Exfoliation

1. Micromechanical exfoliation

Micromechanical exfoliation involves peeling a commercially available highly ordered pyrolytic graphite (HOPG) using adhesive tape [59]. Since graphene layers are bonded to each other by van der Waals forces, which are weak bonds, HOPG can be cleaved, separating one or few layers. Even if this is the easiest method for the production of graphene and is commonly used in laboratory experiments, the production method is not scalable for large-scale graphene production.

2. Liquid Phase Exfoliation

Liquid-phase exfoliation (LPE) involves using a solvent to exfoliate graphite by ultrasonication [60, 61]. Liquid-phase exfoliation of graphite [60, 62] is based on exposing graphite to a solvent with a surface tension similar to that of graphene, in order to obtain an increase in the total area of graphite crystallites, and by sonication, graphite splits into individual platelets, yielding a fraction of monolayer and multilayer flakes in a suspension, which can be further split by centrifugation. This process of liquid based exfoliation of graphite in organic solvent is very promising for large-scale production of graphene.

Graphene can also be obtained by liquid phase exfoliation of graphite oxide, when graphite pellets are first oxidized and then exfoliated by ultrasonication in an aqueous solution [60]. Due to several functional groups like epoxide or hyroxyl, graphene oxide is hydrophilic and can be solvated in water by sonication or stirring. Thereby the layers become negatively charged, and thus a recombination is inhibited by the electrical repulsion. After the exfoliation of graphite oxide, the suspension can be further split by centrifugation, and then it can be reduced to obtain graphene. The reduced graphene oxide has a very bad quality compared to pristine graphene.

Another variation which increases the scalability of the procedure is the oxidation-exfoliation-reduction which uses of a thermal-shock procedure to achieve exfoliation and reduction simultaneously [63]. This method is more industrially relevant in terms of production, but the quality of the graphene is lower than that of pristine graphene obtained from reduced graphene oxide.

3. Intercalation of Small Molecules by Mechanical Exfoliation

This technique consists in incorporating small molecules between the layers of graphite or by non-covalently attaching molecules or polymers onto the sheets, generating graphite intercalation compounds (GICs) without altering the graphite layers. Subsequently the GICs are subjected to shear-intensive mechanical stirring with ultrasonic solvents at room temperature to prepare expandable graphite. The expandable graphite is then expanded at temperatures higher than 900 °C to obtain the expanded graphite (EGt) and trough an additional sonication step pristine graphene is obtained. Li et al. reported the exfoliation-reintercalation-expansion of graphite to produce high quality single layer graphene sheets stably suspended in organic solvents [64]. This metod was adopted for mass production by several companies which produce hundreds of tons annually. This process is easier to scale up, more efficient, causes less pollution than the oxidation route, and has a much higher yield than the direct liquid-exfoliation route.

Growth of Graphene on Surfaces

1. Epitaxial Growth

Surface silicon depletion of SiC substrates is a promising route to produce graphene over large areas with high structural quality directly on an insulating substrate. The process consists in heating the SiC substrate around 1000 °C in ultrahigh vacuum which causes the silicon atoms to evaporate, due to its higher vapor pressure, at a lower temperature then the C atoms, leaving behind small islands of graphitized carbon [65–67]. As a first step, a buffer-layer is formed, which is principally isomorphic to graphene (it has the same honeycomb lattice structure and a similar lattice constant), but about one third of its carbon atoms are covalently bond to the SiC substrate. By heating more, more Si atoms leave the surface and a new buffer-layer forms under the first one, causing it to decouple from the substrate and turn into a graphene layer. Cost-effective methods that can control the stacking order of epitaxial graphene at low temperature, without needing any special pretreatment or high vacuum have been developed as well [68].

The physical properties differ between epitaxially grown and mechanically exfoliated graphene [66], due to the influence of interfacial effects in epitaxial graphene, which are dependent on both the silicon carbide substrate and the growth parameters. Additionally, a main disadvantage of this technique is that it is limited to SiC as the substrate material, which is very expensive and not widely used in semiconductor technology.

2. Molecular beam epitaxy

Molecular beam epitaxy (MBE) is widely used to synthesize a variety of materials on a large variety of templates, at temperatures of around (1000 °C) [69]. MBE is a promising method ensuring a good thickness control, which in the context of graphene might enable the precise growth of not only single- but also few-layer graphene films, as well as the direct growth of heterostructures. It uses atomic species as the precursor so it can be used on a multitude of substrates which is a major advantage over the epitaxial growth on SiC by sublimation.

3. Chemical Vapor Deposition

Chemical vapor deposition (CVD) of graphene on transition metals is one of the most promising, cheap and accessible approaches in applications where large-area continuous films are required. It is an industrially relevant method because it can produce large-area films in a short time, that can then be transferred onto a variety of substrates. Graphene is grown on transition metals such as nickel (Ni) [70–73] and copper (Cu) [74–78], by simple thermal decomposition of

hydrocarbons on the surface or by surface segregation of carbon after cooling from a metastable carbon-metal solid solution. The growth on Ni has proven to give non-uniform graphene areas of few to tens microns, due to the lack of control on the amount of carbon which segregates from the metal carbide upon cooling [79]. In contrast, Cu yields uniform large-area single layer graphene [74].

Graphene growth based on CVD has shown exceptional device properties [75], with electron mobilities up to $7350\,\mathrm{cm\,V^{-2}\,s^{-1}}$ [13]. In addition, the large-scale production of $30''$ graphene films was demonstrated using roll-to-roll CVD [80]. The graphene obtained from this process was of high quality, with a sheet resistance of $125\ \Omega/\square$.

The remaining challenges for both epitaxial and CVD methods are obtaining a good control over the film thickness and preventing secondary crystal formation. In an ideal case, both methods rely on the nucleation and growth of a single crystal without the formation of a boundary or seeding of a second layer. Currently, the best specimens have a variation in thickness of perhaps 1-3 layers and are polycrystalline [81].

The main technological limitation is the transfer step necessary to a place the graphene on an insulating or semiconducting substrate in order to build devices, which can degrade the

Table 2.1: Properties of graphene achieved by different synthesis methods.

Method	**No. of layers**	**Sample size (mm)**	**Mobility ($\mathbf{cm^2V^{-1}s^{-1}}$)**	**Resistivity ($\mathbf{k\Omega/\square}$)**	**Ref**
Exfoliation	1 - 10+	1	15000	0.35	[13]
LPE of graphite	5-7	∞ 0.1-1(1 flake)	100	5.1 (30 nm)	[60]
LPE of GO	<100 nm	∞ >1 (1 flake)	1	2×10^4	[82]
Thermal SiC	1 - 4	50 µm	2000	0.32	[83]
MBE on SiC	1	100	6×10^6(4K)	1.15	[84]
MBE on Al_2O_3	1	50	111±23	4.8	[85]
CVD on Cu	1	10-1000	7350	0.125	[75]
	1		16000	5	[86]
CVD on Ni	1 - 4	650	3700	0.1	[87]
Exfoliation-Reintercalation-Expansion of graphite	1 2 3 (on quartz)	∞ 250 nm (1 flake)	N.A.	150 20 8	[64]

electronic properties of graphene, limiting its applications. Recently, it has been demonstrated that CVD can also be used to grow graphene directly on non-metallic substrates [88]. However, a high substrate temperature (1400 °C) had to be used in this process, which is not compatible with standard silicon technology.

Properties of graphene are different depending on the synthesis method, thus the appropriate method needs to be optimised depending on the applications. The electrical properties of graphene obtained by the main methods are summarized in Table 2.1.

2.1.2 Experimental Methods

In this work, we have used single- (SLG), bi- (BLG) and multi- or few-layer (FLG) CVD-grown graphene on Cu and Ni. The experimetal procedures are briefly discussed below.

For proof-of-concept devices, exfoliated flakes were prepared in DTU. Natural graphite (grafit.de) was exfoliated onto SiO_2/Si silicon wafers with 90 nm thermal oxide.

Monolayer Graphene on Cu

SLG using C_6H_6, CH_4, and C_2H_4 as hydrocarbon precursors was performed in customized CVD reactors on commercially available cold rolled polycrystalline Cu foils (Alfa Aesar, 25 µm thick 99.999 % purity) or on electrodeposited foil from Gould GmbH, which is electrochemically polished to attain an RMS surface roughness <10 nm and a thickness of approximate 18 µm. The synthesis follows the steps:

- **Loading and heating:** The Cu foil is placed in a quartz tube furnace and the temperature is raised to 1000 °C over 15 min.
- **Annealing:** Initial annealing in 0.5 mbar in hydrogen atmosphere at 1000 °C for 30 min was performed to clean the surface of contaminants.
- **Growth and Cooling:** A 2:1 mixture of methane to hydrogen was flown over the copper at a pressure of 0.2 mbar for 20 min resulting in complete coverage of the Cu foil with monolayer graphene. Then the furnace was cooled down in H_2 for 2 h.
- **Take out:** Graphene on Cu was taken out at room temperature after the reactor was filled with argon (Ar).

The process parameters for graphene growth are presented in Figure 2.2. In Figure 2.3, the graphene on Cu foil is examined by SEM, and it can be observed that it is mostly monolayer, with few FLG islands. The main features of the layer can be observed: grain boundaries,

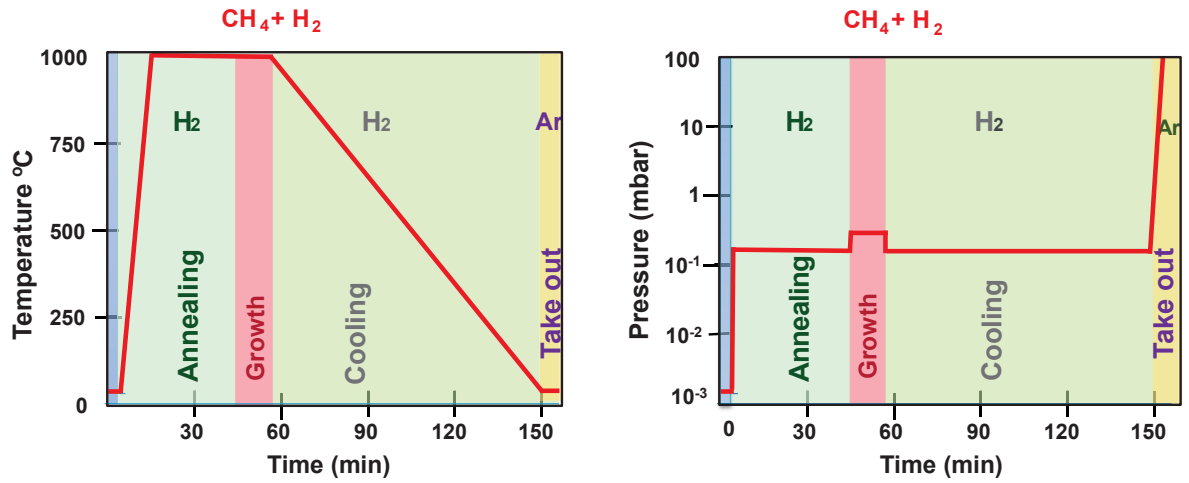


Figure 2.2: CVD graphene parameters. Temperature and pressure profiles over time.

nucleation sites, multilayer patches, ripples and Cu grain boundaries. It has been shown previously that CVD graphene is under significant compressive strain following growth due to a significant mismatch in thermal expansion parameter with the underlying copper [89], strain which is partially mitigated by the formation of thermal expansion folds [90], which can be observed in the image. The graphene also contains a defective lattice in regions that grow on copper grain boundaries [91]. It is expected that this strain will dominate the behavior of the graphene during transfer through the formation of wrinkles and folds as a strain relief mechanism. In addition, other monolayer samples were provided by Graphenea, AIXTRON, UCAM and TCD under the framework of the Grafol european project.

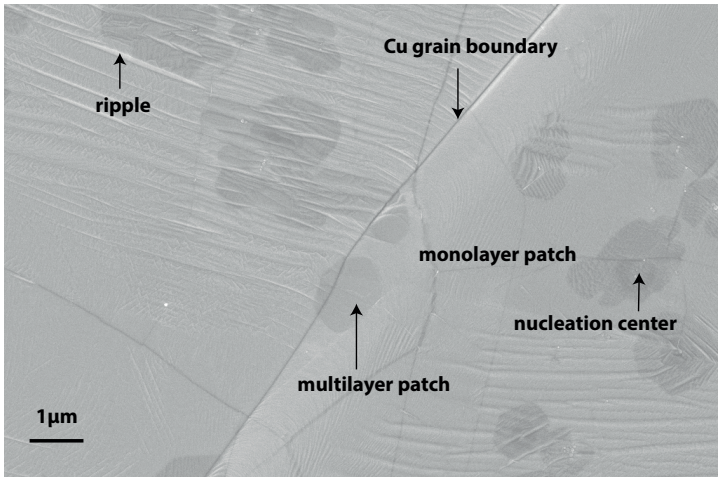


Figure 2.3: SEM image of monolayer graphene on poly-crystalline Cu foil.

Multilayer Graphene on Ni

FLG graphene was grown in UCAM, by exposures of Ni (25 µm) foils, in C_2H_2 at 10^5 mbar and 900 °C for 15 min. The CVD process included a H_2 pretreatment step (0.2 mbar), followed by a quick pump-down to base pressure before introducing the carbon precursor. The FLG sample was grown by a similar procedure as SLG, using an extended hydrocarbon exposure.

The samples used in Section 3.5 were prepared in AIXTRON, UK using the Black Magic set-up, by a similar procedure, on Si/Ni wafers with 500 nm thick Ni layers.

Graphene on Ni wafers in presented in Figure 2.4 showing a non-uniform film with islands of different thicknesses, of areas around tens of microns. From the contrast we can identify 4 different thicknesses along the film. The presence of ripples can also be observed.

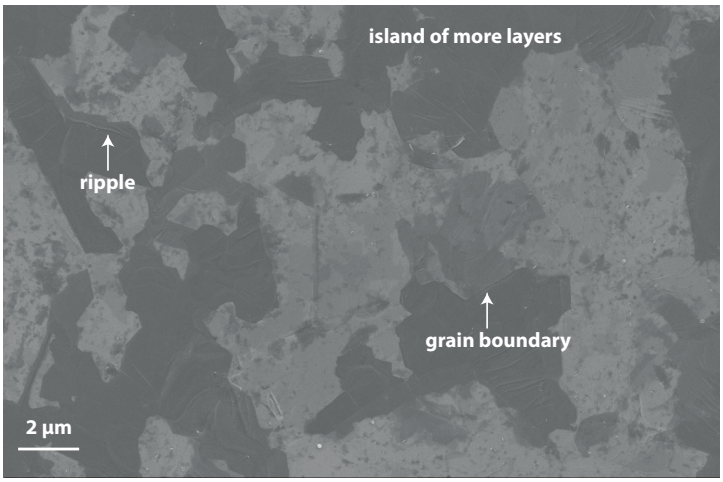


Figure 2.4: SEM image of multilayer graphene on Ni wafer.

2.2 Transfer

2.2.1 Overwiew

As discussed in the previous section, CVD graphene is generally grown on substrates not suitable for device fabrication, so in consequence an essential step in the fabrication process is transferring graphene to the desired substrate. This is the main bottleneck of graphene integration with current CMOS technology. Tremendous work has been done in the past years to optimise this process [77, 92], however it still remains slow, difficult to reproduce, hardly scalable and has a heavy impact on the environment as it involves chemicals such as acids and solvents.

This section presents the methods employed to exploit CVD graphene in device fabrication, namely transferring it from the catalysts to the desired substrates. The transfer method consists basically in etching the underlying graphene substrate and by using a support layer, placing it on the desired substrate either in a wet or dry environment.

In addition, several transfer techniques are developed to suspend graphene on cavities, both with exfoliated and CVD single layer graphene (SLG) and few-layer graphene (FLG).

Wet Transfer

Wet polymer-assisted transfer (PAT) is the most common used method and mainly consists in:

- **Coat Graphene by a Protective Support Layer (SL):** A resin is either spun or drop coated on top of the as grown graphene on metal catalyst.
- **Etch the Underlying Metal Layer:** The SL/graphene/metal stack is gently placed on the surface of the etching solution, mostly hydrochloric acid (HCL) for Ni, iron nitrate (IN), iron chloride (IC) or ammonium persulphate solution (APS) for Cu. The etching time depends on the solution concentration and the metal surface.
- **Rinse and Clean:** The SL/graphene stack is scooped up from the metal etchant to be successively rinsed in several baths of distilled water in order to remove any trace of etching agent.
- **Deposit on the Target Substrate:** The SL/graphene stack is generally scooped from the final rinsing bath with the taget substrate and left to dry. Graphene will adhere to the substrate.
- **Remove the Support Layer:** The resin layer on graphene is dissolved.

This method was first proposed by Reina who transferred graphene grown on Ni with PMMA as SL and using HCL etchant [93]. Kim improved this method and achieved a large-scale transfer of patterned graphene films [87]. A Ni thin film evaporated on a patterned substrate was used instead of Ni foil to obtain graphene patterns.

When CVD graphene on Cu was established, a similar transfer procedure was performed in 2009, using PMMA as SL and IN as etchant [94]. The process was then optimised, demonstrating that this method can reduce the amount of cracks, tears and wrinkles in the final transferred film [95]. In 2010, Iijima introduced the R2R technology, adapting the way electronic devices were created on a roll of fexible plastic or metal foil, to graphene transfer [75].

The choice of transfer polymer and metal etchant solution are important because the presence of residues on graphene surface will drastically influence its properties. Many works demostrated

how absorbed molecules and substrates infuence the properties of graphene [96–98]. The molecules at the interface with graphene modify its electrical properties by introducing dopants or scattering sites, which alter its electronic structure and reduce the mean free path of charge carriers or phonons. The effect of the polymer layers deposited on graphene on its properties was investigated by Pirkle et al., who showed that the thin PMMA residues left after transfer cause p-type doping in graphene field-efect transistors (GFET) and lower the charge carrier mobility [99]. They performed UHV annealing to clean the sample. Other studies indicate that the thermal annealing does not remove the residues entirely [100] and up to temperatures of 600 °C graphene remains p-doped as, at temperature below 400 °C the functional carboxyl groups are present in PMMA, and at high temperature, above 400 °C, doping originates from defects introduced by oxidation during functional groups removal [101]. Etching was also demonstrated to affect graphene properties in various works. Particles of metallic residues can remain on graphene and introduce a strong doping efect by charge transfer [102, 103]. It was also assumed that the metal particles can cause cracks, folds and tears in transferred films since such metals can etch graphene [104, 105]. In addition, it was demonstrated that the strength of graphene is diminished due to the IC etchant [106]. Moreover, other parameters such as etching time, concentration and exposition duration might also have an important effect on the structure and properties of graphene but they have not been investigated.

Wet transfer was also used to transfer graphene on top of cavities, however to date, very low coverage with no intact, and only 6.3 % partially covered membranes was obtained [107]. Even though this method is regularly used for transferring graphene on a large variety of substrates, it was considered not suitable for suspending graphene over sealed cavities, due to liquid trapped inside the cavities by the graphene. However, in this work we demonstrate a good yield of suspended membranes on sealed cavities.

Dry Transfer

The dry transfer method is also generally based on PAT, and the first 3 steps are similar to the previous method. It mainly consists in:

- **Coat Graphene by a Protection Support Layer (SL):** A resin is either spun or drop coated on top of the graphene on metal catalyst.
- **Coat Additional Thick Handle Layer (HL):** On top of the thin support layer a thicker polymer is coated to facilitate graphene handling.
- **Etch the Underlying Metal Layer:** The HL/SL/graphene/metal stack is gently placed on the surface of the etching solution.
- **Rinse, Clean and Dry**: The HL/SL/graphene stack is removed from the metal etchant

using the thick handle layer to be rinsed and dried.

- **Deposit on the Target Substrate:** The HL/PL/graphene film is mechanically deposited on the targeted substrate. The adhesion of graphene to the substrate is strong enough to peel off the handle layer without delaminating the SL/graphene film.
- **Remove the Support Layer :** The resin protection layer on graphene is dissolved.

This process is not as widely used, but lately several variations have been developed, with good results [108, 109]. A method using an intermediate photoresist layer between a PDMS stamp and a PMMA SL was developed, which proved to facilitate a reliable release of the PDMS layer [110]. The combination of this method with a bubbling transfer method, used to delaminate the stack from the copper layer, provides an effective method for high-quality graphene transfer. The main advantage of a dry transfer method is the removal of the etchant molecules which alter graphene's properties. Furthermore, the mechanical stress induced during stamping usually generates cracks or ripples.

This process was employed to achieve suspended graphene on top of predefined cavities, with more success than the wet transfer [107]. In order to avoid issues due to mechanical stability, thermal tape transfers were proposed [107] or an optimised PDMS transfer was described by Suk et al. [77], where a thicker layer of PMMA was used as SL to increase the stability compared to the approach using a photoresist layer between PMMA and PDMS [107].

Next, the transfers performed for this work, in order to achieve the various suspended or supported devices, are discussed in detail. For clarity and an easier connection with the following processes, the sections are structured depending on process type and configuration (supported or suspended graphene). Graphene is transferred on top of predefined cavities in order to achieve suspended graphene for NEMS (Chapter 3). Another strategy used to suspend graphene was to transfer graphene on a sacrificial SiO_2 layer, and subsequently remove it from below the graphene membrane by wet etching. For this structure and the devices in Chapter 4 and 5 a standard wet transfer on various oxide substrates is used.

2.2.2 Transfer on Arbitrary Surfaces

Substrates Preparation

The test structures consist of $1\,cm^2$ CVD graphene transferred on top of a high-k (Al_2O_3) and a low-k (SiO_2) dielectric, respectively, as depicted in Figure 2.5.a. The schematic representation of the fabrication steps of the two different types of substrates is shown in Figure 2.5.b. The substrates consist of high-resistivity silicon ($> 10\,k\Omega\,cm$) on account of its excellent high frequency losses from GHz to IR. Subsequently $72\,nm$ Al_2O_3 were deposited by atomic layer

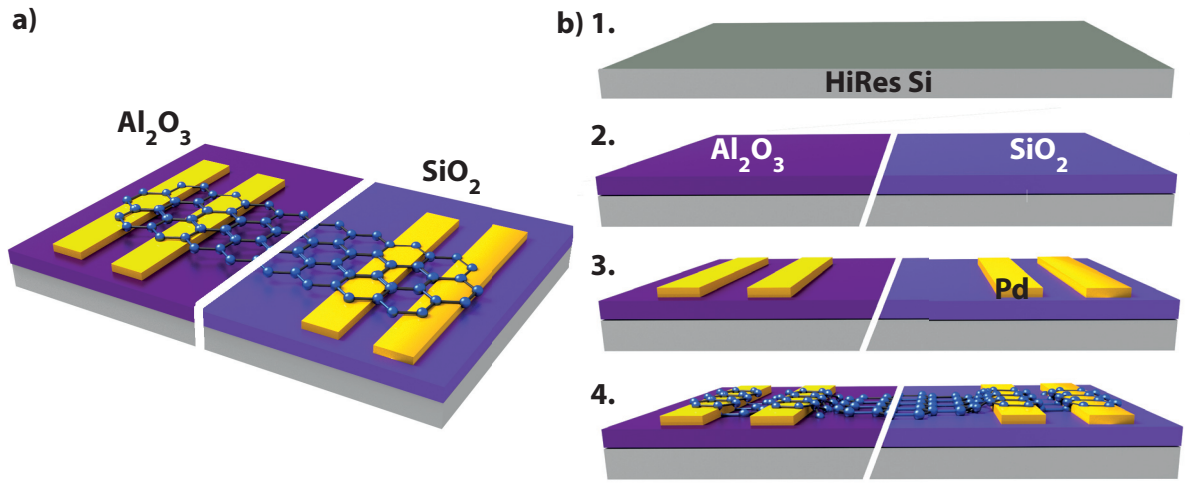


Figure 2.5: a) Representation of the final 2 types of test structures. b) Main steps of the fabrication process.

deposition (ALD) and respectively 90 nm of SiO_2 were grown by thermal oxidation on two different substrates (Figure 2.5.b-2). The thicknesses were chosen to allow optical contrast of graphene so it can be easily identified by optical microscopy. The metal pads are then defined by lift-off of 50 nm palladium (Pd) with 5 nm chromium (Cr) layer. The graphene is aligned on top of 4 metal pads (Figure 2.5.b-4), in order to allow biasing the samples during further characterization, in Section 2.3.1. CVD SLG, BLG and MLG are transferred to various substrates with the following procedure. BLG is obtained by the consecutive transfer of two SLG sheets.

Transfer Method

Figure 2.6 illustrates the steps of the transfer. The SL layer used is PMMA spin-coated directly on the Cu foil (b). The graphene is grown on both sides of the Cu foil but only one side is used, so the layer on the back is removed mechanically with sand paper (c). Subsequently, the foil is cut in 1 cm^2 pieces with scissors (d). The PMMA layer stabilizes the graphene sheet while the copper foil is etched away using a 1 M ammonium persulphate solution (Figure 2.6.e) and then through rinsing in consecutive DI water baths (f, g). The SL/graphene is scooped from the water bath with the target substrate and left to dry (h). Then the PMMA is removed in a hot acetone bath (80 °C) for 2 h and rinsed in IPA and water. A similar process is used for all the types of catalysts: Ni foil or Ni layer on wafer.

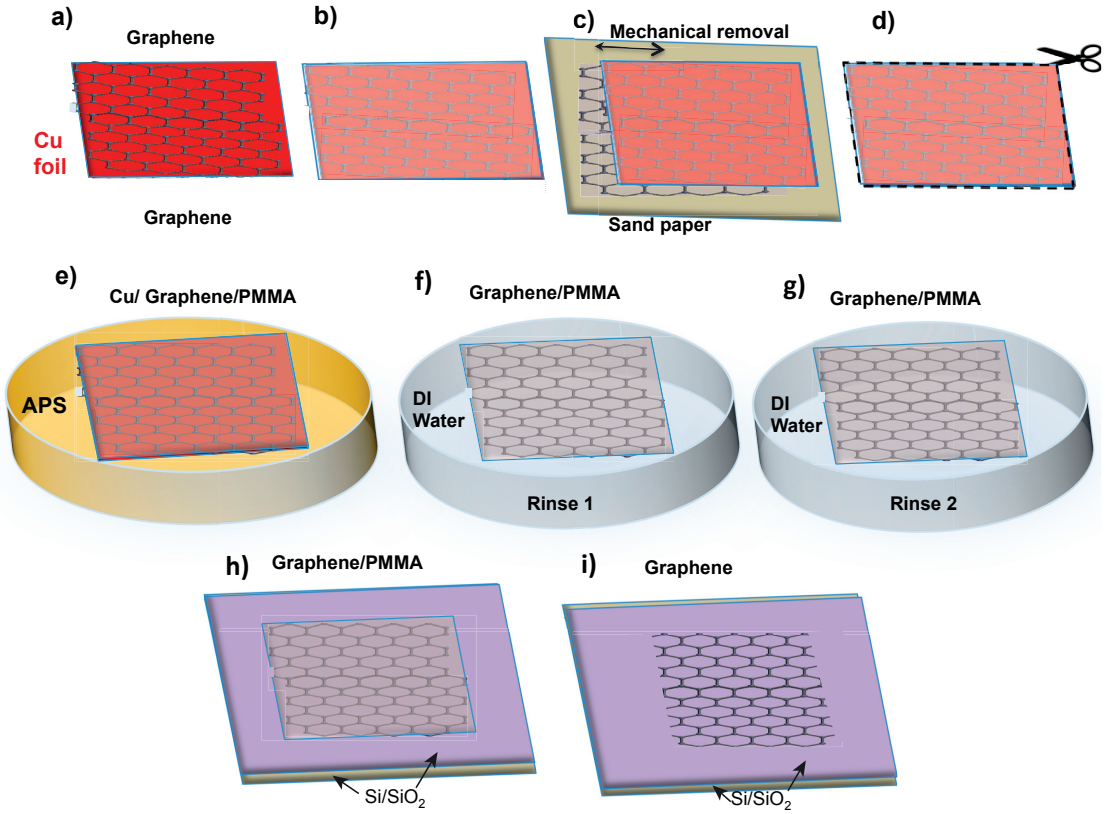


Figure 2.6: Sample preparation and transfer. a) graphene grown on both sides of the Cu foil. b) spin coat PMMA and hard bake the PMMA/graphene stack at 180 °C for 5 min c) remove graphene on the back side of the Cu foil by mechanical pressing d) cut desired size with scissors e) etch Cu foil f) DI water rinse 1 g) DI water rinse 2 h) place PMMA/graphene on substrate i) remove PMMA in acetone + rinse in water.

2.2.3 Small Scale Wet Transfer on Predefined Cavities

Substrates Preparation

This transfer was performed on the structures developed in Section 3.6. Exfoliated SLG and FLG flakes, having dimensions in the order of tens of µm, have been transferred by a method developed in 2010 by Schneider et al. [111], called wedging, and aligned on top of cavities in SiO_2 with few µm precision.

Transfer Method

The wedging technique is based on the hydrophobic effect, removing graphene covered by a hydrophobic polymer from a hydrophilic substrate, which will lift off simply when introduced

in water. In contrast to the first transfer method, where large area graphene sheets are placed on a substrate and are subsequently patterned, here it is important that the micron-sized flakes are precisely aligned on the substrate.

The process is illustrated in Figure 2.7. A graphene flake, which is hydrophobic, is placed on a hydrophilic substrate (e.g. SiO_2, glass, quartz) in our case 90 nm SiO_2 on Si to allow a good optical contrast of graphene, allowing to identify the number of layers of the flake (Figure 2.7.a). A solution of 25 g of cellulose acetate butyrate (CAB) in 100 mL ethyl acetate was spin casted on the wafer and baked at 80 °C for 5 min. Four cuts were wade in the CAB SL 2-5 mm around the flake to be transferred, using a scalpel (Figure 2.7.b). Subsequently, a droplet of DI water was placed over the cut and the piece of CAB was nudged to allow the water to be drawn between the CAB layer and the Si/SiO_2 substrate by capillary action, thereby releasing the graphene from the substrate (Figure 2.7.c). The CAB/graphene piece was then transferred and manually aligned on the target substrate, in water (Figure 2.7.d). Then the water dries out and the polymer film/graphene is fixed on the receiver substrate. The substrate is baked on a hotplate at 135 °C for 1 min with a 10 minute temperature ramp from room temperature (Figure 2.7.e). The CAB was dissolved by placing the substrate in ethyl acetate and then washed in acetone and isopropanol, and finally dried using critical point drying (CPD) (Figure 2.7.f).The success of the transfer was investigated by SEM, shown in Figure 2.8. Reliable and clean transfers of SLG and FLG, on cavities down to 500 nm deep have been achieved. As the graphene sheets are manipulated individually, the transfer is cleaner and less

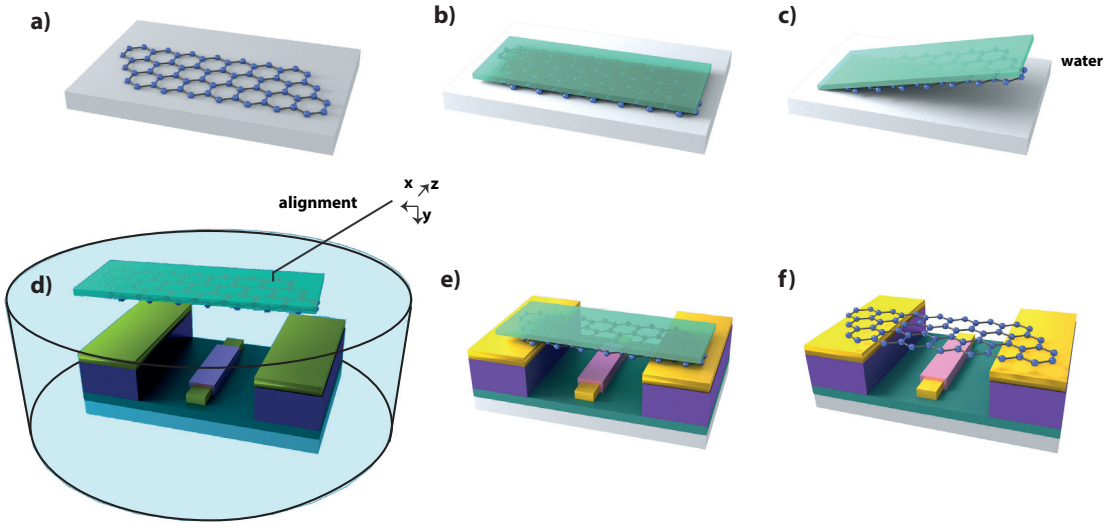


Figure 2.7: Transfer procedure and precise alignment of graphene exfoliated flakes on predefined substrates. a) graphene on hydrophilic substrate (SiO_2/Si)

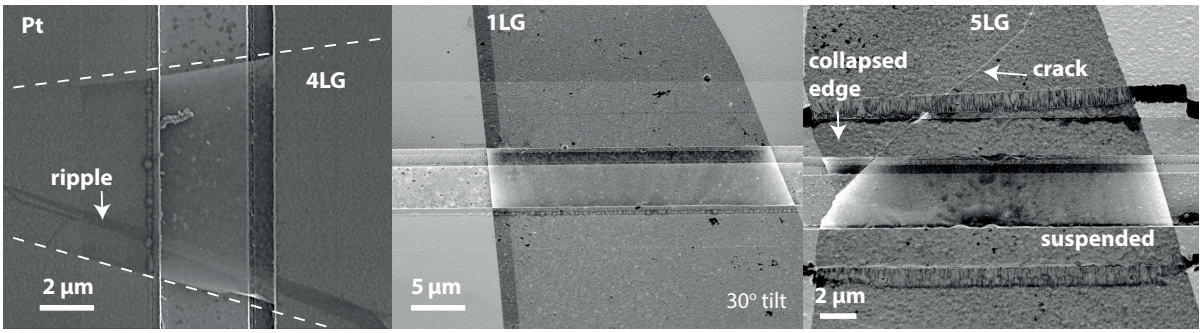


Figure 2.8: SEM of transferred graphene flakes, suspended on cavities. Right: membrane partially collapsed due to a crack.

strain, ripples and cracks are observed. However, this process is ideal for laboratory experiments and process development, but it cannot be scaled for mass production. Nevertheless, this result is instrumental for developing proof-of-concept graphene NEMS (GNEMS) varactors and for validating and optimising a scalable process, described in Chapter 3.

2.2.4 Large Scale Wet Transfer on Predefined Cavities

Substrates Preparation

To optimize the transfer techniques for suspended graphene, SiO_2/Si substrate with cavities defined in SiO_2 with a variety of widths, from 2 to 100 µm, have been developed. A set of samples has a 50 nm layer of evaporated palladium (Pd) layer around the cavities in order to enable biasing them during measurements. The samples consisted in 938 cavities with various sizes and different shapes (square, circular) and depths (0.5, 1, and 2 nm in order to determine the influence of geometry on the transfer. In Figure 2.9, a region of square cavities can be seen.

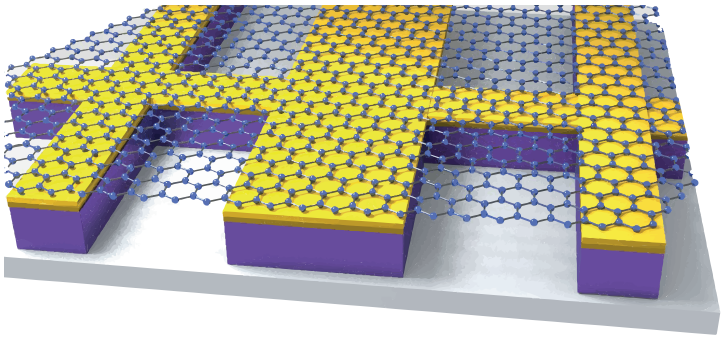


Figure 2.9: Illustration of transferred non-pattern graphene on a SiO_2 substrate with predefined cavities.

Non-patterned SLG and BLG 1 cm^2 films were transferred as illustrated in Figure 2.9. The BLG films were obtained by two consecutive SLG transfers.

Transfer Method

The transfer has been performed in Graphenea SA, Spain and it is a wet PAT method with PMMA SL, like the one described in Section 2.2.2. The difference is that the polymer layer has been removed by a thermal treatment of 2 h at 450 °C, in N_2 atmosphere, to avoid stiction during drying and to remove the water trapped inside the cavities.

The success of the transfer can be assessed by SEM, as shown in Figure 2.10. The cavities where graphene is broken have a bright white edge. The yield is quantified and presented in Figure 2.11 for circular and square cavities for SLG. The inset presents the yield for large scale suspended membranes showing explicitly the number of suspended membranes from the total number of devices. No clear trend was observed between the yield of SLG and BLG. Suspending graphene on circular cavities showed a higher success rate and membranes up to 30 µm in diameter have been suspended.

A closer investigation reveals very clean graphene and the SEM images in Figure 2.12 reveal interesting insights on the influence of graphene structure on the success of the process. It can be observed that nano-cracks start propagating at the grain boundaries. We can also observe that the membranes are slightly strained which again causes ripples or a curtain effect [112] also between grains and islands of FLG. This is an indication that the development of devices on crystalline, uniform graphene is essential for a reliable technological development.

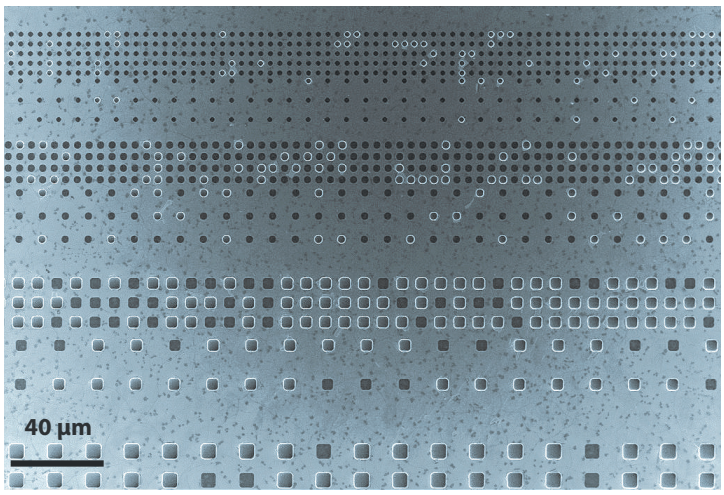


Figure 2.10: SEM image of the transferred CVD graphene on a SiO_2 substrate with predefined cavities, using a wet PAT.

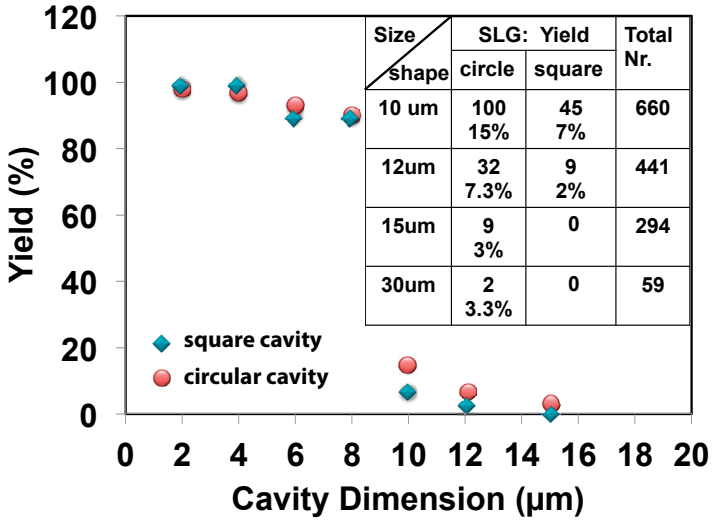


Figure 2.11: Yield of SLG suspended membranes depending on cavity size and shape.

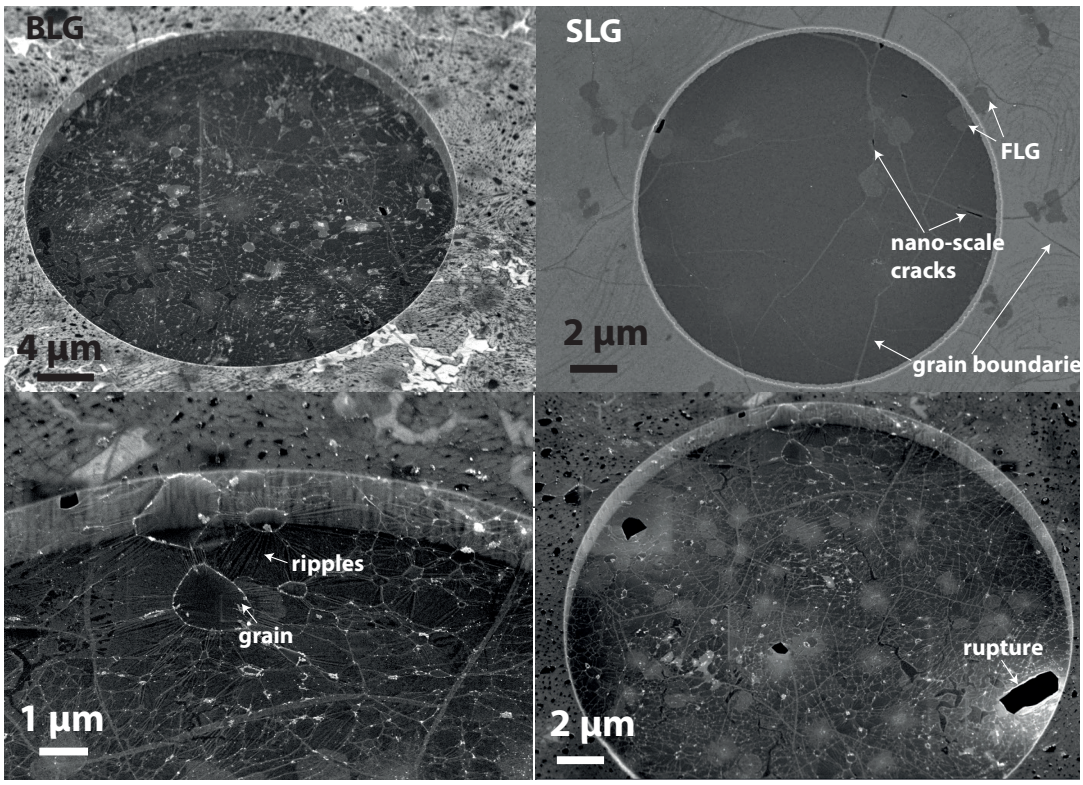


Figure 2.12: SEM image of selected cavities in SiO_2 with suspended SLG and BLG.

This approach proved successful for small size membranes, with an almost perfect yield up to $8 \times 8\,\mu m^2$ and few 30 µm circular suspended membranes have been demonstrated. This gives important insights on size and processing for the devices based on suspended graphene. However, further developments are required to integrate it in device fabrication.

2.2.5 Large Scale Dry Transfer on Predefined Cavities

Substrates Preparation

The test substrates are similar to the ones described in the previous section (§2.2.4), with a layer of 50 nm evaporated palladium (Pd) layer around the cavity in order to enable biasing the samples. *CVD* patterned *SLG* is transferred on an area of $1\,cm^2$.

Transfer Method

In order to avoid the issues of wet transfer of suspended graphene membranes a dry transfer of pre-patterned stripes is developed. The stripes are transferred onto a stamp, representing the HL, used to place them on the target substrate.

The stamp is made of Polydimethylsiloxane (PDMS) by mixing a curing agent and PDMS prepolymer (SYLGARD 184 Silicone Elastomer Kit, Dow Corning) in a 1:5 volume ratio, which were cast onto a polystyrene Petri dish. The stamp was then cured at 22 °C in laboratory atmosphere for 48 h.

CVD SLG was grown on Cu foil (Figure 2.1.2). To avoid processing of graphene once on the destination substrate, it is patterned while still on the Cu (Figure 2.13.a) into 20 µm wide stripes. The Cu foil with graphene was mounted on Dittko thermal tape for ease of handling. It was subsequently patterned by UV lithography and etched in 15 s directional oxygen plasma in an Oxford ICP etcher with low (20 V) acceleration voltage. The patterned graphene is covered with a thin layer of cellulose nitrate SL (2.13.b). The copper foil was etched away in a 1M APS. Identical to the standard polymer-assisted method, the SL/graphene stack is then rinsed by floating on deionized water. However, in this method, instead of picking up the floating film with the substrate, it was picked up with the PDMS stamp and dried in air (Figure 2.13.c). The cellulose nitrate layer was then removed in an acetonitrile bath (2 h) and dried in air. This solvent is compatible with PDMS, which is very sensitive to swelling in certain solvents [113].

The stamp with graphene is flipped over and placed onto the destination substrates forming a van der Waals interface (Figure 2.14.a). Peeling of the PDMS stamp, with a controlled low speed (5–20 $mm\,s^{-1}$) using a Physik Instrumente translation stage, leads to suspended graphene on top the cavities (Figure 2.14.b)

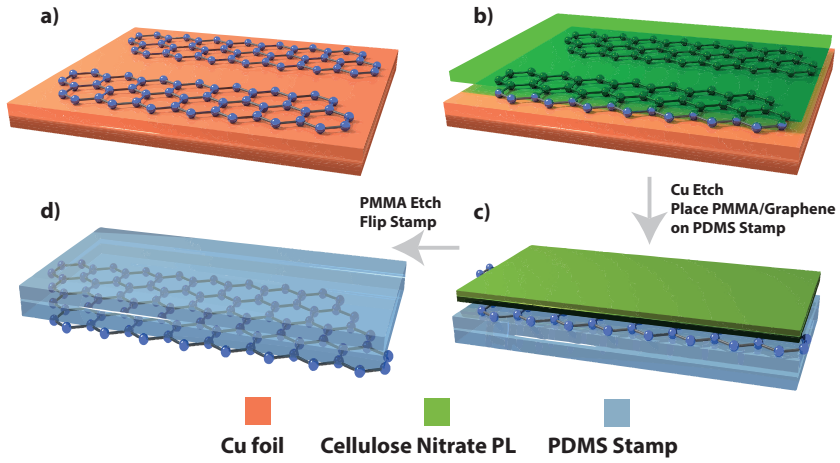


Figure 2.13: The process flow for creating the PDMS Stamp. a) Graphene is grown on copper by CVD and UV lithography is used to pattern graphene. b) A polymer handling layer is spun onto the graphene c) Cu is etched away and Graphene/polymer stack is placed onto PDMS. d) Graphene on PDMS stamp is ready to be placed onto destination substrate.

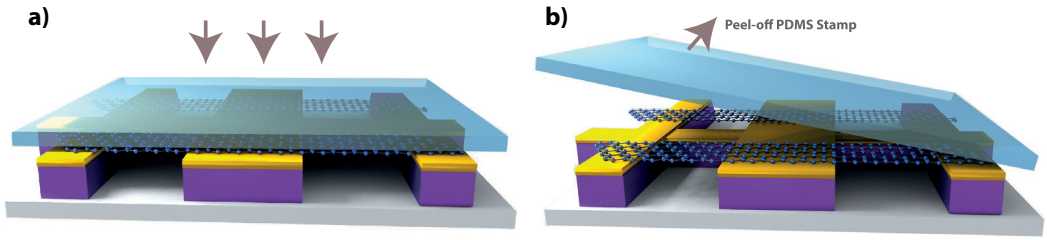


Figure 2.14: Printing large area suspended graphene. a) Graphene on PDMS stamp is placed onto destination substrate. b) Peeling of the stamp leaves graphene on the target substrate, suspended on the cavities.

Figure 2.15 shows a SEM image of the transferred graphene sripes, showing the quality of the transfer. AFM and KPFM characterization of the samples are presented in Section 2.3.2. It can be observed that the complete graphene films were transferred from the stamp to the substrate, but they can contain folds and the uncontrolled shear forces at the cavity edge occasionaly cause the SLG sheets to crack. This can be due to the deformation of the PDMS stamp during printing. Wrinkles can also be observed, and they are due to the release of compressive strain inherent to CVD graphene during transfer from Cu [114].

Here, the suspended graphene membrane is bowed outwards. We attribute this to the evaporation of residual acetonitrile solvent within the cavity leading to a net positive pressure. Not all cavities show the protruding membrane (presumably due to small holes in the graphene)

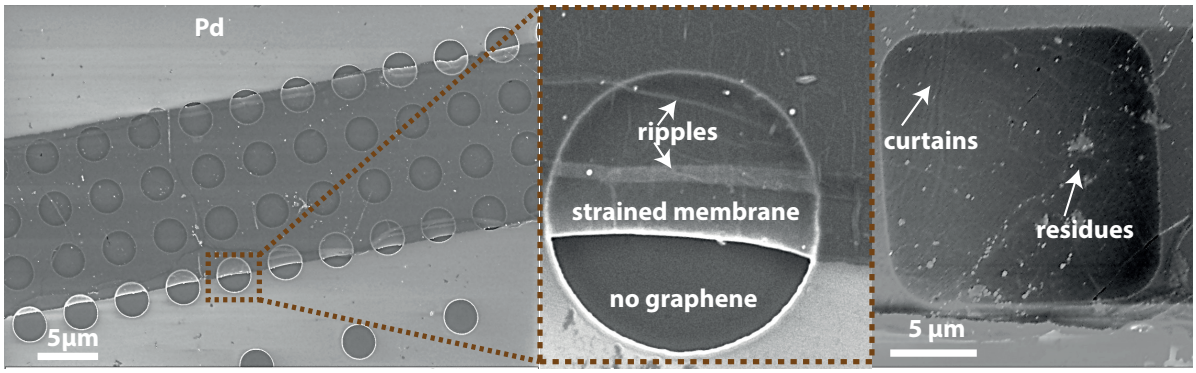


Figure 2.15: SEM images of the transferred CVD graphene on a Pd/SiO_2 substrate with predefined cavities, using a dry PAT.

but it is the predominant behavior in the samples that were investigated. This is consistent with previous reports on CVD graphene membranes which were found to have a very low leak rate for molecules larger than H_2 [115].

The yield of the suspended membranes is determined from the SEM images, depending on the geometry of the cavity. It was observed that the depth and the shape of the cavities do not strongly influence the yield. Instead, cavity lateral dimensions are the limiting factor (Figure 2.16). Similar to the wet transfer method, this technique shows a high yield for membranes up to $8 \times 8\,\mu m^2$, and a higher yield for medium size membranes, possibly due to avoiding wet chemistry, which is susceptible to capillarity effects that can lead to membrane

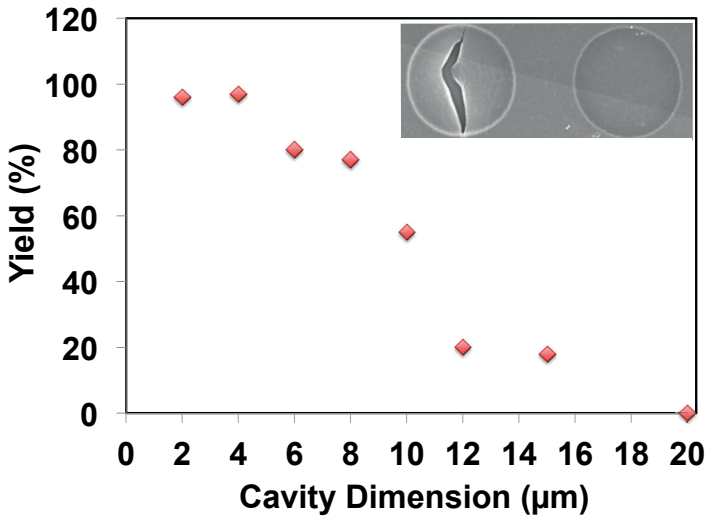


Figure 2.16: Yield of suspended SLG membranes for different cavity sizes.

strain, sagging, or even collapsing. This process is suitable for cavities up to $15 \times 15\,\mu m^2$, area comparable with reports of the largest areas of suspended graphene [116]. This approach proved to be promising for the realization of GNEMS. It is further investigated in §2.3.2.

2.3 Characterization

In order to assess the success of the various synthesis and transfer methods and their viability to be integrated in devices, the samples described in Section 2.2 are characterized.

Due to the unique structure of graphene and of the variability of its properties depending on the environment, sample size, disorder as well as on the frequency range, complementary methods of characterization have been employed to thoroughly understand the factors that need to be taken into account for device manufacturing.

Variability in graphene can result from the material synthesis or post-processing steps as well as the surrounding environment. This is a critical issue for the performance of large area devices as well as for the large-scale production of micro- and nano-scale graphene devices, leading to low yield and reliability. We demonstrate a combination of Kelvin probe force microscopy (KPFM) and non-contact Fourier transform infrared spectroscopy (FTIR) measurements for centimeter-scale quantitative mapping of the electrical variability of large-area CVD graphene films. KPFM provides statistical insight into the influence of micro-scale defects on the surface potential, while FTIR gives the spatially averaged chemical potential of the graphene structures.

2.3.1 Graphene on Dielectric Substrates

The test structures are described in Section 2.2.2, and consist in SLG, BLG and FLG on Al_2O_3 and SiO_2 substrates.

Electrical Characterization

1. Kelvin Probe Force Microscopy

Kelvin Probe Force Microscopy (KPFM) is an atomic force microscopy (AFM) based investigation that provides quantitative values for the work function allowing the extraction of graphene thickness, distribution of the electrical potential and charge at the nanoscale. This method is extremly important for graphene characterization, providing a deeper understanding on its spatial distribution of electrical properties, which heavily influence its behavior. Kelvin probe measurements are performed under ambient conditions using a Veeco NanoMan Vs with NanoScope V controller in amplitude modulation mode (AM-KPFM). The working principle

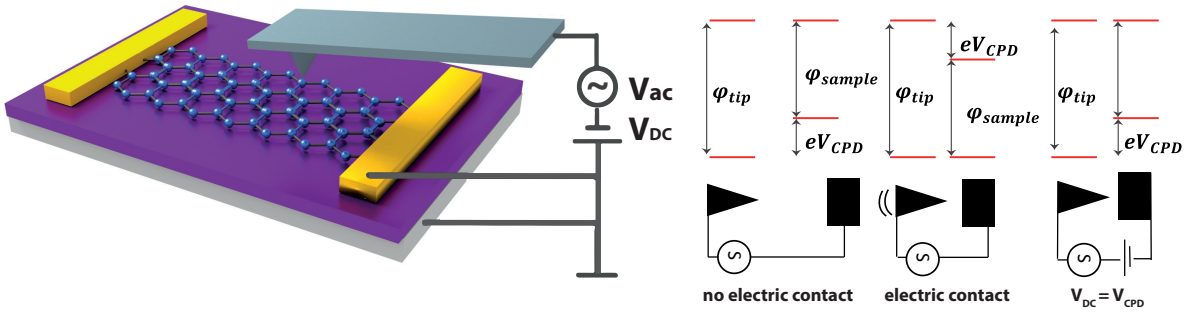


Figure 2.17: KPFM measurement setup and principle.

and biasing scheme are shown in Figure 2.17. An electrical modulation, $V_{\mathrm{AC}}\sin(\omega t)$, is applied to the AFM tip, matching its resonance frequency. When the tip is put in electrical contact with the sample, the Fermi levels of the tip and sample align and the electrostatic force has a componenent modulated at ω, proportional to the contact potential difference V_{CPD} between the tip and the sample [117]:

$$F_\omega = -\frac{dC}{dz} V_{CPD} V_{AC} \sin(\omega t) \tag{2.1}$$

where C is the capacitance between the tip and the sample and z is their separation.

The electrostatic forces are cancelled by adjusting the bias voltage of the tip, $V_{\mathrm{DC}} = V_{\mathrm{CPD}}$ (contact potential difference), until zero amplitude is reached.

From the V_{CPD} value and by knowing the tip work function, ϕ_{tip}, the work function of the sample, ϕ_{sample}, can be extracted, using the formula:

$$V_{\mathrm{CPD}} = \frac{\phi_{\mathrm{tip}} - \phi_{\mathrm{sample}}}{e} \tag{2.2}$$

where e is the electron charge.

The characterization was performed in two scanning steps. The first step records the topography and in the second step the feedback loop is open and the piezo scanner is following the contour recorded during the first scan while measuring V_{CPD}. A PtIr5 coated tip from Nanosensors with $\sim 75\,\mathrm{kHz}$ resonance frequency was used at a scan height of 10 nm. Before the measurements, the work function of the platinum-coated tips is calibrated with highly ordered pyrolytic graphite (HOPG), which has a work function of $\Phi_{\mathrm{HOPG}} = 4.8 \pm 0.1\,\mathrm{eV}$. The absolute surface work function of the sample is:

$$\phi_{\mathrm{sample}} = 4.8\,\mathrm{eV} + V_{\mathrm{CPD-HOPG}} - V_{\mathrm{CPD-sample}} \tag{2.3}$$

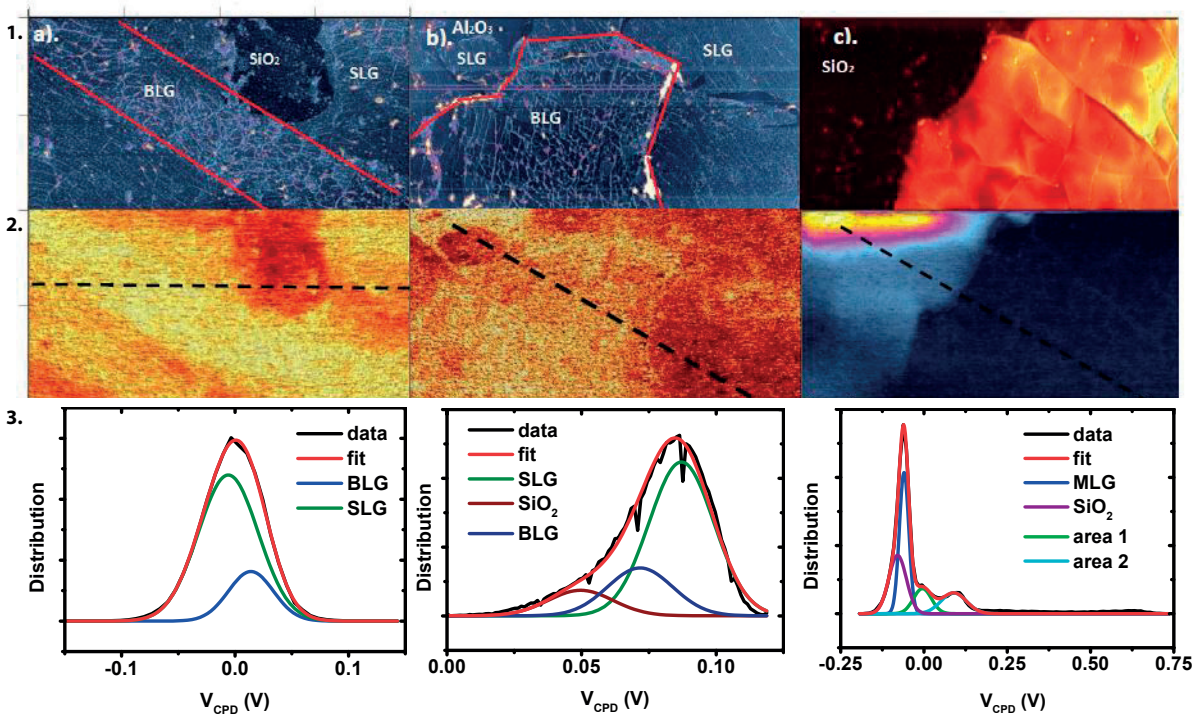


Figure 2.18: KPFM of supported graphene; 1) topography measurements; 2) Surface potential V_{CPD} and 3) the corresponding histograms on a) SiO_2, b) Al_2O_3 and c) FLG on SiO_2. The black dotted lines indicate the area averaged for obtaining the histograms.

Figure 2.18 shows the KPFM images of graphene on SiO_2 and Al_2O_3 showing SLG, BLG and FLG domains as identified on the topography images, in Figure 2.18.1.a-c. The surface potential (V_{CPD}) uniformity in Figure 2.18.2 is determined by a histogram analysis. Figure 2.18.3.a-c shows the KPFM data acquired over the region indicated in Figure 2.18.2.a-c. The data is fitted to a sum of Gaussians in order to show the average values of the measured surface potentials of SLG, BLG and FLG which show a difference of approximately $V_{\mathrm{CPD}} \approx 30\,\mathrm{mV}$. From the KPFM data we compute the Fermi level and charge density (Table 2.2) using the methods shown in [118], assuming that the chemical potential is high enough to approximate the band structure to that of monolayer graphene. For the BLG samples, we assume that the carriers are distributed equally in each independent layer. The scattering, i.e. the width of the distribution of the surface potential of $\delta V_{\mathrm{DC}} \approx 27\,\mathrm{mV}$ can be attributed to an inhomogeneously charged background, as can be observed on the left edge of Figure 2.18.2.c. We observe that the samples on Al_2O_3 show a higher variability $\delta V_{\mathrm{DC}} \approx 55\,\mathrm{mV}$, which could be explained by a larger number of charges trapped at the interface between graphene and high-k dielectrics.

2. Fourier Transform Infrared Spectroscopy

This section presents the non-contact Fourier Transform Infrared Spectroscopy (FTIR) characterization of the graphene samples. The measurements were done in transmission using a Bruker VERTEX 70 FTIR spectrometer in mid and far IR (400 to 8000 cm^{-1}) ranges, at room temperature in a nitrogen atmosphere. The principle is schematically illustrated in Figure 2.19.

Graphene exhibits important spectral features in this range, namely the Drude peak in the THz/far IR region and the interband step in the mid-IR (illustrated in Figure 2.20), which allow the optical carrier mobility, the number of layers and the chemical potential to be determined.

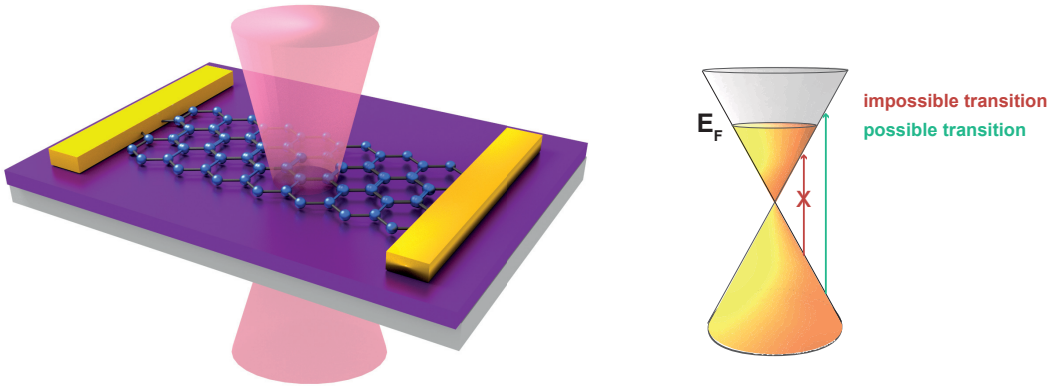


Figure 2.19: Determination of graphene properties measuring the interband step with FTIR.

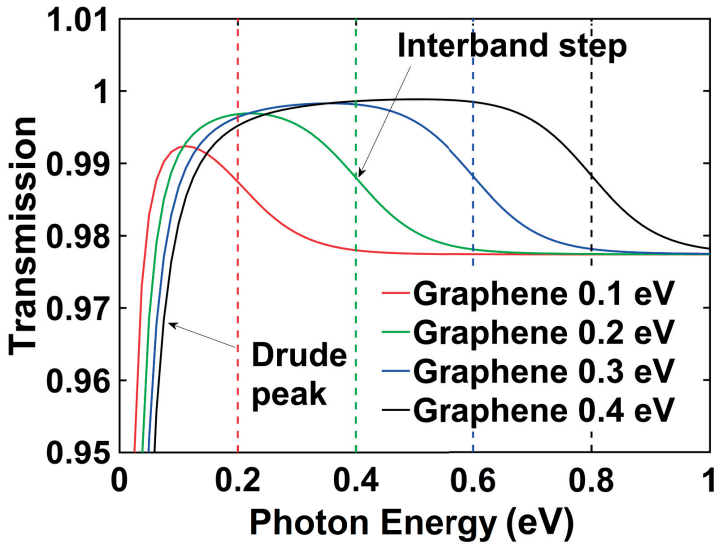


Figure 2.20: FTIR theoretical spectra for suspended graphene, for different chemical potentials.

The width of the Drude peak is directly related to the carrier mobility [119]. In the mid-IR, for a photon energy larger than two times the Fermi level, graphene exhibits universal optical conductivity (16.6 kΩ), while below it shows extremely low conductivities (due to the tail of the Drude peak). From this interband absorption step we can accurately estimate the Fermi level and extract graphene parameters at Infrared. Graphene's universal optical conductivity leads to 2.3 % absorption for normally incident photons at frequencies higher than the interband step and suspended single layer graphene. When graphene is placed on a substrate, the expected absorption is lower, because the optical impedance of the environment is lower, hence the light-matter interaction in graphene is reduced. To retrieve the real value of the absorption step and remove the influence of the substrate, the energy transmitted through the bare substrate is measured first, then the energy transmitted through our graphene structures is normalized to it. For graphene on a substrate with a relative permittivity ε_r, assuming that Fabry-Perot resonances in the substrate are averaged out at the detector, the ratio can be theoretically predicted:

$$R = \frac{2(\varepsilon_\mathrm{r} + 1)}{\varepsilon_\mathrm{r} + (\varepsilon_\mathrm{r} + 1)(1 + \eta\sigma)^2} \tag{2.4}$$

where η is the wave impedance and σ is the electrical conductivity; the relative amplitude of the step is simply (1-R). The measured results for the various samples are presented in Figure 2.21. The features observed near 0.4 eV (2900 cm^{-1}) are due to C-H vibrations bands caused by water absorption on graphene [120]. The peaks in mid-IR near 0.2 eV, were previously observed in single and multilayer graphene [121] and were associated with different band structures of multilayer graphene flakes.

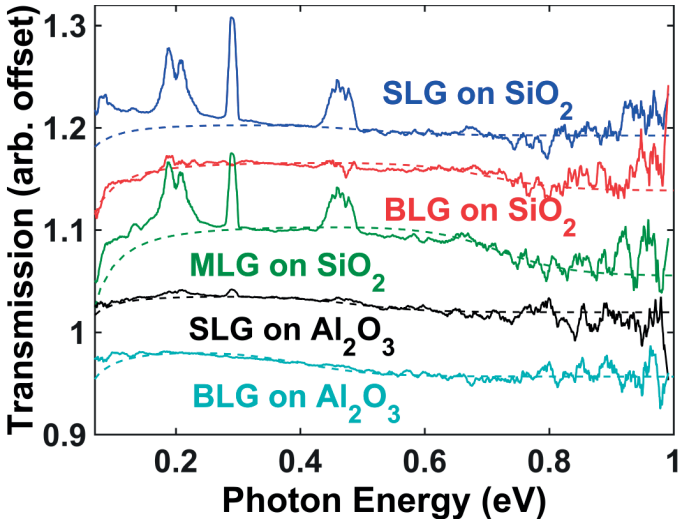


Figure 2.21: FTIR Spectra of the different samples and the corresponding fitting (offset along y axis); insets: determination of graphene properties measuring the interband step with FTIR

Comparing the measured step with the expected step size for a monolayer we can estimate the number of layers. A non-integer number of layers indicates the variability of the number of layers for different positions on the sample, giving important insights into the uniformity of the samples. For accurate results, the measured spectrum can be fitted with the theoretical prediction using as free parameters the carrier scattering time, the chemical potential and the number of layers. The conductivity as a function of these parameters and frequency can be computed using the Kubo formula [122]. The charge density is then estimated from the Fermi level and the number of layers [118]. From the charge density (n_s) and DC conductivity we obtain the DC mobility (μ_{DC}). By fitting the partial Drude peak in the spectra we obtain the IR mobility (μ_{FTIR}).

Raman Spectroscopy

Raman spectroscopy is used to confirm the graphene quality, number of layers and compute the Fermi level of the various samples measured on 2 different areas for comparison. The results are plotted in Figure 2.22. The D band intensity is very low across all samples confirming the low density of defects in the graphene produced [123]. The G and 2D modes are stiffened in comparison with intrinsic graphene. The stiffening of the 2D mode is an indication of p-doping [119] and from the G band frequency we can extract the Fermi level:

$$\omega_G - 1580\,\mathrm{cm}^{-1} = (42\,\mathrm{cm}^{-1}/eV) \times |E_F| \tag{2.5}$$

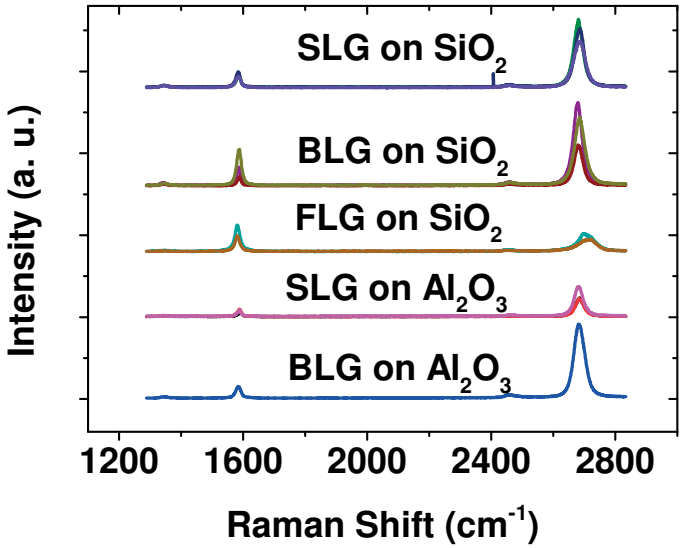


Figure 2.22: Raman spectra ($\lambda = 532\,\mathrm{nm}$) of SLG, BLG, FLG on the 2 substrates.

We plot the computed values in Figure 2.23, for comparison with the values obtained by the other methods. We observe that SLG and BLG both have a typical SLG spectra, due to the fact that BLG is obtained by double transfer and the layers are not perfectly coupled.

Discussion

The parameters obtained by the different characterization methods are discussed, the information they provide about the electrical variability of graphene at small and large scale as well as the differences due to the techniques used, in order to attain a valid evaluation of the quality of the transfers and samples. We observe that the parameters extracted by KPFM and FTIR are different and we can attribute this to the different scattering mechanism at DC and at infrared. The substrate and graphene phonons might reduce the mobility at infrared, whilst charge non-uniformity and imperfections in graphene induced by transfer, like cracks and ripples highly influence the conductivity at DC but not at IR. These imperfections are particularly important for large-area graphene, and they often cause a DC equivalent mobility much lower than the one expected from infrared or small-scale measurements. Figure 2.23 shows the average value as well as the standard deviation of E_F computed from the KPFM data, showing the variability of all the measured areas. The E_F measured by FTIR and Raman are also shown for comparison. We observe a difference of 0.1 to 0.2 eV, which can be attributed to the charges at the interface detected by KPFM, as it is known that KPFM is extremely sensitive to fixed charges and surface dipoles [124], while FTIR measurements are immune to this issue. FTIR and Raman data are consistent, however there are small variations due to the spatial nonuniformity of the samples. The graphene electrical parameters extracted from the different measurements are summarized in Table 2.2.

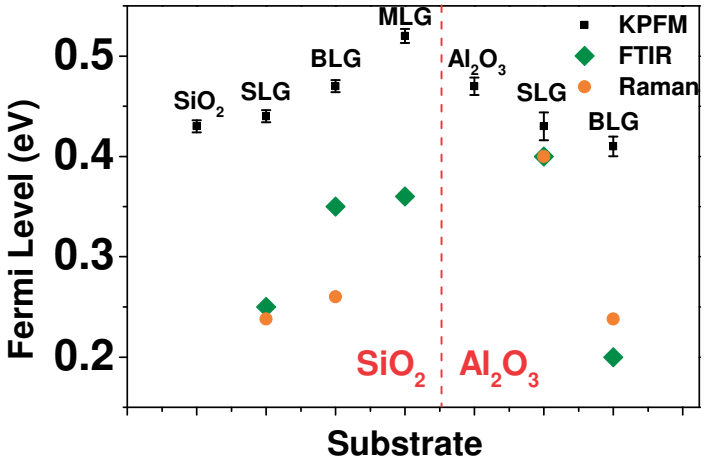


Figure 2.23: Fermi level of the different samples and the variability (standard deviation) measured with KPFM and Raman Spectroscopy and the spatial average measured with FTIR.

Table 2.2: Extracted Electrical Properties of Graphene.

Sample	no. L FTIR	E_F (eV) FTIR	$n_{s\text{-}FTIR}$ cm^{-2}	$n_{s\text{-}KPFM}$ cm^{-2}	μ_{FTIR} $cm^2/(V\cdot s)$	μ_{DC} $cm^2/(V\cdot s)$	$R_\square$ $(\Omega/\square)$
SLG SiO_2	1	0.25	4.63×10^{12}	1.42×10^{13}	800	1400	960
BLG SiO_2	2.1	0.35	1.83×10^{13}	3.24×10^{13}	1000	314	1050
FLG SiO_2	4	0.36	3.84×10^{13}	7.94×10^{13}	1250	111	1125
SLG Al_2O_3	1.3	0.4	4.3×10^{12}	1.35×10^{13}	1540	667	170
BLG Al_2O_3	2.2	0.2	5.92×10^{12}	2.47×10^{13}	1650	1400	675

2.3.2 Suspended Graphene

Electrical Characterization

1. Kelvin Probe Force Microscopy

KPFM is a good indication that the graphene is clean and suspended across cavities. The measurements were done on the samples described in §2.2.5, consisting in printed stripes on top of cavities etched in SiO_2, surrounded by a Pd layer, in order to investigate the transfer used for the GNEMS in §3.7. The KPFM data is presented in Figure 2.24. A topography map is shown in Figure 2.24.a and the surface potential map of a graphene stripe placed on a cavity is shown in Figure 2.24.b. We can clearly observe the state of the suspended graphene, and the particles and water on the surface are more evident in the potential distribution plot than trough other microscopy methods (such as SEM or AFM). The data is evaluated by a histogram analysis, fitting the data to a sum of Gaussians to determine the average values of the different regions, similar to the previous section.

The supported graphene on Pd exhibits a work function of approximately 0.1 eV above that of the tip material (PtIr); 5.05 eV), while suspended graphene exhibits a work function of only 0.07 eV above that of the tip material. We can also see similar values in bubbles and folds in the surrounding graphene. These structures contain locally suspended graphene, resulting in a similar local work function. The surrounding regions are coated in palladium and show a work function 0.15 eV above that of the tip material. Our measured values are slightly lower than the reported values ($\approx$0.3 eV) which we attribute to less impurities, which could induce surface dipole caused by atmospheric water [125]. Several isolated particles (in bright blue)can be identified, where the transfer polymer has been incompletely dissolved. However the histogram analysis shows that their number is very low. This effect has been previously observed for MoS_2 films [126]. Another interesting observation is the accumulation of impurities below graphene

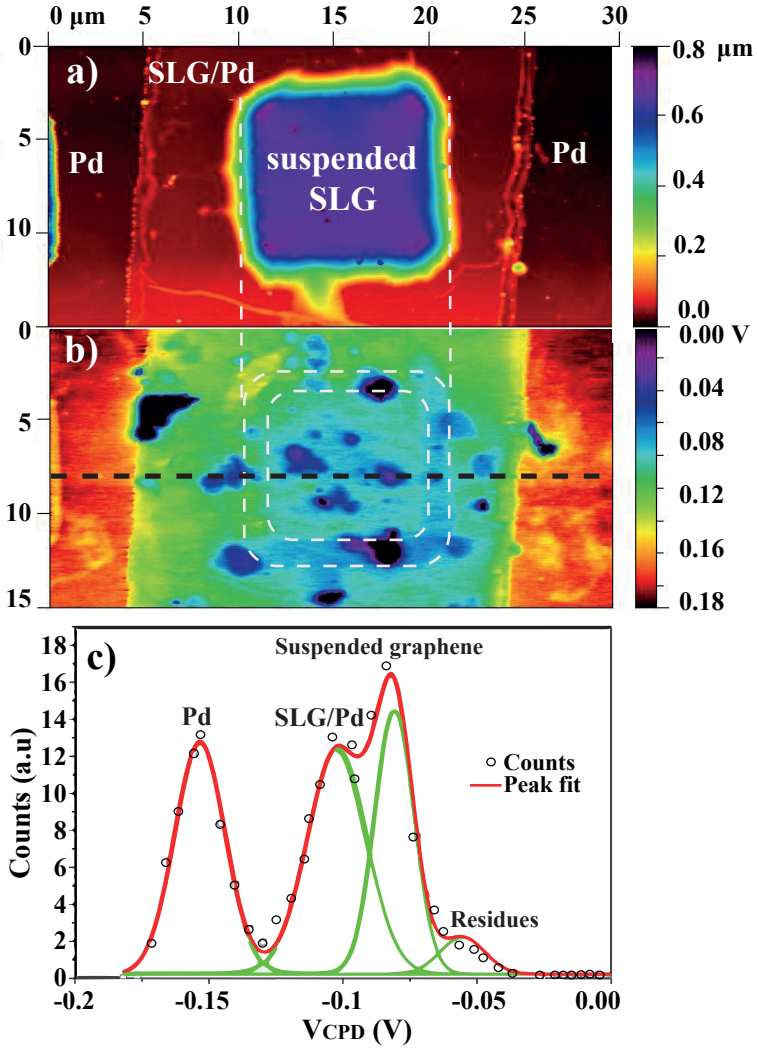


Figure 2.24: KPFM of SLG stripe suspended on cavity; a) topography measurements; b) Surface potential V_{CPD} and c) the corresponding histogram, obtained averaging data along the black dashed line.

around the edges of the cavity. This can have an impact on the GNEMS performance, affecting the electrical contact with the metal pads. Apart from the offset, the overall difference in work function between the Pd and the suspended graphene matches with the previously reported values showing that the graphene is free-standing and free from other contaminants, apart from omnipresent water. Similar to supported graphene we compute the chemical potential of the suspended graphene from the work function value, obtaining a value of 0.8 eV. This high chemical potential value could mean a very high doping level, corresponding to a carrier density $n \approx 4.74 \times 10^{13}\mathrm{cm}^{-2}$, due to impurities accumulated during transfer. In addition, it

can also be due to a high strain in membranes. It can be observed that the suspended graphene membrane is bowed outwards, which can be observed in the topography plot. We attribute this to the evaporation of residual acetonitrile solvent within the cavity leading to a net positive pressure. Not all cavities show the protruding membrane (presumably due to small holes in the graphene) but it is the predominant behavior in the samples that were investigated. This is consistent with previous reports on CVD graphene membranes which were found to have a very low leak rate for molecules larger than H_2 [115].

The scattering (the width of the distribution of the surface potential) obtained in this case is $\delta V_{\mathrm{DC}} \approx 17\,\mathrm{mV}$, lower than the one observed in SLG supported graphene, removing the effect of the background charges. Here, this variation is given only by the surface contaminants resulted during synthesis and transfer. It can be concluded that the substrate has an essential influence on the electrical properties. Also, the developed printing method can lead to folds and impurities on the suspended graphene.

2. Fourier Transform Infrared Spectroscopy

FTIR has been performed on suspended graphene samples, presented in §2.2.4 in a reflection configuration, which allows determining the number of layers and chemical potential and in addition to the transmission method, the depth of the cavity. BLG suspended over a square cavity (having a side length of 20 µm) etched in 2 µm of SiO_2 grown on silicon, was characterized. FTIR was also performed on an empty cavity (bare silicon) and on an area outside the cavity (Si/SiO_2) to extract the influence of the substrate from the measurements. Due to the size of the laser beam, the minimum size that can be investigated is of $20 \times 20\,\mu\mathrm{m}$, with low resolution (as only part of the power of the laser is used). The reflectivity of the bare substrate is constant due to the light reflected at the interface between air and silicon. The reflectivity of the suspended graphene shows an oscillating behaviour due to the Fabry-Perot resonance due to the interference of the light reflected from graphene and from the substrate, as it can be observed in Figure 2.25. The periodicity of the frequency is inversely proportional to the separation of the interfaces, in particular between the graphene and silicon (given by the cavity depth and graphene bending. This curve shows a good fit to BLG suspended over a 1.9 µm deep cavity. The fit is done using the universal optical conductivity of graphene (approximately 61 µS) multiplied times a number of layers of 2. The fitted distance between silicon and graphene is 1.9 µm against the expected 2 µm, showing excellent agreement and indicating that the membrane is flat. In addition, the well-defined Fabry-Perot resonance indicates that graphene is flat and does not bend downwards towards the silicon, or upward as in the previous case. To further confirm the validity of the method and the model, the reflectivity outside the cavity is measured, which shows a Fabry-Perot resonance matching the thickness of 1.96 µm of SiO_2, using a refractive index of 1.44 as expected for this material in

this frequency range. This is consistent with the SiO_2 thickness measured by ellipsometry. The fact that the universal optical conductivity model matches well the curve, down to 0.4 eV, indicates that the Fermi level is significantly lower than 0.2 eV, indicating lower graphene disorder than the printed samples. This can be due to a lower number of impurities on the surface. As expected, the chemical potential is also lower than the value obtained for supported graphene (around 0.35 eV), consistent with the important influence of substrate scattering on the electrical properties.

The analysis could not be extended to frequencies lower than 0.4 eV because the required spot would be comparable to the cavity size introducing unwanted interference effects.

The results prove that the corresponding transfer method and the thermal removal of the support polymer is a promising, clean method to obtain good quality suspended graphene.

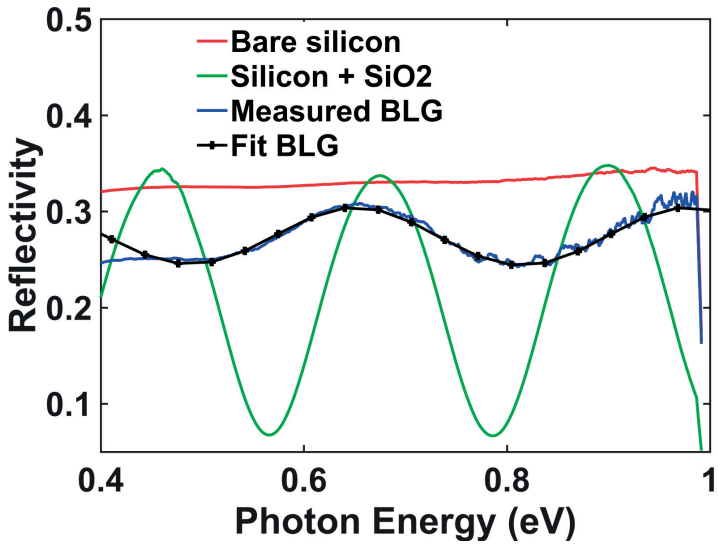


Figure 2.25: FTIR Spectra of the different samples and the corresponding fitting (offset along y axis); insets: determination of graphene properties measuring the interband step with FTIR

2.4 Conclusion

This chapter has presented a generic overview of the main synthesis and transfer methods, in an attempt to identify the most viable options for a scalable and reliable integration of supported and suspended graphene in electronic systems. In this frame, the experimental details on the manufacturing procedures employed for this thesis are provided briefly. While exfoliated graphene has proven ideal for prof-of-concept experiments, CVD graphene was used to achieve large scale, CMOS compatible fabrication of electronic devices.

The main technical contributions of this chapter are:

Sample preparation and investigation of different transfer strategies to suspend graphene on cavities for NEMS:

Clean suspended exfoliated flakes up to $20 \times 15\,\mu m^2$ were successfully produced by a wedging procedure combined with a wet transfer, which enables further investigations on the potential of graphene for NEMS stuctures. This method is ideal for proof-of-concept experiments but it is not suitable for the large scale implementation of GNEMS.

A scalable approach was also validated for suspending large areas of CVD graphene over predefined cavities, both by wet and dry transfer methods. Areas of $10 \times 10\,\mu m$ were obtained, with a yield higher than 50 %, superior to any results achieved to date. Transfer printing shows a higher yield, and can be used to achieve suspended membranes up to $15 \times 15\,\mu m^2$. Graphene was patterned into stripes while still on copper, to facilitate the integration in the devices and avoid any post-processing after transfer.

These results open important manufacturing opportunities for GNEMS such as varactors, and their large scale integration for RF applications, developed in Chapter 3.

Characterization of graphene test structures obtained by different methods:

Several transfer strategies have been investigated and their potential for supported and suspended graphene has been assessed by microscopy and electrical characterization. Due to the fact that several graphene sizes are needed for the applications investigated in this thesis, from micron sizes in the RF range, up to 1 mm at THz (comparable to the wavelength), both a spatial electrical characterization at nanoscale, and a large scale averaging technique are employed by KPFM, respectively FTIR. These techniques offer a more comprehensive assessment of specific effects due to graphene than simple IV measurements.

Investigation of the effect of disorder in graphene on the electrical properties:

We have demonstrated that disorder in single and few-layer graphene has an important effect on its electrical properties due to the spatial nonuniformity. First, KPFM revealed the small-scale variability of electrical properties, which may affect the reproducibility of small-scale devices. Second, FTIR based on a focused probe beam enables the study of large-scale variability, while average sample parameters can be obtained using large spot sizes on the sample. Finally, the comparison with DC measurements indicates that an equivalent mobility definition (including the effect of cracks and ripples) is needed to correctly characterize large area samples that

might significantly differ from the mobility estimated with other methods. The results provide important insights on the influence of disorder from environmental disturbances and material imperfections on the electrical properties of graphene, showing the importance to address this issue for device applications. These results are an important guideline in the investigation of the effects of disorder on the performance of graphene quantum capacitors detailed in §4.7.

The results obtained in this chapter are instrumental for this work, considering that the exploitation of graphene's unique properties is predicated on the development of growth and integration technologies.

This chapter includes the following contributions:

- Several transfer strategies have been proposed and test structures were fabricated to assess the capabilities of transfer of supported and suspended graphene.
- Electrical properties of transferred CVD graphene and their spatial distribution on large area samples have been investigated.
- The most suitable transfer methods for the realization of RF GNEMS have been investigated experimentally.

3. Graphene NEMS Switches for Reconfigurable RF Applications

This chapter describes the first proof-of-concept and wafer-level fabrication and characterization of RF capacitive Nanoelectromechanical (NEM) capacitive switches based on graphene. Different fabrication strategies are explored and their potential to achieve large scale reliable graphene NEMS is discussed in detail. Their potential for wideband RF phase shifters for analog and digital applications is assessed trough calibrated simulations, using the developed equivalent circuit and the characterization data of fabricated NEMS switches.

3.1 Introduction

Currently there is a critical need in microwave technology for reconfigurable systems that can be fine-tuned, for applications like radar systems, telecommunications, satellite navigation, radio astronomy or heating and power applications. As discussed in Chapter 1, the "More than Moore" era requires miniaturized devices with exceedingly higher performance, functional diversity, reliability, low power consumption, and higher efficiency.

In this work, two different types of tunable capacitors for RF applications are developed: NEMS tunable capacitors described in this chapter and analog planar tunable capacitors described in Chapter 4.

The most important performance indicators for tunable technologies at high frequencies are:

- *Tuning ratio:* an indication of how much the variable parameter can be modified.
- *Loss versus frequency (bandwidth)*
- *Voltage Standing Wave Ratio (VSWR) versus frequency (mismatch)*: a measure of how efficiently radio-frequency power is transmitted from a power source, through a transmission line, into a load
- *On-off isolation (feed-through)*
- *Isolation to other circuitry (crosstalk)*
- *Power consumption*
- *Power handling*: maximum input power that does not cause irreversible breakdown or unacceptable levels of distortion at the output

- *Tuning speed*
- *Linearity*
- *Operating lifetime (reliability, mean time to failure)*

3.1.1 Overview

Tunable Elements for High Frequency Applications

The most important tunable devices are phase shifters, tunable resonators and filters. They all rely on a tunable component for device control. The most employed tunable elements are: PIN diodes, field effect transistors (FETs), semiconductor varactors, and micro-electro-mechanical (MEM) switches or varactors. Figure 3.1 depicts the typical characteristics of PIN diodes and FET switches compared to the capacitance versus voltage measurement of a MEMS capacitive switch, showing the ON and OFF working states, the approximate device cross sections and the simplified equivalent circuits for each switch.

Table 3.1 summarizes the main figures of merit for the various tunable technologies for high frequency applications. We can observe that PIN diodes are still viable in high power and high frequency applications, but the most used technology is currently the GaAs MMIC, which still

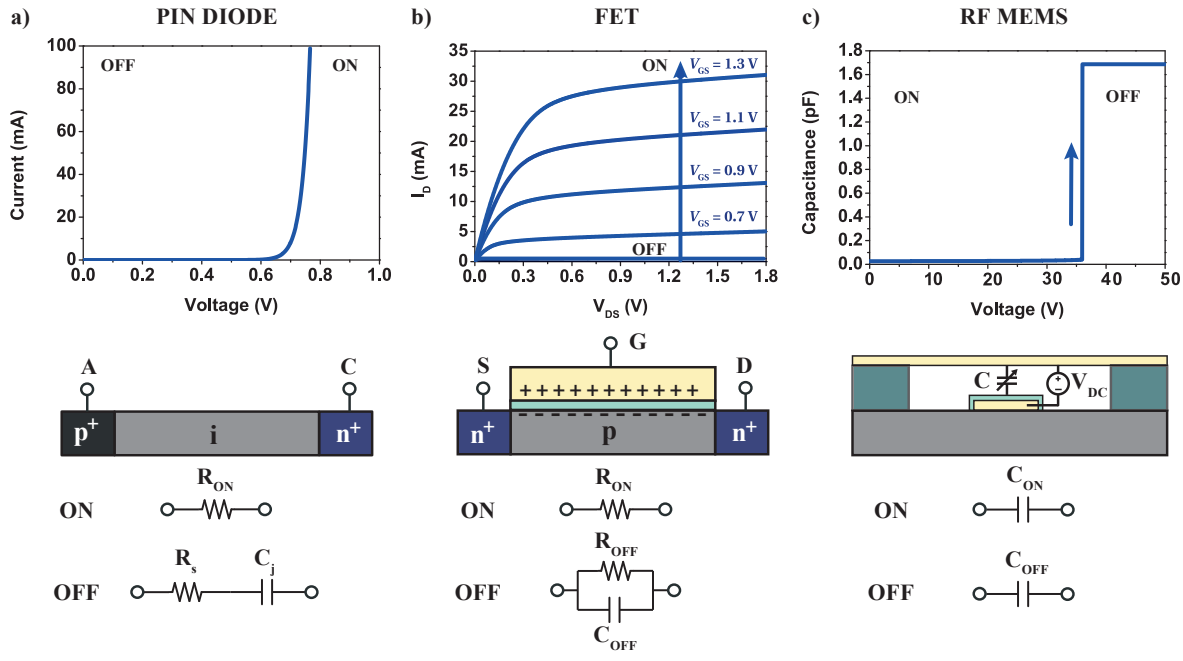


Figure 3.1: Comparison of the solid state devices (TSMC RF 0.18 µm CMOS) and MEMS tunable characteristics, structure and equivalent circuits.

Table 3.1: Figures of merit of the various RF switches [127].

Switch Technology / Parameter	PIN Diode	FET			RF MEMS
		CMOS SOI/SOS	GaAs MMIC	GaN MMIC	
Insertion Loss (dB)	0.3-1.5	0.3-2.5	0.3-2.5	0.1-1.5	0.1-5
Isolation (dB)	>30	>30	>25	>30	>40
Power Consumption	High	Low	Low	Low	Negligible
Power Handling (W)	<50	<50	<10	<100	<10
Tuning Speed	ns-µs	µs	ns-µs	ns	µs
$R_{on}xC_{off}$ (fs)	100-200	250 (0.18 µm)	224	400	20
Cost	High	Very Low/Low	High	High	Medium
Linearity* (dBm)	27-45	27-45	27-45	27-45	66-80

*third order intercept point

offers the best performance for high frequency (over a few GHz) and broadband applications at low power levels. Silicon on Sapphire (SOS) and silicon on insulator (SOI) CMOS switches are approaching GaAs MMICs performance at frequencies up to a few GHz, with significant cost and integration advantages. GaN MMIC switches are promising to replace PIN diodes for high power applications. MEMS switches are showing great promise to replace the solid state alternatives for tunable RF applications, and their main advantages are discussed in detail later in this section.

Another essential aspect for a complete comparison is the device's performance over a wide frequency range. Figure 3.2 illustrates the typical operation frequencies for the main technologies and the intervals where they have an optimal performance.

PIN diode switches usually have higher insertion loss at low frequencies due to sharing of DC

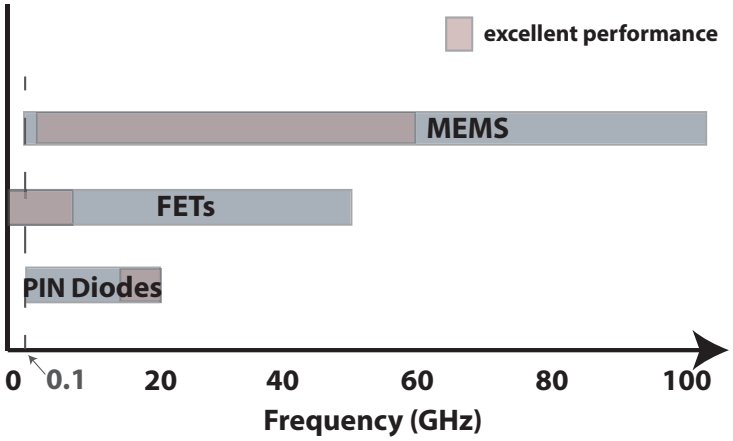


Figure 3.2: Frequency range for the operation of the main types of RF switches [127].

biasing and RF paths, while FET switches have higher insertion loss at higher frequencies due to the higher ON resistance of FETs. MEMS have been demonstrated to show an excellent performance from few hundreds MHz up to over 60 GHz and a good performance up to 100 MHz.

MEMS Technology

Micro/Nano-Electro-Mechanical Systems (MEMS/NEMS) are one of the most promising candidates to fulfil the requirements of reconfigurable electronic systems through innovative research techniques combined with technology developed for CMOS. A particular MEMS device that is beneficial to the microsystems of the future is the MEMS switch

RF MEMS tunable elements use mechanical movement to achieve a short circuit or an open circuit in an RF transmission line in the case of switches or to modulate the RF signal if they are used in the analog region. They can be designed to operate at RF-to-milimeter-wave frequencies (0.1 to 100 GHz), a much larger range than their traditional counterparts, as previously observed in Figure 3.2. They can be actuated using electrostatic, magnetostatic, piezoelectric, or thermal principles. So far, only electrostatic switches have been demonstrated at 0.1–100 GHz with high reliability and wafer-scale processing [128], and the principle is illustrated in Figure 3.3 for an RF MEMS switching device. This type of switch operates based on the amount of actuation voltage and the capacitance between the transmission line and the membrane and has a superior performance to the other types in all parameters except actuation voltage, which is very high [129].

The advantages of RF MEMS switches over solid state alternatives are:

- **Virtually Zero Power Consumption:** Electrostatic actuation requires 20–80 V but it does not consume any current, thus a very low power dissipation is achieved (10–100 nJ per switching cycle).
- **Very Low Insertion Loss at High Frequencies**: RF MEMS switches have an insertion loss of -0.1 dB up to 40 GHz.
- **Linearity:** MEMS switches are very linear devices and, therefore, have very low intermodulation products. Their performance is around 30 dB better than PIN or FET switches.
- **Ability to Operate in Harsh Environments:** MEMS can operate in extreme conditions, such as high temperatures and high Ionizing Radiation that CMOS alternatives cannot withstand.

MEMS are also CMOS compatible, thus being easily integrated with CMOS circuits on the same chip.

However, RF MEMS have a series of drawbacks, such as:

- **High-Voltage Drive:** Electrostatic MEMS switches require 20–80 V for reliable operation, needing a voltage up-converter circuit, so even if the actuation power is virtually zero, a high drive power is necessary for their operation.
- **Low Speed:** The switching speed of most MEMS switches is around 2–40 µs which is not sufficient for most applications (communications, radar systems).
- **Low Power Handling:** Most MEMS switches are limited to 20–50 mW. For high power applications, switches that can handle 0.2–10 W are required.
- **Reliability:** The reliability of mature MEMS switches is 0.1–10 billion cycles, but 20–200 billion cycles are required for many systems. The long-term reliability (years) is an important issue as well, but it has not been investigated to date.
- **Packaging:** MEMS switches need to be packaged in inert atmospheres (nitrogen, argon, etc.) and in very low humidity, in hermetic or near-hermetic seals.
- **Cost:** While MEMS switches have the potential of low cost manufacturing, the packaging costs and the high-voltage drive circuits significantly increase the costs.

RF MEMS consist of three components [127, 128, 130], that can be identified in Figure 3.3 for a MEMS Switch loaded on a CPW:

- The substrate, for which high resistivity silicon or porous silicon [131–133] is used due to the high loss of normal silicon at the high frequencies required for IC circuit integration.
- A transmission line, used for transferring the RF signals from the input to the output ports. For practical reasons (the pads are on one side of the substrate, lower loss at high frequencies), we used a coplanar wave guide (CPW) for this purpose.
- A cantilever or membrane, which are the movable parts for connecting and disconnecting the signal line.

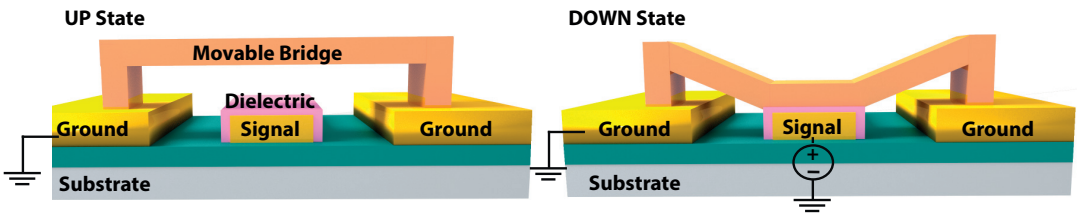


Figure 3.3: Configuration and biasing of an electrostatically actuated capacitive Shunt Switch implemented on a CPW transmission line.

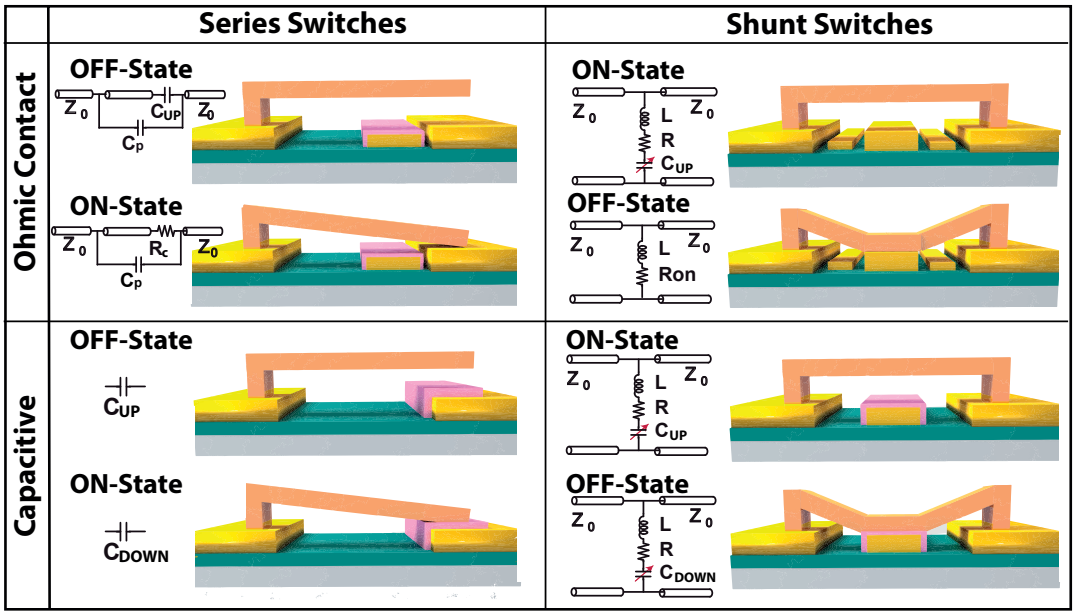


Figure 3.4: Classification of MEMS switches by contact type and electrical connection.

Depending on the operating principle, namely on the tunable element, MEMS switches are divided in ohmic and capacitive switches, having a metal-to-metal or, respectively, a capacitive contact. With regard to the transmission line, a MEMS switch can be placed either in a series or a parallel (shunt) configuration. The schematics of the various types of switches are illustrated in Figure 3.4.

The MEM series contact switches perform a short or open in an electrical path, typically with metal-to-metal contacts and hence show good insertion loss and exhibit excellent linearity. They have been validated in a range of frequencies ranging from DC up to 60 GHz. They are suitable for applications that demand the lowest attainable insertion loss. Capacitive MEMS switches are more suitable for high frequency applications (10-100 GHz), especially in shunt configuration, where a high isolation and a higher reliability are required. The operation frequency ranges of the possible MEM switch configurations are summarized in Figure 3.5.

In this thesis, electrostatic shunt capacitive MEMS switches have been developed. RF MEMS tunable capacitors are mostly used as switches, in digital applications requiring 2 states, ON and OFF, corresponding to the UP and DOWN states of the switch. However, its advantages compared to solid state technologies are also valid in the case of analog tuning of the MEMS, deflecting the membrane only until the instability point, reason why MEMS in the analog regime have been widely investigated as well [134–139].

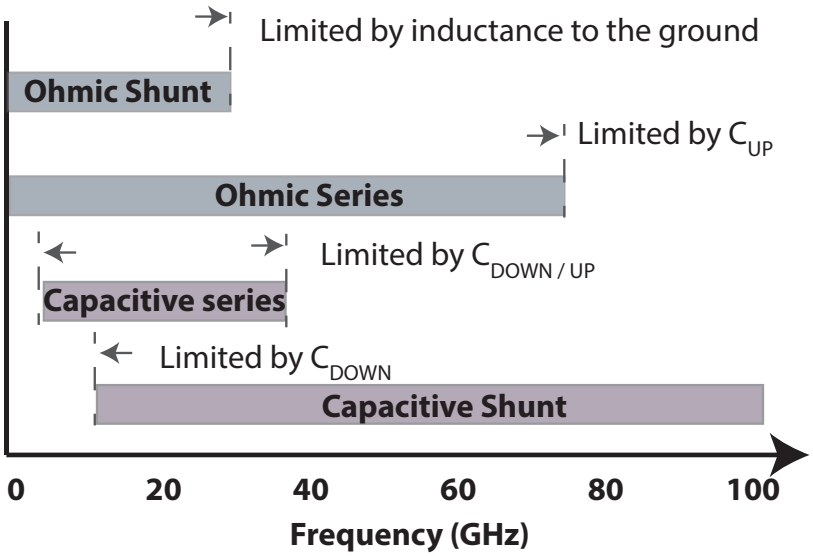


Figure 3.5: Classifications of RF MEMS switches, frequency operation region based on the equivalent circuits shown in Figure 3.4.

Graphene NEMS Technology

Carbon switches have a beam thickness in the range of a few nanometers, therefore they are mostly named NEMS switches. Due to its exceptional mechanical properties and low mass, graphene has been considered a promising candidate for NEMS. Most of the applications using graphene in a NEMS configuration are resonators and pressure sensors, as summarized in Table 3.2, with a fairly good performance. The scope of the table is to review the fabrication techniques used to realize the graphene-based MEMS and suspended graphene test structures. Suspending graphene is the major challenge this type of devices needs to overcome. In general, graphene-based devices are processed using the mature CMOS technology, used for top-down MEMS fabrication, in order to ease the integration of such devices in circuits, on the same chip. However, the major difference is the graphene manipulation, adding a degree of complexity in terms of processing and releasing it without affecting its extraordinary properties. The main limitation on the road toward integration of graphene with silicon is the large-scale production of defect-free graphene and its placement on the appropriate substrate, as previously discussed in Chapter 2. Having discussed the main synthesis and transfer methodologies, and the yielded results, we now focus on using these techniques for NEMS manufacturing.

The first suspended graphene sheets were produced using mechanical exfoliation. Exfoliated single layer graphene (SLG) flakes were suspended on a predefined cavity in SiO_2, resulting in a doubly clamped beam [53]. Mechanical exfoliation was intensively used to produce mechanical

resonators and other types of devices based on graphene because it yields very clean graphene without the need for lithography. Today, exfoliation techniques enable the production of very large suspended graphene sheets up to 50 or even 100 µm. However, the major drawback is that the technique is not scalable, yielding a small number of devices. It is mostly suitable for proof-of-concept experiments.

A more scalable option for graphene device production would be growing a large-area sheet of graphene on a substrate and subsequently processing it to create devices. Ideally, graphene should be processed on the surface on which it was grown. For example, Shivaraman et al. [140] grow the graphene epitaxially on silicon carbide (SiC) and subsequently etch the underlying layer of SiC to release the membranes. However, the types of substrates that can grow graphene are not suitable for devices or are not compatible with the standard technology. A lot of research is currently directed towards growth of graphene on CMOS-compatible substrates, but this approach is still far from practical realization.

The most employed large scale fabrication method is growing large-area graphene on transition metals by CVD and then transferring it to the desired substrate. The suspended graphene is achieved either by a sacrificial etch of the underlying sacrificial layer [54] or by transferring the graphene directly on predefined cavities [107, 141–143]. This method was also used to achieve few-layer graphene (FLG) resonators out of reduced graphene oxide transferred to a pre-patterned substrate [144]. Suspended graphene has proven very useful for the graphene community, for basic studies of its properties as well. Tombros et al. showed that suspended graphene could be used to achieve ultrahigh electron mobility, up to $600\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [145].

The resonance frequencies are also indicated in Table 3.2, where applicable. They are of interest for our case as they offer an indication of the level of the switching time of such configurations, which can be extracted based on the Muldavin and Rebeiz model [146]: $t_\mathrm{s} = 3.67(V_\mathrm{PI}/V_\mathrm{OP}\omega_0)$, where V_PI is the pull-in or actuation voltage, V_OP is the operation voltage and ω_0 is the resonant frequency.

While we do not have information on the pull-in voltage, we can roughly estimate switching times in the range of tens of ns, assuming a $V_\mathrm{PI} < 10\,\mathrm{V}$.

Table 3.2: SOA of Graphene NEMS.

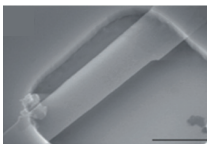
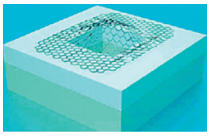
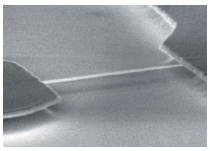
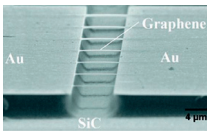
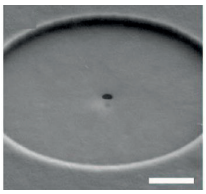
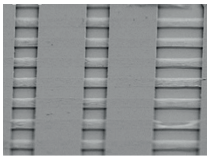
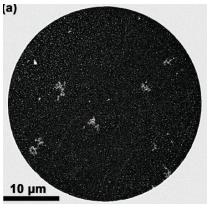
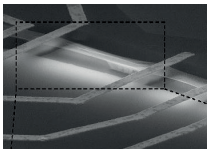
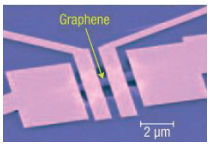
Ref.	Config.	Graphene	Fabrication	Performance	Area
 [53]	Resonator Double clamped	Exfoliated FLG 15 nm	Transfer on SiO_2 trenches. Gate: Si substrate	$f_0 = 42$ MHz Q = 210	L=5 µm W=2 µm Gap=0.5 µm
		SLG 0.3nm		$f_0 = 70.5$ MHz Q = 78	L = 1.1 µm W = 2 µm
		FLG 20nm		Q = 100@300K Q = 1800@50 K	L = 5 µm W = 2 µm
 [147]	Pressure sensor & Separation membrane	Exfoliated SLG 1.5 nm	Transfer on cavity in SiO_2.	$E \approx 1$TPa $f_0 = 66$ MHz Q = 25	L = 4.75 µm W=4.75 µm Gap = 380 nm
 [148]	Resonator Double clamped	Exfoliated SLG	Sacrifical etching of SiO_2 in BOE + CPD	G = 0.8mS (Vg = −7 V) $f_0 = 65$ MHz Q = 125(300 K)	L = 1.1 µm W = 3 µm
				$f_0 = 120$ MHz (125 K) Q = 14000 (5 K)	L = 0.5-2 µm W = 0.2-2 µm
 [148]	Resonator Double clamped	Epitaxial graphene (SiC)	Sacrificial etch of SiC in KOH	$f_0 = 85$ MHz L= 3 µm $f_0 = 8$ MHz	Gap=1-8 µm L=3-20 µm w=0.5-3.5 µm
 [144]	Drum resonator	GO exfoliation, isolation, resuspension 6-15 nm	Custom spincasting on cavities in SiO_2	$E > 185$ GPa 5 N/m Q=1500 $f_0 = 20 - 60$ MHz ($T > RT$)	$D : 5 - 7.25$ µm Gap=250 nm

Table 3.2 – continued from previous page

Ref.	Config.	Release	Fabrication	Performance	Area
 [116]	Resonators Double clamped Drum resonator	CVD	Stripes transferred on cavities in SiO_2 Transfer on suspended Si_3N_4 membrane with holes	$f_0 = 9.77$ MHz Q = 52 $f_0 = 40$ MHz(100 K) Q> 9000(9 K) μ =1000-4000 $cm^2\,V^{-1}\,s^{-1}$	L = 2 µm W = 3 µm G = 285 nm
 [141]	Drum resonators	CVD SLG	Transfer on holes in suspended Si_3N_4	f_0 = 1-25 MHz $2400 > Q > 100$	D = 2–30 µm
 [145]	Hall bar structure	Exfoliated graphene	LOR-sacrificial layer Exposed in EBL Dev. in ethyllactate N_2 dry	$\mu >$ $6 \times 10^5\,cm^2\,V^{-1}\,s$ at n = $5 \times 10^9\,cm^{-2}$ (77 K)	L=10 µm w=1 µm Gap=1.4 µm
 [149]	MEMS voltage controlled oscillator	CVD	Sacrificial etching of SiO_2 in BOE CMP oxide for adhesion	FM signal ≈ 100 MHz	D = 3 µm Gap = 200 nm
 [150]	Hall bar	SLG exfoliated	Transfer on cavities in SiO_2	$n = 4 \times 10^9\,cm^{-2}$ μ = 120000 $cm^2\,V^{-1}\,s^{-1}$ (100 K)	L=0.5 µm W=1.4 µm

Graphene NEMS Switches

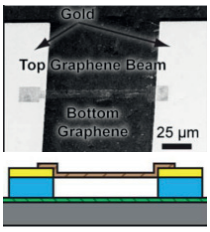
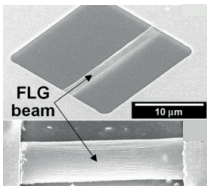
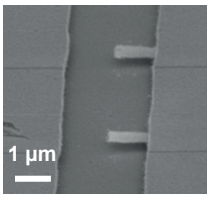
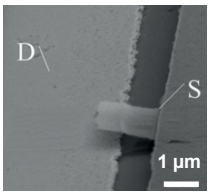
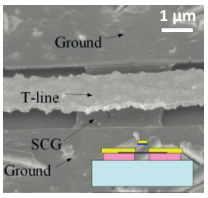
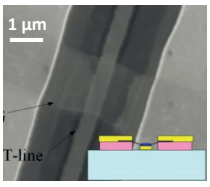
Even though graphene experienced an important progress in the area of nanomechanics very few works develop graphene NEMS switches and they are summarized in Table 3.3, emphasizing the switch type, graphene release strategy and performance. All the switches developed to date are ohmic switches, fabricated by releasing the graphene membrane by a sacrificial wet etch of the underlying SiO_2 layer in buffered hydrofluoric acid (BHF). The first graphene switch was developped in 2009 by Milaninia et al. [55], using 3 nm thick multilayer CVD graphene to realize an ohmic DC switch, with graphene as back gate. The switch is actuated at 5 V and the performance was limited by the contact resistance between the two graphene sheets, which was attributed to the nonuniform surface of the CVD-grown graphene. The device experiences mechanical failure by tearing of the membrane after 1–3 cycles.

Kim et al. [151] reported an ohmic switch, using the silicon substrate as a back gate, coated by 3 nm of Al_2O_3 by atomic layer deposition, in order to prevent possible welding of the FLG beam onto Si during the switching operations. To facilitate the release process, an amorphous silicon (a-Si) layer is deposited on the graphene beam, to offer support, preventing its stiction, during the wet release. It is subsequently removed in SF_6 plasma. However, it was reported that this method induced notable defects in graphene. Here, it is noted that the V_{PI} is not consistent for all actuation cycles. This can be due to the fact that the physical contact point and/or the air-gap height are not identical among successive switching operations or when the switch is ON, the Joule heating can cause ambient molecular species to adsorb/desorb onto graphene and thus modify the mechanical and surface properties of the FLG beam as reported in [52].

Graphene cantilever switches have also been demonstrated [152], in 2 terminal (2-T) and 3 terminal (3-T) configurations. The contact of 12 out of 19 cantilevers is broken after the bias is turned off and they recover to an UP state. The main failure mechanism in this case is stiction to the gate electrode.

To date, only one report experimentally investigated the RF properties of ohmic graphene switches, up to 100 GHz with a very good isolation. They operate at very low voltage, of 1 V, for 5000 consecutive cycles. The superior reliability is due to using single crystalline CVD graphene.

Table 3.3: SOA of Graphene NEM Switches.

Ref.	Config.	Release	Size (μm)	V_{pi} (V)	t_s (ns)	Performance
 [55]	2LG CVD(3 nm); Double Clamped DC Ohmic Gate: Graphene	sacrificial SiO_2 BHF + CPD	g =0.5 L = 60 W = 3	4.5	N.A.	I_{ON}/I_{OFF}=10 R=1k$\Omega/\square$ Rc=200kΩ
 [151]	MLG CVD(2.5 nm) Double Clamped DC Ohmic Gate: Si substrate	sacrificial 100 nmSiO_2 BHF +KOH + CPD	g =0.15 L = 20 W = 2	4.5	40[a]	I_{ON}/I_{OFF}=10^3 < 7 mV/dec 6 cycles
 [152]	MLG Exf.(4 nm); Cantilever 2-T DC Ohmic MLG (2.5 nm)	sacrificial a-Si support SiO_2 BHF + CPD	g =0.3 L = 1 W = 4 W = 2.5 W = 2	$\backsim$ 4.9 $\backsim$6 $\backsim$11	25 (10 V)	I_{ON}/I_{OFF}=3.5
 [152]	” Cantilever 3-T Gate: Si substrate		W = 2	8	N.A	I(8 V)=28 µA (V_{DS} = 0.5 V) I(0 V)=0 A
 [153]	CVD single- crystalline Double Clamped RF Ohmic Top Gate: Suspended Au	sacrificial SiO_2 BHF +CPD	g =N.A L $\backsim$ 3 W $\backsim$2.5	1	N.A.	I_{ON}/I_{OFF} >1500 S_{21-UP}=−6 dB S_{21-D}=−30 dB @ 40 dB
 [153]	 Back Gate: Au	” Stiction				

3.1.2 Motivation

This work proposes the realization and optimisation of FLG graphene NEMS switches for reconfigurable RF application. As we have discussed in the previous sections, MEMS have proven to be ideal candidates for tunable applications up to 100 GHz, however some of their major drawbacks are the very high actuation voltage and slow switching time. In order to overcome these issues, the moving parts of the MEMS need to be miniaturized and thinned. In general, three-dimensional (3D) materials, such as metals or poly-Si, which are normally used for the active part of MEMS/NEMS devices, become brittle when scaled down to nanometers. For this reson, using graphene instead of metal for the movable part of the MEMS seems like an ideal solution due to its outstanding mechanical properties, at the nanoscale, like high mechanical stiffness, high strength and low mass [55, 154]. These qualities make graphene NEMS achieve significantly faster switching than traditional metal MEMS, making them more promising for fast scanning applications.

On top of its excellent electrical, mechanical and thermal properties, graphene is also hydrophobic which could minimize the stiction probability to the back electrode, which is one of the main causes of failure in traditional MEMS.

First experimental data shows that FLG graphene can be successfully used in NEM switching structures and enables very fast operation, down to 25 ns, opening a new design space for ohmic NEMS switches. However, graphene based capacitive switches have never been investigated. This type of switches offer a more reliable performance, avoiding a direct contact between graphene and the metal transmission line, on top of the advantage of higher isolation, enabling their operation at higher frequencies (Figure 3.5).

In this work we investigate the potential of SLG and FLG graphene capacitive shunt NEMS switches for reconfigurable RF applications, area which is not yet explored. We develop, optimize and characterize the devices at GHz frequencies and assess their potential for future graphene NEMS based applications.

3.2 Principle

Figure 3.6 schematically shows the proposed graphene-based RF NEMS capacitive switch. It consists of a graphene membrane suspended over the central conductor of a CPW and clamped by the ground planes of the CPW. The central and ground conductors are high-conductivity metals (such as gold), placed on a low loss substrate (such as high resistivity silicon). A dielectric layer is used to isolate the switch from the CPW center conductor in DC. When the membrane is in the UP state, the RF signal can propagate trough the central conductor, and

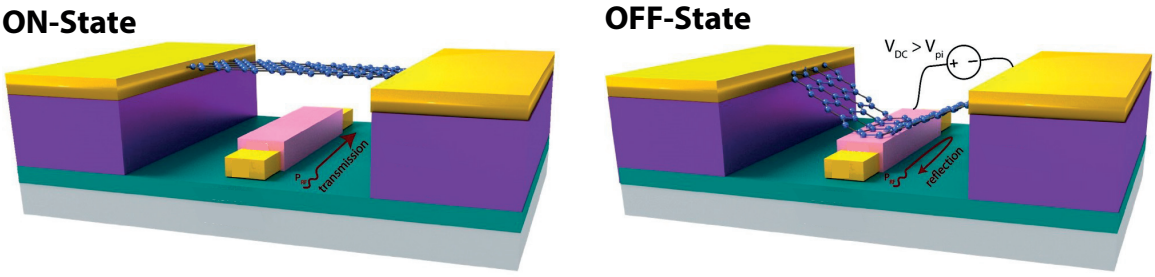


Figure 3.6: Schematic rendering of a graphene based RF NEMS capacitive shunt switch. Left: signal transmitted with the switch in UP state; right: signal reflected with the switch in DOWN state.

the switch is ON. When a DC voltage is applied across the membrane and the central conductor (superimposed to the RF signal), the electrostatic force causes the membrane to snap down on the dielectric surface, forming a low-impedance mainly capacitive RF path to the ground. The RF signal is reflected in this case, turning the switch OFF.

The operation principle of a RF MEMS is illustrated schematically in Figure 3.7, emphasizing the two operation regimes: analog and digital. For a classic design the analog tunability is 1.5, but this has been significantly improved to surpass the performance of the solid state alternatives and it is linear before approaching the instability point as indicated.

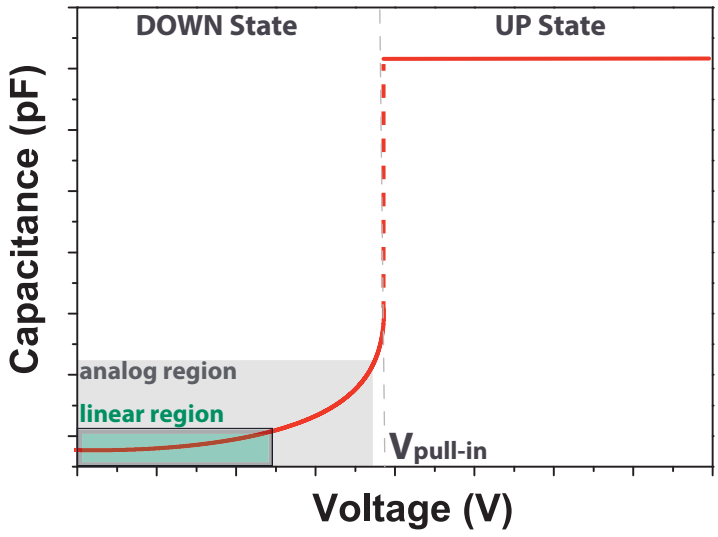


Figure 3.7: Characteristic of a capacitive RF MEMS indicating the analog and digital regimes of operation.

3.3 Graphene NEMS Model

3.3.1 DC Model

The mechanical model of an RF MEMS capacitive switch is illustrated in Figure 3.8. The electrostatic force is given by the DC source and the capacitor between the bottom conductor and the membrane. The elastic force is modelled as a spring and it depends on the shape, material (stiffness and tension) and size of the membrane.

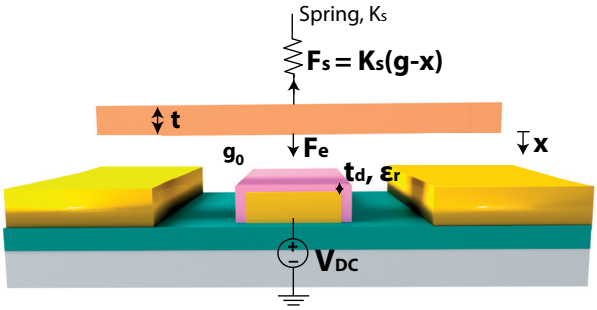


Figure 3.8: Schematic view of a general RF MEMS capacitive shunt switch.

The DC bias, V_{DC} starts pulling the membrane towards the bottom electrode, decreasing the original air gap (g_0) resulting in an increase of the capacitance value and the electrostatic force (F_{e}) on the membrane. At a high enough voltage, when the gap height corresponds to a 2/3 of g_0, the mechanical system reaches an instability point, causing the membrane to suddenly collapse onto the bottom electrode. This voltage is the pull-in voltage and it is given by [155]:

$$V_{\mathrm{PI}} = \sqrt{\frac{8k}{27\epsilon_0 W w} g_0^3} \tag{3.1}$$

where k is the effective spring constant of the membrane, W is the CPW center conductor width, w is the membrane's width and g_0 is the height of the suspended membrane above the dielectric layer (which is over the central conductor). According to continuum mechanics, the effective spring constant of the doubly clamped membrane with load applied at the center of the membrane and under axial tension, is given by [22, 156]:

$$k = 32Ew(t/L)^3 + 17T/L \tag{3.2}$$

where E is Young's modulus, T is the tension in the beam, and t and L are the thickness and length of the membrane, respectively. Reducing k via reduction in the thickness of the

membrane t, will allow us to reduce the pull-in voltage. The switching time t_s can be calculated as:

$$t_s = 3.67\frac{V_{PI}}{V_s\omega_0} \qquad V_s \approx 1.3V_{PI} \qquad \omega_0 = \sqrt{\frac{k}{m_{eff}}} \qquad m_{eff} = 0.735Lwt\rho$$

where $m_{eff} = 0.735Lwt\rho$ where ρ is the graphene mass density.

These equations show, in particular, that using graphene as the material for membranes in RF NEMS switches has the great benefit of a reduced pull-in voltage and switching time due to its ultra-low thickness.

3.3.2 High Frequency Conductivity of Graphene

The complex conductivity of graphene, as shown in Section 1.2.2, Equation (1.10), depends on graphene intraband and interband contributions [157]. However, since the operation of the device is far below the THz regime, the interband contributions are negligible and graphene conductivity can be represented as [158]:

$$\sigma(\omega, \mu_c, \Gamma, T) \approx -j\frac{q_e^2 k_B T}{\pi\hbar^2(\omega - j\Gamma)}\left(\frac{|\mu_c|}{k_B T} + 2ln\left(e^{-\frac{|\mu_c|}{k_B T}} + 1\right)\right) \tag{3.3}$$

where Γ is the scattering rate (inverse of the relaxation time τ, $\Gamma = 1/\tau$), $T = 300\,\mathrm{K}$ is the temperature, $\hbar$ is the reduced Planck's constant, k_B is Boltzmann's constant and μ_c is the chemical potential. Unlike metal membrane switches where the conductivity of the membrane remains the same in both the up- and down-states, in the case of graphene it is important to note that the conductivity of graphene membrane changes due to the parameters Γ and μ_c, which take different values in these two states.

3.3.3 High Frequency Electrical Equivalent Model

Figure 3.9 shows the equivalent circuit model of the graphene RF NEMS shunt switch. The device is modelled by C, L, and R components. L represents the inductance of the switch, R shows the insertion loss, and C, which is the dominating parameter, represents the capacitance between the bridge and the transmission line. In the circuit model of metal membrane MEMS, C is the only variable component. However in the present case, R is also variable due to the change in graphene resistivity in UP- and DOWN-state positions. The graphene inductance is negligible.

The effect of graphene quantum capacitance is neglected because its impact is negligible for the values of V_{DC} and the dielectric thickness applicable for the RF NEMS switches.

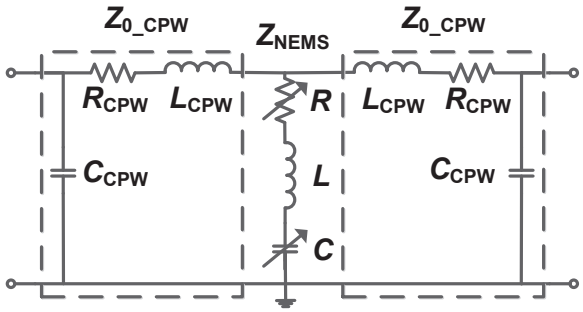


Figure 3.9: Equivalent circuit model of a graphene-based NEMS capacitive switch.

The effect of contact resistance between graphene and ground conductor is also neglected as its effect is almost negligible at higher frequencies [154].

3.4 Design

The main trade-offs for the design parameter optimization are investigated in terms of the GNEMS figures of merit.

3.4.1 DC Performance

Actuation Voltage

The actuation voltage V_{PI} of graphene NEMS capacitive switches is highly dependent on the following parameters:

- height of the gap g_0 between graphene membrane and bottom electrode ($V_{\mathrm{PI}} \propto g_0^{1.5}$);
- length L of the graphene membrane and bottom electrode ($V_{\mathrm{PI}} \propto L^{-1.5}$);
- the thickness of graphene membrane t_{g} ($V_{\mathrm{PI}} \propto t_g^{1.5}$).
- spring constant k ($V_{\mathrm{PI}} \propto k^{1/2}$)

The results on the dependence of V_{PI} on g_0, w and t_{g} for devices with different graphene membrane lengths L are summarized in Figure 3.10. Three different lenghts are considered in order to cover the full range of trade-offs from fabrication yield to RF performance. V_{PI} decreases as the beam length increases for a constant beam width, which is consistent with the model proposed by Pamidighantam et al. and it is attributed to lowering of the bending stiffness [159]. In order to minimise the actuation voltage, a low gap, small graphene width and a low thickness are desired. However, a high thickness t_{g} of the graphene membrane will reduce

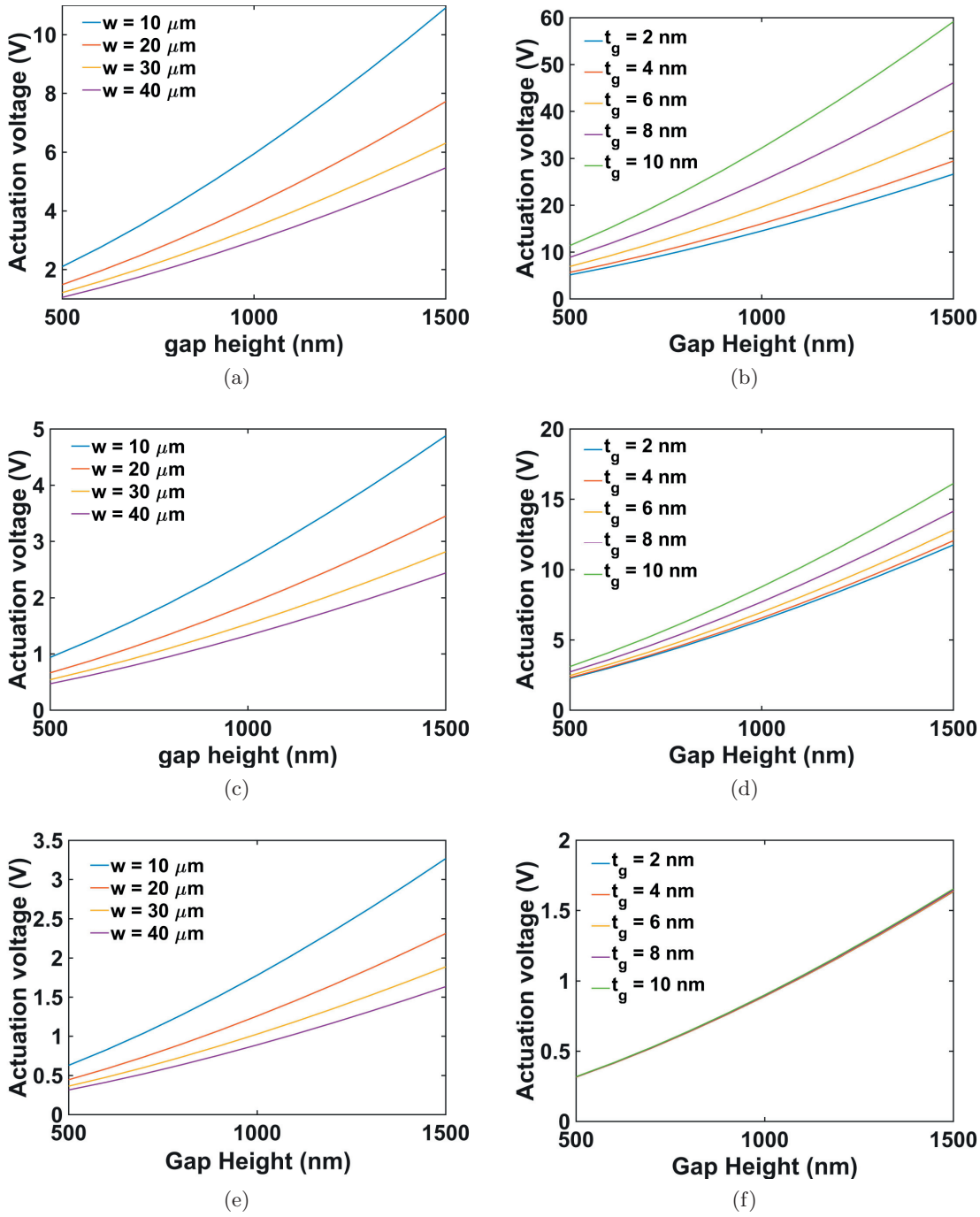


Figure 3.10: Actuation voltage versus gap size for different geometrical parameters of GNEMS: a) L = 7 µm, varying membrane width, w and b) membrane thickness, t_g; c) L = 15 µm, varying membrane width, w and d) membrane thickness, t_g; e) L = 90 µm, varying membrane width, w and f) membrane thickness, t_g.

the sheet resistance improving the RF performance. MLG is more conductive than SLG, thus a trade-off between conductivity and actuation voltage is necessary.

Another essential trade-off to be considered is the fabrication feasibility. In order to increase the yield of suspending graphene membranes, both the gap g_0 and the length L have to be scaled in a way that would increase V_{PI} (higher g_0, smaller L). A high V_{PI} would prevent the use of very thin dielectric layers, and therefore decrease the capacitance ratio, which is detrimental for the RF performance.

In addition to these parameters, residual stress accumulated during graphene growth and processing (discussed in §2.1.2, §2.2.2, §2.2.4) has an important effect on k, resulting in a high actuation voltage.

Switching Time

The switching time depends on the geometrical parameters of the graphene beam and of the material properties, mainly beam tension. The air gap does not play a role in the actuation speed. Figure 3.11 shows an important improvement in switching time with the increase of the beam tension.

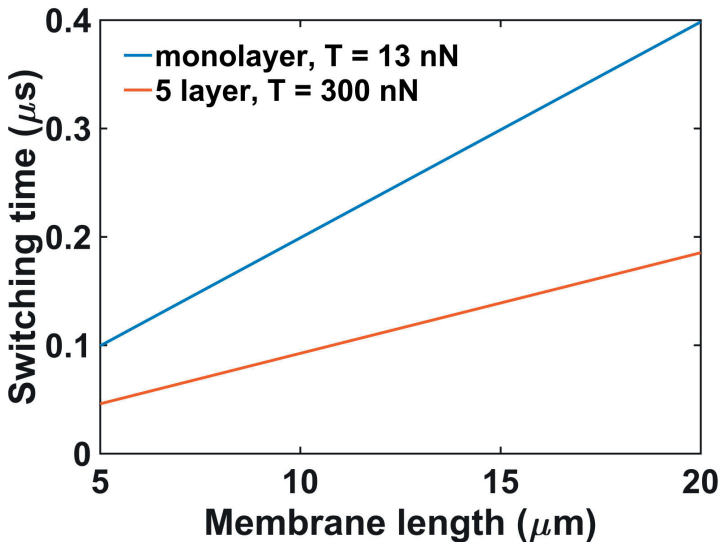


Figure 3.11: Switching time versus geometrical parameters of the GNEMS.

3.4.2 RF Performance

Substrate

It is essential to pick a substrate that has low losses in RF. High resistivity ($> 10\,\mathrm{k\Omega\,cm}$) Si wafers are used, as standard silicon is not suitable. A passivation layer of a-Si is added to prevent the accumulation of charges at the interface with the oxide as it was demonstrated in [160]. The dielectric insulation layer is chosen to be Si_3N_4 due to its excellent dielectric properties and compatibility with the following fabrication steps.

CPW Size

The impact of the geometric parameters of the CPW and graphene on the RF performance of GNEMS was thoroughly investigated by Sharma et al. through HFSS simulations and is presented in [154]. Influence of the CPW width, W on the main performance metrics of the graphene switch, namely the insertion loss and isolation are discussed.

Increasing W increases the overlap area between graphene membrane and central conductor, therefore the capacitive coupling is improved, allowing to reach higher isolation values with still acceptable levels of insertion loss up to 30 GHz.

However, increasing the CPW size means a longer graphene membrane has to be suspended, which makes the fabrication more challenging. This is the most important performance trade-off in the case of GNEMS, and needs to be chosen carefully to ensure the process' feasibility and good performance.

Graphene Size and Resistance

The insertion loss $S_{21-\mathrm{UP}}$ is not a concern, since the decreased overlap area between membrane and bottom electrode, combined with the increased gap would result in a lower parasitic capacitance C_{UP} in the UP state of the switch. On the other hand, the device geometry has to be carefully optimized in order to have a good isolation $S_{21-\mathrm{DOWN}}$ at high frequency in the DOWN state. With the constraints on L and g_0 set to increase the membrane suspension yield, the graphene membrane width W is identified as the key parameter for the performance of the capacitive switch. The simulation results in [154] show the improvement in isolation with increasing W. First, the increased overlap area with the bottom electrode increases the down state capacitance C_{DOWN}. Second, and more important at high frequency, the series resistance is decreased, improving the coupling from signal to ground. Devices with lengths L ranging from $7\,\mu\mathrm{m}$ to $90\,\mu\mathrm{m}$, widths ranging from $w = 10\,\mu\mathrm{m}$ to $40\,\mu\mathrm{m}$ and gaps g_0 ranging

from 500 nm to 2 µm are designed. Isolation levels better than −10 dB are achievable for all the designed devices with a graphene width $W = 40\,\mu m$ and sheet resistivity $R_{\square} \approx 100\,\Omega/\square$.

Dielectric layer

A thin dielectric layer (t_d) on the central conductor is necessary to achieve a high capacitance ratio (C_r). The importance of this parameter manifests itself not only in achieving high RF isolation performance by increasing the down-state capacitance but also in avoiding excessive DC dielectric charge currents, which is directly related to the switch lifetime. For the same reasons, it is also desirable to use a high permittivity dielectric to increase the C_r while maintaining good isolation after cycling tests. Switching voltages across a thin dielectric layer induce trapped charges into the dielectric by tunneling effect. In addition, dielectric charging is the main reason for lifetime limitation. The dielectric layer should also be able to withstand high electrical field strengths without dielectric breakdown. Moreover, it should be thin enough to achieve high C_r but thick enough to avoid pin-holes.

In Figure 3.12, a few dielectrics are evaluated by HFSS simulations to assess their effect on the switch isolation. Figure 3.12.a shows the effect on isolation of the proposed dielectrics, with the thicknesses indicated in the legend chosen to allow applying 12 V. Figure 3.12.b shows the performance for the same dielectric thickness, to make a direct assessment of the influence of the dielectric constant on the performance.

HfO_2, a high-k dielectric, is chosen in this work, for two main reasons. First, high-k dielectrics are known to reduce the impurity scattering [161] in graphene. Second, its higher dielectric constant ($\epsilon_r = 25$) and a low loss tangent ($\tan\delta = 0.0098$) [162] lead to a better switch performance at high frequency, as observed in Figure 3.12. Furthermore, it is noted that the maximum V_{bias} that can be applied without causing dielectric breakdown of HfO_2 is 0.85 V/nm x t_d [163]. In this case, for t_d=30 nm, the maximum V_{bias} which can be applied is 25 V, which is much larger than the maximum voltage needed for actuation as shown later.

The main performance trade-offs between the DC and RF performance are summarized in Table 3.4.

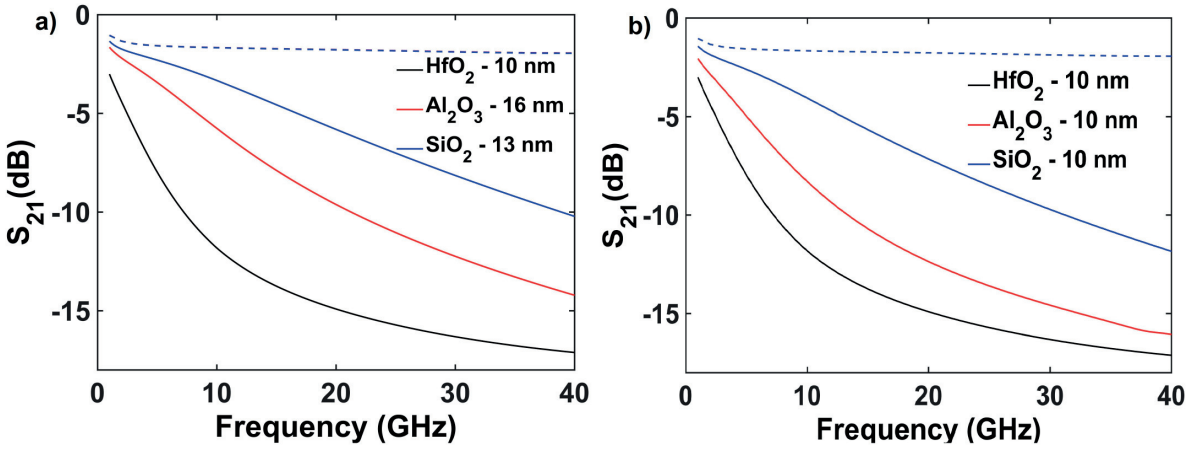


Figure 3.12: Influence of the dielectric type on the S-parameters. Oxides of: a) different thicknesses to have a BV higher than 12 V; b) the same thickness.

Table 3.4: Effects of Physical Parameters on the DC and RF Properties of the GNEMS.

Phvsical Parameters	DC Voltage		RF Performance	
	Actuation Voltage	Switching Time	Insertion Loss	Isolation
Reduce gap, g	Reduce	No effect	Reduce	No effect
Increase length, L	Reduce	Increase	Reduce	Reduce
Increase width, w	Reduce	Increase	Increase	Increase
Reduce spring, K	Reduce	Reduce	No effect	No effect

3.5 Graphene NEMS—Graphene Release by Sacrificial Etching

3.5.1 Fabrication

MLG obtained by CVD on Ni films, as described in Section 2.1.2 is used to fabricate GNEMS. Multilayer graphene is chosen instead of monolayer as it has a significantly lower resistance, improving the device performance [154], as well as a higher stiffness, making it easier to suspend. The device fabrication consists in releasing a graphene membrane, clamped by the metal ground planes of the CPW on top of the back electrode, representing the signal line of the CPW, by under-etching a sacrificial layer. Figure 3.13 shows the main steps of the fabrication process. 500 nm of low stress Si_3N_4 are deposited by LPCVD on a high resistivity silicon substrate ($>10\,k\Omega\,cm$) (Figure 3.13a). The back electrode is defined by a Pt/Cr (200/10 nm) lift-off process. Then, 30 nm of HfO_2 are deposited by atomic layer deposition as insulation layer for graphene in the down state (Figure 3.13b). Subsequently, low temperature SiO_2 (LTO) is

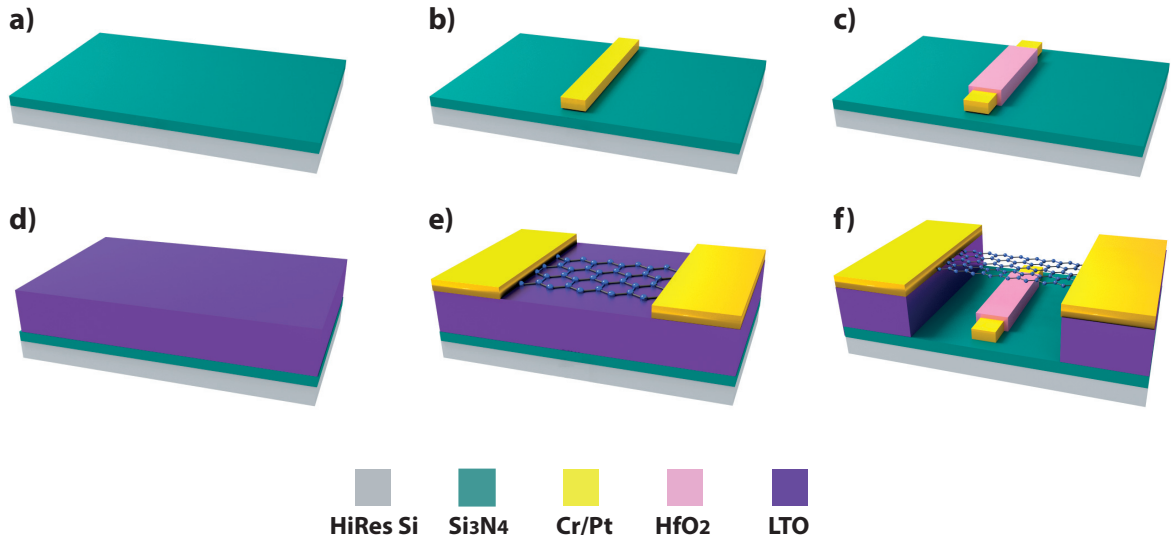


Figure 3.13: Main steps of the fabrication process for graphene NEMS with graphene release by sacrificial etching.

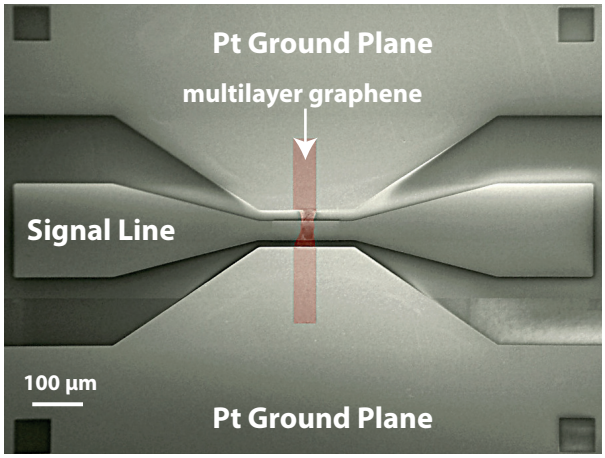


Figure 3.14: SEM of the graphene GNEMS with graphene release by sacrificial etching.

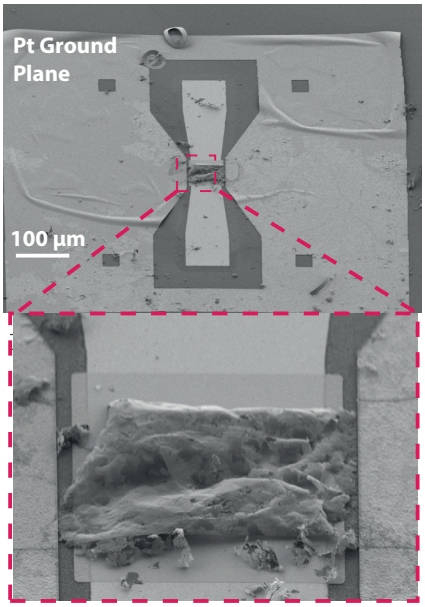
deposited by LPCVD as sacrificial layer (Figure 3.13c). An area of 1 cm^2 of multilayer graphene is deposited on top by wet transfer using PMMA as transfer polymer (as described in 2.2.2), then patterned by one minute of etching in oxigen plasma (Figure 3.13d). Then the Pt/Cr top contacts constituting the ground planes of the CPW are defined by lift-off (Figure 3.13e). The critical step is the membrane release (Figure 3.13f), done by sacrificial etching of the LTO in buffered oxide etch, followed by critical point drying (CPD) in order to avoid membrane stiction.

A top view of the final device is shown in Figure 3.14. It can be observed that one edge of the membrane is bent or broken due to its very large size.

Fabrication Challenges

The main challenges, due to graphene manipulation and processing are discussed next.

♦ Bad Metal Adhesion



Cause:

–CVD FLG non-uniformity.

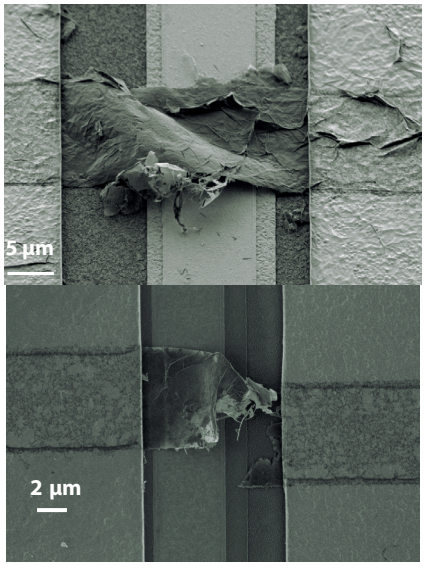
–Transferred graphene is not perfectly flat on the substrate causing ripples and folds (§2.3.1).

–Polymers used for transfer as well as subsequent lithography cannot be completely removed from graphene.

Consequences:

–Device fabrication failure: bad metal adhesion leading to lifted pads during lift-off, leading to membrane strain and rupture.

♦ Strained Graphene Membranes



Cause:

–Residual strain is accumulated during growth, transfer and post-processing.

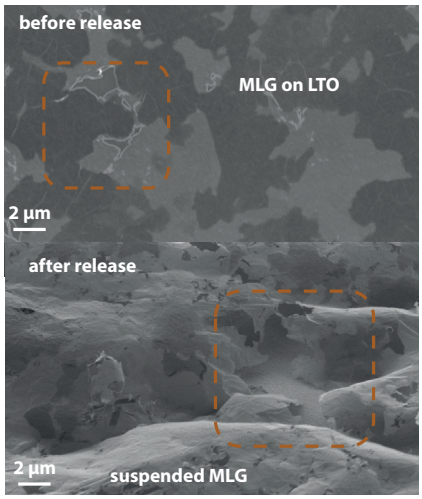
–The sacrificial etching of LTO and CPD also induces high strain in the graphene membranes leading to membrane buckling and tearing.

Consequences:

–Increase actuation voltage.

–Short device lifetime–membrane tears during actuation cycles.

♦ Cracks in the Graphene Membranes



Cause:

Transfer can lead to cracks in graphene, which will propagate during release leading to tears in the membranes.

Consequences:

–Increased actuation voltage.

–Short life-time - membrane tears after few actuation cycles.

These issues affect the fabrication yield and the device performance. Contamination during processing is one of the main limitations in the current graphene technological development and is still an open problem. The most important step towards a successful process is a high quality synthesis and transfer with no contaminants.

3.5.2 Characterization

Graphene Membrane Characterization

The essential graphene parameters which directly affect the performance of an RF capacitive switch are the sheet resistance which is the limiting factor at high frequency, the membrane thickness which affects the actuation voltage and the uniformity which ensures the possibility of subsequent processing and reproducibility. A SEM of the membrane before release is presented in Figure 3.15, indicating the various multilayer islands by the difference in contrast. From I-V measurements performed before the membrane release we obtain a sheet resistance, $R_{\square} = 110\,\Omega/\square$ and a contact resistance of $R_{\text{contact}} = 266\,\Omega\,\mu\text{m}$.

In order to determine the membrane thickness, we employ Raman spectroscopy (Figure 3.16) to do a $20 \times 20\,\mu\text{m}^2$ scan, covering islands of different thicknesses, selected by observing the optical contrast. From the 2D/G ratio, the 2D and G shifts we deduce the number of layers using references [123, 164]. We observe areas of 2 to 5 layers or more. The Raman technique is limited to 5 layers, it cannot distinguish additional layers above.

From the scan we can estimate that more than 77 % of the area consists of more than 5 layers. The data is summarised in Figure 3.17.

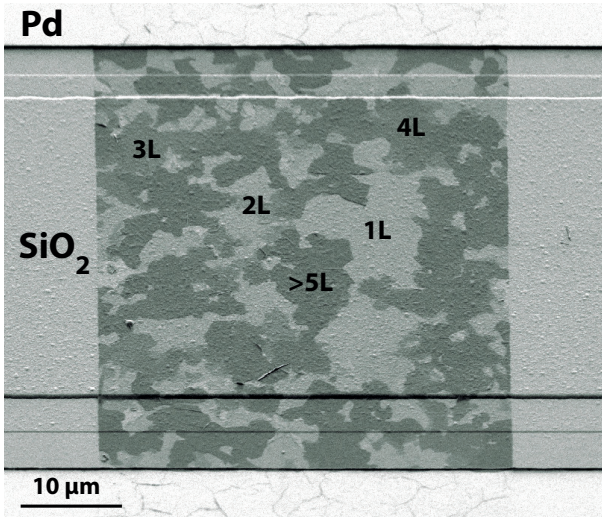


Figure 3.15: SEM of the multilayer graphene membrane of the NEM Switch before release.

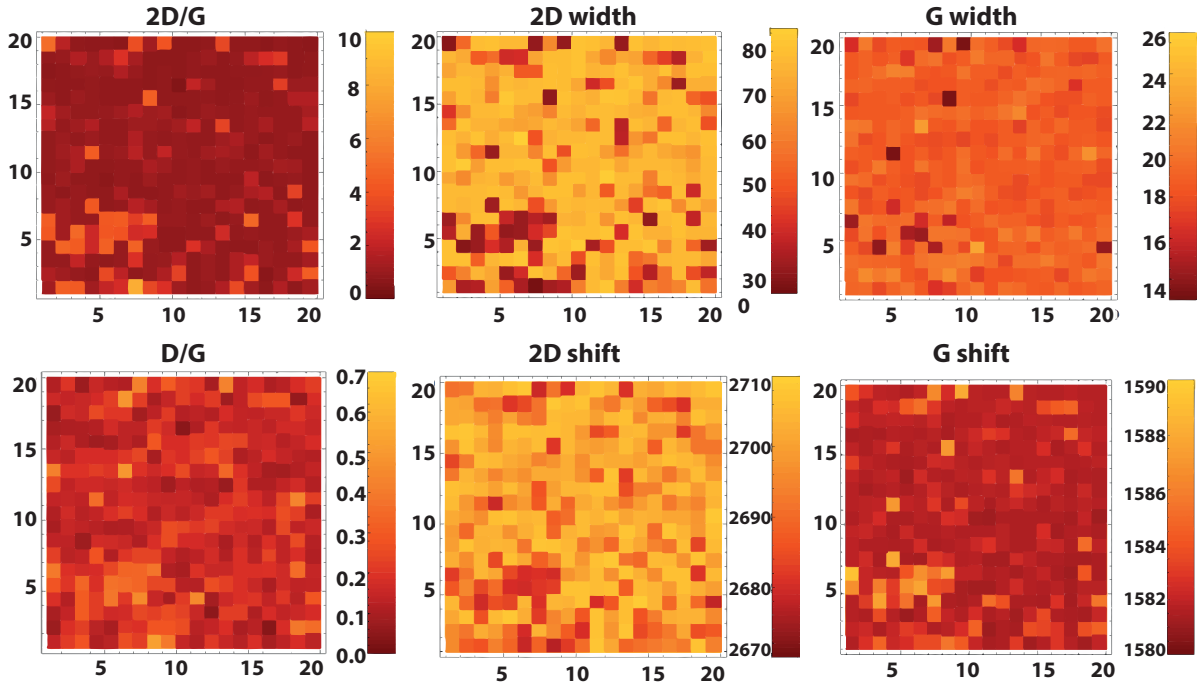


Figure 3.16: Micro-Raman mapping of the multilayer graphene membrane before release. The laser wavelenth is 532 nm and the resolution is 3 µm.

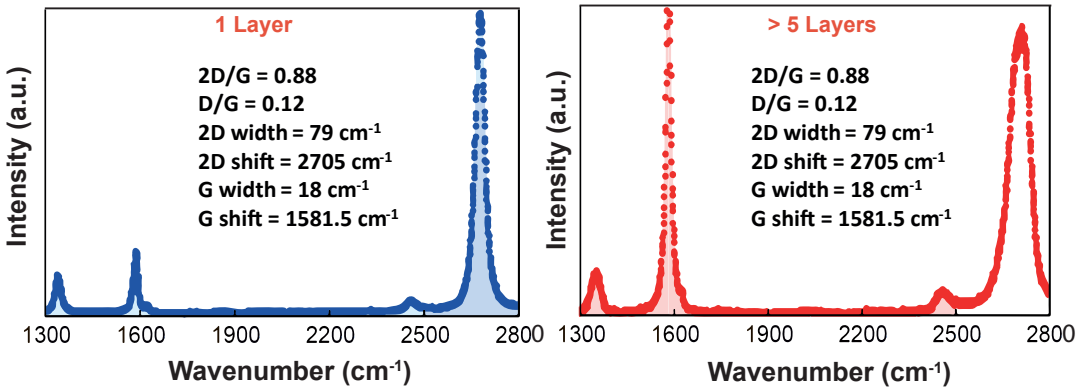


Figure 3.17: Average Raman spectra extracted from the scan in 3.16 for 1 (left) and more than 5 layers (right) and the extracted parameters.

RF NEM Switch Characterization

The fabricated NEMS switches were characterized by RF measurements up to 6 GHz (Figure 3.18) using a N5230C microwave vector network analyzer (VNA) and SOLT (Short, Open, Load, Thru) calibration. In order to operate the device, a DC voltage V_{DC} was superimposed to the RF signal, inducing an electrostatic force between the graphene membrane and the bottom electrode. First, an unloaded CPW structure was measured, with the same geometry as the characterized device but no graphene membrane in order to de-embed all parasitics and obtain the intrinsic properties of the device and a precise characterization of the graphene membrane.

The device was characterized at different V_{DC} values, and the corresponding S-parameters were fitted to the equivalent circuit shown in Figure 3.19. The S-parameters corresponding to an equivalent circuit obtained from theoretical estimations based on nominal dimensions are also shown for comparison. A first set of measurements with no applied V_{DC} bias confirms that the membrane was successfully released, since the extracted value of the capacitance is low ($C_{\mathrm{UP-0V}}$ = 270 fF) and close to the expected value (120 fF), calculated from the standard parallel plate capacitor model. The insertion loss $S_{21-\mathrm{UP}}$ is relatively low (−1.6 dB at 6 GHz) and comparable to the theoretical value. We also demonstrate the actuation of the graphene membrane, by increasing the V_{DC} bias until a steep decrease in S_{21} with frequency is observed, indicating a high capacitive coupling to ground due to the contact between the membrane and the thin dielectric on the bottom electrode. The isolation $S_{21-\mathrm{DOWN}}$ is limited to −1.75 dB because of the high resistivity of the graphene membrane, in series to the capacitance. The extracted circuit parameters for all the V_{DC} values are reported in Figure 3.20. The capacitance in the UP state is higher than the theoretical value, as mentioned above, mostly because of partial

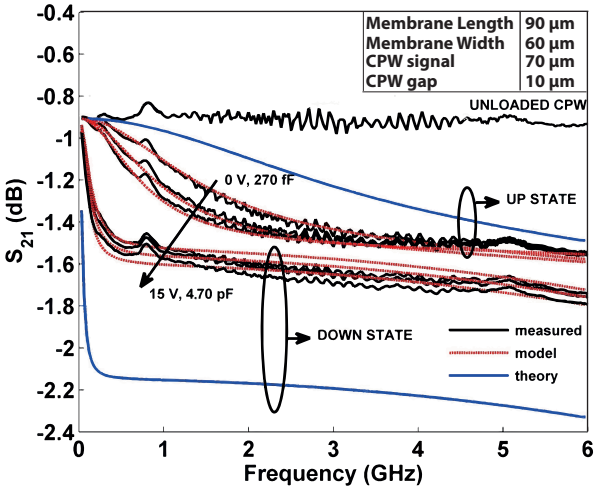


Figure 3.18: S-parameter measurements up to 6 GHz of a graphene RF NEMS capacitive switch.

sagging of the membrane resulting in a lower effective gap between the graphene membrane and the bottom electrode. When applying a DC bias, the membrane is gradually pulled down resulting in a slight capacitance tuning in the up-state. After reaching the pull-down voltage, $V_{\mathrm{PI}} = 10\,\mathrm{V}$ the membrane snaps down and a steep increase in capacitance is observed ($C_{\mathrm{DOWN-10V}} = 2.9\,\mathrm{pF}$). This value is considerably lower than the expected capacitance in the down state (20 pF), suggesting that the contact with the bottom electrode is smaller than estimated, consistent with the observation in the SEM (Figure 3.14). However, increasing the applied V_{DC} bias allows to increase linearly C_{DOWN}, gradually improving the contact area. The obtained capacitance ratio of $C_{\mathrm{DOWN-15V}}/C_{\mathrm{UP-0V}} = 17.4$. The extracted sheet resistance in the UP state is $R_{\square-\mathrm{UP}} = 253\,\Omega/\square$, while in the DOWN state the resistance is tuned down to $R_{\square-\mathrm{DOWN-15V}} = 220\,\Omega/\square$ due to the field effect. The resistance is higher than the value measured before release, which can be attributed to tears during fabrication.

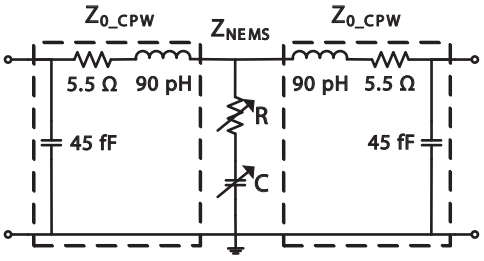


Figure 3.19: Equivalent circuit model of the suspended graphene RF NEMS capacitive switch in shunt configuration on a coplanar waveguide.

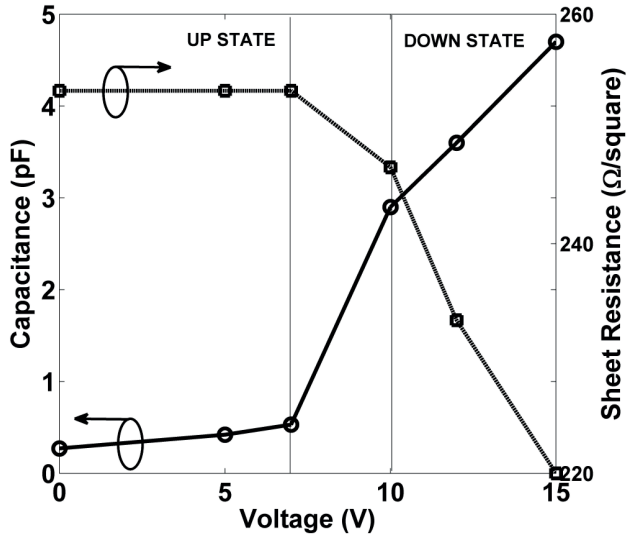


Figure 3.20: Extracted capacitance (left) and resistance (right) using the equivalent circuit in 3.19.

3.5.3 Optimisation

In order to fully assess the potential of this technology, the performance of the GNEMS with an intact graphene membrane is obtained by calibrated simulations. Optimizing the release process would allow considerable improvement of the isolation values, as shown in Figure 3.21.

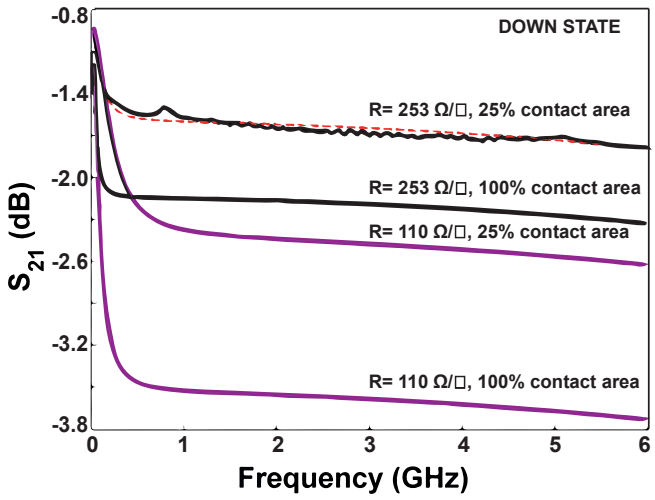


Figure 3.21: Isolation curves for different graphene resistivities: 110 Ω/□ (before release), 253 Ω/□ (after release).

3.6 Graphene NEMS—Transfer of Exfoliated Graphene on Predefined Cavities

In order to improve the GNEMS manufacturing yield and performance, a different fabrication strategy has been implemented, based on transfer procedures customised for this work as part of the "Grafol" project, and evaluated in Section 2.3.2. The main goal is to optimise the process of suspending graphene membranes. The employed strategy is to suspend graphene directly by transfer on top of predefined cavities. This chapter uses the method presented in Section 2.2.3, developed in collaboration with Danmarks Tekniske Universitet.

3.6.1 Fabrication

The fabrication flow is represented in Figure 3.22. The first 4 steps (Figure 3.22a-d), are identical to the process previously described. Then, the metal ground plane is defined by a lift-off process of Pd/Cr (200/20 nm) (Figure 3.22.e). One advantage of this process, compared to the previous one, is the possibility to deposit a thicker metal, resulting in lower RF losses due to the CPW structure. Previously, we have observed that the maximum metal thickness that can be deposited on graphene with good adhesion is 70 nm. Subsequently, cavities are defined in the LTO by a CF_4 plasma etching process. This avoids the pads underetching. The final step (Figure 3.22f) consists in suspending graphene over the CPW in order to realize the

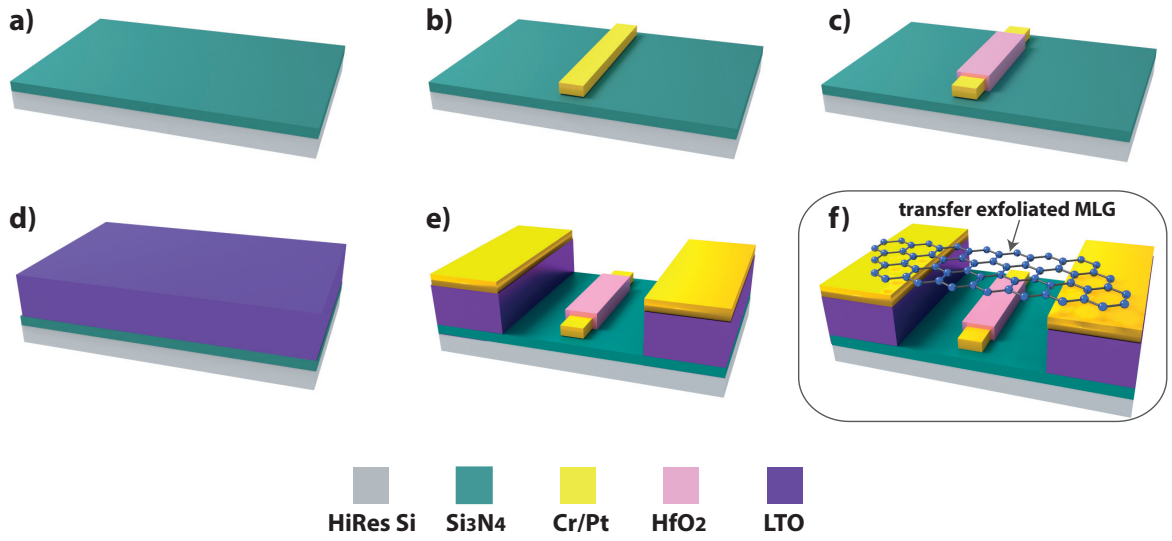


Figure 3.22: Main steps of the process flow for graphene NEMS with suspended exfoliated MLG on predefined cavities.

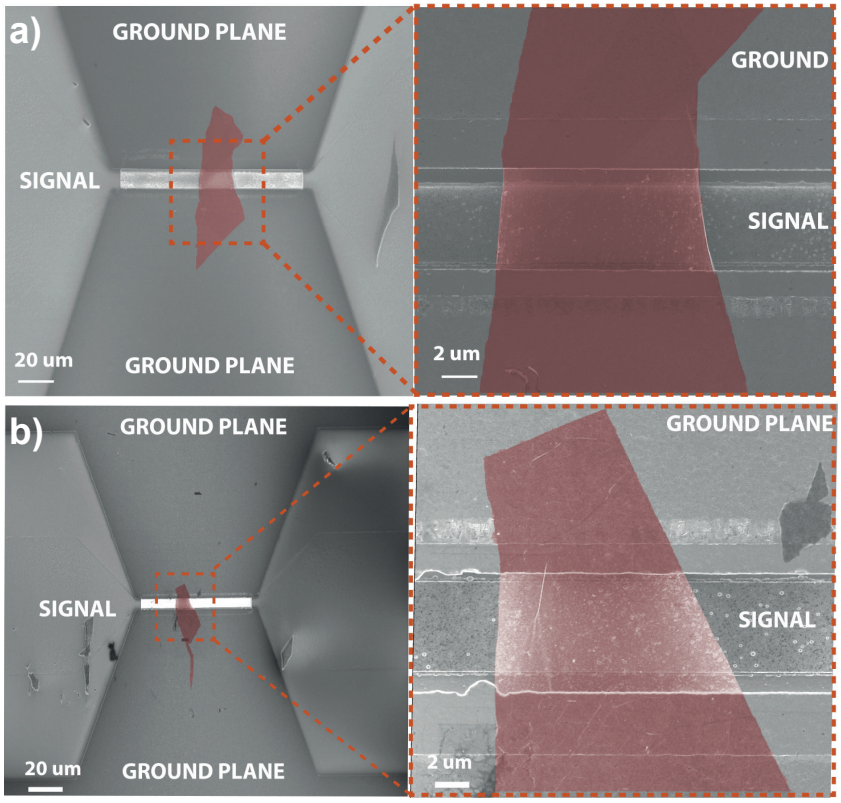


Figure 3.23: False colored SEM of the Graphene NEMS and zoom on the suspended graphene membrane: a) 5 layer graphene b) 3 layer graphene.

GNEMS, by a process described in Section 2.2.3. Another advantage of this technique is that no additional post-processing step of graphene is required. On the other hand, the contact resistance is high due to impurities trapped between graphene and the metal pads.

Two fabricated GNEMS are presented in Figure 3.23, with 5 layer (a) and 3 layer (b) graphene.

3.6.2 Characterization

Graphene Membrane Characterization

To validate the transfer, flakes of different sizes and thicknesses have been successfully suspended on 500 nm and 2 µm deep cavities on CPW structures. They were characterised by IV measurements and the extracted resistances for each flake are shown in the table below and the sheet resistance is calculated based on the flake suspended area as measured by SEM.

We observe that the resistance decreases with the number of layers, however not by the expected ratio. This can be attributed to the contact resistance between the graphene and the metal.

Table 3.5: Measured DC Resistance of the graphene flakes transfered on the GNEMS.

		1 Layer	2 Layers	3 Layers	4 Layers	4 Layers-2	5 Layers
Gap 2 µm	**Measured R [kΩ]**	3.4	2 MΩ	2.1	1.1	3.5	1.2
	Sheet R [kΩ/□]	6.63	/	3.53	2.46	7.93	2.98
Gap 500 nm	**Measured R [kΩ]**	-	81.9	8.6	9.0	7.5	2.1
	Sheet R [kΩ/□]	-	363	37	39	25.1	4.3

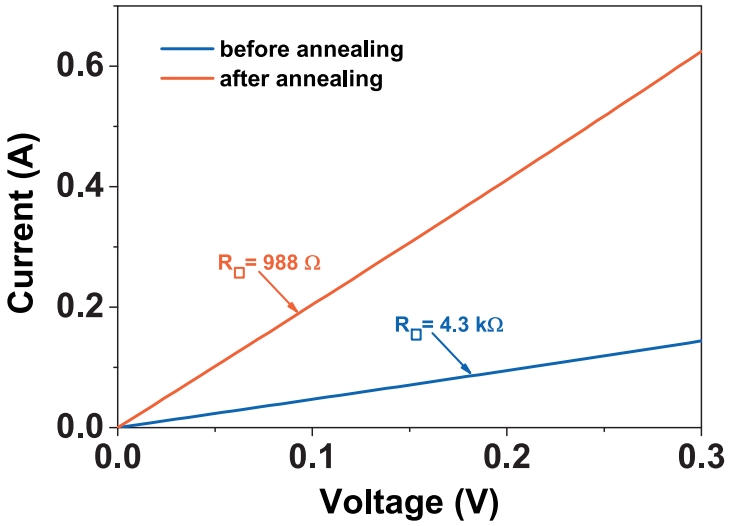


Figure 3.24: Current annealing of a 5-layer flake, showing a decrease in resistance.

We perform a current annealing by a short pulse of 4–5 mW applied power, to improve the metal contact to graphene. As shown in Figure 3.24 the resistance shows a 4-fold improvement and the IV characteristic becomes linear showing improved contact. Applying a high current for extended periods of time was also attempted but it did not show any improvement on the results.

RF NEMS Switch Characterization

The devices in Figure 3.23 were characterized in RF, up to 40 GHz and the results are shown in Figure 3.25 for a 3 layers (3L) GNEMS (a) and a 5 layers (5L) GNEMS (b), with a 500 nm gap. The GNEMS with 2 µm air gap could not be actuated up to 40 V. TRL (Thru, Reflect, Line) calibration is performed on an unloaded device (the CPW with no graphene) of the same geometry. It is used to de-embed the parasitics and extract the intrinsic properties of the

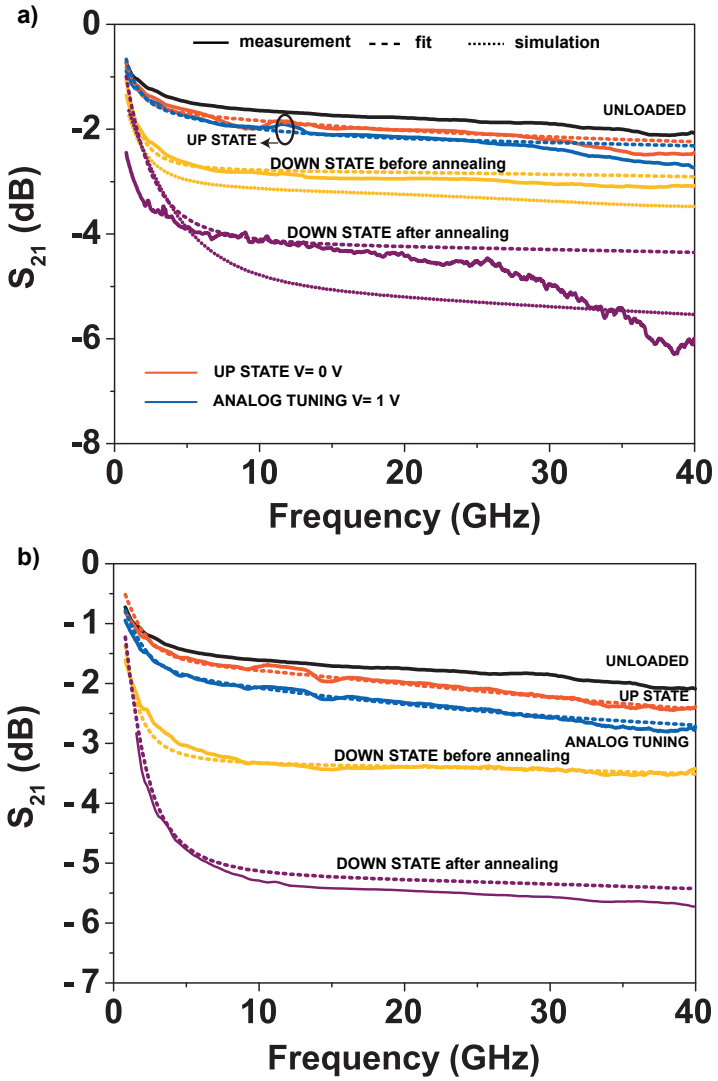
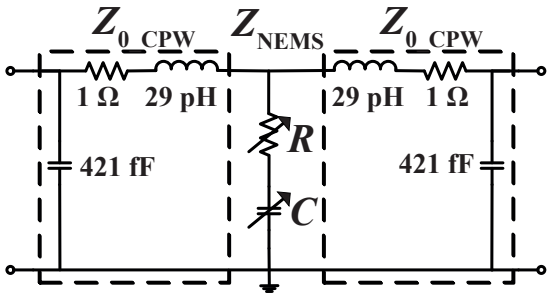


Figure 3.25: S parameters of a) 3L GNEMS and b) 5L GNEMS while increasing the DC bias, before and after annealing. CPW size: 2/3/2 (µm); graphene flakes: $L = 7\,\mu m$ and $w \approx 20\,\mu m$.

GNEMS. The simulation data is also shown for comparison. The experimental insertion loss is higher than the theoretical data, which can be due to membrane sagging during processing.

The irregular shape of the flake is approximated by a rectangle in simulations, which can further cause differences. The 5LG based device has a better RF performance than the 3LG flake to the higher resistance. The actuation voltages, V_{PI} are 3.1, respectively 2.9 V. They are higher than the theoretical values and are not proportional to the number of layers as expected, due to the high strain in the flakes, effect that dominates in the actuation event. Next, the performance of the 5L GNEMS is detailed. We observe that annealing significantly improves



NEMS equivalent parameters		Simulated	
C_{up} = 50 fF	R_{up}= 300 Ω	C_{up} = 25 fF	R_{up}= 1.4 kΩ
C_{down} = 2.5 pF	R_{down}= 300Ω	C_{down} = 2.5 pF	R_{down}= 252 Ω

Figure 3.26: Equivalent lumped circuit of the NEMS switch and corresponding extracted parameters.

the isolation, consistent with the decrease in resistance. Also, at a $V_{\mathrm{DC}} = 2.5\,\mathrm{V}$ we observe an intermediary membrane position, enabling analog tuning applications for the GNEMS.

The dashed line shows a good fit to the electrical circuit shown in Figure 3.26. Matching the S-parameters to the equivalent circuit, we extract the series resistance and capacitance of the NEM switch in UP and DOWN state. We obtain a high $C_{\mathrm{down}}/C_{\mathrm{up}}$ capacitance ratio of 50. The extracted parameters are summarized in the figure, both for the measured data, as well as for the simulated data.

The 5L GNEMS switch is also characterized using an impedance analyzer E4991A, at a frequency of 3 GHz, to obtain a direct measurement of the equivalent series resistance and capacitance as a function of the applied voltage. The measurements in Figure 3.27 clearly show the pull-in at low actuation voltage $V_{\mathrm{pi}} = 2.9\,\mathrm{V}$. We obtain a sheet series resistance of $828\,\Omega/\square$ in UP-state and $500\,\Omega/\square$ in DOWN state, observing a 1.65-fold field effect tuning that improves the switch performance.

The resistance and capacitance values are slightly different than the ones extracted from the S-parameters, for which the parameter extraction is not very precise due to the very high graphene resistance dominating the switch behaviour. Also we have considered a constant resistance in the UP and DOWN states, neglecting the field-effect tuning in DOWN state. The RF resistance is also considerably lower than the DC resistance, possibly due to the smaller influence of the contact resistance in RF, shunted by an equivalent parallel capacitor above certain frequency values.

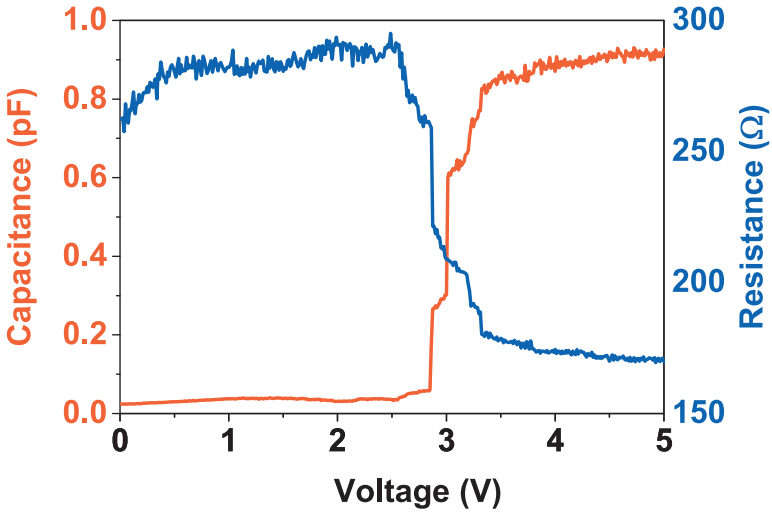


Figure 3.27: Series capacitance and resistance of the graphene switch at 3 GHz.

Optimisation

As already discussed, the main performance limitation of GNEMS is the high graphene resistance, severely limiting the performance at high frequency. One solution would be to dope graphene and values down to 100 Ω/□ are feasible in the case of FLG. In order to assess the potential of the technology, we present the performance of an optimised switch, obtained by calibrated simulations considering a graphene resistance of 100 Ω/□ (Figure 3.28).

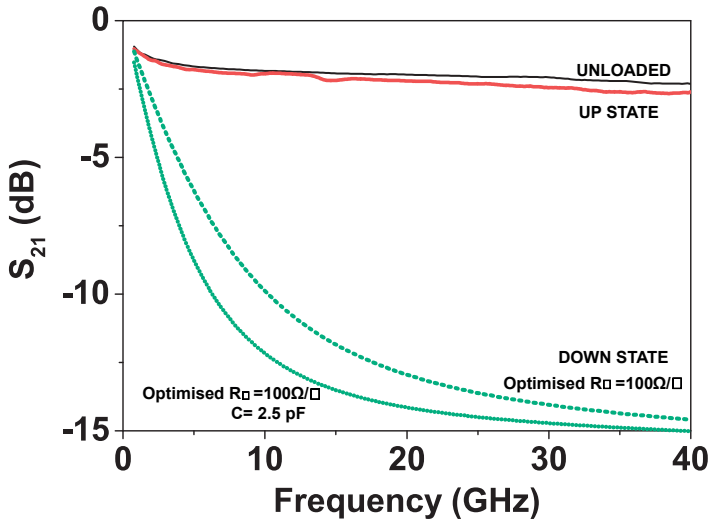


Figure 3.28: S-parameters of optimised GNEMS, considering a sheet resistance $R_{\square} = 100\,\Omega/\square$.

The UP state is similar to the measured one. An isolation of −14.5 dB is obtained at 40 GHz, which is comparable to metal MEMS. By improving the contact in DOWN state (less strained flakes, back electrode surface engineering) the isolation at lower frequencies is further improved. The results show that this process is suitable for the realization of GNEMS switches with good performance, if the graphene resistance can be further reduced. The causes of the very high resistance need to be investigated further to understand if they are caused by defects, high contact resistance due to impurities, and whether changes have to be made to the material, the exfoliation procedure or the transfer, to improve the process.

3.7 Graphene NEMS—Printing of Graphene Stripes on Predefined Cavities

After assessing the performance of a proof-of-concept device using single exfoliated flakes deposited individually on each device, we propose a scalable solution for wafer-scale fabrication of GNEMS capacitive switches for reconfigurable RFICs.

3.7.1 Fabrication

The fabrication flow of the CPW (Figure 3.29.a-e) was described in Section 3.6.1. The final devices are assembled using a PDMS stamp to suspend pre-patterned CVD SLG stripes on predefined cavities on the CPW, as shown in Figure 3.29. The transfer procedure was described in detail in Section 2.2.5. A standard wet transfer is used to place the patterned graphene stripes on the PDMS stamp.

To avoid the necessity of a precise alignment of the membranes on the CPWs at this stage, the layout was designed to make sure that at least one stripe will be suspended on one cavity. Then the additional stripes that short the device are cut by FIB or in some cases scratched away with the probes during measurements, method that proved effective. This is of course a proof-of-concept approach.

Owing to the fact that the PDMS stamp is transparent, a precise alignment under the optical microscope could easily be achieved.

The printed stripes on 2 GNEMS structures, one successful (right) and one failed (left), are depicted in Figure 3.30.

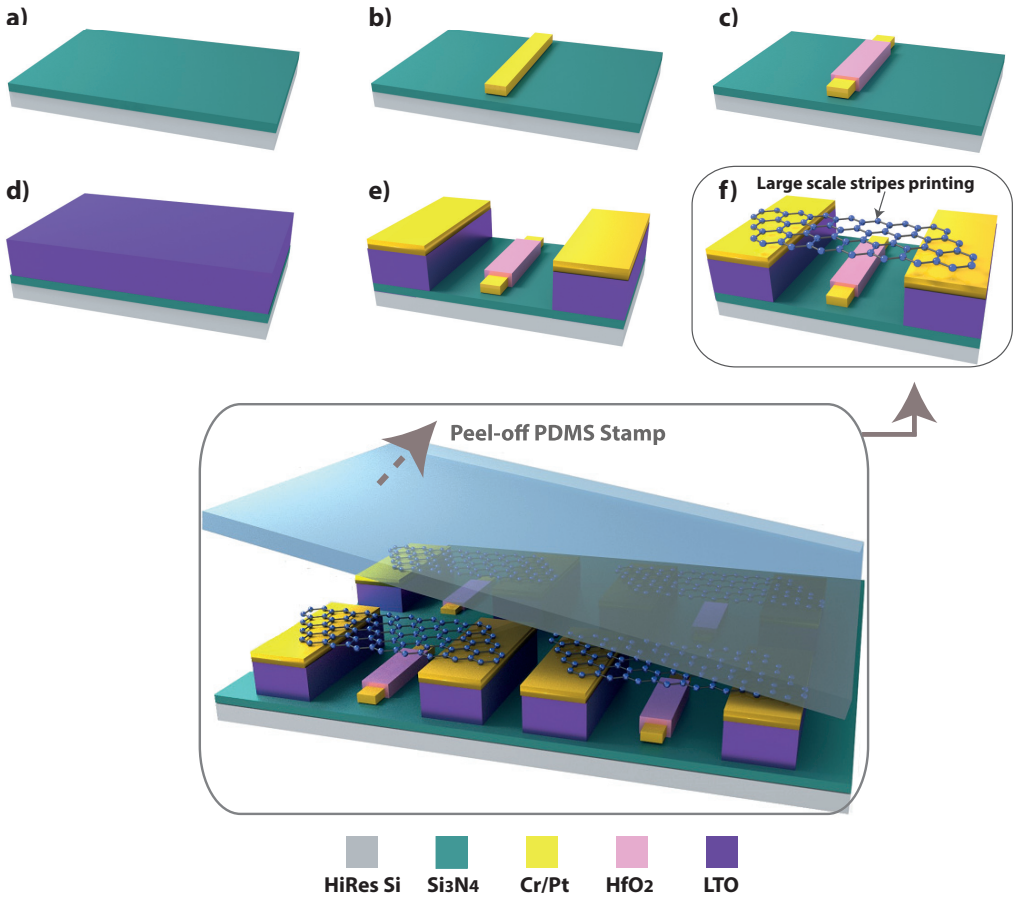


Figure 3.29: Fabrication process emphasizing the final step: graphene NEMS Switches are finalized by dry transfer using a PDMS stamp, suspending graphene on predefined cavities.

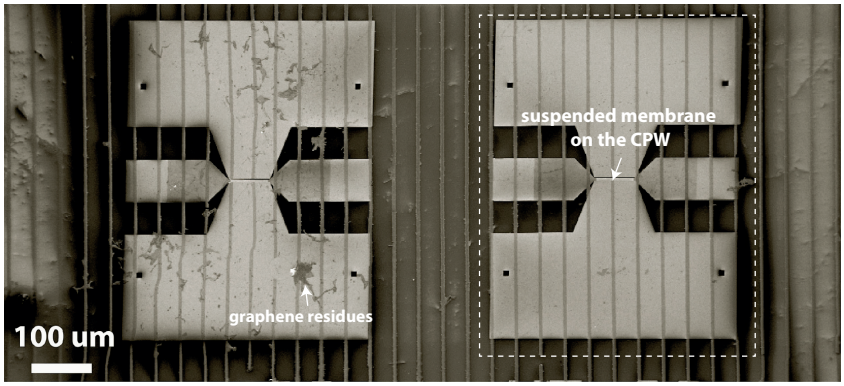


Figure 3.30: Graphene stripes transferred on the CPW.

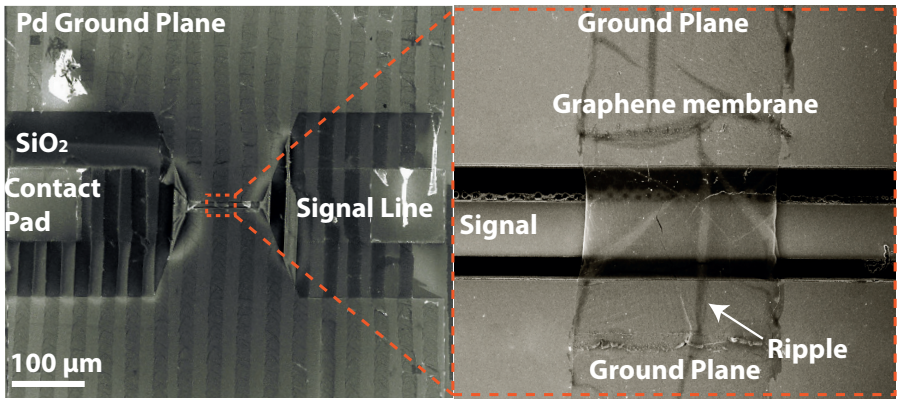


Figure 3.31: NEM Switch with 500 nm gap and zoom on the suspended membrane.

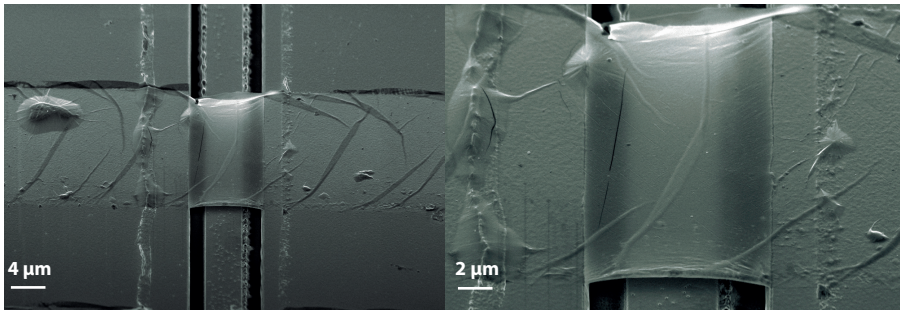


Figure 3.32: Suspended membrane on the CPW and zoom on the active area of the device.

3.7.2 Characterization

Graphene Membrane Characterization

A zoom on the active area of the GNEMS is presented in Figure 3.31 (left), with a zoom on the suspended membrane (right). In the SEM images, and additionally in Figure 3.32, which offers a more clear view on the suspended graphene, ripples, folds and impurities below graphene are observed. This device is characterized in DC in the UP-state. The results are presented in Figure 3.33. As shown in the inset, current annealing by applying a 1 mW short pulse is necessary to improve the graphene-metal contact, however the contact resistance is still in the order of 1 k$\Omega/\square$. We extract a sheet resistance of 800 $\Omega/\square$. The results are consistent along the sample for intact, successfully suspended membranes.

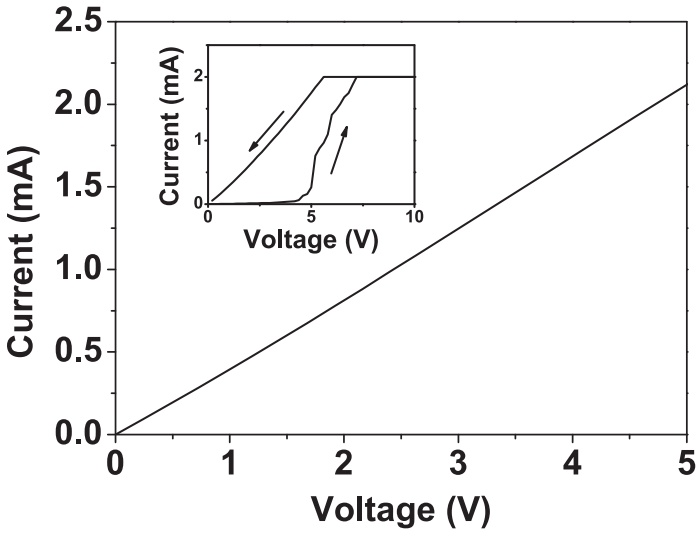


Figure 3.33: Up state I-V characteristics.Inset: Current annealing cycle, reducing the graphene-metal contact resistance.

RF Characterization

The GNEMS switches are characterized up to 40 GHz. A TRL calibration and measurements of an unloaded CPW are used in order to de-embed the losses. Figure 3.34 shows the up-state RF characteristics up to 40 GHz for 5 different devices with the same geometrical parameters, which show reliable results for different suspended membranes.

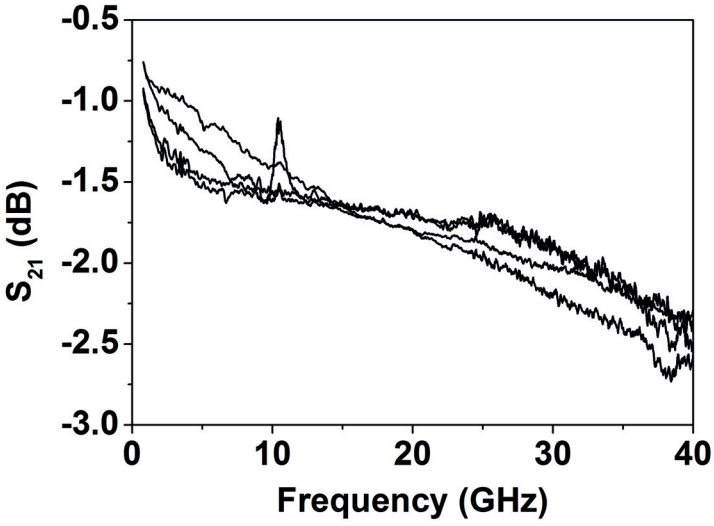


Figure 3.34: Experimental RF characterization of the UP state of different fabricated devices.

However, we observe slightly different shapes, consistent with different UP-state capacitances, indicating that some membranes are bent upwards, or in other cases sagged. The full RF characterization compared to the simulations and the fit to the equivalent lumped circuit is shown in Figure 3.35. The device geometry is specified in the inset. The experimental data matches very well the simulations and we obtain an excellent fit to the equivalent circuit reported in Figure 3.36. The extracted parameters for the measured devices and the ones extracted from the simulations results are in good agreement. We obtain a $C_{\mathrm{DOWN}}/C_{\mathrm{UP}}$ capacitance ratio of 79. In the UP state, the very low capacitance dominates the resistance.

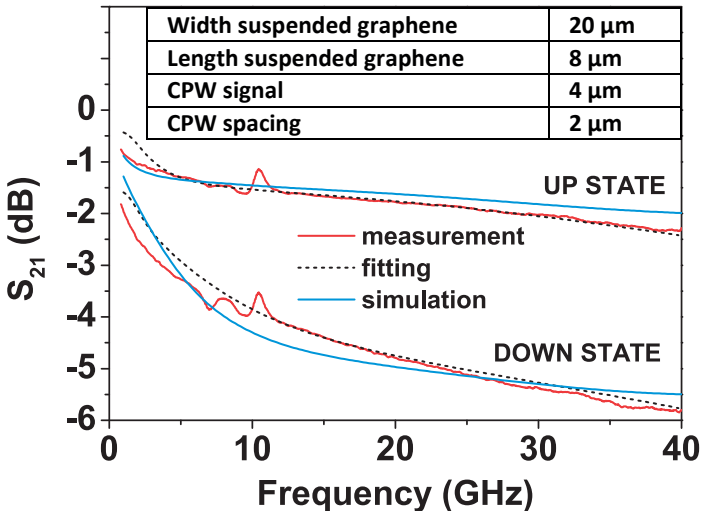
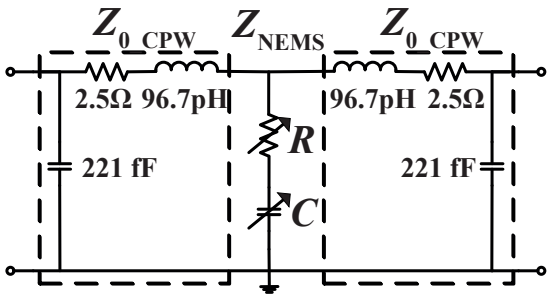


Figure 3.35: Simulation and experimental RF characterization of a switch in ON (UP) and OFF (DOWN) states; Inset: geometry of the measured device.



NEMS equivalent parameters		Simulated	
C_{up} = 10 fF	R_{up}= 70.9 Ω	C_{up} = 20 fF	R_{up}= N.A
C_{down} =790 fF	R_{down}= 70.9 Ω	C_{down} = 644 fF	R_{down}= 70.9 Ω

Figure 3.36: Equivalent circuit of the NEMS switch and the extracted parameters.

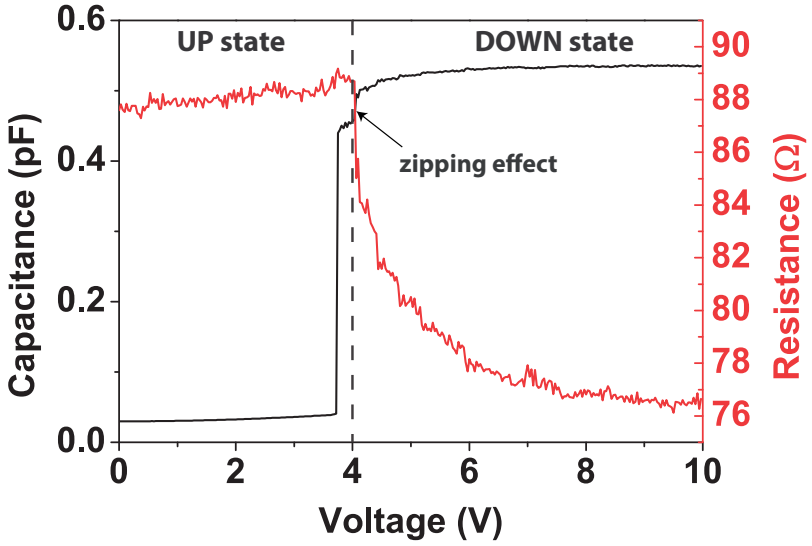


Figure 3.37: Series capacitance and resistance of the graphene switch at 3 GHz. We obtain a sheet series resistance of 704 Ω/□ in the UP state.

Impedance analyser measurements at 3 GHz are done and the results are presented in Figure 3.37. The GNEMS switch is actuated at 3.9 V and the contact is further improved after pull-down. This is indicated on the plot as a zipping effect. The measured values are close to the ones obtained by S-parameters.

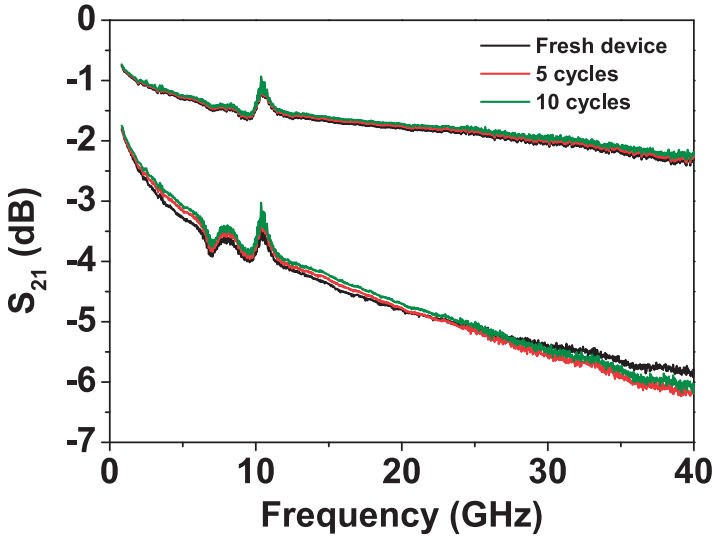


Figure 3.38: Stability of the device performance during 10 actuation cycles.

Furthermore, we investigated the reliability of the switch by repeating the RF characterization after multiple actuation events. As shown in Figure 3.38, the results are reproducible after several actuation cycles, showing that the membrane did not degrade.

Optimisation

Following the same procedure as in §3.5 and §3.6, the optimal performance is determined, in the case of a graphene sheet resistance of $100\,\Omega/\square$ (Figure 3.39), which leads to an isolation of $-8\,\mathrm{dB}$. This value is lower compared to the proof-of-concept GNEMS, due to the different geometry resulting in a higher resistance of the NEMS membrane, and due to errors arising from the fitting procedure.

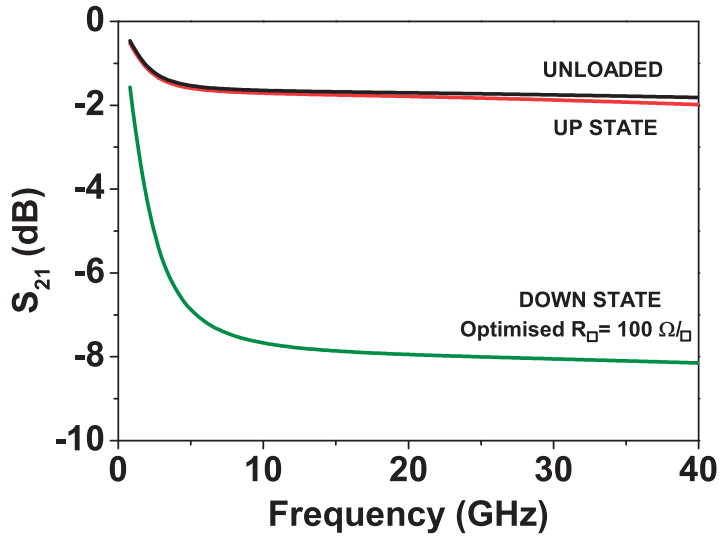


Figure 3.39: S-parameters of optimised GNEMS, considering a sheet resistance $R_\square = 100\,\Omega/\square$.

3.8 Discussion

We have empirically determined that a bottom-up approach is more reliable for GNEMS fabrication, having a better chance to suspend graphene membranes on top of predefined cavities on the CPW than sacrificial etching. In addition, defining the ground plane before the graphene deposition leads to a reliable metal lift-off process, unaffected by polymer residues on top of the graphene, which, as observed in Section 3.5, can lead to device failure. However, depositing graphene on the metal results in a high contact resistance, even after an annealing process. One solution would be to clamp the suspended graphene with a second metal layer on top, using a shadow mask in order to avoid any wet processing.

The bottom-up approach shows a superior performance, showing a possibility to achieve −15 dB at 40 GHz, in the case of a 100 Ω/□ graphene sheet resistivity, which is the major limiting factor for the performance of this technology.

The theoretical and experimental mechanical parameters of the three fabrication approaches are summarized in Table 3.6.

The GNEMS fabricated by a top-down approach, consisting of the sacrificial release of graphene, has a large area, thus a very low theoretical actuation voltage. However, due to the high strain in the membrane, an experimental V_{PI} of 10 V is obtained.

The developed DC model has been used to extract the equivalent tension of the beam T and estimate the switching time t_{s} for the fabricated devices. For the proof-of-concept switch based on wet polymer assisted transfer (PAT) of ExG, having a pull-in voltage $V_{\mathrm{PI}} = 2.9\,\mathrm{V}$, considering the geometry of the switch and assuming a Young's modulus of 0.8 TPa, we obtain that the theoretical limits with no beam tension are $k = 0.02\,\mathrm{N/m}$, $t_{\mathrm{s}} = 0.32\,\mu\mathrm{s}$ and $V_{\mathrm{PI}} = 1.23\,\mathrm{V}$. In order to match the measured value of V_{PI}, we have to introduce a beam tension of T = 36.2 nN, resulting in $k = 0.15\,\mathrm{N/m}$, $t_{\mathrm{s}} = 162\,\mathrm{ns}$. For the large-scale approach, based on dry PAT CVD SLG, a beam tension of 130 nN is estimated, giving a 51 ns switching time. These values are comparable with the semiconducting alternatives, constituting the main advantage of this technology compared to metal MEMS.

Table 3.6: Theoretical and Estimated DC Performance for the GNEMS Technologies Used.

Technology & Dimensions	**V_{PI} (V)**		**K (N/m)**		**T (nN)**		**ts (ns)**
	Theory	**Meas.**	**Theory**	**Meas.**	**Theory**	**Meas**	**Estimated**
Release FLG W = 70 um w = 60 um L = 90 um	0.28 V	10 V	0.056	100.4	300	$53.1\text{x}10^3$	15 ns
Dry PAT SLG W = 4 um w = 20 um L = 8 um	1.2 V	3.8 V	0.028	0.27	13	130	51 ns
Wet PAT ExG W = 3 um w = 25 um L = 7 um	6.4 V	2.9 V	0.74	0.15	300	36.2	162 ns

3.9 Applications: Phase Shifters

In this section, we perform a comprehensive study of the use of graphene based NEM capacitive switches in distributed NEMS transmission lines (DNTL) analog and digital phase shifters, by microwave circuit analysis based on electromagnetic simulations using the equivalent circuit model and the data obtained from the experimental characterization of a graphene NEMS switch (presented in Section 3.5).

3.9.1 Motivation

Phase shifters are crucial components in smart antennas, beam steering or scanning applications for wideband communications and remote sensing systems. RF MEMS have shown various advantages for the realization of phase shifters over conventional semiconductor switching devices, as field-effect transistors (FETs) or PIN diodes, such as low losses at high frequency, low power consumption and excellent linearity [165,166]. Conventional metal MEMS switches have been demonstrated reliably up to 40 GHz with low insertion loss and high linearity [167, 168]. However, MEMS based phase shifters are limited to relatively slow scanning applications due to their mechanical switching time (1-15 µs). One potential solution to overcome this drawback is to use graphene instead of metal for the MEMS membrane, due to its outstanding mechanical properties like high mechanical stiffness, high strength and low mass [55, 154]. These qualities make graphene NEMS achieve faster switching than traditional metal MEMS, thus they are more promising for fast scanning applications. However, the potential of graphene-based NEMS for phase shifters at RF frequencies has never been investigated before.

3.9.2 Principle

Distributed MEMS transmission lines (DMTLs) are the most common type of phase shifters based on the loaded-line topology [169], particularly suitable for RF MEMS integration. They mainly consist of a CPW transmission line periodically loaded by lumped tunable capacitors in shunt configuration. In this section we use as loading elements graphene-based RF NEMS voltage-controlled switches. These tunable loads affect the characteristic impedance of the line and consequently, the propagation velocity and resulting phase shift can be controlled. By applying a single analog control voltage to the signal line of the CPW, below the pull-in voltage V_{PI} of the graphene-based tunable capacitor, the resulting electrostatic force causes the graphene membrane height to vary, thus the distributed capacitive loading on the transmission line and, therefore, its propagation characteristics, can be varied. Analog DMTL phase shifters achieve a continuous variable phase shift commonly limited by the low capacitance ratio ($C_{\mathrm{r}} < 1.5$) of MEMS switches in their UP-state stable region. Furthermore, digital DNTLs

are investigated, based on digital capacitive switches with two controllable capacitive states (UP and DOWN positions of the switch), achieved by using a NEMS digital capacitor to achieve a C_r of 3. This MEMS digital capacitor was first introduced by Hayden [170] and is defined as the standard MEMS capacitive switch in series with a fixed small capacitance C_{FIX} possibly realized with metal-insulator-metal (MIM) capacitor, metal-air-metal (MAM) capacitor or interdigitated capacitors. Digital DNTL phase shifters achieve higher differential phase shift than analog approaches and are only limited by acceptable impedance matching. They have the advantages of size reduction and Brownian noise effects alleviation [165] in spite of higher actuation voltage and power consumption.

3.9.3 Design and Simulations

DNTL Phase Shifters Our goal was the design and simulation of DNTLs based on the graphene NEMS tunable capacitors presented in the previous section, operating at a frequency around 2.4 GHz, standard for RFID applications. The design of the DNTLs requires an accurate knowledge of the distributed loading capacitance and resistance of the NEMS membranes. These parameters are highly dependent on the fabrication process, which must be carefully characterized in order to obtain an accurate design. Figure 3.40 shows the approximated distributed equivalent circuit of an analog and digital DMTL phase shifter loaded with graphene NEM capacitors. The proposed DNTLs comprise 30 stages with 500 µm period, in order to obtain a good tradeoff between phase shift and loss at 2.4 GHz. For more controllable and miniaturized solutions, we propose a digital phase shifter using periodically-loaded digital capacitors in series with fixed capacitors, in order to achieve a well-controllable capacitive ratio of 3.

The DNTL design procedure is based on the metamaterial transmission line theory; we obtained the phase shift Φ (rad) and attenuation S_{21} (dB) of the whole DNTL by calculating the propagation constant $\gamma = \alpha + j\beta$ of the unit cell:

$$\gamma = -ln(\xi)/(\Delta L) \tag{3.4}$$

$$\Phi = \beta \cdot \Delta L \tag{3.5}$$

$$S_{21} = 20 \cdot \log_{10}[e(\alpha \cdot N \cdot \Delta L)] \tag{3.6}$$

where N is the number of stages, ΔL is the period and ξ is the eigenvalue of the ABCD matrix of the unit cell [171].

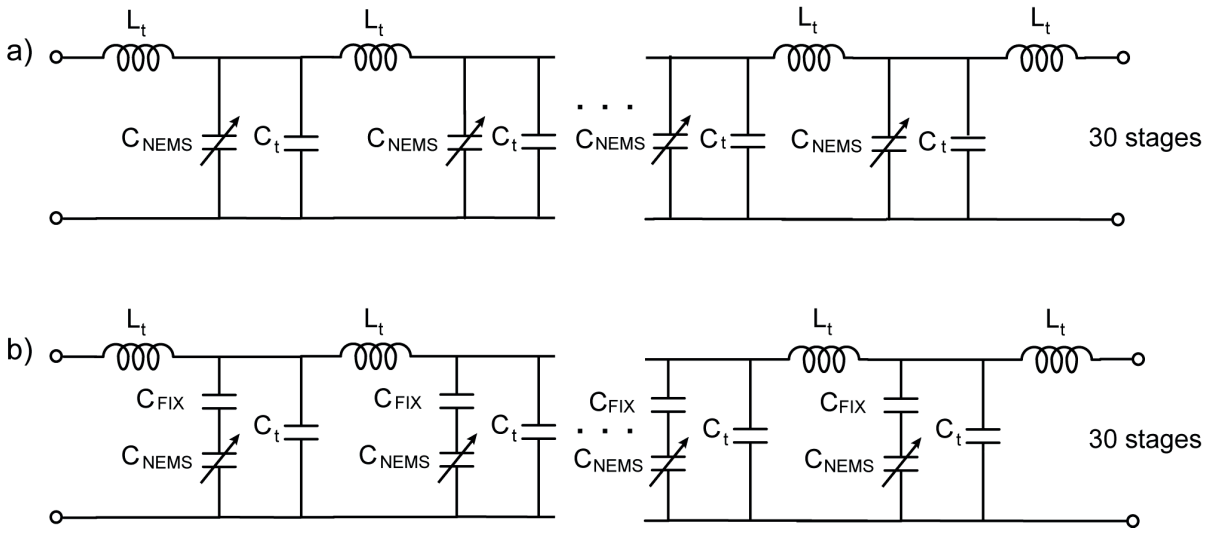


Figure 3.40: Simplified equivalent circuit of a loaded DNTL a) for analog and b) for digital applications

3.9.4 Characterization

DNTL Analog Phase Shifters

To assess the feasibility of a DNTL phase shifter using the presented graphene RF tunable capacitors, we perform microwave circuit analysis based on electromagnetic simulation of the CPW and the extracted lumped circuit model of the capacitor, as explained in the design section. The results for the DNTL analog phase shifter are summarized in Figure 3.41, showing the phase shift (normalized per cm and dB), the attenuation and the differential phase shift, respectively for each characterized bias voltage and corresponding switch capacitance value. The DNTL analog phase shifter, actuated below the pull-in voltage V_{PI}, achieves a continuous and quasi-linear phase shift in the whole range of frequencies employed for the characterization of the tunable capacitor (0–6 GHz), with a maximum value of 220° at the design frequency (2.4 GHz) when actuated at the highest voltage level measured before actuation (7 V). The differential phase shift presents a peak of 30° at 2.4 GHz, but the high resistance of graphene deteriorates the differential phase shift linearity and attenuation (8.5 dB at 2.4 GHz).

DNTL Digital Phase Shifters

The analysis of the performance of DNTL digital phase shifters using calibrated simulations is shown in Figure 3.42. DNTL digital phase shifters allow increasing the differential phase shift, as a consequence of the higher capacitance ratio, at the expense of higher attenuation

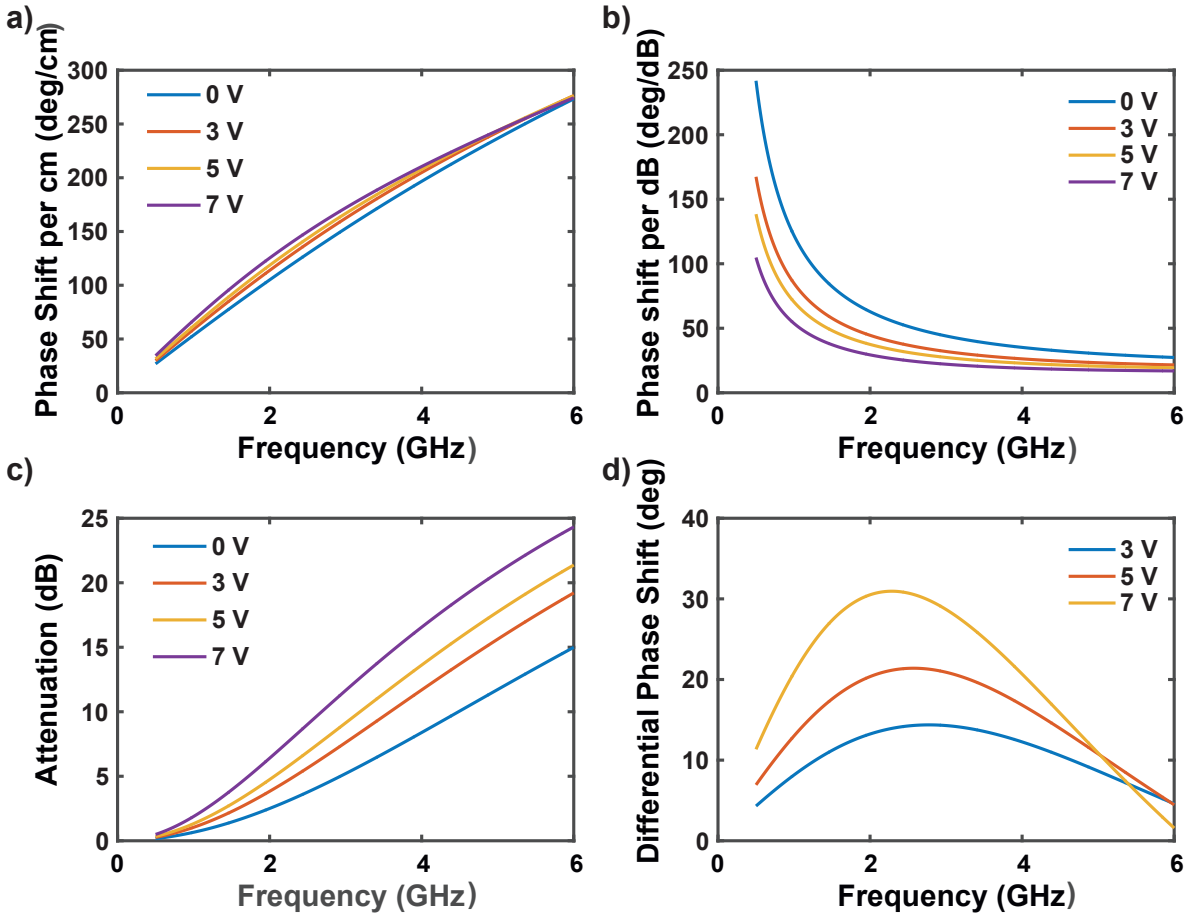


Figure 3.41: Performance of the DNTL analog phase shifter assessed by calibrated simulations. a) Phase shift per cm; b) phase shift per dB; c) attenuation; d) differential phase shift.

and no ability to continuously tune the phase shift. The DNTL digital phase shifter obtained using the parameters extracted from RF measurements achieves a phase shift of 150° and a differential phase shift of 42° with 12.7 dB attenuation at 2.4 GHz.

3.9.5 Optimisation

DNTL Analog Phase Shifters

To more accurately assess the potential of the graphene tunable capacitor for DNTL phase shifters in the presence of a feasible superior release process, we perform simulations using the graphene resistance measured before release, $R_{\square} = 80\,\Omega/\square$, and a capacitance $C_{\mathrm{UP}} = 100\,\mathrm{fF}$ in the UP state, calculated considering the theoretical gap and a parallel-plate capacitance model. For the actuation we consider the maximum value of capacitance obtainable in the analog tuning

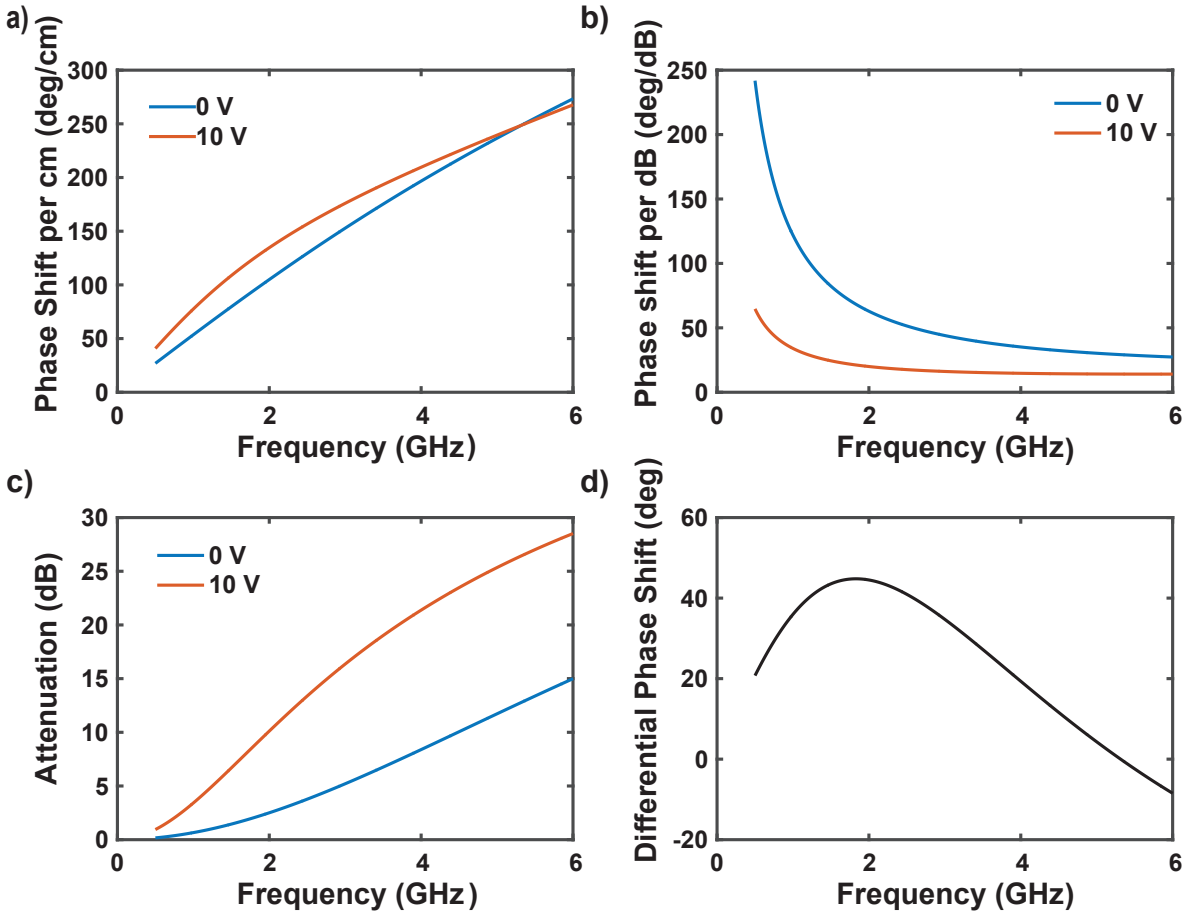


Figure 3.42: Performance of the DNTL digital phase shifter assessed by calibrated simulations. a) Phase shift per cm; b) phase shift per dB; c) attenuation; d) differential phase shift.

region, $C_{\max} = 1.5\,C_{\mathrm{UP}}$ The results of this analysis are summarized in Figure 3.43, showing an improvement for all the figures of merit of the phase shifter, which exhibits an increase in phase shift per dB at 2.4 GHz from 25.5°/dB to 355°/dB and a linear differential phase shift over the entire frequency range.

DNTL Digital Phase Shifters

Similarly, optimised parameters for the digital phase shifter are obtained and they are presented in Figure 3.44. The performance is greatly improved for the phase shifter employing optimized capacitor parameters, which achieves a differential phase shift of 54° at 2.4 GHz with attenuation limited to 1.45 dB.

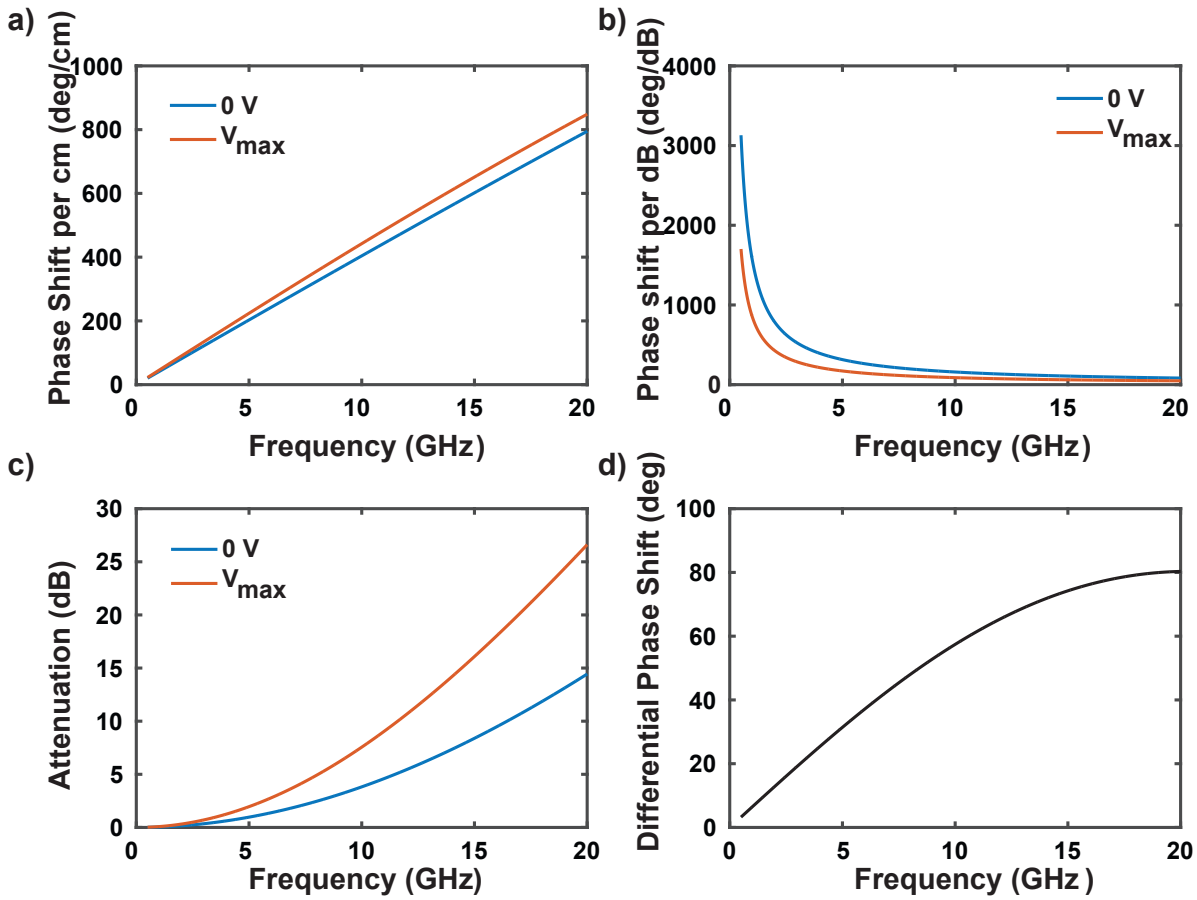


Figure 3.43: Performance of the optimized DNTL analog phase shifter. a) Phase shift per cm; b) phase shift per dB; c) attenuation; d) differential phase shift.

3.9.6 Discussion

The results are summarized in Table 3.7. Digital DNTL phase shifters allow obtaining higher differential phase shift than analog DNTLs, at the expense of higher actuation voltage, power consumption and losses. The performance-limiting factor for both the analog and digital DNTL phase shifters is the high resistance shown by the characterized suspended graphene membranes, which are attributed to imperfections caused by the release process, such as cracks and high residual stress. In order to better assess the potential of graphene tunable capacitors for phase shifters applications, we repeated the analysis of the proposed devices by using graphene parameters achievable with an optimized release process. The obtained results ("opt" rows in Table 3.7) show a dramatic improvement in performance due to the much lower attenuation caused by the graphene membrane resistance.

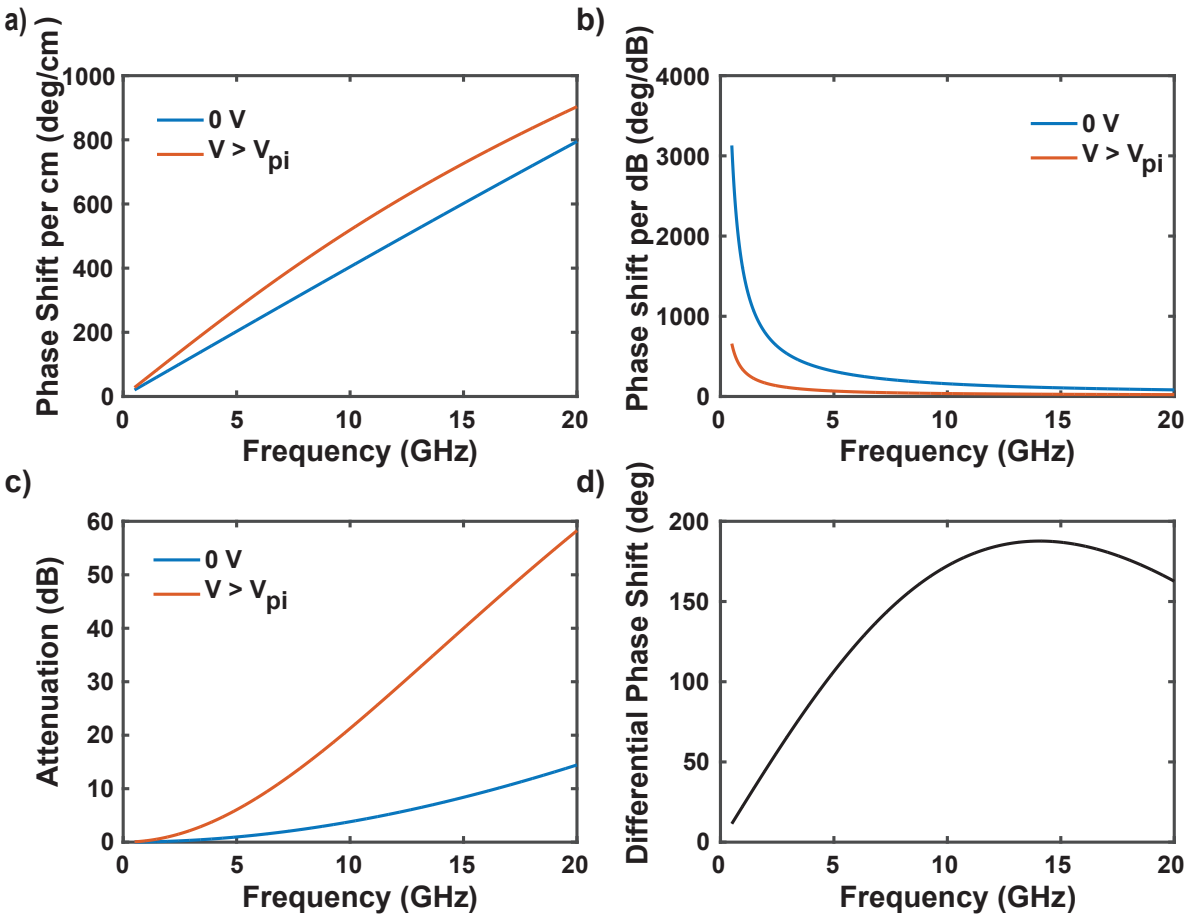


Figure 3.44: Performance of the optimized DNTL digital phase shifter. a) Phase shift per cm; b) phase shift per dB; c) attenuation; d) differential phase shift.

Table 3.7: Simulated phase shifters performance.

Phase Shifter Type		°/cm 2.4 GHz	°/dB 2.4 GHz	Attenuation (dB) 2.4 GHz	Attenuation (dB) 1-6 GHz
No bias	real	124	53.3	3.5	14
	opt	98	652	0.22	3.8
Analog tuning	real	145	25.5	8.5	24.9
	opt	108	355	0.45	2.8
Digital tuning	real	153	20	12.75	28
	opt	133	138	1.45	8.5

3.10 Conclusion

We have presented the first demonstration of graphene capacitive switches, as the first step toward the development of a robust platform for large-scale integration of graphene NEMS in reconfigurable RFICs. The switches have been designed based on an extensive original study on modeling and simulations. Three different fabrication approaches have been evaluated, realized and fully-characterized for GHz applications.

GNEMS based on a graphene release process by sacrificial etching. This technique was fully developed at EPFL, and suspended multilayer graphene membranes up to 60 × 90 µm^2 have been produced. The switches have been actuated at 10 V and capacitive ratio of 17 was achieved. This was the first demonstration of an RF capacitive switch employing graphene as a movable part of the NEMS. The switch did not recover after one actuation event, but this experiment led to important observations about the process and its main performance limitations, allowing to develop optimised strategies in order to boost the GNEMS performance.

GNEMS based on suspending exfoliated multilayer graphene on cavities on the CPW. A wet transfer method of exfoliated flakes on the CPWs has been developed, successfully obtaining suspended graphene on cavities down to 500 nm deep. This was employed for the fabrication of GNEMS varactors, promising for both analog and tunable RF applications. GNEMS have been actuated at $V_{\mathrm{PI}} = 2.9$ V for multiple cycle without a variations in performance. After a current annealing procedure, we obtain a capacitance ratio of 50 and an isolation of −5.5 dB at 10 GHz. At higher frequencies the performance is limited by the high resistance of graphene. Furthermore, we demonstrate that by decreasing graphene sheet resistance to 100 Ω/□, an isolation of -15 dB can be achieved at 40 GHz, proving the potential of our technology to be competitive with metal MEMS. However, this fabrication approach is not suitable for a scalable production of devices.

GNEMS based on suspending CVD single graphene on cavities on the CPW by a scalable approach. To facilitate large scale introduction, using a scalable process that consists in PDMS stamping prepatterned stamps, validated in Section 2.2.5 we obtain a fabrication yield > 50 % for suspended membranes over areas as high as 15 × 20 µm^2, superior to the state-of-the-art. The switches are actuated at 4 V and were operated for 15 cycles. A capacitance ratio superior to the previous GNEMS was achieved, due to the lower graphene resistance. However, the isolation is −6 dB at 40 GHz, comparable to the ExGNEMS. This is due to the high resistance of ExG, which hinders the performance. The proposed graphene-based RF switches offer a viable CMOS-compatible solution for RF reconfigurable circuits.

These results confirm that we developed a scalable fabrication process for graphene RF MEMS switches with a good RF performance up to 40 GHz, demonstrating a promising scalable method

for the mass production of graphene based RF devices and circuits integrated with silicon electronics.

Finally, we have demonstrated **analog and digital wideband compact phase shifters** ($10\,mm^2$) by employing graphene based RF NEMS tunable capacitors periodically loaded on a coplanar waveguide. The analog device has shown a differential phase shift of 30° at 2.4 GHz and the digital one a differential phase shift of 42° at 2.4 GHz. Repeating the analysis using improved graphene parameters achievable with an optimized membrane release process in which the sheet resistance preserves its value ($80\,\Omega/\square$ before release), we have obtained a 14-fold improvement in phase shift per dB at 2.4 GHz for the analog DNTL and 6.9-fold for the digital DNTL. These results show that graphene-based RF NEMS are interesting candidates for RF phase shifters, providing additional features with respect to metal RF NEMS, if graphene release could be further controlled and optimized.

This work represents an important milestone for the development of a mature graphene NEMS technology, expected to replace MEMS for essential applications with strict requirements in terms of actuation voltage and switching time.

The main technical contributions in this chapter are:

- Three general approaches, one based on sacrificial etching and two on graphene transfer on defined cavities, have been proposed to fabricate GNEM capacitive shunt switches.
- RF GNEMS switches for reconfigurable applications have been successfully demonstrated for the first time.
- RF characteristics of the GNEMS have been determined experimentally and a route towards performance optimization has been defined.
- The potential of GNEM switches for implementation in phase shifters for reconfigurable applications has been investigated by calibrated simulations.

4. Graphene Quantum Capacitors for Reconfigurable RF Applications

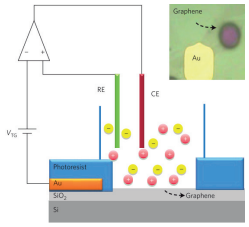
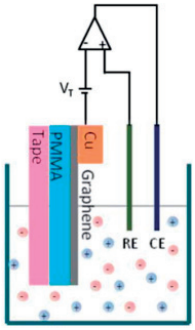
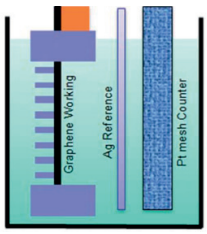
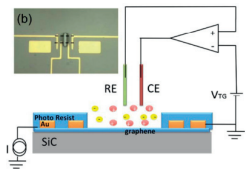
This chapter introduces graphene quantum capacitors (GQC) as enablers of Radio-Frequency (RF) functions through voltage-tuning of their capacitance. It is shown that GQCs represent a technology option complementary to MEMS and MOSFET in terms of tunability and performance for high frequency analog applications. The fabrication process of QGCs and the first experimental assessment of their performance up to 10 GHz are described in detail. The figures of merit of graphene variable capacitors are studied from 150 K to 350 K and, furthermore, we propose and demonstrate a systematic approach to optimise the performance, in order to achieve superior performance to alternative technologies at frequencies above 2.1 GHz. Finally, its potential for RF applications is demonstrated experimentally, for phase shifters designed for 5.8 GHz RFID applications, fabricated and characterized up to 6 GHz.

4.1 Introduction

4.1.1 Overview—Graphene Quantum Capacitance

Most of the research carried out on graphene for nanoelectronics has focused on active devices exploiting its high carrier mobility [41, 172]. In this work, the focus was on another interesting property of graphene: the high tuning range of its capacitance by changing the charge density trough applied bias, which is of great interest for both fundamental science and for applications. This behavior is based on the Pauli exclusion principle; the capacitance tuning is achieved because the quantum capacitance of graphene changes with its electron density [173], modulated by its chemical potential, which in turn can be tuned by the gate voltage. This differentiates graphene from conventional two-dimensional electron systems where the quantum capacitance has only a small and constant contribution that is difficult to be extracted from the experimental data. Graphene quantum capacitance has received a lot of attention in fundamental studies [173–175] as well as in studies of graphene properties [175–178] and scaling down graphene FETs [179–181]. These results are summarized in Table 4.1 and 4.2. The data obtained in Table 4.1 presents the initial studies of the quantum capacitance, in electrochemical cell configurations. It is interesting to observe that high tuning ratios can be obtained, up to 26, with voltages below 0.5 V, depending on the electrolyte. Table 4.2 shows a summary of the

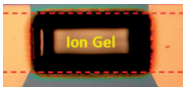
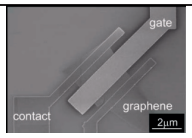
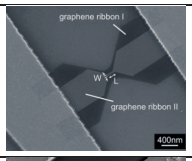
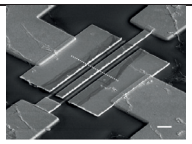
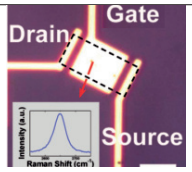
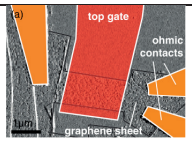
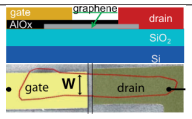
Table 4.1: SOA of graphene quantum capacitors in electrochemical cells configuration.

Ref	Xia, 2009 [173]	Zhang,2012 [176]	Stoller, 2011 [182]	Xia, 2010 [183]
				
Config. Substrate	exfoliated SiO_2/Si substrate Au electrode	CVD tape/PMMA Cu electrode	CVD 1/2 sides Cu electrode	epitaxial SiC Au electrode
EOT (nm)	0.55 (ε=7)	N.A.	N.A.	0.3 (ε=7)
Area (μm^2)	79	0.84 cm^2	55 mm^2	4.3 x 30
Bias (V)	-0.17...-0.4 -0.17...0	0..-0.56 V 0..0.4 V	-0.7...-0.2 -0.2...0.5	-0.05...0.45 0.45...0.6
C_{min} ($\mu F/cm^2$)	6.7	2.9	0.3/0.1	7.9
TR	1.52	4.5	26/50	1.26
C_{tot} ($\mu F/cm^2$)	N.A	2.4..8.2	27	6.6
Slope ($\mu F/Vcm$)	11	22	23	N.A
R_{series} ($k\Omega/\square$)	N.A	N.A.	N.A.	7

experimental quantum capacitance measurements on transistor configurations and other test set-ups.

In spite of the vast experimental work, the quantum capacitance of graphene was only recently proposed as the operating mechanism of an electronic device, more specifically as a variable

Table 4.2: SOA of Graphene Quantum Capacitors in Solid State Configurations.

Ref	Config.	Diel. (nm)	Bias (V)	C_{min} (fF/cm^2)	TR	R_{series} ($k\Omega/\square$)
 [180]	CVD; Pt ref	ionic gel	-0.2...0.7	25	3.5	0.1..0.6
 [179]	top gate SLG top gate MLG	10 nm Al2O3	0.2...1.9 -1.5...2	4.2 4.2	1.17 0	N.A.
 [184]	CVD	4nm HfO_2	0..-300meV	4.5	6	N.A.
 [185]	CVD back gate spacing 100nm spacing 300nm	30 nm Al_2O_3	 -0.5...2 -1.5...2	 15 12	 3.3 4.16	N.A.
 [181]	exfoliated	EOT:1.5 Y_2O_3	0...-0.4	18	3.9	N.A.
 [186]	CVD top gate	12 nm Al_2O_3	-2...2	4.8	1.4	13..16
 [187]	GNR/h-BN/ graphene sheet	14.7 h-BN 13.8 14.8	 0...28	10 20 10	8 2 4	N.A.
 [174]	SCS: exfoliated gr./SiO_2/n^+Si	100 nm SiO_2	0...-2	1.9×10^{-4}	44.4	N.A.
 [188]	RF admittance: exfoliated top gate	8 nm AlO_x $\varepsilon = 7$	0...1	13	3.9	N.A.

capacitor in a passive low frequency (up to few MHz) LC sensing circuit. The state of the art of low frequency interdigitated quantum capacitors (Figure 4.4)is summarized in Table 4.3.

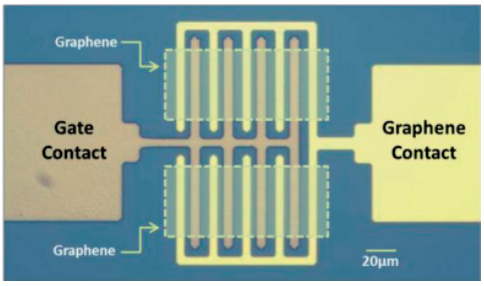


Figure 4.1: Interdigitated configuration of graphene quantum capacitor [189].

Table 4.3: Interdigitated graphene quantum capacitors employed in devices.

Ref	EOT. (nm)	Bias (V)	C_{min} (fF/μm^2)	TR	Slope (fF/Vμm^2)	Lin. range (V)
[189]	4.1	-0.5...1.5	3.7	1.17	(+)0.67	(+)0.3...0.5 V
		-0.5...-2			(-)0.682	(-) -1.08...-1.28V
[189]	2.7	-0.5...1	4.8	1.38	(+)2.48	(+)-0.2...0V
		-0.5...-2			(-)2.26	(-)-0.5...-1V
[190]	2.52	0...2	9.7	1.2	(+)1.327	(+)0.25...1V
		0...-2			(-)1.24	(-) -0.1...-1V
[191]	6.8	0...2	3.37	1.22	(+)0.93	(+)0...-0.32V
		0...-2			(-)0.96	(-)-0.95...-0.62V

4.1.2 Motivation

Graphene is very attractive for densely integrated high-frequency/RF IC applications due to its extraordinary electrical and thermal properties, while its ability to handle high RF power and the quantum capacitance shows great promise for reconfigurable devices. However, its potential for these applications has not yet been investigated.

As previously discussed in §3, there is an important need in wireless communications for reconfigurable systems that can be fine-tuned, and recently, microelectromechanical systems (MEMS) have been proposed [192] to replace semiconducting varactors (MOSCAPs) owing to their low losses, high quality factor (Q) and linearity. However, MEMS themselves have several drawbacks: high control voltage, packaging needs and large size and costs [192]. In order to address these issues, we propose GQCs as a novel alternative type of tunable planar capacitors. They have several advantages compared to the existing technologies; in comparison

to MEMS they have an increased tuning range, low control voltage, significantly smaller size, limited temperature drift, ease of fabrication, no required packaging and reduced costs. Simultaneously, they offer a promising alternative to MOSCAPs, which are limited by high loss at high frequencies.

In this section, a comprehensive characterization of GQC at GHz frequencies is performed from a device perspective, with the purpose of advancing its implementation in high-frequency circuits such as voltage-controlled oscillators, tunable filters, impedance matching networks and phase shifters. In addition, we present the route to a further performance increase, which enables a new class of varactors replacing conventional semiconducting devices such as MOSCAPs, or the passive NEMS devices proposed in RF analog application.

4.2 Principle

Two capacitors are symmetrically placed on a coplanar waveguide (CPW) in a parallel configuration in order to characterize them at microwave frequencies; the biasing scheme and a simplified equivalent circuit are represented in Figure 4.2. A DC bias voltage is applied on the top gate, superimposed on the RF signal using bias tees.

The principle of operation of a graphene tunable capacitor can be seen as the result of the Fermi level shift within the graphene energy band due to the gate induced charges. When

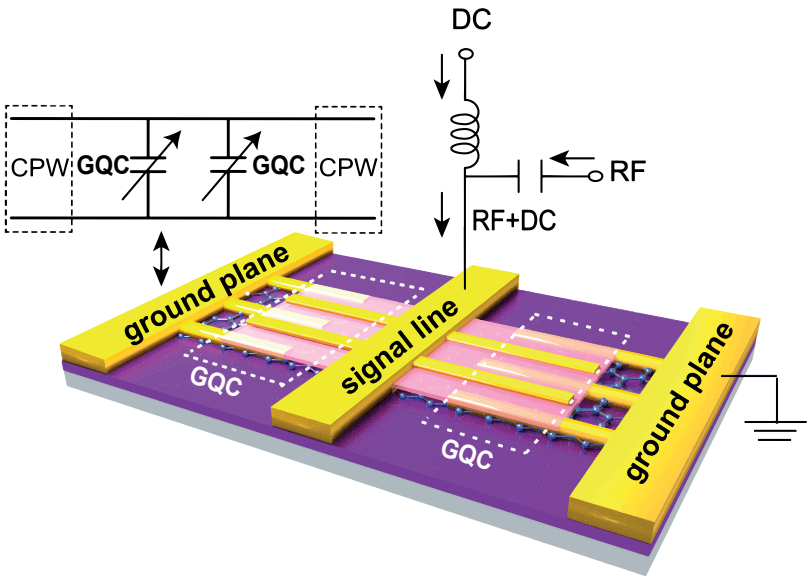


Figure 4.2: Schematic rendering of the GQC (two for symmetry) in a shunt configuration, on a CPW for RF characterization, the biasing scheme and the circuit schematic.

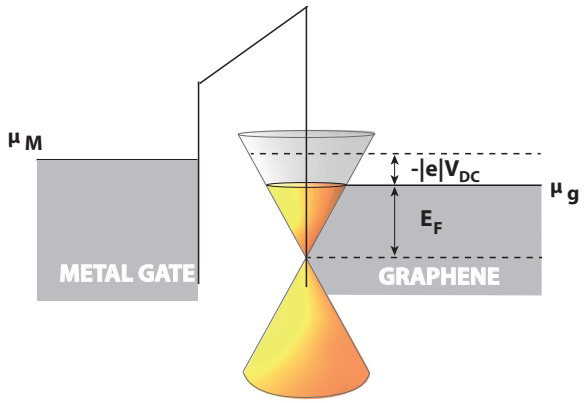


Figure 4.3: Schematic band diagram of the graphene capacitor showing the effect of increased charge density by applying a finite bias.

a gate bias induces more electrons, or holes, to fill the energy band of graphene, the Fermi level position is shifted to a higher, respectively lower, energy level with respect to the Dirac point, as represented in Figure 4.3. The underlying principle of the quantum capacitance tunability is explained by charge density modulation with voltage shown in Figure 4.4. For voltage levels near the Dirac point, the charge modulation is dominated by the effect of the quantum capacitance, while for higher values we observe the conventional linear dependence due to the field effect. For the GQC, the ideal operation range is the linear range and it is desirable to obtain steep slopes ensuring a high tunability with a low operation voltage.

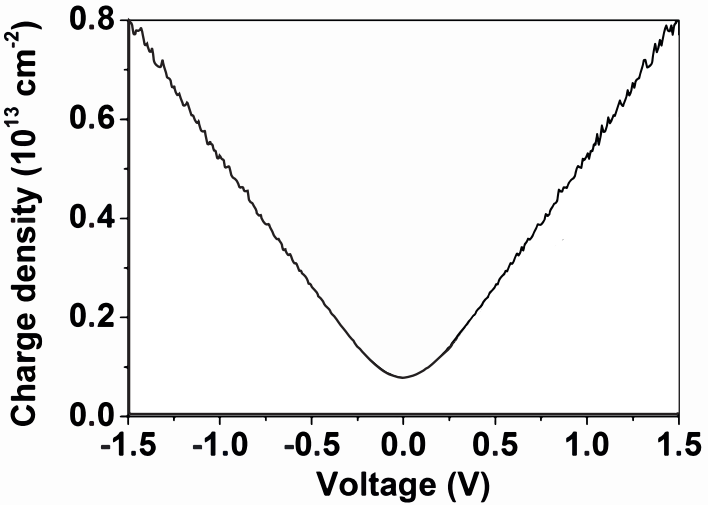


Figure 4.4: Charge density modulation by voltage bias, in a quantum capacitor with the geometry D1 (Table 4.4).

4.3 Model

4.3.1 Quantum Capacitance Model

The expression of quantum capacitance can be derived as [193]:

$$C_{\mathrm{q}} = \frac{2e^2 k_B T}{\pi(\hbar v_{\mathrm{F}})^2} \ln\left[2\left(1+\cosh\frac{eV_{\mathrm{ch}}}{k_{\mathrm{B}}T}\right)\right] LWN \tag{4.1}$$

where e is the electron charge, V_{ch} is the average graphene potential, k_{B} is Boltzmann's constant, $\hbar$ is the reduced Planck constant, v_{F} is the Fermi velocity, and N is the number of gate fingers. L and W are geometrical parameters defined in Figure 4.6.

4.3.2 Electrical Equivalent Model

The device can be modeled by the circuit in Figure 4.5.a, which can be further detailed as in Figure 4.5.b.

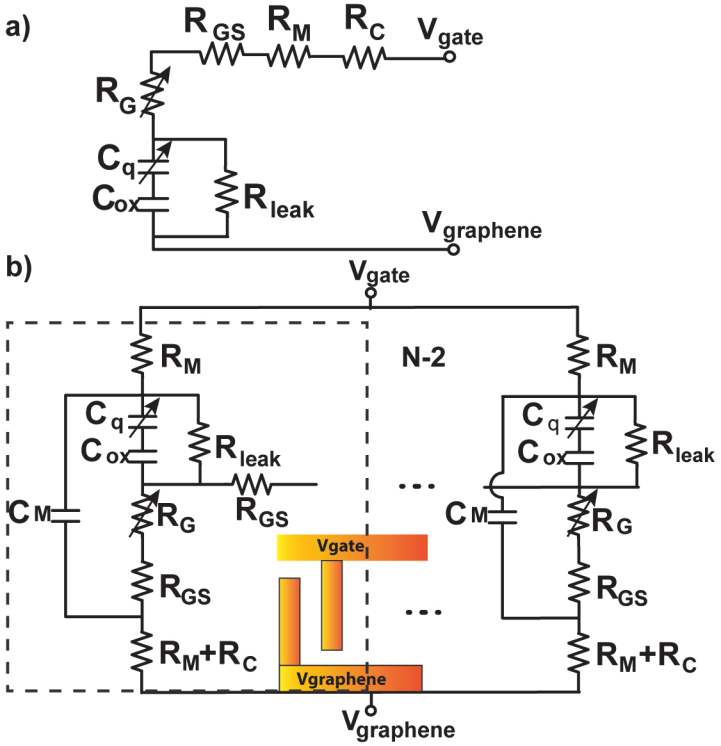


Figure 4.5: a) Lumped circuit model used to extract the total capacitance and series resistance from the impedance measurements. b) Detailed circuit model.

4.4 Design

In an attempt to gain a deeper understanding of the quantum capacitance from a device perspective, as well as of the effect of scaling on the device performance, different GQC geometries are considered in a top gate configuration shown in Figure 4.6, using a multi-finger design in order to increase the capacitance while minimizing the graphene series resistances, by reducing the graphene length the current needs to pass through. The figure presents the schematic of the geometry, where L is the finger length, W the finger width and S the spacing between the graphene contact and gate fingers.

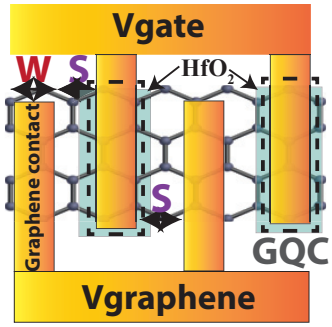


Figure 4.6: Top view of the device indicating the geometry.

Table 4.4: Devices geometries and effective areas.

Device no	No fingers	Width (nm)	Spacing (nm)	Length (µm)	EOT (nm)	Area (µm^2)	Effective area (µm^2)
1	9	500	300	30	2.48	414	252.5 (61%)
2	12	500	300	30	2.52	558	340.4 (61%)
3	9	500	300	20	2.50	276	171.1 (62%)
4	6	300	300	30	2.45	198	108.9 (55%)
5	6	500	300	30	2.52	270	143.1 (53%)
6	6	1000	300	30	2.52	450	261 (58%)
7	12	1000	300	30	2.49	918	587.5 (64%)
Opt. geometry	270	70	70	3	2.5	226	140.1 (62%)
Opt. geometry + 0.5 nm EOT	120	70	70	3	0.5	100.4	62.2 (62%)

The geometries of the devices fabricated in this work (D1-D7) are summarized in Table 4.4. The effective areas of the devices and the EOTs resulted from the fit to the model are also presented.

Figure 4.7 summarizes the effects of the main geometrical parameters on performance. It can be observed that finger length L and width W influence the capacitance values by modifying the area, but have no influence on the tuning range. However, reducing L and W is beneficial to obtain a higher and wider-band Q, due to reduced finger resistance (part of the series resistance of the quantum capacitor) and, respectively the capacitance.

It is interesting to observe that for small finger dimensions, their resistance becomes dominant, being more important than the effect of the graphene resistance. For this reason, increasing the finger thickness also has a beneficial effect on the Q.

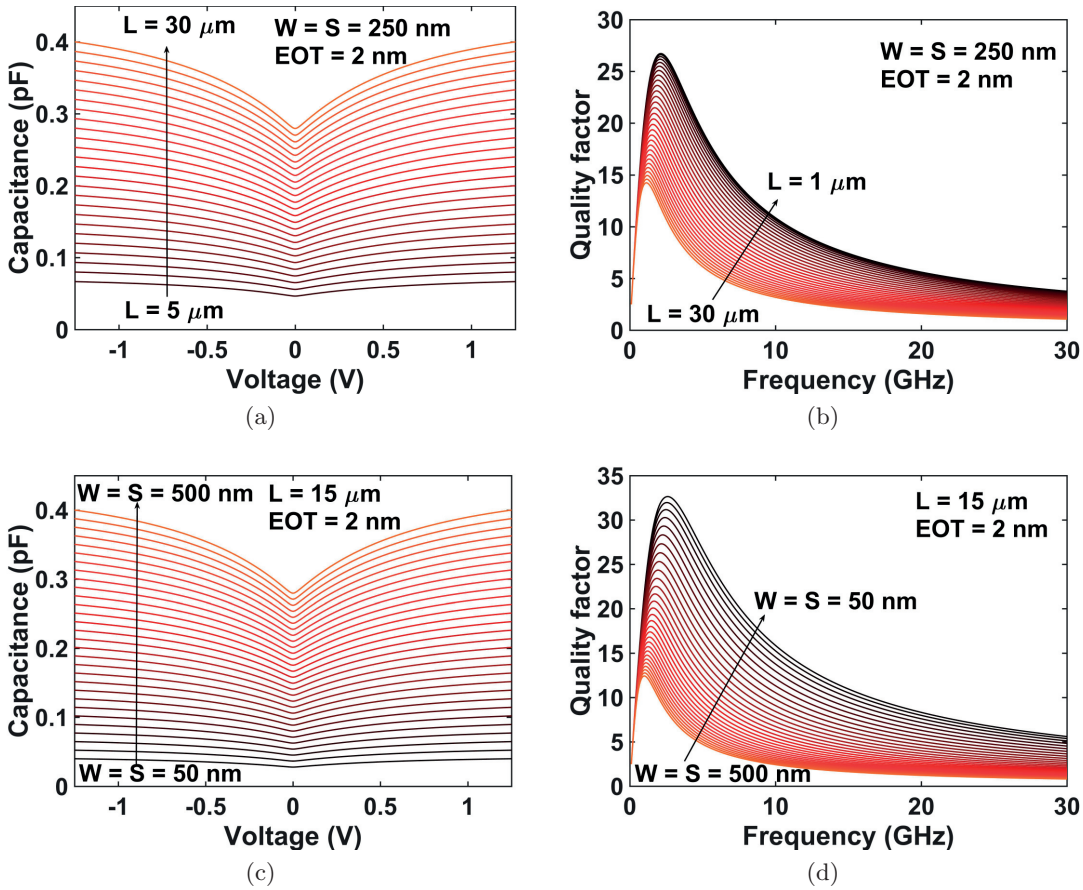
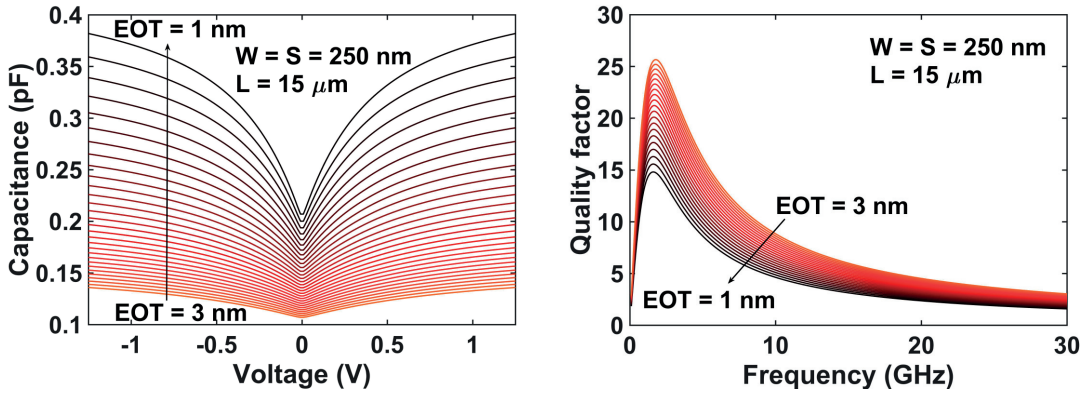


Figure 4.7: The main figures of merit of the GCQ in function of the geometry. Influence of finger length L on: a) Capacitance values vs voltage b) Q-factor vs frequency. Influence of finger width, W, and spacing, S on: c) Capacitance values vs voltage d) Q-factor vs frequency.



(a) (b)

Figure 4.8: Influence of EOT shown for values between 3 and 1 nm on: a) Capacitance values and tuning ratio vs. voltage b) Q-factor vs. frequency.

The dielectric of the capacitor has an essential influence on the performance, it needs to allow a high biasing range at a very low thickness, with low losses. The effects of scaling down the oxide thickness are presented in Figure 4.8. It can be observed that a thinner EOT significantly improves the tuning range, with a detrimental effect on Q, due to higher losses. A trade-off must be carefully chosen depending on the desired application.

As it can be observed, scaling down the dielectric is required to achieve a good tunability, for this reason it is essential to obtain thin, high quality dielectrics. Similar to the GNEMS, HfO_2 is chosen due to its high dielectric constant and low losses. Different thicknesses of HfO_2 have been deposited by ALD and characterized in MIM configurations (of areas of $100 \times 100\,\mu m$). The results are presented in Table 4.5. It is observed that below 10 nm a lower dielectric constant is measured, possibly due to imperfections in the thin oxide layer. For this work, a thickness of $\approx$10 nm is targeted.

Table 4.5: HfO_2 Characterization.

Thickness (nm)	Ellipsometry (nm)	Breakdown voltage (V/nm)	Permittivity	Resistivity DC (Ω·m)	Resistivity AC (Ω·m)
10	10.8	-0.60, +0.45	19.5	4.3×10^{11}	1.4×10^{8}
5	5.9	-0.67, +0.5	12.5	1.5×10^{11}	1.6×10^{8}
3	4.0	-0.95, +0.5	12.8	2.1×10^{7}	2.4×10^{7}

4.5 Fabrication

The fabrication process is designed at full wafer scale, using graphene obtained by chemical vapour deposition (CVD), and is detailed in Figure 4.9. The substrate is ultra-high resistivity silicon ($> 10\,\mathrm{k\Omega{\cdot}cm}$), covered by 90 nm of thermally grown silicon oxide in order to minimize losses in the substrate. The device active regions were patterned using electron beam lithography and etched by 15 s of oxygen plasma (Figure 4.9a). The metal fingers contacting graphene and the top gates were fabricated by a lift-off process of Titanium/Palladium/Gold (Ti/Pd/Au) (5 nm/20 nm/40 nm) (Figure 4.9b and Figure 4.9d). The Pd/Au stack is used to minimize the contact resistance. The dielectric on top of graphene is constituted of 5 nm HfO_2 deposited on a seed layer of 1.5 nm Al thermally oxidized at 120 °C for 6 h (Figure 4.9c). A SEM of the final device with a zoom on the active area is presented in Figure 4.10.

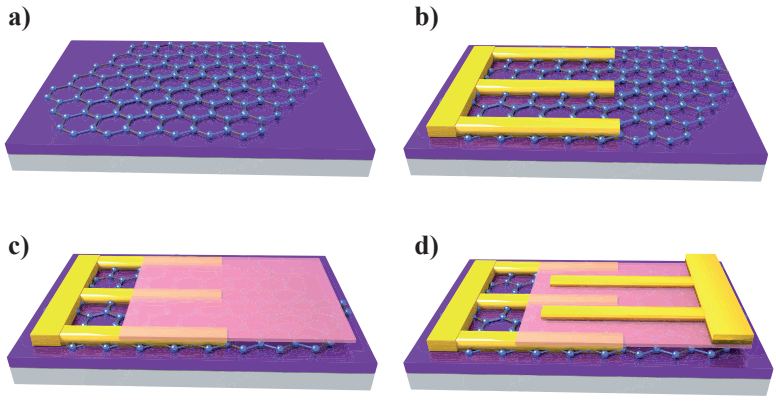


Figure 4.9: The fabrication flow of the capacitor in a top gate configuration. a) Graphene transfer on Si/thermal SiO_2 substrate. b) Lift-off Ti/Pd/Au contacts on graphene c) ALD HfO_2 on 1.5 nm thermally oxidized Al d) Lift-off of Ti/Pd/Au as top gate.

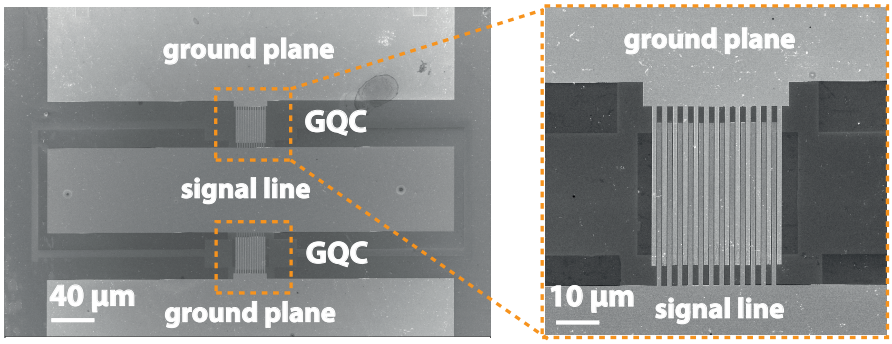


Figure 4.10: SEM of the final device D3, showing the CPW and the GQCs.

4.6 Characterization

The 7 different devices geometries are characterized in RF by S-parameters measurements up to 10 GHz and impedance measurements up to 3 GHz. In order to remove the losses we have performed a TRL calibration for the S-parameter measurements and a SOLT calibration for the impedance analyzer measurements.

The characterization is done in vacuum using an Impedance Analyzer E4991A connected to a PMC 150 Suss Microtech probe station at room temperature. We apply a DC bias in the range of -1.25 to +1.25 V which corresponds to average electron and hole densities of $n_c = \pm 1 \times 10^{13}\,\mathrm{cm}^{-2}$, to study the quantum capacitance in both the positive and negative regions. To offer a benchmark for this technology we study the main figures of merit of tunable elements, focusing on tuning ratio, quality factor, variation with temperature and linearity of capacitance tuning with voltage.

High Frequency S-parameters Characterization

The high frerquency measurements, up to 10 GHz, were performed using a VNA E8361A. The S-parameters of 3 devices are presented in Figure 4.11, showing the minimum and maximum state for the capacitance. We obtain low losses at low frequency, indicating a low series resistance. The dashed lines indicate an excellent fit to the circuit model, and the extracted parameters are presented in Figure 4.12

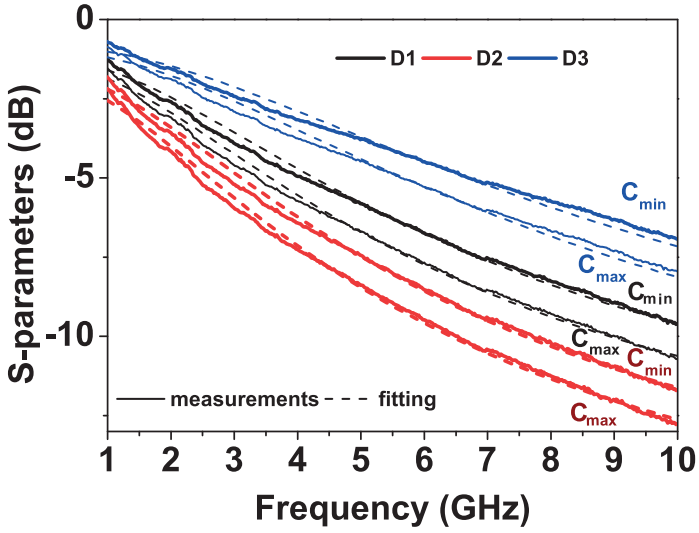


Figure 4.11: S_{21} measurements of D1, D2, D3.

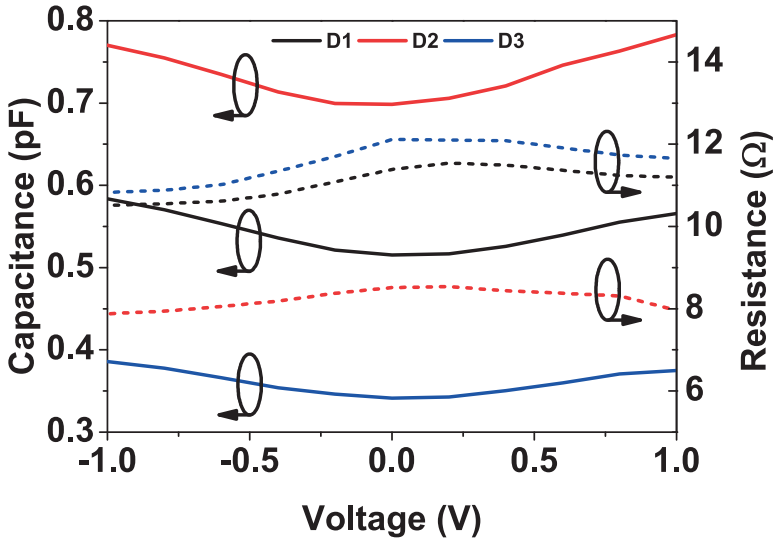


Figure 4.12: Extracted device parameters: R_s, C_q, from S parameters, using the lumped circuit model in Figure 4.5.

Figure 4.12 shows the equivalent capacitance C_q and resistance R_s, extracted using the lumped circuit in Figure 4.5.

Impedance Spectroscopy Characterization

Characterization at 3 GHz

The peak-to-peak amplitude of the AC voltage is 10 mV and the frequency 3 GHz. Figure 4.13 shows the variation of C_q (4.13a) and R_s (Figure 4.13b) with voltage for all the fabricated devices. Consistent with the theory, GQC shows non-zero minimum at the Dirac point, and a quasi-linear increase on both sides, until it begins to saturate at higher voltages. The curves are not perfectly symmetric due to the chemical hole doping from the metal contact in the electron region. However, the differences are very small, which indicates that the contact resistance is almost negligible. The capacitance density of our C_q is in the range 1.70–2.97 fF/µm^2, which is more than 100 times higher than in MEMS capacitors.

The measurements are very well matched to the equivalent lumped circuit shown in Figure 4.5. The capacitance between the metal fingers is not included in the model, as it is in the order of tens of fF and therefore it is negligible. The measurements are fitted to the model using the EOT and the effective area as adjustable parameters. Additionally, in order to emulate the dispersion of the charge density in graphene (discussed in §2.3.1), we consider a normal distribution of the chemical potential along the sample, and add the chemical potential standard

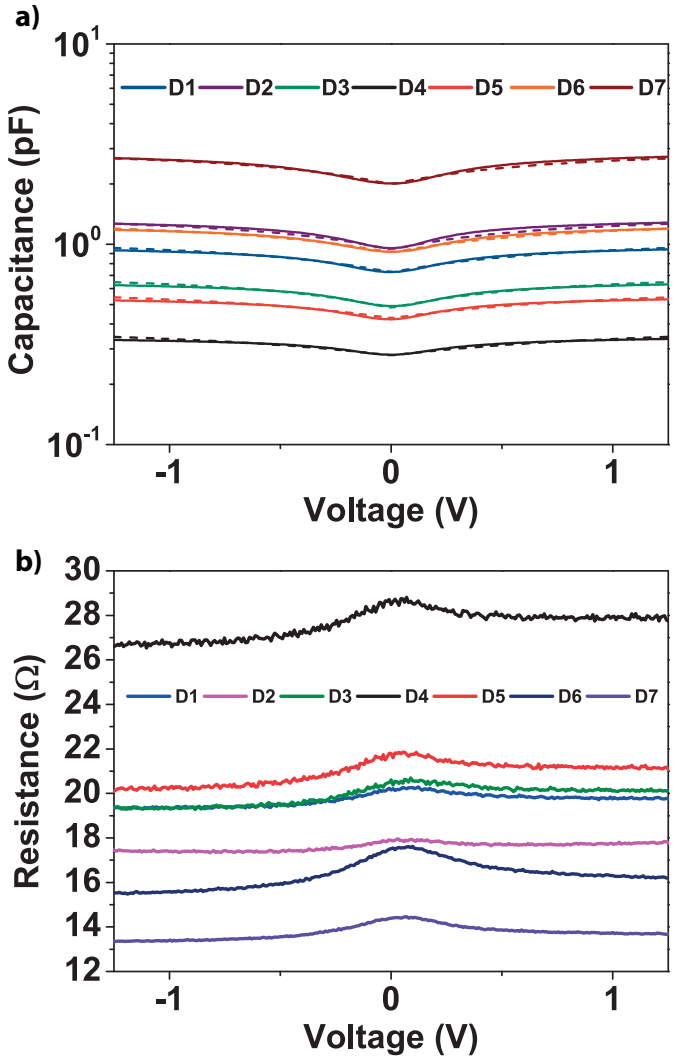


Figure 4.13: a) Capacitance and b) resistance of all the 7 measured devices. The dashed lines show a good fit to the circuit model.

deviation σ, as an adjustable parameter in the model. We have investigated in detail the graphene non-uniformity in Section 2.3.1, where we obtain a variation of around 50 meV along the sample [194]; here we obtain a deviation up to 160 meV, higher than the results we have previously observed for CVD graphene on SiO_2, possibly due to the post-processing steps or to the larger areas investigated. We perform an individual fit for each device considering the graphene variability in different regions and oxide non-uniformity along the wafer ($\pm$0.03 nm EOT). The effective area is smaller than expected due to graphene delamination, tears during transfer and post-processing. The dielectric leakage has an important effect on performance, and the values are shown in Table 4.6.

Table 4.6: Leakage resistance of the GQCs.

Device	D1	D2	D3	D4	D5	D6	D7
$R_L(\Omega)$	6023	4586	8960	16498	10566	4827	2161

At high voltage, the measurements show a higher saturation than predicted by the model, possibly due to an increase in leakage with voltage,which is not considered in our model. A more complex model is needed to account for the effect of leakage dependence of high voltage, interface traps, and other imperfections between the graphene and HfO_2.

Frequency Response

Figure 4.14.a shows the Q-factors versus frequency for all the devices. The Q of a tunable capacitor can be calculated as the ratio between the imaginary and the real part of the admittance:

$$Q = \frac{\mathrm{Imag}(Y)}{\mathrm{Real}(Y)} \tag{4.2}$$

Q varies with frequency following the analytical formula:

$$Q = \frac{\omega C}{\omega^2 C^2 R_\mathrm{s} + R_\mathrm{s} G_\mathrm{L}^2 + G_\mathrm{L}} \tag{4.3}$$

where C is the total capacitance, R_s is the series resistance (graphene, contact and metal finger resistance) and $G_\mathrm{L} = 1/R_\mathrm{leak}$ is the leakage conductance. Compared to previous experimental data on graphene, we obtain record Q-factors up to 14 at 0.6 GHz and 12 at 1 GHz for device D3 and 9 and 9.2 respectively for devices D1 and D2 at 1 GHz, showing an improvement in Q due to reduced series resistance, given by reduced finger length in this particular case. Comparing devices D2 and D3 we observe that the number of fingers does not have an important effect on Q. Q's dependence on finger area and quasi-independence on the number of fingers suggests that GQCs can be scaled to any value by modifying the number of fingers without degrading Q. The capacitance has a low dependence of frequency as seen in Figure 4.14.b. The peak of the Q is given by the dependence of the series resistance on frequency (Figure 4.14.c).

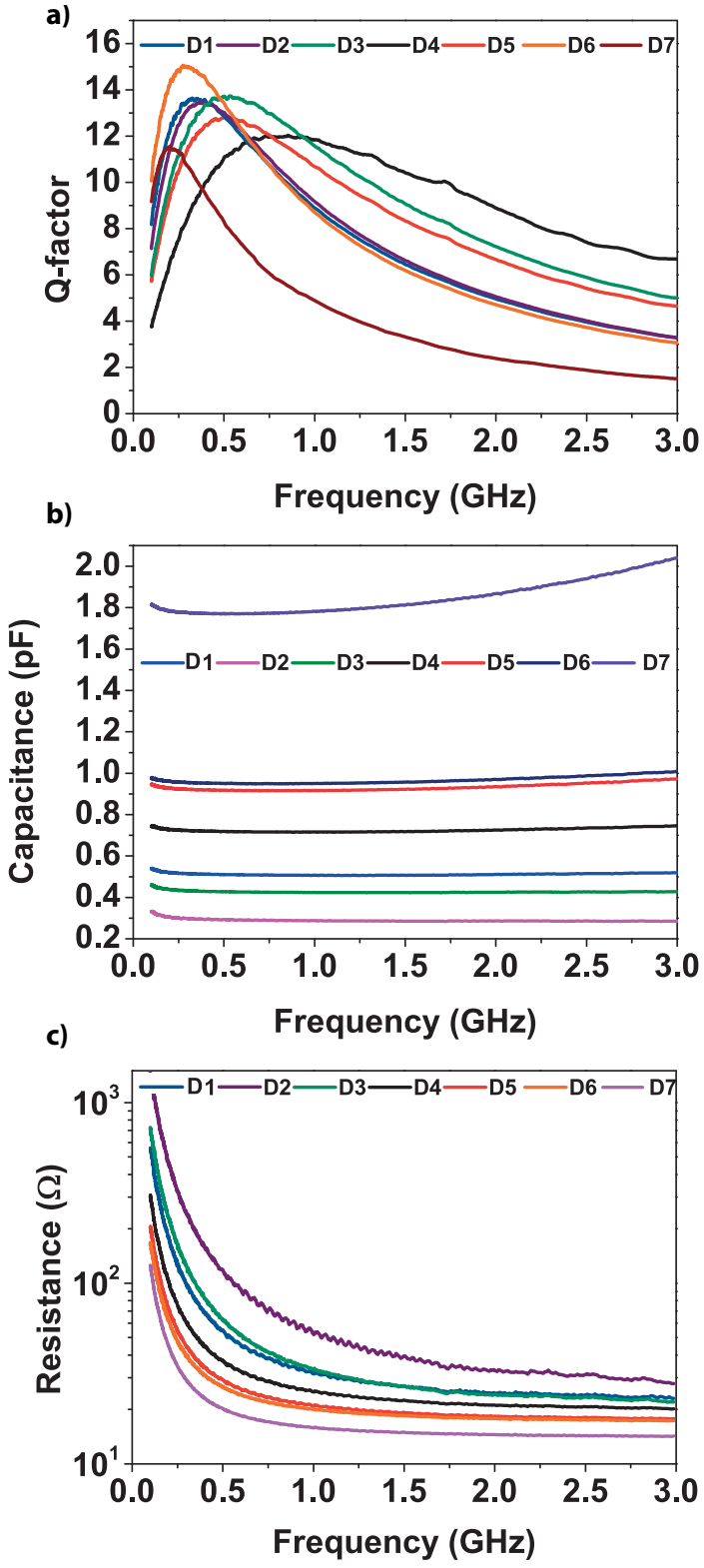


Figure 4.14: Variation of a) Q, b) Capacitance and c) Resistance with frequency for the 7 fabricated devices.

Performance evaluation

Next, the characterization of three devices D1, D2 and D3, obtained by varying the number of fingers between device D1 and D2, and the finger length between devices D1 and D3, is described, in order to systematically study the performance effects of device geometry. Figure 4.15 shows the capacitance density variation with voltage and the characteristic derivative, representing the slope, for device D1, which is almost identical for all the presented devices, with a small variation of $\pm 0.25\,\mathrm{fF/\mu m^2}$ due to graphene and dielectric nonuniformities and defects. We observe a linear increase on both sides of the Dirac point until $\pm 0.5\,\mathrm{V}$, with relatively abrupt slopes, as shown in the inset, decreasing when approaching Dirac point. We obtain a tunability of around 7 % in the linear range, with slopes up to $1.13\,\mathrm{fF/(\mu m^2\,V)}$ in the negative region and $1.25\,\mathrm{fF/(\mu m^2\,V)}$ in the positive region, in a linear range of around 100 mV. Beyond this voltage the dependence is non-linear but enables significant tuning with low voltage (1.3:1 at 1.25 V).

The GQC is constituted of the tunable graphene quantum capacitance, C_q, in series with the fixed oxide capacitance, C_ox. Figure 4.16 shows the two capacitance value separately. By reducing the oxide thickness the tuning range can be significantly improved and values higher than 4 were demonstrated theoretically for an EOT of 1 nm [190].

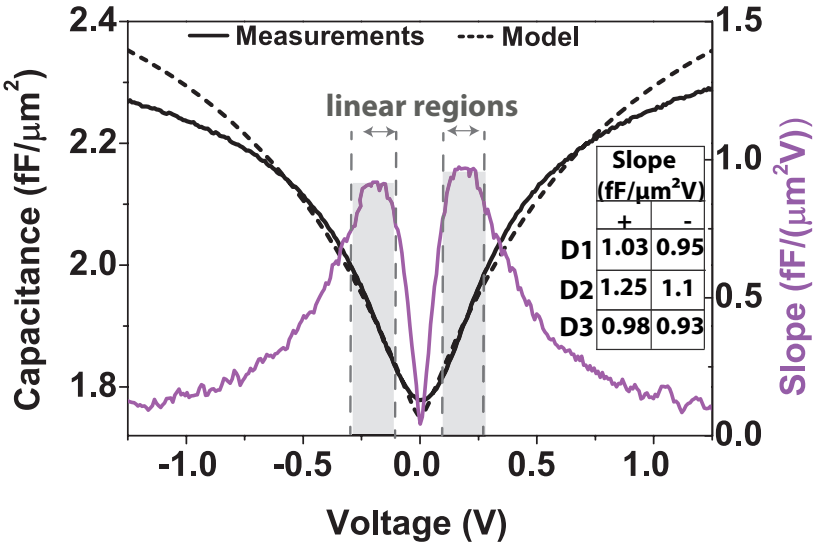


Figure 4.15: Capacitance density dependence on voltage; slope of the CV characteristic given by the derivative. Inset: slopes of D1, D2, D3 positive and negative characteristics.

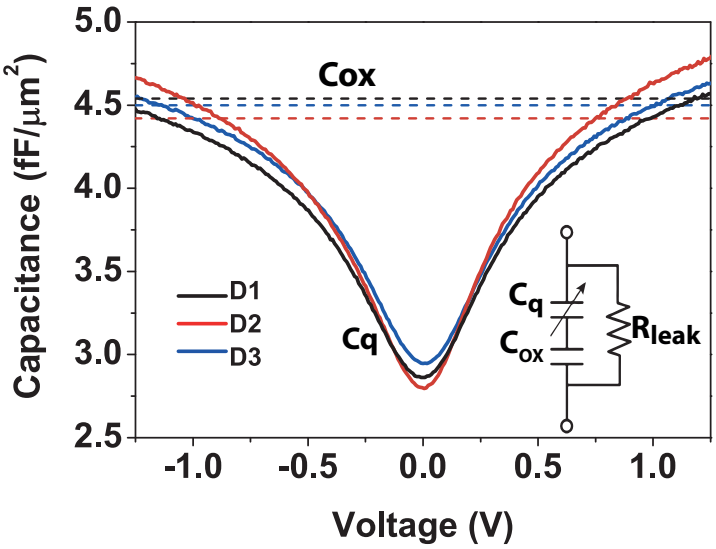


Figure 4.16: Capacitance density dependence on voltage; extracted quantum capacitance, C_{q} and oxide capacitance, C_{ox} from the total device capacitance.

Temperature Dependence

Another major figure of merit of GQC to be assessed for RF applications is the inherent temperature dependence; the dependence of applied bias, tuning range and Q-factor should be minimal. In monolayer graphene, the intrinsic density of electrons/holes does not depend on temperature following Arrhenius law; it has a T^2 dependence, due to the absence of a band gap, and to the linear energy dispersion [193]. In Figure 4.17 we observe that decreasing the temperature toward the cryogenic regime improves the tuning range, from 1.27 at 350 K to 1.38 at 150 K, due to the dependence of the charge density and Dirac point on temperature. Near the Dirac point, the capacitance value shows a strong temperature sensitivity, while at higher bias levels, temperature variations cause very small changes in the characteristics. Measurements show that the C_{min} and C_{max} capacitance change is less than 5 % and the tuning range variation is approximately 8 % when the temperature is varied from 150 K to 350 K.We observe a slight shift, of less than 110 mV, of the gate voltage at the Dirac point as the temperature decreases. This can be attributed to the fact that the minimum quantum capacitance is affected by the thermal activation of carriers and the formation of electron-hole puddles.

Q increases quasi-linearly with the decrease in temperature (Figure 4.18), due to the decrease in capacitance; the effect of resistance is reduced due to the multi-finger geometry, the finger resistance dependence on temperature dominating on graphene series resistance. At higher frequencies the variation of the Q is moderate, obtaining less than 13 % at 3 GHz. The results

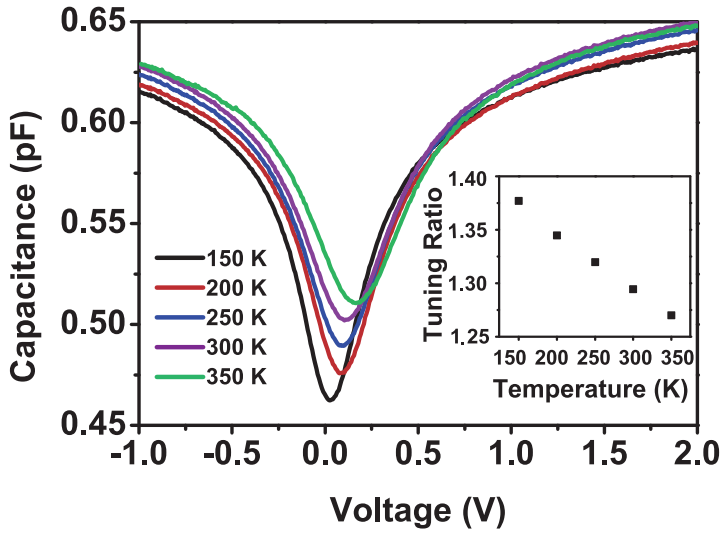


Figure 4.17: Capacitance versus voltage from 150 K to 350 K. Inset: capacitance ratio (C_{max}/C_{min}) giving the device tuning ratio as a function of temperature.

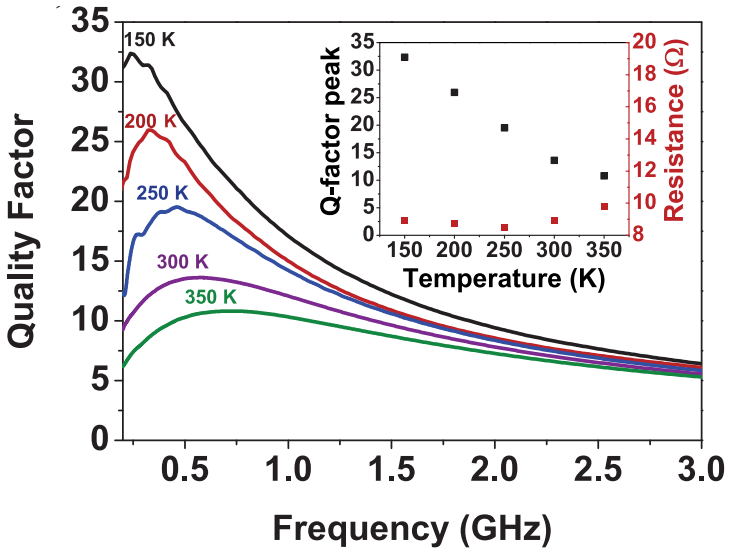


Figure 4.18: Q-factor variation with temperature; inset: dependence of Q-peak and R_s on temperature.

indicate that the capacitance values have little dependence on temperature, between 150 K and 350 K, if operated further from the Dirac point and the obtained values are superior to MEMS variable capacitors and semiconductors.

Annealing

To overcome the variability of the devices due to impurity dopants and water we perform a thermal annealing process for 6 h at 80 °C in vacuum (10^{-5} mbar). This shifts the Dirac point towards 0 V while improving the Q as shown in Figure 4.19. We show the subsequent annealing effect after 4, respectively 6 h at around 80 °C.

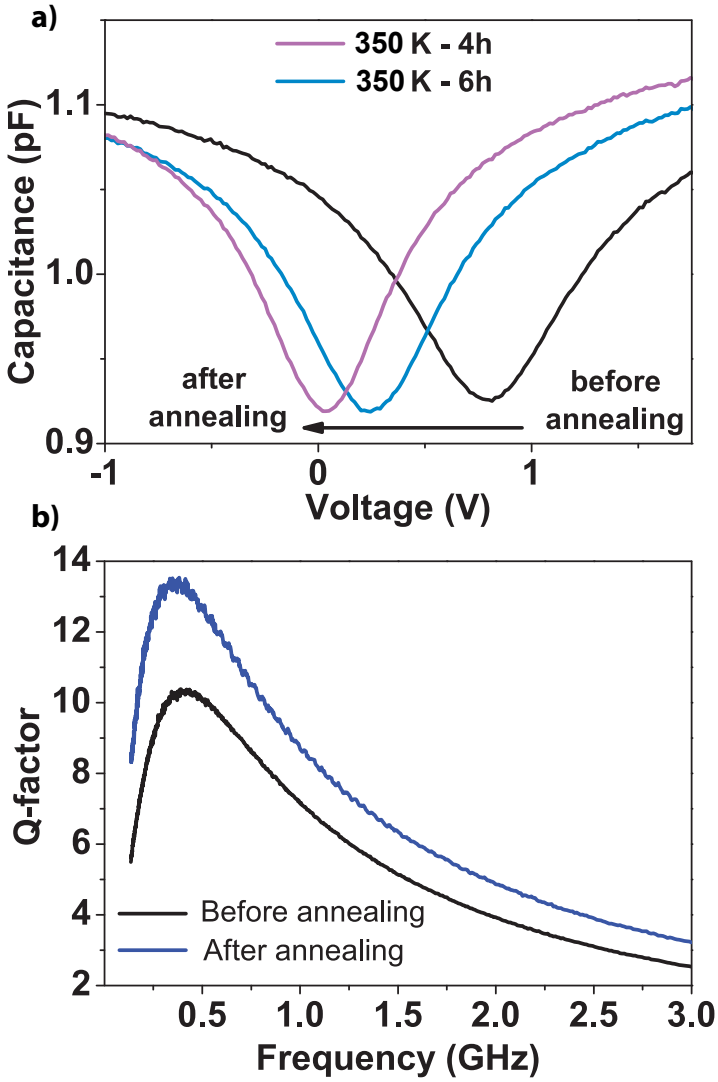


Figure 4.19: Annealing device D5 for 6 h at 340 K; a) CV characteristic evolution with annealing b) We obtain an increase in Q-factor after annealing, consistent with the decrease in capacitance.

We observe that by removing water and impurities trapped at the interface and on graphene, we decrease the capacitance and shift the Dirac point towards 0 V, consistent with decreasing the number of charge carriers. We observe a decrease in the minimum capacitance and an improvement in Q from 10.45 up to 13.64 at 0.38 GHz due to the decrease in capacitance. The series graphene resistance increases during annealing due to the dopant removal, however the contact resistance is improved, leading to a decrease of the total series resistance, further increasing the Q.

4.7 Optimisation

The results obtained led us to propose a systematic approach to achieve an optimised design with a significantly improved performance. We discuss the main figures of merit, their influence on performance and a route towards a performance boost trough an additive approach. In Figure 4.20 we show the device optimisation and the effect of each parameter by adding one improved geometrical parameter at a time and keeping the capacitance value constant. We start the optimisation process from the geometry correspondent to device D3. Decreasing the fingers area and inter-spacing leads to an increase of the Q by reducing the series resistance. The main concern for the design was the high series resistance of graphene but we observe that the metal finger resistance dominates, the effect of graphene resistance being very small. The finger resistance is further reduced by increasing its thickness, thus increasing Q. With an optimised geometry involving 70 nm $\times$ 3 µm finger area and a 70 nm finger thickness, we reach by calibrated simulations a Q of 44 at 1 GHz, 122 at 5.3 GHz and above 50 from 1.1 to 24.8 GHz, with a capacitance density of 2.78 fF/µm^2. Thus we obtain a 8-fold increase in Q peak and wideband performance. These values are obtained without a trade-off in tuning range, which is independent of the geometry.

Next, the effects of EOT scaling and disorder in graphene (dispersion of chemical potential) on tuning range and Q-factor are studies and the main trade-offs in performance are discussed. Figure 4.20.b shows a strong decrease of the Q-factor at the Dirac point with these two parameters, optimised to maximize the tuning ratio as discussed in the following figures. To improve the tuning range of the devices, the EOT can be scaled down. Graphene quality plays an important role in performance as well, since less disorder results in a higher tuning ratio.

Figure 4.21 shows the tunability improvement by decreasing EOT, obtaining values as high as 2.6 for 0.5 nm EOT. The linearity is improved as well, obtaining a slope of 24 fF V/µm leading to a tunability of 18 % within 30 mV (Figure 4.22). This leads to a decrease in Q due to the leakage in the oxide. Unlike in [190] (at MHz frequencies), where R_s is dominant on the leakage due to the micrometric scale of the capacitor fingers, when working at GHz frequencies we need

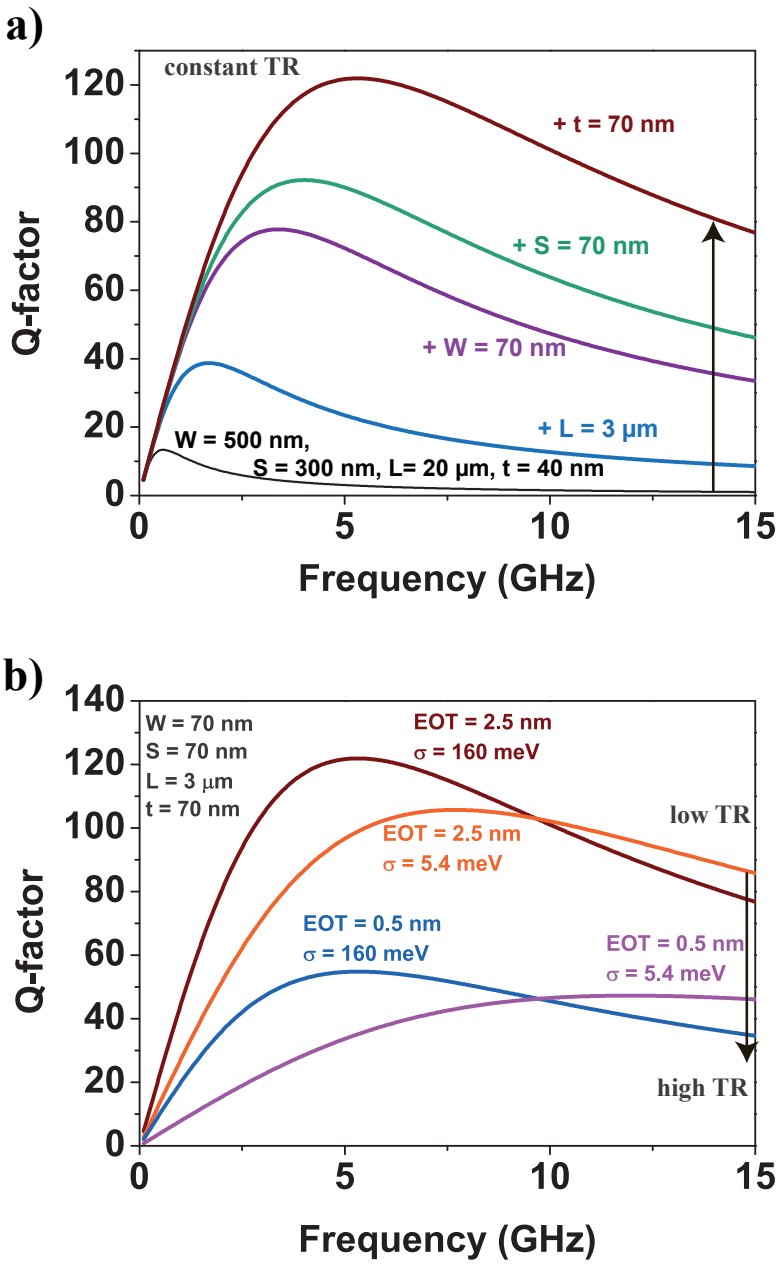


Figure 4.20: a) Optimisation of the Q-factor with device geometry, starting from device D3 and keeping the C value constant. The addition of each indicated parameter leads to an improvement in performance, by minimizing the fingers and graphene series resistance b) Trade-off of Q-factor with tuning range.

to consider the strong dependence of Q on the leakage with shrinking EOT. G_{L} degrades Q when G_{L} is on the order of $j\omega C_q$, which shows that at low frequencies the varactors are less

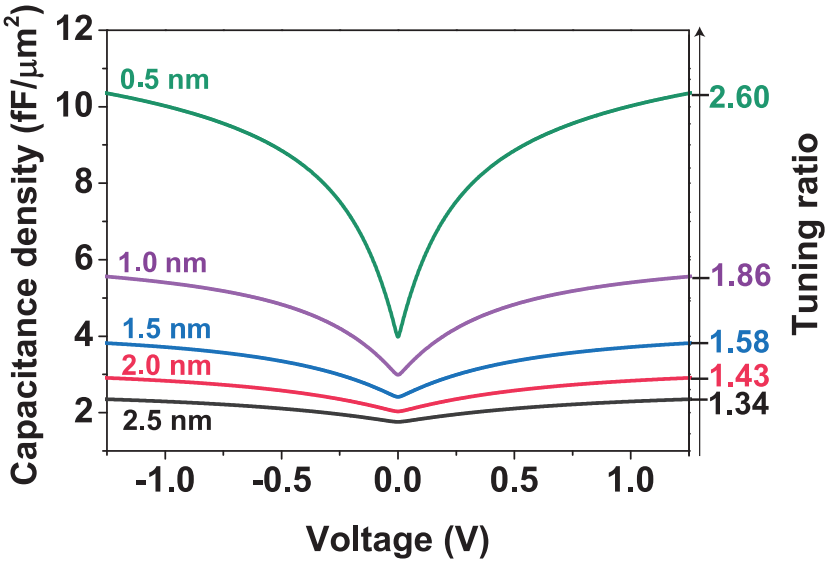


Figure 4.21: Effect of EOT on the tuning ratio.

sensitive to gate leakage relative to MOSFETs [190]. However the Q is low in this case due to the large graphene series resistance which dominates over the leakage resistance.

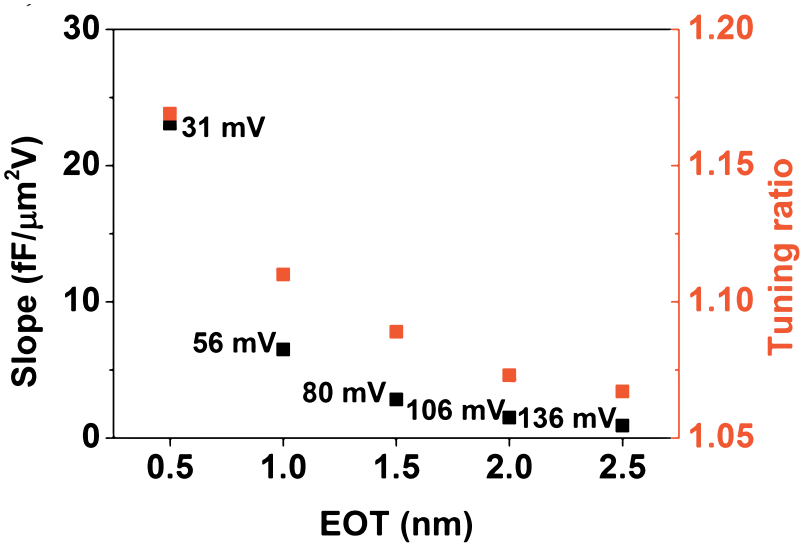


Figure 4.22: Effect of EOT on the slope (black) and maximum tuning range (red) achieved in the linear region. For each slope, the linear corresponding region is indicated.

Another important graphene characteristic that has a tremendous effect on the device performance is disorder, leading to variability of the chemical potential distribution across the sample,

originating from defects, impurities and the substrate and environment. Typical micron sized devices on SiO_2 substrates exhibit disorder chemical potential variation of around 40 meV and higher [17, 150]. Eliminating the effect of the substrate, 1.2 meV disersion has been achieved in suspended graphene [195]. However, suspended graphene has a few inherent limitations for devices such as: their area is limited to micrometers and the difficulties to fabricate multi-terminal devices [196, 197], top gates [197] and nano-structures [198].

One solution is to use h-BN as a substrate for graphene, which leads to a standard deviation of the chemical potential of 5.4 meV [199], value used as the minimum realistic value in our model. Various advances have been obtained in this direction, significantly improving the disorder in graphene by h-BN encapsulation [195, 200, 201].

Figure 4.23 shows the effects of disorder on the CV characteristics and tuning range. We observe a significant increase in tunability, up to 2.28, for minimum disorder in graphene. The curves are steeper, leading to an improved linearity as shown in Figure 4.24, which implies that a higher tunability is reached with a significantly reduced voltage.

However, this causes a decrease in Q at the Dirac point, due to the increase in resistance, so a trade-off must be chosen carefully depending on application. The influence of EOT and disorder on the tuning ratio are depicted more clearly in Figure 4.25, showing a dramatic increase in tuning ratio for low EOT and low disorder, up to 7 in an ideal case.

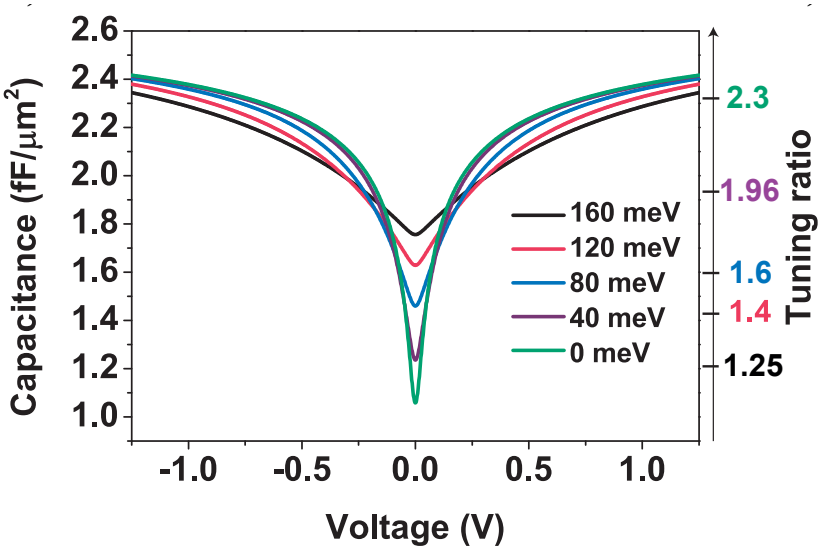


Figure 4.23: Effect of disorder in graphene on the tuning ratio.

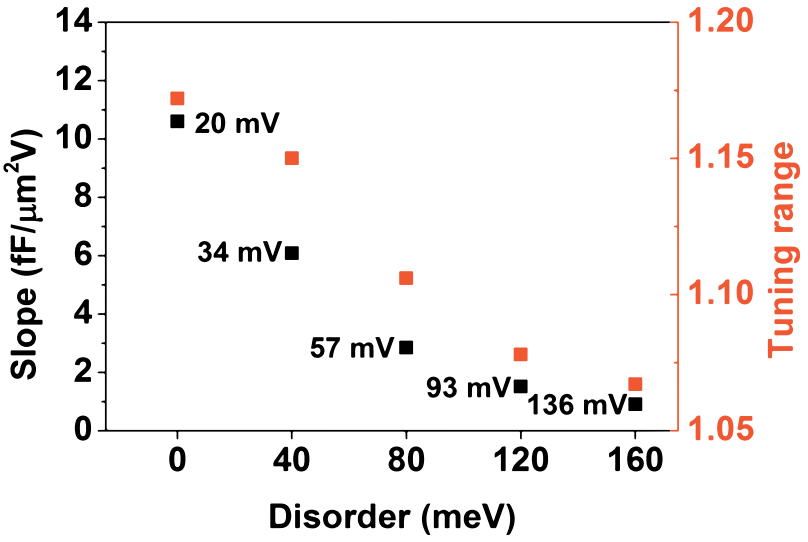


Figure 4.24: Effect of disorder in graphene on the slope (black) of the characteristic in the linear range and maximum tuning range (red) achieved in the linear region. For each slope, the extent of the corresponding linear region is indicated.

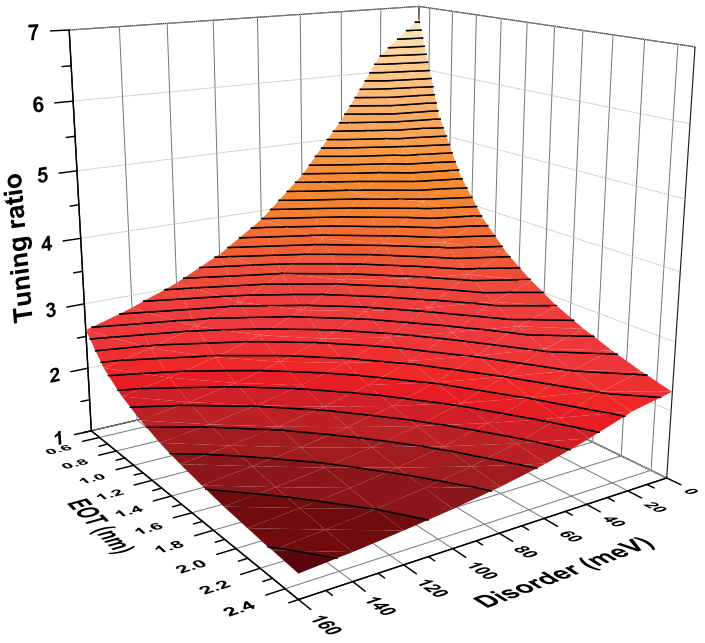


Figure 4.25: Effect of disorder in graphene and EOT on the tuning ratio.

4.8 Discussion

The device performance for the various geometries is summarized in Table 4.7. The optimised designs are also included to give a clear indication of the trade-offs between maximizing Q and maximizing the tuning ratio. It can be observed that the tuning ratio is not affected by the geometry, the small variation resulted from the non-uniformity of the EOT along the wafer. The tuning range can be improved by scaling EOT as discussed. As detailed in the Section 4.7, scaling the fingers geometry achieves a wide-band Q, with a peak approaching 122 at 5.3 GHz.

Table 4.7: Performance of the measured and optimised tunable capacitors.

Device	**Fitted parameters**				**Performance**	
D no	**C_{min} (pF)**	**C_{max} (pF)**	**C_{max} (fF/µm^2)**	**R_{series} (Ω)**	**Tunability**	**Q_{peak}**
1	0.727	0.943	2.278	26.5	1.30	13.6 (@350 MHz)
2	0.956	1.282	2.298	20.1	1.34	13.5 (@380 MHz)
3	0.492	0.630	2.283	19.3	1.28	13.7 (@550 MHz)
4	0.287	0.337	1.702	17.3	1.17	12 (@800 MHz)
5	0.422	0.531	1.967	19.3	1.26	12.5 (@500 MHz)
6	0.917	1.195	2.655	15.5	1.30	15 (@280 MHz)
7	2.019	2.733	2.977	13.3	1.34	11.6 (@200 MHz)
Opt. geometry	0.492	0.630	2.783	0.11	1.28	122(@5.3 GHz)
Opt. geometry + 0.5 nm EOT	0.494	1.284	12.789	0.17	2.59	55(@5.3 GHz)

4.9 Benchmarking

In order to assess the real potential of GQC we benchmark it against alternative technologies such as MOSCAPs and MEMS, considering the same capacitance value, achieved by the technologies and geometries indicated in Figure 4.26.

In Figure 4.26a we compare the CV characteristics of GQC D2 with a 180nm CMOS process MOSCAP and a traditional parallel-plate MEMS tunable capacitor, with comparable capacitance values and operation voltage ranges. The MOSCAP has a larger EOT value of 4 nm, and

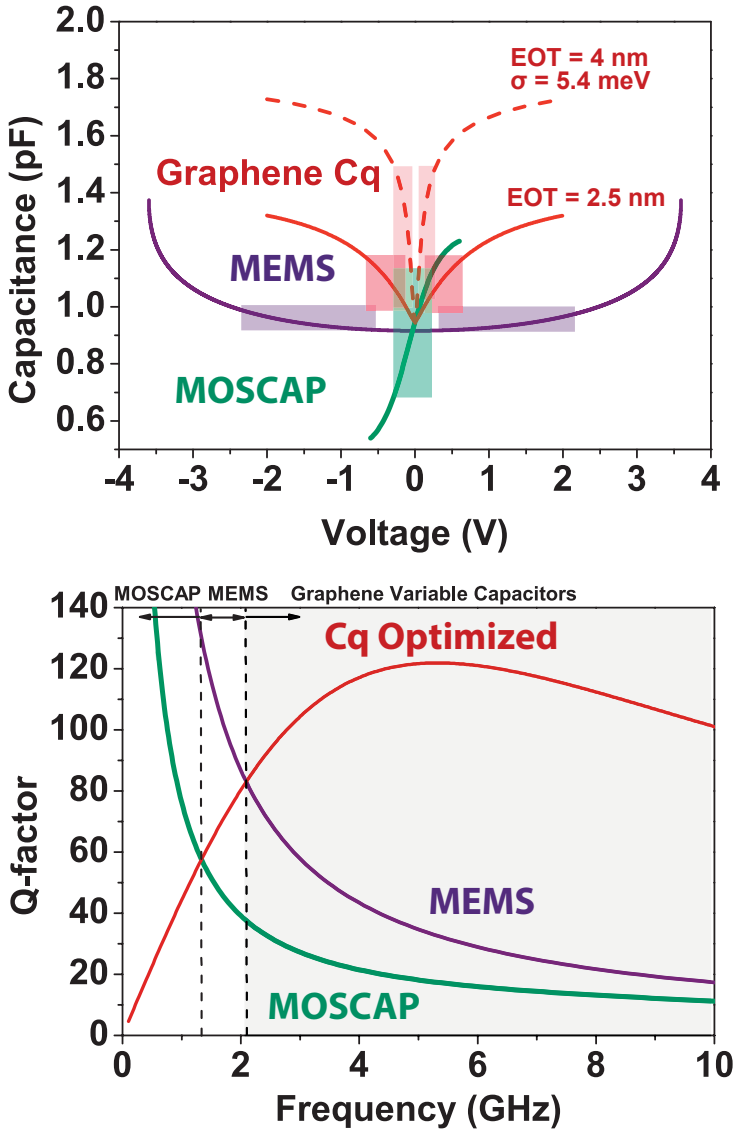


Figure 4.26: Benchmarking of C_q against MEMS and MOSCAPs considering the tuning range, linearity of capacitance dependence on voltage and Q-factor. MOS: 180 nm technology; EOT=4 nm. MEMS: double-clamped with $L = 250\,\mu m$, $W = 100\,\mu m$, gap $= 1\,\mu m$, $k = 10\,N/m$ values, thus having an area 150 times larger than the C_q to achieve the same capacitance value. a) Tuning behavior of GQC, MOSCAP, MEMS having the same capacitance value at 0 V. The linear regions are highlighted on the plot. b) Comparison of Q-factor dependence of frequencies for the different technologies.

a tuning ratio of 2.3:1 within 1.2 V, higher than the measured device due to the high disorder observed in graphene. However, we show that a low disorder GQC with the same EOT of 4 nm would give a comparable tunability (1.8:1) in the same voltage range. Moreover, we have

demonstrated in the optimisation section, the potential to reach tuning ratios as high as 7:1 with an encapsulated device and a scaled EOT (Figure 4.25), much higher than the one of conventional parallel-plate MEMS tunable capacitors, limited to 1.5:1. Values up to 8.4:1 have been achieved with MEMS tunable capacitors based on comb-drive actuators [202], but with relatively low Q-factors at high frequency [202–204].

GQCs offer a dramatic improvement in performance at high frequency with respect to alternative technologies as shown in Figure 4.26b, where we use the theoretical optimised geometry and obtain a Q-factor superior to the semiconducting counterparts at frequencies above 1.3 GHz and superior to MEMS above 2.1 GHz, without the instability point of traditional designs and implementations, and at a much lower power consumption.

Benchmarking and comparison results in Figure 4.26 suggest that GQCs offer a highly promising perspective for RF analog applications, for high frequencies where they have a superior performance compared to MEMS and MOSCAP alternatives in terms of Q and achieve a good tunability with very low voltage.

4.10 Applications

In this section, we discuss the performance of reconfigurable LC tanks using GQCs, based on calibrated simulations, as building blocks for numerous RF reconfigurable circuis such as voltage-controlled oscillators (VCOs), RF tunable filters and impedance matching networks.

In addition, the implementation of GQCs in phase shifters is experimentally investigated.

4.10.1 LC Tanks as a Building Block for RF Functions

Figure 4.27 shows calibrated simulations predictive for the performance benchmarking of high frequency reconfigurable LC tanks employing quantum capacitors, critical for industrially relevant applications such as tunable filters and voltage-controlled oscillators. The use of C_{q} enables high tuning over wide frequency bands with voltages below 1.5 V (true low power, whilst MEMS usually require charge pump ICs) with a simplified fabrication process. The optimised designs, obtained by scaling the C_{q} geometry, outperform the alternative technologies in terms of Q-factor at high frequency (Figure 4.28).

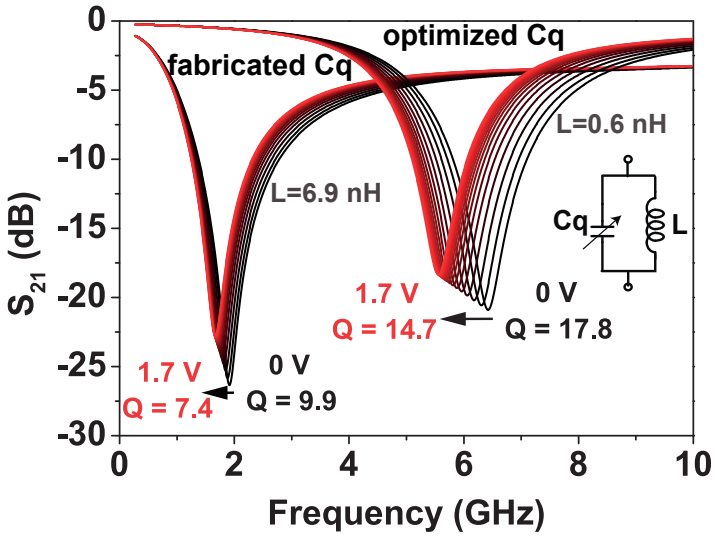


Figure 4.27: S21-parameters of reconfigurable LC tanks obtained by simulations using spiral planar inductors in 0.18 µm RF CMOS technology and tunable capacitors (fabricated D6 and optimised D6). The improvement in quality factor in the optimised design (as shown in Figure 4.27) allows the operation at higher frequencies.

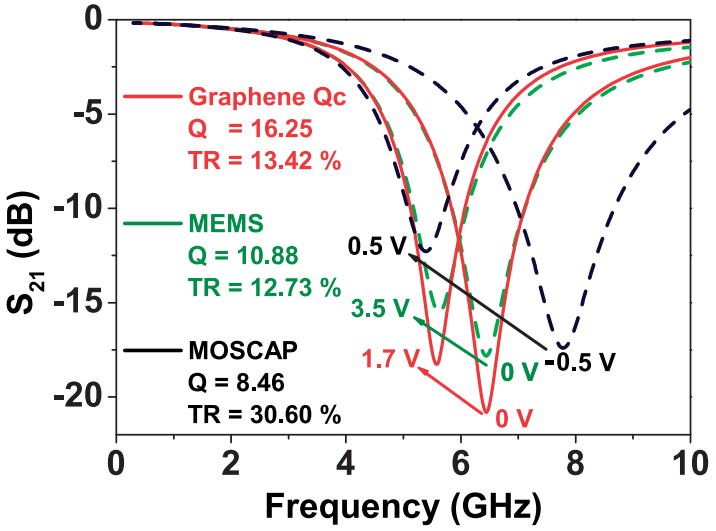


Figure 4.28: Comparison of graphene C_q and alternative technologies, showing a considerable improvement in the Q-factor of the LC resonator (given as the mean value between the two states).

4.10.2 Phase Shifter

In this section, an optimised new quantum capacitor, GQCn, geometry is fabricated, characterized and phase shifters including the GQCn are demonstrated experimentally.

As discussed in §3.9, reconfigurable phase shifters are key components in phased array antennas for microwave communications, radars, and remote sensing systems. Dynamic reconfiguration of microwave devices is in fact becoming essential for controlling antenna characteristics (e.g., coverage, polarization, frequency of operation) in real time.

In this context, low-loss reconfigurability, complexity, and cost are driving factors in the choice of a given technology. Reconfigurable phase shifters are currently implemented using several technologies, including monolithic microwave integrated circuit (MMIC), ferromagnetic, and RF MEMS.

In the previous chapter we have discussed RF GNEMS-based phase shifters and their advantages compared to metal MEMS. In short, metal MEMS-based phase shifters exhibit very low insertion loss, high linearity, and low power consumption, but their use is still limited by their reliability issues and low switching speed. Graphene NEMS on the other hand, have really high speed but exhibit high losses due to the high resistance of graphene. In this chapter we demonstrate the superior performance of the GQCs compared to alternative technologies, and experimentally analyze their potential for phase shifters.

4.10.3 Graphene Variable Quantum Capacitor

We fabricated an optimised capacitor geometry, adjusting its dimensions in order to enhance the performance, following the optimisation path described in §4.7. The capacitor structure is different than the structures described in §4.2: both sets of fingers, contacting the signal and the ground, are deposited in the same plane. Then, a thin dielectric and graphene are deposited on top. Graphene is biased by an external DC pad. The capacitor has 3 terminals (Signal, Ground of the CPW and the DC pad) and the bias is applied between the DC pad and the signal. The final structure is illustrated in Figure 4.29. In this case, the capacitance is reduced by half, in respect to the previous fabrication strategy (where one set of the fingers of the interdigitated structure is on top on graphene), losing in terms of integration density. The advantages are the ease of fabrication, avoiding the e-beam alignment step and less processing steps on top on graphene, as well as removing the effect of the contact resistance. Moreover, depositing the metal contacts on graphene can lead to bad adhesion resulting in difficulties to contact, and this also avoids depositing a dielectric on top of graphene, which requires a passivation layer and can induce defects in graphene.

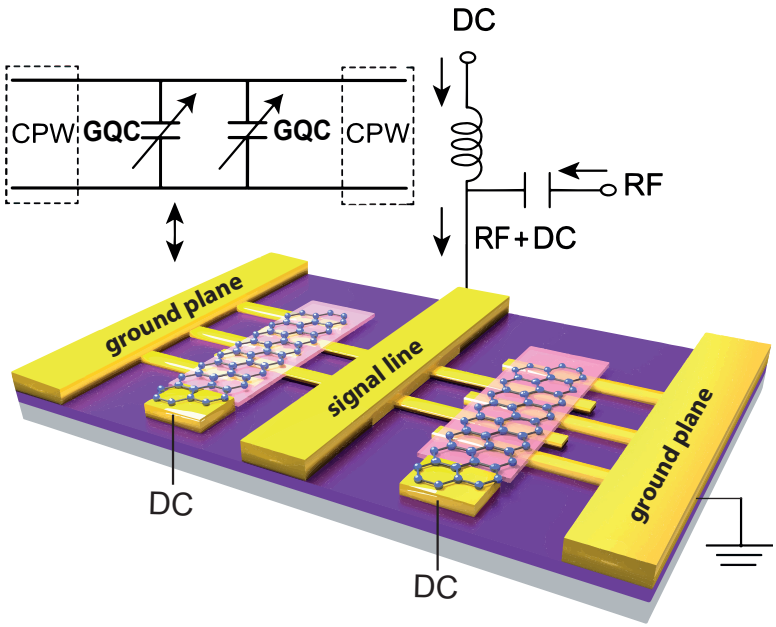


Figure 4.29: Schematic rendering of the GQCn in shunt configuration on a CPW, the equivalent circuit schematic and the biasing scheme.

The proposed equivalent model of the GQC is illustrated in Figure 4.30.

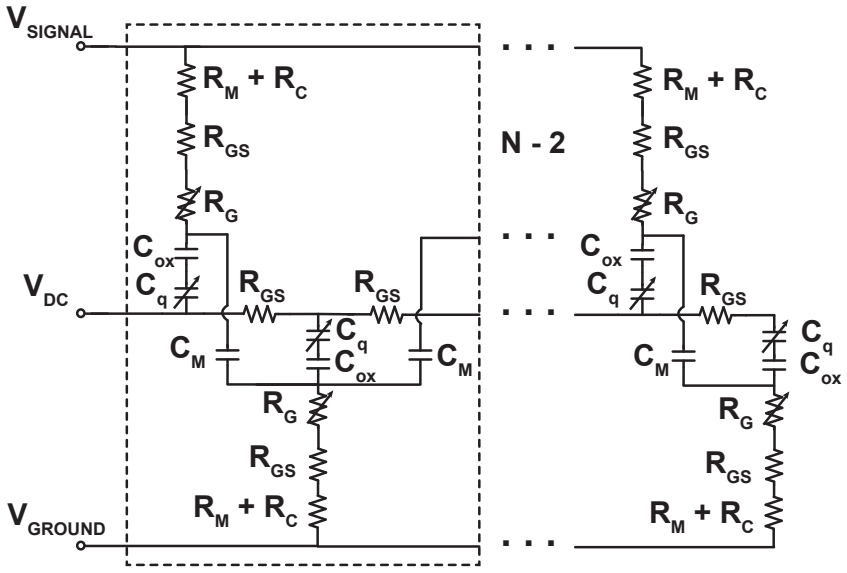


Figure 4.30: Equivalent lumped circuit model of the GQCn.

Fabrication

The fabrication process is illustrated in Figure 4.31. The substrate is ultra-high resistivity silicon, covered by 300 nm thermal SiO_2 to minimize substrate losses (Figure 4.31.a). The metal fingers, CPW structure and DC biasing pad are defined by a lift-off process of Cr/Au (5/50 nm) (Figure 4.31.b). Subsequently, 10 nm of HfO_2, constituting the dielectric of the capacitor, are deposited by ALD (Figure 4.31.c). Then CVD SLG is transferred by a standard wet PAT (§2.2.2) and patterned by e-beam (Figure 4.31.d). A SEM of the final structure is presented in Figure 4.32, with a zoom on the graphene conformally deposited on the fingers and the DC external pad. It can be observed that cracks can appear in graphene at the interface with the DC pad due to topography and post processing. However, the graphene on the fingers looks mostly intact.

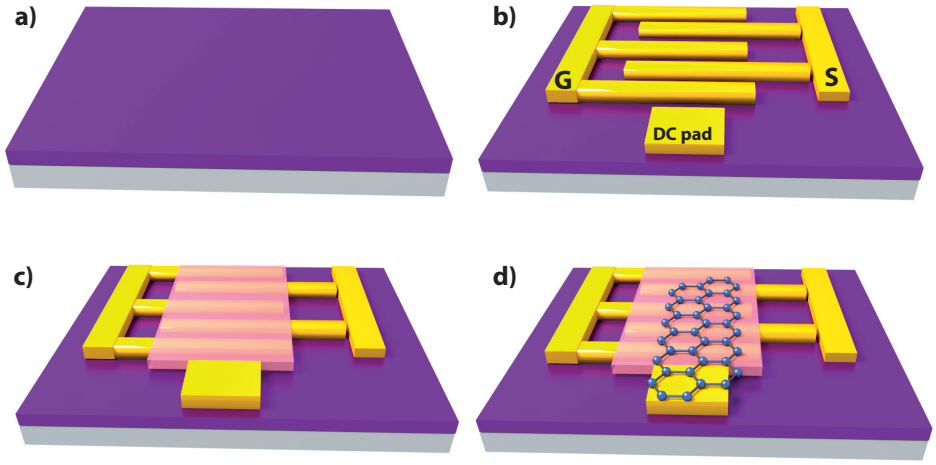


Figure 4.31: The fabrication flow of the graphene variable quantum capacitor in a bottom gate configuration. a) Thermal growth of 300 nm SiO_2. b) Lift-off of 5-50 nm Cr/Au layer. c) ALD of 10 nm HfO_2. d) Graphene transfer and e-beam patterning.

Characterization

We characterized the GQCn by impedance spectroscopy, following the same procedure described in the previous sections. Figure 4.33 shows the typical variation of the capacitance and Q with the applied DC bias. The tuning ratio is 1.15:1 and the Q is 10 at 3 GHz. The capacitance values are in good agreement with the model using an effective area of 0.93 and a disorder of 250 meV. The Q values are significantly lower than expected, and are caused by high losses in the HfO_2 dielectric.

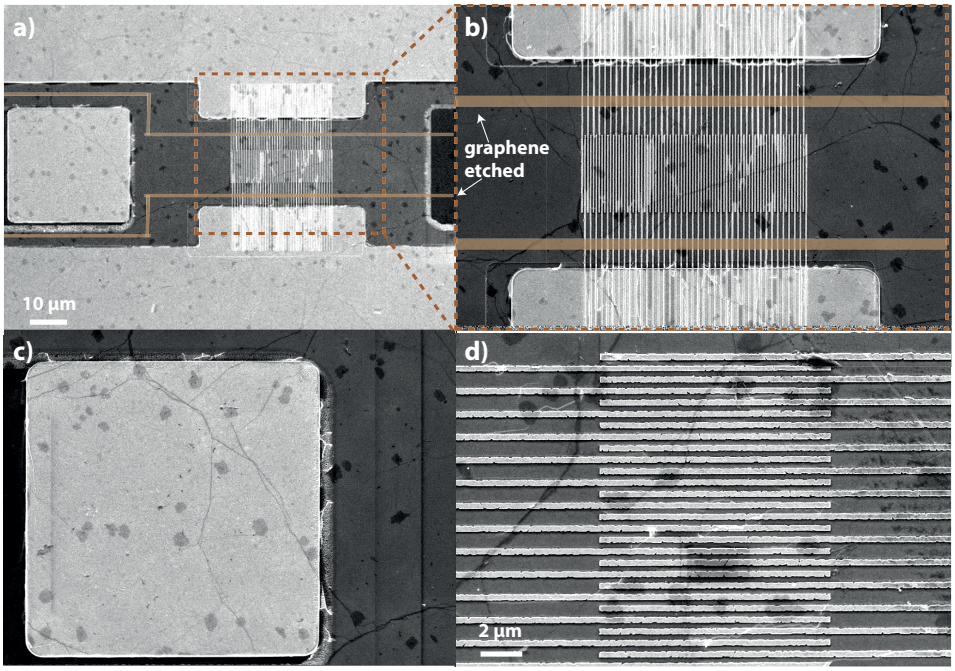


Figure 4.32: SEM of the fabricated optimised GQCn. a) single capacitor with b) a zoom on the fingers. c) metal pad contacting graphene d) conformally deposited graphene on the metal fingers. GQC geometry: $W = S = 100\,\text{nm}$, $L = 7.5\,\mu\text{m}$, $t = 50\,\text{nm}$, $N = 60$, EOT $= 3.1\,\text{nm}$.

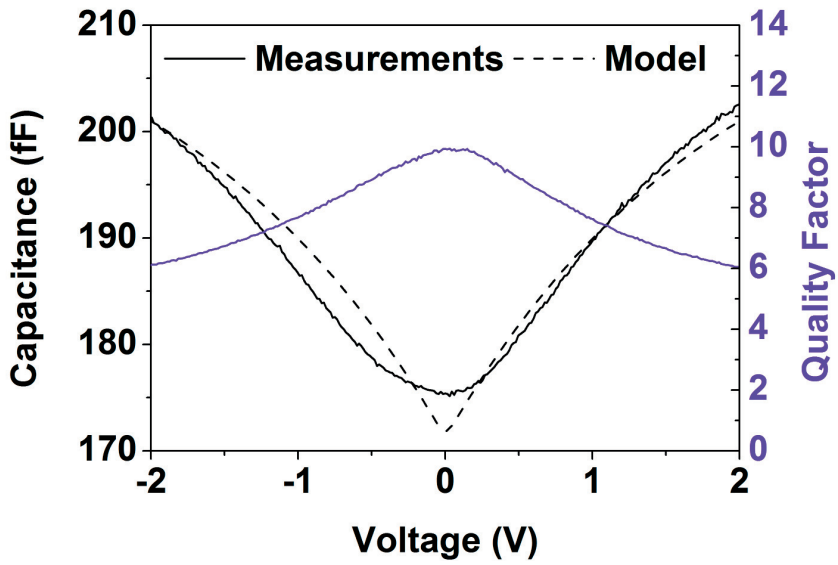


Figure 4.33: Capacitance and Q-factor dependence on voltage for the described GQCn.

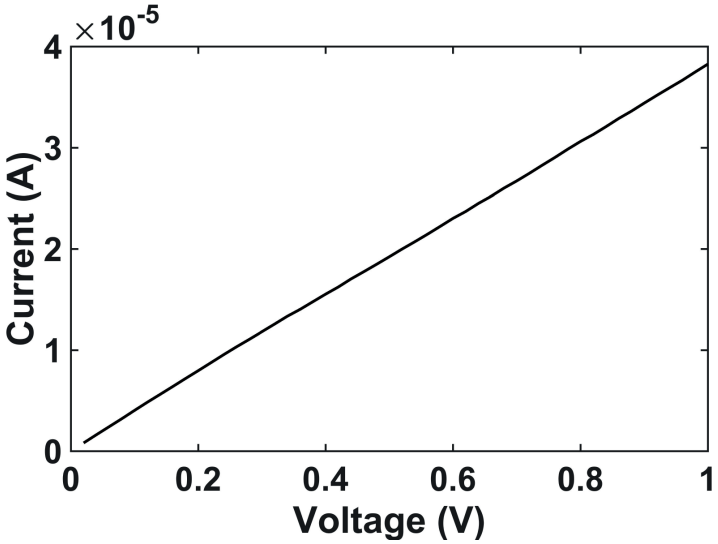


Figure 4.34: Leakage current trough the dielectric. The IV characteristics are measured between signal and graphene.

A DC leakage resistance of 26 kΩ is measured, and a linear IV characteristic from signal to ground is observed, indicating that the dielectric is broken (Figure 4.34). However, the resistance is still high enough to ensure sufficient isolation to maintain the tunability of the capacitor. The Q is higher than in the previous fabrication run, due to the scaled geometry, however the poor dielectric quality hinders performance. This can be due to contamination of the ALD process, or damage during transport or graphene deposition.

As the GQC has a low tuning ratio, due to the losses in the oxide, the phase shifter must be very long to achieve a significant phase change. The increased length results in higher losses from the line. In addition, significant losses are added due to the high oxide leakage (resulting in a low Q). This can be improved by optimising the thin oxide deposition and quality.

4.10.4 Graphene Quantum Capacitor Phase Shifters

Design

In this section we present the design and fabrication of a phase shifter based on graphene quantum capacitors, operating up to 5.8 GHz. The design follows the same principle described in §3.9, loading two GQCn (for symmetry) on the CPW, instead of the GNEMS.

Using the GQCn variable capacitor, a broadband phase shifter can be designed by simply loading the coplanar waveguide periodically with quantum capacitors, with a periodic spacing

ΔL. The phase shifter unit cell can be modeled as shown in Figure 4.35:

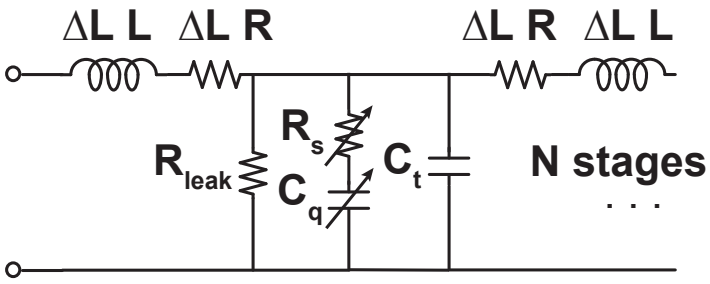


Figure 4.35: Equivalent circuit of the unit cell of the phase shifter, consisting in two GQCn in parallel on a CPW. The final device is constituted of a series of N unit cells.

The variable capacitance induces changes in the phase velocity of the line, $v_\mathrm{p} = \frac{1}{\sqrt{LC}}$, which introduces a time delay in the signal as it propagates through the phase shifter, and hence the phase is changed. This results in analog control of the transmission line phase velocity and, therefore, in a true-time delay (TTD) phase shifter.

The periodic structure has an upper frequency limit due to the Bragg reflection occurring at:

$$f > f_\mathrm{b} = v_\mathrm{p}/\pi\Delta L \tag{4.4}$$

The periodic spacing, ΔL and the GQC area need to be adjusted in order to push the Bragg frequency above the region of interest and maintain the loaded-line impedance at 50 Ω.

Phase shifters were designed and simulated electromagnetically, using Ansys High Frequency Structural Simulator (HFSS). The oxide dielectric constant was varied to mimic the tuning ratio of the GQCn (1.15:1), and the resulting phase shift, insertion and return losses were used to optimize the structure. Figure 4.36 shows the simulated results of a phase shifter with 196 stages and spacing ΔL = 400 µm (7.84 cm total length), achieving 180° at 5.8 GHz.

Fabrication

As transferring long graphene sheets is challenging, we fabricate shorter phase shifters, composed of 20 stages in order to demonstrate the principle. Since the phase shift can then be increased proportionally simply by adding more stages, we can reliably demonstrate the capabilities of GQCs for reconfigurable functions using fewer stages. We fabricated the shifters by the process previously described in §4.10.3, and we show the image of the resulting device's section in Figure 4.37.

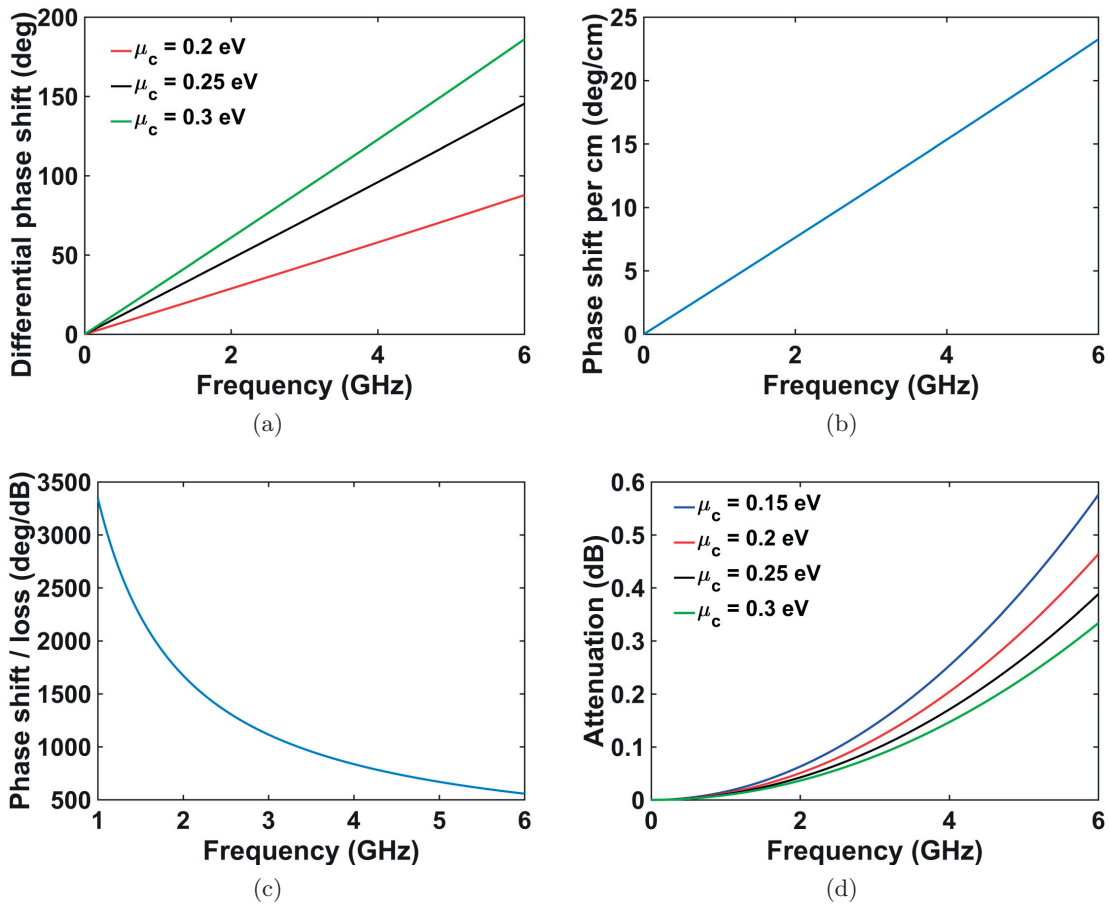


Figure 4.36: Simulated phase shifter designed to achieve a differential phase shift of 180° at 5.8 GHz. a) Differential phase shift. b) Differential phase shift normalized to the length. c) Differential phase shift normalised per loss. d) Attenuation.

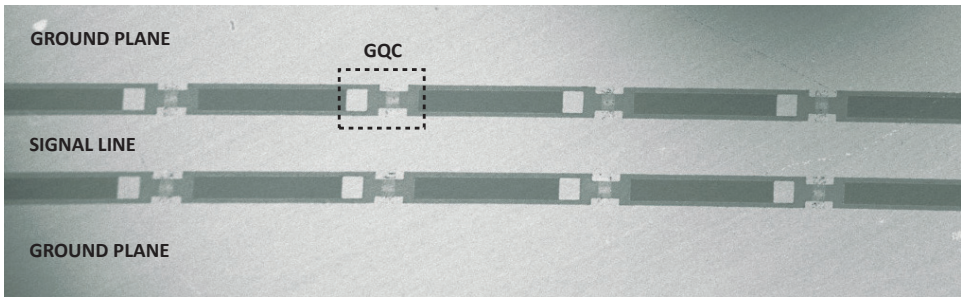


Figure 4.37: SEM of 4 phase shifter stages.

Characterization

S-parameters were measured using a VNA N5230C vector network analyzer and groundsignal-ground (G-S-G) probes. TRL calibration was performed on wafer, setting the reference planes at the probe tips. The GQC capacitance is varied using a single control voltage, varying the distributed capacitive loading on the transmission line and, therefore, its propagation characteristics. The DC bias is applied on one external pad touching the continuous graphene stripe, using a semiconductor parameter analyzer HP4156C, while the signal line is grounded in DC, superimposing a DC signal on the RF one. The measured results are presented in Figure 4.38.

A maximum differential phase shift of 20° is achieved at 5.8 GHz (Figure 4.38.a), which can be increased at will by proportionally increasing the number of stages due to the TTD working

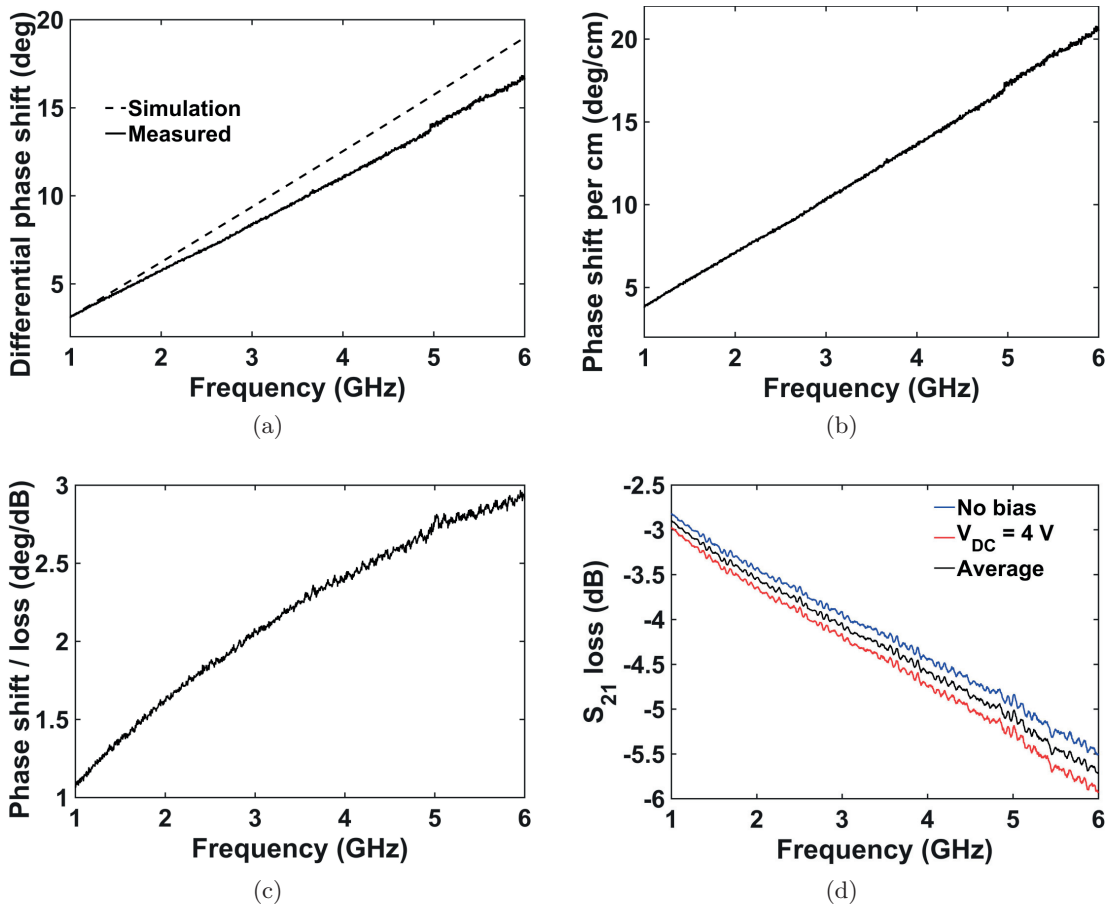


Figure 4.38: Measured phase shifter working at 5.8 GHz. a) Differential phase shift: measurement and simulation. b) Differential phase shift normalized to the length. c) Differential phase shift normalised per loss d) Attenuation.

principle. As can be seen, the measured phase shifts agree very well with the simulated ones, for GQC with tunability of 1.15:1. The phase shift normalized per length is 20°/cm (Figure 4.38.(b)) but the normalized phase shift per loss is very low, 3°/dB (Figure 4.38.c). The attenuation was 5.4 dB at 0 V and increased to 5.8 dB at 4 V (Figure 4.38.d). However the losses do not match as the high oxide losses were not included in the simulations.

Even though the obtained values are lower than expected and than the state-of-the-art, they clearly demonstrate the potential of GQCs for phase shifters, for miniaturized solutions in the low GHz range, reconfigurable with very low actuation voltage. Further investigations are necessary to assess the losses of such devices with a good quality dielectric layer.

The presented GQC reconfiguration could also be applied to the implementation of other tunable devices in the microwave to terahertz band, such as proposed novel phases-array scanning [205] or THz tunable filters [206].

4.11 Conclusion

In conclusion, we have used a scalable process to fabricate high-performance tunable capacitors based on the graphene quantum capacitance tunability. We have performed a detailed analysis and then presented and discussed the most important performance parameters: tuning ratio, quality factor, linearity, graphene quality and temperature dependence, and observed a marked improvement from previous reported values. Furthermore, we have presented an unprecedented analysis in the GHz range, obtaining Q values up to 12 at 1 GHz and a tuning ratio up to 1.34:1. The GQC tunability can be further enhanced by scaling the dielectrics and improving their quality, reaching theoretical values on the same order as the semiconducting alternatives currently employed, at a noticeably reduced power. We have demonstrated how, by scaling the geometry, we obtain a significant increase in performance in terms of Q, capacitance density, and have provided clear guidelines to establish a pathway for design and fabrication optimisations of GQC. The simple and robust design can be adapted to achieve competitive solutions for large scale, high density integrated low-power RF analog circuits.

Furthermore, we demonstrate that graphene quantum capacitor is an alternative tunable device, complementary to the graphene NEMS switch, covering RF circuit applications requiring analog tunability such as VCOs, microwave filters and phase shifters. This device represents a real breakthrough for RF reconfigurable electronics, with properties specific to graphene that cannot be mimicked by any alternative technology.

The potential of the device for reconfigurable phase shifters was demonstrated experimentally, by loading an optimised GQCs in a shunt configuration on a true time delay transmission

line. A differential phase shift of 20° was obtained with 20 stages, as a proof of concept of a design with 196 stages reaching 180° at 5.8 GHz. The results successfully demonstrate the reconfigurable functions enabled by GQCs, however the performance of the device is hindered by the high oxide leakage.

To summarize, this chapter includes the following original contributions:

- Graphene quantum capacitors have been proposed for the first time for RF reconfigurable applications.
- The RF characteristics of the variable capacitors have been investigated.
- The small temperature dependence of the main figures of merit has been determined experimentally.
- An optimised design, achieving a superior performance at high frequencies compared to the alternative technologies has been proposed.
- The potential use of GQCs in phase shifters for reconfigurable applications has been investigated experimentally.

5. Technology Platforms for Mid- and Far-Infrared Applications

This chapter introduces the potential of graphene for THz and IR functions. We fabricated stacked graphene structures, working in transmission and reflection, which enable a wide range of applications, such as modulators or isolators. We uses similar structures to characterize single layer graphene at THz and IR frequencies, and finally demonstrate that the reflection measurements provide a novel and precise method to extract the imaginary part of the graphene conductivity in the IR range.

5.1 Introduction

5.1.1 Overview

The terahertz band (THz) is the region of the electromagnetic spectrum which spans the decade from 0.3 THz to 3 THz. Because it lies between the microwave and the infrared regions, THz devices show features similar to both microwave technologies (such as metal CPWs and antennas) and to optical systems (such as lenses and focusing mirrors). Lately, a lot of efforts have been made to bridge the "THz gap" and few of the most important emerging application fields are:

- **Telecommunications:** A high data rate can be achieved due to the wide band, making THz band suitable for local area networks and broadband mobile communications. Attenuation in atmosphere prevents long range communications but allows secure and reusable short range links.
- **Sensing:** Since many biological macromolecules and the DNA molecular rotation and vibration are located in the THz band, they have a unique response in the THz spectrum. Therefore, THz radiation can be used for disease diagnosis, organisms detection and imaging.
- **Security:** systems based on THz scanners to identify metal parts, drugs and explosives through clothes, envelopes and boxes.

- **Space Communications:** In outer space, the transmission of THz is lossless, so long-range space communications can be achieved with very little power. At the same time, compared with the current space optical communication, THz waves have wider beam width, and are easier to point in the long-distance space communication between satellites.
- **Radio-astronomy:** THz technology can be used to study interstellar formations and gas clouds.

One major issue of the terahertz band is a lack of technologies needed to create the building blocks of more complex systems. Sources, for example, have very limited power or are extremely bulky. Also, passive reconfigurable materials to build switches and antennas are limited, and non-reciprocal components have very high losses, in the order of tens of dB.

In spite of these issues, the THz band has been subject to intense research efforts due to the aforementioned promising applications of this particular part of the electromagnetic spectrum. This chapter focuses on reconfigurable and non-reciprocal components, where graphene has the potential to outperform existing technologies. We start by briefly introducing the main reconfigurable technologies used at THz.

One of the first technologies considered for reconfigurability at THz frequencies are liquid crystals (LC). These are molecules in a solvent which can take a precise orientation upon the application of a constant electric field. The obtained matter phase shows strong and controllable birefringent properties which are commonly used at optical frequencies for displays. Recently several devices have considered the use of LC also for THz applications [207], however the absorption due to the liquid phase remains a very important limitation.

PIN diodes, commonly used at microwaves, show poor performances for THz tunable passives, and demonstrated applications do not exceed 0.4 THz [208]. Schottky diodes instead can show moderate amplitude modulation up to 2 THz, but they show also non linearity issues [209].

Photo-excited semiconductors (such as silicon under a visible light laser [210]) have also been proposed, but the use of visible light to perform the switching requires often bulky and power consuming light sources.

Metal isulator transition (MIT) oxides are another reconfigurable technology explored at THz, based on conductivity variation; the most common MIT oxide is vanadium dioxide (VO_2), which can achieve a conductivity change of 5 orders of magnitude, upon temperature variation. The MIT in VO_2 occurs at a temperature of approximately 68 °C [211]. Strontium titanate (STO, $SrTiO_3$) shows a similar abrupt temperature dependence.

Colour changing chalcogenide glasses [212] and ferroelectric complex oxides [213] have also been proposed, but the research on these materials is still at a very early stage.

5.1.2 Terahertz to Infrared Graphene Passive Components

The strong graphene-light interaction has led to the rapid development of graphene applications in the terahertz (THz) and mid-infrared frequency bands [214]. The characterization of single layer graphene structures has already been done for microwaves [215–218], THz [218–220] and optics [214, 221] and some promising applications such as modulators [222–225], plasmonic waveguides [226, 227] and Faraday rotators [228] have been developed.

Several interesting phenomena occur at THz frequency. In particular the tunable conductivity of graphene can be exploited to create THz planar modulators, able to achieve a transmittance variation of approximately 20 % which allows the modulation of a THz beam passing through the device [223].

Better performances can be achieved by a modulator including metal elements, which help focusing the THz energy in graphene [229], enabling modulation efficiency in the order of 40 THz. This technology has been used also to create an imaging device based on a THz modulating matrix [230].

Implementations at THz, however, are affected by intrinsically high insertion losses. A theoretical limit has been found to explain the occurrence of such unavoidable insertion loss, suggesting also that device in reflection could lead to improved performance [231]. This has been experimentally demonstrated for reflection modulators, able to achieve 70 % modulation depth [224]. Additionally, the discovery of Faraday rotation in graphene at microwave to THz frequencies [228] opened the way to non reciprocal devices at THz based on graphene.

The inductive component of the conductivity results in plasmonic resonances, which become important already at THz/Far infrared frequencies (IR) ([222]). Resonances become sharper at mid infrared frequencies ([232]) and this effect has been employed for the realization of label-free biosensors based on the plasmonic electric field enhancement [233]. The resonance is frequency-tunable, a fact which is explained by the varying inductive conductivity.

At near infrared frequencies, instead, the interband conductivity allows the creation of waveguide modulators [234] and photo-detectors [49].

5.2 Graphene Stacks for THz Modulation

5.2.1 Motivation

The gate-controllable complex conductivity of graphene offers unprecedented opportunities for reconfigurable functions at terahertz and mid-infrared frequencies. However, the requirement of a gating electrode close to graphene that this approach offers limits the practical implementation and performance of these devices.

Here graphene stacks composed of two graphene monolayers separated by electrically thin dielectrics are developed and their potential for THz applications is assessed. These structures offer more than one 'tuning knob' for reconfiguring the stack properties:

- In a first implementation, two graphene layers gate each other, thereby behaving as a controllable single equivalent layer, but without any additional gating structure.
- Second, adding an extra gate allows independent control of the conductivity of each layer within the stack, and provides enhanced control on the stack equivalent conductivity.

These results are very promising for the development of THz and mid-infrared devices with enhanced performance and reconfiguration capabilities.

The implementation of graphene for reconfigurable high frequency applications is based on its ability to tune its electrical properties by applying a gate bias. However, the simple implementation and performance of these devices might be hindered by the presence of a gating electrode located close to graphene and the relatively weak control that this approach offers over the conductivity of graphene [222, 235].

These limitations can be overcome by using graphene stacks, structures composed of two or more isolated graphene layers separated by thin dielectrics, which lead to increased tunability and may provide novel reconfiguration strategies. Potential applications of graphene stacks include modulators [223], enhanced metasurfaces [236], antennas [40], or plasmonic parallel-plate waveguides [227,237], among many others. Experimentally, graphene stacks have recently been applied to the development of vertical FETs [238, 239]. In addition, the response of unbiased graphene stacks and devices at infrared frequencies has also been investigated [235]. In this context, this work aims to demonstrate the first experimental validation of the concept of reconfigurable graphene stacks for THz applications trough an easy, incremental fabrication process, using multiple graphene transfers.

5.2.2 Principle

The investigated structure based on graphene stacks is depicted in Figure 5.1, where incident and transmitted beams required for THz time-domain measurements have been schematically rendered. The sample consists of two chemically vapour deposited (CVD) graphene monolayers separated by an electrically thin ($\propto$80 nm) PMMA layer. Although the graphene monolayers within the stack are not close enough to couple through quantum effects [240] their extremely small separation in terms of wavelength allows the stack to behave as a single equivalent layer of increased conductivity.

The sample is measured in the 0.5-2.5 THz frequency range using time-domain spectroscopy. The complex conductivity of the graphene stack is then retrieved using a dedicated formulation [219, 241]. As the dielectric separation layer between the graphene layers is extremely thin in terms of wavelengths [235] ($d/\lambda_0 \ll 10^{-3}$), an incoming electromagnetic wave observes a stack conductivity σ_S:

$$\sigma_S = \sigma_{\text{top}} + \sigma_{\text{bot}} \tag{5.1}$$

where σ_{top}, σ_{bot} are the complex conductivities of the top and bottom layers. When applying a DC bias between the graphene layers, the real and imaginary part of the stack conductivity, σ_S, are varied as shown Figure 5.2. In the low THz band, the real component of the sample conductivity does not vary with frequency, whereas the magnitude of the imaginary part increases with frequency following a standard Drude model.

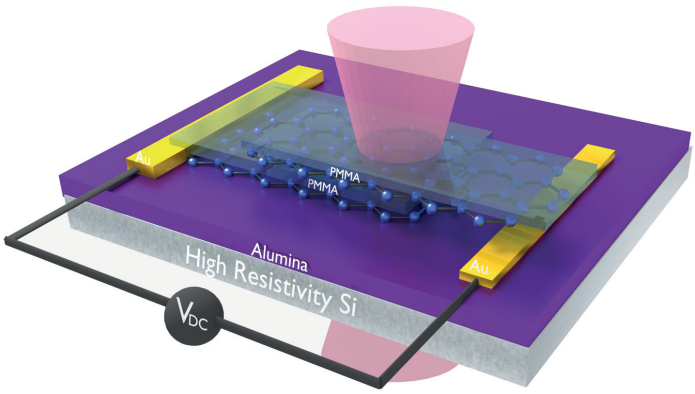


Figure 5.1: Graphene stack composed of two monolayer graphene sheets separated by an electrically thin layer of PMMA. Schematic rendering of the fabricated sample. Incident and transmitted beams, employed for THz time-domain measurements, are illustrated for convenience.

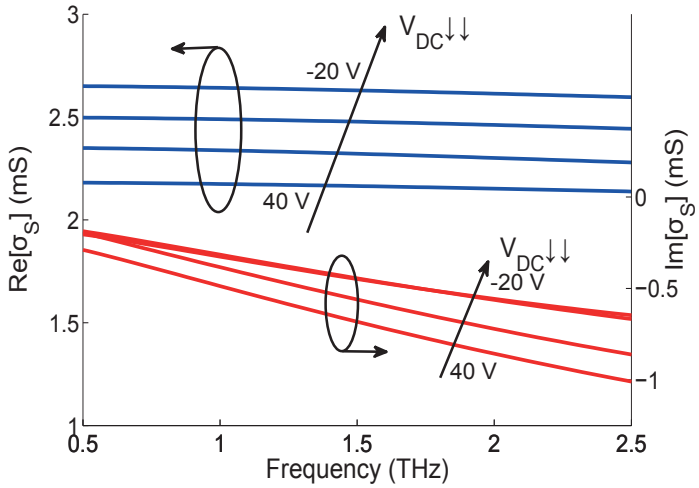


Figure 5.2: Gate-controlled conductivity of the stack at terahertz. Measured real (blue) and imaginary (red) components of the conductivity are plotted versus frequency. Results are shown for various voltages V_{DC} applied between the two graphene sheets of the stack.

5.2.3 Model

The graphene stack is theoretically analysed statically and dynamically by two interdependent steps. First, the carrier density on each graphene layer is determined as a function of the applied gate voltages using an electrostatic approach. Second, this information is employed to compute the frequency-dependent conductivity σ_{S} of the stack. In a general case of two graphene sheets biased by different gate voltages V_1 and V_2 (see inset of Figure 5.12), these carrier densities can be approximated as

$$qn_{\mathrm{s}}^{\mathrm{top}} = qn_{\mathrm{si}}^{\mathrm{top}} - C_{\mathrm{ox}}^{\mathrm{top}}(V_2 - V_1) \tag{5.2}$$

$$qn_{\mathrm{s}}^{\mathrm{bot}} = qn_{\mathrm{si}}^{\mathrm{bot}} + C_{\mathrm{ox}}^{\mathrm{top}}(V_2 - V_1) - C_{\mathrm{ox}}^{\mathrm{bot}}V_1 \tag{5.3}$$

where $-q$ is the electron charge, $n_{\mathrm{s}}^{\mathrm{p}}$ is the total carrier density in the p graphene layer (with p = bottom, top), $n_{\mathrm{si}}^{\mathrm{p}}$ corresponds to the pre-doping of the p sheet and $C_{\mathrm{ox}}^{\mathrm{p}}$ is the capacitance of the p dielectric layer. Once the carrier densities are known, the Fermi level of each graphene layer and the conductivity σ_S, which determines the electromagnetic behaviour of the whole stack, can be easily computed [242]. Moreover, equations 5.1, 5.2 and 5.3 confirm that it is possible to control the conductivity of each graphene layer independently. Specifically, the carrier density on both layers similarly depends on the difference between the applied voltages $(V_2 - V_1)$, while the bottom layer additionally depends on the voltage V_1. Consequently, modifying the voltage V_1 while keeping constant the difference $V_2 - V_1$ allows the independent

control of the conductivity of the layer. This simple framework allows a rigorous extraction of the characteristics of the stack from the measured data, including the relaxation time (τ_p) and the Fermi level μ_c of the graphene layers and the capacitance, C_{ox} of the surrounding dielectrics. This procedure relies on applying different sets of gate voltages to the sample to measure various stack conditions, which in turns allows independent extraction of all of the aforementioned parameters. A system of nonlinear coupled equations is then imposed, relating the measured data to the theoretical characteristics of the stack. The theoretical framework was developed in Laboratory of Electromagnetics and Acoustics (LEMA), and it is detailed in [242].

5.2.4 Fabrication

The samples were fabricated using CVD graphene grown on Cu foil and transferred onto the substrate using the standard wet transfer method (§2.2.2). Figure 5.3 shows the fabrication process flow of the double-layer graphene stack. We deposit 72 nm of Al_2O_3 by atomic layer deposition (ALD) on a an ultrahigh-resistivity (>10 kΩ) p-type Si wafer. The ALD is performed at 200 °C using trimethylaluminum and distilled water as the reaction precursors. Before the dielectric deposition, the native oxide is removed from the Si wafer with a buffered oxide etch (Figure 5.3.a). The metal electrodes are patterned by optical lithography followed by a deposition of 5 nm of Cr, 50 nm of Au and a lift-off process (Figure 5.3.b). A graphene sheet is then transferred onto the top of one of the metal contacts (Figure 5.3.c). In the double-layer graphene stack, the PMMA layer used as a support polymer during the transfer process is kept on top of the graphene to act as a dielectric between the two graphene sheets. The second graphene monolayer is subsequently transferred onto the top of the other predefined metal contact, thus obtaining the final structure shown in Figure 5.3.d.

The use of spin-coated PMMA as a separation layer between the graphene sheets allows avoiding problems associated with standard dielectric deposition techniques such as evaporation, sputtering [243] and ALD of oxides, which can induce defects in graphene. This approach is convenient for fabricating graphene stacks, allowing viable biasing schemes without the need of post processing the graphene. It is worth noting that the DC isolation between the two graphene layers of the fabricated stack is not perfect, and some leakage current has been measured. However, it does not hinder the performance of the stack, as (i) the device does not operate at DC but in the THz band; and (ii) the field effect control of graphene is preserved, as the DC biasing voltage source is able to provide the required bias voltage, hence the required electrical field, even when some leakage current occurs.

One disadvantage of this method is that the PMMA dielectric does not allow annealing of the sample. However, we have noticed that PMMA acts as protection layer, as the double stack

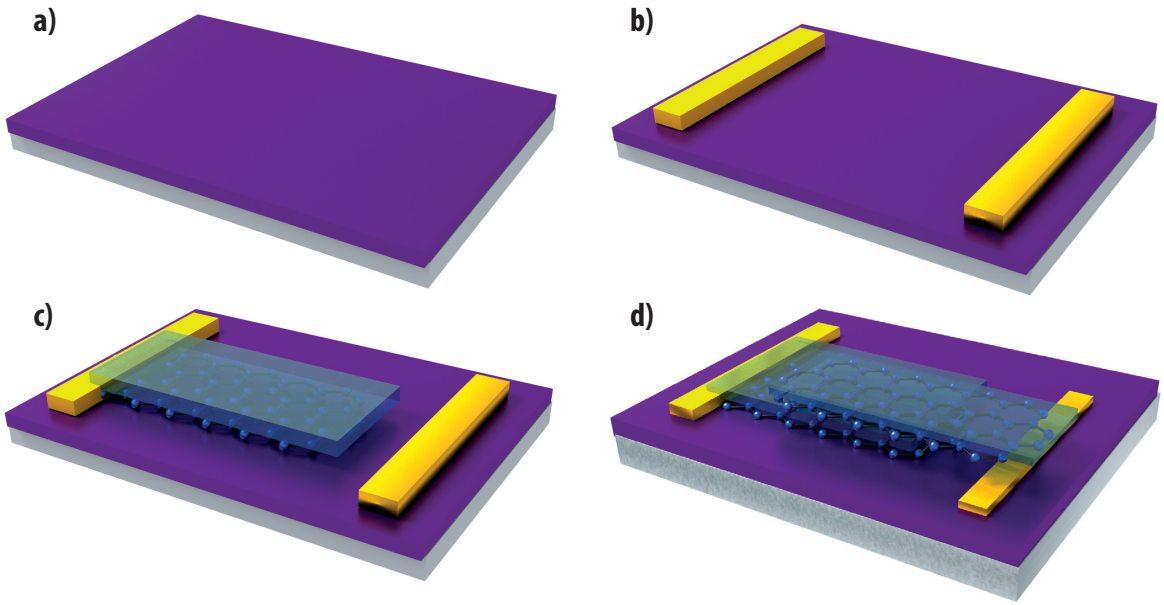


Figure 5.3: Main steps of the fabrication process of a double-layer graphene stack structure. (a) Deposit of an Al_2O_3 dielectric layer on silicon wafer. (b) Patterning of metal electrodes by optical lithography followed by a deposition of 5 nm of chromium, 50 nm of gold and a lift-off process. (c) Mechanical transfer of a graphene sheet on top of one metal contact. The PMMA employed as a support during the transfer process is kept on top of the graphene. (d) Mechanical transfer of another graphene sheet onto the top of the second metal contact and the previous stack. Final structure.

layers were less contaminated then the single layers described later in this section.

A picture of the final fabricated device is presented in Figure 5.4.

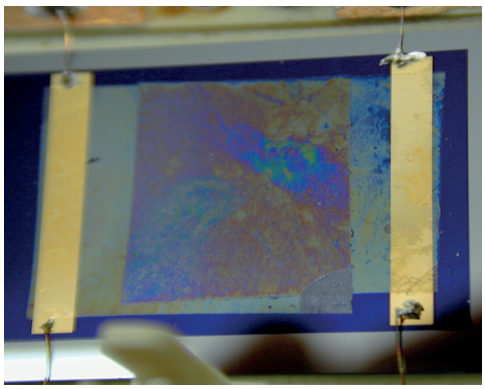


Figure 5.4: Picture of the fabricated device. The overlap area of the 2 graphene sheets is of $1\,cm^2$.

5.2.5 Characterization

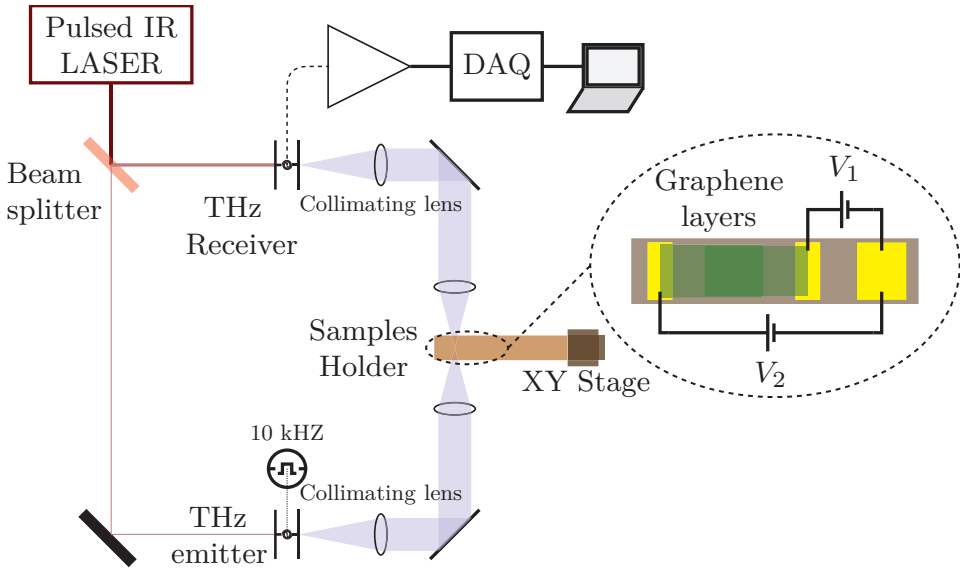
Measurement Setup

The measurements at THz frequencies were performed in the AntennaLAB, Universitat Politecnica de Catalunya, using a commercial Time Domain Spectrometer (Menlo TERA-K8), which consists of a pulsed femtosecond laser at 780 nm with a pulse repetition rate of 100 MHz and a pulse width around 110 fs, offering with the current experimental setup a signal-to-noise ratio of 40 dB up to 2.5 THz. Two photoconductive antennas based on LT GaAs (Tera8-1) are used to generate and detect the THz radiation. A set of lenses focuses the THz beam onto the sample under measurement. The total sample area illuminated by the beam is around $2\,\mathrm{mm}^2$, thus averaging graphenes features. A schematic view of the experimental setup, with the disposition of the samples and voltage sources is illustrated in 5.5. The thickness of the substrate ensures that the pulses corresponding to the different inner reflections in the sample can be filtered out, allowing the parameter extraction to be performed on the first transmitted pulse.

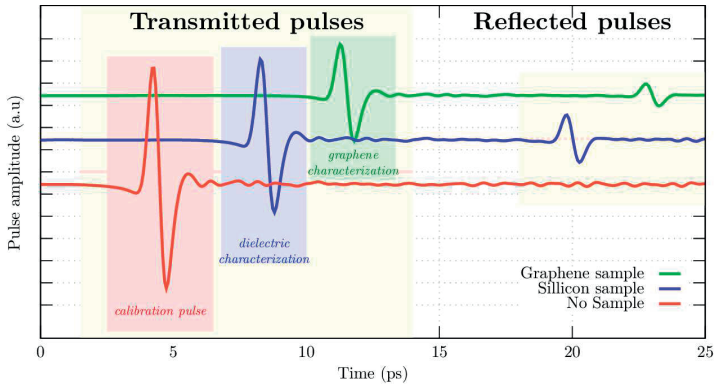
The graphene stack is placed on top of a thick dielectric structure (Si wafer/Al_2O_3), and the influence of the dielectrics must be rigorously removed to extract the actual stack conductivity. This procedure has been performed as follows:

- A pulse is transmitted without the presence of the sample to measure and store the response (including atmosphere and possible impurities) of the sealed cage.
- A pulse is transmitted through an area of the sample without graphene. The combination of this measured pulse with the pulse obtained in the previous step allows the extraction of the permittivity, loss tangent and thickness of the dielectrics using the standard technique [241, 244].
- A pulse is transmitted through the graphene stack sample. Combining this measured pulse with the previous information, it is indeed possible to extract the conductivity of the graphene stack rigorously removing the influence of the dielectrics and surrounding atmosphere [241, 244].

A DC bias of $\pm 75\,\mathrm{V}$ was applied using an Agilent N6700B voltage source. The sample was placed on an X–Y linear stage perpendicular to the THz beam, inside a sealed case purged with N_2 to keep a constant atmosphere during the duration of the measurements.



(a)



(b)

Figure 5.5: a) Schematic view of the THz time-domain experimental setup employed to characterize the samples, illustrating the disposition of the samples and b) voltage sources (red) and characterizing the bare dielectric (blue) and the complete graphene structure (green).

Characterization of SLG at THz

First, to understand the properties of graphene, a single layer of graphene was characterized, using a test structure depicted in Figure 5.7. The structure is fabricated trough a similar process to the stacks, depositing only one layer of graphene and subsequently removing the transfer PMMA. The structure is gated using the Si substrate, contacted by a gold electrode.

The Raman spectra of the graphene shown in Figure 5.6. The G and 2D band points are located at 1589 and 2682 cm^{-1} with a full width at half maximum of 18 and 32 cm^{-1}, respectively.

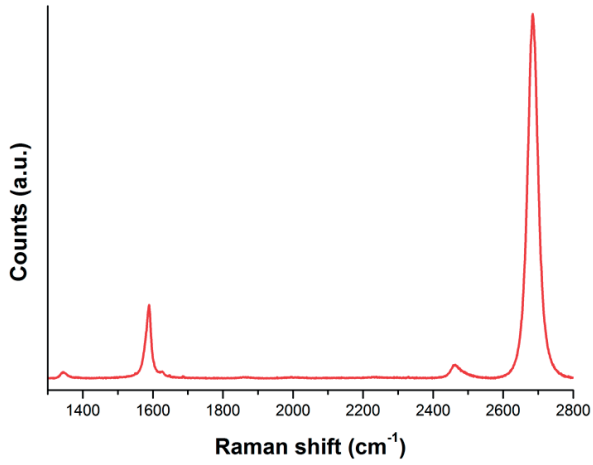


Figure 5.6: Raman spectrum of graphene transferred on Al_2O_3/Si wafer using a 532 nm laser.

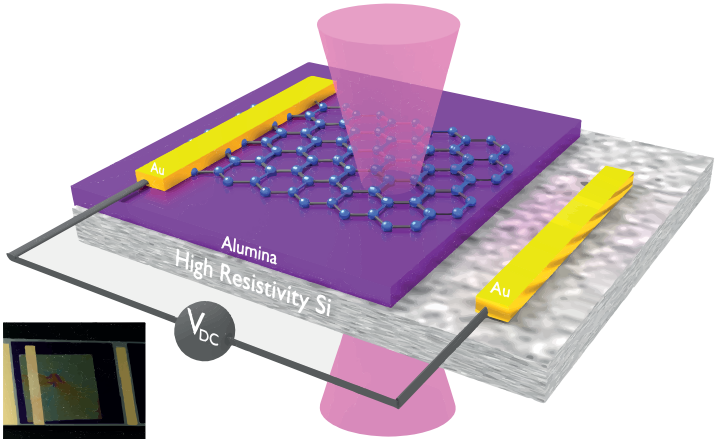


Figure 5.7: Single layer graphene structure fabricated for verification purposes. (a) Sketch of the fabricated sample. The incident and transmitted terahertz beams, employed for THz time-domain measurements, are also illustrated. The insert shows a picture of the fabricated device.

The intensity ratio of the 2D to the G band and of the D to the G band are 5.5 and 0.09, respectively, indicating that the graphene is monolayer [123]. The sample conductivity σ_S is extracted from the THz time-domain measurements, using standard thin-film characterization techniques [219, 241, 244]. An example of the different set of measured pulses employed for the extraction procedure is shown in Figure 5.5.b. To keep the highest possible signal-to-noise ratio, only the first transmitted pulse through the sample was considered. Additional transmitted pulses that arise due to the internal reflections of the THz beam within the layers of the sample are clearly identified, thanks to their temporal delay, and subsequently removed. The

theoretical framework used to extract the data is described in detail in [242]. The measured real and imaginary components of the conductivity are plotted versus frequency in Figure 5.8. Results are shown for various values of the applied gate voltage V_{DC} before (dashed line) and after (sold lines) annealing. In the absence of the applied bias, the layer can be accurately modelled at T = 300 K by a Drude model with relaxation time $\tau = 0.029$ ps and a Fermi level, $\mu_{\mathrm{c}} = -0.425$ eV.

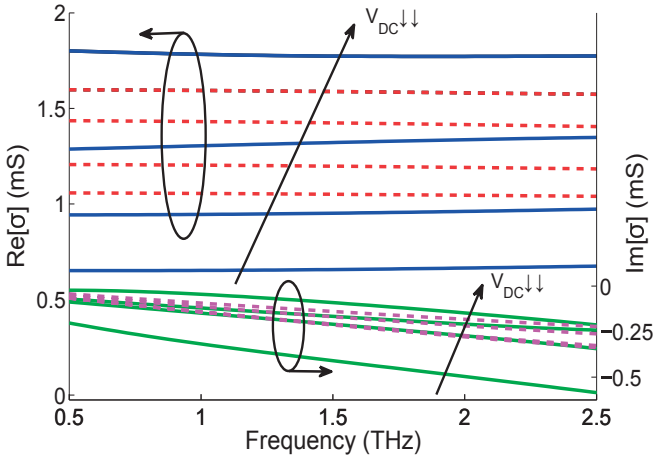


Figure 5.8: Gate-controlled conductivity of a single graphene layer at terahertz.

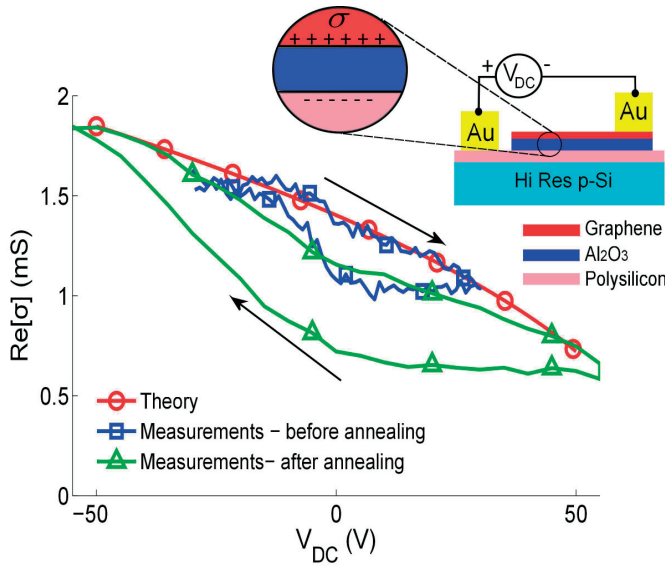


Figure 5.9: Measured conductivity plotted versus the gate voltage applied from the substrate. Inset shows the structure cross-section and biasing scheme.

The dependence of the real part of the conductivity on the gate bias in shown in Figure 5.9. It can be observed that annealing increases significantly the tuning range, but there is still a hysteresis behaviour.

Characterization of the Graphene Stack THz

A similar approach to extract the conductivity is valid in the case of stacks too, thanks to the extremely small thickness of the stack in terms of wavelength ($d/\lambda_0 \ll 10^{-3}$). Next, the measured reconfiguration capabilities of the fabricated graphene stack at $f = 1.5\,\mathrm{THz}$ are presented in different configurations.

In the first case, depicted in Figure 5.10, a gate voltage V_{DC} is applied between the two graphene layers. The results clearly confirm the tunability of σ_S and the ability to bias the stack. The extracted chemical potentials corresponding to each graphene sheet, computed using the procedure detailed in [242], combined with the measured stack conductivity and further validated by Raman scattering measurements [245], are depicted versus the applied gate voltage in Figure 5.11.

Both graphene layers are p-doped and they present slightly different Fermi levels. This difference can be due to the defects induced in the graphene layers during growth or transfer [246] and to the influence of the surrounding dielectrics [247]. In addition to the different morphology

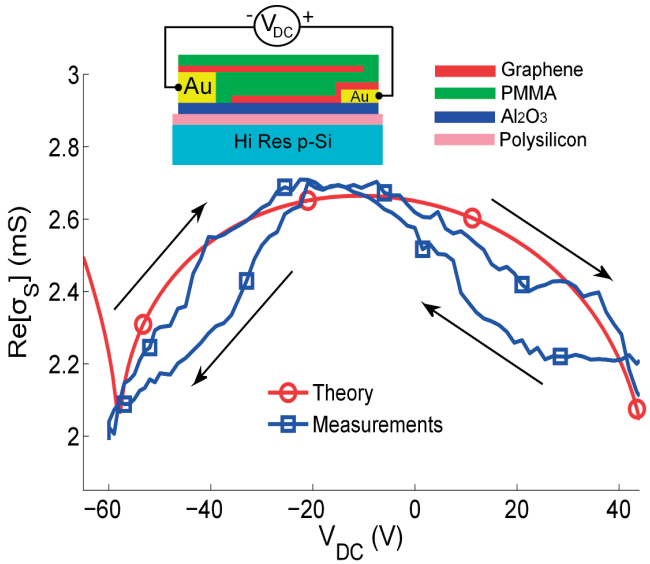


Figure 5.10: Measured conductivity plotted versus a voltage V_{DC} applied between the two graphene sheets. The inset illustrates the sample cross-section and its connection to the voltage sources.

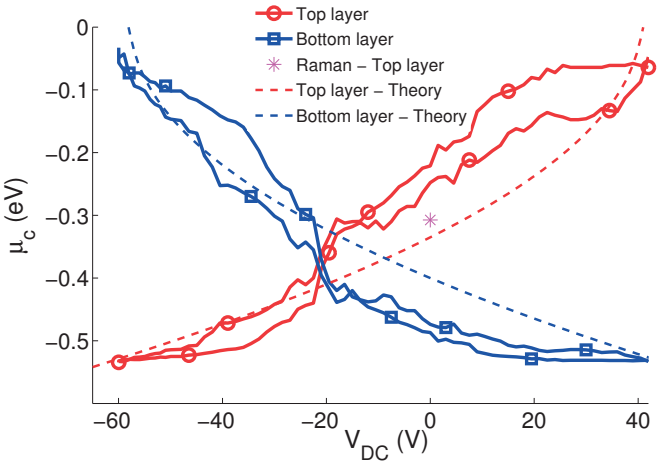


Figure 5.11: Extracted the chemical potentials of the two layers composing the graphene stack versus the applied gate voltage V_{DC} (Figure 5.10). The results obtained by measuring the dopants of the top layer using Raman [245] (at $V_{DC} = 0\,\mathrm{V}$)are shown for comparison.

of the surrounding dielectrics, contamination during processing [248] and molecules absorbed from ambient air [248] play a crucial role. Applying a positive bias between the graphene sheets injects electrons/holes into the top/bottom layers, which in turn increases/decreases their chemical potential (or vice versa in the case of a negative applied bias). Furthermore, the extracted conductivities and chemical potentials exhibit a hysteresis behaviour, which arises due to the charges and impurities trapped in the surrounding dielectrics, as observed in graphene transistors [249].

From these measurements, the graphene parameters can be extracted. In the particular case of the sample shown in Figure 5.10, we can determine $\tau_{top} = 0.033\,\mathrm{ps}$, $\tau_{bot} = 0.03\,\mathrm{ps}$, $\mu_{\mathrm{c}}^{\mathrm{top}} = -0.4\,\mathrm{eV}$ and the gate capacitance of the PMMA separation layer is $C_{\mathrm{ox}}^{\mathrm{top}} = 3.2 \times 10^{-4}\,\mathrm{F\,m^{-2}}$. These values are in good agreement with the measured characteristics of the single-layer graphene transferred onto a similar dielectric ($\tau = 0.029\,\mathrm{ps}$, $\mu_{\mathrm{c}}^{\mathrm{top}} = -0.425\,\mathrm{eV}$) and with the gate capacitance, obtained using the approximate parallel-plate formula, $C_{\mathrm{ox}}^{\mathrm{top}} = 3.315 \times 10^{-4}\,\mathrm{F\,m^{-2}}$. The measured hysteresis behaviour, is not considered in the model.

Another interesting possibility for controlling the stack conductivity and boost its tuning range consists in applying voltages V_1 and V_2 to the bottom and top graphene layers, as illustrated in Figure 5.12. This biasing scheme was implemented by including an additional polysilicon gate below the lower graphene layer, which is transparent at THz. Alternatively, this configuration might be implemented by stacking a higher number of graphene layers in the same structure.

Finally, Figure 5.13 presents a simple biasing procedure able to control the conductivity of each

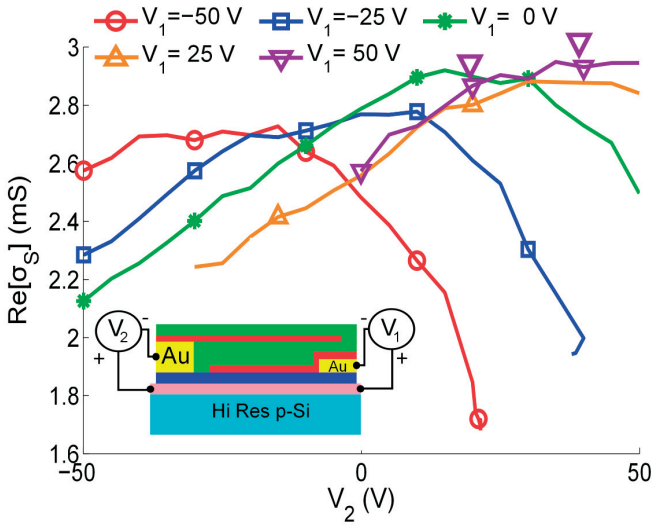


Figure 5.12: Measured conductivity plotted versus the voltage V_2 applied to the top graphene sheet for different values of the bottom gate voltage V_1. The inset illustrate the sample cross-section and its connection to the voltage sources.

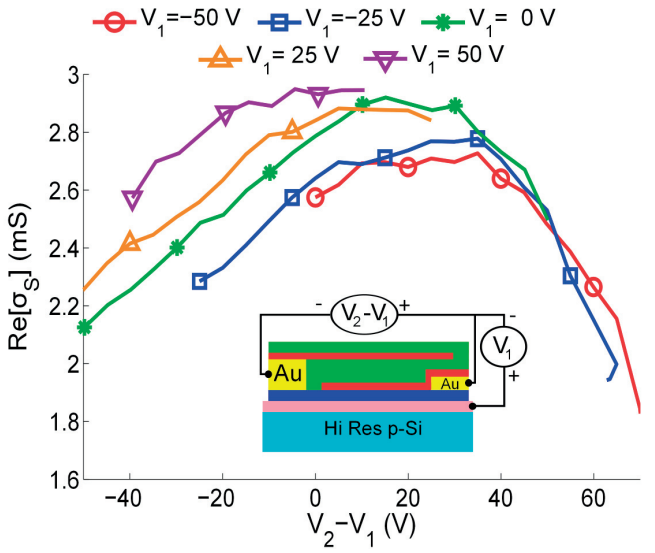


Figure 5.13: Measured conductivity plotted versus the voltage $V_2 - V_1$ applied between the graphene layers for different values of the bottom gate voltage V_1. The inset illustrate the sample cross-section and its connection to the voltage sources.

layer independently, by applying a fixed voltage $V_2 - V_1$ between the graphene sheets. This way, the chemical potential of the top layer is fixed, whereas the carrier density on the bottom layer is tuned by modifying the voltage V_1.

Samples Uniformity

The fabricated graphene samples are relatively large ($\approx 0.8\,\mathrm{cm}^2$ and $\approx 1\,\mathrm{cm}^2$ for the stack and single layer graphene structures, respectively) and thus their characteristics might slightly differ depending on the specific point that is being probed for the measurements, as discussed in §2.3.1. The non-uniformity of graphene can be due to different factors, like the presence of individual grains and grain boundaries, defects induced during growth or transfer, molecules absorbed from the environment, or contamination during processing. In order to keep the maximum consistency during measurements, the setup is completely automatized allowing the terahertz beam to impinge always on the same physical point on the sample. In this way, the influence of the sample's non-uniformity in the extracted conductivities is minimized. The focus point on the sample provided by the terahertz beam has a total area of around $2\,\mathrm{mm}^2$, thus averaging graphene features in the respective area. The uniformity of graphene was investigated by focusing the terazertz beam towards different location of the samples before applying any bias. These points are illustrated in Figure 5.14, for the case of a stack and the single layer graphene structures.

Figure 5.15 plots the variation of the extracted conductivities (real parts) on each point with respect to the measured conductivities on the center of the sample (point P_{02} in both cases). The measurements in this work, including tunability, have been performed in the central position of the samples, i.e. point P_{02}. The maximum variation among the different points is kept below 8 % and 15 % for the stack and single layer graphene structure, respectively. These results confirm that despite the discussed factors which can modify the sample uniformity (§2.3.1) and the tolerances of the THz-TDS equipment [241], the extracted conductivities are

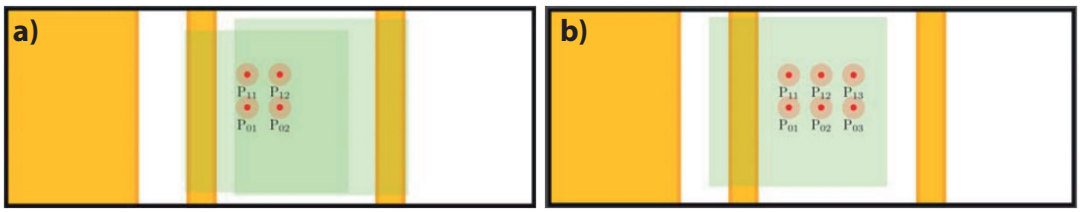


Figure 5.14: Various spatial points representing the incoming THz beamwidth distributed along a) graphene stack and b) single layer graphene surfaces employed to study the uniformity of the samples.

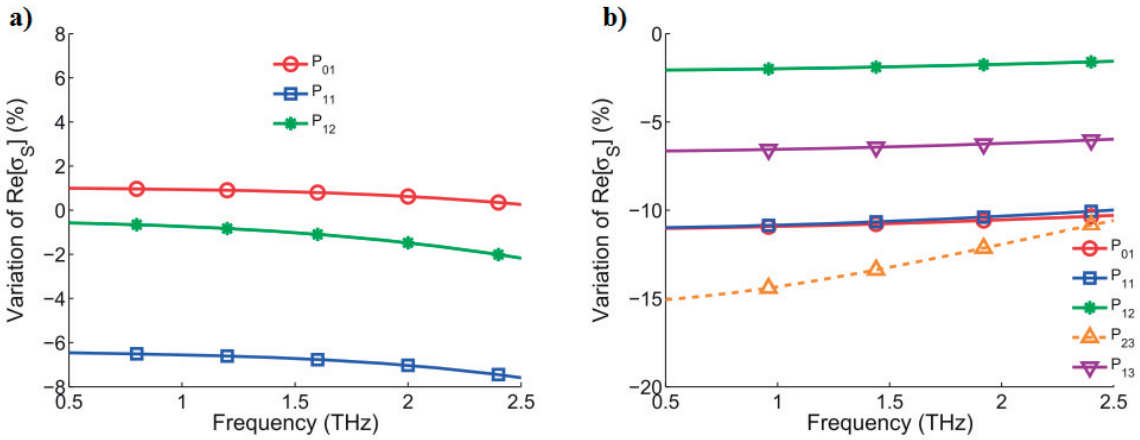


Figure 5.15: Variation of the extracted conductivity (real part in %) on different spatial position on the a) stack and b) single-layer graphene structures versus the measured conductivity in the center of the samples (P_{02}). The position of the points on the samples is illustrated in Figure 5.14.

very similar along the surface of the sample. We attribute the weak influence of the samples non-uniformitiy to the averaging process carried out by the terahertz beam [241].

5.2.6 Discussion

This framework can be further employed to forecast the reconfiguration capabilities of a wide variety of graphene or other 2D material stacks, allowing the design of structures with desired reconfigurable properties. In the case presented in Figure 5.10, applying a bias between the 2 graphene layers, if we consider, for simplicity, a stack where the graphene layers have a different type of doping, that is, one sheet is p-doped and the other is n-doped, the carriers injected by the voltage source alter the carrier density on each layer in a similar way, that is, simultaneously increasing/decreasing their chemical potential, $|\mu_c|$ while keeping an opposite nature. As a result, the stack conductivity is approximately twice the conductivity of an individual layer. The behaviour of the stack conductivity differs with respect to the case when the layers have the same type of doping, that is, if they are both p-doped or n-doped. In this case, the carriers injected by the source modify the carrier density on each graphene sheet in an opposite direction, increasing —μ_c— of one layer while reducing it on the other layer. Consequently, the stack conductivity presents a symmetrical behaviour for positive and negative gate voltages, exhibiting points of minimum conductivity in both cases. The theoretical results shown in [242] are consistent with the experimental observations that in graphene stacks, (i) the imaginary component of σ_S can be double than the one of a single-layer structure, while avoiding the

presence of metallic bias, and (ii) the tuning range is significantly boosted for similar voltage values. In addition, the conductivity of graphene stacks can be controlled further by considering two different gate sources, as shown in the inset of Figure 5.12. Similar to the previous case, the tunable behaviour of the stack conductivity will strongly depend on the initial level and the type of doping of each graphene layer, leading to a wide variety of scenarios and reconfiguration possibilities.

This experimental study of graphene stacks has demonstrated that the available range of complex conductivities in graphene stacks can be significantly boosted by two different approaches as follows:

- mutually biasing the graphene sheets without requiring the presence of any metallic gate
- including a third gate source to control the conductivity of each layer independently

The development of graphene stacks for THz modulators also faces some important challenges from the technological point of view, as it would be desirable to independently control the doping nature of each layer while decreasing the separation distance between the graphene sheets, to further enhance the reconfiguration possibilities of the stack. In addition, it would also be interesting to extend the concept of reconfigurable stacks to an arbitrarily large number of layers.

5.2.7 Applications

The unique characteristics of graphene stacks pave the way towards the development of a low-dimensional THz and IR platform with enhanced performance and reconfiguration capabilities. For instance, graphene stacks are the building block of the recently proposed tunable bulk hyperbolic metamaterials [250], whereas it was also demonstrated that they are able to boost the spontaneous emission of emitters [251] much further than the usual monolayer graphene structures. In a different context, the large range of imaginary conductivity values provided by the stacks can easily be exploited in planar hyperlenses. Currently, graphene-based hyperlenses [252] are based on achieving large contrast of conductivities within the surface by using non-uniform metallic gates located very close to graphene. However, these gates are difficult to fabricate and impair the performance of the lenses. This device could easily be implemented by a patterned graphene stack, simultaneously solving the problems related to the limited values of the imaginary conductivity and the presence of the non-uniform metallic gate. Finally, it is worth noting that the aforementioned features of graphene stacks can also be applied to develop improved devices such as modulators, isolators, sensors or antennas in the THz and infrared frequency bands.

5.3 Graphene Stacks for THz Isolators

5.3.1 Motivation

Another very promising research direction in the THz frequency range is the possibility to break the time-reversal symmetry in photonic devices based on magnetostatically biased graphene. A clear evidence of such non-reciprocal effects is the experimental demonstration of Faraday rotation in graphene for terahertz frequencies [228, 253]. Several theoretical works have proposed devices based on magnetostatically biased graphene [231, 254], including non-reciprocal isolators (also known as optical diodes) [255], i.e. photonic devices that support unidirectional light propagation. In addition, a narrowband graphene isolator was recently measured at 20 GHz [256]. Alternative magneto-optical materials (e.g. ferrite) show high losses above 0.5 THz [257], reason why the realization of low loss non-reciprocal isolators is considered one of the most important challenges in terahertz research. However, no final isolator design and characterization has been demonstrated yet for these materials, and rarely the considered frequencies exceed 1.5 THz. The main point of this work is to fully exploit the non-reciprocity of magnetically biased monolayer graphene using a reflection configuration for circularly polarized waves. This thesis covers mainly the technological development of the device, and the full characterization of the isolator is the scope of another thesis, and will be presented in details there.

5.3.2 Principle

A non-reciprocal isolator is a device allowing the transmission of an electromagnetic wave in a given direction while strongly attenuating it in the other one. The proposed graphene terahertz isolator is illustrated in Figure 5.16. A number N_S of graphene sheets are placed on a back-metallized thin silicon layer of thickness 10 µm (in this work $N_S = 3$). The sheets are separated by thin PMMA layers (approximately 60 nm), while the thickness of the metallization (chromium and platinum) is 200 nm. The whole structure is bonded to a Pyrex wafer which has solely a function of mechanical support. A magnetostatic field B is applied orthogonally to graphene.

The device operation is based on reflecting incident LHCP (left hand circularly polarized) plane waves as RHCP (right hand circularly polarized) ones, while absorbing the RHCP incident waves. The device thus achieves non-reciprocal unidirectional propagation and isolation for circularly polarized waves [255, 257]. In addition, simple reciprocal polarizers and polarization converters can be combined with this device to achieve terahertz isolation and source protection also for linearly polarized light. The device exploits Fabry-Perot resonances in the silicon layer

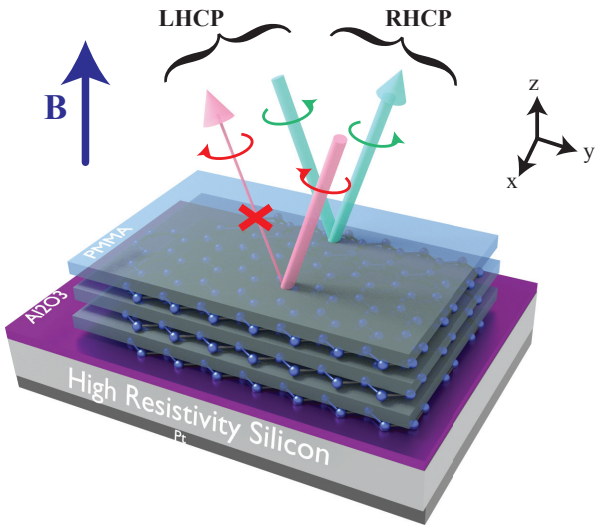


Figure 5.16: Structure and principle of operation of the THz isolator. The behaviour with respect to circularly polarized light is shown. Incident LHCP terahertz waves are reflected as RHCP by the isolator, while incident RHCP waves are absorbed

to increase light-matter interaction in graphene. As a result, three monolayers of graphene are sufficient to obtain near perfect isolation. The principle of the isolator consists in creating a total surface impedance equal to the impedance η of free space (i.e. impedance matching), seen by the clockwise (CW) rotating waves (incident RHCP or reflected LHCP), which causes the total absorption (reflection coefficient $\Gamma_{R\to L} \cong 0$). On the contrary, for counter-clockwise (CCW) ones (incident LHCP or reflected RHCP) the impedance is mismatched, and waves are reflected ($\Gamma_{R\to L} \neq 0$). Graphene conductivity can be expressed as a scalar quantity for circular polarization (Figure 5.17.a), taking two different values σ_{CW} and σ_{CCW} in the CW and CCW cases respectively.

The yellow region in Figure 5.17.b shows that at 3 THz and for B =7 T the real part of σ_{CW} is very close to $(3\eta)^{-1}$ and thus the total impedance of the three monolayers stack is very close to η. The role of the metallized silicon reflector is to cancel the imaginary part of σ_{CW} at the working frequency in order to enable full impedance matching in the CW case. The simulated performances of the device are shown in Figure 5.17.b. A part from the main working point at 2.9 THz, the device shows a second one at 7.6 THz where, however, the direction of the isolator is reversed (RHCP is reflected as LHCP and LHCP is absorbed). This inversion is explained by the different conductivity of graphene at higher frequency (Figure 5.17.a).

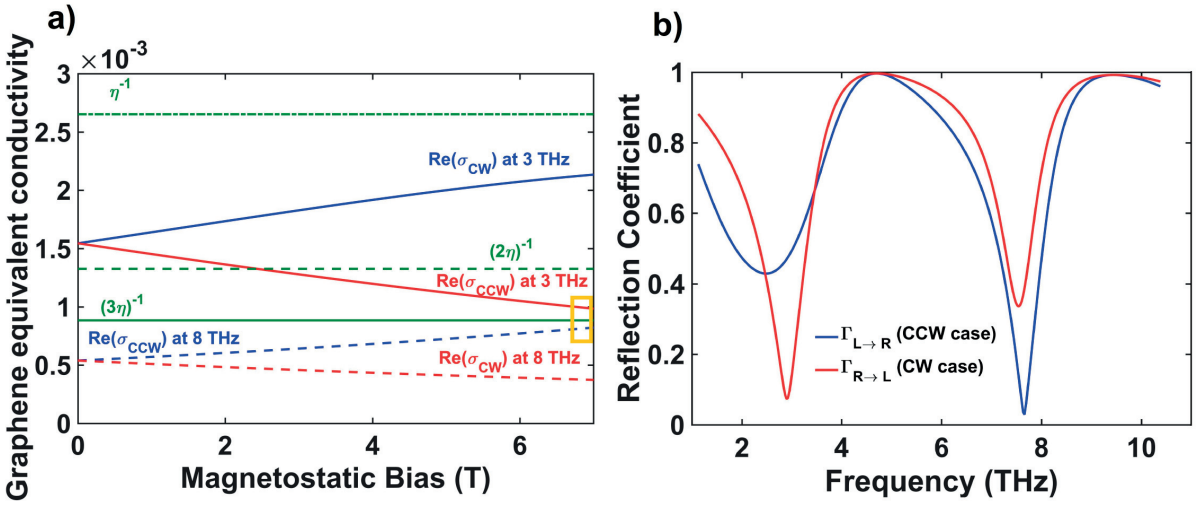


Figure 5.17: Principle of operation of the THz isolator. a) Magnetic field induced splitting of σ_{CW} and σ_{CCW} as a function of the bias B (f = 3 THz and 8 THz, μ_{c}=0.53 eV, τ = 35 fs, T=290 K) computed using Kubo formula. The real part of the equivalent conductivity for the clockwise and counter-clockwise cases is shown for monolayer graphene and compared with multiples of the free space impedance η. The area of interest for the design is highlighted in yellow. b) Simulation of the reflection coefficients for wave converted from right-handed to left-handed or vice-versa. Two working points are observed, however the direction of the isolation in the second one is reversed. Reflection coefficients expressed in dB follow the rule $20\log_{10}\Gamma$ consistently with the definition of Γ in terms of reflected field amplitude.

5.3.3 Fabrication

The fabrication consist in the creation of a low loss silicon layer, with a thickness of 10 µm with a back metallization providing good reflectivity for terahertz waves. To this aim, SOI (silicon on insulator) wafers having a device layer with the required specifications (thickness, d_{SI}, 10 µm, resistivity > 10 kΩ cm) were used (ULTRASIL corporation). The handle Si layer was 500 µm thick, while the box SiO_2 layer had a thickness of 750 nm. 200 nm of Pt (with 10 nm Cr adhesion layer) were evaporated on the device layer, constituting the metallic reflector. The metallized face of the SOI wafer was subsequently bonded to a support pyrex wafer (500 µm) using parylene bonding [258]. The pyrex wafer, chosen due to its thermal expansion coefficient very close to the silicon one, works as a support for the thin device layer for the subsequent fabrication steps. The pyrex wafer is first cleaned in piranha followed by silanization and parylene-D coating (1.64 µm of measured thickness). The two substrates were bonded at 380 °C (10 °C above parylene-D melting point) under vacuum using a tool pressure of 1000 mbar in a Suss SB6 vacuum bonder for a total time of 40 min. The handle layer of the bonded SOI wafer was then grinded for a total depth of 400 µm, and the remaining 100 µm of silicon were etched

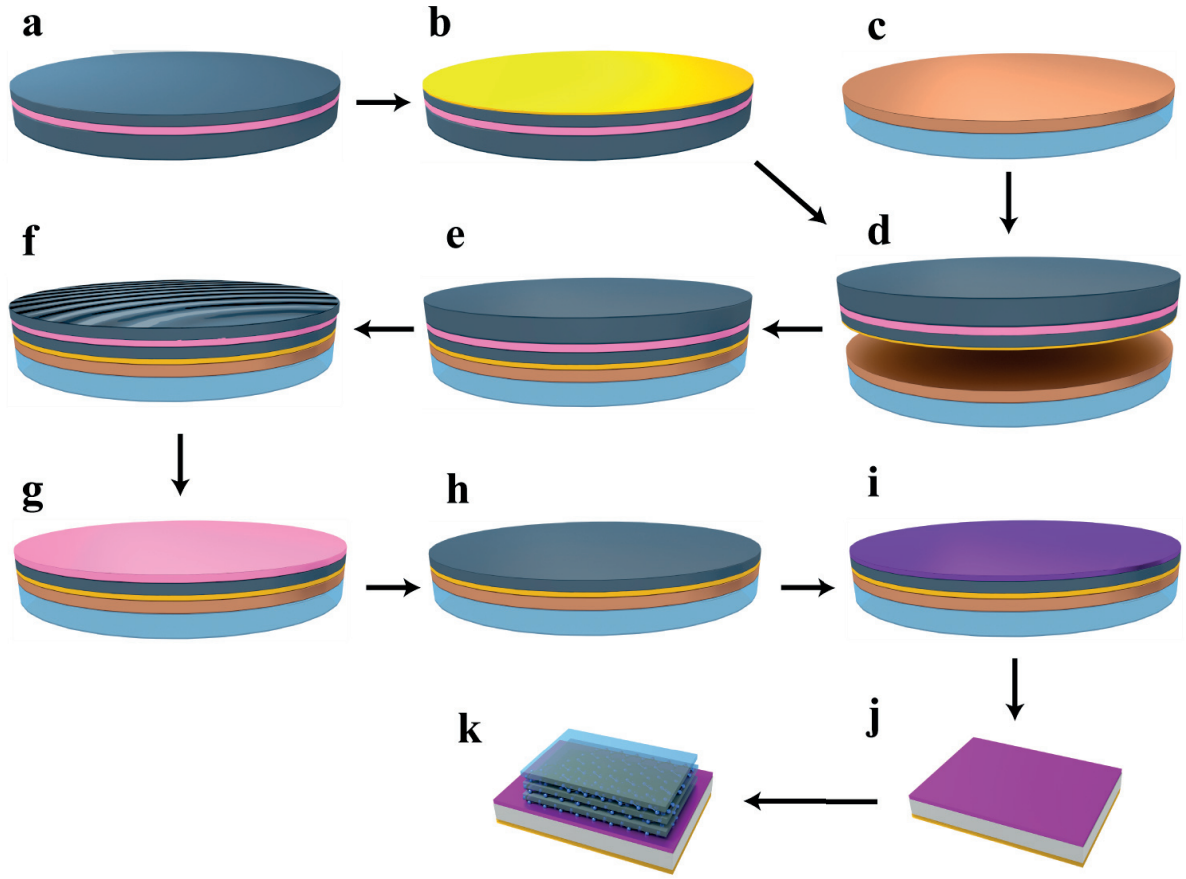


Figure 5.18: Fabrication process flow. The main steps of the fabrication of the isolator are represented. a) initial SOI wafer. b) evaporation of the Pt ground plane. c) silanization and parylene-D coating of the pyrex glass. d-e) parylene-based wafer bonding. f) partial grinding of the SOI silicon handle wafer. g) dry etching of the remaining part of the handle wafer. h) dry etching of the SiO_2 box layer. i) ALD deposition of the Al_2O_3 layer. j) dicing into 12 mm square chips. k) graphene + PMMA transfer.

using a deep reactive ion etching (DRIE) process, selective over the SiO_2, to prevent damages to the device layer. The SiO_2 box layer was then removed using a dry etching process with high selectivity over silicon. Using ALD, 72 nm of Al_2O_3 were then deposited on the device layer as final substrate for graphene. After dicing the wafer, CVD monolayer graphene provided by Graphenea S.A. was transferred on the chip by a wet transfer process (§2.2.2), using a support PMMA layer of 60 nm. Three graphene monolayers were transferred on the chip without removing the PMMA, thus avoiding inter-layer coupling and preserving the conductivity properties of monolayer graphene. Figure 5.19 shows a cross section of the isolator

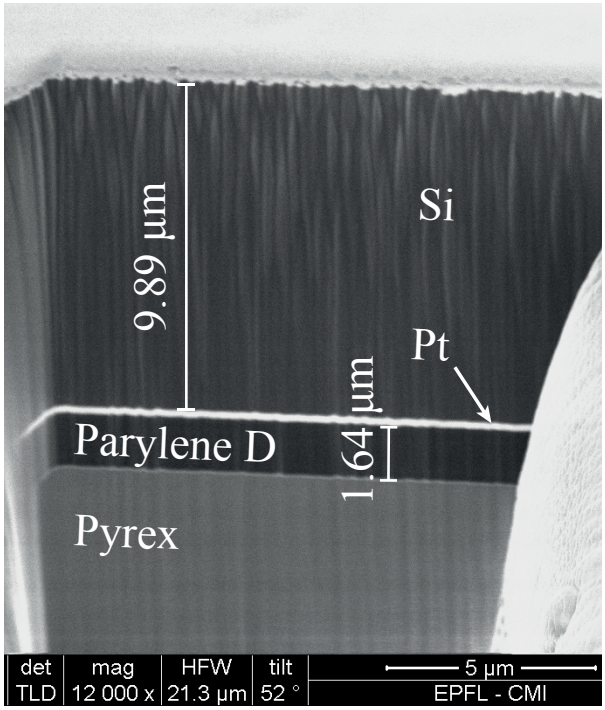


Figure 5.19: FIB cross-section of the device. The cross section confirms the thickness of the silicon layer (expected to be 10 µm). Because this is a destructive analysis, it has been performed on another chip from the same wafer, hence no graphene-PMMA stack is visible in this picture.

stack, before graphene transfer, obtained with a focused ion beam (FIB).

5.3.4 Characterization

The fabricated device has been measured using a FTIR (Fourier Transform InfraRed spectrometer) connected to a split-coil superconducting magnet. A polarizer is used to create a linearly polarized incident light, while an analyser (i.e. a second polarizer) is used in front of the detector (see Figure 5.20.a). The reflected elliptical polarization is mapped by repeating the measurement for different values of the angle Θ between the two polarizers. The magnetostatic field is normal to the sample surface, while the light $\vec{k}$ vector is close to normal. The normalized reflection shows strong absorption dips. These strong absorption features have a periodicity of 4.65 THz, corresponding to Fabry-Perot oscillation in a silicon layer of 9.43 µm in very good agreement with the nominal value. Figures 5.20.b show instead a rich polarization behaviour for B = 7 T. This is also shown better by the polarization diagrams in Figure 5.17.c at selected frequencies of interest. At the first working point we also notice that the Kerr rotation φ goes up to 90°, and continues from -90° to 0°.

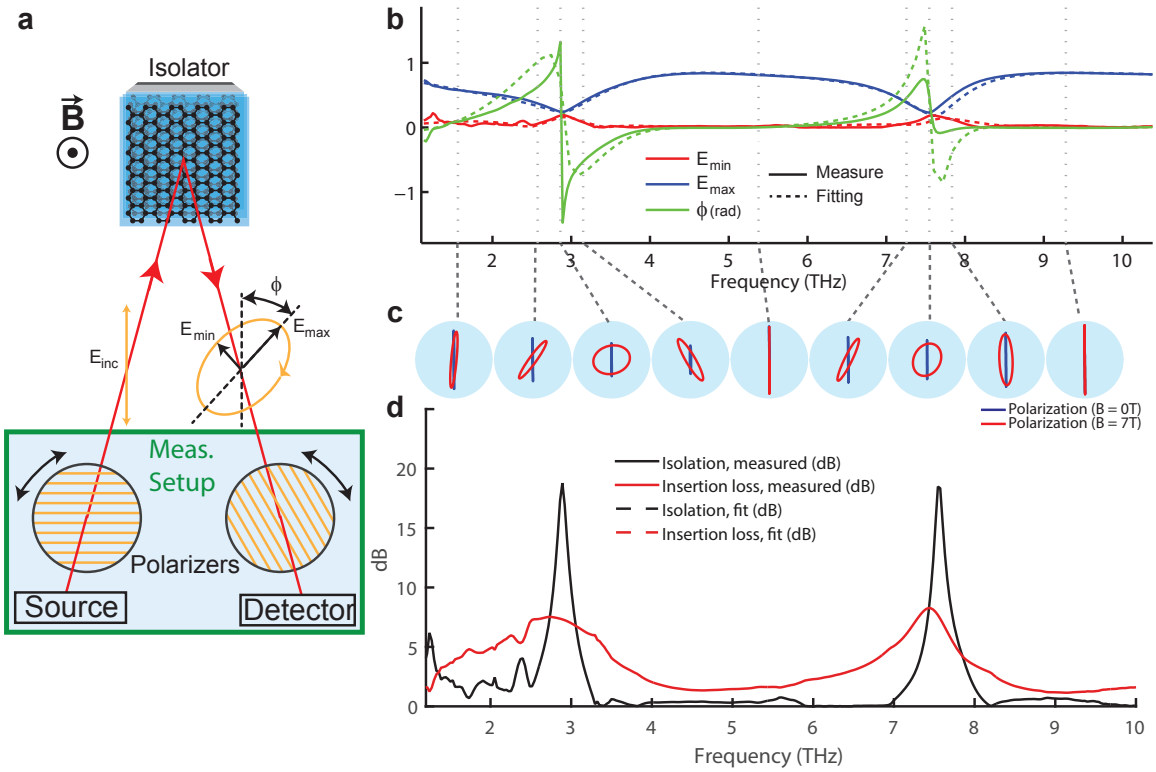


Figure 5.20: Measured isolator performances. Measures have been performed at T = 290 K. a) Schematic of the measurement setup configuration and definition of elliptical polarization parameters. b) measured elliptic polarization parameters (major and minor axis $E_{\min}$, $E_{\max}$ and Kerr rotation angle φ) as a function of frequency for $B = 0\,\mathrm{T}$ and $7\,\mathrm{T}$. $E_{\min}$, $E_{\max}$ are normalized with respect to E_{inc}. The measures have been fitted (dashed traces) with the analytical multilayer model, presented, and the best fit is obtained for $\mu_c = 0.53\,\mathrm{eV}$, $\tau = 35\,\mathrm{fs}$, $d_{\mathrm{SI}} = 9.15\,\mu\mathrm{m}$, additional loss: 30 %. c) polarization state shown for some representative frequencies. d) the extracted performances (isolation and insertion loss) of the isolator for circularly polarized waves.

5.3.5 Discussion

Near-optimal terahertz isolators based on graphene have been demonstrated. Equivalent devices operating in transmission require more complicated structures or lead to suboptimal performances [255, 256]. In addition we identify the following advantages related to this particular device geometry:

- Due to the fact that it is planar, it can work for several incident beams at the same time.
- Electric field effect could be used to fine tune the device to virtually infinite isolation, as demonstrated also at microwave frequencies [259].

- The absolute bandwidth is in the order of 50 GHz, which is an excellent value for telecommunications and for continuous wave applications. This value can possibly be increased using more complex designs including graphene patterning, added metal structures and more complex multilayer structures.
- The working frequency is given by the substrate thickness, and hence it can be controlled and fine-tuned in a precise way by polishing the substrate or using additive dielectric depositions.
- The reflection configuration of the device eliminates completely the input impedance mismatch (return loss), which is instead a concern for any device operating in a transmission configuration. This is due to the fact that an incident left hand wave cannot be possibly reflected as left hand because the device is invariant to rotation.

On the other hand, the main drawbacks of the device are the need of high magnetic field (7 T) and an insertion loss of more than 5 dB. The way to lower the insertion loss and reduce the required B biasing field is to use graphene with higher mobility. With a mobility of $40\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and a biasing field of 1 T (easily generated by rare earth permanent magnets) the insertion loss for perfect isolation would be as low as 0.3 dB according to theoretical estimations of the maximum performance [231], paving the way to commercially relevant devices.

5.3.6 Applications

The applications of the proposed isolator consist mainly in source protection, namely the isolator is placed in front of the source and, while it allows the energy from the source to propagate, it blocks any incoming wave which could potentially damage the source. More complex non reciprocal devices could be used as circulators, enabling the so called full duplex communication scheme, where the power from an electromagnetic mode can be coupled to a receiver and a transmitter at the same time.

5.4 Graphene for IR Applications

5.4.1 Motivation

In this section we present a method to measure the IR properties of graphene using FTIR. As mentioned in the previous section, this technique enables the measurements of transmittance or reflectance of graphene placed on a substrate. Unfortunately, the standard technique enables only the extraction of the real part of the conductivity, which is linked to the absorbance of

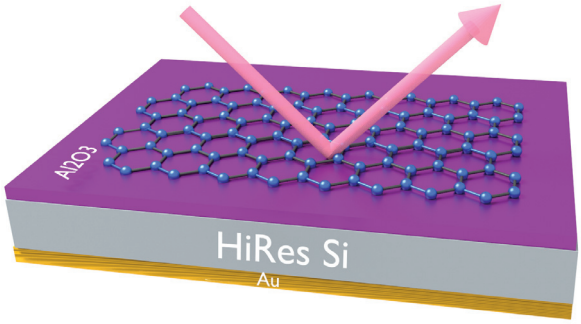


Figure 5.21: Fabricated reflection structure used for FTIR measurements.

the graphene sample. Very important information is hence lost in the process. Moreover, the ratio of the real and imaginary conductivity, which is an indicator of the quality of the sample, cannot be observed directly.

Kramers-Kronig relations can be used to reconstruct the imaginary conductivity from the real one, but have several important limitations. First, their accuracy can be easily spoiled in presence of e.g. Fabry-Perot resonances induced by the substrate. It is important to note that graphene conductivity shows very broadband features, such as the interband step. Kramers-Kronig, on the contrary, are effective only in presence of sharp and narrowband features, while they are impractical for broadband effects as they require integration of a very broad frequency range, often outside the range of the instrument.

Because of the important limitations of Kramer-Kronig reconstruction, ellipsometry has been used to retrieve directly the complex conductivity of graphene [260]. Unfortunately mid infrared ellipsometry requires large spot size (in the order of two centimetres) and the method shown in [260] relies on CaF_2 substrates, preventing Fermi-Level tuning.

In collaboration with the Laboratory of Electromagnetics and Acoustics (LEMA) and the BioNanoPhotonic Systems Laboratory (BIOS) at EPFL, a new method has been developed to measure the full complex conductivity of gated graphene at infrared frequencies using an FTIR setup. The method has the advantage of being able to resolve the conductivity in samples as small as 200 µm with the aid of a microscope connected to the FTIR setup. It consists in placing graphene over a special substrate composed of a pyrex support bonded to a 10 to 20 µm thick high resistivity silicon layer with a metallization on the back, as the one used for the THz isolator described in the previous section §5.3, where a more complete description including the detailed fabrication is available. The schematic of the measured structure is illustrated in the Figure 5.21.

The thin silicon layer acts as a reflective Fabry-Perot etalon, namely a device showing strong and frequency-periodic absorption peaks in the reflectivity. The presence of graphene affects the shape of the peaks as noticed in [261]. There are two independent effects:

- The real part of the conductivity affects the depth of the peak;
- The imaginary part of the conductivity introduces a phase shift in the peak.

By comparing the peaks in a region of the substrate with and without graphene, its complex conductivity can be successfully measured. Graphene is gated using the silicon layer, thus tuning its Fermi level. We verified that the interband step changes upon bias, as well as the features of the measured complex conductivity. The rest of this section illustrates the obtained experimental results.

5.4.2 Characterization

The samples are characterized by Fabry-Perot infrared complex conductivity measurements. Figure 5.22 illustrates an example of the reflection coefficient of the bare substrate for different frequencies. The periodicity in frequency is due to the thickness of the silicon etalon (10 µm) which behaves as a dielectric with relative permittivity of 11.6 in the IR region.

Figure 5.23 shows a single absorption dip measured on bare substrate and on graphene (biased at −16 V to increase graphene conductivity and better show the effect). It is clear that graphene

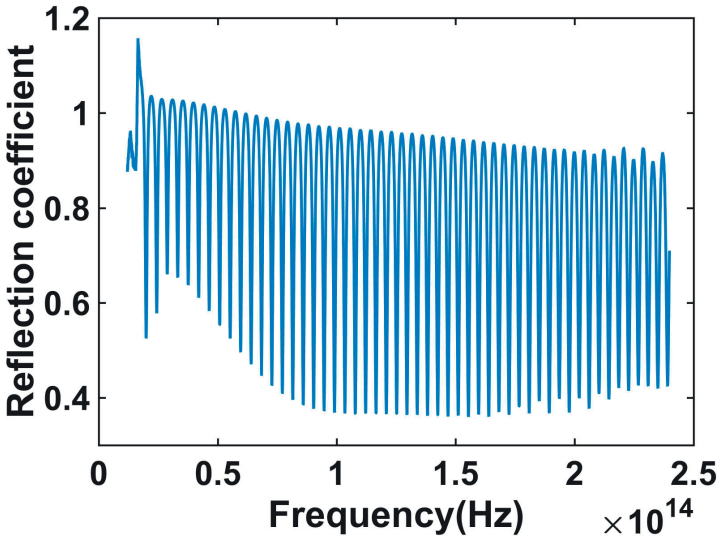


Figure 5.22: Fabry-Perot periodic dips in the reflection coefficient of the bare substrate

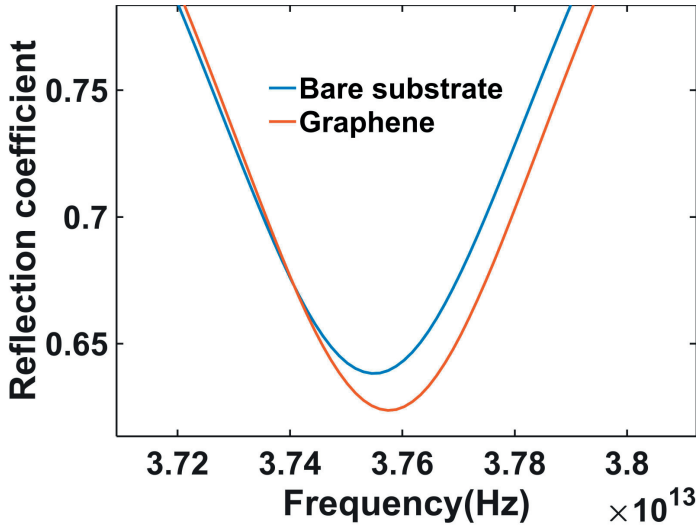


Figure 5.23: Perturbation of a single Fabry-Perot absorption dip induced by graphene

contributes to higher absorption (due to the real part of graphene conductivity) and to a frequency shift which correspond to an inductive behaviour, as expected for graphene in this frequency band.

Figure 5.24 shows an example of characterized complex conductivity for $-4\,\mathrm{V}$, and the corresponding fitting with Kubo formula, while Figure 5.25 shows the conductivity for different biasing voltages.

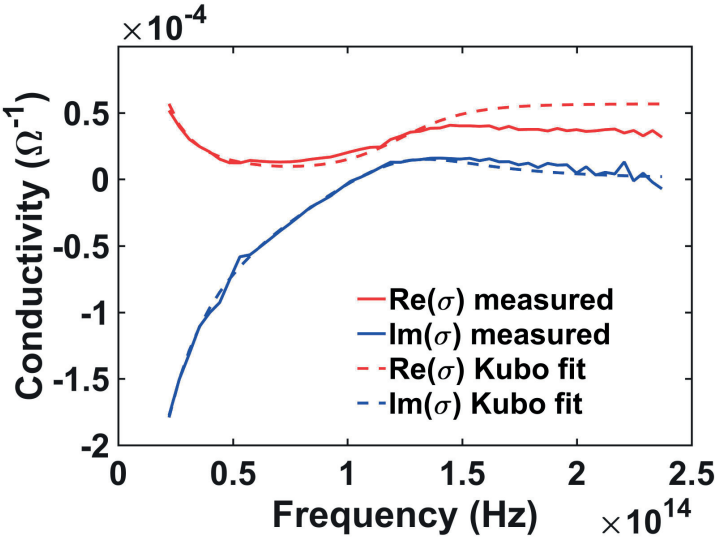


Figure 5.24: Measured complex conductivity of graphene for gate voltage of -4V and corresponding fitting with Kubo formula, parameters τ=24.4 fs, μ_c=0.253eV

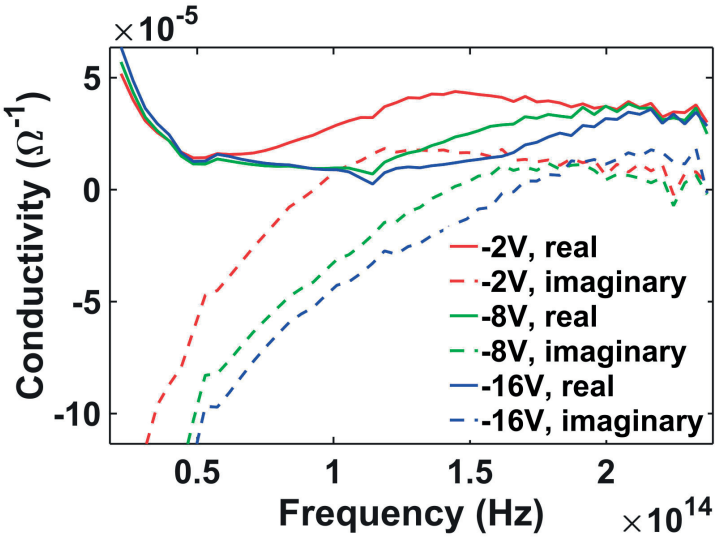


Figure 5.25: Measured complex conductivity of graphene for different biasing voltages.

It is evident that, the larger the absolute value of the voltage, the larger is the frequency for the interband step, and also the the larger is the imaginary part of the conductivity, due to the increase of carrier number.

5.4.3 Applications

The proposed technique has mainly the purpose of characterizing the full 2D conductivity of any bidimensional material. It could be used for instance to measure other materials, such as MoS_2, black phosphorous, WS_2 or WSe_2. Unlike ellipsometry, this method allows the full measurement of anisotropic conductivities (e.g. in black phosphorus). The sample configuration allows biasing the materials, and hence enables a full thorough characterization. A part from the evident applications of spectroscopy of 2D materials, the study of conductivity variation in real time becomes possible, opening the way to sensing applications, which require a constant monitoring of the material upon interactions with gas or other substances. Furthermore the material can be patterned and, or, metal elements can be added in order to extract the effect of these elements on the global material conductivity. Finally, these possibilities can be extended to any heterostructure composed of arbitrary assemblies of 2D materials, providing a novel tool for 2D materials characterization.

5.5 Conclusions

Reconfigurable graphene stacks for THz applications have been demonstrated. Measuring the total stack conductivity for various combinations of gate voltages permits the extraction of the different parameters that define each of the layers but also the determination of the effective gate capacitance of the surrounding dielectrics. The results show that reconfigurable graphene stacks boost the conductivity tunability provided by single-layer structures, thus facilitating the easy implementation of THz and mid-infrared devices with enhanced reconfiguration capabilities.

Moreover, the possibility to design and implement close to optimal terahertz isolators based on graphene has been demonstrated. To achieve this goal, a reflection structure which exploits the Fabry-Perot resonances in a thin layer of silicon to obtain isolation using just three graphene monolayers has been fabricated using a customized process. In addition, it was demonstrated that the same reflection structure can be used to characterize the graphene impedance in the IR frequency range.

This chapter includes the following contributions:

- A general iterative fabrication of large area graphene/dielectric stacks has been developed and its THz applications have been demonstrated.
- Reflection substrates for THz applications consisting in a metal/silicon stack have been developed and employed in the manufacturing of a graphene THz isolator.
- Characterization of graphene at THz and infrared frequencies has been performed.

6. Conclusion

6.1 Summary of Thesis Achievements

We have demonstrated in this work graphene's potential for reconfigurable high frequency functions, and investigated experimentally its integration compatibility with traditional CMOS and MEMS technologies. Several graphene-based devices have been proposed as basic elements in reconfigurable technologies for high frequency.

We briefly reiterate the main contributions of this thesis:

Graphene Synthesis, Transfer and Characterization

- We have proposed several techniques for the transfer of suspended and supported graphene and evaluated the electrical properties of the samples by KPFM and FTIR. We obtained a quantification of the effect of disorder due to transfer on the electrical properties.
- Exfoliated graphene with dimensions up to 15×20 µm has been suspended on cavities by a clean reliable process, suitable for proof-of-concept integration of graphene in NEMS.
- A scalable process to suspend CVD patterned graphene by a dry transfer method has been developed. Suspended membranes up to 15×15 µm have been achieved, with a yield higher than 50 %, superior to previous reports.
- We have shown through an empirical study the suitability of these techniques for device manufacturing and discussed the challenges specific to graphene growth, manipulation and processing, and their influence on its electronic properties.

Graphene NEMS Switches for RF Applications

- We have developed a novel process and method for a graphene RF NEM switch configuration: the capacitive shunt switch.
- The switches were fabricated using standard MEMS processing by suspending graphene membranes on a coplanar waveguide by three different strategies: sacrificial etching of an underlying LTO layer, wet transfer of exfoliated flakes on top of the NEMS cavities and a large scale printing of CVD graphene stripes on cavities.

- We have shown that sacrificial etching has low reliability in the case of graphene membranes and have discussed in detail the main technological challenges. The process resulted in strained or even teared suspended membranes. The GNEMS realized using this strategy are actuated at 10 V (due to high membrane strain), leading to a very low down state isolation of −1.6 dB at 6 GHz. The capacitance ratio was ∽17.5, superior to similar devices realized with CNTs. The switch did not recover after actuation. This did not represent a viable method for graphene switches manufacturing, but offered important insights into the main limitations of using graphene for NEMS, allowing a process optimization for the next fabrication runs. Also, this was the first demonstration of an RF GNEMS shunt capacitive switch.

- We have successfully demonstrated proof-of-concept GNEM switches based on exfoliated graphene that achieve an isolation of −6 dB at 40 GHz, limited only by the high resistance of the exfoliated graphene. The switches were actuated at 2.9 V and the estimated switching time was 136 ns, results superior to metal MEMS. However, the results are poorer than expected for graphene due to the high strain in the membranes. The switches have been actuated for over a hundred times during experiments without degrading their properties, showing good reliability. However, a thorough reliability study has not been performed yet. In addition, we have shown by calibrated simulations that the developed technology can achieve isolations of −15 dB by using graphene with a sheet resistance of 100 Ω/□. This result makes GNEMS competitive with metal MEMS for switching applications in terms of RF performance with superior mechanical parameters.

- The equivalent circuit model has been established and validated experimentally, obtaining an excellent fit to the measured results for all the fabrication strategies. Based on the model, the potential of optimised devices and their use in applications has been assessed.

- Analog and digital phase shifters, based on the RF GNEMS tunable capacitors, periodically loaded on a coplanar waveguide were demonstrated by calibrated simulations, using the experimental data for the GNEMS varactor. For an optimised release process, the analog device consisting of 30 stages has shown a differential phase shift of 30° at 2.4 GHz and the digital one a differential phase shift of 42° at 2.4 GHz. The digital design achieves a higher phase shift with miniaturized dimensions at the cost of higher loss. These results show that graphene-based RF NEMS could be considered as future candidates for RF phase shifters, providing additional features with respect to metal RF NEMS, if graphene release is further controlled and optimized. This would require the reliable fabrication of more than 60 devices (30 stages), and therefore a very well established process to suspend graphene in a controllable way. This work constitutes a first exploratory step in this direction, with future optimisations required to make this task feasible.

Graphene Quantum Capacitors for RF Applications

- A tunable capacitor structure based on graphene quantum capacitance has been demostrated for the first time in the radio-frequency range.
- Very good performance is reported, achieving a tunability factor of 1.32:1 extracted with 1 V voltage tuning. Therefore its operating voltage and tunability are better, respectively comparable, to the ones of metal M/NEMS and even GNEMS capacitors.
- Based on the developed model, we have presented and evaluated a performance booster strategy. By scaling the geometrical parameters of the device, we can achieve a Q of 122 at 5.3 GHz and a superior performance compared to alternative technologies above 2.1 GHz. Novel guidelines were provided to establish a pathway for design and fabrication optimizations of GQC. The simple and robust design can be adapted to achieve competitive solutions for large scale, high density integrated low-power RF analog circuits.
- This device represents a breakthrough, specific to graphene that cannot be mimicked in any other existing technology. Its analog tunability makes it highly desirable for RF applications such as microwave filters and phase shifters.
- Phase shifters have been demonstrated experimentally, obtaining a differential phase shift of 20° at 5.8 GHz with 20 stages, as a proof-of-concept for successfully employing GQCs for analog tuning of the phase shift of a transmission line. A phase shifter operating at 5.8 GHz was designed, achieving 180° at 5.8 GHz by increasing the number of stages to 196, and its performance can be accurately predicted bases on the performed measurements. The main limitation of the phase shifter is the loss due to the thin dielectric and the difficulty to transfer large area graphene (8 cm long).
- This solid state device has the advantage of a straightforward scalable fabrication, compared to GNEMS, and a superior performance for analog RF applications, as the high resistivity of graphene, which is generally the limiting factor for RF applications, can be accounted for by an interdigitated design.

Graphene for THz Applications

- We have demonstrated graphene integration in far and mid-infrared applications, and have established technological frameworks for transmission and reflection experiments. This allowed the experimental evaluation of graphene's potential for various applications at THz and IR.

- We have demonstrated that reconfigurable graphene stacks boost the available range of conductivity values provided by single-layer structures, facilitating an easy implementation of THz and mid-infrared devices with enhanced reconfiguration capabilities.

- We have transferred graphene multi-stacks on custom engineered substrates allowing the realization of the first THz isolator, with optimal performance.

- We have shown that graphene offers reconfigurability possibilities in the mid and far-IR frequency range with relatively simple architectures, difficult to achieve by other technologies.

6.2 Outlook and Perspectives

Tremendous progress has been achieved in the past years in graphene production and manufacturing methods as well as toward its integration in devices. However, large scale production, reliability of processing and performance are still open issues to be addressed. We have shown in this thesis how the properties of graphene are still highly influenced by production methods, substrate, environment, post-processing methods etc. This is the major milestone that needs to be achieved in order to exploit the unique properties of graphene for reliable devices with increased performance.

Below, a few of the most stringent requirements and issues that need to be addressed in order to adopt graphene as the next technological standard for reconfigurable electronics as well as for more general purposes, are briefly mentioned:

- A reliable production of uniform graphene with a sheet resistance of $30\,\Omega/\,\square$ would enable the use of graphene in high frequency applications with a competitive performance with the traditional reconfigurable elements (semiconductors or metal MEMS), with the gain of added specific functionalities.

- Optimize the growth of graphene on the desired substrates (for example insulators on silicon wafers) or establish a reliable transfer method of large area graphene. In the framework of the "Grafol" European project, the first steps toward the achievements of a roll-to-roll technology have been validated. The development of this technology constitutes a major breakthrough in wafer scale processing of graphene devices, and could eventually enable reliable, defect free transfer of large area graphene on wafers, integrating this process in CMOS or MEMS technological flows.

- Removing polymer residues left from transfer or lithography steps. One solution could be the use of passivation layers protecting the graphene sheets from the environment (substrate, atmosphere, impurities) and one option that has been explored was 2 dimensional hexagonal boron nitride (h-BN) that proved efficient in maintaining the properties of graphene.
- Contact resistance engineering is still ongoing, and to date ohmic contacts with resistances in the order of few ohms have not been achieved. The contact resistance is generally highly dependent on sample and processing.
- Monolithic integration: the high resistivity of graphene hinders the possibility to achieve monolithically-integrated reconfigurable high-frequency functions.

One area where graphene has a significant advantage compared to conventional technologies is flexible and wearable electronics, due to its superior elastic properties compared to metals or traditional semiconductors. Also, at far and mid-infrared frequencies graphene opens novel possibilities for applications that could not be achieved with traditional technologies.

Although fundamental issues still need to be resolved, we have taken a step towards realizing graphene's tremendous potential for high frequency reconfigurable electronics, bringing unique advantages that cannot be matched by alternative technologies.

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List of symbols

Symbol	Units	Description
a_{B}	m	Effective Bohr radius
B	T	Magnetostatic field
C_{d}	F	MOSFET deplection capacitance
C_{max}	F	GQC maximum capacitance
C_{min}	F	GQC minimum capacitance
C_{ox}	F	MOSFET oxide capacitance
$C_{\mathrm{ox}}^{\mathrm{p}}$	F	Capacitance of the p dielectric layer in graphene stacks
C_{p}	F	Shunt capacitance of the g tunable capacitor
C_{q}	F	Graphene quantum capacitance
C_{s}	F	Series capacitance of the g tunable capacitor
D	m	Interatomic distance
d	m	Thickness of the dielectric layer in graphene stacks
d_{SI}	m	Thickness of the device layer in the THz isolator
E_{F}	eV	Chemical potential
e	C	Electron charge
F_{ω}	N	Electrostatic force monitored in KPFM
f	Hz	Frequency
f_{b}	Hz	Bragg frequency
G_{L}	S	Leakage conductance
g_0	m	Height of the suspended membrane
k	$\mathrm{N\,m^{-1}}$	Effective spring constant
k_{B}	$\mathrm{eV\,K^{-1}}$	Boltzmann's constant
I_{d}	A	Drain current
I_{DC}	A	DC current source
L	m	Device length
l	m	Mean free path length
N	1	Number of gate fingers in GQC

N_S	1	Number of graphene sheets
n	m^{-3}	Carrier density
n_c	m^{-3}	Carrier density
n_i	m^{-3}	Impurity carrier density
n_s^p	m^{-3}	Carrier density in the p layer in graphene stacks
n_{si}^p	m^{-3}	Pre-doping of the p layer in graphene stacks
Q	1	Quality factor
R_{leak}	Ω	Leakage resistance
R_s	Ω	Series resistance
S	m	Spacing between gate fingers in GQC
S_{11-ON}	dB	Return loss
S_{21-OFF}	dB	Isolation
S_{21-ON}	dB	Insertion loss
T	K	Temperature
T_{MIT}	K	Metal-Insulator Transition temperature
TR	1	Tuning ratio
t_g	m	Thickness of the graphene's membrane
t_{ox}	m	Oxide thickness
V_{act}	V	Actuation voltage
V	V	Voltage
V_{AC}	V	AC voltage source amplitude
V_{ch}	V	Average graphene potential
V_{DC}	V	DC voltage source
V_1	V	Voltage on the bottom layer in graphene stacks
V_2	V	Voltage on the top layer in graphene stacks
v_F	$m\,s^{-1}$	Fermi velocity
V_{OP}	V	Operation voltage
V_{PI}	V	Pull-in or actuation voltage
v_p	$m\,s^{-1}$	Phase velocity
W	m	Device width
Γ	1	Scattering rate
$\Gamma_{L\to R}$	dB	Reflection coefficient in the THz isolator (CCW)

$\Gamma_{R\to L}$	dB	Reflection coefficient in the THz isolator (CW)
Δ_{L}	m	Periodic spacing in a phase shifter
ϵ_r	1	Effective dielectric constant
η	Ω	Free space impedance
λ	m	Wavelength
$\mu_{\mathrm{c}}^{\mathrm{bot}}$	eV	Chemical potential of the bottom layer in graphene stacks
$\mu_{\mathrm{c}}^{\mathrm{top}}$	eV	Chemical potential of the top layer in graphene stacks
E_{F}	eV	Chemical potential
ρ	$\Omega\,\mathrm{m}$	Electrical resistivity
σ	eV	Chemical potential standard deviation
σ_{CCW}	S	Graphene conductivity in the THz isolator (CCW)
σ_{CW}	S	Graphene conductivity in the THz isolator (CW)
σ_{S}	S	Stack conductivity
σ_{bot}	S	Stack conductivity of the bottom layer
σ_{top}	S	Stack conductivity of the top layer
τ	s	Relaxation time
τ_{bot}	s	Relaxation time of the bottom layer in graphene stacks
τ_{top}	s	Relaxation time of the top layer in graphene stacks
Θ	$^\circ$	Angle between polarizers
ϕ	$^\circ$	Kerr rotation
ϕ_{sample}	eV	Sample work function
ϕ_{tip}	eV	KPFM Tip work function
Ψ_{S}	V	Surface potential
ω	rad	Angular frequency

Acronyms and Abbreviations

AC	Alternate Current
ADS	Advanced Design System
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
APS	Ammonium persulphate solution
a.u.	Arbitrary Unit
BHF	Buffered Hydrofluoric Acid
BLG	Bilayer Graphene
CMOS	Complementary Metal-Oxide-Semiconductor
CPW	Coplanar Waveguide
CPD	Critical Point Drying
CVD	Chemical Vapour Deposition
CCW	Counter-Clockwise
CW	Clockwise
DC	Direct Current
DMTL	Distributed MEMS transmission lines
DNA	Deoxyribonucleic acid
DNTL	Distributed NEMS transmission lines
DRIE	Deep Reactive Ion Etching
EBL	Electron Beam Lithography
EG	Epitaxial graphene
EGT	Expanded graphite
EOT	Equivalent oxide thickness

E-MIT	Electrically Induced Metal-Insulator-Transition
e.g.	exempli gratia
et al.	et alii (and others)
FET	Field Effect Transistor
FIB	Focused Ion Beam
FLG	Few-Layer Graphene
FM	Frequency Simulation
FTIR	Fourier Transform Infrared Spectroscopy
GFET	Graphene field effect transistors
GICs	Graphite intercalation compounds
GQC	Graphene quantum capacitors
GQCn	Optimised new graphene quantum capacitors
GNEMS	Graphene Nano Electromechanical Systems
GO	Graphene oxide
HFSS	High Frequency Structural Simulator
HOPG	Highly ordered pyrolytic graphite
HR	High Resistivity
IC	Integrated Circuit
ICT	Information and Communication Technology
IR	Infrared
IT	Information Technology
ITRS	International Technology Roadmap for Semiconductors
i.e.	id est (that is)
KPFM	Kelvin Probe Force Microscopy
LED	Light Emitting Diode

LHCP	Left Hand Circularly Polarized
LPCVD	Low-Pressure Chemical Vapor Deposition
LQ	Liquid Crystals
LTO	Low Temperature Oxide
MBE	Molecular beam epitaxy
MEMS	Microelectromechanical Systems
MIM	Metal Insulator Metal
MIT	Metal Insulator Transition
MLG	Multilayer Graphene
MOCVD	Metal-Organic Chemical Vapor Deposition
MOSCAP	Semiconductor Varactors
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
MTBF	Mean time between failures
NEMS	Nano Electromechanical Systems
OLED	Organic light-emitting diode
PAT	Polymer-assisted transfer
PCB	Printed Circuit Board
PDMS	Polydimethylsiloxane
PMMA	Poly(methyl methacrylate)
PNA	Programmable Network Analyzer
RF	Radio Frequency
RFID	Radio Frequency Identification
RHCP	Right Hand Circularly Polarized
RT	Room Temperature
SLG	Single Layer Graphene
SEM	Scanning Electron Microscope

SI	International System of Units
SL	Signal Line of the Coplanar Waveguide
SNR	Signal to Noise Ratio
SOI	Silicon on Insulator
SOLT	Short-Open-Load-Through
SOS	Silicon on Sapphire
TEM	Transmission electron microscope
THz-TDS	Terahertz Time Domain Spectroscopy
TRL	Thru-Reflect-Line
TTD	True-Time Delay
UV	Ultra Violet
UHV	Ultra High Vacuum
VCO	Voltage Controlled Oscillator

List of Publications

JOURNAL PAPERS

C.F. Moldovan et al., "RF NEMS Graphene-Based Capacitive Switches," ACS Nano, in preparation, 2016.

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Clara Moldovan

Phone: +41(0)788243800
e-mail: clara.moldovan@epfl.ch
Rue de Chavannes 17
1007, Lausanne, Switzerland
https://ch.linkedin.com/in/claramoldovan

Objective

I am passionate about designing and developing electronic devices based on reconfigurable technologies and novel materials for electronic and sensing applications.

Education

PhD, Microengineering **2011 – 2016**

École Polytechnique Fédérale de Lausanne (EPFL), Switzerland - Nanoelectronic Devices Laboratory

PhD Thesis: Enabling High Frequency Reconfigurable Functions with Graphene

- I have investigated the use of graphene for various high frequency and sensing applications. This project was done under the framework of the European project "GRAFOL—Graphene Chemical Vapor Deposition: Roll to Roll Technology ", whose main objective was the development of the first roll-based chemical vapor deposition machine for mass production of few-layer graphene and use it in applications like transparent electrodes for OLEDs and GaN LEDs, VLSI interconnects, sensors and RF NEMs.
- I have developed a process to suspend multilayer graphene, I designed, fabricated and characterized NEM capacitive switches and quantum varactors.
- I explored the opportunities offered by graphene's properties for reconfigurable devices at THz and IR frequencies.
- I have performed a thorough structural and electrical characterization of graphene membranes using techniques like conductive atomic force microscopy, Kelvin force microscopy and scanning electron microscopy.

MSc, Microengineering **2009 – 2011**

École Polytechnique Fédérale de Lausanne, Switzerland

MSc Thesis: Towards Ultra-sensitive Mass Sensing with Resonant Body Transistors

- I performed various experiments on a novel NEM- FET device in different operating conditions.
- I demonstrated its potential use as a biosensing platform and established a method for biomolecules deposition on the active area of the device.

BSc, Electrical Engineering **2005 – 2009**

Polytechnic University of Bucharest, Romania

BSc Thesis: Fabrication and Characterization of Silicon Nanowire Transistors for Biosensing Applications

Experience

Visiting Researcher **June – Aug. 2010**

Laboratory of Physical Chemistry of Polymers and Membranes, EPFL, Switzerland

I have performed Reverse Fluorescence Correlation Spectroscopy measurements for single molecule detection using zero-mode waveguides. The aim of the project was to immobilize quantum dots on the walls of nanocavities constituting the waveguides, in order to facilitate the ultrasensitive detection of molecules as they enter the cavities. The project offered me experience with confocal microscopes and an introduction to surface functionalization, biomolecule immobilization protocols and COMSOL simulations.

Intern **June – Aug. 2008**

Tyndall National Institute, Cork, Ireland

I worked on protein-silicon interface simulation and bio-ICT interfaces analysis within the "Modelling Bio/ICT interfaces for Next Generation Bionanoelectronics" project. I did molecular dynamics simulations of the interaction of a hydrophobic protein with a silicon surface using NAMD software. The simulations were done on a Blue Gene supercomputer, with training provided by IBM, Dublin.

Intern **June – Aug. 2007**

National Institute for R&D in Microtechnology (IMT-Bucharest)

I worked on microfluidic simulations of microchannels used in biosensors using CoventorWare, in the Laboratory of Microsystem for Biomedical and Environmental Application. The main work was on simulating the flow and thermal dissipation of a preheated liquid inside microfluidic channels.

Intern **Aug. 2006**

National Institute for R&D in Microtechnology (IMT-Bucharest)

I have simulated the behavior of a piezoresistive differential pressure sensor created from a 1mm x 1 mm membrane, 10 micron thick, with four integrated resistors on top.

Extracurricular Activities

Venture Challenge, Swiss Confederation **Sept. 2010 – Jan. 2011**

I participated, in a team of 5 people, to the Venture Challenge course, to improve my entrepreneurship skills, business and legal knowledge, and meet investors and startup experts, through writing a business plan and preparing a pitch for our startup idea, performing market studies and discussing with potential customers. Our startup idea was to develop and sell flexible pressure sensors suitable for orthopedic implants.

iGEM Competition on Synthetic Biology **June – Oct. 2011**

The International Genetically Engineered Machine competition (iGEM) challenges groups of students to design and build biological systems and operate them in living cells. My team developed a pipeline for the selection and characterization of new transcription factors. I have worked on the in vitro characterization of affinity and specificity of mutants using a MITOMI microfluidic platform. On the community outreach side of the project, I have developed and fabricated a microfluidic system for introducing biology students to microfluidics.

Languages

Romanian, English, French