Hybrid NRZ/Multi-Tone Signaling for High-Speed Low-Power Wireline Transceivers

PAR

Kiarash GHARIBDOUST

EPFL

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Suisse
2016

The only thing greater than the power of the mind
is the courage of the heart.
— John Nash

To my wife Haniyeh, my mother Parvaneh
and
to the memory of my father ...

Acknowledgements

This thesis work would not have been possible without all the people that supported me throughout these years. I have been especially lucky to have had so many great people helping me out with different aspects of my life in EPFL.

I would first like to express my sincere gratitude to my advisor, Prof. Yusuf Leblebici for his endless support, for his patience, motivation, and immense knowledge. His guidance helped me to overcame the biggest obstacles I faced during my PhD, both on technical and non-technical sides. I would like to thank him for his tolerance and patience in letting me explore different ideas, and for always encouraging me to think revolutionary about the issues that I faced. I am extremely thankful to my co-advisor, Dr. Armin Tajalli, for his advices and the fruitful discussions during the entire length of my PhD studies. I do appreciate his interest, commitment and responsibility to my work. He has always been kind to me with any questions during the course of my PhD research.

I am very grateful towards the members of my thesis committee: Prof. Pavan Kumar Hanumolu, Dr. Thomas Toifl, Prof. Amin Shokrollahi and Dr. Jean-Michel Sallese for taking the time to read this manuscript and provide feedback. I would like to thank Dr. Alain Vachoux for his timeless support on CAD tools and Dr. Alexandre Schmid for his support with computing infrastructure.

I am indebted to my master thesis advisor, Prof. Mehrdad Sharif Bakhtiar for always encouraging me in finding new solutions and giving me the best advice. Most part of my PhD research relies on the analog design techniques, which I learned from this master. I am grateful to Prof. Sadegh Jamali, my undergraduate professor, for always supporting me and help me out in the most difficult time of my undergraduate study.

I am thankful towards my colleagues with whom discussions have been source of new ideas and solutions to difficult problems: Dr. Vahid Majidzadeh, Dr. Alessandro Cevrero, Dr. Hossein Afshari and Dr. Nikola Katic.

Many people in EPFL have contributed to this work. I acknowledge Gain Kim for his assistance on system level analysis and simulation. I should thank Masoud Shahshahani for his assistance in silicon measurements. I acknowledge Cosimo Aprile, Jonathan Narinx, Elmira Shahrabi and Jury Sandrini for their positive attitude and the useful discussions during all the coffee breaks. Having good friends like them made everything nicer in

EPFL for me. Thanks to Sylvain Hauser, for his patience and kind support for providing the test setups for prototype measurements. I would like to thank Dr. Mahbod Heidari and Dr. Omid Talebi for their great friendship and support.

I am grateful to my colleagues in Microelectronic Systems Laboratory (LSM) for their friendship, fruitful discussions and collaborations: Dr. Radisav Cojbasic, Dr. Vladan Popovic, Dr. Masha Shoaran, Reza Ranjandish, Sebastian Rodriguez, Seniz Kucuk and also amazing Kerem Seyid.

I am hugely indebted to my parents, my brother and other family members who always believed in me. Their timeless and countless supports were always motivating during all years of my education. I am very thankful to my brother Kianoosh for his constant love, and for filling in for me at home while I have been away.

My special thanks and enormous gratitude go to my mother Parvaneh for always believing in me, and supporting me with her infinite motherly love. Her unconditional love has been always the major source of motivation for me during all my life.

I would like to greatly thank my beloved wife Haniyeh for giving me the reason to be happy, and strength to work and live. I owe a special thanks to her for always supporting me with her patience and everlasting love, and bearing with times of my mental and physical absence. Without any doubt, she is the secret of my success. I am also very grateful to Haniyeh's family, and especially my mother-in-law Farideh, for being extremely kind and supportive to me in these years.

Going through my life period, I have had many great advisors and teachers. Without any doubt, my father was one of the greatest teacher and also my best friend among them all. Although I lost him many years ago, I can still get enormous motivation by his memory. I am hugely indebted to him and I just hope that some day I will repay the debt by trying to approach the parenting ideal that he set by his example.

Lausanne, 11 March 2016   Kiarash Gharibdoust.

Abstract

Over the past few decades, incessant growth of Internet networking traffic and High-Performance Computing (HPC) has led to a tremendous demand for data bandwidth. Digital communication technologies combined with advanced integrated circuit scaling trends have enabled the semiconductor and microelectronic industry to dramatically scale the bandwidth of high-loss interfaces such as Ethernet, backplane, and Digital Subscriber Line (DSL). The key to achieving higher bandwidth is to employ equalization technique to compensate the channel impairments such as Inter-Symbol Interference (ISI), crosstalk, and environmental noise. Therefore, today's advanced input/outputs (I/Os) has been equipped with sophisticated equalization techniques to push beyond the uncompensated bandwidth of the system.

To this end, process scaling has continually increased the data processing capability and improved the I/O performance over the last 15 years. However, since the channel bandwidth has not scaled with the same pace, the required signal processing and equalization circuitry becomes more and more complicated. Thereby, the energy efficiency improvements are largely offset by the energy needed to compensate channel impairments. Moreover, as the supply voltage scaling has saturated in finer technology nodes, the power dissipation in digital circuits cannot benefit from voltage scaling, hence, the overall energy-efficiency improvement has diminished.

In this design paradigm, re-thinking about the design strategies in order to not only satisfy the bandwidth performance, but also to improve power-performance becomes an important necessity. It is well known in communication theory that coding and signaling schemes have the potential to provide superior performance over band-limited channels. However, the choice of the optimum data communication algorithm should be considered by accounting for the circuit level power-performance trade-offs.

In this thesis we have investigated the application of new algorithm and signaling schemes in wireline communications, especially for communication between microprocessors, memories, and peripherals. A new hybrid NRZ/Multi-Tone (NRZ/MT) signaling method has been developed during the course of this research. The system-level and circuit-level analysis, design, and implementation of the proposed signaling method has been performed in the frame of this work, and the silicon measurement results have proved the efficiency

and the robustness of the proposed signaling methodology for wireline interfaces.

In the first part of this work, a 7.5 Gb/s hybrid NRZ/MT transceiver (TRX) for multi-drop bus (MDB) memory interfaces is designed and fabricated in 40 nm CMOS technology. Reducing the complexity of the equalization circuitry on the receiver (RX) side, the proposed architecture achieves 1 pJ/bit link efficiency for a MDB channel bearing 45 dB loss at 2.5 GHz. The measurement results of the first prototype confirm that NRZ/MT serial data TRX can offer an energy-efficient solution for MDB memory interfaces. The core size area is 85×60 μm^2 and 150×60 μm^2 for the transmitter (TX) and receiver (RX), respectively.

Motivated by the satisfying results of the first prototype, in the second phase of this research we have exploited the properties of multi-tone signaling, especially orthogonality among different sub-bands, to reduce the effect of crosstalk in high-dense wireline interconnects. A four-channel transceiver has been implemented in a standard CMOS 40 nm technology in order to demonstrate the performance of NRZ/MT signaling in presence of high channel loss and strong crosstalk noise. The proposed system achieves 1 pJ/bit power efficiency, while communicating over a MDB memory channel at 36 Gb/s aggregate data rate. The MT nature of the proposed transceiver helps to control the ISI and reduce the far-end crosstalk (FEXT), which results in a very energy-efficient implementation. The core size area is 80×60 μm^2 and 130×60 μm^2 for the TX and RX blocks (including the clock unit), respectively.

Keywords: Decision-feedback equalizer (DFE), differential signaling, inter-symbol interference (ISI), multi-drop bus (MDB), multi-tone signaling, nonreturn-to-zero (NRZ) signaling, far-end crosstalk (FEXT), source-synchronous architecture, dual in-line memory module (DIMM), double-data rate (DDR), Internet of Things (IoT), high-performance computing (HPC).

Résumé

Au cours des dernières décennies, la croissance incessante du trafic du réseau internet et du calcul haute performance ("high performance computing") a conduit à une demande énorme de bande passante. Les technologies de communications digitales combinées avec les tendances de mise à l'échelle des circuits intégrés de haute performance ont permis l'industrie des semi-conducteurs et de la microélectronique à augmenter considérablement la bande passante des interfaces à taux élevé de perte telles que Ethernet, fond de panier (backplane) et ligne d'accès numérique (Digital Subscriber Line). La solution pour obtenir une augmentation radicale de bande passante est d'employer des techniques d'égalisation pour compenser les déficiences du canal de propagation telles que l'interférence inter-symbole (inter-symbol interference), la diaphonie (crosstalk), et le bruit environnemental. Par conséquent, les entrées-sorties (I/Os) d'aujourd'hui ont été équipés avec des techniques d'égalisations sophistiquées pour repousser la limite en bande passante des systèmes.

A cette fin, les avancées technologiques ont continuellement augmenté la capacité de calcul de donnée et amélioré les performances des entrées-sorties durant ces 15 dernières années. Cependant, étant donné que la bande passante du canal n'a pas été élargie au même rythme, le traitement du signal requis et les circuits électrique d'égalisations sont devenus de plus en plus compliqués. Ainsi, les améliorations de l'efficacité énergétique sont largement contrebalancées par l'énergie utilisée pour compenser les déficiences du canal. De plus, puisque la mise à l'échelle de la tension d'alimentation a saturé dans les nœuds technologiques les plus fins, la dissipation de puissance dans les circuits digitaux ne peut en bénéficier. De ce fait, les améliorations globales en terme d'efficacité énergétique ont été affaiblies. Dans ce paradigme de conception, une réévaluation des stratégies de design est devenue une importante nécessité dans le but non seulement de satisfaire les performances en terme de bande passante mais aussi en terme d'efficacité énergétique. Dans la théorie de la communication, il est bien connu que les systèmes de codage et de signalisation ont le potentiel de fournir des performances supérieures sur les canaux de communication limités en bande passante. Cependant, le choix de l'algorithme de communication de données optimal doit être considéré en tenant aussi compte des compromis sur les performances énergétique au niveau du circuit.

Dans cette thèse, nous avons examiné l'application d'un nouvel algorithme et de système

de signalisation pour la communication filaire, particulièrement pour la communication entre microprocesseurs, mémoires et périphériques. Une nouvelle méthode de signalisation hybride NRZ/Multi-Tone (NRZ/MT) a été développée au cours de cette recherche. La conception, l'analyse et l'implémentation au niveau du système et du circuit de cette méthode de signalisation ont été accomplies dans le cadre de ce travail, et les résultats des mesures ont prouvé l'efficacité et la robustesse de cette méthodologie de signalisation pour des interfaces filaires.

Dans la première partie de ce travail, un émetteur-récepteur (TRX) hybride NRZ/MT fonctionnant à 7.5 Gb/s pour mémoire à interfaces bus multipoint (multi-drop bus) a été conçu et fabriquer avec la technologie CMOS 40mn. Tout en réduisant la complexité du circuit d'égalisation pour la partie du récepteur (RX), l'architecture proposée atteint une efficacité de lien de 1pJ/bit pour un canal MDB palliant une perte de 45 dB à 2.5GHz. Les résultats des mesures du premier prototype confirme que le NRZ/MT serial data TRX peut offrir une solution efficace en énergie pour les mémoires à interfaces MDB. La taille du cœur est respectivement de $85 \times 60 \ \mu m^2$ et $150 \times 60 \ \mu m^2$ pour le transmetteur (TX) et le receveur (RX).

Motivé par les résultats satisfaisants du premier prototype, dans la seconde phase de cette recherche, nous avons exploité les propriétés de signalisation multipoint, particulièrement l'orthogonalité parmi les différentes sous-bandes, pour réduire l'effet de diaphonie (crosstalk) dans les interconnexions filaires à haute densité. Un émetteur-récepteur 4-canaux a été implémenté dans une technologie CMOS standard 40nm dans le but de démontrer la performance de la signalisation NRZ/MT en présence d'un canal à haute perte et à forte diaphonie (crosstalk). Le système proposé atteint 1pJ/bit d'efficacité énergétique, tout en communiquant dans un canal d'une mémoire MDB à un débit de donnée de 36Gb/s. La nature MT de l'émetteur-récepteur proposé aide à contrôler l'interférence inter-symbole (inter-symbol interference) et réduire la diaphonie distante (far-end crosstalk), ce qui résulte à une implémentation d'une grande efficacité énergétique. La taille du cœur est respectivement de $80 \times 60 \ \mu m^2$ et $130 \times 60 \ \mu m^2$ pour les bloques TX et RX (en incluant l'unité d'horloge).

Mots clefs: Decision-feedback equalizer (DFE), differential signaling, intersymbol interference (ISI), multi-drop bus (MDB), multi-tone signaling, nonreturn-to-zero (NRZ) signaling, far-end crosstalk (FEXT), source-synchronous architecture, dual in-line memory module (DIMM), double-data rate (DDR), Internet of Things (IoT), high-performance computing (HPC).

Contents

List of Figures

List of Tables

1 Introduction

Internet networking traffic has experienced a tremendous growth in recent years, primarily driven by cloud computing, the Internet of Thing (IoT), high-performance computing systems, enterprise servers, flourishing of social media, recent explosive smart phone advancement, etc. As it has been estimated in [1], in year 2019 mobile IP traffic will be 10 times heavier than what it was in 2014, and the total Internet traffic will nearly triple from 2014 to 2019. Fig. 1.1 (a) illustrates this predications for different application types, whereas Fig. 1.1 (b) highlights the network traffic growth more specifically [1]. Among different applications, the greatest growth belongs to the consumer-video, which is indeed a results of dramatic increase of Internet networking traffic. The heart of the Internet network is the service providers' data centers, which should appropriately provide the content, files, data storage, and switching harbors [14]. Inside data centers, there are big racks containing many servers, storages, switches, and routers, which are all connected with cables. Fig. 1.2 (a) shows an image of a data center located in Mayes County, in Pryor, Oklahoma, USA, which consists of such gigantic infrastructures. In order to connect all modules together, variety of cables with different specifications have been employed, and they can be categorized in several serial link standards, as it is shown in Fig. 1.2 (a). Likewise, in a PC blade server there are several units that should communicate together over copper channel, and depending on the channel length and other specifications of the corresponding link, they can be classified in various wireline standards, as shown in Fig. 1.2 (b) for a sample blade server [3].

In order to increase the network capacity, increasing the per-lane data rate has been a standard approach, and many standards have been developed by Optical Internetworking Forum (OIF), Common Electrical I/O (CEI), Joint Electron Device Engineering Council (JEDEC), and Institute of Electrical and Electronics Engineers (IEEE) to cope with the incessant data bandwidth demand. Thanks to the bandwidth demand explosion in
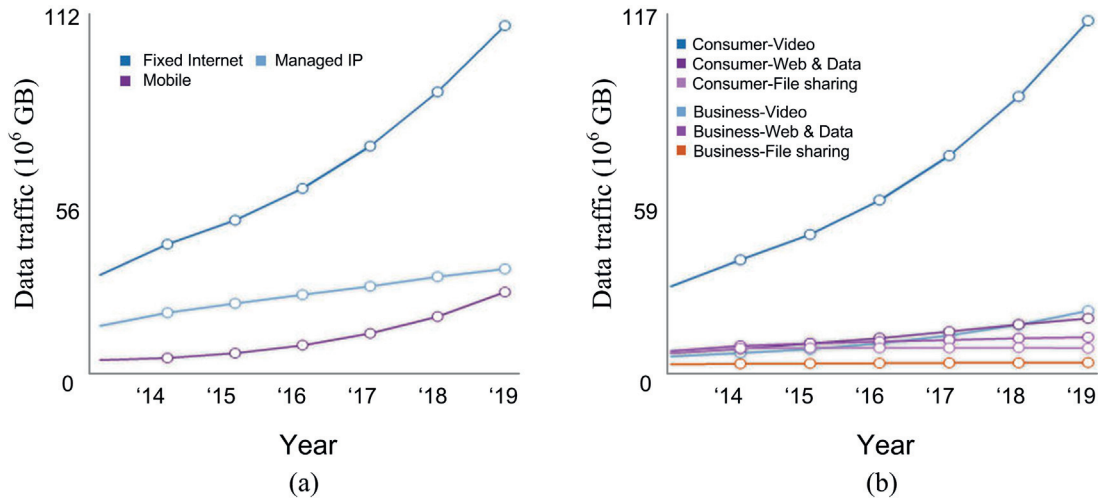
Figure 1.1: Data traffic forecast [1]. (a) Network traffic from 2014 to 2019. (b) Various application data traffic from 2014 to 2019.

Figure 1.2: Differnt serial link applications. (a) a data center in Oklahoma, USA [2]. (b) a blade server containing different links [3].

data centers and telecommunication infrastructures, the data rate growth for wireline transceivers has been consistently increasing at about twice per four years, as shown in Fig. 1.3 for the most-used standards. Hence, peripheral component interconnect express is used ubiquitously in almost all chip-to-chip and chip-to-module interfaces, and OIF, CEI, IEEE, and Ethernet usually come hand-in-hand for different serial link applications. Each standard has its own logic layer, however, the physical layer can be specified by several common parameters, such as data rate, reach (either distance or channel loss in dB), crosstalk, reflections. etc. As an example, multiple 25 Gb/s backplane standards such as CEI-25G long reach (LR) [15], ultra-short reach (VSR) [16], short reach (SR) [17], etc., are developed for various cable lengths. The specification is mainly a bridge among
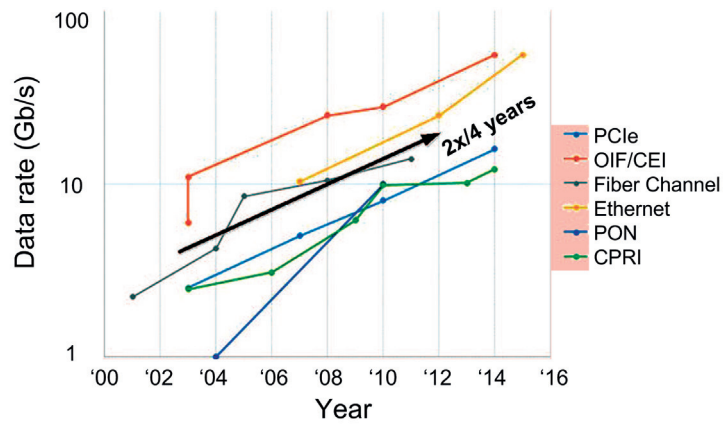
Figure 1.3: Wireline data rates over the years [4].

(a)

(b)

(c)
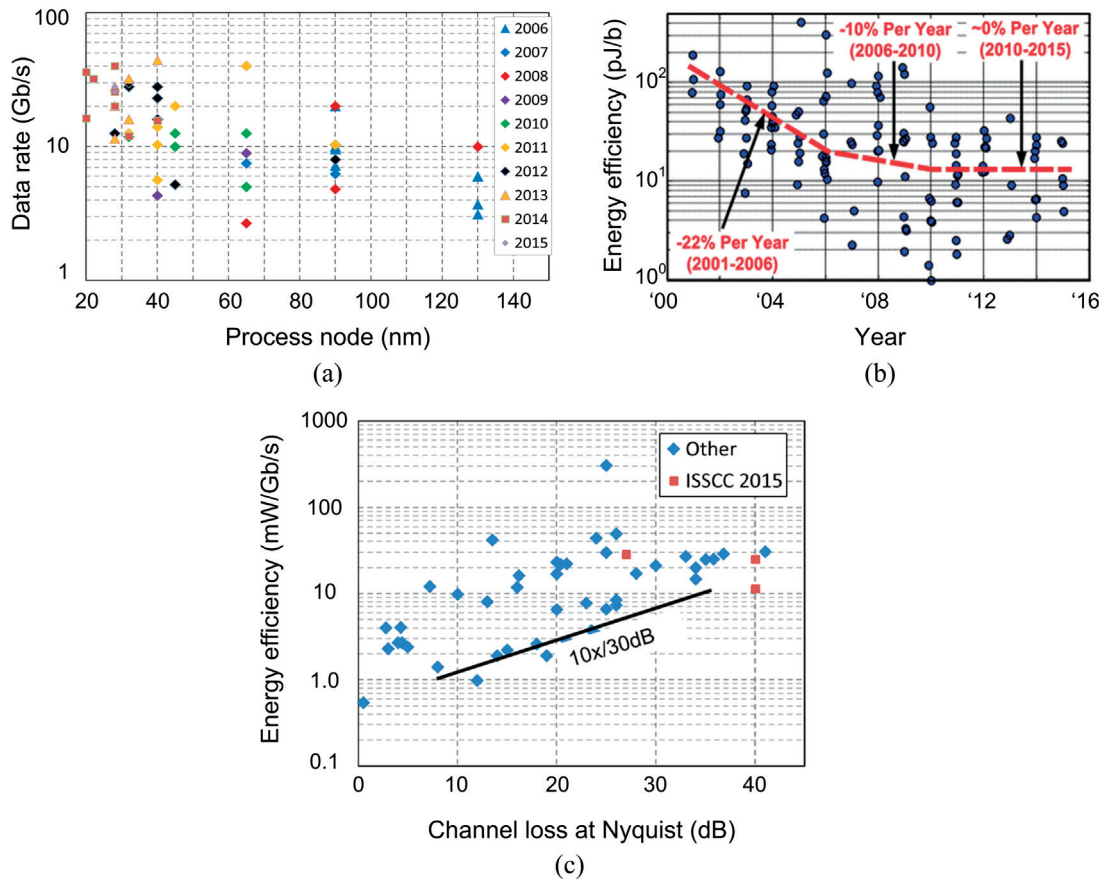
Figure 1.4: (a) Energy efficiency versus publication year [5]. (b) Data rate versus technology node [6]. (c) Energy eficiency versus channel loss [6].

transceiver and module vendors, connector vendors, and system houses so all parties can design their portion ahead of time, which is critical as most of the system and transceiver
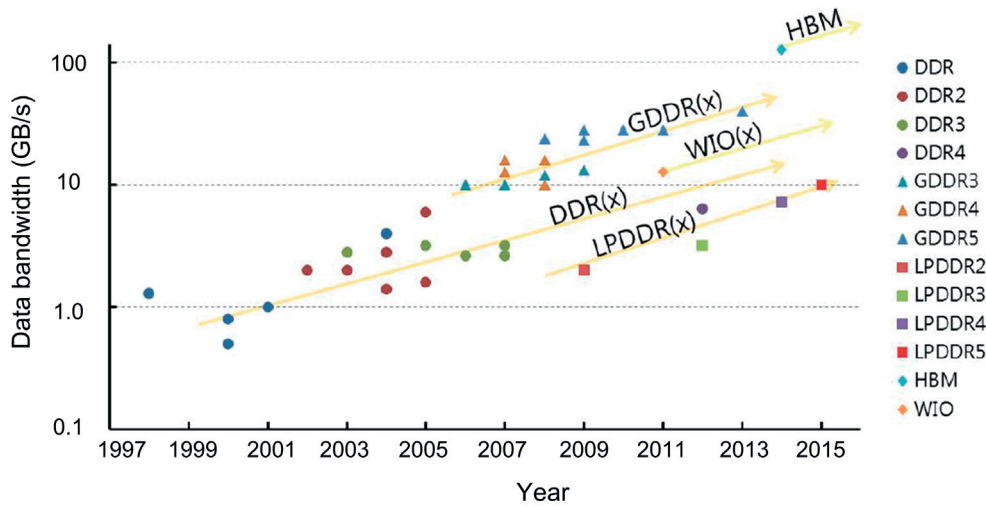
Figure 1.5: DRAM Data Bandwidth Trends [6].

development takes months or even years [4]. In this paradigm, the I/O performance becomes a major specification in practically any high-performance electronic system, from consumer products to enterprise servers. Any future progress in integrated circuit computational capability must naturally be matched with progress on I/O performance. As a result, in recent years there have been many researches for improving the I/O performance, and they have led to tremendous progress in the data rates communicated over different wireline links. Indeed, over the past decade the I/O speed improvement has been fueled by advanced CMOS technology scaling. Fig. 1.4 (a) highlights the important role technology scaling plays in supporting this trend, which has been reported over the past decade at the annual International Solid-State Circuits Conference (ISSCC) [6]. Recently, a 40/50/100 Gb/s Ethernet transceiver has been published in [18]. However, the higher data rate is not the only I/O characteristic that matters in IoT era, and the energy-efficiency should be also properly considered while the industry scales up the data bandwidth.

Power consumption for I/O circuits has been a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os has increased on a die, so has the percentage of total power that they consume. Over the past decade, voltage and process scaling have been the key contributors in improving I/O energy efficiency, and providing higher per-lane data rate. The ratio of I/O power consumption to data rate has become a popular figure of merit in evaluating an I/O performance. The power efficiency ratio is expressed in mW/Gb/s, or equivalently pJ/bit. It is plotted in Fig. 1.4 (b) for recent publications [5]. Moreover, the impact of interconnect channel loss has a great impact on the energy efficiency since advanced equalization techniques become

inevitable for proper link operation. Simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Fig. 1.4 (c) plots the energy efficiency as a function of channel loss for recently reported transceivers. Looking at the provided data in Fig. 1.4 (c), the scaling factor between link power and channel loss[1] is about unity, and shows ten times increase in power consumption for a 30 dB channel loss increase. Therefore, as the uncompensated part of the channel bandwidth is employed for the higher data rate communication, more sophisticated equalization circuits are required, hence, leveraging both power dissipation and occupied silicon die area. Moreover, since the supply voltage does not scale with transistor size in finer CMOS technology nodes, the I/O energy-efficiency improvement has been undermined in recent years, as shown in Fig. 1.4 (b).

Furthermore, from the vantage point of storage devices, the ever increasing data traffic necessitates a great progresses in computer memory business. Such a progress is only possible by constant improvements in area, power and performance of volatile and non-volatile memories. In order to reduce the bandwidth gap between main memory and processor performance, DRAM data-rates continue to increase at the memory interface, and various standards such as double-data rate (DDR), low-power DDR (LPDDR) and graphics DDR (GDDR) have been developed. Fig. 1.5 plots the data rate for different memory application published in ISSCC in recent years [6]. Currently, DDR4 and GDDR5 memory I/Os operate around 3 Gb/s/pin and 7 Gb/s/pin, respectively, which represent aggregate rates of 6 GB/s and 28 GB/s, respectively. Likewise, a 9 Gb/s/pin for GDDR5 application is recently reported in [19]. Nevertheless, the channel impairment in memory interfaces has always been a bottleneck in computing system throughput improvement. Such a limiting factor has been the major reason for introducing new DDR and GDDR standards to avoid the channel impairments, however, employing a point-to-point interface instead of a multi-drop channel creates higher cost and restricts the system storage capacity.

1.1 Thesis Goal

Generally speaking, in the wireline communication it has been known that the channel capacity, which Shannon theory predicts for wireline interfaces, has an order of magnitude (in some cases two order of magnitudes) gap from what contemporary baseband transceivers (TRXs) can practically achieve [20]. In order to bridge this gap, one should reappraise the traditional wireline techniques, both on system and circuit levels, and employ a more efficient system-level architecture, which is indeed realizable within a

---

[1]Channel loss represents the channel attenuation at Nyquist frequency, i.e., half of the transmitted bit rate. More explanation is provided in Chapter 3 of this thesis.

<div align="center">(a)   (b)</div>

<div align="center">(c)</div>
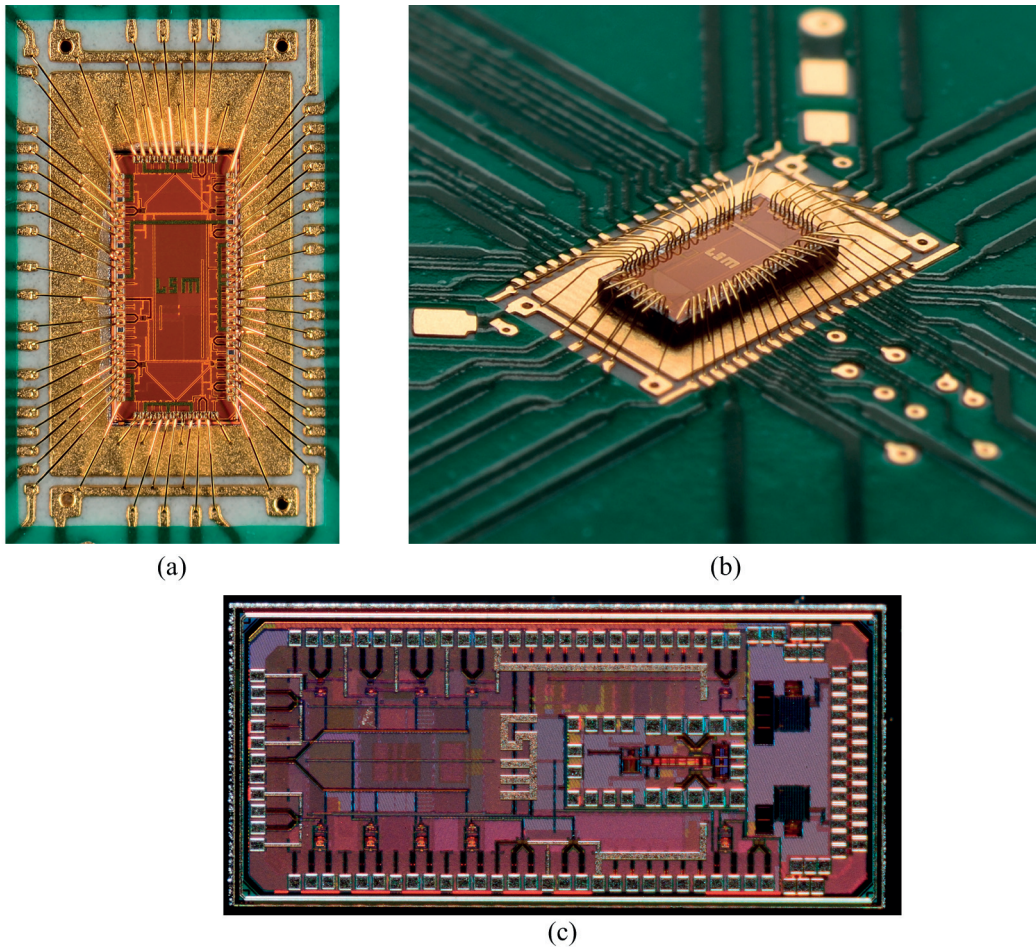
Figure 1.6: (a) 7.5 Gb/s NRZ/multi-tone transceiver first prototype. (b) The COB used for testing the first prototype. (c) The 36 Gb/s NRZ/multi-tone second prototype.

reasonable die area, circuit complexity, and power budget.

Therefore, the goal of this research is to develop a new family of wireline TRXs that can operate at high-speed and low-power over the communication channels, for which the conventional baseband TRX cannot provide a power-efficient solution. The fundamental challenge is to cope with severe channel impairments while meeting at the same time the stringent speed and power requirements. Moreover, the proposed coding scheme and system architecture should be optimize so as to the required circuit specifications become feasible on silicon without compromising the signaling scheme advantages. Fig. 1.6 shows the die photos of two prototype serial data TRXs, along with a chip-on-board (COB) package used for measurement purposes, which has been fabricated in the frame of this work. The first prototype includes a hybrid NRZ/multi-tone TRX that can efficiently communicate over a multi-drop memory channel at 7.5 Gb/s. The second prototype

incorporates the hybrid NRZ/multi-tone core in order to deliver an aggregate 36 Gb/s data rate over four differential lanes, while the power efficiency number remains at 1pJ/b for both prototypes. The prototypes have been implemented in 40 nm bulk CMOS and COB packaging has been used for testing purposes.

1.2 Organization and Content of the Thesis

Chapter Two

In Chapter 2, we have provided a brief review of state-of-the-art contemporary baseband link systems in order to highlight the today's advanced SerDes trends and study some previously published researches, which have applied multi-tone signaling for wireline communication. Then, a preliminary for our proposed signaling scheme is presented. Moreover, system-level modeling and analysis of the proposed hybrid NRZ/multi-tone scheme is presented. The goal of this MATLAB-level modeling and simulation is to evaluate the proposed system performance in presents of different noise sources, and optimize it appropriately. Having modeled the system in MATLAB, the building block specifications that is required to have an error-free link operation is extracted in this chapter.

Chapter Three

In Chapter 3 we present a new signaling scheme, called hybrid NRZ/multi-tone (MT), which can shape the transmitted spectrum of the transmitter (TX) and be customized to the characteristics of the channel, thus, it provides a power efficient solution. Based on the proposed method, the design and implementation of a 7.5 Gb/s TRX for communicating over a multi-drop memory interface is explained in this chapter. The silicon measurement of the aforementioned TRX has been presented at the end of this chapter.

Chapter Four

Chapter 4 presents the design and analysis of the clocking unit, which has been employed in our hybrid NRZ/multi-tone TRX, in details. The measurement result of the clock unit, which is realized on silicon as an independent block from our TRX, is provided in this chapter.

Chapter Five

This Chapter studies the properties of multi-tone signaling for controlling the effect of crosstalk in high-density and compact links constructed using low-cost material such as FR-4. The crosstalk reduction property of the NRZ/multi-tone signaling has been

described in this chapter, and a new TRX has been designed that can communicate at an aggregate 36 Gb/s over a four lane memory channel. Moreover, the inter-symbol interference reduction property of the proposed signaling method has been explained in details, which can be useful for very lossy backplane interfaces.

Chapter Six

In the final chapter the achievements and the main contribution of this research has been summarized and the future works has been described.

Apendix A

Appendix A explains the theoretical background for statistical eye diagram evaluation in details. Such an link estimation method has been employed in Chapter 2 for MATLAB simulations, and can provide great advantage over time-domain simulation.

Apendix B

The clock and data recovery (CDR) algorithm, and circuit design, which is suitable for the proposed hybrid NRZ/multi-tone system in Chapter 3 and Chapter 5, is suggested in Appendix B.

2 State-of-the-Art Link Systems and Preliminaries

Over the past decade, widespread adoption of data-intensive applications such as video streaming and cloud-based computing, which has furnished the Internet of Things (IoT) era, has led to an explosive demand for data bandwidth. In order to satisfy this demand, the input/output (I/O) speed of communication systems such as routers and backplane-based servers should grow accordingly. Recent studies indicate that the I/O bandwidth of link systems must increase by 2-3 times every two years [21] so as to cope with the ever-increasing bandwidth requirement of IT systems. Moreover, to manage such drastic bandwidths with reasonable power dissipation, a power efficiency of around 1 pJ/b has been a long-held goal [22].

While the process technology scaling continues to improve on-chip circuit bandwidth, off-chip interconnect remains the bandwidth bottleneck. As the channel loss increases, the link power efficiency degrades due to the need for complex equalization, larger transmit swing, and low-jitter clock requirements. Additionally, I/O power (and consequently total system power dissipation) will grow if bandwidth demand is not accompanied by a proportional I/O power efficiency scaling [23]. In this paradigm, the majority of link systems traditionally employ a simple baseband signaling (e.g., NRZ, PAM-4, and duobinary) with limited feed-forward and feed-back equalization schemes to compensate for the dispersive nature of the communication channel. A study of the baseband signaling in wireline communication systems shows that the channel capacity predicted by Shannon theory has a large gap (one to two order of magnitudes) from what can be offered by contemporary baseband transceivers [20]. From communication system perspective, the coding schemes and multi-tone signaling are the key points to bridge the aforementioned gap [20, 11, 24, 25, 26].

In this chapter, firstly, we have provided a brief review of state-of-the-art contemporary baseband link systems. Then, the recent researches for employing multi-tone signaling
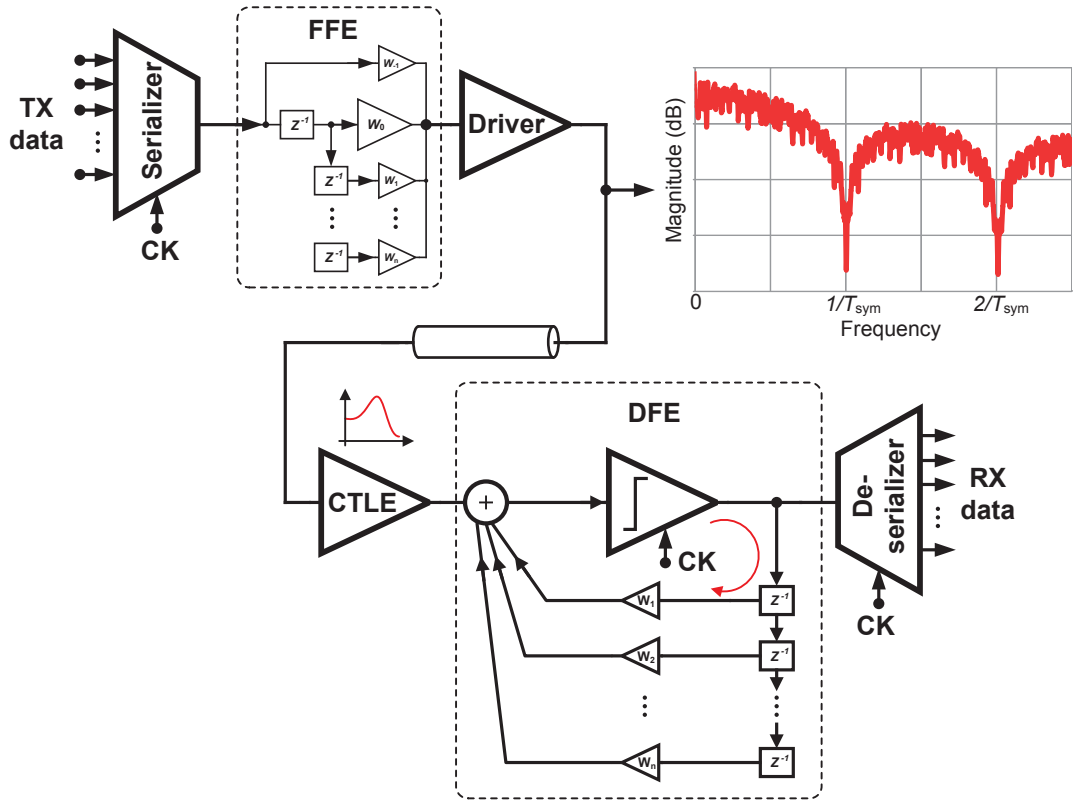
Figure 2.1: A conventional state-of-the-art baseband transceiver with a FFE equalizer at the transmitter, and a CTLE and a DFE at the receiver.

in wireline transceivers has been reviewed, and a preliminary for our proposed signaling scheme is presented.

2.1   Contemporary Baseband Link Systems

Fig. 2.1 presents the architecture of a baseband wireline transceiver, which is employed in the majority of state-of-the-art system links. This link uses non-return to zero (NRZ)[1] signaling with a Feed-Forward Equalizer (FFE) at the transmitter (TX) to cancel pre-cursor Inter-Symbol Interference (ISI), a Continuous-Time Linear Equalizer (CTLE) at the receiver front-end to increase sensitivity and compensate for the high-frequency loss of the channel, and a Decision Feedback Equalizer (DFE) at the receiver to cancel post-cursor ISIs. In this architecture, the FFE and DFE do not require an addition analog to digital converter (ADC), which can be very power hungry at high-sampling rates. Moreover, having a limited number of voltage levels at the TX, the linearity requirements of the

---

[1]Generally speaking, it can be duobinary, ENRZ, or PAM-N signaling. The sub-blocks might have different architectures, depending on the type of baseband signaling.
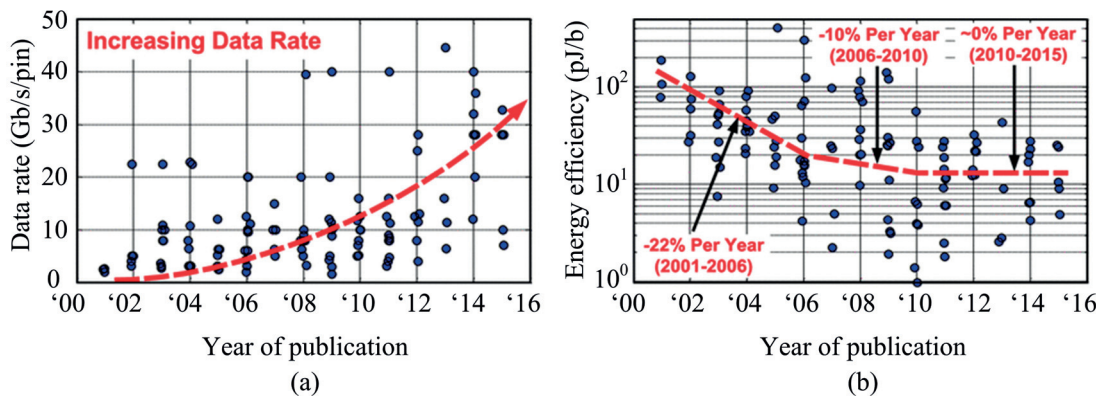
Figure 2.2: Serial link trend for the last 15 years. (a) Data rate versus year of publication. (b) Energy-per-bit versus year of publication.

output driver of TX and the input CTLE at the RX can be kept at a reasonable level so as to avoid power hungry topologies. Furthermore, error correction and detection coding is generally avoided in high-speed link design because of considerable power consumption and data latency that it can add to the system. From the frequency spectrum perspective, the transmitted output spectrum for all types of baseband transceiver (e.g., NRZ, PAM-4, ENRZ, doubinary, etc.) has a *sinc-shaped*[2] spectrum, as shown in the inset of Fig. 2.1, and it bears the first frequency null at $f = 1/T_{\text{sym}}$, where T_{sym} is the symbol period of the transmitted data. Indeed, T_{sym} depends on the bit rate and the adopted baseband modulation scheme. For example, for a simple NRZ signaling $T_{\text{sym}} = 1/T_{\text{b}}$, where T_{b} is the bit period, for duobinary, and PAM-4 modulations $T_{\text{sym}} = 0.5/T_{\text{b}}$. It can be shown that 90% of the TX energy spectrum is located below the first frequency null, whereas 77% of which is located below Nyquist rate, i.e., $f = 0.5/T_{\text{sym}}$.

Having the architecture of Fig. 2.1, the first challenge for baseband TRX in the IoT era is that the higher bandwidth requires increased signaling rate, thus, the data should be transmitted over lossy frequency regions of the communication channel. As a result, the baseband (BB) transceiver not only needs to have wider bandwidth but it should also satisfy a more challenging sensitivity requirement. Moreover, jitter becomes more important in lossy channels [27] necessitating a more sophisticated clock data recovery (CDR) circuit. These requirements push on both ends of the gain-bandwidth trade-off for circuits, which only scales linearly (to the first order) with technology scaling. A study of serial link specifications shows that although process technology scaling improves energy-per-bit efficiency, this measure has started to taper off in recent years [5]. Fig. 2.2 (a), and (b) present the per-pin data-rate and the energy-per-bit metric trends[3], respectively [5].

---

[2]$Sinc(x) = sin(\pi x)/(\pi x)$

[3]The SerDes data is collected from papers published in ISSCC, VLSI symposium, CICC, ESSCIRC, and A-SSCC [5].

This can be explained, to the first order, as a consequence of supply voltage scaling saturation in finer CMOS technology nodes.

Another issue for the conventional BB transceiver in high-loss channels is the required complicated equalization schemes in order to reach the target bandwidth. Therefore, in addition to CTLE in such channels, it is also necessary to use a DFE in order to properly compensate the frequency-dependent channel-loss [27]. The DFE has to subtract a weighted sum of the received symbols from the incoming signal. In particular, to close the feedback loop for the first tap (as shown in Fig. 2.1), the entire operation of detecting the current symbol, multiplying it with the appropriate weight, and subtracting it from the incoming symbol should be performed in less than one symbol period. Having higher symbol-rate reduces the safe margin for closing this feedback loop, and increases the required circuit complexity. Although there have been several system and circuit techniques (e.g., loop-unrolling [28], half-rate/quarter-rate DFE [29], and charge-steering topology [29, 30]) to alleviate this problem, it still remains as one of the major concerns in DFE design for today's advanced CMOS technology. It is constructive to have a brief review of state-of-the-art DFE topology in order to better understand the design challenges arising in today's IoT and high-performance computing (HPC) era.

2.1.1   State-of-the-art DFE Architecture

Unlike a linear equalizer (e.g., CTLE and FFE), a DFE is able to compensate for ISI without amplifying noise or crosstalk, and it is non-linear in nature. A DFE is also more effective than linear equalizers in dealing with reflections from impedance discontinuities, provided that the post-cursor ISI due to reflections falls within the time span of the DFE, i.e., the bit period multiplied by the number of DFE taps[4]. A key challenge in designing a high-speed DFE is ensuring that the feedback signals are accurately established at the slicer input by the time the data decision is made. The critical path, marked with a red line in Fig. 2.1, is the feedback loop, whose delay must be lower than 1 UI. Meeting this timing constraint becomes difficult at data rates above 20 Gb/s [31]. The timing constraint on this feedback path can be relaxed by adopting a technique known as speculation or loop-unrolling [32, 33]. Fig. 2.3(a) presents the block diagram of a half-rate DFE employing one tap of speculation. In this half-rate 5-tap DFE architecture, the previous bit decisions are weighted, fed back, and summed with the input signal such that post-cursor ISI is removed from the received data. The DFE employs a 1-tap loop-unrolled (or speculative) architecture and requires parallel paths in each half of the DFE [7].

---

[4]This means that if the channel shows long-tail pulse response, more DFE taps is required to cancel the post-cursor, hence, the circuit complexity and power dissipation increase proportionally.
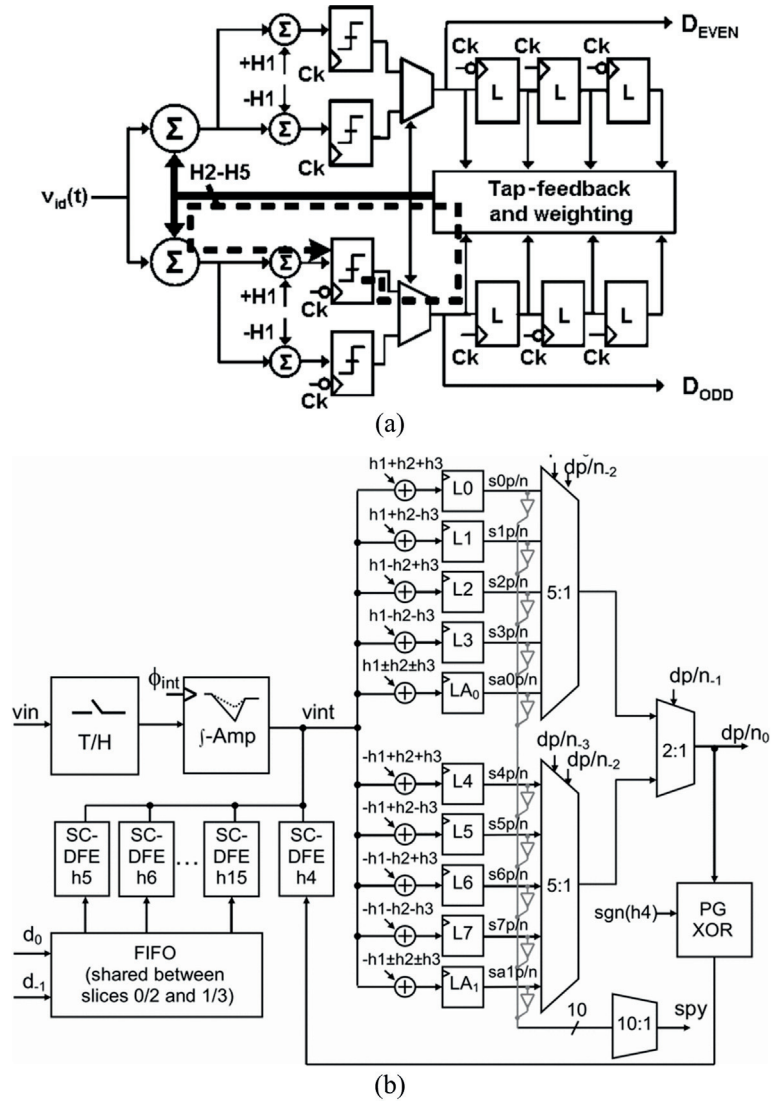
Figure 2.3: (a) A half-rate DFE architecture with speculative first (H1) tap, here the dashed red line shows a new critical timing path [7]. (b) DFE+Demux slice presented in [8].

Employing this architecture, the timing constrain for the first tap is relaxed, however, the second feedback lop becomes the critical path, whose delay must be lower than 2 bit period [or 2 unit intervals (UI)]. Therefore, it can be challenging to meet its time constrain for higher bandwidth. Although other DFE taps may be speculated to achieve higher speed operation, the additional circuitry creates significant cost in the hardware, as the number of parallel slicing paths grows exponentially (2^S) with the number (S) of speculative taps. The largest number of speculative taps reported to date is three [see Fig. 2.3(b)], which was used in implementing a 30-Gb/s 15-tap DFE, and it has 0.1 mW/Gb/tap power efficiency [8].
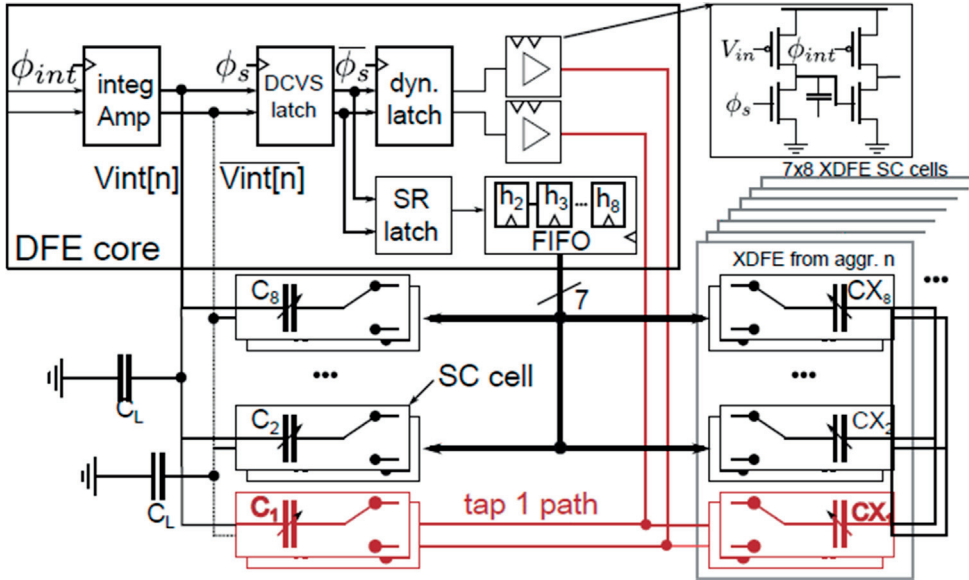
Figure 2.4: 8-lane single-ended RX architecture with XDFE and cross CTLE reported in [9].

The DFE concept can be equally applied to high-dense parallel I/Os to cancel the crosstalk noise in the same way that it removes the ISI. In [9] the cross DFE (XDFE) has been introduced in order to cancel the crosstalk in an 8-lane single-ended parallel I/O as shown in Fig. 2.4. In this work 7×8 XDFE taps have been used for each lane, and they operate with the main 8-tap DFE block, resulting in 64-tap DFE per lane. A first-in first-out (FIFO) data from 7 aggressor lanes drives 56 XDFE taps. Providing a 7 Gb/s/pin in a closely-spaced 8-lane single-ended interface, the RX consumes 5.9 mW/Gb/s, whereas around 4.4 mW/Gb/s of which is used in DFE and XDFE circuits.

Overall, employing conventional baseband signaling, energy efficiency improvements provided by CMOS technology scaling has reached a plateau in recent years since higher channel loss and shorter timing margin for critical circuits necessitate more power consumption. This has largely offset the technology scaling advantages. Bearing in mind that in high-loss and multi-drop channels the number of DFE/XDFE taps should proportionally increase with the post-cursor ISI, the energy efficiency cannot scale with higher data rates. Thereby, re-thinking about design strategies is required to not only increase the bandwidth, but also improve the energy efficiency. From communication system perspective, the coding schemes and multi-tone signaling are to further improve the energy efficiency by optimal employment of the channel capacity [20]. In the next section we provide a brief review of the researches, which have applied a coding scheme or multi-tone signaling in wireline communications.
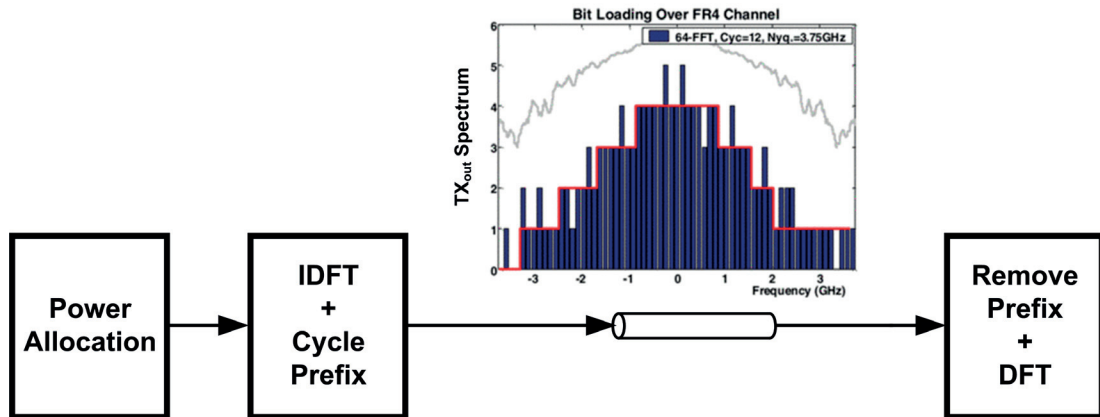
Figure 2.5: Block Diagram of the DMT system studied in [10].

2.2 Multi-Tone Link Systems

An alternative approach for wired communications is to employ multi-tone signaling, as originally performed in Digital Subscriber Line (DSL) systems and later used in wireless communication in the form of orthogonal frequency-division multiplexing (OFDM) [13]. The key advantage of this method is to communicate over a narrower frequency band, hence, less equalization circuits is required, and most of the critical transceiver building blocks (e.g., DFE, FFE, CDR) operate at lower speeds. Multi-tone signaling has promising characteristics for different type of interfaces [11, 24, 25, 26, 12, 13, 34]. However, many other aspects of the transceiver performance that are typically unimportant in binary systems become critical, and the link design requires major modifications to the well-known analysis methods applied to wireline communication systems.

The first research that well studied Multi-Tone (MT) techniques in the communication literature is [34], which has been proposed in 1975 and it was analog in nature. An analog parallel quadrature AM transmission system with overlapping orthogonal carriers and offset quadrature phase shift keying (OQPSK) was proposed in this work. Interestingly, it employs a frequency planning in which the sub-bands has 50% bandwidth overlap, and it shows that if the symbol period is an integer multiple of the sub-carrier period, it is possible to recover each sub-bands appropriately. However, the performance of the system was found to be very sensitive to communication channel variations, which changes the orthogonality between the system sub-channels. Moreover, such a modulation scheme would dictate high quadrature precision and very low phase noise so as to retain orthogonality of the sub-channels. Therefore, it would not be a power efficient and practical solution for high data rate links.

A digital implementation of a MT system has been the subject of many researches. In [35] a communication system based on frequency-division multiplexing (FDM) is presented, in which the discrete Fourier transform (DFT) are computed as part of the modulation and demodulation process. This work is known today as the OFDM or Discrete Multi-Tone (DMT) in communication systems. A more elaborated realization of digital implementation of an orthogonally multiplexed QAM (O-QAM) has been later presented in [36], where a combination of poly-phase filtering and $N/2$-point DFT processing was employed to perform the necessary filtering and mixing.

More recently, a study of the application of DMT to high-speed links has been presented in [10]. The simplified block diagram of the proposed DMT system in this work is shown in Fig. 2.5. The system-level simulation in this research, which has been performed for a sample 20" FR-4 interface, demonstrates that MT signaling has the potential for achieving high data rates in lossy channels, however, it would require high-speed DACs and ADCs with resolutions on the order of 6-7 bits, which add enormous power consumption to the link system. Moreover, this research indicates that the spectrum shaping at TX is the essence of MT approach, and having cyclic prefix in DFT/IDFT algorithm is just a clever way to simplify the implementation. The inset of Fig. 2.5 shows the TX spectrum when the optimum bit loading is adopted, and it illustrates that the TX spectrum has a different shape from conventional Sinc-shaped TX spectrum of Fig. 2.1. Therefore, if one can reduce the DMT block size (i.e., decrease the number of orthogonal carriers) while employing the spectrum shaping, then a MT architecture becomes the most efficient solution for the links in which dispersion and channel loss can be mitigated by independent number of tones.

An analog implementation of the MT link system has been studied in [11], where the insight for TX spectral shaping is leveraged and power hungry ADC and DACs are avoided. The proposed TRX architecture in this work is shown in Fig. 2.6. In this research, a 24 Gb/s transmitter employing analog multi-tone (AMT) signaling with 18 pJ/b energy efficiency is introduced. The proposed TX can be customized to the link characteristics and has the potential to achieve a superior performance compared to conventional baseband (BB) transceivers. Having identical symbol rate for all sub-channels, it has been shown that since the carrier frequencies are the integer multiples of the symbol rate, ICI can be canceled in the same way as ISI; through equalization. Moreover, in the MT architecture the equalization building blocks (e.g., DFE, XDFE, FFE, etc.) runs at sub-stream symbol rate, which is a fraction of the total system bit rate, therefore, the timing constrains are relieved. However, in this research, the receiver is not implemented on silicon, and mixing and integration was performed in MATLAB to generate the eyes.

(a)

(b)
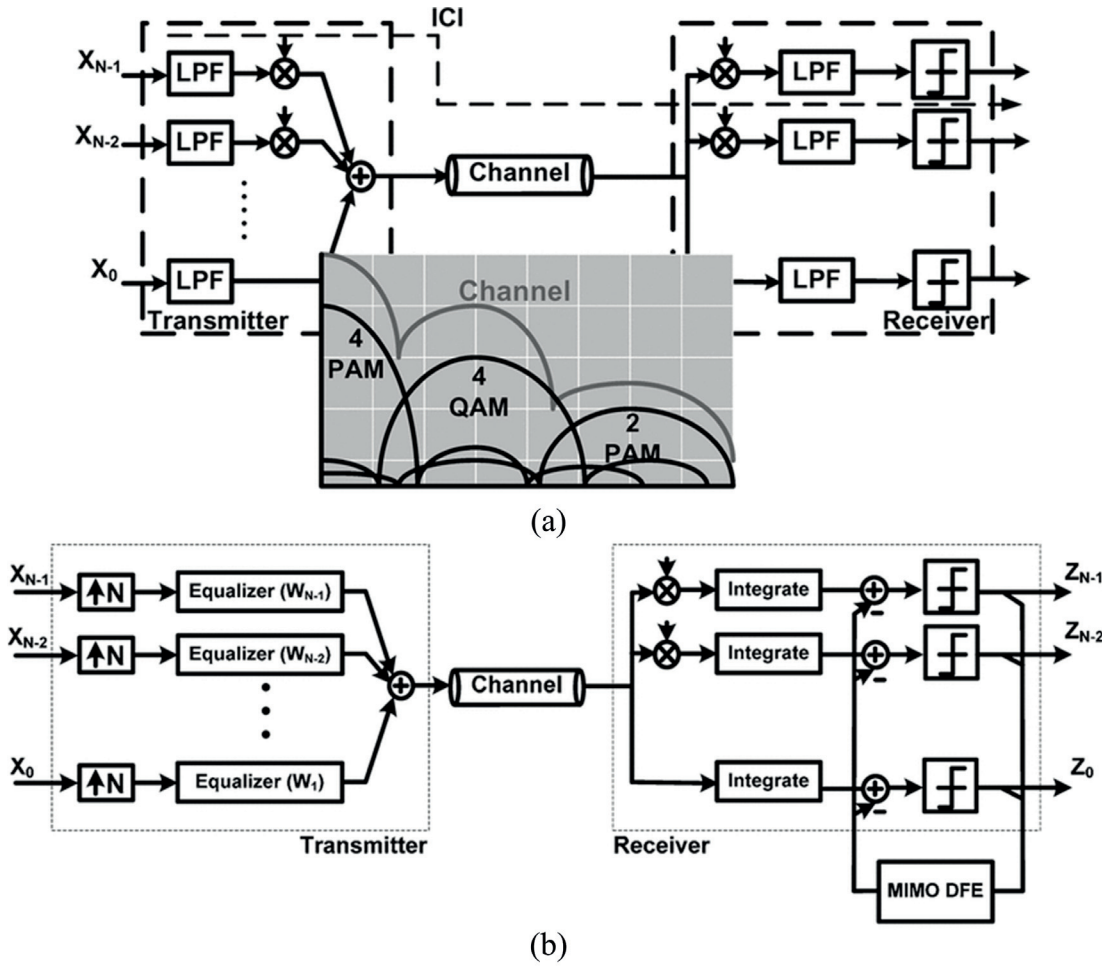
Figure 2.6: (a) Conceptual multi-tone system with low-pass filters and mixers at the transmitter and receiver to create band-limited sub-channels. (b) AMT architecture with per-sub-channel linear N-times over-sampled equalizers at the transmitter, and mixer and integrate-and-dump at the receiver [11].

A 8.4 Gb/s transceiver with 2.5 pJ/b energy efficiency for mobile memory I/Os is presented in [12]. The proposed system architecture and the employed frequency planing are shown in Fig. 2.7 (a) and (b), respectively. This work employs mixed BB signaling and amplitude shift-keying (ASK) to achieve a better performance over a FR-4 channel with 10 cm length, which has a smooth frequency response (i.e., exponentially decaying impulse response) with about 3 dB and 8 dB loss at 5 GHz and 23 GHz, respectively. Having 2.5 pJ/b efficiency over a smooth channel, the whole TRX is implemented in 65 nm CMOS. However, the link system does not demonstrate a superior performance compared to a conventional BB link system for the same channel. Furthermore, due to high carrier-frequency (23 GHz), inductors have been employed in the design for filtering purposes and reducing ICI; thereby, resulting in a bulky design, as shown in Fig. 2.7 (c).

Figure 2.7: (a) The proposed BB+RF architecture with forwarded-clock for simultaneous bidirectional signaling. (b) Dual-band signaling in frequency domain [12]. (c) TRX chip die photo.

A spectrum-shaping coding scheme is proposed in [37]. In this work, it has been shown that by repeating the transmitted pattern every M-bits, the TX spectrum is shaped and it bears an intrinsic null at $f_b/(2M)$, where f_b bit rate. Therefore, knowing the approximate location of the notch frequency, one can adapt the output spectrum to the channel frequency notches by changing the repetition frame length. Hence, the proposed spectrum shaping technique can be employed to improve the data rate of high-speed SerDes communication systems over multi-drop bus interfaces. However, the effective data rate of the link system remains at f_b/M while the whole TRX should operate at f_b data rate, which is indeed higher than the effective data rate.

A system-level analysis of a 20 Gb/s multi-tone serial link for communicating over FR-4 traces, which has 30 dB attenuation at 10 GHz, is presented in [13]. Fig. 2.8 shows a representative architecture, which composes of four sets of 5 Gb/s binary streams, each stream is modulated on a sub-carrier, f_{cj}, and the resulting four sub-channels are summed at the output. In this architecture, the sub-band spectra, shown in Fig. 2.8 (b), have little overlap to avoid the use of high quadrature precision and very low phase noise so as to retain orthogonality of the sub-channels. Moreover, to reduce the overall bandwidth a 16-QAM modulation is employed for each of the sub-streams, thereby, the effective bandwidth is reduce by a factor of four, and the equalization complexity is relieved. Table 2.1 summarizes the required TRX performance for the proposed system, which is

Figure 2.8: (a) Proposed system architecture in [13]. (b) Proposed frequency planning with aggregate data rate of 20 Gb/s.

Table 2.1: Required Transceiver Performance presented in Fig. 2.8 [13].

Transceiver	
Number of Sub-channels	4
Modulation	16-QAM
Baseband Data Rate	5 Gb/s
Phase Noise	−117 dBc/Hz @ 10-MHz offset
Transmitter	
Output Swing	1.2 Vpp (at summing node)
Pulse Shaping	Raised-Cosine Filter with roll-off factor = 0.8
I/Q Mismatches	1% Gain Imbalance
	1° Phase Imbalance
Receiver	
Noise Figure	23.5 − 43 dB
IIP3	−8 − 15.3 dBm
Gain	−1.4 − 28 dB
Equalization	13 dB Pre emphasis at maximum

evaluated by MATLAB time-domain simulation. Although the specifications are not too stringent to be realized on silicon, the use of 16-QAM modulation severely limits the RX equalized eye-opening (less than 20% horizontal eye-opening is illustrated in this work). Moreover, due to the frequency planing, which bears data at odd carrier harmonics, the ICI is mainly affected by clock harmonics. Hence, a pure sinusoidal carrier is required for upconverting the TX sub-streams, which can impose power hungry clock buffers and a complicated clock generation circuits.
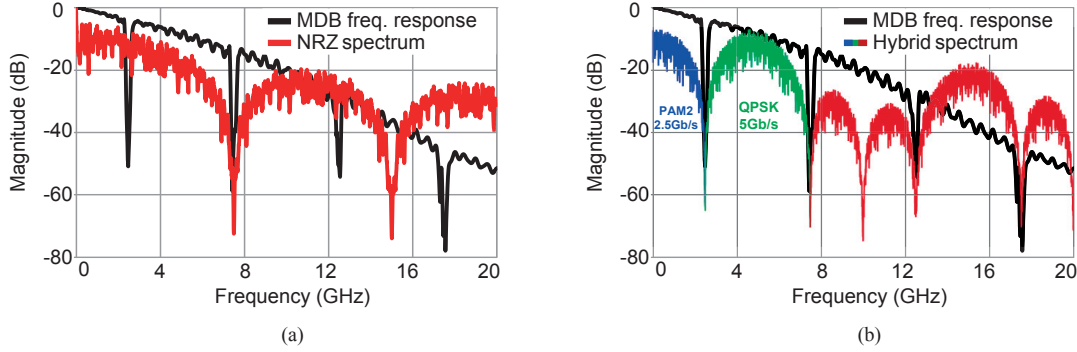
Figure 2.9: Proposed mixed NRZ/MT signaling scheme. (a) NRZ spectrum over a multi-drop channel. (b) Hybrid NRZ/MT spectrum over a multi-drop channel.

Overall, as it can be seen in the simulation and measurement results of MT systems, which are presented in this section, the major advantages of MT signaling in serial link system are twofold. Firstly, the TX spectrum can be shaped according to the channel frequency response, thus, the channel capacity can be better used for data transmission. Secondly, from the circuit realization perspective, most of the system building-blocks (e.g, MUX/DEMUX, CDR, DFE, FFE) operate at only a fraction of the total data rate; therefore, they can be realized with better power efficiency and less complexity. However, the MT transceiver closely resembles an RF communication system, facing similar sensitivity, linearity, and precision issues. Moreover, unlike typical RF systems, the broadband nature of the serial link introduces additional harmonics and interference effects that can severely impact the system performance. Therefore, in order to employ multi-tone signaling in wireline communication systems, one should consider all these requirements so as to the MT link system building-blocks can be designed efficiently, and the advantages that are made available by MT signaling will not be overturned by the tight circuit specifications. In the Chapter 3, a proposed hybrid/multi-tone system is presented, which considers all these design requirements.

2.3 Preliminaries of Hybrid NRZ/Multi-Tone System-level Design

In memory interfaces, the channel frequency response bears some notches due to impedance discontinuity and multiple reflections, as will be discussed in Chapter 3. In this paradigm, shaping the TX spectrum according to the channel frequency response can be a wise solution to improve the system performance and reduced the circuit complexity. Based on this understanding, Fig. 2.9 presents a mixed NRZ/MT spectrum, which can properly increase the power efficiency by avoiding the channel frequency notches. Here, the number of sub-bands is reduced to three, hence, the clock harmonics do not create ICI.

Likewise, a QAM modulation is adopted for the pass-band so as to avoid multi-level data transmission, which limits the horizontal eye-opening. Since the carrier frequencies are integer multiples of the sub-band symbol rate, the ICI pattern does not change from one symbol to another, and consequently, it can be canceled through appropriate time-delay between the transmitted sub-streams on TX side. The proposed system bears the most essential characteristic of the MT signaling (i.e., spectrum shaping), whereas the clock harmonics and ICI impacts on the system performance can be alleviated by proper frequency planning and time-shifting, respectively.

In the next chapter, we will describe this architecture in details, and system- and circuit-level analysis, design, and implementation of the proposed hybrid NRZ/MT transceiver will be presented.

2.4 Conclusion

In this Chapter state-of-the-art serial data transceivers are briefly reviewed, and different types of link system architecture are presented. Furthermore, the advantages and disadvantages of multi-tone signaling in wireline paradigm are reviewed, and based on the wired communication requirements, a preliminary hybrid NRZ/multi-tone signaling method is introduced. The proposed system has the spectrum shaping property, whereas the adverse multi-tone effects (e.g., ICI and clock harmonics) can be reduced by proper frequency planning.

3 Hybrid NRZ/Multi-Tone Signaling

In this chapter we propose a new signaling scheme, called hybrid NRZ/multi-tone (MT), which can shape the transmitted spectrum of the transmitter (TX) and be customized to the characteristics of the channel, thus, it provides a power efficient solution. The proposed system consists of three wide-band sub-channels, and employs source-synchronous clocking architecture that facilitates the clock and data recovery on the receiver (RX) side.

We start this chapter by a short overview of today's popular memory interfaces, which are widely employed by industry. Then, we describe the system level design and study of the proposed hybrid NRZ/MT architecture and compare its equalization complexity to an equivalent baseband (BB) system, for a sample memory channel. We continue the chapter by circuit design and implementation of a 7.5 Gb/s mixed NRZ/multi-tone transceiver (TRX) for multi-drop bus (MDB) memory interfaces in 40 nm bulk CMOS technology is presented. Reducing the complexity of the equalization circuitry on the receiver (RX) side, the proposed architecture achieves 1 pJ/bit link efficiency for a MDB channel with 45 dB loss at 2.5 GHz. The transmitted spectrum is composed of baseband (BB) and I / Q sub-bands with the ability to match the modulation frequency of the entire TRX with respect to the channel response over a $\pm 25\%$ range. A switched-capacitor-based mixer/filter is developed to efficiently down convert and equalize the I / Q sub-bands in the RX. The core size area is $85 \times 60~\mu m^2$ and $150 \times 60~\mu m^2$ for the TX and RX, respectively.

We will show that the proposed hybrid NRZ/MT TRX can achieve a superior performance compared to the conventional BB transceivers, especially for MDB interfaces, through better allocation of the transmit power MDB channels, which has the frequency selective characteristics.

3.1   Multi-Drop Memory Interfaces: Overview

In this section, the multi-drop memory interfaces are studied and the challenge of traditional NRZ signaling for BB transceivers over MDB channels is presented and analyzed.

3.1.1   Multi-Drop Channel Characteristics

Advancement in CMOS technology have enabled exponential growth of computational power over three decades. However, data processing efficiency also relies on sufficient data communication bandwidth between different units of a computing system. For a modern memory system, higher memory capacity, faster memory access and price are the major constraints.

From the memory interface design perspective, achieving these goals requires the design of faster input/outputs (I/Os), which connect to a larger number of memory modules and cost the same or less. To provide higher capacity, either the number of I/O pins should be increased, or the data rate on each I/O pin should be improved. The former solution involves more cost since the chip pin count increases and the routing congestion on the printed circuit board (PCB) grows rapidly. The latter approach has been the industry trend for many years. For example, double-data rate second generation (DDR2) provides the data rates from 400 Mb/s/pin to 1066 Mb/s/pin, while for the third generation DDR (DDR3), the data rates from 800 Mb/s/pin to 1866 Mb/s/pin are available [38, 39]. However, as the speed increases, the communication bandwidth of the PCB traces limits the access speed on each pin. For example, advanced DDR3 memory interfaces can operate at 1.866 Gb/s/pin while for modern graphics DDR (GDDR5) the figure is 10 Gb/s/pin, since it employs a point-to-point memory interface that provides a smooth frequency response [6]. Such a considerable difference reflects the major effect of the channel frequency response at maximum speed that a link can reach within a reasonable power budget.

Memory systems typically apply dual in-line memory modules (DIMMs), shown in Fig. 3.1 (a), because of their high capacity and low cost. In such interfaces, there are one or more notches in the transfer function of the channel that dissipate the major part of the transmitted power and create reflections. Such frequency notches, mainly induced by impedance discontinuity and reflections, create the multi-drop bus (MDB) characteristic between controller and DRAMs. The multi-drop nature channel causes a longer delay, slower rise-and-fall time and long tail pulse response for the data rates beyond the first notch [40]. Fig. 3.1 (b) shows the simplified block diagram of the 3-DIMM
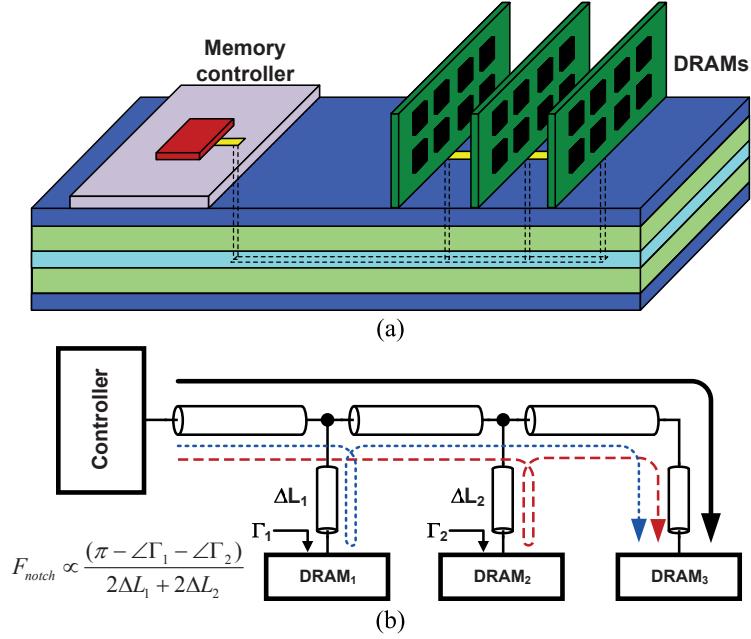
Figure 3.1: (a) Controller to DRAM MDB interface. (b) Simplified block diagram of interface in Fig. 3.1 (a) showing the multi-path fading.

memory interface in Fig. 3.1 (a), with three possible paths for the controller-DRAM$_3$ communication. While the memory controller is communicating with one DRAM module, the other modules are idle and can be partially terminated or non-terminated based on the standard [40]. Hence, in this situation they produce the reflection coefficient of Γ_1 and Γ_2 due to their imperfect termination. The electrical length-differences in these paths and the phase shift, caused by Γ_i, lead to multi-path reflections. These reflections can cause destructive superposition at certain frequencies and produce notches in channel frequency response. Based on this explanation and the block diagram of Fig. 3.1 (b), the first notch in the frequency response of the 3-DIMM memory interface of Fig. 3.1 (a) can be calculated as

$$F_{\text{notch}} = \frac{c}{2\pi} \times \frac{\pi - \angle\Gamma_1 - \angle\Gamma_2}{\Delta L_1 + \Delta L_2} \tag{3.1}$$

where c is the effective speed of light in PCB traces, Γ_1 and Γ_2 are the reflection coefficients of the idle DIMM$_1$ and DIMM$_2$, respectively, and ΔL_1 and ΔL_2 are the physical path difference between direct and reflected paths to DIMM$_1$ and DIMM$_2$, respectively.

A typical MDB memory channel has frequency notches at a nominal F_{notch} and all its odd multiplications due to frequent reflections [41]. To study MDB channel properties, a

(a)   (b)
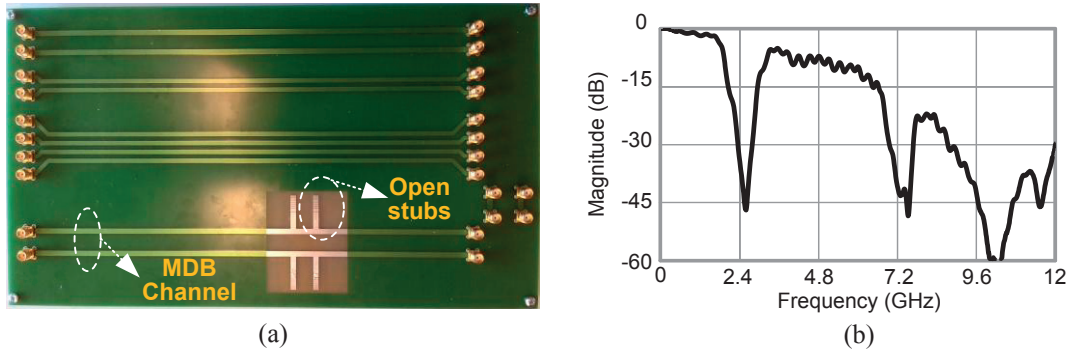
Figure 3.2: (a) The fabricated MDB channel. (b) The frequency response of a sample MDB showing first notch at 2.5 GHz.

sample multi-drop channel is designed and fabricated on FR-4 material that can mimics the behavior of a real MDB interface, which has two DIMMs per channel. The DIMMs are modeled by introducing two open-stubs that create the length difference between the direct and the reflected signals, similar to what is shown in Fig. 3.1 (b). Fig. 3.2 (a) shows the fabricated sample channel that is implemented as a differential wireline interface. The measured reference MDB channel demonstrates the frequency notches around the nominal value of $(2k - 1) \times 2.5$ GHz, $k \in \{1, 2...\}$, as shown in Fig. 3.2 (b). The resonance effect creates nulls in the frequency response of the channel, causing substantial band limiting beyond what is expected from simple RC loads. Since transmission lines have periodic characteristics in the frequency domain, the nulls approximately repeat at odd harmonics of their fundamental frequency. As (3.1) shows, the frequency of the first notch is inversely proportional to the length of the DIMM stubs. Moreover, having the adjustable stub lengths in the fabricated channel, we are able to change the notch frequencies in our sample MDB channel around 40%, as shown in Fig. 3.3. Furthermore, from the time domain point of view, having notches in the frequency response causes several reflections and, thus, long tail pulse response.

Fig. 3.3 illustrates the measurement results of the channel frequency and pulse response for different stub configurations, showing the tunability of the first notch from 600 MHz to 3.5 GHz. As Fig. 3.3 demonstrates, the pulse responses have long tail (2 ns to 4 ns), which makes the equalization process very challenging for conventional baseband TRX.

Overall, in the memory system paradigm, the multi-drop interface between memory units and the controller renders the data equalization even more complicated. This necessitates a comprehensive equalization in the receiver front-end. In addition to being power-hungry, implementing such systems is challenging in the CMOS memory processes since the DRAM technology normally offers only low-cost and simple processes with slower devices.
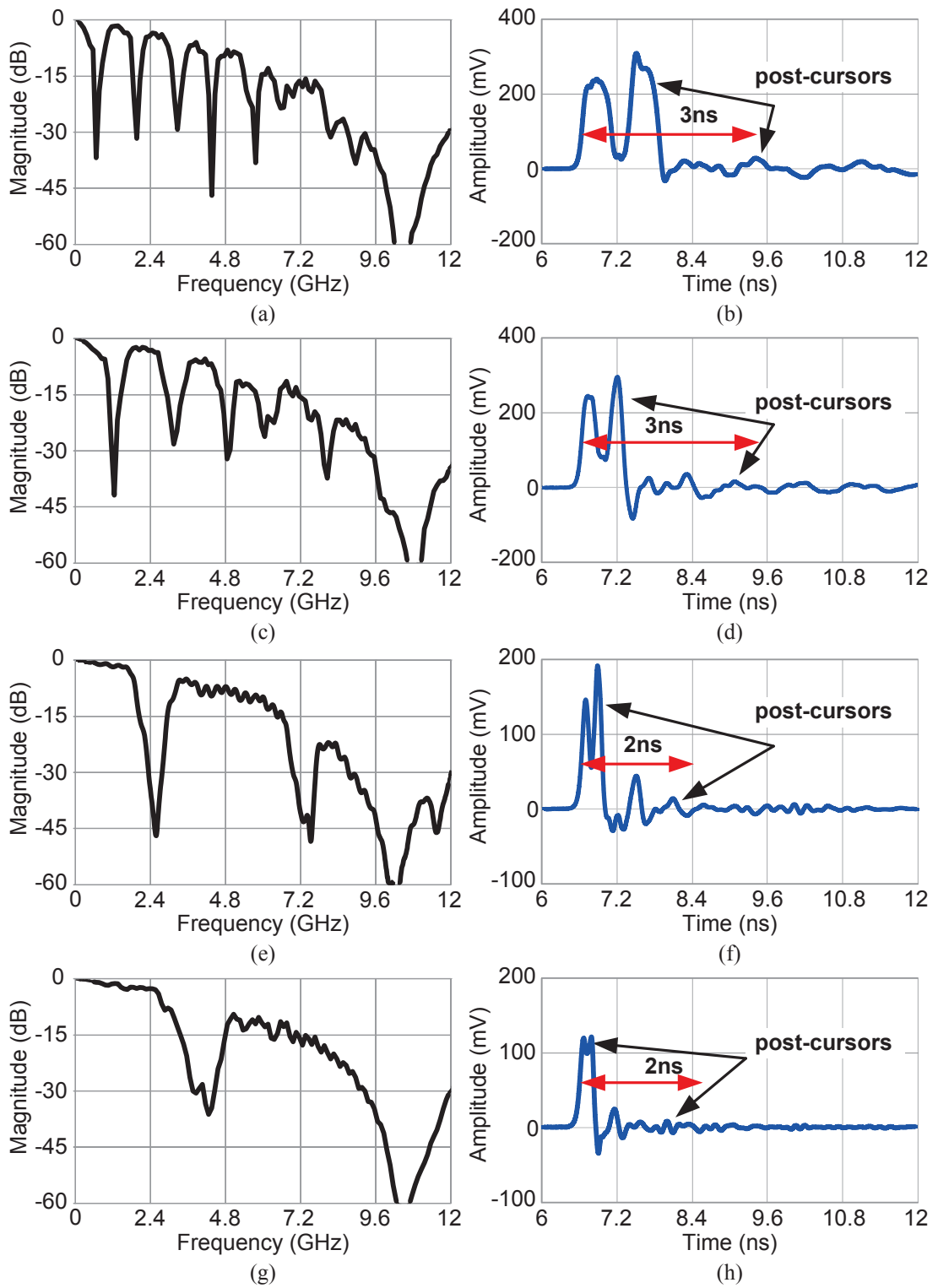
Figure 3.3: The measured frequency response and the $3 \times F_{\text{notch}}$ b/s single-bit pulse response for different stub lengths. (a) F_{notch} =660 MHz. (b) 2 GHz single-bit response. (c) F_{notch} =1.25 GHz. (d) 3.75 GHz single-bit response. (e) F_{notch} =2.5 GHz. (f) 7.5 GHz single-bit response. (g) F_{notch} =3.7 GHz. (h) 11 GHz single-bit response.
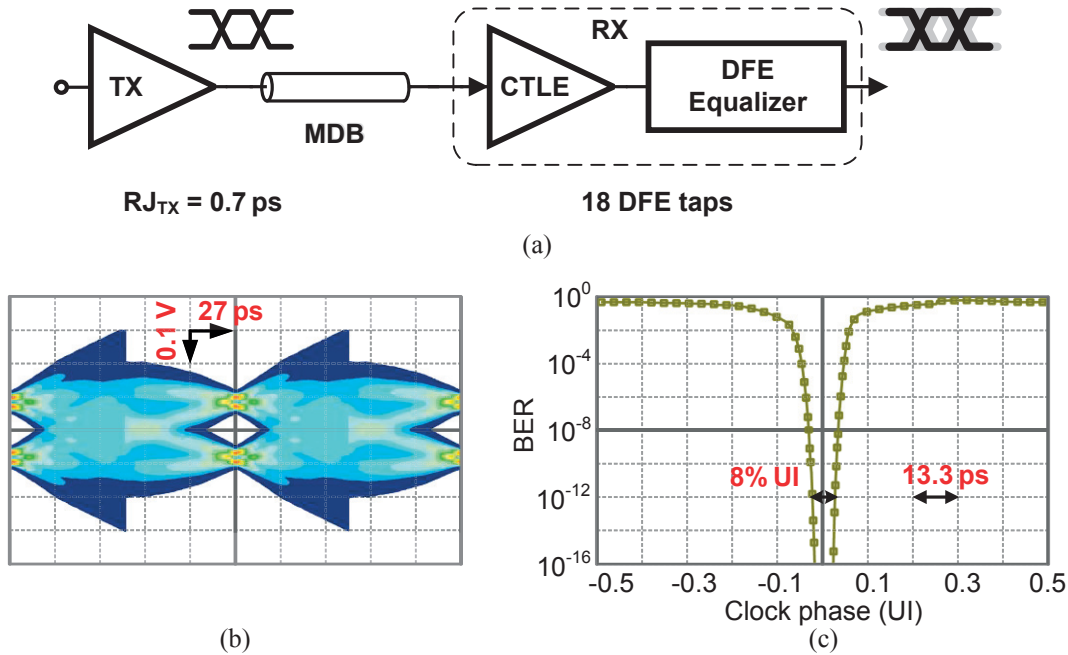
Figure 3.4: (a) Conventional BB transceiver block diagram for communicating at 7.5 Gb/s over MDB interface. System-level simulation results for the link shown in Fig. 3.2 (b). (b) Eye diagram for 7.5 Gb/s data rate, (c) bathtub curve, both after optimizing the CTLE and DFE response.

From the technology-trend point of view, to provide higher speed the maximum number of drops is reduced from eight in DDR2 to four in DDR3. However, reducing the number of drops results in fewer memory slots and reduces the memory capacity. In the next section, we show the complexity of designing a traditional baseband TRX in more detail.

3.1.2 Baseband Signaling in Multi-Drop Interfaces

To illustrate the complexity of designing a traditional BB serial data transceiver for a MDB memory interface, a conventional BB transceiver is modeled and simulated for our reference MDB channel. Fig. 3.4 (a) shows the BB transceiver used in system-level simulation. Here, the transmitter employs NRZ signaling and is assumed to have a 0.7 ps$_{rms}$ output jitter, i.e., 0.05% UI jitter. The receiver has continuous-time linear equalizer (CTLE) and decision feedback equalizer (DFE) for data equalization. Both CTLE and DFE are considered ideal blocks without random noise. The RX employs adaptive least mean squares (LMS) algorithm to find the DFE tap weights while the CTLE provides around 8 dB gain boosting at Nyquist frequency. The transceiver should communicate at 7.5 Gb/s over the reference MDB channel, which has the first notch
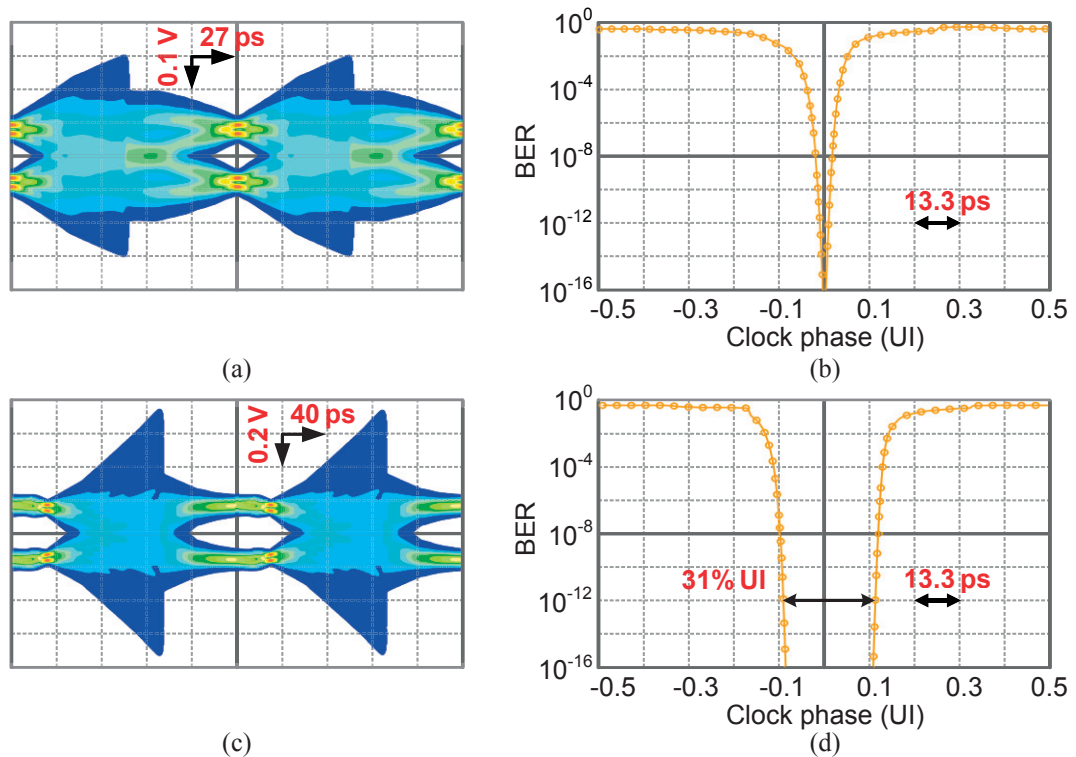
Figure 3.5: System-level simulation results for the MDB channel of Fig. 3.2 (b) having 0.5% jitter on both TX and RX. (a) Eye diagram for 7.5 Gb/s data rate, (b) bathtub curve for 7.5 Gb/s data rate, both after optimizing the CTLE and DFE response. System-level simulation results for the same interface. (c) Eye diagram for 5 Gb/s data rate, (d) bathtub curve for 5 Gb/s data rate, both after optimizing the CTLE and DFE response.

frequency at 2.5 GHz, as shown in Fig. 3.2 (b).

The statistical and bit-by-bit system-level simulation is performed to evaluate the bathtub and eye diagram, respectively, at the receiver output. The system-level simulations show that using the conventional receiver architecture of Fig. 3.4 (a), a DFE with about 18 taps is needed to equalize the effects of the notches and achieve an 8% UI eye-opening, UI = 133 ps for a 7.5 Gb/s data rate, at a bit error rate (BER) of 10^{-12}. The equalized eye diagram and the corresponding bathtub on the RX side are shown in Fig. 3.4 (b) and (b), respectively. Using an 18-tap DFE will certainly lead to significant power dissipation. Assuming 100 μW/Gb/s per tap, the consumption of the DFE block will be about 1.8 mW/Gb/s or more [27]. With such a high level of consumption and circuit complexity, however, the eye-opening would be only 10 ps at BER = 10^{-12} for 7.5 Gb/s data rate. Adding the same amount of random noise on the RX side (i.e., 0.7 ps$_{rms}$ jitter), the horizontal eye-opening for the equalized data becomes almost closed (only 1% UI eye-opening at BER = 10^{-12}), as shown in Fig. 3.5 (a) and (b).
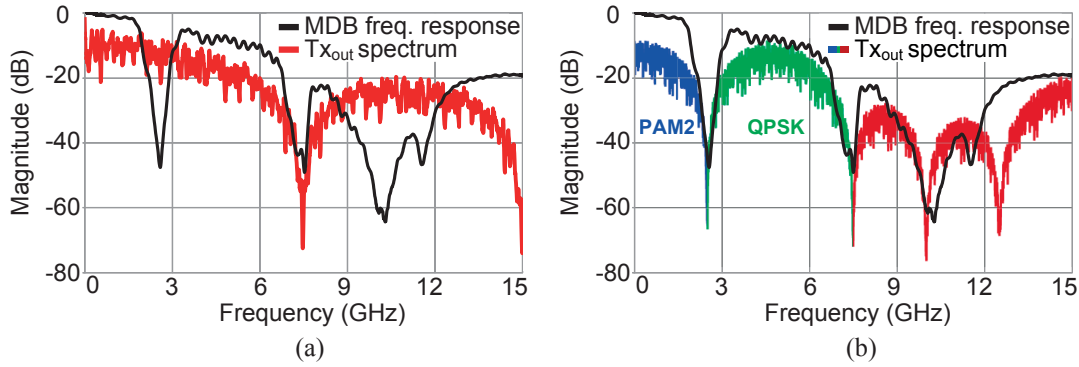
Figure 3.6: Transmitted spectrum in a MDB channel. (a) Conventional NRZ signaling. (b) Hybrid NRZ/MT signaling.

To demonstrate how important is the ratio of the notch frequency to the Nyquist rate of the data stream, the system level simulations is performed for communicating at 5 Gb/s over the same MDB interface of Fig. 3.2 (b). In this simulation, each TX and RX has a 1 ps_{rms} jitter (i.e., 0.5% UI jitter) and the simulation results for the equalized eye diagram and the corresponding bathtub are presented in Fig. 3.5 (c) and (d), respectively. These simulations show that when the Nyquist rate is well above the first notch, the equalization is very challenging, and conventional baseband techniques cannot provide an error free operation even with an ideal CTLE and many DFE taps. However, if the Nyquist rate is around the first notch the link can be well equalized employing the traditional baseband techniques. We will study this behavior from the frequency domain point of view, in the next section.

3.2   Hybrid NRZ/MT Signaling: System Design Overview

In this section, the proposed hybrid NRZ/MT transceiver for communicating over MDB interfaces is describe in details, and the proposed architecture that facilitates a practical circuit implementation is introduced.

A NRZ bit stream with a $1/T_b$ data rate bears around 90% of the transmitted bit energy below $\omega = 2\pi/T_b$, and 77% of which is below the Nyquist rate, i.e., $\omega = \pi/T_b$ [42, 43]. Therefore, employing NRZ signaling for communicating over a MDB interface, which has the first frequency notch well below the Nyquist rate of the data streams, leads to a significant energy loss around the first notch. Fig. 3.6 (a) shows the output spectrum of a NRZ transmitter over a MDB channel. The first notch wastes a significant part of the spectrum energy since it is well below the desired Nyquist frequency.

Avoiding channel frequency notches by employing a proper modulation scheme can prevent
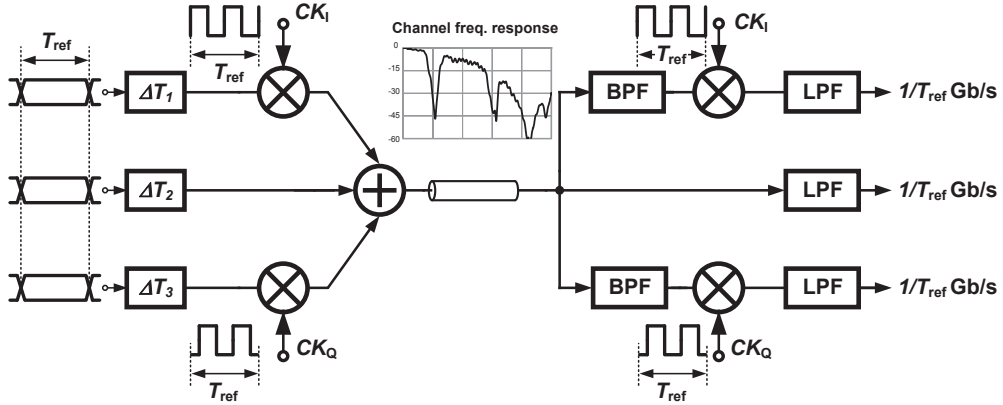
Figure 3.7: Proposed mixed NRZ/MT system architecture.

bit-energy waste around the notches, and reduces the equalization circuit complexity. However, any modulation scheme for wireline communication should be employed carefully to keep the system requirements feasible within a reasonable power budget.

Fig. 3.6 (b) illustrates the proposed NRZ/MT transmitted spectrum over a MDB channel. Here, the lower-frequency band of the channel, from DC to the first notch (i.e., 0-2.5 GHz), is used for transmitting up to 2.5 Gb/s NRZ data and constitutes the PAM2[1] part of the spectrum. Moreover, the upper-frequency band of the channel, between two notches (i.e., 2.5-7.5 GHz), is exploited for transmitting 5 Gb/s data in the quadrature-phase shift-keying (QPSK) format. This sub-band carries 2.5 Gb/s data on each of the in-phase (I) and quadrature-phase (Q) content of the spectrum.

Furthermore, dividing the total bit-stream into three sub-bands (i.e., baseband, I sub-band and Q sub-band) helps the latter to experience less channel loss. Hence, in-band intersymbol interference (ISI) is reduced and as a result the equalizing process can be more power efficient.

By employing this modulation scheme, the NRZ/MT transceiver represents an RF paradigm and the linearity and clock harmonic issue should thus be considered properly [13]. Moreover, in a multi-drop memory channel, although the channel frequency response is well characterized before designing the frequency plan, the channel frequency notches may change to some extent after fabrication due to PCB-related non-idealities. Therefore, the TRX should be able to tolerate these effects, and possibly adapt itself to the channel frequency response.

---

[1]Generally speaking, it can be any kind of PAM-N, ENRZ, or doubinary baseband signaling.
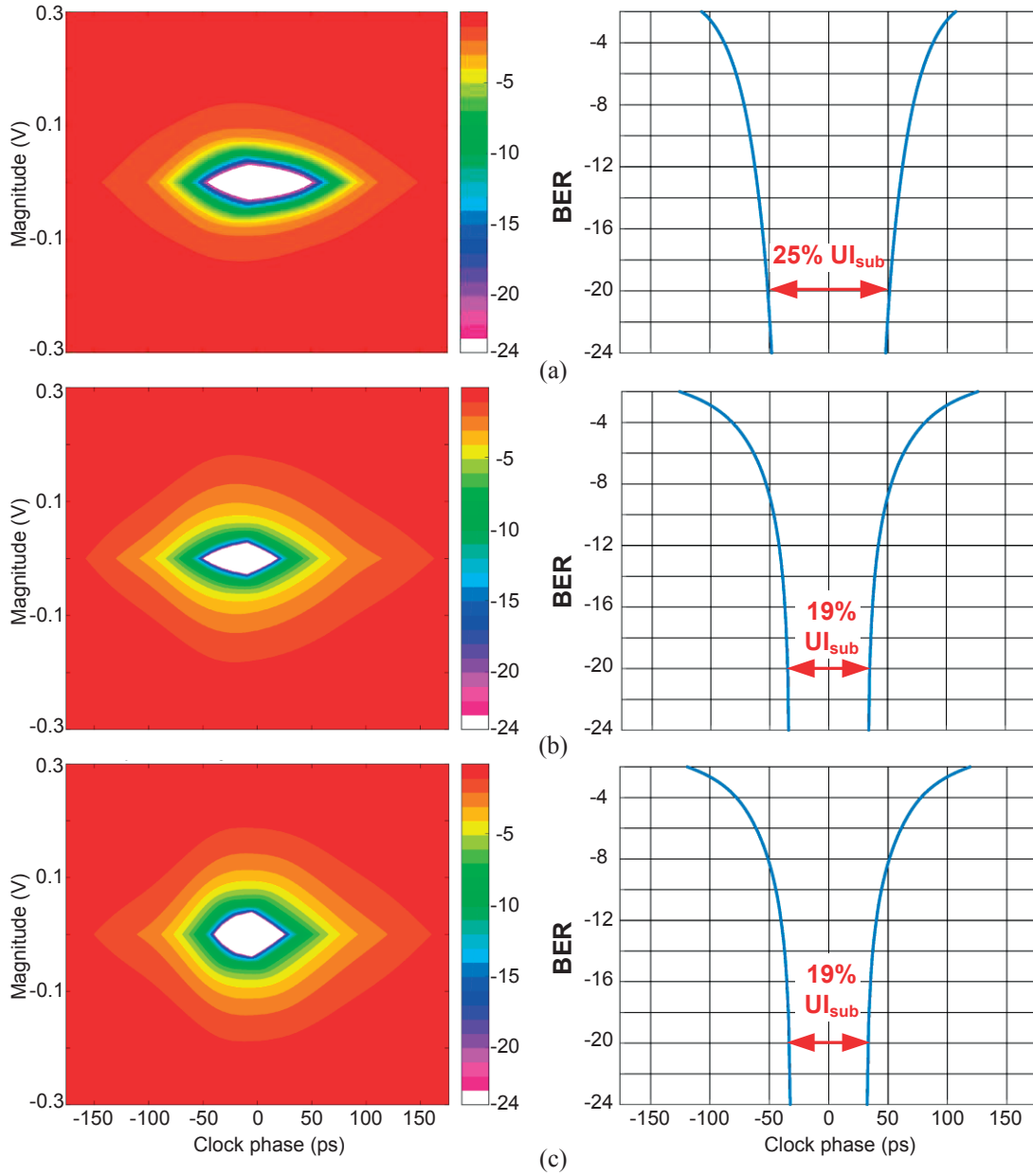
Figure 3.8: System-level statistical simulation for the proposed architecture in Fig. 2.9. (a) Baseband, (b) I sub-band, and (c) Q sub-band statistical eye diagram and corresponding bathtub.

3.2.1   Hybrid NRZ/MT TRX Statistical System-level Modeling

Based on the proposed frequency planning and signaling scheme of Fig. 3.6 (b), Fig. 3.7 illustrates a mixed NRZ/MT serial data transceiver for communicating over a memory channel, whose frequency response has multi-drop nature as shown in the inset of Fig. 3.7. Here, the number of sub-bands is reduced to three, hence, the clock harmonics do not create ICI. Therefore, square-wave clocking scheme is adopted for UP and DOWN
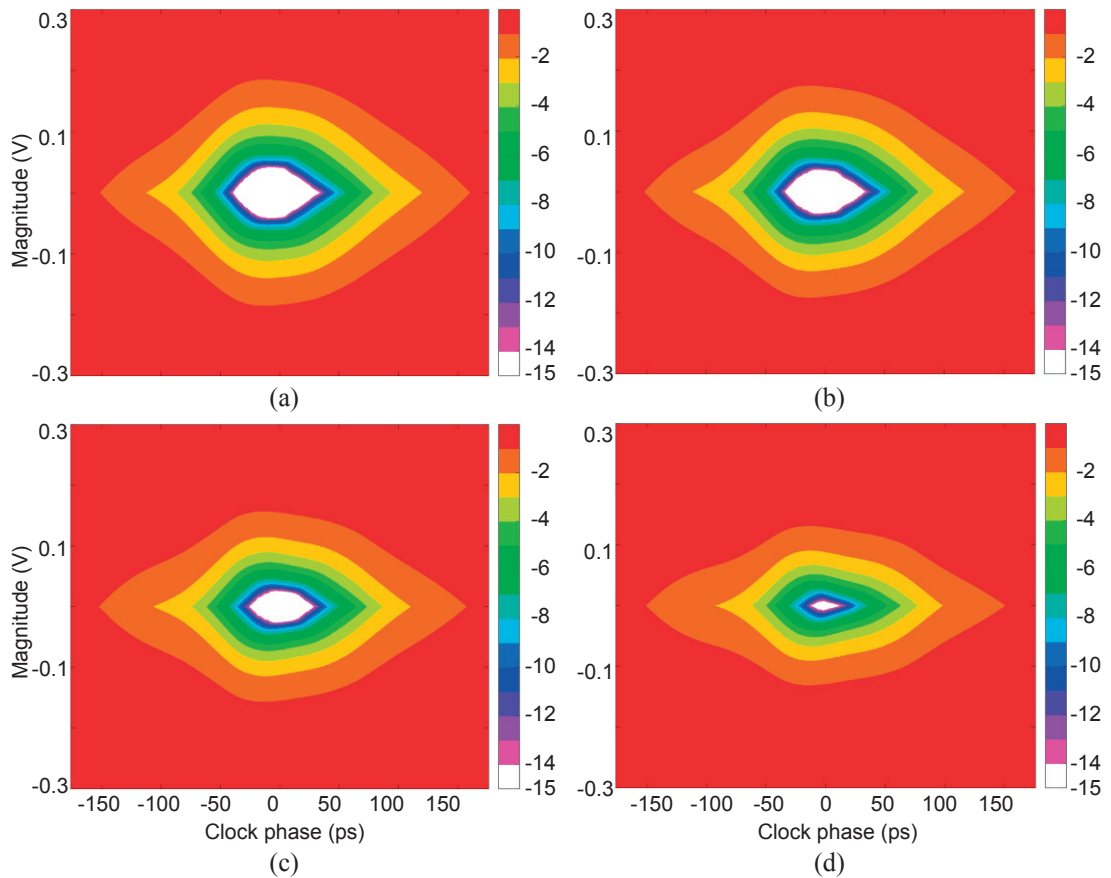
Figure 3.9: Q sub-band eye diagram for different amount of clock phase mismatch. (a) 5°, (b) 10°, (c) 15°, and (d) 20° I/Q phase mismatch.

conversion, which can relax mixer and clock generation unit requirements. Moreover, unlike [13], the baseband part of the channel, which has moderate attenuation, is employed to send a NRZ-based data stream so as to the channel notch is located beyond baseband spectrum null. Likewise, a QAM modulation is adopted for the pass-band so as to avoid multi-level data transmission, which limits the horizontal eye-opening. The only equalizer that is used in this architecture is the 2nd-order low-pass filters[2] (LPF), and a 2nd-order band-pass filter (BPF) on the RX sides, which are used to select the frequency band of interest. Since the carrier frequencies are integer multiples of the sub-band symbol rate, the ICI pattern does not change from one symbol to another, and consequently, it can be canceled through appropriate time-delay between the transmitted sub-streams on TX side, as shown in Fig. 3.7. The proposed system bears the most essential characteristic of the MT signaling (i.e., spectrum shaping), whereas the clock harmonics and ICI impacts on the system performance can be alleviated by proper frequency planning and time-shifting,

---

[2]Filers with sharp frequency-domain roll-off necessitate more in-band equalizer taps (i.e., in-band DFE and FFE), but cause less ICI, hence, require less cross-band DFE and cross-band FFE.

Table 3.1: The hybrid NRZ/MT performance presented in Fig. 3.7.

Transceiver	
Number of Sub-channels	3
Modulation	PAM-2 (BB)/ 4-QAM (PB)
Baseband Data Rate	2.5 Gb/s
Clock RMS Jitter	1% UI$_{sub}$ (4 ps)
Transmitter	
Equalization	Optimum time-delay for each Baseband data
Pulse Shaping	NA
I/Q Mismatches	Gain Imbalance: NA*
	Phase Imbalance < 10°
Receiver	
Horizontal eye-opening at BER=10^{-15}	31%–37% UI$_{sub}$
Jitter	1% UI$_{sub}$ (4 ps)
Equalization	LPF/BPF

* Since full-swing square-wave clocks are used, gain imbalance does not exist.

respectively.
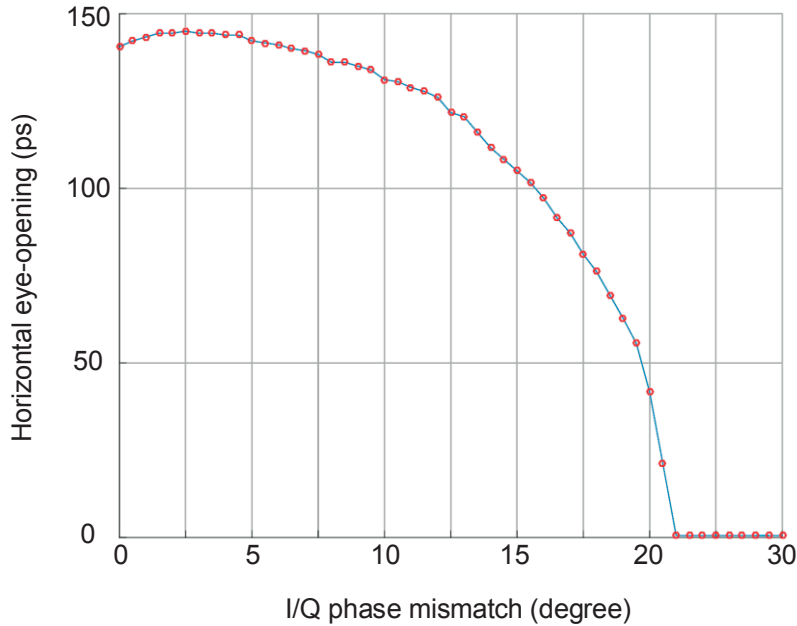
Figure 3.10: Horizontal eye-opening at BER $= 10^{-15}$ versus I/Q phase mismatch.

Statistical system-level simulation[3] of the proposed architecture of Fig. 3.7 has been performed in MATLAB to render a preliminary performance analysis for very low bit

---

[3] In Appendix A a brief overview of statistical simulation for serial data links is presented, and its advantages over time-domain simulation is reviewed.

error rates (BER). Fig. 3.8 presents the simulation results for the equalized eye diagrams on RX side for the BER as low as 10^{-24}. In this simulation the RX has $2\% \times T_{\text{ref}}$ rms jitter, the aggregate data rate is chosen to be 7.5 Gb/s (i.e., $T_{\text{ref}} = 400\,\text{ps}$), and ideal clock with zero I/Q mismatch is employed. As Fig. 3.8 shows, even without any sophisticated equalization scheme (e.g., DFE and XDFE) the horizontal eye-opening can be as large as 100 ps (i.e., 25% UI_{sub}), and 78 ps (i.e., 19% UI_{sub}), for the baseband and the passband at $\text{BER} = 10^{-20}$, respectively. This is a promising result since the system building blocks can be realized with a reasonable efficiency, and we can surmise that in a real design by applying a simple equalization scheme (e.g., CTLE at the RX front-end) the system performance can be largely improved. However, the I/Q mismatch effect should be also well considered so as to prevent any impractical specification for clock generation unit. Fig. 3.9 presents the I sub-band eye diagram for different I/Q mismatch. Although a 5° phase mismatch does not cause a critical eye-closure, this adverse effect becomes largely important for I/Q phase mismatch beyond 20°, i.e., 11.1 ps for a 5 GHz clock. The horizontal eye-opening versus I/Q phase mismatch at $\text{BER} = 10^{-15}$ is shown in Fig. 3.10. It can be seen that having 5°-10° (the reference is a 5 GHz clock signal) still leaves enough margin for the eye diagram to provide error free operation. From the circuit perspective, this amount of phase mismatch can be guaranteed by a power-efficient topology [24]. Table 3.1 summarizes the TRX specifications used in these system-level simulations. As can be construed from this Table, the overall TRX requirements can be realized with power-efficient circuit topologies, and the system can reach a better performance compared with a conventional BB link system. Moreover, having the carrier frequencies as integer multiples of the sub-band, the low-pass filters and the mixer circuits can be implemented efficiently as an integrate-and-dump circuit[4] [44]. In the next Chapter these insights will be applied in a memory system paradigm to realized a very power-efficient and high-speed serial data transceiver for communicating over a multi-drop channel interface.

3.2.2   Hybrid NRZ/MT TRX Detailed System Design

The proposed architecture for realizing the suggested modulation scheme of Fig. 3.6 (b) is shown in Fig. 3.11. This architecture is developed to address the aforementioned multi-tone challenges. The random data is generated by three independent embedded PRBS15 generators, each operating at F_{ref}, i.e., 2.5 GHz. Two mixers upconvert two sets of random data into I and Q sub-bands to create the QPSK band. The local frequency is chosen to be $2 \times F_{\text{ref}}$. The third stream is added together with I / Q sub-bands by the output summer/driver circuit. In this architecture there is no data at the odd multiplication of F_{ref}. Therefore, the local oscillator harmonics do not cause any data

---

[4]Generally speaking, any low-pass filter that forms a perfect reconstruction set together with its up-converted versions can replace the integrators.
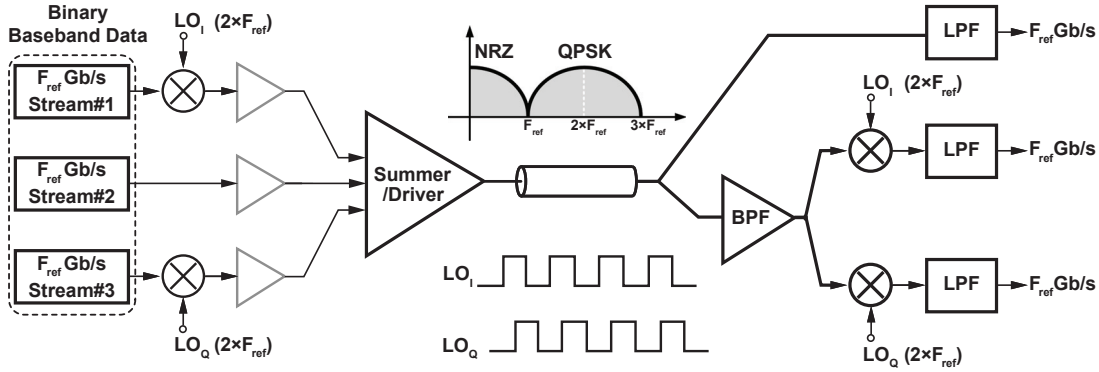
Figure 3.11: Proposed hybrid NRZ/MT transceiver.

corruption. From the linearity requirement point of view, QPSK modulation without pulse shaping does not require a linear output driver [45]. Hence, a current-mode output driver can appropriately add BB, I, and Q sub-bands together and construct the hybrid NRZ/MT output stream. Our system-level simulation shows that without the baseband pulse-shaping, the eye diagram can provide a 55% horizontal opening at BER = 10^{-12}. Adding a pulse-shaping filter (i.e. raised-cosine filter) to TX can improve the eye-opening value by only 8%, i.e., 63% horizontal eye-opening. Hence, no pulse shaping is employed due to the cost it adds to the TRX circuit complexity. A source-synchronous architecture is employed for the clocking scheme. This architecture can relax the complexity of the CDR circuit on the RX side and provide an inherent tracking of correlated jitter for CDR purposes [46].

Beside these, the output spectrum of the proposed TRX has an inherent notch at F_{ref} and $3 \times F_{\text{ref}}$, as shown in Fig. 3.11. Therefore, by adjusting the reference clock frequency the TX spectrum shape can track the channel notches and customize the whole link to the channel. In the NRZ/MT approach, in order to match the transmitted spectrum to that of the channel, an initial calibration phase is applied which can change the reference clock frequency depending on the quality of the received signal. The transmitted spectrum at the output of TX can therefore be shaped with respect to the channel characteristic and the aggregate TX bit rate equal $3 \times F_{\text{ref}}$ b/s, while its spectrum has minimum energy around the notches. The need for frequency adaptability of the system requires the TRX circuits to employ such topologies that are tunable by changing F_{ref}. In addition, as will be shown in Section IV, experimental results show that having a 10% variation on the F_{notch} from its nominal value results in an approximately 30% reduction in horizontal eye-opening and still leaves enough margin for error-free operation.
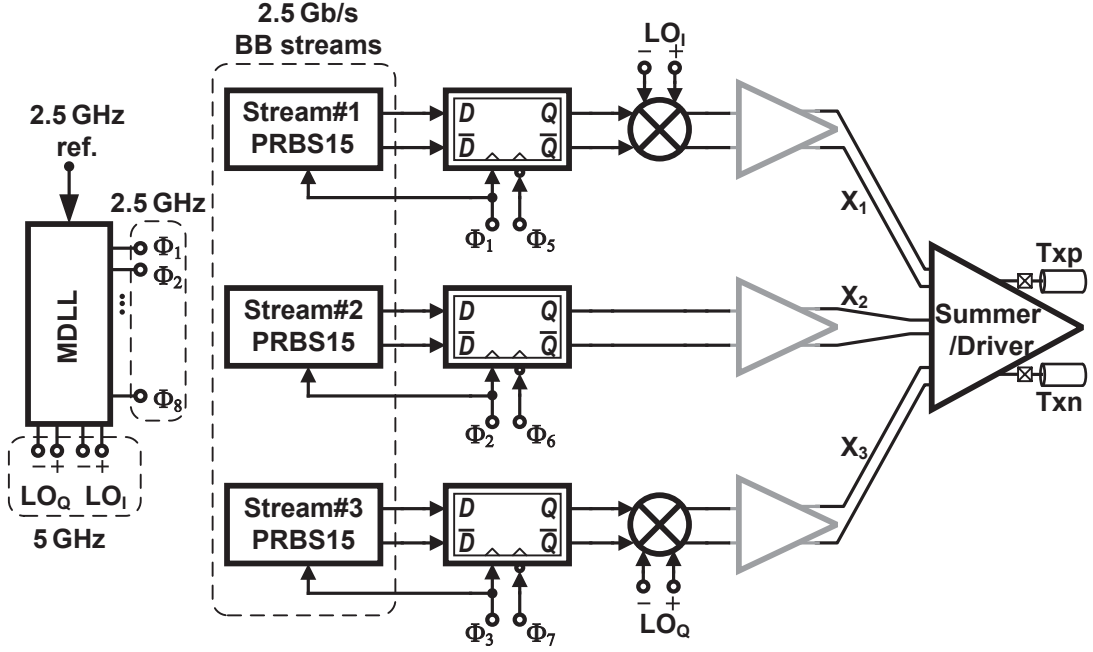
Figure 3.12: The architecture of the proposed mixed NRZ/MT transmitter.

3.3 Hybrid NRZ/MT signaling: Circuit Design

Based on the system-level requirements, the design of RX, TX, and the clock generation unit are described in this section. The goal is to communicate at 7.5 Gb/s over the MDB channel shown in Fig. 3.2 (b).

3.3.1 Transmitter

Fig. 3.12 shows the hybrid NRZ/MT transmitter architecture. Since NRZ plus QPSK frequency planing is employed, two mixers are required to upconvert baseband data and construct the QPSK band. The third stream should then be added on top of the QPSK sub-band. Moreover, as described in Section II, baseband pulse-shaping is not applied.

The concurrent transitions are also avoided at the inputs of the summer/driver circuit. Different clock phases, $\{\Phi_1, \Phi_5\}$, $\{\Phi_2, \Phi_6\}$, and $\{\Phi_3, \Phi_7\}$ are used for generating the baseband streams and proper $LO_{I,Q}$ are employed for upconversion, as shown in Fig. 3.12. The eye diagram for X_1, X_2, and X_3 (the summer/driver input signals) is plotted in Fig. 3.13 (a). It shows that each transition has at least $T_{\mathrm{ref}}/16$ (i.e. 25 ps for $T_{\mathrm{ref}} = 400$ ps) time difference from the nearest transition point. This can efficiently reduce the peak-to-average ratio (PAR) and mitigate inter-channel interference (ICI). Fig. 3.13 (b) illustrates
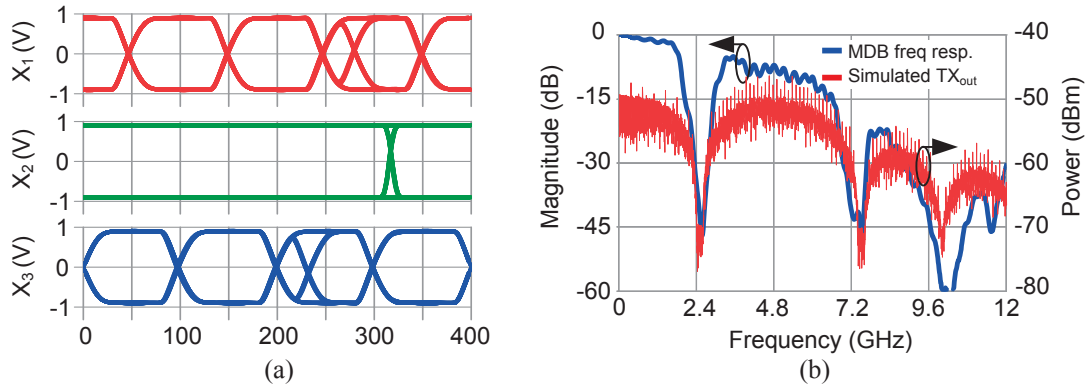
Figure 3.13: (a) Eye diagram of the summer/driver input signals. (b) Simulated TX output spectrum.
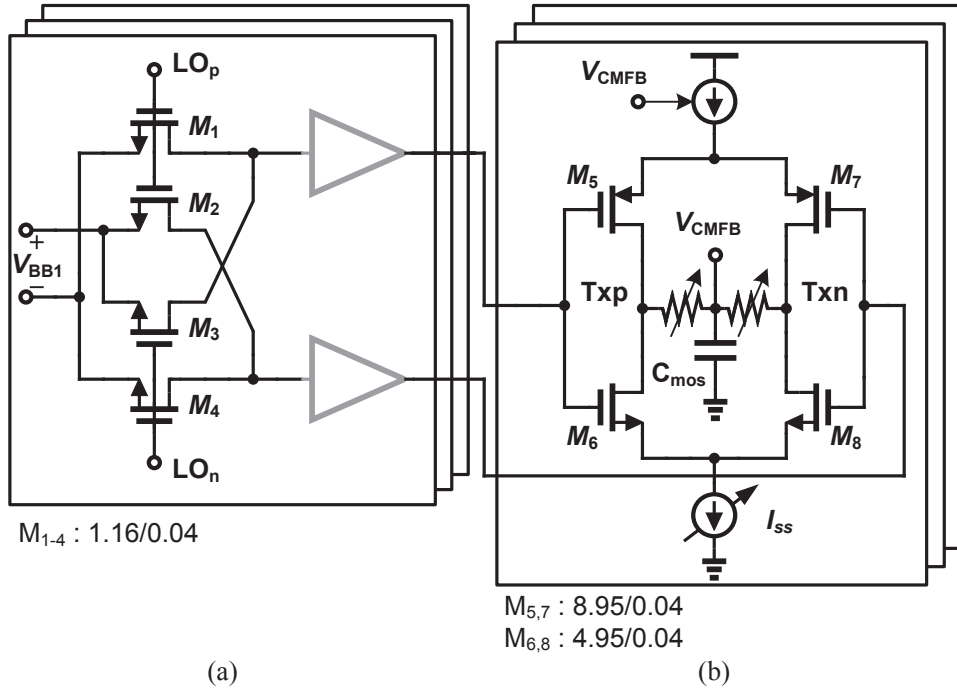
Figure 3.14: (a) Upconversion passive mixer schematic. (b) Output driver schematic.

the simulated output power of the proposed TX of Fig. 3.13 (a), and it shows that the transmitted stream yields matched spectrum notches to which of the MDB interface.

Fig. 3.14 (a) shows the upconversion mixer topology. Two double-balanced passive-type mixers are used to upconvert two sets of baseband data. The schematic of the current-mode summer/driver block is shown in Fig. 3.14 (b). The LVDS summer/driver is designed to add the sub-bands together and provide a 300 mV peak-to-peak swing at the output,
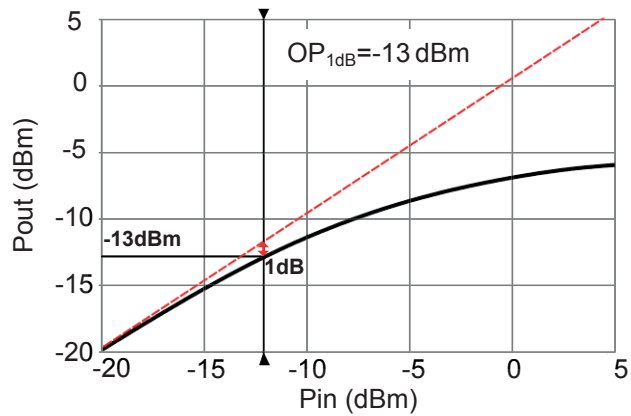
Figure 3.15: Output power of the LVDS driver circuit with respect to the 5 GHz input signal power level.
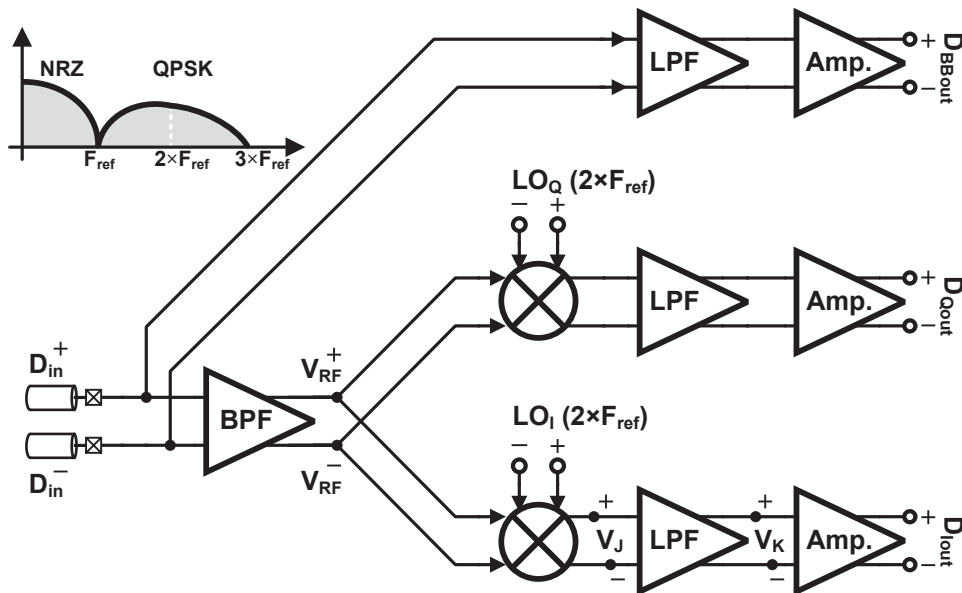
Figure 3.16: The architecture of the proposed mixed NRZ/MT receiver.

while the output termination can be tuned by programmable resistors. The driver output power versus input power is shown in Fig. 3.15 for a 5 GHz sinusoidal signal. The output 1-dB compression point is simulated to be -13 dBm, which is sufficient for the proposed NRZ/MT modulation scheme.
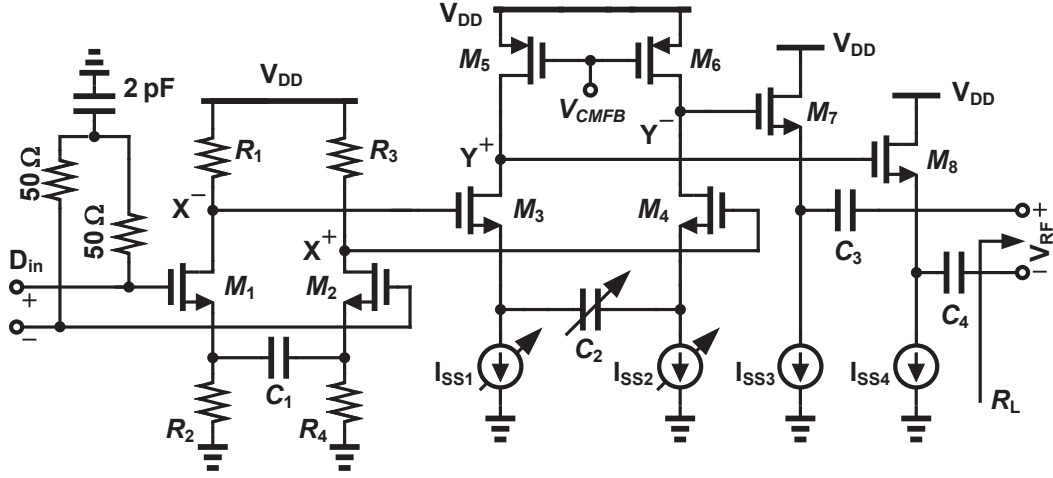
Figure 3.17: Schematic of the BPF to pass QPSK sub-bands.

3.3.2   Receiver

The proposed NRZ/MT receiver is shown in Fig. 3.16. Each of the received sub-bands has a F_{ref} b/s data rate, which provides a $3 \times F_{\text{ref}}$ b/s aggregate data rate. The received signal is filtered by the channel frequency response and is more attenuated for the QPSK band. The attenuation for the NRZ band is around 5 dB, while the QPSK band experiences a 12 dB tilt from F_{ref} to $3 \times F_{\text{ref}}$. Therefore, to recover the NRZ sub-band, low-pass filtering of the QPSK band provides sufficient equalization, and DFE or CTLE is not required. For the QPSK sub-band, after bandpass filtering and gain boosting, the direct-conversion architecture is used for downconversion.

The simulation results over different process corners show that the received signal has at least a total power of -19 dBm and -24 dBm for the NRZ and QPSK sub-bands, respectively. The QPSK modulation necessitates an SNR of about 18 dB for BER $= 10^{-14}$ [45]. The required SNR for the NRZ band is calculated to be 13 dB at BER $= 10^{-14}$. Based on these specifications, the noise figure (NF) of the input amplifier can be calculated as [45]:

$$NF = P_{\text{min}} - 10 \log(BW) - SNR_{\text{min}} + 174 \tag{3.2}$$

where P_{min} is the minimum received signal power, BW is the frequency band of interest, and SNR_{min} is the required SNR level for equalizing received data. Replacing the corresponding numbers in 3.2, the receiver NF for BER $= 10^{-14}$ is found to be 35 dB and 45 dB for the QPSK and NRZ sub-bands, respectively. Hence, the bandpass filter (BPF) and the input lowpass filter (LPF) for the NRZ sub-band should be designed such that this NF is satisfied for each sub-band receiver. Moreover, based on the system-level simulation, $\pm 5°$ phase mismatch between LO_I and LO_Q yields a 2 dB SNR penalty in the

vicinity of BER $= 10^{-12}$. This amount of the SNR penalty can be properly compensated in the input amplifier by providing a 2 dB lower NF specification. Hence, the $LO_{I/Q}$ phase mismatch should be kept lower than $\pm 5°$ and the analog front-end (AFE) should be designed such that the receiver NF remains below 32 dB. We describe the design of these circuits in the following.

3.3.2.1 AFE Circuit Design

BPF Design: The schematic of the input amplifier for the QPSK sub-band is shown in Fig. 3.17. The QPSK sub-band RX front-end employs a bandpass amplifier with +10 dB of peaking at $2 \times F_{\text{ref}}$ to help with channel loss equalization. It should also suppress the baseband part of the received signal, i.e., from DC to F_{ref}. To achieve this target, a two-stage peaking amplifier is used that employs capacitive source degeneration. The final stage of the amplifier consists of a source follower buffer and an ac-coupling capacitor, in order to drive the succeeding mixer stages with a sufficient current and provide a constant source impedance during downconversion. In this circuit, M_5 and M_6 are in strong inversion. This circuit is basically consists of two peaking amplifier and a high-pass common-source circuit (i.e., $M_{7,8}$ with capacitor $C_{3,4}$). The final band-pass transfer function is generated by cascading these three stages. Based n these explanations, the BPF gain can be calculated as

$$H(s) = \frac{V_{\text{RF}}}{D_{\text{in}}}(s) = A_{\text{v01}} \frac{1 + s/z_1}{1 + s/p_1} \cdot A_{\text{v02}} \frac{1 + s/z_2}{1 + s/p_2} \cdot A_{\text{v03}} \frac{s/p_3}{1 + s/p_3}$$
$$\times \frac{1}{(1 + s/p_{\text{X}})(1 + s/p_{\text{Y}})} \tag{3.3}$$

where the zeros and poles are associated to each nodes, shown in Fig. 3.17, and the coefficients can be calculated as

$$A_{v01} = -\frac{g_{m1}}{1 + g_{m1}R_2 + g_{m1}/r_{o1}} \cdot [r_{o1} + R_2 (1 + g_{m1}r_{o1})] \parallel R_1 \tag{3.4a}$$

$$z_1 = -\frac{1}{2C_1R_2} \quad ; \quad p_1 = -\frac{R_1 + r_{o1} + R_2 (1 + g_{m1}r_{o1})}{2C_1 (r_{o1} + R_1) R_2} \tag{3.4b}$$

$$A_{v02} = -\frac{g_{m3}}{1 + g_{m3}R_{ISS1} + g_{m3}/r_{o3}} \cdot [r_{o3} + R_{ISS1} (1 + g_{m3}r_{o3})] \parallel r_{o5} \approx -\frac{r_{o5}}{R_{ISS1}} \tag{3.4c}$$

$$z_2 = -\frac{1}{2C_2R_{ISS1}} \quad ; \quad p_2 = -\frac{r_{o5} + r_{o3} + R_{ISS1} (1 + g_{m3}r_{o3})}{2C_2 (r_{o3} + r_{o5}) R_{ISS1}} \approx -\frac{g_{m3}r_{o3}}{2C_2 (r_{o3} + r_{o5})} \tag{3.4d}$$

$$A_{v03} = \frac{g_{m7}R_{ISS3}}{1 + g_{m7}R_{ISS3}} ; \quad p_3 = -\frac{1}{C_3 Z_L} \tag{3.4e}$$

$$p_X = -\frac{1}{C_X [r_{o1} + R_2 (1 + g_{m1}r_{o1})] \parallel R_1} \tag{3.4f}$$

$$p_Y = -\frac{1}{C_Y [r_{o3} + R_{ISS1} (1 + g_{m3}r_{o3})] \parallel r_{o5}} \tag{3.4g}$$

where C_X and C_Y are the parasitic capacitances at nodes X and Y, respectively, R_{ISS1} and R_{ISS3} are the output resistance of the current sources $I_{SS1,2}$ and $I_{SS3,4}$, respectively, r_{o1}, r_{o3}, and r_{o7} are the output resistance of M_1, M_3, and M_5, respectively, R_L is the load resistance seen by the amplifier, and g_{m1}, g_{m3}, and g_{m7} are the transconductance of M_1, M_3, and M_7, respectively. In deriving (3.4) it is assumed that the circuit operates differentially and the parasitic capacitors at the drain of M_{1-4} are negligible.

To have a better insight into the operation of the BPF, the simplified gain expression of this amplifier, which is indeed a bandpass CTLE, can be written as

$$A_v(s) = \frac{V_{RF}(s)}{D_{in}(s)} \approx A_{v0} \frac{sC_3R_L (1 + 2sC_1R_2)}{(1 + sC_3R_L) (1 + 2sC_1/g_{m1})} \times \frac{1 + 2sC_2R_{ISS1}}{1 + 2\alpha sC_2/g_{m3}} \tag{3.5}$$

where $A_{v0} = g_{m1}g_{m3}/ [(1 + g_{m3}R_{ISS1}) (1 + g_{m1}R_2)] \times g_{m7}r_{o5}R_1R_L/ (1 + g_{m7}R_L)$, R_{ISS1} is the output resistance of the current source $I_{SS1,2}$, $\alpha = r_{o3}/(r_{o3} + r_{o5})$ where r_{o3} and r_{o5} are the output resistance of M_3 and M_5, R_L is the load resistance seen by the amplifier, and g_{m1}, g_{m3}, and g_{m7} are the transconductance of M_1, M_3, and M_7, respectively. In deriving (3.5) it is assumed that the circuit operates differentially, the parasitic capacitors at the drain of M_{1-4} are negligible, and $g_m r_o \gg 1$.

The amplifier frequency response can be adjusted by the different settings. Fig. 3.18 plots the simulation of its transfer function for different capacitor values, and in different PVT
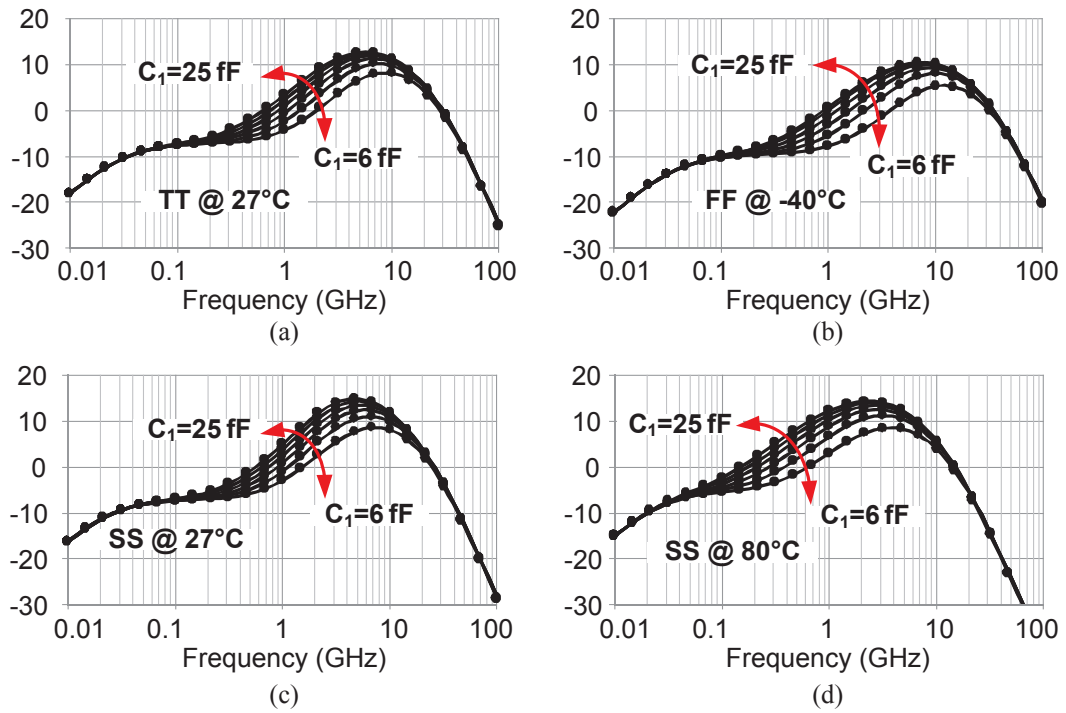
Figure 3.18: Transfer function of the BPF for different capacitor value, C_2, settings. (a) TT corner at 27° C. (b) FF corner at -40° C. (c) SS corner at 27° C. (d) SS corner at 80° C.
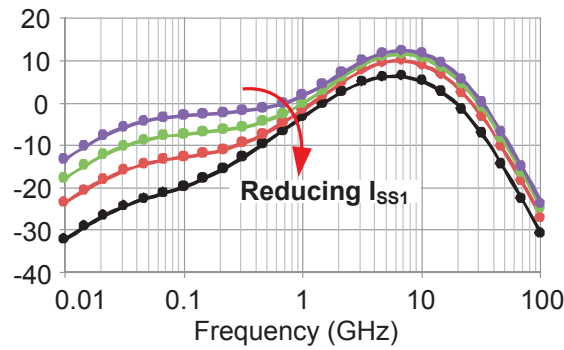
Figure 3.19: BPF transfer function for different gain settings.

corners, revealing a 10 dB high-frequency boosting, while it suppresses the low-frequency content of the spectrum. The peak frequency is tunable over the 3.5-7.5 GHz band and the 3 dB bandwidth is approximately 6.5 GHz for the peak frequency of 5 GHz.

The equalization amount can be changed by changing the second stage gain. This is done by changing the bias current of $M_{3,4}$ and adjusting $g_{m3,4}$. The current source has four different settings. The gain simulation result for different current settings is shown in Fig. 3.19. It shows a 6 dB gain adjustment for the peak frequency.

Figure 3.20: Schematic of the LPF used to select NRZ sub-band.

NRZ Input LPF Design   Fig. 3.20 shows the schematic of the input LPF that is employed for the NRZ sub-band. The G_m-C biquad section consists of transistors M_3-M_6 and the capacitors C_1 and C_2 [47]. In this circuit, M_7 and M_8 convert the input differential current into the voltage for the G_m-C biquad section and they also improve the filter's cut-off frequency. This circuit implements a low-pass transfer function, which helps to further suppress the signal from unwanted sub-bands. The biquad section transfer function (i.e. $H_{\mathrm{bq}}(s) = D_{\mathrm{BBout}}/V_{\mathrm{X}}$), and the input stage transfer functions (i.e., $H_{\mathrm{in}}(s) = V_{\mathrm{X}}/D_{\mathrm{in}}$) can be calculated as

$$H_{\mathrm{bq}}(s) = \frac{s^2 + \left(\omega_{\mathrm{z}}/Q_{\mathrm{z}}\right)s + \omega_{\mathrm{z}}^2}{s^2 + \left(\omega_0/Q_0\right)s + \omega_0^2} \cdot \left(\frac{\omega_0^2}{\omega_{\mathrm{z}}^2}\right) \tag{3.6a}$$

$$H_{\mathrm{in}}(s) = \frac{-g_{\mathrm{m1}}}{[1-H_{\mathrm{bq}}(s)](g_{\mathrm{m3}}+sC_{\mathrm{gs3}})+[1+H_{\mathrm{bq}}(s)](g_{\mathrm{m7}}+sC_{\mathrm{gs7}})} \tag{3.6b}$$

where $\omega_{\mathrm{z}}^2 = g_{\mathrm{m3}}g_{\mathrm{m5}}/[C_1(C_{\mathrm{gs3}}-C_{\mathrm{gs7}})]$, $\omega_0^2 = g_{\mathrm{m3}}g_{\mathrm{m5}}/(2C_1C_2)$, g_{mK} represents the transconductance of M_{K} (K is the transistor number), C_{gsN} is the gate-source capacitance of M_{N} (N is the transistor number), $Q_{\mathrm{z}} = \omega_{\mathrm{z}}C_1(C_{\mathrm{gs3}} - C_{\mathrm{gs7}})/(g_{\mathrm{m3}}C_{\mathrm{gs5}})$, and $Q_0 = 2\omega_0C_2/(g_{\mathrm{m5}})$. In deriving (3.6b) it is assumed that the circuit is operating fully differentially, the drain-source capacitors are negligible, and C_1, $C_2 \gg C_{\mathrm{gsN}}$. The overall filter transfer function can be expressed by

$$H_{\mathrm{LPF}}(s) = H_{\mathrm{bq}}(s) \times H_{\mathrm{in}}(s) \tag{3.7}$$

Figure 3.21: Transfer function of the BPF for different capacitor value, C_2, settings. (a) FF corner at -40° C. (b) SS corner at 100° C. (c) TT corner at 27° C.

This transfer function presents a LPF transfer function, which removes the QPSK sub-band and amplifies the NRZ sub-band. The ratio of C_{gs3}/C_{gs7} is around 6 in this design to improve the bandwidth of the filter and provide a better time-domain pulse response.

This circuit has a common-mode-feedback (CMFB) that sets the output DC value. The simulation of the filter transfer function for different capacitor settings and for different PVT corners is plotted in Fig. 3.21, showing a tunable 3 dB bandwidth from 1.7 GHz to 3.3 GHz. Based on these simulations, the maximum interferer energy from QPSK band (i.e., QPSK-to-NRZ ICI) remains below -15 dBm that is sufficient for our application.

By adjusting the current of the input differential pair (i.e., I_{SS} in Fig. 3.20), $g_{m1,2}$ is adjusted and the DC gain can be tuned from -4.5 dB up to 3.9 dB. The current DACs are placed at the drain and the source of the input differential pairs and the bias current of the input stage is adjusted such that the bias current of the second stage is fairly constant. Therefore, the overall transfer function shape is not changed but the DC gain is tuned.

3.3.2.2   Downconverting Mixer / Filter Unit

To properly recover the data that I/Q sub-bands are carrying over, a switched-capacitor mixer and filter (SCMF) circuit is developed. In addition to downconverting the received signal, the proposed circuit suppresses the unwanted high-frequency components of the
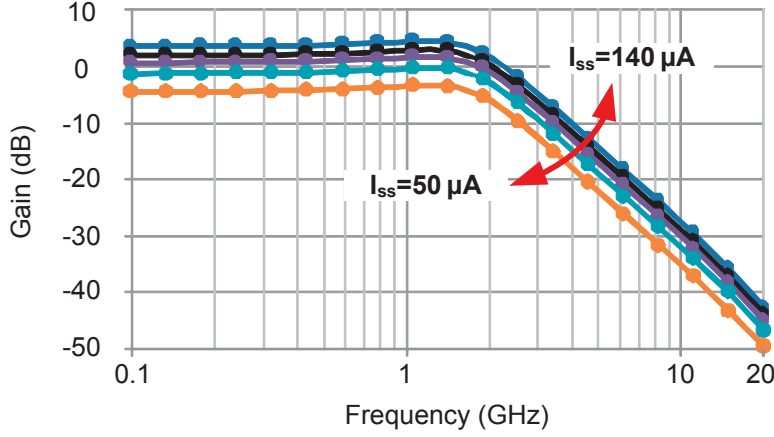
Figure 3.22: LPF transfer function for different gain settings in TT corner.

signal, and meanwhile isolates the I and Q sub-bands from each other. Fig. 3.23 shows the half-circuit implementation of the proposed SCMF, and the baseband amplifier units. The timing diagram for I sub-band and the received data-stream are shown in Fig. 3.24. The SCMF is designed such that the received data is multiplied by the orthogonal basis functions that have been used in the transmitter, i.e., 90° phase-shifted square waveforms. As shown in Fig. 3.23, M_1 is on during $\{\Phi_1, \Phi_2\}$ and also $\{\Phi_5, \Phi_6\}$ time intervals. Assuming that the sampling clock is properly aligned with the received data, this circuit is able to detect I sub-band and suppress the Q sub-band. The input signal (i.e., V_{RF}^+), which is in voltage domain, is sampled at the falling edge of the CK_{I}^+ and CK_{Q}, and is held on the capacitor C_2 in the upper and lower paths, respectively. As shown in the timing diagram of Fig. 3.24, the Q sub-band is held as common-mode signal on sampling capacitors while the I sub-band remains differential on V_{K1}^+ and V_{K1}^-. Therefore, subtracting these voltage nodes yields to I sub-band recovery and Q sub-band cancellation. At the end of this process, after the data is detected, the capacitors will be discharged by a reset clock phase, CK_{RI}, and made ready for the next phase.

Based on this operation and the timing diagram shown in Fig. 3.24, the output of SCMF circuit at $t = (n - 1/2)T_{\mathrm{ref}}$ (i.e., after being sampled by CK_{Q}) can be approximated by

$$V_{\mathrm{K1}}^+(n - 1/2) = V_{\mathrm{Q}}(n) + V_{\mathrm{I}}(n) \tag{3.8a}$$
$$V_{\mathrm{K1}}^-(n - 1/2) = V_{\mathrm{Q}}(n) - V_{\mathrm{I}}(n) \tag{3.8b}$$

where $V_{\mathrm{I}}(n)$ and $V_{\mathrm{Q}}(n)$ represent the corresponding I and Q component of V_{RF}, respectively. Therefore, the output voltage of the amplifier (shown in Fig. 3.17) can be expressed as

$$D_{\mathrm{Iout}}(n - 1/2) = 2 \times g_{\mathrm{m7,8}}R_1 \times V_{\mathrm{I}}(n) \tag{3.9}$$
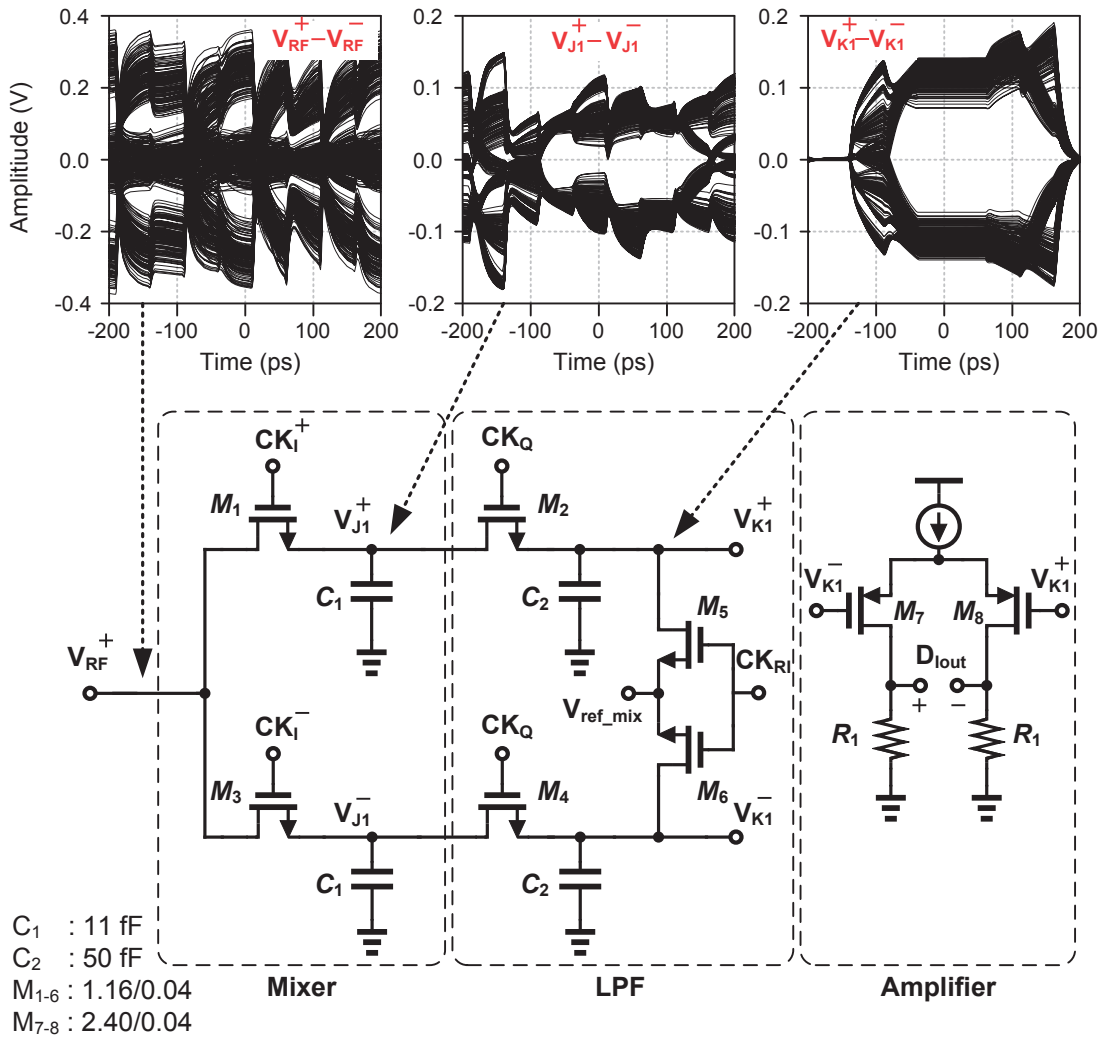
Figure 3.23: Half-circuit implementation of SCMF and baseband amplifier units.

where $g_{m7,8}$ is the transconductance of the $M_{7,8}$ in Fig. 3.23. As (3.9) shows, the Q sub-band is canceled and the I sub-band is recovered.

3.3.3 Clock Generation Unit

A differential source-synchronous architecture is employed for clock and data recovery (CDR) owing to the fact that it inherently tracks the correlated jitter while it reduces the complexity of CDR circuit [46]. The clock unit on transmitter and receiver includes a multiplier delay locked-loop (MDLL) block, which generates eight equally spaced phases from reference input clock, and it provides two orthogonal clock phases at twice of the reference clock, nominally at 5 GHz. The received clock is forwarded from the TX side

R	Reset
T&H	Track and hold
H	Hold
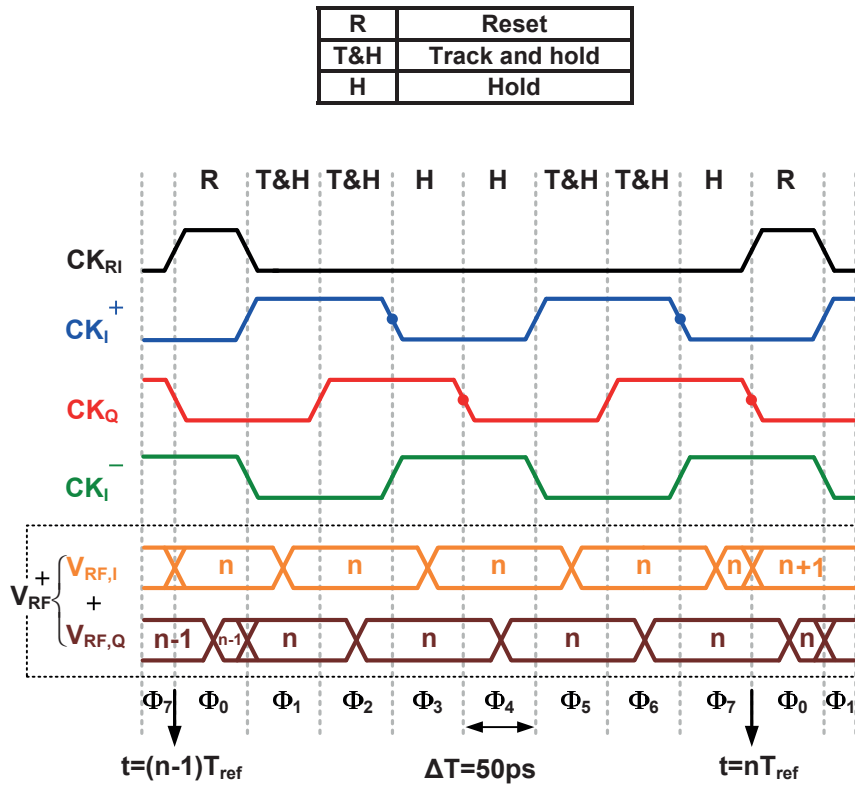
Figure 3.24: The timing diagram of the proposed SCMF.
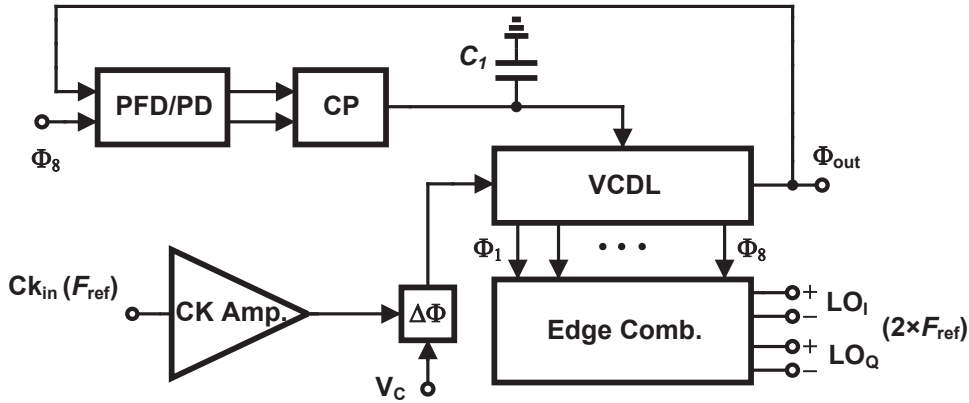
Figure 3.25: Clock generation system block diagram.

and is a single-ended signal, which has a frequency in the range of 1.3-3.2 GHz and an amplitude of approximately $VDD/3$.

Fig. 3.25 shows the main building blocks of the proposed MDLL-based CDR unit. Likewise, in order to facilitate synchronous operation between the TX and RX, the clock unit has
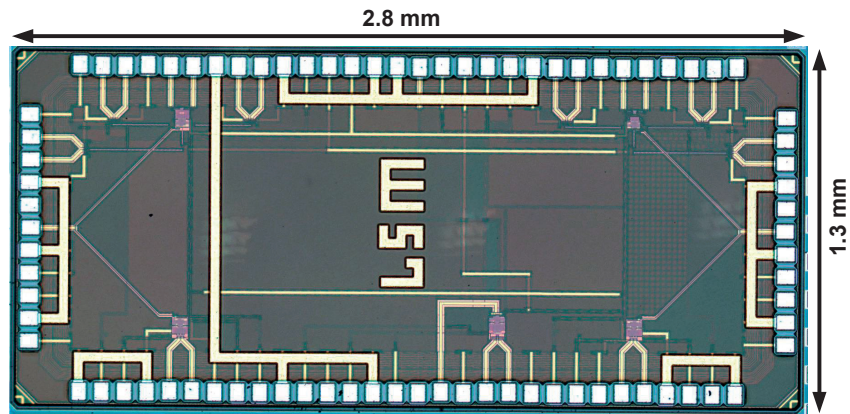
Figure 3.26: Chip die photo.
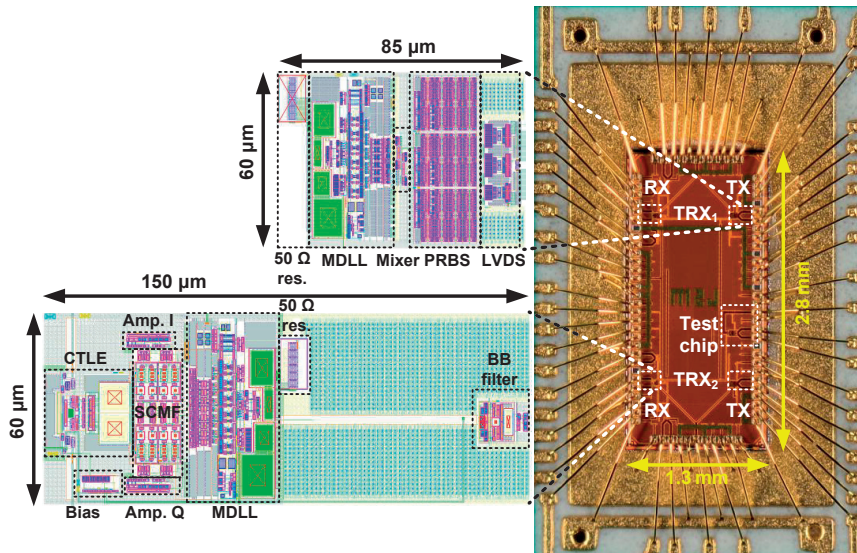
Figure 3.27: Micrograph and layout of the chip. The die size is $1.3 \times 2.8 \ mm^2$. Two identical TRXs are placed at the top and bottom of the chip.

the delay fine-tuning input, V_c in Fig. 3.25, for the phase adjustment, which can delay the input clock within a 100 ps interval and perform phase-alignment function. This delay is manually swept based on the recovered I/Q sub-band signal quality. The design and implementation of the clock generation unit is given in Chapter 4 in more detail.

3.4 Measurement Results

The TRX prototype is fabricated in a 40 nm GP 1-poly 10-metal bulk CMOS process, with the core voltage of 0.9 V. The chip die photo is presented in Fig. 3.26, which

(a)

(b)

(c)
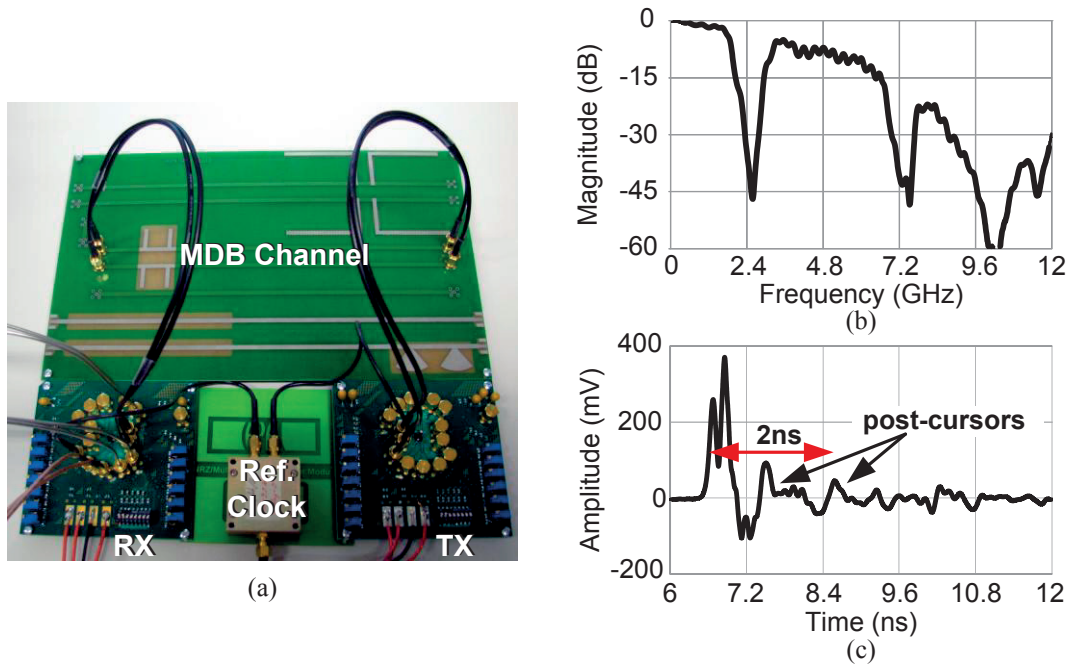
Figure 3.28: (a) Test setup with MDB channel. (b) Measured channel frequency response. (c) Measured channel 7.5 Gb/s single-bit pulse response.

(a)

(b)
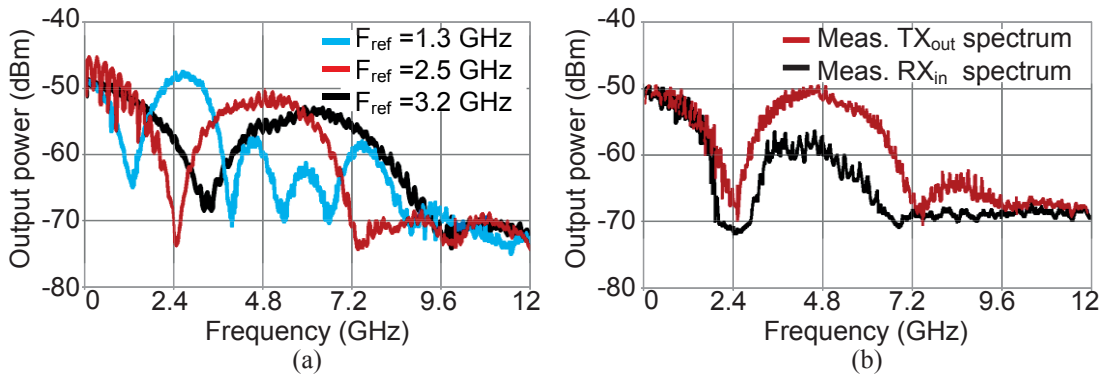
Figure 3.29: (a) Measured TX output spectrum at different F_{ref} settings. (b) Measured spectrum at the input of RX.

includes two independent TRXs and a test chip for the proposed MDLL. The die size is 1.3×2.8 mm^2 and all the RF pads has ESD protection circuit. The chip-on-board package is used for testing the prototype. The chip micrograph and layout is shown in Fig. 3.27, and includes two independent RX and TX circuits occupying 150×60 μm^2 and 85×60 μm^2, respectively. Fig. 3.28 (a) shows the test setup for the proposed NRZ/MT TRX system. The reference FR-4 channel, 30 cm in length, exhibits frequency notches as shown in Fig. 3.28 (b). These notches are introduced by two open stubs and can mimic the frequency response of a MDB channel. For test purposes, using this structure we are
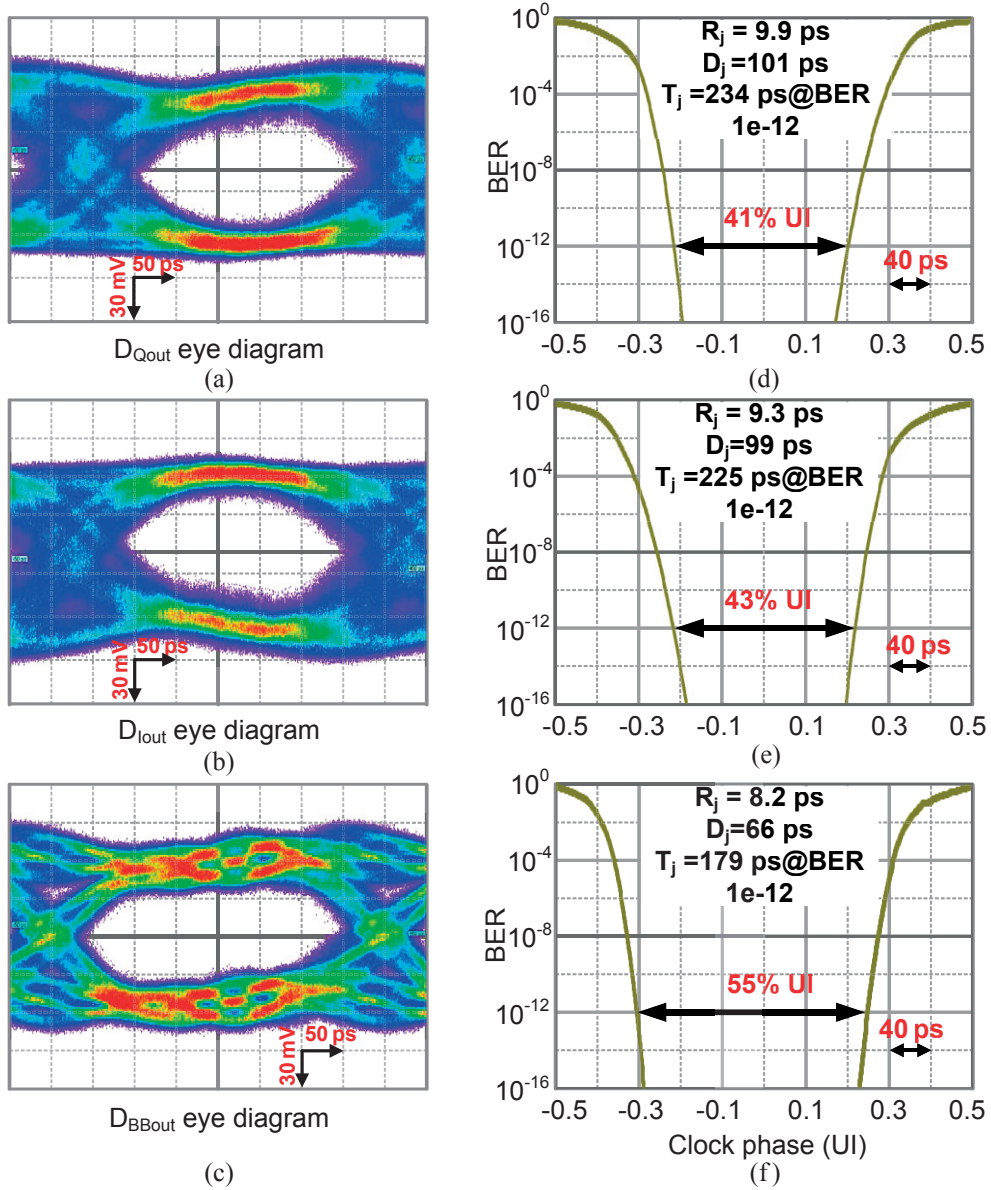
Figure 3.30: Measured RX eye diagram at 7.5 Gb/s data rate. (a) Q sub-band. (b) I sub-band. (c) BB sub-band. Corresponding bathtub curve for (d) Q sub-band, (e) I sub-band, (f) BB sub-band, each operates at 2.5 Gb/s data rate.

able to tune the frequency of the notches within a $\pm 40\%$ range. Fig. 3.28 (c) shows the measured 7.5 Gb/s single-bit pulse response of this channel, illustrating an approximately 2-ns-long tail and severe post-cursors. The strong reflections highlight how challenging it is to equalize such channels for conventional BB transceivers, as explained in Section 2 of this chapter.

The measured spectrum of the TX for the maximum, minimum and nominal working
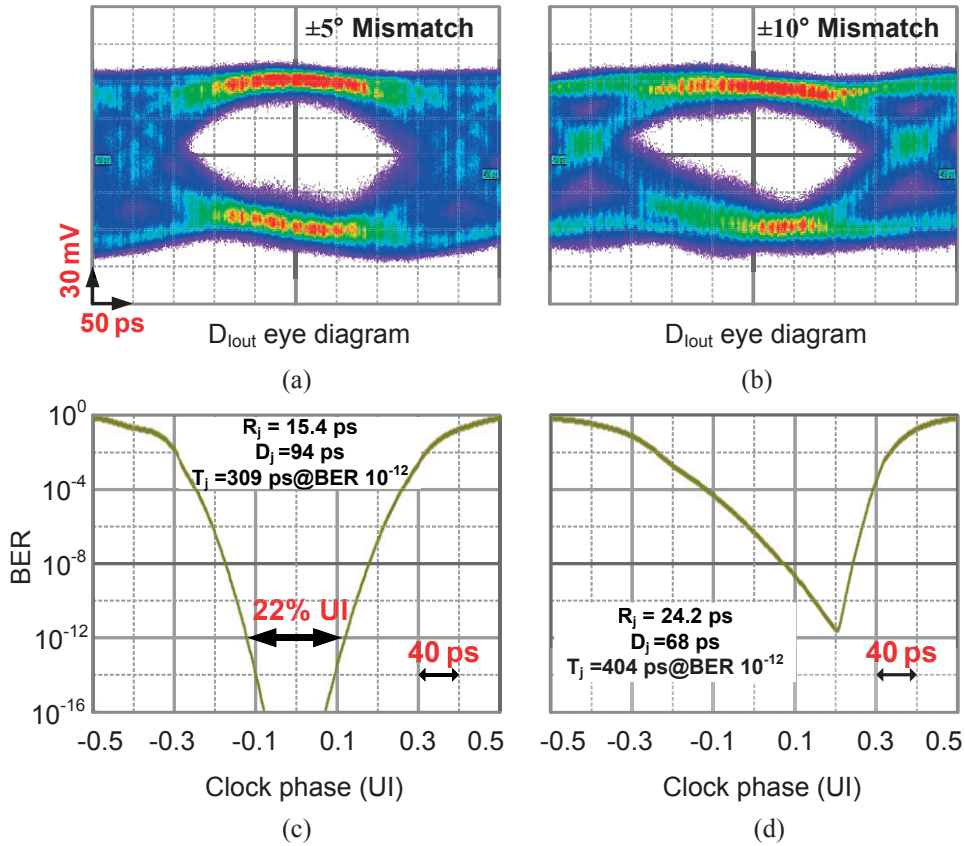
Figure 3.31:   Measured RX eye diagram sensitivity to phase-error. (a) ±5°, and (b) ±10° phase mismatch.

reference frequency, is shown in Fig. 3.29 (a). Based on this measurement, the TX is able to customize the frequency spectrum and the related sub-bands within a ±25% range (i.e., the first null frequency in the TX frequency spectrum can be changed between 1.3 and 3.2 GHz). The measured spectrum at the input of RX is shown in Fig. 3.29 (b) and shows that the QPSK sub-band is more attenuated compared with the NRZ sub-band. Based on this measurement, the received energy for the NRZ and the QPSK sub-bands are -18.4 dBm and -23 dBm, respectively.

Fig. 3.30 (a), (b), and (c) show the measured eye diagram for Q, I, and BB sub-bands, respectively, each having 2.5 Gb/s data rate. The bathtub for each of the Q, BB, and I sub-bands is shown in Fig. 3.30 (d), (e), and (f), respectively. The BB, Q, and I sub-bands have 220 ps, 164 ps, and 172 ps horizontal margin at BER $= 10^{-12}$, respectively. Each of the received sub-bands has sufficient eye-opening to ensure a 40% unit-time-interval horizontal eye-opening (referring to 2.5 Gb/s sub-band data rate) at BER $= 10^{-12}$.

The optimum phase for the LO signals, which are applied to SCMF unit is adjusted by

TX component	Power (mW)
Clock Unit	1.275
LVDS summer/driver	2.4
Mixer	0.225

(b)

RX component	Power (mW)
Clock Unit	1.575
Amplifiers	0.3
SCMF	0.525
AFE	1.125

(a)   (c)
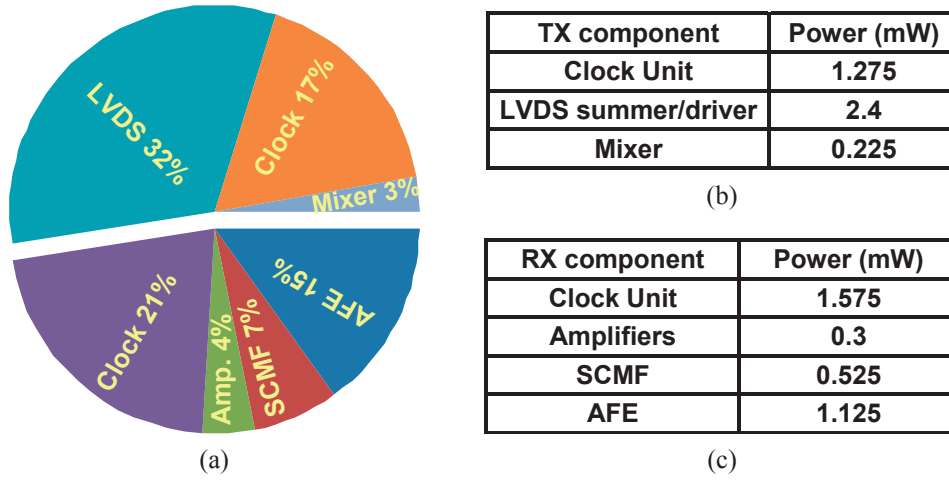
Figure 3.32: (a) Power breakdown for the whole TRX. (b) TX power specification. (c) RX power specification.
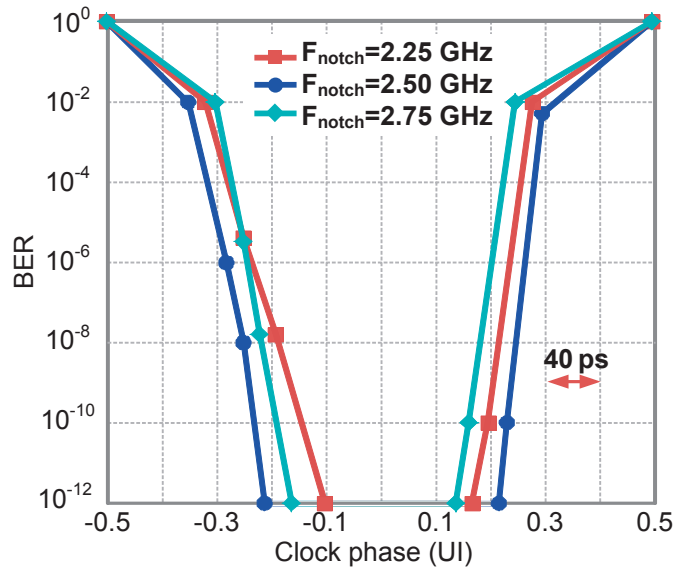
Figure 3.33: I sub-band bathtub curve for different channel notches.

the delay fine-tuning input. However, if there is a phase-error from this optimum value, the horizontal eye-opening is degraded. Fig. 3.31 (a) and (b) illustrate the measured eye diagram for the I sub-band with $\pm 5°$ (i.e., 5.5 ps) and $\pm 10°$ (i.e., 11 ps) phase mismatch, respectively. The corresponding bathtub curves are shown in Fig. 3.31 (c) and (d) and demonstrate 22% horizontal eye-opening at BER $= 10^{-12}$ for a $\pm 5°$ mismatch, while it starts to be closed at BER $= 10^{-12}$ for $\pm 10°$ phase mismatch.

The TRX power breakdown for the total data rate of 7.5 Gb/s is shown is Fig. 3.23 (a).

Table 3.2: TRX Performance Comparison with State-of-the-art Memory Transceivers.

Reference	[48]	[49]	[12]	[50]	[51]	**This Work**
Technology	180 nm CMOS	90 nm CMOS	65 nm CMOS	130 nm CMOS	28 nm LP CMOS	40 nm GP CMOS
Area (mm^2)	0.068 [**]	0.225	0.14 [**]	0.17 [**]	0.28 [*]	0.015 [**]
Channel	4" FR-4	2" FR-4	4" FR-4	MDB (8-drops) 5" Nelco	3.5" FR4+ DIMM connectors	MDB (4-drops) 12" FR4
Data rate (Gb/s)	5	8	8.4 (4.6/3.8) [***]	4.8	6.4	7.5
Link power efficiency (pJ/bit)	20	4	2.5 (2.3/2.7) [***]	14	9.1 [*]	1
BER / Horizontal eye-opening	10^{-12} / 63% UI (126 ps)	10^{-12} / NA	10^{-15} / NA	10^{-9} / 73% UI (152 ps)	10^{-10} / 40% UI (62.5 ps)	10^{-12} / 43% UI (172 ps)
Supply (V)	1.8	1.25	1	1.2	1	0.9
Signaling / Architecture	NRZ / FIR +CTLE	NRZ / CTLE	BB+RF (23 GHz carrier) / BPF+LPF	NRZ / FIR+ CTLE+ DFE	NRZ / CTLE +1-tap DFE	BB+I/Q (5GHz carrier) / LPF+ LPF+SCMF
TX output swing (mV$_{pp}$)	NA	200	350/1000 [***]	NA	285	280

* Area and power are given for one controller unit.
** Core size area.
*** The numbers are reported for BB/RF bands, respectively.

The whole chip consumes 7.5 mW from a 0.9 V power supply at this data rate, leading to 1 pJ/b link efficiency over the MDB channel interface. This includes the power consumption of TX (MDLL, mixers and LVDS driver) and RX (BPF, LPF, SCMF and MDLL). The consumption of the built-in PRBS15 generator and the I/O buffers that drive the measurement equipments are excluded from this calculation. The TX and RX consume 52% and 48% of the total power, respectively. The TX and RX circuit power consumption is shown in Fig. 3.23 (b) and (c), respectively.

The TRX has been designed such that the output spectrum can be well adapted to the channel frequency characteristic. It is also able to tolerate the mismatch in the channel notch frequency, while the frequency plan is kept unchanged (i.e., the first notch is not at 2.5 GHz while F_{ref} = 2.5 GHz). To measure the TRX tolerance, the total data rate is maintained at 7.5 Gb/s (2.5 Gb/s at each sub-band), while the first notch frequency is changed from its nominal value at 2.5 GHz by changing the stub length.

Table 3.3: Silicon Performance Summary.

Technology	40 nm CMOS GP 1P10M
Power supply	0.9 V
Package	Wire bond (1.2-1.8 mm length), COB
Channel	MDB (45dB@2.5GHz, 13dB@5GHz)
Pad capacitance (including ESD)	250 fF @ RF pad
Data rate	5.5-8 Gb/s (2.75-4 Gb/s/pin)
RX/TX link power efficiency	0.48/0.52 pJ/b @ 7.5Gb/s
Horizontal eye-opening @BER 10^{-12}	43% UI
Architecture	NRZ/multi-tone TRX (BB / I / Q sub-bands)
RMS jitter @ RX output	9.2 ps
TX output swing	280mV$_{pp}$ (70mV$_{rms}$)
TX/RX core area	85×60 μm^2/150×60 μm^2
CDR architecture	Source synchronous with fine delay adjustment on RX

Fig. 3.33 shows the I sub-band bathtub for different channel notches and shows that the eye-opening at BER = 10^{-12} is 27% UI (108 ps) and 30% UI (120 ps) for F_{notch} located at 2.25 GHz and 2.75 GHz, respectively. This measurement shows that the horizontal eye-opening degradation is less for the NRZ sub-band than for the QPSK sub-band. The NRZ sub-band demonstrates an approximately 6% UI degradation at BER = 10^{-12} due to the mismatch between the TX spectrum and the channel notches.

Table 3.2 summarizes the silicon performance comparison with state-of-the-art memory interface transceivers [48, 49, 12, 50, 51]. Compared to the other works, the proposed TRX has the link power efficiency of 1 pJ/b, while it operates over a multi-drop memory interface. The horizontal eye-opening is at least 164 ps for each sub-band at BER = 10^{-12}. The total bit-stream is divided into 3 sub-bands, each of which therefore operate at one third of the total bit rate. The horizontal eye margin thus benefits from this fact and the link becomes less sensitive to clock jitter and other non-idealities. The silicon performance summary is given in Table 3.3.

3.5   Conclusion

It has been shown that hybrid NRZ/MT signaling can be used to implement low-power and compact serial data transceivers for multi-drop channels. Using careful frequency planning in addition to discrete-time signal conditioning, a 7.5 Gb/s transceiver with 1 mW/Gb/s energy efficiency has been designed and fabricated in a bulk 40 nm CMOS technology. The measurement results confirm that NRZ/MT serial data TRX can offer an energy-efficient architecture over MDB interfaces. Choosing the proper sub-channels, the linearity requirement of the TX is relaxed and the summer and the output driver can be realized by a LVDS-type output driver. Moreover, by avoiding the channel frequency notches, there is no need to use DFE on the RX side and the LPF, BPF, and SCMF can satisfy the equalization requirements. Hence, significant power-saving on the RX side is achieved, leading to 1 pJ/b link efficiency in the MDB channel interface.

4 Multi-Phase Clock Genaration for Hybrid NRZ/MT Transciever

In this chapter we present the design and implementation of a multiplying delay-locked loop (MDLL), which can be used as clock and data recovery (CDR) unit in source-synchronous wireline communications. The MDLL doubles the reference frequency and delivers differential in-phase (I) and quadrature (Q) clocks by generating 8 equally spaced clock phases and combining these phases appropriately. The clock generation scheme can be employed to perform the CDR function in the NRZ/MT transceiver, which is introduced in the Chapter 3. To improve the system jitter performance, a technique for reducing deterministic jitter (DJ) in MDLL is proposed. The prototype of the proposed clock generation unit is implemented, as an independent block, in 40 nm bulk CMOS process, and it is also used in the proposed NRZ/MT TRX. The prototype dissipates 1.1-1.8 mW over output frequency range of 2.6-6.4 GHz, while the RMS jitter and I/Q mismatch remain below 3 ps$_{\mathrm{rms}}$ and $\pm5°$, respectively, over the entire range. The core size occupies 60×40 μm^2 silicon area.

4.1 MDLL-Based Clock and Data Recovery: Overview

The continuous growth of wireline data communications has driven the link speeds beyond 10 Gb/s. The data in multi-lane high-speed wireline communication systems are distorted by both external and internal noise during transmission, which leads to attenuation, jitter, and skew in the received data. In this paradigm, many emerging I/O standards employ source-synchronous scheme because of its inherent jitter tracking property [52, 53].

The DLL-based CDR topology is a preferable choice for source-synchronous high-speed links since it does not have the jitter accumulation issue and it consumes less power comparing to PLL-based CDR architecture [52]. The primary drawback of DLL-based CDR is its limit to synthesize frequency. Hence, the clean-up PLL should generate the
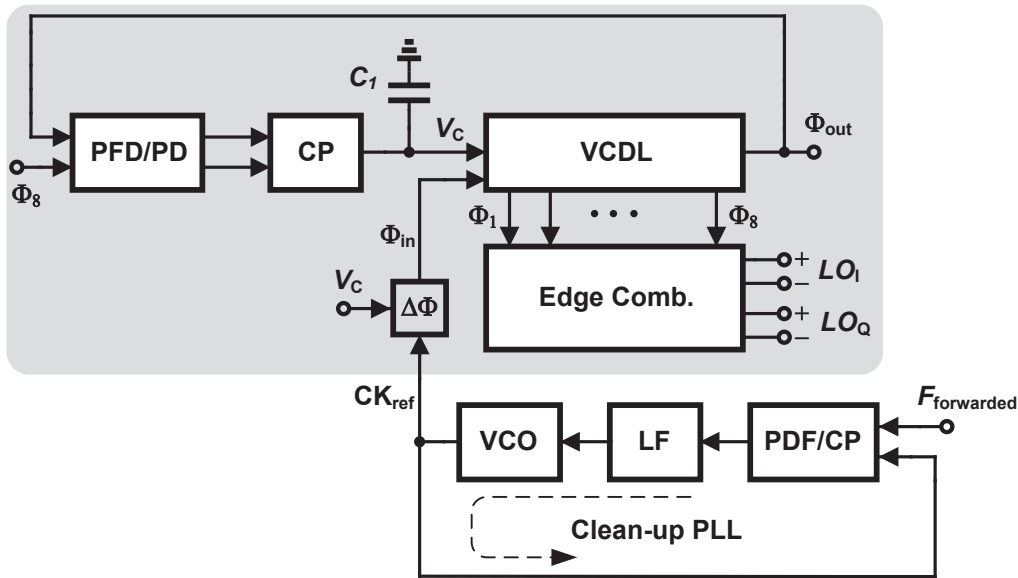
Figure 4.1: Proposed MDLL-based CDR architecture.

full-rate clock and distribute it to all receiver banks. This leads to a considerable power dissipation. However, by distributing half-rate clock from central PLL and multiplying it adequately in each RX bank one can save significant power dissipation in clock tree. For this purpose, the multiplier DLL (MDLL) based CDR is proposed in Fig. 4.1. Comparing to DLL-based CDR topology the total dynamic power consumption in the clock tree is halved for a given data rate. Moreover, the MDLL-based clock generation shows a better jitter performance since the accumulation of thermal-noise-induced timing uncertainties occurs only within one period of the crystal oscillator [54]. Given the same power budget for both PLL and MDLL-based CDRs, the overall jitter performance of the MDLL-based CDR architecture can be reasonably improved.

In the remainder of this Chapter, the design and implementation of low-power MDLL-based CDR unit is presented (highlighted in Fig. 4.1), which can be used in serial data transceivers that employ half-rate or multi-tone architecture. Moreover, the proposed MDLL has a delay fine tunning input, which can properly adjust the clock phase without adding significant jitter. This property facilitates employment of the proposed MDLL for CDR application in the NRZ/multi-tone receivers [24, 26]. This Chapter continues with the analysis and design of the MDLL building blocks in Section 4.2. The measurement and the conclusion are presented in Section 4.3 and 4.4, respectively.
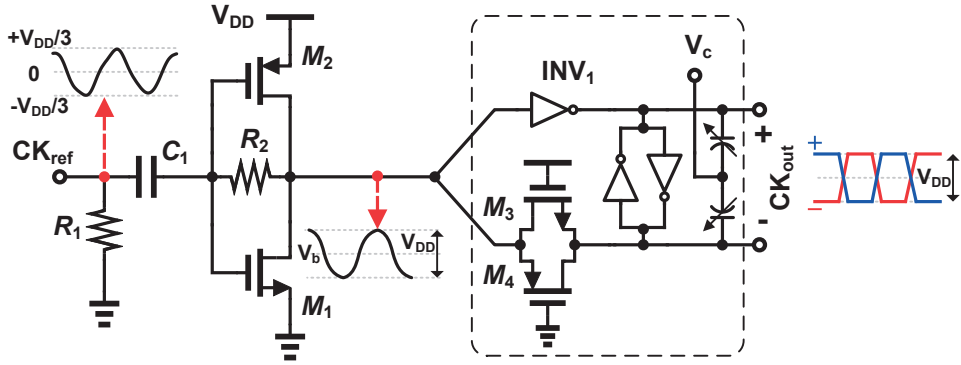
Figure 4.2: Input clock buffer and single-to-differential stage schematic.

4.2 MDLL Circuit Design

Fig. 4.1 shows the main building blocks of the proposed MDLL-based CDR unit. The input reference clock (i.e., CK_{ref}) is a single-ended signal that has a nominal frequency of 2.5 GHz and can vary within ±25% range, i.e., from 1.3 to 3.2 GHz. The forwarded clock should be amplified, converted to differential clock, delayed, and multiplied appropriately. Considering these criteria, the design of the required blocks is presented in this section.

4.2.1 Input Clock Buffer

A single-ended sinusoid signal is applied to the MDLL clock buffer with an amplitude around $V_{DD}/3$, which can be attenuated due to the long clock tree length. The clock buffer should convert this reference clock to a differential square-wave with sharp and rail-to-rail edges. Fig. 4.2 shows the proposed circuit for this block, which can properly operate in different process-voltage-temperature (PVT) corners. This circuit can generate a 50% square-wave from the sinusoidal input in PVT corners and prevents additional spur and jitter generation. The transistors M_1 and M_2 amplify the input clock and make it a rail-to-rail signal. The biasing point of the this resistive feedback amplifier is defined by the feedback loop that consists of M_1, M_2, and R_2. In the PVT corners the bias point, V_b in Fig. 4.2, can change and adapt itself to the transition voltage accordingly. Therefore, the succeeding stage receives a 50% duty cycle clock. The second stage in Fig. 4.2, marked with dashed line, is the single-ended-to-differential converter stage. A transmission gate, consisting of M_3 and M_4, is used to balance the skew between inverted and non-inverted clocks. The cross-coupled inverters couple the differential output signals together and keep the 50% clock in process corners. This block has an input for delay fine tuning, V_c in Fig. 4.2, which can properly delay the received forwarded clock within a 100 ps interval. The transistors are sized properly to provide a 20%-80% rise and fall time of 5 ps for the succeeding stages.
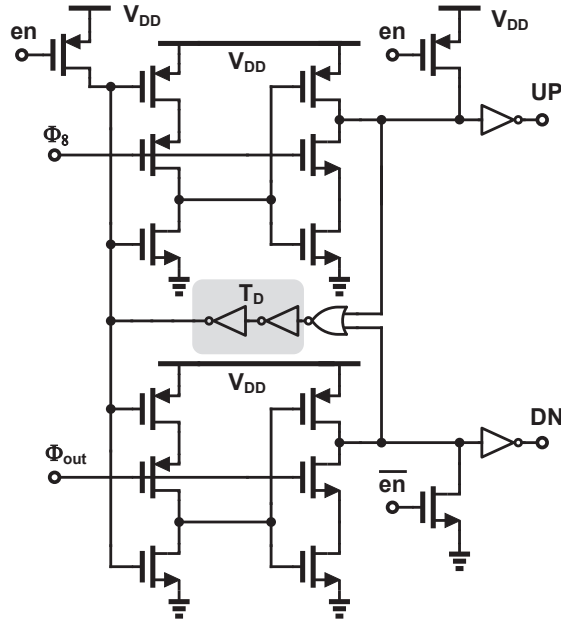
Figure 4.3:   The schemtic of the PFD circuit.

4.2.2   Phase-Frequency Detector (PFD)

In the MDLL block diagram, shown in Fig. 4.1, the DLL loop input (i.e., CK_{ref}) and output frequency (i.e., Φ_{1-8}) have the same value since the DLL loop just delays the input reference and does not generate new frequencies. Therefore, in theory it is possible to use a simple phase-detector instead of PFD, hence, use a simpler circuit. However, the phase detector needs to distinguish not only the absolute phase difference, but also the phase relationship (i.e., lag and lead phases) to remove the static phase error. Hence, in our application the PFD is preferred since it can detect the phase relationship and removes the finite static phase error more effectively [54], [55]. Fig. 4.3 presents the schematic of the PFD, which employs TSPC logic for high-speed operation. In this circuit, transistors $M_1 - M_3$ are used to initialize UP/DN signals such that in the starting point the DLL loop has the highest speed (i.e., the minimum line delay), thus, it can track the input phase by increasing the delay properly. The en signal in Fig. 4.3 is an active high signal and is low just in the beginning of lock process. This initialization helps the overall MDLL to have a better lock range and reaches a reasonable lock time in PVT corners [27].

In the PDF circuit, the static phase error between the PFD inputs, commonly referred as dead-zone, translates to spurious tones with the rate of F_{ref} in the lock condition. To alleviate this problem, a delay element can be added to the reset path of PFD circuit (shown in Fig. 4.4) for increasing both UP/DN pulse widths by the same amount of T_D and leave a sufficient time interval for the PFD to response. However, due to imperfection
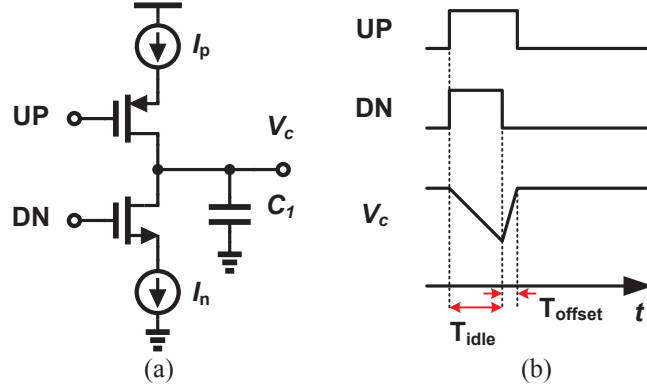
Figure 4.4: (a) CP conceptual schematic. (b) Effect of mismatch on the control voltage.

of the preceding charge pump (CP) circuit, the added delay should be kept as small as possible to minimize the undesired effects of circuit mismatch and random noise. More discussion and also an effective technique for reducing CP mismatch is given in next subsection.

4.2.3 Charge Pump (CP)

Fig. 4.4 (a) shows the conceptual schematic for a charge pump. The UP/DN signals generated by the PFD are used to switch the current sources (i.e., I_p and I_n) into the loop filter capacitor, i.e., C_1. During the idle interval in the lock condition, which is inevitable because of PFD response time, the switches S_1 and S_2 are commutating simultaneously. As a consequence, due to the transistor channel length modulation, an inevitable systematic mismatch between charging (discharging) current is induced into the CP circuit. This non-ideality causes the loop capacitor to be charged (discharged) during the idle interval and forces the overall DLL loop to compensate the introduced mismatch with a static phase error on the recovered clock, i.e., Φ_{out} in Fig. 4.3. The static delay can be calculated as

$$T_{offset} = \frac{\Delta I \cdot T_{idle}}{(I_n + I_p)/2} \tag{4.1}$$

where T_{offset} and T_{idle} are the static time offset and idle time, respectively, shown in Fig. 4.4(b). In (4.1) the $\Delta I/(I_n+I_p)$ ratio is constant regardless of absolute $I_{p,n}$ values [55], and it can be in order of 10% for deep sub-micron technologies. The conventional cascoding techniques for decreasing the channel length modulation are not applicable here due to limited core voltage headroom, i.e., 0.9 V in 40 nm technology. Likewise, due to the variation of the control voltage (i.e., V_c) in different PVT corners, the jitter performance

Figure 4.5:   Proposed CP schematic with reduced mismatch.

of the DLL can be exacerbated.

The voltage ripple on V_c causes spurious tones at F_{ref}, which translates to deterministic jitter (DJ) as [56]

$$\text{DJ}_{\text{out}} = \frac{2}{\pi}\text{T}_{\text{OUT}} \times 10^{\text{Spur(dBc)}/20} \tag{4.2}$$

where DJ_{out} is peak-to-peak induced DJ, T_{OUT} is the period of the output clock, and Spur(dBc) is the relative power difference between the output clock and the spurious tone. To reduce this unfavorable effect in low-voltage regime, the CP in Fig. 4.5 is proposed. In this circuit, M_3, M_4, and the NAND gate perform the mismatch reduction function. When only one of the UP and DN signals is high, M_3 and M_4 are off and the circuit does its normal operation to charge or discharge C_1. When both UP and DN signals are high at the same time, which means the idle interval, the NAND gate turns on both M_3 and M_4 and forces the node voltages X and Y to V_{DD}. As a result, M_8 and M_{10} turn off and the output stage stop charging (discharging) the loop filter capacitor. This can effectively reduce the ripple caused by CP mismatch on the VCDL control voltage. The reduced static delay can be calculated as

$$T_{\text{offset,new}} = \frac{T_{\text{comp}}}{T_{\text{idle}}} \cdot T_{\text{offset}} \tag{4.3}$$

where T_{idle} is the idle interval, T_{comp} is the compensating circuit response time, and T_{offset} is the static offset before compensation. The ratio of $(T_{\text{comp}}/T_{\text{idle}})$ can be in the

Figure 4.6: (a) Schematic of the VCDL. (b) Schematic of the D-cell.

order of 4 to 5, which indeed reduces the static offset, thus, the jitter performance can be improved. The Simulation result shows that turning on the mismatch compensation circuit (highlighted in Fig. 4.5) can reduce the spurs at F_{ref} from -21 dBc to -33 dBc, which translates to 7 ps_{pp} jitter reduction for 6 GHz output.

4.2.4 Voltgae-Controlled Delay Line (VCDL)

4.2.4.1 Delay cell (D-cell)

To double the input clock frequency and generate differential I/Q clocks at $2 \times F_{ref}$, 8 different phases at F_{ref} are required. This can be realized by 4 differential delay cells (D-cells), as shown in Fig. 4.6 (a). In this circuit, the symmetry between the core D-cells is the key point to guarantee the desirable performance of the MDLL in PVT corners, thus, prevent static phase error. Hence, the input clock, coming from the clock buffer shown in Fig. 4.2, first goes through the D_1 to generate a differential reference that has the same loading as the other outputs. In this circuit D_6 is also used to keep the symmetry between the core D-cells. This ensures identical loading on all the outputs and improves matching.

Figure 4.7: (a) Schematic of the proposed V-I converter. (b) D-cell tunning curve using the proposed V-I convertor.

The D-cells employ differential current starved push-pull topology as shown in Fig. 4.6 (b). In this circuit, the current of M_1-M_4 is adjusted by the current source transistors, M_5-M_8, whereas the cross-coupled inverters pairs the quasi-differential output signals and play as a symmetrizer, thereby improving the duty cycle.

4.2.4.2   V-to-I converter

In the D-cell circuit, shown in Fig. 4.6 (b), mismatch is dominated by tail current transistors, M_{5-8}, since the mismatch of the inverter devices is degenerated by the output resistance of the tail devices. The currents of $M_{5,6}$ should well match to those of $M_{7,8}$ to prevent systematic mismatch as well. In order to improve the matching and provide sufficient current to facilitate fast lock at 2.5 GHz, tail devices should operate in strong inversion regime. Therefore, low-voltage cascode current mirror topology is proposed in Fig. 4.7 (a) as bias circuit to provide sufficient current matching. In this circuit, R_1 and R_2 are degeneration resistors, which reduce the corner variation and improve the linearity of the input differential pairs, i.e., M_1 and M_2. Moreover, C_1 and C_2 (65 fF MOS capacitor at $V_{GS} = 0.5\,V$) can filter the noise generated by V-to-I converter and reduce the jitter. Fig. 4.7 (b) illustrates the D-cell tunning curve in different PVT corners using the V-I converter of Fig. 4.7 (a). Sizing the transistors properly, the delay can be adjust within the range of 30-60 ps in all PVT corners, hence, the DLL locking condition is guaranteed.

Figure 4.8: (a) Edge combiner circuit. (b) Symmetrical NAND gate.

4.2.4.3 Edge combiner

The edge combiner circuit shown in Fig. 4.8 (a), is implemented by exclusive addition (XOR) of consecutive phases. The edge combiner should have matched loading effect on all its inputs to avoid additional jitter on the outputs. The NAND gates are designed fully symmetrical to meet this requirement as shown in Fig. 4.8 (b).

4.2.5 Loop Filter Design

The proposed MDLL (shown in Fig. 4.1) is a type-I DLL, and the loop filter consists of capacitor C_1 that is connected to the CP output. Although the DLL loop can be fairly modeled in the s-domain [1] (i.e., continuous-time domain) the system should be modeled in the discrete-time domain for analyzing the loop behavior and stability more precisely [57, 58]. This can provide a better insight in the DLL dynamic, hence, prevents undesired long settling-time or unwanted oscillation, especially, in PVT corners. Fig. 4.9 (a) represents the closed-loop discrete-time model for analyzing the DLL dynamic behavior [57]. Based on this model, the phase transfer function (i.e., $\Phi_{\text{out}}/\Phi_{\text{in}}$) can be expressed as

$$\frac{\Phi_{\text{out}}}{\Phi_{\text{in}}} = \frac{K_{\text{CP}} \cdot K_{\text{VCDL}}}{1 - (1 - K_{\text{CP}} \cdot K_{\text{VCDL}})z^{-1}} \tag{4.4}$$

where $K_{\text{CP}} = I_{\text{CP}}/C_1$ is the CP gain assuming $I_{\text{p}} = I_{\text{n}} = I_{\text{CP}}$, and K_{VCDL} represents the linearized VCDL gain around the VCDL operating control voltage. The transfer function in (4.4) contains a pole at $(1 - K_{\text{CP}}K_{\text{VCDL}})$, thus, the open-loop gain needs to meet the

---

[1]This estimation is only correct if the DLL loop bandwidth is much narrower than the input reference frequency.
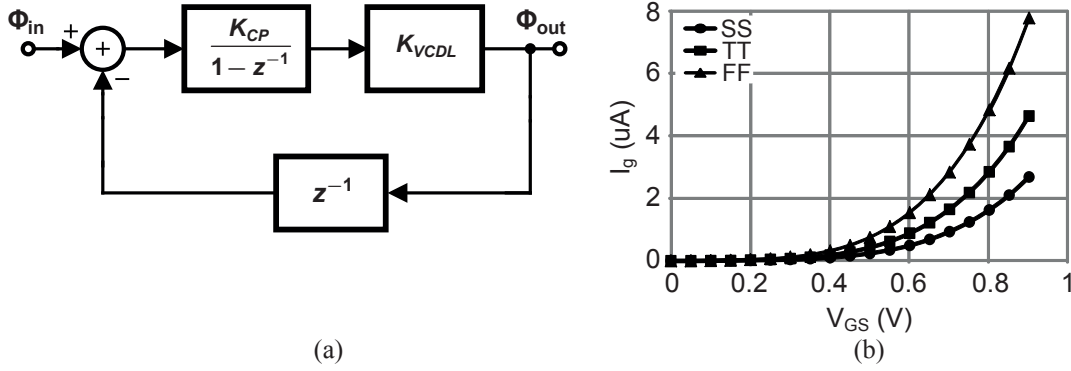
Figure 4.9: (a) DLL discrete-time model. (b) Gate leakage current for 0.6 pF MOS capacitor in 40 nm.

following constraint in the all PVT corners to guarantee the loop stability [58]

$$0 \leq K_{\mathrm{CP}} \cdot K_{\mathrm{VCDL}} \leq 2. \tag{4.5}$$

Likewise, the minimum loop gain (i.e., $K_{\mathrm{CP}} \cdot K_{\mathrm{VCDL}}$) to ensure that the DLL loop settles within a n/F_{ref} time interval by a 99% accuracy, can be calculated as [59]

$$K_{\mathrm{CP}} \cdot K_{\mathrm{VCDL}} = 1 - \exp\left(\frac{1}{n+1}\ln(0.01)\right). \tag{4.6}$$

Replacing n by 20 in (4.6) to yield a maximum 8 ns lock-time, the loop gain can be estimated as

$$K_{\mathrm{CP}} \cdot K_{\mathrm{VCDL}} = 0.197 . \tag{4.7}$$

The estimated loop gain in (4.7) satisfies (4.5), thereby, the DLL remains stable in the PVT corners. Having (4.7), the value of the loop filter capacitor (i.e., C_1 in Fig. 4.1) should be calculated with the worsen design parameters in the PVT corners. In the FF corner, $I_{\mathrm{CP}} \approx 400~\mu\mathrm{A}$, and $K_{\mathrm{VCDL}} \approx 0.5$ ns/V, hence, $C_1 \approx 1$ pF. This quite large capacitor can be realized either by a MOS capacitor, or by a metal-oxide-metal capacitor (MOM capacitor). Although the former offers an efficient die area, it is not used in our design due to gate leakage issue in deep sub-micron regime. The MOS capacitor gate leakage current in 40 nm CMOS technology is depicted in Fig. 4.9 (b) for a $60\mu m/0.5\mu m$ low-voltage n-type device (600 fF at $V_{\mathrm{GS}} = 0.6$). This current can discharge the loop capacitor and introduces undesired voltage ripple on the VCDL control voltage. Therefore, the MOM capacitor is employed in the loop filter, which occupies a $20 \times 14~\mu m^2$ die area using inter-digitated MOM capacitor structure. Applying all available metal layers (i.e., M_{1-8}) in the MOM capacitor, the occupied die area is comparable to the MOS capacitor counterpart.
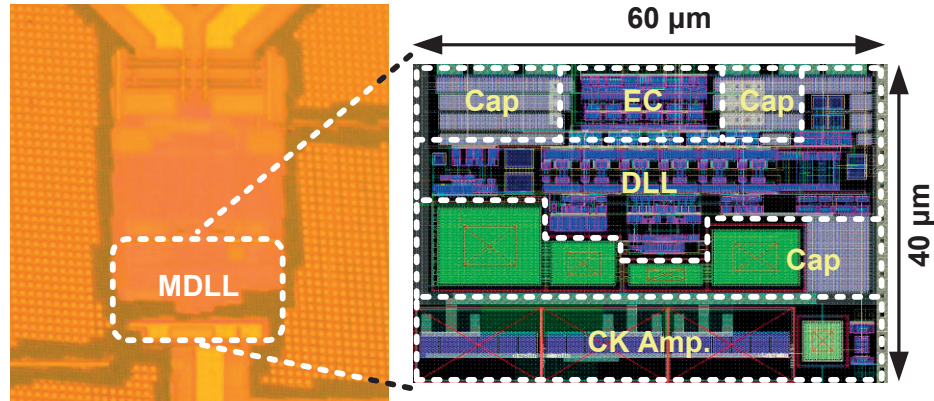
Figure 4.10: Micrograph and layout of the test chip.

(a)

(b)
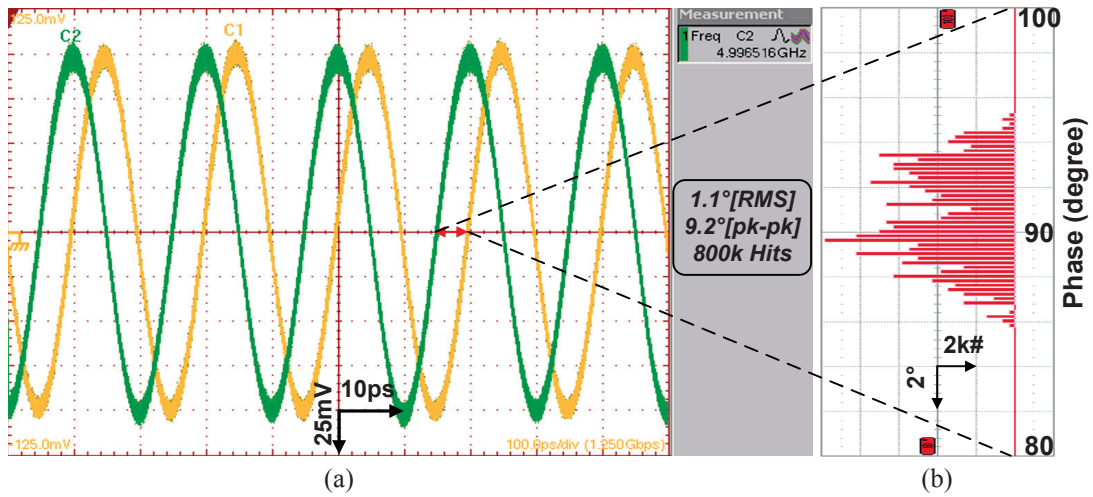
Figure 4.11: (a) Measured I/Q clocks at 5 GHz output. (b) Measured long-term I/Q phase mismatch at 5 GHz output.

4.3 Measurement results

The proposed MDLL is designed and fabricated in 40 nm bulk CMOS technology. Fig. 4.10 shows the die micrograph of this circuit. The core occupies $60 \times 40 \ \mu m^2$ silicon area while 25% of this area is used for loop-filter capacitor. The quadrature I/Q clocks at 5 GHz are shown in Fig. 4.11 (a). The measured phase mismatch over 800 k hits, shown in Fig. 4.11 (b), is 9.2° peak-to-peak.

The jitter accumulation is investigated by measuring long-term jitter. Fig. 4.12 (a) shows the measured jitter histogram at 6 GHz output frequency. The output jitter is about 1.3 ps$_{rms}$ and 13.3 ps$_{pp}$ over 800 k hits.

The measured peak-to-peak jitter degradation due to external supply noise, calculated

(a)   (b)
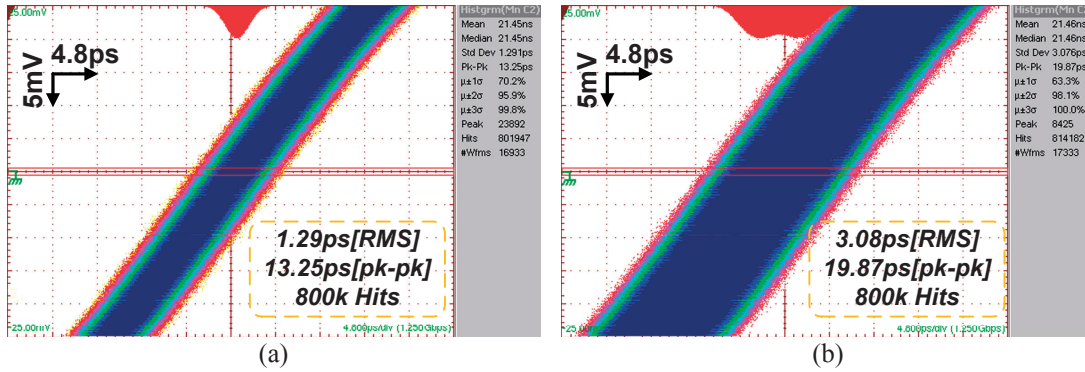
Figure 4.12: (a) Measured long-term jitter histogram at 6 GHz MDLL output. (b) Measured long-term jitter histogram at 6 GHz MDLL output with 200 mV$_{pp}$ external supply noise at 250 MHz (worst case) noise frequency.
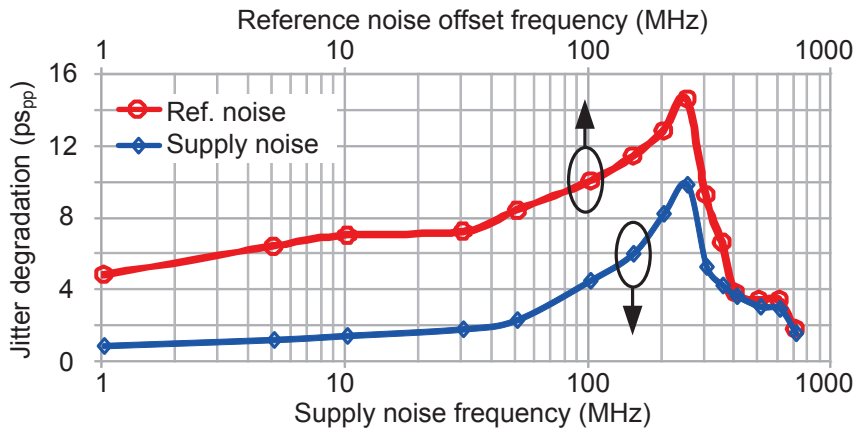
Figure 4.13: Measured peak-to-peak jitter degradation versus supply noise and reference offset noise frequency for 6 GHz output. The supply has 200 mV$_{pp}$ sinusoidal noise. The reference clock has -28 dBc single-tone sideband.

by subtracting the jitter in absence of supply noise, is shown in Fig. 4.13. A 200 mV$_{pp}$ sinusoidal signal is added to MDLL supply and the noise frequency is swept from 1 MHz to 700 MHz. The maximum jitter degradation is 6.6 ps at 250 MHz noise frequency resulting in the supply noise sensitivity of 33 fs/mV. Fig. 4.12 (b) shows the jitter histogram at 6 GHz output in the worst case noise frequency, i.e., 250 MHz.

By adding a single tone spur to the phase of the reference clock (i.e. single-tone sideband with -28 dBc relative magnitude on the reference clock) and sweeping its frequency from 1 MHz to 700 MHz, the jitter transfer characteristics of the circuit is measured in Fig. 4.13. It shows the peaking of the jitter transfer function occurs at 250 MHz offset frequency. Fig. 4.11 (a) shows the measured phase noise at 6 GHz output frequency. The measured

PHASE NOISE					
	Settings		Residual Noise		Spot Noise [T1]	
Signal Freq:	5.999963 GHz	Evaluation from 100 kHz	to 3 GHz	100 kHz	-80.61 dBc/Hz
Signal Level:	-11.19 dBm	Residual PM	3.184 °	1 MHz	-105.93 dBc/Hz
Signal Freq Δ:△	70.33 Hz	Residual FM	17.443 MHz	10 MHz	-117.05 dBc/Hz
Signal Level Δ: △	-0.04 dBm	RMS Jitter	1.1739 ps	300 MHz	-116.84 dBc/Hz
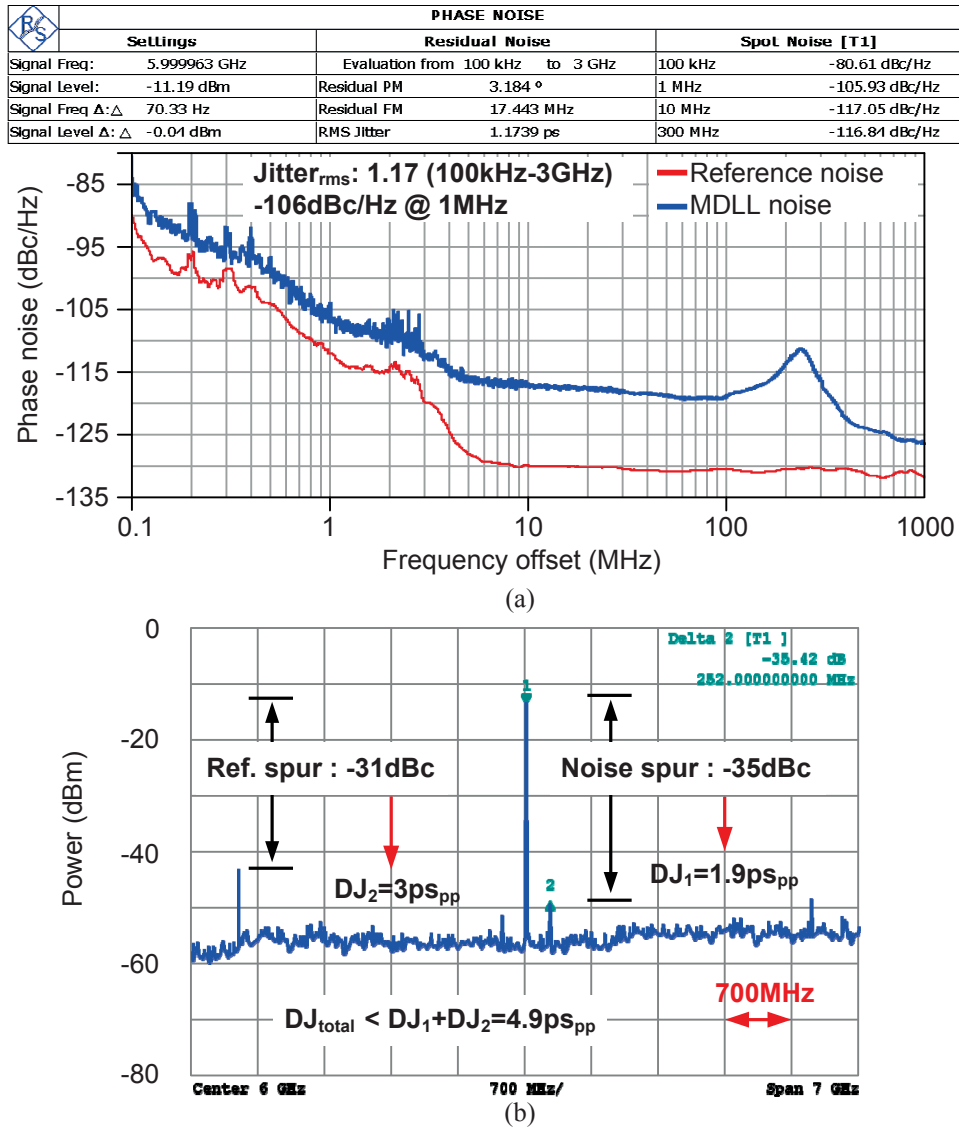
Figure 4.14: (a) Measured phase noise at 6 GHz output. (b) Measured MDLL reference and spurs with 200 mV$_{pp}$ supply noise at jitter-peaking frequency.

phase noise at 1 MHz and 250 MHz offset is nearly -106 dBc/Hz and -105 dBc/Hz, respectively. It is interesting to note that phase noise also shows a peaking at 250 MHz, very similar to the results shown in Fig. 4.13. For measuring the effect of jitter peaking on the deterministic jitter (DJ) generation, a 250 MHz sinusoidal signal with 200 mV$_{pp}$ is added to MDLL supply and the measured spectrum is shown in Fig. 4.14(b). The reference spur and the noise spur is -31 dB and -35 dB which translates to 2.9 ps (DJ$_2$) and 1.9 ps (DJ$_1$) deterministic jitter, respectively, using (4.2). Having DJ$_{total}$ < DJ$_1$ + DJ$_2$ [56], this measurement shows that the maximum DJ remains under 5 ps, which is sufficient for

Table 4.1: Comparison of MDLL performance for frequency generation.

Ref.	[56]	[60]	[61]	This Work
Technology	0.13 μm CMOS	90 nm CMOS	90 nm CMOS	40 nm CMOS
Supply (V)	1.1	1.0	1.2	0.9
Power (mW/GHz)	0.6	1.125	3.7	0.28[b]
F_{ref} (GHz)	0.375	2~5	0.225~0.9	1.3~3.2
F_{out} (GHz)	1.5	40	0.45~5.4	2.6~6.4
Multiplying Factor	4	9	2, 3, 6	2
Jitter RMS/PP (ps)	0.9/9.2	0.87/7.56[a]	NA	1.3/13.25[b]
Supply Sen. (fs/mV)	20	NA	NA	33
Active area (mm^2)	0.25	0.122	0.04	0.0024

[a] For 5 GHz input.
[b] For 6 GHz output.

source-synchronous serial link applications [24].

The power consumption of the core system is 1.1-1.8 mW for the output frequency range of 2.6-6.4 GHz. All measurement results are in good agreement with simulation results and in general satisfy the specification requirement of the system. Table 4.1 compares the measured performance of the fabricated DLL-based frequency multiplier with some published works.

4.4   Conclusion

This chapter presents the design and implementation of a DLL-based frequency multiplier circuit in 40 nm bulk CMOS. The proposed circuit adequately reduces the complexity and power dissipation of CDR unit in wireline transceivers, while satisfying the required jitter and phase mismatch specifications. New strategies are proposed to satisfy these specifications, while they fulfill the stringent power consumption requirements in wireline links. The RMS jitter remains below 3 ps over the entire input frequency range. A low-voltage technique is proposed to improve the mismatch effect in CP circuit and reduces the deterministic jitter. Based on the measurement results, the power consumption does not exceed 1.8 mW over the entire input frequency range results in 280 fJ energy consumption for 6 GHz output.

5 Hybrid NRZ/MT Signaling for Controlling ISI and Crosstalk in Dense Interconnects

This Chapter studies the properties of multi-tone signaling for controlling the effect of crosstalk in high-density and compact links constructed using low-cost material such as FR-4. As the distance between the lanes has to diminish in order to allow for more density, crosstalk turns out to have more and more severe effects on performance of the system. We will exploit the properties of multi-tone signaling, especially orthogonality amongst different sub-bands, to reduce the effect of crosstalk. A four-channel transceiver has been implemented in a standard CMOS 40 nm technology in order to demonstrate the performance of NRZ/MT signaling in presence of high channel loss and strong crosstalk [26].

To further study NRZ/multi-tone (NRZ/MT) signaling and improve the data rate in dense memory interconnects, first, we have implemented four closely spaced transceivers on each die. Likewise, the circuit design of some key building-blocks have been modified in order to improve the performance, and provide 20% higher date rate per pin. Moreover, the crosstalk is studied and analyzed for the NRZ/MT signaling and the silicon results proved its efficiency of the proposed scheme in controlling the crosstalk induced noise.

Furthermore, the design flow and measurement results of a low-power 4-channel hybrid NRZ/MT transceiver for multi-drop bus (MDB) memory interfaces in 40 nm CMOS technology has been presented in this Chapter. The proposed system achieves 1 pJ/bit power efficiency, while communicating over an MDB channel with 45 dB loss at 3 GHz. The multi-tone (MT) nature of the proposed transceiver helps to control the intersymbol interference (ISI) and reduce the far-end crosstalk (FEXT), which results in a very

energy-efficient implementation. The core size area is $80 \times 60 \ \mu m^2$ and $130 \times 60 \ \mu m^2$ for the TX and RX blocks (including the clock unit), respectively.

The remainder of this Chapter is organized as follows. Section 5.1 studies the performance of NRZ/MT signaling in presence of channel loss and far-end crosstalk (FEXT). Sections 5.2 and 5.3 explain the system-level and circuit-level techniques for realizing an 9 Gb/s/lane mixed NRZ/MT serial data transceiver, respectively. Section 5.4 presents the experimental data for the proposed multi-channel transceiver operating at aggregated 36 Gb/s data rate over a multi-drop bus (MDB) channel, and demonstrates the efficiency of the proposed ISI/FEXT reduction schemes at low energy cost. Section 5.5 summarizes this Chapter.

5.1   Analysis of ISI and FEXT for BB and NRZ/MT Signaling

The challenges in design of high data rate links for memory interfaces in presence of ISI and FEXT are studied in this section. Meanwhile, it is shown how NRZ/MT signaling can help to control and reduce the effect of these types of imperfections.

5.1.1   Signal Integrity in Dense Interconnects: Introduction

Overcoming the limitations of data rate and power efficiency in wireline serial data transceivers, data communication have emerged as some of the major challenges to improve speed and performance in modern computing systems. While industry continues the demand for higher data transfer speed over low-cost, high-loss channels, more enhanced communication and circuit techniques are needed to satisfy the required specifications. Moving toward higher data rates over denser communication channels exacerbates both crosstalk and intersymbol interference (ISI). As a consequence, modern serial data transceivers are equipped with very sophisticated equalizers and crosstalk cancellation units [62, 63, 64, 65], which in return increase system complexity and energy consumption. Therefore, due to the power overhead that these techniques add to the transceiver, they could not adapt well to the I/O systems where the power efficiency is the main concern [66]. To alleviate the design challenges and implement a low-power link, more advanced signaling methods can be employed [12, 26, 11, 25, 67, 68, 69]. As shown in [24], hybrid NRZ/multi-tone (MT) signaling can be used to relax the equalization requirements and implement a very energy efficient transceiver. In this signaling method, the spectrum of the transmitted signal has been shaped such that energy loss due to frequency domain notches of the channel is minimized. Therefore, simple continuous-time linear equalization (CTLE) is sufficient to reconstruct the received signal and achieve 1 pJ/b link energy efficiency.
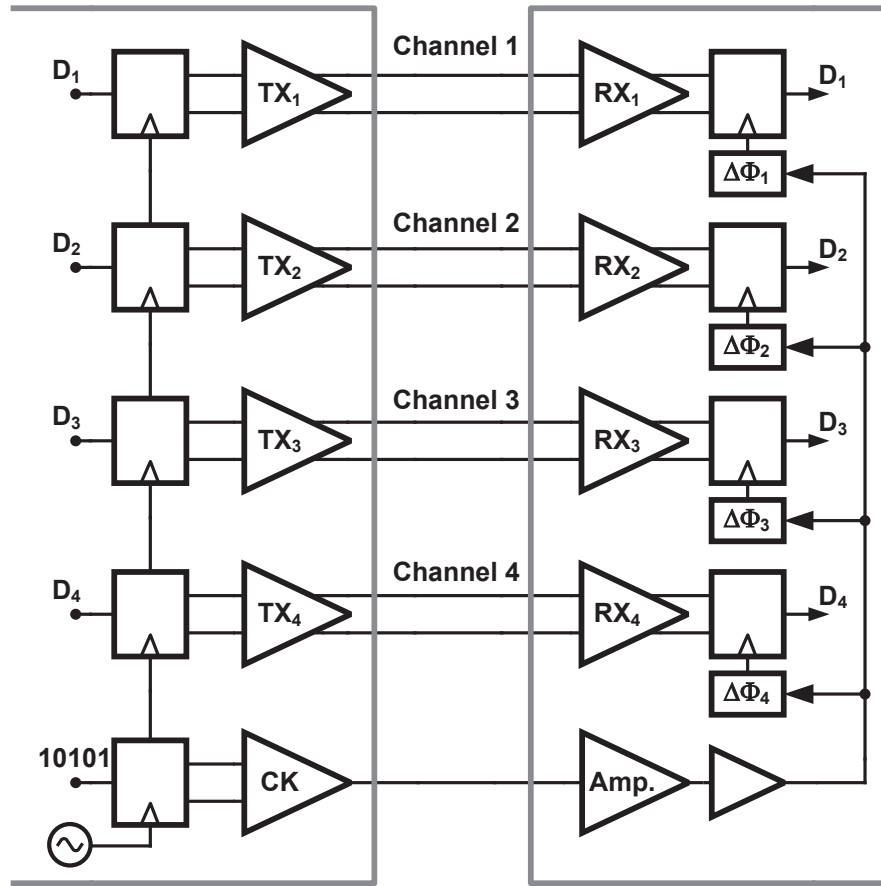
Figure 5.1: Overall block diagram of the 4-channel TRX.

5.1.2 Channel Configuration and BB signaling

The block diagram of the 4-channel transceiver (TRX) arrangement to be studied in this work is shown in Fig. 5.1, with four identical TX/RX pairs implemented side-by-side, in close proximity. The source-synchronous architecture is employed for this wireline interface.

Fig. 5.2 (a) shows a stylized view of the differential parallel multi-lane channel, which is used in our link design. Fabricated on FR-4 substrate, this memory interface consists of four differential lanes in total, each with 30 cm length and 3 mm width, and with the channel spacing of W=3 mm within and between the bundles. Moreover, dual-in-line memory module (DIMM) is employed for communicating between the memory controller and DRAMs. Fig. 5.2 (b) shows the simplified block diagram of a DIMM interface where the controller is writing to one of the DRAMs on the $Rank_1$. Here, while the controller communicates to $DRAM_5$, the electrical length-differences between the controller and

(a)

(b)
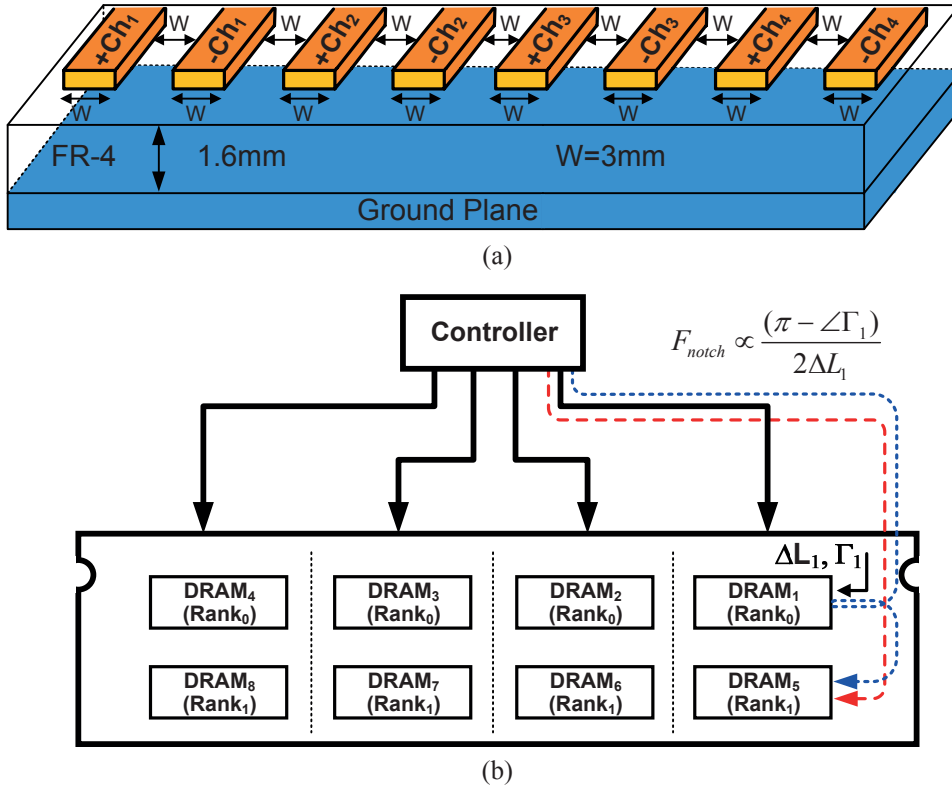
Figure 5.2: (a) Stylized view of the 4 differential channels, side-by-side. (b) Simplified block diagram of a DIMM interface showing the multi-path fading.

the DRAM paths (i.e., ΔL_1), and the phase shift, caused by Γ_1, lead to multi-path reflections [41]. These can cause destructive superposition at certain frequencies and create notches in the channel frequency response. Employing NRZ signaling, the received power spectrum in the absence of aggressor transmitters can be expressed as [43]

$$S_{\text{in}}(\omega) = T_{\text{b}}|H(\omega)|^2 \left[\frac{\sin\left(\frac{\omega T_{\text{b}}}{2}\right)}{\left(\frac{\omega T_{\text{b}}}{2}\right)} \right]^2 \tag{5.1}$$

where T_{b} is the bit period, and $H(\omega)$ is the channel frequency response. This equation shows that 90% of the received power is located below $\omega = 2\pi/T_{\text{b}}$ and 77% of which is below the Nyquist rate, i.e., $\omega = \pi/T_{\text{b}}$. Hence, if $H(\omega)$ bears a notch below the Nyquist rate a significant part of the transmitted energy will be wasted and the equalization will be challenging.

When the aggressor NRZ signal is transmitted on closely spaced channels, there will be strong FEXT induced on the adjacent lanes. Assuming a low-impedance microstrip line of Fig. 5.2 (a), the inductive coupling is dominant and the crosstalk transfer function
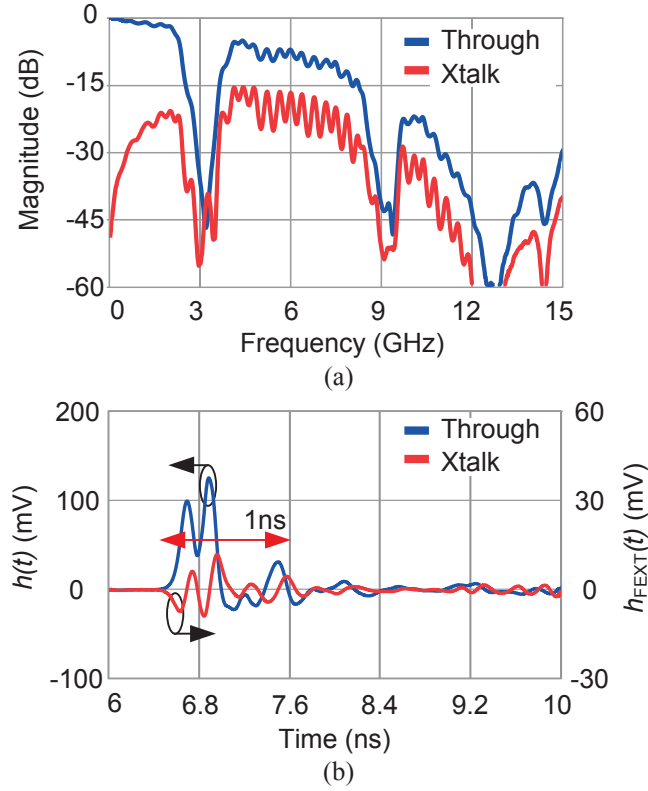
Figure 5.3: (a) Measured channel frequency response. (b) Measured channel 9 Gb/s single-bit pulse response.

is proportional to the derivative of the main channel transfer function [70]. Therefore, the power spectrum of the FEXT coupled to an adjacent differential channel can be calculated as

$$S_{\text{FEXT}}(\omega) = \beta \tau_{\text{f}}^2 \omega^2 \times S_{\text{in}}(\omega) \tag{5.2}$$

where τ_{f} is the forward coupling time constant, and the value of β, which depends on the board type, is between $1/2$ and $1/3$ for the differential channels [65]. Fig. 5.3 (a) shows the measured channel frequency response. The through response shows multiple notches at 3 and 9 GHz, while the crosstalk frequency response is fairly proportional to the derivative of the main channel response and it demonstrates multi-drop nature. From the time domain point of view, the multi-drop frequency characteristic leads to a long tail pulse response. Fig. 5.3 (b) presents the measured 9 Gb/s pulse response for the through and crosstalk transfer functions. Both demonstrate about 1 ns long tail pulse responses. Therefore, the equalization task can be quite challenging for a conventional NRZ-based transceiver.
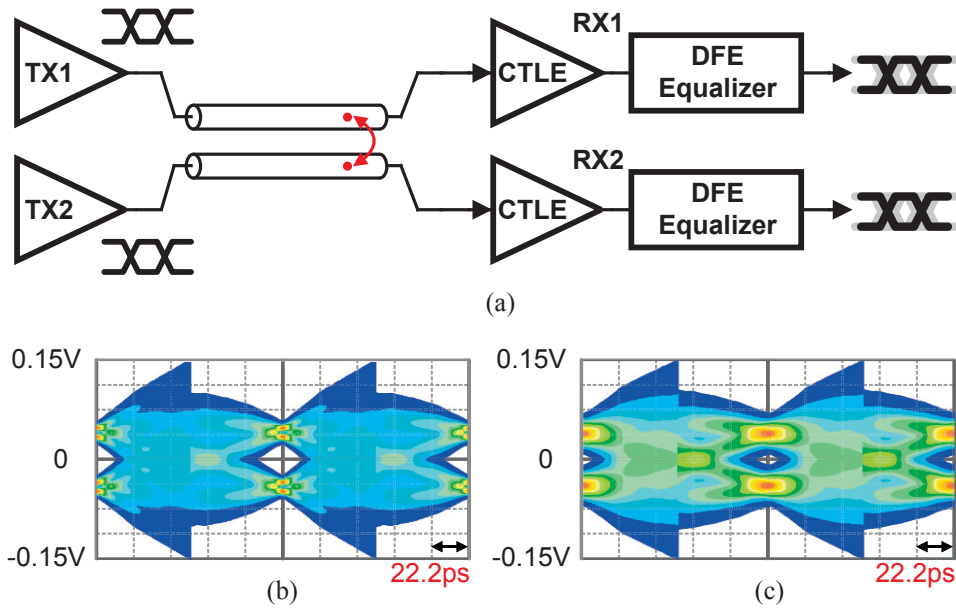
Figure 5.4: (a) Conventional BB transceiver block diagram for communicating at 9 Gb/s over MDB interface. System-level channel simulation eye diagrams for: (b) without, (c) with crosstalk, both after optimizing the CTLE and DFE blocks.

To illustrate the complexity of designing a traditional BB serial data transceiver for a MDB memory interface, a conventional BB transceiver is modeled and simulated for communicating at 9 Gb/s over the channel, which its frequency response is shown in Fig. 5.3 (a). The block diagram of the BB transceiver used in the system-level simulation is presented in Fig. 5.4 (a). The transmitter employs NRZ signaling and is assumed to have 700 fs$_{rms}$ output jitter. The receiver employs CTLE and decision-feedback equalizer (DFE) for data equalization, and both are considered to be ideal blocks without random noise. Fig. 5.4 (b) represents the equalized eye diagram on the RX side when there is no aggressor present on the TX side. The statistical simulation shows that using the conventional receiver architecture of Fig. 5.4 (a), a DFE equalizer with about 15 taps is needed to equalize the effects of the notches and achieve 8% of UI, UI = 111 ps, eye-opening, at a bit error rate (BER) of 10^{-12}. However, adding one aggressor TX to this simulation causes a complete eye closure at BER = 10^{-12}, as shown in Fig. 5.4 (c). Hence, to equalize this link at 9 Gb/s, either advanced techniques should be employed (e.g., XDFE [9], XCTLE [65]), to reduce crosstalk, or the PCB should be redesigned to have more spacing between the lanes, hence, exhibit less crosstalk. Both approaches impose higher cost and make the link design more challenging.

(a)

(b)
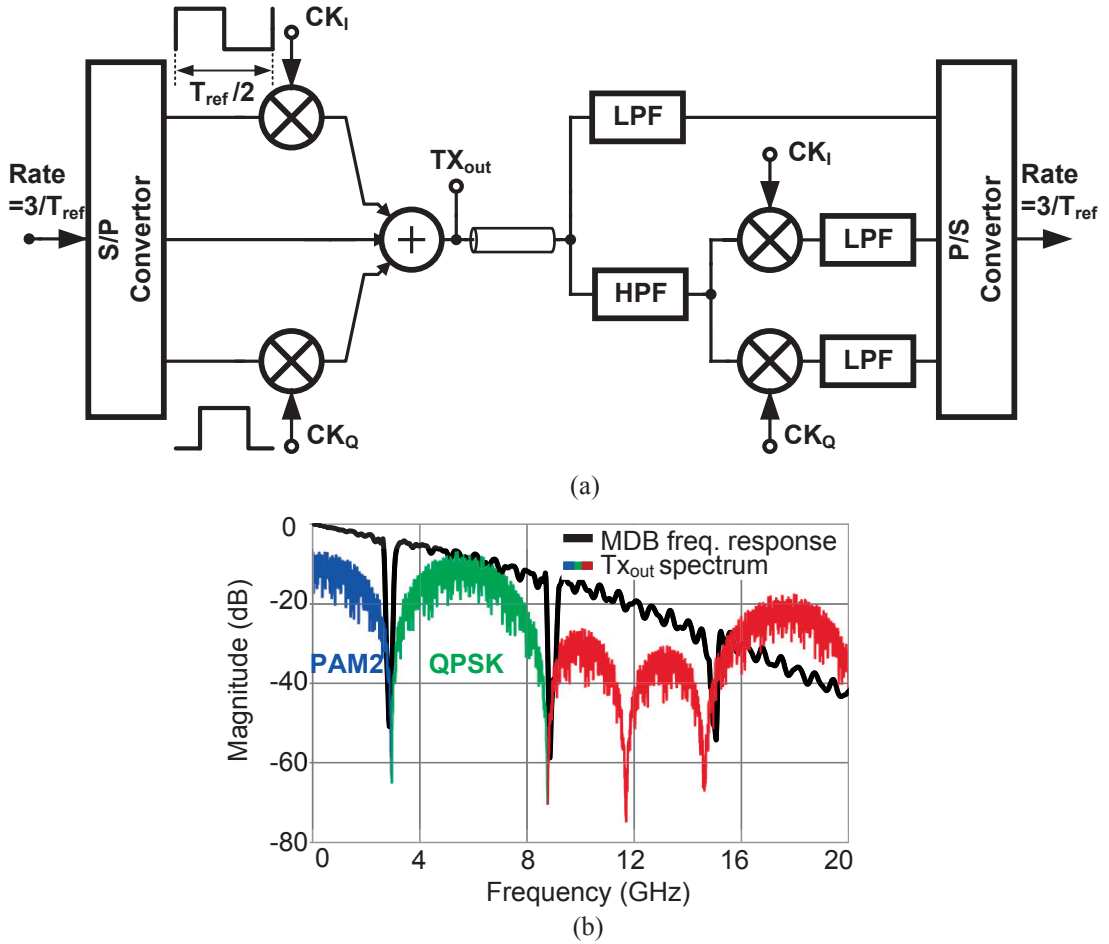
Figure 5.5: (a) Hybrid NRZ/MT transceiver architecture. (b) Output TX spectrum when $F_{ref} = 3$ GHz.

5.1.3   Hybrid NRZ/MT Signaling for Controlling ISI and FEXT

A new Hybrid NRZ/MT architecture suitable for high-speed multi-drop links has been recently proposed in [71, 24]. Employing this modulation scheme has several advantages for controlling ISI. Here we show that this signaling method can also be very useful to reduce the effect of FEXT in high-dense interconnects. Without losing generality, Fig. 5.5 (a) demonstrates the simplified system block diagram that consists of three orthogonal sub-bands. Suppose the input data is constructed from three different data streams each operates at F_{ref} bit rate. Each sub-stream is consequently modulated to its respective carrier frequency and the combined signal is sent over the line. The output spectrum of the TX along with a MDB interface frequency response is presented in Fig. 5.5 (b). Here, the lower-frequency band of the channel, from DC to the first notch (i.e.
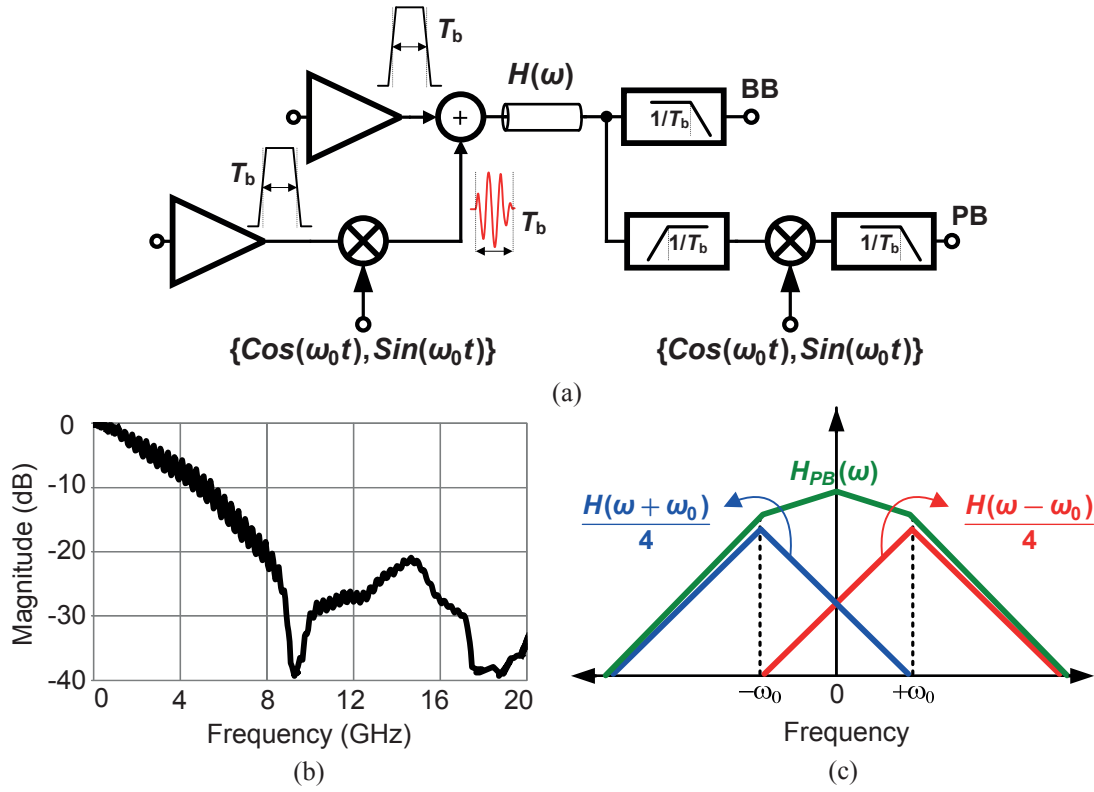
Figure 5.6: (a) Hybrid NRZ/MT simplified block diagram. (b) The channel frequency response used in C2C communications. (c) PB channel construction.

0-3 GHz), is used for transmitting up to 3 Gb/s NRZ data and constitutes the PAM2[1] part of the spectrum. Moreover, the upper-frequency band of the channel, between two notches (i.e. 3-9 GHz), is exploited for transmitting 6 Gb/s data in the quadrature-phase shift-keying (QPSK) format. This sub-band carries 3 Gb/s data on each of the in-phase (I) and quadrature-phase (Q) content of the spectrum.

5.1.3.1   ISI Controlling Analysis

Applying NRZ/MT signaling can efficiently reduce the ISI since each of the sub-band experiences less loss at its corresponding Nyquist frequency. For the MDB interfaces, avoiding channel frequency notches by employing a proper modulation scheme can prevent bit-energy waste around the notches, as shown in Fig. 5.5 (b), and reduces the equalization circuit complexity. However, the potential of the proposed signaling scheme of Fig. 5.5 (a) is not limited to the MDB channels and it can equally be employed for lossy backplane and chip-to-chip (C2C) communications.

---

[1]Generally speaking, it can be any kind of PAM-N, ENRZ, or doubinary baseband signaling.
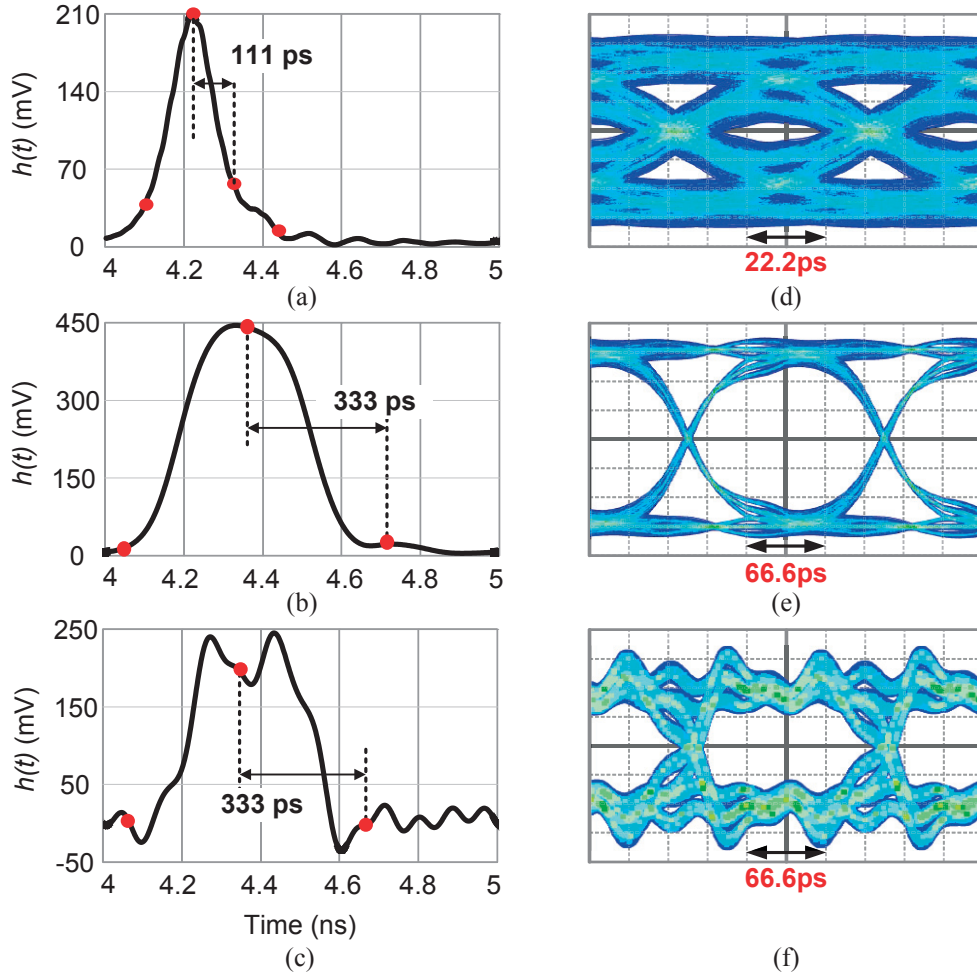
Figure 5.7: (a) 9 Gb/s single-bit pulse response for the C2C channel. (a), (b) BB and PB 3 Gb/s single-bit pulse response. (c) The eye diagram for 9 Gb/s NRZ signaling. (d), (e) BB and PB eye diagram for aggregate data rate of 9 Gb/s.

Fig. 5.6 (a) shows a simplified system block diagram for in-band ISI analysis. The channel is designed for C2C communication, and it has 40 cm length with the frequency response shown in Fig. 5.6 (b). Here, the bit period for each of the sub-bands is T_b, therefore, for BB sub-band the channel loss at the Nyquist rate is $\left|H(\omega = \frac{\pi}{T_b})\right|$. This is typically smaller than the channel loss at $\omega = 3 \times \frac{\pi}{T_b}$, thus, by parallelizing the input stream into three streams the ISI for BB sub-band is considerably mitigated. Considering passband (PB) sub-streams, the channel frequency response should be calculated after downconverting the signal and removing the interfering signals, using a low-pass filter, on the RX side. Then, the effective channel frequency response for the PB can be written as

$$H_{\text{PB}}(\omega) = \frac{1}{4}[H(\omega - \omega_0) + H(\omega + \omega_0)] \tag{5.3}$$

where ω_0 is the carrier frequency. In (5.3) it is assumed that the LPF in Fig. 5.6 (a) can
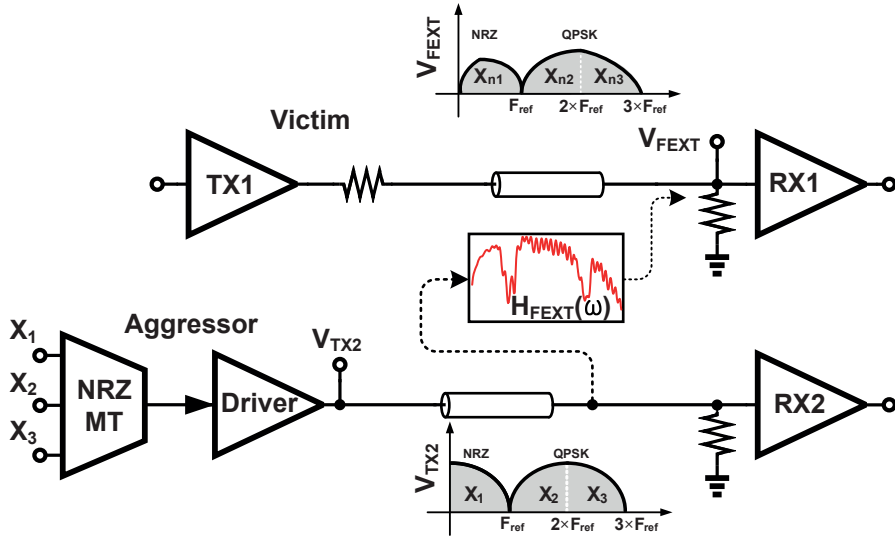
Figure 5.8: FEXT generation mechanism in hybrid NRZ/MT signaling.

efficiently remove all the frequency content around $2 \times \omega_0$. As (5.3) shows, the effective channel for PB is the superposition of shifted versions of the main channel frequency response. Fig. 5.6 (c) illustrates the construction of $H_{\text{PB}}(\omega)$ figuratively. Although the absolute channel loss is pronounced, the loss tilt from DC to $\omega = \pi/T_{\text{b}}$ is mitigated thanks to the averaging of the shifted versions of the channel. Hence, we can surmise that the ISI is consequently reduced.

To show ISI controlling property in time-domain, the single-bit pulse response over the reference channel, shown in Fig. 5.6 (b), is plotted for the conventional NRZ signaling, BB, and PB in Fig. 5.7 (a), (b), and (c), respectively, for $\omega_0 = 4\pi/T_{\text{b}}$. Comparing pre- and post-cursors in traditional NRZ signaling with mixed NRZ/MT one, we can conclude that the equalization complexity is reduced in hybrid NRZ/MT signaling, regardless of channel frequency shape. To evaluate the eye diagram that is generated from these pulse responses, a 9 Gb/s data stream is sent over this channel, using both conventional NRZ and NRZ/MT signaling, and the received data eye diagram is presented in Fig. 5.7 (d), (e), and (f) for conventional, BB, and PB, respectively. As expected, the horizontal and vertical eye-opening are better for the hybrid NRZ/MT signaling.

5.1.3.2 FEXT Controlling Analysis

Similar to any other signaling, transmitting mixed NRZ/MT signal induces a voltage noise, V_{FEXT}, into the neighboring lanes, as shown in Fig. 5.8. Assuming that $v_{\text{TX2}}(t) = x_1(t) + cos(\omega_0 t)x_2(t) + sin(\omega_0 t)x_3(t)$, the crosstalk noise for each of the sub-

band in the hybrid NRZ/MT transceiver, shown in Fig. 5.6 (a), can be calculated as

$$\overline{V_{\mathrm{FEXT,BB}}{}^2} = \int_0^{\omega_\mathrm{b}} S_{\mathrm{FEXT,X_1}}(\omega)d\omega \tag{5.4a}$$

$$\overline{V_{\mathrm{FEXT,I}}{}^2} = \int_0^{\omega_\mathrm{b}} [\cos^2(\theta)S_{\mathrm{FEXT,X_2}}(\omega) + \sin^2(\theta)S_{\mathrm{FEXT,X_3}}(\omega)]d\omega \tag{5.4b}$$

$$\overline{V_{\mathrm{FEXT,Q}}{}^2} = \int_0^{\omega_\mathrm{b}} [\sin^2(\theta)S_{\mathrm{FEXT,X_2}}(\omega) + \cos^2(\theta)S_{\mathrm{FEXT,X_3}}(\omega)]d\omega \tag{5.4c}$$

where $\omega_\mathrm{b} = 2\pi/T_\mathrm{b}$ is the sub-band bit rate, $S_{\mathrm{FEXT,X_K}}$ is the K-th sub-stream FEXT power spectrum given in (5.2), and θ is the phase shift between $H_{\mathrm{FEXT}}(\omega)$ and $H(\omega)$ and is roughly equal to -90° if the crosstalk is more inductive than capacitive.

As (5.4) shows, the FEXT voltage that is induced on the victim channel remains orthogonal as $H_{\mathrm{FEXT}}(\omega)$ does not change this property. Thus, in the victim receivers, the same downconverting/integrating process which is performed for recovering the main TX signal, can automatically cancel out the orthogonal aggressors. Hence, the inter-orthogonal sub-band conversion (IOSC) is reduced in the victim sub-band equalizer, and the effective crosstalk energy is equal to only one of the aggressor sub-bands, and two thirds of crosstalk energy is canceled. For NRZ signaling, as long as the $h_{\mathrm{FEXT}}(t)$ does not settle down to zero, the transmitted bits can convolve with the channel pulse response and they can induce voltage noise on the victim channel. However, in NRZ/MT signaling only one of the three sequences acts as the aggressor for the victim receiver. Therefore, effective V_{FEXT} is reduced for each sub-band RX, and $h_{\mathrm{FEXT}}(t)$ long tail will not cause severe crosstalk compared with the conventional NRZ signaling.

5.2   System Design Overview

In this Section, the system design of the proposed hybrid NRZ/MT transceiver for communicating over a 4-lane differential MDB interface at the aggregate data rate of 36 Gb/s is presented. The proposed hybrid NRZ/MT architecture for communicating over the MDB channel of Fig. 5.3 is presented in Fig. 5.5 (a). The random data is generated by three independent embedded PRBS15 generators, each operating at F_{ref}, i.e., 3 GHz. Two mixers upconvert two sets of random data into I and Q sub-bands to create the QPSK band. The local frequency is chosen to be $2 \times F_{\text{ref}}$. The third stream is added together with I / Q sub-bands by the output summer/driver circuit. There is no data around 3rd clock harmonic in this architecture, thus, we have avoided employing pulse-shaping filters for the baseband data to relax the linearity requirements on TX output driver [71]. Although pulse-shaping has not been employed the inter-channel interference (ICI) still leaves enough margin for error-free operation of the link. The main reason is that only 4.7% of spectrum energy is located between $\omega_{\text{b}} = 2\pi/T_{\text{b}}$ and $\omega_{\text{b}} = 4\pi/T_{\text{b}}$, as can be calculated by integrating the NRZ power spectrum, given in (5.1), in the desired bandwidth. From the linearity requirement point of view, QPSK modulation without pulse shaping does not require a linear output driver [45]. Hence, a current-mode output driver can appropriately add BB, I, and Q sub-bands together and construct the hybrid NRZ/MT output stream. Our system-level simulation shows that without baseband pulse-shaping, the eye diagram can provide up to 60% horizontal opening at BER = 10^{-14}.

The QPSK and NRZ signaling necessitate an SNR of about 18 dB and 13 dB for BER = 10^{-14} [45], respectively. Hence, the minimum received power versus the noise figure (NF) of the RX can be calculated as [41]

$$P_{\min} - NF = 10 \log(BW) + SNR_{\min} - 174 \tag{5.5}$$

where $P_{\min}$ is the minimum received signal power, BW is the frequency band of interest, and $SNR_{\min}$ is the required SNR level for equalizing received data. Substituting the minimum required SNR in (5.5), $P_{\min} - NF$ should be -58 dB and -63 dB for the BB and the PB at BER = 10^{-14}, respectively. This trade-off between $P_{\min}$ and NF gives a valuable insight for optimizing the power efficiency. The TX power can be reduced up to the point that NF on RX side becomes dominant, thereby forcing an increase of power on the RX side.

Moreover, based on the system-level simulation, $\pm5°$ phase mismatch between LO_I and LO_Q yields a 3 dB SNR penalty in the vicinity of BER = 10^{-14}. This amount of the SNR penalty can be compensated either on the TX side by increasing the TX power

by 3 dBm, or on the RX side by providing a 3 dB lower NF specification. Hence, the $LO_{I/Q}$ phase mismatch should be kept lower than $\pm 5°$ and the analog front-end (AFE) should be designed accordingly. A source-synchronous architecture is employed for the clocking scheme, as shown in Fig. 5.1, which relaxes the complexity of the CDR circuit and provide an inherent tracking of correlated jitter [27, 46].

Besides, the output spectrum of the proposed TRX has the inherent notches at $f = 1/T_{\text{ref}}$ and $f = 3/T_{\text{ref}}$, as shown in Fig. 5.5 (b). Therefore, for the MDB channel scenario the TX spectrum shape can track the channel notches by adjusting the reference clock frequency, thus, TRX can be customized to the channel response. In the NRZ/MT approach, in order to match the transmitted spectrum to that of the channel, an initial calibration phase is applied, which can change the reference clock frequency depending on the quality of the received signal. Therefore, the TX spectrum can be shaped with respect to the channel characteristic and no bit energy would be wasted around the channel notches. Thus, the proposed signaling scheme is applicable to any channel, regardless of the number of the notches and their frequencies, and even if there is no notch in the channel frequency characteristic.

5.3   Circuit Design

Based on the system-level requirements, the design of the transceiver is described in the following. The goal is to communicate at 4×9 Gb/s over four differential MDB channels shown in Fig. 5.3, side-by-side.

5.3.1   Transmitter

Fig. 5.9 (a) shows the proposed hybrid NRZ/MT transmitter, which consists of four differential TX all bundled together with a clock lane. The modulation scheme is based on [24] that applies FDM scheme and combines three baseband data streams into three sub-band (BB, I and Q) single stream. Each of the independent baseband data streams, generated by an embedded PRBS15, has F_{ref} b/s data rate, i.e., 3 Gb/s. Two passive mixers upconvert the two sets of baseband streams into PB sub-band using $2 \times F_{\text{ref}}$ orthogonal clock phases. An LVDS-type output driver adds the PB with the BB sub-band and generates 9 Gb/s single stream. These three sub-bands are orthogonal within one sub-unit interval, $\text{UI}_{\text{sub}} = 333$, and can be recovered by downconverting/integrating within one UI on the RX side. Moreover, four TX are placed side-by-side to support an aggregate 36 Gb/s data rate, and as described in Section II, baseband pulse-shaping is not applied. The TX output power is adjustable by using a 3-bit current DAC as the current source,
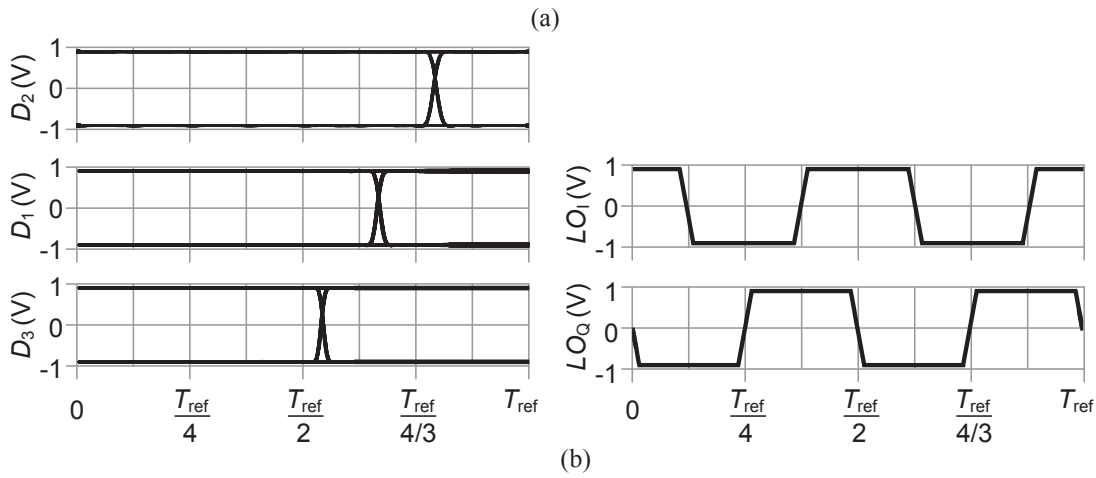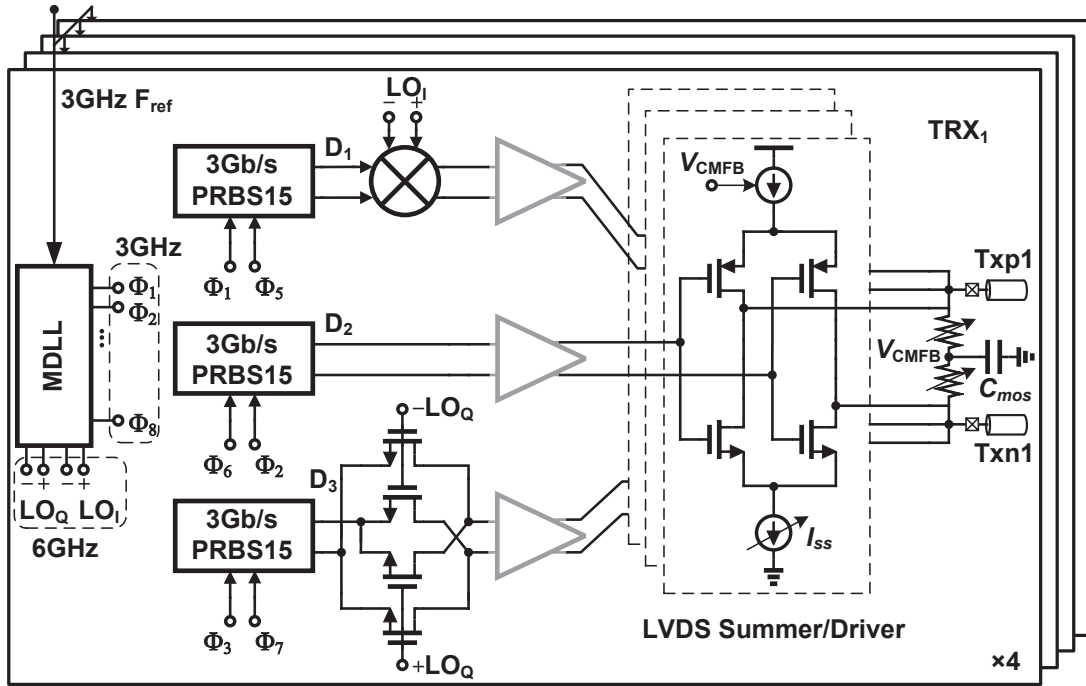
Figure 5.9: Proposed 4×9 Gb/s TX architecture.

i.e., I_{SS} in Fig. 5.9 (a). Based on (5.5), the optimum value for P_{min} is found to be -27 dBm and -22 dBm for PB and BB, respectively, which leaves a sufficient margin for NF to be realized by a low-power circuit on RX side. By applying an appropriate timing for the baseband data and the local clocks, as shown in Fig. 5.9 (b), each transition has at least $T_{ref}/16$ time difference from the nearest transition point. Therefore, the peak-to-average ratio (PAR) and ICI are efficiently mitigated, and the peak-to-peak output swing of the TX is set to be around 300 mV.
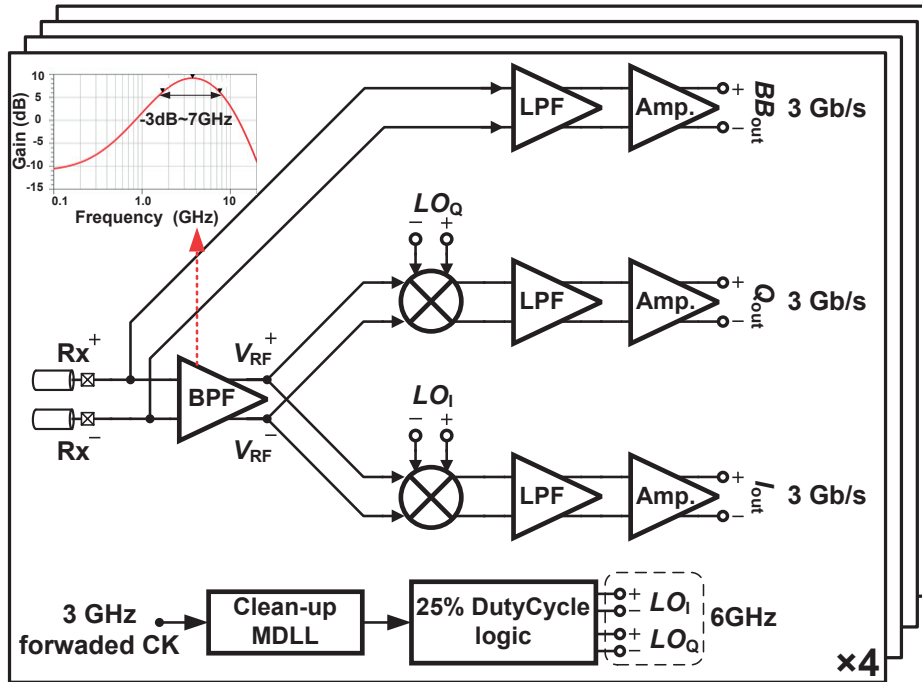
Figure 5.10: Proposed 4×9 Gb/s mixed NRZ/MT receiver.

5.3.2   Receiver

Fig. 5.10 shows the RX block diagram, which supports four differential I/Os side-by-side. The CDR method for the link is based on the proposed architecture in Chapter 3, which employs forwarded clock scheme to amplify, multiply, and delay the received clock on RX side. To reduce the power dissipation, each of TRX has its own clean-up multiplier DLL (MDLL) blocks, while only one single-ended reference clock is forwarded at F_{ref} rate. At the input of RX, the received signal is filtered by the channel frequency response and is more attenuated for the PB sub-band. The attenuation for the BB sub-band is 5 dB at the Nyquist frequency, while the PB sub-band experiences a 14 dB tilt from F_{ref} to $3 \times F_{\text{ref}}$. Therefore, the BB sub-band, can be equalized by low-pass filtering of I/Q contents. Then the signal is amplified and passed to an output buffer. For the PB sub-band, after bandpass filtering and gain boosting, the direct-conversion architecture is used for signal reconstruction. The PB sub-band first pass through a band-pass filter (BPF), which suppresses the BB content. Then, a switched-capacitor mixer/filter (SCMF) unit is used to perform downconverting/integrating task.

The BPF consists of a two-stage peaking amplifier, which provides around 10 dB gain boosting at passband and removes the baseband [71]. The input low-pass filter (LPF) for BB sub-band, presented in [71], is a 2nd-order filter, which sufficiently suppresses
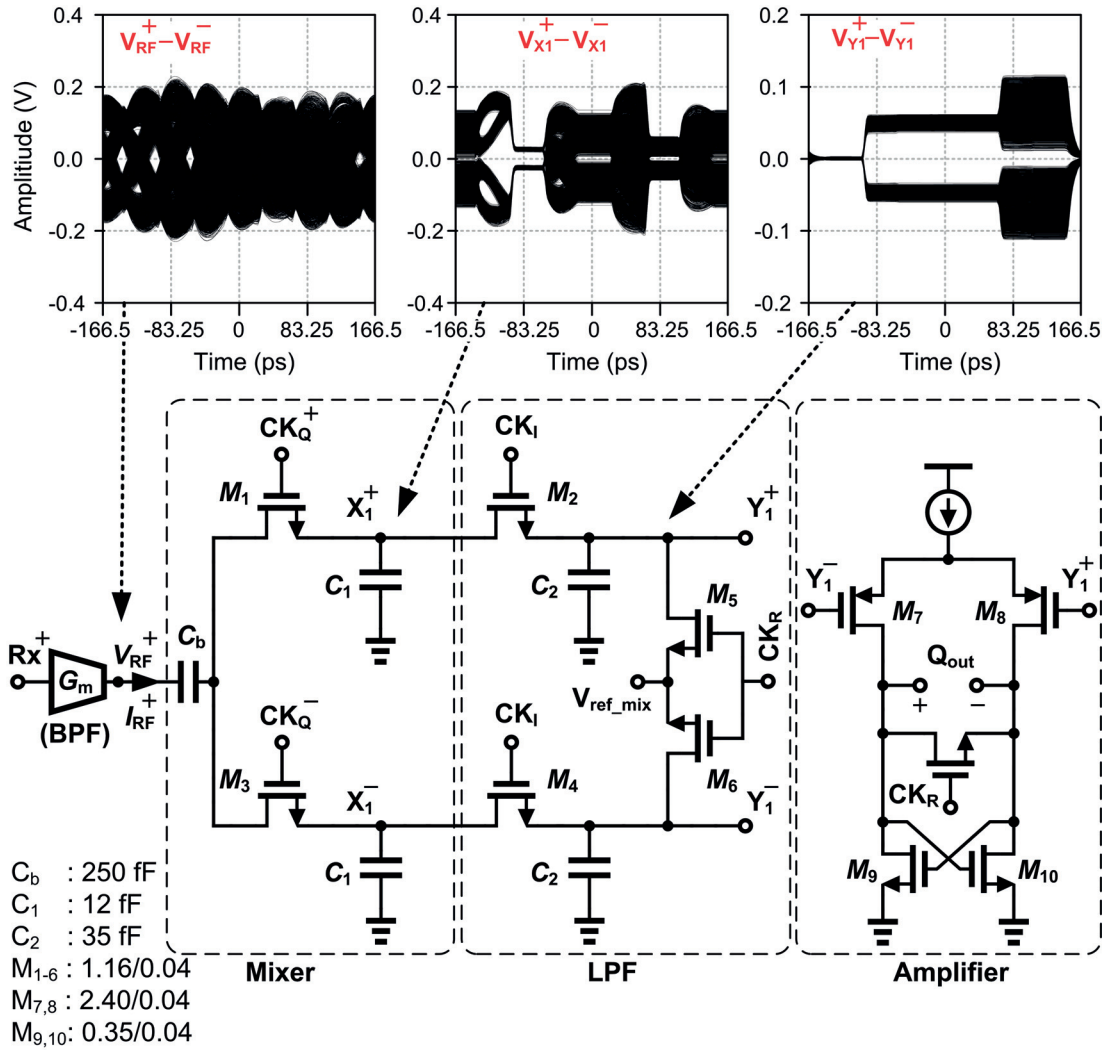
Figure 5.11: Half-circuit implementation of SCMF and baseband amplifier units.

the PB sub-band. The design and analysis of these building-blocks has been presented
in Chapter 3. Comparing to the work that is presented in Chapter 3, SCMF unit
has a different design and an improved clocking scheme, which yields a better circuit
performance. The design of this circuit is described in the following.

5.3.2.1   Downconverting Mixer / Filter Unit

The half-circuit implementation of the proposed SCMF, and the baseband amplifier is
presented in Fig. 5.11, where the G_m stage models the preceding BPF block. In this
circuit, a current-driven mixer with a 25% duty cycle LO is used to downconvert the
received signal, while the non-overlapping clocking scheme helps to provide a better

Φ_1	Reset
$\Phi_{0,2,4,6}$	$\dfrac{1}{C_1}\displaystyle\int_{t_0}^{t_0+\Delta T} I_{RF}(t)dt$
$\Phi_{3,7}$	Charge sharing
Φ_5	Hold
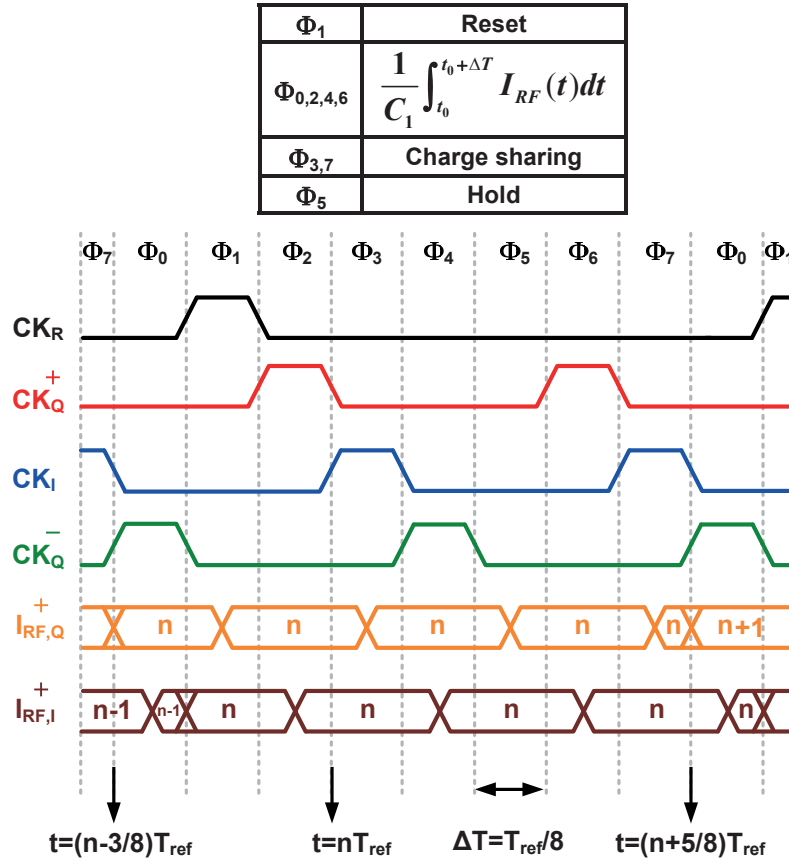
Figure 5.12: The timing diagram of SCMF in Fig. 5.11

low-pass filtering. The downconverted signal is then given to a sense amplifier that properly amplifies the signal, hence, relaxes the noise and linearity requirements of the BPF.

In addition to downconverting the received signal, the proposed circuit isolates the orthogonal I and Q sub-bands from each other. The timing diagram for Q sub-band is presented in Fig. 5.12. The received data-stream can be modeled in the current domain, and it is composed of two orthogonal parts, as shown in Fig. 5.12, $I_{\mathrm{RF}}(t) = I_{\mathrm{RF,I}}(t) + I_{\mathrm{RF,Q}}(t)$, where $I_{\mathrm{RF,I}}(t) = I(t)cos(\omega_0 t)$, and $I_{\mathrm{RF,Q}}(t) = Q(t)sin(\omega_0 t)$. The SCMF is designed such that the received current is integrated by the orthogonal basis functions, i.e., 90° phase-shifted square waveforms. As shown in Fig. 5.11, M_1 is on during Φ_2 and also Φ_6 time intervals, while M_3 conducts during Φ_0 and Φ_4 time intervals. Having the proposed timing diagram of Fig. 5.12, the integration of $I_{\mathrm{RF,I}}(t)$ is zero at the end of all Φ_0, Φ_2, Φ_4, and Φ_6 time intervals. Therefore, assuming that the sampling clocks are properly aligned with the received data, this circuit is able to suppress the I sub-band by appropriate current integration. Meanwhile, the Q sub-band (which is in current domain) is integrated over

Φ_0, Φ_2, Φ_4, and Φ_6 time intervals to amplify and downconvert the main signal. During Φ_3 and Φ_7 time intervals, the charge-sharing between C_1 and C_2 capacitors implements a low-pass IIR filter, which can further reduce the unwanted high-frequency signals. At the end of this process, after the data is detected, the capacitors will be discharged by a reset clock phase, CK_R, and made ready for the next phase.

Based on this operation and the timing diagram shown in Fig. 5.12, the output of SCMF during Φ_3-Φ_6 can be expressed by

$$V_{Y_1}(n) = \alpha V_{Y_1}(n-1) + A_0 \left[\int_{t_1}^{t_1+\Delta T} I_{RF}(t)dt - \int_{t_0}^{t_0+\Delta T} I_{RF}(t)dt \right] \tag{5.6}$$

where $\alpha = C_1/(C_1 + C_2)$, $A_0 = 1/[C_1(C_1 + C_2)]$, $t_0 = (n - 3/8)T_{ref}$, $t_1 = (n - 1/8)T_{ref}$, $\Delta T = T_{ref}/8$, and T_{ref} is the sub-band unit interval time.

As Fig. 5.12 shows, $\int_{t_1}^{t_1+\Delta T} I_{RF}(t)dt = -\int_{t_0}^{t_0+\Delta T} I_{RF}(t)dt = \Delta T \times Q(n)$. Therefore, the output voltage of the baseband amplifier can be calculated as

$$Q_{out}(z) = \frac{2\Delta T A_0 A_1}{1 - \alpha \cdot z^{-1}} \times Q(z) \tag{5.7}$$

where $z = e^{j\omega T_{ref}}$, and $A_1 = g_{m7,8} \times (r_{o7,8}||r_{o9,10} - 1/g_{m9,10})$, where g_{m7-10} and r_{o7-10} denote the small-signal transconductance and output resistance of $M_7 - M_{10}$, respectively. As (5.7) shows, the Q sub-band is downconverted and low-pass filtered by charge-sharing mechanism. The ratio of C_2/C_1 defines the filter bandwidth, which is selected to be around 3 in order to provide sufficient filtering and gain characteristics.

5.3.3   Clock and Data Recovery

The DLL-based CDR topology is a preferable choice for source-synchronous high-speed links since it does not have the jitter accumulation issue, while it consumes less power compared with PLL-based CDR architecture. The design and analysis of the multiplier DLL (MDLL)-based CDR, which can be efficiently employed in NRZ/MT transceivers, is presented in Chapter 4. Most of the CDR building-blocks in our new 36 Gb/s has the same topologies that are presented in Chapter 4. Comparing to the MDLL-based CDR in Chapter 4, We have improved the DLL performance to operates at higher F_{ref} (i.e., 3 GHz nominal frequency), and we add 25% duty cycle clock generation logic to the edge combiner circuit. Therefore, the required clock phases has been generated by some minor modifications of our previous design while the core circuit remains intact, and the power consumption is not degraded.
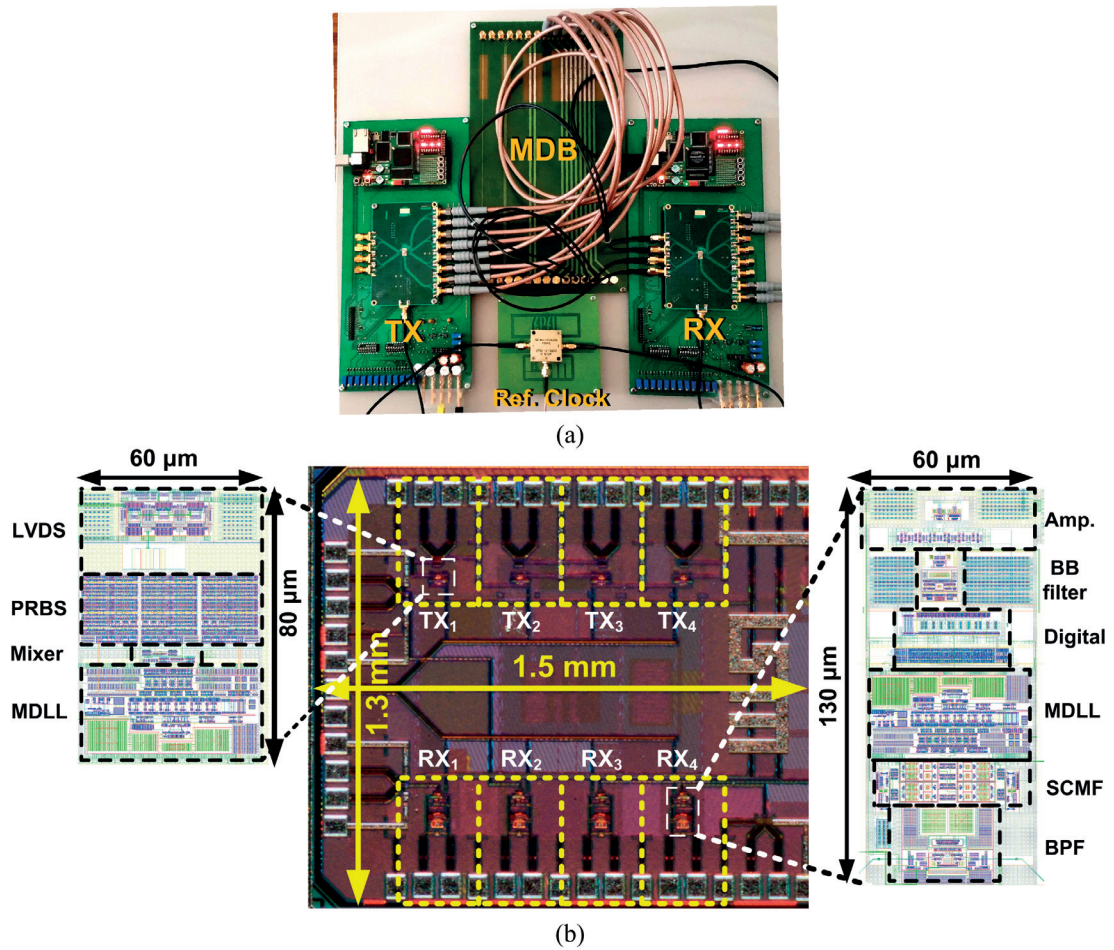
Figure 5.13:   (a) Test setup with MDB channel. (b) Chip die photo and layout in 40 nm CMOS.

5.4   Measurement Results

Fig. 5.13 (a) shows the test setup for the proposed NRZ/MT TRX system. The reference FR-4 channel, 30 cm in length, exhibits frequency notches as shown in Fig. 5.3. These notches are introduced by two open stubs and can mimic the frequency response of a typical MDB channel. Using this structure we are able to tune the frequency of the notches within a $\pm 30\%$ range, for test purpose. The prototype is fabricated in a 40 nm GP 1-poly 10-metal bulk CMOS process and includes four independent RX and TX circuits, each occupying $130 \times 60 \ \mu m^2$ and $80 \times 60 \ \mu m^2$, respectively. The die micrograph is shown in Fig. 5.13 (b).

The measured output spectrum of TX for different F_{ref} setting is shown in Fig. 5.14 (a). Based on this measurement, the TX is able to adjust its spectrum to the frequency
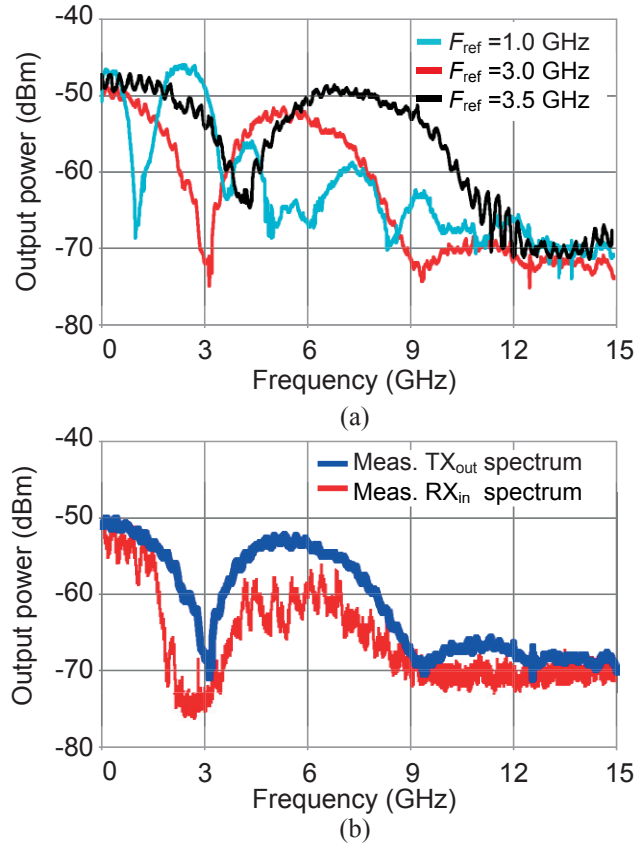
Figure 5.14: (a) Measured TX output spectrum at different F_{ref} settings. (b) Measured spectrum at the input of RX.

response of the channel within a $\pm25\%$ range, i.e., the first null frequency in the TX frequency spectrum can be changed between 1 and 3.5 GHz. The measured spectrum at the input of RX is shown in Fig. 5.14 (b) and shows that the PB sub-band is more attenuated compared with the NRZ sub-band. Based on this measurement, the received energy for the BB and the PB sub-bands are -21.5 dBm and -26 dBm, respectively.

Fig. 5.15 (a), (b), and (c) show the measured eye diagram for Q, I, and BB sub-bands, respectively, each having 3 Gb/s data rate, when no aggressor transmitter is present. The bathtub for each of the Q, I, and BB sub-bands is shown in Fig. 5.15 (d), (e), and (f), respectively. The BB, Q, and I sub-bands have 182 ps, 169 ps, and 177 ps horizontal margin at $\text{BER} = 10^{-12}$, respectively. In this measurement, the configuration bits for offset, bandwidth, and gain setting of amplifiers have been calibrated based on quality of the sub-band eye diagrams, through a serial peripheral interface.

Having aggressor TX on Channel 2 and Channel 4, the measured FEXT on Channel 3
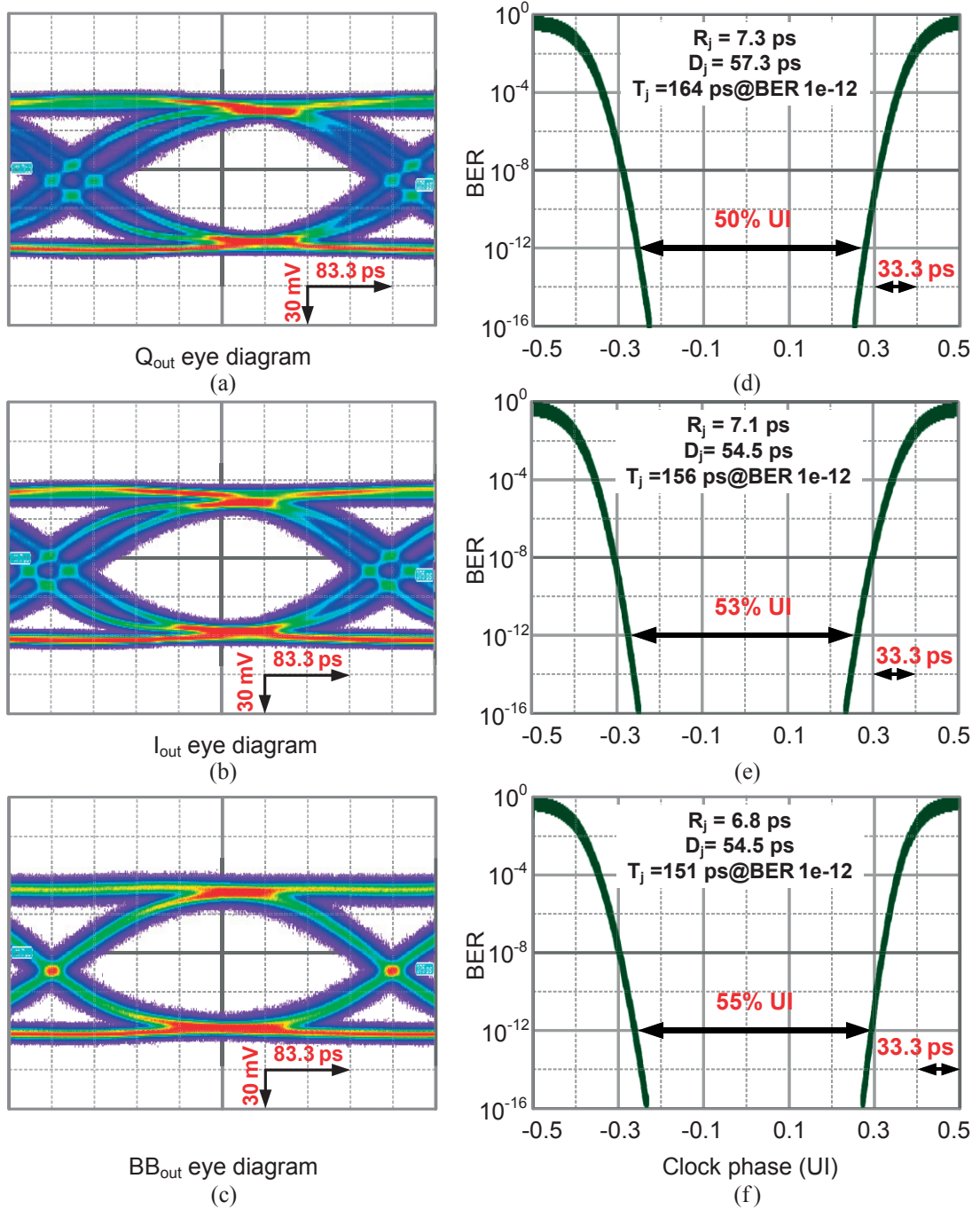
Figure 5.15: Measured RX eye diagram at 9 Gb/s data rate. (a) Q sub-band. (b) I sub-band. (c) BB sub-band. Corresponding bathtub curve for: (d) Q sub-band, (e) I sub-band, (f) BB sub-band, each operates at 3 Gb/s data rate.

is shown in frequency and time domain in Fig. 5.14(a), and (b), respectively. Although the peak-to-peak FEXT is about 60 mV its spectrum has NRZ/MT shape, as discussed in Section II. As explained in Section II, the strong reflections and severe FEXT make

(a)

(b)
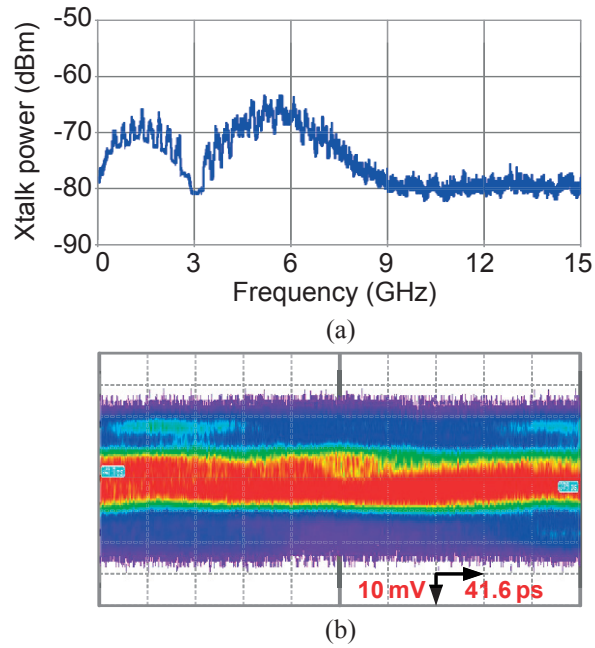
Figure 5.16: Measured FEXT on Channel 3 (a) in frequency, and (b) in time domain.

it impossible to equalize the link by employing conventional NRZ signaling at 9 Gb/s.
However, by applying the hybrid NRZ/MT signaling the measured eye diagram for Q,
BB, and I sub-bands for different lanes are shown in Fig. 5.16. Here, the middle lanes are
labeled as Channel 2 and Channel 3 while the edge lanes are labeled as Channel 1 and
Channel 4, as shown in Fig. 5.1(b). As expected, the middle lanes are more affected by
FEXT, hence, the eye-opening is less for them. However, all of the received sub-bands
have sufficient eye-opening to ensure a 40% unit-time-interval horizontal eye-opening
(referring to 3 Gb/s sub-band data rate) at BER $= 10^{-12}$. Each sub-band operates at
3 Gb/s data rate and the total data rate is 36 Gb/s over four differential lanes. The
bathtub is shown for the PB receivers as the BB receivers demonstrate a better eye-
opening at BER $= 10^{-12}$. This measurement shows that crosstalk degrades the horizontal
eye-opening, shown in Fig. 5.17, by about 15% in the worst case.
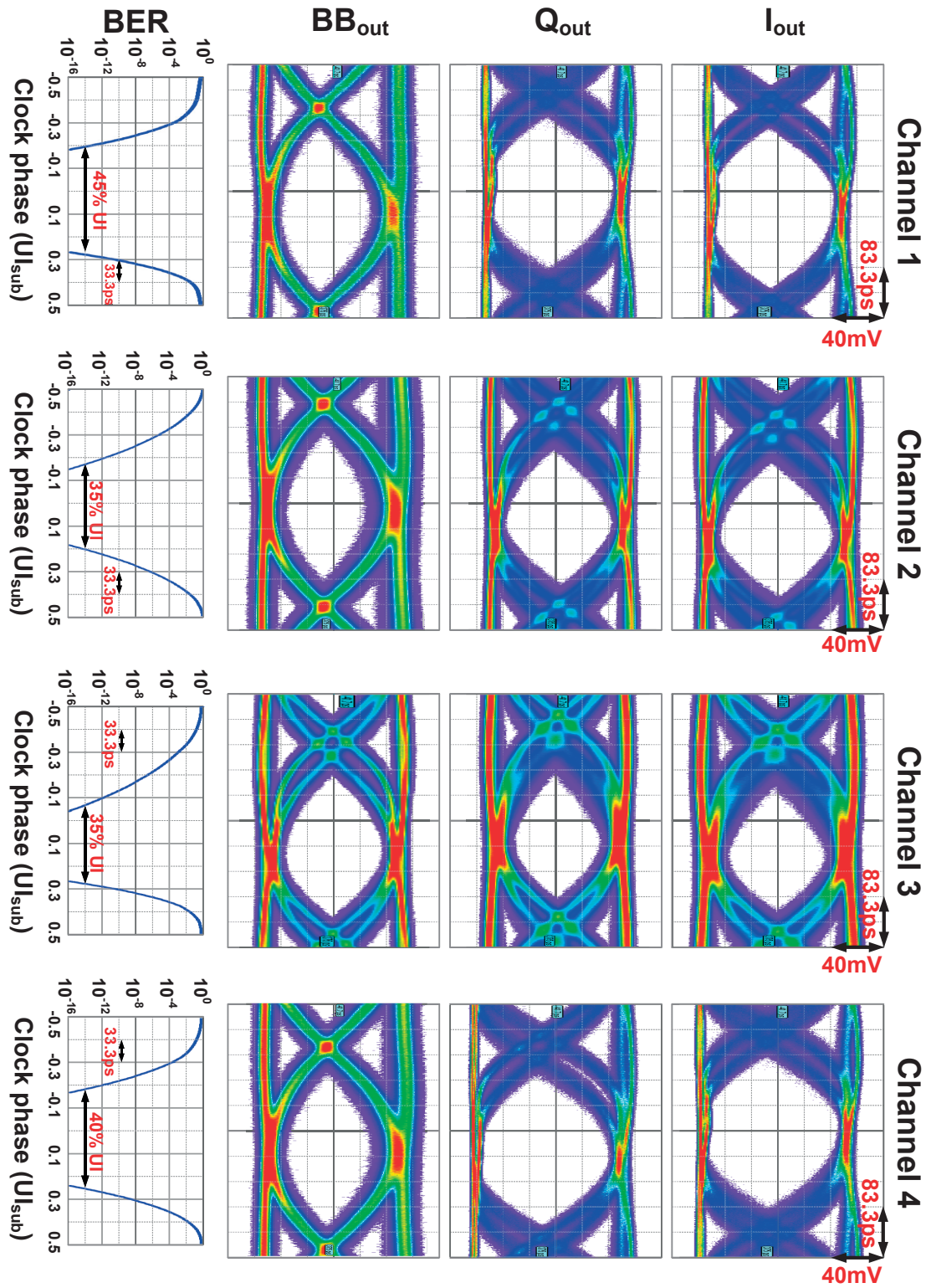
Figure 5.17: Measured RX eye diagram at RX side. The aggregate data rate is 36 Gb/s while each sub-band operates at 3 Gb/s data rate.

TX component	Power (mW)
Clock Unit	1.53
LVDS summer/driver	2.88
Mixer	0.27

(b)

RX component	Power (mW)
Clock Unit	1.95
Amplifiers	0.4
SCMF	0.64
AFE	1.33

(a)   (c)
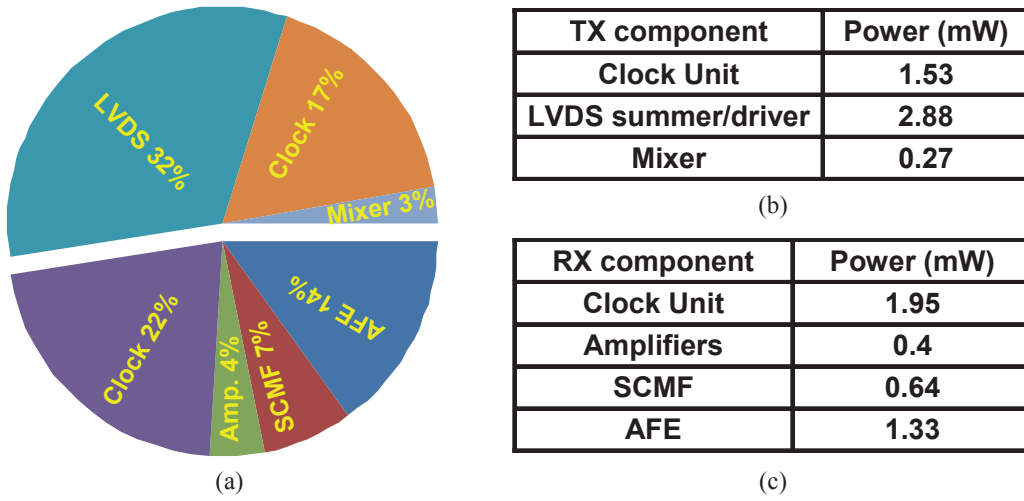
Figure 5.18: (a) Power breakdown for the whole TRX. (b) TX power specification. (c) RX power specification.

Table 5.1: TRX Performance Comparison with State-of-the-art Memory Transceivers.

Reference	[65]	[48]	[69]	This work
Technology	65nm	45nm SOI	180nm	40nm GP
RX/TX Area (mm^2)	0.036*/NA	0.014*/NA	0.036*/0.018*	0.008*/0.005*
Channel	6" FR4	5" FR4	4" FR4	MDB-12" FR4
Multi-lane # × Data rate (Gb/s)	4 × 12	2 × 12.5	8 × 5	4 × 9
RX/TX power efficiency (pJ/bit)	1.78**/NA	0.52**/NA	6.2/11.6	0.49/0.5
BER / Horizontal eye-opening	10^{-8} / 38% UI (32ps)	10^{-12} / 15% UI (12ps)	10^{-12} / 63% UI (126ps)	10^{-14} / 35% UI$_{sub}$ (117ps)
Supply (V)	1.1	1.2	1.8	0.9
IO type / Architecture	Single-ended / Analog-IIR	Differential / SC-DFE	Single-ended / Staggered bus	Differential / Multi-Tone

* Core size area.
** Power is calculated for the whole RX.

The TRX power breakdown for the total data rate of 9 Gb/s is shown is Fig. 5.18 (a). The whole chip consumes 36 mW from a 0.9 V power supply at this data rate, leading to 1 pJ/b link efficiency over the MDB channel interface. This includes the power consumption of TX (MDLL, mixers and LVDS driver) and RX (BPF, LPF, SCMF and MDLL). The consumption of the built-in PRBS15 generator and the I/O buffers that drive the measurement equipment are excluded from this calculation. The TX and RX consume 51% and 49% of the total power, respectively. The TX and RX circuit power

consumption are shown in Fig. 5.18 (b) and (c), respectively.

Table 5.1 summarizes the silicon performance comparison with state-of-the-art memory interface transceivers. Compared to the other works, the proposed TRX has the link power efficiency of 1 pJ/b, while it operates over a multi-drop memory interface. The horizontal eye-opening is at least 110 ps for each sub-band at BER $= 10^{-14}$. The total bit-stream is divided into three sub-bands, therefore, the sub-receivers operate at one third of the total bit rate. The horizontal eye margin, thus, benefits from this fact and the link becomes less sensitive to clock jitter and other non-idealities.

5.5   Conclusion

A multi-lane 4×9 Gb/s transceiver with 1 pJ/b energy efficiency has been demonstrated in 40 nm CMOS technology. Communicating over MDB interface, hybrid NRZ/MT signaling has been employed in order to relax the required equalization, and hence reduce energy consumption. Moreover, it has been shown in this article that NRZ/MT signaling can efficiently reduce the influence of ISI as well as crosstalk. This property is especially interesting for modern high density links where the distances between the lanes are gradually reduced and the effect of crosstalk becomes more evident. Experimental results for the proposed four lane link show that the recovered data demonstrates error-free data transmission, while operating at 9 Gb/s/lane. A modified discrete-time mixer/filter has been employed in the receiver in order to reject more efficiently the side-channels, and hence achieving better eye-opening.

6 Conclusion

6.1 Achievements

In this thesis a new signaling method for wireline application has been investigated, and efficient system architecture and circuit topologies have been introduced in order to implement the proposed signaling method on silicon. This is mainly motivated by the fact that in IoT era the ever increasing demand for higher bandwidth necessitates a tremendous improvement in I/O speed, whereas the energy efficiency should meet the stringent system requirements. While industry continues the demand for higher data transfer speed over low-cost, high-loss channels, a very complex digital and analog signal processing is required to mitigate the channel impairments. Therefore, modern serial data transceivers are equipped with very sophisticated equalizers and crosstalk cancellation units, which in return increase system complexity and energy consumption. Although process scaling has fueled the drastic increase in processing power over the last decade, the energy efficiency improvement has diminished due to supply voltage saturation in finer technology nodes. As a consequence, if the baseband signaling continues to be used in this paradigm, the I/O power cannot scale proportionally with the data bandwidth. Hence, bearing in mind that the solution should be found in system architecture, signaling scheme, and circuit innovation, this thesis focused on development of a **Hybrid NRZ/multi-tone signaling scheme** in order to implement high-speed and low-power serial data transceivers, especially for the channel interfaces where conventional baseband signaling transceivers (e.g., NRZ, PAM-4, ENRZ) cannot offer power efficient solution.

In this Chapter 3 we have proposed a new signaling scheme, called hybrid NRZ/multi-tone (MT), which can shape the transmitted spectrum of the transmitter (TX) and be customized to the characteristics of the channel, thus, it provides a power efficient solution. Having the proposed signaling scheme, the circuit design and implementation of **a**

7.5 Gb/s hybrid NRZ/MT transceiver for multi-drop bus memory interfaces in 40 nm bulk CMOS technology is presented. Reducing the complexity of the equalization circuitry on the receiver (RX) side, the proposed architecture achieves **1 pJ/bit link efficiency for a MDB channel with 45 dB loss at 2.5 GHz**. The transmitted spectrum is composed of baseband (BB) and I / Q sub-bands with the ability to match the modulation frequency of the entire TRX with respect to the channel response over a $\pm 25\%$ range. A switched-capacitor-based mixer/filter is developed to efficiently down convert and equalize the I / Q sub-bands in the RX. The core size area is $85 \times 60~\mu m^2$ and $150 \times 60~\mu m^2$ for the TX and RX, respectively.

In this Chapter 4, the clock and data recovery unit for the proposed hybrid NRZ/MT transceiver has been explained in details. The proposed circuit adequately reduces the complexity and power dissipation of CDR unit in wireline transceivers, while satisfying the required jitter and phase mismatch specifications. New strategies are proposed to satisfy these specifications, while they fulfill the stringent power consumption requirements in wireline links. The RMS jitter remains below 3 ps over the entire input frequency range. A low-voltage technique is proposed to improve the mismatch effect in charge pump circuit and reduces the deterministic jitter. Based on the measurement results, the power consumption does not exceed 1.8 mW over the entire input frequency range results in 280 fJ energy consumption for 6 GHz output.

In Chapter 5, we have exploited the properties of multi-tone signaling, especially orthogonality among different sub-bands, to reduce the effect of crosstalk. A four-channel transceiver has been implemented in a standard CMOS 40 nm technology in order to demonstrate the performance of NRZ/MT signaling in presence of high channel loss and strong crosstalk. Comparing to the first prototype presented in Chapter 3, we have extended the proposed NRZ/MT serial data transceiver to support four closely spaced differential channels, to study the performance of the system in presence of severe crosstalk. Furthermore, we have improved the receiver equalization scheme to reach 9 Gb/s (4.5 Gb/s/pin) that is 20% faster compared with our earlier work without degrading energy efficiency. The multi-tone nature of the proposed transceiver helps to control the ISI and reduce the far-end crosstalk (FEXT), which results in a very energy-efficient implementation. The final prototype can deliver an aggregate **36 Gb/s data rate** while demonstrates an error-free operation over our reference MDB channel. The core size area is $80 \times 60~\mu m^2$ and $130 \times 60~\mu m^2$ for the TX and RX blocks (including the clock unit), respectively.

6.2   Future Works

There are still some aspects in the proposed method to be improved for communicating at higher speeds and lower power, and for delivering robust product-level hybrid NRZ/MT I/O cells. The automatic adaptability of the proposed TRX is one of the important subject to be investigated so as to the whole TRX can be customized to the link characteristics and operates at the optimum power efficiency. It should be done by delivering a fixed data rate, while the modulation scheme adapts to link characteristics through a background calibration. Likewise, employing different modulation schemes (ENRZ, duobinary,PAM-4, etc.) for different sub-bands should be investigated in the proposed multi-tone method. Based on a preliminary study, this technology shows a great potential for communicating beyond 100 Gb/s/wire over lossy backplane channels, where the channel impairments becomes so severe that baseband TRX cannot offer any functional solution. The CDR implementation, which is presented in Appendix B, needs careful circuit implementation and precise system-level investigation so as to the circuit realization becomes robust and energy efficient. Moreover, employing MT technique for capacitive-coupled 3D integration can be a subject of future research.

A System-Level Statistical BER Modeling for Hybrid NRZ/MT Link

Accurate modeling and analysis of a link is critical to evaluate system timing and voltage margin by including link imperfections and environmental noises, e.g., deterministic and random jitter. In today's high-speed I/O paradigm, where the error-free system operation is the designers' milestone, such system-level simulation should evaluate the link system performance for a very low BER (i.e., $< 10^{-16}$), and should also provide a time-efficient solution for system designers to optimize the link performance.

Traditional SPICE-based simulation techniques can precisely simulate various deterministic jitter sources, such as ISI and crosstalk from passive channels. However, the inclusion of random jitter in SPICE simulations necessitates very long simulation time. Likewise, the very-low targeted BER requires simulation of tremendous bit counts, thereby time-domain SPICE-based simulation becomes more and more time consuming in today's high-speed serial link modeling. Innovative simulation techniques have been recently introduced to accurately model link performance for low BER efficiently. The most popular approaches are based on a statistical eye consisting of the ISI probability distributions at different sampling phases [72, 73, 74, 75]. In this Appendix we briefly review the statistical eye analytical model, and explain the algorithm that we used in our MATLAB simulations for extracting the eye diagram and bathtub for hybrid NRZ/MT system presented in Chapter 2.

The statistical eye methodology is based on the calculation of the probability distribution function (PDF) for a received bit at a given sampling time. Assuming the link as a linear time-invariant (LTI) system, the PDF for a received bit is calculated by convolving the PDF for ICI, ISI, TX/RX induced jitter, which are evaluated independently. Then, the BER is estimated from the resulting PDF. To include the TX and RX jitter into the
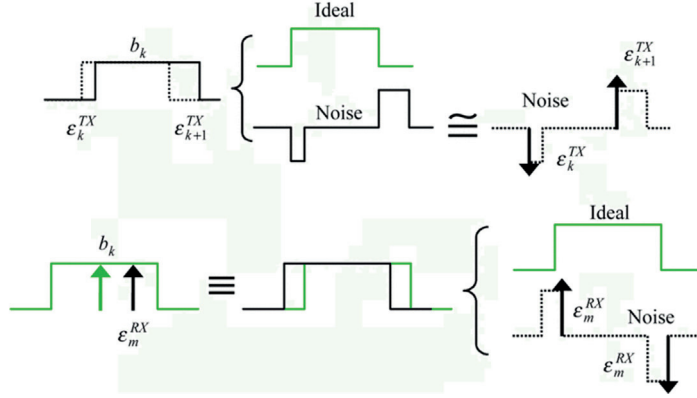
Figure A.1: Transmitter and receiver jitter models.

model, the *Dual Dirac model* for jitter is used [73].

Transmitting binary data over all sub-bands, the received signal at the corresponding sub-RX front-end (before sampling) can be written as

$$
y(t) = \sum_k (a_\mathrm{k} - a_\mathrm{k-1}) s^{th}(t - \varepsilon_\mathrm{k}^{TX} - kT_\mathrm{b}) + \sum_l (b_\mathrm{l} - b_\mathrm{l-1}) s^{ICI}(t - lT_\mathrm{b})
$$
$$
+ \sum_p (c_\mathrm{p} - c_\mathrm{p-1}) s^{XTK}(t - pT_\mathrm{b}) \tag{A.1}
$$

where $s^{th}(t)$, $s^{ICI}(t)$, and $s^{XTK}(t)$ are the through, ICI, and crosstalk step response (including mixer and filter effects into the step responses), respectively, T_b is the bit period, k, l, and p are the transmitted symbol index, a_k is the binary output of the sub-TX, b_l, and c_p represent the output of the aggressor sub-band TX, and the aggressor neighbor TX, respectively, and $\varepsilon_\mathrm{k}^{TX}$ is the main sub-TX jitter. At the corresponding sub-RX side and after sampling at $t = mT_\mathrm{b} + \varepsilon_\mathrm{m}^{RX}$, where $\varepsilon_\mathrm{m}^{RX}$ is the sub-RX jitter, the sampled signal can be written as

$$
y_m = \sum_k (a_\mathrm{k} - a_\mathrm{k-1}) s^{th}[\varepsilon_\mathrm{m}^{RX} - \varepsilon_\mathrm{k}^{TX} + (m-k)T_\mathrm{b}] +
$$
$$
\sum_l (b_\mathrm{l} - b_\mathrm{l-1}) s^{ICI}[\varepsilon_\mathrm{m}^{RX} + (m-l)T_\mathrm{b}] + \sum_p (c_\mathrm{m} - c_\mathrm{m-p}) s^{XTK}[\varepsilon_\mathrm{p}^{RX} + (p-l)T_\mathrm{b}].
$$
$$
\tag{A.2}
$$

The transmitter and receiver jitter are modeled as impulses at the transition edge times, formally known as a Dual Dirac model, as shown in Fig. A.1 [76, 73]. Hence, the received signal at the input of the sub-RX sampler, given by (A.2), can be fairly estimated using

Taylor series expansion as follows:

$$y_m \cong \sum_k (a_\mathrm{k} - a_\mathrm{k-1})s^{th}[(m-k)T_\mathrm{b}] + \sum_l (b_\mathrm{l} - b_\mathrm{l-1})s^{ICI}[(m-l)T_\mathrm{b}]$$

$$+ \sum_p (c_\mathrm{p} - c_\mathrm{p-1})s^{XTK}[(m-p)T_\mathrm{b}] + \sum_k (a_\mathrm{k-1} - a_\mathrm{k})\varepsilon_\mathrm{k}^{TX} h_\mathrm{m-k}^{th}$$

$$+ \varepsilon_\mathrm{m}^{RX}\left[\sum_k (a_\mathrm{k} - a_\mathrm{k-1})h_\mathrm{m-k}^{th} + \sum_l (b_\mathrm{l} - b_\mathrm{l-1})h_\mathrm{m-l}^{ICI} + \sum_p (c_\mathrm{p} - c_\mathrm{p-1})h_\mathrm{m-p}^{XTK}\right]$$

$$= \sum_k a_k p_{m-k}^{th} + \sum_l b_l p_{m-l}^{ICI} + \sum_p c_p p_{m-p}^{XTK} + n^{TX} + n^{RX} \tag{A.3}$$

$$= y_0 + ISI + ICI + Xtalk + n^{TX} + n^{RX} \tag{A.4}$$

where h_m^{th}, h_l^{ICI}, and h_p^{XTK} are the data-rate sampled impulse response of the through, ICI, and crosstalk channel, respectively, ISI, ICI, and $Xtalk$ are the amount of ISI, ICI, and crosstalk at the sample time, respectively, n^{TX}, and n^{RX} represent the effective voltage noise for TX and RX timing jitter, respectively, p_m^{th}, p_m^{ICI}, and p_m^{XTK} are the pulse response of the through, ICI, and crosstalk channel, respectively, and y_0 is the received signal without ISI, ICI, and crosstalk.

Each of the ISI, ICI, and crosstalk PDFs can be calculated as [72, 77]

$$P_{\mathrm{ISI_k}} = P_0\delta(x) + P_1\delta(x - p_\mathrm{k}^{th}) \tag{A.5}$$

$$P_{\mathrm{ICI_l}} = P_0\delta(x) + P_1\delta(x - p_\mathrm{l}^{ICI}) \tag{A.6}$$

$$P_{\mathrm{Xtalk_p}} = P_0\delta(x) + P_1\delta(x - p_\mathrm{p}^{XTK}) \tag{A.7}$$

$$P_{\mathrm{ISI}} = \cdots \otimes P_{\mathrm{ISI_{-2}}} \otimes P_{\mathrm{ISI_{-1}}} \otimes P_{\mathrm{ISI_1}} \otimes P_{\mathrm{ISI_2}} \otimes \cdots \tag{A.8}$$

$$P_{\mathrm{ICI}} = \cdots \otimes P_{\mathrm{ICI_{-2}}} \otimes P_{\mathrm{ICI_{-1}}} \otimes P_{\mathrm{ICI_1}} \otimes P_{\mathrm{ICI_2}} \otimes \cdots \tag{A.9}$$

$$P_{\mathrm{Xtalk}} = \cdots \otimes P_{\mathrm{Xtalk_{-2}}} \otimes P_{\mathrm{Xtalk_{-1}}} \otimes P_{\mathrm{Xtalk_1}} \otimes P_{\mathrm{Xtalk_2}} \otimes \cdots \tag{A.10}$$

where $P_{\mathrm{ISI_k}}$, $P_{\mathrm{ISI_l}}$, and $P_{\mathrm{ISI_p}}$ represent the PDF of the ISI, ICI, and crosstalk from the k-th, l-th, and p-th bit, respectively, P_{ISI}, P_{ICI}, and P_{Xtalk} are the overall PDF of ISI, ICI, and crosstalk, respectively, $\otimes$ represent the convolution symbol, and $\delta(x)$ is the unit impulse function.

The variables in (A.4) are statistically correlated since they are all functions of symbol pattern and different channel impulse responses. Although the exact method for BER calculation should analyze the correlation between these variables, it can be fairly assumed that they are independent to simplify the computation [76, 72]. With this assumption, the overall jitter PDF can be calculated by convolving the PDFs of ISI, ICI, crosstalk,
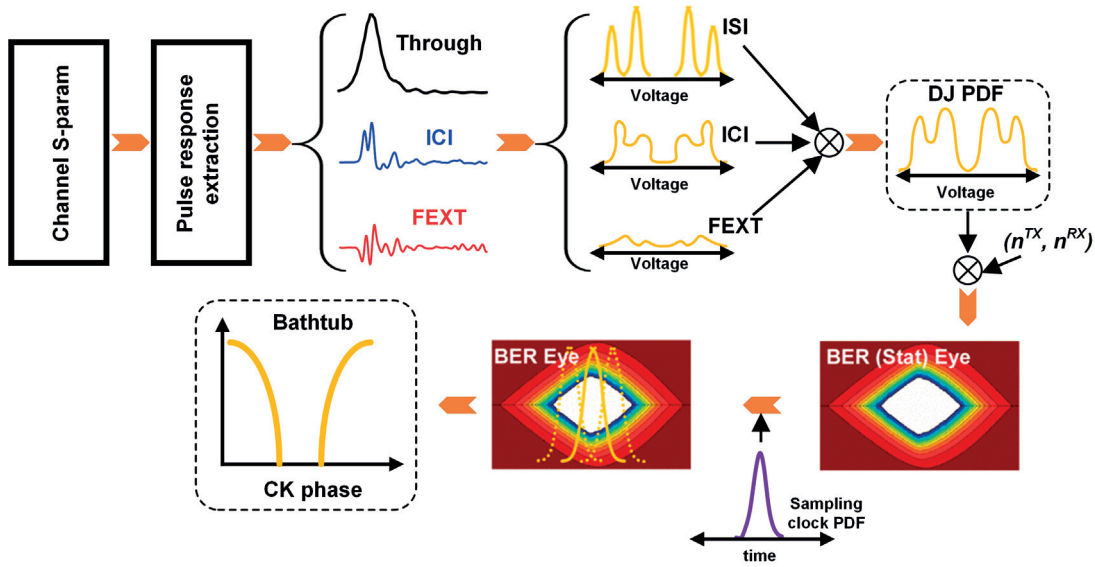
Figure A.2: Flowchart of BER calculation using statistical eye.

and TX/RX jitter. The resulting PDF is then used to calculate BER as follows

$$\mathrm{BER}(v_{\mathrm{REF}}) = P\left(J_{\mathrm{TOT}} < v_{\mathrm{REF}} - y_0 | 1\right) P_1 + P\left(J_{\mathrm{TOT}} > v_{\mathrm{REF}} - y_0 | 0\right) P_0 \qquad (A.11)$$

where $J_{\mathrm{TOT}} = ISI + ICI + Xtalk + n^{TX} + n^{RX}$ represents the total induced jitter at the main sub-RX, v_{REF} is the reference voltage, which is typically zero for differential signaling I/Os, and P_0, and P_1 are the probabilities of the input bit being 0 and 1, respectively.

The statistical eye diagram is calculated by sweeping (A.11) over the sampling phase and the reference voltage. The horizontal bathtubs can then be obtained from horizontal and vertical slices of the statistical eye diagram. Fig. A.2 illustrates the flowchart of the BER bathtub calculation presented in this Appendix.

The flowchart in Fig. A.2 along with the mathematical analysis of BER calculation in this Appendix has been implemented in a MATLAB code to evaluate and optimize the proposed hybrid NRZ/MT transceiver for BER as low as 10^{-20}. It provides an accurate link estimation while the simulation time can be reasonably short, e.g., less than 3 minutes for calculating the eye diagram up to BER $= 10^{-24}$. The results of such simulations have been presented in Chapter 2.

B CDR Techniques for Hybrid NRZ/MT Link System

An important part of a serial link transceiver is the clocking circuitry, which can consume around 40% of the total power budget in the link design. Therefore, the demand for high-performance clock and data recovery (CDR) fabricated in standard CMOS processes, which can provide a power efficient solution, continues to grow where the accumulated jitter performance is paramount to CDR performance. In this paradigm, most of today's high-performance I/O interfaces may be categorized as either *mesochronous*[1] or *plesiochronous*[2], and both require clock and data resynchronization at the RX side.

Source-synchronous links, which is a subset of mesochronous system, are widely adopted in variety of high-speed parallel I/O interfaces such as GPU to memory, CPU to memory, CPU to bridge chips, where the cost and power overhead of additional forwarded clock link is amortized across multiple TRX banks in the system. Likewise, owing to inherent tracking of the correlated jitter between data and clock in such clocking architecture, the jitter performance of the link system is improved [78, 79, 80]. The proposed hybrid NRZ/MT link system presented in Chapter 3 and Chapter 5 employs source-synchronous architecture, as it has been explained in these chapters. However, the delay fine-tuning, which is incorporated in the proposed MDLL and is used for adjusting the clock phase at RX, is manually tuned based on the received signal quality, as discussed in Chapter 4. Nevertheless, it is possible to design a CDR unit so as to automatically adjust the RX clock phases and facilitate the transceiver error-free operation. In this Appendix, we explain the system design of a CDR unit that can be used in the proposed hybrid NRZ/MT transceiver to find the optimum clock phase.

---

[1]*Mesochronous* interfaces adopt precisely identical clock frequencies at either ends of the link, however, the TX and RX clocks have different phase shifts relative to the date.

[2]*Plesiochronous* interfaces operate at almost, but not precisely, the same frequencies at the transmitter and receiver.
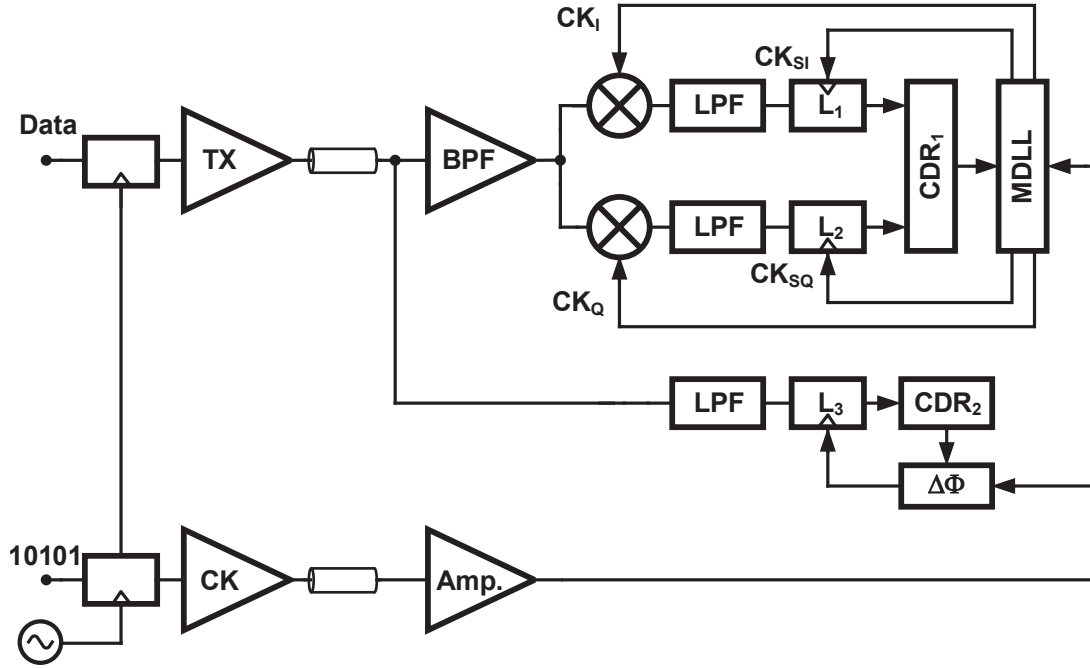
Figure B.1: Forwarded clock CDR architecture for proposed hybrid NRZ/MT link system.

Fig. B.1 shows the proposed CDR architecture for the hybrid NRZ/MT system presented in Chapter 3. Here, the I/Q sub-bands have a shared CDR unit while NRZ sub-band has its own CDR. The CDR for the NRZ sub-band (i.e., CDR_2 and $\Delta\Phi$ blocks in Fig. B.1) can have a conventional architecture, which most NRZ links employ, e.g., the CDR topology in [81, 82]. It should nominally operates at 2.5 GHz, detect the $1\rightarrow0$ and $0\rightarrow1$ transitions, adjust the phase of received forwarded clock (e.g, phase interpolator), and the operation frequency be tunable within a 30% frequency range. The design of such block with these specifications is well studied in literatures, therefore, we focus on the design of CDR for pass-bands in this Appendix.

CDR circuits incorporating bang-bang phase detectors (BBPDs) can be a good choice for realizing the CDR unit in Fig. B.1, since they do not require a charge pump in their architecture; thereby, eliminating the need for amplification of very short high-frequency pulses. Moreover, if a tristate PD such as Alexander topology is employed [83] pattern-dependent jitter can be efficiently suppressed, therefore, deterministic jitter (DJ) performance can be fairly improved [84, 85]. Furthermore, the proposed MDLL circuit in Chapter 4, which incorporates delay fine-tuning in its topology, can be used efficiently along with an Alexander PD, therefore, the implementation of CDR circuits can be done with a set of minor changes in the proposed hybrid NRZ/MT transceiver[3]. The timing

---

[3]The PD should be designed and implemented.
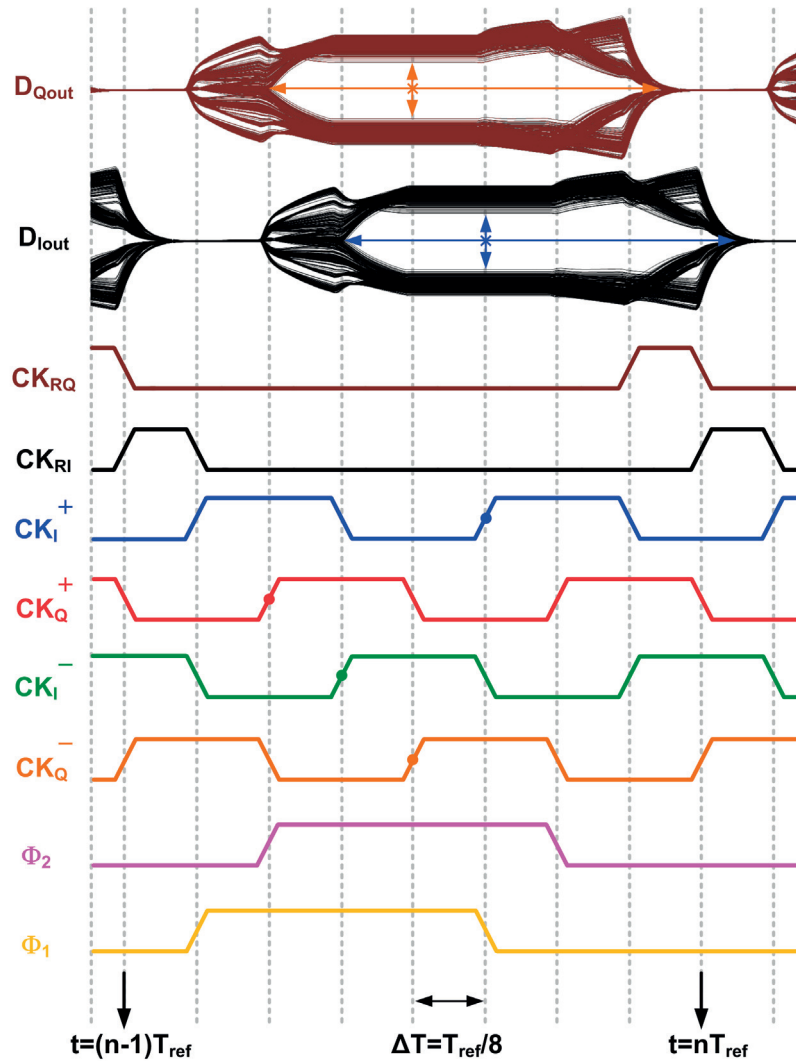
Figure B.2: The timing diagram of the clock signals for recovering I sub-band, which presented in Fig 3.23.

diagram for the clock signals, which have been used in SCMF unit, has been illustrated in Fig B.2 along with the recovered I/Q sub-bands (i.e., D_{Iout} and D_{Qout} in Fig 3.23), which have been aligned with the other waveforms in Fig B.2. The Φ_1 and Φ_2 are the DLL output phases shown in Fig 3.25.

Based on the timing diagram in Fig. B.2, the Alexander PD principle, also known as "early-late" phase detection, can be employed to sample the recovered I/Q sub-bands at the middle point of the eye diagrams, as it is marked on D_{Iout} and D_{Qout} in Fig. B.2. The circuit topology for realizing the CDR circuit for the pass-band, which can replace CDR$_1$ in Fig. B.1, is illustrated in Fig. B.3. The output of this block is then wired to the MDLL delay fine-tunning input, i.e., V_{c} in Fig. 4.2 and Fig. 4.3. In this circuit, the transistors
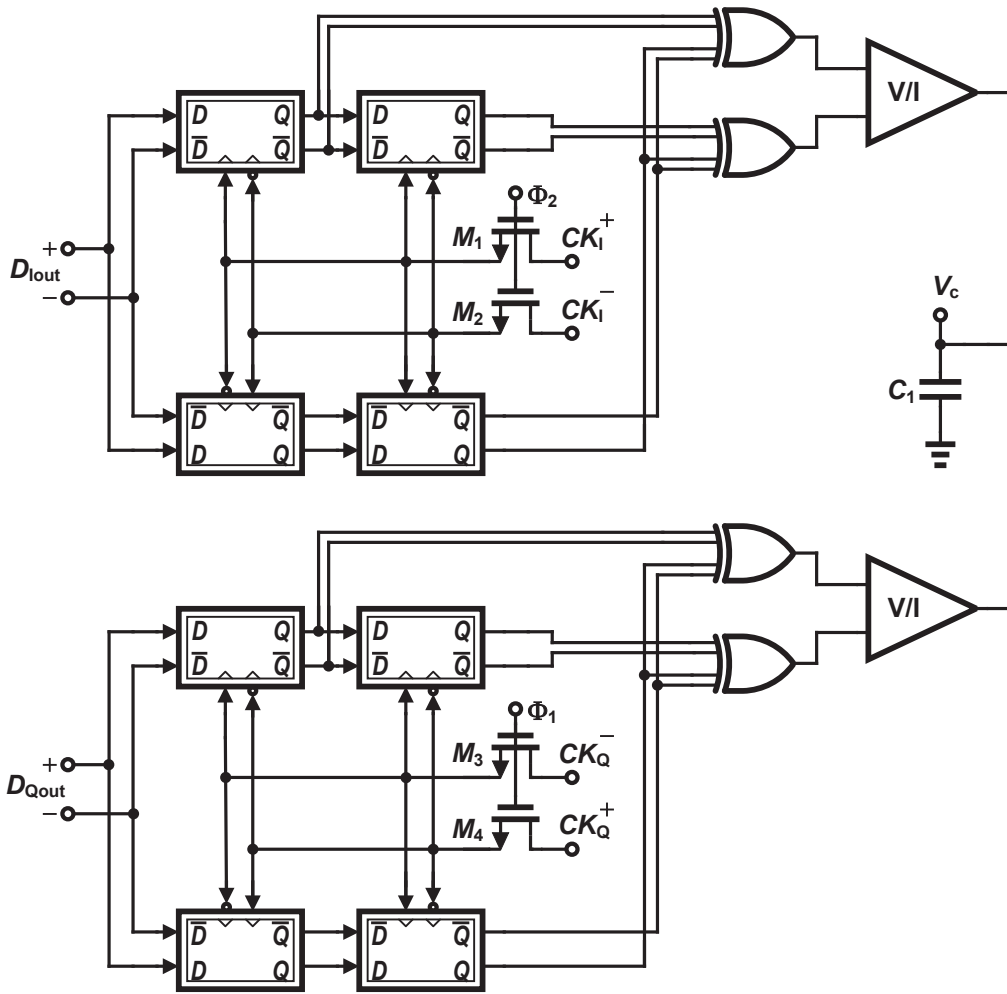
Figure B.3: The proposed CDR architecture for pass-band data.

$M_{1,2}$ and $M_{3,4}$ are used to let the data be sampled only at F_{ref} frequency within the timing windows, which are provided by the Φ_2 and Φ_1 clock phases, respectively. Then, the sampled data is given to the XOR gates to create "early" and "late" signals. The XOR gates drive voltage-to-current (V/I) converters, and the two outputs of the V/I converters are summed in current domain, and the result is applied to the integrating capacitor, i.e., C_1 in Fig. B.3. Having summed the I/Q sub-band PDs together, the final sampling phase will be set so as to an optimum sampling point for both of I/Q sub-bands is achieved. A preliminary study of the performance of this type of CDR indicates that the performance of the proposed circuit is satisfiable, although the statistical delay caused by M_{1-4} can increase DJ, hence, degrade the system jitter performance.

List of Acronyms

- **3D** - **Three**-**D**imensional

- **ADC** - **A**nalog-to-**D**igital **C**onverter

- **AFE** - **A**nalog **F**ront-**E**nd

- **ASIC** - **A**pplication-**S**pecific **I**ntegrated **C**ircuit

- **BB** - **B**ase **B**and

- **BER** - **B**it **E**rror **R**ate

- **BPF** - **B**and **P**ass **F**ilter

- **CML** - **C**urrent-**M**ode **L**ogic

- **CMOS** - **C**omplementary **M**etal-**O**xyde-**S**emicondutor

- **CP** - **C**harg **P**ump

- **CPU** - **C**entral **P**rocessing **U**nit

- **CTLE** - **C**ontinuous-**T**ime **L**inear **E**qualizer

- **DAC** - **D**igital-to-**A**nalog **C**onverter

- **DDR** - **D**ouble **D**ata **R**ate

- **DFE** - **D**ecision **F**eedback **E**qualizer

- **DIMM** - **D**ual **I**n-line **M**emory **M**odule

- **DLL** - **D**elay **L**ocked **L**oop

- **DRAM** - **D**ynamic **R**andom **A**ccess **M**emory

- **FEXT** - **F**ar-**E**nd **C**ross **T**alk

- **FFE** - **F**eed-**F**orward **E**qualizer

- **FIFO** - **F**irst **I**n **F**irst **O**ut

- **FIR** - **F**inite **I**mpulse **R**esponse

- **FOM** - **F**igure-**o**f-**M**erit

- **FPGA** - **F**ield-**P**rogrammable-**G**ate-**A**rray

- **GDDR** - **G**raphics **D**ouble **D**ata **R**ate

- **HPC** - **H**igh-**P**erformance **C**omputing

- **I/O** - **I**nput/**O**utput

- **ICI** - **I**nter-**C**hannel **I**nterference

- **IIR** - **I**nfinite **I**mpulse **R**esponse

- **IoT** - **I**nternet **o**f **T**hings

- **ISI** - **I**nter-**S**ymbol **I**nterference

- **LF** - **L**oop **F**ilter

- **LPF** - **L**ow **P**ass **F**ilter

- **LPDDR** - **L**ow **P**ower **D**ouble **D**ata **R**ate

- **LTI** - **L**inear **T**ime **I**nvariant

- **LUT** - **L**ook-**U**p **T**able

- **LVDS** - **L**ow-**V**oltage **D**ifferential **S**ignaling

- **MDB** - **M**ulti-**D**rop **B**us

- **MDLL** - **M**ultiplying **D**elay **L**ocked **L**oop

- **MT** - **M**ulti-**T**one

- **NRZ** - **N**on-**R**eturn to **Z**ero

- **NRZ/MT** - **N**on-**R**eturn to **Z**ero/**M**ulti-**T**one

- **PAM** - **P**ulse-**A**mplitude **M**odulation

- **PC** - **P**ersonal **C**omputer

- **PCB** - **P**rinted **C**ircuit **B**oard

- **PDF** - **P**robability **D**ensity **F**unction

- **PLL** - **P**hase-**L**ocked **L**oop

- **QAM** - **Q**uadrature **A**mplitude Modulation

- **QPSK** - **Q**uadrature **P**hase **S**hift **K**eying

- **RAM** - **R**andom **A**ccess Memory

- **RX** - **R**eceiver

- **RZ** - **R**eturn to **Z**ero

- **SC** - **S**witch **C**apacitor

- **SCMF** - **S**witched-**C**apacitor **M**ixer/**F**ilter

- **SoC** - **S**ystem-**o**n-**C**hip

- **SPI** - **S**erial **P**eripheral **I**nterface

- **SRAM** - **S**tatic **R**andom **A**ccess Memory

- **TX** - **T**ransmitter

- **TRX** - **T**ransceiver

- **V/I** - **V**oltage-to-**C**urrent

- **XDFE** - **C**ross **D**ecision **F**eedback **E**qualizer

- **ZF** - **Z**ero **F**orcing

Bibliography

[1] Cisco VNI forecast widget @ONLINE, Feb. 2015. `http://ciscovni.com/forecast-widget/index.html`.

[2] `http://www.google.com/about/datacenters/gallery/#/tech`.

[3] Gray Nichol. Chip-to-module interface requirements a system vendor's perspective. In *OIF 400G workshop*, Feb. 2014.

[4] Ken Chang, G. Zhang, and C. Borrelli. Evolution of wireline transceiver standards: Various, most-used standards for the bandwidth demand. *IEEE Solid-State Circuits Mag.*, 7(4):47–52, Fall 2015.

[5] T. Anand, M. Talegaonkar, A. Elkholy, S. Saxena, A. Elshazly, and P.K. Hanumolu. A 7 Gb/s embedded clock transceiver for energy proportional links. *IEEE J. Solid-State Circuits*, 50(12):3101–3119, Dec. 2015.

[6] S. Narendra, L. Fujino, and K. Smith. Through the looking glass?the 2015 edition: trends in solid-state circuits from ISSCC. *IEEE Solid-State Circuits Mag.*, 7(1):14–24, winter 2015.

[7] T. Beukema, M. Sorna, K. Selander, S. Zier, B.L. Ji, P. Murfet, J. Mason, Woogeun Rhee, H. Ainspan, B. Parker, and M. Beakes. A 6.4-Gb/s CMOS SerDes core with feed-forward and decision-feedback equalization. *IEEE J. Solid-State Circuits*, 40(12):2633–2645, Dec. 2005.

[8] T. Toifl, M. Ruegg, R. Inti, C. Menolfi, M. Brandli, M. Kossel, P. Buchmann, P.A. Francese, and T. Morf. A 3.1mW/Gbps 30Gbps quarter-rate triple-speculation 15-tap SC-DFE RX data path in 32nm CMOS. In *IEEE VLSI Symp. Dig. Tech. Papers*, pages 102–103, June 2012.

[9] A. Cevrero, Cosimo Aprile, P. A. Francese, U. Bapst, C. Menolfi, et al. A 5.9mW/Gb/s 7Gb/s/pin 8-lane single-ended RX with crosstalk cancellation scheme using a XCTLE

and 56-tap XDFE in 32nm SOI CMOS. In *IEEE VLSI Symp. Dig. Tech. Papers*, pages C228–C229, June 2015.

[10] A. Amirkhany, A. Abbasfar, V. Stojanovic, and M.A. Horowitz. Practical limits of multi-tone signaling over high-speed backplane electrical links. In *Communications, 2007. ICC '07. IEEE International Conference on*, pages 2693–2698, June 2007.

[11] A. Amirkhany, A. Abbasfar, J. Savoj, M. Jeeradit, B. Garlepp, R.T. Kollipara, V. Stojanovic, and M. Horowitz. A 24 Gb/s software programmable analog multi-tone transmitter. *IEEE J. Solid-State Circuits*, 43(4):999–1009, Apr. 2008.

[12] Gyung-Su Byun, Yanghyo Kim, Jongsun Kim, Sai-Wang Tam, and M.-C.F. Chang. An energy-efficient and high-speed mobile memory I/O interface using simultaneous bi-directional dual (base+RF)-band signaling. *IEEE J. Solid-State Circuits*, 47(1):117–130, Jan. 2012.

[13] S. Ibrahim and B. Razavi. Design requirements of 20-Gb/s serial links using multi-tone signaling. In *Signals, Circuits and Systems, ISSCS 2009 Symposium on*, pages 1–4, July 2009.

[14] Bo Zhang, K. Khanoyan, H. Hatamkhani, H. Tong, K. Hu, S. Fallahi, M. Abdul-Latif, K. Vakilian, I. Fujimori, and A. Brewster. A 28 Gb/s multistandard serial link transceiver for backplane applications in 28 nm CMOS. *IEEE J. Solid-State Circuits*, 50(12):3089–3100, Dec. 2015.

[15] OIF CEI-25G-LR OIF2008.161.12 . *CEI-25G-LR Long Reach Interface*.

[16] CEI-25G-LR and CEI-28G-VSR multi-vendor interoperability testing. *CEI-28G-VSR Very Short Reach Interface*, 2012.

[17] CEI-28G-SR OIF2008.029.12. *CEI-28G-SR Short Reach Interface*.

[18] K. Gopalakrishnan, A. Ren, A. an, A. Farhood, et al. A 40/50/100Gb/s PAM-4 ethernet transceiver in 28nm CMOS. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016.

[19] H-Y. Joo, S-J. Bae, Y-S. Sohn, Y-S. Kim, et al. A 20nm 9Gb/s/pin 8gb GDDR5 dram with an NBTI monitor, jitter reduction techniques and improved power distribution. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016.

[20] K. Chang, F. O'Mahony, E. Alon, Hyeon-Min Bae, N. Da Dalt, and E. Fluhr. F6: I/O design at 25Gb/s and beyond: Enabling the future communication infrastructure for big data. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 1–2, Feb. 2015.

[21] F. O'Mahony, G. Balamurugan, J.E. Jaussi, J. Kennedy, M. Mansuri, S. Shekhar, and B. Casper. The future of electrical i/o for microprocessors. In *VLSI Design, Automation and Test, 2009. VLSI-DAT '09. International Symposium on*, pages 31–34, April 2009.

[22] K. Fukuda, H. Yamashita, G. Ono, R. Nemoto, E. Suzuki, N. Masuda, T. Takemoto, F. Yuki, and T. Saito. A 12.3-mW 12.5-Gb/s complete transceiver in 65-nm CMOS process. *IEEE J. Solid-State Circuits*, 45(12):2838–2849, Dec. 2010.

[23] M. Mansuri, J.E. Jaussi, J.T. Kennedy, Tzu-Chien Hsueh, S. Shekhar, G. Balamuru-gan, F. O'Mahony, C. Roberts, R. Mooney, and B. Casper. A scalable 0.128-1 Tb/s, 0.8-2.6 pJ/bit, 64-lane parallel I/O in 32-nm CMOS. *IEEE J. Solid-State Circuits*, 48(12):3229–3242, Dec. 2013.

[24] Kiarash Gharibdoust, Armin Tajalli, and Yusuf Leblebici. A 7.5mW 7.5Gb/s mixed NRZ/multi-tone serial-data transceiver for multi-drop memory interfaces in 40nm CMOS. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 180–181, Feb. 2015.

[25] K. Therdsteerasukdi, Gyung-Su Byun, J. Ir, G. Reinman, J. Cong, and M.-C.F. Chang. Utilizing radio-frequency interconnect for a many-DIMM DRAM system. *IEEE J. Emerg. Sel. Topics Circuits Syst.*, 2(2):210–227, June 2012.

[26] Kiarash Gharibdoust, Armin Tajalli, and Yusuf Leblebici. A 4x9 Gb/s 1 pJ/b NRZ/multi-tone serial-data transceiver with crosstalk reduction architecture for multi-drop memory interfaces in 40nm CMOS. In *IEEE VLSI Symp. Dig. Tech. Papers*, pages C180–C181, June 2015.

[27] T. Toifl, C. Menolfi, M. Ruegg, R. Reutemann, D. Dreps, et al. A 2.6 mW/Gbps 12.5 Gbps RX with 8-tap switched-capacitor DFE in 32 nm CMOS. *IEEE J. Solid-State Circuits*, 47(4):897–910, Apr. 2012.

[28] V. Stojanovic, A. Ho, B.W. Garlepp, F. Chen, J. Wei, G. Tsang, E. Alon, R.T. Kollipara, C.W. Werner, J.L. Zerbe, and M.A. Horowitz. Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery. *IEEE J. Solid-State Circuits*, 40(4):1012–1026, Apr. 2005.

[29] A. Manian and B. Razavi. A 40-Gb/s 9.2-mW CMOS equalizer. In *IEEE VLSI Symp. Dig. Tech. Papers*, pages C226–C227, June 2015.

[30] Jun Won Jung and B. Razavi. A 25-Gb/s 5-mW cmos CDR/deserializer. In *IEEE VLSI Symp. Dig. Tech. Papers*, pages 138–139, June 2012.

[31] J.F. Bulzacchelli. Equalization for electrical links: Current design techniques and future directions. *IEEE Solid-State Circuits Mag.*, 7(4):23–31, Fall 2015.

[32] S. Kasturia and J.H. Winters. Techniques for high-speed implementation of nonlinear cancellation. *IEEE J. Sel. Areas Commun.*, 9(5):711–717, Jun 1991.

[33] J.F. Bulzacchelli, A.V. Rylyakov, and D.J. Friedman. Power-efficient decision-feedback equalizers for multi-Gb/s CMOS serial links. In *IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, pages 507–510, June 2007.

[34] B. Saltzberg. Performance of an efficient parallel data transmission system. *Communication Technology, IEEE Transactions on*, 15(6):805–811, Dec. 1967.

[35] S. Weinstein and P. Ebert. Data transmission by frequency-division multiplexing using the discrete fourier transform. *Communication Technology, IEEE Transactions on*, 19(5):628–634, Oct. 1971.

[36] B. Hirosaki. An orthogonally multiplexed QAM system using the discrete fourier transform. *Communications, IEEE Transactions on*, 29(7):982–989, Jul. 1981.

[37] A. Hormati, A. Tajalli, C. Walter, K. Gharibdoust, and A. Shokrollahi. A versatile spectrum shaping scheme for communicating beyond notches in multi-drop interfaces. In *DesignCon 2016, Santa Clara, CA, USA*, Jan. 2016.

[38] Kyomin Sohn, Taesik Na, Indal Song, Yong Shim, Wonil Bae, et al. A 1.2 V 30 nm 3.2 Gb/s/pin 4 Gb DDR4 SDRAM with dual-error detection and PVT-tolerant data-fetch scheme. *IEEE J. Solid-State Circuits*, 48(1):168–177, Jan. 2013.

[39] Addendum No. 1 to JESD79-3 - 1.35 V DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866. *JEDEC Std., JESD79-3-1A.01*, May 2013.

[40] B. Jacob, D. Wang, and S. Ng. *Memory Systems: Cache, DRAM, Disk.* Morgan Kaufmann, 2008.

[41] F. Aryanfar and A. Amirkhany. A low-cost resonance mitigation technique for multidrop memory interfaces. *IEEE Trans. Circuits Syst. II*, 57(5):339–342, May 2010.

[42] Kiarash Gharibdoust, Armin Tajalli, and Yusuf Leblebici. A 4x9 Gb/s 1 pJ/b hybrid NRZ/multi-tone I/O with crosstalk and ISI reduction for dense interconnects. *IEEE J. Solid-State Circuits*, in press, 2016.

[43] Behzad Razavi. *Design of Integrated Circuits for Optical Comunications.* McGraw-Hill, Avenue of the Americas, NY, USA, 1 edition, 2003.

[44] S. Sidiropoulos and M. Horowitz. A 700-Mb/s/pin CMOS signaling interface using current integrating receivers. *Solid-State Circuits, IEEE Journal of*, 32(5):681–690, May 1997.

[45] Behzad Razavi. *RF Microelectronics*. Prentice Hall Press, Upper Saddle River, NJ, USA, 2 edition, 2012.

[46] R. Reutemann, M. Ruegg, F. Keyser, J. Bergkvist, D. Dreps, T. Toifl, and M. Schmatz. A 4.5mW/Gb/s 6.4Gb/s 22+1-lane source-synchronous link RX core with optional cleanup PLL in 65nm CMOS. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 160–161, Feb. 2010.

[47] A. Tajalli and S.M. Atarodi. A compact biquadratic gm-C filter structure for low-voltage and high frequency applications. In *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2003.

[48] Kwang-Il Oh, Lee-Sup Kim, Kwang-Il Park, Young-Hyun Jun, Joo Sun Choi, and Kinam Kim. A 5-Gb/s/pin transceiver for DDR memory interface with a crosstalk suppression scheme. *IEEE J. Solid-State Circuits*, 44(8):2222–2232, Aug. 2009.

[49] Young-Sik Kim, Seon-Kyoo Lee, Seung-Jun Bae, Young-Soo Sohn, Jung-Bae Lee, Joo Sun Choi, Hong-June Park, and Jae-Yoon Sim. An 8Gb/s quad-skew-cancelling parallel transceiver in 90nm CMOS for high-speed DRAM interface. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 136–138, Feb. 2012.

[50] Woo-Yeol Shin, Gi-Moon Hong, Hyongmin Lee, Jae-Duk Han, Sunkwon Kim, Kyu-Sang Park, Dong-Hyuk Lim, Jung-Hoon Chun, Deog-Kyoon Jeong, and Suhwan Kim. A 4.8Gb/s impedance-matched bidirectional multi-drop transceiver for high-capacity memory interface. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 494–496, Feb. 2011.

[51] K. Kaviani, M. Bucher, B. Su, B. Daly, B. Stonecypher, et al. A 6.4Gb/s near-ground single-ended transceiver for dual-rank DIMM memory interface systems. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 306–307, Feb. 2013.

[52] Mingta Hsieh and G. Sobelman. Architectures for multi-gigabit wire-linked clock and data recovery. *IEEE Circuits Syst. Mag.*, 8(4):45–57, Fourth Quarter 2008.

[53] P. Gui, F.E. Kiamilev, Xiaoqing Wang, M.J. MacFadden, Xingle Wang, Nick Waite, M.W. Haney, and C. Kuznia. A source-synchronous double-data-rate parallel optical transceiver ic. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, 13(7):833–842, July 2005.

[54] G. Chien and P.R. Gray. A 900-MHz local oscillator using a DLL-based frequency multiplier technique for PCS applications. *IEEE J. Solid-State Circuits*, 35(12):1996–1999, Dec. 2000.

[55] B. Razavi. The role of PLLs in future wireline transmitters. *IEEE Trans. Circuits Syst. I*, 56(8):1786–1793, Aug. 2009.

[56] A. Elshazly, R. Inti, B. Young, and P.K. Hanumolu. Clock multiplication techniques using digital multiplying delay-locked loops. *IEEE J. Solid-State Circuits*, 48(6):1416–1428, June 2013.

[57] M.-J.E. Lee, W.J. Dally, T. Greer, Hiok-Tiaq Ng, R. Farjad-rad, J. Poulton, and R. Senthinathan. Jitter transfer characteristics of delay-locked loops - theories and design techniques. *IEEE J. Solid-State Circuits*, 38(4):614–621, Apr. 2003.

[58] Keng-Jan Hsiao and Tai-Cheng Lee. The design and analysis of a fully integrated multiplying DLL with adaptive current tuning. *IEEE J. Solid-State Circuits*, 43(6):1427–1435, June 2008.

[59] Tai-Cheng Lee and Keng-Jan Hsiao. The design and analysis of a DLL-based frequency synthesizer for UWB application. *IEEE J. Solid-State Circuits*, 41(6):1245–1252, June 2006.

[60] Chi-Nan Chuang and Shen-Iuan Liu. A 40 GHz DLL-based clock generator in 90nm CMOS technology. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 178–595, Feb. 2007.

[61] Fang-Ren Liao and Shey-Shi Lu. A programmable edge-combining DLL with a current-splitting charge pump for spur suppression. *IEEE Trans. Circuits Syst. II*, 57(12):946–950, Dec. 2010.

[62] Hae-Kang Jung, Kyoungho Lee, Jong-Sam Kim, Jae-Jin Lee, Jae-Yoon Sim, and Hong-June Park. A 4 Gb/s 3-bit parallel transmitter with the crosstalk-induced jitter compensation using TX data timing control. *IEEE J. Solid-State Circuits*, 44(11):2891–2900, Nov. 2009.

[63] J.F. Bulzacchelli, C. Menolfi, T.J. Beukema, D.W. Storaska, J. Hertle, et al. A 28-Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32-nm SOI cmos technology. *IEEE J. Solid-State Circuits*, 47(12):3232–3248, Dec. 2012.

[64] T. Musah, J. Jaussi, G. Balamurugan, S. Hyvonen, T.-C. Hsueh, et al. A 4-32 Gb/s bidirectional link with 3-tap FFE/6-tap DFE and collaborative CDR in 22 nm CMOS. *IEEE J. Solid-State Circuits*, 49(12):3079–3090, Dec. 2014.

[65] Taehyoun Oh and R. Harjani. A 12-Gb/s multichannel I/O using MIMO crosstalk cancellation and signal reutilization in 65-nm CMOS. *IEEE J. Solid-State Circuits*, 48(6):1383–1397, June 2013.

[66] G. Balamurugan, J. Kennedy, G. Banerjee, J.E. Jaussi, M. Mansuri, F. O'Mahony, B. Casper, and R. Mooney. A scalable 5-15 Gbps, 14-75 mw low-power I/O transceiver in 65 nm CMOS. *IEEE J. Solid-State Circuits*, 43(4):1010–1019, Apr. 2008.

[67] W.T. Beyene and A. Amirkhany. Controlled intersymbol interference design techniques of conventional interconnect systems for data rates beyond 20 Gbps. *IEEE Trans. Advanced Packaging*, 31(4):731–740, Nov. 2008.

[68] W. Volkaerts, N. Van Thienen, and P. Reynaert. An FSK plastic waveguide communication link in 40nm CMOS. In *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pages 178–179, Feb. 2015.

[69] M.H. Nazari and A. Emami-Neyestanak. A 15-Gb/s 0.5-mW/Gbps two-tap DFE receiver with far-end crosstalk cancellation. *IEEE J. Solid-State Circuits*, 47(10):2420–2432, Oct. 2012.

[70] Taehyoun Oh and R. Harjani. A 6-Gb/s MIMO crosstalk cancellation scheme for high-speed I/Os. *IEEE J. Solid-State Circuits*, 46(8):1843–1856, 2011.

[71] Kiarash Gharibdoust, Armin Tajalli, and Yusuf Leblebici. Hybrid NRZ/multi-tone serial data transceiver for multi-drop memory interfaces. *IEEE J. Solid-State Circuits*, 50(12), 2015.

[72] B.K. Casper, M. Haycock, and R. Mooney. An accurate and efficient analysis method for multi-Gb/s chip-to-chip signaling schemes. In *IEEE VLSI Symp. Dig. Tech. Papers*, pages 54–57, June 2002.

[73] V. Stojanovic and M. Horowitz. Modeling and analysis of high-speed links. In *IEEE Custom Integr. Circuits Conf.*, pages 589–594, Sept. 2003.

[74] B. Ahmad. Performance specification of interconnect. In *DesignCon 2003, Santa Clara, CA, USA*, Jan. 2003.

[75] Kyung Suk Oh, F. Lambrecht, Sam Chang, Qi Lin, Jihong Ren, Chuck Yuan, J. Zerbe, and V. Stojanovic. Accurate system voltage and timing margin simulation in high-speed I/O system designs. *IEEE Trans. Adv. Packag.*, 31(4):722–730, Nov. 2008.

[76] J. Caroselli and C. Liu. An analytic system model for high speed interconnects and its application to the specification of signaling and equalization architectures for 10

Gbps backplane communication. In *DesignCon 2004, Santa Clara, CA, USA*, Jan. 2006.

[77] Kangmin Hu, L. Wu, and P.Y. Chiang. A comparative study of 20-Gb/s NRZ and duobinary signaling using statistical analysis. *IEEE Trans. VLSI Syst.*, 20(7):1336–1341, July 2012.

[78] Kangmin Hu, Tao Jiang, Jingguang Wang, F. O'Mahony, and P.Y. Chiang. A 0.6 mW/Gb/s, 6.4-7.2 Gb/s serial link receiver using local injection-locked ring oscillators in 90 nm CMOS. *IEEE J. Solid-State Circuits*, 45(4):899–908, Apr. 2010.

[79] M. Hossain and A.C. Carusone. 7.4 Gb/s 6.8 mW source synchronous receiver in 65 nm CMOS. *IEEE J. Solid-State Circuits*, 46(6):1337–1348, June 2011.

[80] Sang-Hye Chung, Lee-Sup Kim, Seung-Jun Bae, Kyoung-Soo Ha, Jung-Bae Lee, and Joo Sun Choi. An 8Gb/s forwarded-clock I/O receiver with up to 1GHz constant jitter tracking bandwidth using a weak injection-locked oscillator in 0.13 um CMOS. In *IEEE VLSI Symp. Dig. Tech. Papers*, pages 84–85, June 2011.

[81] Seong-Jun Song, Sung Min Park, and Hoi-Jun Yoo. A 4-Gb/s CMOS clock and data recovery circuit using 1/8-rate clock technique. *IEEE J. Solid-State Circuits*, 38(7):1213–1219, July 2003.

[82] J.L. Sonntag and J. Stonick. A digital clock and data recovery architecture for multi-gigabit/s binary links. *IEEE J. Solid-State Circuits*, 41(8):1867–1875, Aug. 2006.

[83] J.D.H. Alexander. Clock recovery from random binary signals. *Electronics Letters*, 11(22):541–542, Oct. 1975.

[84] Jri Lee, K.S. Kundert, and B. Razavi. Analysis and modeling of bang-bang clock and data recovery circuits. *IEEE J. Solid-State Circuits*, 39(9):1571–1580, Sept. 2004.

[85] Jri Lee and Ke-Chung Wu. A 20-Gb/s full-rate linear clock and data recovery circuit with automatic frequency acquisition. *IEEE J. Solid-State Circuits*, 44(12):3590–3602, Dec. 2009.

Kiarash Gharibdoust

Chemin des Abbesses 18
1027 Lonay, Switzerland
+41(0)787006612
Nationality: Iranian (Swiss B permit)
Birth Year: 1984
kiarash.gharibdoust@gmail.com
https://www.linkedin.com/in/kiarashgharibdoust

PROFILE

- Proactive R&D and Analog/Mixed-signal circuit designer with strong motivation in seeking innovative solution for cutting-edge IC products.

- Expertise in high-speed wireline and wireless custom IC design in advanced CMOS technology node.

- Remarkable presentation skill sharpened through experiences at prestigious international conferences.

WORK EXPERIENCE

EPFL, Microelectronic System Laboratory (LSM)   Lausanne, Switzerland

Research Assistant   February 2012 – February 2016

- Hybrid NRZ/Multi-Tone Serial Data Transceiver for Memory Interfaces, mandated by Kandou Bus SA

- High-Speed and Low-Power Multi-Phase Clock Generation for Wireline Applications

- Crosstalk Reduction Techniques for Parallel I/O in Dense Interconnects

Kandou Bus SA   Lausanne, Switzerland

Contractor   February 2012 – July 2012

July 2015 – August 2015

- Advanced Low-Power Techniques for High-Speed Wireline Transceivers

- Multi-Tone Signaling for Communicating beyond 100Gb/s/pin over Backplane Channel

Sharif University of Technology, Integrated System Design Laboratory (ISDL)   Tehran, Iran

Junior Analog Design Engineer   March 2010 – December 2011

- Design and Implementation of X-Band Phased-Array Transceiver in 180nm CMOS

Sharif University of Technology, Electronics Research Institute (ERI)   Tehran, Iran

Developer Engineer   December 2008 – December 2009

- Design and Software Implementation of Audio Streaming Channel over ZigBee Network

Sharif University of Technology, Integrated System Design Laboratory (ISDL)   Tehran, Iran

Research Assistant   September 2006 – October 2008

- Design and Implementation of Low-Noise Band-Pass Filter for FM Receivers

EDUCATION

Swiss Federal Institute of Technology in Lausanne (EPFL)   Lausanne, Switzerland
Doctoral of Philosophy (PhD) in Microsystems and Microelectronics   Feb. 2012- Feb. 2016
Supervisor: Prof. Yusuf Leblebici

Sharif University of Technology (SUT)   Tehran, Iran
Master in Electronic Circuits (Major of Microelectronic Circuits)   Sept. 2006- Oct. 2008
Supervisor: Prof. Mehrdad Sharif Bakhtiar

Iran University of Science and Technology (IUST)   Tehran, Iran
Bachelor in Electrical Engineering (Major of Electronics)   Sept. 2002- Aug. 2006

AWARDS / HONORS

- IEEE Solid-State Circuits Society Student Travel Grant Award (STGA) for ISSCC 2016.
- ISSCC Certificate of Recognition for 2015 Demonstration Session.
- Ranked 1st among Bachelor graduates, with highest honors, Iran University of Science and Technology.
- Ranked 2nd (Silver Medal) in 2006 National Electrical Engineering Olympiad.
- Ranked 2nd in Nationwide M.Sc. Entrance Exam of more than 14,000 participants.

SKILLS / INTERESTS

- **Language:** English: fluent (C1), French: upper intermediate (B2), Farsi (Native speaker)
- **CAD Tools:** Cadence Virtuoso, Calibre, Agilent ADS, Momentum ADS, ANSYS HFSS, HSPICE, Modelsim, Encounter Digital Implementation (EDI), Altium designer
- **Programing Language:** Verilog, C, VHDL, Verilog-A, Matlab
- **Text editing and OS:** Latex, Lyx, MS Office Suite, Adobe Illustrator, MS Windows, Linux, Mac OSX
- **Extracurricular Activities:** Alpine sports, Cycling, Persian-Swiss fusion cuisine, travelling

MAIN PUBLICATIONS

- K. Gharibdoust, A. Tajalli, Y. Leblebici, "A 7.5mW 7.5Gb/s Mixed NRZ/Multi-Tone Serial Data Transceiver for Multi-Drop Memory Interfaces in 40nm CMOS," *ISSCC Dig. Tech.* Papers, pp. 180-181, 2015.
- K. Gharibdoust, A. Tajalli, Y. Leblebici, "A 4×9 Gb/s 1 pJ/b NRZ/Multi-Tone Serial-Data Transceiver with Xtalk Reduction Architecture for Multi-Drop Memory Interfaces in 40nm CMOS," *Symposium on VLSI Circuit (VLSIC)*, pp. C180-C181, June 2015.
- K. Gharibdoust, A. Tajalli, Y. Leblebici, "Hybrid NRZ/Multi-Tone Serial Data Transceiver for Multi-Drop Memory Interfaces," *IEEE Journal of Solid State Circuits (JSSC),* vol. 50, num. 12, 2015.
- K. Gharibdoust, A. Tajalli, Y. Leblebici, "A 4×9 Gb/s 1 pJ/b Hybrid NRZ/Multi-Tone I/O with Crosstalk and ISI Reduction for Dense Interconnects," *IEEE Journal of Solid State Circuits (JSSC),* vol. 51, num. 4*, 2016.
- K. Gharibdoust, N. Mousavi, M. Kalantari, M. Moezzi, A. Medi, "A Fully Integrated 0.18-um CMOS Transceiver Chip for X-Band Phased-Array Systems," *IEEE Transaction on Microwave Theory and Techniques (MTT)*, vol. 60, num. 7, pp. 2192-2202, 2012.
- K. Gharibdoust, M. Sharif Bakhtiar, "A Method for Noise Reduction in Active-RC Circuits," *IEEE Transaction on Circuits and Systems-II, Express Briefs (TCAS-II)*, vol. 58, num. 12, pp. 906-910, 2011.