Transparent Electrodes in Silicon Heterojunction Solar Cells: Influence on Contact Passivation

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***Abstract*—Charge carrier collection in silicon heterojunction solar cells occurs via intrinsic/doped hydrogenated amorphous silicon layer stacks deposited on the crystalline silicon wafer surfaces. Usually, both the electron and hole collecting stacks are externally capped by an n-type transparent conductive oxide, which is primarily needed for carrier extraction. Earlier, it has been demonstrated that the mere presence of such oxides can affect the carrier recombination in the crystalline silicon absorber. Here, we present a detailed investigation of the impact of this phenomenon on both the electron and hole collecting sides, including its consequences for the operating voltages of silicon heterojunction solar cells. Based on our findings, we define guiding principles for improved passivating contact design for high-efficiency silicon solar cells.**

***Index Terms*—Amorphous silicon, charge carrier lifetime, crystalline silicon, heterojunctions, passivating contacts, photovoltaic cells, solar cells.**

I. Introduction

TRANSPARENT conductive oxides (TCOs) play an important role in silicon heterojunction (SHJ) solar cells. Two obvious tasks that these layers need to fulfill are efficient light coupling into the silicon wafer and conduction of electrical current to the front metal grid [1]. In addition, they also should guarantee efficient transverse carrier extraction from the electron and hole collectors of the device. These charge carrier collectors consist of thin intrinsic hydrogenated amorphous silicon [a-Si:H(*i*)] surface passivation films, capped by n- and p-type doped hydrogenated amorphous silicon films [hereafter abbreviated as "a-Si:H(*n*)" and "a-Si:H(*p*)"], respectively. For such transverse carrier extraction to be efficient, at least two requirements need to be fulfilled. First, the TCOs should yield minimal contact resistivity needed for efficient carrier transport. Second, the TCOs (and their deposition methods) should not degrade the surface passivation properties of the underlying layers. The more these two requirements are fulfilled, the higher the "carrier selectivity" of the contact will be, collecting one carrier type while repelling the other. In practice, these two requirements critically depend on the energetic line-up of the TCO with the silicon layers underneath, but so far it remains elusive to what extent these phenomena are interlinked.

In this paper, we mainly focus on this second requirement, identifying the conditions for best contact passivation in SHJ solar cells. By carrier lifetime measurements, we first probe the influence on passivation of the doped a-Si:H film thickness in SHJ charge carrier collectors, yet uncapped by TCOs. Then, we investigate how the doping of TCO films affect the passivation of underlying a-Si:H layer stacks. We pay specific attention to both electron and hole contacts, defined as a-Si:H(*i*)/a-Si:H(*n*) (hereafter abbreviated as "*in*") and a-Si:H(*i*)/a-Si:H(*p*) (hereafter abbreviated as "*ip*") stacks, respectively, capped by TCOs. Importantly, throughout the whole paper, we refer to TCOs as standard n-type TCO materials.

Next, we report on illumination intensity versus open-circuit voltage ($V_{\rm oc}$) measurements (i.e., the so-called suns–$V_{\rm oc}$ curves [2]) of SHJ devices, featuring TCO films with a variety of electrical properties. The $V_{\rm oc}$ at low illumination intensity ($<$1 suns) is directly affected by surface passivation. Conversely, tracking the $V_{\rm oc}$ of SHJ devices under very high illumination intensities ($>$10 suns) has been argued to give insight in the carrier extraction properties of the involved contacts, especially at the a-Si:H(*p*)/TCO interface [3], [4]. Here, to identify possible correlations between the TCO impact on surface passivation and on carrier extraction, we study $V_{\rm oc}$ at high and low illumination intensities, respectively. The presented methodology can easily be extended to other solar cell concepts employing passivating contacts [5]–[10].

To conclude, we analyze the implications of our findings on the design of high-efficiency SHJ solar cells and discuss possible routes toward optimum contact passivation.

II. Experimental Details

Crystalline Si (c-Si) wafers (4-in float-zone, n-type, nominal resistivity of 2.8 Ω·cm) were textured and cleaned by a wet-chemical process. Subsequently, they were dipped in a diluted hydrofluoric solution to strip off the chemical oxide. Thin blanket intrinsic/doped a-Si:H layer stacks were deposited on both wafer surfaces in a plasma-enhanced chemical vapor deposition (PECVD) reactor, at 200 °C. More details on our a-Si:H

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stacks for hole and electron collection can be found elsewhere [11]. The thickness of the standard a-Si:H layers, measured by spectroscopic ellipsometry on a planar glass substrate, equals 10 nm for the a-Si:H(*i*) layer and 14 and 8 nm for the a-Si:H(*n*) and a-Si:H(*p*) layer, respectively. Indium tin oxide (ITO) films were sputtered from an In_2O_3:Sn target [12], nominally at room temperature. Boron-doped zinc oxide (ZnO:B) layers were deposited by low-pressure chemical vapor deposition (LPCVD) [13] at a temperature of around 175 °C. Further details on the used deposition system and related methodology can be found elsewhere [14]. The wafer edges were protected during TCO depositions and remained uncoated. During each TCO deposition, we codeposited films on a bare glass witness sample in order to measure TCO properties (thickness, resistivity, carrier density, carrier mobility). The film thickness was assessed by a stylus profilometer, its resistivity by four-point-probe measurements, and the carrier density and mobility by Hall effect measurements. TCO layer thicknesses, measured on glass, range between 180–250 nm, which are typical TCO thicknesses used in our SHJ device back contacts [1], [15]. In the case of the least doped ZnO:B film, the carrier density and mobility values, extracted from Hall measurements, are not considered reliable, due to the excessively high film resistivity.

The effective minority carrier lifetime of the passivated c-Si wafers, $\tau_{\rm eff}$, was assessed in the excess minority charge carrier density (Δn) range $10^{14} - 10^{16}{\rm cm}^{-3}$, by transient photoconductance decay measurements [16]. To cover the entire device-relevant Δn range, each sample was measured in two distinct ranges (high $> 10^{15}{\rm cm}^{-3}$ and low $< 10^{15}{\rm cm}^{-3}$). Subsequently, the two datasets were stitched together to build the final $\tau_{\rm eff}(\Delta n)$ curve. Suns–$V_{\rm oc}$ measurements were acquired with a standard suns–$V_{\rm oc}$ setup [2]. Similarly as for $\tau_{\rm eff}(\Delta n)$ measurements, suns–$V_{\rm oc}$ measurements were taken at *high* (∼5–200 suns) and *low* (<5 suns) illumination intensities and then merged in final *high–low* suns–$V_{\rm oc}$ curves.

III. Results and Discussion

A. Effects on Effective Minority Carrier Lifetime

Photoconductance decay lifetime measurements yield $\tau_{\rm eff}$ versus Δn curves. The characteristic shape of these data reveals direct information about the nature of the sample's surface passivation (chemical or field effect). In the case of a-Si:H(*i*) passivating films, the passivation is mainly chemical, resulting in low a-Si:H/c-Si interface defect densities [17]. Despite this, for the case of a-Si:H-based charge carrier collectors, important differences in $\tau_{\rm eff}$ values at Δn values lower than $\sim 10^{15}{\rm cm}^{-3}$ can be observed and are associated with field-effect passivation (or the lack thereof) [18], [19].

To quantitatively assess the impact of such Δn dependencies on device performance, we chose as metrics the implied fill factor (implied-FF) [20] and the implied open-circuit voltage (implied-$V_{\rm oc}$) [16]. Throughout this entire paper, we explicitly use the prefix "implied-" for all quantities derived from carrier lifetime data. In the following, we stepwise build up our hole and electron contacts and systematically verify the impact of each layer on their passivation properties.

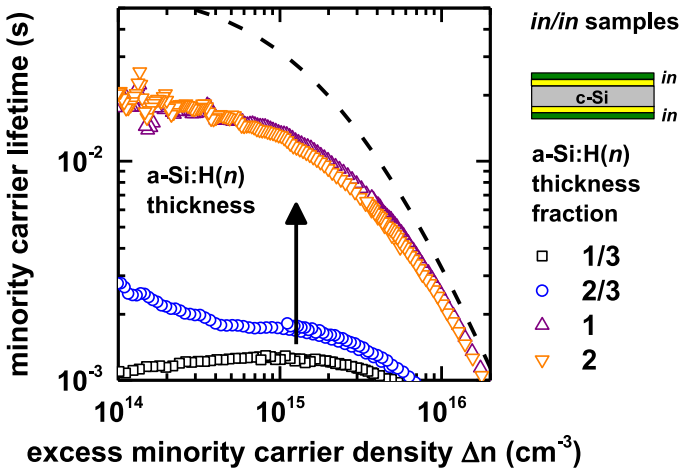

Fig. 1. Measurements of $\tau_{\rm eff}(\Delta n)$ on n-type c-Si absorbers, featuring a symmetric electron collector (*in/in* samples), of which the a-Si:H(*n*) layer thickness was varied from one third to twice its standard thickness. The combined Auger and radiative limit is indicated by the dashed line [22].

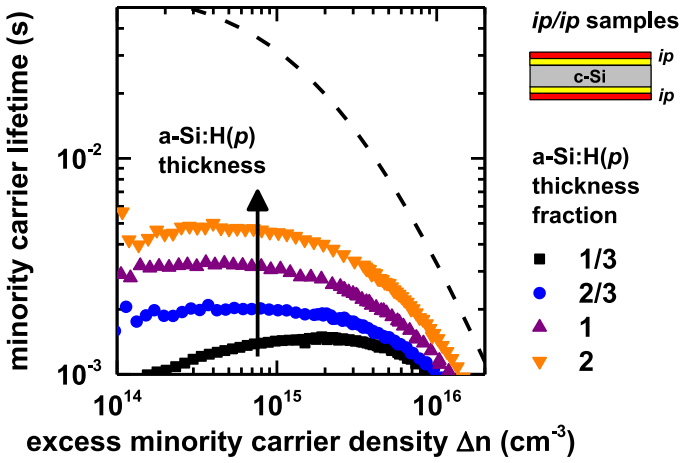

Fig. 2. Measurements of $\tau_{\rm eff}(\Delta n)$ on n-type c-Si absorbers, featuring a symmetric hole collector (*ip/ip* samples), of which the a-Si:H(*p*) layer thickness was varied from one third to twice its standard thickness. The combined Auger and radiative limit is indicated by the dashed line [22].

1) Impact of Doped a-Si:H layers[1]*:* To simplify the interpretation of our results, we study n-type c-Si wafers featuring either symmetric *in* or *ip* stacks (hereafter referred to as "*in/in* samples" and "*ip/ip* samples," respectively). The thickness of the doped a-Si:H layers was varied between one-third to twice their standard thickness, as typically used in our devices [21] (see also Section II). Figs. 1 and 2 give measured $\tau_{\rm eff}(\Delta n)$ data for both types of charge carrier collectors under study, not yet capped by any TCO. In either case, we witness lower $\tau_{\rm eff}$ for thinner doped a-Si:H layers. This loss seems particularly important at low Δn, which especially impacts implied-FF values. Implied-$V_{\rm oc}$ values increase slightly with increasing doped a-Si:H layer thicknesses; the overall variation is < 10 mV and < 20 mV

[1]For this experiment, the a-Si:H layer stacks were deposited in a different PECVD reactor, compared with all other a-Si:H layers reported in this study.

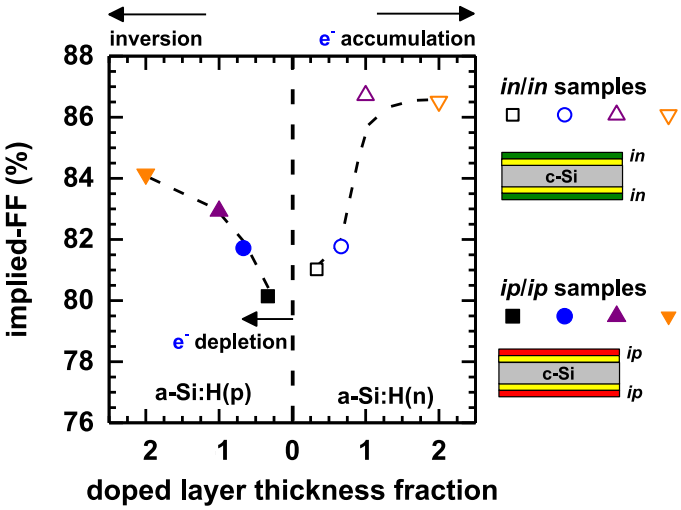

Fig. 3. Implied-FF values extracted from $\tau_{\rm eff}(\Delta n)$ curves measured on n-type c-Si absorbers featuring symmetric electron (*in/in* samples) and hole (*ip/ip* samples) collectors for varying doped a-Si:H layer thickness fractions (see Figs. 1 and 2). Regions corresponding to electron (e^-) accumulation, depletion, and inversion conditions at the c-Si wafer surface are also indicated.

in the case of the a-Si:H(p) and a-Si:H(n) layer thickness series, respectively. Implied-FF values vary more significantly. However, one can obtain values $\geq$84% for sufficiently thick a-Si:H(p) layers and $\geq$86% for sufficiently thick a-Si:H(n) layers (see Fig. 3). Such thickness dependence may be the outcome of two competing mechanisms. On the one hand, the presence of the defective (doped) a-Si:H overlayers may lead to recombination of carriers tunneling through the thin a-Si:H(i) layers [23]. On the other hand, their recombination is conditioned by surface field effects, as those discussed in more details below, which gain in importance with doped layer thickness.

Remarkably, very similar implied-FF trends were observed also by external corona charging of test structures featuring a simple a-Si:H(i)/n-type c-Si wafer structure [24]. To enable corona charging, these samples were capped by a 1-μm-thick silicon oxide dielectric film. The extremely good correspondence of the results achieved in these two different experiments highlights the prime importance of field effects on the overall surface passivation associated to state-of-the-art a-Si:H-based carrier collectors. From this perspective, the layer-thickness dependencies observed in Figs. 1–3 are driven mainly by the work function (WF) of the different n- and p-type doped a-Si:H layer, yielding field effects inside the wafer, also needed for (selective) charge collection. For the electron collector, the a-Si:H(n) layer introduces a downward band bending inside the wafer (electron accumulation, hole depletion). Conversely, for the hole collector, the presence of the a-Si:H(p) layer results in a strong upwards band bending inside the wafer that can result in surface inversion (hole accumulation, electron depletion) [25]. In our experiment, different asymptotic implied-FF values ($\sim$86% and $\sim$84% for increasingly thick a-Si:H(n) and a-Si:H(p) films, respectively) are attributed to these two opposite situations. Intriguingly, these asymptotic values also match very closely those determined in the corona charging experiment by Reusch *et al.* [24]. They can be explained by larger interface defect capture cross sections for electrons versus holes, similarly to the case of thermal silicon oxide passivated surfaces [26]. It is worth noting that our typical a-Si:H(i) film provides better surface passivation, and better implied-FF values, without than with the thin doped a-Si:H overlayers. This latter observation can be put in relation with the amphoteric nature of Si dangling bonds at the interface a-Si:H(i)/c-Si, which determines a carrier recombination minimum in case of comparable free hole and electron densities, i.e., low band bending at c-Si surface [19]. The variations observed for the $\tau_{\rm eff}(\Delta n)$ data, for changing doped layer thicknesses, are most likely a distinctive signature of efficient hole and electron collectors. They demonstrate the capability of the doped a-Si:H layers to induce a certain electrical field in the proximity of the c-Si wafer surface despite the presence of the a-Si:H(i) passivating film.

2) Impact of Transparent Conductive Oxides: The next step in contact fabrication consists in the deposition of a TCO on the doped a-Si:H films. Earlier, it was already established that deposition of TCOs on *ip* stacks (i.e., hole collectors) can result in additional Δn dependences of the wafer surface passivation [27]–[30], leading to a reduction in $\tau_{\rm eff}$ values at low Δn values ($\Delta n < 10^{15}{\rm cm}^{-3}$). This was reported for a variety of TCOs, including aluminum doped zinc oxide (ZnO:Al) [27], [29], [30] and ITO films [28], [29]. Numerical simulations suggested that the $\tau_{\rm eff}$ variation at low Δn is caused by the presumed existence of an ultrathin highly defective (recombination-active) layer in-between the a-Si:H(p) layer and ITO [28]. However, although some TCO deposition methods can cause damage to underlying films [31], the described $\tau_{\rm eff}$ variations were also observed using ultrasoft deposition techniques such as atomic layer deposition [29], [30], and vanished after TCO removal via chemical etching [27], [30]. Therefore, the most accepted physical interpretation associates this phenomenon rather to the WF of the bare TCO film, being lower than the one of the a-Si:H(p) layer. This energetic mismatch may deteriorate the field effect of the *ip* stack, reducing the band bending—and thus hole accumulation—at the n-type c-Si wafer surface. In support of this, the presence of a ZnO:Al layer capping an *ip* layer stack was observed, by surface photovoltage measurements, to result in band bending modifications at the n-type c-Si wafer surface [27]. For a schematic representation of the TCO-induced effects on c-Si band bending, at the hole contact, see [29]. According to this interpretation, it is reasonable to expect variations in $\tau_{\rm eff}$, at low Δn, with changing TCO electrical properties such as the TCO carrier density and WF. To clarify further the implications of the TCO layer on the passivation properties of the substrate underneath, we now present a more detailed study, starting with ITO because it is one of the most commonly used TCO materials in high-efficiency SHJ devices [32].

3) Sputtered Indium Tin Oxide: In this study, we again fabricated symmetric *in/in* and *ip/ip* samples, this time using a-Si:H doped layers with device-relevant thicknesses but adding ITO films with a variety of electrical properties to both wafer surfaces. We then track the effect of these different films on the $\tau_{\rm eff}(\Delta n)$ data. It is well known that oxygen vacancies in ITO dictate material carrier density and mobility [33]. Hence, by

TABLE I
ELECTRICAL PARAMETERS OF ITO LAYERS

Layer	Carrier density (cm^{-3})	Hall Mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	ρ_{ITO} ($\Omega \cdot cm$)
ITO_1	4.0×10^{19}	14.2	1.1×10^{-2}
ITO_2	1.0×10^{20}	18.0	3.4×10^{-3}
ITO_3	5.9×10^{20}	28.8	3.7×10^{-4}

The values are measured after postdeposition annealing for 20 min at 200 °C (coherently with reported $\tau_{\rm eff}(\Delta n)$ measurements).

varying solely the oxygen partial pressure during ITO deposition, we achieved ITO film carrier densities in the range of 10^{19}–10^{20} cm^{-3}, yielding resistivities comprised between 10^{-2} and 10^{-4} $\Omega \cdot cm$ (see Table I). The recorded mobility increase, in ITO films with higher carrier densities, is most likely related to grain barrier-limited carrier transport [34]. This range of materials also includes the ITO films we use in our state-of-the-art n-type SHJ devices, featuring hole collection at the front (hereafter denoted as "*standard*-SHJ").

As already reported earlier [29], [31], following ITO sputtering, an overall degradation of the measured $\tau_{\rm eff}(\Delta n)$ curve is seen. Succeeding ITO deposition, the samples were annealed for 20 min at 200 °C. This treatment recovers passivation, but not for low Δn values, which is linked again to field effects further discussed below. Fig. 4 shows the $\tau_{\rm eff}(\Delta n)$ data, after deposition of solely the a-Si:H layers and after ITO sputtering followed by postdeposition annealing.

In the case of the *in/in* samples, we observed only a slight increase in $\tau_{\rm eff}$, which is comparable for all the ITO films tested here, at least for Δn down to $\sim 5 \times 10^{14} cm^{-3}$. Implied-$V_{\rm oc}$ values are all comprised in the range 732–735 mV and implied-FF in the range 83.2–83.8%.

In contrast, for the *ip/ip* samples, the measured $\tau_{\rm eff}(\Delta n)$ data show a stronger decrease for increasing ITO conductivity and carrier density. Implied-$V_{\rm oc}$ values, extracted from the $\tau_{\rm eff}(\Delta n)$ curves reported in Fig. 4, range from 736 mV (layer ITO_1) to 726 mV (layer ITO_3), whereas implied-FF values decrease from 83.8% (layer ITO_1) to 81.8% (layer ITO_3). It is noteworthy that the relative variation in measured implied-FF values is higher than that in implied-$V_{\rm oc}$ values. Considering the data shown in Fig. 4, converted to a suns–implied-$V_{\rm oc}$ plot [16] given in Fig. 5, we can directly visualize the expected impact of the observed phenomena also on the $V_{\rm oc}$ of SHJ devices (see Section III-B).

4) Low-Pressure Chemical Vapor Deposition Boron-Doped Zinc Oxide: To further investigate the nature of the effects observed for the sputtered ITO films, we now extend our analysis to ZnO:B layers deposited via LPCVD, an ultrasoft deposition technique that preserves pristine a-Si:H films. ZnO:B deposited via LPCVD is widely used in thin-film solar cells [14] and has found applications also in SHJ photovoltaic devices [35], [36]. Using these films has two advantages: 1) A wide range of carrier densities is accessible, aiding the identification of physical trends; and 2) sputter-damage is completely avoided, enabling unambiguous proof of the "electrical field" origin of the observed phenomena.

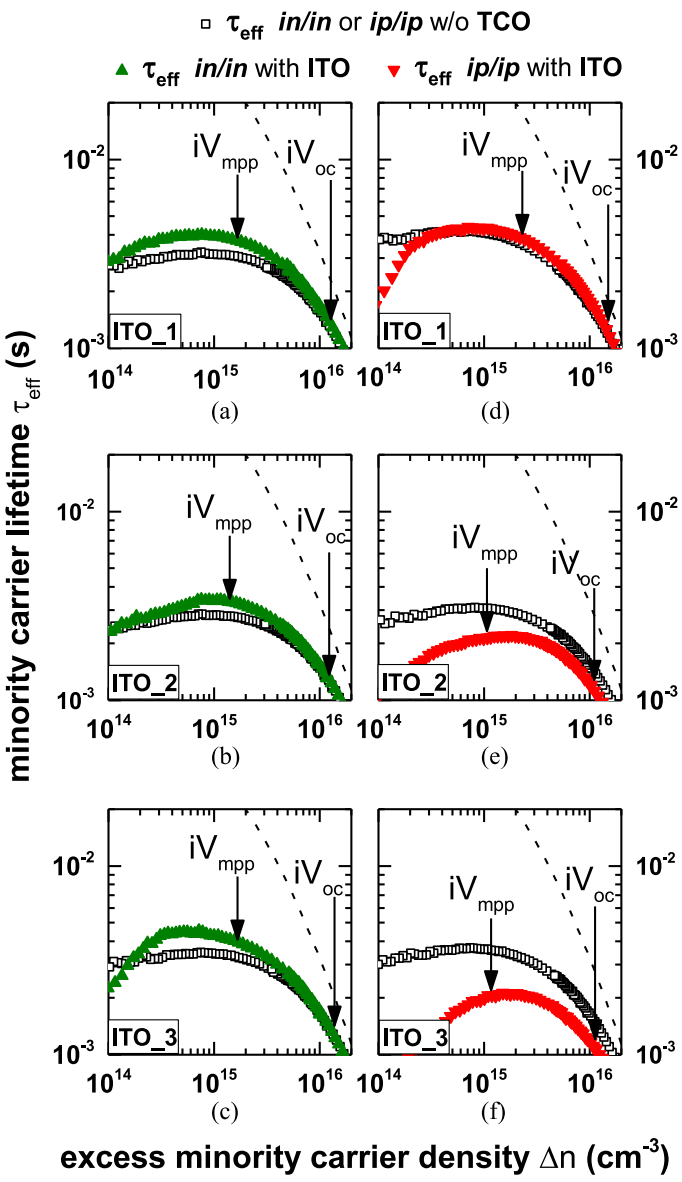

Fig. 4. Measurements of $\tau_{\rm eff}(\Delta n)$ on n-type c-Si absorbers featuring either a symmetrically codeposited (a)–(c) electron collector (*in/in* samples) or (d)–(f) hole collector (*ip/ip* samples), before and after deposition, on both sides of ITO films of different resistivity and subsequent annealing at 200 °C (see Table I). Δn corresponding to implied-$V_{\rm oc}$ and implied maximum power-point voltage (here referred as $iV_{\rm oc}$ and $iV_{\rm mpp}$, respectively) are identified by arrows for the $\tau_{\rm eff}(\Delta n)$ curves measured after deposition of the ITO layers. The combined Auger and radiative limit is indicated in each graph, for comparison, by a dashed line [22].

In this experiment, we codeposited ZnO:B layers with four different resistivities (see Table II) on both surfaces of *in/in* and *ip/ip* samples. The electrical properties of ZnO:B are tuned by varying the flow ratio of the precursor-dopant gas (diborane, B_2H_6) and the zinc-precursor gas [diethyl zinc, $(C_2H_5)_2Zn$)]. As for ITO, also in ZnO:B films, higher carrier mobilities correspond to higher carrier densities [37]. We measured $\tau_{\rm eff}(\Delta n)$ curves before and after deposition of the different ZnO:B layers. For the *in/in* samples, we observed a slight increase in $\tau_{\rm eff}$ for all samples after the deposition of the ZnO:B layers, (see the

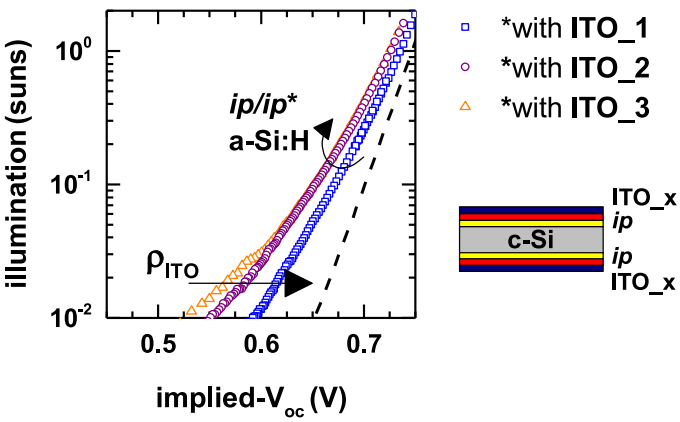

Fig. 5. Implied-$V_{\rm oc}$ versus illumination intensity values of the photoconductance decay lifetime measurements, whose $\tau_{\rm eff}(\Delta n)$ data are given in Fig. 4(d)–(f). The combined Auger and radiative limit is indicated, for comparison, by the dashed line [22].

TABLE II
ELECTRICAL PARAMETERS OF ZNO:B LAYERS

Layer	Carrier density ($\rm cm^{-3}$)	Hall Mobility ($\rm cm^2{\cdot}V^{-1}{\cdot}s^{-1}$)	$\rho_{\rm ZnO:B}$ ($\Omega{\cdot}$cm)
ZnO:B_1	-	-	105
ZnO:B_2	1.0×10^{19}	0.3	2.5
ZnO:B_3	6.1×10^{19}	3.9	2.6×10^{-2}
ZnO:B_4	1.4×10^{20}	13.0	3.5×10^{-3}

left side of Fig. 6) similar to what we observed with ITO films [see Fig. 4(a)–(c)]. The strongest increase is obtained for the sample featuring the most conductive ZnO:B layer. Conversely, for the *ip/ip* samples, we observed a stronger decrease in $\tau_{\rm eff}$ at low Δn values for samples featuring increasingly conductive ZnO:B films (see the right side of Fig. 6), confirming the trend observed for sputtered ITO films. In addition to these effects, during ZnO:B deposition, our samples also undergo *in-situ* annealing at a temperature below 200 °C for about 5 min. This annealing could be sufficient to explain a slight improvement in passivation [38], as witnessed for the lowly doped ZnO:B layers in both the *in/in* sample series (layer ZnO:B_1, ZnO:B_2, and ZnO:B_3 on the left side of Fig. 6) and the *ip/ip* sample series (layer ZnO:B_1 and ZnO:B_2 on the right side of Fig. 6).

Compared with the case of *ip/ip* samples with sputtered ITO films, implied-$V_{\rm oc}$ values do not reveal any obvious trend here [see Fig. 7(a)]. The implied-FF values vary significantly for samples exhibiting the most conductive ZnO:B film that yields the highest and the lowest implied-FF values for the *in/in* and *ip/ip* passivated sample, respectively [see Fig. 7(b)].

Therefore, our tentative conclusions are the following: Doped a-Si:H overlayers have a clear and strong impact on the surface passivation, especially at low Δn. This results from the band bending they induce at the c-Si wafer surface (i.e., surface field effect or lack thereof). The presence of TCOs on such overlayers can further affect the low-Δn passivation, again modifying the band bending in the c-Si wafer. Only from a passivation perspective, the presence of a highly doped (n-type) TCO can be beneficial when capping *in* stacks, but is detrimental for *ip* stacks. These two opposite observations are coherent with a reduced and augmented, TCO/a-Si:H(*n*/*p*) WF mismatch, respectively [39], as result of TCO doping and bare TCO WF variations (for a more detailed discussion on the factors determining energy-band lineup and band bending in the c-Si wafer; see also the Appendix). These phenomena may directly impact the FF upper limits, for the different SHJ device architectures (see Section IV).

In the following section, we now evaluate the described effects and their impact on the voltage of our devices and its illumination dependency.

B. Effects on Operating Voltage

1) High–Low Suns–$V_{\rm oc}$ Curves of Silicon Heterojunction Devices: The $V_{\rm oc}$ of a solar cell, obtained from the 1-sun current–voltage characteristics, is a first indication of the recombination losses occurring in the device. However, this parameter also contains important information about the quality of contacts and carrier collectors [40]. Our aim here is to verify to what extent the TCO-induced effects on $\tau_{\rm eff}(\Delta n)$, described in Section III-A, also hold relevance for the $V_{\rm oc}$ and, especially, for its illumination (i.e., Δn) dependence.

As a starting point for our discussion, we plot in Fig. 8(a) a typical *high–low* suns–$V_{\rm oc}$ curve measured for one of our *standard*-SHJ devices (conversion efficiency >20% and $V_{\rm oc}>$ 720 mV). In Fig. 8(b), for the same typical suns–$V_{\rm oc}$ curve, the local ideality factor *n* was also derived, which is defined as $n = q/kT\,(d(\ln(I))/dV_{\rm oc})^{-1}$, where *k* is Boltzmann's constant, *T* is the absolute temperature, *q* is the elementary charge, and *I* is the illumination intensity. In the same graphs, we also show the upper limit of implied-$V_{\rm oc}$, and the relative *n*, for our c-Si substrates (see dashed lines in Fig. 8). This implied-$V_{\rm oc}$ limit is dictated exclusively by the c-Si wafer properties (thickness and doping) and the intrinsic recombination processes in the wafer (Auger and radiative, described in [22]). For the precise conversion from Δn-dependent lifetime to suns–implied-$V_{\rm oc}$ data, we followed the procedure outlined in [16].

Earlier, the *high*-illumination suns–$V_{\rm oc}$ data were argued to be a useful diagnostic tool to characterize back-contacts in diffused homojunction c-Si devices [41]. Later on, as already mentioned in Section I, the same approach was also applied for the characterization of the a-Si:H(*p*)/TCO interface in SHJ devices [3], [4]. For such samples, a lowering of the measured $V_{\rm oc}$ at high illumination intensities was sometimes observed. This evidence supports the belief that the WF of the n-type TCO, being lower than the one of a-Si:H(*p*), may result rather in a Schottky than an ohmic contact, causing a $V_{\rm oc}$ drop and resistive losses under solar cell operation conditions [39], [42]. The value of *n* at 100 suns (n_{100}) was proposed as indicator for the strength of this effect [4].

The *low*-illumination suns–$V_{\rm oc}$ data instead give direct information about the performance of the device under the excess minority carrier density levels occurring during actual operation. From the $V_{\rm oc}$ data in the illumination range $\sim 0.04-1$ suns, the so-called pseudo-FF can be extracted [2], which represents

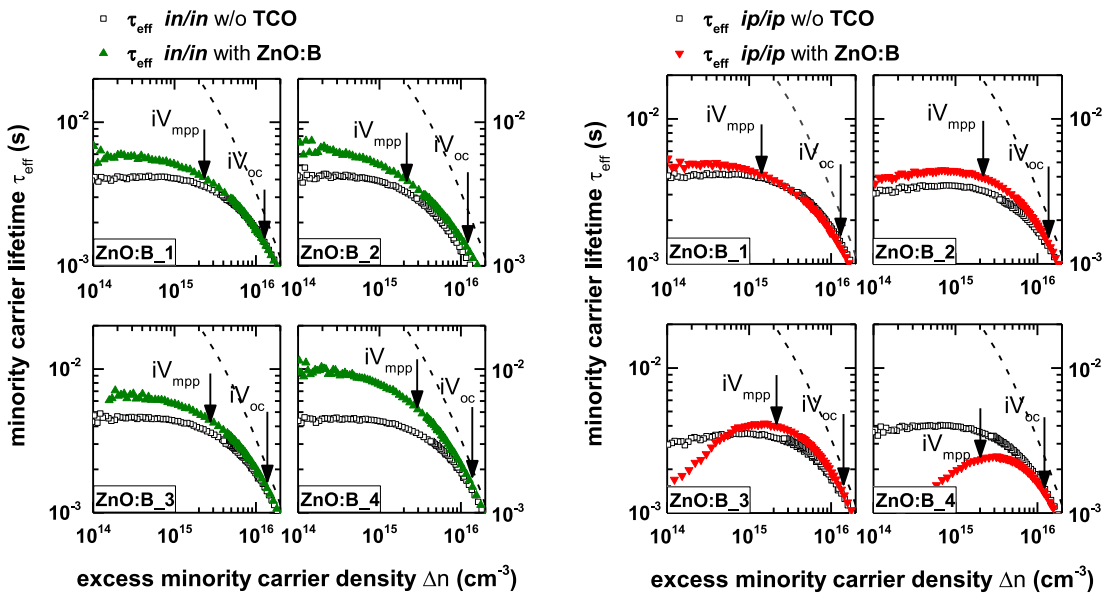

Fig. 6 Measurements of $\tau_{\rm eff}(\Delta n)$ on n-type c-Si absorbers featuring either a symmetrically codeposited electron collector (*in/in* samples) or hole collector (*ip/ip* samples), before and after deposition on both sides of ZnO:B films. In the bottom left corner of each graph, the type of ZnO:B layer to which the data refer is identified (for the layer electrical properties see Table II). Δn corresponding to implied-$V_{\rm oc}$ and implied maximum power-point voltage (here referred as $iV_{\rm oc}$ and $iV_{\rm mpp}$, respectively) are identified by arrows for the $\tau_{\rm eff}(\Delta n)$ curves measured after deposition of the ZnO:B layers. The combined Auger and radiative limit is indicated in each graph, for comparison, by a dashed line [22].

the upper FF limit imposed by carrier recombination processes only (assuming thus zero resistive losses in the device). Higher n at low illumination imply lower pseudo-FFs. Importantly, if the TCO-related effects acting on the illumination dependence of the implied-$V_{\rm oc}$ (see Fig. 5) equally affect also the $V_{\rm oc}$, the calculated pseudo-FF value would be consequently affected.

Comparing the illumination-dependent $V_{\rm oc}$ (from suns–$V_{\rm oc}$ measurements) in our *standard*-SHJ device to the theoretical implied-$V_{\rm oc}$ limit, we observe the following:

I) A moderate deviation of the *high*-illumination $V_{\rm oc}$, resulting in $0.5 < n_{100} < 2/3$ [see Fig. 8(b)]. This value is slightly lower than the one of the implied-$V_{\rm oc}$ limit but is still far above zero, indicating *high*-illumination $V_{\rm oc}$ "pinning" rather than "bending," using the terminology of [43].

II) $V_{\rm oc}$ values closely approach the limit in the illumination range 1–10 suns, indicating the attainment of an Auger-limited recombination regime.

III) Increasing deviation of the measured $V_{\rm oc}$ for lower illumination (<1 suns). This deviation accounts mainly for suboptimal surface passivation provided by a-Si:H-based hole and electron contacts.

2) Impact of Indium Tin Oxide Electrical Properties: Following the description of Suns–$V_{\rm oc}$ data of typical SHJ devices, we now discuss the impact of varying ITO electrical properties at the front of such solar cells, on such curves. The test structures are fabricated on n-type c-Si wafers featuring full-area *ip* and *in* stacks at front and back sides, respectively. The back contact is completed by a full-area ITO/metal stack, as in our *standard*-SHJ devices, whereas at the front, we deposited 1-cm^2 ITO pads connected to a small silver dot to allow for a good electrical contact. The properties of the ITO films used at the front are identical to those given in Table I.

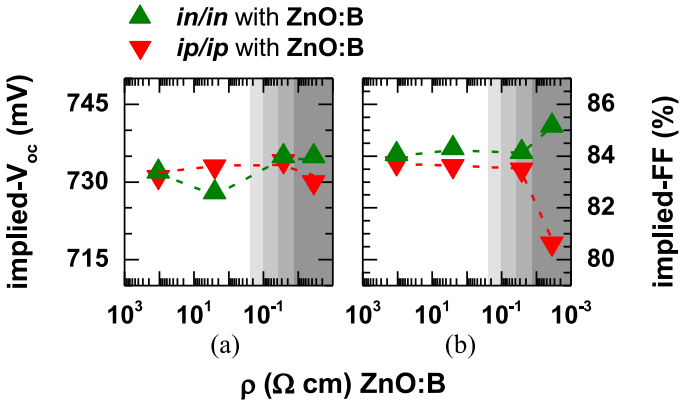

Fig. 7. Implied-$V_{\rm oc}$ and implied-FF values extracted from the $\tau_{\rm eff}(\Delta n)$ curves given in Fig. 6 (left and right panel). The gray background indicates the range of TCO resistivities that are more relevant with respect to applications in SHJ devices.

The *high–low* suns–$V_{\rm oc}$ curves measured on these samples are plotted in Fig. 9. Focusing on the low-illumination data, a weaker $V_{\rm oc}$ decrease is observed for the ITO films with higher resistivity and lower carrier density. Here, the overall influence of varying the TCO properties is moderate. The change in ITO-induced band bending at the c-Si surface results in suns–$V_{\rm oc}$ curves differing only at low illumination. In this regard, the a-Si:H(p) layer reveals itself as crucial in dampening the ITO influence on surface field effects (see also the discussion in the Appendix). The trend observed for the *high–low* suns–$V_{\rm oc}$ curves is consistent with the suns–implied-$V_{\rm oc}$ plot of Fig. 5,

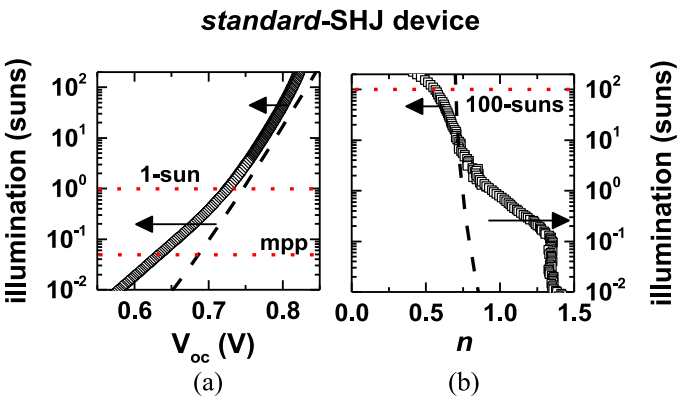

Fig. 8. Typical *high–low* suns–$V_{\rm oc}$ curve (a) measured on one of our *standard*-SHJ devices and (b) the respective local ideality factor n. For comparison, the combined Auger and radiative implied-$V_{\rm oc}$-limit (for our 2.8 Ω·cm, 250-μm-thick n-type c-Si wafers at 300 K) is indicated by the dashed lines [22]. The deviations of the measured $V_{\rm oc}$ from this limit, at high and low illuminations, are highlighted by arrows. The illumination levels corresponding to 1-sun and maximum power point (mpp) conditions, as well as to 100-sun conditions, are denoted by horizontal dotted lines in (a) and (b), respectively.

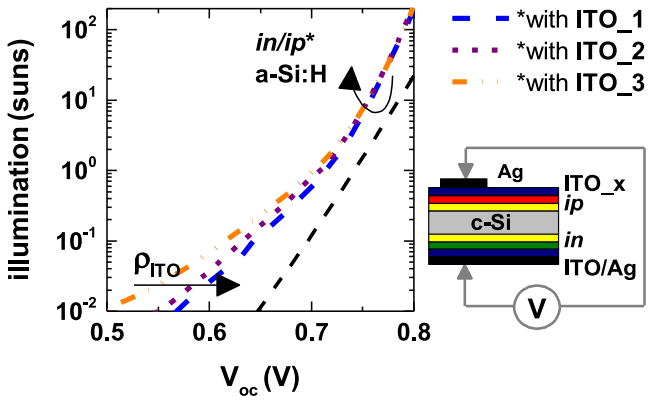

Fig. 9. Suns–$V_{\rm oc}$ measurements of 1-cm^2 test devices featuring "a-Si:H(*i*)/a-Si:H(*p*)/ITO/metal" and "a-Si:H(*i*)/a-Si:H(*n*)/ITO/metal" as front and back contacts, respectively (*in/ip* a-Si:H samples). The ITO films used in the front contact are layer ITO_1, ITO_2, and ITO_3 of Table I.

where the data were extracted directly from the $\tau_{\rm eff}(\Delta n)$ curves. This result confirms that the TCO-induced change in $\tau_{\rm eff}$ at low Δn can indeed affect the operating voltage of our devices at low illuminations. As such, it proves that the carrier recombination effects studied here are relevant toward pseudo-FF values, in addition to implied-FF values (as already extensively shown in Section III-A), and can impact high-efficiency SHJ devices.

For these samples, in Fig. 9, the absence of variations in the *high*-illumination suns–$V_{\rm oc}$ data is also remarkable. The perfect superposition of all the curves shown here, and the coincidence of their n_{100} values indicates that—within the explored carrier density range—the ITO properties do not impact those of the presumed "Schottky contact" [39], [42].

IV. Outlook on Transparent Electrodes for High-Efficiency Silicon Heterojunction Devices

As discussed elsewhere [1], the electrical and optical properties of optimized front and back TCO layers for high-efficiency SHJ devices differ significantly. For instance, in our *standard*-SHJ devices, the front ITO layers have typically a resistivity in the order of $\sim 10^{-4}\Omega\cdot$cm and a carrier density of $\sim 2-3\times10^{20}$cm^{-3}. In contrast, at the back, ITO films have usually a slightly higher resistivity in the range $10^{-3}-10^{-2}\Omega\cdot$cm and a carrier density of $\sim 1-9\times10^{19}$cm^{-3}. Higher resistivities can be tolerated at the rear thanks to the absence of lateral transport requirements in the TCO, when coated by a metallic layer. This allows the use of films with lower carrier densities, resulting in more transparent layers and improved short-circuit current values [1].

In this context, based on the experimental results discussed above, we concluded that from a surface passivation perspective, the presence of highly doped TCOs is not detrimental if contacting *in* stacks (i.e., electron collectors), whereas this may be when contacting *ip* stacks (i.e., hole collectors). Therefore, it would be preferable to avoid contacting the *ip* stack by a highly doped standard TCO at the front. This requirement is fulfilled by SHJ devices collecting holes at the rear (often called "rear emitter" solar cells). In this case, the front TCO is in contact with the *in* stack. In addition, without any optical penalty, the back a-Si:H(*p*) layer could be thickened, thereby improving the screening of the c-Si wafer against the TCO. Notably, this architecture, exploiting better the substrate conductivity, relaxes the requirement for the front TCO lateral conductivity, and a highly conductive TCO is no longer required [44].

Finally, in all SHJ device architectures, electrical screening of the c-Si wafer surfaces could be further improved by implementing p-type hydrogenated microcrystalline silicon layers, exploiting their much better dopability compared with a-Si:H [45]. Along similar lines, an improved a-Si:H(*i*) passivating layer, reducing the density of available defect states at the c-Si wafer surface, would also diminish the detrimental impact that field effects–such as those induced by TCOs–can have on surface passivation [18].

A. Transport and Recombination at the Hole Contact

Evidently, regarding the ideal properties of TCO as contact layer for high-efficiency SHJ devices, the effects on carrier recombination examined here represent only part of the wider and more complex problem of passivating contact optimization. As briefly already mentioned in Section I, the latter must address the minimization of charge carrier recombination and transport-activated losses (while preserving simultaneously also broadband transparency), as both contribute to determine the final solar cell FF.

For the case of the hole contact, in *standard*-SHJ devices, these losses can be probed only by using stacked TCO layers. This way, the impact of the TCO quality as contact layer on FF can be assessed, independent of its lateral conductivity properties. For this configuration, experimental results [4], [46], [47] indicate that for high FFs (and high n_{100} [4]), sufficiently conductive TCO films are needed to contact the a-Si:H(*p*) layer. Such high TCO conductivities are needed for low contact resistivities. In contrast, as argued in our work (see Section III-A), from a surface passivation perspective, it would be rather

beneficial to have a lowly doped TCO at the surface with the p-type a-Si:H film. These seemingly competing requirements have both implications toward the FF of high-efficiency SHJ devices. However, the FF loss observed for lowly doped TCO-contact films [4], [46], [47] cannot be explained by their higher WF, which instead should mitigate possible detrimental "Schottky-contact" effects [39], [42].

This contradiction evokes other determining factors, in addition to the TCO WF, for the quality of carrier transport across the hole contact, which occurs via thermionic emission, across the c-Si/a-Si:H(*i*) interface, and band-to-band tunneling, at the a-Si:H(*p*)/TCO interface [48]. Looking into the requirements for efficient band-to-band tunneling, the FF loss observed with insufficiently doped TCOs was recently explained–treating the TCO-contact film as a semiconductor material—with inefficient carrier tunneling through a wider space charge region at the a-Si:H(*p*)/TCO interface [47].

V. Conclusion

In this paper, we have demonstrated how the electrical properties of TCO layers can affect the surface passivation of SHJ contacts. Next, we showed that the effects observed with carrier lifetime measurements at low excess minority charge carrier densities fully correspond to those observed when measuring the $V_{\rm oc}$ at low illumination intensities. Based on our observations, we concluded that from a surface passivation perspective, highly doped TCOs should be avoided to contact hole collectors in n-type SHJ devices. This would lead to the best contact passivation and to the highest device FF's upper limits, which are imposed by carrier recombination. As front TCO layers in *standard*-SHJ devices are constrained by lateral conductivity requirements, our findings suggest increased design freedom and efficiency benefits for rear hole collector and back-contacted SHJ device architectures.

Appendix

In metal–semiconductor or semiconductor–semiconductor contacts, the WFs of the two distinct materials are often the starting point to determine the energy-band lineup. However, when considering absolute WF values in practical contacting problems extreme care should be taken. When bringing two material in intimate contact, indeed the resulting interfacial WF is mostly determined by Fermi-level pinning effects [49], [50]. These effects, which are dependent on the energy and density of interface electronic states, may in turn be influenced by the employed material deposition techniques or surface preparation methods. In addition, the WF of a certain material is a "surface," rather than a "bulk," characteristic. It was shown to vary importantly, in different material systems, either with surface crystallographic orientation or surface termination [51].

Based on these arguments, we did not consider of primary importance the quantitative characterization of our bare TCO film WFs. The individuation of all factors defining the doped a-Si:H/TCO interfacial WF (bare ITO film WF modified by interfacial Fermi-level pinning effects) seems hardly practicable. However, it is qualitatively possible to envisage how a shift in the bare TCO WF, as result for instance of TCO doping, would affect the doped a-Si:H/TCO interfacial WF and the corresponding band bending in c-Si. In the case of the hole contact, a lower bare TCO WF tends to diminish the interfacial WF opposing the field generated by the a-Si:H(*p*) layer at the c-Si surface. Conversely, at the electron contact, a diminished interfacial WF reinforces the field effect generated by the a-Si:H(*n*) layer at the c-Si surface [49]. Unfortunately, the relation between TCO doping and the bare TCO WF is not always trivial. This is related to the fact that the doping-induced Fermi-level shift in the TCO can be accompanied by changes in ionization potential (i.e., energetic distance between valence band and vacuum level), which, in turn, also impact WF [52]. For the case of ZnO:B films, we could not find relevant data in this regard. Yet, for ITO, earlier findings show a rather direct relation between higher doping, upward Fermi-level shift, and WF reduction [52]. In addition, with the ITO films of Table I, we realized the same test structures of Section III-B, but omitting the front a-Si:H(*p*) layer [3], [46], [53]. In these test devices, the a-Si:H(*i*)/ITO stack behaves as hole collector, whose properties are dictated by the resulting a-Si:H(*i*)/ITO interfacial WF and the corresponding c-Si surface band bending. They exhibit decreasing $V_{\rm oc}$ with decreasing film resistivities and increasing film carrier densities (1-sun $V_{\rm oc}$ of 542, 475, and 360 mV for ITO_1, ITO_2, and ITO_3 film, respectively), suggesting a correspondent interfacial and bare ITO film WF decrease. In the case of the more defective a-Si:H(*p*) film, Fermi-level pinning effects at the interface with ITO may be more important. Nevertheless, the experiment supports the argument that, in our ITO films, higher film doping and higher carrier densities correspond to lower bare ITO film WFs.

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