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NANO LETTERS

Letter

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From Twinning to Pure Zincblende Catalyst-Free InAs(Sb) Nanowires

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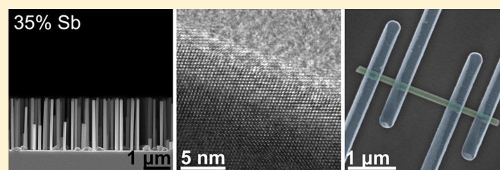
Supporting Information

ABSTRACT: III−V nanowires are candidate building blocks for next generation electronic and optoelectronic platforms. Low bandgap semiconductors such as InAs and InSb are interesting because of their high electron mobility. Fine control of the structure, morphology, and composition are key to the control of their physical properties. In this work, we present how to grow catalyst-free $InAs_{1-x}Sb_x$ nanowires, which are stacking fault and twin defect-free over several hundreds of nanometers. We evaluate the impact of their crystal phase purity by probing their electrical properties in a transistor-like configuration and by measuring the phonon−plasmon interaction by Raman spectroscopy. We also highlight the importance of high-quality dielectric coating for the reduction of hysteresis in the electrical characteristics of the nanowire transistors. High channel carrier mobilities and reduced hysteresis open the path for high-frequency devices fabricated using $InAs_{1-x}Sb_x$ nanowires.



KEYWORDS: *InAs nanowires, InAsSb, catalyst-free, self-catalyzed, molecular beam epitaxy, crystal structure, electronic properties, surface passivation, atomic layer deposition, mobility, phonon−plasmon interaction*

III−V semiconductor nanowires are considered next generation building blocks in electronics, optoelectronics, and energy harvesting applications.[1−4] At the same time, they have proved to be an ideal platform to probe novel physical properties resulting from the small size or lower dimensionality.[5−7] Indium-based III−V nanowires are of particular interest due to their high electron mobility, high spin−orbit coupling, and large g-factor.[8,9] III−V nanowires typically show polytypism, that is, a mixture phases of zincblende (ZB) and wurtzite (WZ) stacking, as well as stacking faults and rotational twins. The coexistence of different polytypes can dramatically modify the optical and transport properties. In particular, it has been found that the photoluminescence energy changes due to the presence of mixed crystal phases,[10] the resistivity of polytypic nanowires is up to 2 orders of magnitude higher[11] and even a single twin plane acts as an optically active nanodot.[12] Using gold as a catalyst particle, it has been possible to achieve control of the nanowire crystal structure.[13,14] Although this is still highly controversial, gold could be incorporated as an impurity in the nanowires, thereby harming the functional properties.[15−18] In order to avoid the risk of metal incorporation, a self-catalyzed or catalyst-free growth process is favored, though reducing the stacking fault density in InAs nanowires grown without a foreign catalyst has been found to be a difficult task.[19−21] One pathway toward pure phase nanowires is the incorporation of Sb, resulting in the growth of ternary antimonide nanowires. For antimonide crystals, zincblende stacking is favored due to the small ionicity of the bond.[22] In the case of GaAs, it has been shown that the incorporation of antimony allows for the growth of defect-free ZB $GaAs_{1-x}Sb_x$ nanowires both for gold-catalyzed nanowires using metal organic vapor phase epitaxy[23] and for self-catalyzed nanowires using molecular beam epitaxy (MBE).[24] In the case of $InAs_{1-x}Sb_x$ nanowires, defect-free wires have been reported using gold as a catalyst,[25] whereas without a foreign catalyst, even the least defective nanowires still show a considerable density of rotational twins.[26−28]

In this work, we demonstrate the growth of $InAs_{1-x}Sb_x$ using MBE and report for the first time that the stacking defect density in $InAs_{1-x}Sb_x$ nanowires grown without a foreign catalyst can be reduced to a few twins per micrometer by increasing the antimony content. The change in crystal structure as a function of the antimony content is studied quantitatively while showing that increasing the antimony content results in a strong reduction of the defect density in $InAs_{1-x}Sb_x$ nanowires and the hexagonal wurtzite phase can be completely suppressed. Pure ZB nanowires with only a few rotational twins per micrometer are obtained for an antimony content greater than 25%. The defect density is therefore more than 1 order of magnitude lower than the best results reported in literature.[26] We further investigate the material composition of $InAs_{1-x}Sb_x$ nanowires with energy dispersive X-ray (EDX) spectroscopy maps that show that the antimony content along the nanowire growth axis is homogeneous. Using nanowire cross sections, we also observe a homogeneous antimony content in the nanowire core and a slightly lower antimony content in the radial overgrowth, with antisegregation at the nanowire corners. Field-effect transistor measurements and

Received: October 28, 2015
Revised: November 26, 2015
Published: December 19, 2015

Raman spectroscopy show that incorporation of antimony also has a significant effect on the electrical and optical properties of $InAs_{1-x}Sb_x$ nanowires. Finally, we demonstrate that a high-quality ALD-grown aluminum oxide deposited around the nanowires enables the fabrication of top-gated devices with increased on−off ratios, steeper subthreshold slope and reduced hysteresis during transconductance measurements. Our results constitute an important step toward high electron mobility InAs(Sb) nanowire-based devices.

We start by comparing the growth rate and morphology of our $InAs_{1-x}Sb_x$ nanowires as a function of their antimony content. Our nanowires grow vertically on GaAs(111)B substrates and the optimum growth temperature was found to be 520 °C (more details available in Supporting Information). We refer to our growth process as catalyst-free because no external metal is used to initiate and drive the one-dimensional growth. We note the exact growth mechanism for InAs nanowires without a foreign catalyst (self-catalyzed or not) is still highly controversial and both vapor−liquid−solid[19] and vapor−solid[20] growth has been reported. In order to study the effect of antimony incorporation on the nanowire morphology and crystal structure, samples were grown at different antimony fluxes, while keeping the rest of the growth parameters constant. SEM micrographs of representative samples are shown in Figure 1a−b. All nanowires exhibit a hexagonal cross section with facets parallel to the {110} orientation of the substrate. Nanowire lengths and diameters were quantified as shown in Figure 1c. The incorporation of antimony leads to a slightly increased nanowire diameter and a decreased length. This observation stands in contrast to the growth of pure InAs nanowires, where it is well established that an increase of the group V flux results in longer and thinner nanowires (more details available in Supporting Information).

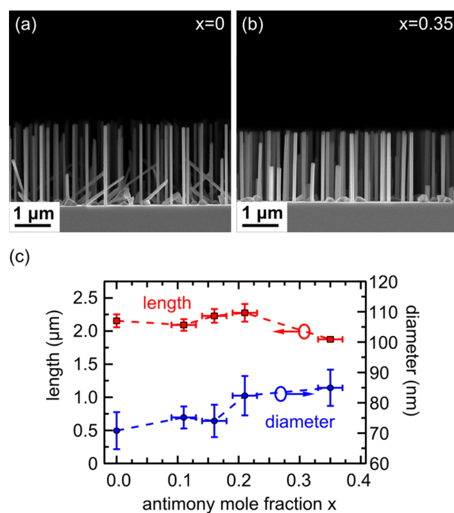


Figure 1. (a) and (b) Cross-sectional SEM micrographs of an InAs sample and an $InAs_{0.75}Sb_{0.35}$ sample grown for 1 h. (c) Quantification of the nanowire length and diameter as a function of the antimony content.

We turn now to the analysis of the crystal structure of the nanowires as a function of the Sb content. In order to show a figure of merit that integrates both polytypism and stacking-fault formation, we count the number of interfaces, that is, the sum of ZB/WZ transitions, stacking faults and rotational twins. Pure InAs nanowires show polytypism and a high density of interfaces. Interestingly, wurtzite stacking predominantly occurs at the nanowire stem, and pure WZ segments of several tens of nanometers in length can be observed as shown in Figure 2a. The existence of a WZ stem seems to be favored for thin diameters, which occur at the early stages of growth and at higher V/III ratios. A more detailed study is required to confirm this assumption. In the rest of the wire, the defect density is approximately 400 interfaces/μm (Figure 2b), confirming the findings of other groups.[19,26] We observe a strong decrease of defects with increasing antimony content. Representative HRTEM micrographs are shown in Figure 2c−d, respectively. $InAs_{1-x}Sb_x$ nanowires with a Sb content of 16% show a reduced defect density and the hexagonal phase is completely suppressed. Nanowires with an antimony content greater than 35% are almost defect-free, with only a few twins per micrometer. Figure 2e summarizes the evolution of the structure as a function of the Sb content, by plotting the number of interfaces (ZB/WZ and stacking faults) as a function of the Sb content in the nanowires. For increasing antimony content, the number of interfaces is reduced steadily. At 11% Sb, the number of interfaces is reduced to approximately 300 interfaces per micron and wurtzite sections are shorter and less frequent. For an antimony content of 21%, there are only about 100 interfaces per micron, and for samples with a higher content, there are only a few interfaces per micron. For all $InAs_{1-x}Sb_x$ nanowires, we observe that the interface density is lower at the nanowire stem and increases toward the nanowire tip, implying slightly different conditions during growth. Our findings are in agreement with the results in ref 28 and 26, where the suppression of WZ stacking and a reduction of twin defects was reported for wires with an antimony content up to 15%. By further increasing the antimony incorporation, we were able to achieve almost complete suppression of defect formation. Compared to gold-catalyzed nanowires in ref 25, we observe that the threshold for defect-free nanowires is higher without a foreign catalyst. Figure 3a shows a high angular annular dark field (HAADF) scanning transmission microscope (STEM) micrograph of a wire with 21% antimony, showing a few twin defects along the wire. The antimony content along the nanowire is uniform for all samples, as shown by longitudinal EDX maps in Figure 3b−d.

To understand the growth of $InAs_{1-x}Sb_x$ nanowires in more detail, nanowire cross sections were fabricated by first embedding a nanowire forest in epoxy and cutting slices of 60 nm thickness with an ultramicrotome.[29,30] Figure 3e shows a HAADF STEM micrograph of a nanowire cross section, confirming the hexagonal nanowire morphology with {110} facets. A hexagonal core and a shell of approximately 15 nm thickness can be observed, suggesting radial overgrowth of the initial nanowire core. This radial overgrowth is further supported by a time series of the nanowire growth (more details available in Supporting Information). The interface shows some strain contrast due to the lattice mismatch of two materials with slightly different composition. Figure 3f shows a HRTEM micrograph of one of the nanowires corners. From the inverse Fourier transform image in the inset, we can see that there are no misfit dislocations at the interface. EDX maps of the cross section are shown for indium, arsenic, and antimony in Figure 3g−h. Overlaying the arsenic and the antimony map shows that the antimony content is homogeneous in the core, a bit lower in the shell, and there is antisegregation of antimony at the six corners of the hexagonal cross section. Our observations are in agreement with the

DOI: 10.1021/acs.nanolett.5b04367
Nano Lett. 2016, 16, 637−643

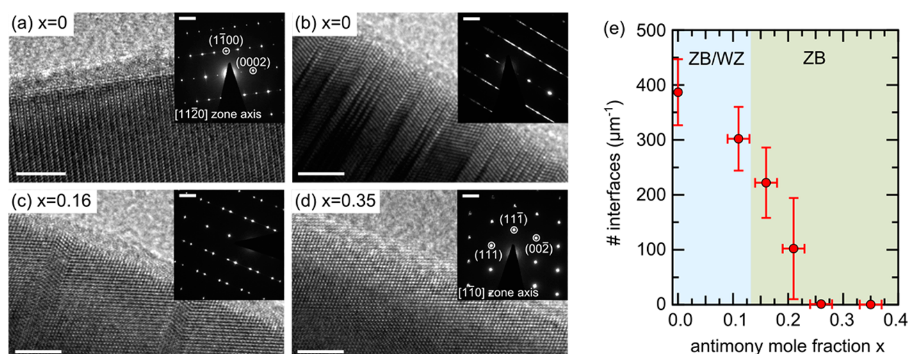


Figure 2. (a)−(d) High resolution TEM micrographs and diffraction patterns of different nanowires. The scale bar is 5 and 2 nm^{-1} respectively. (a) InAs nanowire stem where the crystal structure is pure WZ for several tens of nanometers. (b) Typical polytypic InAs nanowire crystal structure. (c) Nanowire with 16% antimony where the crystal structure is ZB with rotational twins. (d) Nanowire with 35% antimony. The nanowire is pure ZB with very few rotational twins. (e) Quantification of the number of interfaces as a function of the antimony content. The defect density dramatically decreases with increasing antimony content. Wurtzite segments are suppressed at an antimony content above 15% (green region).

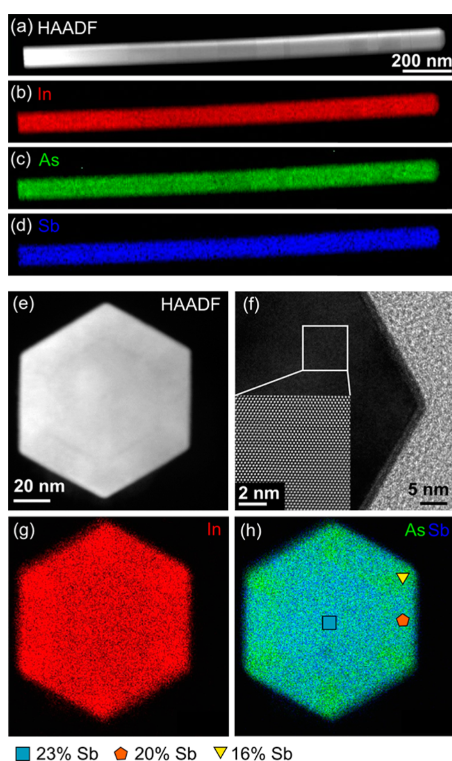


Figure 3. (a) HAADF STEM micrograph of a nanowire with 21% antimony. (b)−(d) EDX maps of indium, arsenic, and antimony showing a homogeneous composition along the wire. (e) HAADF STEM micrograph of a nanowire cross section showing a hexagonal nanowire core with a 15 nm thick shell. (f) High resolution image of a nanowire corner showing no dislocations at the shell interface. (g)−(h) EDX maps of the nanowire cross section. A homogeneous composition can be observed in the nanowire core. The shell has a slightly lower antimony content and shows antisegregation at the six corners.

results in ref 24, where a similar antisegregation of antimony was observed for $GaAs_{1-x}Sb_x$ nanowires. Quantification of the EDX map indicates the Sb content is 23% in the core, 20% in the shell, and 16% at the corners. Interestingly, it has been shown for gold-catalyzed nanowires that the antimony content in the core is lower compared to the radial overgrowth.[25] In this sense, catalyst-free growth may be a better approach for achieving a high, homogeneous antimony content compared to metal-assisted growth.

The impact of the crystal structure and composition on the properties of the nanowires is evaluated using field-effect transistor devices. All electrical transport measurements were performed at room temperature. Figure 4a shows the SEM micrograph of a nanowire device with four contacts. We studied as-grown InAs(Sb) nanowires as well as InAs(Sb) nanowires coated with a 10 nm shell of Al_2O_3. A high quality interface between the nanowire and the oxide was achieved by capping the nanowire with arsenic after growth and depositing 10 nm

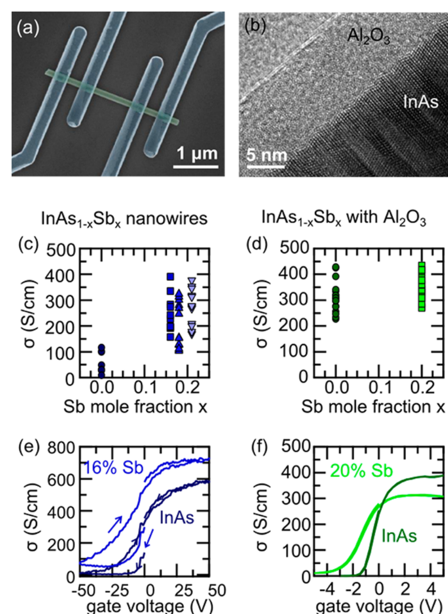


Figure 4. (a) False-colored SEM micrograph of a nanowire device. The nanowire (green) is contacted with four contacts (blue). (b) High resolution TEM micrograph of an InAs nanowire coated with 10 nm Al_2O_3. (c) Conductivity of $InAs_{1-x}Sb_x$ nanowires with different antimony content. (d) Conductivity of Al_2O_3 coated $InAs_{1-x}Sb_x$ nanowires with different antimony content. (e) Comparison of field-effect data for an InAs nanowire device and a device with 16% antimony using the substrate as back gate. (f) Comparison of field-effect data for Al_2O_3 coated nanowire devices using a top gate. The uncertainty in the conductivity measurements is about 10% due to uncertainty in the measurement of the device dimensions.

DOI: 10.1021/acs.nanolett.5b04367
Nano Lett. 2016, 16, 637−643

Al_2O_3 by atomic layer deposition.[31] Figure 4b is a TEM micrograph of an InAs−Al_2O_3 nanowire showing the crystalline nanowire core and the amorphous alumina shell. For these nanowires, a top gate was deposited between the two center contacts. The four-point configuration was used to measure the nanowire conductivity and the contact resistance. Ohmic contacts with a contact resistance less than 5×10^{-7} Ω cm^2 were obtained without annealing, confirming high-quality contacts. We start by comparing the conductivity, σ, of four types of wires with an antimony content of 0%, 16%, 18%, and 21%. In general, the conductivity is found to be higher for antimony containing wires as shown in Figure 4c. This result is consistent with our expectations because (1) the conductivity of bulk InSb is higher compared to InAs[32] and (2) InAs shows a charge accumulation layer at the surface,[33,34] which makes scattering at surface defects a limiting factor for the conductivity. Values ranging from σ = 10−100 S/cm for InAs devices and σ = 100−400 S/cm for $InAs_{1-x}Sb_x$ devices have been measured. We observe a large variance in the conductivity values as well as fluctuation of the current over time. We attribute this to the surface accumulation layer and surface sensitivity of InAs nanowires, making it difficult to compare the results in a quantitative and absolute manner. In contrast, much more consistent values were achieved for wires coated with Al_2O_3. For these nanowires, conductivity values of 200−400 S/cm and 250−450 S/cm were obtained for InAs and $InAs_{0.8}Sb_{0.2}$ nanowires, respectively (see Figure 4d). The high conductivity of the alumina coated nanowires is a sign of a high quality oxide−nanowire interface and stands in contrast to previous results, where highly deteriorated electrical properties have been reported for oxide coated nanowires.[35] Particularly for InAs nanowires, we observe that the measured conductivity is significantly higher when the wires are coated with Al_2O_3. This result could be explained considering that Al_2O_3 often acts as a negative charge dielectric.[36] Negative fixed charges near the interface would suppress electron trapping at interface defects, resulting in a larger population of mobile carriers and therefore in a higher conductivity. Furthermore, the alumina will prevent water adsorption onto the nanowire, which has been shown to have a detrimental influence on electrical properties.[37]

Figure 4e,f show the gate-dependent measurements. For measurements of wires not coated by ALD-Al_2O_3, the two inner contacts were used as source and drain, and the highly doped silicon substrate was used as a back gate while nanowires coated with Al_2O_3 were gated by a local top gate. A table with all relevant device and measurement parameters can be found in the Supporting Information. Figure 4e shows typical field-effect measurements of an InAs nanowire and an InAsSb device with 16% antimony. Both devices show n-type hysteretic behavior, as commonly observed for InAs nanowires due to the presence of surface states.[38] The hysteresis was successfully reduced by applying a pulsed gate sweep.[39] The baseline current at zero gate voltage varied as a function of time and sweep history, which we attribute to the additional gating of surface contamination. Nanowires coated with Al_2O_3 showed a significantly reduced hysteresis, especially with the pulsed gate sweep, see Figure 4f. In this case, we also do not observe any major change in baseline current. This is consistent with a reduced electron trapping at the interface due to fixed negative charges in the alumina.

We move now to the quantitative analysis of the gate dependent measurements. Assuming diffusive transport in the linear regime of the standard transistor model, the field-effect mobility can be calculated by $\mu = g_m(L^2/C)/V_{ds}$. Here, g_m is the transconductance $g_m = (dI_{ds})/(dV_g)$, where V_g is the gate voltage, and C is the nanowire-gate capacitance. For bottom gated devices, the capacitance is typically approximated by $C = 2\pi\varepsilon_0\varepsilon_r L/\mathrm{acosh}[(r + t_{ox})/r]$, where r is the nanowire diameter, t_{ox} is the thickness of the dielectric layer, and ε_r is the relative dielectric constant. Following ref 40, we use ε_r = 2.25 to account for the fact that the nanowire is not completely surrounded by the dielectric. Assuming bulk conductivity of electrons the carrier density at zero gate voltage, the electron density n can be estimated by $n = \sigma/e\mu$, where σ conductivity and e is the elementary charge of the electron. The transconductance of the data shown in Figure 4e would be consistent with a mobility of μ = 1540 cm^2/(V s) and μ = 2560 cm^2/(V s) and a charge density of $n = 5.6 \times 10^{17}$ cm^{-3} and $n = 7.3 \times 10^{17}$ cm^{-3} for the InAs and the InAsSb device, respectively. The trend of increased mobility with antimony content is in agreement with the results reported for gold-catalyzed nanowires.[11] The on−off ratios of the devices presented here are 58 and 9, respectively. We observe that the InAsSb nanowires cannot be turned off completely, which might be related to the larger diameter of the nanowires though future investigations are required to understand this behavior. One should also note that we observe a change in baseline current during the measurement, for example, the starting point and the end point of the gate sweep are not the same (more details in Supporting Information). Therefore, the mobility and the on−off ratio tend to be overestimated by the extracted values.

In order to extract the mobility in the case of Al_2O_3 coated nanowires, we estimate the capacitance of the top-gated devices by a parallel-plate capacitor, where the area is approximated as three nanowire facets, assuming shadowing of the bottom three nanowire facets during gate metal evaporation. A relative permittivity of ε_r = 8 was used for the amorphous ALD-Al_2O_3. The voltage across the gated nanowire length is obtained from the applied source-drain voltage and normalized using the ratio between the gated/nongated nanowire lengths (more details in Supporting Information). Mobility values consistent with μ = 1005 cm^2/(V s) and μ = 825 cm^2/(V s), charge densities of $n = 1.81 \times 10^{18}$ cm^{-3} and $n = 2.49 \times 10^{18}$ cm^{-3}, and on−off ratios of greater than 2755 and 29 were extracted from the gate sweeps respectively for InAs and InAsSb nanowires. However, it has been shown that in top-gated devices, the semiconductor capacitance has a significant contribution to the total capacitance.[41] To get a more realistic estimate of the mobility, the semiconductor capacitance C_s at the peak transconductance was calculated using a quasistatic model, which accounts for the electron degeneracy at the conduction band, the non-parabolicity effect of the Γ valley, and possible influence due to the interface traps.[42,43] In the calculation, the flat band voltage of the MOS structure was approximated to be the same as the threshold voltage in the I_{ds}/V_g curve. Using the total capacitance $1/C_{tot} = 1/C_{ox} + 1/C_s$, we estimate mobility values of 1400 cm^2/(V s) for InAs, which accounts for an error of 40% with the state-of-the-art formula. The uncertainty in the estimation of the gate capacitance along with hysteresis and unstable baseline-currents make it difficult to quantitatively assess mobility and carrier concentration from field-effect measurements. More sophisticated mobility measurements can be obtained by simulating the capacitance via finite element methods and directly fitting the transconductance[37] or also with Hall effect measurements,[44] Seebeck coefficient measure-

DOI: 10.1021/acs.nanolett.5b04367
Nano Lett. 2016, 16, 637−643

ments,[45] terahertz spectroscopy,[46] and Raman spectroscopy. In the following, we present our estimations of the mobility and electron carrier concentration from Raman spectroscopy.

Figure 5 shows the Raman spectra of pristine InAs and InAsSb with Sb 35% nanowires. In the spectra, LO and TO phonons frequencies as well as the SO (surface optical modes) typically detected in nanowires[47,48] are indicated. In the case of InAs, TO and LO modes of zincblende phase are present, no modes related to wurtzite crystal phase are observed.[49] In the case of InAsSb, the position of the TO and LO modes are consistent with the composition and follow a two mode model of ternary alloys: Raman modes of InAs and InSb are present, the position and intensity weighted by the composition.[50,51]

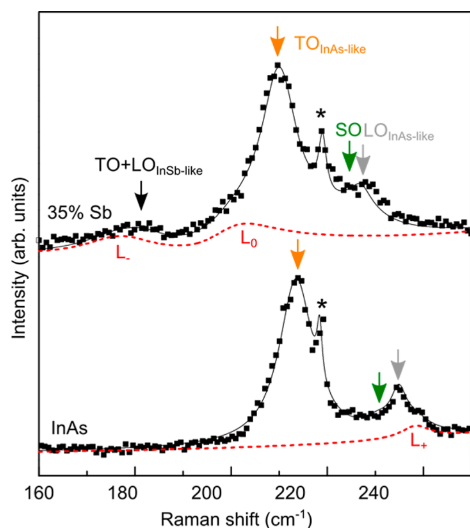


Figure 5. Raman spectra of InAs nanowires and of InAsSb nanowires with 35% antimony. The solid lines are the convolution of the ternary modes with a Lorentzian profile and the coupled modes' line shape obtained by fitting the model. The dashed lines show the coupled modes obtained by the fitting. The star indicates a plasma laser line.

The Raman spectra show additional spectral features in the LO region for the InAs and in the InAs-like TO mode region for InAsSb, which are not related to the composition, crystal phase, or shape of the nanowires. We attribute these additional peaks to the interaction of the carriers with the polar phonons. Longitudinal phonon−plasmon interaction is expected in polar semiconductor with free carriers.[52,53] Raman scattering by coupled plasmon−optical−phonon modes in n-type ternary III−V compounds results in three characteristic modes. In n-type InAsSb there is an intermediate mode (L_0) between the InAs-like TO and InSb-like LO phonon, in addition to lower frequency (L_-) and higher frequency (L_+) signatures.[52] The frequency position and the width of these modes are related to the plasmon (carrier) density and the lifetime (mobility). We fitted the whole spectra by modeling both the modes related to the composition and to the presence of free carriers. A Lorentzian profile was used for the TO and LO modes, whereas the line shape of the coupled modes included the effect of damping (mobility) as in ref 54. More details are given in the Supporting Information. We extract an electron concentration and mobility consistent with $n = 3.0 \times 10^{16}$ cm^{-3} and $\mu = 3900$ cm^2/(V s) for InAs and $n = 1.7 \times 10^{17}$ cm^{-3} and $\mu = 8300$ cm^2/(V s) for uncoated InAsSb nanowires. Overall, Raman spectroscopy gives higher mobility and lower carrier density values. The origin of this difference will be investigated in the future by contrasting with other measurements such as pump−probe THz spectroscopy.[55]

In conclusion, we have grown $InAs_{1-x}Sb_x$ nanowires with an antimony content up to 35% using a catalyst-free MBE growth process on GaAs substrates. The nanowires have a hexagonal cross section and show no tapering all along the wire. The crystal structure and chemical composition has been studied using HRTEM and EDX. We observed that the stacking fault density can be reduced to a few per micron by increasing the antimony content above 25%. These results confirm a universal trend of Sb to reduce stacking faults and polytypism in III−V nanowires, regardless of the synthesis method. We also studied for the first time the radial composition of the $InAs_{1-x}Sb_x$ nanowires using cross-sectional EDX analysis. A nanowire shell with slightly lower antimony content and antisegregation at the corners was observed, indicating that the nanowire diameter increases due to radial overgrowth. The electronic properties of $InAs_{1-x}Sb_x$ nanowires were studied using field-effect transistor measurements and Raman spectroscopy. We find that the incorporation of antimony increases the nanowire conductivity and mobility. We further use high-quality ALD grown Al_2O_3 as a gate dielectric for top gated nanowire devices and demonstrate better gate control and lower current drift without harming the nanowire properties. Raman spectroscopy shows that both the mobility and the charge density are increased for ternary antimonide nanowires. Our results shed light on the growth mechanism of ternary antimonide nanowires, and pave the pathway toward high-quality nanowire devices.

Experimental Methods. *Nanowire Growth.* The nanowires were grown in a DCA P600 MBE system on GaAs(111)B substrates by self-assembly and without the use of a foreign catalyst. The substrates were covered with a 4.5 nm silicon oxide layer, obtained by spin coating a diluted solution of hydrogen silsesquioxane (HSQ) (HSQ:MIBK 1:10) at 6000 rpm and annealing at 300 °C for 10 min. A similar substrate preparation was previously used for InAs and GaAs nanowire growth without a foreign catalyst.[19,56] The substrates were degassed at a manipulator temperature of 400 °C in ultrahigh vacuum conditions for 2 h prior to growth. Once in the growth chamber, they were annealed for 1 h at the growth temperature under constant arsenic and antimony flux. Nanowire growth was started by opening the indium shutter. After 60 min the growth was terminated by closing the indium and antimony supplies. The sample was cooled down under arsenic within 10 min. Standard fluxes are an indium beam equivalent pressure (BEP) of 1.4×10^{-7} Torr (corresponding to a 0.14 Å/s growth rate), and an arsenic BEP of 1.9×10^{-6} Torr. The antimony content in the nanowires was controlled by adjusting the antimony tank temperature, resulting in a BEP of 1.4−2.6 × 10^{-7} Torr. The cracker and conductance zone temperature was fixed at 800 °C for all samples. The crystal structure and composition of the nanowires was characterized by high resolution transmission electron microscopy (HRTEM) in a FEI Tecnai OSIRIS microscope operated at 200 kV. The antimony content of the nanowires was measured by EDX spectroscopy in the same microscope.

Device Fabrication. Single-nanowire field effect transistors (FET) were fabricated on highly p-doped silicon substrates with a 200 nm thermal oxide layer following a standard procedure.[57,58] For devices based on standard $InAs_{1-x}Sb_x$ nanowires the native oxide was removed by argon milling in order to achieve ohmic contacts. Chromium/gold (20 nm/100 nm) contacts were then deposited by sputtering in the same

DOI: 10.1021/acs.nanolett.5b04367
Nano Lett. 2016, 16, 637−643

deposition chamber as the argon milling, thereby avoiding reoxidation of the surface. For devices based on Al_2O_3-coated $InAs_{1-x}Sb_x$ nanowires the nanowires were capped with arsenic in the MBE chamber after growth by cooling down the sample to room temperature and opening arsenic for 30 min. The protective arsenic layer was then evaporated in the ALD chamber before starting deposition of the oxide. This procedure allowed us to prevent the growth of native oxide on the nanowires and to obtain a high-quality interface between the InAs and the alumina. Titanium/gold (10 nm/100 nm) was deposited on the alumina as top gate using e-beam evaporation. For the contacts, the alumina was removed by ion beam etching before sputtering chromium/gold.

Raman Spectroscopy. Raman measurements were done using the 488 nm line of $Ar-Kr^+$ for excitation. The laser with power of 250 μW was focused on the nanowire with a microscope objective with numerical aperture NA = 0.75. The scattered light was collected by a TriVista spectrometer and detected by a CCD camera. The measurements were realized in backscattering geometry with the nanowires suspended over a trench, in order to enhance the response of the longitudinal optical phonon mode.[59]

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b04367.

Additional information on the growth of InAsSb nanowires, electrical characterization, and Raman spectroscopy. (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Funding

SNF through NCCR-QSIT, projects nr 156081 and 143908 and Ambizione.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

We thank Duncan Alexander and Thomas La Grange for fruitful discussions, and Colette Vallotton for help with the ultramicrotome.

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DOI: 10.1021/acs.nanolett.5b04367
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