

CMOS IMAGE SENSOR

BACKGROUND

[0001] The present disclosure relates to the field of CMOS image sensors. It particularly aims at a low-noise CMOS image sensor, capable of operating in low brightness conditions.

DISCUSSION OF THE RELATED ART

[0002] Conventionally, a CMOS image sensor comprises pixels arranged in an array of rows and columns. Each pixel comprises a photodiode used in reverse mode, having its junction capacitance discharged by a photocurrent according to a received light intensity. At the end of a period, called image acquisition or integration period, before and after which the pixel is reset by recharging of its photodiode, the photogenerated charges stored in the photodiode are transferred to a capacitive sense node of the pixel. The illumination level received by the pixel is measured by measuring the potential variation of the pixel sense node, caused by the transfer, on this node, of the charges photogenerated in the photodiode of the pixel.

[0003] In practice, various noise sources are capable of affecting the measurement, which may raise an issue when the quantity of charges photogenerated in the photodiode is small, particularly when the sensor is used in low brightness conditions.

[0004] There is a need for a CMOS image sensor overcoming all or part of the disadvantages of existing sensors. More particularly, there is a need for a low-noise CMOS image sensor, capable of operating in low brightness conditions.

SUMMARY

[0005] Thus, an embodiment provides a CMOS image sensor comprising at least one pixel comprising: a photodiode having a first terminal connected to a first reference potential; a first MOS transistor connecting a second terminal of the photodiode to a sense node of the pixel; a second MOS transistor connecting the sense node to a second reference potential; and a third MOS transistor assembled as a follower source having its gate connected to the sense node and having its source intended to be connected to a read circuit, wherein the third transistor has a gate oxide thickness smaller than the gate oxide thickness of the first and second transistors, the potential difference between the first and second reference potentials is greater than the maximum voltage capable of being applied between two terminals of the third MOS transistor, and the body region or the drain region of the third transistor is connected to a third reference potential in the range between the first and second potentials.

[0006] According to an embodiment, the body region of the third transistor is insulated from the body region of the first transistor and the potential applied to the body region of the third transistor is different from that applied to the body region of the first transistor.

[0007] According to an embodiment, the third transistor is a P-channel transistor.

[0008] According to an embodiment, the first and second transistors are N-channel transistors, the body regions of the first and second transistors are connected to the first reference potential, the body region of the third transistor is connected to the second reference potential, and the drain region of the third transistor is connected to the third reference potential.

[0009] According to an embodiment, the pixel further comprises a fourth MOS transistor connecting the source of the third transistor to an output track of the pixel.

[0010] According to an embodiment, the fourth transistor has a gate oxide thickness greater than the gate oxide thickness of the third transistor.

[0011] According to an embodiment, the fourth transistor is a transistor of the same type as the third transistor.

[0012] According to an embodiment, the photodiode is a pinned diode comprising an N-type doped storage region, formed in a P-type doped substrate, and a P-type doped layer coating the storage region, this layer having a higher doping level than the substrate.

[0013] According to an embodiment, the first, second, and third transistors are N-channel transistors, the body regions of the first and second transistors are connected to the first reference potential, the body region of the third transistor is connected to the third reference potential, and the drain region of the third transistor is connected to a fourth reference potential.

[0014] According to an embodiment, the third transistor has a gate surface area smaller than that of the first and second transistors.

[0015] The foregoing and other features and advantages will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 is an electric diagram of an example of a pixel of a CMOS image sensor;

[0017] FIG. 2 is a simplified cross-section view of the pixel of FIG. 1;

[0018] FIG. 3 is an electric diagram of an embodiment of a CMOS image sensor pixel; and

[0019] FIG. 4 is a simplified cross-section view illustrating an embodiment of the pixel of FIG. 3.

[0020] For clarity, the same elements have been designated with the same reference numerals in the various drawings and, further, as usual in the representation of integrated circuits, the various drawings are not to scale.

DETAILED DESCRIPTION

[0021] FIG. 1 is an electric diagram showing an example of a pixel **100** of a CMOS image sensor. Pixel **100** comprises a photodiode **101**, a storage node K formed by the cathode of photodiode **101**, and a sense node SN. The anode of photodiode **101** is connected to a node of application of a low reference potential GND, for example, the ground. Pixel **100** further comprises a transfer transistor **103** having its conduction nodes (source/drain) respectively connected to node K and to node SN, a reset transistor **105** having its conduction nodes respectively connected to node SN and to a node of application of a high reference potential VDDH, a read transistor **107** assembled as a source follower, having its gate connected to node SN and having its drain connected to a node of application of a reference potential, and a selection transistor **109** having its conduction nodes respectively connected to the source of read transistor **107** and to an output conductive track **111**, generally called column, which may be common to a plurality of sensor pixels.

[0022] In the shown example, transistors **103**, **105**, **107**, and **109** are N-channel MOS transistors, and transistor **107**,

assembled as a source follower (or common drain assembly), has its drain connected to a node of application of a high reference potential, potential VDDH in this example.

[0023] In operation, the potential variations of node SN are transferred to the source of transistor **107** in a substantially identical form, that is, with no amplification or with a gain in the order of 1. Pixel **100** receives control signals TX, RT, and RS respectively applied to the gates of transistors **103**, **105**, and **109**.

[0024] As an example, pixel **100** may be controlled as follows:

[0025] During a pixel integration phase (preceded by a step of resetting photodiode **101**), transfer transistor **103** may be kept non-conductive (signal TX in the low state in the present example) to isolate storage node K from sense node SN. The electric charges generated in photodiode **101** under the effect of light then cause a progressive decrease of the voltage of node K.

[0026] Before the end of the integration phase, reset transistor **105** may be turned on (signal RST in a high state in this example) to reset the potential of sense node SN to potential VDDH, after which transistor **105** may be turned off to isolate node SN from node VDDH.

[0027] After the step of resetting node SN, the potential of node SN may be read and stored in a first read step, to be used as a reference for a subsequent step of measuring the discharge level of the photodiode. To achieve this, selection transistor **109** is turned on (signal RS in a high state in this example), so that the potential of node SN is transferred to output track **111**, via transistors **107** and **109**. The potential of track **111** may then be read and stored, via a read circuit, not shown.

[0028] After the first reading step, transfer transistor **103** may be turned on (signal TX in the high state in this example) to cause the transfer of the photogenerated charges stored in the photodiode onto sense node SN. The voltage at node SN then decreases by a value representative of the amount of photogenerated charges stored in the photodiode, and thus of the light intensity received by the photodiode during the integration.

[0029] The potential of node SN, transferred onto output track **111** by transistors **107** and **109**, can then be read again during a second read step, by a read circuit, not shown.

[0030] The output value of the pixel is for example equal to the difference between reference potential V_{OUT1} read from track **111** during the first reading step and potential V_{OUT2} read from track **111** during the second reading step.

[0031] An advantage of such a reading method, generally called CDS in the art, for “Correlated Double Sampling”, is that it enables to at least partly do away with certain sources of noise, such as the reset noise introduced by transistor **105**.

[0032] Other reading methods may be used to decrease the noise, for example, a reading of the type generally called CMS in the art, for “Correlated Multiple Sampling”, comprising integrating a plurality of successive samples of the output value of the pixel, which enables to increase the signal-to-noise ratio.

[0033] FIG. 2 is a simplified cross-section view illustrating an embodiment of pixel **100** of FIG. 1. In this example, pixel **100** is formed inside and on top of a portion of a P-type doped semiconductor substrate **201** (for example, made of silicon).

[0034] Photodiode **101** is formed close to the surface of substrate **201**, and comprises an N-type doped region **203**, topped with a P-type doped region **205** of higher doping level than substrate **201**. Region **203** defines a photogenerated charge storage area. In this example, photodiode **101** is a so-called pinned photodiode, or buried photodiode. In the absence of photogenerated charges, the potential of storage region **203** is defined by the doping levels of regions **201**, **203**, and **205**, and is for example equal to 1.5 V. The use of a pinned diode enables to significantly decrease the pixel noise, and more particularly the noise due to dark currents and the reset noise.

[0035] Transistor **103** comprises an N-type doped region **207**, for example having a higher doping level than region **203**, separated from photodiode **101** by a region of substrate **201**, and an insulated gate **209** coating the surface of substrate **201** between photodiode **101** and region **207**. Region **207** defines the drain of transistor **103**, and region **203** defines the source of transistor **103**. The portion of substrate **201** located under gate **209**, between regions **203** and **207**, defines a body region (also called “well”), or channel-forming region, of transistor **103**.

[0036] Transistor **105** comprises an N-type doped region **211**, for example having the same doping level as region **207**, separated from region **207** by a portion of substrate **201**, and an insulated gate **213** coating the surface of substrate **201** between region **207** and region **211**. Region **207** defines the source of transistor **105**, and region **211** defines the drain of transistor **105**. The portion of substrate **201** located under gate **213**, between regions **207** and **211**, defines the body region, or channel-forming region, of transistor **105**.

[0037] Transistor **107** comprises an N-type doped region **215**, for example having the same doping level as region **207**, separated from region **211** by a portion of substrate **201**, and an insulated gate **217** coating the surface of substrate **201** between region **211** and region **215**. Region **215** defines the source of transistor **107**, and region **211** defines the drain of transistor **107**. The portion of substrate **201** located under gate **217**, between regions **211** and **215**, defines the body region, or channel-forming region, of transistor **107**.

[0038] Transistor **109** comprises an N-type doped region **219**, for example having the same doping level as region **207**, separated from region **215** by a portion of substrate **201**, and an insulated gate **221** coating the surface of substrate **201** between region **215** and region **219**. Region **219** defines the source of transistor **109**, and region **215** defines the drain of transistor **109**. The portion of substrate **201** located under gate **221**, between regions **215** and **219**, defines the body region, or channel-forming region, of transistor **109**.

[0039] In this example, gate **209** of transistor **103** is connected to a node of application of signal TX, gate **213** of transistor **105** is connected to a node of application of signal RT, gate **217** of transistor **107** is connected to node SN, gate **221** of transistor **109** is connected to a node of application of signal RS, region **207** is connected to node SN, region **211** is connected to a node of application of high reference potential VDDH, substrate **201** (and accordingly, the anode of diode **103** as well as the body regions of transistors **103**, **105**, **107**, and **109**) is connected to a node of application of low reference potential GND, and region **219** is connected to output track **111**.

[0040] A node source which raises a particular issue in applications with a low illumination level is the read noise generated by the read transistor assembled as a source fol-

lower, and more particularly the $1/f$ component of the read noise, also called flicker noise. Such a noise source indeed remains significant even when a reading of CDS or CMS type is implemented, and may become preponderating in low brightness conditions.

[0041] Based on analytic calculations detailed in an article entitled "Comparison of two optimized readout chains for low light CIS", of Assim Boukhayma et al. (SPIE Proceedings Vol. 9022), the content of which is incorporated herein by reference, it has been shown that variance $\overline{Q^2}$ (in [Coulomb²]) of the $1/f$ read noise relative to the input, introduced by the read transistor assembled as a source follower, can be expressed as:

$$\overline{Q^2} = \alpha_{CMS} \frac{K}{C_{ox}^2 WL} (C_{SN} + c_{GS} WL + c_{GD} W)^2,$$

K being a parameter proportional to kT depending on the considered technology (where k is Boltzman's constant and T is the absolute temperature), α_{CMS} being a noise reduction factor independent from the pixel structure and only depending on the product of the circuit bandwidth by the time between the read samples, as well as on the number of stored samples (in the case of a CMS-type reading), C_{ox} being the gate-substrate surface capacitance formed by the gate oxide of the read transistor assembled as a source follower, W and L respectively being the gate width and length of the read transistor, C_{SN} being the capacitance of sense node SN, particularly depending on the stray capacitances of the reset transistor and of the transfer transistor, and c_{GS} and c_{GD} respectively being the gate-source surface capacitance and the gate-drain linear capacitance of the read transistor.

[0042] Generally, in a given CMOS integrated circuit chip manufacturing process, two different gate oxide thicknesses are available to form MOS transistors. Conventionally, in an image sensor comprising pixels with four MOS transistors of the type described in relation with FIGS. 1 and 2, the four transistors of the pixel (transistors 103, 105, 107, and 109) are thick-oxide transistors. Thick-oxide transistors may indeed operate at nominal voltages greater than the nominal operating voltages of thin-oxide transistors, and thus enable to form pixels having a larger dynamic range (or measurement range). The use of thick oxide transistors is particularly adapted when the photodiode is a pinned photodiode of the type described in relation with FIG. 2. This type of photodiode indeed has an open-circuit voltage (in the absence of photogenerated charges) which may be relatively high, for example, close to the nominal operating voltage of thin oxide MOS transistors. The use of thin-oxide transistors would then not enable to obtain a sufficient dynamic operating range for the pixel.

[0043] According to an aspect of an embodiment, a pixel comprising a photodiode, a sense node, a transfer transistor, a reset transistor, and a read transistor assembled as a follower source is provided, where the transfer transistor and the reset transistor are thick oxide transistors, and where the read transistor is a thin-oxide transistor. The use of a thin-oxide read transistor enables to increase the gate-substrate surface capacitance formed by the gate oxide of the read transistor with respect to a pixel where the read sensor is a thick-oxide transistor. Tests carried out by the inventors have shown that in such a pixel, the read noise, and more particularly the $1/f$ noise, is significantly decreased with respect to a pixel where the read transistor is a thick-oxide transistor. Preferably, the

read transistor further has a gate surface area (WL) smaller than the gate surface area of the transfer and reset transistors and, more generally, lower than the minimum gate surface area of thick-oxide transistors in the considered technology. This enables to further decrease the $1/f$ component of the read noise.

[0044] To avoid losing dynamics with respect to a pixel where all transistors are thick-oxide transistors, the body region of the read transistor is insulated from the body regions of the transfer and reset transistors. The body and drain regions of the read transistor are biased so that the read transistor can receive on its gate the entire potential swing of sense node SN (from the reset potential to the saturation potential of the pixel), without for the gate-drain or gate-body voltage of the read transistor to exceed nominal operating voltage VDDL of a thin-oxide MOS transistor. The body and drain regions of the read transistor are for example biased so that the body-drain voltage of the read transistor is equal to nominal operating voltage VDDL of thin oxide MOS transistors. The transfer and reset transistors remain biased to a voltage preferably equal to nominal operating voltage VDDH of thick-oxide MOS transistors to maximize the range of possible measurement values.

[0045] FIG. 3 is an electric diagram of an embodiment of a pixel 300 of a CMOS image sensor. Pixel 300 comprises, like pixel 100 of the example of FIG. 1, a photodiode 101, a storage node K formed by the cathode of photodiode 101, and a sense node SN. The anode of photodiode 101 is connected to a node of application of a low reference potential GND, for example, the ground. Pixel 300 further comprises, as in the example of FIG. 1, a transfer transistor 103 connecting node K to node SN, and a reset transistor 105 connecting node SN to a node of application of a high reference potential VDDH. Pixel 300 further comprises a read transistor 307 assembled as a source follower, having its gate connected to node SN and having its drain connected to a node of application of an intermediate reference voltage VL, and a selection transistor 309 having its conduction nodes respectively connected to the source of read transistor 307 and to an output conductive track 111, which may be common to a plurality of pixels of the sensor.

[0046] In the shown example, transistors 103 and 105 are N-channel MOS transistors, and transistors 307 and 309 are P-channel MOS transistors. In this example, transistors 103, 105, and 309 are thick-oxide transistors, and transistor 307 is a thin-oxide transistor. Transistors 103 and 105 have their body regions connected to a node of application of low reference potential GND, and transistors 307 and 309 have their body regions connected to a node of application of high reference potential VDDH. Read transistor 307 has its drain connected to a node of application of an intermediate reference potential VL, between low reference potential GND and high reference potential VDDH. As a variation, the body region of read transistor 307 may be connected to the source of this same transistor.

[0047] In operation, the potential variations of node SN are transferred to the source of transistor 307 in a substantially identical form. Pixel 300 receives control signals TX, RT, and RS respectively applied to the gates of transistors 103, 105, and 309.

[0048] As an example, pixel 300 may be controlled substantially in the same way as pixel 100 of FIG. 1, by adapting the level of the logic signals according to the conductivity type of the transistors.

[0049] Voltage VDDH (relative to ground GND) for example corresponds to the nominal power supply voltage of thick-oxide MOS transistors in the considered technology. Intermediate potential VL applied to the drain of transistor 307 may be selected so that, in normal conditions of use of the pixel, transistor 307 never sees a voltage higher than nominal operating voltage VDDL (relative to ground) of thin-oxide MOS transistors in the considered technology. As an example, voltage difference VDDH-VL corresponds to nominal power supply voltage VDDL of thin-oxide MOS transistors in the considered technology.

[0050] As a non limiting illustration, a technological process where thick-oxide MOS transistors are provided to operate at voltages which may range up to 3.3 V, and where thin-oxide MOS are provided to operate at voltages capable of ranging up to 1.8 V is considered. For example, low reference potential GND is equal to 0 V and high reference potential VDDH is equal to 3.3 V. Photodiode 101 is for example a pinned diode having, in the absence of photogenerated charges (after transfer of the photogenerated charges onto sense node SN), a cathode potential equal to 1.5 V. Intermediate reference potential VL applied to the drain of read transistor 307 is for example equal to 1.5 V.

[0051] It should be noted that in practice, the thick oxide is approximately twice as thick as the thin oxide, and nominal power supply voltage VDDH of thick-oxide MOS transistors is substantially lower than or equal to twice nominal power supply voltage VDDL of thin-oxide MOS transistors.

[0052] If open-circuit voltage V_{pin} of the photodiode is of the same order of magnitude as nominal power supply voltage VDDL of thin-oxide MOS transistors, then, the variation range of potential V_{SN} (or voltage relative to ground) at the sense node has an amplitude substantially equal to VDDL. More specifically, potential V_{SN} varies between a value V_{pin} and the maximum reset voltage of node SN, which is VDDH-V_{tn}, where V_{tn} is the threshold voltage of the reset NMOS transistor. If the variation amplitude at node SN, equal to VDDH-V_{tn}- V_{pin} , is lower than voltage VDDL, it is then possible to find a reference potential VL of the read transistor which enables to respect the maximum voltage capable of being applied across the read transistor. It should be noted that the present invention is particularly advantageous in the case where transistors 103, 105 with a thick oxide are submitted to particularly high voltages (equal or close to nominal voltage VDDH) higher than nominal voltage VDDL capable of being reasonably withstood by a thin-oxide transistor. In this case, the use of a dedicated biasing for the body region of the read transistor or the use of an adapted bias voltage for the drain of the read transistor makes the use of a thin-oxide transistor possible for the read transistor. In other words, the use of an intermediate reference potential VL different from low and high reference potentials GND and VDDH enables in this case to provide a good operation of the thin-oxide transistor.

[0053] Further, selection transistor 109 preferably is a thick-oxide MOS transistor. Indeed, the use of a thin-oxide MOS transistor would require controlling its gate with a control voltage having a controlled swing to avoid damaging the transistor. In the case of the example described hereabove in relation with FIG. 3, the control voltage of the gate of selection transistor 109, made of simple oxide, may for example oscillate between a low level equal to reference potential VL and high reference potential VDDH. Since the gate voltage of selection transistor 109, of PMOS type in the present example, necessarily is at a sufficiently high voltage

(VL) higher than GND (as is the case with a thick-oxide transistor), the on-state resistance of the selection transistor is higher than in the case of a thick-oxide transistor. This accordingly results in slowing down the reading of the pixel, or in degrading the transmitted voltage value (if the pixel reading time does not allow a full charge of output conductive track 111 (column). Further, the circuit complexity is increased in the case where the control levels of the gate of the selection transistor should switch between potential levels which do not correspond to ground or to a power supply voltage (VDDH, VDDL).

[0054] Further, it is preferable for selection transistor 309 to be of the same type as read transistor 307, so that the potential level present on the source of the read transistor is properly transmitted to output conductive track 111 (column).

[0055] FIG. 4 is a simplified cross-section view illustrating an embodiment of pixel 300 of FIG. 3. In this example, pixel 300 is formed inside and on top of a portion of a P-type doped semiconductor substrate 201 (for example, made of silicon). Photodiode 101, transistor 103, and transistor 105 are substantially identical to what has been described in relation with FIG. 2, and transistors 307 and 309 are formed in a same N-type doped well 401, formed in an upper portion of substrate 201.

[0056] Transistor 307 comprises two P-type doped regions 403 and 405, formed in an upper portion of well 401 and separated by a portion of well 401. Transistor 307 further comprises an insulated gate 407 coating the surface of well 401 between region 403 and region 405. Region 403 defines the drain region of transistor 307, and region 405 defines the source region of transistor 307. The portion of well 401 located under gate 407, between regions 403 and 405, defines the body region, or channel-forming region, of transistor 307.

[0057] Transistor 309 comprises a P-type doped region 409, for example, of same doping level as regions 403 and 405, separated from region 405 by a portion of well 401, and an insulated gate 411 coating the surface of well 401 between region 405 and region 409. Region 405 defines the drain region of transistor 309 and region 409 defines the source region of transistor 309. The portion of well 401 located under gate 411, between regions 405 and 409, defines the body region, or channel-forming region, of transistor 309.

[0058] In this example, gate 209 of transistor 103 is connected to a node of application of signal TX, gate 213 of transistor 105 is connected to a node of application of signal RT, gate 407 of transistor 307 is connected to node SN, gate 411 of transistor 309 is connected to a node of application of signal RS, region 207 is connected to node SN, region 211 is connected to a node of application of high reference potential VDDH, substrate 201 (and accordingly the anode of diode 103 as well as the body regions of transistors 103 and 105) is connected to a node of application of low reference potential GND, well 401 (and accordingly, the body regions of transistors 307 and 309) is connected to a node of application of high reference potential VDDH, region 403 is connected to a node of application of intermediate reference potential VL, and region 409 is connected to output track 111.

[0059] An advantage of the embodiments described in relation with FIGS. 3 and 4 is that they enable, due to the surface capacitance increase and, possibly, to the gate surface area decrease, of the read transistor, to significantly decrease the pixel read noise as compared with a pixel of the type described in relation with FIGS. 1 and 2. As an illustration, with a

CMS-type reading with 4 stored samples per read operation, the inventors have measured a $1/f$ noise level relative to sense node SN of $1.25 e^-$ for the pixel of FIGS. 1 and 2, and of $0.2 e^-$ only for the pixel of FIGS. 3 and 4.

[0060] Advantageously, in the case of an image sensor with a plurality of pixels, neighboring pixels may share a same well 401 where transistors 307 and 309 are formed, which enables to decrease the sensor bulk.

[0061] Specific embodiments have been described. Various alterations, modifications, and improvements will readily occur to those skilled in the art.

[0062] In particular, it will be within the abilities of those skilled in the art to adapt the described embodiments to the case where the read transistor assembled as a source follower is an N-type MOS transistor. In this case, the body region of the read transistor is insulated from the body region of the transfer and reset transistors by means of a triple-well structure, to be able to insulate the body region of the read transistor from substrate 201, to be able to bias them to different voltages. The body region of the read transistor is then connected to a node of application of an intermediate reference potential V_{reflow} which is preferably smaller than or equal to the minimum voltage capable of being present on the transistor source, that is, $V_{pin}-V_{t1}$ (where V_{t1} is the threshold voltage of the thin-oxide read transistor), for example, $1.5 V-0.5 V=1 V$. The drain region of the read transistor is then connected to a node of application of a high reference potential $V_{refhigh}$, for example equal to $V_{reflow}+V_{DDL}$ ($V_{refhigh}$ is for example equal to $1 V+1.8 V=2.8 V$). Reference potentials V_{reflow} and $V_{refhigh}$ are thus preferably selected so that the read transistor never sees across its terminals a voltage greater than the nominal operating voltage of thin-oxide transistors in the considered technology.

[0063] Such an embodiment with an NMOS-type read transistor requires using a triple-well structure which is bulky and decreases the pixel density. Further, in practice, two voltage references V_{reflow} and $V_{refhigh}$, different from the power supply voltages and from ground, may appear to be necessary to respect the voltage constraints of the thin-oxide transistor. For this last point, it may be envisaged to bias the drain of reset transistor 105 to the same voltage $V_{refhigh}$ as that applied to the drain of the NMOS selection transistor since the maximum level capable of flowing through the NMOS transistor is equal to $V_{DDH}-V_{tn2}$ (V_{tn2} being the threshold voltage of the thick-oxide reset NMOS transistor), that is, for example, $3.3 V-0.5 V=2.8 V$.

[0064] Further, the inventors have observed that, in practice, the use of an NMOS transistor as a read transistor does not provide the same good results for $1/f$ noise as with a PMOS transistor.

[0065] Thus, in the case of a photodiode of pinned type associated with an NMOS transfer transistor, the preferred embodiment is that described in relation with FIG. 3 with thick-oxide NMOS-type transfer and reset transistors, a thin-oxide PMOS-type read transistor, and a thick-oxide PMOS-type selection transistor.

[0066] Although the use of pinned photodiodes of a type opposite to that shown in FIG. 3 is relatively uncommon, there could be an N+/P/N photodiode, on an N-type substrate, associated with a PMOS-type transfer transistor. In this case, it could be envisaged to only have PMOS-type transistors, the transfer and reset transistors having a thick oxide and the read transistor having a thin oxide, the selection transistor preferably having a thick oxide. Further, in the case of such a

N+/P/N photodiode, the cathode would be connected to high reference potential V_{DDH} and the anode would be connected to the transfer transistor.

[0067] Further, although the above-mentioned examples show transfer and reset transistors of the same type, those could be different. However, for reasons of density and also to limit the surface areas of wells capable of creating parasitic diodes, the use of a same type of transistors will be preferred.

[0068] Further, the described embodiments are not limited to the numerical examples of bias potentials mentioned here-above.

[0069] Further, the described embodiments are not limited to the specific case described hereabove, where the photodiode is a pinned diode.

[0070] Further, the number of transistors present in the pixel is not limited to 3 or 4 as appears in the described examples, the selection transistor being needless in certain cases. It will be within the abilities of those skilled in the art to add other transistors to carry out other functions than those described hereabove. A general reset transistor, directly connected to the photodiode, to carry out functions known as global shutter functions, may in particular be added.

[0071] Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A CMOS image sensor comprising at least one pixel (300) comprising:

- a photodiode (101) having a first terminal connected to a first reference potential (GND);
- a first MOS transistor (103) connecting a second terminal of the photodiode (101) to a sense node (SN) of the pixel;
- a second MOS transistor (105) connecting the sense node (SN) to a second reference potential (V_{DDH}); and
- a third MOS transistor (307) assembled as a source follower having its gate (407) connected to the sense node (SN) and having its source intended to be connected to a read circuit;

wherein the third transistor (307) has a gate oxide thickness smaller than the gate oxide thickness of the first (103) and second (105) transistors, the potential difference between the first (GND) and second (V_{DDH}) reference potentials is greater than the maximum voltage capable of being applied between two terminals of the third MOS transistor (307), and the body region or the drain region of the third transistor (307) is connected to a third reference potential (VL) in the range between the first (V_{DDH}) and second (GND) potentials.

2. The sensor of claim 1, wherein the body region of the third transistor (307) is insulated from the body region of the first transistor (103) and the potential (VL) applied to the body region of the third transistor (307) is different from that applied to the body region of the first transistor (103).

3. The sensor of claim 1, wherein the third transistor (307) is a P-channel transistor.

4. The sensor of claim 3, wherein the first (103) and second (105) transistors are N-channel transistors, the body regions of the first (103) and second (105) transistors are connected to the first reference potential (GND), the body region of the third transistor (307) is connected to the second reference

potential (VDDH), and the drain region of the third transistor (307) is connected to the third reference potential (VL).

5. The sensor of claim 1, wherein said at least one pixel (300) further comprises a fourth MOS transistor (309) connecting the source of the third transistor (307) to an output track (111) of the pixel.

6. The sensor of claim 5, wherein the fourth transistor (309) has a gate oxide thickness greater than the gate oxide thickness of the third transistor (309).

7. The sensor of claim 5, wherein the fourth transistor (309) is a transistor of same type as the third transistor (307).

8. The sensor of claim 1, wherein the photodiode (101) is a pinned diode comprising an N-type doped storage region (203), formed in a P-type doped substrate (201), and a P-type doped layer (205) coating the storage region (203), said layer (205) having a higher doping level than the substrate (201).

9. The sensor of claim 2, wherein the first (103), second (105), and third transistors are N-channel transistors, the body regions of the first (103) and second (105) transistors are connected to the first reference potential (GND), the body region of the third transistor (307) is connected to the third reference potential (Vreflow), and the drain region of the third transistor (307) is connected to a fourth reference potential (Vrefhigh).

10. The sensor of claim 1, wherein the third transistor (307) has a gate surface area smaller than that of the first (103) and second (105) transistors.

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