Comparison of two optimized readout chains for low light CIS

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ABSTRACT

We compare the noise performance of two optimized readout chains that are based on 4T pixels and featuring the same bandwidth of 265kHz (enough to read 1Megapixel with 50frame/s). Both chains contain a 4T pixel, a column amplifier and a single slope analog-to-digital converter operating a CDS. In one case, the pixel operates in source follower configuration, and in common source configuration in the other case. Based on analytical noise calculation of both readout chains, an optimization methodology is presented. Analytical results are confirmed by transient simulations using 130nm process. A total input referred noise bellow 0.4 electrons RMS is reached for a simulated conversion gain of $160\mu V/e^-$. Both optimized readout chains show the same input referred 1/f noise. The common source based readout chain shows better performance for thermal noise and requires smaller silicon area. We discuss the possible drawbacks of the common source configuration and provide the reader with a comparative table between the two readout chains. The table contains several variants (column amplifier gain, in-pixel transistor sizes and type).

Keywords: Low light, CIS, pixel level amplification, 1/f noise, thermal noise, CDS, 4T pixel

1. INTRODUCTION

The market demand for electronic image sensors, and particularly CMOS sensors, is in continuous growth. Over the last decade, mobile handset and digital cameras occupied the biggest part of the market and fuelled the development of CMOS image sensors. Today, markets like medical, security, industrial vision, defence or space are expected to grow and increase the demand for more sensitive CMOS image sensors operating in poor light conditions. For decades charge-coupled devices (CCDs) have been the first choice technology in terms of sensitivity by offering the best noise performance. But the development of pinned photo diodes (PPD) increased dramatically the noise performance of CMOS image sensors and made them more attractive compared to CCD technology thanks to their lower cost, more on-chip functionalities, and higher data rates. In fact PPDs present two major advantages compared to conventional CMOS image sensors, the former consists in reset noise (kTC) cancellation thanks to the correlated double sampling, and the latter consists in dark current noise reduction due to p+ profile protecting from surface states and showing small depletion region.
During the last few years, different works have been presented demonstrating that the read noise of a CMOS image sensor (CIS), based on pixels with PPDs and four transistors, can go under one electron RMS[1 2 3] thanks to circuit techniques like column amplification, bandwidth control, correlated double sampling (CDS) and multiple sampling (CMS). A new challenge is raised consisting in reaching the 0.3 e^- RMS noise which is the limit for 90% quantization accuracy.
In state of the art low light CMOS image sensors readout chains, circuit techniques reduce effectively the reset noise, pixel offset and thermal noise. However, even with a CDS, $1/f$ noise and random telegraph signal originating from in-pixel amplifier dominates the read noise[4] . To address this problem, in-pixel amplifiers, with relatively low in-pixel $1/f$ noise, like pMOS[5] transistor or buried channel nMOS[1] can be used. The $1/f$ noise optimization through transistor dimensions is important to be discussed. In fact, both the pixel conversion gain and the $1/f$ noise power spectral density (PSD) depend on the gate area of the in-pixel amplifying transistor, thus, for a given technology the optimal gate dimensions have to be found.
In this work, we present two optimized low light CIS readout architectures. One is based on in-pixel source follower, high column gain with bandwidth control and CDS. And the other one with pixel level voltage gain using

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cascode common source stage, low gain column amplification and CDS. Analytical noise calculation corresponding to each readout scheme is presented in section 3. Optimization techniques for low readout noise are discussed in section 4. Section 5 compares the two optimized readout schemes and present a summary comparative table.

2. READOUT CIRCUIT ARCHITECTURES

2.1 Readout chain based on in-pixel source follower, high-gain column amplification and CDS

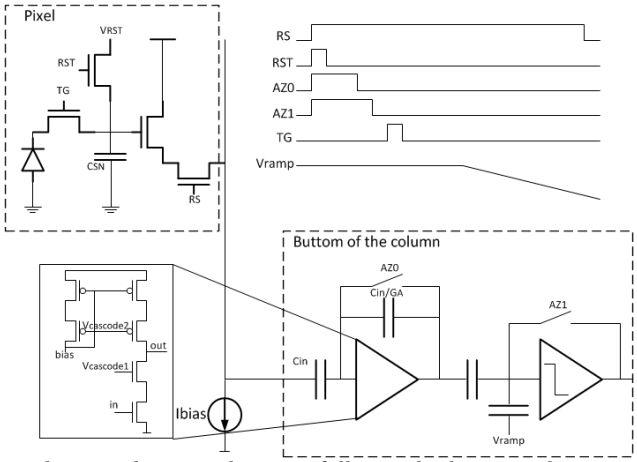

Figure 1: 4T readout chain with in-pixel source follower, high gain column amplification and CDS

The 4T pixel contains a transfer gate, reset and row selection switches and an amplifying transistor biased to operate in source follower configuration. During each readout, the sense node is reset before clocking the transfer gate which allows photo generated electrons to diffuse to the sense node. This induces a voltage drop at the output of the source follower stage. The efficiency of this mechanism is evaluated by the conversion gain (CG) given by[6]

$$CG = \frac{qG_{SF}}{C_{SN} + C_{GD} + (1 - G_{SF})C_{GS}} \tag{1}$$

Where G_{SF} is the gain of the source follower stage, C_{SN} is the sense node capacitance defined by parasitic capacitances of the reset transistor, the transfer gate, the n+ junction and wiring. It is decorrelated from the amplifying transistor parasitic capacitances contribution. C_{GD} and C_{GS} are gate drain and gate source capacitances of the in-pixel amplifying transistor, and q the charge of one electron.
The source follower voltage gain is approximately given by $\frac{g_{m,SF}}{g_{ms,SF}} = \frac{1}{n}$, where $g_{m,SF}$ and $g_{ms,SF}$ are the amplifying transistor gate and source transconductance and n is the slope factor whose value ranges from 1.2 to 1.6[7] . If a pMOS in-pixel amplifying transistor is used (see figure 2), the bulk can be connected to the source leading to a more efficient source follower stage where the gain is approximately equal to unity (0.99 in simulation). In fact $g_{m,SF} = g_{ms,SF}$ for a bulk source connected transistor. In this case the conversion gain increases, it is proximately given by

$$CG = \frac{q}{C_{SN} + C_{GD}} \tag{2}$$

Column amplification is commonly used in sensitive CMOS image sensors to reduce thermal noise by controlling the bandwidth and minimising the noise contribution of ADC stage[8,21] . As depicted in figure 1, column amplifier is implemented using a single stage complete cascode amplifier associated with two capacitors whose ratio determines the gain of the stage. This column amplifier limits the bandwidth at $265kHz$ and introduces variable gain. After auto-zeroing of the column amplifier, the frozen noise charge is transferred from the integrating to the feedback capacitor[9] , a double sampling stage is needed to cancel the frozen noise and perform the correlated double sampling (CDS). This can be done at the input of the single slope ADC thanks to AZ1 as depicted in figure 1. Indeed after AZ1 is clocked down at t_{AZ1}, the voltage variation at the input of the ADC comparator at

time t before ramping is given by $1/2(V_{out,amp}(t) - V_{out,amp}(t_{AZ1}))$ where $V_{out,amp}$ is the voltage at the output of the column amplifier. Auto-zeroing at the column amplifier and ADC comparator cancels their offset.

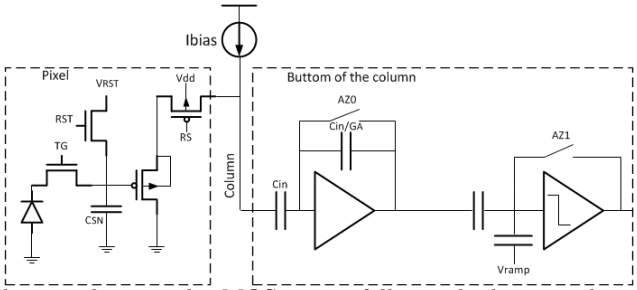

Figure 2: 4T readout chain with in-pixel, pMOS source follower, high gain column amplification and CDS

2.2 Readout chain based on in-pixel common-source, low-gain column amplification and CDS

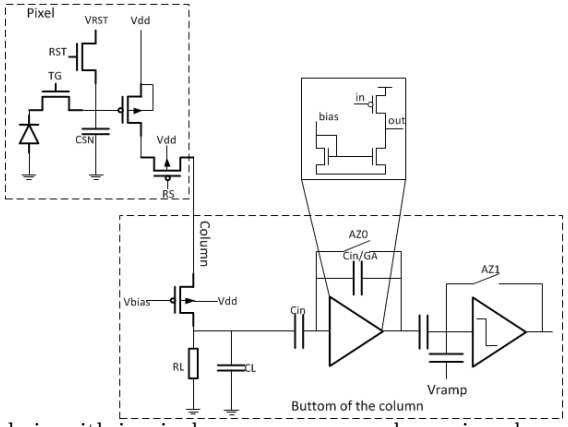

Figure 3: 4T readout chain with in-pixel, common source, low gain column amplification and CDS

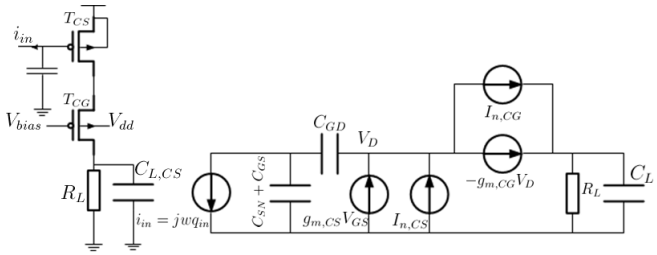

Figure 4: small signal analysis of the cmmon source based pixel circuit during readout

An other readout scheme depicted in figure 3 consists in introducing gain at pixel level as[56] . The in-pixel amplifying transistor can be used in common source configuration leading to open loop in-pixel gain. For common source based in-pixel gain, cascode structure is important to reduce the Miller effect. In fact, based on the small signal analysis depicted in figure 4, the conversion gain of a 4T pixel based on cascode common source is given by

$$CG = \frac{R_L g_{m,CS}}{C_{SN} + C_{GS} + C_{GD} + \frac{g_{m,CS}}{g_{m,CG}} C_{GD}} \tag{3}$$

Where $R_L g_{m,CS}$ is the open loop pixel level voltage gain given by the product of the load resistance R_L and the amplifying transistor transcoductance $g_{m,CS}$ and $g_{m,CG}$ is the transconductance of the cascode transistor. The

term $g_{m,CS}/g_{m,CG}$ is replaced by $R_L g_{m,CS} C_{GD}$ in case cascode is not used. The bandwidth control is achieved by means of C_L and column amplifier resulting in a second order low-pass filtering and CDS is implemented in the same way as in the source follower based readout chain. In this readout architecture, column amplifier noise is no more critical.

3. READ NOISE CALCULATION

3.1 Preliminary to noise calculation

Noise sources

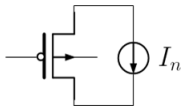

Figure 5: noisy transistor model

For noise calculation, we consider the noisy model of a MOS transistor in saturation depicted in figure 5 where the source drain noise current PSD including thermal white noise and $1/f$ noise is given by[7]

$$I_n^2(f) = 4kT\gamma g_m + \frac{K}{C_{ox}^{\alpha} WL} \frac{g_m^2}{f} \tag{4}$$

Where k is the Boltzmann constant, T the absolute temperature, g_m the transconductance of the transistor, γ the excess noise factor given by, in case the transistor is in strong inversion, $\frac{2n}{3}$ where n is the slope factor,[7] K is a process dependent parameter referred to as the Flicker noise constant, C_{ox} is the gate oxide capacitance area density for a given technology process and α is a process parameter whose value ranges between 1 and 2. For noise calculation in next sections, we consider $\alpha = 1$.

Inpact of CDS on 1/f and thermal noise

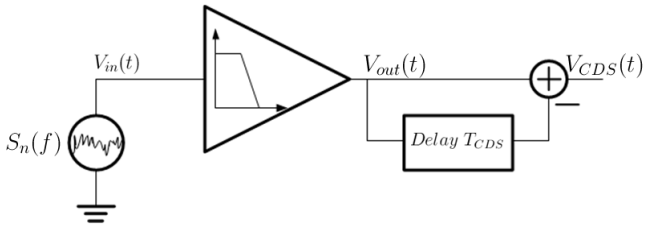

Figure 6: CDS model

The CDS is implemented after amplification and bandwidth control in column level circuitry. Figure 6 shows a simplified model of a CDS circuit. The signal is low-pass filtered before sampling. The output voltage after CDS can be expressed by

$$V_{CDS}(t) = V_{out}(t) - V_{out}(t - T_{CDS}) \tag{5}$$

Considering a first order low pass filtering with a cut-off frequency f_c, the transfer function of the CDS circuit is given by

$$H_{CDS}(f) = \frac{4sin^2(\pi T_{CDS} f)}{1 + (f/f_c)^2} \tag{6}$$

Consider a noise source at the input of CDS circuit with a power spectral density $S(f)$ given by

$$S_n(f) = N_{th} + \frac{N_{1/f}}{f} \tag{7}$$

Where N_{th} is the white noise PSD and $N_{1/f}$ represents a $1/f$ noise constant. The output noise PSD is given by

$$S_{n,CDS}(f) = S_n(f) \times H_{CDS}(f) \tag{8}$$

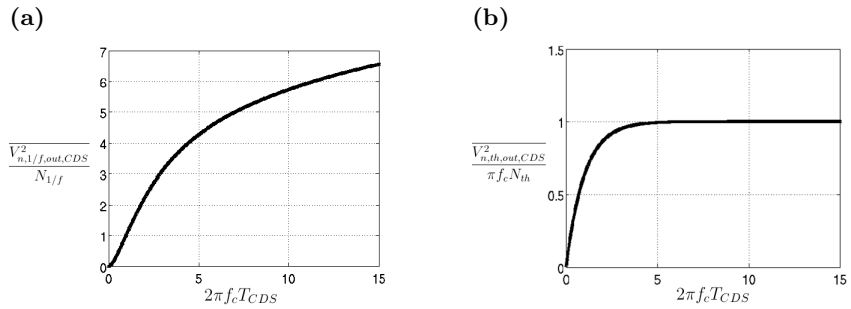

Figure 7: Impact of CDS on a first order low passed filtered white noise and $1/f$ noise: (a) $1/f$ noise variance as a function of $2\pi f_c T_{CDS}$; (b) white noise variance normalized with πf_c as a function of $2\pi f_c T_{CDS}$

Thus, the variances of thermal and $1/f$ noise can be expressed by

$$\overline{V^2_{n,th,CDS}} = N_{th} \int_0^\infty \frac{4sin^2(\pi T_{CDS} f)}{1 + (f/f_c)^2} df \tag{9}$$

$$\overline{V^2_{n,1/f,CDS}} = N_{1/f} \int_0^\infty \frac{4sin^2(\pi T_{CDS} f)}{f(1 + (f/f_c)^2)} df \tag{10}$$

Based on numerical evaluation, Figure 7 shows the $1/f$ noise noise variance after CDS and the thermal noise variance normalized with πf_c as a function of $2\pi f_c T_{CDS}$. Note that $2\pi f_c T_{CDS}$ should be at least equal to 5 for sufficient settling of the signal, thus, thermal noise variance can be given by

$$\overline{V^2_{n,th,CDS}} \simeq \pi f_c N_{th} \simeq 2\overline{V^2_{n,th,out}} \tag{11}$$

Thermal noise variance is then doubled by the CDS, and 1/f noise variance can be given by

$$\overline{V^2_{n,1/f,CDS}} \simeq \alpha_{CDS} N_{1/f} \tag{12}$$

Where α_{CDS} increases with T_{CDS} as depicted in figure 7. For enough settling of the signal $2\pi f_c T_{CDS}$ should be at least equal to 5, in which case α_{CDS} is approximately equal to 4.3.

3.2 In-pixel source follower based readout chain

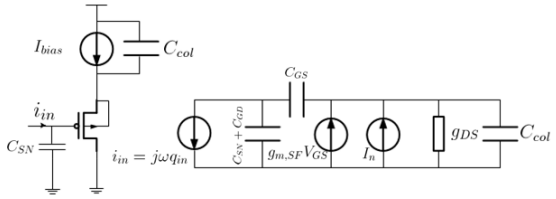

Figure 8: small signal analysis of the source follower based pixel circuit during readout

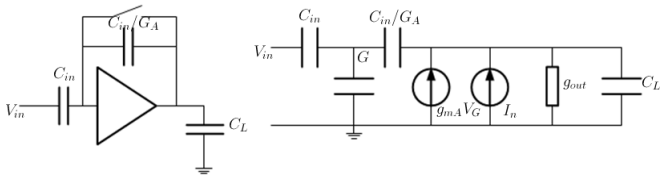

Figure 9: small signal analysis of the column amplifier

Auto-zeroing of the column amplifier cancels its offset. During this auto-zeroing, noise is frozen in the integration capacitor C_{in} and transferred to the output during the amplification phase. But thanks to AZ1 (see

figure 1) this frozen noise is cancelled. Thus we only take under consideration the random temporal noise during amplification phase. During this phase, for calculation of the column amplifier frequency response, we use the small signal analysis depicted in figure 9. For noise originating from the column amplifier, we only consider thermal noise since the column amplifier can be designed with transistors large enough to neglect their $1/f$ noise contribution compared to the one of the in-pixel amplifier transistor. The PSD of the noise current originating from the complete cascode amplifier stage is given by

$$I_{n,A}^2(f) = 4kT\gamma_A g_{m,A} \tag{13}$$

$V_{n,th,A,out}^2(f)$ and $V_{n,th,pix,out}(f)^2$ are, respectively, the noise power spectral densities of noise originating from the column amplifier and the pixel amplifying transistor, at the output of the column amplifier, calculated in the appendix based on the small signal analysis depicted in figure 8 and 9. The two noise sources are decorrelated. Based on equation (11), the variance of thermal noise is doubled after CDS when the signal is settled. Thus the variance of the total input referred thermal noise after CDS is given by

$$\overline{Q_{n,th,SF}^2} = 2\frac{1}{G_A^2 CG^2}\int_0^\infty V_{n,th,A,out}^2(f) + V_{n,th,pix,out}^2(f)df \tag{14}$$

Where CG is the pixel conversion gain and G_A the column amplifier closed loop gain. In case $G_A \gg 1$ and $G_A g_{out} \ll g_{m,A}$, i.e. the open loop gain is much greater than the closed loop gain. We also neglect the zero frequency since it is of the same order of the second pole frequency. The mean square of the input referred thermal noise of the source follower based readout chain is given by

$$\overline{Q_{n,th,SF}^2} = 2\frac{kT\gamma_{SF}}{G_A C}\frac{g_{m,A}}{g_{m,SF}}(C_{SN} + c_{GD}W + c_{GS}WL)^2 + 2\frac{kT\gamma_A}{G_A C}(C_{SN} + c_{GD}W)^2 \tag{15}$$

Where $C = C_L + \frac{C_{in}}{G_A+1}$, W and L are respectively, the width and length of the in-pixel amplifying transistor gate, c_{GD} the overlap capacitance defined by $C_{GD} = c_{GD}W$ and C_{GS} the gate oxide capacitance density defined by $C_{GS} = c_{GS}WL$. For $1/f$ noise, since the noise contribution of the column amplifier can be neglected, using equation (12) and equations (23)(24) in the appendix. The variance of the input referred $1/f$ noise is then approximately given by

$$\overline{Q_{n,1/f,SF}^2} = \alpha_{CDS}\frac{K}{C_{ox}WL}(C_{SN} + c_{GS}WL + c_{GD}W)^2 \tag{16}$$

Where α_{CDS} is the $1/f$ noise factor defined in (12).

3.3 In-pixel common source based readout chain

In this configuration, the noise contribution of the column amplification stage can be neglected thanks to the pixel level voltage gain. Based on the small signal analysis depicted in figure 4 and noisy model of the common source and common gate transistors, the input referred noise PSD is then given by

$$Q_{n,CS}^2(f) = \left((C_{SN} + C_{GS} + C_{GD})^2\left(\frac{I_{n,CS}(f)}{g_{m,CS}}\right)^2 + (C_{GD})^2\left(\frac{I_{n,CG}(f)}{g_{m,CG}}\right)^2\right)\frac{1}{1 + (2\pi R_L C_{L,CS} f)^2}\left|H_A(f)\right|^2 \tag{17}$$

Where $H_A(f)$ is the transfer function of the column amplifier defined in equation (25) (see appendix). Note that the bandwidth control in this configuration can be achieved by the pixel level amplifier stage and column amplifier stage. Due to in-pixel voltage gain, column amplifier noise contribution is insignificant. The input referred thermal noise after CDS is given by

$$\overline{Q_{n,th,CS}^2} = 2(C_{SN} + C_{GS} + C_{GD})^2\frac{kT\gamma_{CS}}{R_L g_{m,CS} C_{L,CS} + G_A\frac{g_{m,CS}}{g_{m,A}}C} + 2\left(C_{GD}\right)^2\frac{kt\gamma_{CG}}{R_L g_{m,CS} C_{L,CS} + G_A\frac{g_{m,CG}}{g_{m,A}}C} \tag{18}$$

Where $C = C_L + \frac{C_{in}}{G_A+1}$.
Since the cascode transistor (T_{CG}) is outside the pixel (column level), this transistor can be designed to obtain

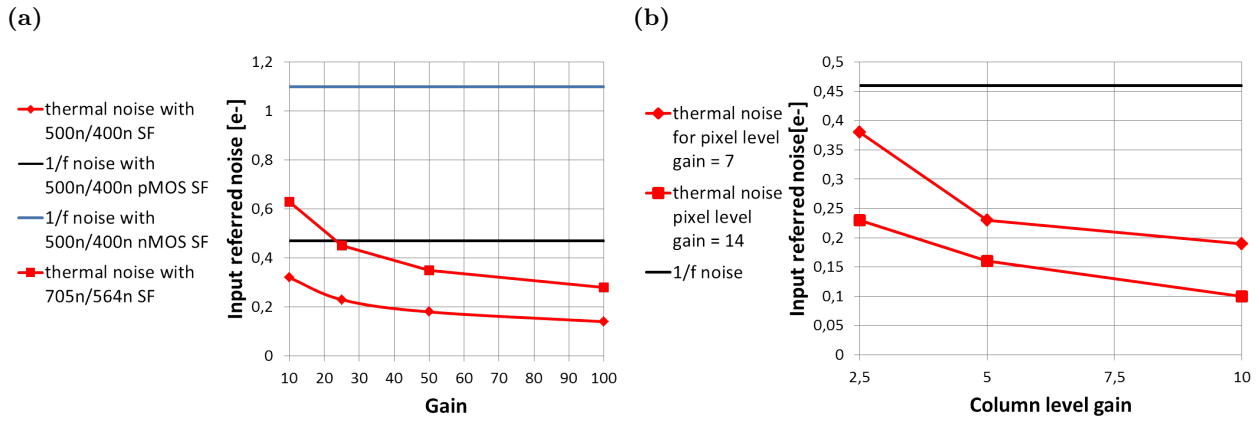

Figure 10: Transient noise simulation results showing: (a) Input reffered thermal and $1/f$ noise contributions in $[e^-]$ RMS of the source follower based readout chain presented in figure 1 and 2 using in-pixel nMOS and pMOS amplifying transistors and different column gains; (b) Input reffered thermal noise in $[e^-]$ RMS of the common source based readout chain presented in figure 3 for different pixel and column level gains

$g_{m,CG}$ higher than $g_{m,CS}$. therefore, thermal noise contribution of the cascode transistor (common gate stage) is insignificant. The input referred thermal noise can be written as

$$\overline{Q^2_{n,th,CS}} = 2\frac{kT\gamma_{CS}}{R_L g_{m,CS} C_{L,CS} + G_A \frac{g_{m,CS}}{g_{m,A}} C}(C_{SN} + c_{GS}WL + c_{GD}W)^2 \tag{19}$$

Note that for common source based readout chain, both column level gain G_A and pixel level gain $R_L g_{m,CS}$ reduce input referred thermal noise. For $1/f$ noise, since T_{CG} can be designed much larger than T_{CS}, the in-pixel amplifying transistor is the dominant contributor and the input referred $1/f$ noise is given by

$$\overline{Q^2_{n,1/f,CS}} = \alpha_{CDS}\frac{K}{C_{ox}WL}(C_{SN} + c_{GS}WL + C_{GD}W)^2 \tag{20}$$

4. DESIGN OPTIMIZATION FOR LOW READOUT NOISE

Equations (15) and (19) suggest that thermal noise, for a given bandwidth and a given sense node capacitance C_{SN}, can be reduced by low amplifying transistor parasitic capacitances (low W and L) and high gain which is a parameter that can be independent of the pixel design, this offers a degree of freedom in readout chain optimization.

For $1/f$ noise, equations (16) and (20) show that the only design parameters for readout chain optimisation are the in-pixel amplifying transistor width and length. Figure 10 shows transient noise simulation results (ELDO) of a source follower based readout chain separating $1/f$ from thermal noise contributions. Simulation confirms the predicted results based on analytical noise calculation. Input referred thermal noise decreases with column gain following $1/\sqrt{Gain}$. Transient noise simulation shows that input referred thermal noise decreases by in-pixel amplifying transistor dimensions decrease from $(705nm/564nm)$ to $(500nm/400nm)$ (conserving the same W/L ratio).

Figure 10 shows an other important result. If in-pixel nMOS amplifier is used, $1/f$ noise dominates clearly the read noise. The most obvious way to reduce $1/f$ noise is by using a pMOS transistor instead of an nMOS, in which case it becomes more fruitful to optimize the in-pixel amplifying transistor dimensions for the best input referred noise.

Thus, for readout chain total noise optimization we suggest to reduce $1/f$ noise by using in-pixel amplifying transistor gate dimensions W and L and reduce thermal noise by using column gain, the latter parameter is independent from the formers.

Based on equations (16) and (20) The design strategy to enhance pixel sensitivity is to find the optimal W and

L values for a given technology by minimising $\frac{\overline{Q^2_{n,1/f,in}}}{\alpha_{CDS}K}$. Figure 11 shows the variation of this expression as a function of W and L for $130nm$ process technology with $c_{GS} = 0.8fF/\mu m^2$, $c_{GD} = 0.4fF/\mu m$, $C_{SN} = 0.658fF$ corresponding to simulated parasitic capacitance of a transfer gate and a reset transistor with minimum gate width, $\alpha_{CDS} = 5$ and $K = 10^{-25}V^2F/s$ for a pMOS transistor. One can notice that for low C_{SN} the best $1/f$ noise performance is obtained for values of W lower than minim width allowed by technology. Thus we fix W at a value W_{min} that can be the minimum length allowed by the technology node or a bit more to minimise the mismatch. The optimal value of the length can be derived from equation (16) and (20). It is then given by

$$L_{optimal} = \frac{c_{GD}}{c_{GS}} + \frac{C_{SN}}{W_{min}c_{GS}} \tag{21}$$

We conclude that for the best $1/f$ noise performance, the layout should be optimised in order to have the smallest sense node capacitance C_{SN}, using the lowest W and choosing L based on equation (21). Figure 12 shows the results of transient noise simulations of the source follower based readout chain. Simulation confirms the analytical prediction. In fact, by fixing W at the minimum width of $500nm$, the input referred $1/f$ noise decreases with gate length increase as predicted by figure 11 based on analytical noise calculation.

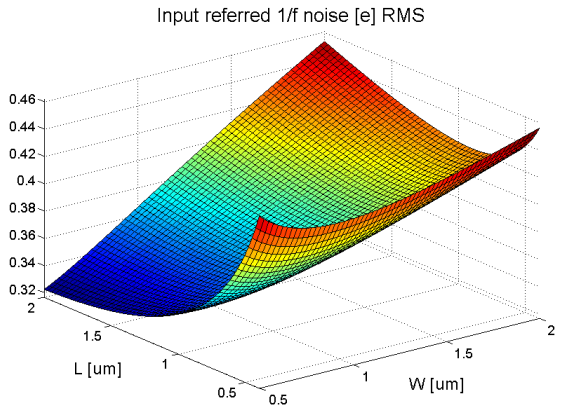

Figure 11: Calculataed input reffered $1/f$ noise of source follower and common source based readout chains as a function of the width W and length L of amplifying transistor with $c_{GS} = 0.8fF/\mu m^2$, $c_{GD} = 0.4fF/\mu m$, $C_{SN} = 0.658fF$, $\alpha_{CDS} = 5$ and $K = 10^{-25}V^2F/s$

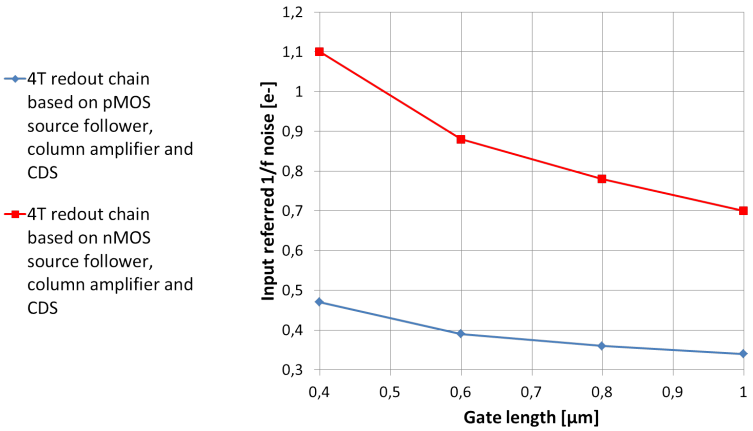

Figure 12: Simulated (transient noise simulation) input referred $1/f$ noise of common source and source follower based readout chains based on in-pixel amplifying transistor with minimum gate width ($500nm$) and increasing gate length

5. COMPARISON

Based on analytical noise calculation and simulation results, both optimized common source and source follower based readout chains exhibits the same $1/f$ noise. For common source based readout chain, the in-pixel voltage gain makes the $1/f$ noise contribution of the column amplifier insignificant. Thus constraints on column amplifier transistors sizes are reduced unlike the source follower based readout chain where column amplifier $1/f$ noise is critical. Therefore large transistors have to be used resulting in silicon area one order of magnitude larger than the column amplifier of the common source based readout chain and more power consumption.
Analytical noise calculation and simulation results give advantage to the common source configuration for input referred thermal noise. The column amplifier gain source follower based readout chain offers a degree of freedom for thermal noise reduction independent on the pixel design. As predicted with analytical noise calculation, simulation results show that, generally, common source based readout noise shows less input referred thermal noise since the noise contribution of the column amplifier is mitigated due to pixel level voltage gain. Both configurations can exhibit the same input referred thermal noise if the column amplifier of the source follower based readout chain exhibits high gain (about 100 in our design).

	Characteristics	Power consumption	$1/f$ noise[e^- RMS]	Thermal noise[e^- RMS]	Total noise[e^- RMS]
In-pixel nMOS ($500nm/400nm$) source follower, column gain and CDS	$Gain = 10$ one stage column amplifier	pixel:$1.5\mu A$ column:$250nA$	1.1	0.32	1.15
In-pixel optimized nMOS ($500nm/800nm$) source follower, column gain and CDS	$Gain = 10$ one stage column amplifier	pixel:$1.5\mu A$ column:$250nA$	0.8	0.34	0.86
In-pixel optimized pMOS ($500nm/800nm$) source follower, column gain and CDS	$Gain = 10$ one stage column amplifier	pixel:$1.5\mu A$ column:$250nA$	0.39	0.44	0.59
	$Gain = 100$ one stage complete cascode column amplifier	pixel:$1.5\mu A$ column:$2\mu A$	0.36	0.16	0.39
In-pixel optimized pMOS ($500nm/800nm$) cascode common source, column gain and CDS	Pixel level gain 7, column level gain of 10 one stage column amplifier	pixel:$4.4\mu A$ column:$250nA$	0.28	0.19	0.34

Table 1: Comparison table of transient noise simulation results (ELDO) of different readout schemes

6. CONCLUSION

In this work, we present analytical noise calculation of two low light CIS readout architectures. One is based on in-pixel source follower, high column gain with bandwidth control and CDS. The other one is based on pixel level voltage gain using cascode common source stage, low gain column amplification and CDS. Thanks to noise calculation confirmed by simulation we come to the following conclusions:

- The readout architecture based on pixel-level gain does not show obvious advantage in terms of readout noise compared to the source follower based one, despite the reduction of constraints on column amplifier design.
- For both configurations, thermal noise is reduced with bandwidth control, gain (column gain for source follower based readout chain and both column and pixel level gain for common source based readout chain) and gate area reduction of the in-pixel amplifying transistor (see equations (15) and (19)).
- If nMOS in-pixel amplifying transistor is used, its $1/f$ noise contribution dominates the readout chain noise.

- The best $1/f$ noise performance of the readout chain is obtained for in-pixel amplifying transistor with the minimum gate width allowed by technology. For a given gate width, $1/f$ noise decreases with gate length increase until the optimal value given by equation (21) is reached.

APPENDIX

Based on the small signal analysis depicted in figure 8, thermal noise power spectral density at the output of the pixel is given by

$$V_{n,th,pix}^2(f) = \frac{4kT\gamma/g_{m,SF}}{1+\left(2\pi f \frac{C_{col}}{g_{m,SF}} \frac{C_{SN}+C_{GD}+C_{GS}}{C_{SN}+C_{GD}}\right)^2} \left(\frac{C_{SN}+C_{GD}+C_{GS}}{C_{SN}+C_{GD}}\right)^2 \tag{22}$$

The $1/f$ noise power spectral density at the output of the pixel is given by

$$V_{n,1/f,pix}^2(f) = \frac{K}{C_{ox}WL}\frac{1}{f}\frac{1}{1+\left(2\pi f \frac{C_{col}}{g_{m,SF}} \frac{C_{SN}+C_{GD}+C_{GS}}{C_{SN}+C_{GD}}\right)^2} \left(\frac{C_{SN}+C_{GD}+C_{GS}}{C_{SN}+C_{GD}}\right)^2 \tag{23}$$

One can find after calculation that the power spectral density of noise originating from the pixel readout circuit can be expressed as

$$V_{n,pix,out}^2(f) = |H_A(f)|^2 V_{n,pix}^2(f) \tag{24}$$

Where $H_A(f)$ is the transfer function of the column amplifier given by

$$H_A(f) = \frac{j2\pi f C_{in} - g_{m,A}G_A}{(G_A+1)g_{out} + g_{m,A} + j2\pi f((G_A+1)C_L + C_{in})} \tag{25}$$

And power spectral density of noise originating from the noise canceller stage can be expressed as

$$V_{n,A,out}^2(f) = \left|\frac{G_A+1}{(G_A+1)g_{out} + g_{m,A} + j2\pi f((G_A+1)C_L + C_{in})}\right|^2 I_{n,A}^2(f) \tag{26}$$

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