Graphene for Nanoelectronic Applications

THÈSE N° 6886 (2015)

PRÉSENTÉE LE 14 DÉCEMBRE 2015
À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DES DISPOSITIFS NANOÉLECTRONIQUES
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

PAR

Pankaj SHARMA

acceptée sur proposition du jury:

Prof. G. De Micheli, président du jury
Prof. M. A. Ionescu, directeur de thèse
Prof. T. Palacios, rapporteur
Prof. G. Fiori, rapporteur
Dr A. Magrez, rapporteur

You must be the change you wish
to see in the world.
— Mahatma Gandhi

To my parents. . .

Acknowledgements

First and foremost, I would like to sincerely thank my supervisor Prof. Adrian Ionescu for giving me the opportunity to be part of his group. Your guidance, not only in terms of giving ideas and solving research problems, but also in terms of giving freedom to do research in my own way has proved to be useful and invaluable. I greatly appreciate his visionary foresight, his inspiring personality and his vast knowledge in a wide range of topics. It's truly been a privilege to work with him and I am deeply grateful for his support, confidence, open-mindedness and for having introduced me to the world of electron device research. Next, I would like to thank late Prof. Julien Perruisseau-Carrier who was my co-advisor for first 3 years of my PhD; he tragically died in mid-2014. I will be ever grateful for his support, encouragement and am sorry that he has not lived to see me graduate. Julien was an extremely supportive supervisor and all in all a wonderful person.

I would like to acknowledge the members of the jury for having accepted to review my PhD thesis : Prof. T. Palacios from Massachusetts Institute of Technology, USA, Prof. G. Fiori from University of Pisa, Italy, Dr. A. Magrez from EPFL and Prof. G. De Micheli, president of the jury, from EPFL.

I would like to express my sincere thanks to Dr. Arnaud Magrez and Laurent Bernard from crystal growth facility, EPFL. Thanks for the fruitful collaboration and for providing graphene samples, Raman data and useful suggestions. Special thanks to Laurent for teaching me how to transfer graphene and for giving invaluable tips in the graphene fabrication process. For the help in device measurements, I would like to thank: Dr. Antonios Bazigos and Dr. Wladek Grabinski. Special thanks to Antonios for sharing with me his extensive knowledge about semiconductor device measurements, and for useful suggestions while preparing different manuscript together. Special thanks also to Juan Sebastián Gómez-Díaz for his immense help in the beginning of my PhD years in terms of his advices and guidance in developing my skills in academic writing and in microwave engineering.

Furthermore, I wish to thank Isabelle, Karin, Marie and Lucie for taking care of the administrative procedures. I am also thankful to the funding sources: Grafol; and to the staffs of EPFL Center of MicroNanoTechnology (CMi) for their support in the device fabrication. I thank all my colleagues in Nanolab for their cheerful characters, kindness and willingness to help.

Finally, special thanks go to my family and friends, in Switzerland and in India, and especially to my parents, for always believing in me, and for their unconditional love, support and encouragement. Last but not least, I would like to thank my wife Preeti, for always being there for me, and for her love and encouragement that was always available when I needed it the

most.

Lausanne, 09 Septembre 2015 P. S.

Abstract

During the past decade, graphene — a monolayer of carbon atoms — has attracted enormous interest for its use in nanoelectronic device applications. The absence of bandgap, however, has stalled its use both in logic (inability to turn off) and radio frequency (poor power gain) applications. Graphene nanoelectronic devices based on alternative and complementary approaches, which yet exploit its fundamental properties rather than trying to change them, are needed for realistic applications. The work in this thesis proposes two such alternative approaches for graphene's application.

The first approach examines the use of graphene as a membrane of radio frequency (RF) nanoelectromechanical systems (NEMS) capacitive switches. Owing to its extreme thinness and exceptional mechanical properties, the use of graphene in RF NEMS switches could enable lower actuation voltages and faster switching. To evaluate its electromagnetic performance, a framework for the full-wave simulation of graphene-based RF NEMS switch is developed for the first time. A rigorous modeling approach for graphene NEMS switch taking into account both its frequency-dependent conductivity, and the variation of conductivity in the up- and down-state is presented. Our results show that RF NEMS switches based on graphene with lower sheet resistivity values can deliver superior isolation and reduced losses at micro and millimeter wave frequencies, and their isolation can also be tuned with bias voltage. An attempt is also made to characterize the fabricated switches.

The second approach deals with the negative differential resistance (NDR) phenomenon in planar graphene solid-state devices. The key advantage of planar graphene-based NDR devices is their ability to exhibit NDR at higher current levels, thanks to its high mobility and saturation velocity. The observation of NDR is reported in the output characteristics of graphene field effect transistors for various channel lengths and dielectric thicknesses at room temperature. The transistors are fabricated using chemical vapor deposition graphene with a top gate oxide down to 2.5 nm of equivalent oxide thickness. To understand the NDR phenomenon in graphene transistors, we perform extensive theoretical studies based on drift-diffusion model. This understanding allows us to design a novel graphene circuit which shows enhanced NDR characteristics and is more relevant for applications. Finally, the potential of this graphene NDR circuit is evaluated for RF reflection amplifiers application.

Key words: Graphene, Nanoelectromechanical systems (NEMS) , RF NEMS (MEMS) switch, microwave, millimeter waves, negative differential resistance (NDR), field effect transistor,

negative differential conductance (NDC), GFET.

Résumé

Au cours de la dernière décennie, le graphène — une monocouche d'atomes de carbone — a attiré un grand intérêt pour son utilisation dans des applications de dispositifs nanoélectroniques. Cependant, l'absence de bande interdite a entravé son utilisation à la fois dans des applications de logique (incapacité à s'éteindre) et de radiofréquence (gain de puissance faible). Des dispositifs nanoélectroniques de graphène basés sur des approches alternatives et complémentaires, qui exploitent ses propriétés fondamentales plutôt que d'essayer de les changer, sont nécessaires pour des applications réalistes. Le travail de cette thèse propose deux de ces approches alternatives pour des applications du graphène.

La première approche examine l'utilisation du graphène comme une membrane de commutateurs capacitifs de systèmes nanoélectromécaniques (NEMS) radiofréquences (RF). En raison de sa minceur extrême et de ses propriétés mécaniques exceptionnelles, l'utilisation du graphène dans les commutateurs RF NEMS pourrait permettre des tensions d'actionnement inférieures et une commutation plus rapide. Pour évaluer son rendement électromagnétique, un cadre pour la « simulation d'onde complète » de l'interrupteur RF NEMS à base sur le graphène a été développé pour la première fois. Une modélisation rigoureuse des commutateurs NEMS de graphène est effectuée en tenant compte à la fois de sa conductivité dépendante de la fréquence, et de la variation de conductivité dans les états haut et bas. Nos résultats montrent que le graphène avec une résistivité de surface inférieure peut fournir une isolation supérieure et des pertes réduites dans la plage de fréquences des micro-ondes et des ondes millimétriques, aussi l'isolation peut également être réglée avec la tension de polarisation. Une tentative de caractérisation des interrupteurs fabriqués est également menée.

La seconde approche traite du phénomène de résistance différentielle négative (RDN) dans les dispositifs semi-conducteurs planaires en graphène. Le principal avantage des dispositifs planaires RDN à base de graphène est leur capacité à présenter une RDN à des niveaux de courant plus élevés, grâce à la grande mobilité et à la vitesse de saturation du matériau. L'observation de la RDN est rapportée dans les caractéristiques de sortie des transistors à effet de champ en graphène pour différentes longueurs de canal et épaisseurs de diélectrique à température ambiante. Les transistors sont fabriqués en utilisant un dépôt chimique en phase vapeur de graphène avec un oxyde de la grille supérieure allant jusqu'à 2.5 nm d'épaisseur d'oxyde équivalente. Pour comprendre le phénomène RDN dans les transistors de graphène, nous effectuons des études théoriques approfondies basées sur le modèle de dérive-diffusion. Cette compréhension nous permet de concevoir de nouveaux circuits de graphène qui montrent des caractéristiques supérieures de RDN et sont plus pertinents pour des applications. Enfin,

la RDN de ce circuit de graphène est évaluée pour l'application des amplificateurs à réflexion.

Mots clefs : graphène, nanoélectromécaniques systèmes (NEMS), RF NEMS (MEMS) commutateur, micro-ondes, des ondes millimétriques, résistance différentielle négative, Transistor à effet de champ, conductance différentielle négative, GFET.

Contents

Contents

List of Figures

List of Tables

1 Introduction

1.1 The Need of Alternative Device Principles and New Materials

We are all well aware of the remarkable progress in silicon integrated circuit technology over the past several decades. This progress has been largely driven by technology innovations that have enabled the scaling of the metal-oxide-semiconductor field-effect transistor (MOS-FET) into smaller dimensions, thereby leading to both higher speed and device density [1, 2]. In the recent past, however, it has become more and more difficult to achieve the required performance improvements when scaling the silicon MOSFET. This realization has spurred an intense search for alternative technologies, an effort that involves searching for both new device principles and materials — popularly known as the *More-than-Moore* domain. The new device principles include areas such as analog/RF (radio frequency), nanoelectrome-chanical systems (NEMS), actuators, sensors, *etc.* whose primary purpose is to enhance the functionality of integrated circuits (ICs) by complementing the digital electronics components. Whereas the sub-domain of new material search aims to replace or complement the existing materials used in the devices with new materials so as to enhance the overall performance of the device.

Carbon-based materials are of great interest for use in nanoelectronic applications. In past, much attention was paid to carbon nanotubes (CNTs) owing to their fascinating electrical and mechanical properties. However, their imprecise positioning on the target substrate is one of its major disadvantage, which impede their introduction into the standard CMOS process where more than 1 billion devices need to be connected [3].

Since last 10 years, graphene — a two-dimensional carbon-based material — has attracted intense research for use in nanoelectronic applications. It has remarkably unique mechanical (Young's modulus up to 1 TPa) [4], electrical (electron mobility up to 200,000 cm^2/Vs for suspended graphene) [5] and thermal (thermal conductivity up to 5000 W/mK) [6] properties. This motivates research that investigates its use in wide range of applications including nanoelectronics, photonics, electrochemical *etc.*

Talking of its electronic properties, graphene is a zero band gap material with high carrier mobility. Because of the absence of band gap, the use of large-area graphene was not considered for digital electronics. Although, significant efforts have been made to induce a band gap in graphene including narrowing it to make nano ribbons, still these methods lack practicality [7]. Being a high mobility material, graphene was extensively considered for radio frequency applications because in these applications graphene transistor is used as an amplifier which need not be turned off. In the last decade, intensive work for graphene's use in RF transistors was carried out targeting mainly the cut-off frequency (f_T) which is one of the metric for accessing the performance of RF transistors [8, 9, 10, 11, 12, 13, 14]; the highest f_T of 427 GHz was demonstrated by [15]. For use in practical RF circuits, however, a good power gain is equally important which is evaluated by the parameter: maximum frequency of oscillation f_{MAX}. Since graphene has no band gap, it suffers from poor f_{MAX} as this parameter depends on the ability to have a good current saturation — a phenomenon more favourable in materials with band gap [16].

Thus, it was concluded that amplifiers and switches may not be the best application for graphene as it does not have the band gap [3, 17, 16, 18]; the focus thus shifted to other two-dimensional materials with band gap [19, 20, 21, 17, 3]. Nonetheless, unconventional approaches to realize switches and amplifiers also exist and is the main goal of this thesis. The first approach concerns with nanoelectromechanical switch using graphene which offer unique advantages over conventional solid-state switches such as reduced leakage currents and power consumption, and improved ON/OFF ratios. The second approach deals with negative differential resistance phenomenon in graphene transistors and circuits which can be exploited to realize numerous applications such as amplifiers, oscillators, switches, memory *etc.*

1.2   Overview of Graphene Research

Graphene is the name given to individual sheets of carbon atoms arranged in a two-dimensional (2-D) honeycomb lattice. It is a fundamental building block for a range of familiar carbon materials such as three-dimensional (3D) graphite, one-dimensional (1D) carbon nanotubes, and zero-dimensional (0D) fullerene as shown in Fig. 1.1 [22]. Theoretically, graphene has been studied since 1947 [23], and its preparation and isolation was thought to be an impossible goal for many decades. In 2004-05, group of papers by Novoselov *et al.* [24], Zhang *et al.* [25], and Berger *et al.* [26] demonstrated — for the first time — the isolation of graphene and the occurrence of the field effect in their samples. These papers ignited tremendous interest in research community to develop nanoelectronic applications for graphene.

In 2007, the experiments in successfully fabricating suspended graphene [27, 28], considerably increased the attention on this material in the field of nanoelectromechanical systems (NEMS). Thus far, the research on graphene-based NEMS has focused mainly on resonators [28, 29, 30, 31, 32, 33, 34, 35], and some on sensors [36, 37] and DC switches [38, 39, 40, 41, 42].
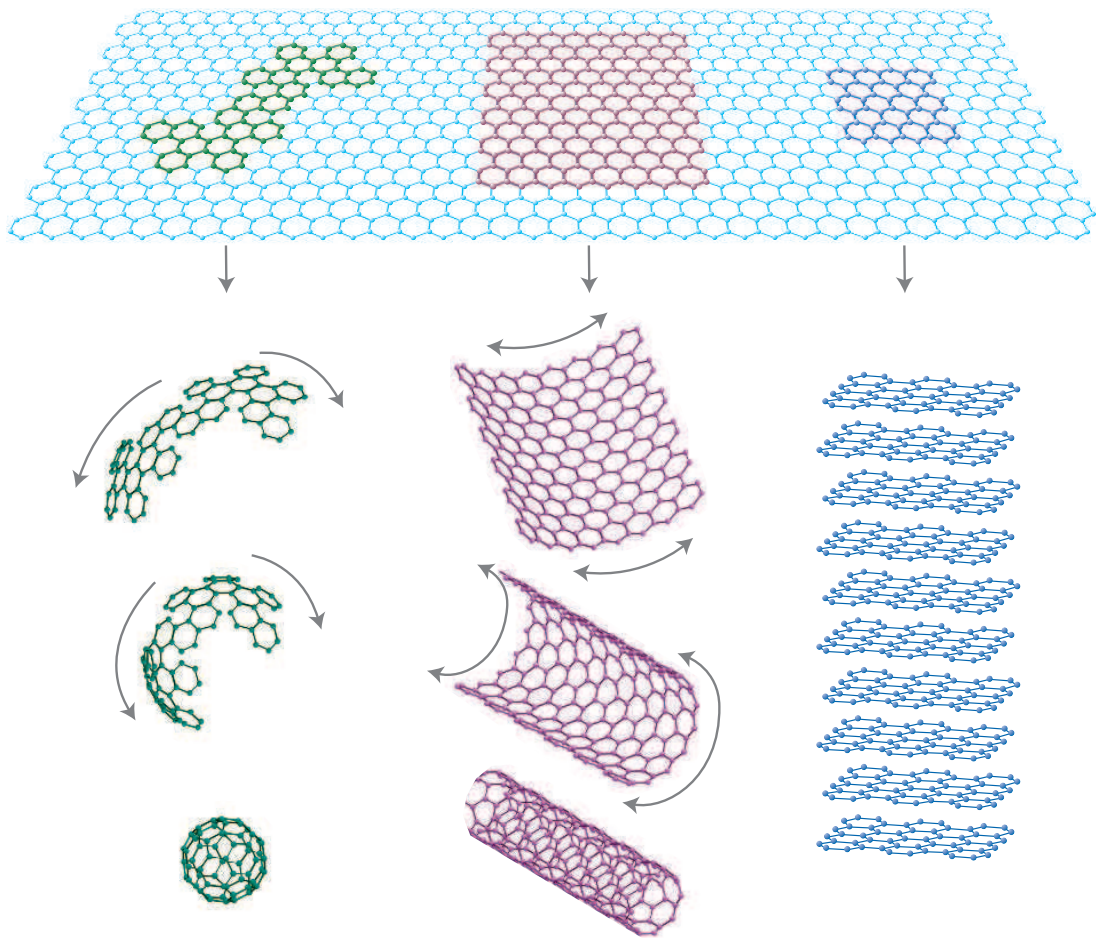
Figure 1.1: Graphene: a 2-D building block for sp^2 carbon allotropes of every other dimentionality: from 0D buckyball, to 1D nanotube, upto 3D graphite. Adapted from [22].

For the case of graphene solid-state devices, as discussed in the previous section, the use of graphene as amplifiers based on the conventional approach (exploiting its transconductance) was intensely researched in the last decade but is less accessed now owing to its poor power gain. A new class of alternative RF nanoelectronic devices — such as frequency multipliers [43, 44], mixers [45], digital modulators [46, 47] — which exploits the amplipolarity of graphene, have also been explored in recent past. Infrared photodetectors [48, 49, 50] are another class of alternative graphene solid-state devices that shows superior performance than its silicon counterpart today.

1.3 Graphene Properties Relevant for Nanoelectromechanical Devices

1.3.1 Mechanical Properties

The mechanical properties of any solid depend on the strength of its inter-atomic bonds. The strong carbon–carbon sp^2 bonds in graphene enable it with ultra-high intrinsic strength which exceeds any other material [22]. The bulk graphite material itself is highly anisotropic material. The in-plane Young's modulus of graphite is 920 GPa and the Poisson's ratio is 0.16 [41]. The mechanical properties of both monolayer and multilayer graphene have been investigated experimentally and theoretically. The first experimental study of elastic properties and strength of graphene has been done by Lee *et al.* [4]. In this study, a graphene membrane was deposited on the array of trenches in SiO_2 and the mechanical measurements were performed by loading the diamond-coated tip of the atomic force microscopy on graphene; a very high Young's modulus of ~1.0 TPa and the ultimate breaking strength of ~130 GPa was reported. Gomez-Navarro *et al.* reported a Young's modulus of 0.25 ± 0.15 TPa for a chemically reduced monolayer graphene oxide beam by AFM nanoindentation [51].

1.3.2 Thermal Properties

Bulk graphite has a basal thermal conductivity of 1000 W m^{-1} K^{-1}, providing a basis for the high thermal conductivity of graphene sheet. Theoretically, the intrinsic thermal conductivity of graphene has been found to be isotropic and calculated to be of value 2200 W m^{-1} K^{-1} at 300 K, independent of the number of the layers [52]. Balandin *et al.* [6] investigated the thermal conductivity in a suspended monolayer graphene performed with the help of confocal micro-Raman spectroscopy. The measured room temperature thermal conductivity was up to 5300 W m^{-1} K^{-1}, which was extracted for a monolayer graphene from the dependence of the Raman G peak frequency on the excitation laser power.

1.3.3 Other Properties

Graphene has the greatest advantage of being a chemically stable material [53]. In particular, since graphene is stable in air at room temperature and remains intact following exposure to all but the most caustic chemicals, it can be straightforwardly exfoliated from graphite via mechanical/chemical methods in an array of commonly available solvents. Following exfoliation, the chemical stability of graphene implies that it can be further subjected to subsequent processing and characterization with minimal precautions. Consequently, graphene can be subjected to most of the wet chemicals used in the standard CMOS processes, making it compatible with silicon-based devices.

Another benefit of graphene is its substrate independence. For instance, graphene can be synthesized by the most widely used chemical vapor deposition (CVD) process where graphene is first grown elsewhere on metal in the furnace, dispersed in wet etchant to remove underlying metal, and then transferred onto any substrate of choice, while keeping its structure and transport properties intact [3]. This allows the highest degree of flexibility in terms of fabricating devices based on suspended or non-suspended graphene on almost any substrate in any pre-defined location.

1.4 Graphene Properties Relevant for Solid-State Devices

1.4.1 Graphene Bandstructure

To understand the physics of graphene-based devices, it is essential to understand its energy band structure — depicted by energy-momentum relationship — which describes those ranges of energy that an electron within the solid may have and ranges of energy that it may not have. The honeycomb structure of graphene containing two atoms per unit cell, as shown in Fig. 1.2a, leads to a unique band structure (Fig. 1.2b); this band structure was first calculated by Walace in 1947 using the tight-binding approach [23]. Since much of the fundamental interest lies in understanding the electron transport at low energies, the band structure can be simplified to two cones with the upper cone (conduction band) touching the lower cone (valence band) at the so called Dirac point [54], having no energy gap in between (Fig. 1.2c). This is the most important aspect of graphene's band structure; that is, it has a linear energy-momentum relationship given by

$$E = \pm \hbar v_F k = \pm \hbar v_F \sqrt{k_x{}^2 + k_y{}^2} \qquad (1.1)$$

where E is the energy, k is the wave vector and v_F is the Fermi velocity. The velocity, v(k), of an electron in graphene is given by the slope of the E(k) curve: v(k)=$1/\hbar dE/dK = v_F$; which has a constant value of $v_F = 1 \times 10^6$ m/s. Graphene is thus a zero band gap semiconductor with a linear, rather than quadratic (as in case of silicon), energy dispersion relationship for both electrons and holes in conduction and valence band, respectively. Further, the position of the Fermi level, E_F, determines the nature of the doping and the transport carrier. For undoped

graphene, E_F lies at the intersection of two cones at $E_F = 0$ (Dirac point); and for n-doped (p-doped) graphene, E_F lies in the upper (lower) cone (Fig. 1.2c).

1.4.2 Density of States

Before we can calculate the carrier density in graphene, we have to know its density of states (DOS), D(E), which tells us the number of states per interval of energy at each energy that are available to be occupied and it depends on the E(k) relationship. The standard procedure for calculating DOS is to consider a constant energy surface of the E(k) diagram, which is the $k_X - k_Y$ plane as shown in Fig. 1.3a. Then, we need to calculate the number of states, N(k), encompassed in the shaded ring (between k and k + dk), which can be written as

$$N(k)dk = \frac{2\pi k dk}{(2\pi/L_x)(2\pi/L_y)} \times g_s \times g_v. \tag{1.2}$$

The numerator of the first part of right-hand side is the area of the shaded ring (Fig. 1.3a). The denominator is the space each state takes up in the k_X - k_Y plane; which is computed by assuming a rectangular box of size L_x, L_y with periodic boundary conditions such that each states takes up the space of $2\pi/L_x$ and $2\pi/L_y$ [56]. The second part of the right-hand is the spin degeneracy, g_s, which is g_s =2 for graphene. The third part is the valley degeneracy, g_v, which is g_v = 2 for graphene. Using the dispersion relation Eq. 1.1, we can convert N(k) into N(E), which tells us the total number of states having an energy less than E. The derivative of this function gives us the DOS, which is normalized to area ($L_x \times L_y$) and energy:

$$D(E) = \frac{2|E|}{\pi(\hbar v_F)^2}. \tag{1.3}$$

Thus, the DOS, as plotted in Fig. 1.3b, increases linearly with energy above and below the Dirac point.

1.4.3 Carrier Density

At this point, we have just calculated the DOS for graphene. In either case, whether for the electron or the hole, the above DOS expression simply tell us the density of available states. They say nothing about whether or not such states are occupied. For this, we need the probability function f(E) — known as the Fermi-Dirac distribution function — which tells us whether an electron or hole is occupied in a given state with an energy E. The Fermi-Dirac distribution function can be written as

$$f(E_F) = \frac{1}{1 + e^{(E-E_F)/k_B T}} \tag{1.4}$$

where k_B is the Boltzmann's constant and T is the temperature in Kelvin. Through this, we can determine the net carrier density, $n = n_e - n_h$, where n_e stands for filled states for E > 0, and n_h stands for empty states with E < 0. The net carrier density n at Fermi energy E_F, for
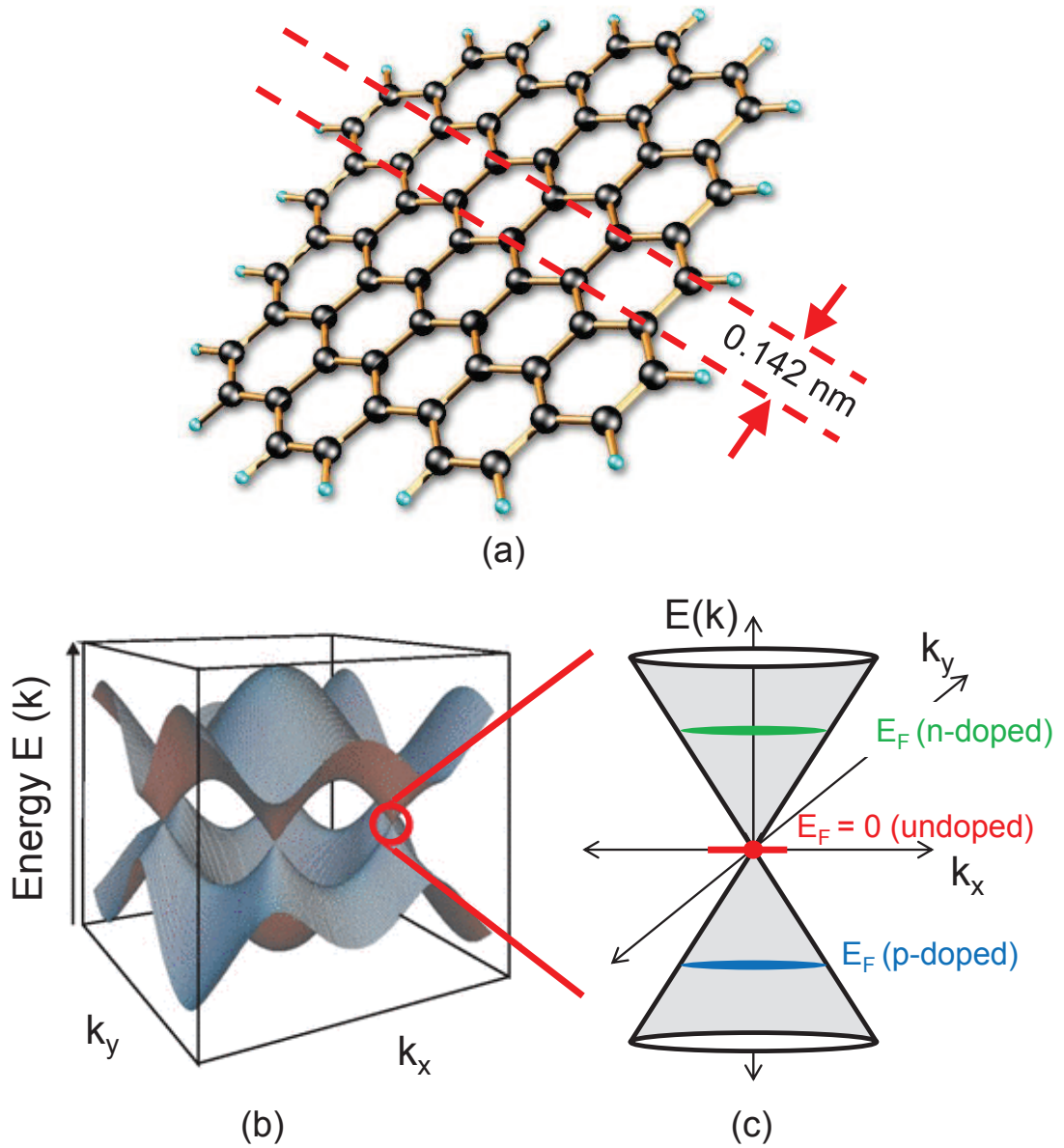
Figure 1.2: (a) Hexagonal honeycomb lattice of graphene. (b) Graphene band structure. Adapted from [55]. (c) Simplified graphene band structure at low energies.
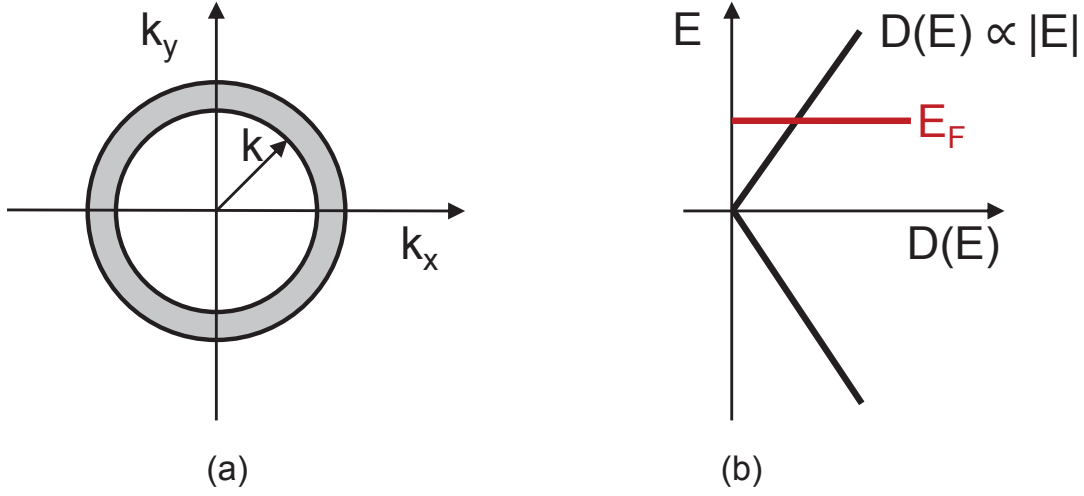
Figure 1.3: (a) Constant-energy described by k_x and k_y for electrons in 2-dimension, and (b) Density of states (DOS) as a function of energy (E).

non-zero T, can then be calculated as

$$n = \int_0^\infty D(E)f(E_F)dE - \int_{-\infty}^0 D(E)(1-f(E_F))dE. \tag{1.5}$$

This equation can be simplified for zero kelvin temperature (T = 0 K) and can be written as (details of the derivation can be found in ref [57, 58]):

$$n(E_F) = sign(E_F)\frac{E_F^2}{\pi(\hbar v_F)^2}. \tag{1.6}$$

Interestingly, graphene behaves like a strong degenerate semiconductor under most conditions. A typical trait of degenerate semiconductors is that its carrier density does not change with temperature. Therefore, the approximation at T = 0 K (Eq. 1.6) works fairly well for T = 300 K [57].

1.5 Thesis Outline

This thesis investigates two main approaches for alternative device concepts for graphene's application: Nanoelectromechanical RF switches based on suspended graphene (Chapter 2); and negative differential resistance devices based on non-suspended graphene (Chapters 3, 4 and 5).

Chapter 2 discusses graphene based RF nanoelectromechanical shunt switches. The chapter starts by introducing the operation principle of RF NEMS switches and the main motivation behind using graphene in these switches. The RF performance of graphene NEMS shunt switch is evaluated via detailed modeling, design and simulation. Various mechanisms which

limit the performance of graphene NEMS switches are also discussed. At the end of this chapter, the preliminary measurements results of the fabricated devices are also presented and analysed.

In **Chapter 3**, graphene solid-state devices, which are not suspended, are presented. This chapter talks about two main topics: device physics and technology of graphene transistors. This serves as the solid basis for next two chapters. In the device physics part, the drift-diffusion model of graphene transistors and the approach for graphene circuit-simulation is presented. In the technology part, first, the common approaches for synthesizing monolayer graphene is reviewed, and particularly the large-scale CVD method, which is used to fabricate devices in this work, is described. Then, various techniques used to fabricate graphene transistors in this PhD work are described, and finally, its low-field DC measurements are presented.

Chapter 4 discusses the negative differential resistance (NDR) phenomenon in graphene solid-state devices which include single GFET [1], and circuit based on three GFETs [2]. First, the NDR phenomenon in fabricated single graphene transistor is discussed. A mechanism to understand the NDR phenomenon in graphene transistors is also presented via modeling. This understanding enables us to design circuit based on graphene which show enhanced NDR performances. Thus, the other half of the chapter is dedicated to this novel circuit consisting of three graphene transistors.

Chapter 5 presents the application of NDR devices in RF reflection amplifiers. The performance potential of both 1-GFET and 3-GFET circuit as reflection amplifiers is evaluated via DC and RF modeling. Also, an experimental evidence of reflection amplification in 3-GFET circuit by measuring it in 1-port configuration is presented.

Chapter 6 provides the overall summary of this work. Several original contributions are highlighted and suggestions for the future research directions are offered.

---

[1]In this thesis, the terms "1-GFET", "single-GFET", and "1-transistor graphene FET" are used interchangeably. Each refer to single GFET.

[2]The terms "3-GFET NDR circuit", "three-GFET NDR circuit", "3-transistor graphene circuit" and "GNDR circuit" are also used interchangeably. Each refer to the circuit comprising of three GFETs exhibiting NDR.

2 Graphene Nanoelectromechanical Microwave Shunt Switch

In this chapter we discuss graphene-based RF NEMS shunt switches. In Section 2.1, we introduce the basic operation principle of RF MEMS/NEMS switches and discuss the main motivation behind using graphene in these switches. In Section 2.2, we outline the specific properties of graphene relevant for RF MEMS/NEMS. To access the RF performance of graphene NEMS shunt switches, it is important to accurately design and model them. Thus, the next two sections (Section 2.3, 2.4) are dedicated to modeling, design and simulation. An attempt is also made to characterize the fabricated NEMS shunt devices based on multilayer graphene; thus, in Section 2.6 we present in detail the fabrication and characterization of this switch. Finally, Section 2.7 summarizes this chapter.

2.1   Introduction

A radio frequency (RF) microelectromechanical systems (MEMS) switches are micromachined devices which use a mechanical movement to achieve switching between on- and off-states. The forces required for a mechanical movement can be obtained using electrostatic [59], electrothermal [60], magnetostatic [61], and electromagnetic designs [62]. Particularly, electrostatic force is widely used as it provides almost zero power consumption and has the highest compatibility with standard CMOS process. Compared with conventional semiconductor devices, MEMS switches offer great advantages such as zero leakage, higher isolation, zero insertion losses, and robustness under harsh environments, which makes them suitable candidate for a variety of applications from mobile communication to advanced radar systems.

There are two main types of RF MEMS/NEMS switches: the series metal-metal switches [63] and shunt capacitive switches [64]. In this work, we focus on shunt capacitive switches. The shunt capacitive switches are very suitable for high-frequency (>10 GHz) applications because of its capacitive coupling nature. The capacitive coupling nature avoids the use of metal-metal contact (as in the case of series switches) which gives rise to large contact resistance, thereby impeding the high frequency operation due to high losses [65]. Fig. 2.1 shows the schematic of RF shunt capacitive switch. The switch consists of a conductive membrane suspended over

the central conductor of a coplanar waveguide (CPW) and fixed to the ground conductor of the CPW. The central and ground conductors are high-conductivity metals (such as gold) on the low loss substrate (such as high resistivity silicon). A dielectric layer is used to dc isolate the switch from the CPW center conductor.

The operation principle of the shunt switch can be understood by its equivalent circuit model as shown in Fig. 2.1c,d. It can be modeled by two short sections of transmission line in series and a lumped CLR components in the shunt branch. The impedance in the shunt branch can be written as

$$Z_P = R_P + j\omega L_P + \frac{1}{j\omega C_P} \tag{2.1}$$

where ω is the angular frequency, R_P and L_P are respectively the resistance and inductance of the membrane, and C_P is the capacitance which is dominated by a low air-gap capacitance in the up-state and a high dielectric capacitance in the down-state position. When the membrane is in up-state position, the shunt impedance is high due to low value of up-state capacitance. As a result, the electromagnetic field propagates almost unattenuated from port 1 to port 2, leading to a full transmission ($| S_{21} |^2 \approx 1$). This represents the ON-state of the switch. When a dc voltage is applied across the membrane and the central conductor with the RF signal, the electrostatic force causes the membrane to snap down on the dielectric surface, forming a low-impedance mainly capacitive RF path to the ground. Hence, the field is strongly suppressed, leading to blocked transmission (($| S_{21} |^2 \approx 0$)). This represents the OFF-state of the switch.

In state-of-the-art RF MEMS shunt switches, metallic membranes are employed which are several micrometers thick. These MEMS switches suffer from a trade-off between high frequency performance and actuation voltage. Typical MEMS actuation voltage (>10 V) are higher than the operational voltages of current integrated circuits (ICs) technology. Therefore, as the available voltage supply for various ICs technology based applications are limited, the actuation voltage of the RF MEMS switches must be reduced.

With regards to the electrostatic actuation, the pull-in voltage of RF MEMS shunt switch is given as [64]

$$V_{pull-in} = \sqrt{\frac{8k}{27\epsilon_0 W w} g_0^3}, \tag{2.2}$$

where k is the effective spring constant of the membrane, W is the CPW center conductor width, w is the membrane's width and g_0 is the height of the suspended membrane above the dielectric layer (Fig. 2.1a). According to continuum mechanics, the effective spring constant of the doubly clamped membrane with load applied at the center of the membrane and under axial tension, is given by [51, 66]

$$k = 32Ew(t/L)^3 + 17T/L, \tag{2.3}$$

Figure 2.1: Schematic of RF capacitive shunt Switch in up-state (a) and down-state (b) and its corresponding equivalent circuit models (c,d).

where E is Young's modulus, T is the tension in the beam and t and L are the thickness and length of the membrane, respectively. Reducing k via reduction in the thickness of the membrane t (Eq. 2.3), will allow us to reduce the pull-in voltage (Eq. 2.2). Using graphene, as the material for membranes in RF MEMS switches, can be of great benefit here as one can exploit its ultra low thinness to reduce the pull-in voltage.

Furthermore, graphene-based MEMS also have an edge over carbon nanotube-based MEMS [67, 68] in terms of the ease of fabrication and higher compatibility with the device geometry. Moreover, graphene-based RF MEMS switches, which are suitable for monolithic integration with graphene RF nanoelectronics, are extremely promising as components for future all-graphene transceivers [69]. In literature, the terminology NEMS (nanoelectromechanical) instead of MEMS is generally associated with graphene mechanical devices. The field of NEMS seeks to explore the behaviour and potential of mechanical devices whose dimensions are deep into the sub-micrometer regime [70].

2.2 Graphene as a membrane of the RF NEMS shunt switch

The main motivation behind using graphene as a membrane of the switch is to lower down the actuation voltages as discussed in the previous section. However, there are some more fundamental requirements which the material of membrane must fulfil. Let us closely examine Eq. 2.1, which is the most important equation for the understanding of RF shunt switches. For

Table 2.1: Specifications for the state of the art materials for the membrane of the RF MEMS shunt switch.

Membrane	Conductivity	Resistivity	Young's Modulus	Coefficient of thermal expansion
Al	36.9×10^6 S/m	$2.7 \times 10^{-8}\Omega$m	69 GPa	23.1 ppm/°C
Au	44.2×10^6 S/m	$2.3 \times 10^{-8}\Omega$m	83 GPa	14.2 ppm/°C
Ni	14.3×10^6 S/m	$7 \times 10^{-8}\Omega$m	207 GPa	13.4 ppm/°C
Mo	20×10^6 S/m	$5 \times 10^{-8}\Omega$m	329 GPa	4.8 ppm/°C

a good RF MEMS shunt switch, Z_P should be high in the up-state and low in the down-state. If R_P is high, Z_P will be high both in up- and down-states, as this value is usually constant in both positions. As Z_P is mainly dominated by C_P in the up-state, the component R_P has negligible effect. In the down-state position, a high value of R_P has the following detrimental effects: (1) It increases Z_P in the down-state, leading to the poor isolation; and (2) it increases the losses of the switch which is proportional to the R_P value of the membrane, as discussed later. Therefore, for a good RF MEMS/NEMS shunt switch, it is crucial to have R_P as low as possible or in other words, the conductivity of the membrane should be as high as possible.

Beyond the requirements of high conductivity, the ideal suspended membrane of RF MEMS/NEMS switch should have the following features: (1) High Young's modulus for good mechanical properties; this translates into reduced switching time for the switch [59]. (2) High thermal conductivity for the good reliability of the switch. 3) Low thermal expansion coefficient (close to underlying substrate); this is to reduce the rate of change in actuation voltage over temperature. 3) Ease of fabrication and compatibility with Si CMOS process. Almost all state of the art RF MEMS switches are fabricated out of metals such as aluminium (*Al*), gold (*Au*) which have high bulk conductivities (Table. 2.1). But metals generally have a thermal expansion coefficient which is usually much higher than that of commonly available substrate materials; thus they have poor performance over broad temperature ranges. Refractory metals — such as molybdenum — have low thermal expansion coefficient and have also been utilized as the membrane for RF MEMS switches [71]. These materials show a stable operation over broad temperature range, however, they have low bulk conductivities leading to high RF losses and poor isolation. Unfortunately, material satisfying all the requirements for an ideal RF MEMS/NEMS switch does not exist, and device engineers must always live with trade-off. How does graphene meet these requirements?

The properties which make graphene an attractive candidate for the membrane of RF NEMS switches are as follows:

1. Monolayer graphene (single layer of carbon atom) and multilayer graphene (few layers of carbon atom) are expected to give low values of actuation voltages because of their atomic thickness's, as discussed in Section 2.1.

Table 2.2: Sheet resistivity of graphene.

Reference	Sheet resistivity	Doping	Layers
[75]	54 $\Omega/\square$	Aucl$_3$-doping layer by layer	4
[76]	99 $\Omega/\square$	HNO$_3$ layer by layer	8
[80, 79, 81]	280 $\Omega/\square$	No doping	Graphene films
[74]	30 $\Omega/\square$	HNO$_3$	4

2. Suspended membrane of the NEMS switch needs to offer faster switching speed. Graphene's high Young's modulus and extremely low mass could enable ultra-fast switching speeds in NEMS switches [28]. The Young's modulus of graphene have been investigated in many works; the reported values varied in the range 250–1500 GPa. Sanchez *et al.* [72] reported a Young's modulus of 1.5 GPa for multilayer graphene sheets suspended over trenches in silicon oxide.

3. Thermal conductivity of the suspended membrane determines the reliability of the NEMS switch. Joule heating between the contacts in NEM switches often lead to the damage of the contact area; this can be reduced by using a material of high thermal conductivity. Carbon materials such as graphite, diamond, CNTs are known to have a high thermal conductivity. Bulk graphite has a basal thermal conductivity as high as 1000 W/mK, providing a foundation for the high thermal conductivity of graphene sheet. A high thermal conductivity of 5300 W/mK in a suspended single-layer graphene measured at room temperature was reported in [6].

4. One serious drawback of graphene has been its higher sheet resistivity. To reduce the sheet resistivity, several methods are employed. The methods include: i) using more number of layers of graphene, i.e. multilayer graphene [73]; ii) chemical doping of graphene [74]; and iii) combination of methods (i) and (ii) [75, 76]. Table. 2.2 lists the lowest sheet resistivity obtained with these methods.

5. One of major disadvantages of carbon nanotube (CNT) based NEMS process has been the unconventional method used for CNT growth [67, 77, 68]. This method involves a high temperature growth of nanotubes followed by the horizontal alignment of nanotubes by liquid-induced flip down method. In addition, this method requires an extra mask step to define the catalyst for nanotube growth. The CVD growth of graphene is also a high temperature process, but thanks to the PMMA transfer method [78] which permits the growth to be done off the wafer. The other advantages of using graphene is the possibility to obtain larger areas of graphene by CVD methods [79]. Graphene can be patterned using standard photolithographic techniques and oxygen plasma etch; and thus allows the membrane to be etched in desired widths and lengths.
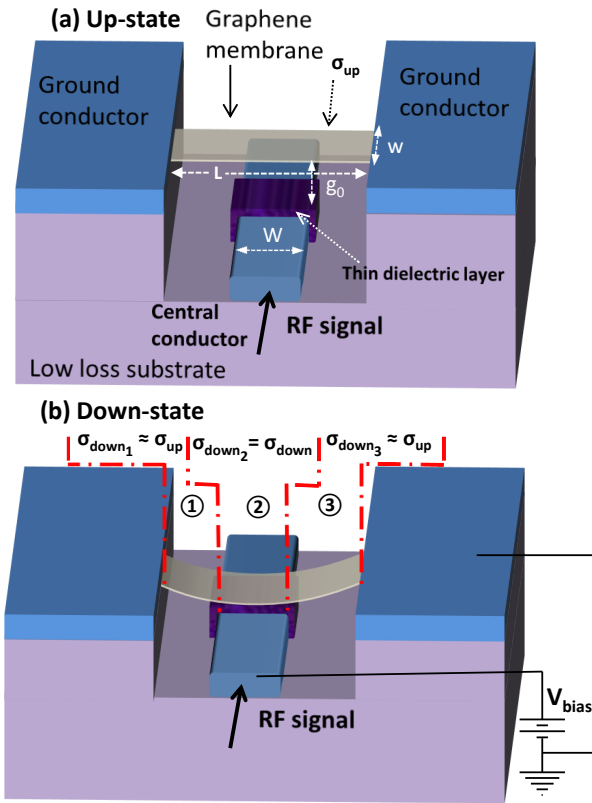
Figure 2.2: Schematic of graphene based RF NEMS switch in (a) up- and (b) down-state.

2.3   Design of Graphene based capacitive shunt switch

The use of graphene as a suspended membrane of RF NEMS shunt switch was also proposed in ref [82] but no details about fundamental issues such as the value of graphene conductivity used for the electromagnetic simulation or the equivalent circuit parameters of the shunt switch, were provided. Herein, we will evaluate the RF performance of graphene NEMS switch via a detailed design and modeling. Both monolayer and multilayer graphene are considered for the design. Unlike metal membrane switches where the conductivity of the membrane remains the same both in up- and down-states. The case of graphene is different. The fact that graphene's conductivity can be tuned via electric field effect [83], we need to consider its conductivity variation in up- and down-states. We will show that graphene's conductivity variation due to electric field effect has a limited yet beneficial impact on the performance of the switch.

2.3.1   Working Principle

Fig. 2.2 schematically shows the proposed graphene-based RF NEMS device. The switch consists of a graphene membrane having a conductivity (σ_{up}) suspended over the central

Figure 2.3: Equivalent circuit model of Graphene-based NEMS capacitive switch.

conductor of a coplanar waveguide (CPW) and fixed to the ground conductor of the CPW. The central and ground conductors are high-conductivity metals (such as gold) on the low loss substrate (such as high resistivity silicon). A dielectric layer is used to dc isolate the switch from the CPW center conductor. When a dc voltage is applied across the membrane and the central conductor with the RF signal, the electrostatic force causes the membrane to snap down on the dielectric surface, forming a low-impedance mainly capacitive RF path to the ground. In this situation, a part of the graphene membrane directly above the dielectric layer (Region 2 in Fig. 2.2b) experiences a perpendicular electric field from the bottom electrode. Since the conductivity of atomically-thin carbon films such as graphene [83] can be tuned by applying a transverse electric field via a gated structure, the conductivity of graphene membrane in Region 2 (σ_{down}) will be higher than the initial conductivity (σ_{up}). The membrane in regions 1 and 3 does not experience any field effect and therefore the conductivities in these regions can be approximated to have the same value as in up-state (σ_{up}).

2.3.2 Equivalent Circuit Model

Fig. 2.3 shows the equivalent circuit model of the graphene RF NEMS shunt switch. In the circuit model of metal membrane MEMS, the capacitance (C_P) is the only variable component. However in the present case, R_P is also a variable component due to the variable resistivity behaviour of the graphene membrane in up- and down-state positions. $\triangle L_S$ and $\triangle R_S$ are corrective series elements in order to keep the length of the discontinuity to zero in the modeling. This choice of zero-length (d_{ref} =0) for the extraction procedure is arbitrary but fully rigorous, namely just a choice of reference planes [84, 85].

In regard to the mechanical actuation of the switch, the pull-in voltage $V_{pull-in}$ (Eq. 2.2) is already discussed in Section 2.1. Another important mechanical figure of merit for the RF

NEMS switch is switching time which can be approximated as [59, 39]

$$t_s = 3.67 \frac{V_{pull-in}}{V_S \omega_0},$$
(2.4)

where $V_S \approx 1.3 V_{pullin}$ is the optimum applied bias at which the switching time is usually calculated [39], and ω_0 is the angular resonant frequency which can be calculated as $\omega_0 = \sqrt{\frac{k}{m_{eff}}}$ ($m_{eff} = 0.735 L w t \rho$ [28], where ρ is the mass density).

2.4 Modeling

2.4.1 Frequency Dependent Conductivity

The complex conductivity of graphene can be computed using Kubo's formula [86]. This formula takes into account graphene intraband and interband contributions. However, since the operation of the device is far below the THz regime, the interband contributions are negligible and graphene conductivity can be represented as [87]

$$\sigma(\omega, E_F, \Gamma, T) \approx -j \frac{q_e^2 k_B T}{\pi \hbar^2 (\omega - j\Gamma)} \left(\frac{|E_F|}{k_B T} + 2\ln(e^{-|E_F|/(k_B T)} + 1) \right),$$
(2.5)

where Γ is the phenomenological scattering rate (inverse of the relaxation time τ, $\Gamma = \tau^{-1}$), $T = 300$ K is the temperature, $\hbar$ is the reduced Planck's constant, k_B is Boltzmann's constant and E_F is the chemical potential (or Fermi energy). In order to compute the conductivity of graphene membrane in up- and down-state position, it is essential to determine the parameters Γ and E_F as they can take different values in these two positions.

2.4.2 Conductivities in Up- and Down-state positions

Recalling from Eq. 1.6, the relation between the chemical potential E_F and the hole (electron) carrier density n_h (n_e) of monolayer graphene can be written as

$$n_e - n_h = sign(E_F) \frac{1}{\pi} \left(\frac{|E_F|}{\hbar v_F} \right)^2,$$
(2.6)

While for multilayer graphene, the relationship is given by [88]

$$n_e - n_h = \frac{2m^* E_F}{\pi \hbar^2},$$
(2.7)

where m^* is the effective mass of multilayer graphene. $m^* \approx 0.052 m_e$ (for 3,4 layers) [89], m_e being the effective mass of the electron.

Let us now consider the up-state position of the switch, where graphene membrane has an initial hole (electron) carrier density n_{hup} (n_{eup}). In this case, the chemical potential,

$E_{Fup_{Mono}}$ in the up-state position for monolayer graphene (from Eq. 2.6) can be written as

$$E_{Fup_{Mono}} = sign(n_{eup} - n_{hup})\hbar v_F \sqrt{|n_{eup} - n_{hup}|\pi}. \tag{2.8}$$

Similarly, the chemical potential $E_{Fup_{Multi}}$ in the up-state position for the multilayer graphene (from Eq. 2.7) can be expressed as

$$E_{Fup_{Multi}} = \frac{\pi\hbar^2}{2m^*}(n_{eup} - n_{hup}). \tag{2.9}$$

We now consider the down-state position of the switch, which is achieved by applying a dc voltage V_{bias} between the central conductor and ground. The resulting electrostatic forces pull the membrane towards the center conductor, and the voltage at which electrostatic forces overwhelm the restoring force is known as the pull-in voltage $V_{pull-in}$. At this voltage or greater ($|V_{bias}| \geq |V_{pull-in}|$), the membrane is in direct contact with the bottom dielectric layer. In this position, a part of the membrane in region 2 (Fig. 2.2b) experiences the field effect from the central conductor. To compute the carrier density in this region, the charge balance relationship [88] is employed, which is given as

$$V_{bias} - V_{Dirac} = \frac{q(n_{edown} - n_{hdown})}{C_{ox}}, \tag{2.10}$$

where q is the elementary charge, n_{hdown} (n_{edown}) is hole (electron) carrier density in the down-state position, C_{ox} is the capacitance of the dielectric between the central conductor and the membrane in down-state position, which is given by $C_{ox} = \frac{\epsilon_r \epsilon_0}{t_d}$, where ϵ_r is the relative permittivity of the dielectric, ϵ_0 is vacuum permittivity and t_d is the thickness of the dielectric, and V_{Dirac} is the bias voltage at the Dirac point. It has a non-zero value for the pre-doped graphene and its magnitude also depends upon the dielectric constant and thickness of the supporting substrate. For the initial hole (electron) carrier density of n_{hup} (n_{eup}), the V_{Dirac} can be calculated as [90] $V_{Dirac} = -q(n_{eup} - n_{hup}))/C_{ox}$. Thus from Eq. 2.10, the down-state carrier density can be expressed as

$$n_{edown} - n_{hdown} = \frac{C_{ox}}{q}V_{bias} + n_{eup} - n_{hup}. \tag{2.11}$$

As a result, the chemical potential in the down-state for monolayer graphene, $E_{FdnMono}$ (Eq. 2.12), and for multilayer graphene, $E_{FdnMulti}$ (Eq. 2.13), can be expressed as:

$$E_{FdownMono} = sign(\frac{C_{ox}}{q}V_{bias} + n_{eup} - n_{hup})\hbar v_F$$
$$\times \sqrt{|\frac{C_{ox}}{q}V_{bias} + n_{eup} - n_{hup}|\pi}, \tag{2.12}$$

$$E_{FdownMulti} = \frac{\pi \hbar^2}{2m^*}(\frac{C_{ox}}{q}V_{bias} + n_{eup} - n_{hup}). \tag{2.13}$$

Note that we have ignored the effect of quantum capacitance [91] in our model because its impact is negligible for the values of V_{bias} and the thickness of dielectric applicable for RF NEMS switches [85].

In addition to chemical potential, the scattering rate Γ may also take a different value in the down-state position of the switch due to the remote polar phonon scattering from the bottom dielectric. However, for the highly doped graphene sample, the contribution due to remote polar phonon scattering rate is usually small [88] and can be ignored [92].

2.5   Simulation, Results and Discussion

The lateral dimensions of the graphene RF NEMS switch considered for the simulation are shown in Fig. 2.4. The suspended graphene membrane is L = 20 μm long and w = 30 μm wide, and is suspended at a height g_0 = 300 nm. These dimensions are chosen to be the same as the experimentally implemented DC NEMS switch by Kim et al [39], where no attempt was made to investigate the microwave properties in a CPW configuration. Furthermore, a wide central conductor width (W = 15 μm) below the membrane is used. This is to achieve a maximum field effect of the membrane in the down state. The substrate is high resistivity silicon (10 kΩ-cm), and the ground and central conductor are treated as perfect conductors for the full-wave simulation (as losses in the metals are negligible with respect to graphene membrane).

A thin dielectric layer (t_d = 20 nm) over the central conductor is considered to achieve a high capacitance ratio of the switch. A high-κ dielectric HfO$_2$ is chosen as a material for the dielectric layer for two main reasons. First, high-κ dielectrics — such as HfO$_2$ — are known to reduce the impurity scattering [93, 94] in graphene. Second, its higher dielectric constant (ϵ_r = 25) and a low loss tangent (tanδ=0.0098) [95], lead to a better switch performance at high frequency. Furthermore, it is noted that the maximum V_{bias} which can be applied without causing dielectric breakdown of HfO$_2$ is 0.85 V/nm $\times$ t$_d$ [96]. In this case, for t$_d$ = 20 nm,
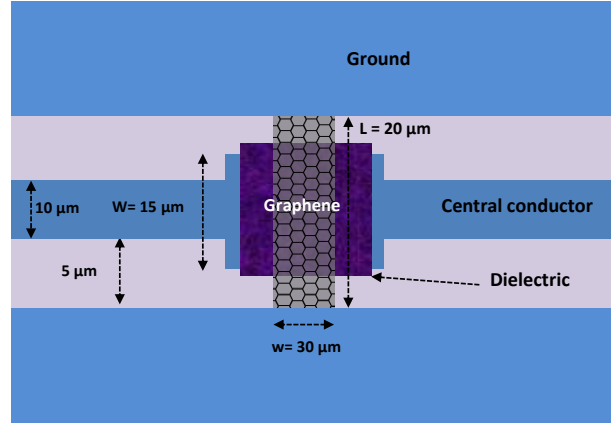
Figure 2.4: Top view with specifications of lateral dimensions used for the simulation.

the maximum V_{bias} which can be applied is 17 V; this is much larger than the maximum voltage needed for actuation as shown later. The full-wave simulation of graphene-based RF NEMS switch is performed using Ansys HFSS. In the full-wave simulation, the graphene membrane is modeled as an infinitesimally thin sheet characterized by frequency ω and bias V_{bias} dependent surface conductivity according to Eq. 2.5. In the up-state, a conductivity $\sigma_{up}(\omega, V_{bias})$ is assigned to the whole membrane. In the down-state, a membrane is divided into three regions, as shown in Fig. 2.2b. In regions 1 and 3, $\sigma_{up}(\omega, V_{bias})$ is assigned and in region 2, $\sigma_{down}(\omega, V_{bias})$. The proposed model is used to compute σ_{up} and σ_{down}. Using the sheet resistivity and carrier density data provided in ref [74], we extract the rest of the parameters based on our model required to compute the conductivities. It is noted that the model presented in Section 2.4 is generalized; that is, it can be applied to any sheet resistivity value of monolayer and multilayer graphene, and is not limited to the example shown in this paper. Table. 2.3 summarizes the extracted model parameters used for the simulation. Low pull-in voltages < 2 V based on the analytical expressions, are closer to the experimentally demonstrated values [39]. Switching time of 0.24-0.43 μs have been obtained which is an order of magnitude below the typical values (2-50 μs) for state of the art MEMS switches [59]. It should be noted that we have not considered the effect of contact resistance which exists between graphene and ground conductor in our simulation as its effect is almost negligible at higher frequencies [85].

An example of typical frequency-dependent surface impedance ($= 1/\sigma$) of graphene based on Eq. 2.5 is shown in Fig. 2.5 both for monolayer and multilayer graphene. At a given frequency, the application of V_{bias} allows to increase E_F, thus reducing the surface resistance. Note that at $V_{bias} = +V_{pull-in}$, the surface resistance is higher (conductivity is lower) than that at $-V_{pull-in}$ because the considered sample is initially p-doped. From the RF point of view, having a higher conductivity for a given bias voltage in the down-state is beneficial as this translates to a higher isolation. From the electrostatic actuation point of view, the polarity of bias applied does not matter, i.e., applying either positive or negative $V_{pull-in}$ will both

Table 2.3: Extracted parameters from the model.

	Monolayer	Multilayer	
$1/\sigma_{up}$ ($\Omega/\square$)	125	30	[74]
Doping	p-doped	p-doped	[74]
Layers	1	4	[74]
n_{hup} (cm^{-2})	9.43×10^{12}	4×10^{13}	[74]
n_{eup} (cm^{-2})	0	0	[74]
τ (ps)	0.186	0.309	[74]
E_{Fup} (eV)	0.365	0.92	Eq. 2.8,2.9
$|V_{pull-in}|$ (V)	0.3	1.4	Eq. 2.2 (monolayer: [E = 0.8 TPa, t ∼ 0.34 nm, T = 13 nN] [28]; multilayer: [E = 0.8 TPa, t ∼ 2 nm, T = 300nN] [66])
t_s (μs)	0.43	0.24	Eq. 2.4 (ρ = 2200 kgm^{-3} [28])
E_{Fdown} (eV)	0.451	0.344	Eq. 2.12, 2.13
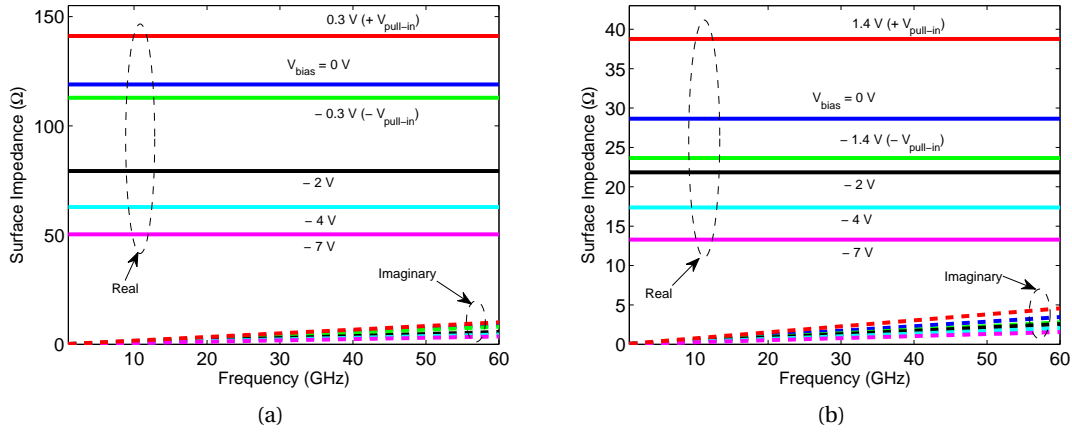
Figure 2.5: Surface impedance vs frequency of (a) monolayer graphene and (b) multilayer graphene using the parameters in Table 2.3. The case $V_{bias} = 0$ and $V_{bias} \neq 0$ corresponds to the up-state surface impedance ($1/\sigma_{up}$) and down-state surface impedances ($1/\sigma_{down}$) respectively.

actuate the switch. Therefore, given the choice of sign of the bias voltage, if the sample is initially p-doped (n-doped), it will be beneficial to apply a negative (or positive) pull-in voltage for a better RF performance [85].

There is also a weak inductive reactance contribution to the surface impedance which was also observed in experiments conducted for sheet characterization of graphene at the microwaves and mm-wave [97, 54].

The scattering parameters (S-parameters) of the switch are then computed in the frequency range from 1 GHz to 60 GHz. Fig. 2.6a shows the S-parameters in the up-state position of the switch. The insertion loss is 0.01-0.3 dB and 0.01-0.2 dB for monolayer and multilayer graphene respectively. The S-parameters in the down-state position are shown in Figs. 2.6b and 2.6c. The isolation of >10 dB for monolayer and >20 dB for multilayer graphene is
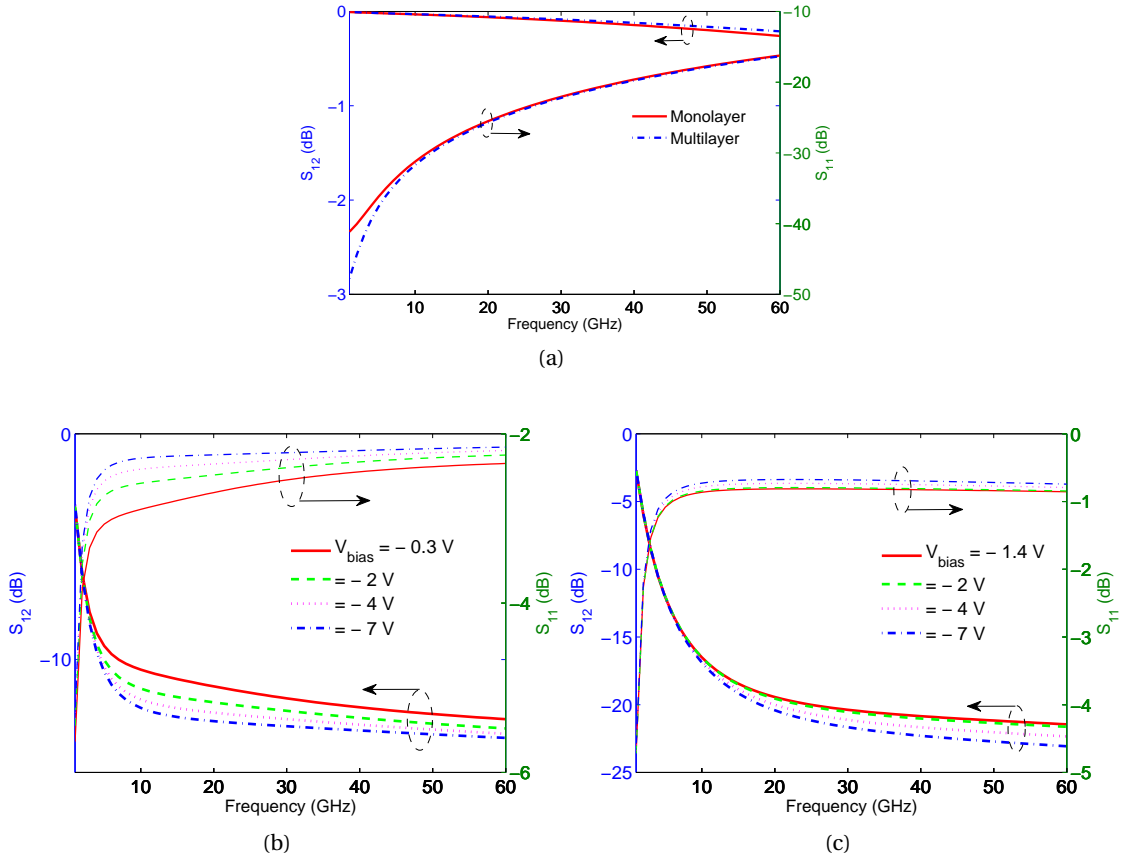
Figure 2.6: S-parameters of RF-NEMS switch shown in Fig. 2.4 in (a) up-state both for mono-layer and multilayer graphene, (b) down-state for monolayer graphene, and (c) down-state for multilayer graphene.

obtained. The multilayer graphene switch offers a superior isolation as compared to the monolayer because of the lower surface resistance of the multilayer graphene. The isolation can further be improved by increasing the bias voltage (V_{bias}). This is due to the reduced resistance of the membrane with increasing V_{bias}.

It is noted that, in the down-state, changing V_{bias} should have a negligible impact on the shunt capacitance. Strictly speaking, the total down-state capacitance is the parallel combination of quantum capacitance C_Q and the dielectric capacitance C_{OX}. C_Q is proportional to the carrier density in graphene [91], which can be tuned by V_{bias} in the down-state. Therefore, the total capacitance, $C_Q \parallel C_{OX}$, will be the function of V_{bias}; that is, the total capacitance will be affected after $|V_{bias}| \geq |V_{pull-in}|$ through the quantum capacitance. The contribution of C_Q, however, is dominant only when: (1) the dielectric is very thin; and (2) when the graphene considered has a very low carrier density. For graphene NEMS switches, a highly conductive graphene is desirable which usually has a high carrier density (through chemical doping), thereby leading to high C_Q. A high value of C_Q, in a parallel combination with C_{OX}, makes its contribution to the total capacitance insignificant ($C_Q \parallel C_{OX} \approx C_{OX}$). Therefore, changing

(a)
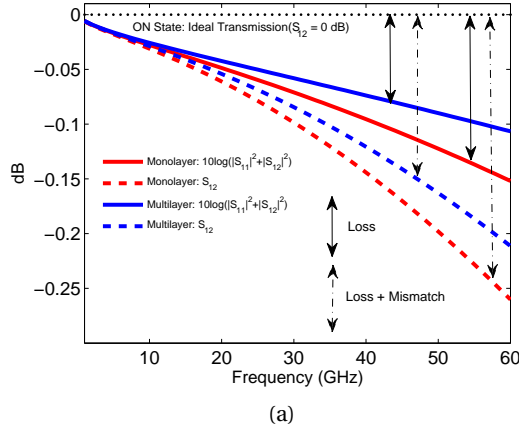
Figure 2.7: Comparison of loss vs S-parameters in the Up-state position. The reference planes are 20 μm from the edge of NEMS switch (width of membrane = 30 μm).

Table 2.4: T-Model Circuit parameter extraction from simulated S-parameters.

Parameter@ 1-60GHz			Parallel Z_P		Series Z_S	
		V_{bias} (V)	C_P (fF)	R_P (Ω)	$\triangle L_S$ (pH)	$\triangle R_S$ (Ω)
Up	Monolayer	0	16.38	19.8	-1.08	0.08
	Multilayer	0	16.05	7.11	-1.035	0.09
Down	Monolayer	-0.3	4410	8.57	-1.09	0.1
		-2	4530	7.77	-1	0.09
		-4	4510	7.51	-1.1	0.1
		-7	4570	7.06	-1.02	0.09
	Multilayer	-1.4	4630	2.16	-1	0.15
		-2	4530	2.17	-1.16	0.16
		-4	4590	1.95	-1.03	0.16
		-7	4620	1.76	-1.01	0.16

V_{bias} will have a negligible impact on the shunt capacitance of this device [85].

The lower insertion loss and isolation obtained for monolayer graphene as compared to multilayer, and the subsequent improvement in isolation with increasing V_{bias}, can be better understood by observing the contribution of thermal losses to the S-parameters. By energy conservation, the loss of a two-port network is simply derived from the S-parameters as $loss = 1 - |S_{11}|^2 - |S_{12}|^2$. The up-state position corresponds to the on-state of the switch, where $S_{12} = 0$ dB would be obtained for an ideal switch. As can be seen from Fig. 2.7a the decrease in S_{12} is not solely due to the increase in the reflected power because of mismatch, but is also due to thermal loss in the switch. By comparing the different curves, it is easily seen that the better performance of the multilayer implementation is related to reduced losses rather than smaller mismatch. The similar argument applies for the superior performance of multilayer graphene in down-state position because of its reduces losses.
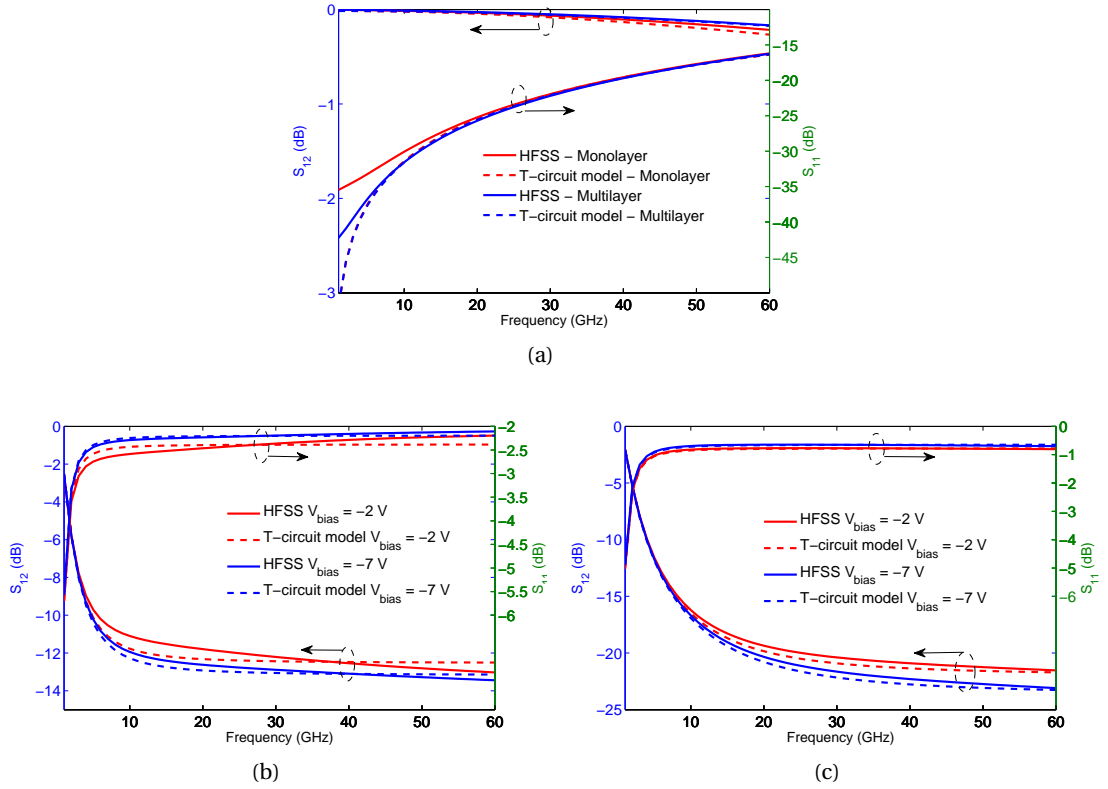
Figure 2.8: Comparison of S-parameters reconstructed from the T-circuit Model and simulated from HFSS in (a) up-state for both monolayer and multilayer graphene (b) down-state for monolayer graphene (c) down-state for multilayer graphene. For the sake of clarity in graph, down-state S-parameters are shown only for two bias voltages, $V_{bias} = -2$ V and $V_{bias} = -7$ V.

Finally, the equivalent circuit parameters are extracted (Table. 2.4) from the S-parameters based on the T-circuit model shown in 2.3. We observe that the shunt impedance is well modeled by a capacitance (C_P) in series with resistance (R_P) alone. Indeed, there is obviously an inductive component linked with the current flowing through the membrane. However, its contribution is small and can be neglected, which can be inferred from the fact that the S-parameters reconstructed from the extracted parameters (R_P and C_P alone) in Table 2.4 agrees well with the HFSS full wave simulations as shown in Fig. 2.8. Furthermore, it can be seen from Table 2.4 that the extracted up-state capacitance [16.05-16.38 fF] is slightly higher than the parallel plate up-state capacitance[$\frac{\epsilon_0 wW}{g_0 + \frac{t_d}{\epsilon_r}}$ =13.23 fF]. This is expected as a result of some contribution of fringing field capacitance. The extracted down-state capacitance[4.41-4.62 pF] from Table 2.4 is also in good agreement with the parallel plate down-state capacitance [$\frac{\epsilon_r \epsilon_0}{t_d} wW$ =4.9 pF].

The simulation results demonstrated that graphene can be used for RF NEMS switches in applications where low-actuation voltage and fast switching are required, at the cost of larger electromagnetic losses when compared to metal-based RF-MEMS. It was shown that multi-

layer graphene can deliver superior isolation and reduced losses at microwave and mm-wave frequency, and isolation can also be tuned with the bias voltage. Nevertheless, monolayer graphene with low sheet resistivity value can also be considered in applications where even lower actuation voltage is required.

2.6 Device Fabrication, Characterization and Discussion

2.6.1 Device Fabrication

The CVD grown multilayer graphene provided by AIXTRON is used as a membrane of the RF NEMS switch. Fig. 2.9a shows the process flow used to fabricate the device [98]. High resistivity silicon (525 μm thick) with resistivity > 10kΩcm is used as a substrate. 500 nm of low-pressure CVD (LPCVD) Si_3N_4 is first deposited on the substrate. The central conductor made of Cr/Pt (10 nm/200 nm) is fabricated by photo-lithography and liftoff. The dielectric employed for the shunt switch is atomic layer-deposited (ALD) 30-nm-thick HfO_2. Further, 800 nm of SiO_2 (LTO) is deposited by LPCVD as sacrificial layer corresponding to an effective gap of 300 nm. Next, large-area multilayer graphene (~ 1 cm^2) is deposited by wet transfer method using PMMA as transfer polymer. The deposited graphene are investigated on certain areas by atomic force microscopy and Raman spectroscopy, and the average number of graphene layers are found to be 2-5 [98]. Then, the membranes are lithographically patterned and etched using oxygen plasma (1 min). The ground planes (top contacts) made up of Cr/Pt is then defined by photo-lithography and liftoff. The devices are then annealed at 200 ^{0}C in N_2 ambient to improve the contacts. Finally, the membrane is released by etching away SiO_2 (LTO) in the buffered oxide etch, followed by critical point drying in order to avoid membrane stiction. Fig. 2.9b,c shows the scanning electron micrograph (SEM) of the fabricated device.

2.6.2 Device Characterization and Discussion

The measurements are carried out in ultra-high vacuum at room temperature. The setup for the device measurement is shown in Fig. 2.10. The scattering parameters are measured up to frequency 6 GHz using an Agilent E8361A PNA microwave network analyzer and standard GSG probes. Short-open-load-thru (SOLT) calibration is performed setting the reference planes at the probe tips. The DC bias for electrostatic actuation of NEMS switch is applied through the bias-tee as shown in Fig. 2.10. The representative NEMS devices are fabricated on the CPW structure with a 70 μm central conductor width and 10 μm gap between central conductor and ground planes. The width W of the membrane is 60 μm.

The measured scattering parameters for a CPW (unloaded) with dimensions 10/70/10 μm, and the NEMS device on the CPW structure of same size (loaded), are shown in Fig. 2.11. As expected, the resistive loading of graphene membrane decreases the transmission amplitude $|S_{21}|$ (in dB) and increases reflection amplitude $|S_{11}|$ relative to the unloaded device. As the V_{bias} increases, $|S_{21}|$ of the loaded device decreases due to electrostatic actuation of the switch
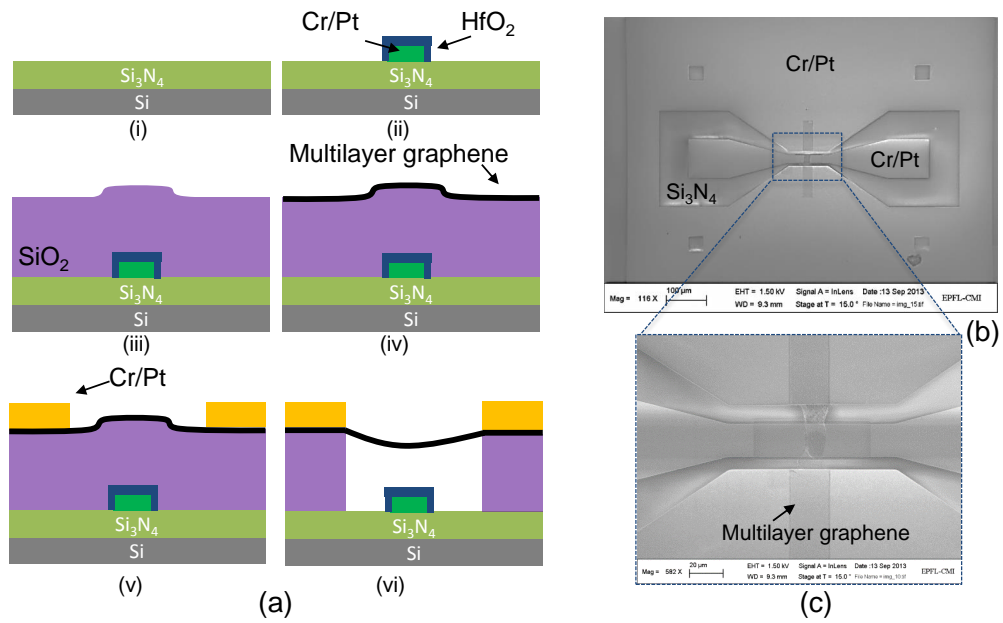
Figure 2.9: Fabrication process of the graphene RF NEMS.
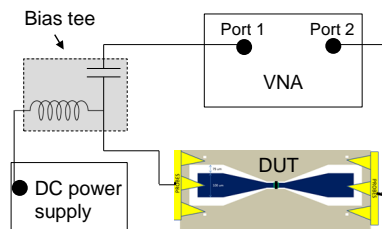
Figure 2.10: Measurement setup for characterization of graphene RF NEMS shunt switches.
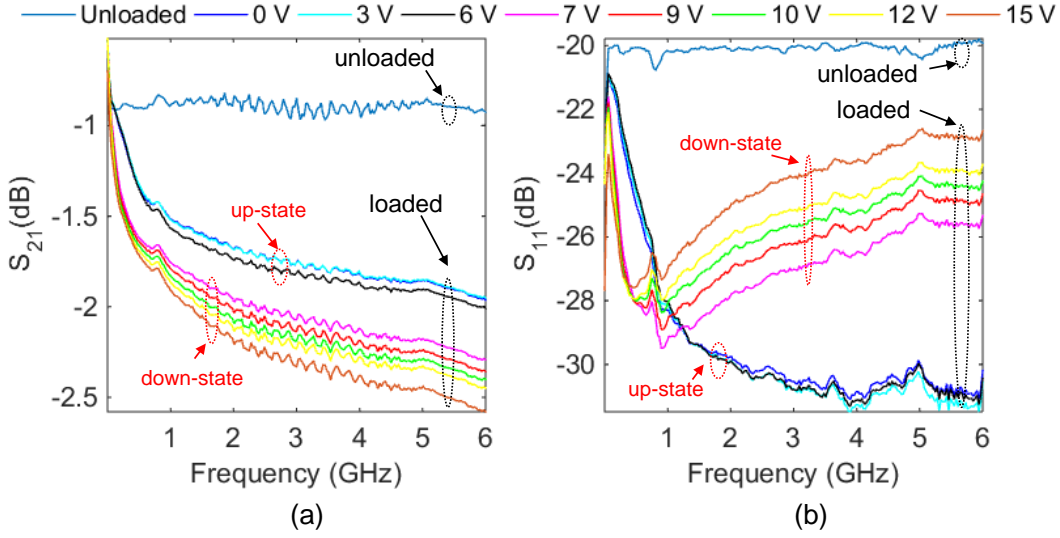
Figure 2.11: Measured S-parameters of graphene RF NEMS shunt switches.

in the up-state. As the V_{bias} increases from 6 to 7 V, sudden decrease in $|S_{21}|$ is observed which indicates the possible pull-in of the switch, and the membrane can now be considered in the down-state position. The further increase of V_{bias} decreases the $|S_{21}|$ (improves the isolation). This improvement in isolation with V_{bias} may be explained by the following effects: (1) The increase in contact area owing to the electrostatic actuation. (2) The reduction in the resistivity of the graphene membrane due to electric field effect [99] as explained in Section 2.5. The pull-out of the switch was not observed; and the measurements were not found repeatable, that is, the number of cycle was limited to 1. The possible cause may be due to the breaking of membrane in a single operation due to stiction.

The equivalent circuit parameters of the measured switch, as extracted from the T-circuit model (Fig. 2.3), are shown in Table. 2.5. To extract the intrinsic parameters of the switch, mainly the shunt components, the following deembedding procedure is performed: (1) The measured S-parameters of the loaded (S_{loaded}) and unloaded ($S_{unloaded}$) are first converted to Z-parameters ($S_{loaded} \rightarrow Z_{loaded}$, $S_{unloaded} \rightarrow Z_{unloaded}$); (2) the intrinsic shunt impedance Z_{P-NEMS} is then calculated as:

$$Z_{P-NEMS} = \left(\frac{1}{Z_{12-loaded}} - \frac{1}{Z_{12-unloaded}} \right)^{-1}; \tag{2.14}$$

and (3) the capacitance C_{NEMS} and the resistance R_{NEMS} of the membrane can thus be respectively approximated as, $C_{NEMS} = Im(1/Z_{P-NEMS})/\omega$, and $R_{NEMS} = Re(1/Z_{P-NEMS})$. This deembedding procedure is fairly accurate and also verified with full-wave simulations. The extracted capacitance and the resistance as function of V_{bias} are plotted in Fig. 2.12. From the extracted C_{NEMS} values, the capacitance ratio is estimated to be 4.3. This value is closer to the capacitance ratio obtained for CNT based NEMS (~ 4) [67], but very low when compared to state of the art metal membrane switches (~ 80) [100].

Table 2.5: Extracted equivalent circuit model parameters.

	R_S (Ω)	L_S (pH)	R_P (Ω)	C_P (fF)
unloaded	5.3	760		244.8
loaded at 0 V	4.7	620	256	1807
loaded at 15 V	4.8	760	240	5441
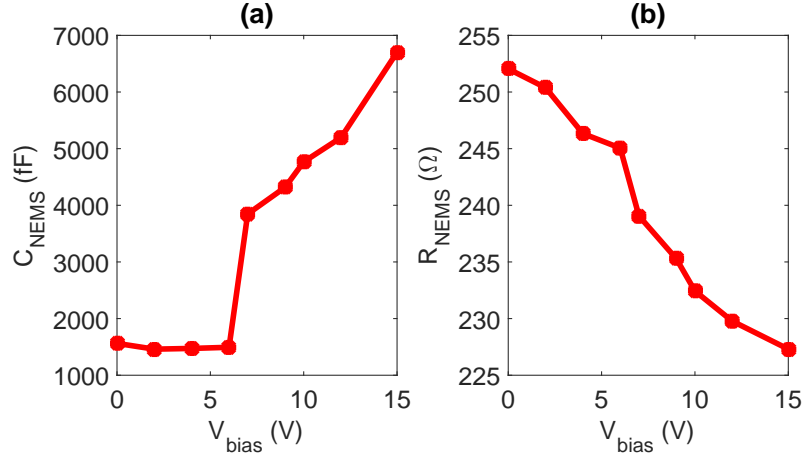
Figure 2.12: Extracted shunt capacitance C_{NEMS} and resistance R_{NEMS} as a function of V_{bias}.

As regards to the up-state capacitance, for the designed air-gap of g_0 = 300 nm, its theoretical value is 123 fF ($= \epsilon_0 w W / (g_0 + t_d/\epsilon_r)$). However, the experimentally extracted value is much higher: $C_{NEMS}(V_{bias} = 0)$ = 1560 fF. Recalculating the effective gap (g_{0-eff}) from the experimentally observed up-state capacitance value, we obtain a gap of 22 nm ($g_{0-eff} = \epsilon_0 w W / C_{NEMS} - t_d/\epsilon_r$). This implies that the membrane may be partially sagged in the initial up-state position as depicted in Fig. 2.13a and might be the possible cause of high insertion losses in the up-state.

Turning now to the down-state position, the capacitance, considering the effect of contact area, can be expressed as a function of V_{bias}: $C_{NEMS-Down}(V_{bias}) = m(V_{bias}).\epsilon_0 w W / (g_0 + \frac{t_d}{\epsilon_r})$ where we define a parameter m which depicts the fraction of total contact area in the down-state. From the experimental value in Fig. 2.12a, the effective contact area m in percentage is calculated and plotted in Fig. 2.13b. As expected, an increase in the effective area with V_{bias} is observed due to electrostatic actuation. This increase in the contact area is one of the reasons responsible for the improvement in isolation with increase in V_{bias} (Fig. 2.11a).

Further, the extracted resistance of the membrane R_{NEMS}, as shown in Fig. 2.12b, decreases with V_{bias} after the pull-in. This decrease in resistance, although limited, might also be responsible in part for the increase in isolation with V_{bias}. From the R_{NEMS} value, one can extract the sheet resistivity of membrane as $\rho_{NEMS} = 2R_{NEMS} w / (l/2)$. The extracted value is found to be in the range 640-680 Ω/□ which is closer to the value of 605.7 Ω/□ obtained
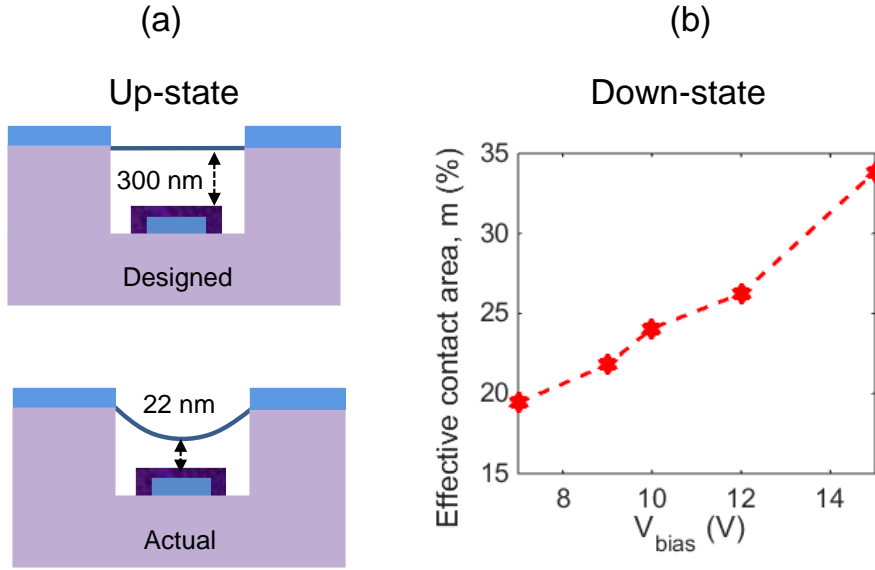
Figure 2.13: (a) Situation of the membrane in the up-state position, (b) The effective area, m in percentage versus V_{bias} in the down-state position.

through test-structures measurements of non-suspended multilayer graphene (see Appendix A).

To understand the low isolation observed for the fabricated NEMS switch, we perform full-wave simulation using the observed sheet resistance value of graphene, and using the dimensions same as our experimental device. Fig. 2.14 compares the isolation of shunt switch with state-of-the-art metal, gold, as a membrane; and graphene (different sheet resistivity values) as a membrane. As can be seen clearly, the real performance killer is the high sheet resistivity of graphene membrane which results in higher switch losses as discussed in Section 2.5. For use in applications, an isolation > 10 dB is mandatory which can be achieved with experimentally reported sheet resistivity of 30 $\Omega/\square$ [74]. To obtain performances close to state of the art, one must use a highly conductive graphene with sheet resistivity value of atleast 1 $\Omega/\square$.

With the advancement in chemical doping and using more number of layers, a high conductive graphene can be obtained as previously discussed in Section 2.2. Cautions should however be made as using more number of layers: (i) would increase the membrane's thickness, thereby increasing the pull-in voltage (Eq. 2.2); (ii) will make the membrane stiffer, i.e. reduced Young's modulus, which will increase the switching time of the switch (Eq. 2.4).

2.7 Summary

In this chapter, we evaluated the performance of NEMS shunt switch based on graphene via rigorous modeling, simulation and design. An attempt is also made to characterize the fabricated devices based on multilayer graphene. We were able to report the following original
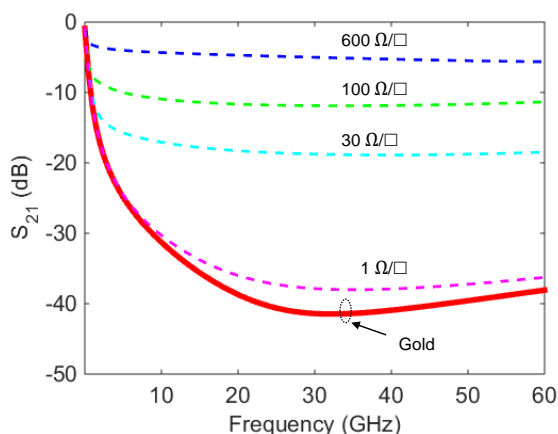
Figure 2.14: Simulated isolation of the shunt switch with different resistivity values of the graphene membrane and with metal (gold: bulk conductivity as shown in Table. 2.1 is used) as a membrane. The dimensions of the switch are same as the experimental device in Fig. 2.11. In the simulation, we consider 100 percent contact area of the membrane with the dielectric in the down-state.

contributions:

- A framework for the full-wave simulation of graphene-based RF NEMS shunt switch — taking into account the frequency- and bias-dependent conductivity of graphene — is developed for the first time. Simulations of a coplanar waveguide double-clamped graphene membrane capacitive switch, using realistic values of graphene conductivity, predict an isolation of 10 dB for monolayer and 20 dB for multilayer graphene over the frequency band from 1 GHz to 60 GHz.

- A unique conductivity variation of the membrane owing to the electric field effect of graphene is proposed for the first time (in the category of NEMS switches) and it was shown to have beneficial yet limited impact on the RF performance of the switch. This effect was also observed in experiments done by our group and by the recent experiments done by Li *et al.* [101, 102] on graphene-based RF NEMS shunt switches.

- The characterization and detailed analysis of graphene NEMS switch fabricated in our lab [98] was performed. The pull-in voltage of 7 V was reported for the fabricated device. We have also measured the RF performance of the device up to frequency 6 GHz. Insertion loss of −1.95 dB and isolation of −2.6 dB was reported. The limited RF performance of the switch was due to the high sheet resistivity of the multilayer graphene sample used for the experiments; the extracted sheet resistivity of 600 Ω/□ was also validated with the separate non-suspended multilayer graphene sheet resistivity measurements (Appendix A).

The simulation results have shown that graphene can be a good candidate for the membrane of RF NEMS switches in applications where low actuation voltage and fast switching are required. It is also demonstrated that while monolayer graphene results in quite high switch losses at

high frequency, the use of multilayer graphene, can considerably reduce the switch losses and improve RF performance. Experimentally, although, the obtained RF performances pales in comparison with state of the art switches, it should not be concluded that graphene is not a promising material for RF NEMS shunt switches as this was merely the very first attempt to fabricate these devices. Further optimization in fabrication process, and the use of graphene with low sheet resistivity will significantly improve the performance.

3 Graphene Solid-State Device Physics and Technology

In contrast to the previous chapter where we talked about suspended graphene, herein we will discuss graphene solid-state devices (which are not suspended). In particular, we focus on field effect transistors based on monolayer graphene. Broadly, this chapter talks about two main aspects: device physics (Section 3.1) and technology (Section 3.2-3.4) of graphene field effect transistors (GFETs). The main aim of this chapter is to set the foundation for next two chapters where we discuss the negative differential resistance phenomenon in GFET and GFET based circuits, and its applications. Section 3.1 focuses on the drift-diffusion model of GFETs and the circuit-simulation approach. In Section 3.2, common approaches for synthesizing monolayer graphene is reviewed; specifically, the large-scale chemical vapor deposition method — which was used to fabricate devices in this work — is discussed. Section 3.3 presents different techniques to fabricate GFETs, and finally, Section 3.4 discusses the low-field DC measurements of the fabricated devices.

3.1 Graphene Device Physics

3.1.1 Drift-Diffusion Model

In this section, we present the drift-diffusion model for top-gated GFETs [103, 104, 105]. The drift-diffusion model provides the insight into the carrier transport at low and high-fields, allows the understanding of I-V characteristics, and enables the use of computer-aided design software to stimulate circuits.

Fig. 3.1a shows the schematic of a typical GFET. The GFET consists of a gate electrode; a large area graphene channel through which charge carriers, electrons or holes, flow from source to the drain; and a dielectric separating the gate from the channel. Source and drain electrodes are connected to the intrinsic channel through an un-gated graphene region having a finite series resistance. Thus, the intrinsic GFET experiences voltages which are different from the
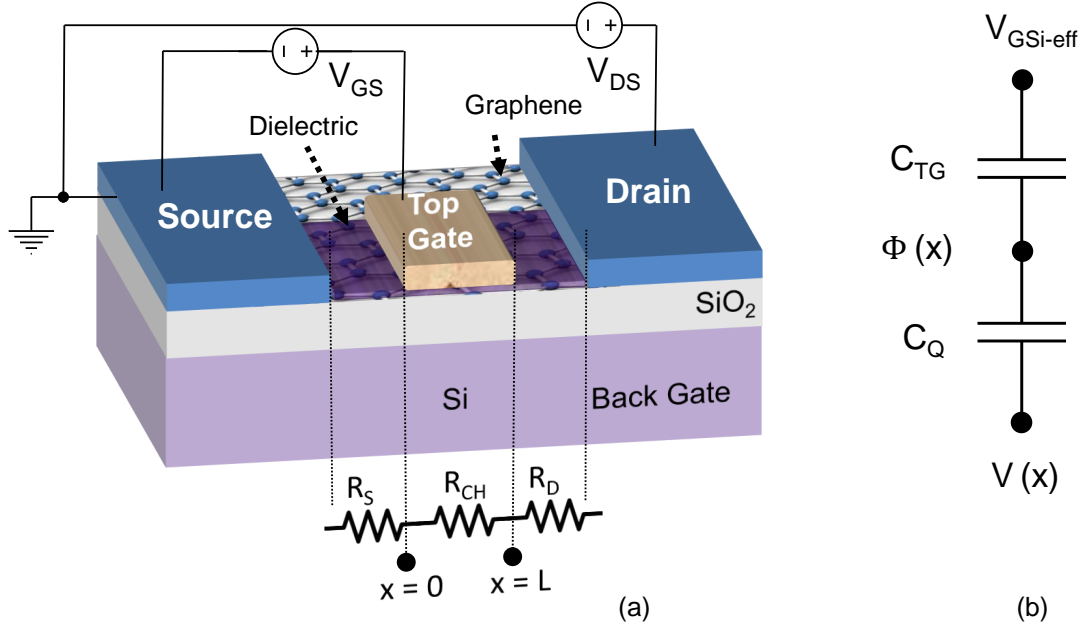
Figure 3.1: (a) Schematic of top-gated GFET. (b) Equivalent capacitive divider circuit model.

applied voltages and can be written as

$$V_{GSi} = V_{GS} - R_S I_{DS} \tag{3.1}$$

$$V_{DSi} = V_{DS} - (R_S + R_D) I_{DS} \tag{3.2}$$

where V_{GS} and V_{DS} are the applied gate-source and drain-source voltage, respectively. The subscript i refers to the intrinsic voltages. R_S (R_D) is the source (drain) series resistance which includes both the access resistance of the un-gated region and the metal-graphene contact resistance. I_{DS} is the drain-source current.

The SiO$_2$ acts as the backgate dielectric and the Si wafer acts as backgate. By applying a constant backgate voltage, the conductivity of the channel and the un-gated graphene region can be adjusted. For the purpose of simplicity, the modeling presented below assumes a constant value of V_{BG}, that is: the access resistance (which can be modulated by V_{BG}) is considered as a constant parameter; and the carrier density of the channel is considered only the function of top-gate voltage (which can also be the function of V_{BG}). Readers who are interested for modeling where combined effects both from top-and back-gate voltages are considered, can refer to [106].

An important quantity in designing nanoscale top-gated transistors is the quantum capacitance [91]. In contrast to conventional parallel plate capacitance model where one can model the total gate capacitance between the top gate and the conducting graphene layer as the

top-gate oxide capacitance, there exists the so-called quantum capacitance which also needs to be taken into account for low-dimensional systems in general (Fig. 3.1b). The quantum capacitance C_Q describes the response of the charge inside the channel to the conduction and valence band movement. Using the definition $C_Q = q\,dn_S/d\Phi_S$ where Φ_S is the surface potential across C_Q, one obtains for monolayer graphene [91]:

$$C_Q = \frac{2q^2 kT}{\pi \hbar v_F{}^2} \ln\left[2\left(1 + \cosh\frac{q\Phi_S}{kT}\right)\right]. \tag{3.3}$$

For $q\Phi_S \gg kT$, the above equation can be reduced to [91]

$$C_Q = \frac{2q^3 |\Phi_S|}{\pi \hbar v_F{}^2}. \tag{3.4}$$

The surface potential Φ_S can be calculated from the capacitance divider circuit as shown in Fig. 3.1b

$$\Phi_S(x) = \frac{C_{TG}}{C_{TG} + C_Q(\Phi_S)}\left(V_{GSi-eff} - V(x)\right) \tag{3.5}$$

where $V_{GSi-eff}$ is the effective internal gate-source voltage which is given by $V_{GSi-eff} = V_{GSi} - V_{Dirac-GS}$, where $V_{Dirac-GS}$ is the top-gate Dirac point voltage. $V(x)$ is the voltage drop in graphene channel which is $V(x) = 0$ at $x = 0$ and $V(x) = V_{DSi}$ at $x = L$.

The drain current I_{DS} flowing in an intrinsic GFET is given by [107, 103]

$$I_{DS} = q\frac{W}{L}\int_0^L n(x) v_{drift}\, dx \tag{3.6}$$

where W and L are width and length of the channel, respectively; $n(x)$ is the carrier density at a position x in the channel; and v_{drift} is the drift velocity. The carrier density $n(x)$ can be more accurately written as

$$n(x) = n_0 + \left| -(\frac{1}{2q})C_Q\Phi_S(x)\right| \tag{3.7}$$

where n_0 is the residual carrier density. Since the quantities C_Q and Φ_S depend on each other, they need to be solved self-consistently for the final estimation of $n(x)$.

The drift velocity v_{drift} is given by [107, 108, 109]

$$v_{drift} = \frac{\mu E}{\left(1 + \left(\frac{\mu E}{v_{sat}}\right)^\gamma\right)^{1/\gamma}}, \tag{3.8}$$

where μ is the low-field mobility, E is the transverse electric field, γ is the fitting parameter, and v_{sat} is the saturation velocity of carriers. The saturation velocity of graphene is mainly governed by the remote interfacial phonon scattering [107] from the bottom dielectric. In
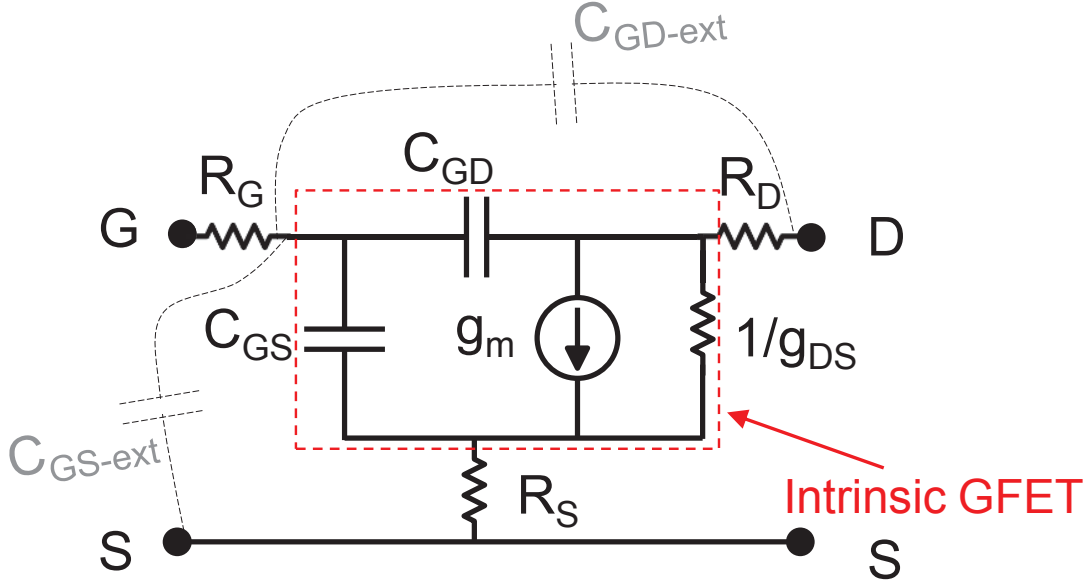
Figure 3.2: Small-signal equivalent circuit of GFET.

this scattering mechanism, the saturation velocity v_{sat} is dependent on the carrier-density of graphene and can be written as

$$v_{sat}(x) = \frac{\hbar\Omega}{\hbar\sqrt{\pi n(x)}},$$ (3.9)

where $\hbar\Omega$ is the optical phonon energy of the bottom dielectric.

3.1.2 Small-Signal and RF Model

The key use of graphene transistor, because of its high carrier mobility and transconductance, is in small signal amplifier and other radio frequency devices. To characterize the GFETs for that purpose, the small-signal model as shown in Fig. 3.2 is used. The intrinsic GFET is described by the transconductance (g_m), the drain-source conductance (g_{DS}), the gate-source capacitance (C_{GS}), the gate-drain capacitance (C_{GD}), and the series resistances R_S and R_D.

The transconductance is defined as the change in drain current caused by the small change in gate-source voltage as

$$g_m = \frac{dI_{DS}}{dV_{GSi}}\bigg|_{V_{DS}}.$$ (3.10)

The drain-source conductance (also referred as differential conductance) is defined as the

Table 3.1: Dimensions and parameters of modeled GFET.

Parameters	Values
L (μm)	0.44
W (μm)	3.4
Top-gate oxide	8.5-nm-thick Boron nitride ($\epsilon_r = 4$)
$V_{Dirac-GS}$ (V)	-0.07
μ (cm^2/(Vs))	10000
n_0 (cm^{-2})	2.2×10^{11}
γ	2
$\hbar\Omega$ (meV)	56
R_S, R_D (Ω)	0

change in drain current caused by the small change in drain-source voltage as

$$g_{DS} = \frac{dI_{DS}}{dV_{DSi}}\bigg|_{V_{GS}}. \tag{3.11}$$

The gate-source and the gate-drain capacitances are given by the expressions:

$$C_{GS} = \frac{dQ_{CH}}{dV_{GSi}}\bigg|_{V_{DS}}, \tag{3.12}$$

$$C_{GD} = \frac{dQ_{CH}}{dV_{DSi}}\bigg|_{V_{GS}}, \tag{3.13}$$

where Q_{CH} is the total charge in the channel which in general can be calculated by $Q_{CH} = W \int_0^L n(x)\,dx$. More accurately, these capacitances can be calculated using the analytical expressions proposed by Zebrev *et. al* [110]; the analytical expressions are given as

$$C_{GS} = WLC_{CH}\left[F(s) + \frac{1}{2}\left(-\frac{dF(s)}{ds}\right)\left(s\left(\frac{dV_{DSA}}{dV_{GSi}}\right) - 1\right)\right], \tag{3.14}$$

$$C_{GD} = \frac{WLC_{CH}}{2}\left(-\frac{dF(s)}{ds}\right), \tag{3.15}$$

where C_{CH} is the channel capacitance given as $C_{CH} = C_{TG}C_Q/(C_{TG} + C_Q)$, V_{DSA} is given as $V_{DSA} = 2q[n(x=0) - n_0]/C_{CH}$, s is a dimensionless parameter which is defined as V_{DSi}/V_{DSA}, and the dimensionless $F(s)$ function is given as

$$f(s) = \begin{cases} \frac{1}{2}[1 + (1-s)s(\coth s - 1)] & : s \leq 1 \\ \frac{1}{4}\left[(1 + \coth s)(1 - e^{-2}) - \frac{e^{s-2} - e^{-s}(1 - 2(1-s)s)}{\sinh s}\right] & : s > 1. \end{cases} \tag{3.16}$$
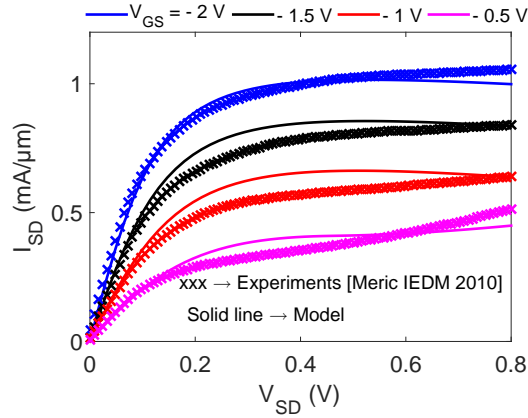
Figure 3.3:   Modeled output characteristics of GFET in Table. 3.1 and its validation with experiments.
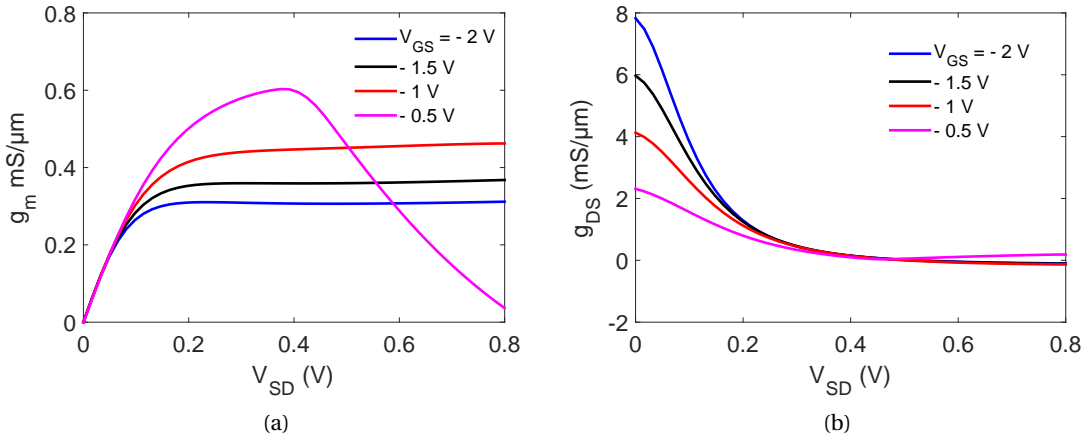
Figure 3.4: (a) Modeled transconductance g_m and (b) differential conductance g_{DS} as a function of V_{SD} of GFET in Table. 3.1.

3.1.3   Model Validation and Circuit Simulation Approach

To validate the model against experimental data, we used the GFET from ref [111]. Table. 3.1 summerizes the GFET dimensions and parameters used for the simulation. Fig. 3.3 shows the modeled output characteristics for this transistor, showing excellent agreement with the experimental data. The output characteristics of typical top-gated GFET has three region of operation: (I) linear region, (II) semi-saturation region, and (III) 2nd linear region [111]. Although, for aggressively scaled top-gated oxide GFETs, a negative differential resistance region can also be observed; this region is discussed in great detail in the next chapter.

The small signal transconductance g_m and the differential conductance g_{DS} from the validated model are plotted in Fig. 3.4. The small signal capacitances as calculated from the Eq. 3.14, 3.15 are shown in Fig. 3.5.
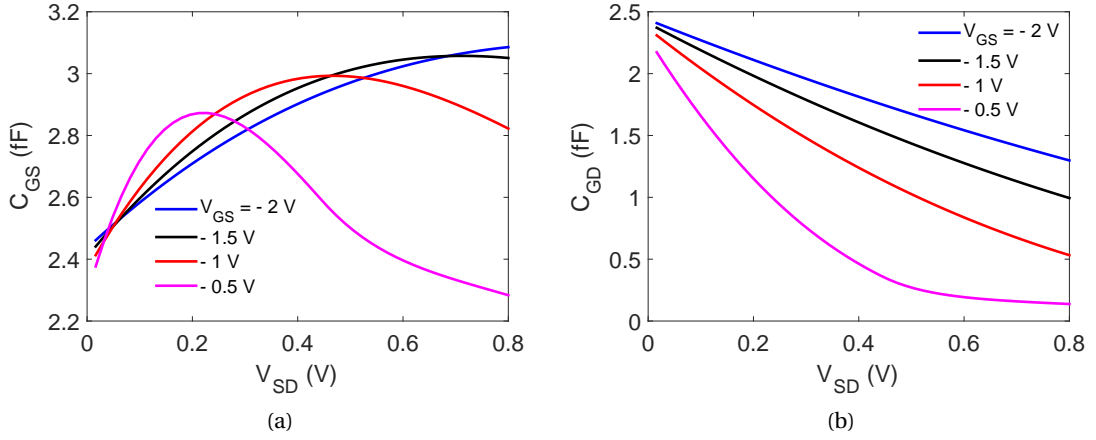
Figure 3.5: (a) Modeled gate-source capacitance C_{GS} and (b) drain-source C_{GD} as a function of V_{SD} of GFET in Table. 3.1.
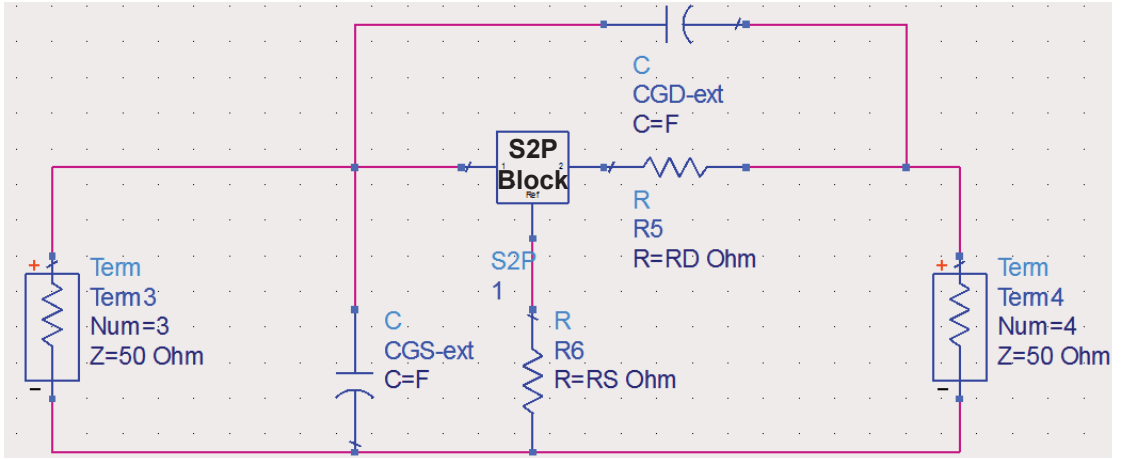
Figure 3.6: Model implementation in Agilent ADS for circuit level simulation.

To this end, we have calculated the intrinsic small-signal parameters. The model is then implemented in Agilent Advanced Design System (ADS) for full circuit level simulation. Parasitic components such as series resistances and the underlap capacitances can also be added as shown in Fig. 3.6. To implement the model in Agilent ADS, the intrinsic components are represented by admittance parameters $[Y]$. It is convenient to use the admittance parameters here because the small signal model (Fig. 3.2) exhibits a π topology. These parameters are

$$Y = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} = \begin{pmatrix} j\omega(C_{GS}+C_{GD}) & -j\omega C_{GD} \\ g_m - j\omega C_{GD} & g_{DS} + j\omega C_{GD} \end{pmatrix}. \tag{3.17}$$

The admittance parameter $[Y]$ is transformed to scattering parameter $[S]$. Next, in Agilent ADS, an 'S2P block' is created, to which $[S]$ parameter file is passed. Parasitic resistances such as gate resistance (R_G), R_S and R_D and parasitic capacitances C_{GS-ext}, C_{GD-ext} can be added

in the simulator to take into account for the extrinsic effects. The implementation in Agilent ADS enables scattering parameter, DC, transient and other measurements.

3.2   Graphene Synthesis

The synthesis methods of graphene include mechanical exfoliation, liquid phase exfoliation, epitaxial growth on SiC substrate, chemical vapor deposition, chemical reduction of graphene oxide, opening of CNTs. Depending on the intended application, there are advantages and disadvantages of each methods. For electronic devices applications, three major methods are used as described below:

3.2.1   Mechanical Exfoliation

Although the first mechanical exfoliation of graphene (~15 layers) was carried out in 1960 by Fernandez-Moran [112], it was Geim's group that firstly discovered the monolayer graphene by mechanical exfoliation in 2005 [113]. This method involves placing small fakes of high-quality carbon such as highly orientated pyrolytic graphite (HOPG) on the adhesive side of the tape and then transferred to the substrate. Peeling the tape off the substrate leaves small areas of irregularly shaped graphene, usually of the order of μm dimensions. The electronic quality of the resulting graphene is very high, with carrier mobilities up to 200,000 $cm^2V^{-1}s^{-1}$. However, this method suffers from major disadvantages such as poor yields, size limitation, difficulty in controlling flake location. Thus the application of this method is limited mainly to laboratory research, studying transport behaviour or as a reference for benchmarking other synthesis methods of graphene.

3.2.2   Epitaxial Growth on SiC

The synthesis of monolayer graphene by thermal decomposition of SiC has been proposed as a practical route for the synthesis of wafer-size graphene for nanoelectronic applications [26, 114, 12]. The major advantage of this technique is that insulating SiC substrate can be used so that the transfer to another substrate is not required. In this method, graphene is directly grown on SiC substrate by heating at about 1300 ^{0}C in ultra-high-vacuum. Under such conditions, the silicon atoms on top sublimate and graphene is formed on the surface. The quality of graphene is highly influenced by the surface terminations which is either Si or carbon. On Si-terminated face, the graphene domain is in the range of 30-100 nm, whereas on carbon-terminated face, the domain size is ~ 200 nm. The electronic quality of graphene produced by this method is lower than graphene by mechanical exfolation method; carrier mobilities up to 10,000 $cm^2V^{-1}s^{-1}$ have been demonstrated with this method [115]. Like other synthesis methods, this method has also has its share of limitations such as: the large-scale structural quality is limited at present by the lack of continuity and uniformity of the grown film [116]; the substrate SiC itself is not a CMOS compatible substrate, consequently
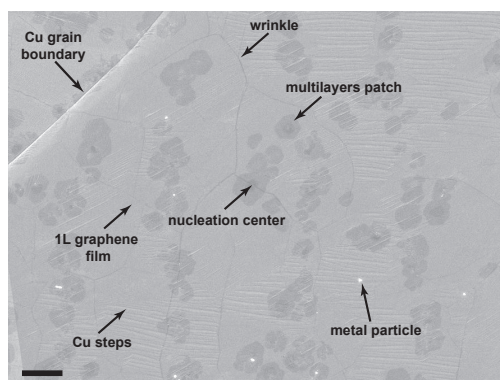
Figure 3.7: SEM image of as-grown graphene on Cu foils. The scale bar is 3 μm.

limiting its use in many applications; and the thermal resistance (frequently called as Kapitza resistance) associated with graphene-SiC is significantly larger than that of graphene-SiO$_2$ interface which should be kept low for many electronic applications [16].

3.2.3 Chemical vapor deposition

Chemical vapor deposition is the most widely used synthesis approach for graphene [117]. The graphene used for the fabrication of devices in the later part of this chapter and in subsequent chapters are obtained using this technique. The major advantage of this technique is the possibility to obtain large-area uniform films of graphene; the production of square metres of graphene has already been achieved. These films have also been transferred onto 300-mm Si wafers on which state-of-the-art devices have been demonstrated [118]. In addition, its high throughput, low cost and CMOS compatibility makes it the most flexible and versatile technique for graphene synthesis. This method involves two major steps: (1) The growth of graphene by CVD on metal such as copper or nickel; and (2) the transfer from the metal support to the substrate of interest.

A. Growth

In typical CVD process, the metallic substrate is exposed to one or more volatile precursors, which react and decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber. The production of graphene using CVD process was first reported in 2008-09, using Ni and Cu substrates [119, 120, 79, 80, 121]. In this work, we will focus on Cu, as the CVD graphene used to fabricate devices in this work is grown on Cu [122].

The graphene films were grown on 25 μm thick Cu foil (99.98 % from Sigma Aldrich) in a horizontal tubular furnace. Initially, Cu foil was first annealed at 1000 ^{0}C for 30 minutes in 3 Torr of H$_2$ with the chamber being closed by a valve. Then a mixture of H$_2$/CH$_4$ was introduced into the system to initiate the graphene growth. After a continuous graphene

layer was formed on Cu foil, the system was cooled down to room temperature. Fig. 3.7 shows the SEM image of Cu foil with the graphene film. The image contains useful legends indicating the key elements of typical graphene growth. There are Cu grain boundaries since the processed foils are polycrystalline. The growth of graphene also occurred at the grain boundaries [123, 124]. The as-grown graphene exhibits wrinkles which are attributed to differences in the thermal expansion coefficients between graphene and Cu. Owing to impurities in the Cu foil composition, some white particles came out at its surface along the process. They have been identified as metallic ones (Si, Al or Fe). The light grey background is the monolayer graphene film. The darker areas are multilayer patches typical for CVD graphene and are unavoidable at such growth pressure and growth time. The Cu steps appear due to the competitions of two events. First, when graphene starts to grow, some Cu areas are covered by the carbon and therefore the sublimation of the Cu in that area is suppressed which interrupts the desorption of the carbon species and reduces the Cu foil thickness which happens at a rate of about 4 μm/h at 1000 ^{0}C [125]. Second, the uncovered Cu areas close to the edge of the graphene grains are still etched by the Cu sublimation and there the graphene keeps growing.

B. Transfer

To make electronic devices with graphene, we need to remove the underlying metal substrate from graphene and transfer graphene onto desired insulating substrate. A schematic diagram of transfer process is shown in Fig. 3.8. Graphene/Cu sample was first spin coated (4000 rpm, 1 min) by a thin layer of polymethyl methacrylate (PMMA) and then baked at 120 ^{0}C to evaporate the solvent. The Cu was then etched away by floating the PMMA/graphene/Cu sample in 0.05 g/ml ammonium persulfate (($NH_4)_2S_2O_8$) solution for 4 hours. The PMMA/graphene film was washed with 1 M HCl and deionized water for several times. Before the transfer of PMMA/graphene, the target substrate (Si/SiO$_2$) was cleaned by oxygen plasma to improve the hydrophilicity of the substrate. The PMMA/graphene film was then placed on the 200 mm Si/SiO$_2$ substrate, positioned and dried. The PMMA coating was removed with acetone and the substrate was rinsed with isopropanol. To minimize the typical PMMA resist residue problem associated with CVD graphene transfer, the sample was annealed 200 ^{0}C in N$_2$ ambient.

The quality of graphene after the transfer was characterized using micro-Raman mapping as shown in Fig. 3.9. Micro-Raman mapping was performed on the area where GFET were to be fabricated. An area of 30×30 μm^2 of the sample was mapped using a 1 μm wide laser spot. A full Raman spectrum was recorded every micrometer: each square of the map represents a Raman signal as depicted in Fig. 3.9a-f. The blue spot on the map exhibits a 2D/G band ratio of 2.2-3 and a 2D band full width at half maximum (FWHM) of 32-37 cm^{-1}, typical for monolayer graphene as shown in Fig. 3.9g. While the green spot exhibits a 2D/G band ratio of 0.7 and a 2D band FWHM of 55 cm^{-1}, typical for multilayers graphene as shown in Fig. 3.9i. In order to observe the average film type in terms of its thickness and quality (defect) in this area, we extracted the mean spectrum (from the 900 Raman spectra) as shown in Fig. 3.9h.
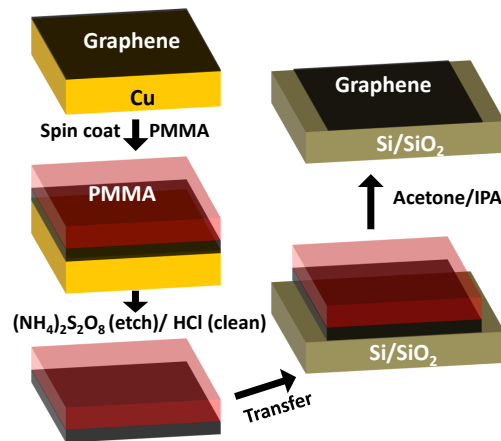
Figure 3.8: Schematic diagram of the graphene transfer process.

The mean spectrum — although has no physical meaning — provides a good way to gauge the global film characteristics. It exhibits a 2D/G band ratio of 2.5 and a 2D band FWHM of 36 cm^{-1}, which are typical hallmarks of monolayer graphene. Therefore, we can conclude that the as-grown film is a high quality monolayer graphene.

3.3 Device Fabrication

3.3.1 Top-gate GFET

The top-gate configuration is the most widely used approach to fabricate GFETs [126, 107, 127, 9, 128, 129]. The main advantage of this configuration lies in the fact that graphene is deposited on a clean substrate (as this is the very first step of the process flow), which results in a better quality graphene. The electronic quality of graphene mainly the carrier mobility is highly affected by the surface roughness of dielectric on which it is sitting [130]. Various dielectric substrates for fabricating top-gated GFETs are reported in literature namely Si/SiO$_2$ [126, 107, 127, 9, 128, 129], sapphire [131], glass [15], SiC [10]. The most common dielectric is Si/SiO$_2$ with either 90 or 300 nm-thick SiO$_2$; the main reason is the ease of visual identification of graphene on this thickness of dielectric [132]. The devices discussed in the next chapters are fabricated using the top-gating approach using either 90 or 300 nm-thick SiO$_2$/Si.

The process flow schematic of top-gated GFET is shown in Fig. 3.10. The devices were made on 100-mm Si substrate. SiO$_2$ dielectric with either 300 nm or 90 nm thickness was grown on the substrate. An approximate 1 cm× 1 cm area of CVD graphene, as described in the last section, was transferred and positioned on the substrate. Graphene was then patterned using electron beam lithography and subsequent oxygen plasma etch. The optical micrograph after the etching is shown in Fig. 3.11. The source and drain electrodes made of Ti/Pd/Au (1 nm/20 nm/40 nm thick) were fabricated by second electron beam lithography and liftoff. The use of 1 nm Ti is for good adhesion of electrode with graphene. As Ti deposited is only 1 nm, the main
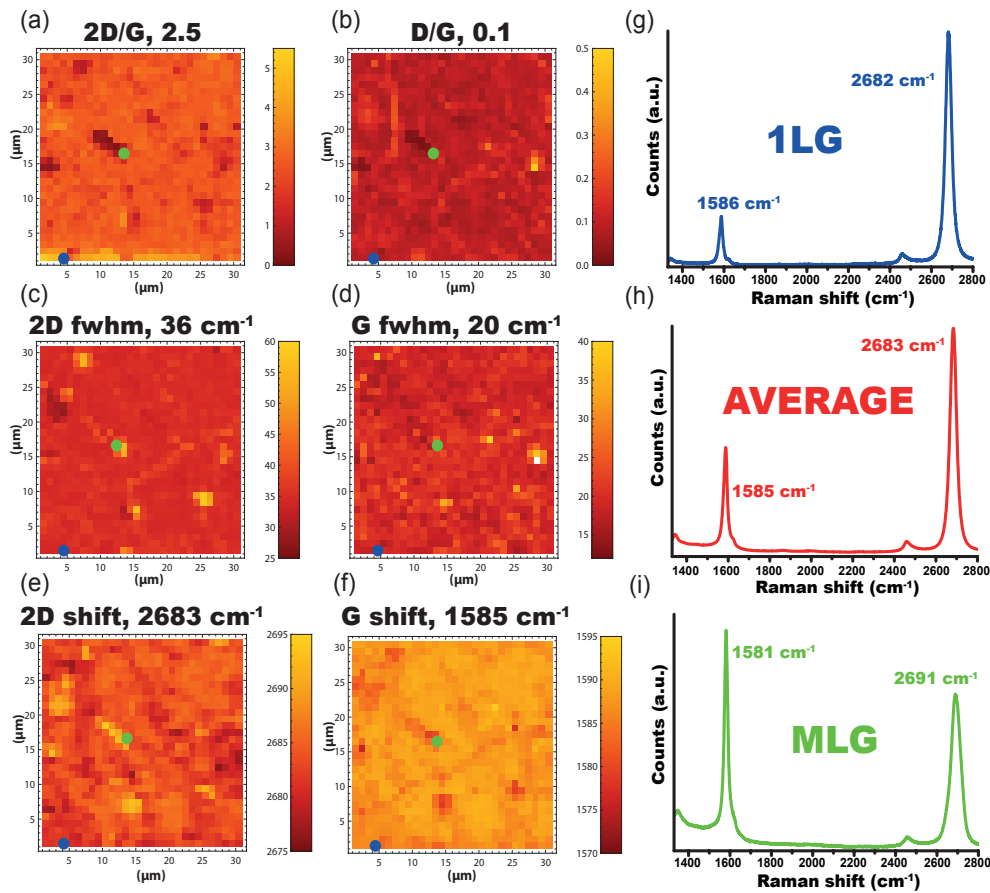
Figure 3.9: Micro-Raman mapping of graphene grown by CVD on SiO_2/Si. Raman maps of the intensity ratio of the 2D band to the G band (a) , of the D band to the G band (b), of the 2D band (c) and G band (d) full-width at half maximum, of the 2D band (e) and G band (f) positions. The numbers above the maps are their average values. (g) Raman spectrum of the blue spot corresponding to monolayer area. (h) Mean spectrum of the 900 spectra recorded to build the maps. (i) Raman spectrum of the green spot corresponding to a multilayers area. All maps have been measured over a 30×30 μm2 area with a 1 μm resolution. The excitation laser wavelength is 532 nm.
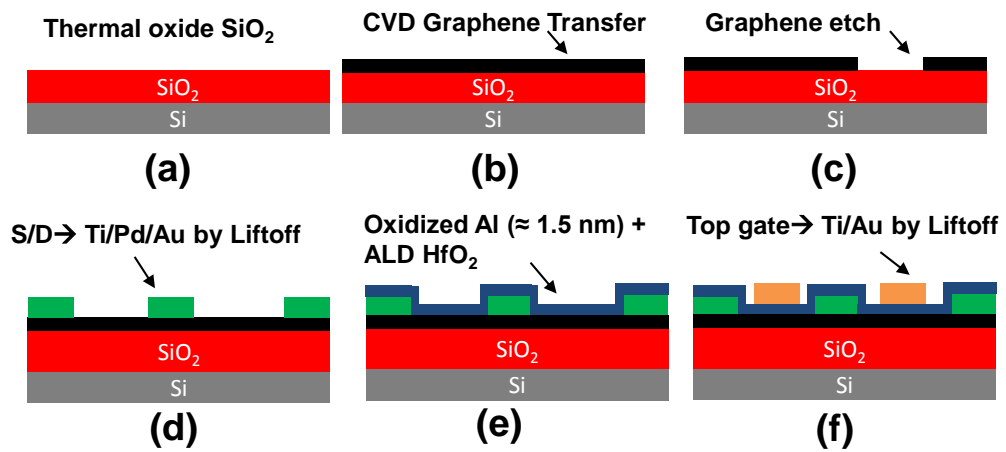
Figure 3.10: Schematic of process flow for fabricating top-gated GFETs.
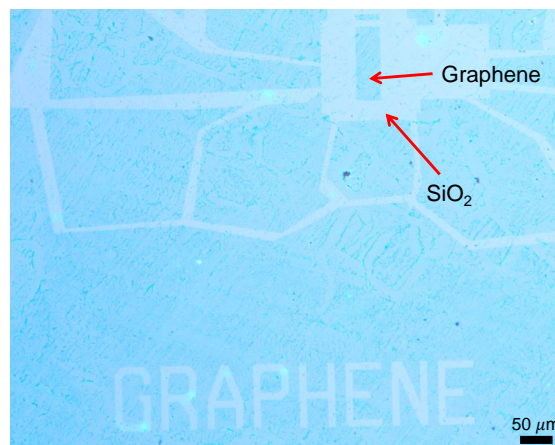
Figure 3.11: Optical micrograph of etched graphene on Si/SiO$_2$.
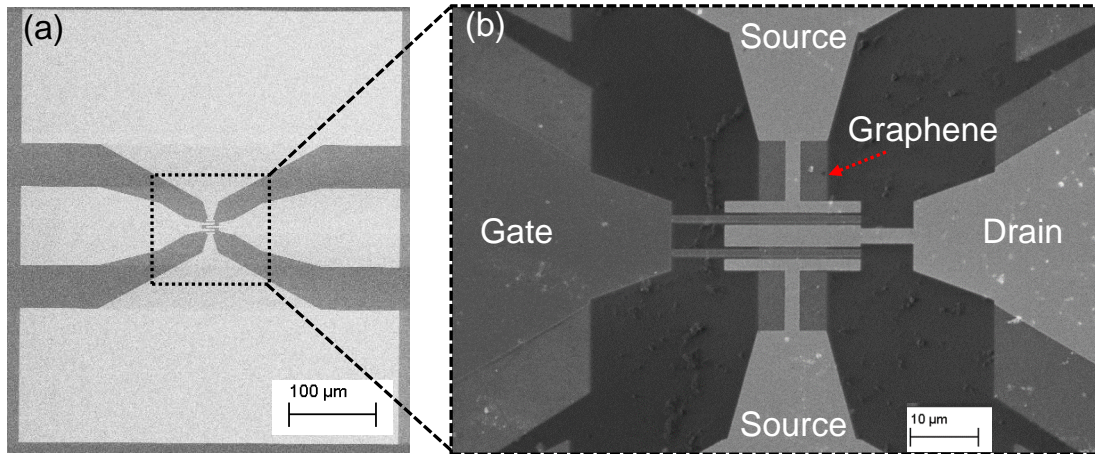
Figure 3.12: SEM image of fabricated top-gated GFET.

chemistry between graphene and electrode is dictated by graphene-Pd. Among all graphene-metal contacts, graphene-Pd contacts are known to give the lowest contact resistance [133]. The next step is to form the top-gate oxide on graphene. We used high-κ dielectric materials, such as Al_2O_3 and HfO_2, which were deposited via atomic layer deposition (ALD). The direct deposition of high-κ dielectric material on graphene using H_2O-based ALD, however, is not possible because of the hydrophobic nature of graphene basal plane [134]. Thus, prior to the oxide deposition, nucleation sites on inert surface of graphene [128] are created intentionally. For this purpose, a seed layer of Al ($\sim$ 1.5 nm) was deposited on graphene using e-beam evaporation and was later thermally oxidized (120 °C, 6 hours). Then, either a 5-nm-thick HfO_2 or a 15-nm-thick Al_2O_3 layer was deposited via ALD. Finally, the metal stack Ti/Au (20 nm/40 nm) was deposited as top-gate electrode. The SEM image of the completed device is shown in Fig. 3.12.

3.3.2 Embedded-gate GFET

One major issue with top-gate configuration is the use of seed layer for top gating of graphene transistors as discussed in the previous section. The use of seed layer — an avoidable step due to the inert nature of graphene surface — leads to problems such as unintentional doping, clustering effects and the inability to scale the dielectric thickness [135]. To avoid this problem, the straight-forward solution would be to make the gate oxide before graphene deposition. The FET made with this configuration is commonly known as embedded gate or buried gate transistors.

The electronic quality of graphene on the substrate depends on the planarity and cleanliness of the substrate surface. Most of the embedded FET based on graphene uses chemical mechanical polishing (CMP) as a technique to make embedded gates [136, 137, 138, 14, 139]. However, the use of CMP may lead to problems such as dishing in the embedded gates and dirty substrate for graphene deposition as discussed later. Herein, we fabricate embedded
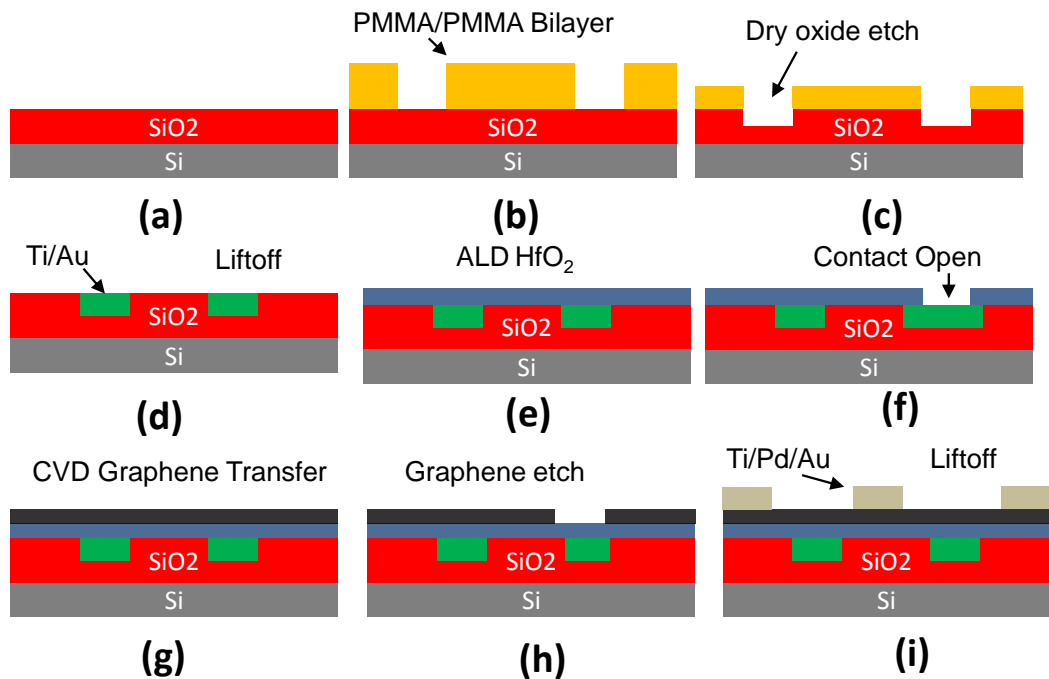
Figure 3.13: Schematic of process flow for fabricating embedded-gate GFETs.

graphene FET without the use of CMP [140, 141]. In addition to achieving a highly planar and clean surface, this technique enables quicker fabrication process with fewer lithography steps. Furthermore, this technique can also be used for fabricating transistors based on any two-dimensional channel material that can be transferred such as MoS_2 [17].

The embedded metal gate GFETs were fabricated using the flow shown in Fig. 3.13 (we refer this process as CMP-free process.). High resistivity 100-mm silicon wafer with 1 μm thick thermal SiO_2 was used as a starting material. First, a PMMA 495K (70 nm)/PMMA 950K (140 nm) bilayer was spun and baked on the wafer. Thereafter, electron beam lithography was carried out to define gate electrodes. Next, plasma etching with a mixture of CHF_3 and SF_6 for 25 seconds was used to remove ~ 60 nm of SiO_2. The plasma etching also removed ~100 nm of resist leaving PMMA 495K (70 nm)/PMMA 950K (40 nm) bilayer for liftoff. Finally, (10-nm Ti/50-nm Au) was deposited using ebeam evaporation and then liftoff. Fig. 3.14a shows the SEM image after the completion of embedded gate step.

To compare, we also fabricated embedded gates using conventional damascene process utilizing CMP with copper on another wafer (we refer this process as CMP process); the SEM image of the embedded Cu gate with CMP is shown in Fig. 3.14b. Our CMP-free process offers several advantages as compared to the CMP process for the definition of embedded gates. First, as shown in Fig. 3.14c-d, our CMP-free process gives a highly planar surface as compared to the CMP process where huge dishing in Cu is usually observed after CMP. Second, the CMP process leaves significant amount of resist residues from the slurry on copper which is usually difficult to clean. In our CMP-free process, there is no such problem of resist residues.
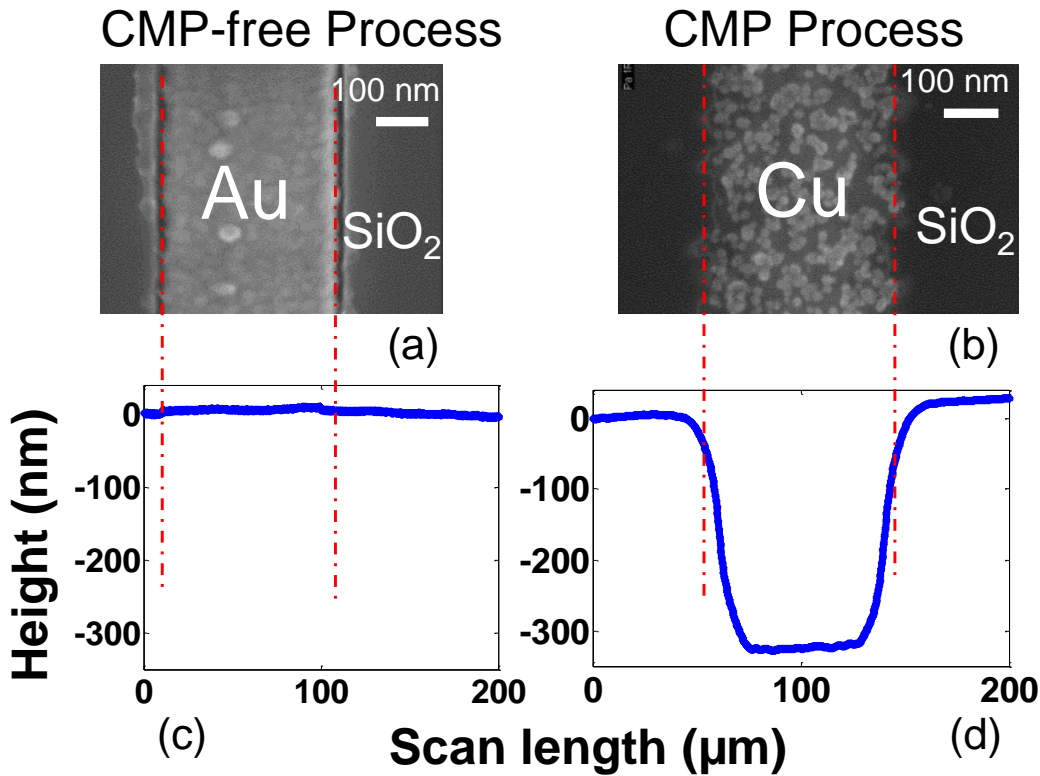
Figure 3.14:   (a) SEM image after step **d** of CMP-free process (Fig. 3.13). (b) SEM image of planerized embedded copper in SiO_2 after CMP process. (c) Surface topography of **a**. (d) Surface topography of **b**.

Finally, the use of gold in CMP-free process allows the writing of alignment markers in the same mask level as embedded gate level, saving one extra masking step. The higher atomic weight contrast of gold with silicon render gold markers automatically detectable by electron beam lithography system. On the other hand, embedded Cu was not detected automatically because of its low atomic weight contrast with silicon.

The fabrication of our CMP-free process continued with the ALD of 20 nm HfO_2. The contact pad to the gate was lithographically patterned and etched open using the argon based ion beam etching. CVD grown graphene was transferred to the embedded gate substrate by typical wet etching (Section 3.2.3). Graphene was patterned with a third lithography step and reactive ion etching in oxygen plasma. The device was completed by evaporating Ti/Pd/Au (1 nm/20 nm/40 nm) source and drain electrodes to contact the graphene. Fig. 3.15 shows the SEM image of a finished device.
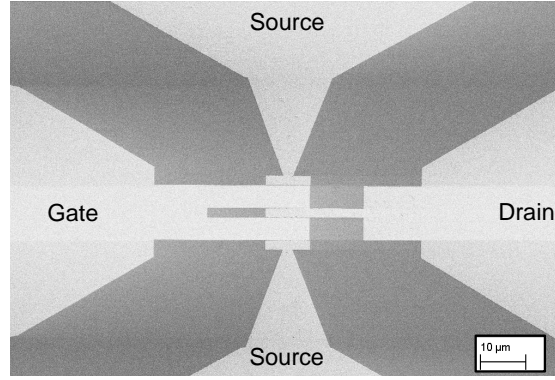
Figure 3.15: SEM image of fabricated embedded-gate GFET.

3.4 Low-Field Measurements

3.4.1 Graphene on Si/SiO$_2$ without top-gating

Herein, we present measurements of monolayer graphene on Si/SiO$_2$ (295-nm-thick SiO$_2$), without any top-gating. The graphene was biased through the back-gated silicon substrate. The measurements were performed after the step (d) of Fig. 3.10. The DC characteristics were measured with an HP 4145B Semiconductor Parameter Analyser. All the measurements were carried out in room temperature in vacuum.

Fig. 3.16a shows the transfer characteristics of device with channel length of $L = 3$ μm and width of $W = 5$ μm. The device exhibits the ambipolar behaviour typical for monolayer graphene. The Dirac point voltage $V_{Dirac-BG}$, defined as the minimum point of current conduction [54], was reached at $\sim$ 80 V indicating strong p-doping. We also extracted the contact resistance of the graphene-metal contact — which in this case graphene-Pd — through the separate array of graphene transistors as shown in Fig. 3.16c. Though the transfer length method (TLM), we extracted the back bias-dependent contact resistance R_C as shown in Fig. 3.16d. The dependency of back bias voltage V_{BG} on R_C is due to the doping of graphene below the metal and is consistent with other reports [133, 142, 143] showing the similar trend.

The carrier density n induced by the back gate voltage V_{BG} was estimated from $n = C_{BG}(V_{BG} - V_{Dirac-BG})$ where C_{BG} is the back gate capacitance which can be approximated as $C_{BG} =$ 11.6 nFcm^{-2} (for a SiO$_2$ layer of 295 nm thickness and relative dielectric constant of 3.9, measured by ellipsometer). The sheet resistivity ρ of graphene was then deduced as $\rho = (V_{DS}/I_{DS} - 2R_C W)W/L$ and was plotted in Fig. 3.17a. Finally, the drude model was employed to estimate the mobility of device $\mu = (qn\rho)^{-1}$. Fig. 3.17b shows the extracted mobility versus carrier concentration of the measured device.
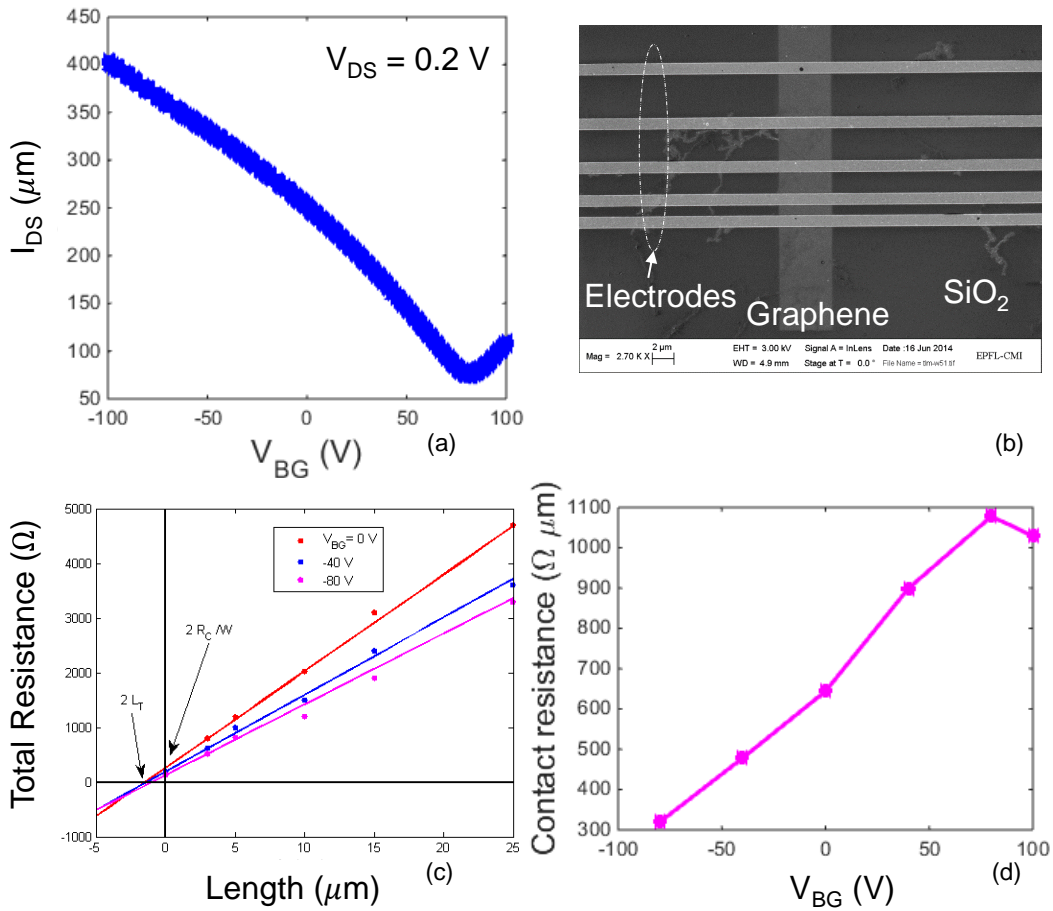
Figure 3.16: (a) Drain current (I_{DS}) as a function of back bias voltage (V_{BG}). (b) SEM image of an array of graphene transistors; the graphene channel width is 5 μm and the channel length varies from 3 μm to 25 μm. (c) Plot of total resistance of the devices as a function of channel length L for $V_{BG} = -80, -40$ and 0 V. (d) R_C as a function of V_{BG}.
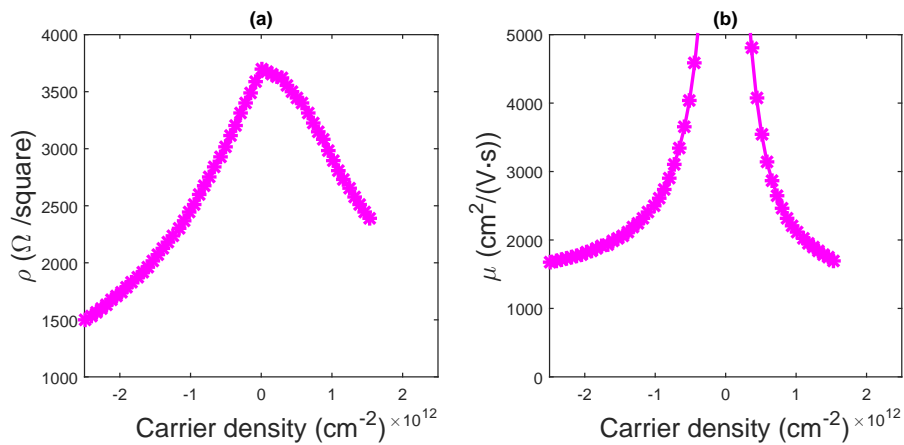
Figure 3.17: (a) Sheet resistivity ρ; and (b) carrier mobility μ as a function of V_{BG}.

3.4.2 Top-gate GFET

The top-gated geometry, whose measurements are presented in this section, is shown in Fig. 3.18a. The top-gate dielectric is 5-nm-thick HfO_2 which was deposited after the thin seed layer of oxidized Al($\sim$ 1.5 nm) as discussed in Section 3.3.1. Fig. 3.18b shows the transfer characteristic of a device with $L = 1$ μm and $W = 20$ μm. The device is a typical ambipolar FET as manifested by the "V" shape of the transfer curve. Fig. 3.18c shows the corresponding transconductance g_m of the device which is defined as $g_m = dI_{DS}/dV_{GS}$. To extract carrier mobility from transfer characteristics, the oxide capacitance of the top-gate stack must be obtained first.

In the dual-gated GFET configuration, the carriers in the graphene channel can be controlled both by top gate bias V_{GS} and back gate bias V_{BG}. Specifically, top-gate voltage Dirac point, $V_{Dirac-GS}$, can be shifted via V_{BG} as shown inFig. 3.19a. This shift in $V_{Dirac-GS}$ is linearly proportional to the change in V_{BG} as shown in Fig. 3.19b; and their ratio is — in fact — related to the back-gate capacitance C_{BG} and top-gate capacitance C_{TG} as $|\triangle V_{BG}/\triangle V_{Dirac-GS}| = C_{TG}/C_{BG}$ [129, 127, 144]. Thus, from the known $C_{TG} \sim 38.3$ nFcm^{-2} (90 nm SiO$_2$, relative dielectric constant of 3.9) and $|\triangle V_{BG}/\triangle V_{Dirac-GS}| = 39.2$ (Fig. 3.19b), C_{TG} is estimated to be 1.5 μFcm^{-2}. This corresponds to an equivalent oxide thickness (EOT) of 2.3 nm.

The carrier mobilities for electron and hole branches are then extracted based on the model proposed by Kim *et al.* [128]; this model assumes a carrier concentration independent mobility. It should, however, be noted as a caveat that this model overestimates the mobility by overcompensating series resistance [145]. Nonetheless, given the fact that majority of groups reported mobility using this model [129, 146, 147, 148, 149, 150, 144, 151, 152, 153, 154, 155], we compute mobilities based on this model itself as this will serve as way to compare mobilities with other reports. The total resistance R_{TOT} in the GFET is given as

$$R_{TOT} = R_S + R_D + \frac{L}{W}\frac{1}{q\mu\sqrt{n_0{}^2 + n^2}}. \tag{3.18}$$

In the above equation, R_{TOT} is calculated as $R_{TOT} = V_{DS}/I_{DS}$ and carrier density n can be calculated using the equation [103]

$$n = \left| -\frac{1}{2q}C_Q\Phi_S \right|, \tag{3.19}$$

where the quantum capacitance C_Q and the surface potential Φ_S are calculated using

$$C_Q = \frac{2q^3|\Phi_S|}{\pi\hbar v_F{}^2}, \tag{3.20}$$

$$\Phi_S = \frac{C_{TG}}{C_{TG} + C_Q}\left(V_{GS} - V_{Dirac-GS}\right). \tag{3.21}$$

(a)

(b)

(c)
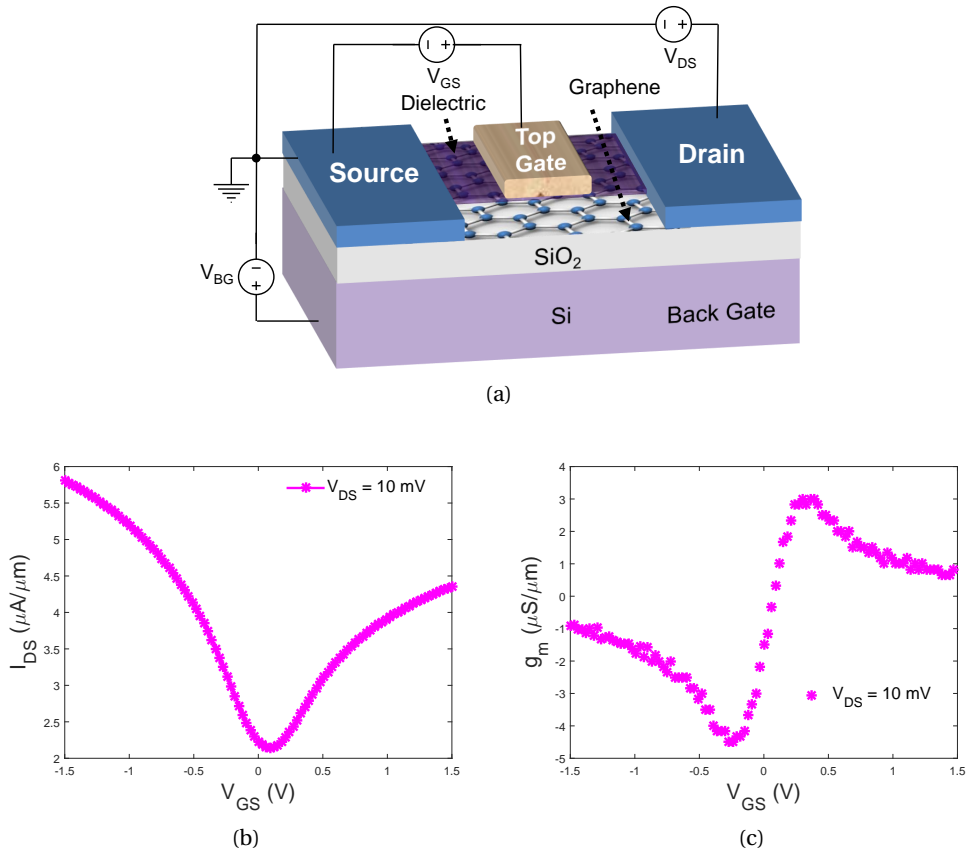
Figure 3.18: (a) Schematic of a top-gated GFET. (b) Transfer characteristics at $V_{BG} = 0V$; and (c) its corresponding transconductance.

Note that the above equations are for top-gated GFET without back-gating as we are mainly interested to calculate the carrier density at $V_{BG} = 0$. Since the quantities C_Q and Φ_S depend on each other, they are solved self-consistently for the final estimation of n as shown in Fig. 3.20a. Using the estimated n and Eq. 3.18, carrier mobilities are calculated — separately for electron and hole branches — by fitting the total resistance to the experimental data as shown in Fig. 3.20b. The hole and electron mobilities of the device are estimated to be 2894 cm^2/(Vs) and 3505 cm^2/(Vs), respectively; whereas, the minimum carrier density n_0 is found to be approximately ~ 6.5 $\times 10^{11}$ in both the branches.

3.4.3   Embedded-gate GFET

Fig. 3.21a shows the schematic of embedded gate structure whose fabrication was discussed in Section 3.3.2. The embedded gate dielectric used in this case is 20 nm ALD HfO$_2$. Fig. 3.21b shows the transfer characteristic of a device with $L = 1$ μm and $W = 10$ μm. The Dirac point was reached at −0.8 V, indicating the n-doping in these devices. Fig. 3.21c shows the corresponding transconductance. The embedded oxide capacitance of 0.6 μFcm^{-2} was estimated from separate capacitance-voltage measurements. The carrier density was then
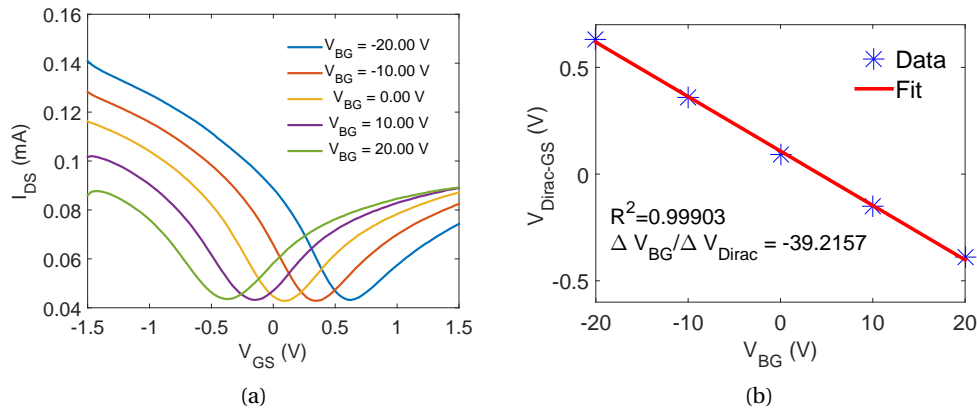
Figure 3.19: (a) Transfer characteristics of a 1 μm long and 20 μm wide GFET. The bottom-gate is swept between -20 V to 20 V in 10 V steps at V_{DS} = 10 mV; and (b) $V_{Dirac-GS}$ as a function of V_{BG}. The inverse of the slope $|\triangle V_{BG} / \triangle V_{Dirac-GS}| \sim 39.2$ has been obtained from a linear fit with an adequate R-squared value of 0.99.

calculated using the method discussed in the last section. Using the model [128], the hole and electron mobilities were found to be 760 and 2111 cm^{2}V^{-1}s^{-1}, respectively (Fig. 3.22). Interestingly, the extracted mobility for electron branch is higher, although, the extrinsic transconductance is higher for hole branch as can be observed from Fig. 3.21b. This is because the model used to extract mobility in Fig. 3.22 assumes higher series resistance in electron branch, which compensates for higher mobility value. The carrier mobilities in GFET can also be extracted from the peak-transconductance method [156]. The mobilities are calculated as $\mu_{FE} = (L/W).g_{m-peak}/(C_{OX}.V_{DS})$ where C_{OX} is the embedded oxide capacitance and g_{m-peak} is the maximum transconductance of the device in each branch. Using this method, the hole and electron mobilities — including the series resistance — are found to be 200 and 50 cm^{2}V^{-1}s^{-1}, respectively.

Compared to top-gated GFET, two direct observations can be found in the electrical characteristics of embedded gate GFET: (1) The overall mobilities values are lower. (2) The asymmetry between electron and hole conduction is higher. We believe that the main reason affecting the quality of graphene in the case of embbedded-gate GFET may be due to the slight gap between Au and SiO$_2$, as can be seen in Fig. 3.14a, which may have occurred due to the undercut profile expected from the bilayer resist. This gap might have led graphene to be suspended and possibly to break partly in subsequent process steps.

3.5 Summary

In summary, we introduced the essential device physics of GFETs; particularly, the drift-diffusion model of GFET was recalled which was also validated against the experimental data. We discussed the approach to simulate GFET and GFET based circuit in Agilent ADS
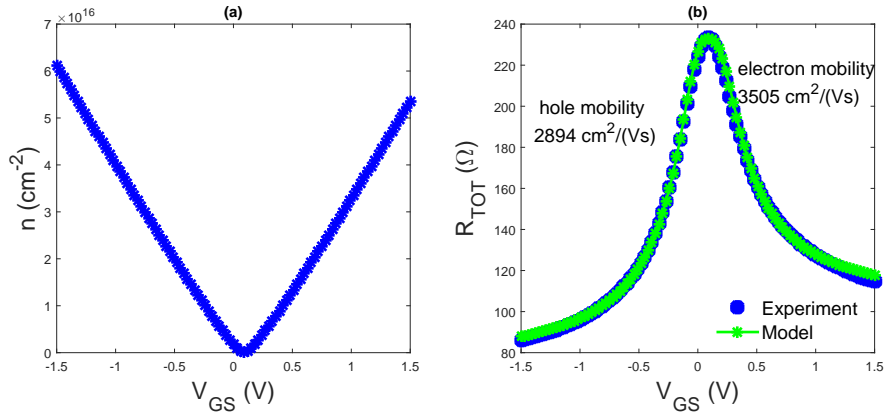
Figure 3.20: (a) Carrier density n; and (b) total resistance $R_{TOT} = V_{DS}/I_{DS}$ as a function of V_{GS} of a GFET from Fig. 3.18b. The blue curve shows the experimental data; the green curve shows the excellent theoretical model fitting for hole and electron branches.

which also takes into account various parasitic effects. The graphene synthesis approach was reviewed with the emphasis on CVD approach which was used for fabrication of devices in this PhD work. Further, we presented two techniques to fabricate GFETs: top-gated GFET and embedded-gate GFET. Compared to top-gated GFET, the embedded-gate GFET exhibited lower mobility, and higher asymmetry between electron and hole conduction. Thus, in the later chapters for NDR devices, we use top-gated GFET device and circuits based on them. This chapter includes the following original contributions:

- The drift diffusion model for the calculation of the dc and small-signal behaviour of GFETs has been recalled. Most importantly, we have included a correct modeling of the quantum capacitance and the carrier density, and have developed a framework for circuit simulation of GFETs which will be utilized in the next two chapters.
- Transfer of CVD-derived graphene has been carried out using wet chemical approach onto SiO_2/Si and embedded gate SiO_2/Si samples. Large-area graphene samples of sizes upto ~1.5 cm were transferred on 100 mm silicon wafer.
- Full fabrication of graphene devices (top-gated GFET and embedded-gate GFET) — from transfer of graphene to full circuit fabrication — has been performed in 100 mm fabrication facility.
- The embedded-gate GFET has been fabricated without the use of CMP. Compared to the CMP process, embedded gate transistors fabricated using our technique showed planar and clean surface for graphene deposition.
- Low field measurements of devices (top-gated GFET and embedded-gate GFET) have been performed. Various electrical parameters — such as carrier mobilities and contact resistances — have been extracted from the measurements; carrier mobilities exceeding 3000 cm^2/(Vs) have been obtained for top-gated GFETs.

(a)

(b)

(c)
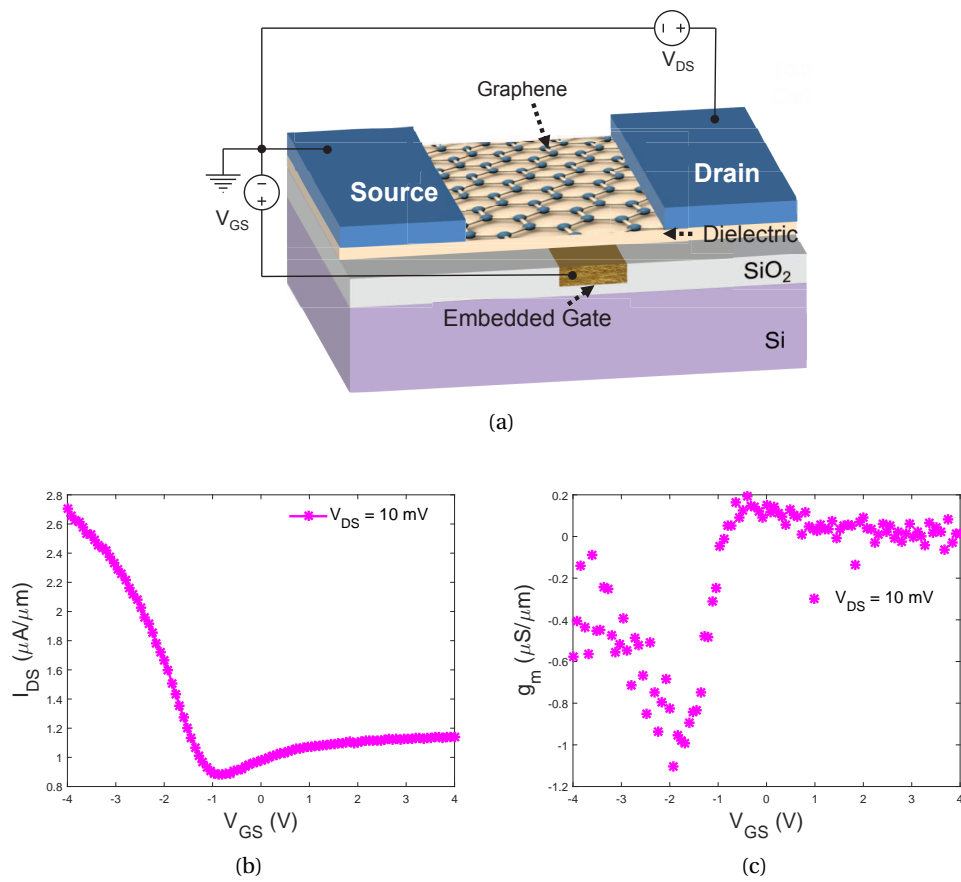
Figure 3.21: (a) Schematic of a embedded-gated GFET. (b) Transfer characteristics of the embedded gate GFET; and (c) corresponding transconductance.
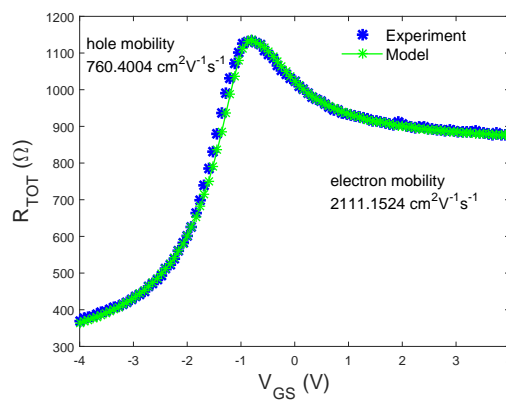
Figure 3.22: R_{TOT} as a function of V_{GS} for the GFET in Fig. 3.21b.

55

4 Negative Differential Resistance in Graphene Solid-State Devices

In this chapter, we discuss the negative differential resistance (NDR) in graphene solid-state devices which include single GFET, and circuit based on three GFETs. Before moving on to NDR based on graphene, in Section 4.1, we introduce the NDR phenomenon and its classification in general accompanied by the essential figures of merit to evaluate an NDR technology; and review recent research on NDR devices based on two-dimensional materials. In Section 4.2, we discuss the NDR in single GFET which include: rigorous experimental work with single GFET, whose channel lengths range between 200 nm and 5 μm and which conditionally show NDR; mechanism behind NDR in single GFETs; and the dependence of the NDR on the oxide thickness. In Section 4.3, we present a novel circuit consisting of three GFETs which shows enhanced NDR characteristics as compared to single GFET. Finally, we summarize our findings and conclude in Section 4.4.

4.1 Introduction

4.1.1 Negative Differential Resistance Phenomenon

Negative differential resistance (NDR) or negative differential conductance (NDC) is a phenomenon in which an increase in the applied voltage across the device's terminals results in a decrease in electric current through it for a certain applied bias range (Fig. 4.1). This appears to be in contrast to the Ohm's law, which states that the current increases proportionally to the the applied voltage. However, NDR phenomenon is not an analogue of Ohm's law; that is, it does not have a constant negative resistance over a arbitrarily wide range of voltage. In fact, NDR occurs over only in a limited portion of their voltage range; and in that limited portion, the ratio of a change in voltage to the resulting change in current dV/dI is negative. Besides, the devices in which this phenomenon occur are simply non-linear.

NDR phenomenon was first discovered in 1918 by Albert Hull at General Electric [157]; he discovered this phenomenon in vacuum tubes technology. Motivated by this discovery, many vacuum tube NDR devices have since then reported [158, 159, 160, 161]. Later, the invention of
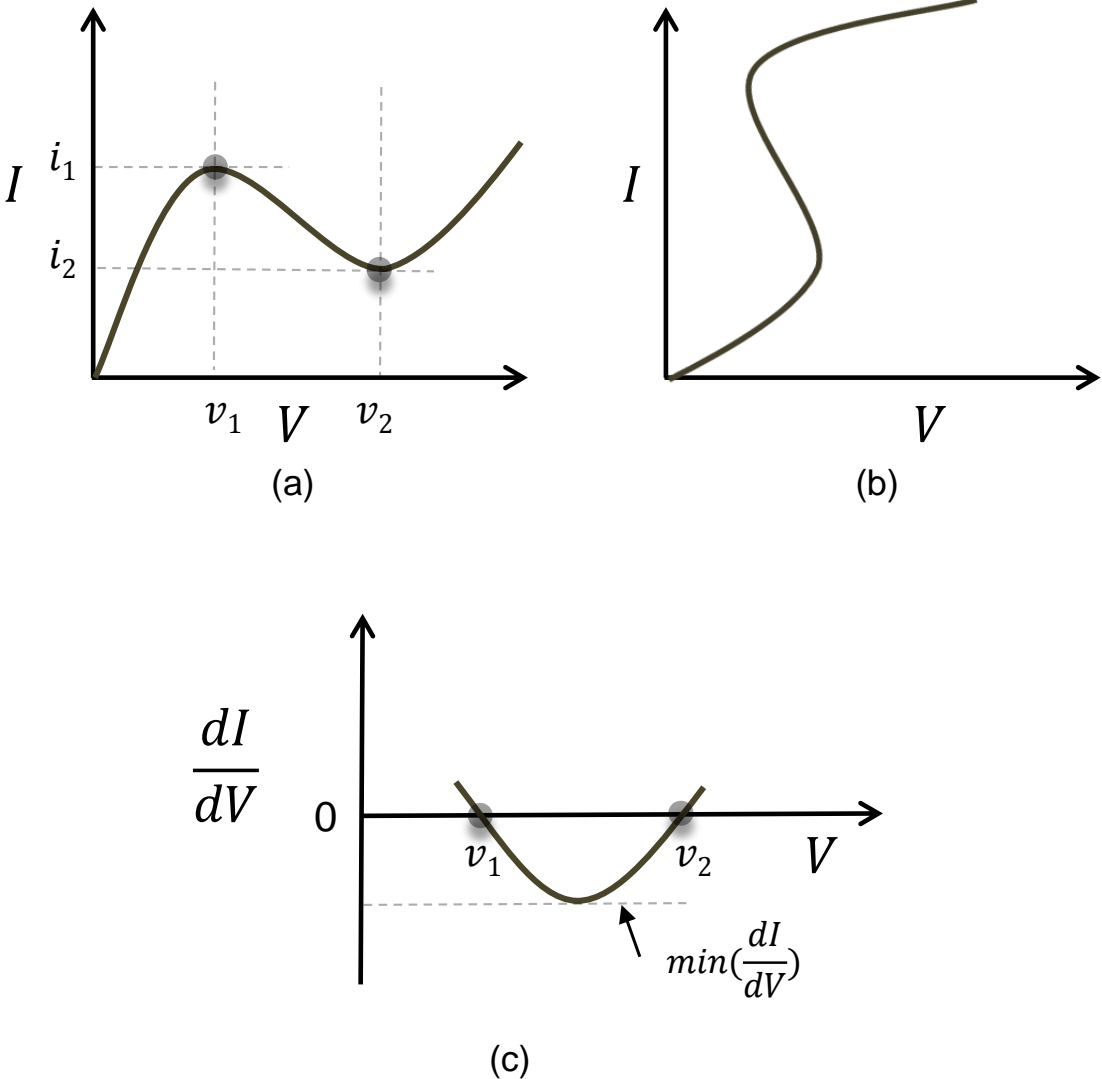
Figure 4.1: (a) $I - V$ characteristics of voltage-controlled N-shaped NDR device, and (b) current-controlled S-shaped NDR device. (c) dI/dV of (a).

solid-state transistors in 1948 triggered the search of NDR phenomenon in solid-state devices. It was not until 1958 before the the first solid-state NDR device, called the tunnel diode, was invented by Esaki [162]. For this discovery, Esaki was also awarded with Nobel Prize in Physics. Since then NDR has been observed in plethora of solid-state devices, and caused by several different mechanisms. The main impetus behind NDR's research over the years has been in its potential to be used in various RF and digital applications.

The most obvious RF application of NDR is the oscillator. In fact, Albert Hull, the inventor of NDR, first exploited this phenomenon to make electronic oscillator, known as dynatron oscillator [157]. As such many design approaches exist to make NDR oscillator. The simplest oscillator consists of an NDR device and a capacitor-inductor component [163, 164]. Another widely used application is reflection amplifiers which has the advantage of keeping power gain over broad frequency range [165, 163]. This application is discussed in the next chapter.

NDR phenomenon can also be exploited in various digital applications. As NDR devices produce oscillation between two states, it is possible to hold either state for some finite time to function as digital latches and memories [166]. It is also possible to construct the non-Boolean logic architecture exploiting NDR phenomenon using the principles of the non-linear networks [167]. Further, as certain NDR devices — such as GaAs based quantum well heterostructures [168] — manifest multiple NDR regions, they can be utilized to produce multiple-valued logics. This may result in highly dense devices and fewer circuit elements than prior generations of transistor-transistor logic (TTL), emitter-coupled logic (ECL), or CMOS logic. Multi-peak NDR devices also find applications in multiple-valued memories [169]. In addition, several other possible applications of NDR include mixers [170], multipliers [171], analog-to-digital converters [172], and binary- and ternary-adder circuits [173].

Broadly, NDR can be classified into two categories: voltage-controlled and current-controlled devices. In general, the voltage-controlled devices — such as tunnel diode [162], Gunn diode [174] — have N-shaped NDR (Fig. 4.1a), and the current-controlled — such as gas discharge tubes [175], IMPATT diode [176] — have S-shaped NDR (Fig. 4.1b). The NDR presented in this work is voltage-controlled N-shaped NDR.

4.1.2   Figures of Merit

To access the performance of NDR, specifically for the case of voltage-controlled N-shaped NDR devices (Fig. 4.1a), the following figures of merit (FOM) must be considered:

Peak-to-valley-current-ratio (PVCR) PVCR is defined as the ratio of peak current i_1 (onset of NDR) to the valley current i_2 (end of NDR) (Fig. 4.1a). For digital logic applications, a PVCR usually need not be more than 5 to 10 [177]. For large-scale memories, though, minimization of standby power consumption is critical and demands as high a PVCR as possible. A high PVCR is also needed for microwave oscillator applications.

Peak current density Peak current density is i_1 (Fig. 4.1a). High peak current density is

required in: (a) digital applications for NDR switches; (b) microwave applications for high speed and/or high power microwave oscillators [177].

Voltage range Voltage range is $v_2 - v_1$ (Fig. 4.1a). A wider voltage range is crucial for a good 1-dB compression point [178], an important performance metric for amplifiers.

NDC level The NDC level is defined as the maximum value of negative dI/dV value (or the $min(dI/dV)$) (Fig. 4.1c). The high NDC level is beneficial for the broadband reflection amplifier applications. Typically, the gain and bandwidth of amplifier depends upon how close is the negative resistance to the terminating impedance (usually $50\,\Omega$). Higher the NDC level, lower will be the negative resistance (closer to $50\,\Omega$), which eliminates the need of matching networks, and hence the reflection amplifiers with high gain over a broad frequency range can be demonstrated [179, 180].

Although widely reported, the FOM PVCR alone is not sufficient for evaluating an NDR technology. For usability in wide range of applications, a good NDR device — in addition to having a satisfactory PVCR — should also posses acceptable values of other FOMs such as voltage range, peak current density. For instance, room-temperature PVCR of 144 was demonstrated in resonant tunnel diode in ref [181]. However, although the PVCR value was very high, the voltage range over which it was valid was extremely small < 0.03 V. Let us imagine if this technology is used in reflection amplifier application. In RF amplifiers, a standard RF power level of −17 dBm is generally used which corresponds to a peak to peak voltage of 0.09 V (−0.045 to 0.045 V) in a $50\,\Omega$ system. Thus, if the NDR is only valid in a small region 0.03 V, and the voltage varies in this wide region of 0.09 V, then this NDR will be diminished (average value will be positive), and such technology will be impractical. Hence, a wide voltage range is equally important FOM for practical applications, which is neglected many times.

4.1.3   Negative Differential Resistance Based on 2-D Materials

Recently, there has been a great deal of interest in NDR devices using 2-D materials. In last 4 years, two types of NDR devices are being explored extensively in literature: (1) Planar transistors based on 2-D material such as mono- or bi-layer graphene, where current flows along the 2-D sheet parallel to the substrate surface [182, 167, 183, 184, 185, 186, 187, 188, 189] (Fig. 4.2a); and (2) vertical heterostructure transistors where current flows normal to the substrate surface [190, 191, 192, 193, 166, 194, 195, 196] (Fig. 4.2b). In the later case, the current at which NDR occurs is rather low ~ nA as the mechanism for current flow in these devices is tunneling. In the former case, particularly for graphene, the NDR occurs at high current levels ~ mA, as they take advantage of high mobility and saturation velocity of graphene. Thus, the planar graphene transistors are very interesting in various applications where high current density is required, and are presented in the this chapter.
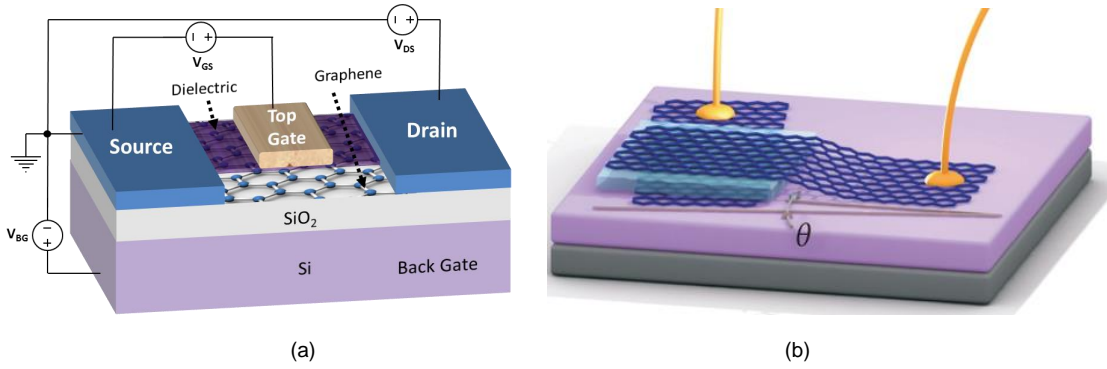
Figure 4.2: (a) Planar transistor based on graphene. (b) Vertical heterostructure transistor (adapted from [191]).

4.2 Negative Differential Resistance in Graphene Transistors

In this section, we report the observation of NDR in the output characteristics of monolayer graphene field effect transistor [184]. The ability to modulate the concentration of charge carriers via the electrostatic gate and the carrier-dependent saturation velocity at high fields are some of the unique properties of graphene. The NDR, as described in this section, stems from these effects.

4.2.1 Room-temperature high-field electrical measurements

Herein, we present NDR behavior under certain biasing conditions in GFETs fabricated using graphene grown by the CVD process (see Section 3.2.3). The GFETs, which are used in this work, employ a thin layer (~5 nm) of HfO_2 as a top gate dielectric, unless otherwise stated. A simplified sketch of the fabricated GFET is shown in Fig. 4.3a; the details of fabrication are described in Section 3.3.1. Fig. 4.3b shows the scanning electron micrograph (SEM) image of a well aligned device with gate length 500 nm and with 50 nm of ungated region between the gate and the source/drain. Short ungated regions and large widths reduce the series resistance. This is crucial for achieving measurable NDR, as discussed later. We present the room temperature measurement results of a similar device with a width of 30 μm. Measurements were carried out at room temperature using a HP 4145B Semiconductor Parameter Analyzer. Fig. 4.3c shows the device transfer characteristics at different back gate voltages V_{BG}. Using the procedure discussed in Section 3.4.2, the top gate equivalent oxide thickness (EOT) of 2.5 nm is estimated. Using the model [128], the hole and electron mobilities of the device are found to be 3525 cm^2/(V s) and 3082 cm^2/(V s), respectively (see Section 3.4.2 for detailed procedure).

Fig. 4.4a shows the output characteristics of the representative 500 nm gate length device. Under the bias $V_{BG} = -40$ V, $V_{GS} = -1.5$ V and $V_{SD} > 1.5$ V, we see a change in the monotony of drain current, resulting in NDR. Fig. 4.4b shows the corresponding differential conductance $g_{DS}(= dI_{SD}/dV_{SD})$ confirming the NDR region for $V_{SD} > 1.5$ V. As can be seen, the NDR is
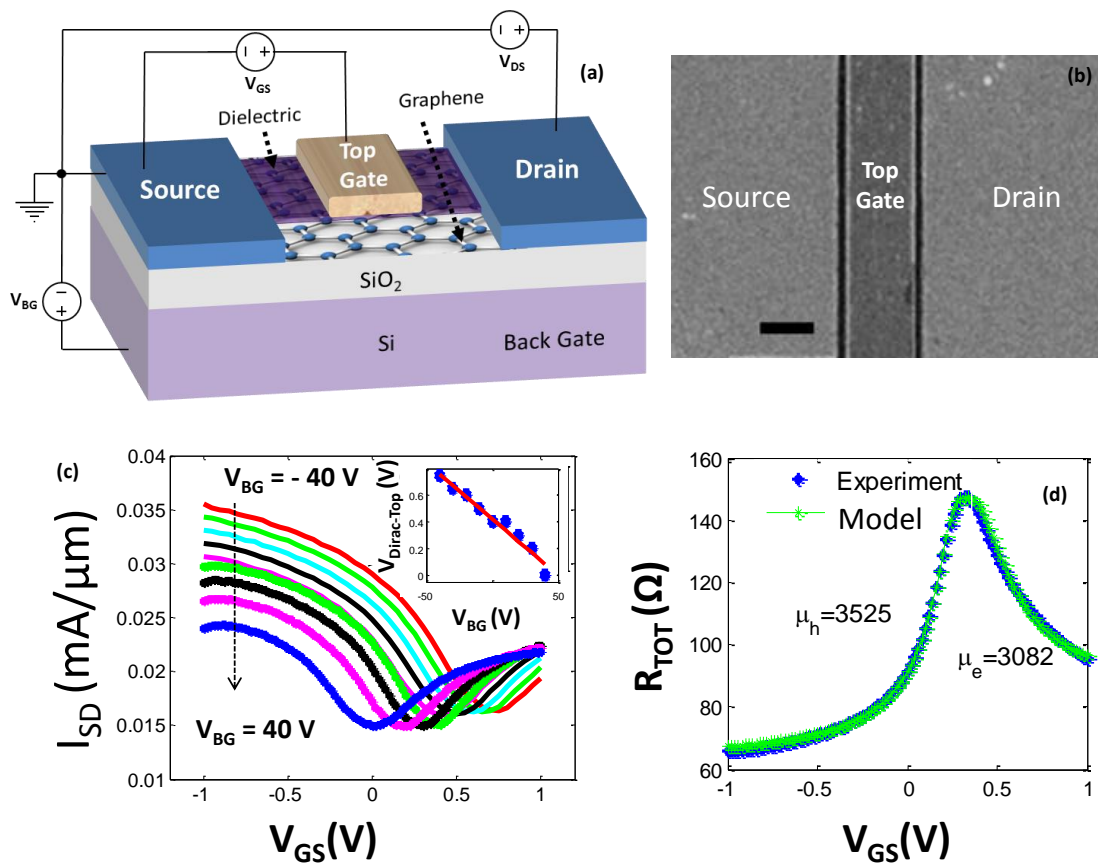
Figure 4.3: (a) Schematic of a GFET on Si/SiO$_2$ substrate, (b) top view SEM with 400 nm scale bar, c) transfer characteristics of a 500 nm long and 30 μm wide GFET. The bottom-gate is swept between -40 V to 40 V in 10 V steps at V_{DS} = 100 mV, and (d) total resistance of the same GFET under V_{DS} = 10 mV, V_{BG} = 0 V, and extracted mobilities of electrons and holes. The blue curve shows the experimental data; the green curve shows the excellent theoretical model fitting for hole and electron branches.
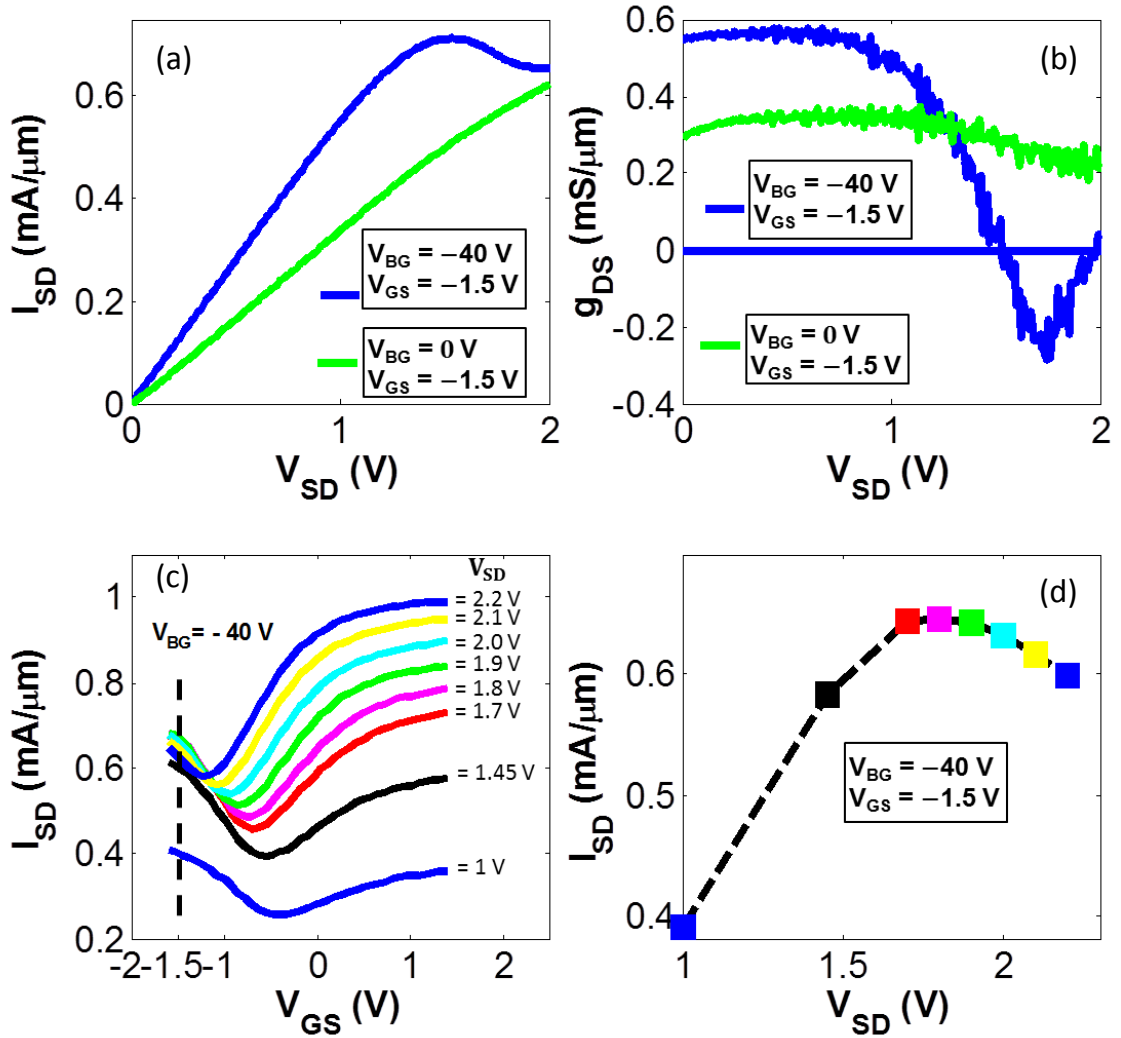
Figure 4.4: (a) Drain current (I_{SD}) as a function of source-drain voltage (V_{SD}) of a GFET with gate length $L = 500$ nm and width $W = 30$ μm at different top gate and back gate biases, (b) corresponding differential conductances (g_{DS}) as a function of V_{SD}, (c) transfer characteristics of the same GFET at different drain biases for $V_{BG} = -40$ V, and (d) I_{SD} as a function of V_{SD} obtained from the transfer characteristics for $V_{GS} = -1.5$ V.
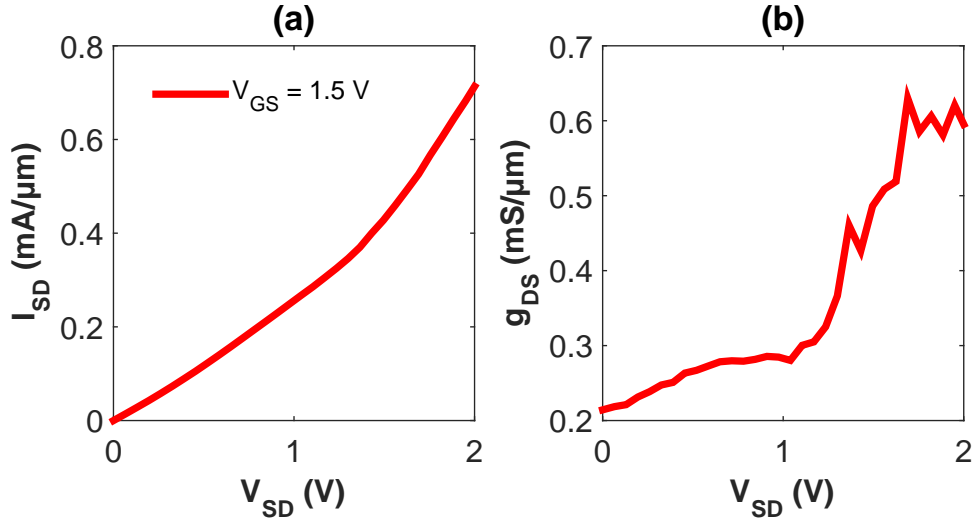
Figure 4.5: (a) I_{SD} as a function of V_{SD} of the GFET in Fig. 4.4 at $V_{BG} = -40$ V and $V_{GS} = 1.5V$, (b) corresponding differential conductance.

observed at $V_{BG} = -40$ V and not at $V_{BG} = 0$ V. This is mainly due to the lower series resistance at $V_{BG} = -40$ V than at $V_{BG} = 0$ V. The lower series resistance for $V_{BG} = -40$ V as compared to $V_{BG} = 0$ V is evident from the saturating current characteristics at high top gate voltages in the hole branch (Fig. 4.3c). A characteristic signature of NDR is reflected in its transfer characteristics at $V_{BG} = -40$ V shown in Fig. 4.4c. As source-drain voltage V_{SD} increases, the Dirac point shifts in the negative direction, ultimately leading to crossing of transfer curves in the hole branch. From the constant top gate voltage slice ($V_{GS} = -1.5$ V), the drain current is plotted for different V_{SD} in Fig. 4.4d showing the NDR characteristics.

Next we discuss the biasing conditions for achieving NDR. The GFET needs to be biased at a high $|V_{GS-eff}|$, and then the drain voltage should be swept so that the total number of carriers in the channel decreases. The local carrier density at a position x in the channel can be approximately expressed as $n(x) = |C_{TG-TOT}(V_{GS-eff}-V(x))/q|$ where C_{TG-TOT} is the total top-gate oxide capacitance and $V(x)$ is the potential in the channel which is zero at $x = 0$ and equal to V_{DS} at $x = L$. Therefore, to decrease $n(x)$, V_{DS} should be swept negatively (positively) if V_{GS-eff} is negative (positive). As illustrated in Fig. 4.4a, when the device was biased in negative V_{GS-eff}, NDR was observed for negative drain voltages. However, when V_{GS-eff} was positive, no NDR was observed for negative values of V_{DS} (Fig. 4.5a). This is because of the increase in the number of carriers in channel as V_{DS} increases negatively. This increase results in increasing g_{DS} (Fig. 4.5b) which goes against the NDR phenomenon.

Fig. 4.6 shows the output characteristics of several graphene devices with gate lengths from 200 nm to 5 μm, all exhibiting NDR. The NDR characteristics obtained for these devices were stable after repeating the measurements several times. Most of the devices showed NDR in the hole branch due to the higher hole mobility of the samples. However, Fig. 4.6f shows the NDR obtained, also, for positive V_{GS-eff} and positive drain voltages (electron branch) which
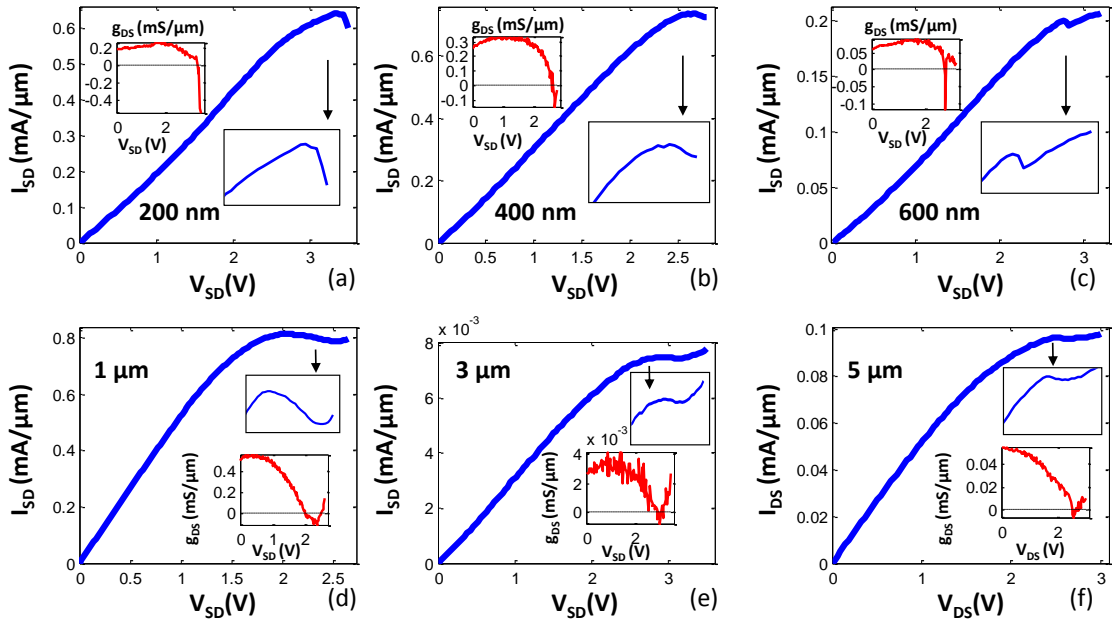
Figure 4.6: Drain current as a function of drain voltage and the corresponding differential conductance (g_{DS}) as a function of drain voltage in the inset for (a) $L = 200$ nm, $W = 19$ μm, at $V_{GS} = -3.2$ V, $V_{BG} = -40$ V; (b) $L = 400$ nm, W = 40 μm, at $V_{GS} = -2.3$ V, $V_{BG} = -40$ V; (c) $L = 600$ nm, W = 40 μm, at $V_{GS} = -3.5$ V, $V_{BG} = -40$ V; (d) $L = 1$ μm, W = 20 μm, at $V_{GS} = -1.7$ V, $V_{BG} = -40$ V; (e) $L = 3$ μm, W = 19 μm, at $V_{GS} = -3.5$ V, $V_{BG} = -40$ V; and (f) $L = 5$ μm, W = 19 μm, at $V_{GS} = 2.5$ V, $V_{BG} = -40$ V.

is yet another possible biasing condition to achieve NDR.

4.2.2   Mechanism

The mechanism behind NDR in GFETs has been discussed in ref [182] in which the explanation was mainly based on the evolution of charge carrier distribution in the channel. The key problem with this explanation, however, is that it does not take into account velocity saturation, which plays an important role in the high field transport of graphene. The drain current flowing in a transistor is the product of charge and velocity. Therefore, to explain any non-linearity in current characteristics, one must take both these quantities into account. In this subsection, we originally explain and demonstrate with systematic simulations that the main mechanism behind NDR is associated with the competition between the charge and velocity in the GFET.

To explain the mechanism behind the NDR phenomenon observed in our experiments, we use a standard drift diffusion model which was presented in Section 3.1. As can be seen from Eq. 3.6, the drain current depends on the carrier density and the drift velocity. We believe that NDR phenomena occur due to the competition between these two quantities. As drain voltage increases, the following happens: (1) The total number of carriers in the channel decreases if the GFET is biased appropriately as discussed previously, and (2) the drift velocity increases owing to the electric field increase. Effect 1 favors the NDR phenomenon, whereas effect 2 opposes it. At high drain voltages, however, v_{drift} saturates to v_{sat} which may further favor the NDR phenomena to occur. This effect is explained in the simulated characteristics below. Fig. 4.7a shows the simulated output characteristics for a 500 nm long device with parameters: EOT = 2.5 nm, $\hbar\Omega$ = 60 meV, μ_0 = 2000 cm^2/(V s), n_0 = 2.2 × 10^{11} cm^{-2} and $V_{Dirac-GS}$ = 0 V. The green curve with V_{GS} = −0.5 V, shows only positive values of g_{DS}, whereas the red curve with V_{GS} = −1 V exhibits NDR starting from V_{SD} = 0.86 V until V_{SD} = 1.12 V. We now focus on the contribution of effect 1 on the curves with NDR (red) and without NDR (green). A good indicator of total number of carriers in the channel is the average carrier density, defined as $< n > = 1/L \int_0^L n(x)dx$ and shown in Fig. 4.7b. As expected, the total carriers in the channel decreases initially with the drain voltage. For instance, the decrease in carriers for the red curve happens until V_{SD} = 1.45 V and then it increases again. It is interesting to note that the rate of decrease of carriers is the same for both red and green curves; however, the NDR was only seen for red curve. Therefore, it is also important to consider effect 2 which is about v_{drift}. As shown in Fig. 4.7c, v_{drift} initially increases due to electric field increase but then saturates to v_{sat}. Interestingly, we see that v_{drift} for the red curve is smaller than that of the green curve mainly around the range where NDR is observed. This can be explained by the carrier density dependent v_{sat} ($\propto 1/n$). At high V_{GS} = −1 V, there are more carriers in the channel than at V_{GS} = −0.5 V which means lower v_{sat} ($\propto 1/n$) and hence lower v_{drift} value for V_{GS} = −1 V. This is the main reason for the NDR to occur, that is, reduced drift velocity due to carrier density-dependent v_{sat} or, in other words, the lowering of the effective carrier mobility.
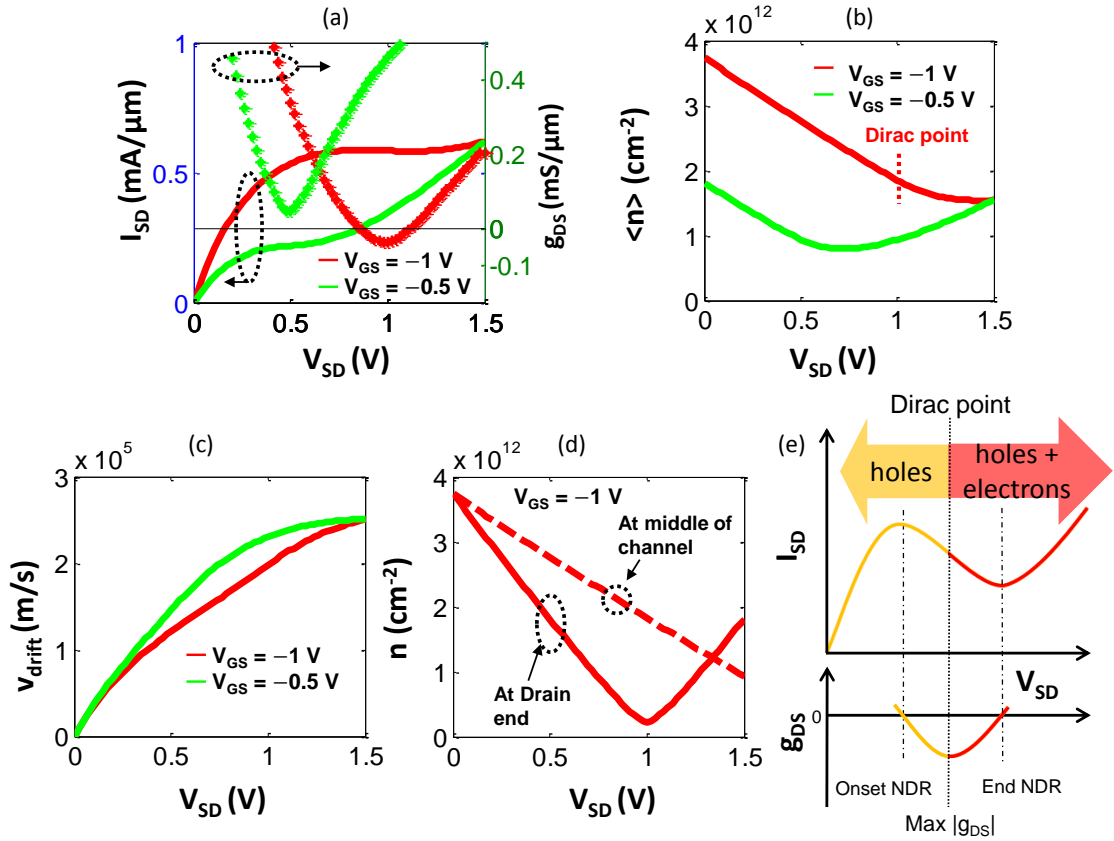
Figure 4.7: (a) Simulated drain current I_{SD} (solid line) as a function of source-drain voltage V_{SD} for $V_{GS} = -1$ V (red) and $V_{GS} = -0.5$ V (green) and corresponding g_{DS} (dotted line) as a function of V_{SD}. The gate length L is 500 nm and EOT is = 2.5 nm; (b) simulated average carrier density in the channel, $< n >$, as a function of V_{SD} for $V_{GS} = -1$ V (red) and $V_{GS} = -0.5$ V (green); (c) simulated drift velocity as a function of V_{SD}; (d) simulated carrier density, n, at drain end (solid line) and at the middle of channel (dotted line) as a function of V_{SD} for $V_{GS} = -1$ V; (e) simplified sketch of the mechanism of NDR. The orange shaded portion corresponds to the hole-dominated channel and the red shaded portion corresponds to the region when both electron and holes are present in the channel.

Further, it is interesting to note that the onset of NDR takes place in the unipolar region and before the Dirac point enters the channel. The Dirac point enters the channel when the drain voltage V_{SD} = 1 V (Fig. 4.7d), whereas the NDR starts at V_{SD} = 0.86 V (Fig. 4.7a). This is the another key indication that reduced v_{drift} is indeed the cause of NDR and not the change of carrier types [182]. In fact, it is observed that when the Dirac point enters the channel, the magnitude of NDR reaches its maximum (maximum negative g_{DS} point at V_{SD} = 1 V as shown in Fig. 4.7a). This can be explained by focusing on the red curve in Fig. 4.7b. After V_{SD} = 1 V, electrons enter the channel (Dirac point highlighted in Fig. 4.7b). However, the decrease in the total number of carriers continues beyond V_{SD} = 1 V. This decrease in total carriers in the channel is solely attributed to electrons (minority carriers in channel) replacing holes (majority carriers in channel) with lower carrier density. Interestingly, this decrease is slower than the decrease observed below V_{SD} = 1 V (from 0 to 1 V) as can be seen clearly in Fig. 4.7b. This slower decrease is the cause of decrease in magnitude of negative g_{DS} after the Dirac point enters the channel. In addition, the NDR region continues until V_{SD} = 1.12 V and not until the Dirac point reaches the middle of the channel [182] which happens at much higher V_{SD} > 1.5 V (Fig. 4.7d). In summary, the relation between the position of the Dirac point entering the channel and the NDR region is illustrated in Fig. 4.7e.

Though the interplay between carrier density and drift velocity in GFETs is the main cause of NDR, other high field effects such as self-heating can also favor NDR [188]. Self heating effects nevertheless play minimal role in GFETs of shorter channel lengths (< 500 nm) or in GFETs which are fabricated on thin supporting insulators [197]. Under similar biasing conditions discussed in the last section, we observed NDR (i) in devices with shorter channel lengths (Fig. 4.6), and (ii) in devices fabricated on thin supporting insulator (black curve in Fig. 4.11b shows NDR in GFET fabricated on 90 nm SiO_2/Si).

4.2.3   Top-Gate Oxide Thickness Dependence

Here we demonstrate the dependence of the NDR phenomena on the top-gate dielectric thickness. Han *et al.* [183] rightly pointed out that as EOT scales down, the drop of carrier density versus drain voltage increases; that is, the fast drop in carrier density helps the saturation phenomena to occur. This can also be correlated to the NDR phenomena. Fig. 4.8a shows the simulated average carrier density < n > normalized to its value at V_{SD} = 0 V as a function of V_{SD} for different thicknesses of EOT. Clearly, as EOT increases, the rate of drop in the carrier density versus V_{SD} decreases and this does not favor the NDR phenomena. However, NDR may still be observed for higher EOTs with the help of reducing the v_{drift} (effect 2), that is, either by applying a high gate voltage or if the samples have a lower v_{sat} value. As it can be seen in Fig. 4.8b, NDR was experimentally observed for a device with larger EOT ~ 12 nm (15 nm Al_2O_3) and with lateral dimensions the same as our central geometry (L = 500 nm, W = 30 μm). A comparison of results of the two EOTs reveals two expected points. First, the NDR for EOT = 12 nm occurs at higher gate voltage as compared with the NDR for EOT = 2.5 nm as shown in Fig. 4.8b. Second, the magnitude of maximum negative g_{DS} is lower for the higher
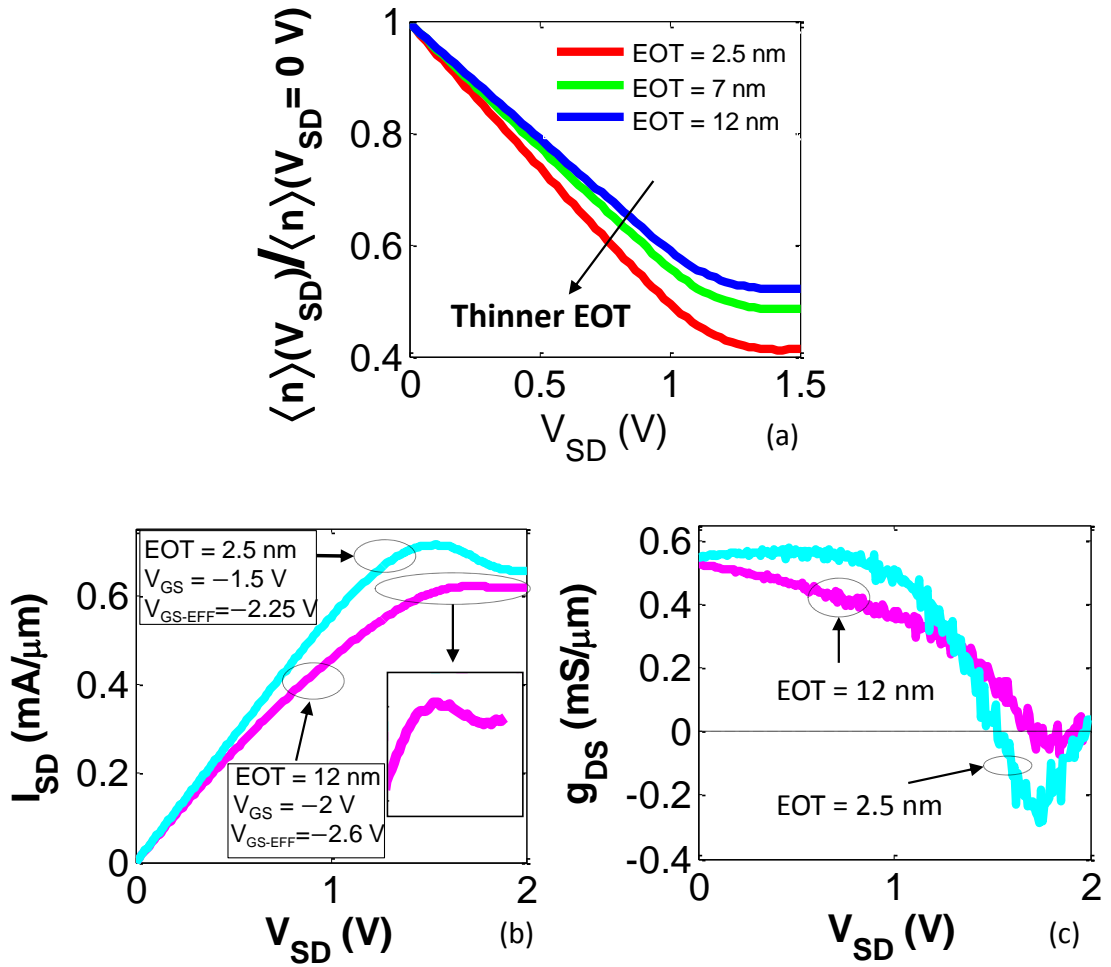
Figure 4.8: (a) Simulated average carrier density $< n >$ normalized to it value at $V_{SD} = 0$ V as a function of V_{SD} for 500 nm GFET with EOT 2.5, 7, and 12 nm at $V_{GS} = -1$ V. (b) Measured I_{SD} versus V_{SD} for two EOTs with gate length $L = 500$ nm and $W = 30$ μm at bias voltages $V_{BG} = -40$ V. The $V_{Dirac-GS}$ (at $V_{BG} = -40$ V) values for EOT = 2.5 nm and EOT = 12 nm were 0.75 and 0.6 V, respectively. (c) Corresponding measured g_{DS} versus V_{SD} characteristics.

EOT, as can be seen in Fig. 4.8c, which is also in accordance with the higher relative decrease of the average carrier density of the channel for the smaller EOTs as shown in Fig. 4.8a.

4.3 Negative Differential Resistance in 3-Transistor Graphene Circuit

Although the NDR in the output characteristics of single GFET (1-GFET) — as discussed in the previous section — occurs at high current density, thanks to the high current carrying capability of graphene, the PVCR and the NDC level are quite low which may not be high enough for applications. In this section we propose a novel graphene NDR (GNDR [1]) circuit consisting of three GFETs, which includes a two GFET inverter connected in a feedback loop with the main GFET in which the NDR is realized. The proposed circuit shows significant performance improvement over NDR based on 1-GFET; it shows stronger NDR, higher PVCR, wider voltage range over which NDR is valid, and higher tunability, as compared to that of 1-GFETs. NDR based on circuit topologies, involving more than one transistor, have also been reported in past for Si-based devices [198].

4.3.1 Operation Principle

Fig. 4.9 illustrates our proposed 3-GFET circuit and its operating principle exploiting some unique properties of GFETs. Let us consider a GFET FET1, as shown in Fig. 4.9a. The necessary condition to achieve NDR in GFET is to bias it in such a way so that the total number of carriers in the channel decreases as drain-source voltage (V_{DS}) increases (Section 4.2.1). This can be achieved by biasing the GFET at some constant high effective gate voltage (V_{GS-eff}), and sweeping V_{DS} positively (if V_{GS-eff} is positive) or negatively (if V_{GS-eff} is negative). The ability to achieve a good NDR depends on how fast the carriers are depleted in the channel. We have shown in Fig. 4.8a that the carriers are depleted faster by the applied drain voltages in devices with aggressively scaled oxide thickness. Now one may ask: "For given oxide thickness, how the carriers can be depleted faster?" This can be achieved if V_{GS} is also made to vary when V_{DS} is increasing. Fig. 4.9b shows the average carrier density versus the drain voltage for both a constant and a varying value of the gate bias. To achieve an NDR effect in practice, a GFET inverter is connected between the drain and the gate terminals of FET1 as depicted in Fig. 4.9c. The inverter consists of FET2 and FET3. The complementary nature between the GFET pairs is uniquely achieved by the drain bias-induced splitting between the Dirac point voltages of FET2 and FET3, and not by any technological doping of graphene[199, 200, 201].

---

[1]The terms "GNDR circuit", "3-GFET NDR circuit", "three-GFET NDR circuit", and "3-transistor graphene circuit" are used interchangeably. All refer to the circuit comprising of three GFETs exhibiting NDR.
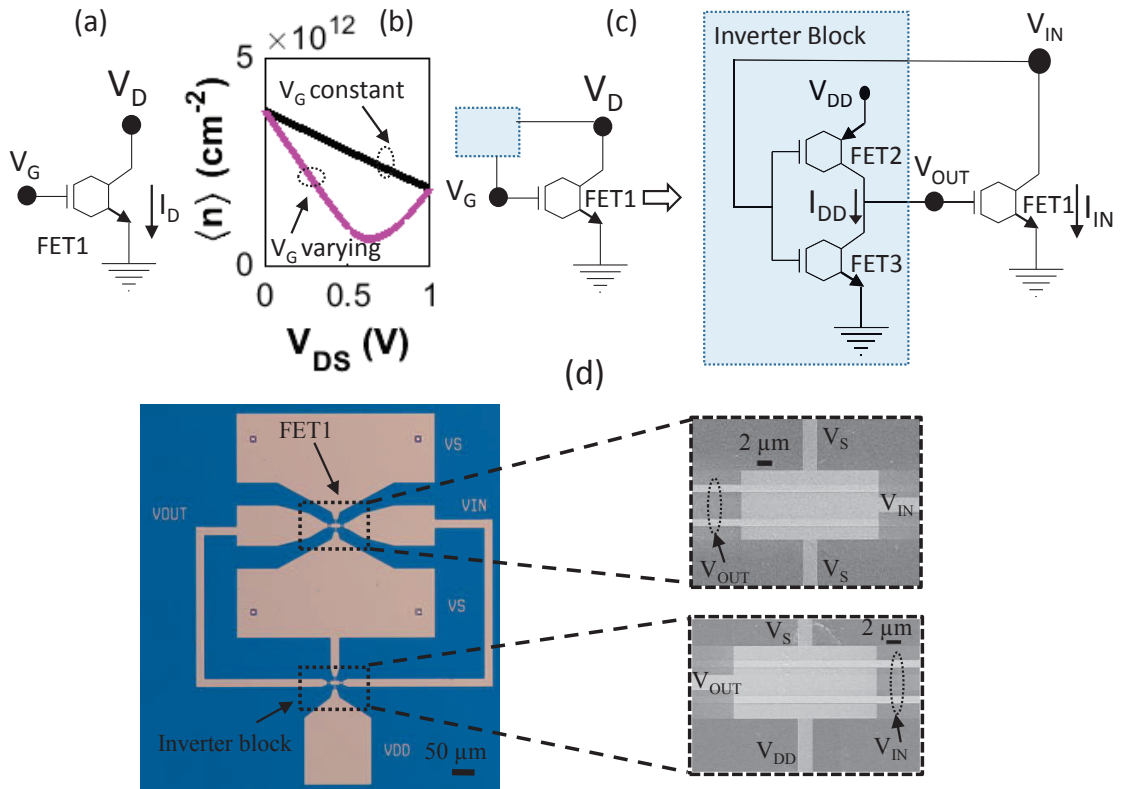
Figure 4.9: (a) Schematic symbol of GFET FET1. (b) Simulated average carrier density ($<n>$) versus V_{DS} with constant $V_{GS} = 1$ V and varying V_{GS} ($V_{GS} = 1 + (-1)V_{DS}$). The simulated channel length is 1 μm. All other parameters of simulation are same as done for Fig. 4.7b of Section 4.2.2). (c) Proposed 3-GFET NDR circuit. (d) Optical micrograph of the fabricated circuit (Left) and corresponding scanning electron micrograph on the zoomed portions (Right).
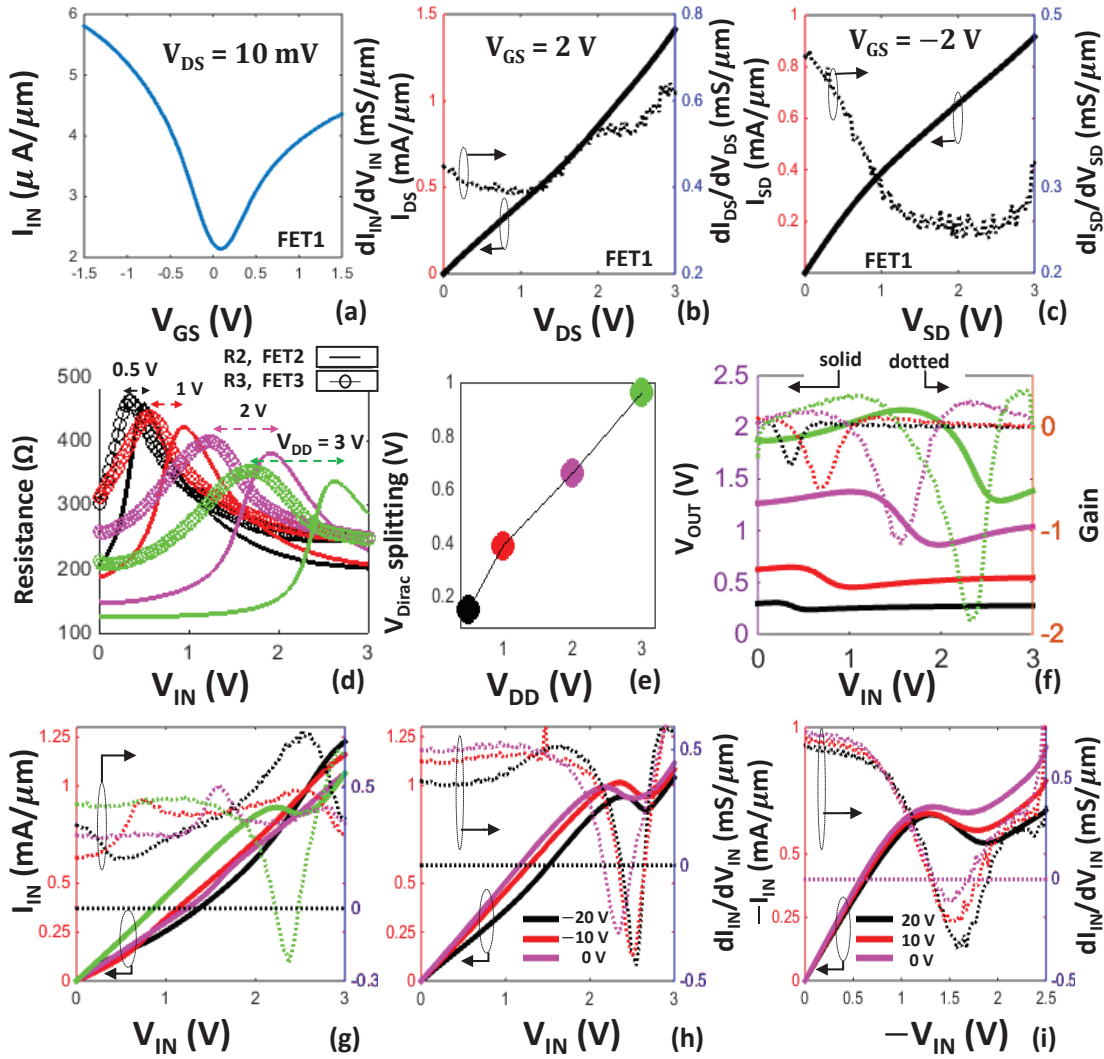
Figure 4.10: (a) Transfer characteristics of FET1 at $V_{BG} = 0$ V. (b) Output I_{DS} versus V_{DS} for FET1. (c) Output I_{SD} versus V_{SD} for FET1. Right axis of b, c shows their corresponding differential conductances. (d) Resistance versus V_{IN} for different values of V_{DD}. (e) The Dirac point splitting between FET2 and FET3 as function of V_{DD}. (f) V_{OUT} and gain of the inverter block as function of V_{IN} for different V_{DD}. (g) I_{IN} and dI_{IN}/dV_{IN} versus V_{IN} for different V_{DD}. (h) I_{IN} and dI_{IN}/dV_{IN} versus V_{IN} for different values of V_{BG} at $V_{DD} = 3$ V. (i) Negative I_{IN} and dI_{IN}/dV_{IN} versus negative V_{IN} for different values of V_{BG} at $V_{DD} = -3$ V.

4.3.2 Measurement Results

The GFETs utilizes CVD graphene which was transferred on 90 nm SiO_2/Si substrate. The process flow to fabricate GFET circuits is described in Section 3.3.1. The optical image of the proposed circuit is shown in Fig. 4.9d. The transistor FET1 is 1 μm long and 20 μm wide, while FET2 and FET3 are 1 μm long and 10 μm wide. The devices employ 5 nm of ALD HfO_2 (with thin layer of oxidized Al), as a top gate dielectric, unless otherwise stated. The top-gate equivalent oxide thickness (EOT) is evaluated to be approximately 2.3 nm, and the mobility of 3505 $cm^2V^{-1}s^{-1}$ for electrons and 2894 $cm^2V^{-1}s^{-1}$ for holes are estimated (Fig. 3.20b). All the measurements are carried out at 300 K.

The transfer characteristics of the FET1, measured independently, is shown in Fig. 4.10a. The device exhibits the expected ambipolar behavior. The output characteristics of FET1 at constant value of V_{GS}, for both electron-dominated (positive V_{DS} and positive V_{GS-eff}) and hole-dominated (negative V_{DS} and negative V_{GS-eff}) branches, exhibits no NDR behavior as shown in Fig. 4.10b and 4.10c, respectively. We now characterize the full circuit by connecting the FET1 to the inverter block. The operation principle of the inverter block is based on the work by ref[199] where the complementary configuration between the GFET pairs was achieved through potential superposition effect from the drain bias. The resistance of the transistors FET2 and FET3 are, respectively given as, $R_2 = (V_{DD} - V_{OUT})/I_{DD}$ and $R_3 = V_{OUT}/I_{DD}$, where V_{DD} is the supply voltage of the inverter block, I_{DD} is the current flowing in the inverter block and V_{OUT} is the output voltage of the inverter block as depicted in Fig. 4.9c. Fig. 4.10d shows these measured resistances versus V_{IN} for different values of V_{DD}. As V_{DD} increases, the splitting between the Dirac point voltages of FET2 and FET3 increases (Fig. 4.10e). At V_{DD} = 3 V, a high gain (~2) is then achieved within the region of Dirac point splitting (Fig. 4.10f). As a result in this region, $V_{OUT}(= V_{DD}R_3/(R_2 + R_3))$, which also acts as the gate voltage of FET1, decreases from 2.1 V to 1.3 V. This decrease in the gate voltage of FET1, as its drain voltage increases, results in the faster decrease of the total carriers in the channel, which favors NDR. Consequently, NDR is observed in the output characteristics of FET1 (I_{IN} versus V_{IN}) for V_{DD} = 3 V as shown in Fig. 4.10g. This figure also shows the corresponding differential conductance, dI_{IN}/dV_{IN} showing negative values for V_{DD} = 3 V, confirming the NDR behavior.

Fig. 4.10h shows the tuning ability of back gate bias voltage (V_{BG}) to modulate the NDR characteristics. As V_{BG} varies from 0 to −20 V, the gain of the inverter block increases which improves the NDC level; that is, the magnitude of maximum negative dI_{IN}/dV_{IN} increases. Fig. 4.10i shows the similar performances obtained for the hole-dominated branch (negative V_{IN} and V_{DD}= −3 V), which is another way to decrease the carriers in the channel [184]. The PVCR value of 1.21 and NDC level of 0.43 mS/μm is obtained for this device. The highest achieved PVCR of value 2.2 and NDC level of value 2.1 mS/μm has been obtained for a different device with dimensions (400 nm long FET1, 500 nm long FET2 and FET3, EOT ~ 12 nm), as shown in Fig. 4.11a, using the proposed operation of 3-GFET NDR circuit.

We now demonstrate that our proposed circuit can also be used to enhance NDR in the GFETs
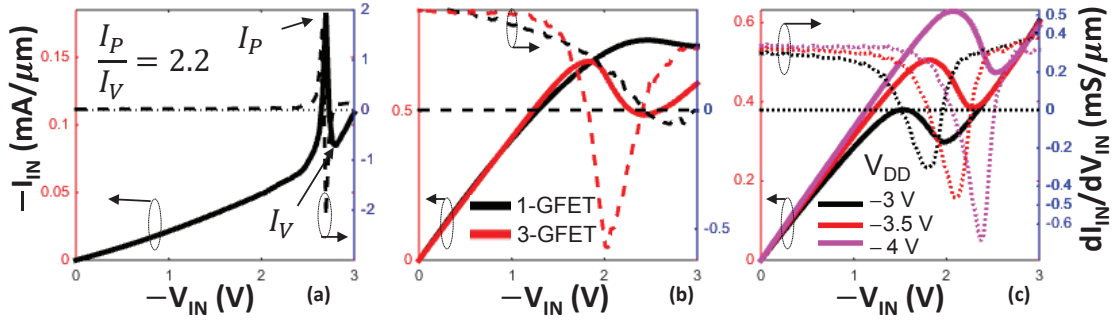
Figure 4.11: (a) NDR characteristics for the device with dimensions: FET1 is 400 nm long and 40 μm wide while FET2 and FET3 are 500 nm long and 5 μm wide each. Top gate oxide: 15 nm of Al_2O_3. (b) Comparison of output characteristics of FET1 operated in 1-GFET (black) and 3-GFET NDR circuit (red) configurations. FET1 is 3 μm long and 19 μm wide. For the black curve, i.e., 1-GFET, $V_{GS} = -1.5$ V and $V_{BG} = -20$ V; for the red curve, i.e., 3-GFET circuit, $V_{DD} = -4$ V and $V_{BG} = -20$ V. The 3-GFET circuit is driven by the inverter whose dimensions are L = 1 μm, 9.5 μm each for FET2 and FET3. (c) NDR characteristics of the same 3-GFET device as in (b) for different V_{DD} at $V_{BG} = 0$ V. Left axis in a-c shows negative I_{IN} versus negative V_{IN} whereas the right axis shows dI_{IN}/dV_{IN} versus negative V_{IN}.

which already show NDR in their output characteristics. The black curve in Fig. 4.11b shows the NDR obtained in the output characteristics of one such GFET ($L = 3$ μm, $W = 19$ μm) at a constant $V_{GS} = -1.5$ V. When operated in the 3-GFET NDR circuit configuration, the same device shows much stronger NDR (Red curve): the PVCR is improved from 1.03 to 1.37; whereas the NDC level is increased from 59.5 μS/μm to 579 μS/μm, an increase by almost an order of magnitude. Fig. 4.11c shows the ability of the terminal V_{DD} to tune NDR; changing V_{DD} from -3 V to -4 V more than doubles ($\times 2.3$) the NDC level (from 305 μS/μm to 686 μS/μm).

4.3.3 Discussion

Table. 4.1 compares essential FOMs obtained for 3-GFET NDR circuit with some other reported NDR technologies. Despite its increased area of implementation (requiring 3 transistors), 3-GFET NDR circuit comes with several unique advantages. For instance, the peak current density achieved in this work is > 1 mA/μm; this is much higher than that obtained using recent vertical heterostructure transistors[190, 191, 166]. In addition, the 3-GFET NDR circuit offers wide voltage range operation over which NDR is valid, up to 0.6 V achieved in this work. A wider voltage range is crucial for a good 1-dB compression point [178], an important performance metric for amplifiers.

Furthermore, there is a much room for performance improvement in the proposed circuit. As the NDR performance of 3-GFET NDR circuit is directly related to the gain of the inverter block, improving the gain would improve the overall NDR performance. Scaling the oxide thickness, reducing the series resistance, and cascading inverter blocks can be some of the techniques

Table 4.1: Comparison of FOMs for NDR technologies at 300 K.

Technology	PVCR	Voltage range (V)	Peak current density
Esaki diode [202]	16	0.38	92 μA/μm^2
Resonant tunnel diode [181]	144	0.03	1 μA/μm^2
Si/SiGe tunnel diode [203]	5.2	0.3	2.8 μA/μm^2
Molecular junction [204]	1.5	0.3	0.16 μA/μm^2
Graphene-BN tunnel FET [190]	1.38	0.32	0.153 μA/μm^2
1-GFET (Section 4.2 [184])	1.07	0.45	0.7 mA/μm
3-GFET (This section [186])	2.2	0.6	1.01 mA/μm

for improving the gain [200] and consequently for enhancing the NDR performances. It is also worth mentioning that our 3-GFET NDR circuit, once encapsulated in a package, acts just like any other three-terminal NDR device. The third terminal V_{DD} can be regarded as the terminal which provides the tuning ability to NDR. The ability of V_{DD} to tune the NDC level in 3-GFET NDR circuit (up to ×2.3) is much higher than the tunability provided by gate terminal in 1-GFET NDR [182].

As previously mentioned, NDR based on circuit topologies has also been demonstrated in past by silicon MOSFETs. The difference graphene brings here is in its potential to exhibit NDR at current levels higher than silicon, because of its higher mobility and saturation velocity. Additionally, for the first time, such topologies that produce NDR are introduced in an all-graphene embodiment, exploiting its unique advantages such as the capability to offer inverters with two identical devices by drain bias-induced Dirac point splitting effect. This allows fabricating inverters without any doping steps. Our experimental work moves along the direction which demonstrates that similar mature silicon based circuits and technologies can be introduced to graphene, and possibly can be done for other two-dimensional materials such as MoS$_2$, phosphorene [17], which keep the advantage of having higher bandgap similar to silicon.

4.4 Summary

In this chapter, we explored experimentally and theoretically the potential of graphene in NDR devices. It has the clear advantage of exhibiting NDR at high current levels as compared to any other technologies, thanks to its high mobility and saturation velocity. We first reported the room-temperature observation of NDR in top-gated GFET under of various gate lengths and dielectric thickness's. The mechanism behind NDR was also explained in detail using the standard drift diffusion model. The main conclusion is that the NDR occurs due to the competition between two core quantities in GFET: the total number of carriers in the channel and their drift velocity. Further, it was analysed with simulations and demonstrated experimentally that lower EOTs provide a higher NDR level. Next, we demonstrated a novel 3-GFET circuit showing enhanced NDR at room-temperature. The NDR characteristics was also highly tunable with voltage. The 3-GFET circuit was fabricated from wafer-scale CVD monolayer graphene

and included an inverter which was realized without any external technological doping step. Therefore, the proposed approach also enables the integration of such graphene NDR devices with silicon-based circuits in future. The successful demonstration of NDR using large area graphene grown from CVD opens up an alternative route in the field of graphene research particularly for its utilization in key applications such as oscillators, amplifiers, memories, and fast switches.

This chapter includes the following original contributions:

- We demonstrated experimentally the observation of NDR in dual-gated GFETs at room temperature for various channel lengths, scaling down from 5 μm to 200 nm.
- We originally explained and demonstrated with systematic simulations that the onset of NDR occurs in the unipolar region itself and that the main mechanism behind NDR is associated with the competition between the specific field dependence of carrier density and the drift velocity in GFET.
- We demonstrated experimentally and theoretically the dependence of the NDR level on the oxide thickness. To the best of our knowledge this is the first work that studies this.
- We proposed and experimentally demonstrated a novel circuit based on GFETs showing excellent NDR characteristics at room temperature. The circuit showed negative differential conductance (2.1 mS/μm) that is almost an order of magnitude better than NDR based on 1-GFET. This conductance level was uniquely tunable ($\times$2.3) with the supply voltage as well as with the back bias voltage. It also exhibited improved peak-to-valley current ratio (PVCR) (2.2) and wide voltage range (0.6 V) over which NDR is valid.

5 Reflection Amplifiers based on Graphene Negative Differential Resistance Solid-State Devices

In this chapter, we begin with an overview of reflection amplifiers including its theory of operation (Section 5.1-5.2). Next we consider the use of planar graphene solid-state devices, which was discussed in the last chapter, in reflection amplifier application. We present the rigorous simulation of 1-port reflection amplifier based on 1-GFET and 3-GFET circuit in Section 5.3 and 5.4, respectively. We also present the RF measurements of 3-GET graphene circuit in Section 5.5; this serves as an experimental evidence that the reflection amplification occurs in proposed 3-GET graphene circuit. Finally, we summarize the results in 5.6.

5.1   Introduction: Reflection Amplifiers

The basic problem of the small-signal microwave transistor amplifiers — such as FET amplifier which exploits its transconductance for amplification — arise at higher frequencies when the gains are substantially reduced. As a result, they require multiple amplification stages; for example, reception of RF signals at 100 GHz requires a 20-dB gain amplifier which consists of more than 4 amplification stages [205]. Multi-stage amplifier consisting of more than 4 stages suffers from higher noise, are bigger in size, and are expensive than the single-stage counterpart [205, 206]. Reflection-type amplifiers based on NDR devices provide means to overcome these problems specially for amplifiers with input signals of a very low level.

Because of their broadband amplification capabilities and low-noise properties, many NDR devices — such as Gunn and Impatt diodes, pseudomorphic MODFET's, silicon bipolar transistors, superlattice structures [207, 180, 165, 208] — have been utilized in reflection amplifiers over the years. Reflection amplifiers are used in radar applications [209, 210] and in low cost RFID sensors operating at millimetre-wave frequencies where the sensors can be physically very compact. They also have the application in the construction of retro-directive arrays based on bi-directional amplifiers [211].

5.2 Theory of Operation

The operating principle of reflection-type NDR amplifier is illustrated in Fig. 5.1. When a two terminal NDR device is operated in CPW configuration and biased in the NDR region, the real part of complex impedance Z_{OUT} seen across its terminal is negative. Under these conditions, if the terminating impedance Z_L is properly adjusted, the magnitude of reflection coefficient S_{11} is greater than unity and the circuit becomes an amplifier with a gain of

$$S_{11} = \frac{Z_{OUT} - Z_L}{Z_{OUT} + Z_L}. \tag{5.1}$$

In other words, the NDR device sends back an amplified signal — which is the reflected wave — back to the incident power source. Thus, in a practical amplifiers, a circulator [212] is used to separate incident and reflected waves; the schematic diagram including the circulator is shown in Fig. 5.2. The matching network (or transforming network) is an optional component which can be included to give the required gain and bandwidth characteristics. In this chapter, we will discuss reflection amplifiers without the use of circulator.

Coming back to Eq. 5.1, for reflection amplification, the magnitude of the real part of Z_{OUT} should be kept greater than the terminating impedance Z_L. The condition for stability can thus be written as

$$|Re(Z_{OUT})| > Z_L \tag{5.2}$$

5.3 Simulation of 1-GFET NDR Reflection amplifier

Fig. 5.3 shows the equivalent circuit diagram of reflection amplifier based on 1-GFET. The NDR characteristics of GFET has been discussed in great detail in Section 4.2. Since GFET is a three-terminal device, it can be implemented in the two-port coplanar waveguide configuration. The NDR is seen in its port 1 (drain-source) while the port 2 (gate-source) is terminated with source impedance Z_S. The method of simulating the GFET circuit in Agilent ADS is elucidated in Section 3.1. The Z-parameters of the GFETs are first calculated including the parasitic effects. The output impedance seen into the drain terminals can thus be written as

$$Z_{OUT} = Z_{11} - \frac{Z_{12} Z_{21}}{Z_{12} + Z_S}. \tag{5.3}$$

The reflection gain can then be calculated from Eq. 5.1. Using the calibrated model presented in Section 3.1 and the parameters of simulation in Table. 5.1, the output characteristics showing NDR are plotted in Fig. 5.4a for the GFET with dimensions $L = 1\ \mu$m, $W = 10\ \mu$m. The full circuit, as shown in Fig. 5.3, is then simulated taking into account the parasitic series resistances and capacitances (Table. 5.1). The gate-source port is terminated with $Z_S = 50\ \Omega$, which is just an arbitrary choice.

When this GFET is biased at the voltage corresponding to maximum negative intrinsic g_{DS},
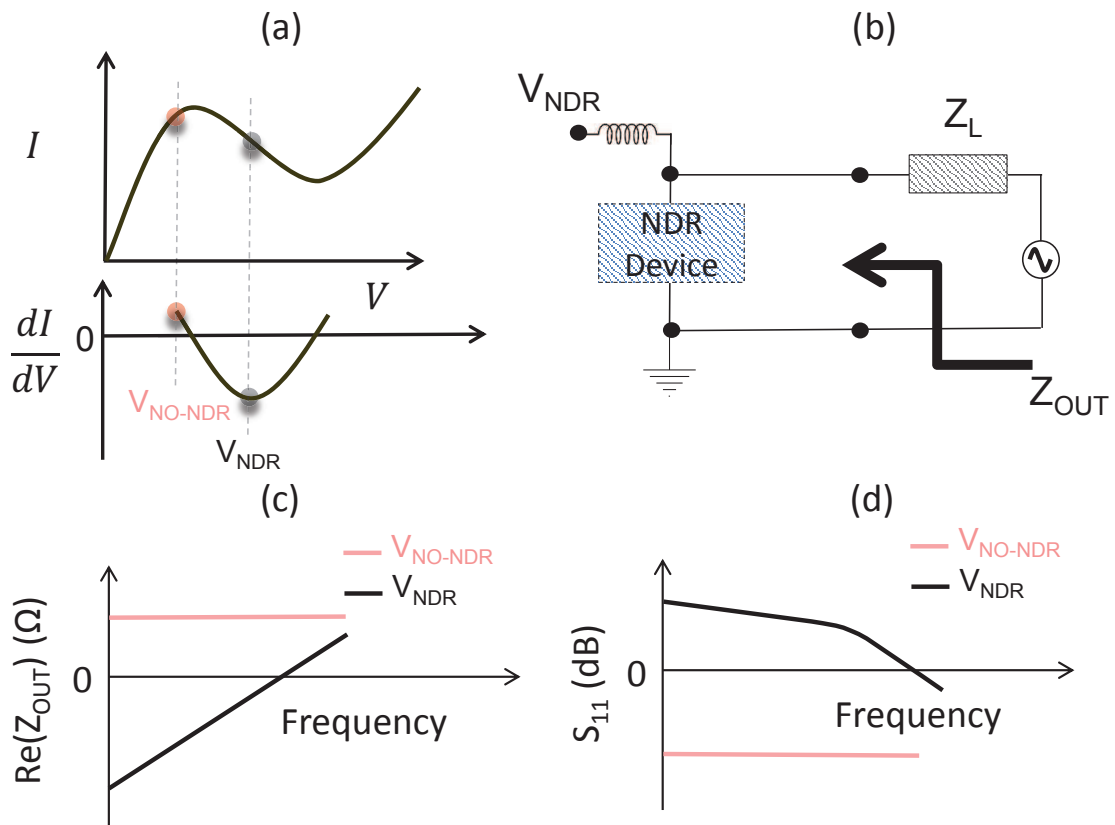
Figure 5.1: Operation principle of reflection-type NDR amplifier. (a) Electrical characteristics of typical NDR device, (b) Equivalent circuit diagram of NDR device terminated with load impedance Z_L. (c) Real part of complex impedance Z_{OUT} seen into the device when the device is biased at V_{NDR}. (d) S_{11} versus frequency.
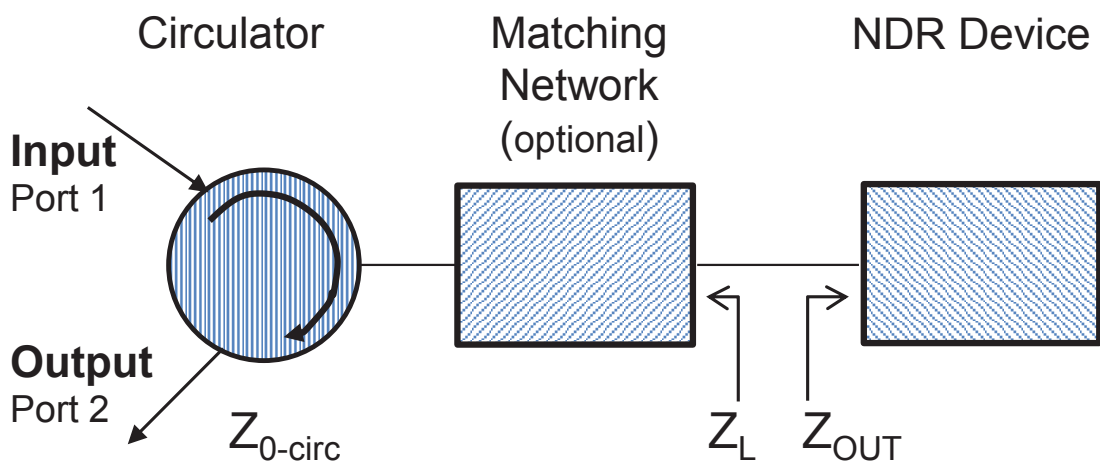
Figure 5.2: Schematic diagram of practical reflection amplifier with circulator and transforming network.
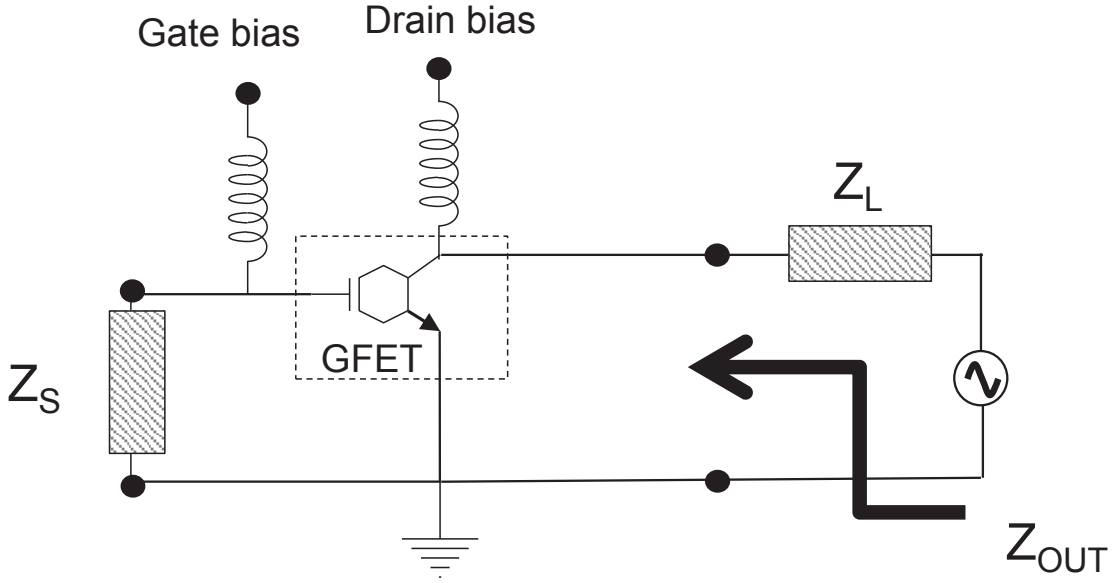
Figure 5.3: Schematic equivalent circuit diagram of reflection amplifier based on 1-GFET.

Table 5.1: Dimensions and parameters for 1-GFET-reflection amplifier.

L (μm)	1
W (μm)	10
EOT (nm)	3
$V_{Dirac-GS}$ (V)	0
μ (cm^2/(Vs))	2000
n_0 (cm^{-2})	2×10^{11}
γ	1
$\hbar\Omega$ (meV)	59
R_S, R_D (Ω)	300 $\Omega\mu$m / W(in μm)

the real part of output impedance Z_{OUT} seen into GFET is negative as shown in Fig. 5.4b. As a result, the reflection gain is seen in the simulated S_{11} characteristics (Fig. 5.4c). The observed gain is close to 0.3 dB and the cut-off frequency is 5 GHz. Both these parameters are dependent on quantities: The NDC level (maximum negative g_{DS}), and the lateral and vertical dimensions. The closer is the value of NDC to the terminating impedance ($Z_L = 50$ Ω), the higher is the gain and the frequency of operation. On other hand, smaller lateral dimensions (L and W) and higher vertical dimensions (oxide thickness), leads to reduced capacitances allowing the higher frequency operation. Scaling, however, must be done with caution as various trade-off exists: (1) Scaling channel widths does not necessarily warrant a high frequency operation as reducing it may lead to increased contact resistances which can completely diminish the NDR effect needed for reflection amplification; and (2) increasing the oxide thickness leads to a poor NDR or no NDR (Section 4.2.3). This effect is expounded in the next section.

Figure 5.4: (a) Simulated output characteristics of intrinsic GFET showing NDR characteristics. (b) Simulated real part of Z_{OUT}, and (c) simulated reflection gain as a function of frequency.

5.4 Simulation of 3-GFET NDR Reflection amplifier

Fig. 5.5a shows the equivalent circuit diagram of reflection amplifier based on 3-GFET circuit. The corresponding small-signal model is shown in Fig. 5.5b. Herein, the NDR is realized across the terminals — V_{IN} and ground. The terminal V_{IN} is connected to the gate terminal of transistors FET2 and FET3, therefore, their gate capacitances and series resistances must be taken into account as shown in the small-signal model (Fig. 5.5b). A circuit compatible model for GFET, as discussed in Section 3.1, is used to model both DC and RF performance of the circuit which includes the effect of parasitics.

The parameters used for simulation are shown in Table. 5.2. In the simulation, all the three transistors in the circuit are assumed to be identical. Fig. 5.6a shows the simulated resistances of FET2 and FET3 as a function of negative V_{IN} for different V_{DD}. At $V_{DD} = -2$ V, the Dirac splitting leads to sufficient gain in the inverter block (Fig. 5.6b) which consequently results in the NDR characteristics in FET1 as shown in Fig. 5.6c. The simulated DC characteristics are

3-GFET NDR circuit

(a)

(b)
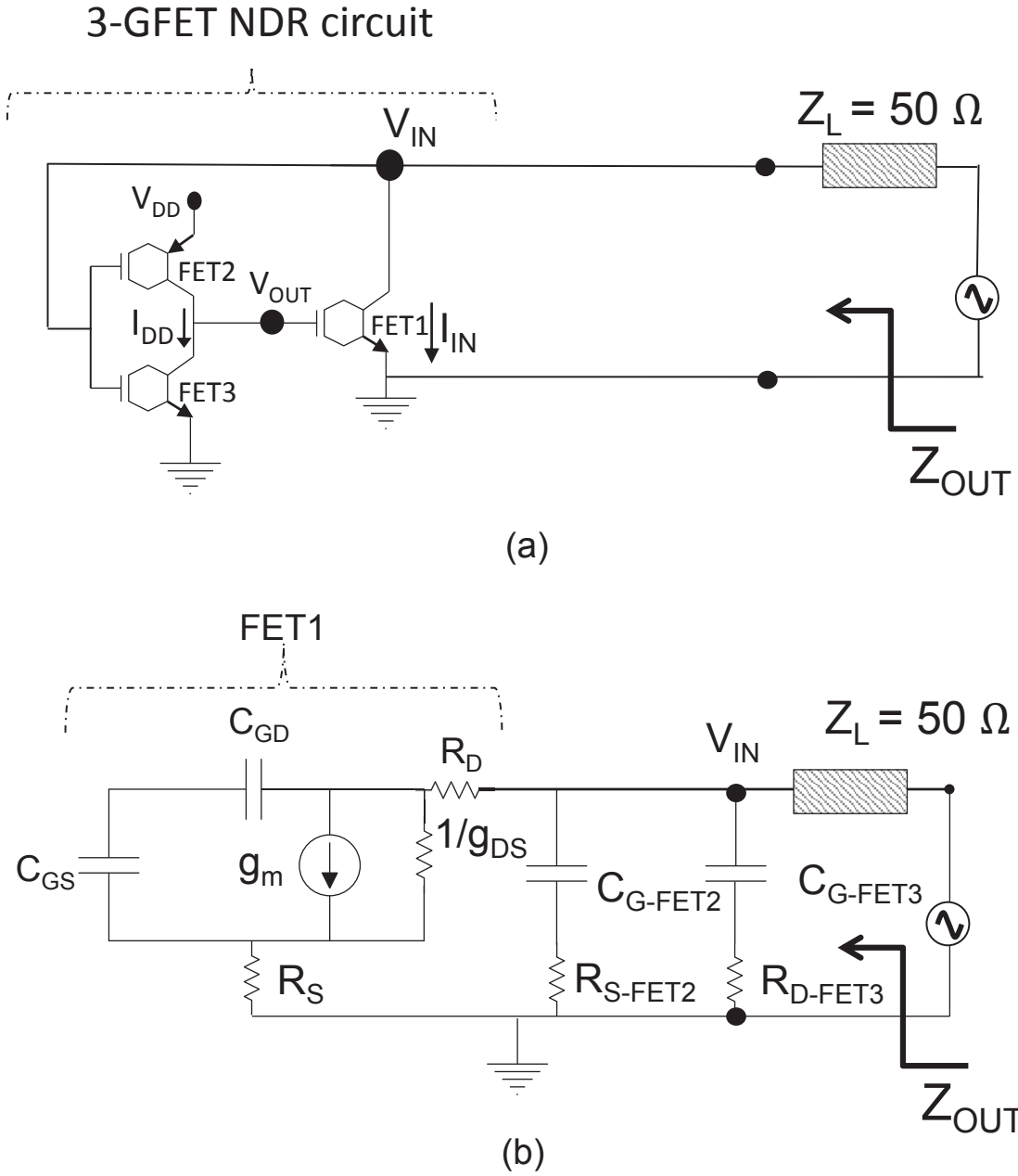
Figure 5.5: (a) Equivalent circuit diagram of 3-GFET NDR circuit based reflection amplifier. (b) Corresponding small-signal model.

Table 5.2: Dimensions and parameters for 3-GFET reflection amplifier.

L (μm)	1
W (μm)	10
EOT (nm)	3
$V_{Dirac-GS}$ (V)	0
μ (cm^2/(Vs))	2000
n_0 (cm^{-2})	2×10^{11}
γ	1
$\hbar\Omega$ (meV)	59
$R_S, R_D, R_{S-FET1}, R_{D-FET2}$, ($\Omega$)	300 $\Omega\mu$m / W (in μm)

similar to those observed experimentally (Fig. 4.10).

The circuit is then biased in the NDR region corresponding to $dI_{IN-i}/dV_{IN-i} = -8$ mS. Under these conditions, the real part of Z_{OUT} is negative as shown in Fig. 5.6d. The biasing also satisfies the condition of stability for reflection amplifier (Eq. 5.2), therefore, the reflection gain is observed as shown in Fig. 5.6e. Varying the bias point in the NDR region allows the tuning of gain (4 dB to 14 dB) as well as the frequency band (from 13 GHz to 70 GHz) as shown in Fig. 5.6f. The tuning by varying the biases in the NDR region occurs due to the change in the NDC level which modifies the output impedance; the closer is the value of output impedance to the terminating impedance ($Z_L = 50\,\Omega$) (Eq. 5.1), the higher is the gain and the frequency of operation.

Further, the frequency response of the circuit is also dependent on the gate capacitances of FET2 and FET3; thus, reducing these capacitances by scaling of channel lengths and widths of the device would allow us to go higher in frequency. Fig. 5.7 shows that broadband reflection gain exceeding 300 GHz frequency can be obtained for scaled geometries with $L = 0.2\,\mu$m and $W = 5\,\mu$m.

5.5 Measurements of 3-GFET NDR Reflection amplifier

The optical micrograph of the measured 3-GFET NDR circuit is shown in Fig. 5.8. Herein, the connection between FET1 and inverter block (FET2 and FET3) is done via external wiring. One port RF measurements are carried out with the RF probe connected to the output terminal of FET1, in which NDR is realized. The gate terminal of FET1 is ac open-circuited (not terminated with any load). The measured device has dimensions: FET1 is 1 μm long and 20 μm wide, while FET2 and FET3 are 1 μm long and 10 μm wide.

The reflection coefficient S_{11} was measured using a vector network analyzer terminated with $Z_L = 50\,\Omega$ and calibrated with short-open-load-through calibration. Fig. 5.9a shows the NDR characteristics for $V_{DD} = -3$ V, which are preserved with a negligible change when swept with RF power of -17 dBm ($V_{pp} \sim 0.09V$) switched on. Fig. 5.9b displays the reflection
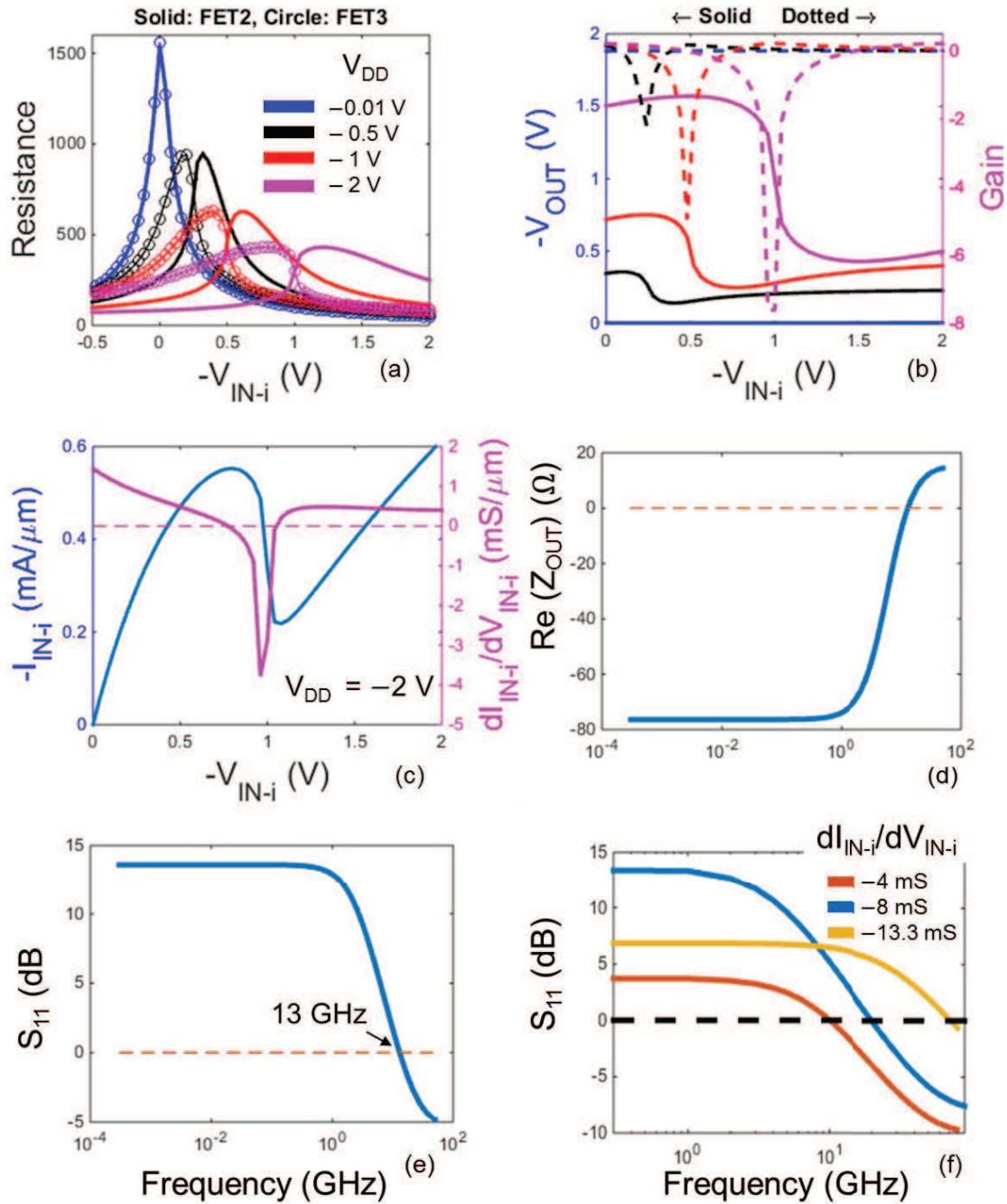
Figure 5.6: (a) Simulated resistances of FET2 and FET3 versus negative V_{IN-i}. (b) Simulated negative V_{OUT} versus negative V_{IN-i} of the inverter. Right axis shows the corresponding gain. (c) Simulated negative I_{IN-i} (right axis) and corresponding differential conductance (right axis) versus negative V_{IN-i}. (d) Simulated S_{11} versus frequency when the device is biased at different points in the NDR region.

Figure 5.7: Simulated S_{11} versus frequency for different L and W. For comparison purpose, all the shown devices are biased in the same point in NDR region corresponding to $dI_{IN-i}/dV_{IN-i} = -8$ mS. Various parasitic effects such as extrinsic capacitances and series resistances (Table. 5.2) are included.
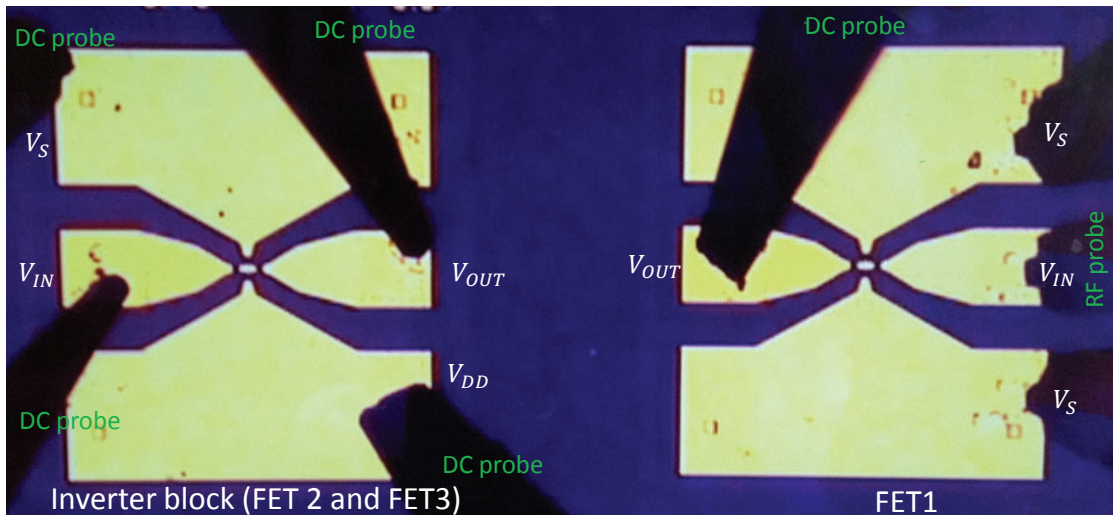
Figure 5.8: Optical micrograph of the 3-GFET NDR circuit under RF measurements.
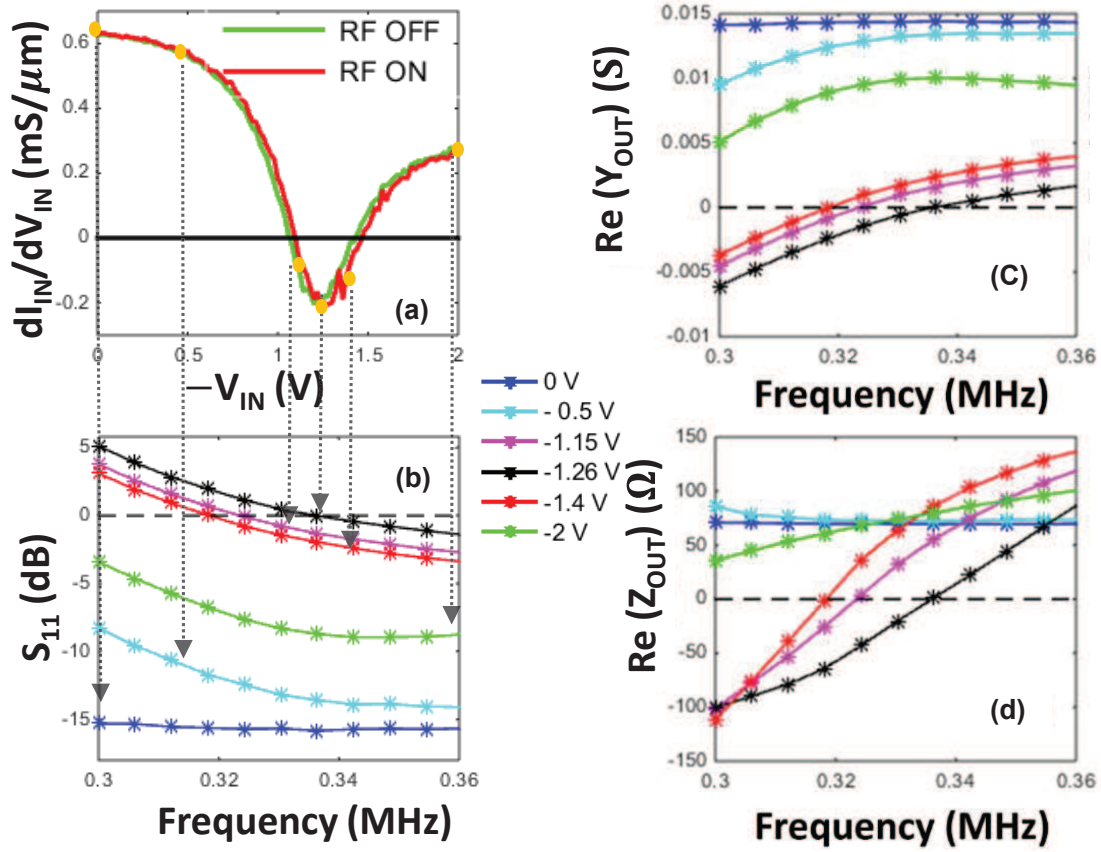
Figure 5.9: (a) Measured dI_{IN}/dV_{IN} vesrus negative V_{IN} with RF power ON and OFF of the device with dimensions: FET1 is 1 μm long and 20 μm wide, while FET2 and FET3 are 1 μm long and 10 μm wide. (b) S_{11} versus frequency. (c) The extracted real part of admittance, and (d) the extracted real part of impedance from the measured S-parameters.
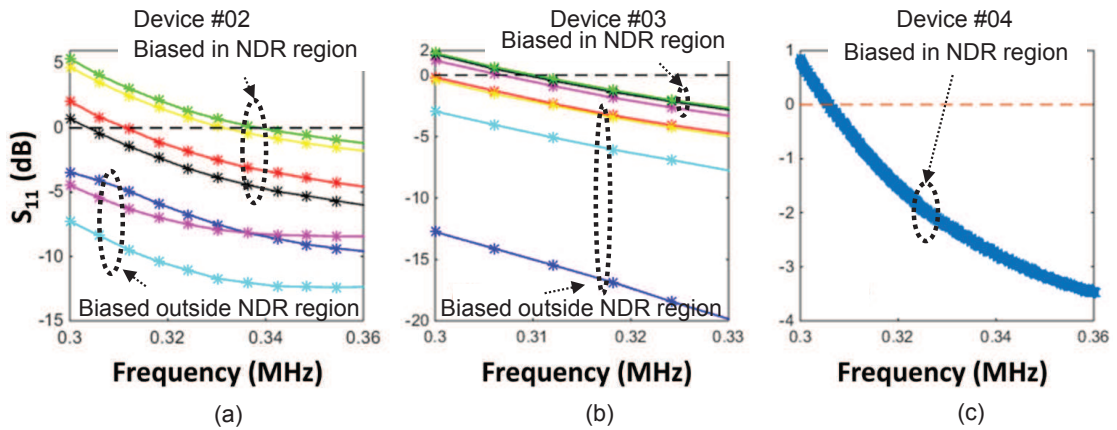
Figure 5.10: Measured S_{11} versus frequency for the devices: (a) FET1 (L = 1 μm, W = 20 μm), and FET2, FET3 (L = 1 μm, W = 10 μm); (b) FET1 (L = 400 nm, W = 20 μm), and FET2, FET3 (L = 3 μm, W = 9.5 μm); (c) FET1 (L = 500 nm, W = 9.5 μm), and FET2, FET3 (L = 1 μm, W = 10 μm).

coefficient S_{11} versus frequency and shows the effect of V_{IN} bias on S_{11}. The magnitude of S_{11} is larger than 0 dB (representing gain) only when the device is biased within the NDR region. A maximum low-frequency gain of approximately 5 dB is seen with the unity gain frequency of 336 KHz. The observed low frequency roll-off is predominantly due to the high parasitic capacitance arising from the external wiring connections done to form the 3-GFET NDR circuit. Fig. 5.9c-d shows the extracted admittance and impedance parameters versus frequency. The real part of Z_{OUT} is negative for the bias values having the reflection gain. Fig. 5.10 shows the reflection gain measured for 3 more devices. The gain is uniquely tunable by varying V_{IN} in the NDR region as can be seen in Fig. 5.9b and 5.10.

To understand the intrinsic performance of the measured device, it is important to isolate the effect of parasitics. In this case, however, it is difficult to calculate the exact contribution from parasitics as off-chip connections are involved in the setup. As an alternative approach, we simulated the device having dimensions and biasing conditions same as the measured device and still taking into account the unavoidable parasitics arising from the layout such as series resistances and underlap capacitances. In this way, we can predict the intrinsic performance of the measured device as if the whole circuit was realized on chip; that is, if the effect of off-chip cable parasitics were removed. Fig. 5.11 shows that the reflection gain of up to 8.9 GHz can be obtained if the same device of Fig. 5.9 is realized on chip.

5.6 Summary

In summary, we evaluated the performance potential of reflection amplifier based on 1-GFET transistor and 3-GFET circuit. The main conclusion is that the gain of reflection amplifier depends mainly on the NDC level; higher the NDC level, lower the output impedance (closer to 50 Ω), and higher the gain. In general the NDC level is much higher for 3-GFET circuit as
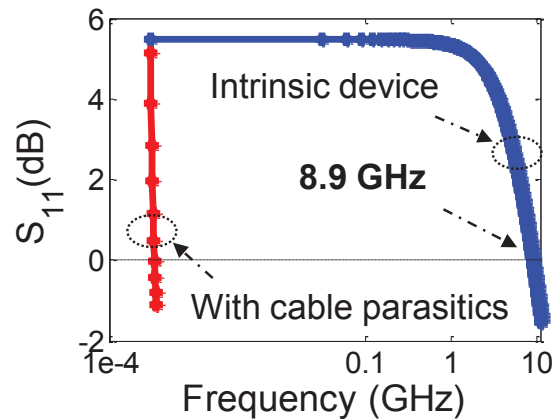
Figure 5.11: Predicted S_{11} versus frequency under ideal conditions. Red line shows the performance of the measured device (Fig. 5.9). Blue line predicts intrinsic device performance as if the effect of cable parasitics are removed.

compared to 1-GFET; therefore, 3-GFET NDR device is more attractive for reflection amplifier application. It was shown that broadband amplification above 300 GHz should be possible for scaled 3-GFET circuits. In addition, both the gain and frequency of operation can be tuned by varying the bias in the NDR region. Finally, we provided experimental evidence of reflection gain in 3-GFET reflection amplifiers.

This chapter includes the following original contributions:

- We explored the performance potential of both 1-GFET transistor and 3-GFET circuit as reflection amplifiers, via drift-diffusion and the proposed RF model.
- 3-GFET circuit can deliver superior RF performance wherein the broadband amplification exceeding 300 GHz should be possible.
- The RF characterization of 3-GFET circuit was performed in one-port configuration. The evidence of reflection amplification up to 330 KHz with low-frequency gain of ~5 dB was reported. The observed low frequency roll-off was mainly due to external connections done to connect the GFETs.

6 Conclusion and Perspective

In this chapter, we present the summary of this work, followed by some perspective for future research.

6.1 Conclusion

In this dissertation, we presented systematic work on graphene-based RF NEMS and NDR solid-state devices.

In the first part of the dissertation, we presented the modeling, simulation and characterization of graphene RF NEMS devices. There are several original contributions of this work:

- A methodology for the full-wave simulation of graphene-based RF NEMS switch was developed for the first time. A rigorous modeling of the switch taking into account the frequency-dependent conductivity and the variation of conductivity in the up- and down-states of the switch was carried out to predict the electromagnetic performance of the switch. In addition, an equivalent circuit model for the graphene-based RF NEMS switch was proposed and its parameters were also extracted. The modeling and simulation approach presented in this work is remarkably rigorous as compared to the previously proposed approach [82], where no details about fundamental issues — such as the value of graphene conductivity used for the electromagnetic simulation and the equivalent circuit parameters of the shunt switch — were provided.
- A unique conductivity variation effect was shown to have beneficial yet limited impact on the RF performance of the switch. This effect was also observed in experiments done by our group and by the recent experiments done by Li *et al.* [101, 102] on graphene-based RF NEMS shunt switches.
- The high sheet resistivity of graphene membrane is really the performance killer for graphene-based RF NEMS switches. Based on the available values of sheet resistivity data in literature, we showed that while monolayer graphene (higher sheet resistivity in general) results in quite high switch losses at high frequency, the use of multilayer

graphene (lower sheet resistivity) can considerably reduce the switch losses and improve RF performance.

- An attempt is also made to characterize the fabricated RF NEMS devices based on multi-layer graphene. The sheet resistivity of the multilayer graphene used as a membrane was rather high ~600 $\Omega/\square$. As a result, the measured devices possessed an insertion loss of −1.95 dB and isolation of −2.6 dB at 6 GHz. The pull-in voltage of 7 V was reported for the fabricated device. Although the obtained RF performances pales in comparison with state-of-the-art switches, it should not be concluded that graphene is not a promising material for RF NEMS shunt switches as this was merely the very first attempt to fabricate these devices. Further optimization in fabrication process, and the use of graphene with low sheet resistivity will significantly improve the performance.

The second part of dissertation deals with negative differential devices based on solid-state graphene devices. Following are the original contributions of this work:

- We described the drift-diffusion model for the GFET, with the intention for using this model for circuit simulation. Various intrinsic and extrinsic parameters of the small-signal model were accurately derived and calculated based on the models available in recent literature.

- We discussed two techniques to fabricate GFETs: top-gated GFET and embedded-gate GFET; complete fabrication of graphene devices from transfer of graphene to full circuit fabrication has been performed in 100 mm fabrication facility. The low-field measurements of the devices fabricated with each of these approaches were also presented. For NDR devices, we used top-gated GFET design because for them, the mobilities, and the symmetry between hole and electron conduction were found to be higher as compared to embedded-gate design.

- We reported the observation of NDR in the output characteristics of top-gated GFET for various gate lengths and dielectric thickness's under certain biasing conditions. The mechanism behind NDR was also explained in detail using the standard drift diffusion model. The main conclusion is that NDR behaviour occurs due to the competition between two core quantities of the GFET: the total number of carriers in the channel and their drift velocity. Further, it was analysed with simulations and demonstrated experimentally that lower EOTs provide a higher NDR level.

- We proposed and experimentally demonstrated a novel circuit based on three GFETs which shows enhanced NDR performance at room temperature. The proposed circuit showed an NDC level of 2.1 mS/μm that was almost an order of magnitude better than NDC based on 1-GFET. Also, this NDC level was uniquely tunable (×2.3) with the supply voltage as well as with the back bias voltage. It also exhibited improved PVCR (2.2) and wide voltage range (0.6 V) over which NDR is valid. In comparison to other NDR technologies, the graphene based solid-state NDR has a very high peak-current-density of the order of 1 mA/μm, which offers unique opportunities for designing circuits for applications requiring high current drive.

- Finally, we assessed the potential of both 1-GFET transistor and 3-GFET circuit as

reflection amplifiers, via drift-diffusion and the proposed RF model. In general the NDC level is much higher for 3-GFET NDR compared to 1-GFET; therefore, 3-GFET NDR device is more attractive for reflection amplifier application. It was shown that broadband amplification above 300 GHz should be possible for scaled 3-GFET circuits. Furthermore, both the gain and frequency of operation can be highly modulated by varying the bias in the NDR region. In addition, we provided experimental evidence of reflection amplification in 3-GFET reflection amplifiers.

6.2 Perspective

In their review article, Novoselov *et al.* [115] rightly summarized the current state of affairs: "Graphene will be of even greater interest for industrial applications when mass-produced graphene has the same outstanding performance as the best samples obtained in research laboratories." Truly, the large-scale production of high-quality graphene is the most desirable challenge to accomplish before its widespread application. This aspect is particularly relevant in the context of this thesis as we utilized mass-production friendly CVD-derived graphene for fabrication of both NEMS and solid-state NDR devices. Compared to exfoliated graphene, CVD graphene exhibits lower mobility, greater impurity doping, and higher asymmetry between electron and hole conduction. For NEMS application, improvement in the mobility would result in low sheet resistivity; a low sheet resistivity graphene membrane is highly desirable for improving the RF performance of the NEMS switch. For NDR devices, improvement in the quality of graphene would improve the NDR performance of both 1-GFET and 3-GFET devices.

In the category of suspended graphene devices, the research, in the past decade, has been mainly focused on graphene-based resonators and less on RF switches. In part because the fabrication of RF NEMS switches is relatively more challenging as it requires the formation of central conductor (embedded central conductor design) prior to the membrane deposition and release step, and in part due to the sense of pessimism that graphene can never compete with metal membrane switches in terms of their RF performance because of its high resistivity. Such a comparison with metal membrane switch, however, is unfair. Graphene (thickness of few nanometres) is compared to metal membrane whose thickness is in micrometre scale. The fair comparison would be to compare them at the same thicknesses (such that they exhibit same levels of low actuation voltages); that is, thinning down the current state-of-the-art metal membrane to the comparable thickness of graphene. The question then would be: Will they retain the same low sheet resistivity as their bulk form? This is highly improbable as bulk metals when thinned down show altogether different transport properties; become brittle; and their isolation from the bulk to their 2-D counterpart is itself an enormous technological challenge. Therefore, the future research should be to access existing 2-D materials which exhibits thinness in nanometre scale (for lower actuation voltages) and yet show lower sheet resistivity (for respectable RF performance). Currently, graphene seems to hold that promise as it is one of the first two-dimensional material to be isolated in its mono- and multi-layer form.

The lowest sheet resistivity of 30 $\Omega/\square$ was demonstrated by Bae *et al.* [74]; such samples of low sheet resistivities remain to be accessed experimentally for RF NEMS switches. A recent report by Li *et al.* [101, 102] have refuelled the interest in the field of graphene RF NEMS switches; this work demonstrated a RF switch exhibiting pull-in voltage of less than 1 V, and a very high isolation of -30 dB and a rather high insertion loss of -6 dB. The outstanding RF performance (mainly the isolation) achieved in this work is because of the use of single-crystalline graphene with very high mobility, and thus possibly exhibiting very low sheet resistivity (value of sheet resistivity not specified in this work). Furthermore, the recently discovered two-dimensional materials [17, 213], also, remain to be explored for its use in RF NEMS switches.

Turning now to the graphene solid-state NDR devices, the NDR in single-GFET is manifested at rather low PVCR values. Although, 3-GFET circuit offers direct solution to improve the NDR performance, the NDR in single-GFET can also be improved by combination of several factors. For instance, a high performance single-GFET NDR device would be a GFET which uses a channel material of high mobility graphene ($> 10,000$ cm^2/(Vs)), a top-gate dielectric of ultra-low EOT (< 1 nm), short un-gated regions with minimal series resistances (< 100 $\Omega\mu$m), and which are deposited on the dielectric material of lower optical phonon energy ($\hbar\Omega < 40$ meV) such as boron nitride.

Owing to its excellent NDR characteristics and the ability to exhibit NDR at higher current levels, 3-GFET NDR graphene circuit are very interesting for various applications. In addition to the refection amplifier application as demonstrated in this work, the other interesting applications are oscillators [214, 191], multipliers [171], mixers, analog-to-digital converters [172], and binary- and ternary-adder circuits [173]. Furthermore, as the improvement in the gain of inverter block in the 3-GFET NDR circuit results in the improvement in its NDR performance, the use of recently discovered two-dimensional materials, which because of their band-gap holds the ability to exhibit higher voltage gains [215, 216], in the proposed NDR circuit may improve the NDR performance significantly.

A Multi-Layer Graphene Characterization

In this appendix, we describe the sheet resistance extraction of multilayer graphene from the high-frequency scattering parameter measurements. The CVD-derived non-suspended multilayer graphene is integrated into coplanar waveguide structures for high frequency measurements as shown in Fig. A.1. The following test structures are measured:

1. **Graphene shunt structure**: CPW structure with multilayer graphene (Fig. A.1a).

2. **Thru structure**: CPW structure without multilayer graphene (Fig. A.1b).

The measured S-parameters of both the structures are shown in Fig. A.2. The extracted equivalent circuit model is represented in Fig. A.3. Full-wave simulation as well as the modeled S-parameters reconstructed from the extracted circuit model gives excellent fit to measurements (Fig. A.4).

From the extracted circuit model, the shunt resistance R_{Multi} is 129.8 Ω (Fig. A.4). This
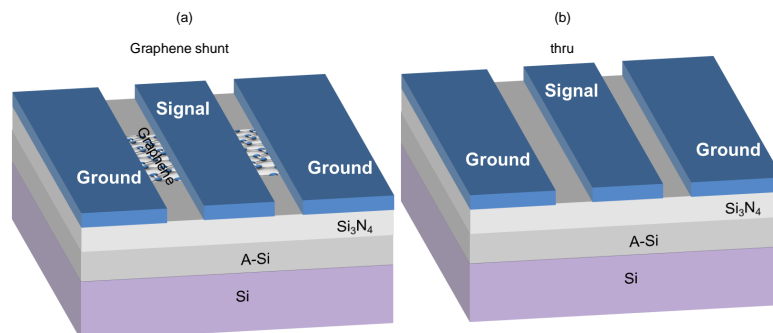
Figure A.1: (a) Multilayer graphene integrated in coplanar waveguide structure (referred as graphene shunt). (b) Coplanar waveguide without multilayer graphene (referred as thru).

Figure A.2: Measured S_{12} (a) and S_{11} (b) of thru and graphene shunt structures.

$L_s = 414$ pH $R_s = 2.7\ \Omega$ $R_s = 2.7\ \Omega$ $L_s = 414$ pH

$R_{multi} = 129.8\ \Omega$ $C = 157.9\ fF$
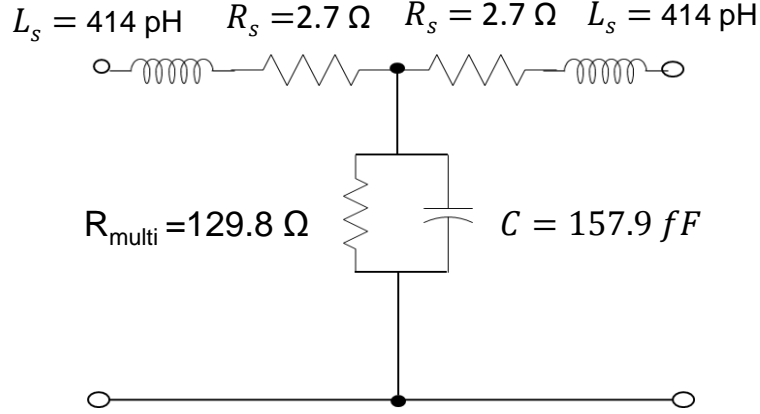
Figure A.3: Extracted circuit model of non-suspended multilayer graphene.

resistance value is related to the sheet resistivity ρ_{Multi} as

$$R_{Multi} = \frac{1}{2}\rho_{Multi}\frac{G_{CPW}}{w_{CPW}} \tag{A.1}$$

where G_{CPW} is the CPW gap, that is, the distance between signal and ground; and w_{CPW} is the width of graphene. Thus for the calculated $R_{Multi} = 129.8\ \Omega$, we obtain the sheet resistance $\rho_{Multi} = 605.7\ \Omega/\square$.
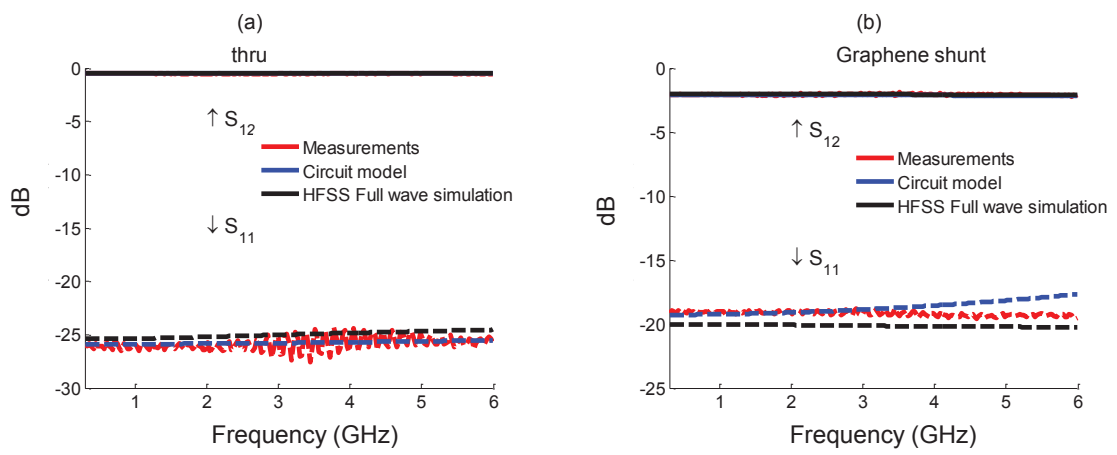
Figure A.4: Full-wave simulation as well as the modeled S parameters reconstructed from the extract circuit model gives excellent fit to measurements.

Bibliography

[1] A. M. Ionescu and K. Banerjee, *Emerging nanoelectronics : life with and after CMOS.* Kluwer Academic Pub, 2005, vol. 1.

[2] M. Lundstrom, "Is Nanoelectronics the Future of Microelectronics.pdf," in *Proceedings of the 2002 international symposium on Low power electronics and design.* ACM, 2002, pp. 172–177.

[3] A. D. Franklin, "Nanomaterials in transistors: From high-performance to thin-film applications," *Science*, vol. 349, no. 6249, pp. aab2750–aab2750, 2015. [Online]. Available: http://www.sciencemag.org/cgi/doi/10.1126/science.aab2750

[4] C. Lee, X. Wei, J. W. Kysar, and J. Hone, "Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene," *Science*, vol. 321, no. 5887, pp. 385–388, 2008. [Online]. Available: http://www.sciencemag.org/cgi/doi/10.1126/science.1157996

[5] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene," *Nature Nanotechnology*, vol. 3, no. 8, pp. 491–495, 2008. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2008.199

[6] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Letters*, vol. 8, no. 3, pp. 902–907, Feb. 2008.

[7] L. Yang, C.-H. Park, Y.-W. Son, M. L. Cohen, and S. G. Louie, "Quasiparticle Energies and Band Gaps in Graphene Nanoribbons," *Physical Review Letters*, vol. 99, no. 18, p. 186801, 2007. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.99.186801

[8] I. Meric, N. Baklitskaya, P. Kim, and K. L. Shepard, "RF performance of top-gated, zero-bandgap graphene field-effect transistors," in *2008 IEEE International Electron Devices Meeting*, no. c. IEEE, 2008, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4796738

[9] Y.-M. Lin, K. Jenkins, D. Farmer, A. Valdes-Garcia, P. Avouris, C.-Y. Sung, H.-Y. Chiu, and B. Ek, "Development of graphene FETs for high frequency electronics," in *2009 IEEE International Electron Devices Meeting (IEDM).* IEEE, 2009, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5424378

Bibliography

[10] Y.-M. Lin, C. Dimitrakopoulos, K. a. Jenkins, D. B. Farmer, H.-Y. Chiu, a. Grill, and P. Avouris, "100-GHz Transistors from Wafer-Scale Epitaxial Graphene," *Science*, vol. 327, no. 5966, pp. 662–662, 2010. [Online]. Available: http://www.sciencemag.org/cgi/doi/10.1126/science.1184289

[11] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, no. 7313, pp. 305–308, 2010. [Online]. Available: http://www.nature.com/doifinder/10.1038/nature09405

[12] Y. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, and Others, "State-of-the-art graphene high-frequency electronics," *Nano letters*, vol. 12, no. 6, pp. 3062–3067, 2012.

[13] J. Gun Oh, S. Ki Hong, C.-K. Kim, J. Hoon Bong, J. Shin, S.-Y. Choi, and B. Jin Cho, "High performance graphene field effect transistors on an aluminum nitride substrate with high surface phonon energy," *Applied Physics Letters*, vol. 104, no. 19, p. 193112, 2014. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/104/19/10.1063/1.4878316

[14] S.-J. Han, A. V. Garcia, S. Oida, K. a. Jenkins, and W. Haensch, "Graphene radio frequency receiver integrated circuit," *Nature Communications*, vol. 5, p. 3086, Jan. 2014. [Online]. Available: http://www.nature.com/doifinder/10.1038/ncomms4086

[15] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan, "High-frequency self-aligned graphene transistors with transferred gate stacks," *Proceedings of the National Academy of Sciences*, vol. 109, no. 29, pp. 11 588–11 592, 2012. [Online]. Available: http://www.pnas.org/cgi/doi/10.1073/pnas.1205696109

[16] F. Schwierz, "Graphene Transistors: Status, Prospects, and Problems," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1567–1584, 2013. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6518205

[17] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, "Electronics based on two-dimensional materials," *Nature Nanotechnology*, vol. 9, no. 10, pp. 768–779, 2014. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2014.207$\delimiter"026E3B2$nhttp://dx.doi.org/10.1038/nnano.2014.207

[18] M. C. Lemme, L.-J. Li, T. Palacios, and F. Schwierz, "Two-dimensional materials for electronic applications," *MRS Bulletin*, vol. 39, no. 08, pp. 711–718, 2014. [Online]. Available: http://www.journals.cambridge.org/abstract_S0883769414001389

[19] B. Radisavljevic, a. Radenovic, J. Brivio, V. Giacometti, and a. Kis, "Single-layer MoS2 transistors," *Nature Nanotechnology*, vol. 6, no. 3, pp. 147–150, 2011. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2010.279

[20] L. Tao, E. Cinquanta, D. Chiappe, C. Grazianetti, M. Fanciulli, M. Dubey, A. Molle, and D. Akinwande, "Silicene field-effect transistors operating at room temperature," *Nature Nanotechnology*, vol. 10, no. 3, pp. 227–231, 2015. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2014.325

[21] M. Xu, T. Liang, M. Shi, and H. Chen, "Graphene-like two-dimensional materials," *Chemical Reviews*, vol. 113, no. 5, pp. 3766–3798, 2013.

[22] A. K. Geim and K. Novoselov, "The rise of graphene," *Nature Mater.*, vol. 6, no. 3, pp. 183–191, 2007. [Online]. Available: http://www.nature.com/doifinder/10.1038/nmat1849

[23] P. R. Wallace, "The band theory of graphite," *Physical Review*, vol. 71, no. 9, pp. 622–634, 1947.

[24] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, a. a. Firsov, a. F. K.S. Novoselov1, A.K. Geim1, S.V. Morozov2, D. Jiang1, Y. Zhang1, S.V. Dubonos2, I.V.Grigorieva1, and K. Using, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004. [Online]. Available: http://arxiv.org/ftp/cond-mat/papers/0410/0410550.pdf$\delimiter"026E3B2$nhttp://www.sciencemag.org/content/306/5696/666.abstract

[25] Y. Zhang, Y. W. Tan, H. L. Stormer, and P. Kim, "Experimental observation of the quantum Hall effect and Berry's phase in graphene," *Nature*, vol. 438, no. 7065, pp. 201–4, 2005. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/16281031

[26] C. Berger, Z. Song, T. Li, X. Li, A. Y. Ogbazghi, R. Feng, Z. Dai, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. a. de Heer, "Ultrathin Epitaxial Graphite: 2D Electron Gas Properties and a Route toward Graphene-based Nanoelectronics," *The Journal of Physical Chemistry B*, vol. 108, no. 52, pp. 19 912–19 916, 2004. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/jp040650f

[27] J. C. Meyer, a. K. Geim, M. I. Katsnelson, K. S. Novoselov, T. J. Booth, and S. Roth, "The structure of suspended graphene sheets." *Nature*, vol. 446, no. 7131, pp. 60–63, 2007. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/17330039

[28] J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, and P. L. McEuen, "Electromechanical resonators from graphene sheets." *Science (New York, N.Y.)*, vol. 315, no. 5811, pp. 490–3, Jan. 2007. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/17255506

[29] C. Chen, S. Rosenblatt, K. I. Bolotin, W. Kalb, P. Kim, I. Kymissis, H. L. Stormer, T. F. Heinz, and J. Hone, "Performance of monolayer graphene nanomechanical resonators with electrical readout." *Nature nanotechnology*, vol. 4, no. 12, pp. 861–867, Dec. 2009. [Online]. Available: http://dx.doi.org/10.1038/nnano.2009.267

[30] A. M. Van Der Zande, R. a. Barton, J. S. Alden, C. S. Ruiz-Vargas, W. S. Whitney, P. H. Q. Pham, J. Park, J. M. Parpia, H. G. Craighead, and P. L. McEuen, "Large-scale arrays of

single-layer graphene resonators," *Nano Letters*, vol. 10, no. 12, pp. 4869–4873, Nov. 2010. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/21080681

[31] S. Shivaraman, R. a. Barton, X. Yu, J. Alden, L. Herman, M. Chandrashekhar, J. Park, P. L. McEuen, J. M. Parpia, H. G. Craighead, and M. G. Spencer, "Free-Standing Epitaxial Graphene," *Nano Letters*, vol. 9, no. 9, pp. 3100–3105, Sep. 2009. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl900479g

[32] Y. Xu, C. Chen, V. V. Deshpande, F. a. DiRenno, A. Gondarenko, D. B. Heinz, S. Liu, P. Kim, and J. Hone, "Radio frequency electrical transduction of graphene mechanical resonators," *Applied Physics Letters*, vol. 97, no. 24, p. 243111, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/97/24/10.1063/1.3528341

[33] S. Lee, C. Chen, V. V. Deshpande, G.-H. Lee, I. Lee, M. Lekas, A. Gondarenko, Y.-J. Yu, K. Shepard, P. Kim, and J. Hone, "Electrically integrated SU-8 clamped graphene drum resonators for strain engineering," *Applied Physics Letters*, vol. 102, no. 15, p. 153101, 2013. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/102/15/10.1063/1.4793302

[34] D. Midtvedt, A. Croy, A. Isacsson, Z. Qi, and H. S. Park, "Fermi-Pasta-Ulam Physics with Nanomechanical Graphene Resonators: Intrinsic Relaxation and Thermalization from Flexural Mode Coupling," *Physical Review Letters*, vol. 112, no. 14, p. 145503, 2014. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.112.145503

[35] V. Singh, S. J. Bosman, B. H. Schneider, Y. M. Blanter, a. Castellanos-Gomez, and G. a. Steele, "Optomechanical coupling between a multilayer graphene mechanical resonator and a superconducting microwave cavity," *Nature Nanotechnology*, vol. 9, no. 10, pp. 820–824, 2014. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2014.168

[36] A. D. Smith, F. Niklaus, A. Paussa, S. Vaziri, a. C. Fischer, M. Sterner, F. Forsberg, A. Delin, D. Esseni, P. Palestri, M. Östling, and M. C. Lemme, "Electromechanical Piezoresistive Sensing in Suspended Graphene Membranes," *Nano Letters*, vol. 13, no. 7, pp. 3237–3242, 2013. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl401352k

[37] A. Smith, S. Vaziri, F. Niklaus, A. Fischer, M. Sterner, A. Delin, M. Östling, and M. Lemme, "Pressure sensors based on suspended graphene membranes," *Solid-State Electronics*, vol. 88, pp. 89–94, 2013. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0038110113001810

[38] K. M. Milaninia, M. a. Baldo, A. Reina, and J. Kong, "All graphene electromechanical switch fabricated by chemical vapor deposition," *Applied Physics Letters*, vol. 95, no. 18, p. 183105, 2009. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/95/18/10.1063/1.3259415

[39] S. M. Kim, E. B. Song, S. Lee, S. Seo, D. H. Seo, Y. Hwang, R. Candler, and K. L. Wang, "Suspended few-layer graphene beam electromechanical switch with abrupt on-off characteristics and minimal leakage current," *Applied Physics Letters*, vol. 99, no. 2, p. 023103, 2011. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/99/2/10.1063/1.3610571

[40] P. Li, Z. You, and T. Cui, "Graphene cantilever beams for nano switches," *Applied Physics Letters*, vol. 101, no. 9, p. 093111, Aug. 2012. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/101/9/10.1063/1.4738891

[41] M. Liao and Y. Koide, "Carbon-Based Materials: Growth, Properties, MEMS/NEMS Technologies, and MEM/NEM Switches," *Critical Reviews in Solid State and Materials Sciences*, vol. 36, no. 2, pp. 66–101, Apr. 2011. [Online]. Available: http://www.tandfonline.com/doi/abs/10.1080/10408436.2011.572748

[42] O. Y. Loh and H. D. Espinosa, "Nanoelectromechanical contact switches," *Nature Nanotechnology*, vol. 7, no. 5, pp. 283–295, 2012. [Online]. Available: http://dx.doi.org/10.1038/nnano.2012.40

[43] Han Wang, D. Nezich, Jing Kong, and T. Palacios, "Graphene Frequency Multipliers," *IEEE Electron Device Letters*, vol. 30, no. 5, pp. 547–549, 2009. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4808221

[44] J. S. Moon, D. Curtis, D. Zehnder, S. Kim, D. K. Gaskill, G. G. Jernigan, R. L. Myers-Ward, C. R. Eddy, P. M. Campbell, K.-M. Lee, and P. Asbeck, "Low-Phase-Noise Graphene FETs in Ambipolar RF Applications," *IEEE Electron Device Letters*, vol. 32, no. 3, pp. 270–272, 2011. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5699337

[45] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-Based Ambipolar RF Mixers," *IEEE Electron Device Letters*, vol. 31, no. 9, pp. 906–908, 2010. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5512599

[46] X. Yang, G. Liu, A. a. Balandin, and K. Mohanram, "Triple-Mode Single-Transistor Graphene Amplifier and Its Applications," *ACS Nano*, vol. 4, no. 10, pp. 5532–5538, 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn1021583

[47] N. Harada, K. Yagi, S. Sato, and N. Yokoyama, "A polarity-controllable graphene inverter," *Applied Physics Letters*, vol. 96, no. 1, p. 012102, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/96/1/10.1063/1.3280042

[48] T. Palacios, "Graphene electronics: Thinking outside the silicon box," *Nature Nanotechnology*, vol. 6, no. 8, pp. 464–465, 2011. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2011.125

[49] H. Wang, A. Hsu, B. Mailly, Ki Kang Kim, J. Kong, and T. Palacios, "Towards ubiquitous RF electronics based on graphene," in *2012 IEEE/MTT-S International*

Microwave Symposium Digest, no. d. IEEE, 2012, pp. 1–3. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6259399

[50] C.-H. Liu, Y.-C. Chang, T. B. Norris, and Z. Zhong, "Graphene photodetectors with ultra-broadband and high responsivity at room temperature." *Nature nanotechnology*, vol. 9, no. 4, pp. 273–8, 2014. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/24633521

[51] C. Gómez-Navarro, M. Burghard, and K. Kern, "Elastic Properties of Chemically Derived Single Graphene Sheets," *Nano Letters*, vol. 8, no. 7, pp. 2045–2049, Jun. 2008. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl801384y

[52] B. D. Kong, S. Paul, M. B. Nardelli, and K. W. Kim, "First-principles analysis of lattice thermal conductivity in monolayer and bilayer graphene," *Physical Review B*, vol. 80, no. 3, p. 033406, 2009. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevB.80.033406

[53] M. C. Hersam, "The Reemergence of Chemistry for Post-Graphene Two-Dimensional Nanomaterials," *ACS Nano*, vol. 9, no. 5, pp. 4661–4663, 2015. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/acsnano.5b02806

[54] P. Sharma, J. Gomez-Diaz, A. M. Ionescu, and J. Perruisseau-Carrier, "Determination of minimum conductivity of graphene from contactless microwaves measurements," in *2012 12th IEEE International Conference on Nanotechnology (IEEE-NANO)*. IEEE, 2012, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6322060

[55] S. Das Sarma, S. Adam, E. H. Hwang, and E. Rossi, "Electronic transport in two-dimensional graphene," *Reviews of Modern Physics*, vol. 83, no. 2, pp. 407–470, 2011.

[56] S. Datta, *Quantum Transport : Atom to Transistor*. Cambridge University Press, 2005. [Online]. Available: http://books.google.com/books?hl=en&lr=&id=Yj50EJoS224C&oi=fnd&pg=PR9&dq=Quantum+Transport+:+Atom+to+Transistor&ots=jmVfovCmEu&sig=oYLWTfZuNxd44-WwK4FwD-Tmg98

[57] D. Berdebes, T. Low, and M. Lundstrom, "Low Bias Transport in Graphene : An Introduction," *Electronics*, pp. 1–23, 2009.

[58] K. Raseong and L. Mark, "Notes on Fermi-Dirac Integrals (3rd Edition)," Sep. 2008. [Online]. Available: https://nanohub.org/resources/5475

[59] G. Rebeiz and J. Muldavin, "RF MEMS switches and switch circuits," *IEEE Microwave Magazine*, vol. 2, no. 4, pp. 59–71, 2001. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=969936

[60] H. Sehr, a. G. R. Evans, a. Brunnschweiler, G. J. Ensell, and C. G. J. Schabmueller, "Design and fabrication of a thermally actuated microrelay based on vertical bimorphs," in

Eurosensors XVI, the 16th European Conference on Solid-State Transducers, 2002, pp. 752–755.

[61] J. Wright and Yu-Chong Tai, "Magnetostatic MEMS relays for the miniaturization of brushless DC motor controllers," in *Technical Digest. IEEE International MEMS 99 Conference. Twelfth IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.99CH36291)*. IEEE, 1999, pp. 594–599. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=746895

[62] H. Hosaka, H. Kuwano, and K. Yanagiswa, "Electromagnetic microrelays: concepts and fundamental characteristics," in *[1993] Proceedings IEEE Micro Electro Mechanical Systems*. IEEE, 1993, pp. 12–17. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=296943

[63] J. Yao and M. Chang, "A Surface Micromachined Miniature Switch For Telecommunications Applications With Signal Frequencies From DC Up To 4 Ghz," in *Proceedings of the International Solid-State Sensors and Actuators Conference - TRANSDUCERS '95*, vol. 2. IEEE, 1995, pp. 384–387. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=721827

[64] J. Muldavin and G. Rebeiz, "High-isolation CPW MEMS shunt switches. 1. Modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 6, pp. 1045–1052, 2000. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=904743

[65] A. Liu, A. Yu, M. Karim, and M. Tang, *RF MEMS Switches and Integrated Switching Circuits*. Springer Science & Business Media, 2007, vol. 7.

[66] I. W. Frank, D. M. Tanenbaum, a. M. van der Zande, and P. L. McEuen, "Mechanical properties of suspended graphene sheets," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 25, no. 6, p. 2558, 2007. [Online]. Available: http://scitation.aip.org/content/avs/journal/jvstb/25/6/10.1116/1.2789446

[67] D. Acquaviva, a. Arun, S. Esconjauregui, D. Bouvet, J. Robertson, R. Smajda, a. Magrez, L. Forro, and a. M. Ionescu, "Capacitive nanoelectromechanical switch based on suspended carbon nanotube array," *Applied Physics Letters*, vol. 97, no. 23, p. 233508, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/97/23/10.1063/1.3525165

[68] A. Ionescu, J. Dijon, and J. Robertson, "Integration for All Configurations," *IEEE Microwave Magazine*, vol. 12, no. 7, pp. 42–50, 2011. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6031951

[69] J. Perruisseau-Carrier, "Graphene for antenna applications: Opportunities and challenges from microwaves to THz," *2012 Loughborough Antennas & Propagation Conference (LAPC)*, pp. 1–4, 2012. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6402934

[70] Changyao Chen and J. Hone, "Graphene nanoelectromechanical systems," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1766–1779, 2013. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6523077

[71] C. Goldsmith, D. Forehand, D. Scarbrough, I. Johnston, S. Sampath, a. Datta, Z. Peng, C. Palego, and J. Hwang, "Performance of molybdenum as a mechanical membrane for RF MEMS switches," *2009 IEEE MTT-S International Microwave Symposium Digest*, pp. 1229–1232, 2009. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5165925

[72] D. Garcia-Sanchez, a. M. van der Zande, a. S. Paulo, B. Lassagne, P. L. McEuen, and a. Bachtold, "Imaging Mechanical Vibrations in Suspended Graphene Sheets," *Nano Letters*, vol. 8, no. 5, pp. 1399–1403, Apr. 2008. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl080201h

[73] C.-Y. Su, A.-Y. Lu, Y. Xu, F.-R. Chen, A. N. Khlobystov, and L.-J. Li, "High-Quality Thin Graphene Films from Fast Electrochemical Exfoliation," *ACS Nano*, vol. 5, no. 3, pp. 2332–2339, Feb. 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn200025p

[74] S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. Ri Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong, and S. Iijima, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," *Nature Nanotechnology*, vol. 5, no. 8, pp. 574–578, Aug. 2010. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2010.132

[75] F. Gunes, H.-J. Shin, C. Biswas, G. H. Han, E. S. Kim, S. J. Chae, J.-Y. Choi, and Y. H. Lee, "Layer-by-Layer Doping of Few-Layer Graphene Film," *ACS Nano*, vol. 4, no. 8, pp. 4595–4600, 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn1008808

[76] A. Kasry, M. a. Kuroda, G. J. Martyna, G. S. Tulevski, and A. a. Bol, "Chemical Doping of Large-Area Stacked Graphene Films for Use as Transparent, Conducting Electrodes," *ACS Nano*, vol. 4, no. 7, pp. 3839–3844, Jul. 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn100508g

[77] A. B. Kaul, E. W. Wong, L. Epp, and B. D. Hunt, "Electromechanical Carbon Nanotube Switches for High-Frequency Applications," *Nano Letters*, vol. 6, no. 5, pp. 942–947, May 2006. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl052552r

[78] X. Li, Y. Zhu, W. Cai, M. Borysiak, B. Han, D. Chen, R. D. Piner, L. Colombo, and R. S. Ruoff, "Transfer of Large-Area Graphene Films for High-Performance Transparent Conductive Electrodes," *Nano Letters*, vol. 9, no. 12, pp. 4359–4363, Dec. 2009. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl902623y

[79] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," *Nano Letters*, vol. 9, no. 1, pp. 30–35, 2009. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl801827v

[80] K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi, and B. H. Hong, "Large-scale pattern growth of graphene films for stretchable transparent electrodes," *Nature*, vol. 457, no. 7230, pp. 706–710, Feb. 2009. [Online]. Available: http://www.nature.com/doifinder/10.1038/nature07719

[81] W. Cai, Y. Zhu, X. Li, R. D. Piner, and R. S. Ruoff, "Large area few-layer graphene/graphite films as transparent thin conducting electrodes," *Applied Physics Letters*, vol. 95, no. 12, p. 123115, 2009. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/95/12/10.1063/1.3220807

[82] M. Dragoman, D. Dragoman, F. Coccetti, R. Plana, and a. a. Muller, "Microwave switches based on graphene," *Journal of Applied Physics*, vol. 105, no. 5, p. 054309, 2009. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/105/5/10.1063/1.3080130

[83] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, a. a. Firsov, a. F. K.S. Novoselov1, A.K. Geim1, S.V. Morozov2, D. Jiang1, Y. Zhang1, S.V. Dubonos2, I.V.Grigorieva1, and K. Using, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004. [Online]. Available: http://arxiv.org/ftp/cond-mat/papers/0410/0410550.pdf$\delimiter"026E3B2$nhttp://www.sciencemag.org/content/306/5696/666.abstract

[84] R. N. Simons, *Coplanar Waveguide Circuits, Components, and Systems*. John Wiley & Sons, Inc., New York, USA, 2001, vol. 7. [Online]. Available: http://doi.wiley.com/10.1002/0471224758

[85] P. Sharma, J. Perruisseau-Carrier, C. Moldovan, and A. M. Ionescu, "Electromagnetic Performance of RF NEMS Graphene Capacitive Switches," *IEEE Transactions on Nanotechnology*, vol. 13, no. 1, pp. 70–79, 2014. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6665041

[86] V. P. Gusynin, S. G. Sharapov, and J. P. Carbotte, "Magneto-optical conductivity in graphene," *Journal of Physics: Condensed Matter*, vol. 19, no. 2, p. 026222, 2007. [Online]. Available: http://stacks.iop.org/0953-8984/19/i=2/a=026222?key=crossref.2b7a1dc16f5538d2a7a575daae6e705b

[87] G. W. Hanson, A. B. Yakovlev, and A. Mafi, "Excitation of discrete and continuous spectrum for a surface conductivity model of graphene," *Journal of Applied Physics*, vol. 110, no. 11, p. 114305, 2011. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/110/11/10.1063/1.3662883

[88] W. Zhu, V. Perebeinos, M. Freitag, and P. Avouris, "Carrier scattering, mobilities, and electrostatic potential in monolayer, bilayer, and trilayer graphene," *Physical Review B*, vol. 80, no. 23, p. 235402, Dec. 2009. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevB.80.235402

[89] M. F. Craciun, S. Russo, M. Yamamoto, J. B. Oostinga, a. F. Morpurgo, and S. Tarucha, "Trilayer graphene is a semimetal with a gate-tunable band overlap." *Nature nanotechnology*, vol. 4, no. 6, pp. 383–388, Jun. 2009.

[90] Y.-W. Tan, Y. Zhang, K. Bolotin, Y. Zhao, S. Adam, E. H. Hwang, S. Das Sarma, H. L. Stormer, and P. Kim, "Measurement of Scattering Rate and Minimum Conductivity in Graphene," p. 246803, Dec. 2007. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.99.246803

[91] T. Fang, A. Konar, H. Xing, and D. Jena, "Carrier statistics and quantum capacitance of graphene sheets and ribbons," *Applied Physics Letters*, vol. 91, no. 9, p. 092109, Aug. 2007. [Online]. Available: http://dx.doi.org/10.1063/1.2776887

[92] P. Sharma, J. Perruisseau Carrier, and a. M. Ionescu, "Nanoelectromechanical microwave switch based on graphene," Coventry, United Kingdom, pp. 189–192, 2013. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6523516

[93] C. Jang, S. Adam, J.-H. Chen, E. D. Williams, S. Das Sarma, and M. S. Fuhrer, "Tuning the Effective Fine Structure Constant in Graphene: Opposing Effects of Dielectric Screening on Short- and Long-Range Potential Scattering," *Physical Review Letters*, vol. 101, no. 14, p. 146805, Oct. 2008. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.101.146805

[94] A. Konar, T. Fang, and D. Jena, "Effect of high-κ gate dielectrics on charge transport in graphene-based field effect transistors," *Physical Review B*, vol. 82, no. 11, pp. 1–7, Sep. 2010. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevB.82.115452

[95] J. Robertson, "High dielectric constant oxides," *The European Physical Journal Applied Physics*, vol. 28, no. 3, pp. 265–291, 2004.

[96] Laegu Kang, Byoung Hun Lee, Wen-Jie Qi, Yongjoo Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. Lee, "Electrical characteristics of highly reliable ultrathin hafnium oxide gate dielectric," *IEEE Electron Device Letters*, vol. 21, no. 4, pp. 181–183, 2000. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=830975

[97] J. S. Gomez-Diaz, J. Perruisseau-Carrier, P. Sharma, and A. Ionescu, "Non-contact characterization of graphene surface impedance at micro and millimeter waves," *Journal of Applied Physics*, vol. 111, no. 11, p. 114908, 2012. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/111/11/10.1063/1.4728183

[98] C. F. Moldovan, W. a. Vitale, P. Sharma, L. S. Bernard, and A. M. Ionescu, "Fabrication process and characterization of suspended graphene membranes for RF NEMS capacitive switches," *Microelectronic Engineering*, vol. 145, no. 0, pp. 5–8, 2015. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0167931715000416

[99] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, a. a. Firsov, a. F. K.S. Novoselov1, A.K. Geim1, S.V. Morozov2, D.

Jiang1, Y. Zhang1, S.V. Dubonos2, I.V.Grigorieva1, and K. Using, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004. [Online]. Available: http://arxiv.org/ftp/cond-mat/papers/0410/0410550.pdf$\delimiter"026E3B2$nhttp://www.sciencemag.org/content/306/5696/666.abstract

[100] G. M. Rebeiz, *RF MEMS: Theory, Design, and Technology.* New York, NY, USA: John Wiley & Sons, Inc., 2003.

[101] P. Li and T. Cui, "Single-crystalline graphene radio-frequency nanoswitches," *Journal of Micromechanics and Microengineering*, vol. 25, no. 7, p. 75022, 2015. [Online]. Available: http://stacks.iop.org/0960-1317/25/i=7/a=075022

[102] P. Li, T. Cui, and P. Instruments, "RF NANO SWITCH BASED ON SINGLE CRYSTALLINE GRAPHENE State Key Laboratory of Precision Measurement Technology and Instruments ,," in *2015 Transducers - 2015 18th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, no. c, 2015, pp. 307–310. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7180922

[103] S. a. Thiele, J. a. Schaefer, and F. Schwierz, "Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels," *Journal of Applied Physics*, vol. 107, no. 9, p. 094505, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/107/9/10.1063/1.3357398

[104] K. Parrish, M. Ramón, S. Banerjee, and D. Akinwande, "A Compact Model for Graphene FETs for Linear and Non-linear Circuits," in *in4.Iue.Tuwien.Ac.At*, 2012, pp. 75–78. [Online]. Available: http://in4.iue.tuwien.ac.at/pdfs/sispad2012/4-4.pdf

[105] S. Fregonese, M. Magallo, C. Maneux, H. Happy, and T. Zimmer, "Scalable Electrical Compact Modeling for Graphene FET Transistors," *IEEE Transactions on Nanotechnology*, vol. 12, no. 4, pp. 539–546, 2013. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6497529

[106] Han Wang, A. Hsu, Jing Kong, D. a. Antoniadis, and T. Palacios, "Compact Virtual-Source Current-Voltage Model for Top- and Back-Gated Graphene Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1523–1533, 2011. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5735198

[107] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nature Nanotechnology*, vol. 3, no. 11, pp. 654–659, 2008. [Online]. Available: http://www.nature.com/doifinder/10.1038/nnano.2008.268

[108] O. Habibpour, J. Vukusic, and J. Stake, "A Large-Signal Graphene FET Model," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 968–975, 2012. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6145637

[109] K. K. Thornber, "Relation of drift velocity to low-field mobility and high-field saturation velocity," *Journal of Applied Physics*, vol. 51, no. 4, p. 2127, 1980. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/51/4/10.1063/1.327885

[110] G. I. Zebrev, A. a. Tselykovskiy, D. K. Batmanova, and E. V. Melnik, "Small-Signal Capacitance and Current Parameter Modeling in Large-Scale High-Frequency Graphene Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1799–1806, 2013. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6515134

[111] I. Meric, C. Dean, A. Young, J. Hone, P. Kim, and K. L. Shepard, "Graphene field-effect transistors based on boron nitride gate dielectrics," in *2010 International Electron Devices Meeting*. IEEE, 2010, pp. 23.2.1–23.2.4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5703419

[112] F.-M. H., "Single crystals of graphite and mica as specimen support for electron microscopy," in *J. Appl. Phys.*, vol. 31, no. 10. AMER INST PHYSICS CIRCULATION FULFILLMENT DIV, 500 SUNNYSIDE BLVD, WOODBURY, NY 11797-2999, 1960, p. 1844.

[113] K. S. Novoselov, a. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and a. a. Firsov, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature*, vol. 438, no. 7065, pp. 197–200, 2005. [Online]. Available: http://www.nature.com/doifinder/10.1038/nature04233

[114] C. Berger, "Electronic Confinement and Coherence in Patterned Epitaxial Graphene," *Science*, vol. 312, no. 5777, pp. 1191–1196, 2006. [Online]. Available: http://www.sciencemag.org/cgi/doi/10.1126/science.1125925

[115] K. S. Novoselov, V. I. Falko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," *Nature*, vol. 490, no. 7419, pp. 192–200, 2012. [Online]. Available: http://dx.doi.org/10.1038/nature11458

[116] H. Hibino, H. Kageshima, F. Maeda, M. Nagase, Y. Kobayashi, and H. Yamaguchi, "Microscopic thickness determination of thin graphite films formed on SiC from quantized oscillation in reflectivity of low-energy electrons," *Physical Review B*, vol. 77, no. 7, p. 075413, 2008. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevB.77.075413

[117] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," *Nano Letters*, vol. 9, no. 1, pp. 30–35, 2009. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl801827v

[118] S. Rahimi, L. Tao, S. F. Chowdhury, S. Park, A. Jouvray, S. Buttress, N. Rupesinghe, K. Teo, and D. Akinwande, "Toward 300 mm Wafer-Scalable High-Performance Polycrystalline Chemical Vapor Deposited Graphene Transistors," *ACS Nano*, vol. 8, no. 10, pp. 10 471–10 479, 2014. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn5038493

[119] Q. Yu, J. Lian, S. Siriponglert, H. Li, Y. P. Chen, and S.-S. Pei, "Graphene segregated on Ni surfaces and transferred to insulators," *Applied Physics Letters*, vol. 93, no. 11, p. 113103, 2008. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/93/11/10.1063/1.2982585

[120] L. De Arco, Yi Zhang, a. Kumar, and Chongwu Zhou, "Synthesis, Transfer, and Devices of Single- and Few-Layer Graphene by Chemical Vapor Deposition," *IEEE Transactions on Nanotechnology*, vol. 8, no. 2, pp. 135–138, 2009. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4757291

[121] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, a. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, 2009. [Online]. Available: http://www.sciencemag.org/cgi/doi/10.1126/science.1171245

[122] L. Bernard, L. Syavoch, Forró, and A. Magrez, "Graphene: from Growth to Devices," Ph.D. dissertation, École polytechnique fédérale de Lausanne EPFL Switzerland, 2015. [Online]. Available: http://infoscience.epfl.ch/record/205097

[123] Q. Yu, L. a. Jauregui, W. Wu, R. Colby, J. Tian, Z. Su, H. Cao, Z. Liu, D. Pandey, D. Wei, T. F. Chung, P. Peng, N. P. Guisinger, E. a. Stach, J. Bao, S.-S. Pei, and Y. P. Chen, "Control and characterization of individual grains and grain boundaries in graphene grown by chemical vapour deposition," *Nature Materials*, vol. 10, no. 6, pp. 443–449, 2011. [Online]. Available: http://www.nature.com/doifinder/10.1038/nmat3010

[124] J. D. Wood, S. W. Schmucker, A. S. Lyons, E. Pop, and J. W. Lyding, "Effects of Polycrystalline Cu Substrate on Graphene Growth by Chemical Vapor Deposition," *Nano Letters*, vol. 11, no. 11, pp. 4547–4554, 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl201566c

[125] I. Vlassiouk, S. Smirnov, M. Regmi, S. P. Surwade, N. Srivastava, R. Feenstra, G. Eres, C. Parish, N. Lavrik, P. Datskos, S. Dai, and P. Fulvio, "Graphene Nucleation Density on Copper: Fundamental Role of Background Pressure," *The Journal of Physical Chemistry C*, vol. 117, no. 37, pp. 18 919–18 926, 2013. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/jp4047648

[126] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A Graphene Field-Effect Device," *IEEE Electron Device Letters*, vol. 28, no. 4, pp. 282–284, 2007. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4137639

[127] H. Xu, Z. Zhang, Z. Wang, S. Wang, X. Liang, and L.-M. Peng, "Quantum Capacitance Limited Vertical Scaling of Graphene Field-Effect Transistor," *ACS Nano*, vol. 5, no. 3, pp. 2340–2347, Mar. 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn200026e

[128] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al[sub 2]O[sub 3] dielectric," *Applied Physics Letters*, vol. 94, no. 6, p. 062107, 2009. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/94/6/10.1063/1.3077021

[129] Yu-Ming Lin, Hsin-Ying Chiu, K. Jenkins, D. Farmer, P. Avouris, and A. Valdes-Garcia, "Dual-Gate Graphene FETs With fT of 50 GHz," *IEEE Electron Device Letters*, vol. 31, no. 1, pp. 68–70, 2010. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5332372

[130] X. Liang, B. a. Sperling, I. Calizo, G. Cheng, C. A. Hacker, Q. Zhang, Y. Obeng, K. Yan, H. Peng, Q. Li, X. Zhu, H. Yuan, A. R. Hight Walker, Z. Liu, L.-m. Peng, and C. a. Richter, "Toward Clean and Crackless Transfer of Graphene," *ACS Nano*, vol. 5, no. 11, pp. 9144–9153, 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn203377t

[131] M. a. Fanton, J. a. Robinson, C. Puls, Y. Liu, M. J. Hollander, B. E. Weiland, M. LaBella, K. Trumbull, R. Kasarda, C. Howsare, J. Stitt, and D. W. Snyder, "Characterization of Graphene Films and Transistors Grown on Sapphire by Metal-Free Chemical Vapor Deposition," *ACS Nano*, vol. 5, no. 10, pp. 8062–8069, 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn202643t

[132] S. Roddaro, P. Pingue, V. Piazza, V. Pellegrini, and F. Beltram, "The Optical Visibility of Graphene: Interference Colors of Ultrathin Graphite on SiO2," *Nano Letters*, vol. 7, no. 9, pp. 2707–2710, 2007. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl071158l

[133] F. Xia, V. Perebeinos, Y.-m. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal-graphene junction resistance." *Nature nanotechnology*, vol. 6, no. 3, pp. 179–184, Mar. 2011. [Online]. Available: http://dx.doi.org/10.1038/nnano.2011.6http://www.nature.com/nnano/journal/v6/n3/abs/nnano.2011.6.html#supplementary-information

[134] B. Lee, S.-Y. Park, H.-C. Kim, K. Cho, E. M. Vogel, M. J. Kim, R. M. Wallace, and J. Kim, "Conformal Al2O3 dielectric layer deposited by atomic layer deposition for graphene-based nanoelectronics," *Applied Physics Letters*, vol. 92, no. 20, p. 203102, 2008. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/92/20/10.1063/1.2928228

[135] A. Pirkle, R. M. Wallace, and L. Colombo, "In situ studies of Al[sub 2]O[sub 3] and HfO[sub 2] dielectrics on graphite," *Applied Physics Letters*, vol. 95, no. 13, p. 133106, 2009. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/95/13/10.1063/1.3238560

[136] I. Meric, C. R. Dean, Shu-Jen Han, Lei Wang, K. a. Jenkins, J. Hone, and K. L. Shepard, "High-frequency performance of graphene field effect transistors with saturating IV-characteristics," in *2011 International Electron Devices Meeting*. IEEE, 2011, pp. 2.1.1–2.1.4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6131472

[137] S.-J. Han, K. a. Jenkins, A. Valdes Garcia, A. D. Franklin, A. a. Bol, and W. Haensch, "High-Frequency Graphene Voltage Amplifier," *Nano Letters*, vol. 11, no. 9, pp. 3690–3693, 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl2016637

[138] S.-J. Han, A. Valdes-Garcia, A. a. Bol, A. D. Franklin, D. Farmer, E. Kratschmer, K. a. Jenkins, and W. Haensch, "Graphene technology with inverted-T gate and RF passives on 200 mm platform," in *2011 International Electron Devices Meeting*. IEEE, 2011, pp. 2.2.1–2.2.4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6131473

[139] S.-J. Han, S. Oida, K. a. Jenkins, D. Lu, and Y. Zhu, "Multifinger Embedded T-Shaped Gate Graphene RF Transistors With High fMAX/fT Ratio," *IEEE Electron Device Letters*, vol. 34, no. 10, pp. 1340–1342, 2013. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6578134

[140] A. D. Franklin, A. Lin, H.-S. P. Wong, and Zhihong Chen, "Current Scaling in Aligned Carbon Nanotube Array Transistors With Local Bottom Gating," *IEEE Electron Device Letters*, vol. 31, no. 7, pp. 644–646, 2010. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5464369

[141] Dong-Wook Park, Tzu-Hsuan Chang, S. Mikael, Jung-Hun Seo, P. F. Nealey, and Zhenqiang Ma, "Graphene RF transistors with buried bottom gate," in *2013 IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2013, pp. 84–86. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6489440

[142] P. Blake, R. Yang, S. Morozov, F. Schedin, L. Ponomarenko, a.a. Zhukov, R. Nair, I. Grigorieva, K. Novoselov, and a.K. Geim, "Influence of metal contacts and charge inhomogeneity on transport properties of graphene near the neutrality point," *Solid State Communications*, vol. 149, no. 27-28, pp. 1068–1071, 2009. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0038109809001367

[143] A. Venugopal, L. Colombo, and E. M. Vogel, "Contact resistance in few and multilayer graphene devices," *Applied Physics Letters*, vol. 96, no. 1, pp. 3–5, 2010. [Online]. Available: http://link.aip.org/link/APPLAB/v96/i1/p013512/s1&Agg=doi

[144] H. Xu, Z. Zhang, H. Xu, Z. Wang, S. Wang, and L.-M. Peng, "Top-Gated Graphene Field-Effect Transistors with High Normalized Transconductance and Designable Dirac Point Voltage," *ACS Nano*, vol. 5, no. 6, pp. 5031–5037, 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn201115p

[145] Y. Gon Lee, Y. Ji Kim, C. Goo Kang, C. Cho, S. Lee, H. Jun Hwang, U. Jung, and B. Hun Lee, "Influence of extrinsic factors on accuracy of mobility extraction in graphene metal-oxide-semiconductor field effect transistors," *Applied Physics Letters*, vol. 102, no. 9, p. 093121, 2013. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/102/9/10.1063/1.4795295

Bibliography

[146] D. B. Farmer, H.-Y. Chiu, Y.-M. Lin, K. a. Jenkins, F. Xia, and P. Avouris, "Utilization of a Buffered Dielectric to Achieve High Field-Effect Carrier Mobility in Graphene Transistors," *Nano Letters*, vol. 9, no. 12, pp. 4474–4478, Dec. 2009. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl902788u

[147] D. B. Farmer, Y.-M. Lin, and P. Avouris, "Graphene field-effect transistors with self-aligned gates," *Applied Physics Letters*, vol. 97, no. 1, p. 13103, 2010.

[148] J. Lee, T.-J. Ha, H. Li, K. N. Parrish, M. Holt, A. Dodabalapur, R. S. Ruoff, and D. Akinwande, "25 GHz Embedded-Gate Graphene Transistors with High-K Dielectrics on Extremely Flexible Plastic Sheets," *ACS Nano*, vol. 7, no. 9, pp. 7744–7750, 2013. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn403487y

[149] J. Lee, L. Tao, K. N. Parrish, Y. Hao, R. S. Ruoff, and D. Akinwande, "Multi-finger flexible graphene field effect transistors with high bendability," *Applied Physics Letters*, vol. 101, no. 25, p. 252109, 2012. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/101/25/10.1063/1.4772541

[150] Y. Wang, B. Huang, and M. Zhang, "High performance graphene FETs with self-aligned buried gates fabricated on scalable patterned ni-catalyzed graphene," in *2011 Symposium on VLSI Technology*. IEEE, 2011, pp. 116–117. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5984667

[151] J. Lee, H.-Y. Chang, T.-J. Ha, H. Li, R. S. Ruoff, A. Dodabalapur, and D. Akinwande, "High-performance flexible nanoelectronics: 2D atomic channel materials for low-power digital and high-frequency analog devices," in *2013 IEEE International Electron Devices Meeting*. IEEE, 2013, pp. 19.2.1–19.2.4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6724658

[152] Y. Liang, X. Liang, Z. Zhang, W. Li, X. Huo, and L. Peng, "High mobility flexible graphene field-effect transistors and ambipolar radio-frequency circuits," *Nanoscale*, vol. 7, no. 25, pp. 10 954–10 962, 2015. [Online]. Available: http://xlink.rsc.org/?DOI=C5NR02292D

[153] C.-C. Lu, Y.-C. Lin, C.-H. Yeh, J.-C. Huang, and P.-W. Chiu, "High Mobility Flexible Graphene Field-Effect Transistors with Self-Healing Gate Dielectrics," *ACS Nano*, vol. 6, no. 5, pp. 4469–4474, 2012. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn301199j

[154] M. E. Ramon, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. P. Movva, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, "Three-Gigahertz Graphene Frequency Doubler on Quartz Operating Beyond the Transit Frequency," *IEEE Transactions on Nanotechnology*, vol. 11, no. 5, pp. 877–883, 2012. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6214614

[155] A. Venugopal, J. Chan, X. Li, C. W. Magnuson, W. P. Kirk, L. Colombo, R. S. Ruoff, and E. M. Vogel, "Effective mobility of single-layer graphene transistors as a function of channel

dimensions," *Journal of Applied Physics*, vol. 109, no. 10, p. 104511, 2011. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/109/10/10.1063/1.3592338

[156] J. Moon, D. Curtis, S. Bui, M. Hu, D. Gaskill, J. Tedesco, P. Asbeck, G. Jernigan, B. VanMil, R. Myers-Ward, C. Eddy, P. Campbell, and X. Weng, "Top-Gated Epitaxial Graphene FETs on Si-Face SiC Wafers With a Peak Transconductance of 600 mS/mm," *IEEE Electron Device Letters*, vol. 31, no. 4, pp. 260–262, 2010. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5420041

[157] a.W. Hull, "The Dynatron: A Vacuum Tube Possessing Negative Electric Resistance," *Proceedings of the IRE*, vol. 6, no. 1, pp. 5–35, 1918. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1646086

[158] L. Tonks, "Space Charge as a Cause of Negative Resistance in a Triode and Its Bearing on Short Wave Generation," *Physical Review*, vol. 30, no. 4, pp. 501–511, 1927. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRev.30.501

[159] C. Brunetti, "The clarification of average negative resistance with extensions of its use," *Radio Engineers, Proceedings of the Institute of*, vol. 25, no. 12, pp. 1595–1616, 1937.

[160] C. Brunetti and L. Greenough, "Some Characteristics of a Stable Negative Resistance," *Proceedings of the IRE*, vol. 30, no. 12, pp. 542–546, 1942. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1694416

[161] J. Gross, "Tuned Circuits Containing Negative Resistance," *Journal of Applied Physics*, vol. 27, no. 6, p. 603, 1956. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/27/6/10.1063/1.1722439

[162] L. Esaki, "New Phenomenon in Narrow Germanium p-n Junctions," *Physical Review*, vol. 109, no. 2, pp. 603–604, 1958. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRev.109.603

[163] M. Hines and W. Anderson, "High-frequency negative-resistance circuit principles for Esaki-diode applications," *1960 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, vol. III, no. 3, pp. 12–13, 1960. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1157279

[164] F. Capasso and R. a. Kiehl, "Resonant tunneling transistor with quantum well base and high-energy injection: A new negative differential resistance device," *Journal of Applied Physics*, vol. 58, no. 3, p. 1366, 1985. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/58/3/10.1063/1.336109

[165] J. Laskar, a.a. Ketterson, J. Baillargeon, T. Brock, I. Adesida, K. Cheng, and J. Kolodzey, "Gate-controlled negative differential resistance in drain current characteristics of AlGaAs/InGaAs/GaAs pseudomorphic MODFETs," *IEEE Electron Device Letters*, vol. 10, no. 12, pp. 528–530, 1989. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=43129

Bibliography

[166] S. Kang, B. Fallahazad, K. Lee, H. Movva, K. Kim, C. M. Corbet, T. Taniguchi, K. Watanabe, L. Colombo, L. F. Register, E. Tutuc, and S. K. Banerjee, "Bilayer Graphene-Hexagonal Boron Nitride Heterostructure Negative Differential Resistance Interlayer Tunnel FET," *IEEE Electron Device Letters*, vol. 36, no. 4, pp. 405–407, 2015. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7027824

[167] G. Liu, S. Ahsan, A. G. Khitun, R. K. Lake, and A. A. Balandin, "Graphene-based non-Boolean logic circuits," *Journal of Applied Physics*, vol. 114, no. 15, p. 154310, 2013.

[168] C.-C. Yang, K.-C. Huang, and Y.-K. Su, "Multi-peak NDR and high PVCR in GaAs/In-GaAs/InAs multi-stepped quantum well resonant interband tunnelling diodes," *Electronics Letters*, vol. 32, no. 8, pp. 774–775, 1996.

[169] H. Inokawa, A. Fujiwara, and Y. Takahashi, "Multipeak negative-differential-resistance device by combining single-electron and metal–oxide–semiconductor transistors," *Applied Physics Letters*, vol. 79, no. 22, p. 3618, 2001. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/79/22/10.1063/1.1421085

[170] R. Mathews, J. Sage, T. Sollner, S. Calawa, Chang-Lee Chen, L. Mahoney, P. Maki, and K. Molvar, "A new RTD-FET logic family," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 596–605, 1999. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=752517

[171] S. Sen, F. Capasso, a.Y. Cho, and D. Sivco, "Multiple-state resonant-tunneling bipolar transistor operating at room temperature and its application as a frequency multiplier," *IEEE Electron Device Letters*, vol. 9, no. 10, pp. 533–535, 1988. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=17835

[172] T. Broekaert, B. Brar, J. van der Wagt, a.C. Seabaugh, F. Morris, T. Moise, E. Beam, and G. Frazier, "A monolithic 4-bit 2-Gsps resonant tunneling analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 9, pp. 1342–1349, 1998. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=711333

[173] J. Huber, J. Chen, J. McCormack, C. Zhou, and M. Reed, "An RTD/transistor switching block and its possible application in binary and ternary adders," *IEEE Transactions on Electron Devices*, vol. 44, no. 12, pp. 2149–2153, 1997. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=644628

[174] J. Gunn, "Microwave oscillations of current in III-V semiconductors," *Solid State Communications*, vol. 88, no. 11-12, pp. 883–886, 1993. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/003810989390262L

[175] Z. L. Petrović and a. V. Phelps, "Oscillations of low-current electrical discharges between parallel-plane electrodes. I. dc discharges," *Physical Review E*, vol. 47, no. 4, pp. 2806–2815, 1993. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevE.47.2806

[176] M.-S. Gupta, "Large-signal equivalent circuit for IMPATT-diode characterization and its application to amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 21, no. 11, pp. 689–694, 1973.

[177] R. L. Franz, "Negative Differential Resistance Leads To Some Positive Results," *Electronic Design*, 2010. [Online]. Available: http://electronicdesign.com/archive/negative-differential-resistance-leads-some-positive-results

[178] J. O. Scanlan, *Analysis and synthesis of tunnel diode circuits.* John Wiley & Sons Ltd, 1966.

[179] W. J. Getsinger, "Prototypes for Use in Broadbanding Reflection Amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 11, no. 6, pp. 486–497, 1963.

[180] B. S. Perlman, C. L. Upadhyayula, and R. E. Marx, "Wide-band reflection-type transferred electron amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 18, no. 11, pp. 911–921, 1970.

[181] H. Tsai, Y. Su, H. Lin, R. Wang, and T. Lee, "P-N double quantum well resonant interband tunneling diode with peak-to-valley current ratio of 144 at room temperature," *IEEE Electron Device Letters*, vol. 15, no. 9, pp. 357–359, 1994. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=311133

[182] Y. Wu, D. B. Farmer, W. Zhu, S.-J. Han, C. D. Dimitrakopoulos, A. a. Bol, P. Avouris, and Y.-M. Lin, "Three-Terminal Graphene Negative Differential Resistance Devices," *ACS Nano*, vol. 6, no. 3, pp. 2610–2616, 2012. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn205106z

[183] S.-J. Han, D. Reddy, G. D. Carpenter, A. D. Franklin, and K. a. Jenkins, "Current Saturation in Submicrometer Graphene Transistors with Thin Gate Dielectric: Experiment, Simulation, and Theory," *ACS Nano*, vol. 6, no. 6, pp. 5220–5226, 2012. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn300978c

[184] P. Sharma, L. S. Bernard, A. Bazigos, A. Magrez, and A. M. Ionescu, "Room-Temperature Negative Differential Resistance in Graphene Field Effect Transistors: Experiments and Theory," *ACS Nano*, vol. 9, no. 1, pp. 620–625, 2015. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn5059437

[185] ——, "Negative Differential Resistance in Top-Gated Chemical Vapor Deposition grown graphene Transistors," in *Graphene Conference 2015*, Bilbao, Spain, 2015. [Online]. Available: http://www.phantomsnet.net/imaginenano/Abstracts2015/Graphene2015_sharma_pankaj_pankaj.sharma@epfl.ch_ndr-graphene-confv5.pdf

[186] ——, "Graphene Negative Differential Resistance Circuit With Voltage-Tunable High Performance at Room Temperature," *IEEE Electron Device Letters*, vol. 36, no. 8, pp. 865–867, 2015. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7124450

[187] P. Sharma, L. Bernard, a. Bazigos, a. Magrez, and a.M. Ionescu, "Graphene negative differential resistance (GNDR) circuit with enhanced performance at room temperature," in *2015 73rd Annual Device Research Conference (DRC)*. Columbus, OH, USA: IEEE, 2015, pp. 267–268. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/ epic03/wrapper.htm?arnumber=7175676

[188] V. Dorgan, "High-field transport in two-dimensional graphene and molybdenum disulfide," Ph.D. dissertation, University of Illinois at Urbana-Champaign, 2014.

[189] G. Junctions and G. Fiori, "Negative Differential Resistance in Mono and Bilayer," *Electron Device Letters, IEEE*, vol. 32, no. 10, pp. 1334–1336, 2011.

[190] L. Britnell, R. V. Gorbachev, a. K. Geim, L. a. Ponomarenko, a. Mishchenko, M. T. Greenaway, T. M. Fromhold, K. S. Novoselov, and L. Eaves, "Resonant tunnelling and negative differential conductance in graphene transistors." *Nature communications*, vol. 4, p. 1794, 2013. [Online]. Available: http://dx.doi.org/10.1038/ncomms2817

[191] A. Mishchenko, J. S. Tu, Y. Cao, R. V. Gorbachev, J. R. Wallbank, M. T. Greenaway, V. E. Morozov, S. V. Morozov, M. J. Zhu, S. L. Wong, and Others, "Twist-controlled resonant tunnelling in graphene/boron nitride/graphene heterostructures," *Nature nanotechnology*, vol. 9, no. 10, pp. 808–813, 2014.

[192] T. Roy, M. Tosun, X. Cao, H. Fang, D.-H. Lien, P. Zhao, Y.-Z. Chen, Y.-L. Chueh, J. Guo, and A. Javey, "Dual-Gated MoS2/WSe2 van der Waals Tunnel Diodes and Transistors," *ACS Nano*, vol. 9, no. 2, pp. 2071–2079, 2015. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn507278b

[193] B. Fallahazad, K. Lee, S. Kang, J. Xue, S. Larentis, C. Corbet, K. Kim, H. C. P. Movva, T. Taniguchi, K. Watanabe, L. F. Register, S. K. Banerjee, and E. Tutuc, "Gate-Tunable Resonant Tunneling in Double Bilayer Graphene Heterostructures," *Nano Letters*, vol. 15, no. 1, pp. 428–433, 2015. [Online]. Available: http: //pubs.acs.org/doi/abs/10.1021/nl503756y

[194] J. F. Rodriguez-Nieva, M. S. Dresselhaus, and L. S. Levitov, "Thermionic Emission and Negative dI/dV in Photoactive Graphene Heterostructures," *Nano Letters*, vol. 15, no. 3, pp. 1451–1456, 2015. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/ nl502522q

[195] Y. Zhao, Z. Wan, X. Xu, S. R. Patil, U. Hetmaniuk, and M. P. Anantram, "Negative Differential Resistance in Boron Nitride Graphene Heterostructures: Physical Mechanisms and Size Scaling Analysis," *Scientific Reports*, vol. 5, no. October 2014, p. 10712, 2015. [Online]. Available: http://www.nature.com/doifinder/10.1038/srep10712

[196] Y.-C. Lin, R. K. Ghosh, R. Addou, N. Lu, S. M. Eichfeld, H. Zhu, M.-Y. Li, X. Peng, M. J. Kim, L.-J. Li, R. M. Wallace, S. Datta, and J. a. Robinson, "Atomically thin resonant tunnel diodes built from synthetic van der Waals

heterostructures," *Nature Communications*, vol. 6, p. 7311, 2015. [Online]. Available: http://www.nature.com/doifinder/10.1038/ncomms8311

[197] S. Islam, Z. Li, V. E. Dorgan, M. H. Bae, and E. Pop, "Role of joule heating on current saturation and transient behavior of graphene transistors," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 166–168, 2013.

[198] L. Chua, J. Yu, and Y. Yu, "Bipolar-JFET-MOSFET negative resistance devices," *IEEE Transactions on Circuits and Systems*, vol. 32, no. 1, pp. 46–61, 1985. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1085599

[199] S.-L. Li, H. Miyazaki, A. Kumatani, A. Kanda, and K. Tsukagoshi, "Low Operating Bias and Matched Input-Output Characteristics in Graphene Logic Inverters," *Nano Letters*, vol. 10, no. 7, pp. 2357–2362, 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl100031x

[200] M. Bianchi, E. Guerriero, M. Fiocco, R. Alberti, L. Polloni, A. Behnam, E. a. Carrion, E. Pop, and R. Sordan, "Scaling of graphene integrated circuits," *Nanoscale*, vol. 7, no. 17, pp. 8076–8083, 2015. [Online]. Available: http://xlink.rsc.org/?DOI=C5NR01126D

[201] B. J. Kim, S.-K. Lee, M. S. Kang, J.-H. Ahn, and J. H. Cho, "Coplanar-Gate Transparent Graphene Transistors and Inverters on Plastic," *ACS Nano*, vol. 6, no. 10, pp. 8646–8651, 2012. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn3020486

[202] D. Ritter, G. Cohen, and C. Cytermann, "High peak tunnel current density Ga0.47In0.53As Esaki diodes," *Electronics Letters*, vol. 31, no. 17, pp. 1511–1512, 1995. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/el_19950979

[203] A. Ramesh, P. R. Berger, and R. Loo, "High 5.2 peak-to-valley current ratio in Si/SiGe resonant interband tunnel diodes grown by chemical vapor deposition," *Applied Physics Letters*, vol. 100, no. 9, p. 092104, 2012. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/100/9/10.1063/1.3684834

[204] J. Chen, "Large On-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device," *Science*, vol. 286, no. 5444, pp. 1550–1552, Nov. 1999. [Online]. Available: http://www.sciencemag.org/content/286/5444/1550.abstract

[205] M. Sholley, G. Barber, R. Lai, M. Barskey, R. Tsai, D. Streit, B. Osgood, J. Dowsing, M. Nishi-moto, Y. Kok, P. Huang, C. Gage, T. Huang, H. Nang, C. Jackson, Y. Chung, S. Chan, J. Mitchell, T. R. W. E. Space, T. Division, O. S. Park, and R. Beach, "119 GHz MMIC RADIOMETER FOR THE (IMAS) INTEGRATED MULTISPECTRAL ATMOSPHERIC SOUNDER," in *Microwave Symposium Digest, 1999 IEEE MTT-S International*, vol. 00, no. c. IEEE, 1999, pp. 5–8.

[206] G. Ng, R. Lai, Y. Hwang, H. Wang, D. Lo, T. Block, K. Tan, D. Streit, R. Dia, a. Freudenthal, P. Chow, and J. Berenz, "A fully passivated ultra low noise W-band

monolithic\nInGaAs/InAlAs/InP HEMT amplifier," in *IEEE 1995 Microwave and Millimeter-Wave. Monolithic Circuits Symposium. Digest of Papers.* IEEE, 1995, pp. 63–66.

[207] R. W. Laton, G. Haddad, and Others, "Characteristics of LMPATT-Diode Reflection Amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 21, no. 11, pp. 668–680, 1973.

[208] J. M. Pond, S. W. Kirchoefer, and E. J. Cukauskas, "Microwave amplification to 2.5 GHz in a quantum state transfer device," *Applied Physics Letters*, vol. 47, no. 11, p. 1175, 1985. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/47/11/10.1063/1.96317

[209] D. Rubin, "Millimeter-Wave Hybrid Coupled Reflection Amplifiers and Multiplexer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 30, no. 12, pp. 2156–2162, 1982. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1131400

[210] ——, "Hybrid Coupled Microstrip Reflection Amplifiers," in *IEEE MTT-S International Microwave Symposium Digest*, 1982, pp. 218–220.

[211] Shyh-Jong Chung, Shing-Ming Chen, and Yang-Chang Lee, "A novel bi-directional amplifier with applications in active van atta retrodirective arrays," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 2, pp. 542–547, 2003. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1179425

[212] B. D. Bates and P. J. Khan, "Multistage negative-resistance amplifier circuit design using nonideal circulators," *IEEE Journal of Solid-State Circuits*, vol. 16, pp. 400–406, 1981.

[213] A. C. Ferrari, F. Bonaccorso, V. Falko, K. S. Novoselov, S. Roche, P. Bø ggild, and S. Borini et al., "Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems," *Nanoscale*, vol. 7, no. 11, pp. 4598–4810, 2014. [Online]. Available: http://pubs.rsc.org/en/Content/ArticleLanding/2014/NR/C4NR01600A

[214] J. Gaskell, L. Eaves, K. S. Novoselov, a. Mishchenko, a. K. Geim, T. M. Fromhold, and M. T. Greenaway, "Graphene-hexagonal boron nitride resonant tunneling diodes as high-frequency oscillators," *Applied Physics Letters*, vol. 107, no. 10, p. 103105, 2015. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/107/10/10.1063/1.4930230

[215] L. Yu, A. Zubair, E. J. G. Santos, X. Zhang, Y. Lin, Y. Zhang, and T. Palacios, "High-Performance WSe2 Complementary Metal Oxide Semiconductor Technology and Integrated Circuits," *Nano Letters*, vol. 15, no. 8, pp. 4928–4934, 2015. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/acs.nanolett.5b00668

[216] M. Tosun, S. Chuang, H. Fang, A. B. Sachid, M. Hettick, Y. Lin, Y. Zeng, and A. Javey, "High-Gain Inverters Based on WSe2 Complementary Field-Effect

Transistors," *ACS Nano*, vol. 8, no. 5, pp. 4948–4953, 2014. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn5009929

List of Publications

Journal Papers

1. P. Sharma, L. Bernard, A. Bazigos, A. Magrez, and A. M. Ionescu, "Graphene Negative Differential Resistance Circuit with Voltage-Tunable High Performance at Room Temperature," **IEEE Electron Device Letters**, vol. 36, no. 8, pp. 865-867, 2015.

2. P. Sharma, L. S. Bernard, A. Bazigos, A. Magrez, and A. M. Ionescu, "Room-Temperature Negative Differential Resistance in Graphene Field Effect Transistors: Experiments and Theory," **ACS Nano**, vol. 9, no. 1, pp. 620–625, 2015.

3. C. F. Moldovan, W. A. Vitale, P. Sharma, L. S. Bernard, and A. M. Ionescu, "Fabrication process and characterization of suspended graphene membranes for RF NEMS capacitive switches," **Microelectronic Engineering**, vol. 145, no. 0, pp. 5–8, 2015.

4. P. Sharma, J. Perruisseau-Carrier, C. Moldovan, and A. M. Ionescu, "Electromagnetic Performance of RF NEMS Graphene Capacitive Switches," **IEEE Transactions of Nanotechnology**, vol. 13, no. 1, pp. 70–79, 2014.

5. J. S. Gomez-Diaz, J. Perruisseau-Carrier, P. Sharma, and A. Ionescu, "Non-contact characterization of graphene surface impedance at micro and millimeter waves," **Journal of Applied Physics**, vol. 111, no. 11, p. 114908, 2012.

Conference Papers

1. P. Sharma, L. Bernard, A. Bazigos, A. Magrez, and A. M. Ionescu, "Graphene negative differential resistance (GNDR) circuit with enhanced performance at room temperature," in **Device Research Conference (DRC)**, 2015 73rd Annual, 2015, pp. 267 – 268.

2. P. Sharma, L. S. Bernard, A. Bazigos, A. Magrez, and A. M. Ionescu, "Negative Differential Resistance in Top-Gated Chemical Vapor Deposition grown graphene Transistors," in **Graphene Conference**, 2015.

3. C. Moldovan, J. Perruisseau-Carrier, P. Sharma, and A. M. Ionescu, "RF NEMS based on suspended graphene structures," 4th **National Conference on Nano- and Micromechanics**, 2014.

Bibliography

4. <u>P. Sharma</u>, L. S. Bernard, A. Bazigos, A. Magrez, J. Perruisseau-Carrier, and A. M. Ionescu, "Fabrication and Characterization of Planar Embedded Gate Graphene Transistors without the use of Chemical Mechanical Polishing," in 40th International **Conference on Micro and Nano Engineering (MNE)**, Lausanne, Switzerland, 2014.

5. <u>P. Sharma</u>, J. Perruisseau Carrier, and A. M. Ionescu, "Nanoelectromechanical microwave switch based on graphene," 2013 14th International Conference on **Ultimate Integration on Silicon (ULIS). IEEE**, Coventry, United Kingdom, pp. 189–192, 2013.

6. <u>P. Sharma</u>, J. S. Gomez-Diaz, A. M. Ionescu, and J. Perruisseau-Carrier, "Determination of minimum conductivity of graphene from contactless microwaves measurements," in **Proceedings of the IEEE Conference on Nanotechnology**, 2012, pp. 1–4.

PANKAJ SHARMA

Email/Phone: pankajsync@gmail.com / +41788176515   Link: https://ch.linkedin.com/in/pankajsync

Address: ELB 331, CH-1015 Lausanne, Switzerland   Date of birth: 18 June, 1986

SUMMARY

- Specialist in multi-disciplinary nanotechnology research in solid-state devices and circuits using exploratory materials (such as 2D material graphene).
- Clean room experience (in industry and in academia) > 5 years.
- Semiconductor device physics expert: Modeling and Simulation (DC and RF).

EDUCATION

Jul' 11–Nov'15   **Ph.D. in Nanonoelectronics**   École Polytechnique Fédérale de Lausanne **Switzerland**

Jul' 09–Dec' 10   **MS in Microelectronics**   National University of Singapore **Singapore**

Aug' 03-May'07   **BS in Electrical Engineering**   National Institute of Technology, Rourkela **India**

WORK EXPERIENCE

EPFL Switzerland (PhD under Prof. A.M. Ionescu)   Jul' 11-Nov'15

- Experimentally demonstrated and proposed a mechanism for a unique negative differential resistance (NDR) phenomenon in graphene transistors.
- Proposed and demonstrated novel graphene circuit showing enhanced NDR, relevant for applications.
- Designed, modeled and characterized of graphene-based Nanoelectromechanical RF switches.
- Involvement in European GRAFOL project. Gave oral presentations and involved in discussions with multicultural team from academia and industry across Europe.
- Worked in Center of MicroNanoTechnology (Class 100 cleanroom) for fabrication of my devices.
- Published in impactful journals: ACS Nano, IEEE EDL and IEEE Trans. Nanotech., as first author.

Institute of Microelectronics, Singapore (Master's project in NUS Singapore)   Jan' 10-Dec' 10

- Supervisors: Prof. Sungjoo Lee (NUS) and Dr. Navab Singh (IME)
- Fabricated and characterized a non-volatile memory device based on Vertical Slit FET Design.
- Fabricated Gate-all-around silicon nanowire transistors with gate length down to 40 nm in the framework of project 'Neuromorphic Computing with Silicon Nanowire Transistors', with the group in Stanford university, USA. I was involved in conference meetings and active discussions with the team and delivered required milestones of the project.

ST Microelectronics Singapore (worked as Device engineer)   Jan' 11-Jun'11

- Worked as Device engineer in the development of Analog/Digital Bi-CMOS Technology.

Atos Origin Mumbai India (worked as Engineer)   Sep' 07-Jun'09

- Worked on the development of various internal websites for Renault France.
- Developed the website for Flight Testing Application for Airbus France.

- Worked on the different programming languages and frameworks such as Java, J2EE, SQL, Xml, Ajax, spring, hibernate and C/C++; for the development of websites.

RELEVANT SKILLS

Fabrication: Clean room experience in 100 mm (EPFL Switzerland), 150 mm (ST Microelectronics, Singapore) and 200 mm (IME Singapore) wafer fabrication facilities.

Simulation: Ansys HFSS, Matlab, Agilent ADS, L-Edit.

Characterization: DC to 110 GHz measurements techniques, cryogenic measurements.

Programming: Java, J2EE, Spring, Hibernate, C/C++, JSP, Ajax, PHP, Derby.

AWARDS AND EXTRACURRICULAR ACTIVITY

- Core member of Association Des Étudiants Indiens De Lausanne Yuva, a cultural organisation in EPFL.
- Won "Spirit Award for Team Excellence-Renault SBC Project" in Atos Origin.
- Best Algorithm prize in robotic event Distance Tracker Kshitij- 2006 at IIT Kharagpur.
- Ranked top 1 percent in 1st National Cyber Olympiad held (Jan 2002).