Energy-Proportional Single-Carrier Frequency Domain Equalization for mmWave Wireless Communication

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***Abstract*—mmWave wireless communication is proposed for high-throughput and high-density applications. Due to the large channel bandwidth, mmWave systems face a large variation in the observed delay spread. Many proposed single-carrier (SC) mmWave systems rely on cyclic-prefix (CP) frequency domain equalization (FDE) in order to deal with worst case channel conditions. A downside of CP-FDE receivers is their constant energy consumption independent of the actual channel conditions. The alternative overlap-save (OS) FDE receiver can adapt its complexity, but exhibits an inferior equalization performance. By proposing a hybrid FDE approach the receiver can adapt its complexity and therefor its power consumption dynamically to the given channel conditions. Using the structural similarity of overlap-save and cyclic-prefix FDE architectures the proposed hybrid receiver can switch between the two modes of operation with minimum required hardware overhead. It is shown that the proposed hybrid receiver can significantly reduce its complexity in benign channel conditions while still matching the equalization properties of a conventional CP-FDE receivers in very frequency selective environments.**

I. Introduction

Wireless communication at mmWave frequencies is considered to be an interesting candidate to satisfy the growing demand for wireless connectivity. The large amount of available spectrum at mmWave frequencies allows symbol rates of multiple GHz. However the significant increase of the carrier frequency comes with an amplified difficulty to design the analog front-end.

Hence, single-carrier (SC) modulation has regained popularity for mmWave because of its less stringent requirements for the analog components. Unfortunately, SC communication is severely impacted by frequency-selectivity of the channel. For multi-gigabit single-carrier (SC) modulated systems a non line-of-sight (NLOS) condition can result in inter-symbol-interference (ISI) of several dozens of symbol periods. Hence single-carrier (SC) cyclic-prefix frequency domain equalization (CP-FDE) as proposed in [1] was suggested for mmWave in [2] due to its excellent equalization performance combined with reasonable complexity. Several implementations of CP-FDE for SC mmWave systems have been demonstrated [3], [4], [5]. While such CP-FDE implementations are very universal, they suffer from a constant complexity and hence operate only very energy efficient in environments with large delay-spreads. For short delay spreads however more energy efficient time-domain solutions are known.

It is characteristic for mmWave environments that in the presence of a line-of-sight (LOS) transmission path or with very directed links the channel can be become nearly frequency-flat. For such nearly frequency-flat conditions time-domain linear equalizer (TD-LE) have been proposed [6] [7] [8]. It was further shown in [7] that such TD-LE can adjust their power-consumption to the channel conditions very well and achieve very high energy efficiency in flat-frequency channel conditions. Unfortunately the maximal delay-spreads such systems can handle is limited and therefor TD-LE can only operate in fewer mmWave channel scenarios compared to CP-FDE based systems.

A. Contribution

We propose a hybrid receiver architecture (cf. Fig. 1) that combines the complexity advantages of time-domain linear equalization (TD-LE) and frequency domain equalization (FDE). Especially it allows to scale the complexity of equalization and therefor the energy consumption of the receiver according to the actually encountered delay spread. It is shown that switching between optimal and suboptimal modes of operation based on the current channel realisation can significantly reduce the receiver complexity with only a small performance penalty. We further present a practical strategy to choose the best operation mode on a per-frame basis. Such a hybrid receiver can be implemented with very little overhead compared to a conventional frequency domain equalizer.

II. System Description

We assume a single-carrier modulated mmWave system with QAM modulation for point to point communication between a transmit (TX) node and a receive (RX) node.

We have defined three different representative mmWave scenarios to generate channel realisations.

- **Scenario A** is under LOS conditions. The path between the two antennas is not obstructed.
- **Scenario B** is under NLOS conditions, with the path between the two antennas obstructed, while beam-forming is employed on both the TX and RX side.

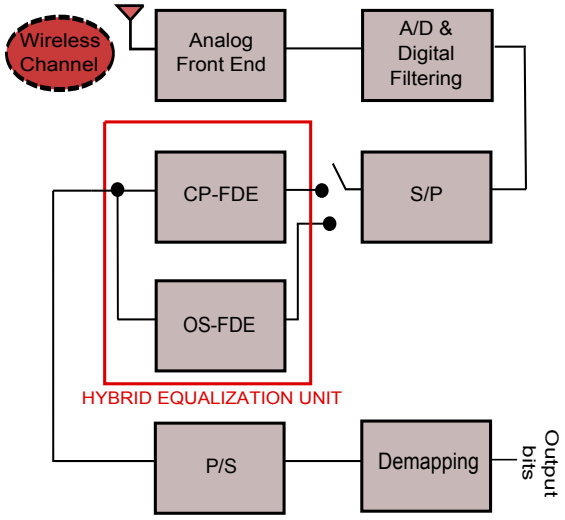


Fig. 1: Block Diagram Receiver

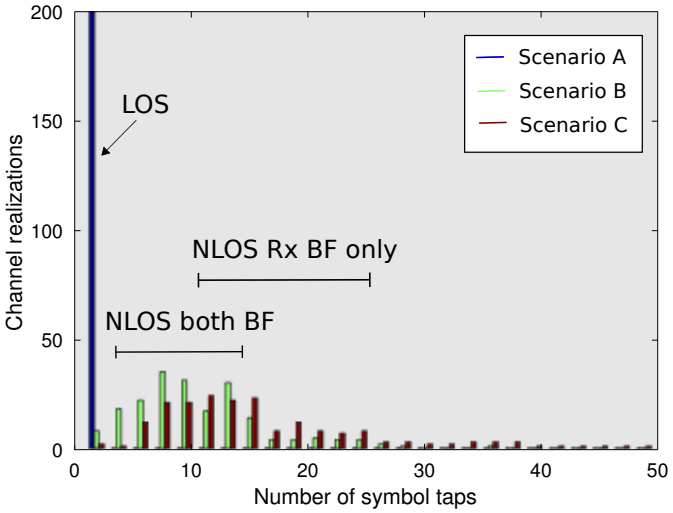


Fig. 2: Distribution of the excess delay spread for the three different representative mmWave scenarios with very different characteristics.

- **Scenario C** is under NLOS conditions, with the path between the two antennas obstructed, while beam-forming is only employed on the RX side.

The distribution of the excess delay spread for the three different proposed scenarios is shown in Fig. 2. The excess delay spread is measured as the smallest window which comprises more then 90% of the channel energy. It can be seen that for the different scenarios there are huge variations in the distribution of the delay spread, which varies between a single tap and dozen of symbol periods. We assume a maximum of 64 symbols of delay spread for which the receiver should be still operable.

III. mmWave Equalization

In situations with a large variation of channel conditions, the need for reliable operation mandates that a receiver anticipates all possible channel conditions. As a result, wireless receivers are generally designed to fulfill worst-case constraints, which are only applicable during a fraction of the operation time.

A. Cyclic Prefix-Frequency Domain Equalization

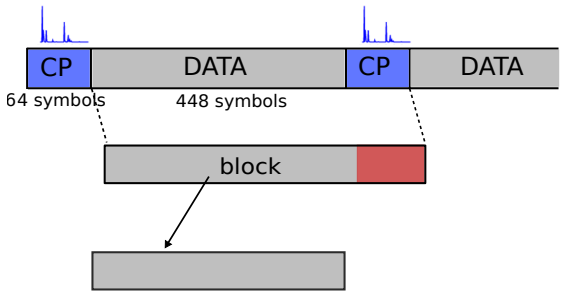
Single-carrier CP-FDE systems require a frame structure which ensures that the channel matrix for each block is circular. Such a structure can be achieved by inserting pilot words as cyclic prefix in regular intervals between data. The resulting circular channel matrix can then be decomposed by using the discrete Fourier transform (DFT) and the channel can be perfectly reversed. The inserted pilot words serve not only as a cyclic prefix for the successive data, but form with the preceding chunk of payload data the blocks for the CP-FDE. Unlike for orthogonal frequency division multiplex (OFDM) the cyclic prefix is part of the equalized block in CP-FDE systems. Hence the length of the cyclic prefix impacts not only the data rate, but also the complexity of equalization. An increase in delay spread requires therefor also an increase in block length to achieve the same efficiency.

The possibility to use the fast-fourier-transform (FFT) for the conversion to and from frequency-domain makes CP-FDE implementations efficient for long block lengths and results in a lower complexity of CP-FDE for long delay spreads compared to TD-LE. In practice the equalization block length (EBL) and therefor the complexity of the CP-FDE system is fixed by the given frame structure, based on the maximal expected delay spread.

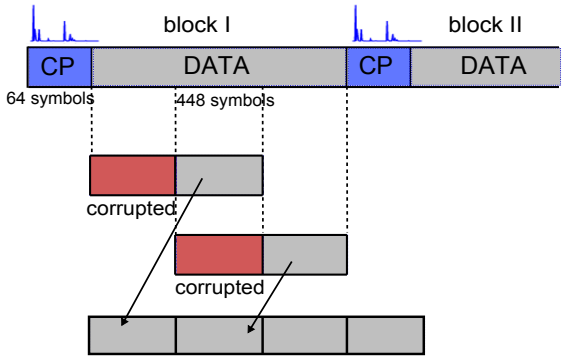
A typical frame structure for CP-FDE in a mmWave scenario would be an EBL of 512 symbol, with 448 payload symbols and a pilot word length of 64 symbols, which can operate under an excess delay spread of up to 65 symbols. With such a frame structure a CP-FDE based system is not very power efficient in situations with a delay spread which is significantly smaller then 65 symbols. A possible solution to overcome the limitations of the CP-FDE receiver is the dynamic adjustment of the frame format. Unfortunately such a solution requires channel state information (CSI) on the TX side before transmission.

B. Overlap-Save Frequency Domain Equalization

Overlap-save frequency domain equalization (OS-FDE) is an alternative algorithm to perform equalization presented in [1]. OS-FDE does not require a cyclic frame structure, instead it uses the effect that corruption due to non-circular channel conditions is concentrated on the beginning of the equalized block. Hence OS-FDE performs equalization in the same way as CP-FDE algorithm using the DFT for conversion between frequency and time domain, but corruption due to the missing cyclic prefix is mitigated by discarding the initial segment of the equalized block. Unlike for CP-FDE during OS-FDE perfect channel inversion can not be guaranteed and there is residual interference. Because of the discarded



(a) Cyclic-prefix (CP) mode



(b) Overlap-save (OS) mode

Fig. 3: The two operations mode of the proposed energy-proportional hybrid equalizer.

initial segment, the OS-FDE equalizer needs to operate on overlapping segments of the received symbol stream as shown in Fig. 3b. It is reported that an overlap of 50% results in a good balance between block length and equalization performance. On average each received symbol is processed more than once by the equalizer, which makes OS-FDE less efficient compared to CP-FDE for the same EBL. Nevertheless OS-FDE can be more efficient, if it uses a smaller EBL.

IV. Energy Proportional FDE

A flexible approach combining CP-FDE and OS-FDE is proposed which does not require dynamic adaptation of the frame format. Energy proportional FDE (EP-FDE) is based on a reconfigurable dual-FFT unit which can switch between between a conventional cyclic-prefix FDE (CP-FDE) and an overlap-save FDE (OS-FDE) mode. Such a hybrid receiver can choose between OS-FDE with various block lengths and CP-FDE. While in general the OS-FDE is more complex than CP-FDE for the same equalization block length, the OS-FDE can adapt its equalization block length independently of the structure of the frame. For a short excess delay spread OS-FDE with a small EBL can provide sufficient equalization with less computational complexity compared to CP-FDE. The ability to switch between CP-FDE and OS-FDE operation allows to choose the configuration with the lowest complexity which provides sufficient equalization performance without sacrificing worst-case equalization capabilities.

TABLE I: Equalization complexity for a frame block of 512 symbols

EBL	8	16	32	64	512
OS-FDE	1344	2016	2800	3640	7184
CP-FDE	-	-	-	-	3592

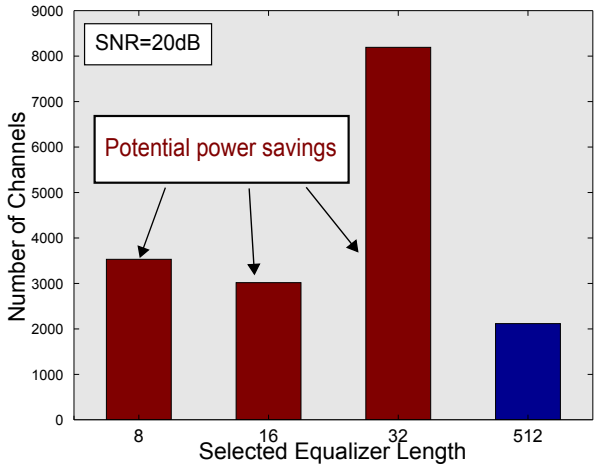


Fig. 4: Distribution of selected EBL in genie-aided hybrid receiver for different channel realizations.

The complexity of the different operation modes is quantified by the number of required non-trivial complex multiplications, which is a common measure for the complexity of FFTs. The number of complex multiplications required to equalize a block of 512 symbols using the CP-FDE and OS-FDE algorithm with different EBLs is given in Table I. It can be seen that only for EBL below 64 using the OS-FDE schemes reduces the complexity.

The hardware overhead of a hybrid compared to a conventional CP-FDE only receiver is negligible as the OS-FDE and CP-FDE use essentially the same hardware resources. Always choosing the optimal configuration promises a significant reduction of overall complexity, but it is not obvious how to determine the optimal block size.

A. Genie-aided Hybrid Receiver

A genie-aided approach is suggested in order to derive an upper bound for the possible complexity reduction by the proposed hybrid equalization scheme. For such a genie-aided receiver, we assume perfect knowledge of the resulting BER of all eligible configurations in advance. Based on this knowledge the configuration with the lowest complexity which still achieves the minimum number of bit errors is chosen for equalization.

It is clear that the genie-aided hybrid scheme will always achieve a performance at least as good as the CP-FDE only receiver. If for some channel realisations a smaller EBL can be chosen, the hybrid scheme achieves an average equalization complexity reduction compared to the CP-FDE only receiver. The distribution of selected EBL in Fig. 6 shows that in the majority of channel realizations a smaller EBL can be chosen.

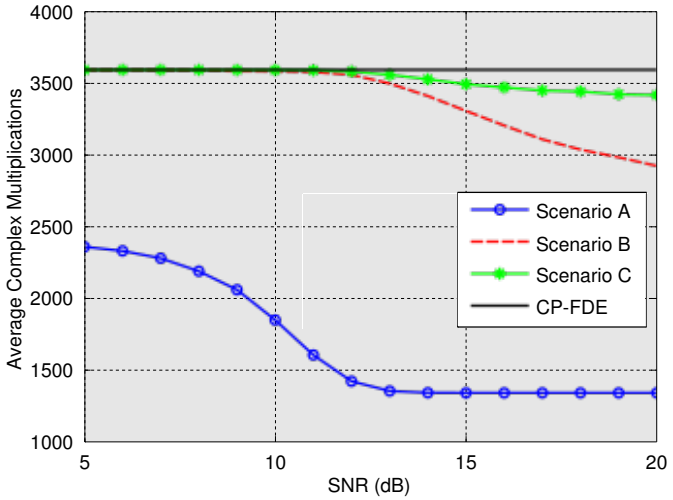


Fig. 5: Comparison of the complexity of the genie-based hybrid receiver with a pure CP-FDE receiver for the three selected channel conditions.

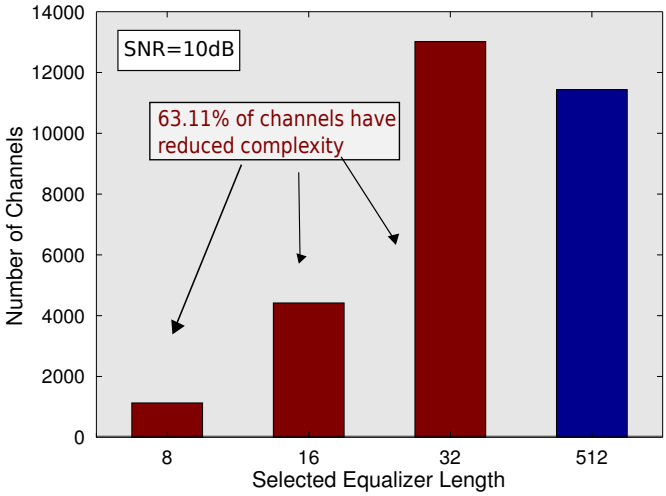


Fig. 6: Selected equalization block length (EBL) in practical receiver for different channel realizations (SNR=10dB)

In Fig. 5 it can be seen that the Genie-based receiver can leverage the channel conditions in the different scenarios to adapt its complexity. In scenario A and B, the average complexity required for equalization can be significantly reduced compared to a CP-FDE only based equalizer.

B. Practical Hybrid Receiver

The genie-aided approach is obviously not suitable for practical receiver implementations. Therefor a practical algorithm which approximates the optimal configuration choice is proposed. Our practical algorithm is sufficiently low in complexity so that it can be performed on-the-fly during the reception of a frame.

As criterion for the choice of the appropriate equalization block length we propose a minimal post-equalization signal-to-interference ratio (SIR). An estimate of the resulting SIR is calculated for each equalization block length from the residual post-equalization channel impulse response (CIR). The residual post-equalization CIR is obtained from the convolution of the estimated CIR with the time-domain response of the equalizer. Although the SIR calculation is only an approximation it will be shown later, that it gives a sufficiently good criterion to judge the quality of equalization. Determining the equalization block length using the SIR criterion allows a complexity reduction for 63% of the channel realizations as shown in Fig. 6. This value depends on the used channel scenario, the operating SNR and the target SIR.

One possible way to define the SIR requirement is, as a function of the current SNR with a back-off parameter b as margin.

$$\mathrm{SIR} = \mathrm{SNR} + b \tag{1}$$

The parameter b offers a performance-complexity trade-off that can be adjusted based on high level considerations as the currently available power budget for the receiver. A small value for b allows a larger amount of interference and hence is more easily satisfied by a shorter equalization block length.

The proposed procedure to determine the SIR is simple enough such that a receiver can try all candidate EBL at the beginning of each frame. In order to avoid costly buffering of received symbols, a mmWave receiver implementing EP-FDE already begins equalization using the CP-FDE algorithm while in parallel determining the appropriate reduced complexity block size. Because of the very long frame size of mmWave systems, this initial increased complexity will not affect the overall complexity reduction.

V. Results

Comparing the complexity of the practical hybrid receiver to a pure CP-FDE as given in Fig. 7 shows that the algorithm adapts to the different channel scenarios. In scenario C the receiver will use nearly exclusively the CP-FDE operation mode and therefor offer the same equalization performance as CP-FDE only receiver, while for scenario A and B a significant complexity reduction can be achieved because of the reduced delay spread. It can also be seen that especially for the scenario B the receiver makes use of the current signal-to-noise operating condition in order to determine the appropriate level of equalization.

This adaptation can be explained by the application of the SNR-based SIR requirement as previously explained. In Fig. 8 it is shown that the resulting equalization complexity decreases with a decreasing back-off parameter. Then again a higher back-off parameter leads to a better performance and reduces the performance gap to the ideal CP-FDE only equalizer as can be seen in Fig. 9.

VI. Conclusion

We have shown that a hybrid FDE approach can unite the advantages of excellent equalization capabilities with energy-proportional complexity scaling in the receiver. The proposed algorithm chooses between CP-FDE and OS-FDE with variable equalization block length based on the encountered delay spread and the given performance requirement.

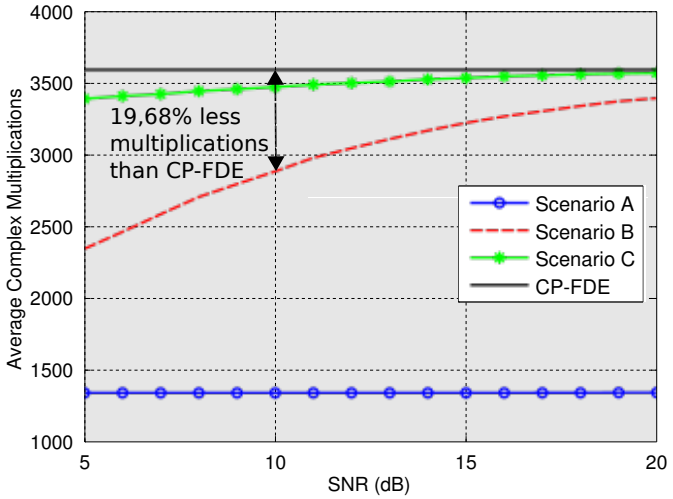


Fig. 7: Complexity comparison of the practical receiver vs CP-FDE for the three defined channel scenarios with the CP-FDE equalizer. Complexity of the CP-FDE is independent of the channel scenario.

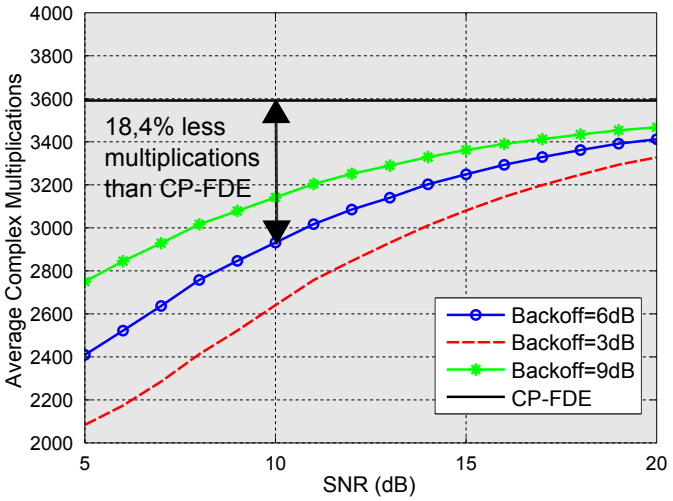


Fig. 8: Complexity of the practical hybrid receiver for different back-off parameters.

Using this hybrid approach such a receiver can achieve significant power savings in frequency flat conditions while still preserving the same performance as a pure CP-FDE for frequency selective scenarios. A practical approach was presented which can determine the appropriate block size during the reception of the frame. A back-off parameter provides a trade-off between the aggressiveness of the complexity reduction and gap to ideal performance.

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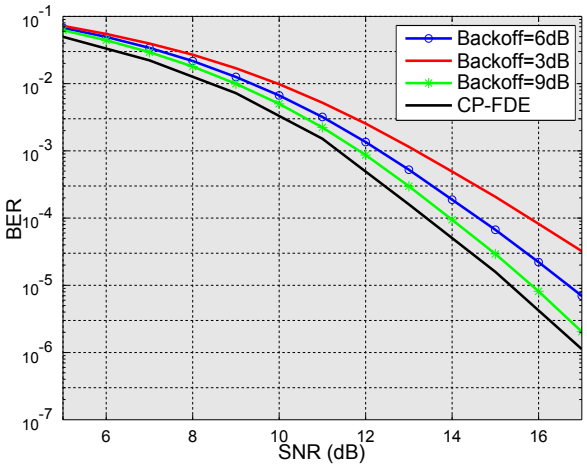

Fig. 9: Performance comparisons of the practical hybrid receivers with different back-off parameters to an ideal CP-FDE only receiver.

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