

Advanced Architectures and Processing for High-Efficiency Silicon Heterojunction Solar Cells

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Résumé

Les cellules solaires basées sur un substrat de silicium cristallin représentent de nos jours la majeure partie du marché du photovoltaïque. Afin de répondre à la demande croissante pour des dispositifs à plus haut rendement, la technologie dite des hétérojonctions silicium, basée sur une plaquette de silicium cristallin et sur de fines couches de silicium amorphes (a-Si:H) qui permettent la réalisation de contacts dits passivants, peut être considérée comme étant l'une des approches les plus prometteuse pour la prochaine génération de cellules photovoltaïques. Ces cellules solaires ont démontré des efficacités record rendues possible par la grande qualité de la passivation de surface conduisant à une tension de circuit ouvert proche des limites théoriques. Cependant, malgré de bonnes propriétés électroniques, les couches a-Si:H induisent d'importantes pertes optiques causées par la faible largeur de bande interdite de ce matériau. Le but de cette thèse est de limiter ces pertes en développant de nouvelles architectures de cellule et de nouveaux procédés de fabrication.

Les principaux résultats de ce travail se déclinent en quatre parties : Premièrement, une nouvelle structure découplant les propriétés optiques et électroniques des couches avant grâce à l'introduction de contacts localisés est étudiée. En utilisant une technique de masquage pour la structuration de ces couches, nous avons démontré la faisabilité d'une telle cellule si une surface de contact suffisamment importante est maintenue. Deuxièmement, en vue de la structuration des couches a-Si:H, nous avons développé un procédé d'attaque basé sur un plasma hydrogène dans un réacteur PECVD. En outre, nous avons démontré l'existence d'une épaisseur critique de la couche a-Si:H intrinsèque nécessaire afin de protéger l'interface amorphe/cristallin. Ainsi, cette technique permet la structuration de couche de a-Si:H avec une précision nanométrique tout en préservant la passivation de surface. Le troisième résultat important de cette thèse est le développement d'une métallisation à l'avant—habituellement réalisée par sérigraphie d'une pâte d'argent—par une électrode déposée par galvanoplastie de cuivre. Afin d'assurer une bonne adhésion de cette métallisation, un premier procédé basé sur une double couche de nickel et cuivre est étudié. D'importants gains optiques sont obtenus par ce biais grâce à la réduction de la taille des géométries de $70\text{ }\mu\text{m}$ à $15\text{ }\mu\text{m}$ conduisant à une amélioration du courant de court-circuit de 1.1 mA cm^{-2} . Dans un deuxième temps, un procédé simplifié basé sur une couche d'accroche en cuivre est proposé et révèle une meilleure adhésion de la métallisation ainsi qu'une bonne compatibilité avec des oxydes transparents conducteurs (TCO) sensibles aux attaques chimiques tels que les matériaux basés sur l'oxyde de zinc. Le quatrième résultat notable de ce travail est le remplacement de la couche de a-Si:H dopée p formant le collecteur de trou par un film hautement transparent

d'oxyde de molybdène (MoO_x). Nous avons montré que ce matériau agit efficacement comme collecteur de trou si les procédés ultérieurs à sa déposition ne dépassent pas les 130°C . D'un point-de-vue optique, cette couche permet une amélioration équivalente à 0.8 mA cm^{-2} de la réponse de la cellule dans la partie bleue du spectre solaire. Cependant, ce gain est réduit par la modification du MoO_x induite par la déposition du TCO conduisant à une absorption parasite de la lumière. Finalement, en combinant un collecteur de trou en MoO_x avec une métallisation à l'avant en cuivre électrodéposée, un impressionnant facteur de forme de la courbe courant-tension de 80.3% est obtenu permettant une efficacité certifiée de 22.5% pour une cellule de 4 cm^2 .

Mots clefs : cellule solaire en silicium, haute efficacité, hétérojonctions silicium, PECVD, sputtering, électrodéposition de cuivre, gravure par plasma d'hydrogène, oxyde de molybdène, oxyde transparent conducteur, transport de porteur de charge, silicium amorphe.

Abstract

Crystalline silicon solar cells currently represent the largest part of the photovoltaic market. In response to the demand for higher efficiency devices, silicon heterojunction technology, which merges a crystalline silicon wafer with thin amorphous silicon (a-Si:H) films enabling the achievement of passivating contacts, may be considered as one of the most promising approaches for the next generation of industrial solar cells. These cells demonstrate record energy conversion efficiency enabled by excellent surface passivation leading to open-circuit voltages close to the theoretical limit. Despite the remarkable electronic properties of a-Si:H, its narrow bandgap induces significant parasitic light absorption. The aim of this thesis is to mitigate this loss through novel cell architectures and new fabrication processes.

The outcome of this work is four-fold: First, a new silicon heterojunction solar cell structure is investigated that decouples the optical and electrical properties of the window layers through localized front contacts. By using shadow masking for the film patterning, we demonstrate the feasibility of the new cell structure under the condition that a sufficiently high contact coverage be maintained. Second, for the patterning of a-Si:H layers, we develop a hydrogen plasma etching technique carried out in a PECVD reactor. In particular, we show that a critical thickness of the intrinsic a-Si:H layer is needed to provide sufficient shielding of the amorphous/crystalline interface to ensure good passivation. This technique enables the patterning of a-Si:H layers with nanometric accuracy while preserving the surface passivation. A third important outcome of this thesis is the replacement of the front metallization—usually made by screen-printing of a silver paste—with a copper front grid formed by electrodeposition. To ensure sufficient adhesion of the metallic fingers, a first process based on a double electrodeposition of a nickel/copper stack is presented. Important improvements in light management are realized with this metallization scheme, reducing the finger width from $70\text{ }\mu\text{m}$ to $15\text{ }\mu\text{m}$ which leads to a short-circuit gain of 1.1 mA cm^{-2} . In a second step, a simplified process based on a copper seed layer is proposed, further improving the metallization adhesion and making this technique compatible with chemically sensitive transparent conductive oxides such as zinc-oxide-based materials. The fourth outcome of this work is the replacement of the p-doped a-Si:H hole collector with a highly transparent molybdenum oxide (MoO_x) film. We show that this material is an efficient hole collector if the post-deposition processes are carried out below $130\text{ }^\circ\text{C}$. From an optical point of view, this layer enables an improvement equivalent to 0.8 mA cm^{-2} of the cell's response in the blue part of the spectrum. Nevertheless, this gain is reduced by the modification of the MoO_x film induced during the TCO sputtering process, which leads to broadband parasitic light absorption. Finally, by merging this MoO_x

hole collector with the electrodeposited copper front metallization, remarkable fill factors of 80.3% are obtained leading to a certified efficiency of 22.5% for a 4 cm² solar cell.

Key words: silicon solar cells, high-efficiency, silicon heterojunction, PECVD, sputtering, copper electrodeposition, hydrogen plasma etching, molybdenum oxide, transparent conductive oxide, charge carrier transport, amorphous silicon.

Contents

Abstract (Français/English)	i
Table of Contents	ix
List of abbreviations and symbols	xi
1 Introduction	1
1.1 General context	1
1.1.1 Photovoltaics as a major contributor to electricity production	1
1.1.2 Brief historical overview	2
1.1.3 Semiconductor physics in solar cells	4
1.1.4 Fundamental operation of a solar cell	8
1.1.5 Photovoltaic limitations	11
1.1.6 Overview of the technology	16
1.1.7 High-temperature crystalline silicon solar cell	16
1.1.8 Silicon heterojunction solar cells	20
1.2 Motivations	21
1.3 Objectives and structure	22
1.3.1 Objectives	22
1.3.2 Structure	23
1.4 Contribution to the field	23
2 Experimental processes and characterization	25
2.1 SHJ baseline process flow overview	25
2.2 Silicon heterojunction solar cell fabrication equipments	26
2.2.1 Wafer texturing and cleaning	26
2.2.2 Plasma-enhanced chemical vapor deposition	26
2.2.3 Transparent conductive oxides and metal sputtering deposition	28
2.2.4 Zinc oxide low-pressure chemical vapor deposition	28
2.2.5 Metals and dielectrics thermal evaporation	29
2.2.6 Silver paste screen-printing metallization	29
2.2.7 Photolithography	29
2.3 Layer characterization	30
2.3.1 Line-, sheet- and contact-resistance measurements	30

2.3.2	Spectroscopic ellipsometry	30
2.3.3	Spectrophotometer	31
2.4	Solar cell characterization	31
2.4.1	Minority-carrier lifetime measurement	31
2.4.2	Illuminated J - V	32
2.4.3	External and internal quantum efficiency	33
2.4.4	Suns V_{OC} measurement	35
2.4.5	Photoluminescence	35
3	Silicon Heterojunction solar cells front-metallization by copper electrodeposition	37
3.1	Introduction and motivation	37
3.1.1	Motivation [†]	38
3.1.2	State-of-the-art of Cu electrodeposition techniques for SHJ solar cells [†] .	39
3.2	Photolithography processes for electrodeposition patterning	40
3.2.1	Photoresist dispensing	41
3.3	Electrodeposition setups	42
3.4	Nickel-Copper front electrodes	43
3.4.1	Experimental [†]	43
3.4.2	Results and discussions [†]	44
3.4.3	Characterization of Ni-Cu metallization by electron microscopy [†]	48
3.4.4	Implementation in high-efficiency SHJ solar cells [†]	50
3.4.5	Conclusions [†]	52
3.5	Towards more versatility and reliability in electrodeposited front-contact	53
3.5.1	Cu-seed layer based electrodeposition process	53
3.5.2	Cu seed-layer back-etching optimization	53
3.5.3	Impact of the Cu seed-layer removal on the a-Si:H surface passivation .	55
3.6	Electrodeposited Cu front-grid on IZO front TCO	55
3.6.1	Motivation for IZO as the front-TCO	55
3.6.2	Experimental	56
3.6.3	Results and discussions	56
3.6.4	Conclusions	58
3.7	Electrodeposited Cu front-grid on LPCVD ZnO:B front-TCO	58
3.7.1	Motivation	58
3.7.2	Experimental	59
3.7.3	Conclusion	61
3.8	Metallization of interdigitated back-contacted silicon heterojunction solar cells	62
3.8.1	Motivation	62
3.8.2	Results and discussion	63
3.8.3	Conclusion	63
3.9	General conclusions on metallization by copper electroplating	63

4	Patterning amorphous silicon layers by hydrogen plasma and wet chemical etching	65
4.1	Introduction and motivation	65
4.2	a-Si:H patterning by wet chemical etching	68
4.2.1	Introduction	68
4.2.2	Experimental	68
4.2.3	Results and discussions	68
4.2.4	Conclusions	69
4.3	Selective etching of doped a-Si:H layers by H ₂ plasma etching [†]	70
4.3.1	Introduction [†]	70
4.3.2	Experimental [†]	71
4.3.3	Effect of hydrogen plasma on surface passivation [†]	71
4.3.4	High resolution transmission electron microscopy investigation of the a-Si:H/c-Si interface [†]	73
4.3.5	Study of a-Si:H film microstructure by attenuated total reflectance Fourier transform infrared spectroscopy [†]	74
4.3.6	Study of hydrogen incorporation in a-Si:H films by H ₂ and D ₂ thermal desorption spectroscopy [†]	76
4.3.7	Conclusions [†]	76
4.4	Influence of H ₂ plasma etching on SHJ device performance	77
4.4.1	Introduction	77
4.4.2	Study of charge-carrier transport in a-Si:H(<i>i</i>) layers exposed to H ₂ plasma etching	78
4.4.3	Doped a-Si:H layer patterning by H ₂ plasma etching on wafers with random pyramids texture	79
4.4.4	Conclusion	79
4.5	General conclusions on a-Si:H film patterning	80
5	Localized front contact silicon heterojunction solar cells	83
5.1	Introduction	84
5.1.1	Motivations	84
5.1.2	Localized contacts in SHJ devices	85
5.2	Light-beam-induced current measurement setup	86
5.2.1	Introduction	86
5.2.2	Experimental setup	86
5.3	LEP devices with a patterned front TCO	88
5.3.1	Introduction	88
5.3.2	Experimental	88
5.3.3	Results and discussion	89
5.3.4	Conclusions	91
5.4	Rear hole collector configuration	91
5.4.1	Motivation	91
5.4.2	Experimental	92

5.4.3	Results and discussion	92
5.4.4	Conclusions	93
5.5	LEP devices with a patterned front a-Si:H layer	94
5.5.1	Introduction	94
5.5.2	Experiments	95
5.5.3	Results and discussion	95
5.5.4	Electrical model and simulations	97
5.5.5	Conclusions	99
5.6	Low-contact-coverage LEP devices	100
5.6.1	Self-masked ZnO etching	101
5.6.2	Impact of silicon nitride deposition on surface passivation	101
5.6.3	Conclusions	102
5.7	Modular LEP devices	103
5.7.1	Experimental	103
5.7.2	Results and discussion	103
5.7.3	Conclusions	104
5.8	General conclusions on LEP-SHJ devices	104
6	Transition metal oxide films as a-Si:H(<i>p</i>) replacement	107
6.1	Introduction and motivation	107
6.1.1	Motivation [†]	108
6.1.2	Band diagram and carrier extraction in TMO-based hole-collector SHJ solar cells	108
6.2	Experimental	109
6.3	Optical properties and films microstructure of MoO _x -based hole-collector . . .	110
6.3.1	Annealing and TCO sputtering impact on MoO _x optical properties [†] . . .	110
6.3.2	Impact of plasma treatments on TMO thin films	112
6.3.3	Molybdenum oxide film microstructure and interfaces [†]	113
6.4	Surface passivation of a-Si:H(<i>i</i>)/ MoO _x hole collector and impact of annealing .	115
6.4.1	Annealing impact on un-capped MoO _x hole collector [†]	115
6.4.2	Annealing impact on TCO-capped MoO _x hole collector	116
6.4.3	Annealing impact on the open-circuit voltage	117
6.5	Molybdenum oxide based SHJ solar cells	117
6.5.1	Impact of the annealing on the device performance [†]	117
6.5.2	Impact of a-Si:H(<i>i</i>) layer thickness on hole collection in MoO _x -based SHJ solar cells	118
6.5.3	Comparison of MoO _x - and a-Si:H(<i>p</i>)-based SHJ device performance [†] . .	119
6.5.4	Temperature dependence of the efficiency for MoO _x -based SHJ devices	120
6.6	Alternative TCOs for MoO _x hole collector	121
6.6.1	LPCVD ZnO:B as MoO _x hole-collector contact	121
6.6.2	Sputtered IZO as MoO _x hole collector contact	123
6.7	High-FF and -efficiency Molybdenum oxide-based devices	124

6.7.1	22.5% certified efficiency MoO _x solar cell [†]	124
6.7.2	<i>J-V</i> curve behavior in forward polarization	126
6.8	General conclusions metal oxide films as a-Si:H(<i>p</i>) replacement	126
7	Conclusions and perspectives	129
7.1	Conclusions	129
7.1.1	Device architecture performance summary	130
7.1.2	Light management	131
7.1.3	Electrical performance	131
7.1.4	Manufacturing and industrialization	132
7.2	Perspectives	133
7.2.1	Standard SHJ devices	133
7.2.2	Electrodeposited metal front grid	133
7.2.3	LEP-SHJ architecture	134
7.2.4	TMO-based SHJ solar cells	134
7.2.5	High-efficiency SHJ solar cell suggestion	135
A	LBIC circuit diagram and software	141
B	LEP-SHJ photolithography masks	143
	Bibliography	166
	Remerciements	167
	Curriculum Vitae	169

List of abbreviations and symbols

Semiconductor

n	Electron density
p	Hole density
Δ_n	Excess electron density
Δ_p	Excess hole density
S_{eff}	Effective surface recombination velocity
E_f	Fermi level
WF	Work function
FCA	Free carrier absorption
τ_{eff}	Effective minority carrier lifetime
E_g	Bandgap

Materials and depositions

TCO	Transparent conductive oxide
ZnO:B	Boron-doped zinc oxide
ITO	Indium tin oxide
IO:H	Hydrogenated indium oxide
IZO	Indium- zinc-oxide
PR	Photoresist
TMO	Transition metal oxide
MoO _x	Molybdenum oxide
WO _x	Tungsten oxide
NiO _x	Nickel oxide
VO _x	Vanadium oxide
a-Si:H	Hydrogenated amorphous silicon
a-Si:H(<i>i</i>)	Intrinsic hydrogenated amorphous silicon
a-Si:H(<i>n</i>)	n-doped hydrogenated amorphous silicon
a-Si:H(<i>p</i>)	p-doped hydrogenated amorphous silicon
μ c-Si:H	Hydrogenated microcrystalline silicon
c-Si	Crystalline silicon
PECVD	Plasma enhanced chemical vapor deposition

Contents

LPCVD	Low pressure chemical vapor deposition
LIP	Light induced plating

Characterizations and cells

η	Energy conversion efficiency
FF	Fill-factor
J_{sc}	Short-circuit-current density
V_{oc}	Open-circuit voltage
J-V	Current-voltage measurement
J	Current density
MPP	Maximum power point
R_s	Series resistance
ρ_c	Specific contact resistivity
EQE	External quantum efficiency
IQE	Internal quantum efficiency
PL	Photoluminence
LBIC	Light beam induced current
SE	Spectroscopic ellipsometry
ATR-FTIR	Attenuated total reflectance Fourier transform infrared spectroscopy
TDS	Thermal desorption spectroscopy
TLM	Transfer length method
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
HR-TEM	High resolution transmission electron microscopy
SHJ	Silicon heterojunction
FHC	Front hole collector
RHC	Rear hole collector
LEP-SHJ	Localized extraction and passivated SHJ cell
IBC	Interdigitated back-contact

1 Introduction

1.1 General context

1.1.1 Photovoltaics as a major contributor to electricity production

Energy is now one of the main challenges of our societies due to our constantly increasing demand. Between 1973 and 2012, the world total primary energy supply increased from 6.1 to 13.4 billion of tons of equivalent oil. Among this energy, 18.1% of the total final energy world consumption is consumed as electricity. [IEA 2014a] Importantly, a major part of this electricity is produced from non-renewable energy sources such as oil, natural gas, coal and nuclear. As a direct consequence of the use of fossil fuels, a massive quantity of CO₂ estimated at 31.7 billion tons are released each year into Earth's atmosphere with a catastrophic impact on the climate. [IEA 2014a] Although, the production of electricity from nuclear plants releases less CO₂ than other non-renewable energy sources, the danger posed by plant failures and the disposal of the waste raise the question of using this technology to produce electricity. Moreover, all these non-renewable energy sources rely on fuels available only in some specific parts of the world. It is therefore of primary importance to ensure the sustainability of our economies by modifying our energy sources, giving preference to renewables such as hydro-, wind- or solar-generation.

In Switzerland, the current market share between the different energy sources is shown in Fig. 1.1. It can be seen that nuclear electricity accounts for more than 36% of our electricity production. [OFEN 2014] After the nuclear disasters that happened in Three Mile Island, Chernobyl and more recently Fukushima, the Swiss government decided in 2011 to progressively abandon nuclear as an electricity production source. [Admin 2011] In this perspective, the new energy strategy of Switzerland towards 2050 is based on several aspects such as: i) lowering the overall energy consumption, ii) implementation of "smart-grid" electricity networks allowing a more clever usage of the electricity, iii) development of hydroelectricity and new renewable energy sources such as wind turbines and solar panels and iv) strengthening of the scientific research to achieve these goals. [Admin 2011].

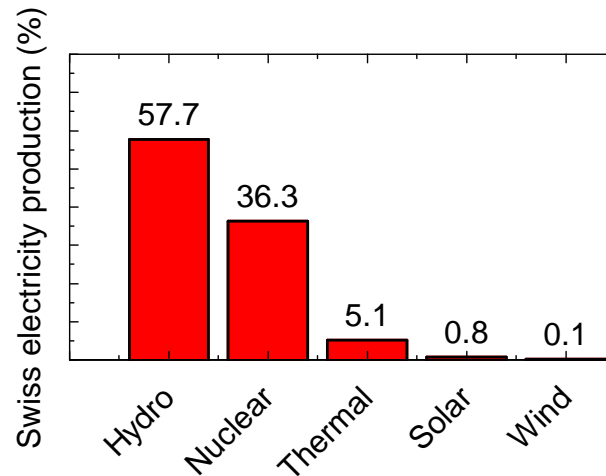


Figure 1.1: Production of the Swiss electricity in 2014. Data from [OFEN 2014]

Even though this challenge may seem difficult to overcome, an example of rapid growth of the solar market was given by Germany where during the 2007–2012 period, photovoltaics' share of the market grew from 0.5% to 6% demonstrating the feasibility of a rapid and radical change in our methods to produce electricity. [Bundesministerium 2014]

1.1.2 Brief historical overview

The first demonstration of the photovoltaic effect was made in 1839 by the French physicist Edmond Becquerel. In his experiment, electricity was generated when noble metal electrodes dipped into an acidic solution were exposed to sunlight. This experiment was the first demonstration of the direct conversion of light into electricity. [Green 1990a] Several decades after Becquerel's discovery, important findings were made by scientists working on the photoconductivity of selenium. In 1883, Charles Fritts realized a solar cell made of a selenium absorber sandwiched in between a gold and a brass electrode forming two Schottky contacts. [Green 1990a] [Nelson 2003]

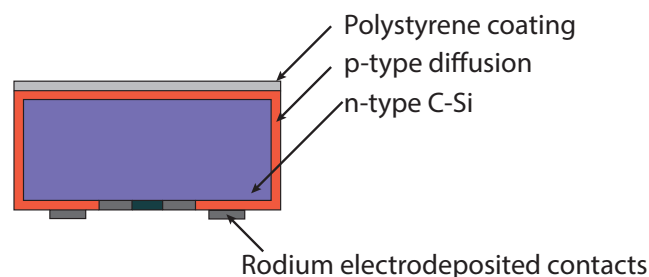


Figure 1.2: Schematic of the 1954 Bell Labs solar cell developed by Chapin, Pearson and Fuller. Schematic made from [Chapin 1957].

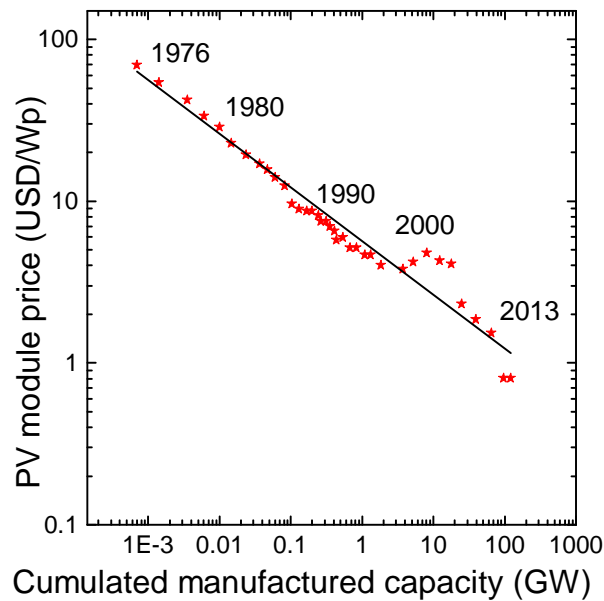


Figure 1.3: Learning curve of the PV module price as a function of the cumulative manufacturing capacity. Data from [IEA 2014b] [ITRPV 2015].

The "birth" of the silicon photovoltaic device as it is known nowadays happened in 1954 at Bell Laboratories. Chapin, Pearson and Fuller realized a revolutionary device based on a p-n junction made by boron diffusion in an n-type silicon wafer. [Chapin 1954] Figure 1.2 shows schematically the structure of this solar cell. Interestingly, this device already featured numerous concepts of advanced solar cells which were developed several decades later as for instance the use of an n-type silicon wafer, a fully back-contacted structure, an emitter wrap-around and electrodeposited contacts (see section 1.1.6). Even more remarkably, Chapin *et al.* reported in their 1954 paper that the solar cell energy-conversion efficiency is limited by recombination of charge carriers, light coupling into the absorber and ohmic losses. [Chapin 1954] More than 60 years later, these limitations are still the center of interest of photovoltaic research. Despite an impressive energy-conversion efficiency of 6% for this pioneer solar cell, its commercial interest was limited due to its high manufacturing cost. As a consequence, the main development of this technology during the next decades was restricted to space applications. [De Wolf 2012] In fact, due to the process complexity and especially the difficulty to purify silicon at a large scale, the price of a solar module was \$70 per Watt peak (Wp) in 1978, 24 years after the discovery of Chapin, Pearson and Fuller. However, the technology improvements made after the late 70s enabled the prices of solar energy to fall following a well-established learning curve as seen in Fig.1.3. [Swanson 2006] This learning curve implies that the photovoltaic production cost is reduced by 20% each time the production capacity is doubled. [ITRPV 2015] Nowadays, the cumulative shipped PV module power is estimated to be ≈ 184 GWp with an average PV module price of 0.62 \$/Wp in 2014. [ITRPV 2015] [IEA 2014b]

1.1.3 Semiconductor physics in solar cells

In this section, we review the main semiconductor physics relevant for the understanding of the solar cell operation.

Generation in semiconductors Figure 1.4 shows the generation of an electron-hole pair which takes place into a semiconductor material with a bandgap E_g . In this process, an electron leaves the valence band to reach the conduction band. To reach the conduction band, the electron must acquire at least the energy equivalent to E_g . This electron-hole pair generation can be induced either by thermal excitation or by absorption of a photon with an energy $h\nu \geq E_g$. The excess energy $h\nu - E_g$ is thermally lost in the semiconductor. We note here that this photogeneration process is extremely efficient in *direct* bandgap semiconductor material—direct transition from the valence to the conduction band such as in gallium arsenide or indium phosphide—compared to *indirect* bandgap semiconductor material—indirect transition requiring a phonon such as in silicon—which requires a thicker absorber. [Sze 2001] [Green 1982] At thermal equilibrium, the electron and hole density n_0 and p_0 can be expressed as:

$$n_0 = N_c e^{\frac{E_f - E_c}{kT}} \quad p_0 = N_v e^{\frac{E_v - E_f}{kT}} \quad (1.1)$$

where E_f , E_v and E_c are the Fermi energy, the valence band and the conduction band energy and N_v and N_c are the effective density of states in the valence band and the conduction band respectively. k is the Boltzmann constant and T is the temperature of the semiconductor.

As photogeneration leads to excess carrier concentration $\Delta_n = \Delta_p$, Eq. 1.1 can be rewritten as:

$$n = \Delta_n + n_0 = n = N_c e^{\frac{E_{fn} - E_c}{kT}} = n_0 e^{\frac{q\phi_n}{kT}} \quad p = \Delta_p + p_0 = p = N_v e^{\frac{E_v - E_{fp}}{kT}} = p_0 e^{\frac{q\phi_p}{kT}} \quad (1.2)$$

where E_{fn} and E_{fp} are the *quasi-Fermi levels* and $\phi_{n,p}$ represent their deviation from E_f . The splitting of these quasi-Fermi levels can be directly linked to an implied potential:

$$iV = \phi_p - \phi_n = \frac{kT}{q} \ln \left(\frac{(n_0 + \Delta n)(p_0 + \Delta n)}{n_i^2} \right) \quad (1.3)$$

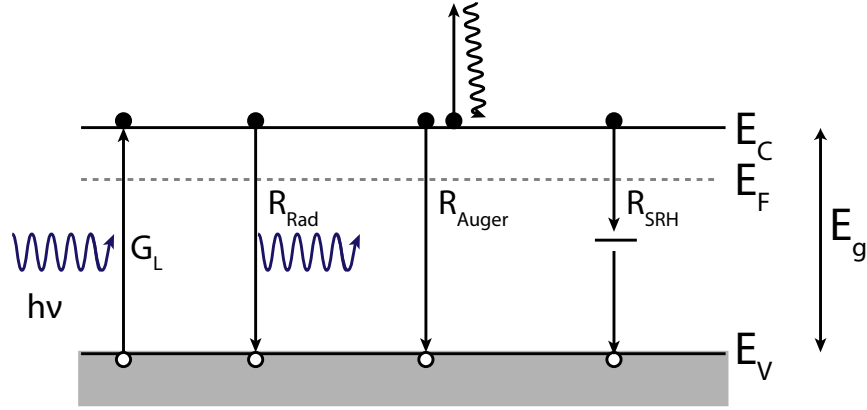


Figure 1.4: Generation and recombination processes occurring in a semiconductor.

Bulk recombination in semiconductors Recombination is the inverse process of generation where an electron falls from the conduction band to the valence band. In the bulk of a semiconductor, we can distinguish three recombination processes as shown in Fig. 1.4. [Sze 2001]

- **Radiative** recombination is the exact inverse of the photogeneration previously described. Here, the electron falls from the conduction band to the valence band and a photon with an energy E_g is generated. The probability that this process happens is higher in direct bandgap material than in indirect bandgap material as the minimum and the maximum of the conduction and valence band are aligned and no phonon is required. The radiative recombination rate is given by Eq.1.4, where B is a constant depending of the material: [Green 1982]

$$U_{Rad} = B(np - n_i^2) \quad (1.4)$$

- **Auger** recombination is a three-particle process where an electron recombines with a hole and transfers its energy to another electron which then thermalizes as shown in Fig. 1.4. Equivalently, this process can happen with a hole transferring its energy to a second hole. The Auger recombination rate is given by: [De Wolf 2005]

$$U_{Auger} = C_n(n^2 p - n_0^2 p_0) + C_p(np^2 - n_0 p_0^2) \quad (1.5)$$

- **Recombination through traps** is a two-step process in which an electron first reaches a defect state located in the bandgap and then reaches the valence band. The recombi-

Chapter 1. Introduction

nation rate is expressed by the Shockley-Read-Hall formalism: [Sze 2001]

$$U_{SRH} = \frac{v_{th} N_t (np - n_i^2)}{\frac{1}{\sigma_p} (n + n_i e^{\frac{E_t - E_f}{kT}}) + \frac{1}{\sigma_n} (p + p_i e^{\frac{E_f - E_t}{kT}})} \quad (1.6)$$

where $\sigma_{n,p}$ are the capture cross section of the trap, N_t is the trap density, E_t is the energy level of the trap and v_{th} is the thermal velocity.

From these recombination rates, we can associate a carrier lifetime $\tau_{n,p}$ reflecting the average time before a charge carrier recombines:

$$U \equiv \frac{\Delta n}{\tau_n} \Rightarrow \frac{1}{\tau_n} \equiv \Delta n U \quad (1.7)$$

Since recombination rates are additive, the three recombination mechanisms yield a *bulk* lifetime expressed as [Nelson 2003]

$$\frac{1}{\tau_{n \text{ bulk}}} = \frac{1}{\tau_{n \text{ Rad}}} + \frac{1}{\tau_{n \text{ Auger}}} + \frac{1}{\tau_{n \text{ SRH}}} \quad (1.8)$$

Surface recombination In addition to the recombination taking place into the bulk of the semiconductor, recombination can also happen at the surface of semiconductor due to the discontinuity of the lattice (i.e. dangling bonds) introducing surface energy states. The surface recombination rate is given by :

$$U_s \equiv S \Delta n|_{surf} \quad (1.9)$$

Where S is the surface recombination velocity. However, due to the bands bending in the surface vicinity, an effective surface recombination velocity S_{eff} can be defined from the recombination rate and the excess carrier density at a distance d from the surface where the bands are flat:

$$S_{eff} \equiv \frac{U_{x=d}}{\Delta n_{x=d}} \quad (1.10)$$

where S_{eff} typically ranges between 10^7 cm s^{-1} for a direct metal/silicon contact down to

$< 10 \text{ cm s}^{-1}$ for a passivated silicon surface. [Cuevas 1996] [Olibet 2007] [Hoex 2006] If S_{eff} is sufficiently small, the *effective* carrier lifetime τ_{eff} taking into account the bulk and the surface recombinations can be expressed as: [Schroder 2006]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{w} \quad (1.11)$$

where, w is the wafer thickness. We can note here that good surface passivation (i.e small a S_{eff} value) is of extreme importance in the case of thin wafers. Importantly, two ways can be used to maximize τ_{eff} by lowering the surface recombination. First, the surface recombination centre density can be lowered by *chemically* passivating the dangling bonds at the wafer surface. This can be achieved for instance by linking hydrogen atoms to the dangling bonds or by growing a thermal oxide that will terminate the dangling bonds. [Olibet 2007] [Kerr 2002a] The second approach is to reduce the minority-carrier concentration at the surface. This can be achieved either by doping the region close to the surface or by placing a material with trapped charges creating an electrical field (as for instance silicon nitride (SiN_x) for positive trapped charges or aluminium oxide (Al_2O_3) for negative trapped charges). [Green 1982]

Charge-carrier transport in semiconductors Two charge-carrier transport mechanisms are important in solar cells: [Wurfel 2015]

- **The drift transport** where an electrical field ϵ acts on the charge carriers. The current density is given by

$$J_{drift\ n} = q\mu_n n\epsilon \quad J_{drift\ p} = q\mu_p p\epsilon \quad (1.12)$$

- **The diffusion transport** where carriers flow from the region where their concentration is the highest towards a region with a weaker concentration. The diffusion current density is given by the Fick's law:

$$J_{diff\ n} = D_n \frac{dn}{dx} \quad J_{diff\ p} = D_p \frac{dp}{dx} \quad D_{n,p} = \frac{kT}{q} \mu_{n,p} \quad (1.13)$$

Importantly, due to the finite lifetime of minority carriers, the length that a minority carrier can diffuse before recombining is as well finite. Figure 1.5 shows an example of how the minority-carrier concentration decays exponentially in a p-type semiconductor when generation occurs exclusively at the surface. Eq. 1.14 expresses the minority-carrier concentration profile at

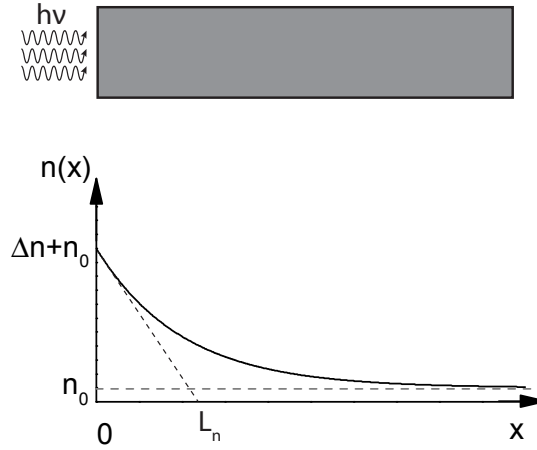


Figure 1.5: P-type semiconductor rod with generation occurring only at the surfaces and associated minority-carrier profile. Figure made from [Sze 2001]

steady state where the characteristic length L_n is called the *diffusion length* and corresponds to the average length that a minority carrier can travel. [Sze 2001]

$$n(x) = n_0 + \Delta n e^{\frac{-x}{L_n}} \quad L_n = \sqrt{D_n \tau_{eff\ n}} \quad (1.14)$$

When both drift and diffusion take place in the semiconductor, the total current is given by the sum of both contributions (expressed here for the electrons):

$$J_{tot\ n} = J_{drift\ n} + J_{diff\ n} = q\mu_n n e + D_n \frac{dn}{dx} \quad D_n = \frac{kT}{q} \mu_n \quad (1.15)$$

An equivalent way to express the forces acting on charge carriers leading to their transport is to refer to the gradient of their quasi-Fermi levels. Equation 1.15 can be rewritten as [Wurfel 2015]

$$J_{tot\ n} = \mu_n n \frac{d}{dx} E_{Fc} \quad J_{tot\ p} = \mu_p p \frac{d}{dx} E_{Fv} \quad (1.16)$$

1.1.4 Fundamental operation of a solar cell

A photovoltaic device can be divided into two distinct parts:

- **The absorber**, which converts the incident photons into electron-hole pairs. After their

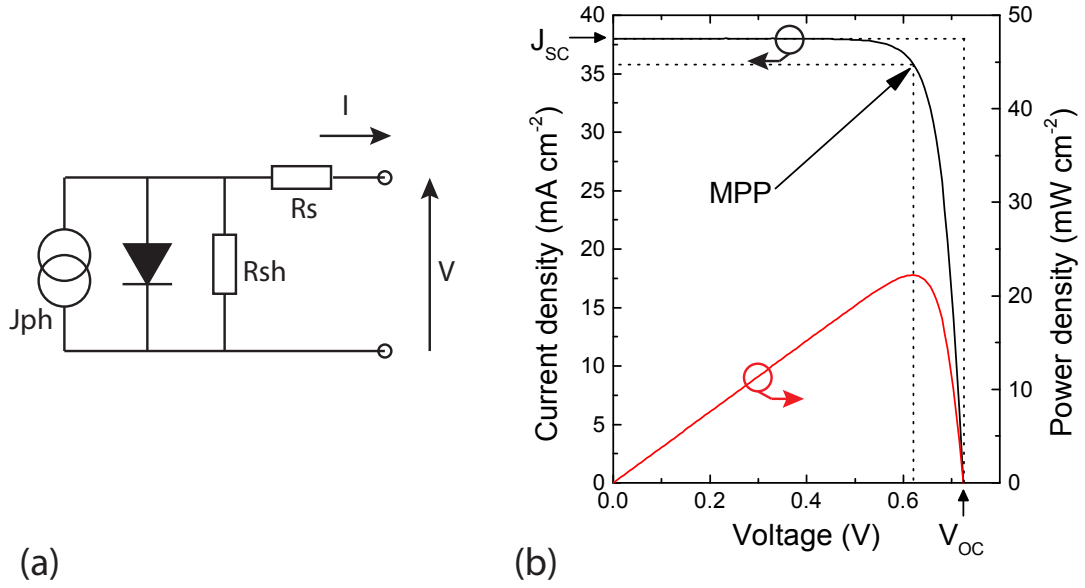


Figure 1.6: (a) Electrical equivalent circuit of the one-diode model of a solar cell (b) Light J - V curve and power-density curve.

generation, charge carriers are transported according to Eq. 1.16 towards their respective contacts. [Demaurex 2014b]

- **Two contacts, (one for electron, one for hole)**, which selectively extract one kind of charge carrier. [Cuevas 2013]

One of the most obvious structures to make the latter in silicon is to form a p-n junction. By doing this the p-side will have a significantly higher conductivity for holes than for electrons, which consequently creates a selective hole contact, and the inverse in the case for the electron collector. [Wurfel 2015].

Insight into how the current density J is extracted out of the solar cell depends on the voltage V at its terminals and can be gained by rewriting Eq. 1.3 as :

$$np = n_0 p_0 e^{\frac{qV}{kT}} \quad (1.17)$$

Chapter 1. Introduction

The current density J is the superposition of the photogenerated current J_{ph} and the recombination current J_{rec} . By assuming only radiative recombinations, it yields

$$J = J_{ph} - J_{rec} = J_{ph} - qwB(np - n_i^2) \quad (1.18)$$

By inserting Eq. 1.17 into Eq. 1.18, we obtain

$$J = J_{ph} - qwBn_i^2(e^{\frac{qV}{kT}} - 1) = J_{ph} - J_0(e^{\frac{qV}{kT}} - 1) \quad (1.19)$$

where J_0 is the saturation current density reflecting the recombinations. We note here that this method does not replace the traditional derivation of the continuity equation of the p-n junctions as it does not explain how the carrier extraction selectivity is obtained. However, this method shows that the typical exponential behavior is a direct consequence of the Fermi-Dirac statistic and does not depend on how carriers are extracted.

The equivalent electric circuit of a solar cell is shown in Fig. 1.6 (a). From this electric circuit, the current density J as a function of the voltage V taking into account the parasitic resistors R_s and R_{sh} is given by the diode equation:

$$J(V) = J_{ph} - J_0 \left(e^{\frac{q(V+J(V)R_s)}{nkT}} - 1 \right) + \frac{V + J(V)R_s}{R_{sh}} \quad (1.20)$$

where n is the ideality factor of the diode. Figure 1.6 (b) shows the plot of the J - V curve of an illuminated solar cell. It is then obvious to see that the extracted power $P(V) = J(V)V$ exhibits a maximum for an operating point of the device called the maximum power point (MPP).

Four parameters describing the performance of a solar cell can be extracted:

- **The open-circuit voltage (V_{oc})** is the potential of the device when no current is extracted from the solar cell. In this condition, the excess carrier concentration within the cell is dictated exclusively by the recombination processes. As a consequence, the V_{oc} gives a direct indication of the bulk lifetime and the surface recombination.
- **The short-circuit current density (J_{sc})** is the maximum current extracted from the solar cell when its terminals are in short-circuit condition (i.e. $V = 0$). This parameter is directly influenced by the optical losses and by the collection losses.

- **The fill factor (FF)** which defines the squareness of the J - V curves is defined as:

$$FF = \frac{V_{mpp}J_{mpp}}{V_{oc}J_{sc}} \quad (1.21)$$

This parameter is influenced by the recombination and by the series and shunt resistance (see section 1.1.5).

- **The energy conversion efficiency (η)** is defined as the ratio of the extracted power at the MPP (P_{out}) to the incident power of the light (P_{in} , $1000 \frac{W}{m^2}$ under A.M.1.5 G conditions). The efficiency can be expressed as

$$\eta = \frac{P_{out}}{P_{in}} = V_{oc}J_{sc}FF \quad (1.22)$$

In the following section, the impacts of the recombination processes and the optical and ohmic losses on these parameters are discussed.

1.1.5 Photovoltaic limitations

A fundamental limit for silicon solar cells The maximum energy conversion efficiency of a solar cell strongly depends on the model and the assumptions used in its determination and has therefore been debated since the beginning of research on solar cells. [Swanson 2005] The first main achievement in the determination of the maximum efficiency was made by Shockley and Queisser in 1961. Their approach was based on a thermodynamic balance between an incident photon flux produced by the radiation of a 6000K blackbody—where all photons with an energy $\geq E_g$ are assumed to create an electron-hole pair in the semiconductor—and the re-emitted radiative photon flux. [Shockley 1961] [Swanson 2005] In this model, a semi-infinite semiconductor piece and no Auger recombination were assumed. Remarkably, the optimum semiconductor bandgap found by Shockley and Queisser was 1.2 eV; we note that this value is quite close to the 1.12 eV bandgap of silicon. Converted to the A.M. 1.5G spectrum, this approach gives a maximum efficiency of 33%. [Swanson 2005] This approach was further investigated by Tiedje and Yablonovitch who additionally assumed a finite wafer thickness with a perfect Lambertian rear reflector and non-radiative Auger recombination. We note that Auger recombination is an unavoidable process in indirect semiconductors such as silicon. With this, the maximum efficiency was found to be 29.8% for silicon with an optimum wafer thickness of 100 μm . [Tiedje 1984] A new parametrization of the Auger recombination was proposed by Kerr and Cuevas in 2002. [Kerr 2002b] From this and by assuming a 90- μm -thick wafer absorber, a maximum efficiency of 29.05% was deduced. We note here that an improved parameterization for the Auger recombination was proposed by Richter in 2012 leading to a maximum efficiency of 29.43% for a 110- μm -thick wafer. [Richter 2012] [Richter 2013]

In the following paragraphs, we investigate qualitatively how the different losses impact the

J - V curve and the V_{oc} , J_{sc} , FF and η .

Recombination losses In this paragraph, we investigate the impact of the recombination processes on the solar cell performances. Figure 1.7 (a) shows the minority-carrier lifetime τ_{eff} as a function of the Δn with: i) only radiative recombination and Auger recombination, ii) with the addition of SRH recombination, and iii) with the subsequent addition of surface recombination. From these lifetime curves, an *implied* J - V curve can be deduced as follows: [Sinton 1996]

$$iV = \frac{kT}{q} \ln \left(\frac{\Delta n(N_A + \Delta n)}{n_i^2} + 1 \right) \quad (1.23)$$

$$iJ = J_{sc}(1 - equSuns) \quad (1.24)$$

$$equSuns = q \times G \times w \quad (1.25)$$

where G is the generation rate and w is the wafer thickness. When only radiative recombination and Auger recombination are considered, a maximum efficiency close to 29% and a maximum V_{oc} of 769 mV are extracted. [Kerr 2002b] Interestingly, by introducing a relatively modest contributions of SRH recombination and surface recombination, a weak influence on the τ_{eff} at the carrier injection level corresponding to the open-circuit condition is seen. This is explained by the dominance of the Auger recombination at this regime. Consequently, the V_{oc} is as well only weakly reduced. However, SRH recombination and surface recombination considerably reduce the minority-carrier lifetime at lower injection. As a consequence, the V_{mpp} is shifted toward lower voltages and leads to lower FF as observed in Fig. 1.7.

Optical losses Several effects lead to optical losses in solar cells. The list below gives the main contributors to optical losses in silicon solar cells

- **Light reflection at the primary interface:** As shown in Fig. 1.8 (a), a bare silicon wafer with a polished surface reflects about 30% of the incident light. A simple and cost-effective way to reduce this is to create random pyramids inducing a second rebound of the light. This reduces the light reflection to about 10%. Additionally this texture increases the optical path in the wafer. One or two materials with the appropriate refractive index can be inserted between the silicon and the air to act as $\frac{\lambda}{4}$ anti-reflective coating (ARC). The light reflection is then reduced to a few percent along the solar

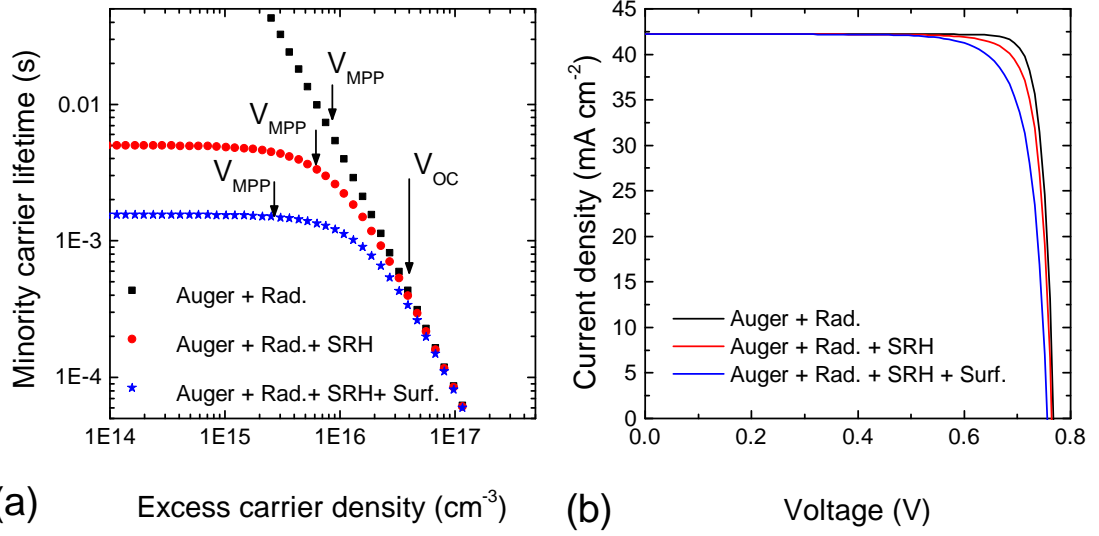


Figure 1.7: (a) Minority-carrier lifetime curves as a function of the excess carrier density for various combinations of recombination processes (b) Implied J - V curves related to the minority-carrier lifetime curves of (a).

spectrum. [Nelson 2003]

- **Parasitic light absorption in the front layers:** When transmitted through the front layers, which do not act as active absorbers (as for instance the ARC layers, see Fig. 1.8 (c)), part of the light is absorbed following the Beer-Lambert law which depends on the absorption coefficient $\alpha = \frac{4\pi k}{\lambda}$ and the film thickness t :

$$I_{transmitted} = I_0 \times e^{-\alpha t} \quad (1.26)$$

- **Near-IR free-carrier absorption:** This phenomenon is especially important with a transparent conductive oxide (TCO). As the FCA coefficient is proportional to the free-carrier concentration, heavily doped TCO leads to significant IR absorption (see Fig. 1.8 (c)). Therefore, high mobilities are required to obtain highly transparent TCOs with high conductivity. [Barraud 2013][Koida 2007]
- **Front-grid reflection:** The metallic front grid directly induces a shadowing of 2 to 6%. [Geissbuhler 2014]. Highly conductive material helps to reduce as much as possible the finger width while avoiding excessive ohmic losses (see chapter 3). The finger geometry is also important as it may partially reflect part of the incident light towards the cell. [Woehl 2008]
- **Back side IR losses:** Infrared light can reach the rear side of the solar cell and be lost by being reflected to the front side or parasitically absorbed by plasmonic effect induced by the metallic rear reflector. [Holman 2013]

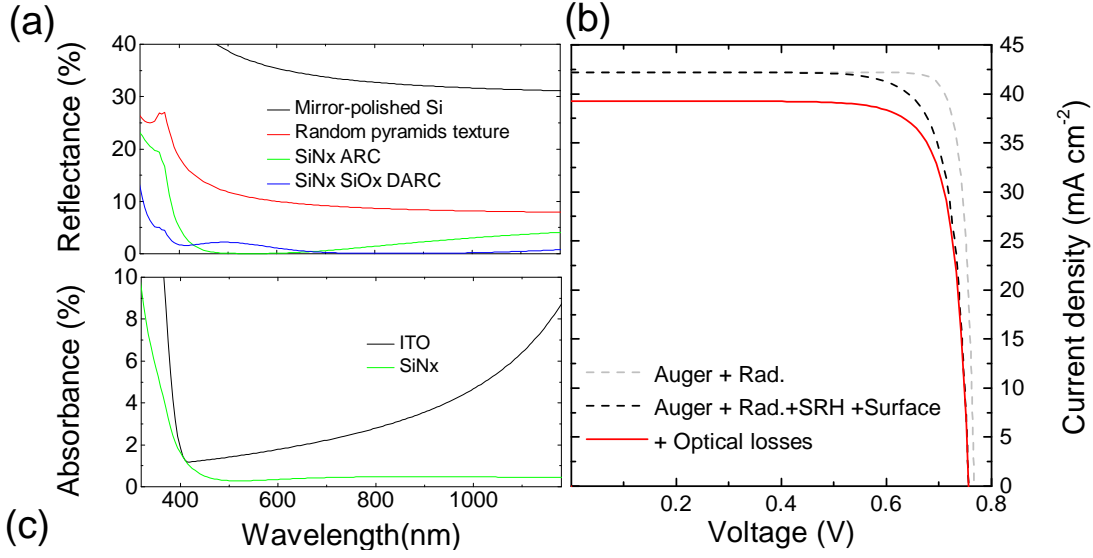


Figure 1.8: (a) Example of reflection losses occurring at the front side of a solar cell with different anti-reflection techniques (obtained by using OPAL [PVLighthouse 2015]) (b) Impact on the J - V curves of optical losses (c) Example of absorbance of different materials (obtained by using OPAL [PVLighthouse 2015]).

Figure 1.8 shows the impact of optical losses on the J - V curve. J - V curves with the recombination contributions previously explained are given for the purpose of comparison.

Ohmic losses The resistivity of the material conducting the charge carrier leads to a series resistance as shown in Fig. 1.6 (a). A significant part of this series resistance is induced by the front electrode. With a typical H-pattern front-grid design for fingers and busbar as shown in Fig. 1.9 (a), three main power losses can be extracted and normalized to the extracted power: [Green 1982]

- **Lateral transport towards the grid:**

$$P_{TCO} = \int_0^{\frac{s}{2}} I^2(x) dR = LJ^2 R_{\square} \int_0^{\frac{s}{2}} x^2 dx = \frac{1}{24} LJ^2 R_{\square} s^3 \quad (1.27)$$

$$P_{TCO \text{ norm.}} = \frac{P_{TCO}}{P_{unit}} = \frac{\frac{1}{24} LJ^2 R_{\square} s^3}{VJL\frac{s}{2}} = \frac{JR_{\square} s^2}{12V} \quad (1.28)$$

- **Transport in the finger:**

$$P_{finger} = \int_0^L I^2(y) dR = \frac{\rho}{tw_f} s^2 J^2 \int_0^L y^2 dy = \frac{1}{3} \frac{\rho}{t \times w_f} s^2 J^2 L^3 \quad (1.29)$$

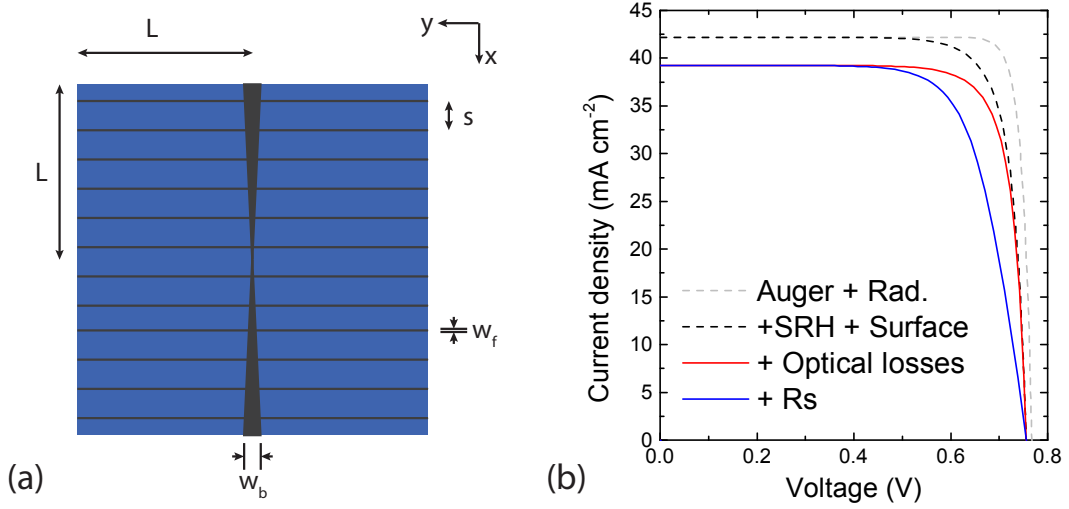


Figure 1.9: (a) Schematic of an H-pattern metallic front grid (b) Impact on the J - V curves of the series resistance.

$$P_{finger\ norm.} = \frac{P_{finger}}{P_{unit}} = \frac{\frac{1}{3} \frac{\rho}{tw_f} s^2 J^2 L^3}{VJLS} = \frac{1}{3} \frac{\rho s J L^2}{tw_f V} \quad (1.30)$$

• **Transport in the busbar:**

$$P_{BB} = \int_0^L I^2(x) dx = L^2 J^2 \rho \frac{2L}{w_b t} \int_0^L x dx = J_{ph}^2 \rho \frac{L^5}{w_b t} \quad (1.31)$$

$$P_{BB\ norm.} = \frac{P_{BB}}{P_{unit}} = \frac{J^2 \rho \frac{L^5}{w_b t}}{VJL^2} = \frac{J \rho L^3}{V w_b t} \quad (1.32)$$

where R_{\square} is the sheet resistance of the material conducting the carriers to the front grid, ρ is the electric resistivity of the metal used for the front grid and J and V are the current density and the voltage of the cell. The impact of the series resistance on the J - V curve is a characteristic variation of the curve's slope close to the open-circuit condition and is directly related to the FF : [Khanna 2015]

$$\Delta FF_{Rs} = \frac{J_{mpp}^2 R_s}{V_{oc} J_{sc}} \quad (1.33)$$

As seen in Fig. 1.6 (a), the equivalent circuit of a solar cell also includes a shunt resistor, which can possibly be induced by parasitic contact between the two terminals of the device. The

typical signature of such losses is the appearance of a tilted J - V curve near short circuit.

1.1.6 Overview of the technology

Figure 1.10 presents the record-efficiency chart over the last 40 years for the main photovoltaic technologies. Starting with the best energy conversion ever obtained for a photovoltaic device, an efficiency of 46% was obtained with a four-junction solar cell based on III-V materials under 508 suns concentration. [Green 2015][Dimroth 2014] Without concentration, similar cell structures demonstrated efficiencies of up to 38.8%. However, their complex processing, including molecular beam epitaxy, makes these technologies far too costly for terrestrial deployment.

For single-junction crystalline silicon solar cells, it is interesting to notice that recently silicon heterojunction (SHJ) solar cells have surpassed the conversion efficiency of diffused-junction devices. These devices will be further discussed in the following paragraphs.

Thin-film technologies offer the important benefits of monolithically interconnecting the different cells of a module during module manufacturing and facilitating the building integration due to their uniform aspect. [Boccard 2014][Heinstein 2013] Among these thin-film technologies, the most industrially spread are CIGS, CdTe, and thin-film silicon made of amorphous silicon or microcrystalline silicon possibly integrated in the micromorph tandem architecture.[Chiril 2011] [Romeo 2004] [Boccard 2014].

More recently, the scientific community has grown interested in perovskite solar cells with their record efficiency of 20.1%. [Yang 2015] Due to their high bandgap and high voltage potential, these solar cells are nowadays investigated as the top cell of tandem devices that have a silicon solar cell as the bottom cell. However, the high-sensitivity of this material against humidity and oxygen leads to important stability issues for such cells. [Loper 2014] [De Wolf 2014]

1.1.7 High-temperature crystalline silicon solar cell

This section discusses solar cell structures based on diffused-junctions in crystalline silicon wafers.

Aluminum-diffused back-surface-field c-Si solar cell The aluminum-diffused back-surface-field (Al-BSF) is the most industrially spread silicon solar cell architecture due to its extreme simplicity of fabrication. [Glunz 2012] To achieve the structure as presented in Fig. 1.11, silicon wafers are first textured to maximize light coupling. This can be realized either by anisotropic wet etching in the case of mono-crystalline wafers (see section 2.2.1) or by acidic etching in the case of multi-crystalline wafers. Usually, the wafer is lightly p-doped with a typical boron concentration of $N_A \approx 10^{16} \text{ cm}^{-3}$. [Fellmeth 2011] Next, a POCl_3 thermal diffusion is

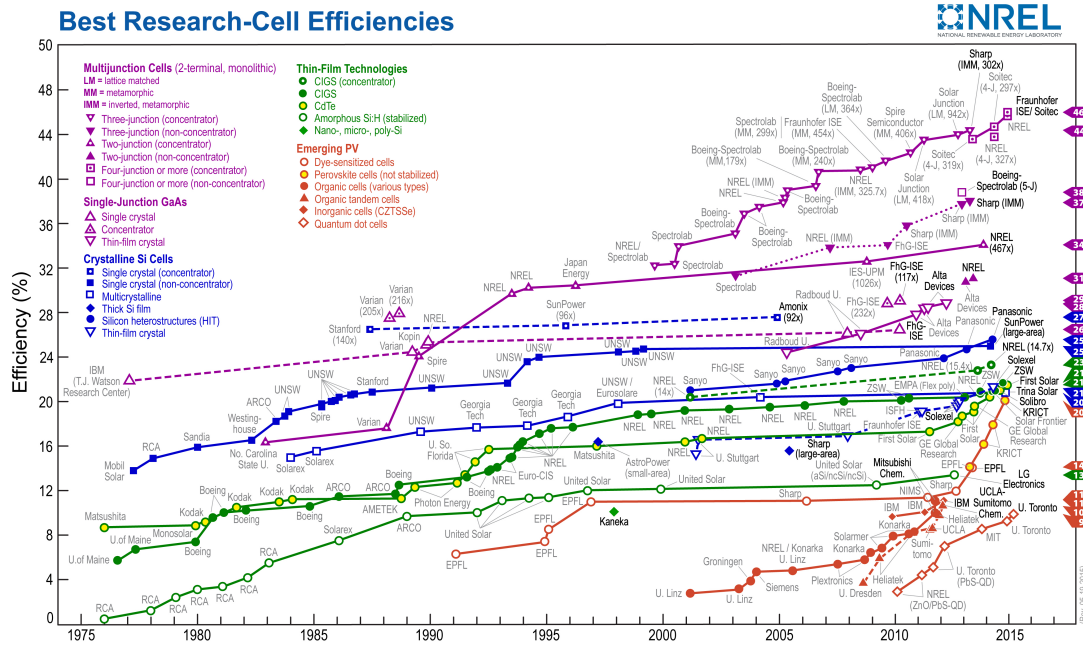


Figure 1.10: Record-efficiency chart over the last 40 years for various photovoltaic technologies. This plot is courtesy of the National Renewable Energy Laboratory, Golden, CO, USA [NREL 2015]

carried at the front side to form the electron collector having a sheet resistance usually ranging between 60 and 100 Ω/\square . [Schultz 2008] After the removal of the phosphorus glass grown during the diffusion and the etching of the diffused layer on the wafer edges, an SiN_x ARC is deposited by plasma-enhanced chemical vapor deposition (PECVD). An aluminium-based metallic paste is screen-printed at the rear side and dried prior to the screen-printing of the silver front-grid. Finally, both contacts are co-fired which respectively creates an aluminium doping at the back side and allows the silver paste to locally dissolve the SiN_x to contact the front n-type diffusion. [Ballif 2003] Despite the attractiveness of this simple process, this architecture suffers from significant recombination losses as both contacts rely on a direct metal-semiconductor contact. This recombination are nevertheless reduced by the front diffusion and the BSF which minimize the minority-carrier density in the contact vicinities. However, these doping concentrations follow a trade-off as a too important doping level will introduce excessive Auger recombination.

Passivated emitter and rear cell (PERC) solar cell To overcome the latter trade-off, the passivated emitter and rear cell structure was proposed in the late 1980s. [Blakers 1986] In this cell structure, the highly recombinative hole contact formed at the rear side by the Al-BSF is restricted to a few points by the addition of a passivating thermal oxide layer locally opened for the metal contact. The contact formation can be typically be carried out by a laser firing process. [Benick 2011] This cell structure is shown in Fig. 1.12 and is considered as the next

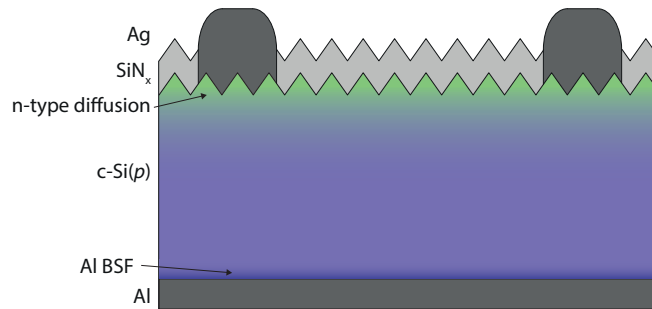


Figure 1.11: Schematic cross-section of an aluminum-diffused back-surface-field c-Si solar cell. Adapted from [De Wolf 2012].

generation for industrial solar cells with an Al_2O_3 layer as a passivating layer. [Burger 2015] An advantage of this structure is the possibility to "update" the existing production facilities by adding specific tools for the passivation layers its opening by laser.

Passivated emitter rear locally diffused (PERL) solar cell A further improvement of the PERC device structure is the passivated emitter rear-locally diffused devices proposed by UNSW in the late 1990s. The key difference is the introduction of a highly p-doped region above the point contacts at the rear side in order to reduce the recombination induced by the metal-semiconductor contact. Additionally, several advanced techniques were used to further increase the cell efficiency such as inverted pyramids, [Blakers 1986] double ARC, electrodeposited front-contact and a more lightly doped electron collector at the front side and locally reinforced under the contact. [Green 1990b] [Zhao 1998]

Interdigitated-back-contacted solar cell (IBC) In the previous cell structures, all layers of the front side are optimized in order to induce as few optical losses as possible (see section

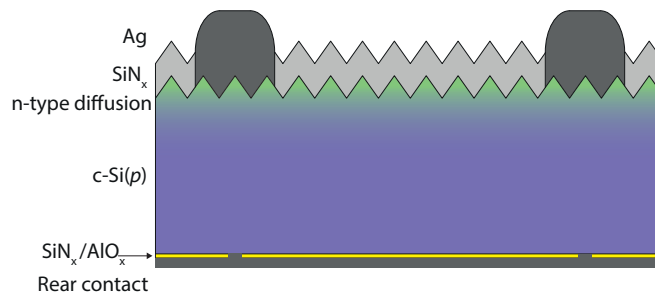


Figure 1.12: Schematic cross-section of a passivated emitter and rear cell structure. Adapted from [Seif 2015a].

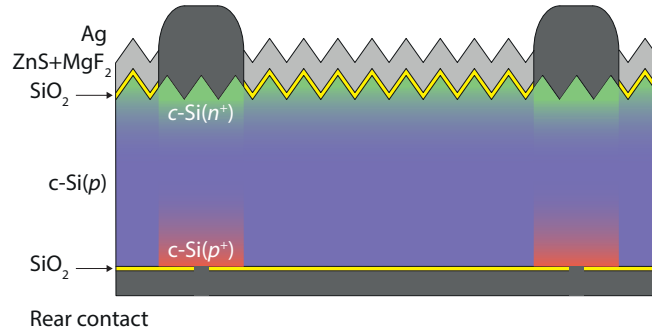


Figure 1.13: Schematic cross-section of a passivated emitter rear locally diffused (PERC) solar cell of UNSW [Zhao 1995]. Adapted from [Seif 2015a].

1.1.5). To overcome this issue, another cell structure was proposed by Lammert and Schwartz in 1975. [Lammert 1977] They proposed to place both electron and hole collectors at the rear side of the device forming two opposite combs. This design leads to the ultimate degree of freedom in the optimization of the front side for optical and passivation purposes exclusively. As minority carriers have to travel laterally to reach the contact, it is crucial to keep this distance smaller than their diffusion length in order to prevent their recombination leading to a J_{sc} loss. This potential loss is called *electrical shading*. [Reichel 2011] Furthermore, majority carriers generated above the opposite contact must as well travel laterally inducing an additional series resistance. [Tomasi 2014] [Granek 2010] [Franklin 2014]

This cell structure is currently industrially produced and commercialized by the company Sunpower. In these device, excessive recombination induced by a direct metal-semiconductor contact are avoided by the use of point-passivated contact enabling V_{oc} up to 725 mV. [Smith 2012] [Smith 2014] At the R&D scale, Sunpower demonstrated a remarkable efficiency of 25% by using this design. [Smith 2014]

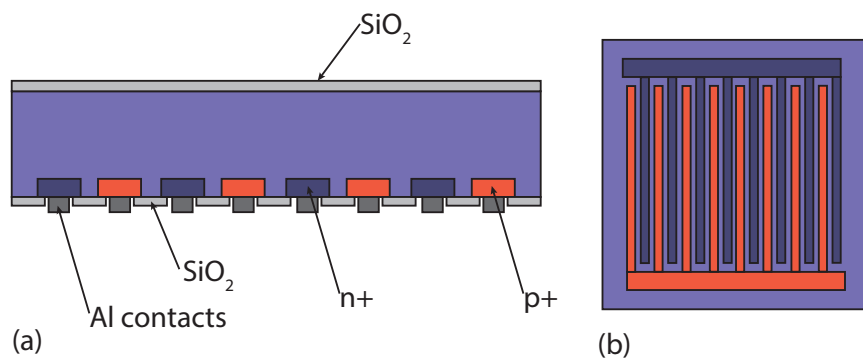


Figure 1.14: (a) Schematic cross-section of an interdigitated-back-contacted solar cell as proposed by [Lammert 1977] and (b) view of the rear-side.

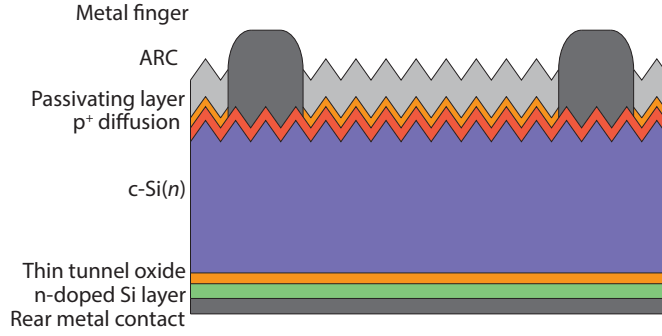


Figure 1.15: Schematic cross-section of a TOPCon cell as proposed by [Feldmann 2014b].

Tunnel oxide passivated contact (TOPCon) A recent demonstration of a passivating contact in high efficiency silicon solar cells was made by the tunnel oxide passivated contact (TOP-Con) demonstrated by Feldmann *et al.* [Feldmann 2014b] Figure, 1.15 shows a schematic cross-section of a TOPCon structure. The passivated contact is formed by ultra-thin silicon oxide usually 14-Å-thick grown by a wet chemical process allowing the transport of charge carrier by tunneling process. Then, to form an electron selective contact, a phosphorus-doped polysilicon layer is deposited and annealed above 600°C to activate the passivation. [Feldmann 2014b] This electron contact—in combination with a hole contact made by a front boron diffusion—demonstrated outstanding FF values above 82% leading to recent demonstration of cell efficiencies as high as 24.4% and 24.9%. [Feldmann 2014c] [Moldovan 2015] We note that both contacts can be realized with this approach by respectively using boron- and phosphorus-doped polysilicon layers. This latter structure showed promising device results with FF values above 81% demonstrating the effectiveness of such contact. [Feldmann 2014a]

1.1.8 Silicon heterojunction solar cells

As seen in the previous paragraphs describing diffused-junction c-Si solar cells, increasingly more complex cell structures have been proposed to optimize the electron and hole contacts with a global trend going to localized contacts. In silicon heterojunction (SHJ) solar cells, a completely different contacting approach is used relying on planar deposited passivating contacts made of amorphous silicon (a-Si:H). Figure 1.16 shows a schematic of the SHJ device structure. A mono-crystalline silicon wafer with random pyramids is used as the photon absorber. To ensure high-quality surface passivation, ≈ 5 -nm-thick intrinsic a-Si:H [denoted a-Si:H(*i*)] layers are deposited on both sides of the wafer. [Descoeudres 2011] To form the electron and hole collectors, n- and p-doped a-Si:H films are deposited on the a-Si:H(*i*) passivating layers. Due to their very low lateral conductivity, a transparent conductive oxide (TCO) is sputtered at the front side to efficiently contact the a-Si:H(*ip*) films, to conduct the charge carrier laterally and to provide an ARC at the front side. [De Wolf 2012] For the rear side, a TCO is used as well to contact the a-Si:H(*in*) and to provide a displaced back reflector in

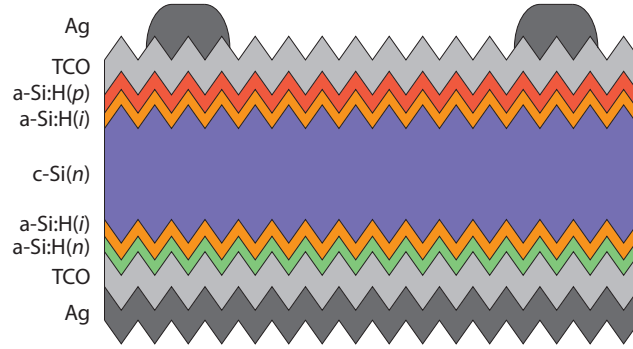


Figure 1.16: Schematic cross-section of a silicon heterojunction solar cell. Adapted from [De Wolf 2012].

combination with a sputtered silver film. [Holman 2013] The lateral conductivity of the front TCO is further reinforced by a screen-printed silver grid. Due to the low stability of a-Si:H layers above 200 °C, special silver pastes with a low curing temperature are used. [De Wolf 2012] A description of the complete process sequence to make a SHJ device is made in section 2.1.

The first demonstration of a SHJ solar cell with a structure as it is known nowadays was demonstrated in 1992 by Tanaka *et al.* from Sanyo (now Panasonic) with an efficiency of 18.1%. [Tanaka 1992] Recently, an increasing interest coming from both academia and industry was experienced for SHJs. This is explained by the outstanding results obtained for this technology notably by Panasonic with an efficiency for a front-contacted SHJ device of 24.7%. [Taguchi 2014] By using an IBC configuration, the efficiency was further increased to 25.6% becoming the new world record for c-Si solar cells. [Masuko 2014] In addition, the simple processing of SHJ devices associated with their high efficiency can make them cost-competitive compared to other solar cell technologies. [Ballif 2014] [Meyer-Burger 2014b]

1.2 Motivations

As previously discussed in section 1.1.5, several losses impact the efficiency of a solar cell. To overcome these losses, various device architectures based on c-Si wafers have been proposed. Table 1.1 gives an overview of the V_{oc} , J_{sc} , FF and efficiency for the different advanced c-Si solar cell architectures discussed in the previous sections. It can be seen that front-contacted SHJ devices have by far the lowest J_{sc} compared to diffused-junction devices. This is explained by the parasitic light absorption in the front a-Si:H and TCO layers and—in this case—by the screen-printed metallic front grid, which results in shadow losses. As a consequence, alternative structures and processes have to be developed in order to solve the latter issue.

Table 1.1: V_{oc} , J_{sc} , FF and efficiency of different c-Si solar cell architectures.

Cell	V_{oc} (mV)	J_{sc} (mA cm ⁻²)	FF (%)	Efficiency (%)
PERL [Zhao 1998]	706	42.7	82.8	25.0
PERC [Blakers 1989]	688	40.8	82.1	23.1
IBC diffused-junction [Smith 2014]	726	41.53	82.84	25.0
TOPCon [Feldmann 2014c]	715	41.5	82.1	24.4
SHJ front contacted [Taguchi 2014]	750	39.5	83.2	24.7
SHJ IBC [Masuko 2014]	740	41.8	82.7	25.6

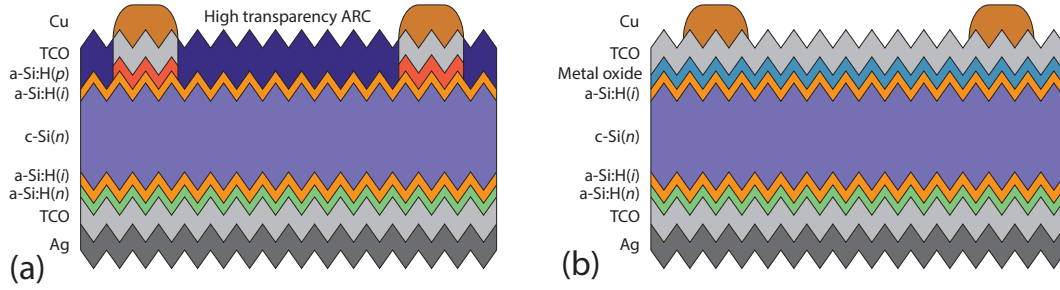


Figure 1.17: Schematic cross-section of novel devices investigated in this thesis: (a) SHJ device with localized contacts (b) SHJ device with metal oxide as a replacement of the a-Si:H(*p*) hole collector. Both devices feature an advanced metallization made by electrodeposited copper.

1.3 Objectives and structure

1.3.1 Objectives

The objectives of this thesis are to further enhance the optical response of SHJ solar cells by developing new architectures and processing techniques.

The scientific goal of this work is the investigation of the two new device architectures shown in Fig. 1.17. The first structure relies on localized front contacts in order to limit the coverage of a-Si:H layers and the parasitic light absorption. The second structure is based on the replacement of the a-Si:H(*p*) hole collector layer by a highly transparent metal oxide as proposed by Battaglia *et al.* [Battaglia 2014a] To realize these structures, a technological goal is the development of several micro-fabrication techniques dedicated to SHJ solar cells. First, an accurate technique capable of patterning a-Si:H layers with a high accuracy and preserving the surface passivation is needed. Secondly, a replacement technique of the silver paste screen-printing is required in order to form a highly conductive front grid with narrower fingers width. Ultimately, these structures or processing techniques can be possibly merged together or applied to other device architectures such as IBC-SHJ.

1.3.2 Structure

This thesis is structured as follows:

- **Chapter 2** presents the experimental setups and characterization tools used during this work.
- **Chapter 3** investigates the processing of an electrodeposited metal front grid. Several processes specifically designed for SHJ solar cells are presented.
- **Chapter 4** investigates wet chemical etching and hydrogen plasma etching in a PECVD reactor with the goal of accurately patterning a-Si:H layers without damaging the surface passivation.
- **Chapter 5** is dedicated to the study of localized contacts at the front side of SHJ devices. Several architectures are investigated and compared. In addition, specific characterization of these devices by light-induced beam current is discussed.
- **Chapter 6** presents a study of the replacement of the a-Si:H(*p*) layer by highly transparent metal oxides such as molybdenum oxide.
- **Chapter 7** presents general conclusions of the outcomes of this work and proposes outlooks for further developments.

1.4 Contribution to the field

This work contributes to the field of research in silicon photovoltaic devices and thin-film electronics and especially for SHJ solar cells as follows:

Studying the metallization of SHJ devices, we demonstrate how the standard front grid usually formed by screen-printing of a low-temperature silver paste may be replaced by a more efficient one, made by electrodeposited metals. Even though this approach was widely studied for homojunction devices, only a few reports of this technology were available for SHJ solar cells. In particular the causes of weak adhesion of the metal finger were investigated in this work and new processes enabling better adhesion were developed. Additionally, we demonstrated how this metallization technique may be adapted to chemically sensitive TCOs enabling for instance the use of non-indium based TCOs. [Geissbühler 2014]

We investigated the etching of extremely thin a-Si:H layers and demonstrated that hydrogen plasma etching is capable of achieving etching with nano-metric resolution. More importantly, we demonstrated that such etching can preserve the surface passivation with proper engineering of the process. These findings are of great importance for advanced devices such as IBC-SHJ cells, for which patterning of the a-Si:H layers is required. [Geissbühler 2013]

We studied SHJ architecture having localized contacts at the front side in order to decrease parasitic light absorption. By studying these structures and their losses, a better understanding of SHJ operation was obtained and cell efficiency up to 20% were demonstrated.¹

Finally, we demonstrated that molybdenum oxide can form an efficient hole collector. More specifically, we showed the hole-blocking behavior experienced with these devices can be avoided by proper engineering. By implementing the advanced electrodeposited front metalization previously developed on molybdenum oxide devices, high certified efficiencies of up to 22.5% were demonstrated.

These findings open new perspectives for SHJ solar cells both by potentially decreasing their manufacturing cost and by enabling improvements in their energy-conversion efficiency. Finally, this work contributes to other related projects or collaborations established during this thesis as the development of new SHJ devices [Demaurex 2014b] [Demaurex 2014a] [Tomasi 2014] [Papet 2013] [Descoeudres 2012] [Terheiden 2015] or the development of advanced a-Si:H-based particle detector [Franco 2014].

¹This work will be part of an upcoming publication by Geissbühler *et al.*

2 Experimental processes and characterization

This chapter presents the main processes and equipment used during this thesis for the fabrication and characterization of silicon heterojunction (SHJ) devices. This chapter is structured as follows: First an overview of the standard SHJ device (denoted as baseline in this work) process flow is presented. Next, a more detailed presentation of the different processing equipment and of the layer characterization techniques is given. Finally, the solar cell characterization tools are presented.

2.1 SHJ baseline process flow overview

Figure 2.1 shows the process flow used to manufacture baseline SHJ devices at PV-Lab. High-quality $\approx 4\Omega \cdot \text{cm}$ float zone monocrystalline silicon wafers (c-Si) with diameter of 100 mm and a thickness of $\approx 230\mu\text{m}$ are usually used. First, wafers are textured and cleaned by using wet chemistry. After a dip in 5% hydrofluoric acid to remove the native silicon oxide, intrinsic hydrogenated amorphous silicon [a-Si:H(*i*)] is deposited on both sides of the wafer by plasma-enhanced chemical vapor deposition (PECVD). These depositions are immediately followed by subsequent depositions of n- and p-doped a-Si:H [denoted a-Si:H(*n*) and a-Si:H(*p*)] to respectively form the electron and hole collectors of the cell. Wafers with a-Si:H(*n*) and a-Si:H(*p*) stacks are denoted as *precursors* here. Indium tin oxide (ITO) is used as the front transparent conductive oxide (TCO) and is deposited through a shadow mask by DC magnetron sputtering. Next, an ITO/Ag stack is deposited at the back side in the same deposition system. Finally, the metallic front grid is made by screen-printing a low-temperature silver paste followed by a 200 °C annealing for 25 min.

Figure 2.1 shows the front layout of baseline devices. The wafer includes three cells with a $2 \times 2 \text{ cm}^2$ area. For characterization purposes—such as transmission line method (TLM), line resistance or external quantum efficiency—specific test patterns are created on the wafer.

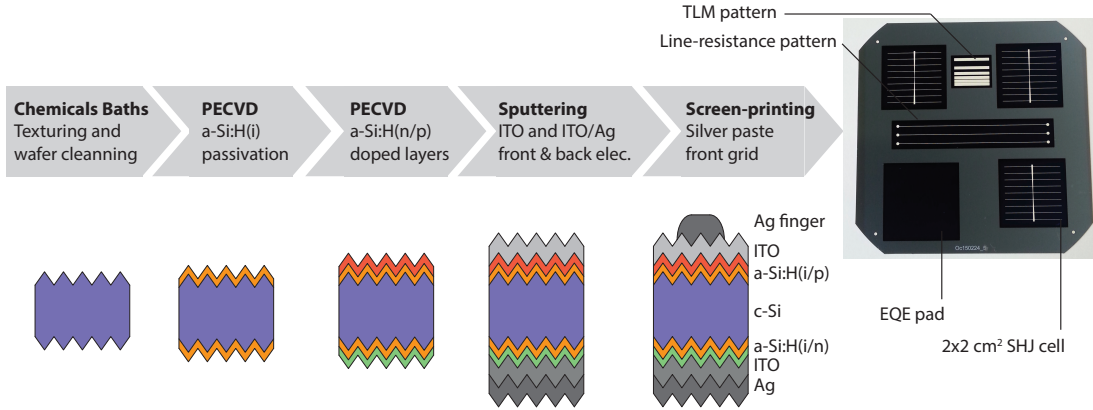


Figure 2.1: Process flow overview of baseline SHJ devices and front layout of a baseline wafer.

2.2 Silicon heterojunction solar cell fabrication equipments

2.2.1 Wafer texturing and cleaning

Anisotropic wet etching is the most common way of texturing monocrystalline silicon wafers, creating random pyramids, in order to reduce the light reflection on its surface. This technique relies on alkaline solutions such as potassium hydroxide (KOH) etching crystalline planes at different rates. [Madou 2002] The standard texturing sequence is usually as follows: First, damages to the crystalline structure induced by wire sawing are removed in a concentrated KOH bath. Next, random pyramids are created in a second KOH bath in which the temperature and the KOH and surfactant concentrations are optimized to promote the pyramid formation. Finally, metallic and organic contaminants are removed using acid baths. [Papet 2006] In this way, a practically perfect optical structure is achieved without the need for expensive patterning techniques. [De Wolf 2012]

2.2.2 Plasma-enhanced chemical vapor deposition

PECVD is the technique used in this work to deposit intrinsic and doped-hydrogenated a-Si:H films as well as silicon-based alloys such hydrogenated amorphous silicon nitride ($\text{a-SiN}_x\text{:H}$) and hydrogenated amorphous silicon oxide ($\text{a-SiO}_x\text{:H}$).

This technique is based on the dissociation of gas precursor molecules in a plasma. Figure 2.2 (a) shows a schematic cross view of a PECVD reactor: The plasma is created between two parallel electrodes separated by a gap ranging typically from 13 to 15 mm. The first of these electrodes is a gas shower that homogenously distributes the gas precursors. The second electrode contains the substrates on which the layer has to be deposited. This assembly of two parallel plates may be sealed in a hermetic box in which the plasma will be confined.

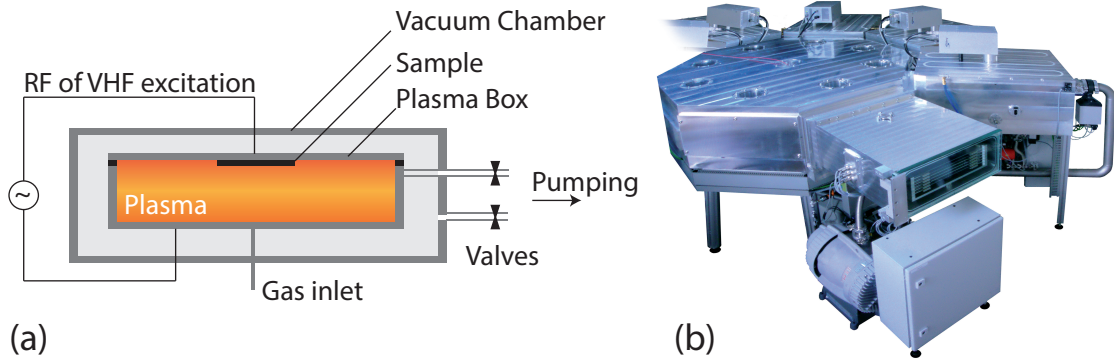


Figure 2.2: (a) Schematic view of PECVD reactor with a *plasma-box* design (b) Photograph of an R&D PECVD reactor Octopus II of Indeotec. Copyright [Indeotec SA](#).

This so-called *plasma-box* or *S-Cube* structure is placed in a main chamber in order to reach a high primary vacuum. This *box-in-a-box* concept keeps a differential pressure with the main vacuum chamber and therefore prevents contaminants coming from the cold walls of the main chamber from reaching the plasma. Furthermore, this concept enables to reverse the differential pressure during the reactor cleaning to avoid the interaction of fluorine with the metal walls. [Perrin 2000] [Stueckelberger 2014] During the process, the mixing of gases is realized with mass-flow-controller valves which accurately regulate the amount of each precursor gas. The standard precursor gases used to deposit a-Si:H layers are silane (SiH_4) and hydrogen (H_2) which can be mixed with trimethylborane ($\text{B}(\text{CH}_3)_3$) or with phosphine (PH_3) to respectively p- or n-dope the a-Si:H films. The process pressure is automatically regulated by a butterfly valve placed between the chamber and the process pumping unit. The plasma is ignited and maintained by applying a radio frequency (RF, 13.56 MHz up to 40.68 MHz) or very high frequency (VHF, above 40.68 MHz) excitation between the two electrodes. The four PECVD systems used during this thesis are listed and described below:

- Indeotec, Octopus I** This versatile R&D tool is based on the cluster configuration and has four independent deposition chambers that can be set up at different frequencies and dedicated for specific materials in order to avoid cross-contamination. During this work, one chamber was dedicated to a-Si:H(*i*) exclusively and the deposition of n- and p-doped a-Si:H films took place in a second chamber. Each time before entering in the intrinsic chamber, a coating of the substrate holder was made to avoid cross-contamination. The two other deposition chambers were used for developments on other Si-based materials such as amorphous silicon oxide or micro-crystalline silicon (a-SiO:H_x or $\mu\text{c-Si:H}$). The deposition area is $163 \times 153 \text{ mm}^2$ which allows for the deposition of a single 4-inches Si wafer and an AF32 glass witness per run.

- **Indeotec, Octopus II** This PECVD tool is the next generation of the Octopus I and offers the possibility to deposit up to twelve 4-inches Si wafers per run while maintaining the advantages of a cluster tool.
- **TEL Solar, KAI-M** This PECVD system is used as a mono-chamber reactor where both intrinsic and doped a-Si:H layer depositions take place. Its large deposition area of $61 \times 50 \text{ cm}^2$ allows for co-deposition of twelve 4-inches Si wafers per run. This tool was used to provide co-deposited baseline precursors.
- **XL PECVD, reactor built in-house** This un-automated PECVD mono-chamber reactor has additional NH_3 and N_2O gas lines in order to deposit high optical quality silicon nitride (a-SiN_x:H) and a-SiO_x:H layers. The deposition area is $40 \times 44 \text{ cm}^2$ and the excitation frequency is fixed to 81.36 MHz.

2.2.3 Transparent conductive oxides and metal sputtering deposition

As presented section 2.1, the contact of a-Si:H layers is made by using TCO films deposited by magnetron sputtering technique. The sputtering is based on the bombardment by Ar ions of a target in the material to be deposited. The Ar ions created in the plasma are accelerated towards the target by an electric field and are magnetically concentrated on the target. The plasma may be maintained by either RF or DC excitation. An O₂ flux is added to the Ar in order to tune the doping concentration in the indium-based TCOs. The different sputtering tools used during this work are described below:

- **Material research company (MRC) 603** This sputtering tool has three different targets (ITO, IO, Ag) vertically mounted. Up to six 4-inches wafers can be mounted on the substrate holder and co-deposited in a single run. The deposited thickness is adjusted by varying the substrate holder transit speed in front of the target. For IO:H layers, H₂O vapor can be inserted to the gas flux in order to incorporate hydrogen into the In₂O₃. [Koida 2007] [Barraud 2013].
- **Oerlikon Clusterline** This tool is based on the cluster architecture and is equipped of four chambers including either a single target or four targets of 4-inches in diameter. This system can deposit on substrates up to 8-inches and is in particular used for ITO, IZO, ZnO:Al, Ag depositions. [Morales-Masis 2015]

2.2.4 Zinc oxide low-pressure chemical vapor deposition

As mentioned in section 1.1.8 boron-doped zinc oxide can be used as a substitute for indium-based TCOs and can be deposited by low-pressure chemical vapor deposition (LPCVD). Diethylzinc (DEZ, $\text{Zn}(\text{C}_2\text{H}_5)_2$) and H₂O vapor are used as precursor gases for ZnO, and diborane (B_2H_6) is inserted as the dopant source. The substrates are heated to $\approx 170^\circ\text{C}$ to enable the precursor gases to dissociate, which initiates the deposition. [Choong 2010] [Ding 2013b]

2.2.5 Metals and dielectrics thermal evaporation

Thermal evaporation is a versatile deposition technique in which a specific material can be deposited without any hardware modification such as a target exchange as in the sputtering case or adding gas lines as for PECVD or LPCVD techniques. In this technique, the material is heated in high vacuum (below 10^{-5} mBar) up to its evaporation. We use in this work the Joule effect technique where the material to be deposited is heated by an intense electric current in a resistive boat made of tungsten or molybdenum. If the material to be deposited has a high boiling point—e.g. Al_2O_3 —, an electron beam focused on the crucible can be used as the heat source. However, an important disadvantage of this technique is the intense X-ray production due to the electron Bremsstrahlung which may affect the a-Si:H(*i*) passivation layer of a SHJ cell. The substrates are mounted onto a rotary substrate holder to ensure a good deposition homogeneity. The control of the deposited thickness is made by an in-situ piezoelectric micro-balance. This deposition technique is used in this thesis for a wide range of metals (e.g. Ag, Al, Ni, Cu, Au, etc.) and for dielectrics (MgF_2 , MoO_x , ZnS, SiO_2 , etc.).

2.2.6 Silver paste screen-printing metallization

Screen-printing is the most used metallization technique to produce the narrow lines of the solar cell front grid. For SHJ cells, a low-temperature silver paste is applied through a screen which consists of a metallic mesh covered by a resist and locally opened. This operation is performed in an automated screen-printer (Essemtec S.A.) which accurately controls the wafer alignment and the pressure applied to the squeegee. Next, the silver paste is cured close to 200 °C on a belt furnace. [Zicarelli Fernandez 2010][De Wolf 2012] The front-grid design used in this thesis consists of nine fingers spaced 2.1 mm apart connected to each other by a central busbar (see Fig. 2.1). This metallization layout has a coverage of $\approx 6\%$. [Holman 2012]

2.2.7 Photolithography

Photolithography is one of the most common patterning techniques in the semiconductor industry. [Madou 2002] [Sze 2001] Its usage is however restricted to research in the photovoltaic field due to its relatively high cost compared to screen-printing. In this technique, a photoresist is deposited either by spin coating, dip coating or spray coating to form a film with a thickness ranging from less than $1\mu\text{m}$ to several tens of μm . A more detailed investigation of the photoresist deposition technique for the specific case of substrates with random pyramids is presented in section 3.2. Next, the photoresist is exposed to UV light through a soda-lime mask featuring the layout on a patterned chromium layer. A mask aligner (MA/BA 6, Suss MicroTec) is used for the UV exposure and allows the accurate alinement of the design on existing geometries or on the wafer edges. After the UV exposure, the photoresist is developed in an alkaline solution. Two different kinds of photoresist can be used: (i) a *positive-tone* for which the exposed part dissolves in the developer and (ii) a *negative-tone* resist for which the exposed part is cross-linked during the UV exposure and remains after the developing.

2.3 Layer characterization

2.3.1 Line-, sheet- and contact-resistance measurements

- **Line resistance** The bulk resistivity of the screen-printed silver used for the front grid is evaluated by measuring the resistance of a test pattern as drawn in Fig. 2.3. As the resistances to be measured are in the 1Ω range, a four-probes sensing is used to suppress the resistance contribution of the probes. The resistivity is then deduced by using $\rho_{Ag} = \frac{w \times t}{L}$ where w , t and L are the line width, thickness and length respectively.
- **Sheet resistance** For thin films, the sheet resistance (R_{\square}) defined as $R_{\square} = \frac{\rho_c}{t}$ with t the film thickness, is often used to characterize a conductive film. The R_{\square} of a thin film is usually measured by using four probes equally distant one from each other in which the two outside probes inject a current and the two inside probes measure the voltage drop in the film. The resistance obtained by this technique is then multiplied by a geometric factor to take into account the finite geometry of the sample.
- **Contact resistance** The transfer length method (TLM) is a common way to evaluate the contact resistance between two different materials. The structure is made as follows: one material is deposited on the entire sample surface (denoted as planar film) and the second material is patterned into several pads forming a ladder pattern as shown in Fig. 2.3 (b). By measuring the resistance between the pads and applying a linear fit, the interception with the ordinate gives two times the contact resistance of one pad with the planar film. As the current does not flow homogenously from the planar film toward the contact pad and leads to a voltage distribution, the contact resistance R_C does not depend linearly on the contact-pad width w as described by Eq. 2.1. [Berger 1972] [Vinod 2011]

$$R_C = \frac{\sqrt{R_{\square}\rho_c}}{W} \coth\left(w\sqrt{\frac{R_{\square}}{\rho_c}}\right) \quad (2.1)$$

where R_{\square} is the sheet resistance of the planar film, w and W are respectively the width and the length of the contact pads and ρ_c is the specific contact resistivity. As R_C depends on the contact geometry, it is preferable to characterize a contact by ρ_c . This parameter can be expressed as: $\rho_c = R_C L_t^2$ where L_t is the transfer length. This length can be understood as the minimum length needed for the current to be efficiently inject from the planar film to the pad. If we rewrite Eq. 2.1 as $R_C \propto \coth\left(\frac{w}{L_t}\right)$ we see that R_C dramatically increases when $w \ll L_t$. It is therefore crucial during the design of a contact keep $w \gg L_t$.

2.3.2 Spectroscopic ellipsometry

Spectroscopic ellipsometry (UVISEL from Horiba Jobin Yvon) is used in this thesis for the characterization of a-Si:H films. For this technique, the film of interest can be deposited

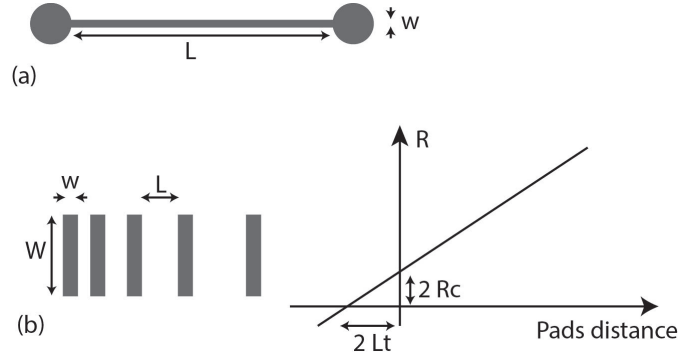


Figure 2.3: (a) Line-resistance test pattern (b) TLM ladder test pattern.

on a co-deposited glass witness or on polished c-Si wafers. The models used for the fitting include a bulk layer of the deposited a-Si:H film and a mixed layer containing voids to take into account the surface roughness of the film. The material is modeled by a Tauc-Lorentz oscillator in which the optical bandgap (E_g) and the film thickness are extracted. [Jellison 1996] [Stueckelberger 2014]

2.3.3 Spectrophotometer

A Lambda 950 Perkin Elmer spectrophotometer equipped with a 150-mm InGaAs integrating sphere is used to assess the total reflectance (TR) and the total transmittance (TT) of films deposited on AF32 glass witnesses. The wavelength range is typically from 320 nm to 1200 nm and can be extended down to 250 nm if a D_2 lamp is used. The absorptance (A) is obtained by : $A(\lambda) = 100\% - TT(\lambda) - TR(\lambda)$. [Ding 2013b]

2.4 Solar cell characterization

2.4.1 Minority-carrier lifetime measurement

A common technique to measure the minority-carrier lifetime τ_{eff} is the photogeneration of charge carriers by a flash lamp combined with measurement of the wafer photoconductance. [Sinton 1996] The evolution over time of the excess minority-carrier density Δn follows the continuity equation:

$$\frac{\partial \Delta n}{\partial t} = G - U + \frac{1}{q} \nabla J \quad (2.2)$$

By using the $U = \frac{\Delta n}{\tau_{\text{eff}}}$ relationship, Eq. 2.2 can be rewritten as the *generalized* expression of τ_{eff} . From this, two separate cases can be identified : (i) *the transient* where τ_{eff} is larger than the flash lamp duration and (ii) *the quasi-steady states (QSS)* where τ_{eff} is smaller than the

flash lamp duration : [Nagel 1999][Kerr 2002a]

$$\text{Generalized: } \tau_{eff}(\Delta n) = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n(t)}{dt}} \quad (2.3)$$

$$\text{Transient: } \tau_{eff}(\Delta n) = \frac{\Delta n(t)}{\frac{d\Delta n(t)}{dt}} \quad (2.4)$$

$$\text{QSS: } \tau_{eff}(\Delta n) = \frac{\Delta n(t)}{G(t)} \quad (2.5)$$

As presented in section 1.1.3, the implied open-circuit voltage iV_{oc} can be deduced from τ_{eff} and the wafer thickness and doping concentration : [Sinton 1996]

$$iV_{oc} = \frac{kT}{q} \ln \left(\frac{\Delta n(N_A + \Delta n)}{n_i^2} + 1 \right) \quad (2.6)$$

In this work, a WCT-120 lifetime measurement tool from Sinton Instruments was used to determine τ_{eff} and iV_{oc} . As most of the measurements were for wafers with $\tau_{eff} > 1\text{ms}$, the transient mode was the most often used.

2.4.2 Illuminated J - V

An illuminated J - V measurement is the most important characterization of a solar cell as it directly measures its behavior under illumination and enable to assess its the energy-conversion efficiency, short-circuit current (J_{sc}), open-circuit voltage (V_{oc}) and fill factor (FF). These parameters are extracted by placing the cell under illumination and by sweeping the voltage at the cell terminals while recording the electrical current. As a direct consequence of their good surface passivation, SHJ solar cells have a comparatively large capacitance which may lead to measurement artifacts if the voltage is swept too fast. [Virtuani 2012] To avoid this, steady-state light exposures of ~ 1 second are preferred to flash exposures < 100 ms. The illumination source is a continuous light solar simulator (Wacom, WXS-90S-5,AM1.5G) composed of a xenon and a halogen lamp to respectively cover the blue and red part of the solar spectrum. Before each measurement set, the light intensity of the solar simulator is recorded by a calibration cell with a known J_{sc} . To ensure precise temperature control, the cell is held by vacuum on a brass chuck coated with gold. The chuck is regulated in temperature with peltier elements themselves cooled by a water chiller. This setup permits easy tuning of the cell temperature from 10°C to 70°C to achieve temperature-depend J - V measurements (denoted J - $V(T)$ in this thesis). An example of J - $V(T)$ is shown in Fig. 2.4 (b). A multi-purpose version of this measurement chuck developed during this thesis is shown in Fig. 2.4 (c). The contribution of the probe resistances is avoided by using a four probes configuration. Finally, a sourcemeter (Keithley, 2601A) is used to sweep the voltage from the reverse polarization up to above the cell's V_{oc} . The light J - V technique can be carried at variable illuminations in order to easily

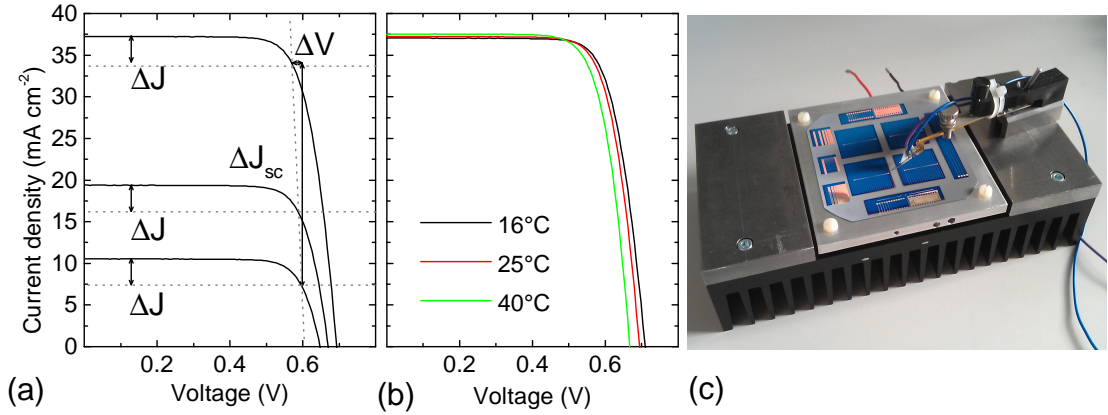


Figure 2.4: (a) J - V curves at three different illuminations and extraction method of R_s (b) J - V curves measured at different cell temperatures (c) Multi-purpose temperature-controlled measurement chuck.

extract the series resistance R_s of the cell. This method is shown in Fig. 2.4 (a): Intersections of the several J - V curves at different illuminations with horizontal lines shifted of ΔJ from their respective J_{sc} are plotted and linked by a straight line. ΔJ is chosen in order to have the intersection at a voltage slightly above the V_{mpp} . Finally R_s is extracted from the slope of the fitting curve with ΔJ and ΔV as defined in Fig.2.4(a): [Pysch 2007]

$$R_s = \frac{\Delta V}{\Delta J_{sc}} \quad (2.7)$$

2.4.3 External and internal quantum efficiency

The measurement of how efficiently a solar cell converts photons *at a given wavelength* in collected charge carriers may be expressed in three ways:

- **The external quantum efficiency (EQE)**, defined as the ratio of the number of collected charge carriers over the number of *incident* photons.
- **The internal quantum efficiency (IQE)**, defined as the ratio of the number of collected charge carriers over the number of photons *that enter in the cell*. The link between EQE, IQE and reflectance are expressed as : $IQE(\lambda) = \frac{EQE(\lambda)}{1 - Refl(\lambda)}$
- **The spectral response (SR)**, defined as the ratio of the collected charge carrier current to the incident photon power.

The experimental setup is presented in Fig. 2.5 (b). A white halogen light source is monochromatized at a specific wavelength and then chopped to allow a lock-in detection. This is necessary

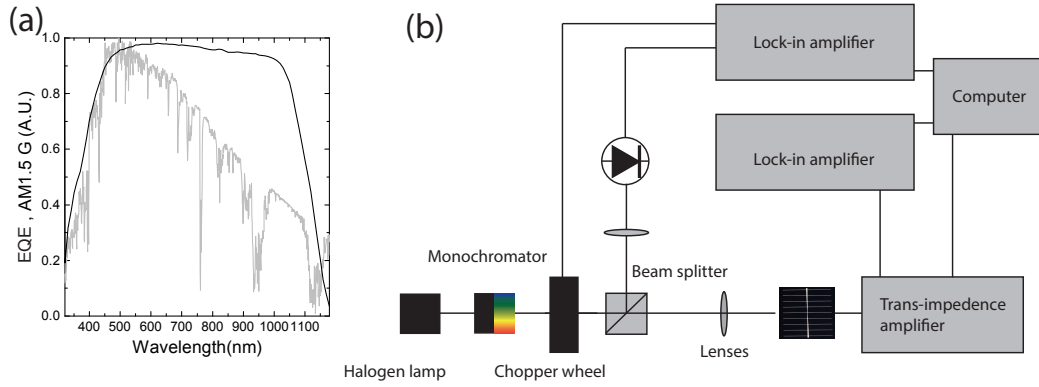


Figure 2.5: (a) EQE measurement and the AM1.5 G solar spectrum intensity (b) Schematic of the EQE experimental setup.

as the generated current of the probing beam is orders of magnitude lower in intensity compared to ambient light or light bias. After this modulation, the light beam is divided in two: half of the beam is collected by a reference photodiode with a known EQE and half is focused in a $1 \times 2 \text{ mm}^2$ spot between two fingers of the front grid. The J_{sc} can be deduced from the EQE measurement by multiplying the EQE curve with the AM1.5 G spectrum and by integrating this product between 310 nm and 1200 nm as shown by Eq. 2.8. [Stueckelberger 2014]

$$J_{sc|EQE} = \int_{310}^{1200} EQE(\lambda) \cdot spectrum(\lambda) \cdot d\lambda \quad (2.8)$$

In this thesis, EQE is measured mainly in an in-house built setup based on a Horiba micro HR grating monochromator allowing a spectral range from 310 nm to 1200 nm. The reflectance needed to assess the IQE is measured with a spectrophotometer as presented in section 2.3.3. Figure 2.5 (a) shows an EQE measurement and the AM1.5 G solar spectrum intensity.

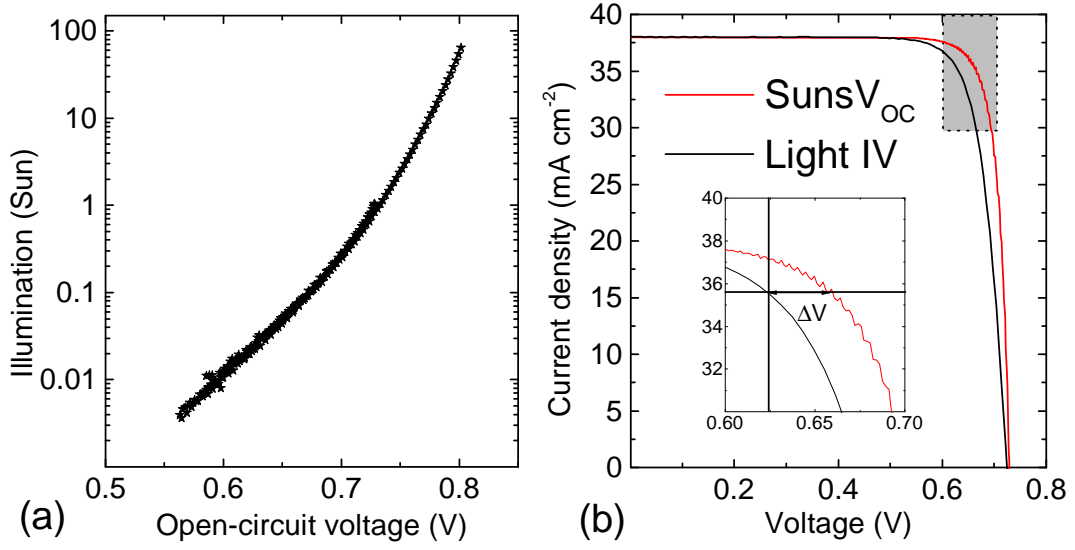


Figure 2.6: (a) Log-Lin plot of illumination as a function of the cell V_{oc} (b) Equivalent J - V curve from $SunV_{OC}$ with light J - V curve and method to extract the series resistance.

2.4.4 $SunsV_{OC}$ measurement

$Suns-V_{OC}$ is based on the direct measurement of the cell V_{oc} at different light intensities. The cell is illuminated with a flash lamp while the cell's V_{oc} and the light intensity are simultaneously recorded by a voltmeter and a calibrated photodiode respectively. [Sinton 2000] An example of an illumination- V_{oc} Log-Lin plot is shown in Fig.2.6 (a). The light intensity typically ranges from 100 Suns to less than 10^{-3} Sun. As no current flows out of the cell during the measurement, an equivalent J - V curve free of any transport related losses (i.e. no series resistance) can be plotted. Figure 2.6 (b) shows both light- and $Suns-V_{OC}$ - J - V . By extracting the voltage difference ΔV between the two J - V curves at the maximum power point (MPP) of the light J - V , the series resistance evaluated at the MPP is found as the relation expressed in Eq. 2.9. [Wolf 1963][Pysch 2007]

$$R_s|_{SunsV_{OC}} = \frac{\Delta V}{J_{MPP}} \quad (2.9)$$

2.4.5 Photoluminescence

Photoluminescence allows to probe the minority carrier lifetime through the intensity of the radiative recombination. In this technique, the sample is illuminated with a sub-bandgap light source and the light re-emitted by the radiative recombination process is recorded by a camera with a filter to suppress the light source signal. This technique allows to record mapping of the minority carrier lifetime and may be used for instance to probe the homogeneity of the surface passivation. [Trupke 2005] [Seif 2015a]

3 Silicon Heterojunction solar cells front-metallization by copper electrodeposition

Summary

We show in this chapter how electrodeposition of metals can be used for the metallization of high-efficiency SHJ solar cells. In particular, we first discuss a process based on a double electrodeposition of a Ni-Cu stack. As a result, this technique significantly improves the device performance, increasing the efficiency by 0.4 % absolute due to an 1.1 mA/cm^{-2} gain in the J_{sc} . However, occurrence of nano- and macro-voids at the Ni/ITO interface were evidenced which can possibly reduced the finger adhesion. To overcome this, a second metallization process based on a Cu seed-layer was developed. For this approach, we demonstrated that by using the proper chemistry for the seed-layer back-etching and for the electrolyte, a Cu front-grid can be electrodeposited on TCOs with high sensitivity to chemical etching such as IZO and ZnO. Finally, a variant of this process was developed for the back-metallization of IBC-SHJ.

3.1 Introduction and motivation

This chapter discusses the front-metallization of SHJ devices by using Cu electrodeposition to form the metallic front-grid and is partially based on a paper published in the [IEEE Journal of Photovoltaics](#). [Geissbuhler 2014]¹ Sections taken from this paper are marked by the symbol †.

The structure of this chapter is as follow: First, we describe the benefits for SHJ devices to replace the standard Ag paste screen-printing by a Cu electrodeposition. In this respect, a state-of-the-art of the copper electrodeposition technique applied to SHJ devices is then

¹The results presented here were obtained with the help of A. Lachowicz, A. Faes, N. Badel, Q. Jeangros, Maroua Mestiri, Fabienne Bobard, A. Tomasi, L. Barraud, A. Descoeudres, M. Despeisse, S. De Wolf and C. Ballif. Contributions are gratefully acknowledged.

Chapter 3. Silicon Heterojunction solar cells front-metallization by copper electrodeposition

presented. Next, experimental aspects specific to the Cu electrodeposition are discussed. The integration of this metallization process in SHJ solar cells is thus two-fold: First, an approach based on a double Ni-Cu electrodeposition is investigated. Then, a second approach based on a Cu seed-layer is developed and its advantages compared to the Ni-Cu stack are discussed. Finally, we show how this metallization technique can be adapted in order to be used with front-TCOs highly sensitive to chemical etching.

3.1.1 Motivation[†]

Silver-free front-contact metallization is a topic of increasing interest for crystalline silicon solar cell processing [ITRPV 2015] [Lennon 2013], mainly because of the high price of silver, which is becoming increasingly incompatible with cost-effective photovoltaics. [Green 2011] For diffused-junction silicon solar cells, the most common alternative to screen printing of silver paste is the plating of a nickel-copper stack. [Bartsch 2010] In this process, the dielectric antireflective coating (ARC) can be used as a self-aligned plating mask by opening it either by laser ablation or by sintering of a seed layer, possibly firing-through the ARC. [Aleman 2009][Glunz 2006] A nickel layer is then deposited by plating, which forms a nickel-silicide barrier against copper diffusion after post-metallization annealing. [Tous 2012] Finally, copper is plated onto the seed layer to create the conductive core of the metal finger. Thanks to the absence of contact-firing-related wafer warping effects, plating is also more compatible with the use of thin wafers. Recently, electroplated copper front-contact metallization was demonstrated for silicon heterojunction (SHJ) solar cells. [Hernandez 2012] [Munoz 2012] [Papet 2013]

As previously seen in section 2.2.6, at the front side of SHJ devices, where optical shadowing and electrical resistivity losses must be balanced, the metallic grid is usually made by silver paste printing. [Zicarelli Fernandez 2010] To preserve the electronic quality of the a-Si:H layers, processes above 250 °C must be avoided. Therefore, thick-film metallization procedures can rely on curing but not on sintering processes, implying for silver pastes electrical resistivity three to six times higher than their high-temperature counterparts and consequently increased silver consumption to guarantee similar grid conduction. [De Wolf 2012] The latter point is a second reason (next to cost benefits) for the replacement of low-temperature silver pastes by plated copper in SHJ devices, since this allows for a significant reduction in metallization coverage at the front side while keeping the same front-grid resistance. Thirdly, during the annealing needed for silver paste curing in SHJ solar cell fabrication, the electronic and optical properties of the transparent electrodes may change. [Barraud 2013] For some transparent electrodes such as hydrogenated indium oxide, the interface with the metal may deteriorate as well. [Barraud 2013] In addition, annealing can also affect the passivation quality of the a-Si:H either beneficially when damage induced during the ITO sputtering processes are recovered [Demaurex 2012], or detrimentally when additional deep defects are created due to doped a-Si:H degradation. [De Wolf 2009] Copper plating does not require curing of the metal, which may offer additional advantages, allowing post-processing annealing to be fully geared towards

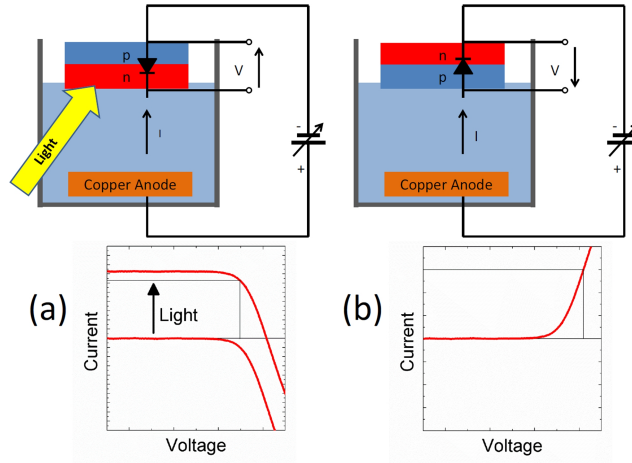


Figure 3.1: Schematic of electrodeposition setups for (a) light-induced plating and (b) electroplating. Figure from [Geissbuhler 2014]

optimizing the transparent electrodes and passivation films. Finally, ITO is known to provide an efficient barrier against copper diffusion, a problem for many silicon-based electronic devices that want to use copper for contact formation. [Liu 2005][Hsieh 2009] Fortunately, SHJ architecture provides this barrier intrinsically without any additional step or material in the process flow.

3.1.2 State-of-the-art of Cu electrodeposition techniques for SHJ solar cells[†]

Electro-induced plating metallization techniques can be separated into two classes: i) Light-induced plating (LIP), where the deposition current is "self-generated" by the solar cell under processing and ii) electroplating, where the deposition current is provided externally. [Lennon 2013] Figure. 3.1 (a) shows a schematic view of an LIP setup and the cell J - V curve in both dark and illuminated conditions. In this diagram, the voltage is defined with respect to the negative cell terminal and the current direction is indicated by the arrow inside the electrolyte (i.e. positive when flowing from the copper anode to the cell). In the LIP case, the deposition side of the cell is its negative terminal. Since the deposition current must flow in the direction opposite to the solar cell diode, this current cannot be supplied by an external source (Fig. 3.1 (a), dark J - V curve). To enable deposition, the sample is illuminated in such way the metal deposition current is self-generated by the cell. The point of operation of the cell can be maintained close to the short-circuit condition by using an external source. [Lennon 2013] If the positive terminal of the cell structure needs to be metallized, illumination should be omitted and the deposition current can be directly applied by an external source to the rear side of the cell which has to be kept dry or insulated. Fig. 3.1 (b) shows the electroplating setup and the related J - V curve in this case. Based on this, for SHJ devices, the plating technique depends on the cell structure: In the case of a front-emitter device on an n-type wafer (i.e. hole collection at the front or illumination side), the deposition current flows in the cell diode

Chapter 3. Silicon Heterojunction solar cells front-metallization by copper electrodeposition

direction and electroplating can be used. In the case of a rear-emitter cell on an n-type wafer or a front-emitter device on a p-type wafer (i.e. electron collection at the front), the device needs to be illuminated to enable metal deposition. [Descoeudres 2013] We note that electroplating may also be carried out by applying the potential of an external source directly on the side to deposit. However, in this case, a sufficiently conductive seed layer must be present to improve the lateral conductivity of the front TCO to ensure good plating homogeneity. Recently, Hernandez *et al.* demonstrated a solar cell with a remarkable conversion efficiency of 24.2% with a cell area of 171.28 cm². In this case, copper was grown by using electroplating on a pre-deposited seed layer. [Hernández 2013] The same authors also demonstrated that electroplated copper metallization can significantly improve device performance to enable operation under moderate light concentration. By placing the cell under 15 suns, cell efficiency was enhanced by 15% relative by using a redesigned front grid, whereas silver printed cells suffered from excessive resistive losses under similar test conditions. [Hernández 2013] Recent progress has also been reported on patterning techniques dedicated to SHJ copper plating. In contrast with diffused-junction silicon solar cells where the dielectric ARC prevents plating between the metallic fingers, SHJ devices feature a front ARC that is conductive over the full device area. Masking is therefore required to pattern the front electrode. For this purpose, industrially compatible inkjet printing of hot-melt masks was reported to enable patterning of 50- μ m-wide metallic fingers with a copper thickness of 15 μ m. [Hermans 2013] Papet *et al.* used this technique to form the plating mask prior to electrodeposition. In their process, a \approx 1- μ m-thick nickel layer was deposited prior to 15 μ m of copper to improve finger adhesion. The same authors demonstrated cell efficiencies of 22.3% and 21.7% on cell areas of respectively 153 cm² and 239 cm². [Papet 2013] Copper-plated cells are also well suited for integration into innovative module concepts such as those using the smart-wire connection technique. As a result, module efficiencies similar to those achieved with silver screen printing have been reached while completely removing silver from the front metallization. Furthermore, this interconnection technique increases the yield compared to soldering as the entire connection process remains below 160 °C. [Söderström 2013] [Faes 2014]

3.2 Photolithography processes for electrodeposition patterning

As previously seen in section 3.1.2, a patterning technique based on an insulating material is required in the case of electrodeposition on a conductive TCO. In this thesis, photolithography was used for this end (see section 2.2.7). Although this technique is far too costly for being used at an industrial scale with the tools usually used in micro-electronic, its high-resolution and high-accuracy in alignment make this technique ideal for research. The use of a photoresist structure to cast a subsequent metal electrodeposition is well known in surface micro-machining as the "lithographic, galvanoformung, abformung" (LIGA) process, where a poly-methyl methacrylate (PMMA) resist is patterned by using a synchrotron x-ray source. This technique enables to produce thick structures ($> 500 \mu$ m) with extreme aspect-ratio up to 100. [Becker 1986] [Sze 2001] To avoid the use of expensive synchrotron radiation source, a

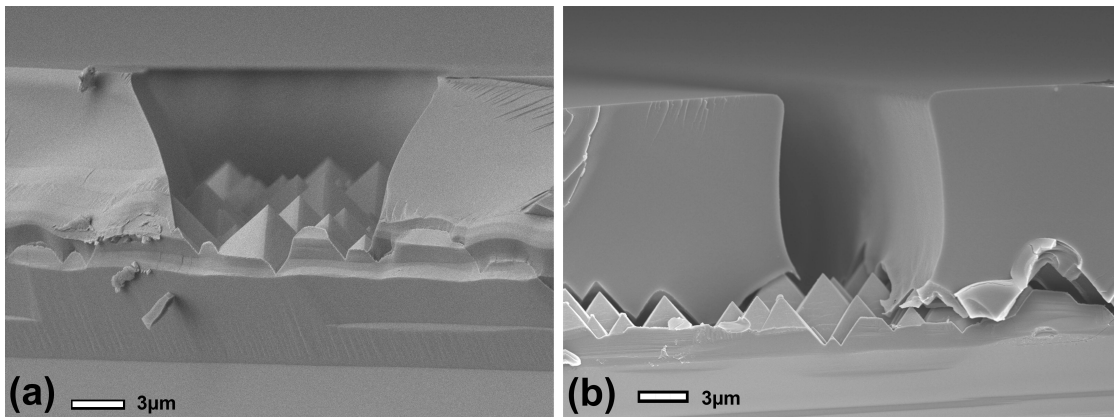


Figure 3.2: Scanning electron microscope cross-section views of: (a) Patterned double-layer of AZ1518 (b) Patterned single layer of AZ40xt.

variant process called UV-LIGA was developed where an UV-sensitive photoresist, such as SU-8, is used instead of PMMA and exposed by using standard UV mask aligner. [Despont 1997] This technique is nowadays widely used to create micro-mechanical compounds such as mechanical watches gears. [Lorenz 1988]

3.2.1 Photoresist dispensing

In the case of using photoresist to cast the growth of metallic fingers for solar cells, photoresist film-thicknesses in the range of $\approx 20\mu\text{m}$ are sufficient. Therefore, positive-tone photoresists which are more easily patternable and removable than SU-8 can be considered such the AZ1518 or the AZ9260. [Carazzetti 2006] However, in contrast of mirror-polished wafers usually processed in surface micro-machining, solar cells wafers feature random pyramids texture with typical pyramid-size ranging between few μm up to $10\mu\text{m}$. Therefore, a sufficiently thick layer must be dispensed in order to prevent the pyramid tips remaining bare and lead to potential unwanted electrodeposition spots. In this thesis three dispensing techniques of photoresist were studied:

- **Spin coating** is one of the most commonly employed technique for photoresist dispensing. In this technique, the wafer is spun at a speed ranging between 400 to 6000 RPM and the photoresist is dispensed either before (static dispensing) or during the spinning (dynamic dispensing). With the AZ9260 photoresist, a single spin coating can provide a film-thickness in the $20\mu\text{m}$ range. However, an important over-thickness was experienced on the wafer edges due to the high-viscosity of this resist. To overcome this issue, AZ1518 was used and deposited by doing two (or eventually three) successive spin coatings at 800 RPM in dynamic-mode. After each spin coating step, a soft-bake at 100°C was done during 3 to 5 min. Figure 3.2 (a) shows a groove in the such photoresist film before the metal growth. The none-vertical sidewalls are due in this case to an over-exposure.

The use of a thick-positive photoresist specifically designed for electrodeposition was investigated with the AZ40xt resist. This photoresist enables to reach a sufficiently important film thickness in a single-step spin coating while avoiding over-thicknesses at the wafer edges. However, a weak-adhesion and the occurrence of a channel in between the photoresist and the TCO was observed as shown in Fig. 3.2 (b).

- **Spray coating** allows the deposition of a photoresist film on rough surfaces with a good coverage. Here, AZ1518 photoresist was manually sprayed on the wafer and subsequently soft-baked at 100°C during 5 min. This technique has the advantage of consuming a smaller amount of photoresist compared to multiple-steps spin coating. However, due to the manual spraying, reproducibility of the film-thickness may be an issue.
- **Dip coating** was tested as well to deposit AZ1518 photoresist films. In this technique, the wafer is vertically withdrawn of a photoresist beaker with a controlled speed which determines the photoresist film thickness. [Madou 2002] In this work, no specific dip coating equipment was available and the wafers were simply dipped in AZ1518 diluted with a solvent and subsequently soft-baked at 85°C during 10 min in an oven. Despite the simplicity of this technique, sufficiently homogenous photoresist films were obtained with the advantage of significantly reducing the processing time compared to spin- or spray-coating.

These three techniques were independently used during this thesis to dispense the photoresist. The UV-exposition was then carried out by using an U.V. mask aligner (MA/BA 6, SUSS MicroTec) with a typical energy density ranging between 500 and 800 mJ/cm². Finally the photoresist development was made by using AZ351b developer diluted in deionized water (ratio 1:4). No hard-bake was made in order to preserve the shape of the photoresist. [Geissbuhler 2014]

3.3 Electrodeposition setups

Two different electrodeposition setups were used during this work for both the electrodeposition of nickel and copper:

- **Suncup from NB technologies** This system is shown in Fig. 3.3 (b) and is based on an overflowing fountain where the wafer is placed on the fountain-top and maintained at its position by a Bernoulli effect. As the wafer "floats" on the electrolyte, its back-side remains dry. The overflow is made by a pump which ensures as well a sufficiently well-mixed electrolyte. This setup can be equipped with LEDs for LIP purposes. [Notarp 2015]
- **Home-build electrodeposition system** This small volume system was designed to be easily disassembled in order to clean it or change its electrolyte and to be operated with

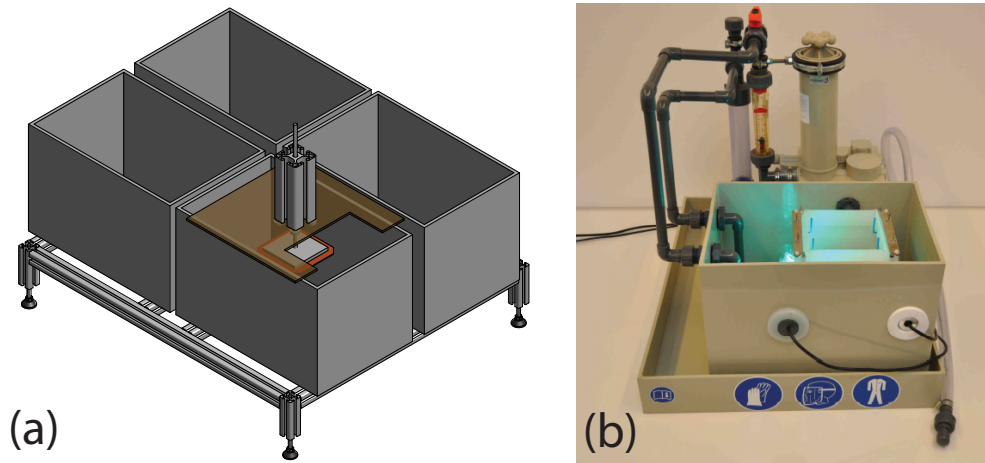


Figure 3.3: (a) Home-build electrodeposition system sketch (b) Suncup electrodeposition tool from NB technologies. [Notarp 2015]

a limited amount of electrolyte (<5L). The electrolyte is contained in a polypropylene tank where a Cu plate placed at the bottom of the tank acts as the anode. The stirring of the electrolyte is realized by a simple magnetic stirring rod. The handling of the wafer is made by a vacuum chuck with an adjusting screw for the fine tuning of the wafer height. The wafer is then adjusted in height in order to have only the front-side in contact with the electrolyte. A schematic of this setup is shown in Fig. 3.3 (a).

3.4 Nickel-Copper front electrodes

This section discusses the first approach to form an front-grid based on a double Ni-Cu electrodeposition and compares it with state-of-the-art screen- and stencil-printing.

3.4.1 Experimental[†]

In this experiment, 12 cells precursors were processed as described in section 2.1 with a-Si:H layers deposited in the KAI-M reactor. ITO and ITO/Ag were respectively used as the front and back electrodes and deposited by sputtering in the MRC 603. Each precursors contains three cells $2\text{ cm} \times 2\text{ cm}$ and feature the hole-collector at the front-side. After the PECVD, cell precursors with equivalent minority-carrier lifetime were sorted into three equal groups: A) metallization by Ni-Cu electroplating, B) metallization by silver paste screen-printing, and C) metallization by silver paste stencil-printing. Precursors from groups B and C were metallized prior to those from group A in order to co-anneal all precursors at $190\text{ }^{\circ}\text{C}$ for 30 min. The finger pitch was optimized for each metallization technique in accordance with the material resistivity and the obtainable finger geometries. A general overview of the Ni-Cu process is given in Fig. 3.4: First, a photolithography with a double spin-coating of AZ1518 as described in section 3.2 was used as the patterning technique. A CO_2 plasma treatment was applied to

Chapter 3. Silicon Heterojunction solar cells front-metallization by copper electrodeposition

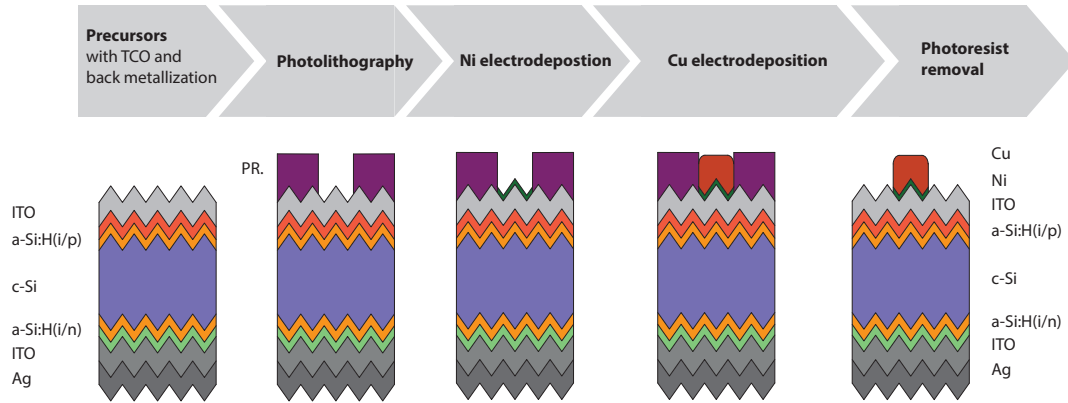


Figure 3.4: Process-flow of the electrodeposited metallization with the Ni-Cu approach.

promote the surface wettability of the resist. This treatment was carried out in the XL PECVD system at room temperature by using a pure CO_2 gas flux. Due to the poor adhesion of Cu when deposited directly on ITO, a $\approx 1\text{-}\mu\text{m}$ -thick Ni layer was electroplated to improve finger adhesion. This deposition was immediately followed by the growth of $\approx 14\text{ }\mu\text{m}$ of Cu. Both Ni and Cu layers were electroplated by using the Suncup plating tool from NB technologies. Nickel and copper electrolytes were based on nickel sulfamate and copper sulfate, respectively. After the metal growth, the photoresist was removed by using acetone and isopropanol alcohol. The geometries of the metal lines were measured by using a confocal microscope (LEXT, Olympus).

3.4.2 Results and discussions[†]

Figure 3.5 presents the short-circuit current density (J_{sc}), the open-circuit voltage (V_{oc}), the fill-factor (FF) and the cell efficiency extracted from light J - V measurements. We present statistics of a minimum of eight cells for each metallization technique. A significant J_{sc} gain of 1.1 mA cm^{-2} is realized with the Cu electroplating technique compared to silver paste screen-printing. Three-dimensional confocal microscopy images of metallic fingers obtained by the three metallization techniques are presented in Fig. 3.6. A significant width reduction from 72 to $15\text{ }\mu\text{m}$ is observed between the silver paste printing technique and the Cu electroplating. Based on the measured geometries, optical shadowing losses of respectively 5.3 and 2.1% are deduced for those two techniques, leading to a theoretical J_{sc} gain of 1.3 mA cm^{-2} when copper plating is used. The difference compared to the measured gain is explained by the round profile of the screen-printed fingers which partially reflects the light towards the cells. [Woehl 2008]

A $\approx 3\text{ mV}$ lower average V_{oc} is measured for the copper electroplated cells compared to their

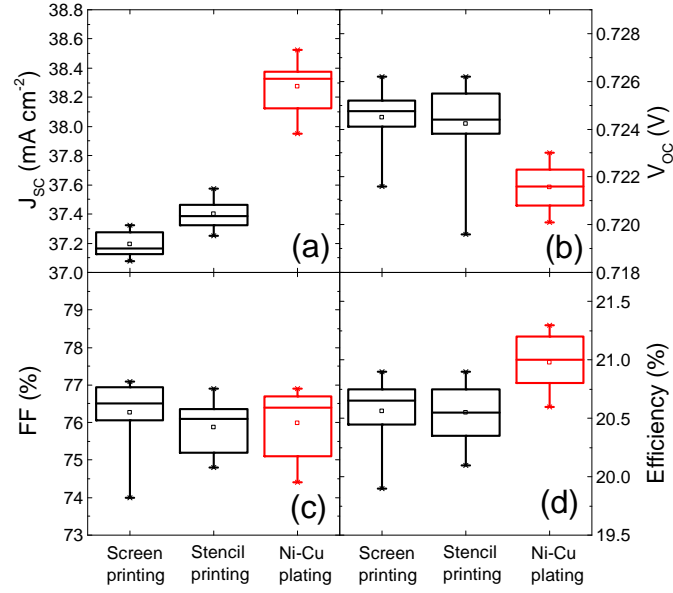


Figure 3.5: Cell parameters extracted from illuminated J - V measurements for the three metallization techniques: (a) short-circuit current density (J_{sc}) (b) open-circuit voltage (V_{oc}), (c) fill-factor (FF) and (d) energy conversion efficiency. Figure from [Geissbuhler 2014]

silver paste printed counterparts. The additional wafer manipulation needed for photolithography in the case of plated metallization may explain this slight drop. However, the magnitude of this effect remains negligible on the cell efficiency. As shown in Fig. 3.5 (c), no clear FF trend is observed between the three metallization techniques. A similar statement can be made for the series resistance presented in Fig. 3.7 (c). To further investigate how the series resistance may differ when comparing silver paste printing to copper electroplating, we evaluated separately all of the front-metallization contributions. The metallization part of the series resistance may be separated into four contributions: i) TCO resistance caused by the lateral flow towards the finger, ii) contact resistance between the front ITO and the metal, iii) finger (line) resistance and iv) busbar (line) resistance. The TCO/metal specific contact resistivity and the metal electrical conductivity assumed in this model were respectively extracted from TLM and line-resistance measurements (Fig. 3.7 (a) and (b), respectively). It is worth underlining that the copper electrical conductivity is close to the bulk value of pure copper reported in the literature. [Schuster 2001] We measured a front-TCO average sheet resistance of $106 \Omega/\square$ by using TLM. These values, combined with the geometries of the metallization extracted from the confocal microscopy images, allow us to evaluate quantitatively the four separate contributions, for both techniques (see section 1.1.5). [Green 1982] For the screen-printed fingers, we assume a finger width of $50 \mu\text{m}$ corresponding to its average width. An overview of all the resistive contributions of the front metallization is presented in Table. 3.1.

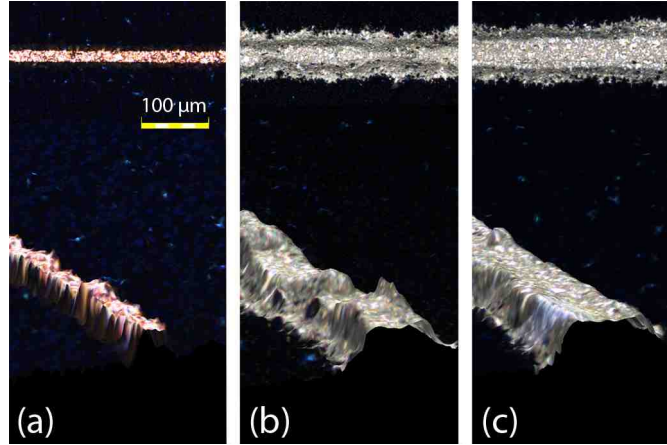


Figure 3.6: Optical microscopy top views and confocal microscopy three-dimensional reconstructions of metallic fingers made by: (a) Ni-Cu electroplating, (b) silver paste screen-printing and (c) silver paste stencil-printing. Figure from [Geissbuhler 2014]

Thanks to its small obtainable feature sizes, electroplated copper metallization can be realized with significantly reduced finger spacing and smaller optical shadowing losses. Therefore, with finger spacing twice as narrow in the copper metallization case, an important lowering of the front TCO's contribution to series resistance is seen. Even if the total contact area between the metal and the front TCO is reduced, transfer lengths deduced from the specific contact resistivity remain shorter than the finger geometries (≈ 3 and $10 \mu\text{m}$ for the silver paste and the copper electroplating, respectively). Hence, the contact resistance contribution related to the TCO/metal interface remains negligible compared to the total series resistance. Due to the lower resistivity of the electroplated copper and to the smaller amount of current flowing through a single finger (as more fingers are present), resistive losses in the metallic fingers are significantly decreased with the copper electroplating. For the busbar, similar values for both techniques are deduced since the busbar dimensions have been strongly reduced in the copper electroplating case. Finally, from this model, front-metallization series resistances of 0.563 ± 0.031 and $0.192 \pm 0.022 \Omega\cdot\text{cm}^2$ are deduced respectively for the silver paste screen-printing and the copper electroplating. Overall, we conclude that the resistive losses related to the front contact are a relatively small part of the overall series resistance, which includes the a-Si:H/TCO interfaces and crystalline bulk resistance. However, the $0.37 \Omega\cdot\text{cm}^2$ difference between the two metallization techniques deduced from the model is not observed in the measured series resistance values [Fig. 3.7 (c)], nor in the FF, as it should give an absolute FF difference of 1.7%. Since the main difference is in the front-TCO contribution, a possible explanation is that a significant part of the current might flow laterally through the crystalline bulk instead of exclusively in the front TCO. To further investigate this, the local voltage across the front TCO was mapped using an in-house-built scanning tool (see section 5.2. From the front-TCO sheet resistance and the voltage drop U_{drop} between the finger and the half finger

Table 3.1: Detailed comparison of the resistive losses in the front metallization and geometries assumed in the model. Data from [Geissbuhler 2014]

	Ag paste screen-printing	Cu electroplating
Number of fingers	9	20
Finger width [μm]	50	15
Metal thickness [μm]	25	15
Busbar width [μm]	500-100	200-30
P_{opt} losses [%]	5.25	2.08
R_{TCO} [$\Omega \text{ cm}^2$]	0.436	0.088
$R_{contact}$ [$\Omega \text{ cm}^2$]	0.004	0.008
R_{finger} [$\Omega \text{ cm}^2$]	0.053	0.03
R_{busbar} [$\Omega \text{ cm}^2$]	0.069	0.066
R_{total} [$\Omega \text{ cm}^2$]	0.563 ± 0.031	0.066 ± 0.022

spacing, the current density flowing through the front TCO (J_{TCO}) can be calculated from:

$$J_{TCO} = \frac{U_{drop}}{R_{\square} \frac{s^2}{8}} \quad (3.1)$$

where s is the finger spacing. Fig. 3.8 [(a) and (b)] shows the voltage profiles at conditions close to the maximum power point (MPP) and to short circuit, respectively. The cell used in this study features the same screen-printed silver front grid as the cells previously presented. At short circuit [Fig. 3.8 (b)], a voltage drop of 14 mV is measured which corresponds to the 13 mV predicted by equation 3.1 with the measured J_{sc} and R_{\square} Sheet (36.5 mA cm^{-2} and $57 \Omega_{\square}$). However, as seen in Fig. 3.8 (a), the magnitude of the voltage drop is dramatically reduced when the cell operates close to the MPP. At this point, a J_{TCO} of 8.5 mA cm^{-2} is deduced from the voltage scan. Therefore, it can be assumed that only part of the generated current is flowing in the front TCO when the cell operates at the MPP. [Bivour 2014] [Aberle 1994] This consideration strongly impacts the model presented in Table 3.1. As a consequence, the TCO series resistance contribution is reduced by one order of magnitude. Hence, for our front-grid designs, the front-metallization series resistance becomes comparable for the screen-printed silver and the electroplated copper cells, consistent with the measured series resistance values shown in Fig. 3.7 (c). Therefore, under one-sun illumination and with the front-grid geometries used in this study, copper electroplating does not lead to an improvement of the electrical properties of the cell but merely to an important optical improvement. Finally, with the J_{sc} gain and similar V_{oc} and FF achieved by using copper electroplating, an efficiency gain of 0.4% absolute is achieved as displayed in Fig. 3.5 (d). We emphasize that, contrary to $2 \text{ cm} \times 2 \text{ cm}$ cells, a FF improvement is expected for larger-area devices such as 5- or 6-inch cells due to the higher conductance in copper-plated fingers. As the resistive power losses go with the finger length squared, the FF gain will be higher for cells featuring a small number of busbars and becomes smaller for multi-busbar or smart-wire approaches. [Söderström 2013]

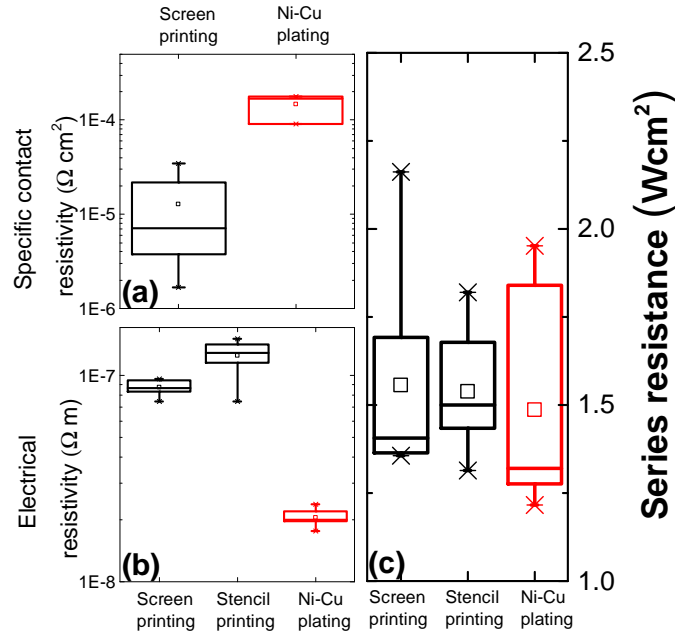


Figure 3.7: Specific contact resistivity between the front ITO and the metallization. (b) Electrical resistivity of deposited metals. (c) Cell series resistance extracted from Suns V_{OC} and light J - V comparisons. Figure from [Geissbuhler 2014]

By comparing silver screen-printed and copper-plated grids for a 6-inch cell, a FF gain of 2.3 and 1.9% absolute is expected for configurations of three and five busbars, respectively.

3.4.3 Characterization of Ni-Cu metallization by electron microscopy[†]

Electron microscopy was used to investigate the structure and the interfaces of the Ni/Cu electroplated fingers. A cross section was prepared using focused ion beam (FIB) milling and then imaged by scanning electron microscopy (SEM) in a Zeiss NVision 40 workstation equipped with an energy-dispersive X-ray (EDX) silicon drift detector. A secondary-electron SEM image, which is sensitive to crystallographic orientation, is shown in Fig. 3.9 (a). The layer observed around the finger in Fig. 3.9 (a) is due to deposition of carbon prior to FIB milling to reduce curtaining effects. Combined with a height of $15 \mu\text{m}$ obtained by confocal microscopy, an aspect ratio of 1:1 is measured from Fig 3.9 (a). The metallic finger presents the inverse shape of the positive-photoresist cast with a narrowing at its base. Each layer can be identified from the EDX map displayed in Fig. 3.9 (b). The conductive copper core does not exhibit any voids at this length scale. This observation can be linked with the measured electrical resistivity, which is close to the bulk value of pure copper. However, microscopic cracks or voids are observed at the ITO/Ni interface, as shown in Fig. 3.9 (c). The origin of such features is so far unclear. Defects observed in flat regions in the middle of pyramid facets probably result from local delamination due to internal stress [inset A of Fig. 3.9 (c)]. Alternatively, voids

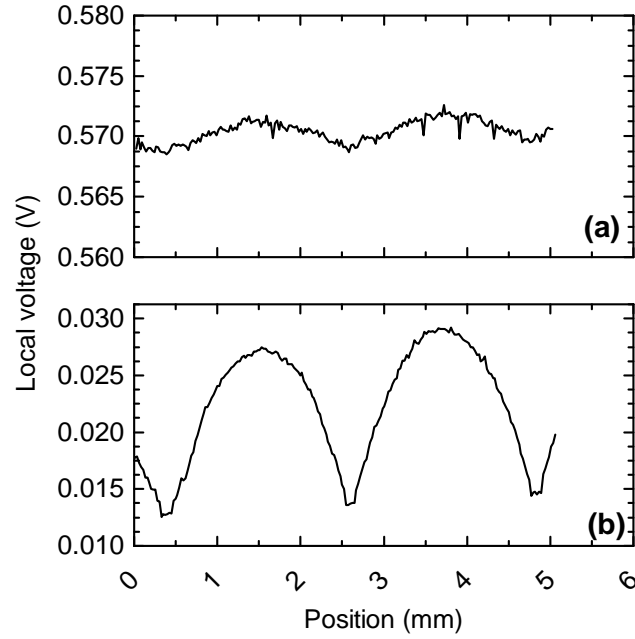


Figure 3.8: Voltage profiles across the front TCO when the cell is operated at (a) the MPP and (b) short circuit. The cell used in this study has a front-TCO sheet resistance of $57 \Omega_{\square}$. Figure from [Geissbuhler 2014]

located within valleys of the random pyramids may be caused by the different growth surfaces of the metal [inset B of Fig. 3.9 (c)].

To further investigate these interfaces using scanning transmission electron microscopy (STEM), a thin lamella was extracted using a conventional FIB lift-out technique from a dedicated sample, which featured a thin copper layer on nickel electrodeposited on a polished wafer. STEM characterization was performed in a FEI Tecnai Osiris equipped with four windowless silicon drift detectors for EDX analysis. Fig. 3.10 (a) shows a bright-field micrograph of the entire Si/ITO/Ni/Cu stack (image of the transmitted electrons, sensitive to crystallographic orientation), while a superposition of the corresponding copper, nickel, indium and silicon EDX signals is displayed in Fig. 3.10 (b). As seen at larger scale in the FIB/SEM cross section, the copper layer appears free of porosity. Fig. 3.10 (c) displays a dark-field (DF) image of the Ni/Cu interface (image made using diffracted electrons, sensitive to crystallographic orientation). The corresponding Ni/Cu EDX map shown in Fig. 3.10 (d) demonstrates a well-defined interface with no significant inclusion of nickel in copper. Some contrast features are observed to span across the Ni/Cu interface in the DF image [arrows in Fig. 3.10 (c)], which probably indicates some copper epitaxy on the nickel layer and results in a good adhesion between these layers. Fig. 3.10 (e) displays a high-angle annular dark-field (HAADF) micrograph of the Si/ITO/Ni interfaces (electrons scattered at high angles, sensitive to mass and thickness). The associated EDX map is shown in Fig. 3.10 (f). As the contrast in the HAADF image depends on the mass and thickness of the sample in each pixel (Fig.

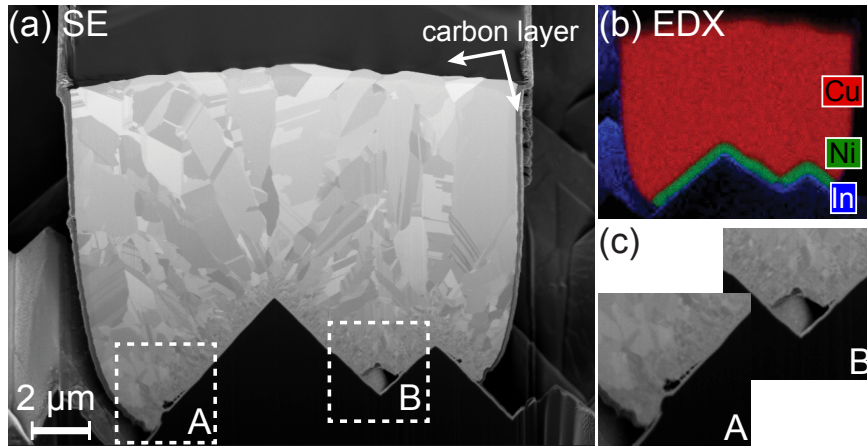


Figure 3.9: (a) Secondary-electron SEM image of a Ni/Cu finger FIB cross section (in lens detector). (b) EDX maps of copper (using the $K\alpha$ X-ray energy), nickel ($K\alpha$) and indium ($L\alpha$). (c) Magnified view of two different kinds of defects observed at the ITO/Ni interface. Figure from [Geissbuhler 2014]

3.10 (e)), the intensity can be interpreted. A line profile across the ITO/Ni interface exhibits a drop of intensity at the position of the interface. As no lighter elements are detected by EDX at this position, it can be assumed that this decrease probably results from the presence of voids of a few nm in size at the ITO/Ni interface. At the macroscopic level, this may result in weaker adhesion at the ITO/Ni interface compared to the Ni/Cu interface. This issue has been avoided for the cells presented in this study by carefully optimizing the growth conditions of the metal layers.

3.4.4 Implementation in high-efficiency SHJ solar cells[†]

Based on the promising results obtained with front-ITO devices, high-efficiency SHJ solar cells were realized by using the copper electroplating technique. The main difference compared to the solar cells previously presented in this paper is in the front-TCO and a-Si:H deposition processes. To further increase J_{sc} , a more transparent IO:H/ITO front TCO stack was used [Barraud 2013], while the intrinsic and doped a-Si:H layers were deposited in an Octopus II cluster tool. Furthermore, light reflection was further reduced by the deposition of a second ARC consisting of 140 nm of MgF_2 . Fig. 3.11 shows the J - V characteristic under one-sun illumination. A J_{sc} gain of 0.9 mA cm^{-2} is observed compared to the ITO-only cells presented in Fig. 3.5 (a). Comparison of the J_{sc} values prior to and after the MgF_2 deposition indicates a gain of $\approx 0.2 \text{ mA cm}^{-2}$ due to the second ARC. Improvements in the a-Si:H deposition led to an increased V_{oc} of 728 mV. The contact between the a-Si:H(n) layer and the rear TCO was also improved. Combined with optimized a-Si:H layers, the FF was thereby improved to 78.6%. Finally, an energy-conversion efficiency of 22.4% was obtained.

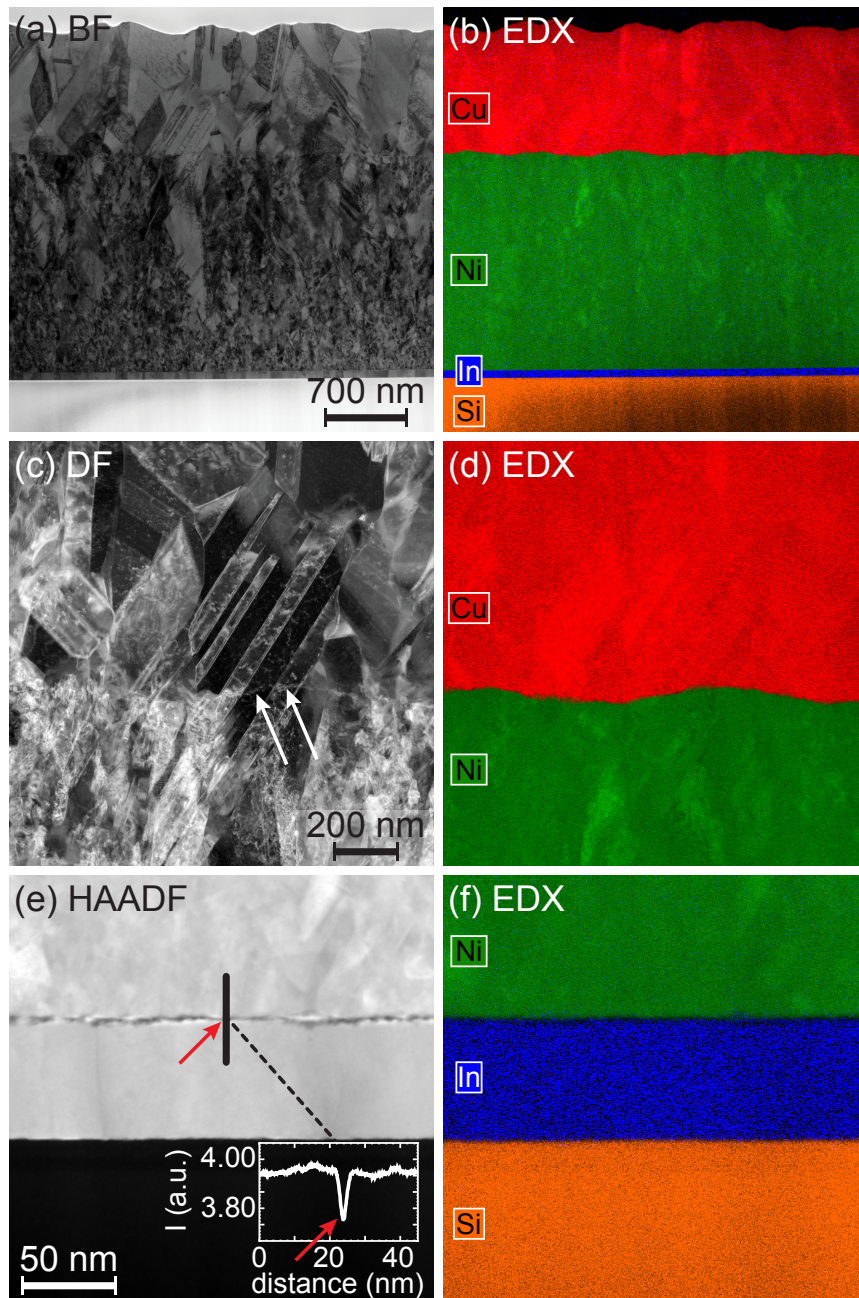


Figure 3.10: (a) Bright-field TEM observation of the entire Si/ITO/Ni/Cu stack, and (b) EDX map of the image displayed in (a). (c) Dark-field image of the Ni/Cu interface, with the corresponding EDX map in (d). Arrows indicate contrast features spanning across the Ni/Cu interface in (c). (e) High-angle annular dark-field image of the Si/ITO/Ni interfaces along with an intensity profile across the ITO/Ni interface, with arrows indicating porosity. (f) EDX map of the image displayed in (e). Figure from [Geissbuhler 2014]

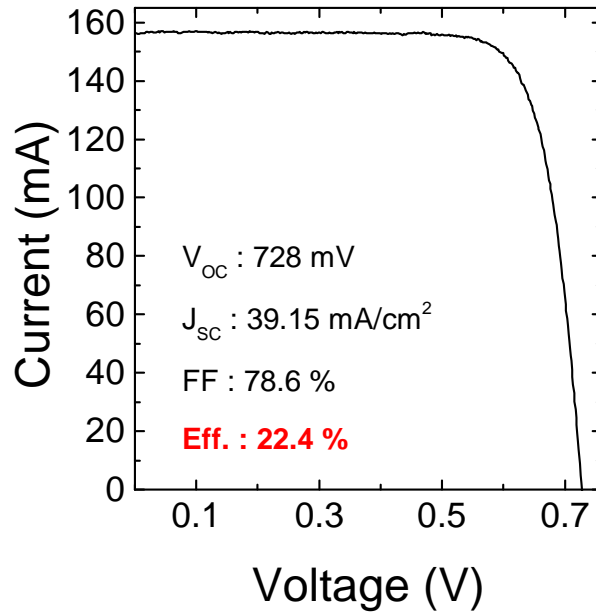


Figure 3.11: J - V characteristic under one-sun illumination. The cell features a copper electroplated front grid, an IO:H/ITO front TCO stack and a MgF_2 second ARC. Figure from [Geissbuhler 2014]

3.4.5 Conclusions[†]

We have demonstrated that Ni-Cu electroplating can be a reliable alternative to screen-printing for the front metallization of SHJ solar cells. While avoiding the use of silver, copper electroplating dramatically reduces the metallization coverage at the front side. Accordingly, the J_{SC} increased by 1.1 mA cm^{-2} . As a result, an average gain of 0.4% absolute in cell efficiency was obtained. A detailed investigation of the front-metallization series resistance contributions has demonstrated that, mainly due to the reduced finger spacing allowed by copper electroplating, the series resistance should be reduced by more than $0.3 \Omega \text{ cm}^2$. However, experimentally, the average series resistance remains identical for the silver paste screen-printing and the copper electroplating techniques. Maps of the local voltage on the front TCO have demonstrated that even if the generated current flows entirely through the front TCO at short circuit, only a fraction uses this path when the cell operates at the MPP. This effect limits the expected gains from reduced finger spacing achievable by plating, especially for small cells. STEM reveals the presence of nanometric voids at the TCO-metal interface possibly reducing the finger adhesion. Although no quantitative measurement of the finger adhesion was made—as this metallization was primarily investigated for record efficiency device—poor finger adhesion was avoided by carefully optimizing the growth conditions of the metal layers. Finally, we have demonstrated a cell with 22.4% energy-conversion efficiency by using this Ni-Cu electrodeposition metallization.

3.5. Towards more versatility and reliability in electrodeposited front-contact

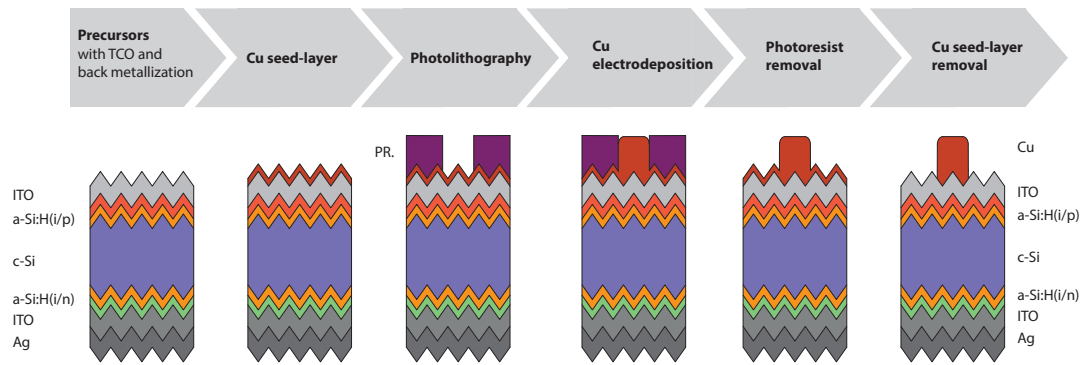


Figure 3.12: Process-flow of the metallization with the Cu seed-layer approach.

3.5 Towards more versatility and reliability in electrodeposited front-contact

3.5.1 Cu-seed layer based electrodeposition process

As previously seen in section 3.4, the direct electrodeposition of Ni on ITO leads to the occurrence of micro and nano-voids at the interface between these two materials. These voids reduce the finger adhesion and thus the reliability of the solar cell. As a consequence, this process is clearly non-compatible with TCOs with higher sensitivity to chemical etching. To overcome this issue, we developed a radically different approach based on a Cu seed-layer, replacing the Ni layer. [Mulligan 2011] A description of this process is presented in Fig. 3.12: First, a blanket Cu seed-layer is thermally evaporated directly on the front-TCO. The photolithography is then carried out as usual for the patterning. Next, the Cu is locally thickened by electrodeposition at the place where the fingers are defined by the photoresist. After the removal of the photoresist in acetone and isopropyl alcohol, the Cu seed-layer remaining in between the fingers is back-etched. Key advantages of this technique compared to the Ni-Cu approach previously described are thus as follows: First, the Ni electrodeposition is completely avoided suppressing therefore the need of a second electrodeposition tool and the maintenance of the Ni electrolyte. Moreover the suppression of the Ni sulfamate based electrolyte presents as well an advantage for the safety and the chemical handling. In addition, the Cu seed-layer can be directly contacted during the electrodeposition, removing the need to pass the deposition current through the wafer. The latter is particularly interesting for cells featuring the positive terminal at the rear-side as no specific LIP-setup is required.

3.5.2 Cu seed-layer back-etching optimization

As previously mentioned, the direct contact of the electrolyte may be detrimental for the front TCO. Although this issue is solved by the insertion of the seed-layer, a new critical step appears in the process proposed in Fig. 3.12 with the necessity to back-etch the Cu seed-layer at the

Chapter 3. Silicon Heterojunction solar cells front-metallization by copper electrodeposition

end of the process while preserving the underlying front-TCO pristine. In this section, we investigate the impact of two Cu etchant on various TCOs. The first Cu etchant considered for this process was based on a solution of sulfuric acid (H_2SO_4) and hydrogen peroxide both diluted at 1% in deionized water. [Battey 1987] By using this etchant, metallization by using the Cu seed-layer approach was successfully demonstrated on SHJ cells with ITO front-TCO without noticing any changes on the front-TCO. However, when applied to amorphous indium zinc oxide (IZO), this TCO was completely etched away in less than 2 min. In order to quantify exactly the etching selectivity between the Cu seed-layer and the front-TCO, a determination of the etch-rate was performed on various TCOs often used for the front-electrode of SHJ devices (IO:H, ITO, IZO, ZnO:B). In this study, a second Cu etchant based on a basic solution water was investigated as well. For both Cu etchants, an etching rate of $\approx 50 \text{ nm min}^{-1}$ was obtained on thermally evaporated Cu. Thus, with a typical Cu seed-layer thickness of $\approx 200 \text{ nm}$, a back-etching time of 4-5 min is required. We note here that the back-etching time is typically overestimated of at least 1 min to ensure a perfect removal of the Cu seed-layer. Therefore, it implies that the TCO is in direct contact with the Cu etchant during a 1-2 min period. Table 3.2 presents the etch-rates obtained during this study.

Table 3.2: Etch-rates of different TCOs for H_2SO_4 - and basic-based Cu etchants.

TCO Layer	Etchant	Etch-rate [nm min^{-1}]
ITO	basic-based	0
ITO	H_2SO_4 -based	11
IO:H	basic-based	0
IO:H	H_2SO_4 -based	12
IZO	basic-based	0
IZO	H_2SO_4 -based	56
ZnO:B	basic-based	25
ZnO:B	H_2SO_4 -based	>6500

As seen in Tab. 3.2, the sulfuric acid based is normally supposed to remove $\approx 10\text{-}20 \text{ nm}$ of ITO or IO:H during the back-etching of the Cu seed layer. The main difference between the preliminary ITO-based solar cells mentioned above is that the TCOs of this study were not annealed reducing therefore their chemical resistance as the films were not yet crystallized. In the case of IZO, no recrystallization happens during the cell annealing needed for the sputtering damage recovery. [Morales-Masis 2015] Hence, accordingly to previous observation of Tab. 3.2, the 55 nm min^{-1} measured etch-rate makes it impossible to use the sulfuric acid based Cu etchant for this TCO. Even more dramatically, the LPCVD ZnO:B shows etch-rates of $> 6 \mu\text{m min}^{-1}$ for this Cu etchant. Conversely, when the basic-based recipe is used, no significant sign of etching can be evidenced for ITO, IO:H and IZO. Even more surprisingly, the LPCVD ZnO:B known for being extremely sensitive to chemical etching is preserved with an etch-rate negligible in respect with the typical ZnO:B film thickness of few μm . [Hupkes 2012] Hence, this second recipe was preferred to the sulfuric acid based one as a prefect selectivity

between Cu and a wide variety of TCOs is demonstrated.

3.5.3 Impact of the Cu seed-layer removal on the a-Si:H surface passivation

An additional question raised by the Cu seed-layer approach is that some parts of the device—as for instance the cells edges—are not necessary protected by the front-TCO which can result to two possible issues: First, the Cu of the seed-layer can more easily diffuse into the device as no TCO diffusion barrier is present and create mid-gap recombination center [Sze 2001]. Second, the Cu etchant can damage the a-Si:H surface passivation if not protected by the front-TCO. This uncovered area may be experienced in industrial 6 inches solar cells where the wafer edges are masked during the TCO sputtering or in the area in between our 2 cm × 2 cm research cells. To answer to these questions, a Cu seed-layer was evaporated directly on a a-Si:H(*ip*) stack and subsequently stripped by using the sulfuric acid based Cu etchant. The minority carrier lifetime was respectively measured before the Cu evaporation, after the seed-layer removal and after a 200°C annealing during 30 min. To disentangle the effect of the Cu evaporation from the back-etching, a second sample was processed in a similar way but without the Cu evaporation. It can be seen on Fig. 3.13 that a τ_{eff} decay is experienced after the removal of the seed-layer only for the sample where a Cu layer was deposited. Importantly, no further decay was recorded after a 200°C annealing during 30 min. We conclude therefore that the τ_{eff} decay is likely induced by the Cu thermal evaporation rather than by the diffusion of Cu atoms. [Rohatgi 1980]. We note here that the magnitude of this effect remains relatively modest as τ_{eff} is still higher than 2 ms in the worst case. Hence, from the Cu seed-layer back-etching point-of-view, no significant losses in efficiency are expected.

3.6 Electrodeposited Cu front-grid on IZO front TCO

3.6.1 Motivation for IZO as the front-TCO

A critical factor in the front-TCO design for high-efficiency SHJ devices is to maintain a sufficiently low parasitic light absorption in the visible and near-infrared spectral regions while maintaining reasonably low sheet resistance to avoid associated series resistance losses. As previously seen, the most commonly used material for this purpose is ITO which can be possibly replaced by high-mobility TCO such as IO:H to further increase the front-electrode transparency as seen in section 3.4.4. However, IO:H exhibits several drawbacks counterbalancing its interesting electrical and optical properties: First, an important specific contact resistance is experienced when such layer is annealed in direct contact with the metallic front-grid. As a consequence, a thin-ITO capping layer is inserted to prevent the latter issue. [Barraud 2013] Although no annealing is made after the deposition of the metallic front-electrode in the electrodeposition case, the thin ITO capping is however required to improve the stability of the IO:H to water ingress. [Barraud 2013] In addition, the IO:H deposition relies on a partial pressure of water vapor which considerably increases the process complexity. To overcome

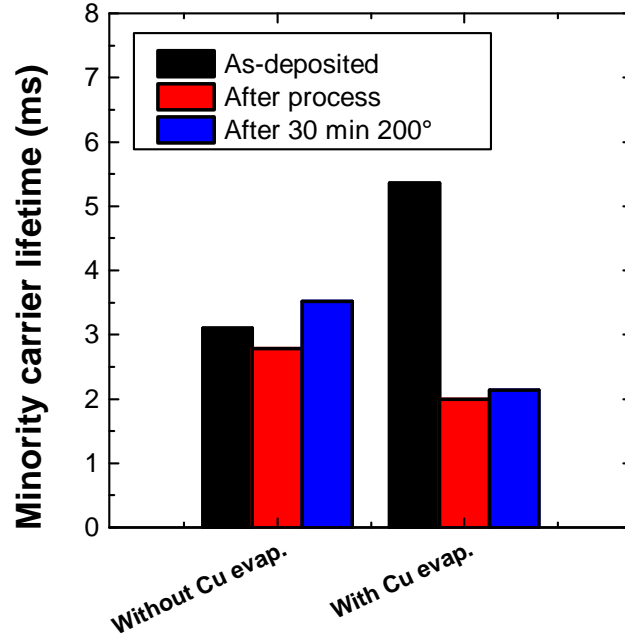


Figure 3.13: Minority carrier lifetime at a carrier injection of 10^{15} cm^{-3} for two process sequences.

these problems, IZO was proposed as a replacement material of IO:H.² [Morales-Masis 2015]

3.6.2 Experimental

We deposited IZO films by using RF sputtering in the Oerlikon Clusterline system, a substrate temperature of 60°C and an IZO target composition of 90 wt.% In_2O_3 and 10 wt.% ZnO. [Morales-Masis 2015] As-deposited IZO films demonstrated a Hall mobility of $60 \text{ cm}^2/\text{Vs}$ and a carrier density of $2 \times 10^{20} \text{ cm}^{-3}$. The cells were then metallized by using the Cu seed-layer approach as described in Fig. 3.12 with a seed-layer thickness of $\approx 200 \text{ nm}$. The back-etching was then carried out during $\approx 5 \text{ min}$ in the basic-based etchant.

3.6.3 Results and discussions

Figure 3.14 shows the certified light J - V curve of the 4-cm^2 device with IZO as the front-TCO and an electrodeposited Cu front-grid. We note here that this 22.3% energy conversion efficiency shown in Fig. 3.14 is the one of highest certified efficiency obtained so far by the EPFL PV-Lab. Despite a good efficiency, a weaker adhesion of the Cu electrodeposited front-grid was observed compared to previous ITO-based devices. To further investigate the quality of the IZO/Cu interface, a FIB cross-section was prepared. Figure 3.15 (a) shows a cross-section

²The results presented here were obtained with the help of S. Martin de Nicolas. Contributions are gratefully acknowledged.

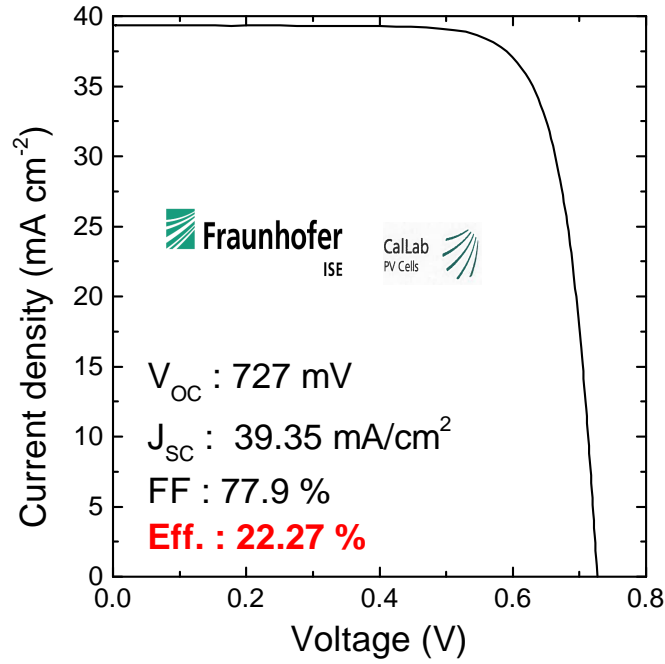


Figure 3.14: J - V characteristics under one-sun illumination certified by the Fraunhofer Callab. The cell features a Cu electroplated front grid, an IZO front TCO and no second ARC.

of an equivalent cell than the record device presented in Fig.3.14. We can clearly identify that an important under-etching is occurring during the removal of the Cu seed-layer and removes almost any contact between the finger and the front-TCO. This effect clearly explains the weaker finger adhesion previously experienced.

To overcome this adhesion issue, we significantly reduced the Cu seed-layer thickness down to ≈ 30 nm. As a direct consequence, the back-etching time is decreased from 5 min down to 1 min. To quantify the impact of the latter, a new FIB cross-section was prepared. It can be seen on Fig. 3.15 (b) that the under-etching is significantly reduced and only appears in less than $2 \mu\text{m}$ from the finger edges. As a consequence, the finger adhesion was significantly improved. The finger of Fig. 3.15 (b) exhibits also a pronounced "mushroom"-shape due to an insufficiently thick photoresist film leading to an anisotropic growth of the Cu finger above the top of the photoresist cavity. Although this effect should be avoided for obvious optical reason, this reduced contact area shows an outstanding adhesion of the Cu finger on the IZO front-TCO, however. A demonstration of high-efficiency SHJ devices featuring an electrodeposited front-metallization with a thin Cu seed-layer is shown in section 6.7.1 for MoO_x hole collector SHJ devices. An additional advantages of reducing the Cu seed-layer thickness is—in addition of reduced processing time—that the Cu seed-layer absorptance is less than 10% for wavelengths above 650 nm enabling therefore LIP-processes.

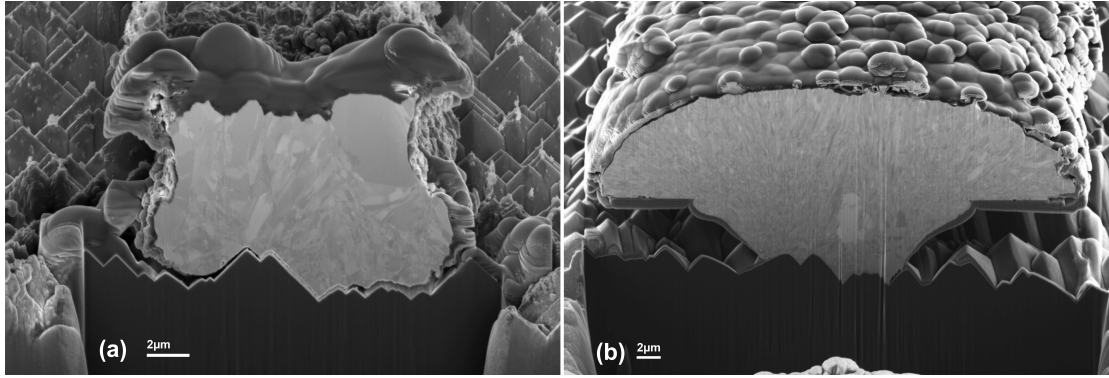


Figure 3.15: Focused ion beam cross-section of electroplated copper finger deposited with the Cu seed-layer layer approach on IZO front-TCO. The Cu-seed layer thickness was respectively (a) 200 nm and (b) 30 nm.

3.6.4 Conclusions

To conclude, we demonstrated that the Cu seed-layer approach is a reliable metallization technique for IZO-based SHJ devices. Due to the higher sensitivity to chemical etching of IZO compared to ITO or IO:H, it is necessary to ensure that the Cu etchant used for the seed-layer removal will not attack the IZO film. In this respect, we demonstrated that basic-based etchant allows a perfect selectivity between Cu and IZO. However, to avoid excessive under-etching underneath the metallic finger possibly leading to lower finger adhesion, we showed that the Cu seed-layer thickness has to be as thin as possible in order to minimize the back-etching time to the minimum. By depositing only a 30-nm-thick seed-layer, the under-etching issue was then entirely solved.

3.7 Electrodeposited Cu front-grid on LPCVD ZnO:B front-TCO

3.7.1 Motivation

Indium is after silver a second rare and expensive element involved in the fabrication of SHJ solar cells. Thus, an increasing interest is seen nowadays in order to find indium-free alternative TCOs. In this respect, a possible candidate is boron-doped zinc oxide (ZnO:B) deposited by LPCVD well known for thin-film silicon solar cells. [Favier 2011] [Boccard 2014] This TCO relies on abundant and non-toxic materials and is obtained by using a soft deposition process. In contrast to the other indium-based TCOs used in this thesis, the carrier concentration of LPCVD ZnO:B is at least one order of magnitude lower than for IO:H requiring therefore a higher film thickness to obtain a reasonable sheet resistance. [Barraud 2013] Thus, the anti-reflection is not anymore obtained by a quarter wavelength ARC but rather by the native film-roughness obtained during the LPCVD growth. [Ding 2013b] Hence, due to the low carrier concentration, excessive FCA can be avoided. [Choong 2010] We present here a study of how

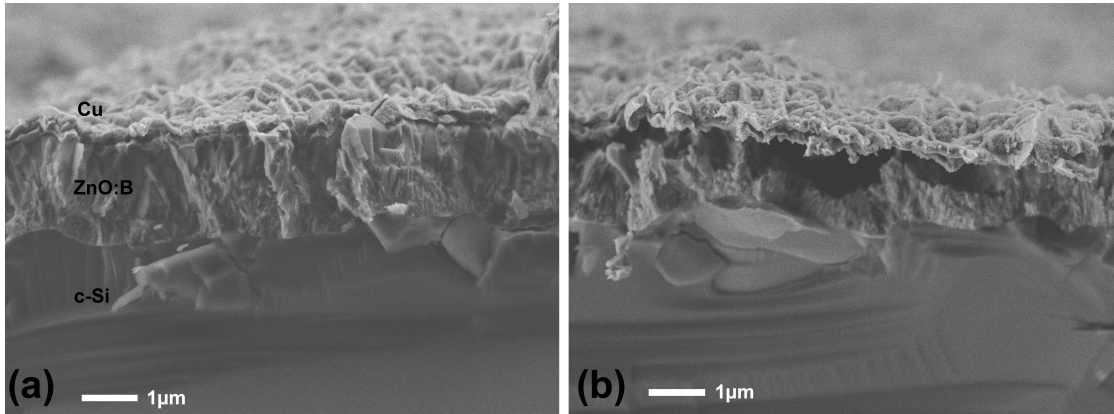


Figure 3.16: Cross-sections of wafer with a ZnO:B and Cu stack (a) without and (b) with a 10 s dip in the sulfuric acid based Cu electrolyte.

Cu electrodeposition can be applied to SHJ devices with a ZnO:B front-TCO.³

3.7.2 Experimental

As previously seen in Tab. 3.2, ZnO:B is well known to be easily etched even in weak acids. When considering the Cu electrodeposition on such TCO, two critical steps can be identified: i) The back-etching of the Cu seed-layer and ii) the Cu electrodeposition step. For Cu seed-layer back-etching, we demonstrated that the basic-based Cu etchant has a sufficiently slow etch-rate on ZnO:B to allow the seed-layer removal. However, during the Cu electrodeposition, the ZnO:B film is only protected from the sulfuric acid based Cu electrolyte by the ≈ 200 -nm-thick Cu seed-layer. To verify if this layer is providing a sufficiently watertight protection, a textured wafer with a $\approx 2 \mu\text{m}$ thick LPCVD ZnO:B and a 200-nm-thick Cu layer was dipped during 10 s in the sulfuric acid based Cu electrolyte. After rinsing in deionized water, the wafer was cleaved to observe its cross-section with SEM. Figure 3.16 (a) and (b) shows the cross-section of a reference sample (i.e not dipped in the Cu electrolyte) and the sample dipped during 10 s. We clearly see that even for such short exposure, the ZnO:B is practically completely etched. This may be either explained by pin-holes present in the Cu seed-layer or by a non-conformal covering of the ZnO:B pyramids allowing the Cu electrolyte to reach the ZnO:B film. As a consequence, a non-acidic Cu electrolyte must be used for LPCVD ZnO:B-based SHJ solar cells.

Cells featuring respectively a 0.9 or 2.2 μm -thick ZnO:B as the front-TCO and the standard ITO/Ag back-electrode were used for this study. After the deposition of a ≈ 200 -nm-thick Cu seed-layer, standard photolithography was carried out. To overcome under-etching of the ZnO:B previously experienced, we replaced the sulfuric acid based Cu electrolyte by an alkaline one (pH = 7.93). [Schafer 2010] The 200-nm-thick Cu seed layer was then removed in 4

³The work presented here was partially made in the framework of the semester project of Maroua Mestiri. Contributions are gratefully acknowledged.

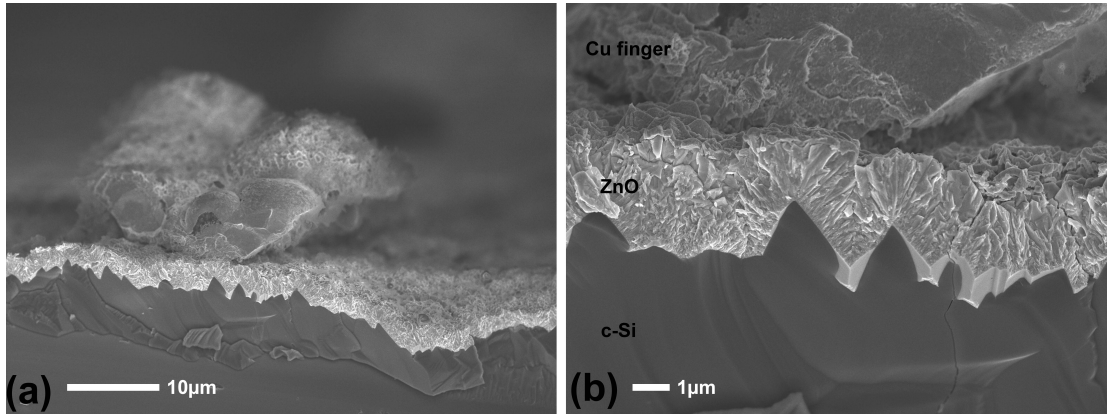


Figure 3.17: Cross-section of a Cu finger electrodeposited on a LPCVD ZnO:B.

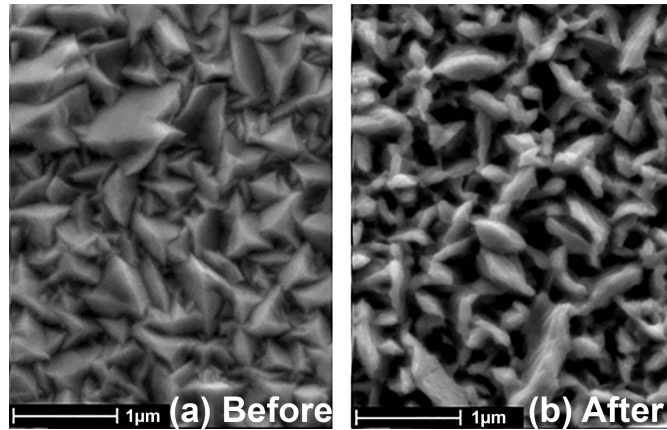


Figure 3.18: SEM top-view observation of LPCVD ZnO:B (a) before and (b) the back-etching in basic-based Cu etchant.

min in the basic-based Cu etchant. Figure 3.17 shows a cross-section of this devices observed in SEM. It can be clearly observed that the alkaline Cu electrolyte preserved the LPCVD ZnO:B layer as no under-etching can be observed.

The impact of the basic-based Cu etchant on the ZnO:B was investigated as well. Figure 3.18 (a) and (b) shows an SEM top-view observation of the ZnO:B surface respectively before and after the back-etching. ⁴ We clearly observe that the surface topography of the ZnO:B is significantly changed with the appearance of more sharp geometries. At the macroscopic level, this effect induces a more efficient scattering of the light. We note that this effect is beneficial in the present case as the anti-reflective effect of our film is solely ensured by the light scattering and not by a quarter wavelength condition ARC.

Finally, we discuss the cell performances of these ZnO:B-based devices with electrodeposited Cu front-grid. Figure 3.19 (b) shows the EQE curves for cells with ZnO:B film-thicknesses of

⁴SEM pictures were taken by A. Hessler-Wyser. Contributions are gratefully acknowledged

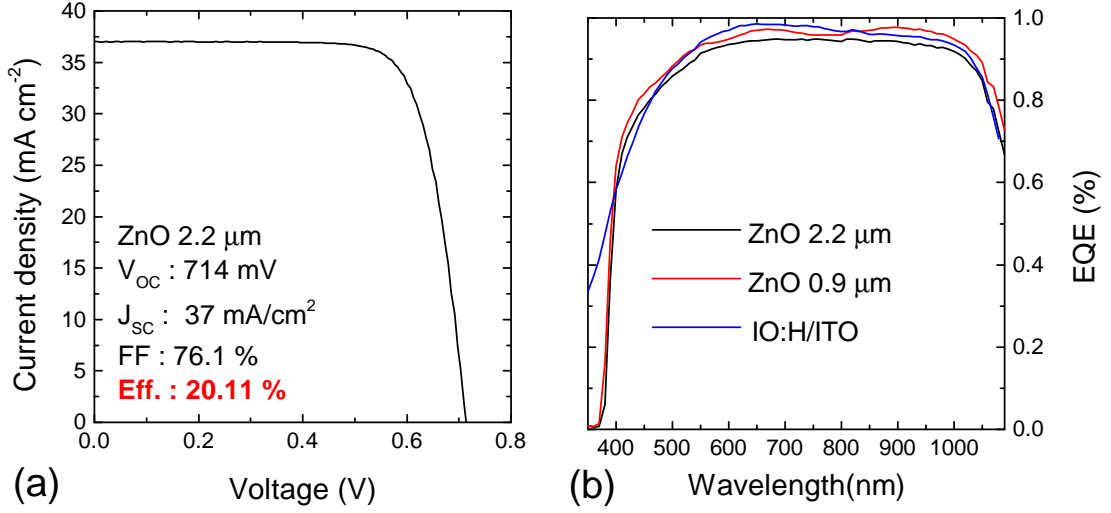


Figure 3.19: (a) light J - V characteristic of the 2.2 μm -thick ZnO:B SHJ devices with electrodeposited Cu front-grid. (b) EQE of the 0.9 and 2.2 μm -thick ZnO:B SHJ devices and of an IO:H/ITO reference.

respectively 0.9 and 2.2 μm . An EQE curve of an IO:H/ITO device is given for comparison purpose. A few percent lower EQE is seen for both ZnO:B thickness compared to the IO:H/ITO front-TCO in the 500-800 wavelength range. This is explained by a less efficient anti-reflective provided by the textured LPCVD ZnO:B than by the quarter wavelength ARC. It is also seen that the thinnest ZnO:B provides a better light-trapping than the thicker one. This is likely explained by the tendency of thick ZnO:B films to "planarize" the c-Si random pyramids thus reducing the double textured effect provided by both the c-Si and ZnO:B pyramids. By integrating these EQE curves with the AM1.5 G spectrum, short-circuit current-density of 38.2 and 39.36 mA cm^{-2} were found for the 0.9 and 2.2 μm -thick ZnO:B films respectively. The light J - V characteristic of the 2.2 μm -thick ZnO:B is shown in Fig. 3.19 (a). Consequently to a front-grid shadowing of a few percent, a J_{sc} of 37 mA cm^{-2} is measured.

3.7.3 Conclusion

To conclude, we demonstrated that Cu electrodeposition to from the metallic front-grid is feasible even on LPCVD ZnO:B front-TCO despite its high sensitivity to chemicals etching. In particular, we showed that the Cu seed-layer does not offer an efficient protection of the ZnO:B and the use of an alkaline Cu electrolyte is therefore required. Finally, SHJ solar cells combining ZnO:B as the front-TCO and electrodeposited front-grid demonstrated an energy-conversion efficiency above 20%.

Chapter 3. Silicon Heterojunction solar cells front-metallization by copper electrodeposition

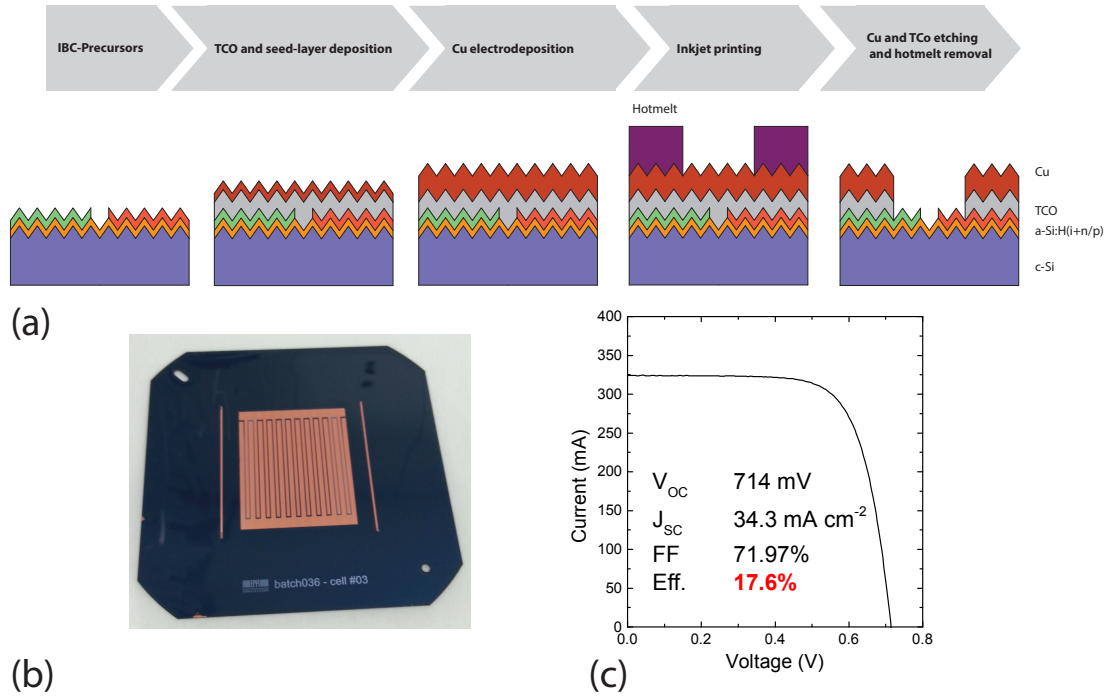


Figure 3.20: (a) Process-flow for the IBC-SHJ back-metallization with Cu electrodeposition (b) picture of the rear-side of an IBC-SHJ with Cu plated contacts (c) light $J-V$ characteristic of the IBC-SHJ device with Cu plated contacts.

3.8 Metallization of interdigitated back-contacted silicon heterojunction solar cells

3.8.1 Motivation

In IBC-SHJ devices as reported by Tomasi *et al.*, the back-electrode is usually formed by the sputtering of a TCO/Ag stack followed by an inkjet patterning and a wet chemical etching. Thus, Cu electrodeposition is interesting to deposit thick metal layer rapidly while avoiding long sputtering depositions. Furthermore, highly conductive fingers present a particular interest due to the high finger length required by the IBC geometry. We discuss here how Cu electrodeposition can be used to substitute the thick Ag layer deposited by sputtering. [Geissbuhler 2014]⁵

Figure 3.20 (a) shows the process-flow we used to fabricate IBC-SHJ devices with Cu electrodeposited back-contacts. First, a TCO/Cu stack is deposited by using respectively sputtering and thermal evaporation. The Cu layer is then thickened of $\approx 5 \mu\text{m}$ by Cu electrodeposition. The patterning is made by using an inkjet printing of a hotmelt resist. Finally, the layers are

⁵The results presented here were obtained with the help of A. Tomasi and B. Paviet-Salomon. Contributions are gratefully acknowledged.

structured by wet chemical etching followed by the removal of the hotmelt. This process follows the one described by Mulligan *et al.* [Mulligan 2011]

3.8.2 Results and discussion

Figure 3.20 (b) shows a picture of the back-side of a finished IBC-SHJ device with Cu electrodeposited contacts. Its light J - V curve and characteristics are displayed in Fig. 3.20 (c). The un-expected low J_{sc} of 34.3 mA cm^{-2} indicates an issue likely induced by a misalignment during the a-Si:H(n) a-Si:H(p) PECVD depositions.

3.8.3 Conclusion

We demonstrated that Cu electrodeposition can be as well used for the thickening of the metal contacts of IBC-SHJ devices. Despite reasonable efficiency likely due to reasons independent of the metallization process, we showed the feasibility to replace the thick sputtered Ag layer used until now by less expensive and more conductive electrodeposited Cu film.

3.9 General conclusions on metallization by copper electroplating

To conclude, we showed in this chapter the important benefits for SHJ-devices when replacing the standard Ag front-grid obtained by Ag screen-printing by an electrodeposited Cu electrode. Due to the high conductivity of the electrodeposited Cu finger and their width $< 20 \mu\text{m}$, an impressive gain of 1.1 mA cm^{-2} was demonstrated. As a consequence of this gain, the energy-conversion-efficiency was increase by 0.4 % absolute. Furthermore, we demonstrated with the Cu seed-layer approach that the electrodeposition process can be simplified—in respect to the Ni-Cu approach—while improving the reliability and allowing the use of TCOs sensitive to chemical etching. However, for the industrialization point-of-view, this metallization still requires additional simplification in the process in order to be competitive with classical screen-printing. Furthermore, the remarkable progresses recently obtained by using the smart-wire interconnection technology enable to massively reduced the silver paste consumption making it challenging for Cu electrodeposition to be cost-competitive. [Faes 2014] However, due to the indium-based coating used in the smart-wire technology, the use of a 3-5 busbars designs may still be of interest in order to limit as much as possible the indium consumption in the SHJ module manufacturing. Therefore, it is crucial for Cu electrodeposition to develop new patterning techniques and reduce the electrodeposition time. For the patterning, this can be for instance enabled by inkjet printing or flexography of the resist-mask. Both techniques already demonstrate a sufficient throughput to be compatible with mass-production. [Hermans 2013] [Lorenz 2015] Furthermore, in the photolithography case, the use of low-cost photoresist has been demonstrated by Lachowicz *et al.* with a LIP deposition of a Ni-Cu stack enabling outstanding efficiencies of up to 22.8% on 6 inches SHJ solar cells. [Lachowicz 2014] For the metal growth, a simplified plating process relying on thin Ni fingers

Chapter 3. Silicon Heterojunction solar cells front-metallization by copper electrodeposition

and the smart-wire interconnection technology was demonstrated. [Russell 2014] Ultimately, by integrating these recent advanced techniques, the use of the Cu electrodeposition may be integrated in mass-production of SHJ-devices as an efficient and silver-free replacement technique of screen-printing.

4 Patterning amorphous silicon layers by hydrogen plasma and wet chemical etching

Summary

Advanced etching techniques were tested in order to form complex a-Si:H film structures needed in advanced SHJ solar cell architectures. Wet chemical etching based on highly diluted alkaline etchants with in-situ photoluminescence monitoring demonstrate sufficiently slow etch rates and a good control of the etching depth. However, the homogeneity was found to be insufficient to accurately remove a doped a-Si:H layer without etching the intrinsic a-Si:H film underneath. Hydrogen plasma etching was then investigated. It was found that defects in the crystalline lattice of the silicon wafer are induced when there is insufficient capping of the surface by the a-Si:H(*i*) layer. Fortunately, the typical a-Si:H(*i*) film thickness used for surface passivation offers a good shielding of the wafer surface. Advanced characterizations were made to understand the extent to which the a-Si:H(*i*) film is modified during H₂ plasma etching. These measurements revealed a significant exchange of hydrogen atoms between the plasma and the a-Si:H film and an increased microstructure factor of the remaining a-Si:H(*i*) film. Finally, the impact of H₂ plasma etching on the electrical performance of cells with layers deposited on the etched film was studied.

4.1 Introduction and motivation

This chapter studies the patterning of a-Si:H layers by etching and is partially based on a paper published in *Applied Physics Letters* and reproduced with permission from [Geissbühler 2013]. Copyright 2013, AIP Publishing LLC.¹ Sections taken from this paper are marked by the symbol †.

¹The results presented here were obtained with the help of B. Demareux, J.P. Seif, D.T.L. Alexander, L. Barraud, S. De Wolf and C. Ballif. Contributions are gratefully acknowledged.

Chapter 4. Patterning amorphous silicon layers by hydrogen plasma and wet chemical etching

As discussed in section 1.1.8, all layers deposited in a standard planar silicon heterojunction (SHJ) cells are optimized regarding the trade-off between their electrical and optical properties. Often in developments of these films, improvement of one aspect can negatively impact the other (as an example, the a-Si:H(*p*) layer thickness has to be kept as thin as possible for optical reasons but thick enough to obtain good fill factor). [Holman 2012] To overcome this trade-off for further improving the energy-conversion efficiency, advanced SHJ devices may have parts of the device specifically optimized either for the light coupling into the absorber or for the electrical extraction of the charge carriers. However, as the contacts are no longer formed by planar depositions, specific patterning techniques must be developed. In standard planar SHJ devices, the majority of parasitic light absorption losses is caused by the a-Si:H(*i*) and a-Si:H(*p*) layers. Holman *et al.* quantified that these losses count for $\approx 1.6 \text{ mA cm}^{-2}$ in the short-circuit current density (J_{sc}). The transparent conductive oxide (TCO) at the front side contributes only for $\approx 0.5 \text{ mA cm}^{-2}$. [Holman 2012] Therefore, a-Si:H films are the most important layers to be structured in advanced SHJ architectures. However, we note that these layers are also the most challenging to pattern due to their extremely small thicknesses (below 10 nm) and the high cleanness required at the crystalline silicon (c-Si) surface to achieve a good surface passivation. In this respect, if a doped a-Si:H layer has to be patterned, ideally, this layer has to be *selectively* etched while preserving the a-Si:H(*i*) layer underneath. Therefore, an etch technique capable of nanometric resolution is required to achieve the latter.

Two advanced SHJ device architectures relying on a-Si:H patterning can be identified : i) the interdigitated-back-contacted SHJ solar cells (IBC-SHJ) where doped a-Si:H layers are patterned in two opposite combs placed at the rear side of the device [Tomasi 2014] [Mingirulli 2011] and ii) localized extraction passivated contact SHJ devices (LEP-SHJ) presented in chapter 5 where areas at the front side are separately optimized either for optical or electrical purposes.

Patterning techniques of a-Si:H films can be divided in two main kinds : i) selective deposition of the a-Si:H films by using a shadow mask stacked on the substrate during the PECVD deposition and ii) planar deposition of a-Si:H films followed by a patterning step and subsequent local etching. Figure 4.1 describes these two approaches to achieve a pattern with two different materials as shown in the final structure of Fig 4.1. This structure has to be achieved to respectively form the a-Si:H(*n*) and a-Si:H(*p*) combs in an IBC-SHJ device or the electrically and optically optimized parts of an LEP-SHJ device (doped a-Si:H and SiN_x respectively). In the *selective deposition* technique, after the deposition of the a-Si:H(*i*) passivation layer, the sample is unloaded to place a shadow mask for the local deposition of the first material. Next the sample is unloaded a second time and a second shadow mask with the opposite pattern is placed and aligned prior the deposition of the second material. This technique was used by Paviet-Salomon, Tomasi *et al.* to manufacture an IBC-SHJ device with energy-conversion efficiency of 22% . [Tomasi 2014] [Paviet-Salomon 2015] A main advantage of this technique is that the a-Si:H(*i*) passivation layer is preserved along the entire process. However, this technique introduces two vacuum breaks and requires complex alignment of the second mask with respect to the previous geometry. In the *local etching* way, the entire intrinsic and doped a-Si:H stack is deposited as usual. After a vacuum break to place a shadow mask, the sample

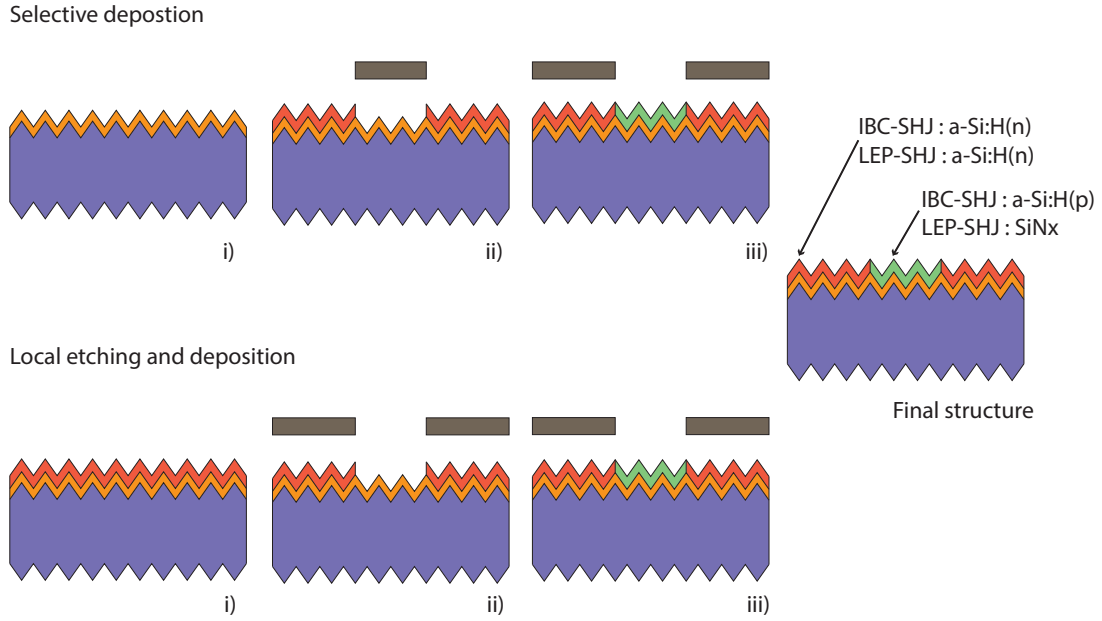


Figure 4.1: Process sequence description of both *selective deposition* and *local etching* approaches to form a complex a-Si:H film structure.

is reloaded in the PECVD to carry out a selective etching directly followed by the deposition of the second material. This process has the key advantage of allowing the etching and the subsequent deposition to happen within the same system. However, an extreme accuracy in the etching-depth is required if—as previously mentioned—the a-Si:H(*i*) layer has to be preserved. This approach was proposed by Scherff *et al.* for the fabrication of IBC-SHJ cells by using the same PECVD system for both etching and deposition. [Scherff 2011] A second approach to carry etching of a-Si:H films for IBC-SHJ purposes is the use of wet chemical etching as investigated by Greil *et al.* [Greil 2011] Even though the advantage of carrying out the etching and the subsequent deposition in the same system is lost with wet chemical etching, this approach nevertheless has advantage of being entirely compatible with photolithography. Indeed, the use of photoresist is often prohibited in PECVD reactors dedicated to a-Si:H deposition in order to avoid contamination.

This chapter is structured as follows: First wet chemical etching is investigated as a technique for a-Si:H film patterning. Next, in order to take advantage of an entirely dry process in PECVD, H₂ plasma etching is studied for a-Si:H film etching. Finally, the use of H₂ plasma etching in SHJ device manufacturing is discussed.

4.2 a-Si:H patterning by wet chemical etching

4.2.1 Introduction

Wet chemical etching is often used in the microelectronic industry for silicon patterning. The most commonly used etchants for silicon are either alkaline solutions as KOH, NaOH or TMAH or based on a pair of acids where one oxidizes the silicon and the second etches the silicon oxide. For instance, mixtures of HNO_3 and HF can be used for this purpose and are called *iso-etch*. Etch-rates of several μm per minutes can be achieved with these etchants, depending of their concentration and temperature. [Robbins 1959] [Madou 2002] Therefore, in the present case of etching a-Si:H layers with typical thickness of ≈ 10 nm, the etch rate must be reduced by several orders of magnitude to allow a good control of the etching depth. In addition, a small variation in the etching concentration, temperature of the bath or the presence of a native oxide at the a-Si:H surfaces can significantly vary the etching time. To overcome these issues, Greil *et al.* realized an *in-situ* monitoring of the passivation by using photoluminescence (PL) during the wet chemical etching with either alkaline or iso-etch etchants. While the a-Si:H(*i*) is removed, the increased surface recombination directly leads to a decay of the PL signal. Therefore, the exact moment when the a-Si:H(*i*) layer is completely etched can be identified and the etching can be stopped at the proper moment. A similar approach was investigated in this work (following the same procedure as used by Greil *et al.*) with the aim of achieving a *selective* etching of a doped a-Si:H layer while keeping the a-Si:H(*i*) passivation layer underneath pristine.

4.2.2 Experimental

For safety reasons, the alkaline etchant was preferred to the iso-etch recipe based on HF and HNO_3 . Here, a highly diluted etching solution of buffered KOH was prepared by diluting 1 part of AZ400K photoresist developer with 200 parts of deionized water. A dip in 5 % HF for 10 s was made in order to prevent an inhomogeneous start of the etching due to the native silicon oxide resistant to KOH etching. [Madou 2002] To quantify the initial passivation quality, the minority-carrier lifetime (τ_{eff}) was measured by photoconductance technique operated in transient mode directly after the HF dip. Finally, the passivated wafer was placed in a beaker containing the diluted KOH etching solution and then placed in the PL setup where images were taken during a period of 2.5 min.

4.2.3 Results and discussions

Figure 4.2 shows the PL images at different etching times. Prior the etching, τ_{eff} was measured at 1.5 ms at an excess carrier concentration of 10^{15} cm^{-3} . Accordingly, at the beginning of the etching (15 s), a strong PL signal was recorded indicating an efficient surface passivation. A clear decay of the PL intensity and thus of the surface passivation can be observed even for etching times under 1 min. If we assume that the PL intensity and the excess carrier

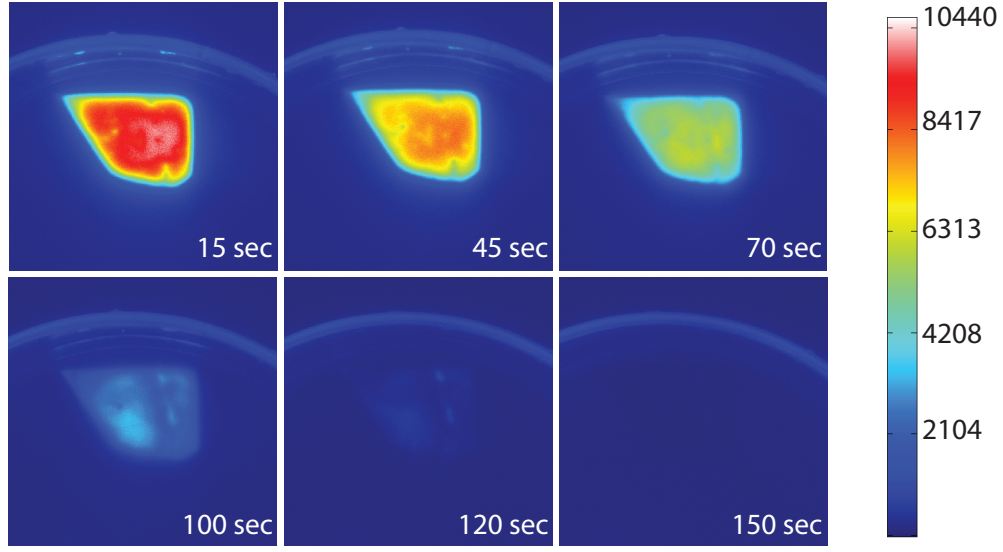


Figure 4.2: Photoluminescence images of the passivation evolution during a diluted alkaline solution etching.

concentration scale as: $I_{PL} \propto \Delta n^2$ and $\Delta n = G\tau_{eff}$ then $\tau_{eff} \propto \sqrt{I_{PL}}$ [Trupke 2005], we can estimate that in less than a minute, the passivation had decayed by about 30%. The complete etching can be observed after 120 s. By assuming a typical 8-nm-thick a-Si:H(*i*) layer, the etch rate is about 4 nm min⁻¹ which may allow a good control of the etch depth. However, we also note that this technique does not etch the a-Si:H(*i*) passivation layer homogeneously. This can be observed by comparing images taken after 15 s and 100 s. Indeed, the area with the best surface passivation observed in the 15 s picture becomes the area with the lowest surface passivation after 100 s of etching. This is likely induced by an inhomogeneous start of the etching over the wafer surface despite the HF dip prior the etching.

4.2.4 Conclusions

We demonstrated here that, in agreement with Greil *et al.*, diluted alkaline solutions can be used to wet chemically etch a-Si:H layers a few nm thick with good accuracy. [Greil 2011] In addition, PL can be used as a reliable way to monitor the progression of the etching in order to stop it at the proper moment. However, as previously mentioned in section 4.1, the a-Si:H(*i*) passivation layer has to be ideally preserved during the etching. Here, it was clearly observed that this technique does not have the required homogeneity—as especially seen after 100 s—to achieve this selective etching. Furthermore this process introduces steps outside the PECVD reactor and therefore additional cleaning steps, which leads to a more complex process flow.

Chapter 4. Patterning amorphous silicon layers by hydrogen plasma and wet chemical etching

For these reasons, this technique was not further investigated and etching by using an entirely dry process in the PECVD reactor was studied as presented in section 4.3.

4.3 Selective etching of doped a-Si:H layers by H₂ plasma etching[†]

4.3.1 Introduction[†]

Hydrogen plasma carried in PECVD reactor is investigated here for a-Si:H film etching. In PECVD-deposited a-Si:H(*i*) films, H₂ plays an important role in the surface passivation. Indeed, to obtain high-quality interface passivation, an atomically sharp a-Si:H/c-Si interface is necessary. [De Wolf 2007a]. Additionally, good passivation is obtained for as-deposited films deposited with high SiH₄ depletion, [Descœudres 2010] yielding film growth close to the amorphous-to-crystalline silicon transition. Further improvements are obtained by interrupting film deposition and inserting short H₂ plasma treatments of the film growth surface. [Descœudres 2011] In this way, the bulk of a-Si:H(*i*) films can come even closer to the amorphous-to-crystalline transition without risking detrimental epitaxial growth. However, we have observed that such treatments may lead to bandgap widening and the presence of nanosized voids in the a-Si:H. Others have confirmed the beneficial electronic effects that such treatments yield, though without an associated increase in material disorder, using their processing conditions. [Mews 2013] The influence of H₂ treatments of the c-Si surface *prior to* a-Si:H deposition has also been studied. Such treatments may introduce severe electronic damage of the c-Si surface, which could not be recovered by subsequent a-Si:H(*i*) passivation. [Granata 2012] [Schüttauf 2011] Hence, some uncertainty regarding the use of H₂ plasma treatments close to the c-Si surface exists in the literature. On the one hand, such treatments may lead to a-Si:H(*i*) material that is better for passivation; on the other hand, c-Si surface defects may be induced, dramatically reducing surface passivation.

The effects of *prolonged* H₂ plasma treatments remain unclear as well. As previously mentioned, a motivation for longer H₂ plasma treatments is to use them for a-Si:H etching (rather than merely for passivation improvement). [Kail 2004] [Van Oort 1987] Indeed, advanced device architectures such as SHJ back-contacted solar cells require doped a-Si:H layer patterning, while preserving pristine a-Si:H(*i*) underlayers for surface passivation and thus the high V_{oc} typical for SHJ devices. [Schwartz 1975] [Mingirulli 2011] [Greil 2011] A clear advantage of dry etching for the fabrication of SHJ back-contacted solar cells is that both etching and deposition can take place in the same system without vacuum break. We report here on the effect of H₂ plasma etching on both the bulk a-Si:H properties and the surface passivation quality of the c-Si underneath. We demonstrate that despite modification of the a-Si:H(*i*) microstructure, good surface passivation can be maintained under the necessary condition that a sufficiently thick (few nanometers) passivation film remain present, shielding the c-Si surface from plasma damage. With this technique, we obtain highly reproducible etch rates. From a device point of view, these findings offer great promise for doped a-Si:H layer patterning while maintaining good surface passivation.

4.3. Selective etching of doped a-Si:H layers by H₂ plasma etching[†]

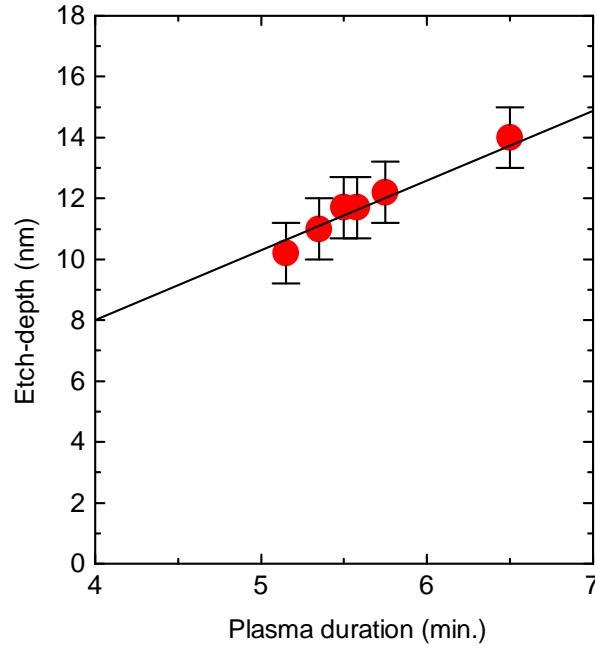


Figure 4.3: Etch depth as a function of the H₂ plasma duration.

4.3.2 Experimental[†]

Figure 4.4 (a) shows the experimental sequence we followed: (1) High-quality float-zone $4 \Omega \cdot \text{cm}$ phosphorus-doped double-side polished $\langle 111 \rangle$ wafers were dipped in diluted hydrofluoric acid solution for 1 min to remove the native oxide. (2) An a-Si:H(*in*) stack was deposited on the back side to provide the most efficient passivation both by lowering the interface-state density and by providing an additional field effect at this surface. PECVD depositions were carried out directly after the HF dip by using an Octopus-I PECVD cluster tool. Deposition details can be found elsewhere. [Descoeudres 2013] (3) An 8-nm-thick a-Si:H(*i*) layer was then deposited on the front side. (4) An 11-nm-thick a-Si:H(*n*) layer was deposited on the front side. The thickness of the layers is representative of those used in real devices. [Descoeudres 2013] (5) H₂ plasma etching of the front a-Si:H(*n*) layer was carried out using the same PECVD reactor with pure hydrogen at 1.5 mBar and a 200 °C substrate temperature; the etching time was varied. The plasma was driven by a radio frequency (13.56 MHz) excitation with $\sim 100 \text{ mW}/\text{cm}^2$ power density. Following steps (3), (4) and (5), the samples were systematically characterized by photoconductance decay (PCD) and spectroscopic ellipsometry (SE) to measure respectively the minority-carrier lifetime (τ_{eff}) and layer thickness.

4.3.3 Effect of hydrogen plasma on surface passivation[†]

With these parameters we obtain a highly reproducible etch rate of $2.3 \pm 0.1 \text{ nm}/\text{min}$ (see Fig. 4.3). We observe an incubation time prior to the start of etching of $\approx 30 \text{ s}$, possibly

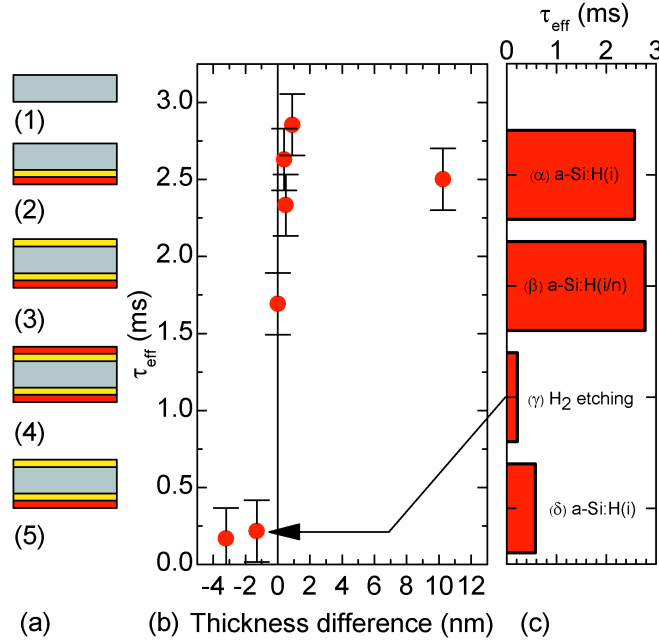


Figure 4.4: (a) Experimental sequence: (1) DSP <111> c-Si wafer after the HF dip, (2) a-Si:H(*in*) stack deposited on the back side, (3) a-Si:H(*i*) deposition on the front side, (4) a-Si:H(*n*) deposition on the front side, (5) H₂ etching on the front side. (b) Minority-carrier lifetime after the H₂ etching at a carrier injection level of $5 \cdot 10^{15} \text{ cm}^{-3}$ vs. the thickness difference between the H₂-etched (after step (5)) and as-deposited a-Si:H(*i*) layer (after step (3)). (c) Minority-carrier lifetime evolution along the entire process for the sample highlighted in (b). Reproduced with permission from [Geissbühler 2013]. Copyright 2013, AIP Publishing LLC.

due to creation of a hydrogen-rich sub-layer at the a-Si:H surface, during which hydrogen diffusion into the film dominates over etching. [Kail 2004] [i Morral 2002] Figure 4.4 (b) shows τ_{eff} measured after etching as a function of the thickness difference between the H₂-etched (after step (5)) and the as-deposited a-Si:H(*i*) buffer layer (after step (3)). Negative values point to partial etching of the underlying a-Si:H(*i*) buffer layer whereas positive values indicate that a-Si:H(*n*) is partially remaining on the a-Si:H(*i*) buffer layer. An abrupt drop in τ_{eff} is observed when the a-Si:H(*i*) layer starts to be etched (i.e. thickness difference < 0). From this, we conclude that it may be possible to etch the doped layer away fully, which opens possibilities for film patterning, but seemingly we need to preserve the nominal buffer layer thickness to guarantee high-quality passivation. To further investigate the effect of reduced a-Si:H(*i*) buffer layer thickness on the passivation quality, a-Si:H(*i*) re-depositions were carried out following over-etching of the a-Si:H(*n*) layer, to restore the initial buffer layer thickness. Figure 4.4 (c) shows the evolution of τ_{eff} for the sample highlighted in Fig. 4.4 (b), following the different process steps including re-deposition. Beginning with the sample having only an a-Si:H(*i*) layer with typical buffer layer thickness (α), a τ_{eff} increase is observed with a-Si:H(*n*) deposition, most likely induced by additional field-effect passivation (β). Next, τ_{eff} drops severely from 2.8 ms to 200 μs due to H₂ etching (γ). This drop is not recovered by

re-deposition of a-Si:H(*i*) (δ). From this, we conclude that the passivation losses are linked to defect formation (either at the c-Si surface, or in the remaining film) rather than merely from the reduction of the passivation layer thickness. To decouple the contribution of c-Si surface defects from a-Si:H modification, etching of the *full* a-Si:H(*in*) stack was carried out. In this case, the plasma duration was set to precisely etch the complete a-Si:H(*in*) stack without over-etching, thus keeping the c-Si wafer pristine. To prevent native oxide formation following the etching, subsequent re-deposition of an a-Si:H(*i*) passivation layer was carried out without vacuum break. In this case, τ_{eff} decreased from 1.3 ms for the a-Si:H(*in*) precursor to 290 μs despite the re-deposition of a buffer layer (data not shown).

4.3.4 High resolution transmission electron microscopy investigation of the a-Si:H/c-Si interface[†]

High-resolution transmission electron microscopy (HR-TEM, Philips CM300 UT) was used to inspect the a-Si:H/c-Si interface following the described experiments. Cross-section samples were prepared using mechanical polishing (Allied High Tech Multiprep) followed by low-energy Ar ion milling. Figure 4.5 (a) shows a HR-TEM image of the c-Si surface with an as-deposited a-Si:H(*in*) stack. We observe an atomically sharp a-Si:H/c-Si transition, as is required to obtain high-quality surface passivation. [De Wolf 2007a] The darker area at the interface may be due to image delocalization or slight lattice imperfections in the first few nanometers of the substrate. A c-Si surface roughness lower than 2 nm is observed, which may indicate imperfect wafer mirror polishing or HF-dip-related wafer etching. Figure 4.5 (b) shows the sample described earlier for which the entire a-Si:H(*in*) stack was etched and followed by a subsequent a-Si:H(*i*) re-deposition. We observe clearly an increase in the c-Si surface roughness to ≈ 5 nm and the appearance of defects in the near-surface crystalline structure (indicated by white arrows). Indeed, with Fourier filtering, defects and distortions are observed in the c-Si lattice as deep as 10–15 nm beneath the wafer surface (see insets). Figure 4.5 (c) shows the a-Si:H/c-Si interface for a sample for which only the a-Si:H(*n*) layer was etched while preserving the full a-Si:H(*i*) buffer layer. This is the sample with a zero thickness difference shown in Fig. 4.4 (b). Contrary to the case of full-stack etching, the initial low c-Si surface roughness and low defect density in the crystalline structure are preserved. This set of images confirms that severe microstructural damage of the c-Si surface occurs when the H₂ plasma starts to interact with this interface. [Shinohara 2003] This effect is avoided by leaving the full a-Si:H(*i*) buffer layer un-etched. According to the steep drop in τ_{eff} observed in Fig. 4.4 (b), about 8 nm of a-Si:H(*i*) is required to provide sufficient shielding of the c-Si surface to avoid irreversible sub-surface defect creation. Despite this, some minor defects seem to be present at the interface in Fig. 4.5 (c); hence it may be asked to what extent the microstructure of the remaining a-Si:H(*i*) buffer layer is modified during etching of the a-Si:H(*n*) overlayer.

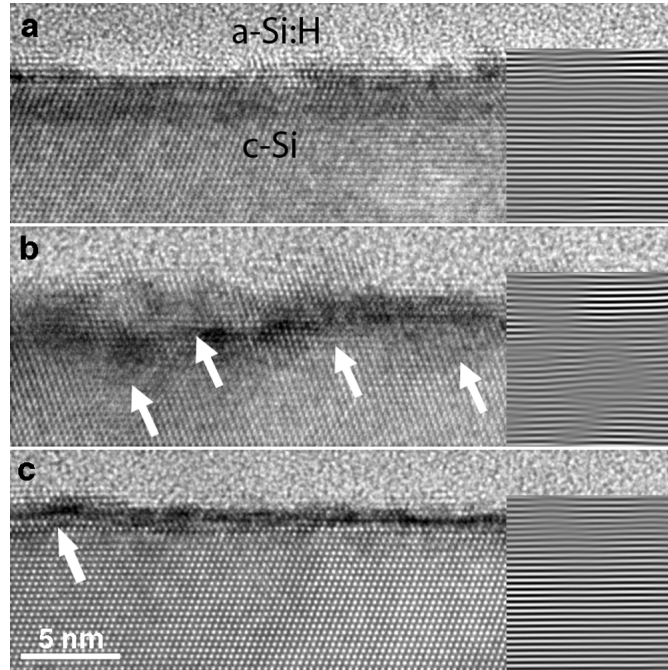


Figure 4.5: HR-TEM micrographs of the c-Si/a-Si:H interface for (a) an as-deposited a-Si:H(*in*) stack, (b) a completely etched a-Si:H(*in*) stack followed by a re-deposited a-Si:H(*i*) layer, and (c) an a-Si:H(*in*) stack after selective etching of the a-Si:H(*n*) layer. The right side of each image is treated with a Fourier filtering, highlighting the (110) crystalline plane. Reproduced with permission from [Geissbühler 2013]. Copyright 2013, AIP Publishing LLC.

4.3.5 Study of a-Si:H film microstructure by attenuated total reflectance Fourier transform infrared spectroscopy[†]

To investigate how the remaining a-Si:H(*i*) buffer layer evolves during H₂ plasma etching, attenuated total reflectance (ATR) Fourier transform infrared (FTIR) and SE were used to probe the a-Si:H(*i*) microstructural modifications. The a-Si:H ATR-FTIR absorbance spectra are largely governed by the silicon-hydrogen bonding environment. Information about the precise Si-H bonding environment can be deduced from the high and low stretching mode (HSM, LSM) absorption peaks at 2070–2100 cm⁻¹ and 1980–2010 cm⁻¹, respectively. [Knights 1979] The LSM is assigned to the monohydride bonding configuration, whereas the HSM is a signature of (hydrogenated) nanometric voids in the bulk material. [Smets 2003] Four c-Si prisms were processed separately and characterized with ATR-FTIR and SE to assess the a-Si:H material properties after each process step. [Demaurex 2012] The deposition parameters were identical to those in the experiments described earlier in this chapter. The a-Si:H(*n*) layer was replaced by an a-Si:H(*i*) layer (labeled i2) to avoid free-carrier absorption artifacts during FTIR characterization. We label the original a-Si:H(*i*) buffer layer as i1. Sample (1) is a 15-nm-thick as-deposited a-Si:H(*i*) reference layer. Sample (3) was prepared as sample (1), and immediately followed by a H₂ etching step of the duration needed (3.48 min here) to completely remove the i2 layer without etching any i1 material. Sample (4) features an

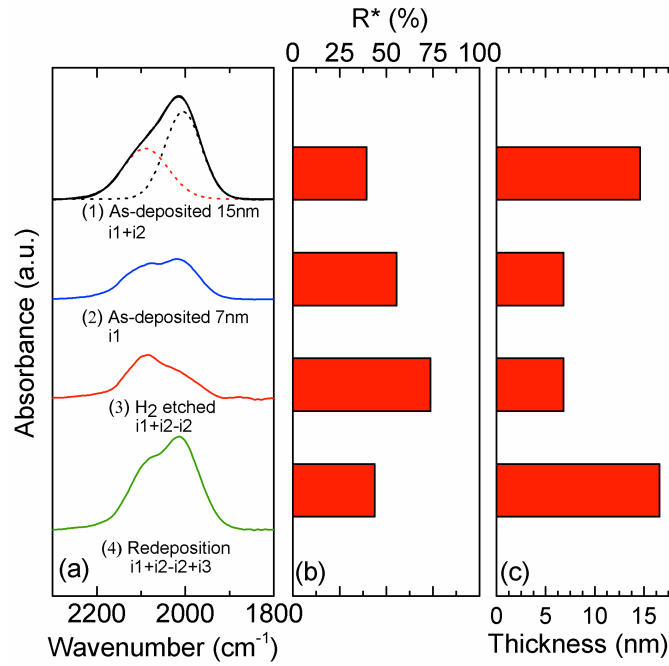


Figure 4.6: (a) ATR-FTIR spectra for (1) 15-nm-thick as-deposited a-Si:H(*i*) (i1 + i2), (2) 7-nm-thick as-deposited a-Si:H(*i*) (i1), (3) H₂-etched a-Si:H(*i*) (i1 + i2 - i2), and (4) 15-nm-thick H₂-etched and re-deposited a-Si:H(*i*) (i1 + i2 - i2 + i3). The deconvolution into the HSM/LSM peaks is shown for sample (1). (b) Microstructure factor extracted from the LSM and HSM deconvolutions. (c) a-Si:H(*i*) layer thickness measured by SE. Reproduced with permission from [Geissbühler 2013]. Copyright 2013, AIP Publishing LLC.

additional a-Si:H(*i*) re-deposition step (labeled i3) after H₂ etching to restore the initial 15 nm thickness. For as-deposited a-Si:H, the Si-H bonding environment is known to vary across the thickness of thin films. [Fujiwara 2005] Therefore, ATR-FTIR spectrum comparisons must be made between samples of similar thickness. For this purpose, sample (2) contains 7 nm of as-deposited a-Si:H(*i*) to provide a reliable comparison with sample (3). Sample thicknesses measured by SE are displayed in Fig. 4.6 (c). Figure 4.6 (a) shows the ATR-FTIR absorbance spectra of the four samples. The HSM/LSM peak deconvolution is displayed for sample (1). A usual figure of merit in infrared spectroscopy of a-Si:H is the microstructure factor R^* , defined as the ratio of the integrated HSM and LSM peaks after deconvolution. [Müllerová 2008] Figure 4.6 (b) shows R^* for the four samples. By comparing the spectra of samples (2) and (3), we note a clear increase of the HSM peak (increase of R^*) after H₂ etching, which points at more void-rich material. A similar comparison can be made between samples (1) and (4) though the re-deposition of the as-deposited i3 layer reduces the magnitude of this effect. A clear increase of the HSM can be seen for sample (4), indicating a higher void-related hydrogen content in the layer. A bandgap widening observed between sample (1) and (4) from 1.86 eV to 1.94 eV confirms such hydrogen incorporation.[Descocudres 2011] [Mews 2013] [Schulze 2011]

4.3.6 Study of hydrogen incorporation in a-Si:H films by H₂ and D₂ thermal desorption spectroscopy[†]

To study the source of hydrogen present in the films after etching, H₂/D₂ etching experiments followed by thermal desorption spectroscopy (TDS) were done. H₂/D₂ effusion rate profiles are characterized by high and low temperature peaks, qualitatively corresponding respectively to monohydride and dihydride bond breaking. Further details can be found elsewhere. [De Wolf 2007b] In addition, the TDS quadrupole mass spectrometer allows for discrimination between H₂ and D₂ species. [Beyer 1991] Therefore, if etching is carried out with D₂ instead of H₂, the HD or D₂ effusion rate profiles will be a signature of atoms incorporated into the film during etching. Several c-Si samples were prepared with on both sides films featuring a sequence consisting of six deposition/etching steps as shown in Fig. 4.7 (a). Depositions were carried out with SiH₄ diluted in H₂ and etching was done either with H₂ or with D₂ using parameters similar to those described earlier in this chapter. The deposition time was kept constant whereas the duration of the H₂/D₂ etching step varied from 0 to 40 s. Therefore, the cumulative duration of the plasma etching varied from 0 min. to 4 min. The samples were characterized by SE and TDS. Figure 4.7 (b) shows the layer thickness measured by SE. A 2.0 nm/min H₂ etch rate was deduced by linear fitting. The difference between this value and the 2.3 nm/min etch rate previously observed we explain by the etching incubation time at the beginning of each etching step. A 4.2 nm/min D₂ etch rate was measured. Given the H₂/D₂ mass ratio, this increased etch-rate ratio suggests a physical sputtering mechanism enhanced by the higher momentum of D atoms impinging on the surface. These results confirm earlier findings. [Iwakuro 1996] Figure 4.7 (c) shows the optical bandgap as a function of the duration of the plasma etching. As mentioned earlier, H₂ etching induces a bandgap widening; apparently, D₂ etching enhances this widening. Figure 4.7 (d) shows the H₂, HD, and D₂ effusion rate profiles of unetched, H₂-etched, and D₂-etched samples with identical film thickness. By comparing the pristine sample with its H₂-etched counterpart, we observe additional H₂ incorporation induced by H₂ etching. This explains the optical bandgap widening. Interestingly, the H₂ effusion rate dramatically drops for the D₂-etched sample, but the HD and D₂ effusion rates indicate that a significant quantity of deuterium is incorporated into the a-Si:H, both as mono- and dihydride. Therefore, this experiment demonstrates that a significant exchange of hydrogen between film and etch plasma occurs during etching, pointing also at film mixing during such a procedure.

4.3.7 Conclusions[†]

Our findings are thus as follows: Hydrogen plasmas can be used to accurately etch a-Si:H films for patterning purposes. [Kail 2004] To guarantee an electronically pristine c-Si surface, at least a few nanometers of a-Si:H should remain on the surface to avoid irreversible damage. [Granata 2012] The remaining film is subject to significant microstructural changes, where exchanges of hydrogen may take place and the film bandgap widens due to hydrogen incorporation. [Mews 2013] These changes have no detrimental effect on the interface passivation

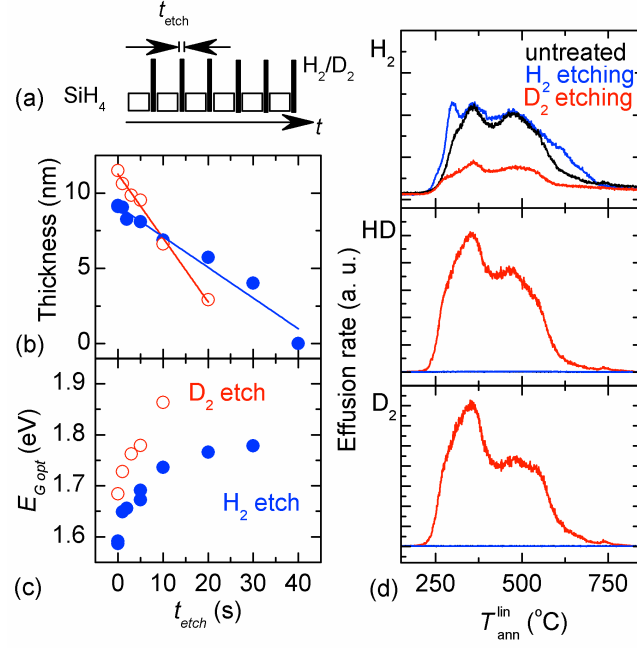


Figure 4.7: (a) Deposition/etching sequence. (b) Thickness measured by SE as a function of the duration of each plasma etching step. (c) Optical bandgap as a function of the duration of each plasma etching step. (d) H₂, HD, and D₂ effusion rate profiles as a function of sample temperature. H₂ etched samples were previously presented in [Descœudres 2011]. Reproduced with permission from [Geissbühler 2013]. Copyright 2013, AIP Publishing LLC.

quality. Since the minimum layer thickness needed to provide an efficient shielding of the c-Si surface from the H₂ etch plasma corresponds precisely with the a-Si:H(*i*) buffer layer thickness used for SHJ solar cells, such etching opens possibilities for doped a-Si:H layer patterning and could be used, e.g., for the development of advanced device architectures such as IBC-SHJ solar cells.

4.4 Influence of H₂ plasma etching on SHJ device performance

4.4.1 Introduction

As presented in section 4.3, H₂ plasma etching in a PECVD reactor demonstrates its ability to achieve selective etching of the doped a-Si:H layer while preserving good *electronic properties* allowing good surface passivation. However, it was as well shown that this process strongly impacts the bandgap and the microstructure of the remaining a-Si:H(*i*) layer. Therefore, for the integration of this process in advanced SHJ structures, it raises the question of how the latter modifications influence the *transport* properties of the charge carriers through the a-Si:H(*i*) film. Moreover, unlike the mirror-polished surfaces of the samples in the previous study of H₂ plasma etching, the surfaces of SHJ solar cells are textured with random pyramids. Therefore,

Chapter 4. Patterning amorphous silicon layers by hydrogen plasma and wet chemical etching

it has to be demonstrated that H_2 plasma etching can also work on such textured surfaces.

In this section, we present first a study of how the doping polarity of an a-Si:H(*in*) stack can be converted into an a-Si:H(*ip*) by selective H_2 etching of the a-Si:H(*n*) followed by an a-Si:H(*p*) deposition. Finally, an investigation of H_2 plasma etching on *textured* wafers is made.

4.4.2 Study of charge-carrier transport in a-Si:H(*i*) layers exposed to H_2 plasma etching

Figure 4.8 (a) shows the process sequence we used in this study to convert the polarity of a symmetric a-Si:H(*in*)/c-Si/a-Si:H(*in*) structure (denoted in/in here) into an a-Si:H(*in*)/c-Si/a-Si:H(*ip*) cell precursor (denoted in/ip): (1) The a-Si:H(*in*) stacks were deposited on double-side polished <111> wafers by using the same procedure described in section 4.3. (2) H_2 plasma etching was carried out in order to achieve a *selective* removal of the front a-Si:H(*n*) layer. Spectroscopic ellipsometry confirmed that the a-Si:H(*n*) layer was entirely removed with an a-Si:H(*i*) thickness variation (i.e. between before the a-Si:H(*n*) deposition and after the H_2 etching) of less than 0.5 nm. At this stage, a good τ_{eff} of 2.3 ms at an injection level of $5 \cdot 10^{15} \text{ cm}^{-3}$ was measured, indicating no significant damage to the surface passivation (iV_{oc} of 713 mV). (3) Finally, an a-Si:H(*p*) layer was deposited and τ_{eff} and iV_{oc} were measured at 1.9 ms and 720 mV, respectively. As a reference cell, an in/ip precursor was deposited. However a modest τ_{eff} of 680 μs leading to an iV_{oc} of 690 mV was measured on this cell precursor. Finally, both precursors were converted in finished cells. It has to be mentioned here that none of the PECVD recipes were optimized for mirror-polished wafers. The deposition time was reduced by a ratio of 1.7 in order to obtain films with thicknesses similar to those on textured pyramids. For the polarity-converted wafer, the a-Si:H(*p*) layer was accidentally deposited too thick.

Figure. 4.8 (b) shows the light J - V curves of both the polarity-converted cell and the reference cell. Accordingly to its low iV_{oc} , the reference cell shows as well a low V_{oc} of 671 mV. The low fill factor (FF) of 64.6% may be explained by un-optimized PECVD and PVD processes for mirror-polished wafers. In the polarity-converted case, lower V_{oc} and FF compared to the reference were recorded and can be explained as follows: i) First, too thick a-Si:H layers may lead to S-shaped J - V curves. ii) The prolonged air exposure between the H_2 etching and the a-Si:H(*p*) may lead to the formation of a native oxide layer which may also introduce an S-shaped behavior. [Seif 2014] iii) The bandgap widening of the a-Si:H(*i*) film observed in section 4.3.5 leads to a bandgap close to 2 eV after the H_2 etching. As reported in literature, this bandgap widening induces an increased valence band offset which in turn may induce a hole collection issue resulting in an S-shape. [Schulze 2011] [Seif 2014] iv) Finally, the increased microstructure factor of an a-Si:H(*i*) layer exposed to H_2 plasma etching—which reveals a more void-rich material—may suggest that such a layer may be more sensitive to sputtering damages which can partially explain the low V_{oc} obtained in this cell. [Demaurex 2012]

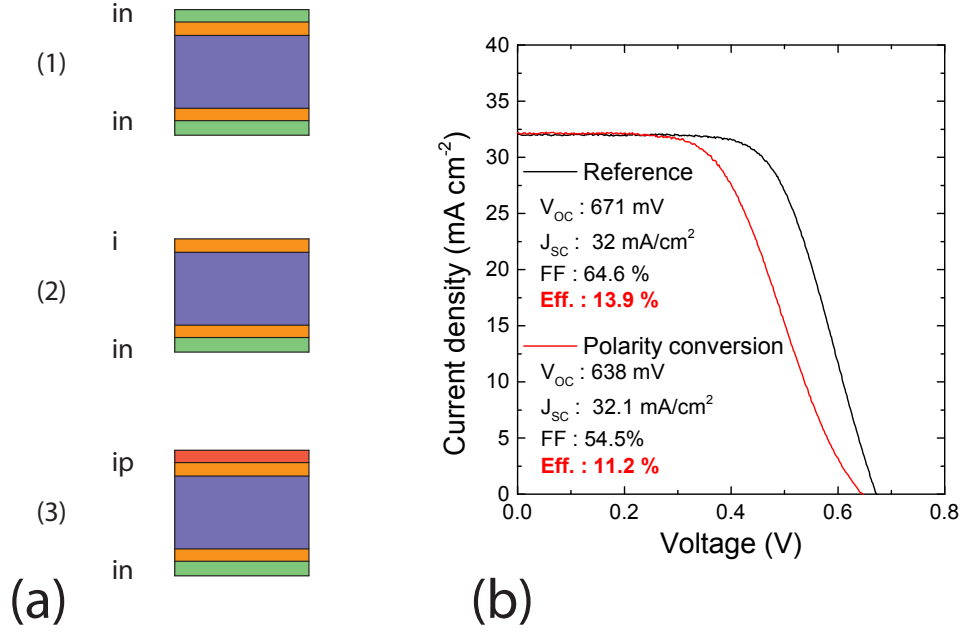


Figure 4.8: (a) Process sequence used in this study : (1) in/in precursor (2) H₂ etching of the front a-Si:H(*n*) layer (3) redepositon of a front a-Si:H(*p*) layer. (b) Light *J-V* curves of a cell with the converted polarity and a reference cell.

4.4.3 Doped a-Si:H layer patterning by H₂ plasma etching on wafers with random pyramids texture

To investigate whether H₂ plasma etching can be used on random pyramids textured wafers, an experiment with the same procedure as described in Fig. 4.4 (a) of section 4.3.3 was made on random pyramids textured wafers. Figure 4.9 shows τ_{eff} at an injection level of $5 \cdot 10^{15} \text{ cm}^{-3}$ as function of the H₂ plasma etching time. Similarly as Fig. 4.4 (b), a clear threshold in τ_{eff} is observed when etching exceeds 9 min. Spectroscopic ellipsometry performed on a co-deposited glass witness indicates that this etching time corresponds exactly to the entire removal of the a-Si:H(*n*) film. We can therefore conclude that H₂ plasma etching behaves similarly on random pyramids textured or mirror-polished wafers.

4.4.4 Conclusion

Our conclusions on the integration of H₂ plasma etching in the fabrication of advanced SHJ devices are thus as follows: The complete removal of a doped a-Si:H layer and subsequent re-deposition of the opposite doping polarity demonstrates the possibility to use this process to realize complex a-Si:H structures suitable for IBC-SHJ devices. However, a lower *FF* was observed for the polarity-converted cell which may point out the presence, in particular, of a

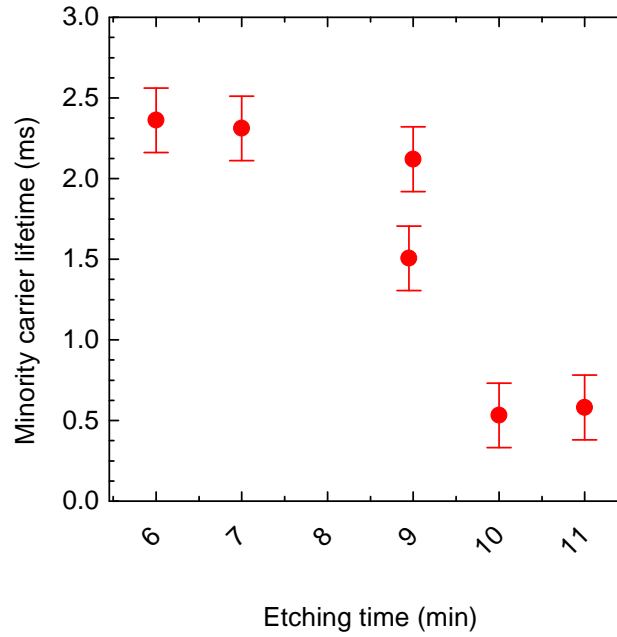


Figure 4.9: Minority-carrier lifetime at an excess carrier density of $5 \times 10^{15} \text{ cm}^{-3}$ of passivated textured wafers after H_2 plasma etching as a function of the H_2 plasma etching duration.

hole collection issue likely induced by an increased valence band offset. Therefore, it may be more efficient to deposit an a-Si:H(*ip*) stack and then to carry out the H_2 etching followed by a deposition of a-Si:H(*n*) to avoid this hole collection issue. Furthermore, we demonstrated here, that H_2 plasma etching can be used indifferently on mirror-polished or on random pyramids textured wafers.

4.5 General conclusions on a-Si:H film patterning

Two techniques based on etching to pattern of a-Si:H layers were investigated. First, we demonstrated that, with wet chemical etching using a highly diluted alkaline solution, etch rates of a few nm per min can be achieved. PL can be used to monitor in-situ the progression of the etching. However, insufficient homogeneity was clearly identified which excludes the use of this process in a selective etching of the doped layer over the a-Si:H(*i*) passivation film. Nevertheless, this does not exclude the possibility to remove the entire a-Si:H stack and subsequently redeposit the a-Si:H(*i*) layer. [Greil 2011] In a different approach, H_2 plasma etching in a PECVD reactor was found to offer nanometric resolution in the control of the etch depth. A key result is that selective etching of doped layers can be achieved since the a-Si:H(*i*) layer underneath offers sufficient protection of the c-Si wafer surface against the plasma damages. Furthermore, from a process point of view, H_2 plasma is preferred to wet chemical etching since this process can be performed in a single PECVD reactor. We also demonstrated that H_2 plasma etching can be used in SHJ devices manufacturing with

4.5. General conclusions on a-Si:H film patterning

random pyramids textured surfaces even though lower electrical performances were obtained yet. These results demonstrate the potential of the hydrogen plasma etching technique for the fabrication of advanced-SHJ solar cells such as IBC-SHJ. Indeed, for this device architecture, an etching/deposition sequence can significantly simplify the process-sequence by suppressing a vacuum-break and the alignment of a second shadow mask. [Scherff 2011] In this respect, further investigations are required in order to verify if layers exposed to such treatments can be employed in SHJ devices.

5 Localized front contact silicon hetero-junction solar cells

Summary

A new SHJ architecture device based on localized front contacts was investigated in this chapter with the aim to decouple the optical and electrical properties of the window films. In the first device generation based on a FHC configuration and where only the front-TCO was patterned, we demonstrated that lowering the contact coverage leads to both a J_{sc} decay induced by electrical shading effect and to a FF drop linked to an increased series resistance. The FF loss was found to be independent of the finger pitch which points out that the a-Si:H(p)/TCO contact is the main limiting factor. Hence, high contact coverage of 75% were required to maintain equivalent device performance as the standard SHJ reference with efficiencies above 20% . In the second device generation, the front doped a-Si:H layer was patterned and both FHC and RHC configurations were investigated. We showed that the direct contact with the a-Si:H(i) and the front TCO must be avoided requiring therefore a second patterning step for the front-TCO. With this latter design, we showed the better suitability of the RHC configuration as the device benefits of an improved lateral transport in the c-Si bulk and of the lower specific contact resistivity of the a-Si:H(n)/TCO interface. However, the relatively low contact coverage required for achieving significant improvements in the light management induces important losses in the electrical performances. As a result, FF of 70% leading to an efficiency of 17.2% were recorded for such SHJ solar cell structure where only 50% of the front-surface is covered by the a-Si:H(n) film. Finally, based on numerical simulations, we discussed the requirement for the a-Si:H(n)/TCO contact needed in order to manufacture a simplified device structure based on a single patterning step.

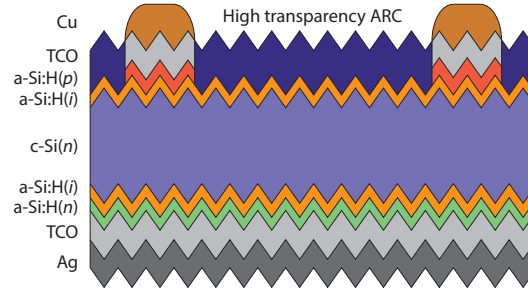


Figure 5.1: Schematic cross-section of a SHJ solar cell with the LEP architecture in the FHC configuration with both the front doped a-Si:H and front TCO layers patterned.

5.1 Introduction

In this chapter, a new SHJ device architecture based on a localized front contact—denoted as the localized extraction and passivated SHJ solar cell (LEP)—is investigated. This chapter is structured as follows: First, the principle of the LEP device is defined and motivated. Then, a light-beam-induced current (LBIC) tool specifically designed and built to characterize these cells is presented. To investigate the impact of a restricted contact area, a study is made on the first generation of LEP devices having exclusively a patterned front TCO and a front hole-collector (FHC) configuration. The rear hole-collector (RHC) configuration is then considered and investigated on standard SHJ cells. Next, the second generation of LEP devices featuring both the FHC and RHC configurations as well as a patterned front doped a-Si:H layer is discussed. Finally, more advanced devices based on the LEP architecture are proposed.¹ [Ballif 2015]

The LEP architecture for SHJ solar cells has been protected under patent number *US 20150144184*.

5.1.1 Motivations

The concept behind the LEP cell architecture, is the decoupling of the electrical and optical properties of the window layers² by forming two parts respectively optimized for each purpose. As reported by Holman *et al.*, a $2.1 \text{ mA cm}^{-2} J_{sc}$ loss is experienced at the front side of SHJ solar cells. [Holman 2012] More precisely, these losses are induced by the relatively narrow a-Si:H bandgap of $\approx 1.6\text{--}1.8 \text{ eV}$ absorbing light with wavelengths below 600 nm. Although, approximately 30% of the charge carriers generated within the front a-Si:H(*i*) layer can be collected, the entire amount generated in the p-doped layer is lost due to its high defect density. [Holman 2012] [Tanaka 1992] In addition to the losses due to the a-Si:H layers, the front TCO leads as well to parasitic light absorption either due to bandgap absorption or

¹The results presented here were obtained with the help of N. Badel, A. Tomasi, B. Paviet-Salmon, L. Barraud, A. Descoedres, M. Despeisse. Contributions are gratefully acknowledged.

²i.e. a-Si:H(*ip*) and TCO in a SHJ solar cell with a front hole-collector.

by FCA. [Holman 2012] [Holman 2013] Hence, by dividing the SHJ front side into two parts respectively optimized for having either the best electrical or the best optical properties, these parasitic losses can be mitigated. An example of such LEP structure is shown in Fig. 5.1: First, in the non-contacted part, the front TCO can be replaced by a highly transparent dielectric such as silicon nitride to form the front ARC. Next, as no extraction happens in this area, the a-Si:H(*p*) layer can be entirely suppressed. Finally, the a-Si:H(*i*) layer may be made thinner as the silicon nitride ARC—possibly deposited by PECVD—can act as a hydrogen reservoir helping to passivate the dangling bonds. Ideally, the a-Si:H(*i*) can be even completely replaced by other transparent materials such as SiO₂ or Al₂O₃ to ensure surface passivation. [Kerr 2001] [Hoex 2008] Hence, in such case, the LEP-SHJ device will be a local passivating contacts solar cell with an entirely low temperature process-flow.

For the contacted part, layers can thus be optimized regardless of their optical properties in order to provide the best selective contact with the c-Si wafer. Therefore, arbitrary thick a-Si:H(*i*) and a-Si:H(*p*) films can be used as well as other materials such as μ c-Si:H. [Seif 2015a] [Watahiki 2015] Furthermore, the front TCO required for efficiently contacting the a-Si:H(*ip*) stack can be deposited with complete freedom in its electrical properties without risking detrimental FCA losses or even completely removed to form a direct a-Si:H(*p*)/metal contact. [Bivour 2012]

5.1.2 Localized contacts in SHJ devices

Point contacts were studied by others for the rear side of SHJ or hybrid (SHJ with diffused-junction or PERC-like rear-side) solar cells. [Bivour 2012] [Bivour 2011] [Colina 2015] [Morales-Vilches 2013] In the SHJ case, De Vecchi *et al.* used an insulating a-Si:H(*i*)/SiO₂ stack at the rear side locally opened by screen-printing masking and wet chemical etching. [Vecchi 2012] Then, either an a-Si:H(*in*) electron collector or an a-Si:H(*ip*) hole collector was deposited with a contact coverage ranging between 16% and 2% . They observed that with a very restrained contact area for the hole collector, a significant J_{sc} loss is experienced as holes (minority-carrier) recombine before being collected. When this contact geometry is applied to the electron collector, a significant FF loss is seen due to an increased series resistance. The J_{sc} was however found to be enhanced while reducing the area coverage of the electron contact as the a-Si:H(*i*)/ SiO₂ stack increases the internal light reflection at the back side. [Vecchi 2012] For the same optical motivation, Qiu *et al.* investigated a localized hetero-contact at the rear side of a hybrid solar cell. [Qiu 2015] Finally, localized contacts were as well used as the front hole collector in SHJ devices to probe the contribution of the inversion layer to the lateral transport. However, Filipič *et al.* found that this channel does not have a sufficiently low sheet resistance to replace the front TCO. [Filipic 2013]

Another kind of SHJ device using localized contacts is the IBC-SHJ solar cell. [Stangl 2008] [Stangl 2009] [Desrues 2011] [Haschke 2012] [Mingirulli 2011]. In recent reported devices, high FF and J_{sc} leading to outstanding cell efficiencies were demonstrated despite a re-

duced contact coverage increasing the contact resistance. [Tomasi 2014] [Watahiki 2015] [Masuko 2014] In particular, Paviet-Salomon *et al.* demonstrated that when surfaces are sufficiently well passivated, the loss attributed to electrical shading counts for less than 0.5 mA cm^{-2} for a design with a pitch of 2.6 mm. [Paviet-Salomon 2015] Hence, these last examples demonstrate the feasibility of high-efficiency SHJ devices while reducing the contact coverage.

5.2 Light-beam-induced current measurement setup

5.2.1 Introduction

LBIC is a commonly used method to directly probe the local response of solar cells. In this technique, a light beam is focused on the solar cell with a spot diameter ranging from a few μm up to $100 \mu\text{m}$. The beam is then scanned across the device surface while the generated current is recorded. [Marek 1984] The scanning can be realized by moving the cell or the beam with linear actuators or by deflecting it with galvano-mirrors. [Cossutta 2014] In order to suppress the contribution of ambient or bias light, lock-in detection is usually employed. Depending on its stability, the beam may be split in order to record its real intensity on a calibrated reference photodiode.

One of the key advantages of LBIC is the possibility to characterize a solar cell in a non-destructive way under real operating conditions (temperature, light intensity, electrical polarization, etc.). [Carstensen 2003] Furthermore, as this technique is based on a light beam probe, investigations on light management in solar cells can also be achieved. [Woehl 2008]

In particular, LBIC can be used for some specific purposes: For instance, LBIC can be employed for mapping the local diffusion length of minority carriers by using a multi-wavelength light beam. [Warta 1998] The local reflectance and local IQE can as well be accessed by adding an integrating sphere above the solar cell recording the amount of reflected light. [Moralejo 2010] [Semilab 2015] For cell characterization in production lines, the LBIC technique can be adapted and the scanning time can be reduced down to 3 s for a 6 inches solar cell. [Acciarri 2002] Finally, LBIC can be applied to various types of solar cells such as CIGS or thin-film silicon modules. [Cossutta 2014] [Vorasayan 2009] [Hänni 2014]

5.2.2 Experimental setup

Figure 5.2 shows the block diagram and the mechanical design of the LBIC system designed during this thesis. The cell is placed on a Peltier temperature-regulated vacuum chuck [see Fig. 2.4(c)] and contacted with a four-probe configuration to a home-built sourcemeter (see appendix A) acting as a trans-impedance amplifier. The cell is placed at a constant voltage and the total current generated by the cell is measured (including both the bias light and the light beam). A 14-bit resolution digital-to-analog (DAC) and analog-to-digital (ADC) converter (DAQ-6008, National Instruments) is used as an interface between the sourcemeter and the

5.2. Light-beam-induced current measurement setup

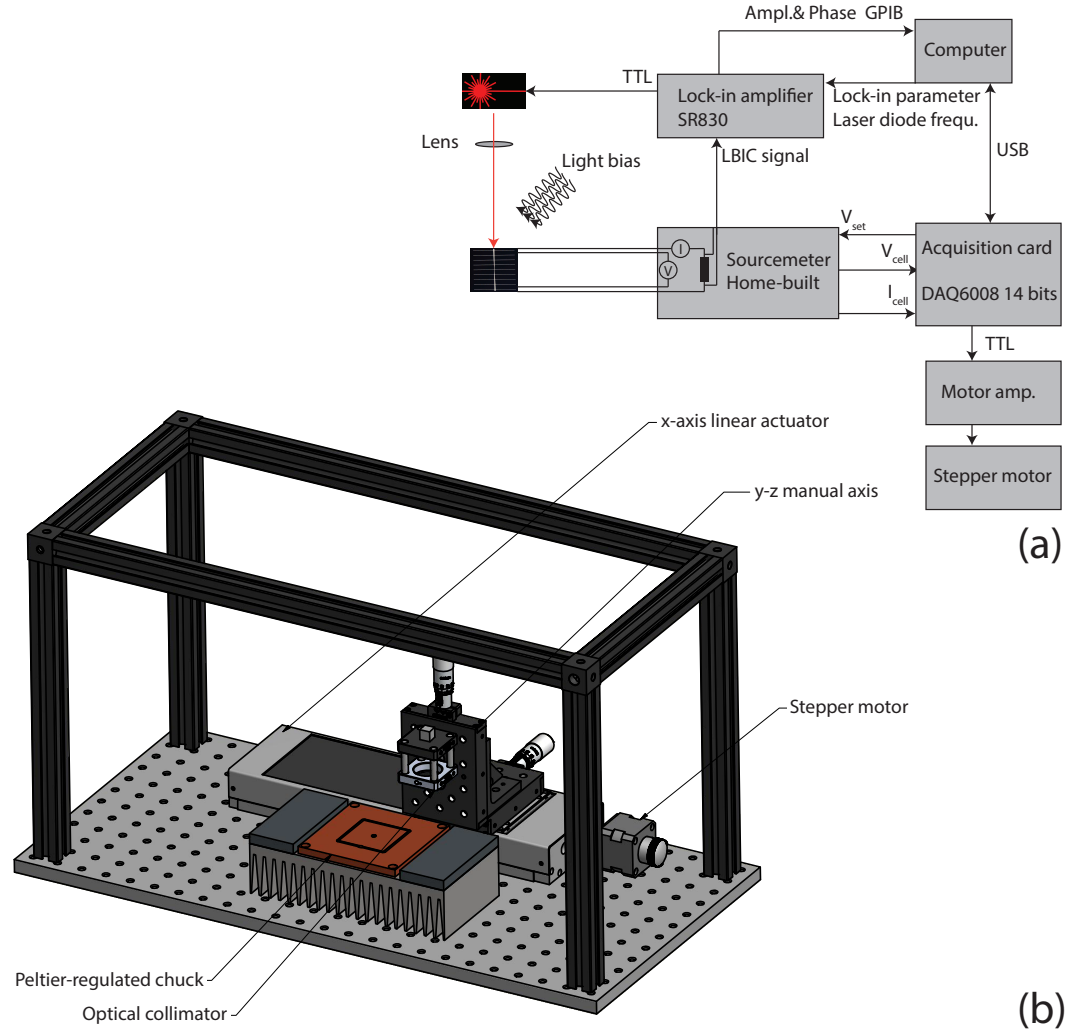


Figure 5.2: (a) Block diagram of the different LBIC components (b) Mechanical design of the LBIC setup.

control computer to provide the cell voltage setpoint and to measure the exact cell voltage and current. The internal load inside the sourcemeter is connected to a lock-in amplifier (SR-830, Stanford Research Systems) for the detection of the beam probe. The lock-in amplifier is connected with a GPIB bus to the control computer for transferring both the amplitude and the phase of the LBIC signal and to set the internal lock-in parameter and the excitation frequency. A TTL signal is generated by the lock-in with the excitation frequency and connected to a solid-state laser module ($\lambda=650$ nm) for the light modulation. Four TTL outputs of the DAQ-6008 are used to control the phase sequence of the stepper motor used for the actuation via a current amplifier. This system features only one motorized axis as one dimensional scans are sufficient for the LEP device characterization. The stepper motor is coupled to a ball screw linear actuator with a step resolution of $\approx 8 \mu\text{m}$ and a total stroke of 200 mm making this system capable of scanning entirely a 6 inch solar cell or a mini-module. The laser diode

beam is collimated by using an aperture and a lens with a 100-mm focal length. Two manual actuators with micrometric screws allow for accurate positioning of the spot beam on the y-axis and for adjustment the focus on the z-axis. We note that due to good stability of the laser diode, no reference cell is used here thus avoiding the use of a second lock-in amplifier. In addition, a sharp metal needle can be mounted onto the moving optics in order to probe the local voltage on the front TCO as shown in Figs. 3.8 and 5.11. [van der Heide 2002]

5.3 LEP devices with a patterned front TCO

5.3.1 Introduction

This section studies the collection of the minority carriers (holes) in SHJ solar cells with a localized front contact and the impact of the contact geometry on the device performance. For this purpose, a first generation LEP device is realized by exclusively patterning the front TCO to reduce the contact coverage. Several designs including different finger pitches and different contact coverage were investigated.

5.3.2 Experimental

The first generation of LEP devices was processed as follows: First, a cell precursor with the intrinsic and doped a-Si:H layers is contacted with ITO as the front TCO and with an ITO/Ag stack for the rear contact [Fig. 5.3(a)]. All layers are deposited on the entire wafer surface. Next, photolithography used to pattern the metallic front grid. The front grid is realized by electrodeposition of a Ni-Cu stack [see chapter 3] followed by photoresist removal made with acetone and isopropanol [Fig. 5.3 (b) and (c)]. Four cells are defined per wafer with finger pitches of 2000, 1000, 500 and 250 μm . A second photolithography is then made for the front-TCO patterning. The design of the photolithography mask used for this purpose corresponds to an opening of 25% of the finger pitch. In order to vary the opening size while using only one photolithography mask, multiple exposures with intermediate shifts of the mask are done. Hence, by using this technique, the contact coverage can be varied from 75% (single exposure) to $\approx 5\%$ (i.e. all the TCO between the fingers is removed). The TCO is etched by using either HF or a HCl FeCl₃ mixture [Fig. 5.3 (e)]. [Kuo 2004] The front TCO of the 2000- μm finger pitch cell is always kept un-etched in order to have one reference cell on each wafer. Before removing the second photoresist by acetone and isopropanol, a self-aligned deposition of an alternative non-conductive ARC can be deposited. Thermal evaporation of ZnS/MgF₂ or low-temperature PECVD silicon nitride can be used for instance for this purpose. [Zhao 1998] Photolithography mask layouts are shown in appendix B

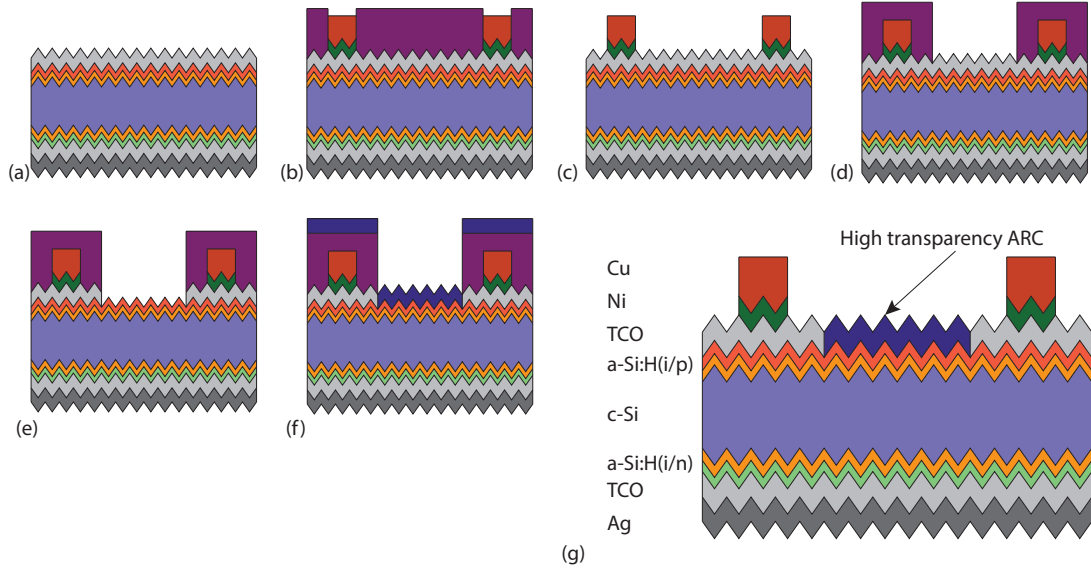


Figure 5.3: Process sequence for manufacturing of the first generation LEP devices: (a) Cell precursors with TCO (b) Photolithography and Ni/Cu plating (c) Photoresist removal (d) Second photolithography (e) Front-TCO wet chemical etching (f) Self-aligned alternative ARC deposition (g) Final device.

5.3.3 Results and discussion

Figure 5.4 (a) shows an optical microscope top view of an LEP device made with the process previously explained. In order to quantify the hole collection while reducing the contact coverage, LBIC measurements were performed on LEP cells with a 1-mm finger pitch and contact coverage of 25, 50, 75 and 100% (i.e. reference cell without ITO etching). We note that these cells do not feature an alternative ARC. The reduced current observed in Fig. 5.4 (b) can be explained by this lack of an ARC in the non-contacted part leading to a drop of $\approx 8\text{--}10\%$ as seen with the cell with 75% contact coverage. By lowering the contact coverage and thus increasing the lateral path of the minority carriers before they are collected, an additional loss of up to 3% is seen for the cells with the lowest contact coverage due to an electrical shading effect. [Reichel 2011] However, such loss is reduced when the cell operates under illumination and close to its MPP due to the higher minority-carrier lifetime at the injection level related to the MPP. This is illustrated in the inset of Fig. 5.4(b) where two LBIC scans show a reduced loss in collection at the MPP condition compared to the measurement carried out at the short-circuit condition and in the dark. [Filipic 2013] The cells were then characterized with light J - V . Figure 5.4 (c) shows the impact of both the finger pitch and the contact coverage on the FF . The cells with a 2-mm finger pitch have full coverage of the front TCO and act as the reference cell for each wafer. Starting with the full contact coverage, it can be observed that varying the finger pitch from 500 to 2000 μm results in a FF loss of $\approx 2\%$ explained by the increased series resistance. While reducing the contact coverage, the FF drops independently of the finger pitch, indicating the possible impact of the a-Si:H(p)/TCO

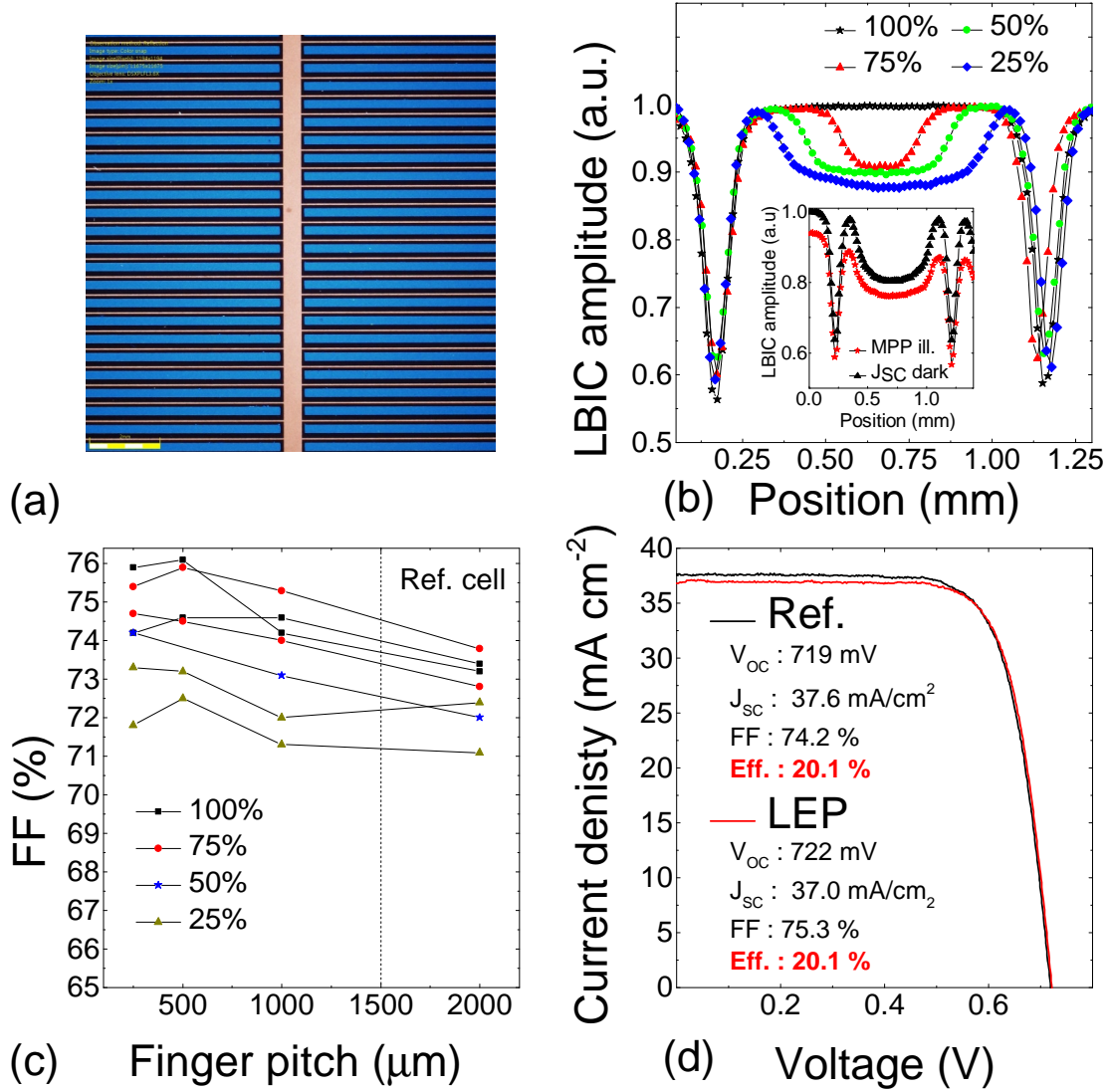


Figure 5.4: (a) Optical microscope top view of an LEP device with a finger pitch of 1 mm and a contact coverage of 50% (b) LBIC scans for LEP cells with a finger pitch of 1 mm and various contact coverages (c) FF as a function of the finger pitch for various contact coverages (d) J - V curve of an LEP cell with a 1-mm finger pitch and a contact coverage of 75% .

contact resistance. The occurrence of an increased series resistance is further confirmed by carrying out J - V measurements at lower illuminations: By decreasing the light intensity from 1 sun down to 0.25 sun, an increase of FF from 71.3 % up to 76.2 % is recorded for a LEP cell with 25 % of contact coverage. As a comparison, the same light intensity variation leads to a less important FF improvement for the reference cells from 76.1 % up to 77.7 % . By extracting the series resistance from the different J - V illuminations (see section 2.4.2), values of $2.11 \Omega\text{cm}^{-2}$ and $1.31 \Omega\text{cm}^{-2}$ were respectively extracted for a 25% contact-coverage LEP device and a reference cell. However, an important spreading of the reference cells' FF is observed

(i.e. with the 2000- μm finger pitch) although these cells have identical characteristics. This spreading makes a quantitative analysis of the impact of the contact coverage and finger pitch on the device performance impossible. However, as shown in Fig. 5.4 (d), cell efficiency of 20.1% can be obtained with 25% of un-contacted area and without alternative ARC.

To validate the feasibility of a self-aligned deposition of a high-quality alternative ARC, a low-temperature recipe to deposit silicon nitride by PECVD at 70 °C was developed. By using such a low temperature for the deposition, the photoresist can still be lifted off. Therefore, the use of ZnS thermal evaporation may be avoided and replaced by non-toxic silicon nitride. Although this process was not fully optimized for both the silicon nitride thickness and transparency, equivalent J_{sc} were measured for LEP devices with a 500- μm finger pitch and a contact coverage of 50% (data not shown).

5.3.4 Conclusions

To conclude this part on the first LEP device generation, we demonstrated the feasibility to realize cells with a given finger pitch and contact coverage. LBIC was successfully used to probe the carrier collection and revealed a loss of up to 3% in the local quantum efficiency for the lowest contact coverage. However, the most important device performance loss appears to come from the reduced contact area. As this loss was found to be independent of the finger pitch, this effect may be attributed to the a-Si:H(*p*)/TCO contact. [Gogolin 2014] However, despite these limitations, equivalent cell performances were obtained for cell with a relatively high contact coverage of 75%.

5.4 Rear hole collector configuration

In this section, SHJ devices with the hole collector placed at the rear side (denoted RHC) are investigated on cells where the charge-carrier extraction takes place on the entire device surface. This architecture is often reported in the literature as a "rear-emitter" SHJ device. This section first reviews the advantages of this device architecture compared to FHC cells and motivates the use of this configuration for LEP devices. Then, a study of how the front a-Si:H layers can be thinned is presented.

5.4.1 Motivation

From an LEP perspective, and as previously seen in section 5.3, the FHC configuration leads inevitably to electrical shading losses as minority carriers have to travel laterally before being collected.[Reichel 2011] Furthermore, in the case of n-type wafers, this architecture reduces the a-Si:H(*p*)/TCO contact surface which was found to be more critical in terms of specific contact resistivity compared to the a-Si:H(*n*)/TCO one.[Gogolin 2014] Hence, for the LEP cells, the RHC configuration presents significant advantages compared to the FHC configuration.

For standard SHJ solar cells, the RHC configuration was recently reported in literature as a possible way to improve the cell efficiency. [Terakawa 2012] [Varache 2015] This configuration was for instance reported by Bivour *et al.* for hybrid SHJ cells or by Descoeudres *et al.* for full heterojunction cells in either n- or p-type wafers. [Bivour 2011] [Descoeudres 2013] Indeed, this device architecture offers numerous advantages compared to FHC cells: First, with n-type wafers, as the majority-carriers are electrons with a mobility three times higher than that of holes, the lateral flow is as well ensured by the bulk of the c-Si absorber and not exclusively by the front-TCO as in the FHC case. Therefore, less constraint remains in the optimization of the front TCO which can be more optimized for optical purposes. [Bivour 2014] Based on this principle, Kobayashi *et al.* made bifacial RHC devices while respectively reducing and increasing the finger pitch on the rear and front side resulting in improved J_{sc} and FF . [Kobayashi 2013] Recently, Watahiki *et al.* replaced the front a-Si:H(*n*) of the RHC architecture with a μ c-Si:H(*n*) layer providing a good contact with IO:H and allowing cell efficiencies as high as 23.43 % . [Watahiki 2015]

5.4.2 Experimental

The cell precursors of this study were processed in the Octopus I PECVD reactor. First, thinning of the a-Si:H(*i*) layer on the n-side was investigated on standard FHC cells by reducing by a factor of ≈ 2 its thickness. Then, this thinned a-Si:H(*i*) layer was implemented in RHC cells while reducing the a-Si:H(*n*) layer thickness. In all cells presented here, an IO:H/ITO bilayer was used as the front-TCO and followed by Ag paste screen-printing and curing. The rear-contact was made by using the standard ITO/Ag contact stack. Instead of FHC where the rear-contact is usually deposited on the entire wafer surface, the same shadow mask than used for the front was used to pattern the back-side in order to avoid an artificially high dark recombination current leading to low FF . [Descoeudres 2013]

5.4.3 Results and discussion

As seen in Fig. 5.5 (a), outstanding surface passivation can be achieved even with an a-Si:H(*i*) layer thinned by a factor of ≈ 2 on the n-side. These cell precursors were then converted in cells and had similar V_{oc} and FF demonstrating that the thinned a-Si:H(*i*) passivation is not more sensitive to sputtering damage and is as well an efficient film in the electron collector. In Fig. 5.5 (b), the EQE curves of a FHC and a RHC cells with the nominal thicknesses of the doped layers are compared. The RHC cell has a thinned a-Si:H(*i*) layer whereas the FHC cell has the standard thickness. It can be observed that both cells show a similar EQE response. This is explained by the fact that the a-Si:H(*p*) layer was specifically optimized for its optical performance and is therefore thinner than the a-Si:H(*n*) layer with its nominal thickness. When reducing the deposition time of the a-Si:H(*n*) layer by up to a factor of two, a significant increase in the blue response is seen in the EQE [Fig. 5.5 (b)]. This improvement is then as well observed on the J_{sc} with a gain of $\approx 0.5 \text{ mA cm}^{-2}$ as shown in Fig. 5.6(b). Despite this impressive thickness reduction, a small reduction of the V_{oc} is seen for the thinnest a-Si:H(*n*)

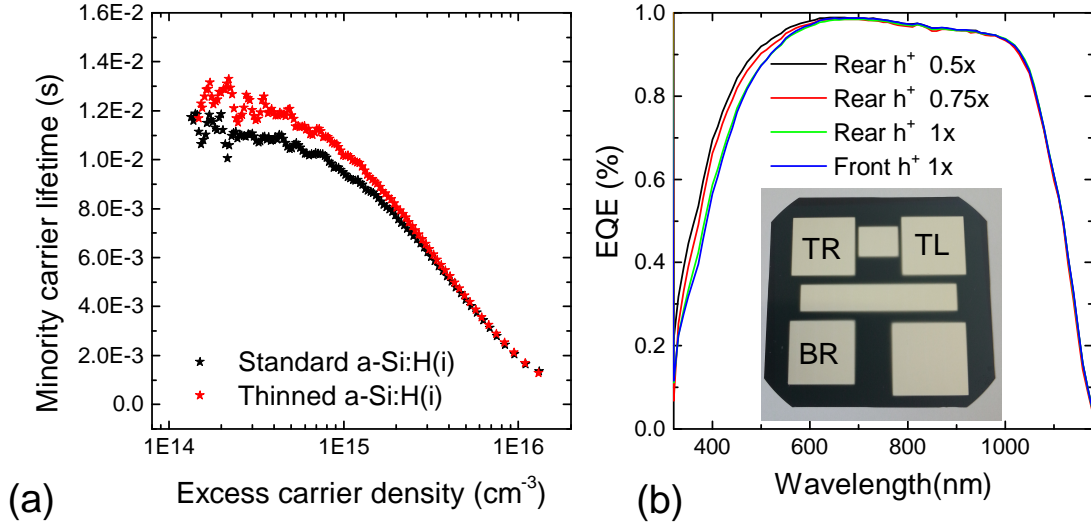


Figure 5.5: (a) Minority-carrier lifetime curves of cell precursors before the hole collector deposition for either the standard or the thinned a-Si:H(*i*) layer on the n-side. (b) External quantum efficiency for RHC cells with various a-Si:H(*n*) layer thicknesses and a FHC reference cell.

layer. This can be explained by a lower field-effect passivation. [Varache 2015] However, even with the thinnest a-Si:H(*in*) stack, V_{oc} of up to 720 mV was demonstrated. Importantly, it can be seen that cells on the same wafer show a significant variation for both the V_{oc} and the FF . This effect is not observed for the FHC cells. Furthermore, it was observed that the best performances were always recorded for the same cell position on the wafer [cell "BR" in the inset of Fig. 5.6 (b)]. This may be explained by more crosstalk between the TR and TL cells with the test structures increasing their saturation dark current. [Descocudres 2013]

5.4.4 Conclusions

To conclude, we showed in this study that the thicknesses of the a-Si:H layers on the n-side of SHJ solar cells can be importantly reduced. [Varache 2015] With our layers, we showed that both the a-Si:H(*i*) and a-Si:H(*n*) layers can be thinned by a factor of two from their nominal thicknesses normally used for FHC cells. Despite a small decay in the V_{oc} , this thickness reduction enables a significant J_{sc} gain enabling cell efficiencies of up to 21%. We showed that although a proper back patterning of the rear side was realized, the wafer layout has a significant impact on both the V_{oc} and the FF . Therefore, even more efficient cells may be realized by suppressing the test structures placed in between the cells or by increasing the cell size, for instance to a $6 \times 6 \text{ cm}^2$. [Demaurex 2014b]

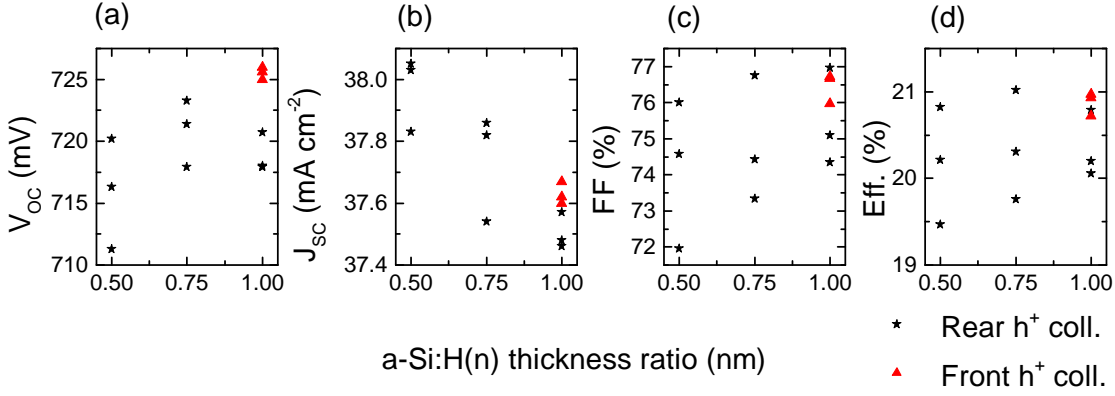


Figure 5.6: Impact of the a-Si:H(*n*) thickness on the (a) V_{OC} , (b) J_{SC} , (c) FF and (d) cell efficiency.

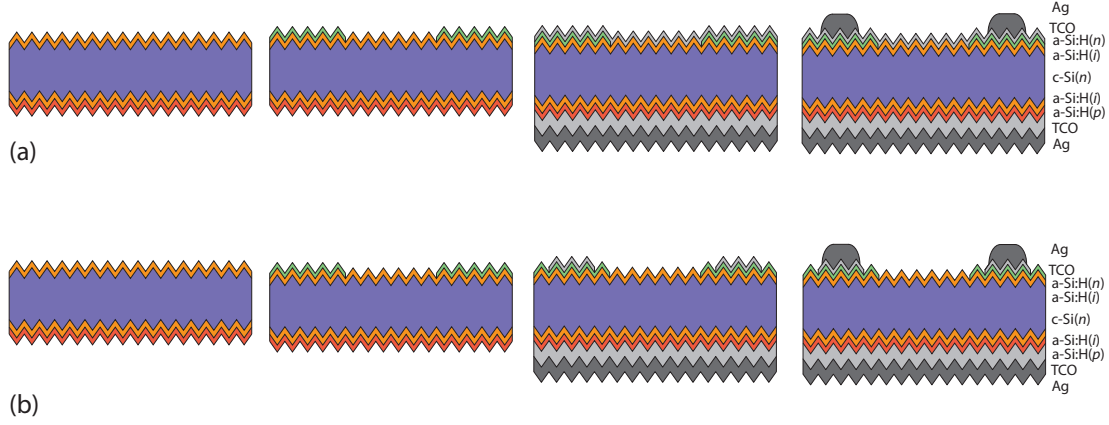


Figure 5.7: Process flow of the second generation of LEP devices with: (a) an un-patterned front TCO (b) a patterned front TCO.

5.5 LEP devices with a patterned front a-Si:H layer

5.5.1 Introduction

In this section, we discuss a second generation of LEP devices in which the front doped a-Si:H layer is patterned. Based on the results obtained with the first generation of LEP devices in which the a-Si:H(*p*)/TCO contact was suspected to significantly affect the device performance, both RHC and FHC configurations were investigated. This study is divided into two parts: First, devices in which only the front doped a-Si:H layer is patterned and then covered by a blanket TCO layer are investigated. Second, devices with patterning on both the front doped a-Si:H and the front TCO layers are studied.

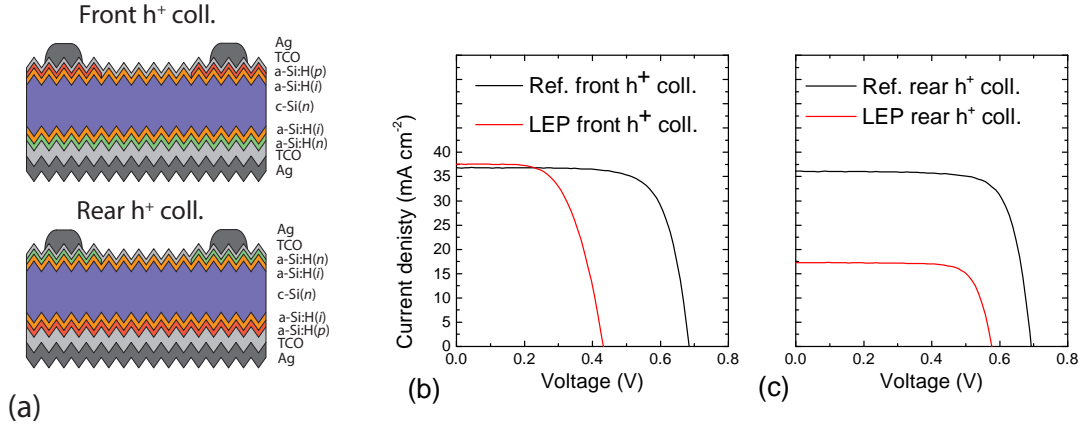


Figure 5.8: (a) LEP device schematics with both FHC and RHC configurations, patterned front doped a-Si:H layer and a blanket front-TCO (b) Light J-V curves for an LEP device with the FHC configuration and a reference cell (c) Light J-V curves for an LEP device with the RHC configuration and a reference cell.

5.5.2 Experiments

Figure 5.7 shows the process flow used for the second generation of LEP devices. In-situ masking was chosen to pattern the front doped a-Si:H layer. The main advantage of this technique is that it can be easily implemented in the process flow without numerous additional steps. However, due to tapering of the a-Si:H thickness deposited through the shadow mask, a minimum feature size is required. [Tomasi 2014] In this experiment, we used the same masking technique as developed by Tomasi *et al.* for the manufacturing of IBC-SHJ solar cells. [Tomasi 2014] 230- μm -thick wafers with the same cleaning procedure as the cell wafers were used for the shadow masks and laser micro-machined to create the openings. To simplify the process flow as much as possible, silver paste screen-printing with a finger spacing of 2.1 mm was used for the metallization. The openings in the a-Si:H shadow mask were fixed to 1 mm, leading to a coverage of the front doped a-Si:H layer of $\approx 50\%$. As depicted in Fig. 5.7(a), in the first version of these LEP devices, the front-side is contacted with blanket TCO layer whereas the second version introduces a second shadow masking for the TCO deposition. In this last case, a 500- μm -wide opening was used to avoid any deposition of the front TCO on the a-Si:H(i) layer. In this study, no alternative ARC was deposited at the front side of the cells with the patterned front TCO.

5.5.3 Results and discussion

Non-patterned front TCO

Figure 5.8 (b) and (c) shows the light J-V curves of LEP devices with a patterned front doped a-Si:H layer capped by a blanket front TCO for the FHC and the RHC configurations respectively. It can be observed in both cases that the direct deposition of the front TCO on the un-protected

a-Si:H(*i*) film has a dramatic impact on the cell performance. In the FHC configuration, the J_{sc} is slightly improved while removing part of the a-Si:H(*p*) layer. This indicates that the a-Si:H(*i*)/TCO interface forms a hole-selective contact. It can be observed in the LBIC scans depicted in Fig. 5.9 (a) that a perfect collection is made on any part of the FHC LEP device. A slight increase of the LBIC response can even be observed due to lack of the a-Si:H(*p*) layer. This effect would be more pronounced with an LBIC probing beam with a shorter wavelength. However, the V_{oc} is dramatically reduced to ≈ 430 mV. We note that such V_{oc} drop cannot be explained solely by a lower minority-carrier lifetime as even a τ_{eff} of 10 μ s would lead to a V_{oc} of ≈ 600 mV as simulated in PC1D. [Clugston 1997] The V_{oc} drop is rather explained by the lack of the a-Si:H(*p*) layer removing therefore the screening of work function of the TCO. [Bivour 2013]

In the RHC configuration, the parasitic contact of the TCO with the a-Si:H(*i*) layers leads to a severe drop in the J_{sc} [Fig. 5.8(c)]. LBIC investigation reveals that all carriers generated in the area with the direct contact between the TCO and the a-Si:H(*i*) are lost [Fig. 5.9 (b)]. As previously seen with the FHC cell, the a-Si:H(*i*)/TCO interface collects the holes. Therefore, in the RHC configuration, this parasitic contact prevents the holes from reaching the hole collector located at the rear side leading to an electronically dead area.

Therefore, we conclude that in both cases, the front TCO must be patterned in order to avoid the formation of a parasitic contact with the a-Si:H(*i*) film.

Patterned front TCO

Based on the previous results, a shadow mask was used to pattern the front-TCO in order to avoid the parasitic a-Si:H(*i*)/TCO contact previously experienced. Figure 5.10 (b) shows the V_{oc} , the J_{sc} , the FF and the cell efficiency of LEP and reference cells in both the FHC and the RHC configurations. It can be seen that, in most cases, V_{oc} values are in the 700 mV range demonstrating an efficient insulation between the front TCO and the a-Si:H(*i*). As the LEP cells have no alternative ARC, their J_{sc} values are expected to be lower. Assuming, a 10% reflectance for a surface of un-coated random pyramids, this would decrease the J_{sc} from 37 mA cm^{-2} to ≈ 33 mA cm^{-2} for the FHC cells and from 36 mA cm^{-2} to ≈ 32 mA cm^{-2} for the RHC cells. Interestingly, the measured J_{sc} values do not match the latter values: For the FHC LEP device, an important electrical shading is experienced as seen in the LBIC scans shown in Fig. 5.11 (e) and leads to an average J_{sc} of ≈ 31 mA cm^{-2} . Conversely, in the RHC LEP device, the patterned a-Si:H(*n*) layer leading to less parasitic absorption allows a J_{sc} of ≈ 35 mA cm^{-2} despite the lack of the front ARC.

Relatively low FF values below 70% were measured for both FHC and RHC devices. Light J - V measurements carried out at lower illuminations confirmed an increased series resistance for the LEP-architectures. This may be first explained by the low contact coverage of $\approx 25\%$. According to this explanation, better FF values were measured for the RHC LEP as the specific contact resistivity is lower for the a-Si:H(*n*)/TCO contact than for the a-Si:H(*p*)/TCO.

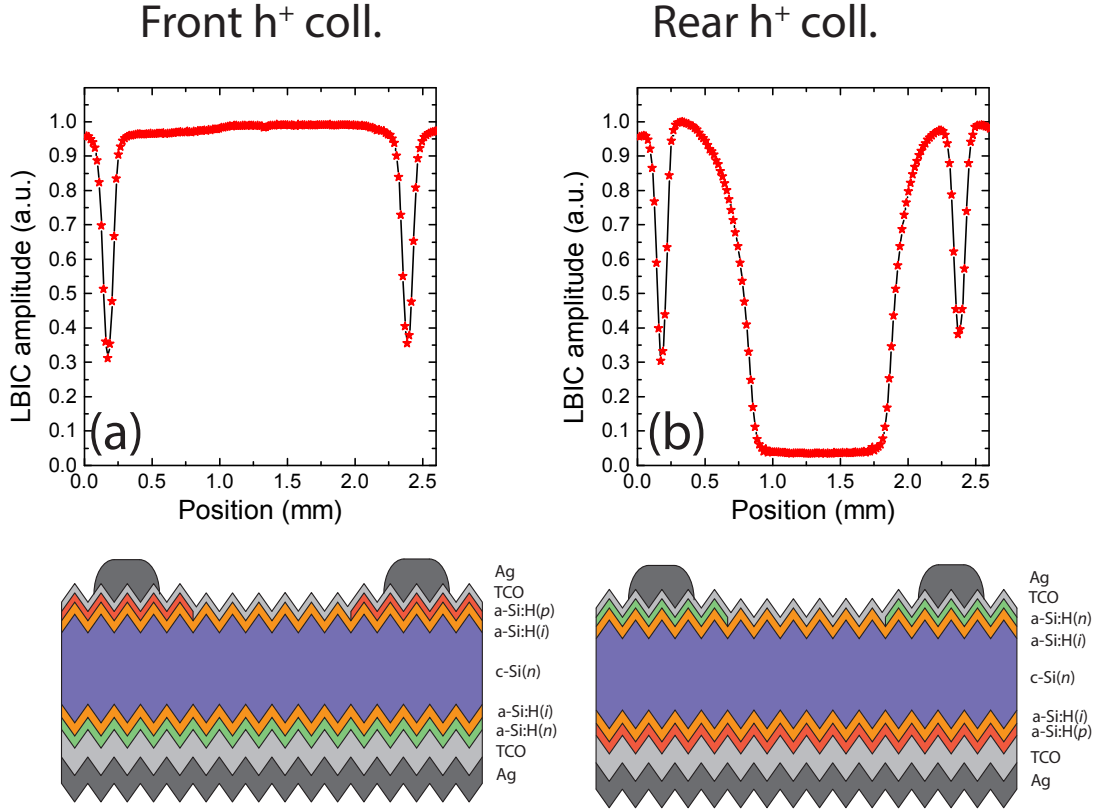


Figure 5.9: LBIC scans for LEP devices with a blanket front TCO and (a) a localized hole collector or (b) a localized electron collector.

[Gogolin 2014] Furthermore, as previously mentioned, the lateral transport is expected to be more efficient in RHC cells. This leads to an efficiency of 17.2 % for such LEP device with the RHC configuration without alternative ARC.

To investigate the lateral transport in such device, scans of the TCO voltage were carried out on the reference cells. As depicted in Fig. 5.11 (a) and (b) for a FHC cell, a lower voltage drop is seen when the cell is operated at its MPP indicating that part of the current flows in the wafer at the MPP but not when the cell is at its J_{sc} [see Chapter 3, Fig. 3.8]. According to Eq. 3.1, a sheet resistance of $105 \Omega_{\square}$ is deduced which matches the front-TCO sheet resistance measured by the four-probe technique. However, for the RHC cells, a significantly lower voltage drop is seen at the J_{sc} operation. This is explained by the transport taking part in the wafer resulting in an effective sheet resistance of $45 \Omega_{\square}$.

5.5.4 Electrical model and simulations

In order to evaluate the impact of the contact area and the finger pitch in RHC LEP devices, a model was developed. This model is based on the cell structure presented in Fig. 5.12 (a): The

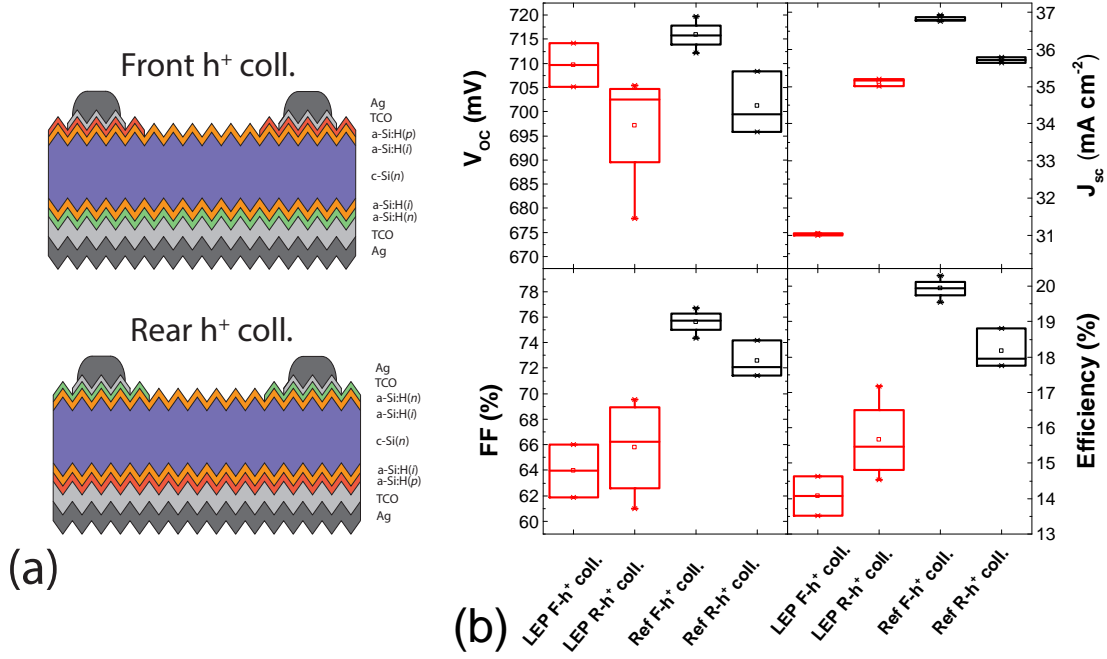


Figure 5.10: (a) LEP device schematics with both FHC and RHC configurations and a patterned front TCO (b) Light J-V characteristics of LEP and reference solar cells.

cell is divided into two parts respectively with and without the a-Si:H(*n*)/TCO stack and with a contact coverage ratio δ . In the contacted part, the power loss P_1 is evaluated by Eq. 5.1 with an effective sheet resistance $R_{\square 1}$ taking into account both the lateral transport in the front TCO and in the wafer. In the non-contacted part, the power loss P_2 is deduced from the lateral transport in the wafer characterized by a sheet resistance $R_{\square 2}$ as shown in Eq. 5.2. In a first approximation, the contact resistance is assumed to scale linearly with the contact coverage. Finally, the non-contacted part is assumed to couple more efficiently the light in the absorber due to the reduced parasitic absorption. We note that the finger shadowing is not taken into account in this model.

$$P_1 = \int_{(1-\delta)\frac{s}{2}}^{\frac{s}{2}} I^2(x) dR = J^2 l R_{\square 1} \int_{(1-\delta)\frac{s}{2}}^{\frac{s}{2}} x^2 dx = \frac{1}{24} J^2 L R_{\square 1} s^3 (1 - (1 - \delta)^3) \quad (5.1)$$

$$P_2 = \int_0^{(1-\delta)\frac{s}{2}} I^2(x) dR = J^2 l R_{\square 2} \int_0^{(1-\delta)\frac{s}{2}} x^2 dx = \frac{1}{24} J^2 L R_{\square 2} s^3 (1 - \delta)^3 \quad (5.2)$$

Here, we assumed a relatively resistive front-TCO with a sheet resistance of $130 \Omega_{\square}$ and the wafer resistivity was set to $4 \Omega cm$. We assumed a $230\text{-}\mu m$ -thick wafer and two specific contact resistivities ρ_c for the a-Si:H(*n*)/TCO contact of either 0.1 or $0.01 \Omega cm^2$. [Gogolin 2014] [Watahiki 2015] Finally, an ideal optical gain of 2 mA cm^{-2} was defined for the non-contacted part. [Holman 2012] The finger pitch was varied from $50 \mu m$ to 2 mm and the contact coverage from 5% to 100% (i.e. full coverage).

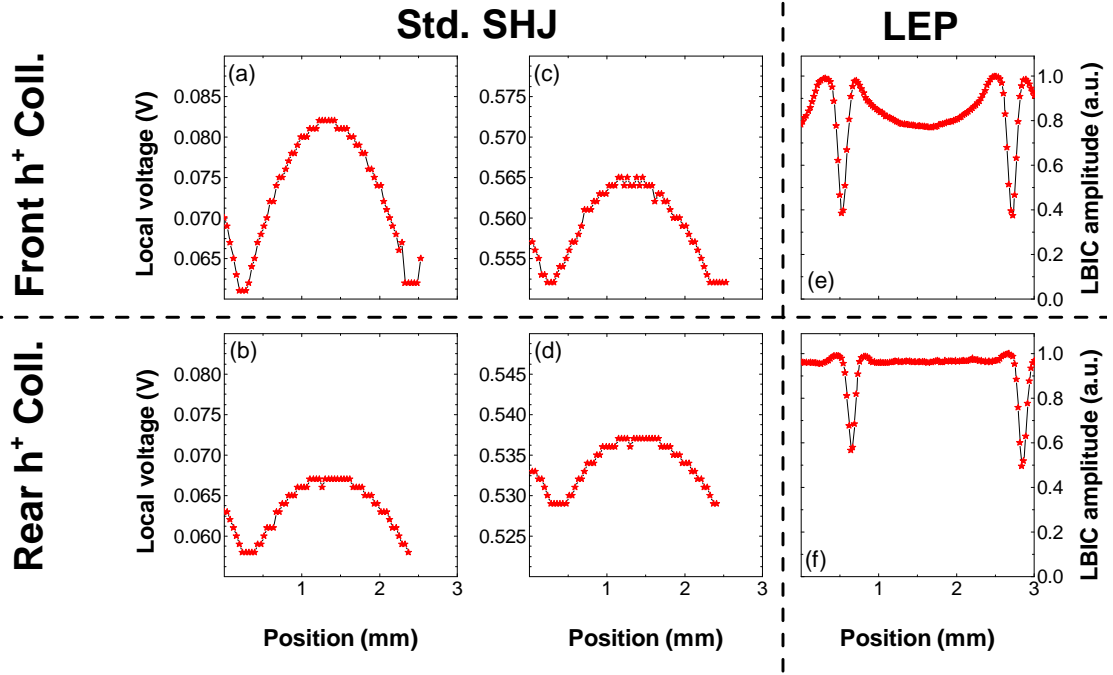


Figure 5.11: Voltage scans on the front TCO of reference cells for (a) FHC at J_{sc} (b) FHC at the MPP (c) RHC at J_{sc} (d) RHC at the MPP (e) LBIC scan of a FHC LEP device (f) LBIC scan of a RHC LEP device.

Figure 5.12 (b) and (c) shows the cell efficiency as a function of the finger pitch and of the contact coverage ratio respectively for a specific contact resistivities of $0.1 \Omega \text{ cm}^2$ and $0.01 \Omega \text{ cm}^2$. The modeled FF of the devices presented in Fig. 5.10—i.e. RHC, 2 mm finger pitch and 25 % and 100 % contact coverage for the LEP and the reference devices respectively—are displayed in Fig. 5.12 (b). A $\approx 2 \%$ loss in FF with the LEP structure is obtained which corresponds to the experimental data shown in Fig. 5.10. By investigating further the results obtained by this model, we see in Fig. 5.12 (b) that with $\rho_c = 0.1 \Omega \text{ cm}^2$, a relatively small gain in efficiency of $\approx 0.5\%$ can be expected for a 1-mm finger pitch. Furthermore, a minimum contact coverage ranging between 20–60% is required to avoid excessive losses due to the a-Si:H(n)/TCO contact. Therefore, two patterning steps are required to realize such device. However, while reducing ρ_c to $0.01 \Omega \text{ cm}^2$, improved cell efficiencies may be achieved even with contact coverage of 5% corresponding to a contact located solely under the front grid. This implies that a $\approx 1 \%$ efficiency improvement may be realized while using a single patterning step as proposed in the section 5.6.

5.5.5 Conclusions

The feasibility of LEP devices with patterned front doped a-Si:H layers was demonstrated. We showed that in all cases, the contact between the front TCO and the a-Si:H(i) layer must be avoided. As demonstrated by LBIC and TCO voltage scans, the RHC configuration is preferred

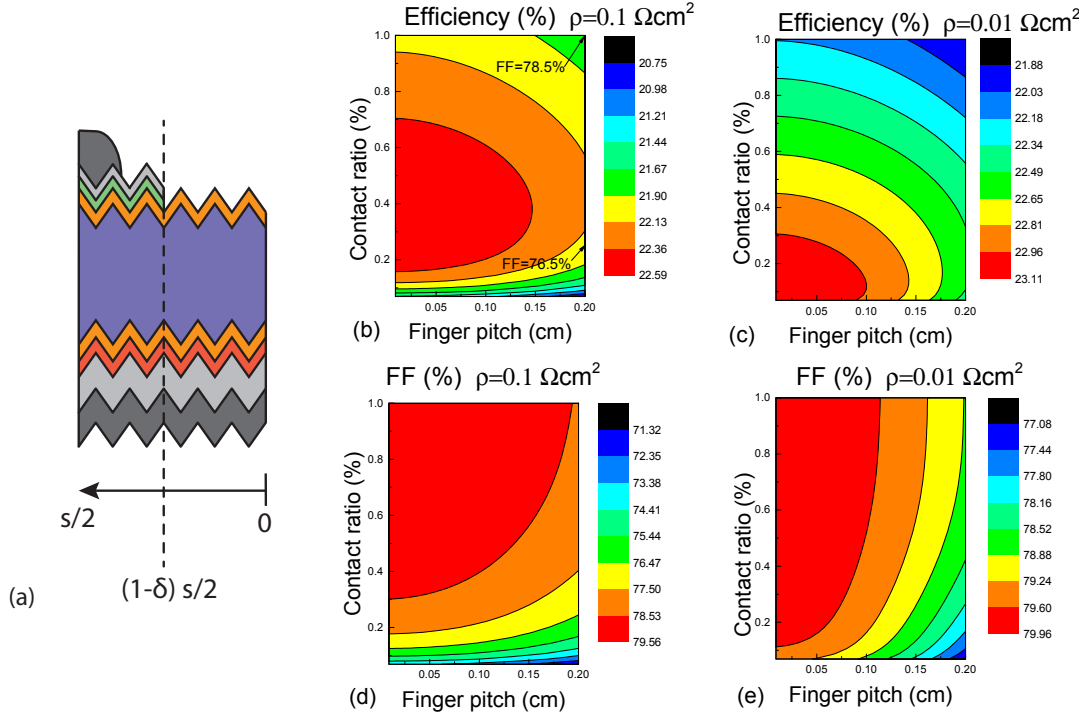


Figure 5.12: (a) Schematic of a RHC LEP cell considered for the model (b) Impact of the finger pitch and of the contact coverage on the cell efficiency with $\rho=0.1\Omega\text{cm}^2$ (c) Impact of the finger pitch and of the contact coverage on the cell efficiency with $\rho=0.01\Omega\text{cm}^2$. (d) Impact of the finger pitch and of the contact coverage on the FF with $\rho=0.1\Omega\text{cm}^2$ (e) Impact of the finger pitch and of the contact coverage on the FF with $\rho=0.01\Omega\text{cm}^2$

to the FHC configuration as no electrical shading is experienced and as a more efficient lateral transport is achieved due to the wafer contribution. This was experimentally seen by better FF and J_{sc} values for RHC LEP devices. By modeling the impact of the finger pitch and the contact coverage on the performance of RHC devices, a minimum contact coverage of $\approx 20\%$ was found to be necessary with high ρ_c values. Nevertheless, by decreasing ρ_c to $0.01 \Omega\text{cm}^2$, efficiency gain may be expected even for devices with a 5% contact coverage. However, this latter point must be experimentally verified.

5.6 Low-contact-coverage LEP devices

This section investigates LEP devices with low contact coverage. The aim of these cells is to verify experimentally whether LEP devices can be realized with a contact located exclusively underneath the metallic fingers. The main advantage of such a device is its extreme simplicity in processing as shown in Fig. 5.13 (a). In this process, the front grid plays the role of the mask for the TCO patterning. Then, hydrogen plasma etching can be used to selectively remove the front a-Si:H(n) layer as demonstrated in Chap. 4. Finally, a highly transparent alternative front ARC can be deposited. Hence, this sequence does not rely on any masking technique except

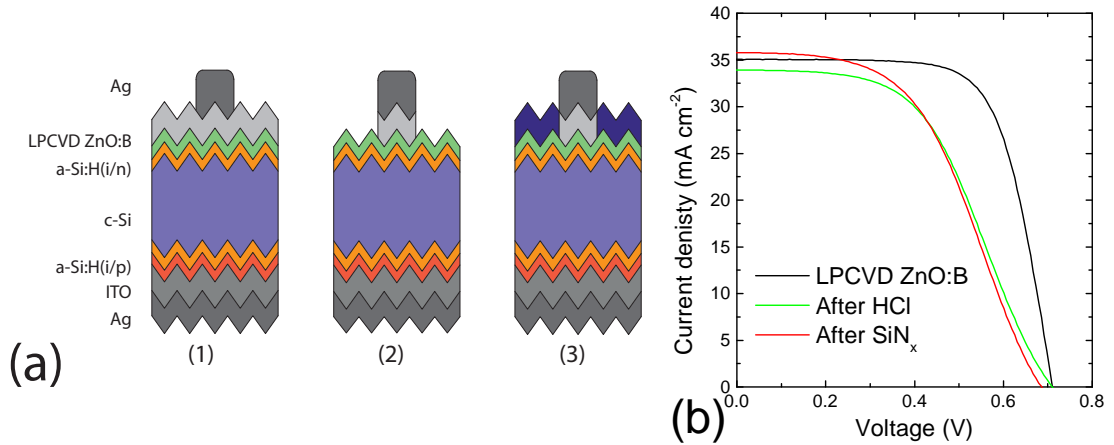


Figure 5.13: (a) Process sequence to make an LEP device with low contact coverage (b) Light J - V curves of the cell before and after the ZnO:B etching and after the deposition of the silicon nitride ARC.

for the screen-printing of the metallic front grid.

In this section, cells results obtained by using this approach are discussed. Finally, the impact of the silicon nitride deposition on the surface passivation is investigated.

5.6.1 Self-masked ZnO etching

The devices processed in this study were realized with cell precursors made in the Kai-M PECVD reactor. LPCVD ZnO:B was used for the front TCO as this material can be easily removed even in weak acids such as diluted HCl [Fig. 5.13 (a) 2]. The rear side is contacted with the standard ITO/Ag stack. Finally, a silicon nitride layer was deposited in the XL PECVD system at 200 °C to form the front ARC [Fig. 5.13 (a) 3].

Figure 5.13 (b) shows the light J - V curves of the cell before and after ZnO:B etching in diluted HCl and after the deposition of the silicon nitride ARC. It can be observed that decreasing the contact coverage from the entire cell surface down to ≈ 5 % induces a significant drop of the FF with the occurrence of a strong series resistance. The FF dropped from 69 % to 50 % leading to a cell efficiency of 12.2 % . This confirms the statement made with the LEP model that sufficient contact coverage must be realized. Interestingly, the deposition of silicon nitride even slightly decreases the V_{oc} of the cell pointing out a possible detrimental effect of the silicon nitride deposition on the minority-carrier lifetime.

5.6.2 Impact of silicon nitride deposition on surface passivation

In order to probe its impact on surface passivation, silicon nitride was deposited on wafers with an a-Si:H(i), a-Si:H(in) or a-Si:H(ip) layers. Figure 5.14 shows the minority-carrier lifetime

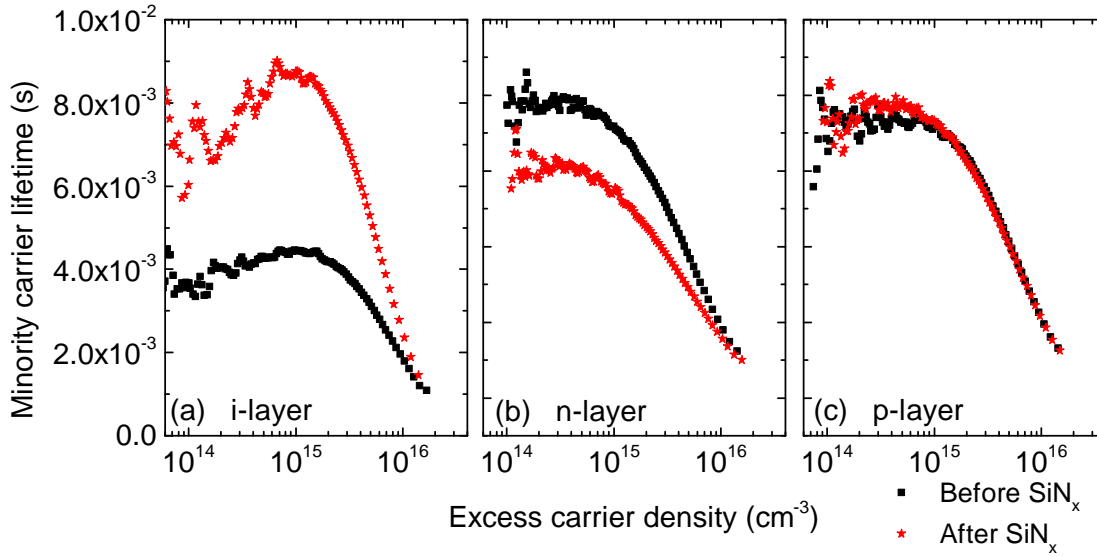


Figure 5.14: Minority-carrier lifetime curve as a function of the carrier injection before and after deposition of silicon nitride on wafers featuring an (a) a-Si:H(*i*) (b) a-Si:H(*in*) or (c) a-Si:H(*ip*) layer.

curves before and after the silicon nitride deposition. Starting with the deposition on the a-Si:H(*i*) layer, a 12-ms lifetime was measured directly after the a-Si:H(*i*) deposition (data not shown). As it was not possible to deposit the silicon nitride directly after the a-Si:H PECVD, the samples were kept under a N_2 storage environment for 45 days. Prior to the silicon nitride deposition, the samples were re-measured and a relatively modest lifetime of ≈ 4 ms was obtained. This shows the sensitivity of thin a-Si:H(*i*) passivating films when not capped by any protective layers. [Olibet 2006] However, the minority-carrier lifetime recovered after the silicon nitride deposition due to the in-situ annealing and hydrogenation of the passivation. For both the a-Si:H(*in*) and the a-Si:H(*ip*) layers, good minority-carrier lifetimes were preserved after the deposition of silicon nitride. Counterintuitively, a slight decay in passivation is seen for the a-Si:H(*in*) layer, although the positive charges of the silicon nitride are expected to further reinforce the passivation by a field effect.

5.6.3 Conclusions

LEP devices with extremely an low contact coverage fraction were realized. A simple process based on the self-masking provided by the metallic front grid and the etching of LPCVD ZnO:B was successfully demonstrated. However, significant series resistance induced by the low contact coverage was evidenced, preventing the proper operation of such devices.

5.7 Modular LEP devices

As seen in section 5.3, reproducibility from one device to another with exactly the same geometry and process sequence was found to be an issue and makes data analysis difficult. Hence, an ideal LEP test structure would be a device able to be arbitrarily reconfigured in any geometry. Based on this idea, we developed a device made of 40 segments of $240\text{ }\mu\text{m}$ by 1 cm placed next to each other forming a 1 cm^2 solar cell. As all the segments are independent, it is therefore possible—by either contacting or let them floating—to create an LEP cell able to be reconfigured in-situ during the J-V characterization. In this section, we describe the specific process flow required for creating such a device structure and present the preliminary results obtained by doing an LBIC characterization of a device made on a polished c-Si wafer.

5.7.1 Experimental

One of the main challenges in manufacturing a modular LEP device (denoted as ModLEP) is that the contacting pads— $\approx 500\text{ }\mu\text{m}$ wide—must be placed outside of the segments and thus be insulated from the rest of the device. Moreover, as the extracted current may be relatively important, especially if the device is operated under light concentration, narrow and highly conductive fingers are required. Figure 5.15 (a) shows the most important steps of the process-flow to realize such device. Starting from a cell precursor featuring an a-Si:H(*ip*)/ITO stack at the front side and an a-Si:H(*in*)/ITO/AG stack as the rear contact, a first photolithography is done to define the $240\text{-}\mu\text{m}$ -wide strips in the front TCO [Fig.5.15 (a) 1]. After an etching in 5% diluted HF, an insulating SiO_2 layer is thermally evaporated while using the photoresist to carry a self-aligned lift-off [Fig.5.15 (a) 2]. A Cu seed layer is then evaporated and locally removed by manually dispensing some Cu etchant on the alignment mark (i.e. for subsequent photolithography alignment). A second photolithography is then carried out to define the metallic fingers geometries [Fig.5.15 (a) 4]. The Cu plating is made either by applying the potential at the rear side of the device (in the FHC case) or directly by contacting the seed-layer (for the RHC case). Finally, the Cu seed-layer was back-etched [Fig.5.15 (a) 5].

5.7.2 Results and discussion

Figure 5.15 (b) and (c) shows the entire surface of the first ModLEP manufactured on a polished c-Si wafer and a magnified 3D laser microscope image reconstruction of one segment. As shown in these figures, a good patterning accuracy was achieved demonstrating the robustness of the process. Figure 5.15 (d) presents an LBIC scan of the area shown in the figure inset when only the first segment is contacted. As expected, an exponential decay is seen while scanning the other segments which demonstrates a good isolation between the different segments.

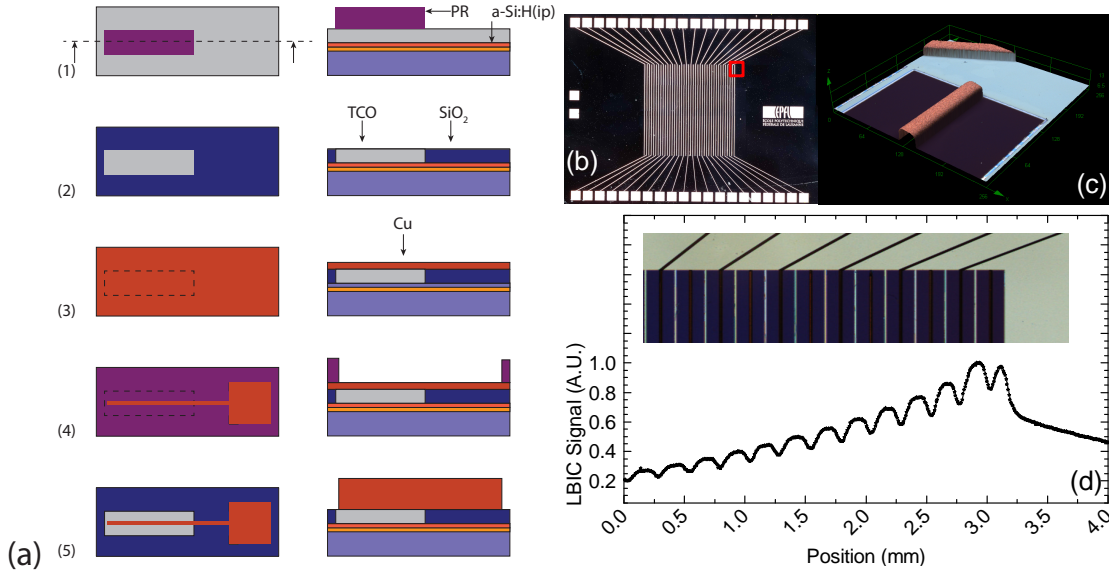


Figure 5.15: (a) Key process steps for the realization of a ModLEP device (b) Optical microscope top view of the entire ModLEP device (c) 3D laser microscope image reconstruction of part of one segment with its Cu finger (d) LBIC scan of the ModLEP device with only the last segment contacted. The inset in (d) shows the 12 first segments displayed at the LBIC scan scale.

5.7.3 Conclusions

We demonstrated the feasibility of a complex device structure based on SHJ solar cells merging numerous micro-fabrication techniques including Cu plating. The LBIC investigation excluded any crosstalk between the different segments. Hence, ModLEP devices are interesting test structures to study lateral transport and the contact coverage impact on cell performance while probing the same device in different configurations.

5.8 General conclusions on LEP-SHJ devices

Based on the experiments and the observations gathered during this chapter, we first conclude that the RHC configuration is necessary for the LEP-SHJ solar cell structure. Indeed, this configuration avoids the electrical shading effect and benefits from the lateral conduction of the c-Si wafer. Furthermore, the lower specific contact resistivity of the a-Si:H(*n*)/TCO contact compared to the a-Si:H(*p*)/TCO is a crucial point when the contact coverage is massively reduced. Second, we demonstrated that with the a-Si:H and TCO layers used for standard SHJ devices, low contact coverage (i.e. below 30%) lead to significant *FF* losses even in the RHC configuration. This prohibits a contact only formed underneath the metallic front grid and necessarily implies the use of two patterning steps to respectively create the fingers and wider TCO contacts. As a consequence, the potential optical improvement is reduced with this geometry. Furthermore, with this additional patterning, the process complexity becomes equivalent to IBC-SHJ devices where higher optical gains were already demonstrated. However,

as suggested by simulations, simple LEP devices with a contact only underneath the front-grid can be realized if a sufficiently low specific contact resistance between the a-Si:H(*n*) and the TCO layer is achieved. Indeed, as shown by de Vecchi *et al.*, *FF* values close to 70 % can be achieved even with a contact coverage of 4% suggesting that the low *FF* values obtained during our investigations are more likely related to the material properties than due to a fundamental limitation of the device structure. A possible approach to reduce this contact resistance may be the use of n-doped microcrystalline silicon layers. [Seif 2015a] [Watahiki 2015]

6 Transition metal oxide films as a-Si:H(*p*) replacement

Summary

We investigate in this chapter the replacement of the a-Si:H(*p*) layer by highly transparent metal oxide materials. In this respect, molybdenum oxide was studied to create a hole-selective collector. First, we observed significant modifications of the optical properties of the MoO_{*x*} film induced by the TCO sputtering and the final cell annealing. A closer investigation revealed that although no detrimental consequences are observed for the surface passivation, the annealing however massively impacts the electrical transport with the occurrence of a reversed Schottky diode blocking the hole transport. At the cell level, this leads to strongly S-shaped *J-V* curves resulting in low *FF*. By avoiding post-deposition annealing above 130 °C and by optimizing the deposition processes, we then demonstrate that MoO_{*x*}-based devices can have *FF* similar to standard SHJ devices, in addition to an improved response in the blue part of the spectrum. Finally, we demonstrate that Cu plating is a suitable and compatible metallization technique for MoO_{*x*}-based devices resulting in a certified efficiency as high as 22.5% with *FF* above 80% for a 4 cm² solar cell.

6.1 Introduction and motivation

This chapter investigates the replacement of the a-Si:H(*p*) hole collector in SHJ solar cells with a thin film of transition metal oxide (TMO) and in particular sub-stoichiometric molybdenum oxide (MoO_{*x*}, *x*<3) and is partially based on a paper accepted for publication in [Applied Physics Letters](#) and reproduced with permission from [Geissbühler 2015]. Copyright 2015, AIP Publishing LLC.¹ Sections taken from this paper are marked by the symbol †.

¹The results presented here were obtained with the help of J. Werner, S. Martin de Nicolas, N. Badel, A. Tomasi, L. Barraud, Aïcha Hessler-Wyser, M. Despeisse, S. Nicolay, D. Sacchetto, B. Niesen, S. De Wolf and C. Ballif.

This chapter is structured as follows: First, a detailed optical characterization of the MoO_x film is made with a particular emphasis on how this material evolves with plasma and thermal processes (as for instance the TCO sputtering and the annealing of the low-temperature Ag paste). The impact of these steps on the MoO_x film microstructure and on the surface passivation of the underlying a-Si:H(*i*) is then studied. Next, the fabrication processes are specifically optimized for the MoO_x -based hole-collector cells and the performances of such devices are then compared to a-Si:H(*p*) references. Finally, the Cu-plated metallization developed in chapter 3 is applied to these devices to realize solar cells with high efficiency and high *FF*.

6.1.1 Motivation[†]

As previously seen in chapter 5, the a-Si:H(*p*) film acting as the hole collector in standard SHJ solar cells leads to parasitic light absorption losses of up to 1.5 mA cm^{-2} due to its $\approx 1.6\text{--}1.8$ eV bandgap and its important dopant concentration. [Holman 2012] Alternative Si-based materials with wider bandgap such as a-SiO_x:H, $\mu\text{c-SiO}_x\text{:H}$ or a-SiC_x:H were proposed to overcome this issue. [Ding 2013a] [Pysch 2011] Unfortunately, proven optical gains for these materials bring along lowered electrical performance due to the increased band offsets at the amorphous/crystalline silicon interface, hindering efficient carrier extraction. [Seif 2014] [Mazzarella 2015] [Fujiwara 2007] Even more important optical gains may be achieved by using highly transparent TMOs as window layers, provided their work function is appropriate for carrier collection. [Bivour 2015][Battaglia 2014b] Metal oxides, and in particular MoO_x , were already investigated as hole-collecting materials for organic [Chen 2012] [Griffin 2013] [Shrotriya 2006] and inorganic [Il Park 2011] [Gretener 2013] [Fang 2014] [Loper 2015] [Werner 2015] thin-film solar cells, as well as for organic light-emitting diodes. [Hamwi 2010] [Meyer 2008] [Meyer 2012] For these applications, the metal oxide layer often also protects sensitive underlying layers from sputtering-induced damage during TCO deposition. [Tate 1991] [Kim 2011] Exploiting their bandgap of ≈ 3 eV, MoO_x films were recently also integrated into SHJ devices to replace the a-Si:H(*p*) layers, resulting in clear optical gains. [Battaglia 2014a] However, the *FF* of these devices remained below 70%, with increasingly pronounced S-shaped illuminated *J-V* curves when increasing the MoO_x film thickness, indicating a hole-collection issue, [Battaglia 2014a] despite its argued appropriate work function. [Bivour 2013] [Bullock 2014]

6.1.2 Band diagram and carrier extraction in TMO-based hole-collector SHJ solar cells

Figure 6.1(a) shows the device schematic of the MoO_x -based solar cell proposed by Battaglia *et al.* [Battaglia 2014a] The hole-collector band structure is sketched in Fig. 6.1(b). Although MoO_x film exhibits an n-type characteristic, [Bullock 2014] its high work function (WF)—up to ≈ 6.9 eV for stoichiometric MoO_3 —leads to the creation of an inversion region in the c-Si

Contributions are gratefully acknowledged.

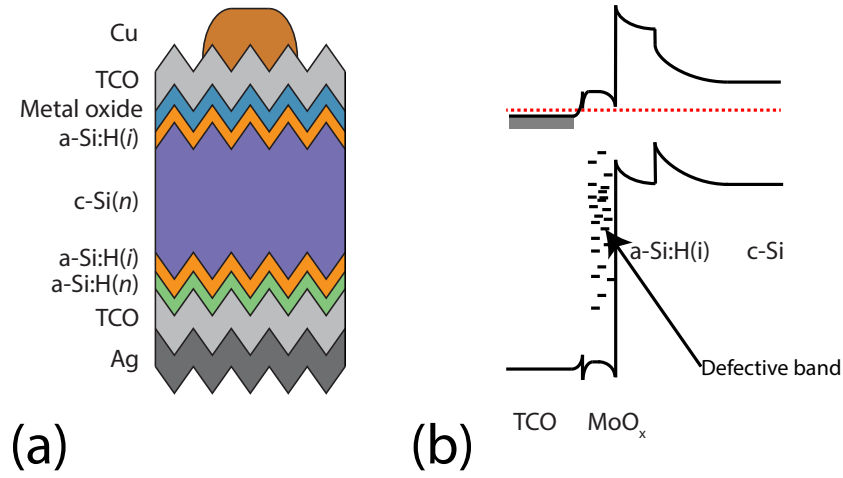


Figure 6.1: (a) Schematic cross-section of a TMO-based hole-collector SHJ solar cell (b) Band diagram of the c-Si/ a-Si:H(*i*)/ MoO_x/TCO interface.

surface vicinity. [Bullock 2015] [Bivour 2015] Contrary to an a-Si:H(*p*) hole collector where the carrier transport takes place through the tail states of the a-Si:H(*p*) material, in the MoO_x case, the hole transport is realized by a band of defective states located in its bandgap induced by the material substoichiometry. [Battaglia 2014a] The bandgap, the WF and the electron affinity (χ) of *stoichiometric* TMOs investigated in this thesis are given in Tab. 6.1.[Greiner 2012] [Meyer 2012] It has to be noted that the WF can strongly deviate from these values depending on their stoichiometry, air exposure and possible contamination.[Greiner 2013] [Bivour 2015] [Battaglia 2014b]

Table 6.1: Bandgap, work function (WF) and electron affinity (χ) of different TMO investigated in this thesis.

	E_g (eV)	WF (eV)	χ (eV)
MoO ₃ [Meyer 2012]	3	6.9	6.7
WO ₃ [Meyer 2012]	3.3	6.7	6.5
V ₂ O ₅ [Meyer 2012]	2.8	7	6.7
NiO [Greiner 2012]	3.1	6.3	3.5

6.2 Experimental

We describe here the experimental procedure used for processing SHJ solar cells with TMO-based hole collector. We used the same process sequence than previously used by Battaglia *et al.* [Battaglia 2014a] In our study, the Octopus I PECVD reactor was used for the deposition of the a-Si:H(*i*) passivation layers as well as for the a-Si:H(*n*) electron collector. After PECVD, the cells were immediately transferred to the Leybold thermal evaporator in order to prevent

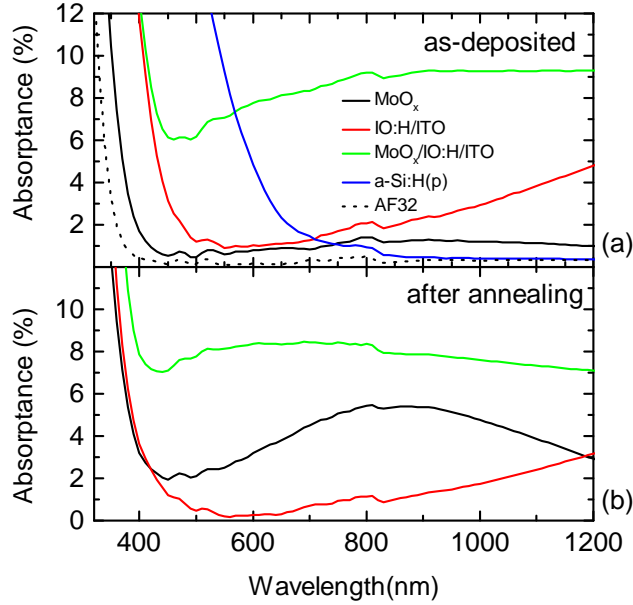


Figure 6.2: Optical absorbance of MoO_x films and IO:H/ITO bilayers deposited separately or sequentially on AF32 glass (a) before and (b) after 200 °C annealing (in N_2 for 25 min). Absorbance spectra of a thin a-Si:H(*p*) film and of bare AF32 glass are given for reference. Reproduced with permission from [Geissbühler 2015]. Copyright 2015, AIP Publishing LLC.

native oxide formation on the a-Si:H(*i*) layer. Stoichiometric MoO_3 powder was used in a Mo boat for Joule effect evaporation. The evaporator was pumped down to a base pressure of $\approx 4 \times 10^{-6}$ mBar. A deposition rate between 0.3 Å/s and 1 Å/s was used to grow a ≈ 7 –10-nm-thick MoO_x film. The film thickness was then measured either by spectroscopic ellipsometry or by profilometer. To minimize the interaction of the deposited MoO_x film with the ambient atmosphere, the cells were immediately transferred to the MRC 603 sputtering system for the deposition of the IO:H/ITO bilayer as the front TCO. [Barraud 2013] Finally, after the deposition of the ITO/Ag stack to form the rear contact, the cells were metallized using either screen-printing or Cu-plated contacts.

6.3 Optical properties and films microstructure of MoO_x -based hole-collector

6.3.1 Annealing and TCO sputtering impact on MoO_x optical properties[†]

An important point with MoO_x films is their sensitivity to air and oxygen exposure, as well as to temperature or plasma treatments, which might impact solar cell performance.[Irfan 2012] To illustrate the influence of subsequent processing steps on the optical properties of the MoO_x layer, Fig. 6.2(a) shows the optical absorbance of device-relevant MoO_x and IO:H/ITO

6.3. Optical properties and films microstructure of MoO_x-based hole-collector

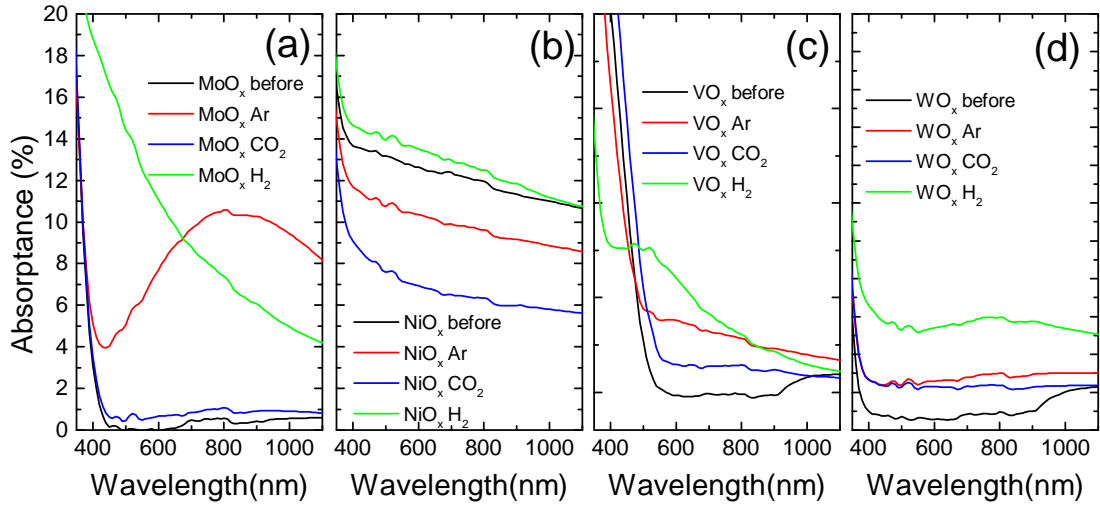


Figure 6.3: Optical absorbance in the as-deposited state and after Ar, H₂ or CO₂ plasma treatment carried out on: (a) MoO_x (b) NiO (c) VO_x (d) WO_x thin films.

films on glass prior to annealing, deposited either separately or sequentially (IO:H/ITO bilayer sputtered on MoO_x film). Absorbance spectra of a-Si:H(*p*) and of bare AF32 glass substrates are also provided for reference. In the as-deposited state [see panel (a)], as a result of its ≈ 3 eV bandgap, the MoO_x spectrum features a cut-off wavelength at 400 nm while the absorbance in the visible and IR ranges remains below 2%. The same graph also shows the absorbance of the IO:H/ITO bilayer (deposited at room temperature) used here as a highly transparent TCO. Surprisingly, when MoO_x is capped with this IO:H/ITO bilayer, the total absorbance is significantly higher than expected from the spectra of the individual layers.[Werner 2015] Increased absorbance of MoO_x is known to result from low-temperature annealing in N₂ atmosphere [see also Fig. 6.2(b)], which can be explained by an increase of oxygen vacancies in this material.[Lin 2009] [Wong 2012] In our case, sputtering takes place at a temperature below 50 °C and can therefore not explain these optical changes. Exposing our MoO_x films directly to a pure Ar plasma revealed that the increased absorbance is induced by both bombardment with energetic particles and by plasma UV luminescence, causing photochromism of MoO_x (see section 6.3.2).[Kim 2011] [He 2003] When subsequently annealed, changes in the optical properties of the MoO_x/TCO layer stack are due mainly to the crystallization of the TCO, as seen by the blue-shift of the cut-off and decreased free-carrier absorption in the IR.[Koida 2007] Additional investigations revealed that the nature of the annealing atmosphere (reducing or oxidizing) has no impact on the optical properties of the MoO_x/IO:H/ITO stack. We attribute this to the efficient capping provided by the TCO bilayer.[Barraud 2013]

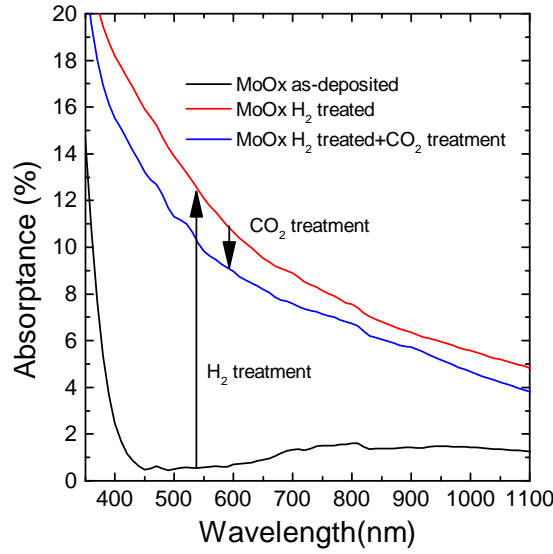


Figure 6.4: Optical absorbance of MoO_x thin film as-deposited, after a H₂ plasma treatment and after a subsequent CO₂ treatment.

6.3.2 Impact of plasma treatments on TMO thin films

Based on the high sensitivity previously observed of MoO_x film to Ar plasma, we further investigated the impact of reducing and oxidizing plasma treatments.² Furthermore, we extended this study to additional TMOs such as tungsten oxide (WO_x), nickel oxide (NiO_x) and vanadium oxide (VO_x). All films were deposited in the Leybold setup by thermal evaporation with thicknesses of ≈ 10 nm. CO₂ and H₂ plasma treatments were used in order to respectively oxidize or reduce the TMO thin films. In addition, pure Ar plasma treatments were as well carried out to simulate the TCO sputtering conditions while avoiding the deposition of any material. All treatments were made at room temperature for 5 min, at a pressure of 0.95 mBar and a power of 96 mW cm⁻². The optical absorbance was measured before and after the treatment with a spectrophotometer.

We see in Fig. 6.3(a) that the pure Ar plasma treatment induces a change in the MoO_x film absorbance spectra similar to that of the TCO sputtering as previously seen in Fig. 6.2. This demonstrates that the film modifications are induced mainly by the Ar bombardment and by the plasma luminescence rather than by the TCO deposition itself. [Kim 2011] [He 2003] Interestingly, when exposed to a hydrogen plasma, a significantly different spectrum was recorded with a higher absorbance at low wavelengths. This may be attributed to the reduction of MoO_x to another oxidation state such as possibly metallic Mo. [Kim 2008] Conversely, the CO₂ plasma has a weak impact on the absorbance spectra despite the ion bombardment and luminescence experienced during this plasma treatment. This can be explained by a reversed effect of the oxygen ions keeping the film closer to the MoO₃ stoichiometry. [Tracy 1986]

²The results presented here were obtained with the help of J. Werner. Contributions are gratefully acknowledged.

6.3. Optical properties and films microstructure of MoO_x-based hole-collector

Nickel oxide (NiO) is an interesting p-type TMO with a high WF.[Sato 1993] In our case, the as-deposited film exhibits an unexpectedly high absorptance indicating that the deposition parameters used here lead to a film that is highly substoichiometric. This is further evidenced by the significant impact of the CO₂ plasma to further oxidize the film. In this respect, plasma oxidations of metallic Ni films were already reported in the literature for the formation of NiO layers.[Wang 2010] However, due to the poor optical properties of as-deposited NiO, this material was not further investigated in this thesis.

For VO_x, an significant blue-shift of the bandgap cut-off is observed after the H₂ plasma treatment. VO_x is known to present a variety of different intermediate oxides.[Porter 1972] However, due to the high cut-off of the as-deposited film located at ≈ 500 nm, this material was not further investigated either in this thesis.

Finally, the WO_x shows a relatively low sensitivity to plasma treatments. Both CO₂ and Ar plasma treatments increase its optical absorptance, likely due to the energetic particles of the plasma and to the photochromism of the WO_x film.[Kim 2011] [He 2007] Hence, among all TMOs investigated here, WO_x was found to be the most stable material with respect to plasma treatments and is thus an interesting candidate to form a transparent hole collector in SHJ solar cells. However, MoO_x was preferred to WO_x for the first investigations on the a-Si:H(*p*) replacement as this material was already successfully demonstrated for SHJs. [Battaglia 2014a] [Bivour 2015]

Reversibility of plasma-induced optical degradation

In order to study the extent to which CO₂ plasma treatment can be used to recover the initial oxidization state and the optical transparency of a TMO film after a plasma treatment, a MoO_x film was *successively* treated by a H₂ and by a CO₂ plasma, and characterized between treatments. This was motivated by the known ability of annealing in oxidizing atmospheres to "bleach" the MoO_x, previously degraded. Furthermore, it is known that once its optical properties are recovered, the MoO_x cannot be degraded again.[He 2003] Figure 6.4 shows the optical absorptance of the MoO_x film deposited on glass respectively in the as-deposited state and after the H₂ and CO₂ plasma treatments. According to previous observations of Fig. 6.3(a), the reduction of the MoO_x leads to an important increase of the absorptance in the blue part of the spectrum. However, we observed that the subsequent CO₂ plasma treatment can at least partially recover its optical properties. Further investigations will be necessary in order to determine whether such a degradation/recovery sequence may stabilize the MoO_x film prior to TCO sputtering.

6.3.3 Molybdenum oxide film microstructure and interfaces[†]

To further investigate the MoO_x/TCO interaction and its evolution during annealing, HR-TEM was carried out on mirror-polished c-Si samples, capped with a full a-Si:H(*i*) / MoO_x/IO:H/ITO

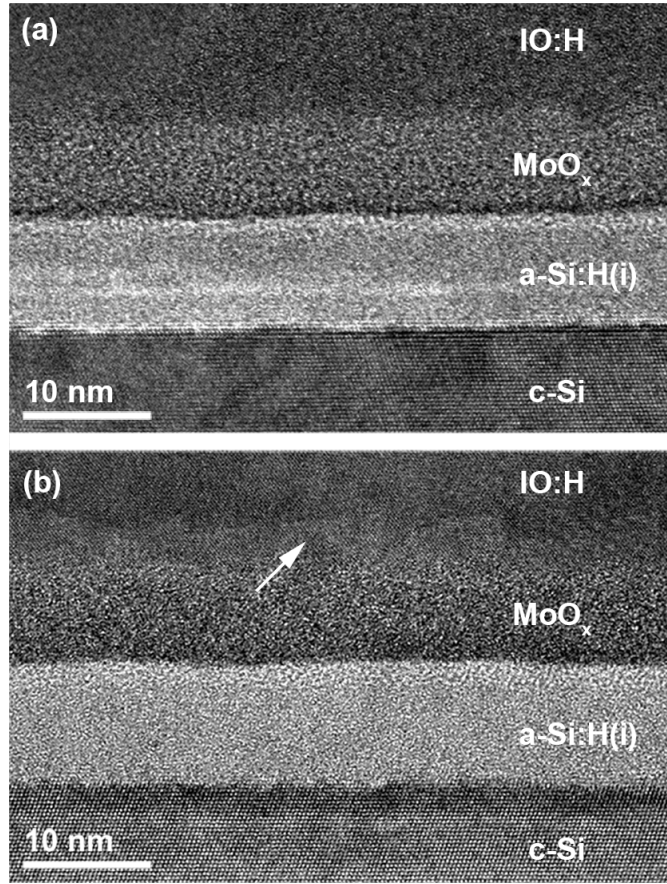


Figure 6.5: HR-TEM micrographs of the c-Si/a-Si:H(*i*)/MoO_x/IO:H interfaces for: (a) an as-deposited sample and (b) after annealing at 200 °C in N₂ for 25 min. Images are purposely defocused to increase the contrast of the MoO_x/IO:H interfacial layer. Reproduced with permission from [Geissbühler 2015]. Copyright 2015, AIP Publishing LLC.

contact stack. High-resolution transmission electron microscopy was carried out on selected samples using a FEI Osiris instrument. For this, cross-section samples were prepared using mechanical tripod polishing (Allied High Tech Multiprep) followed by low-energy Ar ion milling (Gatan PIPS). Figure 6.5(a) and (b) shows such a stack in its as-deposited and annealed states (25 min at 200°C in a N₂-purged oven), respectively. In both cases, an atomically sharp and defect-free c-Si/a-Si:H(*i*) interface is seen, required for high-quality surface passivation. [Geissbühler 2013] Similarly, the a-Si:H(*i*)/ MoO_x interface is clearly delimited. In contrast, the MoO_x/IO:H interface is less sharply resolved, suggesting the presence of a ≈ 1 –2-nm-thick intermixing layer induced by the sputtering process [Fig. 6.5(a)]. Panel (b) indicates that, during annealing, the presence of this intermixing layer becomes more pronounced and reaches a thickness of 5–7 nm with the occurrence of epitaxial nano-grains on the IO:H lattice [Fig. 6.5(b), indicated by the white arrow].

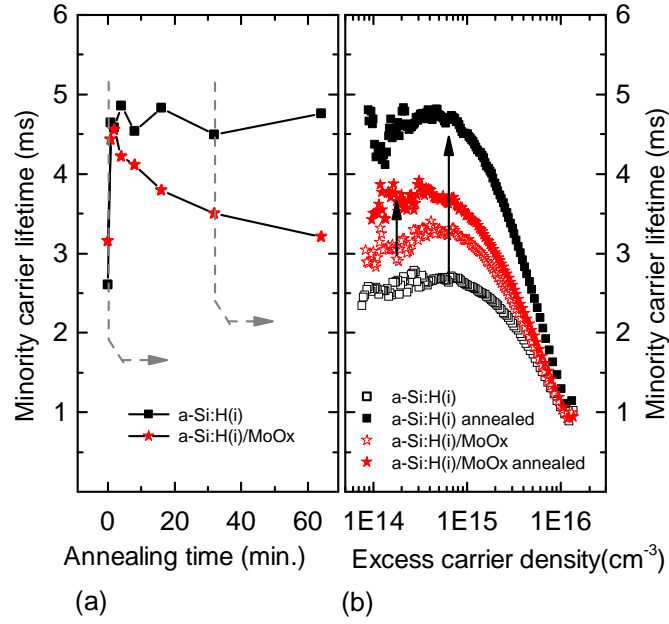


Figure 6.6: (a) Minority-carrier lifetime at an injection level of 10^{15} cm^{-3} as a function of the sample annealing time. (b) Minority-carrier lifetime curves in function of the injection level before and after 32 min of annealing. Reproduced with permission from [Geissbühler 2015]. Copyright 2015, AIP Publishing LLC.

6.4 Surface passivation of a-Si:H(i)/ MoO_x hole collector and impact of annealing

6.4.1 Annealing impact on un-capped MoO_x hole collector[†]

As previously seen, annealing has an important impact on the MoO_x film properties. Here, we investigate the impact of the presence of the MoO_x layer and the subsequent annealing on the passivation properties of the a-Si:H(i) buffer layer. For this, we evaluated the τ_{eff} of the silicon wafer by transient photoconductance measurements (Sinton Instruments, WCT-120) which gives direct information on the surface passivation quality. [Sinton 1996] [Nagel 1999] Figure 6.6(a) shows τ_{eff} (at a carrier injection level of 10^{15} cm^{-3}) as a function of the annealing time (at 200 °C in a N₂ environment). Both passivation samples (with and without MoO_x overlayer) increase their τ_{eff} within the first minutes of annealing, which is explained by a reorganization of the passivating film's microstructure. [De Wolf 2008] [El Mhamdi 2014] However, for longer annealing, τ_{eff} slightly decays for the MoO_x sample. Similar annealing effects were observed in the past when capping a-Si:H(i) buffer layers with p-type a-Si:H films, which was explained by Fermi-level induced native defect generation in the passivating films. [De Wolf 2009] Here, the magnitude of this effect remains modest, as seen in Fig. 6.6 (b), where τ_{eff} is increased for all injection levels excluding any negative effect on device performance.

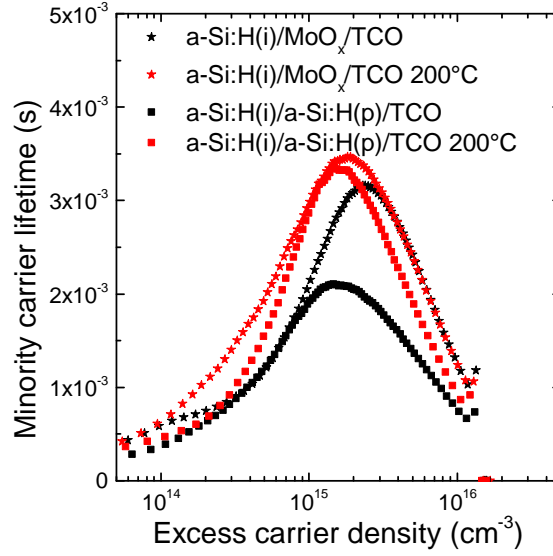


Figure 6.7: Minority-carrier lifetime curve as a function of the excess-carrier density for lifetime samples featuring either a MoO_x or an a-Si:H(*p*) hole collector.

6.4.2 Annealing impact on TCO-capped MoO_x hole collector

Motivated by the occurrence of the interlayer at the MoO_x/TCO interface as evidenced by HR-TEM in Fig. 6.5(b), the impact of annealing on the passivation of *TCO-capped* MoO_x lifetime samples was investigated as well. In this respect, lifetime samples consisting of an a-Si:H(*ip*)/IO:H/ITO or an a-Si:H(*i*)/ MoO_x /IO:H/ITO front stack were processed. At the rear side, both lifetime samples have an a-Si:H(*in*) stack un-capped by the TCO. Samples were annealed at 200 °C in a N_2 environment and τ_{eff} was measured after different annealing durations. Figure 6.7 shows the minority-carrier lifetime curves of both MoO_x and a-Si:H(*p*) samples in the as-deposited state as well as after 36 min of annealing. As already reported in the literature for an a-Si:H(*p*) hole collector, the TCO deposition modifies the minority-carrier lifetime curve both by the damages induced during the sputtering and by a tailing of the curve at low injection due to the WF mismatch between the a-Si:H(*p*) and the TCO. [Demaurex 2012] [Demaurex 2014a] [Bivour 2014]. Interestingly, such tailing is similarly experienced for the MoO_x film and can be explained by the lower TCO WF ($\approx 4\text{--}5$ eV for ITO [Centurioni 2003]) compared to the MoO_x WF, reducing therefore the inversion layer in the amorphous/crystalline Si interface vicinity and thus increasing recombination in this region. When annealed, both MoO_x and a-Si:H(*p*) lifetime samples behave similarly and show an increase of τ_{eff} as previously observed for un-capped lifetime samples. Therefore—as in the un-capped case—annealing of MoO_x films with TCO overlayers has no detrimental consequences from the passivation point of view.

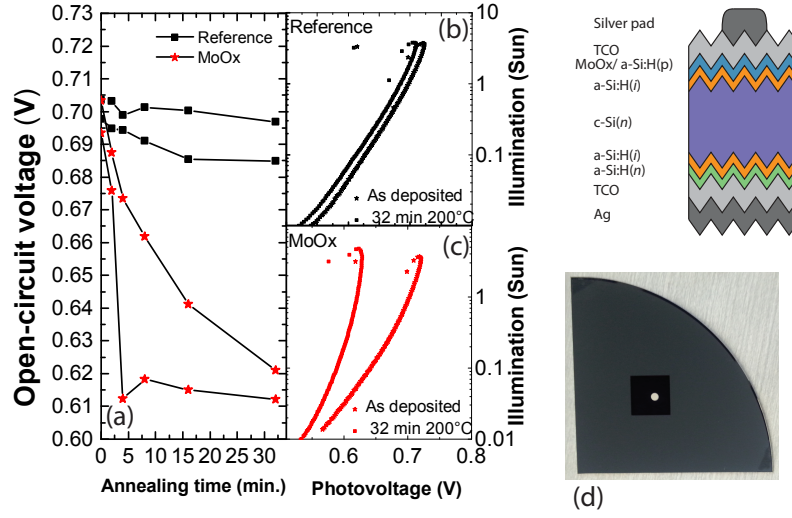


Figure 6.8: (a) V_{OC} at one sun for Sun V_{OC} test devices featuring either a MoO_x or an a-Si:H(p) hole collector. Illumination vs V_{OC} curve before and after 32 min of annealing at 200 °C for (b) an a-Si:H(p) hole collector and (c) a MoO_x hole collector (d) Schematic and photography of the test device considered here.

6.4.3 Annealing impact on the open-circuit voltage

To verify that the annealing at 200 °C has no impact on the V_{OC} as suggested by the findings of section 6.4.2, where τ_{eff} and thus the *implied* V_{OC} are preserved, Sun V_{OC} samples were processed with the structure shown in Fig. 6.8(d) with either a MoO_x or an a-Si:H(p) hole collector. These devices consist of 1-cm² solar cells with a central sputtered silver dot to avoid voltage measurement artifacts occurring when directly probing the TCO with the Sun V_{OC} probe. Contrary to the τ_{eff} improvements previously observed, the measured V_{OC} dramatically decays for the MoO_x samples with the annealing. A verification of the V_{OC} was made at the end of the annealing sequence under continuous illumination of the light $J-V$ setup. The ≈ 90 mV drop was confirmed excluding therefore a measurement artifact due to potential capacitive effect. As displayed in Fig. 6.8(c), the illumination- V_{OC} curve is dramatically modified after 32 min of annealing for the MoO_x sample, indicating the possible occurrence of a reversed diode counteracting the V_{OC} of the device. [Sinton 2000] [Glunz 2007] [Bivour 2015]

6.5 Molybdenum oxide based SHJ solar cells

6.5.1 Impact of the annealing on the device performance[†]

To investigate the impact of annealing on device level, we fabricated solar cells featuring either MoO_x or standard a-Si:H(p) hole extraction layers. The cells were metallized by using screen-printing, followed by annealing at the lowest possible temperature to evaporate the solvents contained within the silver paste. This pre-drying is mandatory to obtain a reasonable

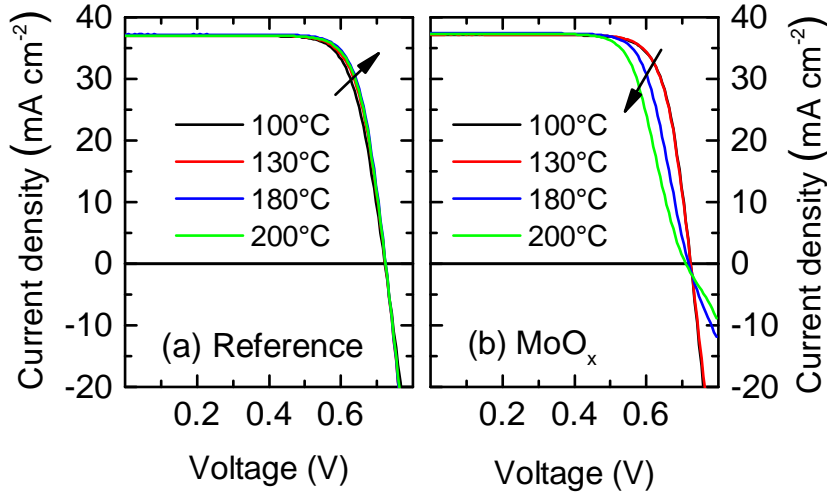


Figure 6.9: Light J - V characteristics of (a) reference and (b) MoO_x -based SHJ solar cells after post-processing annealing at various temperatures. Measurements were taken at room temperature. Reproduced with permission from [Geissbühler 2015]. Copyright 2015, AIP Publishing LLC.

electrical conductivity and mechanical stability and was carried at 100 °C for 25 min (instead of the typically used 200 °C for 25 min). Once finished, the cells were subsequently annealed at 130 °C, 180 °C and 200 °C in steps of 15 min. For the reference cell, Fig. 6.9(a) confirms that increasing the annealing temperature up to 200 °C improves the device performance (FF improves from 75.4% to 77.1%), linked to the improved metal conductivity as well as to improved passivation (seen also in Fig. 6.6). [Demaurex 2012] In contrast to this, Fig. 6.9(b) shows that annealing above 130 °C dramatically deteriorates the performances of our MoO_x -based cell. The J - V characteristics become S-shaped (FF deteriorates from 76.6% to 69.7%), strongly suggesting the appearance of a hole-blocking barrier. A possible cause for this barrier is the MoO_x /TCO interlayer discussed earlier, which thickens with annealing. However, a complete characterization of the interlayer film composition remains necessary to fully establish this view. The occurrence of the S-shaped curves was found to be independent of the annealing ambient (air or N_2 -purged, data not shown). Hence, processing above 130 °C temperature must be avoided to preserve efficient hole collection. In addition, we note that the J_{sc} remains unchanged after annealing as the decreased absorptance in the 650–1200 nm range is counterbalanced by losses in the 400–650 nm range accordingly to Fig. 6.2.

6.5.2 Impact of a-Si:H(*i*) layer thickness on hole collection in MoO_x -based SHJ solar cells

The occurrence of S-shaped J - V curves induced by the post-deposition annealing was investigated as a function of the a-Si:H(*i*) passivation thickness on the hole-collector side. Four different thicknesses ranging from 0.5 to 1.4 times the nominal thickness were deposited.

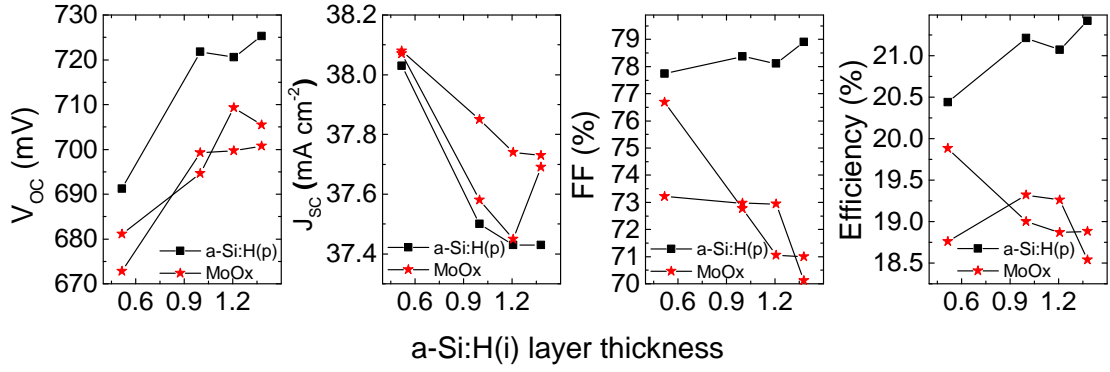


Figure 6.10: Impact of the a-Si:H(*i*) layer thickness on the : (a) V_{oc} (b) J_{sc} (c) FF and (d) cell efficiency.

Samples were then cleaved in two parts to respectively deposit either a MoO_x or an a-Si:H(*p*) hole collector for the reference device. For each a-Si:H(*i*) layer thickness, one cell for the reference and two cells for the MoO_x were processed. Finally, the cells were contacted with the TCO layers as described in section 6.2 and screen-printed and annealed at a temperature of $\approx 170^\circ\text{C}$.

The J - V characteristics of MoO_x and a-Si:H(*p*) devices as a function of the a-Si:H(*i*) passivation thickness are displayed in Fig. 6.10. Starting with the nominal a-Si:H(*i*) passivation-layer thickness, relatively low FF values of $\approx 73\%$ are measured for the MoO_x device due the S-shaped J - V curve. It is then clearly seen in Fig. 6.10(c) that increasingly thick a-Si:H(*i*) layers lead to more S-shaped J - V curves resulting in a lower FF . Recently, Bivour *et al.* observed as well a negative impact of cell annealing on hole collection, similar to what we described in section 6.5.1. They attributed the latter effect to a decay of the MoO_x WF induced by the annealing, thus reducing the carrier selectivity of the contact. In our case, increasing the a-Si:H(*i*) layer thickness may be seen as further decoupling the MoO_x hole collector from the c-Si thus explaining the lower electrical performances for thick layers. Unfortunately, although thinner a-Si:H(*i*) layers can overcome the MoO_x WF decay, they induce as well a significant loss in V_{oc} due to lower surface passivation.

6.5.3 Comparison of MoO_x- and a-Si:H(*p*)-based SHJ device performance[†]

We now directly compare the MoO_x-based and reference devices. Figure 6.11 shows both cell structures featuring identical TCO layers (IO:H/ITO bilayer), but annealed at their respective optimal conditions (namely, 100°C for the MoO_x-based cell and 200°C for the reference device). Focusing on the solar-spectrum integrated EQE curves, we see a substantial gain of 0.88 mA cm^{-2} in the 310–610 nm wavelength range for the MoO_x-based device. However, this gain is partially lost by parasitic light absorption, caused by the MoO_x/TCO interaction, and by the lower optical transparency of non-cured IO:H/ITO films (Fig. 6.2). At 800 nm, the EQE of the MoO_x-based cell is 2% absolute lower than its reference counterpart. This

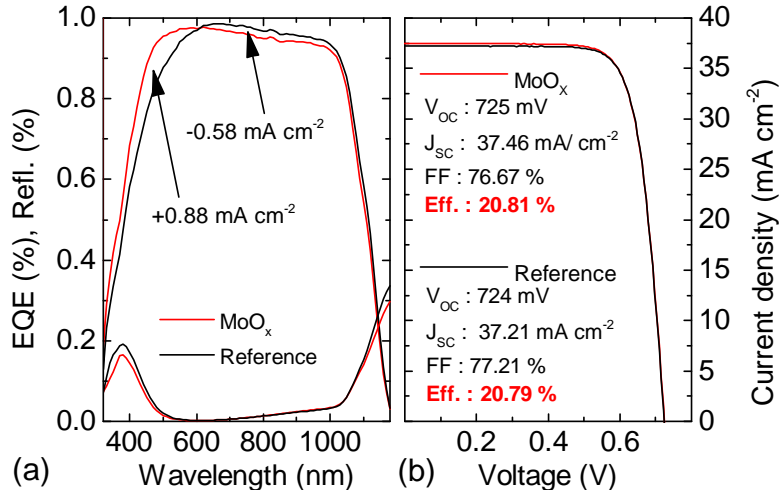


Figure 6.11: (a) EQE and (b) light J - V characteristic of MoO_x-based and a-Si:H(p) reference SHJ solar cells with adapted silver paste curing temperature. Reproduced with permission from [Geissbühler 2015]. Copyright 2015, AIP Publishing LLC.

difference is actually smaller than expected from the data in Fig. 6.2, which can be explained by the 1.7-times-thinner layers in our devices, compared to test structures shown in Fig. 6.2. These detrimental effects lead to a 0.58 mA cm^{-2} loss for wavelengths above 610 nm. We note that despite different refractive indices, both a-Si:H(p) and MoO_x devices present similar reflectance characteristics. [Liu 2014] This was confirmed by optical simulations in which only a $\approx 1\%$ difference was obtained due to the extremely thin films considered here. Consequently, the illuminated J - V curve of the MoO_x-based cell shows a $\approx 0.3 \text{ mA cm}^{-2}$ total gain in J_{sc} .

6.5.4 Temperature dependence of the efficiency for MoO_x-based SHJ devices

In the device reported by Battaglia *et al.*, the hole collection issue resulting in a S-shaped J - V curve was found to be less pronounced when the cell was operated at higher temperature ($\approx 60^\circ\text{C}$). This resulted in a positive FF temperature coefficient and in an impressively low efficiency temperature coefficient of $\approx 0.1 \frac{\%}{^\circ\text{C}}$. [Battaglia 2014a] The latter behavior was as well reported for a-SiO_x devices in which the barrier resulting from an increased valence band offset is more efficiently overcome by thermionic emission at higher operating temperatures. [Seif 2014] As seen in section 6.5.3, the S-shaped J - V curve can be avoided in MoO_x devices by carefully engineered processes. Hence, to evaluate the temperature coefficient of a well-behaving MoO_x-based SHJ cell, temperature dependent measurements were carried out by using the Peltier-regulated stage of the light J - V setup (section 2.4.2). Figure 6.12 (a)-(d) shows respectively the V_{oc} the J_{sc} the FF and the cell efficiency as a function of the operating temperature for both a MoO_x and an a-Si:H(p)-reference solar cell. Interestingly, a similar trend is observed between the MoO_x and the a-Si:H(p) devices for all parameters: In panel (a), the V_{oc} is governed by the temperature dependency of the intrinsic carrier concentration. [Taguchi 2008] [Seif 2015b] Conversely, the bandgap narrowing induced by increasing the

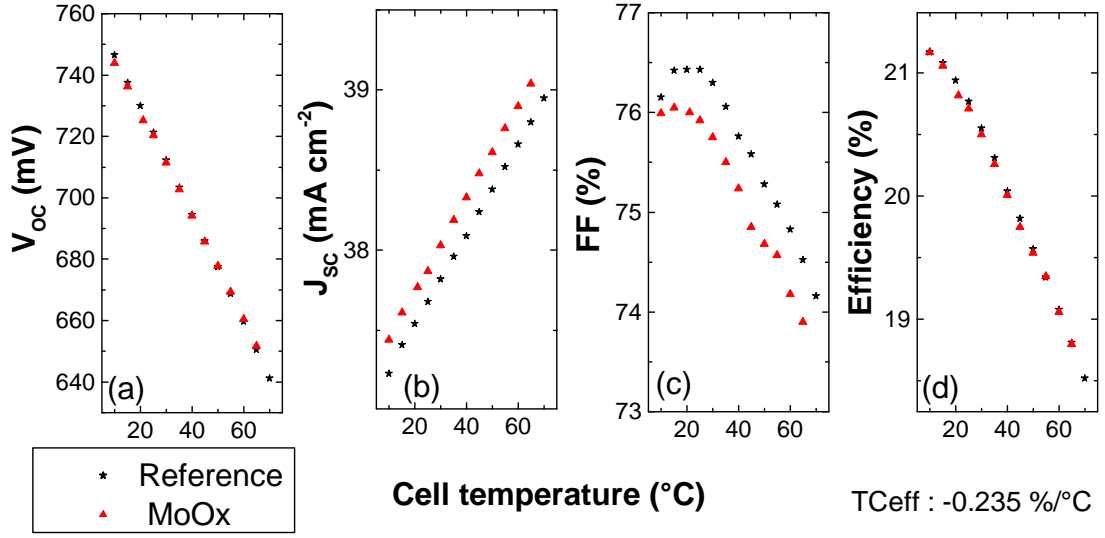


Figure 6.12: T-dependence of the: (a) V_{oc} (b) J_{sc} (c) FF (d) cell efficiency for both MoO_x - and a-Si:H(*p*)-based devices.

temperature has, as expected, a positive impact on the J_{sc} as shown in Fig. 6.12 (b). As the implied voltage is reduced for any injection level, this results in a FF decay. As a consequence, the efficiency for both the MoO_x and the a-Si:H(*p*)-reference solar cells shows an efficiency temperature coefficient of $-0.235 \frac{\%}{^\circ\text{C}}$. This demonstrates that MoO_x can be an efficient hole collector for the entire operating temperature range.

6.6 Alternative TCOs for MoO_x hole collector

In this section, we discuss alternative TCOs to replace the IO:H/ITO bilayer used so far to contact the MoO_x hole collector. Indeed, as the IO:H deposition relies on a partial water vapor pressure during the deposition, its processing remains more complex than for other TCOs. Furthermore, as previously seen in section 6.3.1, the IO:H/ITO bilayer has relatively poor optical properties when not annealed. This represents a second motivation for its replacement by a TCO that does not rely on a post-deposition annealing to tune its electrical and optical properties. [Morales-Masis 2015] In this respect, two different approaches based on LPCVD ZnO:B, or sputtered IZO were tested.

6.6.1 LPCVD ZnO:B as MoO_x hole-collector contact

As seen in sections 6.3.1 and 6.3.2, MoO_x film presents a high sensitivity to plasma soaking due to both its photochromism and its sensitivity to ion bombardment. [He 2003] [Kim 2011]. Thus LPCVD ZnO:B—as presented in section 3.7 as a front TCO—is an interesting candidate for IO:H replacement as this technique does not rely on a plasma process for the TCO deposition.

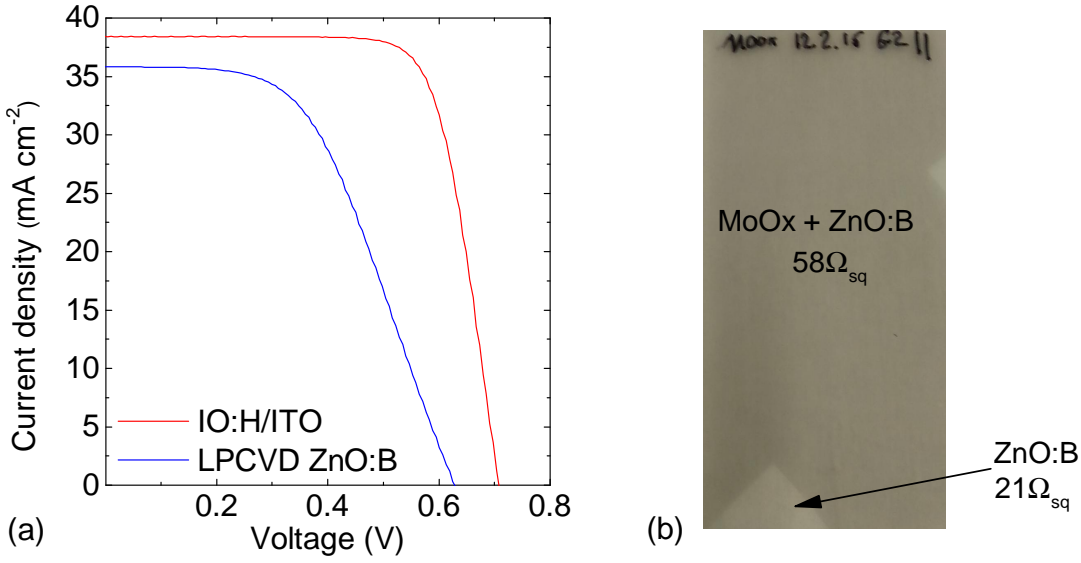


Figure 6.13: (a) Light J - V curves of MoO_x -based devices with either a LPCVD ZnO:B or an IO:H/ITO front-TCO (b) Glass with a $\text{MoO}_x/\text{ZnO:B}$ stack, the arrow points an area with no MoO_x .

In this study, a MoO_x cell precursor was made as described in section 6.2. Directly after the MoO_x deposition, a $\approx 2.2\text{-}\mu\text{m}$ -thick ZnO:B layer was deposited as the front TCO by LPCVD. The back electrode was realized with the standard sputtered ITO/Ag stack. Finally, the metallic front grid was made by screen-printing³ and the ZnO:B in between the 4-cm^2 cells was removed by using a 1:10 HCl solution while protecting the cells with a manually dispensed resist.

Figure 6.13 (a) shows the J - V curves of MoO_x -based devices with the ZnO:B front TCO as well as a reference with the standard IO:H/ITO front TCO. In accordance with the observations made in section 3.7, a lower J_{sc} is recorded for the ZnO:B cell due to a less efficient ARC. Importantly, the V_{oc} is dramatically reduced compared to the IO:H/ITO reference and the occurrence of a massive series resistance is observed. To further investigate the cause of this series resistance, the ZnO:B film was co-deposited on a glass with the same MoO_x film as the one deposited on the cell. During the MoO_x evaporation, some parts of the glass were covered resulting in area free of MoO_x . As shown in Fig. 6.13 (b), the $\text{MoO}_x/\text{ZnO:B}$ stack shows a grey color whereas the parts without MoO_x show the usual aspect of the LPCVD ZnO:B deposited alone. This clearly indicates a strong interaction between these two materials occurring during the growth of the ZnO:B film. This may be induced by a combination of the $\approx 180\text{ }^\circ\text{C}$ and the water vapor atmosphere undergone during the LPCVD deposition. [Pergament 2014] In addition, the sheet resistance of the stack was found to be ≈ 3 times higher than ZnO:B directly deposited on glass (either on the MoO_x -free parts or on a co-deposited sample). The reason for this dramatic modification of the ZnO:B electrical properties remains uncertain. Due to

³These cells are annealed at $\approx 190^\circ\text{C}$ which explains relatively low FF values for the reference cells ranging between 70 to 74 %

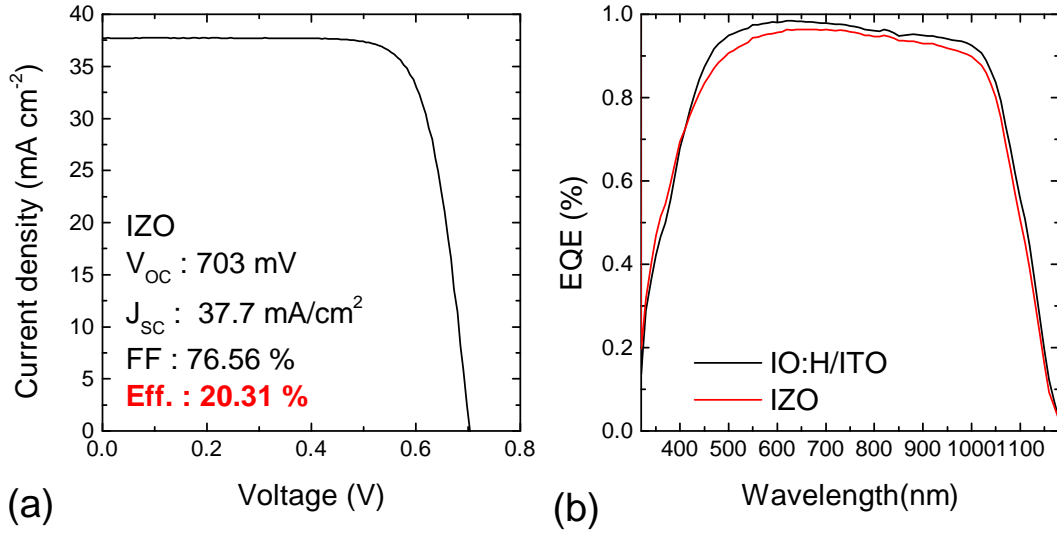


Figure 6.14: (a) J - V characteristic of MoO_x-based devices with IZO front TCO (b) Comparison of the EQE of MoO_x-based devices with either an IZO or an IO:H/ITO front TCO

the important difference in film thickness (≈ 7 nm for the MoO_x compared to ≈ 2.2 μ m for the ZnO:B), we may argue that chemical intermixing is excluded to be the cause of the higher sheet resistance. However, the MoO_x film may significantly change the nucleation of ZnO:B crystals during the LPCVD growth and may lead to the occurrence of vertical cracks thus increasing the film sheet resistance. [Ding 2011] [Ding 2013b] However, no evidence of such cracks was found by SEM observations.

As a consequence of the results shown here, LPCVD ZnO:B was not further investigated to contact the MoO_x hole collector.

6.6.2 Sputtered IZO as MoO_x hole collector contact

Another alternative material to contact the MoO_x film is sputtered IZO. Although this TCO relies on a plasma deposition, it can be deposited at a low power density likely reducing the impact on the MoO_x optical properties. In addition, this amorphous TCO has a mobility of up to $\approx 60 \frac{\text{cm}^2}{\text{Vs}}$ in the as-deposited state and therefore does not require any post-deposition annealing contrary to IO:H. [Morales-Masis 2015] Furthermore, the use of IZO was already successfully demonstrated to contact MoO_x films in perovskite solar cells. [Werner 2015]

In this study, we used an IZO front TCO sputtered in a Leybold Univex 450B system with a target composition of 90wt% In₂O₃ and 10wt% ZnO on a cell precursor prepared as described in section 6.2. Finally the cell was metallized by using an electrodeposited Cu front grid as described in sections 3.6 and 6.7.1.

Figure 6.13 (a) shows the J - V curve of the MoO_x-based device with the IZO front TCO and

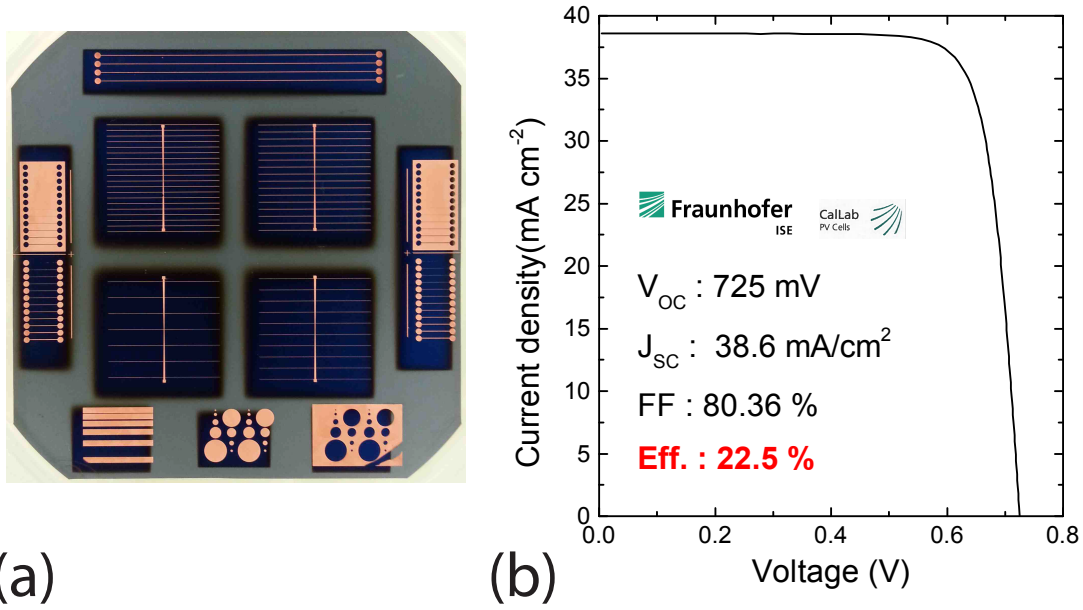


Figure 6.15: (a) Photograph of a Cu-plated MoO_x wafer with four 4-cm² cells with various finger pitches. (b) Light *J-V* characteristic of MoO_x-based SHJ solar cells with Cu electrodeposited front grid (certified by the Fraunhofer ISE CalLab). Reproduced with permission from [Geissbühler 2015]. Copyright 2015, AIP Publishing LLC.

the Cu-plated front grid. We observe an unusually low V_{oc} of 703 mV. This lower V_{oc} may be explained by the damages to the passivation induced during the sputtering as the recipe used here was not specifically optimized for SHJ solar cells and relies on a long deposition time above 40 min. [Demaurex 2012] Interestingly, the J_{sc} remains relatively modest compared to the IO:H/ITO reference with a difference of $\approx 1 \text{ mA cm}^{-2}$. As seen in the EQE displayed in Fig. 6.14(b), a lower response of the IZO cell is recorded for the entire spectrum which may point to a stronger interaction of the MoO_x layer with the IZO than previously observed for IO:H in Fig. 6.2. However a complete optical study may be necessary to confirm the latter statement. Finally, a well-behaving *J-V* curve is observed excluding the presence of hole-collection issues and leading to a *FF* of 76.6% and a cell efficiency of 20.3%. This demonstrates the potential of IZO as the front TCO for MoO_x-based devices if the deposition recipe is further optimized for this cell architecture.

6.7 High-FF and -efficiency Molybdenum oxide-based devices

6.7.1 22.5% certified efficiency MoO_x solar cell[†]

We discuss here how the thermal processing limitation for these devices does not exclude ultimate device performance. In this context, a significant improvement can be achieved by replacing the Ag-printed metallization by Cu electrodeposition, not requiring any thermal

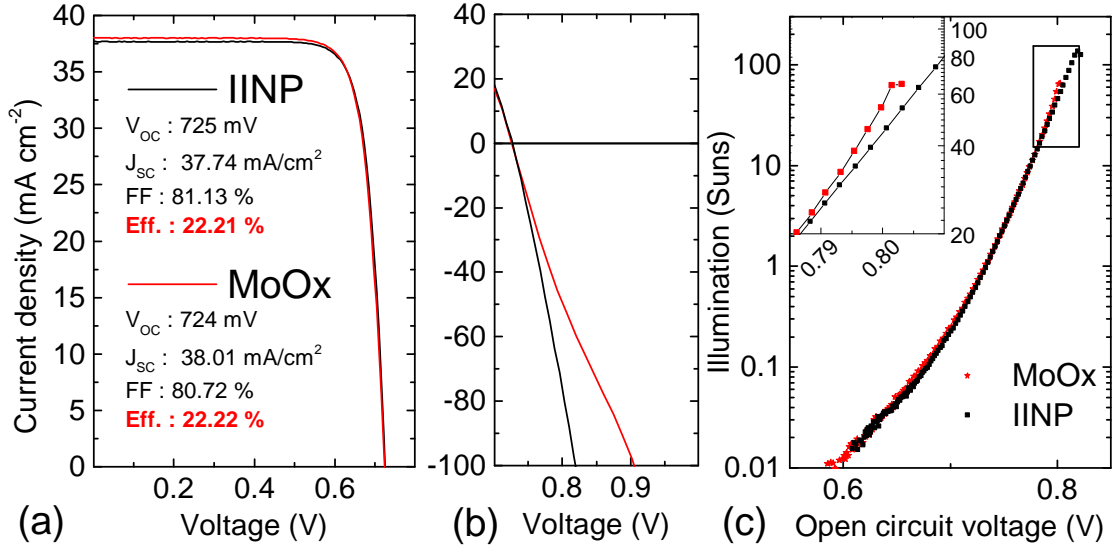


Figure 6.16: (a) Comparison of the J - V curves for both a MoO_x - and an $\text{a-Si:H}(p)$ -based cells with Cu plated contacts (b) Behavior of the J - V curves of the cells displayed in (a) in the forward polarization (c) Suns V_{oc} comparison of the cells shown in (a). The inset shows a magnification of the 20–100 Suns range.

treatment (see Chap. 3). Furthermore, this process reduces substantially the finger width ($20 \mu\text{m}$, compared to $70\text{--}80 \mu\text{m}$ for screen-printing), reducing optical shadowing from 5–7% down to 2–3% while increasing the number of fingers from 9 to 20.[Geissbuhler 2014] To test this in MoO_x -based devices, we first deposited a $\approx 30\text{-nm}$ -thick Cu seed layer on the front TCO by thermal evaporation (Leybold Vacuum) which was selectively masked by a photolithographically patterned resist. In the unmasked areas the Cu was then thickened by electrodeposition at room temperature, in a home-built system using a Cu sulfate electrolyte. Finally, after photoresist removal, the seed layer between the fingers was removed in 1 min. in a basic Cu etchant at room temperature.[Geissbuhler 2014] [Mulligan 2011] Using this modified metallization scheme, the FF of the finished device is significantly increased to 80.36%, as can be deduced from the illuminated J - V characteristics given in Fig. 6.15 (b). This is explained by a lower line resistivity in the Cu electrodeposited front grid compared to the screen-printed cells previously presented in section 6.5.1⁴, corresponding to a reduction in series resistance from $1.62 \Omega \text{ cm}^2$ to $0.83 \Omega \text{ cm}^2$. Moreover, the overall front-grid shadowing is reduced compared to screen-printed cell, resulting in an additional J_{sc} gain.[Geissbuhler 2014] With these FF and J_{sc} improvements, while maintaining a similar V_{oc} , we obtained an energy-conversion efficiency of 22.5% for a 4 cm^2 solar cell certified by the Fraunhofer ISE CalLab (Fig. 6.15 (b)).

6.7.2 *J-V* curve behavior in forward polarization

In this section, we further characterize the record-efficiency MoO_x-based cell in forward polarization. An a-Si:H(*p*) reference cell was processed with the same a-Si:H(*i*), a-Si:H(*n*), TCO layers and the front Cu-plated metallization. We note that—identical to the MoO_x cell—the reference was not annealed before the metallization. It can be seen in Fig. 6.16 (a) that an outstanding *FF* of 81.1% was obtained for the reference cell. When compared to the MoO_x device, the relatively small difference in the *J*_{sc} is explained by a slightly different front grid causing more shadowing in the MoO_x cell. Despite a well-behaving *J-V* curve in the quadrant where power is delivered, a singularity appears when the cell is operated in forward polarization. At polarization above 0.8 V, the cell becomes significantly S-shaped (see Fig. 6.16 (b)). Figure 6.16 (c) shows the illuminations vs *V*_{oc} curves measured by SunV_{OC}. It can be observed that at high injection—in the 20 to 100 Suns range, as seen in the inset of Fig. 6.16 (c)—a slightly more bent SunV_{OC} curve is measured for the MoO_x device. This deviation is consistent with the light *J-V* curve in forward polarization shown in panel (b) as the separation of the curves appears at the same voltage. This can be compared to the SunV_{OC} experiment shown in section 6.4.3 where it was evidenced that annealing leads to the occurrence of a reverse Schottky diode counter-acting the cell voltage at high injection. Importantly, we can conclude that this parasitic Schottky diode is already present in un-annealed devices. The annealing then modifies its characteristics due to the MoO_x WF reduction and finally results to a shift of the S-shape toward lower voltages. Further investigations are needed to assess the origin of this reverse Schottky diode.

6.8 General conclusions metal oxide films as a-Si:H(*p*) replacement

Our conclusions on the a-Si:H(*p*) hole-collector replacement by highly transparent TMO and more particularly by a ≈ 7-nm-thick MoO_x layer are as follows: The processes involved in the SHJ fabrication such as the TCO sputtering and the final annealing made after the screen-printing have an important impact on the optical properties of the MoO_x film. According to the literature, MoO_x films show an important photochromism effect and a high sensitivity to ion bombardment occurring during the TCO sputtering, resulting in the end in a parasitic optical absorptance. Further investigations on the plasma impact on MoO_x films revealed the possibility to recover at least partially the initial optical properties by using an oxidizing plasma. HR-TEM images of the film microstructure and its interfaces revealed the formation of an ≈ 5–7 nm-thick interlayer at the MoO_x/IO:H interface thickened during the final cell annealing. Based on this previous observation, we investigated as well the annealing impact on the surface passivation for both TCO-capped and un-capped samples and demonstrated that the previously experienced film modifications have no significant consequences on the surface passivation. However, investigations carried on SunV_{OC} test devices revealed the formation of an important reverse diode triggered by the cell annealing. In this respect, MoO_x SHJ solar cells were successively annealed at different temperatures and the occurrence of an S-

⁴i.e. Silver paste cured at 100°C.

shaped J - V curve was observed for temperatures above 130 °C. Hence, by carefully optimizing the processes and by avoiding annealing above 130°C, we demonstrated FF and cell efficiency similar to standard a-Si:H(*p*)-based SHJ devices with a clearly improved response in the blue part of the solar spectrum. However, the IO:H optical properties are significantly lower due to the reduced annealing temperature. As a direct consequence of the latter phenomenon and with in addition the parasitic optical losses induced by the TCO sputtering, a J_{sc} loss of ≈ 0.6 mA cm⁻² is observed in the 610–1200 nm wavelength range. Therefore, the development of a new TCO is crucial for further increasing the cell efficiency. For this, alternatives to IO:H front TCO were tested in order to simplify this process step. LPCVD ZnO:B was found to be incompatible with the MoO_x layer, however IZO demonstrated interesting preliminary results. Taking advantage of the fact that a Cu-plated front grid does not rely on any annealing for its formation, we successfully integrated this metallization in a MoO_x-based cell and demonstrated a 22.5% certified efficiency with a remarkable FF of above 80%.

7 Conclusions and perspectives

This chapter presents a general conclusion of the work realized during this thesis. First, we present a summary of the device performances of the different SHJ structures addressed during this work. Then, these architectures are discussed and compared to each other with respect to their potential improvements in light management, electrical performance and their possible industrialization. Finally, we discuss the perspectives for further increasing cell efficiency by merging the different outcomes of this thesis with other structures developed beyond this work.

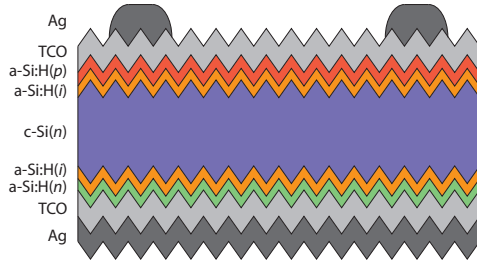
7.1 Conclusions

Four principal device architectures were investigated during this thesis:

- **Standard SHJ solar cells** made with regular a-Si:H and TCO layers and metallized by Ag paste screen-printing. They can be realized with the hole collector at the front or at the rear side of the cell (FHC or RHC).
- **Cu-plated front-grid SHJ solar cells** made with the standard SHJ structure metallized by Cu electroplating for the front grid. These cells can either feature the standard TCOs (ITO or IO:H) or more specific materials such IZO or LPCVD ZnO:B.
- **LEP-SHJ solar cells** where the front contact is localized allowing the decoupling of the electronic and optical properties of the window layers. These devices can be made in the FHC or RHC configuration. The patterning of the front contact is done only on the front TCO or on the entire front doped a-Si:H/TCO stack.
- **TMO-based SHJ solar cells** where the front hole collector is realized by a highly transparent TMO film such as MoO_x. These devices can be metallized either by screen-printing or by Cu electroplating.

Chapter 7. Conclusions and perspectives

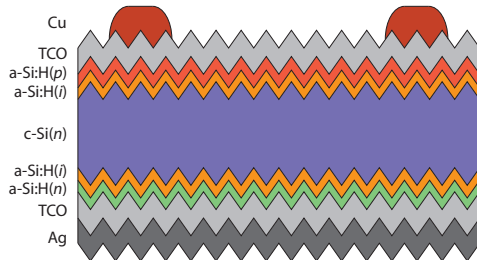
7.1.1 Device architecture performance summary



Standard SHJ devices

Cell	V_{oc} (mV)	J_{sc} (mA cm ⁻²)	FF (%)	Eff. (%)
FHC	725	37.4	78.9	21.4
Best EPFL device ^a	727	38.9	78.4	22.14
RHC	723	37.9	76.7	21

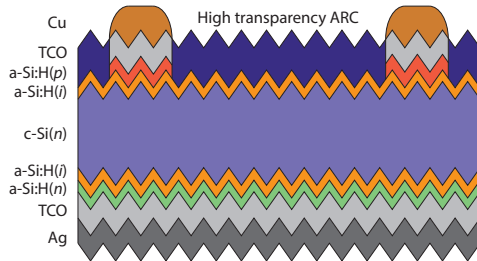
^aAchieved by [Descoedres 2013] and certified by Fraunhofer ISE Callab



SHJ devices with Cu-plated front grid

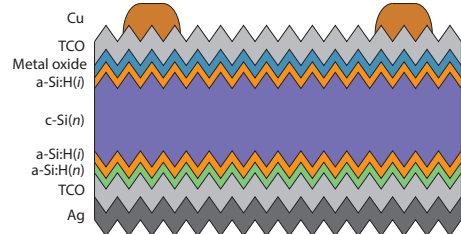
Cell	V_{oc} (mV)	J_{sc} (mA cm ⁻²)	FF (%)	Eff. (%)
IO:H/ITO	728	39.2	78.6	22.4
IO:H/ITO	724	37.74	81.1	22.2
IZO	727	39.4	77.9	22.3 ^a
LPCVD ZnO:B	714	37	76.1	20.1

^aCertified by Fraunhofer ISE Callab



LEP-SHJ devices

Cell	V_{oc} (mV)	J_{sc} (mA cm ⁻²)	FF (%)	Eff. (%)
TCO patt.	722	37.0	75.3	20.1
TCO/a-Si:H(n) patt.	705	35.0	69.6	17.2



MoO_x-based SHJ devices

Cell	V_{oc} (mV)	J_{sc} (mA cm ⁻²)	FF (%)	Eff. (%)
Ag front grid	725	37.5	76.7	20.8
Cu front grid	725	38.6	80.4	22.5 ^a

^aCertified by Fraunhofer ISE Callab

7.1.2 Light management

The four device architectures presented in section 7.1.1 all have the potential to improve the optical properties of SHJ cells by allowing a reduction in parasitic losses, although they address completely different strategies which may, in some cases, be applied together. Starting with standard SHJ cell structures, the RHC configuration was demonstrated to allow important degrees of freedom for the optimization of the window layers. Indeed, we showed that both the a-Si:H(*i*) and the a-Si:H(*n*) layer at the front can be thinned by a factor of 2 without significant variation of the *FF* or V_{oc} . Hence, a J_{sc} gain of up to 0.5 mA cm^{-2} can be realized with such optimized layer thicknesses. [Varache 2015] To further reduce parasitic light absorption in the a-Si:H window layers, two device structures were studied: First, LEP-SHJ cells were developed to create an area without the front doped a-Si:H layer and with a high-transparency front ARC. Although demonstrations of such devices were achieved, no outstanding J_{sc} gain was recorded due to the relatively high contact coverage still needed to efficiently extract the charge carriers and to the non-optimized alternative ARC films. In a second approach, the front a-Si:H(*p*) layer was replaced by a highly transparent MoO_x film. With this layer substitution, a massive gain of 0.88 mA cm^{-2} was achieved in the blue part of the solar spectrum. This gain was nevertheless partially mitigated by the parasitic absorption in the MoO_x film induced by the TCO sputtering on the MoO_x film and by the low optical performances of the uncured front TCO. Overall, this material allows a J_{sc} gain 0.3 mA cm^{-2} with the possibility for improvement by using a front TCO which does not rely on annealing for tuning its optical properties. Finally, the front metallization of SHJ devices by Cu electrodeposition demonstrated outstanding reduction of the shadow losses by decreasing the front-grid coverage from 7–6% to 3–2%. In our SHJ devices, this new metallization led directly to a J_{sc} gain of $\approx 1.1 \text{ mA cm}^{-2}$.

7.1.3 Electrical performance

The different device architectures summarized in section 7.1.1 enable as well potential V_{oc} and *FF* improvements. First, the RHC configuration was reported in the literature to benefit from a better lateral transport in the c-Si wafer. In our study, from an electrical performance point of view, no *FF* improvements were recorded, likely due to issues related to the small cell area. With LEP-SHJ devices, this structure was found to bring important *FF* losses mainly due to the localized contact when realized with the standard a-Si:H and TCO layers. These losses were nevertheless mitigated while keeping a sufficiently high contact coverage. However, with this last approach, the potential optical gain remains relatively small. A more reliable approach to improve the light management while keeping good electrical performance was brought by the MoO_x -based devices. Indeed, this material proved to be an efficient hole collector if processes above 130°C are avoided. This clearly prohibits the use of screen-printed Ag front metallization with a busbar design as the finger line resistance of the Ag paste cured at this temperature will be detrimental to the device's series resistance. However, other metallization schemes such as Cu electrodeposition allow for a highly conductive front grid while keeping the entire process below 100°C . By using this metallization on MoO_x -based SHJ cells, we

demonstrated a remarkable FF of 80.36% leading to a certified efficiency of 22.5%.

7.1.4 Manufacturing and industrialization

In addition to improving the light management and the electrical performance, another criterion for device sustainability is its ability to be easily processed and thus industrialized. This requires that the number of additional processing steps are minimized in order to maintain low production costs and reliable manufacturing. In this respect, the RHC structure enhances the device performance while keeping the same equipment and process sequence as used for FHC SHJ devices. For this reason, this cell configuration is nowadays often presented as being a better configuration than FHC cells from an industrialization point-of-view even though the RHC will be more sensitive to the material bulk lifetime. [Kobayashi 2013] [Watahiki 2015]

In the case of the advanced device structures proposed in this thesis, new processing steps are required for their manufacturing. Starting with the LEP-SHJ cells, we demonstrated that due to the high contact coverage needed to keep good electrical performance, two patterning steps are required. Thus, the process sequence becomes equivalently complex as for IBC-SHJ cells where higher efficiencies were already demonstrated making meaningless the realization of LEP-SHJ devices. [Paviet-Salomon 2015] [Masuko 2014] [Nakamura 2014] Nevertheless, if sufficiently low contact resistivity can be achieved, LEP-SHJ devices may then be made by using the front metallization as a mask for patterning the front a-Si:H(n) and TCO layers. For this purpose, we demonstrated that hydrogen plasma etching can achieve a-Si:H layer etching with an outstanding accuracy. Importantly, this technique enables us to selectively remove a doped a-Si:H layer while keeping the surface passivation pristine. This process, beyond its possible use for LEP-SHJ cells, may considerably simplify the IBC-SHJ process sequence by avoiding a second shadow mask and its alignment in respect to the first deposition. [Scherff 2011]

An important feature of MoO_x -based cells is that their process-sequence complexity is equivalent to standard a-Si:H(p)-based SHJ devices. From the manufacturing equipment perspective, the PECVD chamber dedicated to a-Si:H(p) has to be replaced by a MoO_x deposition tool relying either on thermal evaporation, sputtering or ALD deposition. [Macco 2015] For their front metallization, two approaches may be investigated: First, the smart-wire contacting technology can overcome the issue of the high line resistance induced by the low-temperature annealing. [Söderström 2013] [Faes 2014] Second, copper plating may be implemented with the advantage of entirely keeping the processing temperature below 100 °C. However, we note that the module lamination process takes usually place between 130 °C and 160 °C. [Li 2013] [Chen 2015] Therefore a more accurate determination of the upper temperature limit for MoO_x should be done in order to assess if this technology is compatible with the usual module manufacturing scheme.

From the industrialization point of view, the main limitation of this process—as presented in this thesis—is the photolithography patterning step that relies on expensive photoresist and long UV exposure and development time. In addition to the photolithography, the first plating

process proposed in this thesis and based on a nickel-copper stack introduces numerous additional steps compared to silver paste screen-printing and the use of two electrodeposition systems. However, with the second approach based on a copper seed layer investigated in this work, the nickel layer is replaced by the deposition of a thin copper seed layer possibly deposited directly after the front TCO in the same sputtering tool. An additional advantage of this process is the increased finger adhesion compared to the nickel-copper process, improving the reliability of the device. Finally, as shown in this work, copper plating is compatible with non-indium-based TCOs such as LPCVD ZnO:B, opening the possibility of manufacturing indium- and silver-free SHJ solar cells.

7.2 Perspectives

7.2.1 Standard SHJ devices

As previously discussed, the RHC structure is the "standard" SHJ device configuration having the largest potential for improvement. From the current state-of-the-art of RHC cells developed at PVLab, further optimizations of the a-Si:H(*in*) stack must be carried out to reach the best tradeoff between optical and electrical performances. Then, as suggested by Bivour *et al.*, careful tuning of the front-TCO properties may enable to further improve the cell efficiency.[Bivour 2014] In this work, important FF and V_{oc} deviations were recorded even for cells placed on the same wafer. This points out a possible negative impact of the 4 cm^2 cell design and is a motivation for investigating larger cell-size such as for instance a $6 \times 6\text{ cm}^2$ design. Importantly, as the a-Si:H(*ip*) stack is placed at the rear-side of the cell, this stack can be optimized regardless to its optical properties to provide the best surface passivation and the most efficient hole selective contact.[Holman 2012] Furthermore, as reported in literature, more freedom is as well experienced for the front-metallization design as the finger pitch can be increased allowing additional J_{sc} improvements. [Kobayashi 2013]

7.2.2 Electrodeposited metal front grid

An important perspective for the electrodeposited copper metallization is the simplification of this technique to become competitive with silver screen-printing. Based on the process developed during this thesis, the patterning by photolithography must be simplified. In this respect, several alternative techniques such as inkjet printing, pad-printing or screen-printing may be considered. [Hermans 2013] These techniques indeed avoid the complex photoresist dispensing, exposure and development. In combination with the copper-seed-layer based process, the number of additional processing steps is thus limited. As the finger adhesion was notably improved with the copper-seed-layer approach, a higher Cu deposition rate—which may lead to more internal stress within the finger—may be used without risking adhesion issues. Finally, copper electroplating must be adapted in order to metallize RHC cells with a copper seed-layer approach. This may be achieved while directly contacting the front side of

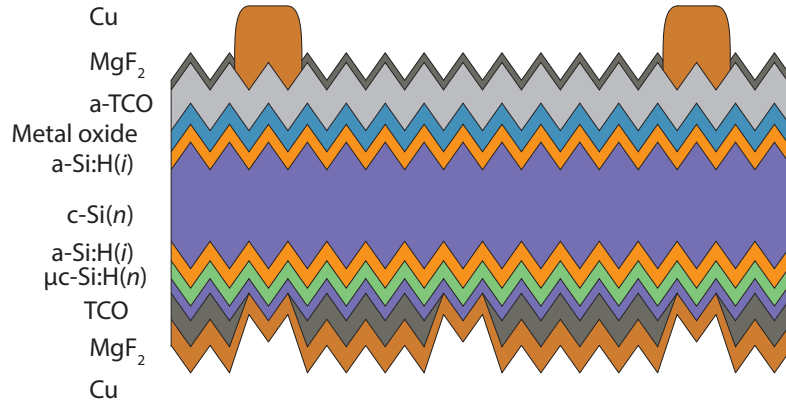


Figure 7.1: Schematic cross-section of the suggested device structure.

the device and maintaining a sufficiently thick seed layer to avoid inhomogeneous deposition due to voltage drop. A second approach may be, inversely, to thin down the seed layer so that it is sufficiently transparent to enable light-induced plating.

7.2.3 LEP-SHJ architecture

A necessary condition to make LEP-SHJ cells efficient is to reduce significantly the a-Si:H(*n*)/TCO specific contact resistivity. In this respect, alternative materials such as $\mu\text{c-Si:H}(n)$ may be investigated. Although this cell structure may have only a limited potential to enhance the cell efficiency, LEP-SHJ cells are nevertheless an ideal test structure to study the a-Si:H/TCO interface as the effects of electrical properties of this interface are magnified due to the localized contact.

7.2.4 TMO-based SHJ solar cells

In MoO_x-based SHJ devices, currently the main limitation experienced is the parasitic light absorption in the MoO_x film induced by the TCO sputtering. To suppress or reduce this effect, O₂ or CO₂ plasma treatments may be investigated to stabilize the MoO_x film prior the TCO sputtering. Other TMO materials such as WO_x have also revealed promising results for SHJ perspectives and possibly a better robustness to subsequent TCO sputtering. [Bivour 2015] Another important limitation of MoO_x-based devices reported in this thesis is that the IO:H/ITO front TCO is not optimized for use without annealing. In this respect, an amorphous TCO such as IZO may be an interesting candidate to replace the IO:H/ITO bilayer.

7.2.5 High-efficiency SHJ solar cell suggestion

In this section, we suggest and describe a SHJ solar cell that integrates different outcomes of this thesis with developments made beyond this work. A schematic of the suggested device is shown in Fig. 7.1

As often reported in high-efficiency solar cells, light reflection at the front surface can be significantly reduced by adding a second ARC (section 1.1.5). MgF_2 is often used for this purpose due to its low refractive index. Although a relatively small improvement was recorded in the case shown in section 3.4.4, likely due to an un-optimized process, we obtained a J_{sc} enhancement of up to 0.6 mA cm^{-2} by using this process. For the front metallization, copper electrodeposition is the most suitable technique for high-efficiency SHJ solar cells: As demonstrated in this work, $15\text{-}\mu\text{m}$ -wide fingers can be achieved with the potential to be reduced to $\approx 10 \mu\text{m}$ while keeping a good aspect-ratio and thus low finger line resistance resulting in an additional J_{sc} gain of $\approx 0.2 \text{ mA cm}^{-2}$. As previously mentioned, IO:H must be replaced by another material that does not rely on annealing to tune its optical properties such as amorphous IZO. [Morales-Masis 2015] To enhance the blue response of the device, the suggested structure shown in Fig. 7.1 is based on a highly transparent TMO-based hole collector such as MoO_x or WO_x . If the interaction induced by the TCO sputtering can be mitigated—either by optimizing the TCO sputtering or with prior plasma treatments of the TMO film—a J_{sc} enhancement of up to 0.5 mA cm^{-2} can be achieved. A thin c-Si wafer with a thickness down to $100 \mu\text{m}$ is suggested for reducing the wafer cost and to reach higher V_{oc} beneficial for improving the efficiency temperature coefficient. [Meyer-Burger 2014a] [Kinoshita 2011] [Taguchi 2014] [Seif 2015b] [Tsunomura 2009] At the rear side, the electron collector may be improved by replacing the a-Si:H(n) with $\mu\text{c-Si:H(n)}$ providing a more efficient contact with the TCO with the potential to improve the FF up to 2%. [Seif 2015a] [Watahiki 2015] To improve light management at the rear side, a low refractive index dielectric layer can be inserted between the rear TCO and the metal film to suppress the parasitic plasmonic losses, with a potential J_{sc} improvement of up to 0.5 mA cm^{-2} . [Holman 2013] Finally, we propose to replace the metallic rear contact usually made of sputtered silver with copper. [Holman 2014] Due to the MgF_2 rear reflector, similar reflectance can be expected with copper with the additional benefit of a cost reduction. [Holman 2013] To avoid the oxidation of front and rear copper contacts, a final electroless deposition of a protective tin capping film may be used.

Hence, with this suggested structure, a SHJ solar cell with 24% to 25% efficiency can be manufactured with an entirely silver-free process compatible with mass production providing that n-type material with good lifetime properties is available. [Bätzner 2014]

Publication list

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Publications as first author in peer-reviewed journals

- J. Geissbühler, S. De Wolf, B. Demareux, J. P. Seif, D. T. L. Alexander, L. Barraud and C. Ballif, "*Amorphous/crystalline silicon interface defects induced by hydrogen plasma treatments*", *Appl. Phys. Lett.* **102**, 231604 (2013)
- J. Geissbühler, S. De Wolf, A. Faes, N. Badel, Q. Jeangros, A. Tomasi, L. Barraud, A. Descoeudres, M. Despeisse, and C. Ballif, "*Silicon Heterojunction Solar Cells With Copper-Plated Grid Electrodes: Status and Comparison With Silver Thick-Film Techniques*", *IEEE J. Photovoltaics* **4**, 4 (2014)
- J. Geissbühler, J. Werner, S. Martin de Nicolas, L. Barraud, A. Hessler-Wyser, M. Despeisse, S. Nicolay, A. Tomasi, B. Niesen, S. De Wolf, and C. Ballif, "*22.5% efficient silicon heterojunction solar cell with molybdenum oxide hole collector*", *Appl. Phys. Lett.* **107**, 081601 (2015)

Patent

- C. Ballif, J. Geissbühler, US Patent 20,150,144,184, (2015)

Publications as co-author in peer-reviewed journals

- J. P. Seif, A. Descoeudres, G. Nogay, S. Hänni, S. Martin de Nicolas, N. Holm, M. Duchamp, A. Hessler-Wyser, J. Geissbühler, S. De Wolf and C. Ballif, "*Thin Microcrystalline Silicon doped Layers for Silicon Heterojunction Solar Cells*" manuscript in preparation, 2015.
- A. Tomasi, F. Sahli, J. P. Seif, L. Fanni, S. Martin de Nicolas, J. Geissbühler, B. Paviet-Salomon, S. Nicolay, B. Niesen, S. De Wolf and C. Ballif, "*Transparent Electrodes in Silicon Heterojunction Solar Cells: Influence on Contact Passivation*", submitted to IEEE J. Photovoltaics, (2015)

- B. Terheiden, T. Ballmann, R. Horbelt, Y. Schiele, S. Seren, J. Ebser, G. Hahn, V. Mertens, M. B. Koentopp, M. Scherff, J. W. Müller, Z. C. Holman, A. Descoeudres, S. De Wolf, S. Martin De Nicolas, J. Geissbuehler, C. Ballif, B. Weber, P. Saint Cast, M. Rauer, C. Schmiga, S. W. Glunz, D. J Morrison, S. Devenport, D. Antonelli, C. Busto, F. Grasso, F. Ferrazza, E. Tonelli, W. Oswald, "*Manufacturing 100 μm thick silicon solar cells with efficiencies greater than 20% in a pilot production line*", Phys. Status Solidi A, **212**, 13–24, (2015)
- A. Tomasi, B. Paviet-Salomon, D. Lachenal, S. Martin de Nicolas, A. Descoeudres, J. Geissbuehler, S. De Wolf, C. Ballif, "*Back-contacted silicon heterojunction solar cells with efficiency > 21%*", IEEE J. Photovoltaics, **4**, 4, (2015)
- Andrea Franco, J. Geissbuehler, N. Wyrsh and C. Ballif, "*Fabrication and characterization of monolithically integrated microchannel plates based on amorphous silicon*", Nature scientific report, **4**, (2014)
- B. Demareux, R. Bartlome, J. P Seif, J. Geissbuehler, D.T.L. Alexander, Q. Jeangros, C. Ballif, S. De Wolf, "*Low-temperature plasma-deposited silicon epitaxial films: Growth and properties*", J. of Appl. Phys., **116**, 053519, (2014)
- B. Demareux, J. P Seif, S. Smit, B. Macco, W.M.M. Kessels, J. Geissbuehler, S. De Wolf, C. Ballif, "*Atomic-layer-deposited transparent electrodes for silicon heterojunction solar cells*", IEEE J. Photovoltaics, **4**, 6, (2014)

Conferences presentations as first author

- J. Geissbuehler, S. Martin de Nicolas, M. Morales Masis, A. Faes, A. Lachowicz, A. Tomasi, B. Paviet-Salomon, B. Demareux, J. Seif, N. Holms, D. Lachenal, P. Papet, N. Badel, L. Barraud, A. Hessler-Wyser, A. Descoeudres, P. Löper, M. Despeisse, S. De Wolf, and C. Ballif, "*Electrodeposited copper front metallization for silicon heterojunction solar cells: materials and processes*", Oral presentation, Workshop on Metallization of Crystalline Silicon Solar Cells, Konstanz, Germany, (2014)
- J. Geissbuehler, S. De Wolf, B. Demareux, J. P. Seif, D. T.L Alexander, L. Barraud and Ch. Ballif, "*Amorphous/crystalline silicon interface modification by hydrogen plasma treatments*", Oral presentation, Materials research society (MRS pring meeting), San Fransisco, USA, (2014)
- J. Geissbuehler, A. Faes, N. Badel, B. Demareux, J. Seif, A. Tomasi, L. Barraud, Q. Jeangros, A. Descoeudres, S. Martin de Nicolas, B. Paviet-Salomon, J. Holovsky, M. Despeisse, P. Papet, S. De Wolf and C. Ballif, "*High-efficiency silicon heterojunction solar cells with electrodeposited copper metallization*", Oral presentation, 28th European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC), Paris, France (2013)

- J. Geissbühler, S. De Wolf, A. Faes, N. Badel, B. Demaurex, J. Seif, A. Tomasi, L. Barraud, A. Descoeurdes, S. Martin de Nicolas, B. Paviet-Salomon, J. Holovsky, M. Despeisse, Z.C. Holman, P. Papet and C. Ballif, "*Electrodeposited copper front metallization for High-efficiency silicon heterojunction solar cells*", Oral presentation, Workshop on Metallization of Crystalline Silicon Solar Cells, Konstanz, Germany, (2013)

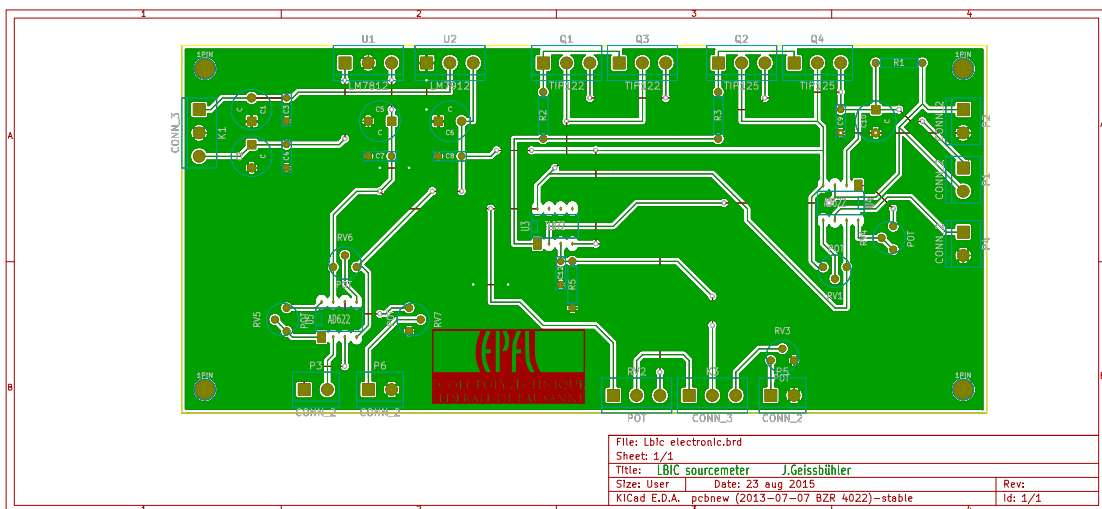
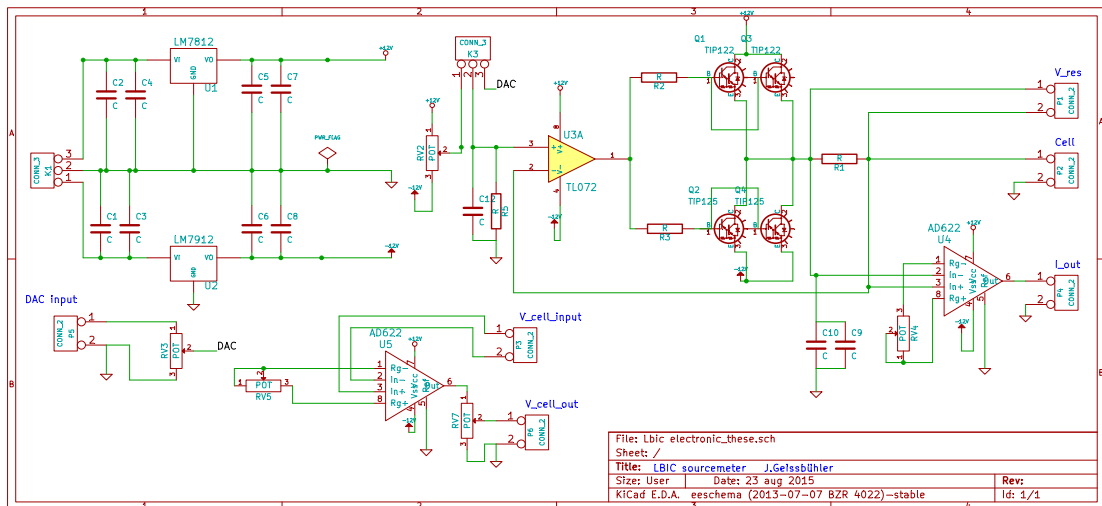
Conferences presentations as co-author

- J. P. Seif, B. Demaurex, S. Martin de Nicolas, N. Holm, J. Geissbühler, S. Smit, B. Macco and E. Kessels S. De Wolf and C. Ballif, "*Fill-Factor Loss Analysis of Silicon Heterojunction Solar Cells with Atomic-Layer-Deposited Transparent Electrodes*", MRS Spring Meeting, San Francisco, California, USA, (2015)
- B. Demaurex, R. Bartlome, J. P. Seif, J. Geissbühler, D. T. L. Alexander, Q. Jeangros, C. Ballif, and S. De Wolf, "*PECVD silicon homo-epitaxy: interface and bulk properties*", MRS Spring Meeting, San Francisco, California, USA, (2015)
- A. Tomasi, F. Sahli, L. Fanni, J. P. Seif, S. Martin de Nicolas, N. Holm, J. Geissbühler, Philipp Löper, S. Nicolay, S. De Wolf and C. Ballif, "*Transparent Conductive Oxides in Silicon Heterojunction Solar Cells: Influence on Carrier Recombination*", 42th IEEE Photovoltaic Specialists Conference, New Orleans, Louisiana, USA, (2015)
- A. Tomasi, B. Paviet-Salomon, S. Nicolay, A. Tajalli, J. P. Seif, J. Geissbühler, S. Martin de Nicolas, N. Holm, S. De Wolf, M. Despeisse, and C. Ballif, "*Efficient Electrodes for Back-Contacted Silicon Heterojunction Solar Cells*" 27th European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, Germany, (2015)
- S. De Wolf, J. Geissbühler, P. Löper, S. Martin de Nicolas, J. P. Seif, A. Tomasi, and C. Ballif, "*High-Efficiency Silicon Heterojunction Solar cells: Achievements and Perspectives*", E-MRS: Conference & Exhibit, Lille, France, (2015)
- J. Levrat, C. Allebe, N. Badel, L. Barraud, M. Bonnet-Eymard, J. Champlaud, F. Debrot, A. Descoeurdes, A. Faes, A. Lachowicz, S. Nicolay, L. Sansonnens, C. Ballif, J. Geissbühler, S. De Wolf, M. Despeisse, "*High-performance hetero-junction crystalline silicon photovoltaic technology*" Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th ,**8-13**, pp.1218,1222, (2014)
- S. De Wolf, B. Demaurex, J. Geissbühler, P. Löper, S. Martin de Nicolas, B. Paviet-Salomon, J. P. Seif, A. Tomasi and C. Ballif, "*High-efficiency Silicon Heterojunction Solar Cells: Status and Perspectives*", 40th IEEE Photovoltaic Specialists Conference, Denver, Colorado, USA, (2014)
- S. Martin de Nicolas, B. Demaurex, J. Geissbühler, N. Holm, P. Löper, B. Paviet-Salomon, J. P. Seif, A. Tomasi, S. De Wolf, and C. Ballif, "*Increase the photogenerated current in*

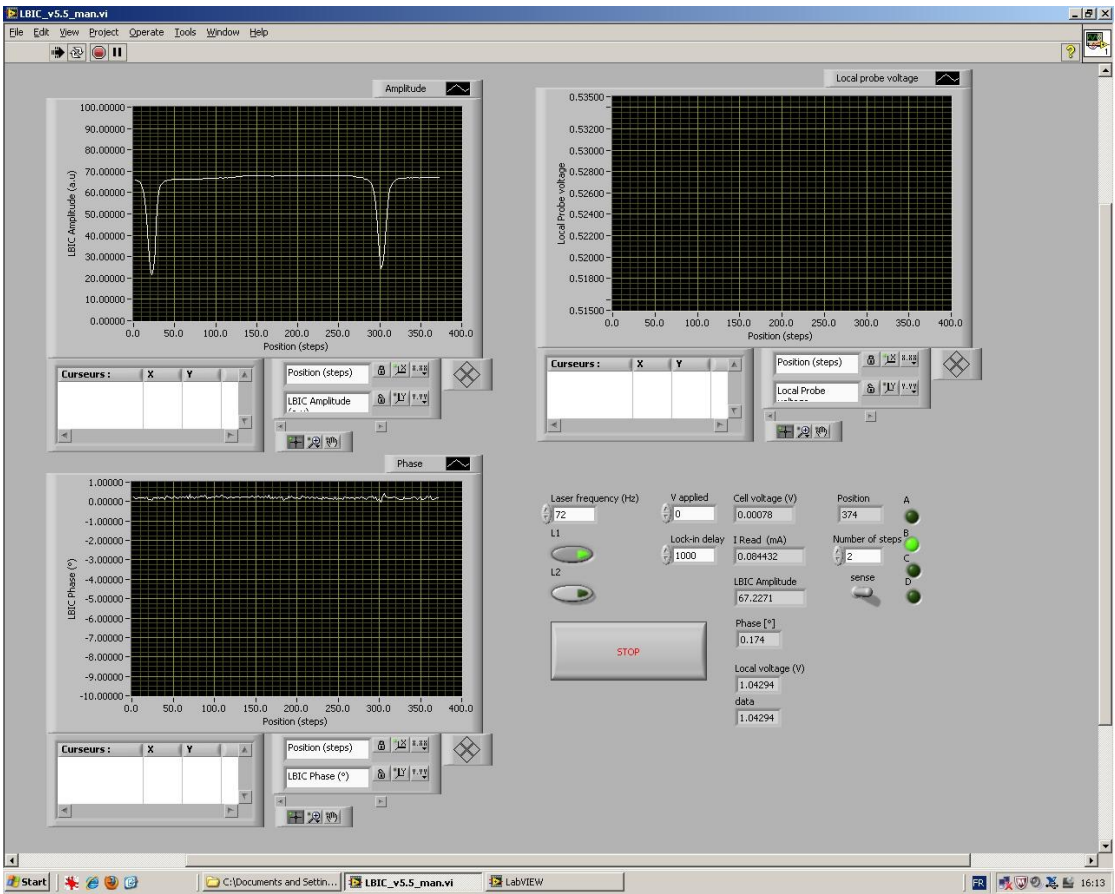
amorphous/crystalline silicon solar cells", 6th World Conference on Photovoltaic Energy Conversion, Kyoto, Japan, (2014)

- A. Lachowicz, A. Faes, P. Papet, J. Geissbühler, J. Levrat, C. Allebé, N. Badel, J. Champiaud, F. Debrot, J. Cattin, A. Hessler-Wyser, B. Strahm, S. De Wolf, M. Despeisse and C. Ballif, "*Plating on Thin Conductive Oxides for Silicon Heterojunction Solar Cells*", Workshop on Metallization of Crystalline Silicon Solar Cells, Konstanz, Germany, (2014)
- A. Faes, A. Lachowicz, C. Allebé, F. Debrot, N. Badel, M. Despeisse, P.-J. Alet, F. Galliano, L. E. Perret-Aebi, J. Geissbühler, S. De Wolf, C. Ballif, D. Lachenal, G. Waehli, P. Papet and B. Strahm, "*Advanced Metallization for Silicon Heterojunction Solar Cells*", 29th European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC), Hamburg, Germany, (2014)
- P. Papet, J. Hermans, T. Söderström, M. Cucinelli, L. Andreetta, D. Bätzner, W. Frammelsberger, J. Meixenberger, D. Lachenal, B. Legradic, B. Strahm, G. Wahli, W. Brok, J. Geissbühler, A. Tomasi, C. Ballif, E. Vetter, S. Leu, "*Heterojunction Solar Cells with electroplated Ni/Cu front grid*", 28th European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC), Paris, France (2013)
- A. Descoeudres, C. Allebé, N. Badel, L. Barraud, F. Debrot, B. Demareux, A. Faes, J. Geissbühler, N. Holm, Z.C. Holman, J. Holovsky, S. Martin de Nicolas, B. Paviet-Salomon, J. Seif, A. Tomasi, M. Despeisse, S. De Wolf and C. Ballif, "*Recent progress in high-efficiency silicon heterojunction solar cells at EPFL*", Tech. Digest 23rd PVSEC, Taipei, Taiwan, (2013).
- A. Descoeudres, Z.C. Holman, L. Barraud, S. Morel, B. Demareux, J. Geissbühler, J.P. Seif, S. De Wolf, and C. Ballif, "*Silicon Heterojunction Solar Cells on n- and p-Type Wafers with Efficiencies above 20%*", 27th European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC), Frankfurt, Germany, (2012)
- A. Descoeudres, L. Barraud, P. Bôle Rothen, S. De Wolf, B. Demareux, Z. C. Holman, J. P. Seif, F. Zicarelli Fernandez, C. Ballif, J. Geissbühler, "*21% efficiency silicon heterojunction solar cells produced with very high frequency PECVD*", 21st International Photovoltaic Science and Engineering Conference (PVSEC-21), Fukuoka, Japan, (2011)

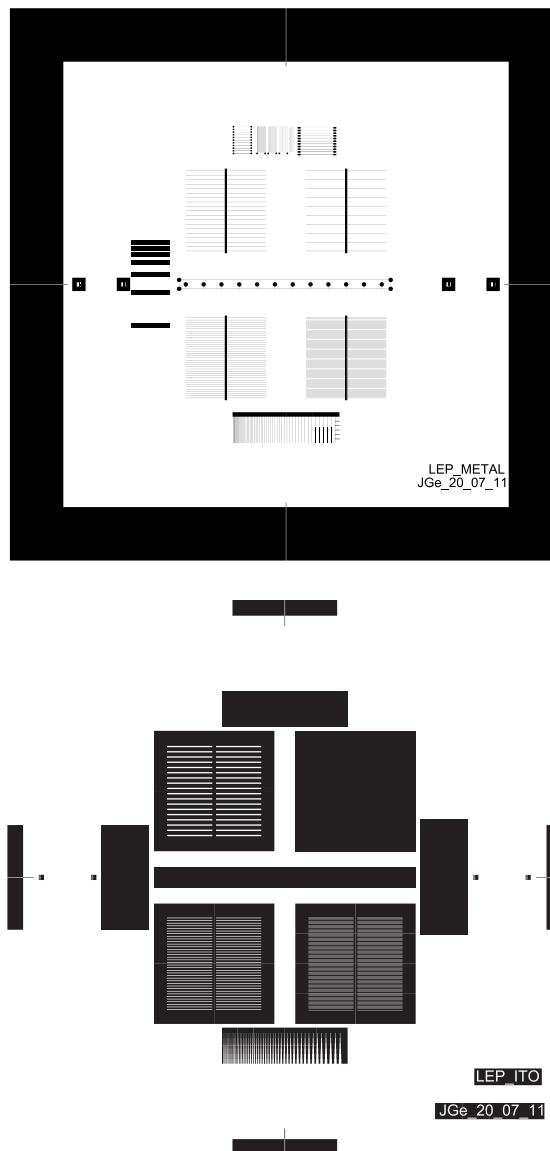
A LBIC circuit diagram and software



Appendix A. LBIC circuit diagram and software



B LEP-SHJ photolithography masks



Bibliography

- [Aberle 1994] A. G.Aberle, S. R.Wenham, M. A.Green and G.Heiser. *Decreased emitter sheet resistivity loss in high-efficiency silicon solar cells*. Progress in Photovoltaics: Research and Applications, vol. 2, no. 1, pages 3–17, 1994.
- [Acciarri 2002] M.Acciarri, S.Binetti, A.Racz, S.Pizzini and G.Agostinelli. *Fast LBIC in-line characterization for process quality control in the photovoltaic industry*. Solar Energy Materials and Solar Cells, vol. 72, no. 1–4, pages 417 – 424, 2002. {EMRS} 2001 Symposium E: Crystalline Silicon for Solar Cells.
- [Admin 2011] Admin. *Dans sa nouvelle stratégie, le Conseil fédéral se décide pour l'abandon progressif du nucléaire*. 2011.
- [Aleman 2009] M.Aleman, N.Bay, D.Barucha, A.Knorz, D.Biro, R.Preu, S.Glunz, M.Assmus, S.Jack and M.Koehl. *Advances in electroless nickel plating for the metallization of silicon solar cells using different structuring techniques for the ARC*. Proc. of the 24th EPVSEC, pages 1414–1418, 2009.
- [Ballif 2003] C.Ballif, D. M.Huljić, G.Willeke and A.Hessler-Wyser. *Silver thick-film contacts on highly doped n-type silicon emitters: Structural and electronic properties of the interface*. Applied Physics Letters, vol. 82, no. 12, 2003.
- [Ballif 2014] C.Ballif, S.De Wolf, A.Descoeurdes and Z. C.Holman. *Amorphous Silicon/Crystalline Silicon Heterojunction Solar Cells*. Advances In Photovoltaics, Pt 3, vol. 90, pages 73–120, 2014.
- [Ballif 2015] C.Ballif and J.Geissbuhler. *SOLAR CELL*, May 28 2015. US Patent 20,150,144,184.
- [Barraud 2013] L.Barraud,
and C.Ballif. *Hydrogen-doped indium oxide/indium tin oxide bilayers for high-efficiency silicon heterojunction solar cells*. Solar Energy Materials and Solar Cells, vol. 115, no. 0, pages 151 – 156, 2013.
- [Bartsch 2010] J.Bartsch, V.Radtke, C.Schetter and S.Glunz. *Electrochemical methods to analyse the light-induced plating process*. Journal of Applied Electrochemistry, vol. 40, no. 4, pages 757–765, 2010.

Bibliography

- [Battaglia 2014a] C.Battaglia, S. M.de Nicolás, S.De Wolf, X.Yin, M.Zheng, C.Ballif and A.Javey. *Silicon heterojunction solar cell with passivated hole selective MoOx contact*. Applied Physics Letters, vol. 104, no. 11, page 113902, 2014.
- [Battaglia 2014b] C.Battaglia, X.Yin, M.Zheng, I. D.Sharp, T.Chen, S.McDonnell, A.Azcatl, C.Carraro, B.Ma, R.Maboudian, R. M.Wallace and A.Javey. *Hole Selective MoOx Contact for Silicon Solar Cells*. Nano Letters, vol. 14, no. 2, pages 967–971, 2014. PMID: 24397343.
- [Battey 1987] J.Battey, N.Nelson and D.Barnett. *Copper etching process and product*. September 22 1987. US Patent 4,695,348.
- [Becker 1986] E.Becker, W.Ehrfeld, P.Hagmann, A.Maner and D.Münchmeyer. *Fabrication of microstructures with high aspect ratios and great structural heights by synchrotron radiation lithography, galvanofforming, and plastic moulding (LIGA process)*. Microelectronic Engineering, vol. 4, no. 1, pages 35 – 56, 1986.
- [Benick 2011] J.Benick, K.Zimmermann, J.Spiegelman, M.Hermle and S. W.Glunz. *Rear side passivation of PERC-type solar cells by wet oxides grown from purified steam*. Progress in Photovoltaics: Research and Applications, vol. 19, no. 3, pages 361–365, 2011.
- [Berger 1972] H.Berger. *Models for contacts to planar devices*. Solid-State Electronics, vol. 15, no. 2, pages 145 – 158, 1972.
- [Beyer 1991] W.Beyer. *Hydrogen effusion: a probe for surface desorption and diffusion*. Physica B: Condensed Matter, vol. 170, no. 1–4, pages 105 – 114, 1991.
- [Bivour 2011] M.Bivour, M.Rüdiger, C.Reichel, K.-U.Ritzau, M.Hermle and S.Glunz. *Analysis of the diffused front surface field of n-type silicon solar cells with a-Si/c-Si heterojunction rear emitter*. volume 8, pages 185–192, 2011. cited By 6.
- [Bivour 2012] M.Bivour, C.Reichel, M.Hermle and S. W.Glunz. *Improving the a-Si:H(p) rear emitter contact of n-type silicon solar cells*. Solar Energy Materials and Solar Cells, vol. 106, pages 11 – 16, 2012. SiliconPV.
- [Bivour 2013] M.Bivour, S.Schröer and M.Hermle. *Numerical Analysis of Electrical TCO / a-Si:H(p) Contact Properties for Silicon Heterojunction Solar Cells*. Energy Procedia, vol. 38, no. 0, pages 658 – 669, 2013. Proceedings of the 3rd International Conference on Crystalline Silicon Photovoltaics (SiliconPV 2013).
- [Bivour 2014] M.Bivour, M.Reusch, S.Schroer, F.Feldmann, J.Temmler, H.Steinkemper and M.Hermle. *Doped Layer Optimization for Silicon Heterojunctions by Injection-Level-Dependent Open-Circuit Voltage Measurements*. Photovoltaics, IEEE Journal of, vol. 4, no. 2, pages 566–574, March 2014.
- [Bivour 2015] M.Bivour, J.Temmler, H.Steinkemper and M.Hermle. *Molybdenum and tungsten oxide: High work function wide band gap contact materials for hole selective contacts of silicon solar cells*. Solar Energy Materials and Solar Cells, no. 0, pages –, 2015.

- [Blakers 1986] A. W.Blakers and M. A.Green. *20% efficiency silicon solar cells*. Applied Physics Letters, vol. 48, no. 3, 1986.
- [Blakers 1989] A. W.Blakers, A.Wang, A. M.Milne, J.Zhao and M. A.Green. *22.8% efficient silicon solar cell*. Applied Physics Letters, vol. 55, no. 13, 1989.
- [Boccard 2014] M.Boccard, M.Despeisse, J.Escarre, X.Niquille, G.Bugnon, S.Hanni, M.Bonnet-Eymard, F.Meillaud and C.Ballif. *High-Stable-Efficiency Tandem Thin-Film Silicon Solar Cell With Low-Refractive-Index Silicon-Oxide Interlayer*. Photovoltaics, IEEE Journal of, vol. 4, no. 6, pages 1368–1373, Nov 2014.
- [Bätzner 2014] D.Bätzner, L.Andreetta, W.Lachenal D. Frammelsberger, B.Legradic, J.Meixenberger, P.Papet, B.Strahm and G.Wahli. *Silicon Material Considerations for Heterojunction Solar Cells: Potential and Limitations*. In proceedings of 29th EUPVSEC, Amsterdam, The Netherlands, pages 789–792, 2014.
- [Bullock 2014] J.Bullock, A.Cuevas, T.Allen and C.Battaglia. *Molybdenum oxide MoOx: A versatile hole contact for silicon solar cells*. Applied Physics Letters, vol. 105, no. 23, page 232109, 2014.
- [Bullock 2015] J.Bullock. To be submitted, 2015.
- [Bundesministerium 2014] Bundesministerium. *Zeitreihen zur Entwicklung der erneuerbaren Energien in Deutschland*. 2014.
- [Burger 2015] M.Burger. *MB PERC technology*. 2015.
- [Carazzetti 2006] p.Carazzetti. *High Quality Micromachined Inductors for Integrated Communication Systems*. Ph.D. dissertation, 2006.
- [Carstensen 2003] J.Carstensen, G.Popkirov, J.Bahr and H.Föll. *CELLO: an advanced LBIC measurement technique for solar cell local characterization*. Solar Energy Materials and Solar Cells, vol. 76, no. 4, pages 599 – 611, 2003. Photovoltaics and photoactive materials - properties, technology and applications.
- [Centurioni 2003] E.Centurioni and D.Iencinella. *Role of front contact work function on amorphous silicon/crystalline silicon heterojunction solar cell performance*. IEEE Electron Device Letters, vol. 24, no. 3, pages 177–179, 2003. cited By 62.
- [Chapin 1954] D. M.Chapin, C. S.Fuller and G. L.Pearson. *A New Silicon p-n Junction Photocell for Converting Solar Radiation into Electrical Power*. Journal of Applied Physics, vol. 25, no. 5, 1954.
- [Chapin 1957] D.Chapin, C.Fuller and G.Pearson. *Solar energy converting apparatus*, February 5 1957. US Patent 2,780,765.
- [Chen 2012] S.Chen, J. R.Manders, S.-W.Tsang and F.So. *Metal oxides for interface engineering in polymer solar cells*. J. Mater. Chem., vol. 22, pages 24202–24212, 2012.

Bibliography

- [Chen 2015] B.-M.Chen, C.-Y.Peng, J.-L.Cho and G. A.Porter. *Optimization of Solar Module Encapsulant Lamination by Optical Constant Determination of Ethylene-Vinyl Acetate*. International Journal of Photoenergy, vol. 3, page 276404, 2015.
- [Chiril 2011] A.Chiril, S.Buecheler, F.Pianezzi, P.Bloesch, C.Gretener, A. R.Uhl, C.Fella, L.Kranz, J.Perrenoud, S.Seyrling *et al.* *Highly efficient Cu (In, Ga) Se₂ solar cells grown on flexible polymer films*. Nature materials, vol. 10, no. 11, pages 857–861, 2011.
- [Choong 2010] G.Choong, P.Bôle, L.Barraud, F.Zicarelli Fernandez, A.Descoeurdes, S.De Wolf and C.Ballif. *Transparent Conductive Oxides for Silicon Heterojunction Solar Cells*. In proceedings of the 25th EUPVSEC, Valencia, Spain, 2010.
- [Clugston 1997] D.Clugston and P.Basore. *PC1D version 5: 32-bit solar cell modeling on personal computers*. In Photovoltaic Specialists Conference, 1997., Conference Record of the Twenty-Sixth IEEE, pages 207–210, Sep 1997.
- [Colina 2015] M.Colina, A.Morales-Vilches, C.Voz, I.Martin, P.Ortega and R.Alcubilla. *Low Surface Recombination in Silicon-Heterojunction Solar Cells With Rear Laser-Fired Contacts From Aluminum Foils*. Photovoltaics, IEEE Journal of, vol. 5, no. 3, pages 805–811, May 2015.
- [Cossutta 2014] H.Cossutta, K.Taretto and M.Troviano. *Low-cost system for micrometer-resolution solar cell characterization by light beam-induced current mapping*. Measurement Science and Technology, vol. 25, no. 10, page 105801, 2014.
- [Cuevas 1996] A.Cuevas, P. A.Basore, G.Giroult Matlakowski and C.Dubois. *Surface recombination velocity of highly doped n type silicon*. Journal of Applied Physics, vol. 80, no. 6, 1996.
- [Cuevas 2013] A.Cuevas and D.Yan. *Misconceptions and Misnomers in Solar Cells*. Photovoltaics, IEEE Journal of, vol. 3, no. 2, pages 916–923, April 2013.
- [De Wolf 2005] S.De Wolf. *Rear Passivation for Thin Base Low-Cost Silicon Solar Cells*. Ph.D. dissertation, Katholieke Universiteit Leuven, 2005.
- [De Wolf 2007a] S.De Wolf and M.Kondo. *Abruptness of a-Si:H/c-Si interface revealed by carrier lifetime measurements*. Applied Physics Letters, vol. 90, no. 4, pages –, 2007.
- [De Wolf 2007b] S.De Wolf and M.Kondo. *Boron-doped a-Si:H/c-Si interface passivation: Degradation mechanism*. Applied Physics Letters, vol. 91, no. 11, pages –, 2007.
- [De Wolf 2008] S.De Wolf, S.Olibet and C.Ballif. *Stretched-exponential a-Si:H/c-Si interface recombination decay*. Applied Physics Letters, vol. 93, no. 3, pages –, 2008.
- [De Wolf 2009] S.De Wolf and M.Kondo. *Nature of doped a-Si:H/c-Si interface recombination*. Journal of Applied Physics, vol. 105, no. 10, pages –, 2009.

- [De Wolf 2012] S.De Wolf, A.Descoeudres, Z. C.Holman and C.Ballif. *High-efficiency Silicon Heterojunction Solar Cells: A Review*. Green, vol. 2, no. 1, pages 7–24, 2012.
- [De Wolf 2014] S.De Wolf, J.Holovsky, S.-J.Moon, P.Löper, B.Niesen, M.Ledinsky, F.-J.Haug, J.-H.Yum and C.Ballif. *Organometallic Halide Perovskites: Sharp Optical Absorption Edge and Its Relation to Photovoltaic Performance*. The Journal of Physical Chemistry Letters, vol. 5, no. 6, pages 1035–1039, 2014.
- [Demaurex 2012] B.Demaurex, S.De Wolf, A.Descoeudres, Z.Charles Holman and C.Ballif. *Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering*. Applied Physics Letters, vol. 101, no. 17, pages –, 2012.
- [Demaurex 2014a] B.Demaurex, J.Seif, S.Smit, B.Macco, W.Kessels, J.Geissbuhler, S.De Wolf and C.Ballif. *Atomic-Layer-Deposited Transparent Electrodes for Silicon Heterojunction Solar Cells*. Photovoltaics, IEEE Journal of, vol. 4, no. 6, pages 1387–1396, Nov 2014.
- [Demaurex 2014b] B.Demaurex, R.Bartlome, J. P.Seif, J.Geissbühler, D. T. L.Alexander, Q.Jeangros, C.Ballif and S.De Wolf. *Low-temperature plasma-deposited silicon epitaxial films: Growth and properties*. Journal of Applied Physics, vol. 116, no. 5, pages –, 2014.
- [Descoeudres 2010] A.Descoeudres, L.Barraud, R.Bartlome, G.Choong, S.De Wolf, F.Zicarelli and C.Ballif. *The silane depletion fraction as an indicator for the amorphous/crystalline silicon interface passivation quality*. Applied Physics Letters, vol. 97, no. 18, pages –, 2010.
- [Descoeudres 2011] A.Descoeudres, L.Barraud, S.De Wolf, B.Strahm, D.Lachenal, C.Guérin, Z. C.Holman, F.Zicarelli, B.Demaurex, J.Seif, J.Holovsky and C.Ballif. *Improved amorphous/crystalline silicon interface passivation by hydrogen plasma treatment*. Applied Physics Letters, vol. 99, no. 12, pages –, 2011.
- [Descoeudres 2012] A.Descoeudres, L.Barraud, S.De Wolf, B.Demaurex, J.Geissbuhler, Z. C.Holman, S. V.Morel, J. P.Seif and C.Ballif. *Silicon heterojunction solar cells on n-and p-type wafers with efficiencies above 20%*. in proceedings of the 27th European Photovoltaic Solar Energy Conference and Exhibition, Frankfurt, Germany, pages 647–651, 2012.
- [Descoeudres 2013] A.Descoeudres, Z.Holman, L.Barraud, S.Morel, S.De Wolf and C.Ballif. *> 21% Efficient Silicon Heterojunction Solar Cells on n- and p-Type Wafers Compared*. Photovoltaics, IEEE Journal of, vol. 3, no. 1, pages 83–89, Jan 2013.
- [Despont 1997] M.Despont, H.Lorenz, N.Fahrni, J.Brugger, P.Renaud and P.Vettiger. *High-aspect-ratio, ultrathick, negative-tone near-UV photoresist for MEMS applications*. pages 518–522, 1997.

Bibliography

- [Desrues 2011] T.Desrues, S.De Vecchi, F.Souche, D.Diouf, D.Muñoz, M.Gueunier-Farret, J.-P.Kleider and P.-J.Ribeyron. *Development of Interdigitated Back Contact Silicon Heterojunction (IBC Si-HJ) Solar Cells*. Energy Procedia, vol. 8, pages 294 – 300, 2011. Proceedings of the SiliconPV 2011 Conference (1st International Conference on Crystalline Silicon Photovoltaics).
- [Dimroth 2014] F.Dimroth, M.Grave, P.Beutel, U.Fiedeler, C.Karcher, T. N. D.Tibbits, E.Oliva, G.Siefer, M.Schachtner, A.Wekkeli, A. W.Bett, R.Krause, M.Piccin, N.Blanc, C.Drazek, E.Guiot, B.Ghyselen, T.Salvetat, A.Tauzin, T.Signamarcheix, A.Dobrich, T.Hannappel and K.Schwarzburg. *Wafer bonded four-junction GaInP/GaAs//GaInAsP/GaInAs concentrator solar cells with 44.7% efficiency*. Progress in Photovoltaics: Research and Applications, vol. 22, no. 3, pages 277–282, 2014.
- [Ding 2011] L.Ding, M.Boccard, G.Bugnon, M.Benkhaira, M.Despeisse, S.Nicolay, P.Losio, O.Kluth, P.Carroy, O.Caglar and C.Ballif. *New generation transparent LPCVD ZnO electrodes for enhanced photocurrent in micromorph solar cells and modules*. In Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE, pages 002578–002578, June 2011.
- [Ding 2013a] K.Ding, U.Aeberhard, F.Finger and U.Rau. *Optimized amorphous silicon oxide buffer layers for silicon heterojunction solar cells with microcrystalline silicon oxide contact layers*. Journal of Applied Physics, vol. 113, no. 13, pages –, 2013.
- [Ding 2013b] L.Ding. *Low-Pressure Chemical Vapor Deposited Zinc Oxide Films:Toward Decoupled Opto-Electrical and Morphological Properties for More Efficient Electrodes*. Ph.D. dissertation, École polytechnique fédérale de Lausanne, 2013.
- [El Mhamdi 2014] E. M.El Mhamdi, J.Holovsky, B.Demaurex, C.Ballif and S.De Wolf. *Is light-induced degradation of a-Si:H/c-Si interfaces reversible?* Applied Physics Letters, vol. 104, no. 25, pages –, 2014.
- [Faes 2014] A.Faes, M.Despeisse, J.Levrat, J.Champlaud, N.Badel, M.Kiaee, T.Söderström, Y.Yao, R.Grischke, M.Gragert, J.Ufheil, P.Papet, B.Strahm, B.Cattaneo, J.Cattin, Y.Baumgartner, A.Hessler-Wyser and C.Ballif. *SmartWire Solar Cell Interconnection Technology*. presented at the 29th Eur. Photovoltaic Solar Energy Conf. Exhib., pages 2555 – 2561, 2014.
- [Fang 2014] L.Fang, S. J.Baik and K. S.Lim. *Transition metal oxide window layer in thin film amorphous silicon solar cells*. Thin Solid Films, vol. 556, no. 0, pages 515 – 519, 2014.
- [Favier 2011] A.Favier, D.Munoz, S. M.de Nicolas and P.-J.Ribeyron. *Boron-doped zinc oxide layers grown by metal-organic CVD for silicon heterojunction solar cells applications*. Solar Energy Materials and Solar Cells, vol. 95, no. 4, pages 1057 – 1061, 2011.
- [Feldmann 2014a] F.Feldmann, M.Simon, M.Bivour, C.Reichel, M.Hermle and S. W.Glunz. *Carrier-selective contacts for Si solar cells*. Applied Physics Letters, vol. 104, no. 18, pages –, 2014.

- [Feldmann 2014b] F.Feldmann, M.Bivour, C.Reichel, M.Hermle and S. W.Glunz. *Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics*. Solar Energy Materials and Solar Cells, vol. 120, Part A, pages 270 – 274, 2014.
- [Feldmann 2014c] F.Feldmann, M.Bivour, C.Reichel, H.Steinkemper, M.Hermle and S. W.Glunz. *Tunnel oxide passivated contacts as an alternative to partial rear contacts*. Solar Energy Materials and Solar Cells, vol. 131, pages 46 – 50, 2014. SI: SiliconPV 2014.
- [Fellmeth 2011] T.Fellmeth, S.Mack, J.Bartsch, D.Erath, U.Jager, R.Preu, F.Clement and D.Biro. *20.1% Efficient Silicon Solar Cell With Aluminum Back Surface Field*. Electron Device Letters, IEEE, vol. 32, no. 8, pages 1101–1103, Aug 2011.
- [Filipic 2013] M.Filipic, Z. C.Holman, F.Smole, S.De Wolf, C.Ballif and M.Topic. *Analysis of lateral transport through the inversion layer in amorphous silicon/crystalline silicon heterojunction solar cells*. Journal of Applied Physics, vol. 114, no. 7, pages –, 2013.
- [Franco 2014] A.Franco, J.Geissbuhler, N.Wyrsch and C.Ballif. *Fabrication and characterization of monolithically integrated microchannel plates based on amorphous silicon*. Scientific reports, vol. 4, 2014.
- [Franklin 2014] E.Franklin, K.Fong, K.McIntosh, A.Fell, A.Blakers, T.Kho, D.Walter, D.Wang, N.Zin, M.Stocks, E.-C.Wang, N.Grant, Y.Wan, Y.Yang, X.Zhang, Z.Feng and P. J.Verlinden. *Design, fabrication and characterisation of a 24.4% efficient interdigitated back contact solar cell*. Progress in Photovoltaics: Research and Applications, pages n/a–n/a, 2014.
- [Fujiwara 2005] H.Fujiwara and M.Kondo. *Real-time monitoring and process control in amorphous/crystalline silicon heterojunction solar cells by spectroscopic ellipsometry and infrared spectroscopy*. Applied Physics Letters, vol. 86, no. 3, pages –, 2005.
- [Fujiwara 2007] H.Fujiwara, T.Kaneko and M.Kondo. *Application of hydrogenated amorphous silicon oxide layers to c-Si heterojunction solar cells*. Applied Physics Letters, vol. 91, no. 13, page 133508, 2007.
- [Geissbühler 2013] J.Geissbühler, S.De Wolf, B.Demaurex, J. P.Seif, D. T. L.Alexander, L.Barraud and C.Ballif. *Amorphous/crystalline silicon interface defects induced by hydrogen plasma treatments*. Applied Physics Letters, vol. 102, no. 23, pages –, 2013.
- [Geissbühler 2015] J.Geissbühler, J.Werner, S.Martin de Nicolas, L.Barraud, A.Hessler-Wyser, M.Despeisse, S.Nicolay, A.Tomasi, B.Niesen, S.De Wolf and C.Ballif. *22.5% efficient silicon heterojunction solar cell with molybdenum oxide hole collector*. Applied Physics Letters, vol. 107, no. 8, page 081601, 2015.
- [Geissbuhler 2014] J.Geissbuhler, S.De Wolf, A.Faes, N.Badel, Q.Jeangros, A.Tomasi, L.Barraud, A.Descoeudres, M.Despeisse and C.Ballif. *Silicon Heterojunction Solar*

Bibliography

- Cells With Copper-Plated Grid Electrodes: Status and Comparison With Silver Thick-Film Techniques*. Photovoltaics, IEEE Journal of, vol. 4, no. 4, pages 1055–1062, July 2014.
- [Glunz 2006] S.Glunz, A.Mette, M.Alemán, P.Richter, A.Filipovic and G.Willeke. *New concepts for the front side metallization of silicon solar cells*. in proceedings of the 21st European Photovoltaic Solar Energy Conference and Exhibition, Dresden, Germany, 2006.
- [Glunz 2007] S. W.Glunz, J.Nekarda, H.Mackel and A.Cuevas. *Analyzing back contacts of silicon solar cells by Suns-Voc-measurement at high illumination densities*. 2007.
- [Glunz 2012] S.Glunz, R.Preu and D.Biro. *1.16 - Crystalline Silicon Solar Cells: State-of-the-Art and Future Developments*. In A.Sayigh, editeur, Comprehensive Renewable Energy, pages 353 – 387. Elsevier, Oxford, 2012.
- [Gogolin 2014] R.Gogolin, M.Turcu, R.Ferre, J.Clemens, N.-P.Harder, R.Brendel and J.Schmidt. *Analysis of Series Resistance Losses in a-Si:H/c-Si Heterojunction Solar Cells*. Photovoltaics, IEEE Journal of, vol. 4, no. 5, pages 1169–1176, Sept 2014.
- [Granata 2012] S.Granata, T.Bearda, F.Dross, I.Gordon, J.Poortmans and R.Mertens. *Effect of an in-Situ {H₂} Plasma Pretreatment on the Minority Carrier lifetime of a-Si:H(i) Passivated Crystalline Silicon*. Energy Procedia, vol. 27, no. 0, pages 412 – 418, 2012. Proceedings of the 2nd International Conference on Crystalline Silicon Photovoltaics SiliconPV 2012.
- [Granek 2010] F.Granek. High-efficiency back-contact back-junction silicon solar cells. 2010.
- [Green 1982] M. A.Green. *Solar cells: operating principles, technology, and system applications*. University of NSW, 1982.
- [Green 1990a] M.Green. *Photovoltaics: coming of age*. in proceedings of the 21th Photovoltaic Specialists Conference, Kissimmee, USA, pages 1–8 vol.1, May 1990.
- [Green 1990b] M.Green, A. W.Blakers, J.Zhao, A. M.Milne, A.Wang and X.Dai. *Characterization of 23-percent efficient silicon solar cells*. Electron Devices, IEEE Transactions on, vol. 37, no. 2, pages 331–336, Feb 1990.
- [Green 2011] M. A.Green. *Ag requirements for silicon wafer-based solar cells*. Progress in Photovoltaics: Research and Applications, vol. 19, no. 8, pages 911–916, 2011.
- [Green 2015] M. A.Green, K.Emery, Y.Hishikawa, W.Warta and E. D.Dunlop. *Solar cell efficiency tables (Version 45)*. Progress in Photovoltaics: Research and Applications, vol. 23, no. 1, pages 1–9, 2015.
- [Greil 2011] S. M.Greil, N.Mingirulli, L.Korte, K.Hartmann, A.Schöpke, J.Rappich and B.Rech. *Etching of a-Si:H on c-Si absorber monitored by in situ photoluminescence measurements*. Energy Procedia, vol. 8, no. 0, pages 269 – 274, 2011. Proceedings of the SiliconPV 2011 Conference (1st International Conference on Crystalline Silicon Photovoltaics).

- [Greiner 2012] M. T.Greiner, M. G.Helander, W.-M.Tang, Z.-B.Wang, J.Qiu and Z.-H.Lu. *Universal energy-level alignment of molecules on metal oxides*. Nature materials, vol. 11, no. 1, pages 76–81, 2012.
- [Greiner 2013] M. T.Greiner and Z.-H.Lu. *Thin-film metal oxides in organic semiconductor devices: their electronic structures, work functions and interfaces*. NPG Asia Materials, vol. 5, no. 7, page e55, 2013.
- [Gretener 2013] C.Gretener, J.Perrenoud, L.Kranz, C.Baechler, S.Yoon, Y.Romanyuk, S.Buecheler and A.Tiwari. *Development of MoOx thin films as back contact buffer for CdTe solar cells in substrate configuration*. Thin Solid Films, vol. 535, no. 0, pages 193 – 197, 2013.
- [Griffin 2013] J.Griffin, D. C.Watters, H.Yi, A.Iraqi, D.Lidzey and A. R.Buckley. *The Influence of MoOx Anode Stoichiometry on the Performance of Bulk Heterojunction Polymer Solar Cells*. Advanced Energy Materials, vol. 3, no. 7, pages 903–908, 2013.
- [Hamwi 2010] S.Hamwi, J.Meyer, M.Kröger, T.Winkler, M.Witte, T.Riedl, A.Kahn and W.Kowalsky. *The Role of Transition Metal Oxides in Charge-Generation Layers for Stacked Organic Light-Emitting Diodes*. Advanced Functional Materials, vol. 20, no. 11, pages 1762–1766, 2010.
- [Haschke 2012] J.Haschke, N.Mingirulli and B.Rech. *Progress in Point Contacted Rear Silicon Heterojunction Solar Cells*. Energy Procedia, vol. 27, pages 116 – 121, 2012. Proceedings of the 2nd International Conference on Crystalline Silicon Photovoltaics SiliconPV 2012.
- [He 2003] T.He and J.Yao. *Photochromism of molybdenum oxide*. Journal of Photochemistry and Photobiology C: Photochemistry Reviews, vol. 4, no. 2, pages 125 – 143, 2003.
- [He 2007] T.He and J.Yao. *Photochromic materials based on tungsten oxide*. J. Mater. Chem., vol. 17, pages 4547–4557, 2007.
- [Heinstein 2013] P.Heinstein, C.Ballif and L.-E.Perret-Aebi. *Building integrated photovoltaics (BIPV): review, potentials, barriers and myths*. Green, vol. 3, no. 2, pages 125–156, 2013.
- [Hermans 2013] J.Hermans, R.van Knippenberg, E.Kamp, W.Brok, P.Papet, B.Legradic and B.Strahm. *Inkjet Printing for Solar Cell Mass Production on the PiXDRO JETx Platform*. presented at the 28th Eur. Photovoltaic Solar Energy Conf. Exhib., pages 780 – 784, 2013.
- [Hernandez 2012] J.Hernandez, D.Adachi, K.Yoshikawa, D.Schroos, E.Van Assche, A.Feltrin, N.Valckx, N.Menou, J.Poortmans, M.Yoshimi, Uto, H.T. Uzu, M.Hino, H.Kawasaki, M.Kanematsu, K.Nakano, R.Mishima, T.Kuchiyama, G.Koizumi, C.Allebé, T.Terashita, M.Hiraishi, N.Nakanishi and K.Yamamoto. *High Efficiency Copper Electroplated Heterojunction Solar Cells*. presented at the 27th Eur. Photovoltaic Solar Energy Conf. Exhib. Frankfurt, Germany, pages 655 – 656, 2012.

Bibliography

- [Hernández 2013] J.Hernández, D.Adachi, D.Schroos, N.Valckx, N.Menou, Uto, M.T. Hino, M.Kanematsu, H.Kawasaki, R.Mishima, K.Nakano, H.Uzu, T.Terashita, K.Yoshikawa, T.Kuchiyama, M.Hiraishi, N.Nakanishi, M.Yoshimi and K.Yamamoto. *High Efficiency Copper Electroplated Heterojunction Solar Cells and Modules – The Path towards 25% Cell Efficiency*. presented at the 28th Eur. Photovoltaic Solar Energy Conf. Exhib. Paris, France, pages 741 – 743, 2013.
- [Hänni 2014] S.Hänni. *Microcrystalline Silicon for High-Efficiency Thin-Film Photovoltaic Devices*. Ph.D. dissertation, Ecole Polytechnique Federale de Lausanne, 2014.
- [Hoex 2006] B.Hoex, S. B. S.Heil, E.Langereis, M. C. M.van de Sanden and W. M. M.Kessels. *Ultralow surface recombination of c-Si substrates passivated by plasma-assisted atomic layer deposited Al₂O₃*. Applied Physics Letters, vol. 89, no. 4, pages –, 2006.
- [Hoex 2008] B.Hoex, J. J. H.Gielis, M. C. M.van de Sanden and W. M. M.Kessels. *On the c-Si surface passivation mechanism by the negative-charge-dielectric Al₂O₃*. Journal of Applied Physics, vol. 104, no. 11, pages –, 2008.
- [Holman 2012] Z.Holman, A.Descoeudres, L.Barraud, F.Fernandez, J.Seif, S.De Wolf and C.Ballif. *Current Losses at the Front of Silicon Heterojunction Solar Cells*. Photovoltaics, IEEE Journal of, vol. 2, no. 1, pages 7–15, Jan 2012.
- [Holman 2013] Z. C.Holman, M.Filipič, A.Descoeudres, S.De Wolf, F.Smole, M.Topič and C.Ballif. *Infrared light management in high-efficiency silicon heterojunction and rear-passivated solar cells*. Journal of Applied Physics, vol. 113, no. 1, pages –, 2013.
- [Holman 2014] Z. C.Holman, M.Filipič, B.Lipovšek, S. D.Wolf, F.Smole, M.Topič and C.Ballif. *Parasitic absorption in the rear reflector of a silicon solar cell: Simulation and measurement of the sub-bandgap reflectance for common dielectric/metal reflectors*. Solar Energy Materials and Solar Cells, vol. 120, Part A, pages 426 – 430, 2014.
- [Hsieh 2009] S.Hsieh, C.Chien, W.Liu and W.Chen. *Failure behavior of ITO diffusion barrier between electroplating Cu and Si substrate annealed in a low vacuum*. Applied Surface Science, vol. 255, no. 16, pages 7357 – 7360, 2009.
- [Hupkes 2012] J.Hupkes, J. I.Owen, S. E.Pust and E.Bunte. *Chemical Etching of Zinc Oxide for Thin-Film Silicon Solar Cells*. ChemPhysChem, vol. 13, no. 1, pages 66–73, 2012.
- [i Morral 2002] A. Fi Morral and P. Ri Cabarrocas. *Etching and hydrogen diffusion mechanisms during a hydrogen plasma treatment of silicon thin films*. Journal of Non-Crystalline Solids, vol. 299–302, Part 1, no. 0, pages 196 – 200, 2002. 19th International Conference on Amorphous and Microcrystalline Semiconductors.
- [IEA 2014a] IEA. [Key World Energy Statistics](#). 2014.
- [IEA 2014b] IEA. [Technology Roadmap Solar Photovoltaic Energy](#). 2014.

- [Il Park 2011] S.Il Park, S.Jae Baik, J.-S.Im, L.Fang, J.-W.Jeon and K.Su Lim. *Towards a high efficiency amorphous silicon solar cell using molybdenum oxide as a window layer instead of conventional p-type amorphous silicon carbide*. Applied Physics Letters, vol. 99, no. 6, pages –, 2011.
- [Irfan 2012] I.Irfan and Y.Gao. *Effects of exposure and air annealing on MoO_x thin films*. Journal of Photonics for Energy, vol. 2, no. 1, pages 021213–1–021213–12, 2012.
- [ITRPV 2015] ITRPV. *International Technology Roadmap for Photovoltaic, 6th edition*. 2015.
- [Iwakuro 1996] H.Iwakuro, T.Kuroda, D. H.Shen and Z.Lin. *Enhanced dry etching of silicon with deuterium plasma*. Journal of Vacuum Science & Technology B, vol. 14, no. 2, 1996.
- [Jellison 1996] G. E.Jellison and F. A.Modine. *Parameterization of the optical functions of amorphous materials in the interband region*. Applied Physics Letters, vol. 69, no. 3, 1996.
- [Kail 2004] F.Kail, A.Fontcuberta I Morral, A.Hadjadj, P.Roca I Cabarrocas and A.Beorchia. *Hydrogen-plasma etching of hydrogenated amorphous silicon: a study by a combination of spectroscopic ellipsometry and trap-limited diffusion model*. Philosophical Magazine, vol. 84, no. 6, pages 595–609, 2004.
- [Kerr 2001] M. J.Kerr, J.Schmidt, A.Cuevas and J. H.Bultman. *Surface recombination velocity of phosphorus-diffused silicon solar cell emitters passivated with plasma enhanced chemical vapor deposited silicon nitride and thermal silicon oxide*. Journal of Applied Physics, vol. 89, no. 7, 2001.
- [Kerr 2002a] M. J.Kerr, A.Cuevas and R. A.Sinton. *Generalized analysis of quasi-steady-state and transient decay open circuit voltage measurements*. Journal of Applied Physics, vol. 91, no. 1, 2002.
- [Kerr 2002b] M.Kerr, P.Campbell and A.Cuevas. *Lifetime and efficiency limits of crystalline silicon solar cells*. presented at the 29th Photovoltaic Specialists Conference., pages 438–441, May 2002.
- [Khanna 2015] A.Khanna, K.-U.Ritzau, M.Kamp, A.Filipovic, C.Schmiga, M.Glatthaar, A. G.Aberle and T.Mueller. *Screen-printed masking of transparent conductive oxide layers for copper plating of silicon heterojunction cells*. Applied Surface Science, no. 0, pages –, 2015.
- [Kim 2008] B.-S.Kim, E.young Kim, H.-S.Jeon, H.-I.Lee and J.-C.Lee. *Study on the Reduction of Molybdenum Dioxide by Hydrogen*. MATERIALS TRANSACTIONS, vol. 49, no. 9, pages 2147–2152, 2008.
- [Kim 2011] J. H.Kim, Y. J.Lee, Y. S.Jang, J. N.Jang, D. H.Kim, B. C.Song, D. H.Lee, S. N.Kwon and M.Hong. *The effect of Ar plasma bombardment upon physical property of tungsten oxide thin film in inverted top-emitting organic light-emitting diodes*. Organic Electronics, vol. 12, no. 2, pages 285 – 290, 2011.

Bibliography

- [Kinoshita 2011] T.Kinoshita, D.Fujishima, A.Yano, A.Ogane, S.Tohoda, K.Matsuyama, Y.Nakamura, N.Tokuoka, H.Kanno, H.Sakata *et al.* *The approaches for high efficiency HIT solar cell with very thin ($< 100\mu\text{m}$) silicon wafer over 23%*. pages 871–874, 2011.
- [Knights 1979] J.Knights, G.Lucovsky and R.Nemanich. *Defects in plasma-deposited a-Si: H*. Journal of Non-Crystalline Solids, vol. 32, no. 1–3, pages 393 – 403, 1979. Electronic Properties and Structure of Amorphous Solids.
- [Kobayashi 2013] E.Kobayashi, N.Nakamura, K.Hashimoto and Y.Watabe. *Rear-emitter Silicon Heterojunction Solar Cells with Efficiencies Above 22%*. In proceedings of the 28st European Photovoltaic Solar Energy Conference and Exhibition, Paris, France, 2013.
- [Koida 2007] T.Koida, H.Fujiwara and M.Kondo. *Hydrogen-doped In_2O_3 as High-mobility Transparent Conductive Oxide*. Japanese Journal of Applied Physics, vol. 46, no. 7L, page L685, 2007.
- [Kuo 2004] Y.Kuo. Thin film transistors. 1. amorphous silicon thin film transistors, volume 1. Springer Science & Business Media, 2004.
- [Lachowicz 2014] A.Lachowicz, A.Faes, P.Papet, J.Geissbühler, J.Levrat, C.Allebé, N.Badel, J.Champlaud, F.Debrot, J.Cattin, A.Hessler Wyser, B.Strahm, S.De Wolf, M.Despeisse and C.Ballif. *Plating on Thin Conductive Oxides for Silicon Heterojunction Solar Cells*. Metallization Workshop, Konstanz, Germany, 2014.
- [Lammert 1977] M.Lammert and R. J.Schwartz. *The interdigitated back contact solar cell: A silicon solar cell for use in concentrated sunlight*. Electron Devices, IEEE Transactions on, vol. 24, no. 4, pages 337–342, Apr 1977.
- [Lennon 2013] A.Lennon, Y.Yao and S.Wenham. *Evolution of metal plating for silicon solar cell metallisation*. Progress in Photovoltaics: Research and Applications, vol. 21, no. 7, pages 1454–1468, 2013.
- [Li 2013] H.Li. *Open the Black Box: Understanding the Encapsulation Process of Photovoltaic Modules*. Ph.D. dissertation, École polytechnique fédérale de Lausanne (EPFL), 2013.
- [Lin 2009] S.-Y.Lin, Y.-C.Chen, C.-M.Wang, P.-T.Hsieh and S.-C.Shih. *Post-annealing effect upon optical properties of electron beam evaporated molybdenum oxide thin films*. Applied Surface Science, vol. 255, no. 6, pages 3868 – 3874, 2009.
- [Liu 2005] C.Liu, W.Liu, W.Chen, S.Hsieh, T.Tsai and L.Yang. *ITO as a diffusion barrier between Si and Cu*. Journal of The Electrochemical Society, vol. 152, no. 3, pages G234–G239, 2005.
- [Liu 2014] R.Liu, S.-T.Lee and B.Sun. *13.8% Efficiency hybrid Si/organic heterojunction solar cells with MoO_3 film as antireflection and inversion induced layer*. Advanced Materials, vol. 26, no. 34, pages 6007–6012, 2014.

- [Loper 2014] P.Loper, B.Niesen, S.-J.Moon, S.Martin de Nicolas, J.Holovsky, Z.Remes, M.Ledinsky, F.-J.Haug, J.-H.Yum, S.De Wolf and C.Ballif. *Organic 2013;Inorganic Halide Perovskites: Perspectives for Silicon-Based Tandem Solar Cells*. Photovoltaics, IEEE Journal of, vol. 4, no. 6, pages 1545–1551, Nov 2014.
- [Loper 2015] P.Loper, S.-J.Moon, S. M.De Nicolas, B.Niesen, M.Ledinsky, S.Nicolay, J.Bailat, J.-H.Yum, S.De Wolf and C.Ballif. *Organic–inorganic halide perovskite/crystalline silicon four-terminal tandem solar cells*. Physical Chemistry Chemical Physics, vol. 17, no. 3, pages 1619–1629, 2015.
- [Lorenz 1988] H.Lorenz. *Nouvelles Technologies de microfabrication de type UV-LIGA et fabrication de composants micromécaniques*. Ph.D. dissertation, Ecole Polytechnique Federale de Lausanne, 1988.
- [Lorenz 2015] A.Lorenz, A.Senne, J.Rohde, S.Kroh, M.Wittenberg, K.Krüger, F.Clement and D.Biro. *Evaluation of Flexographic Printing Technology for Multi-busbar Solar Cells*. Energy Procedia, vol. 67, no. 0, pages 126 – 137, 2015. Proceedings of the Fifth Workshop on Metallization for Crystalline Silicon Solar Cells.
- [Macco 2015] B.Macco, M. F. J.Vos, N. F. W.Thissen, A. A.Bol and W. M. M.Kessels. *Low-temperature atomic layer deposition of MoOx for silicon heterojunction solar cells*. physica status solidi (RRL) – Rapid Research Letters, vol. 9, no. 7, pages 393–396, 2015.
- [Madou 2002] M.Madou. Fundamentals of microfabrication: The science of miniaturization, crc press,second edition. 2002.
- [Marek 1984] J.Marek. *Light beam induced current characterization of grain boundaries*. Journal of Applied Physics, vol. 55, no. 2, 1984.
- [Masuko 2014] K.Masuko, M.Shigematsu, T.Hashiguchi, D.Fujishima, M.Kai, N.Yoshimura, T.Yamaguchi, Y.Ichihashi, T.Mishima, N.Matsubara, T.Yamanishi, T.Takahama, M.Taguchi, E.Maruyama and S.Okamoto. *Achievement of More Than 25%; Conversion Efficiency With Crystalline Silicon Heterojunction Solar Cell*. Photovoltaics, IEEE Journal of, vol. 4, no. 6, pages 1433–1435, Nov 2014.
- [Mazzarella 2015] L.Mazzarella, S.Kirner, B.Stannowski, L.Korte, B.Rech and R.Schlatmann. *p-type microcrystalline silicon oxide emitter for silicon heterojunction solar cells allowing current densities above 40mA/cm²*. Applied Physics Letters, vol. 106, no. 2, pages –, 2015.
- [Mews 2013] M.Mews, T. F.Schulze, N.Mingirulli and L.Korte. *Hydrogen plasma treatments for passivation of amorphous-crystalline silicon-heterojunctions on surfaces promoting epitaxy*. Applied Physics Letters, vol. 102, no. 12, pages –, 2013.
- [Meyer-Burger 2014a] Meyer-Burger. *Cell and module design from the LCOE perspective*. 2014.
- [Meyer-Burger 2014b] Meyer-Burger. *Heterojunction technology*. 2014.

Bibliography

- [Meyer 2008] J.Meyer, T.Winkler, S.Hamwi, S.Schmale, H.-H.Johannes, T.Weimann, P.Hinze, W.Kowalsky and T.Riedl. *Transparent inverted organic light-emitting diodes with a tungsten oxide buffer layer*. Adv. Mater, vol. 20, no. 20, pages 3839–3843, 2008.
- [Meyer 2012] J.Meyer, S.Hamwi, M.Kroger, W.Kowalsky, T.Riedl and A.Kahn. *Transition metal oxides for organic electronics: energetics, device physics and applications*. Advanced Materials, vol. 24, no. 40, pages 5408–5427, 2012.
- [Mingirulli 2011] N.Mingirulli, J.Haschke, R.Gogolin, R.Ferré, T.F.Schulze, J.Düsterhöft, N.-P.Harder, L.Korte, R.Brendel and B.Rech. *Efficient interdigitated back-contacted silicon heterojunction solar cells*. physica status solidi (RRL) – Rapid Research Letters, vol. 5, no. 4, pages 159–161, 2011.
- [Müllerová 2008] J.Müllerová, P.Šutta, G.van Elzakker, M.Zeman and M.Mikula. *Microstructure of hydrogenated silicon thin films prepared from silane diluted with hydrogen*. Applied Surface Science, vol. 254, no. 12, pages 3690 – 3695, 2008. Special Issue on Solid State Surfaces and Interfaces (SSSI 2006).
- [Moldovan 2015] A.Moldovan, F.Feldmann, M.Zimmer, J.Rentsch, J.Benick and M.Hermle. *Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO₂ layers*. Solar Energy Materials and Solar Cells, pages –, 2015.
- [Moralejo 2010] B.Moralejo, M.González, J.Jiménez, V.Parra, O.Martínez, J.Gutiérrez and O.Charro. *LBIC and Reflectance Mapping of Multicrystalline Si Solar Cells*. Journal of Electronic Materials, vol. 39, no. 6, pages 663–670, 2010.
- [Morales-Masis 2015] M.Morales-Masis, S.Martin De Nicolas, J.Holovsky, S.De Wolf and C.Ballif. *Low-Temperature High-Mobility Amorphous IZO for Silicon Heterojunction Solar Cells*. Photovoltaics, IEEE Journal of, vol. PP, no. 99, pages 1–8, 2015.
- [Morales-Vilches 2013] A.Morales-Vilches, C.Voz, M.Colina, G.Lopez, I.Martin, A.Orpella, J.Puigdollers, M.Garcia and R.Alcubilla. *Progress in silicon heterojunction solar cell fabrication with rear laser-fired contacts*. In Electron Devices (CDE), 2013 Spanish Conference on, pages 345–348, Feb 2013.
- [Mulligan 2011] W.Mulligan, M.Cudzinovic, T.Pass, D.Smith, N.Kaminar, K.McIntosh and R.Swanson. *Solar cell and method of manufacture*, March 1 2011. US Patent 7,897,867.
- [Munoz 2012] D.Munoz, T.Desrues, A.Ozanne, S.De Vecchi, S. M.de Nicolas, F.Jay, F.Souche, N.Nguyen, C.Denis, C.Arnalet *al.* *Key aspects on development of high efficiency heterojunction and IBC heterojunction solar cells: Towards 22% efficiency on industrial size*. page 576, 2012.
- [Nagel 1999] H.Nagel, C.Berge and A. G.Aberle. *Generalized analysis of quasi-steady-state and quasi-transient measurements of carrier lifetimes in semiconductors*. Journal of Applied Physics, vol. 86, no. 11, 1999.

- [Nakamura 2014] J.Nakamura, N.Asano, T.Hieda, C.Okamoto, H.Katayama and K.Nakamura. *Development of Heterojunction Back Contact Si Solar Cells*. Photovoltaics, IEEE Journal of, vol. 4, no. 6, pages 1491–1495, Nov 2014.
- [Nelson 2003] J.Nelson. The physics of solar cells, volume 57. Imperial College Press, 2003.
- [Notarp 2015] D. L.Notarp. *NB technologies*. 2015.
- [NREL 2015] NREL. *Research Cell Efficiency Records chart*. 2015.
- [OFEN 2014] OFEN. *Statistique suisse de l'électricité 2013*. 2014.
- [Olibet 2006] S.Olibet, E.Vallat-Sauvain and C.Ballif. *Effect of light induced degradation on passivating properties of a-Si:H layers deposited on crystalline Si*. Proceedings of the 21st EU PV Conference, Dresden, Germany, page 1366–1370, 2006.
- [Olibet 2007] S.Olibet, E.Vallat-Sauvain and C.Ballif. *Model for a-Si:H/c-Si interface recombination based on the amphoteric nature of silicon dangling bonds*. Phys. Rev. B, vol. 76, page 035326, Jul 2007.
- [Papet 2006] P.Papet, O.Nichiporuk, A.Kaminski, Y.Rozier, J.Kraiem, J.-F.Lelievre, A.Chaumartin, A.Fave and M.Lemiti. *Pyramidal texturing of silicon solar cell with {TMAH} chemical anisotropic etching*. Solar Energy Materials and Solar Cells, vol. 90, no. 15, pages 2319 – 2328, 2006. Selected Papers from the Solar Cells and Solar Energy Materials Symposium -IMRC 2005 {XIV} International Materials Research Congress.
- [Papet 2013] P.Papet, J.Hermans, T.Soderstrom, M.Cucinelli, L.Andreetta, D.Batzner, W.Frammelsberger, D.Lachenal, J.Meixenberger, B.Legradicet *al.* *Heterojunction solar cells with electroplated Ni/Cu front electrode*. vol. 30, 2013.
- [Paviet-Salomon 2015] B.Paviet-Salomon, A.Tomasi, A.Descoeurdes, L.Barraud, S.Nicolay, M.Despeisse, S.Wolf and C.Ballif. *Back-Contacted Silicon Heterojunction Solar Cells: Optical-Loss Analysis and Mitigation*. Photovoltaics, IEEE Journal of, vol. PP, no. 99, pages 1–11, 2015.
- [Pergament 2014] A.Pergament, V.Malinenko, L.Aleshina, E.Kazakova and N.Kuldin. *Electrical switching in thin film structures based on molybdenum oxides*. Journal of Experimental Physics, vol. 2014, 2014.
- [Perrin 2000] J.Perrin, J.Schmitt, C.Hollenstein, A.Howling and L.Sansonens. *The physics of plasma-enhanced chemical vapour deposition for large-area coating: industrial application to flat panel displays and solar cells*. Plasma Physics and Controlled Fusion, vol. 42, no. 12B, page B353, 2000.
- [Porter 1972] V. R.Porter, W. B.White and R.Roy. *Optical spectra of the intermediate oxides of titanium, vanadium, molybdenum, and tungsten*. Journal of Solid State Chemistry, vol. 4, no. 2, pages 250–254, 1972.

Bibliography

- [PVLighthouse 2015] PVLighthouse. *PV Lighthouse*. 2015.
- [Pysch 2007] D.Pysch, A.Mette and S.Glunz. *A review and comparison of different methods to determine the series resistance of solar cells*. Solar Energy Materials and Solar Cells, vol. 91, no. 18, pages 1698 – 1706, 2007.
- [Pysch 2011] D.Pysch, M.Bivour, M.Hermle and S. W.Glunz. *Amorphous silicon carbide heterojunction solar cells on p-type substrates*. Thin Solid Films, vol. 519, no. 8, pages 2550 – 2554, 2011.
- [Qiu 2015] Z.Qiu, C.Ke, A.Aberle and R.Stangl. *Efficiency Potential of Rear Heterojunction Stripe Contacts Applied in Hybrid Silicon Wafer Solar Cells*. Photovoltaics, IEEE Journal of, vol. 5, no. 4, pages 1053–1061, July 2015.
- [Reichel 2011] C.Reichel, F.Granek, M.Hermle and S. W.Glunz. *Investigation of electrical shading effects in back-contacted back-junction silicon solar cells using the two-dimensional charge collection probability and the reciprocity theorem*. Journal of Applied Physics, vol. 109, no. 2, pages –, 2011.
- [Richter 2012] A.Richter, S. W.Glunz, F.Werner, J.Schmidt and A.Cuevas. *Improved quantitative description of Auger recombination in crystalline silicon*. Phys. Rev. B, vol. 86, page 165202, Oct 2012.
- [Richter 2013] A.Richter, M.Hermle and S.Glunz. *Reassessment of the Limiting Efficiency for Crystalline Silicon Solar Cells*. Photovoltaics, IEEE Journal of, vol. 3, no. 4, pages 1184–1191, Oct 2013.
- [Robbins 1959] H.Robbins and B.Schwartz. *Chemical Etching of Silicon I. The System, and*. Journal of the electrochemical society, vol. 106, no. 6, pages 505–508, 1959.
- [Rohatgi 1980] A.Rohatgi, J.Davis, R.Hopkins, P.Rai-Choudhury, P.McMullin and J.McCormick. *Effect of titanium, copper and iron on silicon solar cells*. Solid-State Electronics, vol. 23, no. 5, pages 415 – 422, 1980.
- [Romeo 2004] A.Romeo, M.Terheggen, D.Abou-Ras, D.Batzner, F.-J.Haug, M.Kalin, D.Rudmann and A.Tiwari. *Development of thin-film Cu (In, Ga) Se₂ and CdTe solar cells*. Progress in Photovoltaics: Research and Applications, vol. 12, no. 2-3, pages 93–111, 2004.
- [Russell 2014] R.Russell, L.Tous, A.Uruena de Castro, I.Kuzma Filipek, D.Hendrickx, F.Duerinckx, J.Szlufcik, Y.Yao and T.Soederstroem. *Potential for Cu-free Ni Plated contacts Enabled by Smart Wire Connection Technology*. Presentation at 5th Workshop on Metallization for Crystalline Silicon Solar Cells, Konstanz, Germany, 2014.
- [Sato 1993] H.Sato, T.Minami, S.Takata and T.Yamada. *Transparent conducting p-type NiO thin films prepared by magnetron sputtering*. Thin Solid Films, vol. 236, no. 1–2, pages 27 – 31, 1993.

- [Schafer 2010] S.Schafer. *Cyanide free electrolyte composition for the galvanic deposition of a copper layer*. January 21 2010. WO Patent App. PCT/US2009/050,683.
- [Scherff 2011] M.Scherff. *Novel Methode for Preparation of Interdigitated Back Contacted a-Si:H/c-Si Heterojunction Solar Cells*. 2011.
- [Schroder 2006] D. K.Schroder. *Semiconductor material and device characterization*. John Wiley & Sons, 2006.
- [Schüttauf 2011] J.Schüttauf, C.van der Werf, W.van Sark, J.Rath and R.Schropp. *Comparison of surface passivation of crystalline silicon by a-Si:H with and without atomic hydrogen treatment using hot-wire chemical vapor deposition*. Thin Solid Films, vol. 519, no. 14, pages 4476 – 4478, 2011. Sixth international conference on hot-wire {CVD} (Cat-CVD) process.
- [Schultz 2008] O.Schultz, A.Mette, M.Hermle and S. W.Glunz. *Thermal oxidation for crystalline silicon solar cells exceeding 19% efficiency applying industrially feasible process technology*. Progress in Photovoltaics: Research and Applications, vol. 16, no. 4, pages 317–324, 2008.
- [Schulze 2011] T. F.Schulze, L.Korte, F.Ruske and B.Rech. *Band lineup in amorphous/crystalline silicon heterojunctions and the impact of hydrogen microstructure and topological disorder*. Phys. Rev. B, vol. 83, page 165314, Apr 2011.
- [Schuster 2001] C. E.Schuster, M. G.Vangel and H. A.Schafft. *Improved estimation of the resistivity of pure copper and electrical determination of thin copper film dimensions*. Microelectronics Reliability, vol. 41, no. 2, pages 239 – 252, 2001.
- [Schwartz 1975] R.Schwartz and M.Lammert. *Silicon solar cells for high concentration applications*. In Electron Devices Meeting, 1975 International, volume 21, pages 350–352, 1975.
- [Söderström 2013] T.Söderström, P.Papet and J.Ufheil. *Smart Wire Connection Technology*. presented at the 28th Eur. Photovoltaic Solar Energy Conf. Exhib., pages 495 – 499, 2013.
- [Seif 2014] J. P.Seif, A.Descoeurdes, M.Filipic, F.Smole, M.Topic, Z.Charles Holman, S.De Wolf and C.Ballif. *Amorphous silicon oxide window layers for high-efficiency silicon heterojunction solar cells*. Journal of Applied Physics, vol. 115, no. 2, pages –, 2014.
- [Seif 2015a] J.Seif. *Window Layers for Silicon Heterojunction Solar Cells: Properties and Impact on Device Performance*. Ph.D. dissertation, École polytechnique fédérale de Lausanne, 2015.
- [Seif 2015b] J.Seif, G.Krishnamani, B.Demaurex, C.Ballif and S.De Wolf. *Amorphous/Crystalline Silicon Interface Passivation: Ambient-Temperature Dependence and Implications for Solar Cell Performance*. Photovoltaics, IEEE Journal of, vol. 5, no. 3, pages 718–724, May 2015.

Bibliography

- [Semilab 2015] Semilab. *LBIC technique*, 2015.
- [Shinohara 2003] M.Shinohara, T.Kuwano, Y.Akama, Y.Kimura, M.Niwano, H.Ishida and R.Hatakeyama. *Interaction of hydrogen-terminated Si(100), (110), and (111) surfaces with hydrogen plasma investigated by in situ real-time infrared absorption spectroscopy*. Journal of Vacuum Science & Technology A, vol. 21, no. 1, 2003.
- [Shockley 1961] W.Shockley and H. J.Queisser. *Detailed Balance Limit of Efficiency of p-n Junction Solar Cells*. Journal of Applied Physics, vol. 32, no. 3, 1961.
- [Shrotriya 2006] V.Shrotriya, G.Li, Y.Yao, C.-W.Chu and Y.Yang. *Transition metal oxides as the buffer layer for polymer photovoltaic cells*. Applied Physics Letters, vol. 88, no. 7, pages –, 2006.
- [Sinton 1996] R. A.Sinton and A.Cuevas. *Contactless determination of current–voltage characteristics and minority carrier lifetimes in semiconductors from quasi steady state photoconductance data*. Applied Physics Letters, vol. 69, no. 17, 1996.
- [Sinton 2000] R.Sinton and A.Cuevas. *A quasi-steady-state open-circuit voltage method for solar cell characterization*. volume 25, 2000.
- [Smets 2003] A. H. M.Smets, W. M. M.Kessels and M. C. M.van de Sanden. *Vacancies and voids in hydrogenated amorphous silicon*. Applied Physics Letters, vol. 82, no. 10, 2003.
- [Smith 2012] D. D.Smith, P. J.Cousins, A.Masad, A.Waldhauer, S.Westerberg, M.Johnson, X.Tu, T.Dennis, G.Harley, G.Solomon *et al.* *Generation III high efficiency lower cost technology: Transition to full scale manufacturing*. In Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE, pages 001594–001597. IEEE, 2012.
- [Smith 2014] D.Smith, P.Cousins, S.Westerberg, R.De Jesus-Tabajonda, G.Aniero and Y.-C.Shen. *Toward the Practical Limits of Silicon Solar Cells*. Photovoltaics, IEEE Journal of, vol. 4, no. 6, pages 1465–1469, Nov 2014.
- [Stangl 2008] R.Stangl, J.Haschke, M.Bivour, M.Schmidt, K.Lips and B.Rech. *Planar rear emitter back contact amorphous/crystalline silicon heterojunction solar cells (RECASH / PRECASH)*. In Photovoltaic Specialists Conference, 2008. PVSC '08. 33rd IEEE, pages 1–6, May 2008.
- [Stangl 2009] R.Stangl, J.Haschke, M.Bivour, L.Korte, M.Schmidt, K.Lips and B.Rech. *Planar rear emitter back contact silicon heterojunction solar cells*. Solar Energy Materials and Solar Cells, vol. 93, no. 10, pages 1900 – 1903, 2009.
- [Stueckelberger 2014] M. E.Stueckelberger. *Hydrogenated amorphous silicon: impact of process conditions on material properties and solar cell efficiency*. Ph.D. dissertation, Ecole Polytechnique Federale de Lausanne, 2014.

- [Swanson 2005] R.Swanson. *Approaching the 29% limit efficiency of silicon solar cells*. In proceedings of the 21th IEEE Photovoltaic Specialists Conference, 2005, pages 889–894, Jan 2005.
- [Swanson 2006] R. M.Swanson. *A vision for crystalline silicon photovoltaics*. Progress in Photovoltaics: Research and Applications, vol. 14, no. 5, pages 443–453, 2006.
- [Sze 2001] S.Sze. *Semiconductor devices, Physics and Technology*. Wiley, 2001.
- [Taguchi 2008] M.Taguchi, E.Maruyama and M.Tanaka. *Temperature Dependence of Amorphous/Crystalline Silicon Heterojunction Solar Cells*. Japanese Journal of Applied Physics, vol. 47, no. 2R, page 814, 2008.
- [Taguchi 2014] M.Taguchi, A.Yano, S.Tohoda, K.Matsuyama, Y.Nakamura, T.Nishiwaki, K.Fujita and E.Maruyama. *24.7 % Record Efficiency HIT Solar Cell on Thin Silicon Wafer*. Photovoltaics, IEEE Journal of, vol. 4, no. 1, pages 96–99, Jan 2014.
- [Tanaka 1992] M.Tanaka, M.Taguchi, T.Matsuyama, T.Sawada, S.Tsuda, S.Nakano, H.Hanafusa and Y.Kuwano. *Development of New a-Si/c-Si Heterojunction Solar Cells: ACJ-HIT (Artificially Constructed Junction-Heterojunction with Intrinsic Thin-Layer)*. Japanese Journal of Applied Physics, vol. 31, no. 11R, page 3518, 1992.
- [Tate 1991] T. J.Tate, M.Garcia Parajo and M.Green. *Ion implantation effects in polycrystalline WO₃ thin films*. Journal of Applied Physics, vol. 70, no. 7, 1991.
- [Terakawa 2012] A.Terakawa and T.Asaumi. *Cellule photovoltaïque*. April 11 2012. EP Patent 1,696,492.
- [Terheiden 2015] B.Terheiden, T.Ballmann, R.Horbelt, Y.Schiele, S.Seren, J.Ebser, G.Hahn, V.Mertens, M. B.Koentopp, M.Scherff *et al.* *Manufacturing 100-um-thick silicon solar cells with efficiencies greater than 20% in a pilot production line*. physica status solidi (a), vol. 212, no. 1, pages 13–24, 2015.
- [Tiedje 1984] T.Tiedje, E.Yablonovitch, G.Cody and B.Brooks. *Limiting efficiency of silicon solar cells*. Electron Devices, IEEE Transactions on, vol. 31, no. 5, pages 711–716, May 1984.
- [Tomasi 2014] A.Tomasi, B.Paviet-Salomon, D.Lachenal, S.Martin de Nicolas, A.Descoeudres, J.Geissbuhler, S.De Wolf and C.Ballif. *Back-Contacted Silicon Heterojunction Solar Cells With Efficiency above 21 %*. Photovoltaics, IEEE Journal of, vol. 4, no. 4, pages 1046–1054, July 2014.
- [Tous 2012] L.Tous, D.van Dorp, R.Russell, J.Das, M.Aleman, H.Bender, J.Meersschaut, K.Opsomer, J.Poortmans and R.Mertens. *Electroless nickel deposition and silicide formation for advanced front side metallization of industrial silicon solar cells*. Energy Procedia, vol. 21, no. 0, pages 39 – 46, 2012. Proceedings of Third Metallization Workshop on Metallization for Crystalline Silicon Solar Cells.

Bibliography

- [Tracy 1986] C.Tracy and D.Benson. *Preparation of amorphous electrochromic tungsten oxide and molybdenum oxide by plasma enhanced chemical vapor deposition*. Journal of Vacuum Science & Technology A, vol. 4, no. 5, pages 2377–2383, 1986.
- [Trupke 2005] T.Trupke, R. A.Bardos and M. D.Abbott. *Self-consistent calibration of photoluminescence and photoconductance lifetime measurements*. Applied Physics Letters, vol. 87, no. 18, pages –, 2005.
- [Tsunomura 2009] Y.Tsunomura, Y.Yoshimine, M.Taguchi, T.Baba, T.Kinoshita, H.Kanno, H.Sakata, E.Maruyama and M.Tanaka. *Twenty-two percent efficiency {HIT} solar cell*. Solar Energy Materials and Solar Cells, vol. 93, no. 6–7, pages 670 – 673, 2009. 17th International Photovoltaic Science and Engineering Conference.
- [van der Heide 2002] A.van der Heide, J.Bultman, J.Hoomstra, A.Schonecker, G.Wyers and W.Sinke. *Optimizing the front side metallization process using the Corescan*. In Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE, pages 340–343, May 2002.
- [Van Oort 1987] R.Van Oort, M.Geerts, J.Van Den Heuvel and J.Metselaar. *Hydrogen plasma etching of amorphous and microcrystalline silicon*. Electronics Letters, vol. 23, no. 18, pages 967–968, 1987.
- [Varache 2015] R.Varache, O.Aguila, A.Valla, N.Nguyen and D.Munoz. *Role of the Front Electron Collector in Rear Emitter Silicon Heterojunction Solar Cells*. Photovoltaics, IEEE Journal of, vol. 5, no. 3, pages 711–717, May 2015.
- [Vecchi 2012] S. D.Vecchi, T.Desrues, F.Souche, D.Muñoz, P.-J.Ribeyron and M.Lemiti. *Point Contact Technology for Silicon Heterojunction Solar Cells*. Energy Procedia, vol. 27, pages 549 – 554, 2012. Proceedings of the 2nd International Conference on Crystalline Silicon Photovoltaics SiliconPV 2012.
- [Vinod 2011] P.Vinod. *Specific contact resistance measurements of the screen-printed Ag thick film contacts in the silicon solar cells by three-point probe methodology and TLM method*. Journal of Materials Science: Materials in Electronics, vol. 22, no. 9, pages 1248–1257, 2011.
- [Virtuani 2012] A.Virtuani, G.Rigamonti, P.Beljean, G.Friesen, M.Pravettoni and D.Chianese. *A fast and accurate method for the performance testing of high-efficiency C-Si photovoltaic modules using A 10 Ms single-pulse solar simulator*. In Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE, pages 000496–000500, June 2012.
- [Vorasayan 2009] P.Vorasayan, T.Betts, A.Tiwari and R.Gottschalg. *Multi-laser LBIC system for thin film PV module characterisation*. Solar Energy Materials and Solar Cells, vol. 93, no. 6–7, pages 917 – 921, 2009. 17th International Photovoltaic Science and Engineering Conference.

- [Wang 2010] Z. Y.Wang, S.-H.Lee, D.-H.Kim, J.-H.Kim and J.-G.Park. *Effect of NiO x thin layer fabricated by oxygen-plasma treatment on polymer photovoltaic cell*. Solar Energy Materials and Solar Cells, vol. 94, no. 10, pages 1591–1596, 2010.
- [Warta 1998] W.Warta, J.Sutter, B.Wagner and R.Schindler. *Impact of diffusion length distributions on the performance of mc-silicon solar cells*. In Proceedings of the 2nd World Conference on Photovoltaic Energy Conversion, pages 1650–1653, 1998.
- [Watahiki 2015] T.Watahiki, T.Furuhata, T.Matsuura, T.Shinagawa, Y.Shirayanagi, T.Morioka, T.Hayashida, Y.Yuda, S.Kano, Y.Sakai, H.Tokioka, Y.Kusakabe and H.Fuchigami. *Rear-emitter Si heterojunction solar cells with over 23% efficiency*. Applied Physics Express, vol. 8, no. 2, page 021402, 2015.
- [Werner 2015] J.Werner, G.Dubuis, A.Walter, P.Löper, S.-J.Moon, S.Nicolay, M.Morales-Masis, S. D.Wolf, B.Niesen and C.Ballif. *Sputtered rear electrode with broadband transparency for perovskite solar cells*. Solar Energy Materials and Solar Cells, vol. 141, no. 0, pages 407 – 413, 2015.
- [Woehl 2008] R.Woehl, M.Hörteis and S.Glunz. *Analysis of the optical properties of screen-printed and aerosol-printed and plated fingers of silicon solar cells*. Advances in Opto-Electronics, vol. 2008, 2008.
- [Wolf 1963] M.Wolf and H.Rauschenbach. *Series resistance effects on solar cell measurements*. Advanced Energy Conversion, vol. 3, no. 2, pages 455 – 479, 1963.
- [Wong 2012] K. H.Wong, K.Ananthanarayanan, J.Luther and P.Balaya. *Origin of Hole Selectivity and the Role of Defects in Low-Temperature Solution-Processed Molybdenum Oxide Interfacial Layer for Organic Solar Cells*. The Journal of Physical Chemistry C, vol. 116, no. 31, pages 16346–16351, 2012.
- [Wurfel 2015] U.Wurfel, A.Cuevas and P.Wurfel. *Charge Carrier Separation in Solar Cells*. Photovoltaics, IEEE Journal of, vol. 5, no. 1, pages 461–469, Jan 2015.
- [Yang 2015] W. S.Yang, J. H.Noh, N. J.Jeon, Y. C.Kim, S.Ryu, J.Seo and S. I.Seok. *High-performance photovoltaic perovskite layers fabricated through intramolecular exchange*. Science, vol. 348, no. 6240, pages 1234–1237, 2015.
- [Zhao 1995] J.Zhao, A.Wang, P.Altermatt and M. A.Green. *Twenty four percent efficient silicon solar cells with double layer antireflection coatings and reduced resistance loss*. Applied Physics Letters, vol. 66, no. 26, 1995.
- [Zhao 1998] J.Zhao, A.Wang, M. A.Green and F.Ferrazza. *19.8% efficient “honeycomb” textured multicrystalline and 24.4% monocrystalline silicon solar cells*. Applied Physics Letters, vol. 73, no. 14, 1998.
- [Zicarelli Fernandez 2010] F.Zicarelli Fernandez, A.Descoeudres, G.Choong, P.Bôle, L.Barraud, S.De Wolf and C.Ballif. *Metallisation for Silicon Heterojunction Solar Cells*. In proceedings of the 25th EUPVSEC, Valencia, Spain, 2010.

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Neuchâtel, le 26 octobre 2015

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- J. Geissbühler, S. De Wolf, B. Demarex, J. P. Seif, D. T. L. Alexander, L. Barraud and C. Ballif, "Amorphous/crystalline silicon interface defects induced by hydrogen plasma treatments", [Appl. Phys. Lett.](#) **102**, 231604 (2013)
- J. Geissbühler, S. De Wolf, A. Faes, N. Badel, Q. Jeangros, A. Tomasi, L. Barraud, A. Descoeudres, M. Despeisse, and C. Ballif, "Silicon Heterojunction Solar Cells With Copper-Plated Grid Electrodes: Status and Comparison With Silver Thick-Film Techniques", [IEEE J. Photovoltaics](#) **4**, 4 (2014)
- J. Geissbühler, J. Werner, S. Martin de Nicolas, L. Barraud, A. Hessler-Wyser, M. Despeisse, S. Nicolay, A. Tomasi, B. Niesen, S. De Wolf, and C. Ballif, "22.5% efficient silicon heterojunction solar cell with molybdenum oxide hole collector", [Appl. Phys. Lett.](#) **107**, 081601 (2015)