Engineered substrates with embedded strain relief for stretchable thin-film electronics

THÈSE N^{O} 6798 (2015)

PRÉSENTÉE LE 6 NOVEMBRE 2015

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
CHAIRE FONDATION BERTARELLI DE TECHNOLOGIE NEUROPROSTHÉTIQUE
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

PAR

Alessia ROMEO

acceptée sur proposition du jury:

Prof. H. Shea, président du jury
Prof. S. Lacour, directrice de thèse
Prof. A. R. Studart, rapporteur
Prof. J. P. Conde, rapporteur
Prof. J. Brugger, rapporteur

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE
Suisse
2015

Abstract

Stretchable electronics are integrated circuitry that can reversibly expand and relax while retaining their functionality. This emerging technology has great potential in unconventional electronic application areas, especially in biomedical sector. To attain stretchability, new class of substrates, based on highly elastic polymers, have to be used. The resulting stretchable circuits are hybrid systems, combining *hard* functional materials on *soft* substrates. However, manufacturing of stretchable electronics sets new challenges due to significantly different material properties between the stretchable substrates and electronic devices, and,therefore, optimized mechanical architectures are required.

In this thesis a simple and robust approach to design and manufacture stretchable substrate for stretchable electronic applications is reported. The proposed solution is based on engineered stretchable substrates with embedded strain relief. The substrate is engineered by embedding stiff platfroms within a soft elastomer. Since the platforms are significantly stiffer than the surrounding silicone matrix, the stiff regions distributed across the substrate allow for large global strains with local areas that remain un-strained. These local, un-strained regions act as non-stretchable areas on the plain top surface of the elastomer, which can host brittle devices and protect them from exceeding their fracture strain. Optimization of the platforms geometry and layout, as well as, grading of the mechanical compliance at the rigid-to-soft transition zones have been performed to adjust the strain distribution on the top surface. Associated design rules to produce stretchable circuits based on experimental as well as modeling data are presented.
This innovative approach is compatible with conventional, additive thin-film processing. Direct integration of metal oxide thin film transistors onto the planar but mechanically engineered heterogeneous elastic substrate is demonstrated. IGZO TFTs interconnected with stretchable metallization spanning across the rigid platform were manufactured directly on the non deformable elastomer regions, using standard, dry and low temperature processing. IGZO TFT could sustained applied tensile strain up to 20% without electrical degradation and mechanical fracture.
Elastomeric substrates with engineered strain relief are, thus, a promising solution to carry reliable and durable stretchable electronics.

Additionally, concurrent mechanical and structural photopatterning in photosensitive elastomer was discovered.
To date, photosensitive elastomers have mainly been implemented in soft lithography or to locally modulate the elasticity. This thesis demonstrates that shape and stiffness can be

engineered in a single elastomeric membrane using simple UV exposure through standard photolithography mask. Modulating the UV dose defines mechanical stiffness gradient within the elastomer as well as topography across the elastomer surface. This process eliminates lithography wet development step therefore offers a new technique to silicone microstructuring, allowing for mold and development free 3D patterning of microfluidic channels. Therefore, single-step photopatterning of photosensitve elastomers enables for rapid prototyping approach for soft MEMS, microfluidics and stretchable electronic.

Keywords: stretchable electronics, mechanical patterning, thin film transistor (TFT), IGZO, photosensitive elastomer.

Sintesi

L'elettronica estensibile permette ai circuiti elettronici di espandersi e rilassarsi senza che il loro funzionamento venga. Questa nuova tecnologia possiede un grande potenziale per applicazioni in aree non convenzionali dell'elettronica, ad esempio, nel settore biomedicale. Per rendere un circuito elettrico estensibile è necessario l'utilizzo di una nuova classe di substrati, basata su polimeri altamente elastici. I circuiti estensibili che ne derivano sono sistemi ibridi, che combinano materiali funzionali, tipicamente rigidi, con substrati deformabili. Di conseguenza, la produzione di elettronica estensibile richiede nuove sfide dovute alla grande differenza tra le proprietá meccaniche dei materiali utilizzati per i substrati estensibili ed i dispositivi elettronici. Pertanto é perció necessaria un'ottimizzazione dell'architettura meccanica.

In questa tesi viene presentato un nuovo approccio per progettare e realizzare un substrato elastico che possa essere utilizzato per realizzare circuiti estensibili. La soluzione proposta è basata su un substrato estensibile con *strain relief* integrato. Il substrato è stato progettato integrando piattaforme rigide all'interno di una matrice elastica. Dato che le piattaforme sono significativamente piú rigide rispetto alla matrice elastica che le circonda, all'allungamento del substrato, alcune zone in corrispondenza delle piattaforme rimangono non-deformate. Queste regioni rigide formano delle aree non estensibili sulla superficie superiore dell'elastomero, le quali sono idonee ad ospitare i dispositivi elettronici, impedendo che questi vengano deformati fino alla rottura. Per migliorare la distribuzione della deformazione sulla superficie superiore del substrato, sono state eseguite sia l'ottimizzazione della geometria e del *layout* delle piattaforme, sia la modulazione della rigiditá in corrispondenza delle zone di transizione tra le regioni rigide e quelle elastiche. In questo studio, si definiscono le regole per la progettazione e la realizzazione di circuiti estensibili, basate sia sui risultati sperimentali, sia sui dati di modellazione.
Questo approccio innovativo è compatibile con le tecniche convenzionali di lavorazione a film sottile. Si dimostra l'integrazione diretta di *thin film transistors*, basati su ossido di metallo, sul substrato elastico ingegnerizzato. IGZO TFTs, interconnessi con metallizzazioni elastiche, sono stati fabbricati direttamente sulle regioni non deformabili del substrato, utilizzando tecniche di fabbricazione standard a bassa temperatura. E'stato dimostrato che IGZO TFT puó sostenere deformazioni fino al 20 % senza alcun deterioramento delle sue prestazioni elettriche né frattura meccanica.
Il substrato elastomerico, con *strain relief* integrato, offre, perció , una soluzione promettente per sviluppare circuiti estensibili affidabili e durevoli.

E'inoltre presentato il *photopatterning* simultaneo, meccanico e strutturale, degli elastomeri fotosensibili.
Fino ad oggi, gli elastomeri fotosensibili sono stati usati principalmente in *soft photolithography* o per modulare a localmente il livello di elasticitá. Questa tesi dimostra che sia la forma sia la rigiditá possono essere progettati in un'unica membrana elastomerica semplicemente con l'esposizione ai raggi UV tramite una maschera fotolitografica standard. Modulando la dose UV è possibile definire un gradiente di rigiditá meccanica all'interno dell'elastomero, cosícome la topografia della superficie dello stesso. Questo processo elimina lo step di sviluppo in soluzione, tipico della fotolitografia, offrendo quindi una nuova tecnica per il *microstructuring* del silicone e consentendo lo sviluppo di patterns 3D per la formazione di canali microfluidici. Pertanto, il *single-step photopatterning* degli elastomeri fotosensibili consente un nuovo approccio per la prototipazione rapida di soft MEMS, microfluidica ed elettronica estensibile.

Parole chiave: elettronica estensibile, patterning meccanico, transistori a film sottile (TFT), IGZO, elastomeri fotosensibili.

Acknowledgements

It has been a long, but fortunately not lone journey towards the degree of Ph.D. It took more than four years to complete it and a fair amount of initiative, dedication and perseverance. This would not have been possible without the support and encouragement that I received along the way from a number of great people.

I would first like to thank my advisor, Professor Stéphanie Lacour for providing me with the opportunity to be part of the Laboratory of Soft Bioelctronic Interfaces (LSBI). She patiently supported and encouraged my work throughout my PhD. From her, I learned how to think and plan independently, how to handle stressful situations. I believe these skills will continue to be tremendously helpful after my graduation from EPFL.

I would like to thank the members of the jury, who read through my manuscript and provided me with solid feedback. I thank Prof. Herbet Shea, president of the jury and head of the Microsystem for Space Technologies Laboratory at EPFL, Prof. André R. Studart head of the Complex Materials group at ETHZ and Prof. Joao Pedro Conde from the Department of Bioengineering at the University of Lisbon. A special thank goes to Prof. Jugger Brugger, head of the Microsystems Laboratory 1 at EPFL, who took the time to personally discuss some points of the manuscript.

I would like to thank Prof. Zhingang Suo and Qihan Liu from the Mechanics of Materials and Structures Group at Harvard University, for their help in thin film mechanics. Their contributions to micromechanics modelling were very helpful to complete a part of my research.

It would be unthinkable to finish any device batch without the help of the staff of the EPFL Center of MicroNanoTechnology (CMi), who I thank for their precious support with the cleanroom equipment. They have been exceptionally responsive and ready to help.

My thanks go out to present and past members of the entire LSBI for their friendliness and daily presence, which created a pleasant working environment. To Amèlie, Arthur, Hadrien, Cedric, Kate, Huge, Tom, Sandra, Frèdèric, Nicolas, Laurent, Kristie, Anna and Yi-lin, with whom I shared scientific discussions, coffee/lunch breaks and lab outings. A particular thanks go to Aaron Gerratt and Ivan Minev. The discussions with them on various aspects of the project have been helpful and inspiring. I would also like to thank Tero Kulmala. Even if for a short period, it was great working together on the transistors. Many thanks go to Swati

Gupta.In the last year, she has always been willing to discuss the experimental results and answer my questions. A special thank goes to Alba de Luca, for her sense of humor and the emotional support she gave me in the final part of my PhD. More than a colleague she has been a friend.

Furthermore, I would like to thank Marco, Pietro ed Enrica for having played at my jury members asking me a lot of interesting questions and giving me important feedbacks.
A special thank goes to Marco Letizia, who fully support me over these four years. I am truly grateful for sharing his experience and his time with me, for soothing away many anxieties in my graduate and private life and to be such a great friend.

I would also like to thank all my friends who made my life outside of EPFL extraordinary, full of great days and nights in and around Lausanne. A special thank go to Alberto for being more than just flatmates but also a friend; to Giulia for her delicious dinners; to Marta for her guidance over these years; to Carlo for his enthusiasm, his support and the interesting social and political discussions; to Erica for the runs, the hiking, the chats and the rest...
I would also like to thanks the fellows from ITALaus, with whom we organized so many successful events, and to all the team mates of Sfigatos, with whom we had such a great time playing and winning the EPFL volleyball tournament.

Thanks to my "evergreen"friends from Minervino: Ciccio, Stefania, Salvatore, Antonio, Sara, Rosalba e Carmine, that made me laugh almost everyday over these years, even at hundreds km of distance. I also would like to thank my historical friends from Milan: Giulia, Andrea Gabriele, Patato and Federica for being always part of my life.

My greatest thanks goes to my family. To my parents for their unconditional support and trust they have put in me. I would like to dedicate this work to them. To my sister, who was always there for me, for her priceless understanding, advices and love. To Giosué for cheering me up with his crazy stories and his delightful company.

And finally, I would like to thank my beloved Alessio, for his support, patience and encouragement he gave me in the last part of this intense experience. Thank you Ale for being beside me because you are able to bring out the best in me.

Table of Contents

List of Figures

List of Tables

1 Introduction

This chapter gives the motivation and a brief overview on the state of the art on stretchable electronics. The objectives and the outline of this thesis are separately described.

1.1 Motivation

Stretchable electronics are integrated circuitry that can reversibly expand and relax while maintaining their functionality. Stretchability ensures the electronic circuits can conform curved and complex shaped objects and comply to the elastic surfaces that expand and relax. Stretchable devices provide interesting opportunities, particularly in biomedical applications, where shape adaptability is a highly desirable feature, enabling for example skin like circuits for health care monitoring.
These applications are hardly achievable with conventional planar, rigid and brittle silicon-based electronic circuits. Therefore, there is currently a strong tendency integrate circuits on elastic carriers. While the semiconducting devices do not stretch, substrate and electrical interconnects take up the applied deformation.

Stretchability can be introduced into electronic systems by the use of suitable stretchable substrate materials, hosting rigid electronic components interconnected with elastic wiring. The resulting stretchable systems are therefore hybrids of soft and hard materials, which mechanical and thermal properties differ by several orders of magnitude. The realization of stretchable electronics is still a challenge since the integration of brittle and fragile device materials with elastomeric substrates is limited among others by two main critical issues: (i) electronic device materials are brittle and typically fracture at 1-2% tensile strain, and (ii) maximum working temperature imposed by the soft substrate is limited to $< 150°C$.
In order to integrate such disparate materials, it is essential to carefully select the device materials and associated processing techniques, and derive reliable circuits's mechanical architectures ensuring the most fragile elements are strain-free.

1.1.1 Stretchable electronics

Conventional electronic circuits are constructed on planar, rigid substrates, (*e.g.* silicon). Although they exhibit remarkable electronic performance and stability, they possess poor mechanical robustness. They may face limitations when placed in environments that are dominated by stretchable or three-dimensional structures, including those within the human body. Recent studies have led to the development of a new class of electronics with improved mechanical features. A first way to convey mechanical compliance to electronic circuit was the development of flexible electronics, which enables electronic devices to be bendable, rollable and even wearable. Electronics could be made flexible by patterning thin film device materials onto freestanding flexible substrate [1]. Fabrication of flexible electronics is nowadays well established in the research and the industrial communities.
However, the ability to be bent is not enough to satisfy compliance needs, for devices that intimately integrate with the human body [2–7]. Stretchable electronics is a relatively new field, emerging from flexible electronics. Imagine an electronic skin, that senses like a real skin and needs to be applied conformally on a prosthetic arm. As the arm moves, the system is subjected to various levels of strain. For example, the skin wrapped over the elbow stretchs and relaxes many times to $\sim$15% strain [8]. This requirement is impossible to meet with designs that offer only bendability. Stretchability demands that the circuits have the capacity to absorb large levels of strain (>1%) and often multiaxial deformations without fracture or significant degradation in their electronic properties.

Applications

Stretchable electronics offer exciting opportunities in the biomedical field.
Stretchable electronics would allow electronic circuits to be "perfectly"attached to any organ in the body and monitor or assist its functions for health monitoring or treatment. Stretchable microelectrode arrays (SMEA) that conform complex surfaces or operate in mechanically active environments have been produced [9–12]. Figure 1 highlights some of the recent developments in stretchable electronics for body interfaces. Figure 1.1a displays a stretchable neural implants, called electronic dura matter, because its mechanical properties match those of natural dura matter. The proposed solution embeds interconnects, electrodes and chemotrode, and was implemented to deliver electrochemical spinal neuromodulation that restored locomotion after paralyzing spinal cord injury. [6] . Stretchable electronics have also been used for biological monitoring devices. Deformable arrays of multifunctional sensors and electronic components were developed to monitor the function of the beating heart (Fig. 1.1b) [13, 14]. Also, tattoo-like epidermal electronic systems, extremely thin and perfectly conformable, were mounted onto the surface of the skin to record electrical activity produced by the heart, brain, and skeletal muscles (Fig. 1.1c) [15]. Electronic eye which is able adjust thickness of lens was developed [16, 17]. Moreover, stretchable sensing systems which mimic the mechanical properties and tactile and temperature sensing properties of human skin

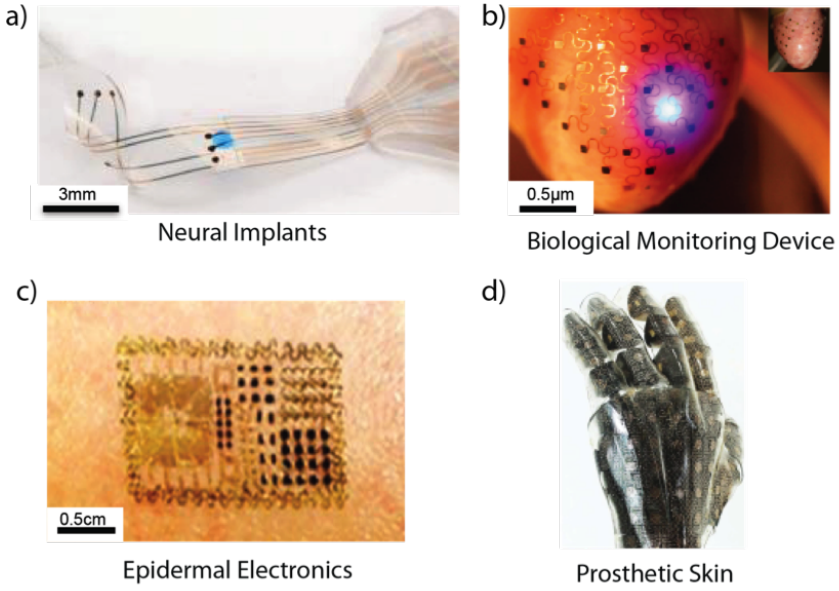


Figure 1.1: Four examples of stretchable electronics are presented: a) stretchable neural implants embedding electrods and chemotrode for spinal cord stimulation, e-dura, the image is adopted from Minev et al. [6]; b) 3D deformable membrane for spatiotemporal cardiac measurements and stimulation across the entire epicardium, the image is adopted fromXu et al. [13]; c) epidermal electronic for electrophysiological characterizatelectronic ion of human skin, the image is taken from Kim et al. [15]; d) electronic artificial skin or E-skin, where organic devices are used to read out pressure images from the sensors, the image is taken from Someya et al. [24]

have been attracting significant interest, as shown in figure 1.1d [8, 18–22]. Electronic skin (e-skin) are crucial property for future generation robots or to produce prosthetic limbs that would "feel "like the natural limb [23, 24].

Fabrication Strategies

If stretchability of electronic circuits opens to a new class of applications, an important associated challenge is the manufacturing of stretchable electronic devices.
Stretchable electronics are hybrid systems, combining mechanically disparate, soft and hard, materials within a single structure [25]. Figure 1.2 illustrate the rage of Young's modulus of the materials employed in stretchable electronics. In most cases, the carrier substrate is an elastic or viscoelastic polymer, e.g., silicones or polyurethanes, characterized by low elastic modulus (E$<$ 10 MPa), large ductility (elongation at break$>$ 100%), Poisson's ratio ν close to 0.5, and thickness in the 10 μm to 1 mm range. By contrast, electronic device materials, used either in thin-film or thinned forms, are stiff (elastic modulus in the GPa range), brittle

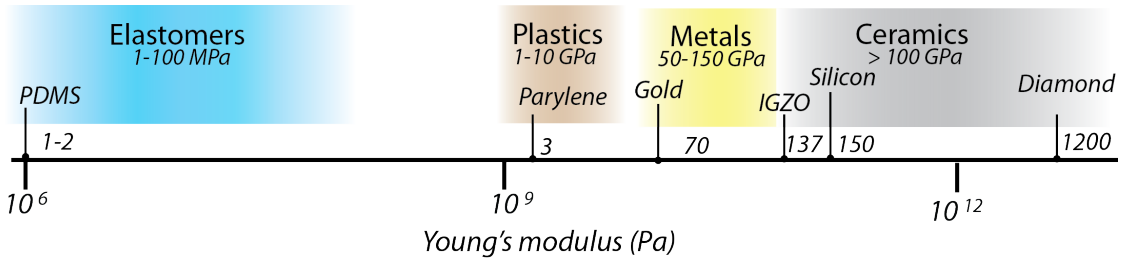


Figure 1.2: The wide range of Young's modulus of different types of materials used for stretchable electronics.

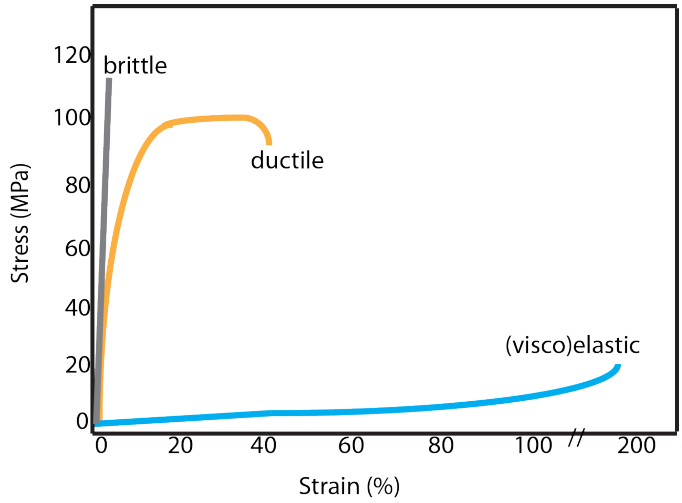


Figure 1.3: Stress-strain behavior of brittle, ductile and elastic materials.

(fracture strain $< 5\%$), and thin (thickness$< 1\mu m$) [26]. Figure 1.3 illustrates three types of stress-strain behavior of respectively a brittle (e.g. *Silicon*), ductile (*e.g. metals*) and elastic (*e.g. silicone*) materials. The integration of these materials onto elastic substrates to implement stretchable devices is a primary challenge and requires a carefully mechanical design.

To overcome this mechanical mismatch, different strategies have been proposed, where mechanics meets geometry to enable large, reversible deformation of the structure.

A first approach relies on a wavy layout. Thin-film devices are prepared on sacrificial substrate and then transferred on a prestretch elastomer. Upon releasing of the strain, the films relax into a strain-induced wavy geometry (Fig.1.4a) that enables the stretchable system to sustain strain to up the initial prestretch [29–32]. However, this technique limits the stretchability of the circuit to a predefined direction.
A related strategy is to pattern the substrate to enable the film to flex out of the plane of the strain. Instead of adhering completely on top of the elastomeric substrate, the circuits

are patterned in an open mesh layouts and locally bonded to the prestretched stretchable matrix, as shown in figure 1.4b. When the pre-strain is released the "not-attached"areas form out-of-plane but controlled buckling that can more effectively accommodate macroscopic strain [16, 33, 34]. The functional devices are deposited on non-wavy (non-stretchable) islands to ensure reliable electromechanical performance. The out-of-plane buckling structure interconnects the functional islands and accommodates the deformation. Sophisticated "pick-and-place"steps to transfer the devices onto the pre-strained substrate are required to achieve such complex layouts. This open mesh layout is based on the pixellated architecture, commonly used for stretchable electronics. Figure 1.5 shows a schematic of the pixellated macroscopic structure [35–37]. Here, the "pixels"or nodes are made of hard materials for device placement and distributed on the surface of an elastomeric substrate and interconnected with elastic wiring. When the stretchable system is deformed, the soft elastomeric substrate, together with the elastic interconnects, support the mechanically rigid nodes and isolates them from the applied macroscopic strain. This prevents fragile device materials from exposure to deformation exceeding their fracture strain, while ensuring the circuit deforms.

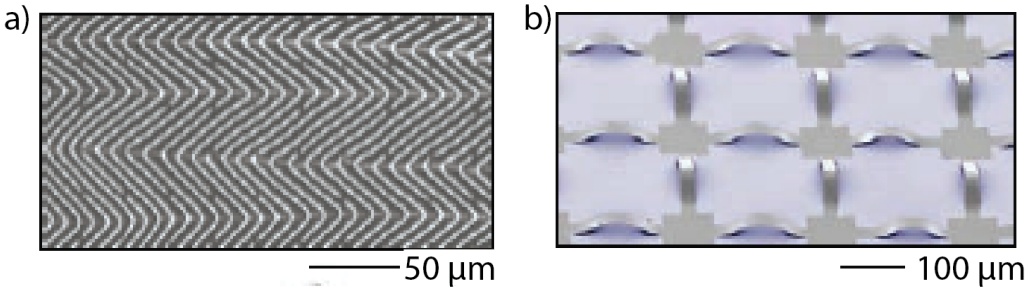


Figure 1.4: Concept of stretchable electronics with wavy and open mesh layout of a 100 nm thick silicon membrane: a) stretchable thin silicon membrane configured in a wavy shape and bonded to a piece of rubber; b) stretchable thin silicon membrane patterned into a mesh geometry and geometry and bonded to a rubber substrate only at square pads located between arc shaped bridge structures. The images are adopted from Rogers et al. [27].

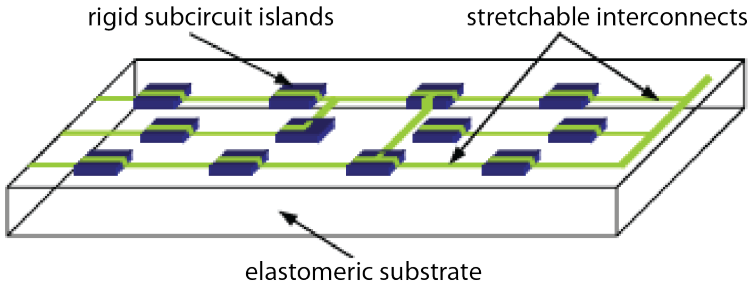


Figure 1.5: Concept of pixellated architecture for stretchable electronics. Rigid subcircuit islands are distributed on an elastomeric substrate. The cells are interconnected with stretchable metallization. The image is adopted from Lacour et al. [28].

Stretchable Interconnects

Since the stretchable conductors have to withstand most of the deformations, a reliable design is essential to avoid losing electrical performance and structural integrity. Different materials have been employed to produce highly stretchable interconnects, such as conductive polymer composites [41–43], carbon based materials [31, 44–46], liquid metal [47], metal nanowires [48, 49], nanoparticles [50, 51] and thin metal films [38, 39, 52]. Among these, stretchable metallization based on thin gold films on rubbery substrate has received significant interest and research efforts. It was demonstrated that thin gold films well attached on polymeric substrates are more resistant to tensile strain than free standing films, since strain is delocalized over the whole area [53, 54]. Combining this ability with proper strain relief patterns produces highly stretchable metallization bonded to elastomeric substrates. Technologies based on wavy layout [38, 55] and coplanar [39, 56], or off-plane [40] meandering structures, have been adopted to provide strain relief within the interconnects. Figure 1.6 gives an examples of the three different strategies. However, they are difficult to fabricate, requiring complicated layout and process flow.

In 2005 by Lacour et al.proposed an alternative strategies whg ere the strain relief patterns are embedded in thin metal film omitting the need of complex layouts [57] . The authors demonstrated that thin gold films, deposited by evaporation onto silicone substrates, support an unique micro-cracked topography (Fig. 1.7) that allows films to stretch up to and beyond 20% tensile strain, for repeated cycles, without electrical failure [58]. The strain-induced cracks are formed in the continuous thin film of the deposited metal while maintaining a

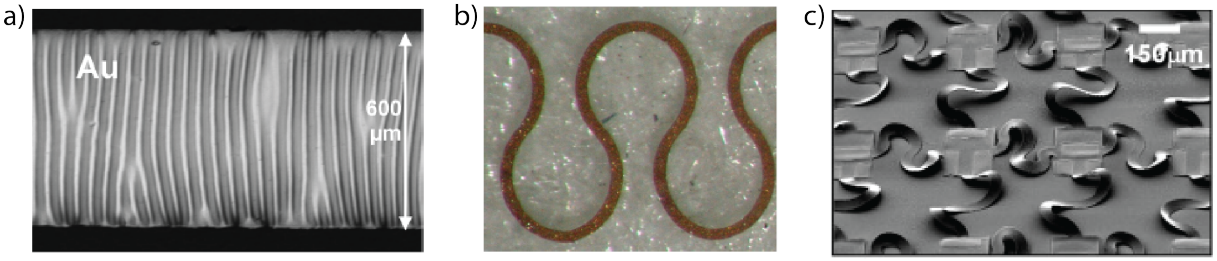


Figure 1.6: Different relief patterns of stretchable thin gold interconnects. a) wavy layout: built-in waves are observed in gold conductor patterned on relaxed PDMS. The wavelength is $25\mu m$, the image is adopted from Lacour et al. [38]. b) coplanar meandering structure: horseshoe metal interconnects embedded into PDMS matrix, the image is adopted from Gonzalez et al. [39]. c) off-plane meandering structure: noncoplanar conductors bridges with serpentine layouts, the image is adopted form Kim et al. [40].

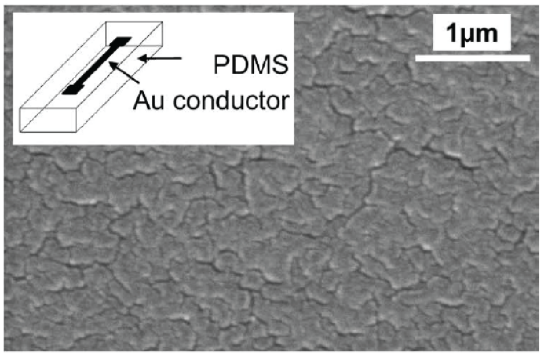


Figure 1.7: Thin gold film deposited onto PDMS substrate: the gold ligaments percolate between the micron-size microcracks. The inset illustrates the schematic of a gold conductor on PDMS. The image is adopted from Lacour et al. [57].

percolating pathway which ensure the reversible elasticity of the gold film. Rational control of the crack formation process can improve the stretchability to values as large as 100% in gold films [59, 60]. Microcracked thin gold film, thus offer a simple and straightforward method for stretchable interconnects, forgoing complex layout and fabrication process.

1.1.2 TFTs on Stretchable Substrates

Beside stretchable electrical interconnections, thin film transistors (TFTs) are the basic element for electronic circuits. Several advanced stretchable organic and inorganic TFTs with elastic conductors, prepared using pixellated design, have recently been demonstrated [2, 4, 18].
One of the common fabrication approaches to produce stretchable electronics is based on the transfer techniques, where the soft elastomeric polymer is introduced only after all the high-temperature fabrication steps have been completed. Here active device materials are first deposited and patterned on a rigid or plastic substrate, using standard high-temperature fabrication steps. The substrate is then machined into a thin mesh defining the rigid nodes, and subsequently transferred onto the elastic matrix [9, 13, 16, 30, 52, 61]. These approaches allow for stretchable circuits with good electronic performance and stability, however, it requires complex, multi-step, multi-carrier processing.

An alternative way to implement stretchable circuits is to fabricate the thin film devices directly on the elastic substrates by planar and standard cleanroom methods. Fabricating functional devices directly on elastomeric substrates brings unique challenges such as compatibility with microfabrication process, patterning resolution and reproducibility. In particular, two technological challenges need to be overcome: (i) the limitation on the maximum process temperature due to the polymeric nature of the substrate, and (ii) the chemical stability of the substrate. Organic and inorganic TFTs, using respectively pentacene and amorphous silicon

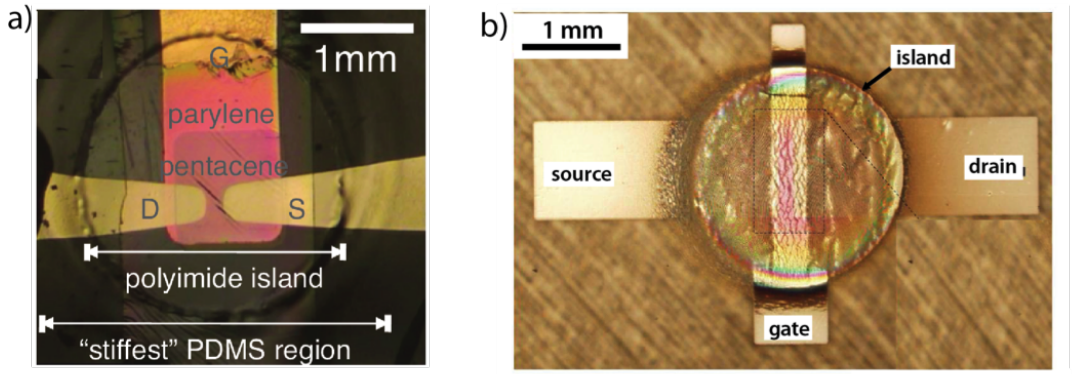


Figure 1.8: Thin film transistor fabricated directly onto elastomeric substrate: a) pentacene TFT onto engineered PDMS substrate, the image is adopted from Graz et al. [37]; b) amorphous silicon TFT onto PDMS substrate with rigid SiN_x subcircuit islands, the image is adopted from Lacour et al. [28]

as active layer (Fig. 1.8), were directly manufactured onto silicone substrates using only low temperature deposition techniques and dry patterning process are required. Both kinds of transistors performed similarly to their counterparts on, flexible, plastic foil, [28, 37].
Despite the limitations imposed by the polymeric substrate, this fabrication technique based on direct integration of micro-electronic devices onto elastomeric substrates enables to simplify the manufacturing process and devices layout, thereby, promises low cost manufacturing and scalability.

1.2 Objectives

The aim of this project is to develop a planar but mechanically engineered heterogeneous elastic substrate compatible with direct fabrication of thin film devices.

A first objective is to develop a simple and robust approach for designing and manufacturing versatile elastic substrates for stretchable electronic applications.
Engineered substrate with built-in strain relief is proposed as compliant yet reliable substrate to host stretchable circuitry. First the geometry and density of the embedded platforms are optimized to maximize the stiff region and minimize the far field strain. A simulation by finite element method (FEM) predicts the mechanical behavior of the engineered substrates. Associated design rules based on experimental as well as modeling data are presented. Then greyscale photolitography is implemented to smooth out the strain concentration at the stiff-to-soft interface. Last, new geometrical layout is presented to further decrease the strain along the interconnects. Compatibility of the proposed engineered substrate with standard, additive thin-film processing is also demonstrated.

The second objective is to fabricate metal oxide based TFTs on the engineered stretchable substrate. IGZO TFT with organic dielectric layer are manufactured directly on top of the soft polymeric substrate. Different dielectric structures are tested in order to achieve a robust transistor-like behavior. Further, the electrical performance is measured under tensile strain to validate the design of the stretchable electronic devices.

In addition concurrent photopatterning of elastic modulus and structures in photosensitive silicone elastomers has been discovered and studied.
The aim is to simultaneously patterning the topography and elasticity of positive photopatternable PDMS, P-PDMS, solely by dry UV light irradiation, avoiding any wet chemistry. First the elastic modulus of the photosensitive elastomer is evaluated as function of UV light energy density. Then P-PDMS patternability against feature, size and spacing is investigated. Next the combined topographical and mechanical patterning of P-PDMS is explored to investigate the resulting stiffness of the photosesitive elastomer. Microfluidic devices are fabricated through the proposed technique and demonstrate a interesting application of the single-step photopatterning of P-PDMS.

1.3 Thesis outline

This thesis is organized in four chapters.
After this introduction, the following first three chapters are structured in four main sections: (i) *introduction*, where more precise theory and state of the art of the discussed topic are presented, (ii) *materials and methods*, (ii) *results and discussion*, and (iv) *conclusions*. The last chapter summarizes the key findings of the thesis and give an outlook on the future work.

Chapter 2 focuses on the mechanical optimization of the engineered substrate. This chapter presents a particular structure, composed by a general introduction on the available stretchable substrate strategies, followed by multiple *introduction-materials and methods-results and discussion-conclusion* structures.
The first section introduces the engineered stretchable substrate with embedded strain relief. In particular it focus on the optimization of the embedded platforms geometry, thickness and spacing, to increase the stiff area to host the electronic devices and to decrease the strain along the interconnects. Modeling and experimental data are compared to produce design rules of the engineered substrate.
The second section aims to reduce the peak of strain concentration at the edge of the embedded platforms and to maximize the stiff area without affecting the spatial resolution. Pixelated greyscale mask are employed to grade the large mechanical mismatch at the stiff-to-soft interface, by grading the mechanical compliance of the elastomeric matrix or by sloping the side wall of the embedded platforms.
The last section presents additional designs to further reduce the along the elastic wiring interconnecting adjacent devices. The proposed designs are based on hexagonal and rhomboidal layouts of the embedded platforms together with a mechanically patterned elastomeric matrix.

Chapter 3 reports on fabrication and electro-mechanical characterization of rigid IGZO TFTs on the engineered stretchable substrates. The active devices are patterned directly on the pre-defined, rigid regions of the elastomeric substrate, and interconnected with stretchable metallization spanning across the rigid platforms. Brittle transistors, with different dielectric hybrid stack, are electrically characterized before and after annealing. An IGZO TFT on the engineered substrate is monitored under tensile strain.

Chapter 4 introduces a single-step photopatterning of positive P-PDMS membrane. The chapter illustrates how both mechanical and topographical patterning of the elastomeric film can be achieved simultaneously and without any wet development step. The ability to concurrently photopatterning the elastic modulus and relief structures in P-PDMS film is investigated. Then, proof of concept designs using the photosensitive elastomer in microfluidics are presented.

Finally, Chapter 5 summarizes the key results obtained in the thesis. An overall conclusion and an outlook for future objectives are presented.

References

[1] C. I. and W. S., *"Overview of Flexible Electronics Technology"in Flexible Electronics*, Springer, Ed., London, 2009.

[2] T. Sekitani and T. Someya, "Stretchable organic integrated circuits for large-area electronic skin surfaces," *MRS Bulletin*, vol. 37, no. 03, pp. 236–245, Mar. 2012. [Online]. Available:

[3] D.-H. Kim, N. Lu, R. Ghaffari, and J. a. Rogers, "Inorganic semiconductor nanomaterials for flexible and stretchable bio-integrated electronics," *NPG Asia Materials*, vol. 4, no. 4, p. e15, Apr. 2012. [Online]. Available:

[4] D.-H. Kim, N. Lu, Y. Huang, and J. A. Rogers, "Materials for stretchable electronics in bioinspired and biointegrated devices," *MRS Bulletin*, vol. 37, pp. 226–235, 2012.

[5] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, I. Graz, S. Bauer-gogonea, S. Bauer, T. Someya, M. Drack, and R. Schwo, "An ultra-lightweight design for imperceptible plastic electronics."

[6] I. R. Minev, P. Musienko, a. Hirsch, Q. Barraud, N. Wenger, E. M. Moraud, J. Gandar, M. Capogrosso, T. Milekovic, L. Asboth, R. F. Torres, N. Vachicouras, Q. Liu, N. Pavlova, S. Duis, a. Larmagnac, J. Voros, S. Micera, Z. Suo, G. Courtine, and S. P. Lacour, "Electronic dura mater for long-term multimodal neural interfaces," *Science*, vol. 347, no. 6218, pp. 159–163, 2015. [Online]. Available:

[7] J.-H. Ahn and J. H. Je, "Stretchable electronics: materials, architectures and integrations," *Journal of Physics D: Applied Physics*, vol. 45, no. 10, p. 103001, Mar. 2012. [Online]. Available:

[8] S. Wagner, "Electronic skin: architecture and components," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 25, no. 2-3, pp. 326–334, Nov. 2004. [Online]. Available:

[9] J. Viventi, D.-H. Kim, J. D. Moss, Y.-S. Kim, J. a. Blanco, N. Annetta, A. Hicks, J. Xiao, Y. Huang, D. J. Callans, J. a. Rogers, and B. Litt, "A conformal, bio-interfaced class of silicon electronics for mapping cardiac electrophysiology." *Sci. Transl. Med.*, vol. 2, no. 24, p. 24ra22, Mar. 2010. [Online]. Available:

[10] C. Tsay, S. P. Lacour, S. Wagner, and B. M. Iii, "Architecture , Fabrication , and Properties of Stretchable Micro-electrode Arrays," *Electrical Engineering*, pp. 1169–1172, 2005.

[11] Z. Yu, C. Tsay, S. P. Lacour, S. Wagner, and B. Morrison, "Stretchable microelectrode arrays-a tool for discovering mechanisms of functional deficits underlying traumatic brain injury and interfacing neurons with neuroprosthetics." *IEEE Engineering in Medicine and Biology Society. Conference*, vol. Suppl, pp. 6732–5, Jan. 2006. [Online]. Available:

[12] S. Khoshfetrat Pakazad, a. M. Savov, a. van de Stolpe, S. Braam, B. van Meer, and R. Dekker, "A stretchable Micro-Electrode Array for in vitro electrophysiology," *2011 IEEE 24th International Conference on Micro Electro Mechanical Systems*, pp. 829–832, Jan. 2011. [Online]. Available:

[13] L. Xu, S. R. Gutbrod, A. P. Bonifas, Y. Su, M. S. Sulkin, N. Lu, H.-J. Chung, K.-I. Jang, Z. Liu, M. Ying, C. Lu, R. C. Webb, J.-S. Kim, J. I. Laughner, H. Cheng, Y. Liu, A. Ameen, J.-W. Jeong, G.-T. Kim, Y. Huang, I. R. Efimov, and J. a. Rogers, "3D multifunctional integumentary membranes for spatiotemporal cardiac measurements and stimulation across the entire epicardium," *Nature Communications*, vol. 5, pp. 1–10, Feb. 2014. [Online]. Available:

[14] D.-H. Kim, N. Lu, R. Ghaffari, Y.-S. Kim, S. P. Lee, L. Xu, J. Wu, R.-H. Kim, J. Song, Z. Liu, J. Viventi, B. de Graff, B. Elolampi, M. Mansour, M. J. Slepian, S. Hwang, J. D. Moss, B. L. S, and J. A. Rogers, "Materials for multifunctional balloon catheters with capabilities in cardiac electrophysiological mapping and ablation therapy," *Nature Materials*, no. 10, pp. 316–323, 2011. [Online]. Available:

[15] D.-H. Kim, N. Lu, R. Ma, Y.-S. Kim, R.-H. Kim, S. Wang, J. Wu, S. M. Won, H. Tao, A. Islam, K. J. Yu, T.-i. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H.-J. Chung, H. Keum, M. McCormick, P. Liu, Y.-W. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, and J. a. Rogers, "Epidermal electronics." *Science (New York, N.Y.)*, vol. 333, no. 6044, pp. 838–43, Aug. 2011. [Online]. Available:

[16] H. C. Ko, M. P. Stoykovich, J. Song, V. Malyarchuk, W. M. Choi, C.-J. Yu, J. B. Geddes, J. Xiao, S. Wang, Y. Huang, and J. a. Rogers, "A hemispherical electronic eye camera based on compressible silicon optoelectronics." *Nature*, vol. 454, no. 7205, pp. 748–753, 2008.

[17] I. Jung, J. Xiao, V. Malyarchuk, C. Lu, M. Li, Z. Liu, J. Yoon, Y. Huang, and J. a. Rogers, "Dynamically tunable hemispherical electronic eye camera system with adjustable zoom capability." *Proceedings of the National Academy of Sciences of the United States of America*, vol. 108, no. 5, pp. 1788–1793, 2011.

[18] A. Chortos and Z. Bao, "Skin-inspired electronic devices," *Materials Today*, vol. 00, no. 00, Jun. 2014. [Online]. Available:

[19] D. J. Lipomi and Z. Bao, "Stretchable, elastic materials and devices for solar energy conversion," *Energy & Environmental Science*, vol. 4, no. 9, p. 3314, 2011. [Online]. Available:

[20] A. P. Gerratt, H. O. Michaud, and P. Stéphanie, "[SOM]Elastomeric Electronic Skin for Prosthetic Tactile Sensation," *Advanced Functional Materials*, vol. 25, 2015.

[21] D. Son, J. Lee, S. Qiao, R. Ghaffari, J. Kim, J. E. Lee, C. Song, S. J. Kim, D. J. Lee, S. W. Jun, S. Yang, M. Park, J. Shin, K. Do, M. Lee, K. Kang, C. S. Hwang, N. Lu, T. Hyeon, and D.-H. Kim, "Multifunctional wearable devices for diagnosis

and therapy of movement disorders," *Nature Nanotechnology*, no. March, Mar. 2014. [Online]. Available:

[22] L. Pan, A. Chortos, G. Yu, Y. Wang, S. Isaacson, R. Allen, Y. Shi, R. Dauskardt, and Z. Bao, "An ultra-sensitive resistive pressure sensor based on hollow-sphere microstructure induced elasticity in conducting polymer film." *Nature communications*, vol. 5, p. 3002, Jan. 2014. [Online]. Available:

[23] S. P. Lacour, I. Graz, D. Cotton, S. Bauer, and S. Wagner, "Elastic components for prosthetic skin." *Conference proceedings : ... Annual International Conference of the IEEE Engineering in Medicine and Biology Society. IEEE Engineering in Medicine and Biology Society. Conference*, vol. 2011, pp. 8373–6, Jan. 2011. [Online]. Available:

[24] T. Someya, T. Sekitani, and T. Agency, "Exploratory Research for Advanced Technology (ERATO), Japan Science and Technology Agency BIONIC SKINS USING FLEXIBLE ORGANIC DEVICES," pp. 68–71, 2014.

[25] T. Someya, *Stretchable electronics*, Wiley-VCH, Ed., Weinheim, Germany, 2013.

[26] Z. Suo, "Fracture in Thin Films," *Encyclopedia of Materials Science and Technology*, pp. 1–17, 2001. [Online]. Available:

[27] J. A. Rogers, T. Someya, and Y. Huang, "Materials and mechanics for stretchable electronics." *Science (New York, N.Y.)*, vol. 327, no. 5973, pp. 1603–7, Mar. 2010. [Online]. Available:

[28] S. P. Lacour and S. Wagner, "Thin Film Transistor Circuits Integrated onto Elastomeric Substrates for Elastically Stretchable Electronics," *Film*, vol. 00, no. c, pp. 20–23, 2005.

[29] J. Song, H. Jiang, W. M. Choi, D. Y. Khang, Y. Huang, and J. a. Rogers, "An analytical study of two-dimensional buckling of thin films on compliant substrates," *Journal of Applied Physics*, vol. 103, no. 1, p. 014303, 2008. [Online]. Available:

[30] K. Park, D.-K. Lee, B.-S. Kim, H. Jeon, N.-E. Lee, D. Whang, H.-J. Lee, Y. J. Kim, and J.-H. Ahn, "Stretchable, Transparent Zinc Oxide Thin Film Transistors," *Advanced Functional Materials*, vol. 20, no. 20, pp. 3577–3582, Oct. 2010. [Online]. Available:

[31] M. Shin, J. H. Song, G.-H. Lim, B. Lim, J.-J. Park, and U. Jeong, "Highly Stretchable Polymer Transistors Consisting Entirely of Stretchable Device Components," *Advanced Materials*, pp. n/a–n/a, Mar. 2014. [Online]. Available:

[32] H. Wu, S. Kustra, E. M. Gates, and C. J. Bettinger, "Topographic substrates as strain relief features in stretchable organic thin film transistors," *Organic Electronics*, vol. 14, no. 6, pp. 1636–1642, Jun. 2013. [Online]. Available:

[33] J. a. Rogers, "Materials for semiconductor devices that can bend, fold, twist, and stretch," *MRS Bulletin*, vol. 39, no. 06, pp. 549–556, Jun. 2014. [Online]. Available:

[34] D.-H. Kim, Y.-S. Kim, J. Wu, Z. Liu, J. Song, H.-S. Kim, Y. Y. Huang, K.-C. Hwang, and J. a. Rogers, "Ultrathin Silicon Circuits With Strain-Isolation Layers and Mesh Layouts for High-Performance Electronics on Fabric, Vinyl, Leather, and Paper," *Advanced Materials*, vol. 21, no. 36, pp. 3703–3707, Sep. 2009. [Online]. Available:

[35] S. Wagner, S. P. Lacour, J. Jones, P.-h. I. Hsu, J. C. Sturm, T. Li, and Z. Suo, "Electronic skin: architecture and components," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 25, no. 2-3, pp. 326–334, Nov. 2004. [Online]. Available:

[36] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi, and T. Sakurai, "A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications," *PNAS*, vol. 101, no. 27, pp. 9966–9970, 2004.

[37] I. M. Graz, D. P. J. Cotton, A. Robinson, and S. P. Lacour, "Silicone substrate with in situ strain relief for stretchable thin-film transistors," *Applied Physics Letters*, vol. 98, no. 12, p. 124101, 2011. [Online]. Available:

[38] P. Lacour, J. Jones, and P.-h. I. Hsu, "Electronic skin : architecture and components," vol. 25, pp. 326–334, 2004.

[39] M. Gonzalez, F. Axisa, M. Bulcke, D. Brosteaux, B. Vandevelde, and J. Vanfleteren, "Design of metal interconnects for stretchable electronic circuits," *Microelectronics Reliability*, vol. 48, no. 6, pp. 825–832, Jun. 2008. [Online]. Available:

[40] D.-H. Kim, J. Song, W. M. Choi, H.-S. Kim, R.-H. Kim, Z. Liu, Y. Y. Huang, K.-C. Hwang, Y.-w. Zhang, and J. a. Rogers, "Materials and noncoplanar mesh designs for integrated circuits with linear elastic responses to extreme mechanical deformations." *Proceedings of the National Academy of Sciences of the United States of America*, vol. 105, no. 48, pp. 18 675–80, Dec. 2008. [Online]. Available:

[41] M. Vosgueritchian, D. J. Lipomi, and Z. Bao, "Highly Conductive and Transparent PEDOT:PSS Films with a Fluorosurfactant for Stretchable and Flexible Transparent Electrodes," *Advanced Functional Materials*, vol. 22, no. 2, pp. 421–428, Jan. 2012. [Online]. Available:

[42] Z. Xiong and C. Liu, "Optimization of inkjet printed PEDOT:PSS thin films through annealing processes," *Organic Electronics: physics, materials, applications*, vol. 13, no. 9, pp. 1532–1540, 2012. [Online]. Available:

[43] J. Lessing, S. a. Morin, C. Keplinger, A. S. Tayi, and G. M. Whitesides, "Stretchable Conductive Composites Based on Metal Wools for Use as Electrical Vias in Soft Devices," *Advanced Functional Materials*, pp. n/a–n/a, Jan. 2015. [Online]. Available:

[44] Y. Ohno, "Frontiers of Graphene and Carbon Nanotubes," pp. 269–283, 2015. [Online]. Available:

[45] Z. Chen, W. Ren, L. Gao, B. Liu, S. Pei, and H.-M. Cheng, "Three-dimensional flexible and conductive interconnected graphene networks grown by chemical vapour deposition." *Nat. Mater.*, vol. 10, no. 6, pp. 424–428, Jun. 2011. [Online]. Available:

[46] S. Tuukkanen, M. Hoikkanen, M. Poikelispää, M. Honkanen, T. Vuorinen, M. Kakkonen, J. Vuorinen, and D. Lupo, "Stretching of solution processed carbon nanotube and graphene nanocomposite films on rubber substrates," *Synthetic Metals*, vol. 191, pp. 28–35, May 2014. [Online]. Available:

[47] R. K. Kramer, C. Majidi, and R. J. Wood, "Wearable tactile keypad with stretchable artificial skin," *2011 IEEE International Conference on Robotics and Automation*, pp. 1103–1107, May 2011. [Online]. Available:

[48] H. O. U. Yuqun, M. O. Lixin, Z. Qingbin, and L. I. Luhai, "Synthesis of Silver Nanowires and Its Application on Stretchable Conductor b," vol. 731, pp. 593–596, 2015.

[49] P. Lee, J. Lee, H. Lee, J. Yeo, S. Hong, K. H. Nam, D. Lee, S. S. Lee, and S. H. Ko, "Highly stretchable and highly conductive metal electrode by very long metal nanowire percolation network." *Advanced materials (Deerfield Beach, Fla.)*, vol. 24, no. 25, pp. 3326–32, Jul. 2012. [Online]. Available:

[50] M. Park, J. Im, M. Shin, Y. Min, J. Park, H. Cho, S. Park, M.-B. Shim, S. Jeon, D.-Y. Chung, J. Bae, J. Park, U. Jeong, and K. Kim, "Highly stretchable electric circuits from a composite material of silver nanoparticles and elastomeric fibres." *Nature nanotechnology*, vol. 7, no. 12, pp. 803–809, Nov. 2012. [Online]. Available:

[51] G. Corbelli, C. Ghisleri, M. Marelli, P. Milani, and L. Ravagnan, "Highly Deformable Nanostructured Elastomeric Electrodes With Improving Conductivity Upon Cyclical Stretching," *Advanced Materials*, pp. n/a–n/a, Aug. 2011. [Online]. Available:

[52] D.-H. Kim, Y.-S. Kim, J. Amsden, B. Panilaitis, D. L. Kaplan, F. G. Omenetto, M. R. Zakin, and J. a. Rogers, "Silicon electronics on silk as a path to bioresorbable, implantable devices." *Applied physics letters*, vol. 95, no. 13, p. 133701, Sep. 2009. [Online]. Available:

[53] T. Li, Z. Huang, Z. Suo, S. P. Lacour, and S. Wagner, "Stretchability of thin metal films on elastomer substrates," *Applied Physics Letters*, vol. 85, no. 16, p. 3435, 2004. [Online]. Available:

[54] Y. Xiang, T. Li, Z. Suo, and J. J. Vlassak, "High ductility of a metal film adherent on a polymer substrate," *Applied Physics Letters*, vol. 87, no. 16, pp. 1–3, 2005.

[55] L. Yu, P.-J. Alet, G. Picardi, and P. Roca i Cabarrocas, "An In-Plane Solid-Liquid-Solid Growth Mode for Self-Avoiding Lateral Silicon Nanowires," *Physical Review Letters*, vol. 102, no. 12, pp. 2–5, Mar. 2009. [Online]. Available:

[56] D. Brosteaux, F. Axisa, M. Gonzalez, and J. Vanfleteren, "Design and Fabrication of Elastic Interconnections for Stretchable Electronic Circuits," *Electron Device Letters, IEEE*, vol. 28, no. 7, pp. 552–554, 2007.

[57] S. P. Lacour, D. Chan, S. Wagner, T. Li, and Z. Suo, "Mechanisms of reversible stretchability of thin metal films on elastomeric substrates," *Applied Physics Letters*, vol. 88, no. 20, p. 204103, 2006. [Online]. Available:

[58] I. M. Graz, D. P. J. Cotton, and S. P. Lacour, "Extended cyclic uniaxial loading of stretchable gold thin-films on elastomeric substrates," *Applied Physics Letters*, vol. 94, no. 7, p. 071902, 2009. [Online]. Available:

[59] N. Lambricht, T. Pardoen, and S. Yunus, "Giant stretchability of thin gold films on rough elastomeric substrates," *Acta Materialia*, pp. 1–8, Nov. 2012. [Online]. Available:

[60] ——, "Giant stretchability of thin gold films on rough elastomeric substrates," *Acta Materialia*, vol. 61, no. 2, pp. 540–547, 2013. [Online]. Available:

[61] R. M. Erb, K. H. Cherenack, R. E. Stahel, R. Libanori, T. Kinkeldei, N. Münzenrieder, G. Tröster, and A. R. Studart, "Locally Reinforced Polymer-Based Composites for Elastic Electronics." *ACS applied materials & interfaces*, Jun. 2012. [Online]. Available:

2 Engineered Stretchable Substrate with Embedded Strain Relief *†

Contents

*A. Romeo, Q. Liu, Z. Suo, S.P. Lacour, "Elastomeric substrates with embedded stiff platforms for stretchable electronics ," *Applied Physics Letters*, April 2013.

†A. Romeo, Y. Hofmeister, S.P. Lacour, "Implementing MEMS technology for soft, (bio)electronics interfaces," *proc. of SPIE DSS, Baltimore,USA*,May 2014

2.1 Pixellated Layout

Stretchable electronics are integrated circuitry that can reversibly expand and relax while maintaining their functionalities. This cannot be achieved with the hard, planar integrated circuits that exist today. Stretchability can be introduced into electronic systems by the use of suitable stretchable substrate materials, electrical interconnections and active electronic components. Therefore stretchable system are mostly hybrids of soft and hard materials that span more than 12 orders of magnitude in elastic modulus [1].
The main challenge to implement stretchable electronics is how to integrate fragile electronic device materials with compliant elastomeric substrates. Device material are brittle and crack at strains of a few tenths of percent [2] while the rubbery substrate can be repeatedly deformed with different strain levels on objects with arbitrary shapes. Thus, to enable large deformation, while keeping brittle materials intact, it is highly desirable to reduce the applied mechanical strain in such device structure on deformable substrates. One possible solution is the implementation of a pixellated matrix of rigid platform interconnected with elastic wiring (Fig2.1) [3–5]. The rigid platform are designed to host fragile device materials, preventing them from exceeding their critical fracture strain, while the exposed substrate together with the interconnects accommodate most of the deformation.

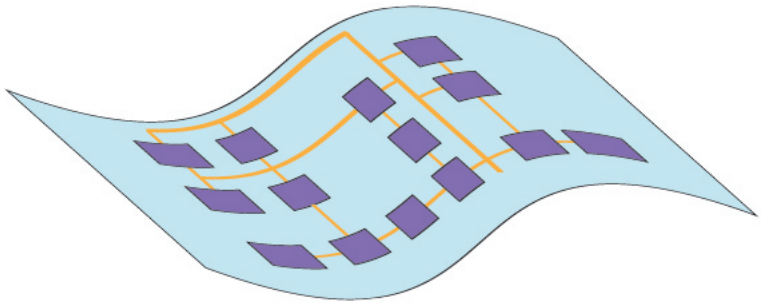


Figure 2.1: Concept of pixellated architecture for stretchable electronic. Stiff cell which host electronics devices is replicated many times and interconnected with elastic wiring.

In order to achieve electro-mechanical stability for this architecture the following mechanical conditions must be fulfilled [6].

- the stiffness of the platforms should be high enough to assure the strain within the device stack remains below the materials fracture strain i.e.$< 1\%$. Defining the stiffness as the product between the Young's modulus E and the thickness t of a material it necessary that:

$$E_{platform} \cdot t_{platform} \gg E_{substrate} \cdot t_{substrate} \tag{2.1}$$

- the strain profile along the interconnects running from the stiff platform to the soft matrix should be as smooth as possible. There is an abrupt transition of material properties at the stiff/soft interfaces, which cause strain localization at the interface of the islands

Mechanics and materials of the pixellated substrate will be analysed in the following subsections.

2.1.1 Mechanics

Two different strategies based on the pixellated architecture will be presented in the following paragraphs. The first one implements thin-film stiff islands deposited on top of the deformable substrate, the other relies on rigid thick platforms embedded in the elastomeric membrane.

Thin superficial stiff islands

One approach is to pattern directly onto thick (ranging from tens μm to $1mm$) polymeric substrate, thin (few hundreds nm)rigid platforms which work as functional non stretchable islands and can host active electronic devices. To guarantee the architecture function, appropriate island material must be chosen in order to fulfill the following conditions

- according to the equation 2.1, since the substrate is thicker than the stiff platforms, for those to be stiffer than the substrate, they should have a Young' s modulus much larger than the substrate one:
- the stiff platform materials need to be deposited with standard thin-film techniques at low temperature process in order to be compatible with organic substrates
- the stiff platform materials should be an electrical insulator in order not to influence the electrical performance of the hosted electronic devices

Only few materials satisfy the above requirements, which include silicon nitrate and diamond-like carbon.

Figure 2.2 shows four different mechanical configurations of the pixellated architecture considering different substrate materials and applications.

Hsu et al. [7] first proposed stiff device islands on a compliant substrates as solution to prevent active device from fracturing when the substrate is deformed on a spherical dome, where the substrate total biaxial tension is of $\approx 6\%$. Thin SiN_x islands hosting a TFT stack were first patterned on a flat polyimide (PI)substrate whose Youngś modulus is almost 40 times smaller than that of the stiff islands (Tab.2.1). Then the structure is plastically deformed on a spherical dome with a 66° field of view. Metal interconnects were deposited

only after deformation (Fig.2.2 (a)). They demonstrate, through experiments and finite element analysis, that by patterning brittle device materials onto isolated islands on top of a plastic substrate, device islands can remain crack free after deformation, and TFTs circuit was properly working.
The qualitative concept of this structure is that the soft substrate can flow beneath the island during the deformation so that the island itself might not be excessively strained. This concept was confirmed by theoretical modeling showing that the strains are pinned to low values in the island and the nearby substrate by the high Youngś modulus of the island, but increase farther from the island and deep underneath it [8].
To guarantee the architecture function, the strain in the device island should never exceeds its fracture strain. This strain is mostly influenced by the islands size and substrate material. On one side islands with larger diameter crack easily when the deformation is applied. This can be prevented by substrate heating at $150°C$ during deformation, which soften the substrate, or by implementing mesa structures (Fig.2.2 (b)). The critical island size, the maximal islands diameter above which no islands remains intact after deformation, is increased from $20\mu m$ with planar PI substrate at room temperature to $80\mu m$ by using mesa structure [8]. On the other side the shear stress on the interface at the edges of the islands makes the islands susceptible to debonding. Flaws at the edges of the islands may cause the islands to debond. According to the fracture criterion an interfacial crack will not propagate if the maximal energy release rate G_{max} is below the interface toughness, Γ_i. Finite element simulation showed that G_{max} diminishes as the island size or substrate stiffness decrease. Therefore the critical island size can be increased by decreasing the substrate stiffness [9].

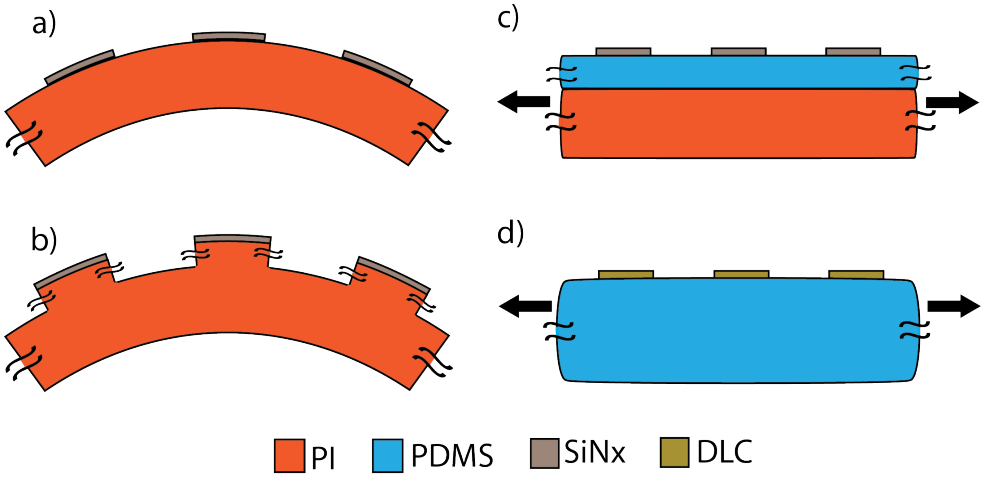


Figure 2.2: Schematic of different substrate structures with thin superficial stiff islands: a) SiN islands fabricated on top a planar PI substrate, b) SiN islands fabricated on top of PI substrate with mesa structures, c)soft strain isolation layer structure with PDMS layer is sandwiched between the PI substrate and SiN islands, d) DLC islands fabricated onto elastomeric PDMS substrate.

Table 2.1: *Young's modulus of substrate materials considered in Fig. 2.2.*

Materials	DLC	SiN_x	PI	PDMS
E(GPa)	100-213	200	5	0.001

The structures presented above have been used for plastic irreversible deformation, with limited applied strain ($\approx 6\%$) and islands size ($< 100\mu m$). Fully stretchable electronic system should be able to reversibly conform any surface shape, which implies it may experience larger deformation strains once or many times.

One structural solution is introducing a soft strain isolation layer between the islands and the substrate (Fig.2.2 (c)) [10] [11]. By sandwiching a thin polydimethylsiloxane(PDMS) layer between the PI substrate and the stiff islands, experiments show that the islands can withstand applied strain over 20% without cracking or debonding. The PDMS layer, whose Youngś modulus is 5 orders of magnitude smaller than the one of the stiff islands (Tab.2.1), works as a buffer which isolates the islands from the strain imposed on the substrate. For a $10\mu m$ thick PDMS isolation layer the critical islands size, which allow to not fracturing when stretched up to 20% is increased to $200\mu m$ [10].
Wagner at al. [12] employ the pixellated structure to describe the conceptual hardware architecture of skin like circuits. Here the plastic substrate is replaced by a fully elastic one, onto which stiff islands hosting electrical devices are electrically connected with stretchable metal conductor. When the structure is deformed by a large strain, the islands deform by small strains and remain intact, while elongation and compression are distributed in the substrate and interconnects. This concept has been demonstrated by diamond like carbon DLC subcircuit islands patterned on top of a thick PDMS substrate (Fig.2.2 (d)) [13]. The $200\mu m$ large stiff islands remain intact even when the substrate is stretched beyond 25% of strain, deforming by a maximum strain of 5% without fracturing. Even if this strain value is greater than the fracture device materials fracture strain ($> 1\%$), the experiments validated the pixellated architecture for stretchable electronic applications.

A pixellated architecture based on thin stiff islands on top of the soft substrate prevent electronic device material from fracturing but this has some important limitation. Fabrication of thin film device on top of PDMS requires low temperature and mostly dry process (section 2.1.2) and therefore often relies on shadow mask and eye alignment patterning. The feature size resolution is then limited and islands larger than $200\mu m$ are required to properly fabricate multilayer functional device on top of them. A different approach, which does not restrict the islands size is described in the following section.

Embedded local stiffness

In this approach the stiff platform are not anymore deposited as thin film on top of the substrate, but local mechanical reinforcements are embedded in the substrate in order to generate a planar elastic membrane with heterogeneous and patterned mechanical properties.

Two main leading strategies implementing this new solution are described in Fig.2.3

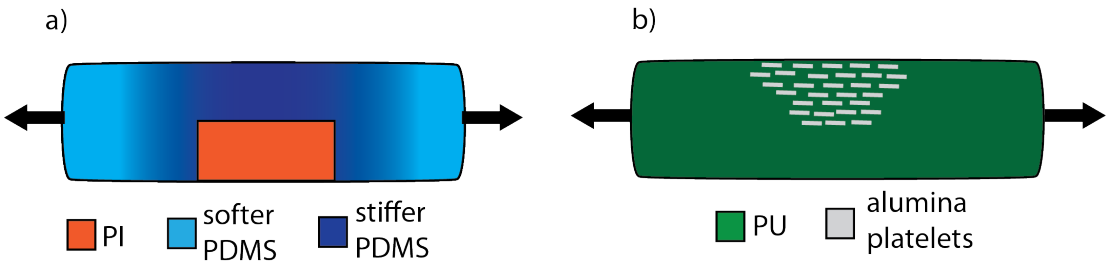


Figure 2.3: Schematic of different substrate structures with embedded local stiffness: a)PI platform embedded P-PDMS substrate with patterned compliance b) locally reinforced PU substrate with alumina stiff platelets .

The first approach is based on the strain relief method enabled by combining embedding stiff platform silicone matrix with localized and graded stiffness [14] . When PI platforms are embedded at the bottom of the PDMS membrane, the large difference in stiffness between the two materials ($E_{PI} \gg E_{PDMS}$) can provide "zero-strain"zones on the surface of the substrate above the center of the stiff platforms. To increase the width of these zones as well as to achieve a gradual transition between stiffer and softer regions the authors have implemented photopatternable PDMS (P-PDMS) as elastomeric membrane, with stiffer regions in correspondence of the PI platform (Fig.2.3 (a)) . The elastic modulus of P-PDMS range from 2.9 MPa to 0.65 MPa by increasing the elastomeric cross-link through UV exposure [15]. $50\mu m$ thick, $2mm$ large PI platforms were embedded in $100\mu m$ thick P-PDMS membrane with patterned elastic modulus. Organic pentacene thin film transistors were fabricated on the stiff areas using planar vapor phase deposition processes. The TFTs did not experience any electrical or mechanical degradation when cycling strain up to 13% was applied [14].

Another strategy implements a particle-reinforced polymer-based composite [16]. Here magnetically responsive stiff alumina platelets are used as stiff reinforcing elements of both polyurethane PU and PDMS elastomeric substrate(Fig.2.3). Embedding the platelets in the substrate, close to the top surface, it is possible to create stiff regions to protect electronic device materials from fracturing during applied strain. Embedding 20 vol% platelets the PU and PDMS elastic modulus are increased respectively of about 5 and 5.5 times. Even if the surface strain of these region increases above 1% for applied strain $\geq$5%, this method allows to keep the top surface sufficiently smooth to enable the direct fabrication of high performances metal oxide based TFTs [16].

The stretchable substrate structures described above are not anymore limited in pixel size and can host electronic devices with large foot-print that can be easily fabricated with dry step processing. At the same time embedded stiffness approach avoids the abrupt jump in materials properties at the islands-substrate interface experienced with the thin stiff islands one.
The following section describes few strategies implemented to make the transition from stiff to soft region still smoother.

Smooth strain gradient across interconnects

In the pixellated architecture, the stiff regions designed for hosting thin film electronic devices need to be interconnected by elastic wiring, that together with the elastomeric substrate accommodate most of the applied strain. This design produces strain concentration at the stiff-to-soft interface due to mechanical mismatch of the substrate materials. So it is important to smooth this strain localization at the interface to minimize the potential mechanical failure of an electrical interconnects running off the rigid regions.

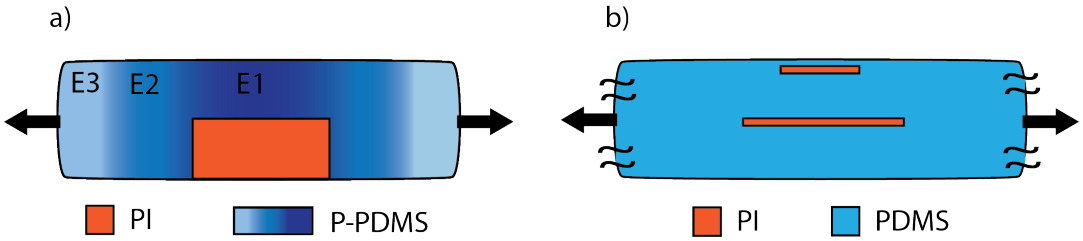


Figure 2.4: Schematic of different substrate structures with Smooth strain gradient across interconnects: a)PI platform embedded P-PDMS substrate with 3 moduli patterned compliance ($E1 > E2 > E3$) b) double PI disk embedded in stretchable PDMS substrate.

Cotton et al. [15] proposed a graded P-PDMS solution to suppress the strain concentration at the stiff/soft interfaces and reduce the resistance change of metal stretchable interconnects when stretched up to 20% of strain. Finite element modelling demonstrates that implementing concentric three-moduli P-PDMS membrane, E respectively of 2.9, 1.35 and 0.65 MPa, with stretchable substrate with strain relief method (Fig.2.4a) helps in smoothing out the strain peak on the top surface above the PI platform edges. The smoothing process can be improved by improving the grading level which can be done by increasing the amount of the concentric patterned P-PDMS modulus [14].
Another approach is to embed in the membrane two concentric PI ($50\mu m$ thick) platforms at different thickness of $1mm$ thick PDMS membrane [17]. A first small disk is positioned close to the top surface of the elastomer to ensure the strain at the top surface immediately above it is pinned to zero, while a second disk with larger diameter is embedded at the half of the PDMS thickness to suppress the strain peak across the hard-soft transitions(Fig.2.4b).

These two methods demonstrate that is possible to smooth the strain localization by grading the mechanical stiffness discrepancy of the substrate materials.

2.1.2 Substrate Materials Selection

In the sections above we presented different approaches of pixellated designs for stretchable electronics. Among them, elastomeric substrates with engineered strain relief [14], is the most promising alternative to realize fully stretchable integrated circuits. This strategy is efficient to ensure TFT materials are not stretched above their fracture strains, at the same time it is compatible with planar and standard microfabrication, providing the ability to simplify the manufacturing process for potential large-area and lightweight applications. Based on this approach we develop an optimized engineered substrate to carry reliable and durable stretchable electronics.
In this subsection engineered substrate materials selection and properties will be discussed.

Elastomeric Matrix

Elastomers are polymeric materials characterized by low Young's modulus and high failure strain and can be stretched reversibly to many times their original length. Therefore they are good candidates to replace stiff Si or glass substrate for stretchable electronics application.

The most widely used elastomer to imparts elasticity in electronics is Polydimethylsiloxane (PDMS). It is an organosilicon polymer, or silicone, consisting of repeating siloxane $(-Si-O-)n$ units where two methyl groups $(-CH3)$ are attached to each Si atom of the backbone [18]. PDMS is an optically clear, chemical inert, nontoxic and a biocompatible material [19]. It is also hydrophobic and support surface modification but it swells in organic solvents used for photolitograbhy and microfabrication. This parameter together with the high coefficient of thermal expansion CTE (Tab 2.2) [20], hudnreds time larger than that of inorganic device materials, need to be taken into account when processing directly on PDMS substrate.. Its Youn'g modulus can be tuned from 0.75-2.5MPa by altering elastomer cross-linking and processing conditions, such as temperature and curing time [21] [22]. As all silicones, PDMS is an isotropic, hyperelastic material, therefore its linearly elastic only for tensile strain up to 50%. Beyond this value the polymer undergoes little viscous flow and its elastic modulus is only weakly dependent on tensile strain rate [22] [23].
Thanks to his mechanical propoerties PDMS have been selected for the elastomeric matrix of the stretchable engineered substrate.

PDMS can be made photosensitive, so called P-PDMS, by adding to the base compound a photoiniziator [24], negative P-PDMS, or a photoinibitor, positive P-PDMS, [18] [25] to respectively promote or prevent polymer crosslinking after UV activation. PDMS base monomer is vinyl terminated $-CH = CH2$ group while the crosslinkers are methyl-

terminated and contain silicon hydride $-OSiHCH3-$ units. When the polymerization occurs cross-links form between the monomer vinyl groups and the silicon hydride groups of the cross-linkers to form $Si-CH2-CH2-Si$ linkages. By adding benzophenone to the initial prepolymer-cross linker mixture PDMS become photosenstive. Benzophenone is a photoinibitor, and generates free radicals under UV light exposure (wavelength range between 200 and 400nm). These radicals react with both the silicon hydride units in the PDMS cross-linkers and the vinyl groups in the PDMS monomers. In both cases, the binding sites of the two components are reduced, limiting the potential cross-link density of the exposed area [18]. Cotton et al. [15] demonstrated that by modulating the cross-link densities of non-developed P-PDMS is possible to locally patterning its tensile modulus from 2.9 to 0.65 MPa within a single continuous rubber film. Mechano-photopatterning of P-PDMS offer an excellent solution for peak of strain suppression at the stiff-to-soft area transition [14].

In this study we have improved this approach by implementing greyscale photopatterning of P-PDMS to further smooth out the strain concentration at the interfaces.

Stiff Embedded Platforms

The platforms are embedded deep in the substrate aiming to produce non stretchable areas on the top surface which can host brittle electronic devices. A suitable material for the platforms should satisfy the following requirements:

- it should be stiff enough in order to be able to create a non-stretchable area on the top surface when embedded in soft elastomeric matrix ($E_{platforms} \gg E_{PDMS}$)
- it should be compatible with clean room processing
- it should be easily patternable material to improve and accelerate the fabrication process

SU8 negative epoxy fulfils all the three condition. SU8 is a negative photoresist widely used for MEMS and general micro-devices fabrication. Among its advances there are low price, feasibility of batch processing, high aspect ratio and good chemical resistance [26] [27]. SU8 can achieve a maximal thickness of 2mm, and most important its stiffness is three orders of

Table 2.2: *Thermo-mechanical properties of engineered substrate materials, where E is the Youn'g modulus, CTE is the coefficient of thermal expansion and λ is the thermal conductivity.*

Materials	E (GPa)	CTE ($ppm/°C$)	λ(W/mK)
PDMS	~ 0.001	340	0.15
SU8	~ 4	52	0.2

magnitude higher than the PDMS one (Tab 2.2). Therefore SU8 is an optimal candidate as stiff platforms materials since its much stiffer than the elastomeric matrix which allows for generating non-stretchable top surface area, and it can be easily patterned through standard photolitography process in desired platforms shape and size.

2.1.3 Mechanical Requirements

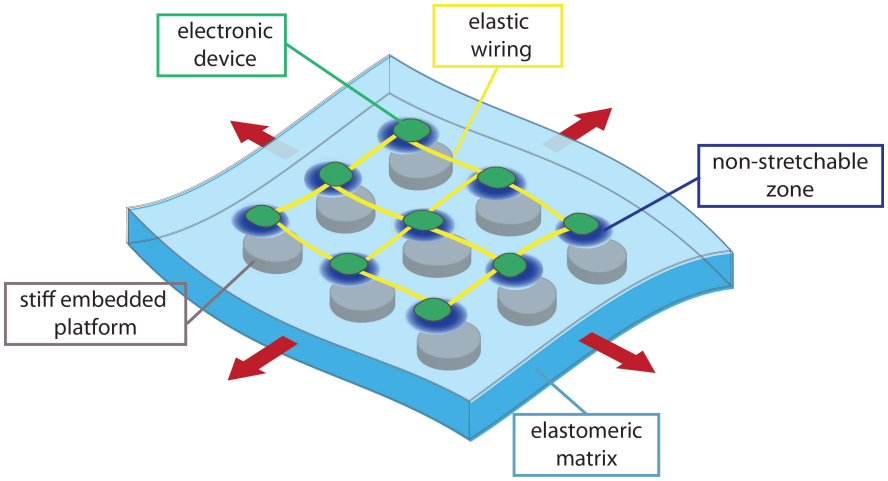


Figure 2.5: Engineered substrate schematic. Stiff platforms embedded in an elastomeric matrix help in producing non-stretchable areas on the top surface which can host brittle electronic devices connected with elastic wiring. This stiff areas prevent the electronic device materials from fracturing when the substrate is macroscopically stretched.

Engineered substrate with the strain relief method combining rigid plastic SU8 platforms embedded in a silicone matrix (PDMS), and stretchable metal interconnects have been developed. Embedding SU8 platforms in a silicone membrane help in producing a stretchable substrate with intrinsic stiff regions while maintaining plain and uniform top surface onto which electronic materials can be directly processed. Since the platforms are significantly stiffer than the surrounding silicone matrix (Tab 2.2), the elastomer volume immediately above the platform is little strained when the matrix is macroscopically stretched. Therefore non-stretchable areas are formed on the elastomer top surface, which can host fragile devices and protect them from large mechanical deformations (>1%) (Fig 2.5 (a)).

A strain value of 20% was defined as maximal strain required for possible bio-medical applications of the stretchable circuits. On the other hand, a strain value of 0.5% was defined as the *critical strain* not to be exceeded in the device materials above the platforms. To prevent electronic devices from fracturing the following requirements on the top surface of the substrate must be fulfilled even when 20% macroscopic strain is applied:

- Identify a non-stretchable area in correspondence of the center of the platform which is

not strained beyond the critical strain (0.5%) upon stretching, the *safe area* A_s (Fig 2.6)

- Maximize this non-stretchable area to increase the surface available for the active devices
- Minimize the strain concentration at the rigid-to-elastic transition zones to prevent electro-mechanical failure of the interconnects running off the safe areas.

In the following sections substrate optimization that has been implemented to satisfy the above mechanical conditions will be described. First the geometry and density of the SU8 platforms have been optimized to define a threshold between the size of safe area and the inter-platforms strain. Then greyscale photolitography is implemented to smooth out the strain concentration at the stiff-to-soft interface. Last a new geometrical layout is presented to further decrease the strain along the elastic metallizations running across the the non stretchable areas.

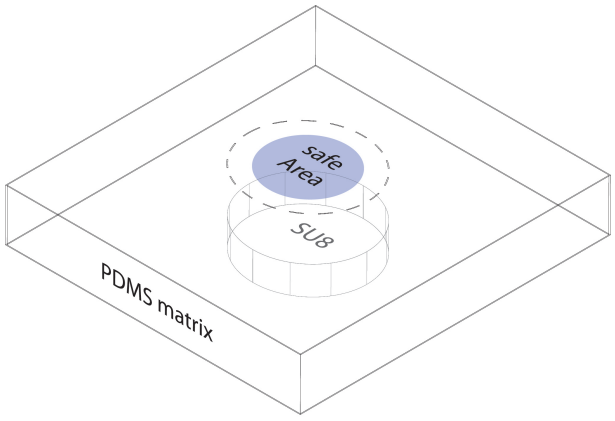


Figure 2.6: *Safe area* schematic.The *safe area* is defined as the part of the non-stretchable (delimited by the dashed line) area on the elastomer top surface in correspondence of the center of the SU8 platform which is never strained beyond 0.5% of strain even when large deformations, up to 20% of strain, are applied.

2.2 Stiff Platform Geometry Optimization

Engineered substrate with embedded strain relief working principles have been presented. To maximize the available surface area of the active circuits and to minimize the strain concentration at the rigid-to-elastic transition zones design optimization on the engineered substrate have been implement in order to derive simple guidelines on the geometry and density of the embedded platforms and safe area.

First, micromechanics modeling is expounded to predict where the highest strain appears, define how far inside the platform it is safe to pattern the devices and clarify how these factors are influenced by the structure geometry. Then experimental measurements have been executed o confirm the theoretical results. Finally, we demonstrate the engineered elastomeric substrate is compatible with standard, additive thin-film processing.

2.2.1 Finite Element Modeling

In order to optimize the design of the heterogeneous substrate, a better understanding of the strain distribution on the top substrate where electronic devices and elastic interconnects will lie have first been achieved with micromechanics modeling. Numerical analysis has been implemented in a collaboration with Prof. Zhigang Suo research group of Mechanics of Materials and Structures at the University of Harvard using finite-element modeling (FEM).

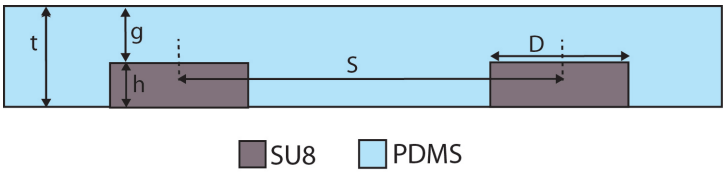


Figure 2.7: Schematic cross sectional view of the substrate and geometrical parameters

Finite element simulations were conducted with ABAQUS software. Both SU8 platforms and PDMS substrate were modeled as Neo Hookean material, with initial shear modulus and bulk modulus respectively of 4GPa, 400GPa for SU8 and 2MPa, 200MPa for PDMS. Since the stiffness difference between the two materials is so large that their specific moduli do not affect the result much, we may well treat the platform as rigid body and our problem becomes a pure geometric problem. The following geometric parameters come into the system, as is labeled in Figure :
-t the thickness of the substrate
-g the gap above the platform
-D the diameter of the platform
-S the spacing between the neighboring platforms

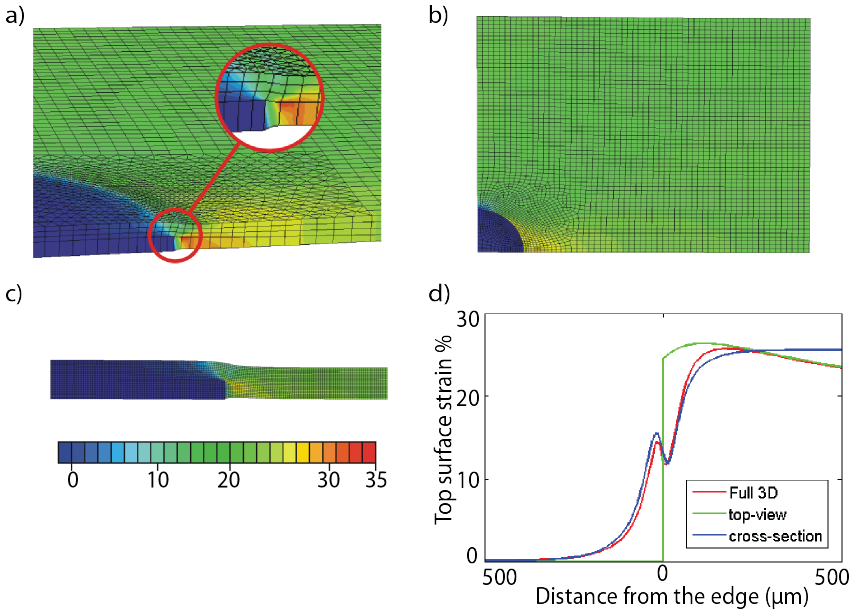


Figure 2.8: Computed strain distribution trough FEM of the engineered substarte with $g/t = 0.5$, $S/D = 6$ and $\varepsilon_{applied} = 20\%$. a) 3D FEM simulation of a quarter of SU8 platforms embedded at the bottom of the PDMS membrane. Inset: localized, non-homogeneous strain distribution along the thickness. The 3D simulation can be decoupled in two complementary 2D models: b) top view 2D in-plane stress model and c) cross-section 2D in-plane strain model. d) Strain profiles of the three simulations.

These parameters will give rise to three dimensionless parameters and the strain distribution will take the following functional form :

$$\varepsilon\left(\frac{\mathbf{x}}{t}\right) = f\left(\frac{\mathbf{X}}{t}, \frac{g}{t}, \frac{D}{t}, \frac{S}{D}, \varepsilon_{applied}\right) \tag{2.2}$$

where $\varepsilon_{applied}$ is the applied strain. Here $\mathbf{X}$ is a 2D vector of position, since we only care about the strain on the top surface.
To simplify the analysis, we next took advantage of a feature in our geometric design. Since the local dimensions t, g and the global dimensions D, S are on different scales(i.e. $S, D \gg t, g$), they can decouple from each other, reducing the 3D parametric space into two independent 1D parametric spaces, which is a huge advantage in design.

Consequently, the system is decoupled into two parts: the local behavior near the edge is dominated by the thickness ratio of the platform comparing to the film and is not affected by the size or the arrangement of the platforms; the global behavior is dominated by the spatial distribution of the platforms and their diameter, but not influenced by the thickness of the platform. According to this strategy, the 3D analysis (Fig.2.8 (a)) can be well represented by using two types of two-dimensional finite element analyses to predict respectively the global and the local strain distribution.

For the global design a top-view modeling is performed , on a scale much larger (1 mm range) than the thickness of the substrate. Therefore we neglect the inhomogeneity across the thickness, and the strain distribution takes the form:

$$\varepsilon\left(\frac{\mathbf{x}}{D}\right) = f_{global}\left(\frac{\mathbf{X}}{D}, \frac{S}{D}, \varepsilon_{applied}\right) \tag{2.3}$$

This distribution will be erroneous only near the platform's edge of the platform, where the heterogeneity is important. For the local design we focus on this area, within a few thickness distances from the edge. Here the strain distribution is dominated by the heterogeneity andthe local parameters t and g, while the global scale geometric factors, S and D cannot be felt directly, which will give the following distribution:

$$\varepsilon\left(\frac{x}{t}\right) = f_{local}\left(\frac{x}{t}, \frac{g}{t}, \varepsilon_{far}\right) \tag{2.4}$$

The local strain is only function of the scalar x, which is the distance from the edge, instead of the vector because the radius of curvature of the platform is significantly larger than t or g, and cannot influence the local strain distribution . ε_{far} is the limit of the local distribution far away from the edge, it reflects the indirect influence of global scale on the local scale.
Also even if the materials are modelled Neo-Hookean materials, the materials nonlinearity is much less significant than the geometrical difference(less than 10%). Thus assuming that the strain is approximately linearly proportional to the applied strain and the far field strain, we can further simplify the f_{global} and f_{local} in one parameters functions:

$$\varepsilon\left(\frac{\mathbf{x}}{D}\right) = \varepsilon_{applied} \times f_{global}\left(\frac{\mathbf{X}}{D}, \frac{S}{D}\right) \tag{2.5}$$

and

$$\varepsilon\left(\frac{x}{t}\right) = \varepsilon_{far} \times f_{local}\left(\frac{x}{t}, \frac{g}{t}\right) \tag{2.6}$$

To get the global design plane stress simulation of the top view is performed, taking the average of the material parameters over the thickness, as showed in Figure 2.8 (b). While, the local design is implemented with a plane strain simulation of the cross section, as showed in Figure 2.8 (c).

For practical purpose, we only care about the highest strain level. This correspond to the line which goes through the center of the platforms along the stretching direction. Figure 2.8 d compares the strain line profiles of the global and local simulation with the 3D one. As expected, the two kinds of simulations capture the strain profile asymptotically, which justify the decoupled design. The local-scale analysis can approximate the real solution near the edge of the platform where the global-scale analysis gives satisfactory approximation to the strain

far away from the edge.

Figure 2.9 shows the strain profile calculation of the equation 2.5 , for the S/D values equal to 3, 6 and 11, when 20% of strain is applied. Since the platform is hardly deformable, the applied strain is averaged over the surrounding area, the larger the S/D, the lower the average strain on this area. There is stress concentration due to the presence of the embedded platform, where the size of the influenced region is proportional to the size of the platform. Figure 2.10 (a) shows the calculation of equation 2.6. There is a strain peak due to the presence of the step of the platform, the thicker the PDMS above the platform, the smoother the transition. In the meantime, as the PDMS above the platform becomes thicker, the region on the platform that is influenced by the far field strain gets larger. To characterize this kind influence and define a safe area above the platform (section 2.1.3), we define the penetration depth p as the distance from the edge for which the strain decays to 0.5% if the far field strain is 20%, which gives the criterion 0.025 ε_{far} (Fig. 2.10 (b)). The penetration depth value is plotted in Figure 2.10 (c). The result is almost linear up till $g/t = 0.6$, above which the bending of the platform becomes significant, and the local scale assumption is not valid . The linear relation shows that approximately $p = 5g$, we used this value as the borderline between the local and global solutions in figure 2.8 (d).

Both 3D and 2D finite element simulations were conducted with ABAQUS software. Symmetric boundary conditions were applied to any edge (surface for 3D case) running through the center of the platform in all three kinds of simulations showed in figure 2.8. Uniform displacement boundary conditions were applied to the right hand side edge/surface to get desired overall strain.
The described computing results are compared with experimental ones in the next section.

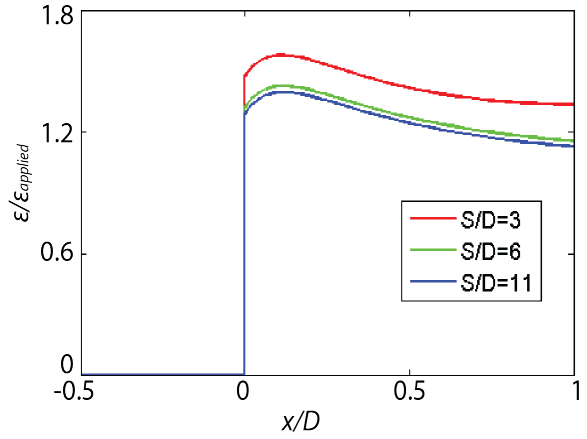


Figure 2.9: f_{global} surface strain profile calculations at different S/D ratios, when $g/t = 0.5$ ratio and $\varepsilon_{applied} = 20\%$.

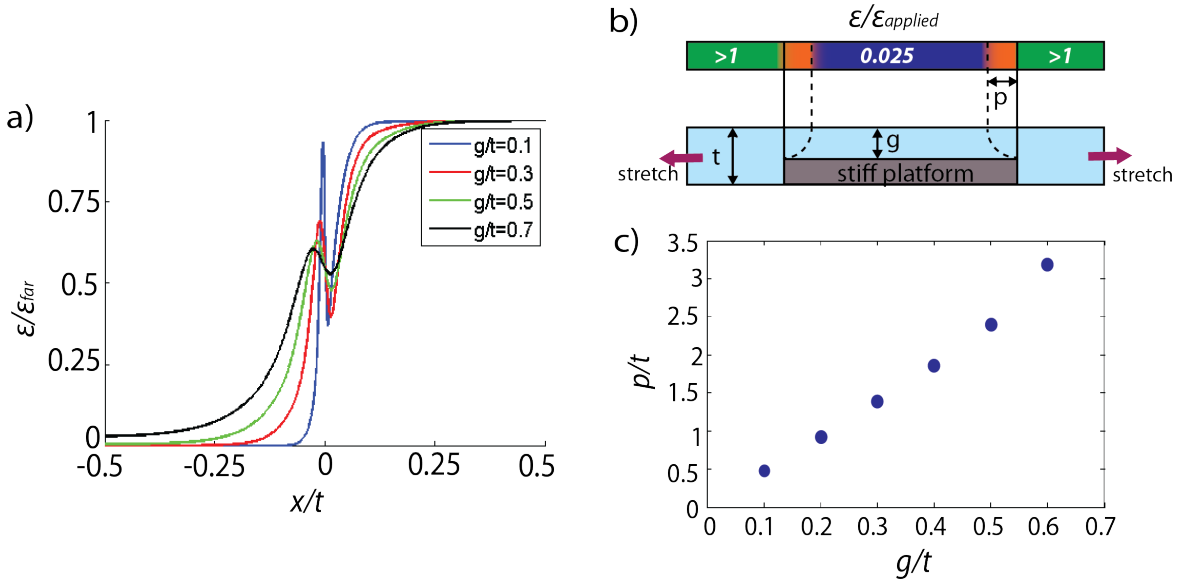


Figure 2.10: Local-scale: a) f_{local} surface strain profile calculations at different g/t ratios, when $\varepsilon_{far} = 20\%$, b) cross-sectional schematic illustrating the penetration depth p, c) penetration depth as a function of the PDMS thickness above the platform at a given g/t ratio.

2.2.2 Experimental: Materials and Methods

Substrate fabrication

The engineered substrate were manufactured using polymer spin-coating and photolithography using CMi facilities. The fabrication steps were implemented on top of rigid 4 inch Silicon wafer, covered with 5/50 nm thick Ti/Al releasing layer. Only after the substrate, and eventual electronics on top, were completed the heterogeneous structure were released from the Si wafers to obtain a free-standing stretchable system.
First, stiff SU8 (Gersteltec GM 1070) platforms were patterned by standard UV photolithography (Karl Suss MJB4 contact mask aligner, λ=365nm) on the rigid substrate. The platforms are 1 mm diameter , 10-90 μm thick and organized in a square pattern of 2-10 mm interplatform distance. After development, 100 μm thick PDMS (Sylgard 184, Dow Corning) was spin-coated on the wafers and cured at 150°C for 24h onto a hot plate. The engineered substrates was then released from the Si wafers. Rectangular sample were first cut on the elastomeric substrate still attached to the rigid wafer and released together with the embedded SU8 platforms after anodic dissolution of the metal releasing layer.

Mechanical characterization

In stretch experiments, the rectangular sample were clamped to the jaws of an automated custom built uni-axial stretcher. The terminal parts of the samples clamped in the stretcher

did not contain any embedded platforms but only bare PDMS. The stretcher was controlled through a LABVIEW interface and was capable of delivering a variety of strain steps and rates. The tensile stress was applied along the x direction

A first stretch test was performed on samples with 3×3 square patterns of platforms 50 μm thick and with 3 mm interplatform distance. The samples were stretched to a maximal strain of 50% with a strain rate of 0.5% × s and optical pictures were taken every 5% of applied strain, in order to identify the critical strain at which the SU8 platforms starts to delaminate from the sourronded PDMS.

Then, to evaluate the strain distribution on the top surface of the engineered substrate we have used a Digital Image Correlation DIC system, LIMESS Messtechnik und Software GmbH and the related software Istra 4D v4.3.0 . DIC is a non invasive optical technique which is able to measures changes on speckle images. An accurate image correlation algorithms tracks the changes in gray value pattern in small neighborhoods called subsets during deformations. Trough this system we have been able to map the strain across the top surface of the elastic substrate and compare the extrapolated strain profiles with the computed ones. In order to

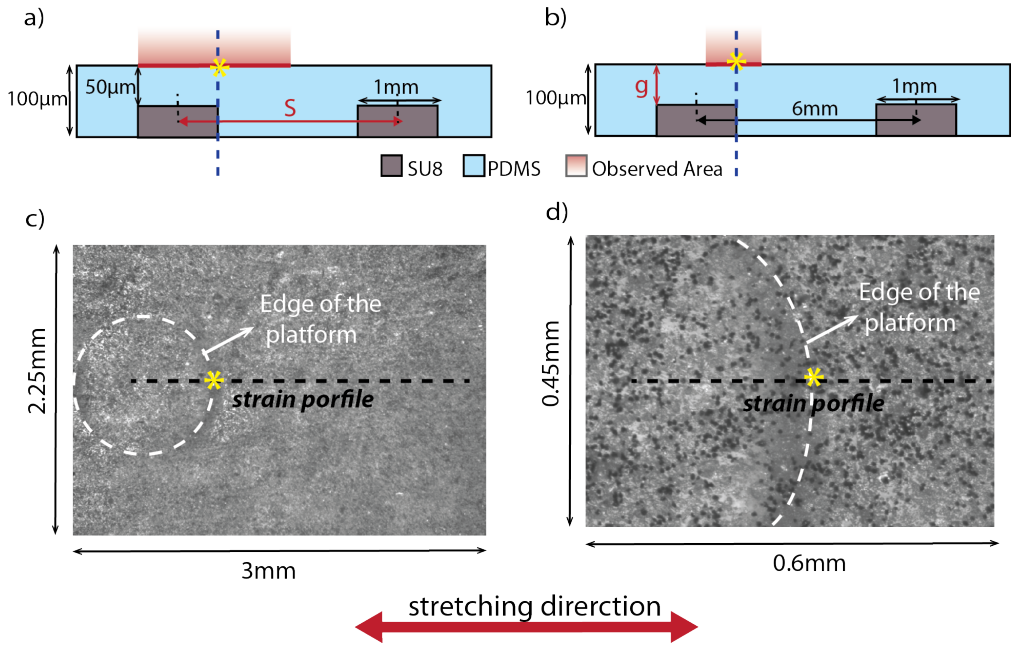


Figure 2.11: Global and local scale design: a) schematic cross-sections of the samples used to investigate respectively the global and the local strain behaviour. c) and d) are optical speckle images of the correspondent top surface observed area for the two designs with respectively 100x and 500x magnification. The white dotted line underline the edge of the embedded platform, while the black one show the extrapolated strain profile line. The yellow star indicate the point of the strain profile in correspondence of the edge of the platform.

achieve speckle images, talcum and printer toner powder were dispersed onto the samples top surface with 3 × 3 squared pattern platforms. Tensile test were performed, up to 20% of macroscopic strain. Microscopic images of the samples were taken at different applied strain to calculate the evolution of the distance between the particles as the sample is stretched from 0% to 20%.
The images were taken with a long working distance microscope objective mounted above the stretcher setup (Keyence VHX-500F).
Strain distribution at the global and local scale was analysed using the DIC system.The global behaviour is dominated by the spatial distribution of the platforms aiming for understanding the strain distribution on large region of the top surface, from the area above the platform to the area in-between two adjacent platforms. Here t and g, which are in the order of 100 microns, are too small to come into play, and everything is characterized by S and D. Samples with SU8 platforms array with fixed thickness of $50\mu m$, and different spacing, S changing between 3 and 11 mm, were stretched to analyse the strain distribution at the global scale. On the other hand, the local behaviour focuses on top surface strain across the edge of the platform, where the strain concentration caused by the mechanical mismatch occurs. Here lateral dimensions S and D can be treated as infinite. The strain above the edges is dominated only by the thickness of the platform comparing to the film. Therefore to investigate local design samples with SU8 platforms with fixed spacing of 6 mm and different thicknesses (from 10 to 90 μm) have been tested. Figure 2.11 shows the the schematic cross sections of the analysed sample and the correspondent top surface speckle images, recorded trough a single lens microscope with two different magnifications of 100× and 500× respectively for the global and the local design. From the strain map of the observed region were extrapolated strain profiles taken along the stretching direction through the center of the platform, in order to compare them with the FEM results described above. The point underlined with the yellow star, indicates the point in correspondence of the edge of the embedded platform and correspond to 0 value in the x axis of the strain profile.

Thin-film processing compatibility

To first demonstrate the proposed approach to evaluate the substrate compatibility with thin-film multilayer processing, brittle materials and elastic metal interconnects were fabricated

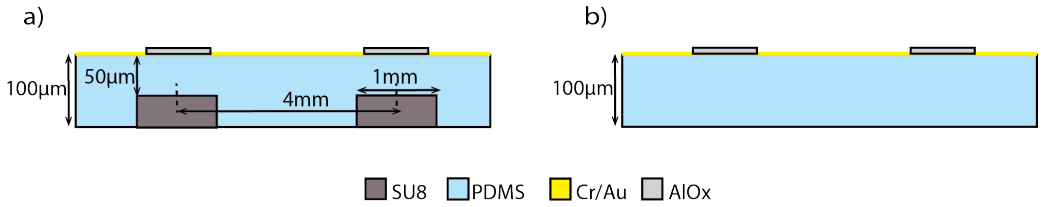


Figure 2.12: Cross sectional view of brittle 150 nm thick AlO_x disks and interconnected with elastic Au wiring directly manufactured onto the elastomer surface of a) the engineered substrate above the stiff platforms and b) the bare PDMS membrane

on top of the substrate.
Engineered substrate samples were prepared with a matrix of 6 × 5 square pattern of SU8 platform 50 μm thick, 1 mm diameter and 4 mm spacing embedded in a PDMS membrane 100 μm thick. In correspondence with the embedded platforms brittle Alumina (AlO_x) disks, 0.75 mm diameter, 150 nm thick were deposited by e-beam evaporation (Leybold Optics LAB 600 H). Then thin Gold stretchable conductors were evaporated to interconnect 6 disks on a row. Gold tracks (0.5 × 2mm) were formed as a Chromium/Gold multilayer of 3/30 nm thickness respectively. The Chromium adhesion layers ensured bonding of the Gold layer to the carrier substrate underneath. The sample were then released from the Si wafer and prepared for the electromechanical test. The same AlO_x islands - Gold interconnects were deposited on top of a bare PDMS substrate, in order to compare and validate the proposed approach. Figure 2.12 shows the schematic cross section of the two different structures. Flexible polyimide PI shadow masks (50 μm thick) were used to pattern thin film features.

The samples were clamped in the home-built, computer-controlled, and motorized uniaxial stretcher. The samples were stretched up to 20% of strain with a speed rate of 0.5% of strain per second, for 100 times. The stretch direction was along the interconnects tracks. The electrical resistance of the gold film was monitored with a Keithley 2400 source meter. Electrical contacts were established at both ends of an Au interconnect via thin silver wires (125 μm diameter). The connection between each wire and an electrode pad was made through a small globule of conductive silver paste (H27D, Epo-Tek). As the paste was not cured, it remained soft during experiments, preventing the delamination of the contacts when the sample were stretched. Gold metallisation were inspected after the cycling tensile test using a Zeiss MERLIN scanning electron microscope (SEM).

2.2.3 Experimental Results and Discussion

Mechanical characterization

We first investigated the stability of the engineered substrate structure upon stretching. Stretch experiments showed that PDMS-SU8 structure remains unchanged till applied strain up to 35%, above which lateral delamination of the SU8 platforms occurs. The side-walls of the SU8 platform start to detach from the surrounded PDMS. This delamination space increases with the applied strain (Fig. 2.13) causing a large strain concentration on the surrounded PDMS which can cause mechanical failure of the substrate. In the previous subsection, the local strain computed with a plane strain simulation of the cross section showed that there is a strain concentration along the thickness of the substrate in the PDMS portion close to the embedded corner of the platform (Fig 2.8 a,b). For example, this peak of strain is $> 30\%$ when 20% macroscopic strain is applied. Therefore, the delamination originate at this area when the perceived strain breaks the adhesion force between the PDMS matrix and the SU8 platforms. Since a maximal strain of 20% was imposed for the experiments, therefore the heterogeneous structure remained steady during the stretching

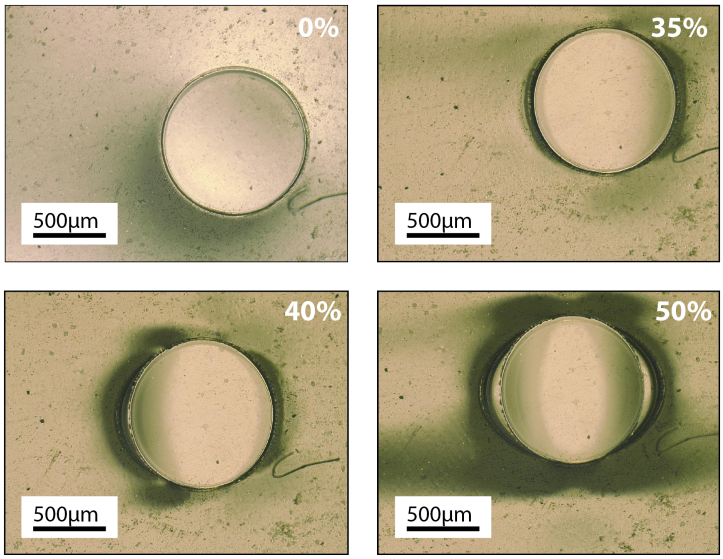


Figure 2.13: Delamination test: optical images of the bottom surface of the engineered substrate taken at different applied strain 0%, 35%, 40% and 50%

test. If larger strains are needed it would be necessary to encapsulate the SU8 platform with a PDMS layer on the bottom and/or to enhance the adhesion between the two polymers.

After assuring the substrate structure is reliable in the implemented range of strain, we studied the strain distribution on the top surface as function of the geometrical parameters S (global behaviour) and g (local behaviour).
Figure 2.14 shows experimental strain maps and strain profile of the global design recorded at the top surface of the engineered substrate using DIC system as a function of the spacing between SU8 platforms when 20% macroscopic strain is applied. The SU8 platforms are 1mm in diameter and 50 μm in thickness, half of the PMDS thickness, while S changes between 3 and 11 mm. In particular Figure 2.14 (a) shows on the top the speckle images of three samples with different S taken at 20% of applied strain and on the bottom the respective strain map. The strain immediately above the SU8 remains low, close to 0% independently on S. However, the strain in between the platforms and the peak strain at the edge of the SU8 platforms increase with decreasing spacing. Since the platforms are rigid and all the strain is accommodated by the PDMS in between,it is obvious that the more the PDMS to share the overall strain, the lower the average strain level. Strain profiles taken from the black dotted line on the strain maps, have been plotted in Figure 2.14 (b). 3D computed finite-element profiles of the same architectures achieved with the equation 2.2, shown in Figure 2.14 (c), match well with the experimental data. Both experimental and computed results shows that the larger the S/D ratio the lower is the far field strain. In our case ($\varepsilon_{applied} = 20\%$) this ratio should be larger then 3 in order to produce a far field strain similar to the applied strain.

Then the strain distribution on the top surface as function of the PDMS thickness above

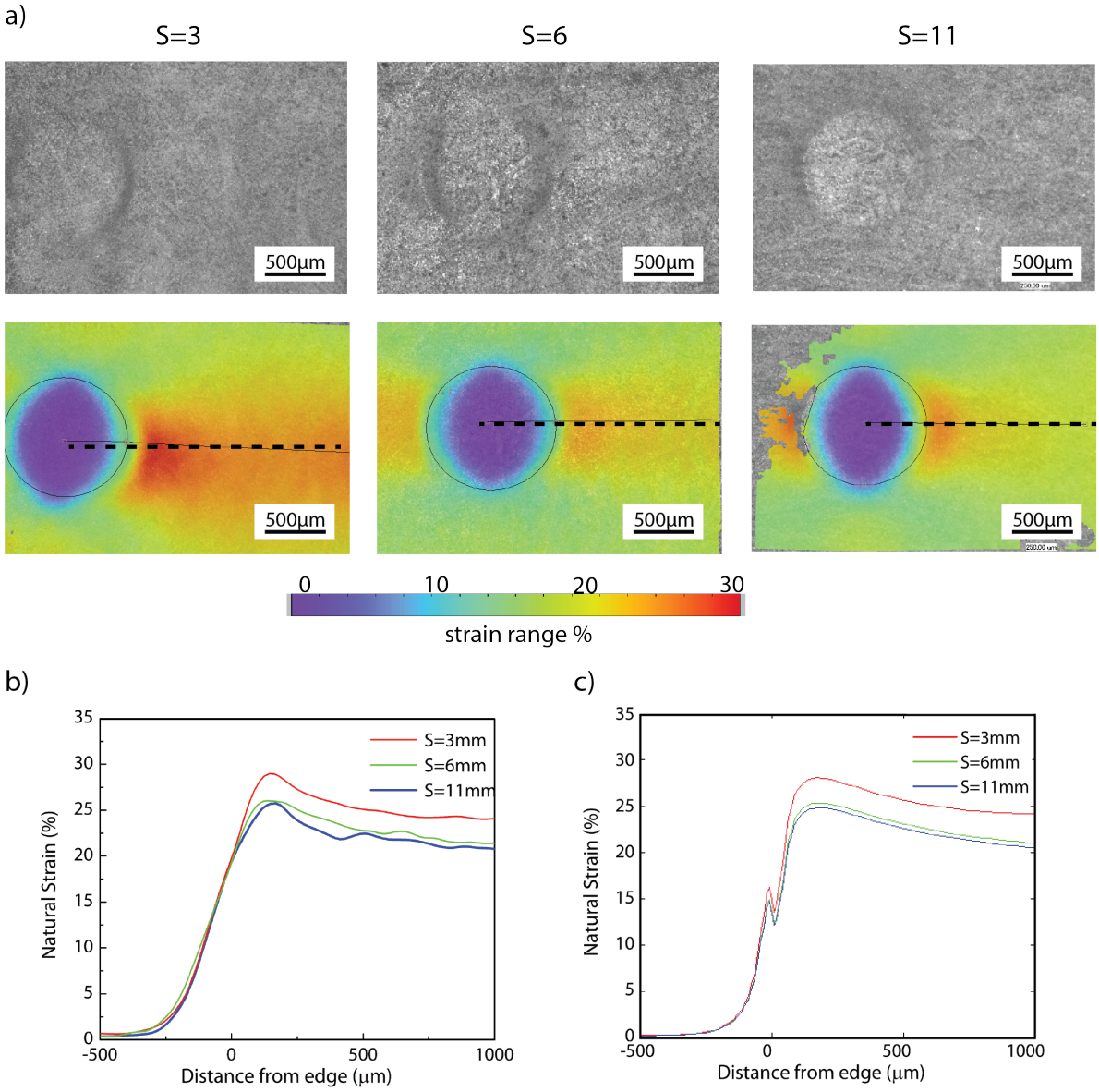
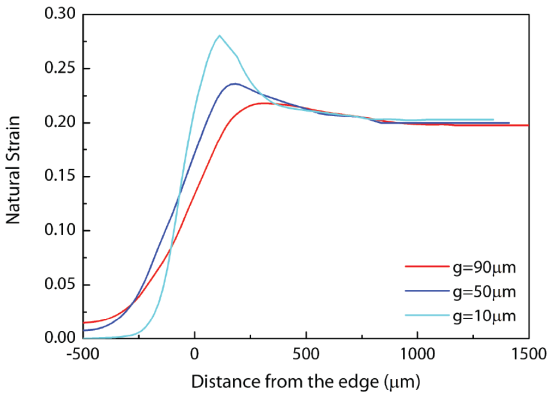


Figure 2.14: Global strain: a) Experimental strain mapping at the top surface of the engineered substrate at different S when 20% macroscopic strain is applied along the x-axis. 50 μm thick, 1mm diameter SU8 platforms are embedded at the bottom of the PDMS membrane. The platforms spacing S varies from 3mm to 11mm; (top) top view, optical images and (bottom) colored strain maps. b) Strain profiles taken along the x-axis from the center of the SU8 platform. c) Corresponding 3D, finite element, simlated profile.

the platform g at a given S was investigated. The intermediate spacing value $S/D = 6$ was chosen, since it is a good compromise between the far field strain and the spacial resolution,



§

Figure 2.15: Experimental strain profile of the engineered substrate with different g, when 20% of strain is applied. SU8 platforms are 1 mm diameter, spaced 6 mm and thickness changing from 10 and 90 μm .

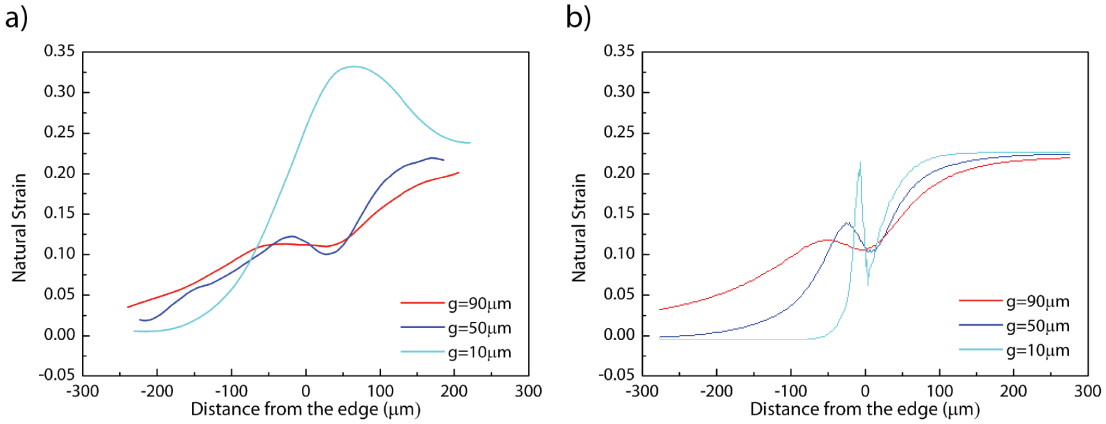


Figure 2.16: Local strain:strain profile of engineered substrate at the rigid-to-soft interface as function of g when 20% of strain is applied: a) experimental results, evaluated with DIC system, b) computed cross-section modeling.

while the thickness of the platform h, and therefore the PDMS above it g, were inversely changing between 10 and 90 μm .

Figure 2.15 shows experimental strain profile as a function of g when 20% macroscopic strain is applied. The far field strain remain stable for all three profiles, while a strain peak is observed on the edge of the platform, caused by the sharp corner of the platform, which become deeper and sharper as g decreases. The thicker is the PDMS above the platform the smoother is the strain profile across the the stiff-to-soft interface. At the same time the penetration depth decreases, for thick PDMS above the platform the penetration depth covers all the area above it and safe area is not anymore produced. To better understand the strain behavior at the rigid-to-elastic interface, we focus only on the strain concentration across the

edges of the embedded platform as function of g. Figure 2.16.a and b shows respectively the experimental and the computed strain profile at the stiff-to-soft interface of engineered substrate sample with different platform thicknesses when a strain of 20% is applied. The computed strain profile have been achieved by implementing the 2D cross-section plain strain equation2.6. It is possible to notice that the experimental set-up fails to capture accurately the sharp strain peak when $g = 10\mu m$. The implemented DIC system is based on a 2D evaluation, thus it cannot capture large out of plane deformation which occurs at the rigid-to-elastic region above the edge of the platforms while the sample is stretched. Therefore for the local design optimization I relied on the computed micromechanical model. For example, for a 50 μm thick and 1 mm diameter SU8 platform, when $\varepsilon_{applied}$=20% the penetration depth is 250 μm per side, so on the 50% of the central area above the platform can be consider safe area.

Thin film processing compatibility

To first demonstrate our approach and its compatibility with multilayer thin-film dry processing, thin film of Aluminum Oxide, AlO_x, disks interconnected by stretchable gold conductors have been deposited. Figure 2.17. a and b show the thin film structure evaporated directly on top of respectively the bare PDMS and the engineered substrate. The optical images represent the substrate-thin film stack before the strain is applied, when the sample is stretched to 20% of strain, and after that the strain is released.

When the samples are stretched catastrophic cracks occurs at low strain ($< 5\%$) in the alumina film on bare PDMS (Fig2.17 (a)). These cracks propagate also in the gold thin film, interrupting the electrical conduction of the interconnects. On the other hand, AlO_x disks patterned on PDMS above the SU8 platforms do not crack, even when cyclically stretched to 20% total strain (Fig 2.17 (b)). The engineered substrate succeeds in its mechanical purpose of preventing that a brittle inorganic material, such as AlO_x, from exceeding its fracture strain ($< 5\%$), even when large deformations are applied. Moreover, the stretchable gold interconnects remain electrically stable over 100 cycles, and no mechanical failure occurs. Figure 2.18 displays the electrical resistance of a gold conductor running across 6 AlO_x islands during stretch cycles to 20% of strain. The outer envelope of the resistance versus cycling is similar to those reported in Refs. [28] and [29].

We have then investigated the morphological structure of the thin Au interconnect after 100 stretch cycle to 20% of strain. The metal shows the microcraked morphology typical of thin gold film thermal evaporated on top PDMS substrate [29], which allow the metal to be reversibly stretchable. Figure 2.19 shows SEM images of the gold interconnect at different positions along the strain direction: in the area above the platform, in the area above the edge of the platform, and in the area in between two platforms. The black dots on the pictures are salts contamination during the releasing step of the substrate from the the Si wafer. During the stretch test, these three positions experience three different maximum strains, and thus strain rates. The strain above the platform remains close to 0, the one

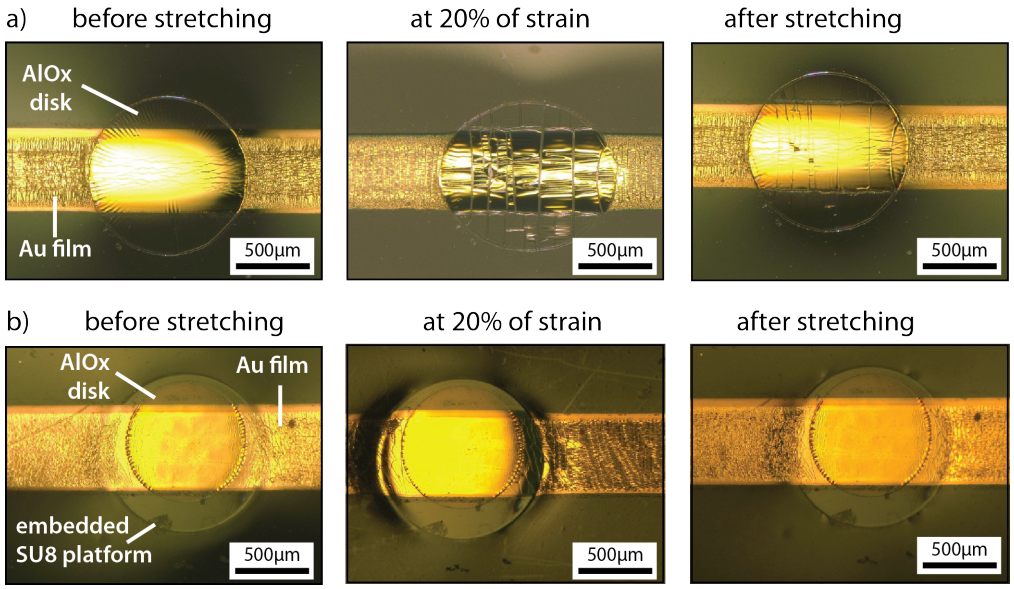


Figure 2.17: Stretchable alumina disks on engineered elastomeric substrate. Top- view optical images recorded during a stretch cycle to 20% applied strain of a) a 150 nm thick, 1mm diameter, AlO_x disk deposited onto 0.1mm thick, bulk PDMS substrate and interconnected with a thin metal conductor (3/30 nm Cr/Au thin films), b) a 150nm thick, 0.75mm diameter, AlO_x disk deposited above 1 mm diameter, 50 μm thick SU8 platform embedded in the 0.1 mm thick PDMS substrate and interconnected with a thin metal conductor (3/30 Cr/Au thin films)

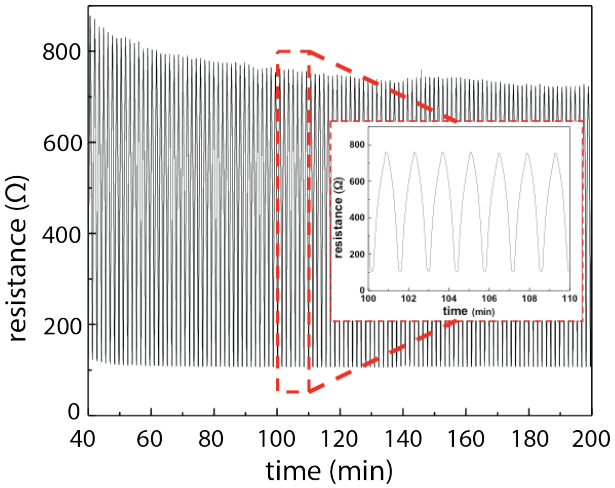


Figure 2.18: Electrical resistance as a function of time of the metallic conduc- tor running across 6 AlO_x disks on engineered substrate during 100 stretch cycles to 20% strain.

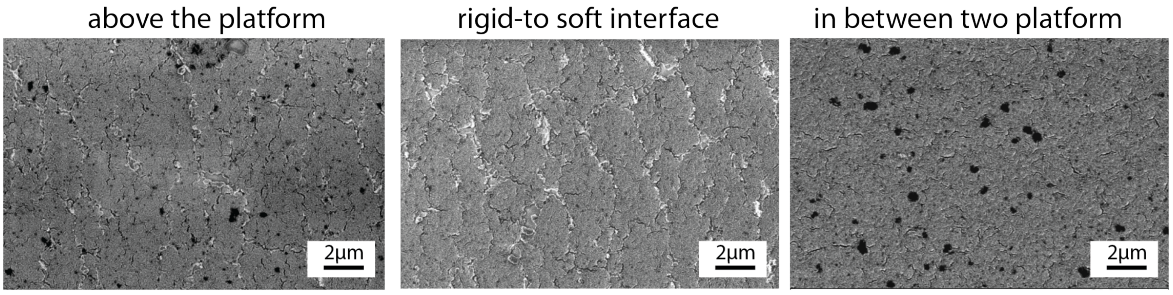


Figure 2.19: SEM picture of the microcracked thin gold interconnect on engineered substrate after 100 stretch cycles to 20% strain at different top surface position.

in between two platform is close to the applied strain (20%), while at the rigid-to-elastic interface the strain raises till almost 30%. It is possible to notice that bigger cracks are formed in the Au interconnect above the edge of the platform (central SEM picture of Figure 2.19) , if compared with other two images. This different morphology is most probably related to the high value of strain and strain rate experienced in this area.
There is an abrupt transition of material properties at the stiff-to-soft interfaces, which cause strain localization above the edge of platform. The interconnect running from the stiff materials to the soft matrix is thus prone to mechanical failures at these points. Reinforcement of such weak points is proposed in the following section.

2.2.4 Conclusions

A simple and robust approach to design and manufacture versatile elastic substrates for stretchable electronic applications was presented. The geometrical configuration of the engineered substrate can be accurately optimized using two types of two-dimensional finite-element analyses prior to the microfabrication of the substrate using standard UV photolithography and materials. Simple guidelines on the geometry and density of the rigid platforms embedded into the elastic matrix as well as on the effective "safe "device island dimensions can be summarized as following:

- the stiff platform thickness should be selected so that the penetration depth is minimized and the strain at its edge is smooth
- the platform densities should be selected so that the far field strain is similar to the applied strain and the spatial resolution of the active electronic is maximized

Moreover, we demonstrate the potential of patternable engineered elastomeric substrate with standard microfabrication processing, thus it is a promising carrier for thin-film device materials and metallization.

2.3 Greyscale-photolitography for Top Surface Strain Optimization

The engineered substrate with embedded strain relief offers the possibility of direct patterning thin film electronics on top of a heterogeneous substrate and prevent them from fracturing when large strain is applied. In the above section the associated design rules to produce reliable stretchable circuitry were presented. Here I further optimize the strain distribution above the top surface in order to suppress the strain concentration above the edge of the embedded platform without reducing the size of the safe area. On one hand we would like to smooth down the strain profile along the interconnects running from the stiff materials to the soft matrix. On the other hand we would try to minimize the penetration depth in order to make the maximum use of the platform. These two factors are inversely related with the platform thickness, so by increasing the thickness the penetration depth decreases, but at the same time the strain concentration at the interface increases.
In this section we propose two different methods to suppress the strain concentration at the stiff-to-soft interface as well as to increase the safe area above the platform:

- sloping the side-wall of the SU8 embedded platforms
- replacing the PDMS matrix with a P-PDMS one with locally graded mechanical properties

Both strategies allow to grade the mechanical stiffness discontinuity of the substrate materials. Both implement greyscale phtolotigraphy.

First greyscale photolitography techniques are introduced. Then materials and methods to fabricate graded P-PDMS and sloped SU8 platforms experiments are described. To demonstrate the validity of the two strategies, the correspondant mechanical results are presented and compared with the previous ones of non-optimized engineered substrate.

2.3.1 Greyscale photolitography

As the name suggests, greyscale lithography methods allow controlled variable-dose exposure to control the development depth in photoresist. They are typically used to create sloped walls or 3D structures in phtosensitive materials, that would normally require multiple exposures with different binary masks.

Current greyscale photolithography technologies can be separated into two primary groups. The first involves maskless direct-beam writing. This technique uses a "software" mask instead of a physical mask, to directly expose the photoresist with a finely focused beam. Software-based techniques include electron-beam (e-beam) lithography [30, 31], focused-ion beam [32] and laser lithography [33]. These enable realization of a wider variety of structures but longer fabrication times and specialized equipment are required.

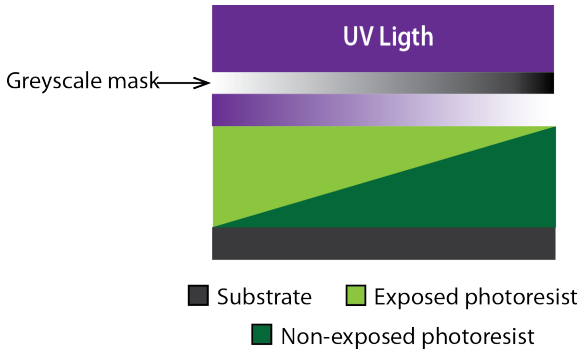


Figure 2.20: The gray-scale optical mask controls the UV light intensity across the wafer using a single exposure, resulting in a sloped profile. After development only the exposed photoresist remains on the substrate.

The second group exploits variable-transmission gray-scale masks. This technique uses a photomask in a conventional exposure system to pattern photoresist. However, gray-scale masks contain variable-transmission patterns that transmit only part of the UV intensity. These UV transmission patterns control the dose delivered to the photoresist. The mechanism to control the UV intensity gradient in gray-scale photolithography varies with each technique and has been demonstrated with continuous-tone [34, 35] and pixelated [**?**, 36, 37]. Continuous-tone masks use an energy-beam sensitive mask material to directly write the optical density onto the mask, thereby controlling the UV absorption. This strategy uses a technology that is limited to five inch or six inch mask plates, which limits the wafer size using contact photolithography and the die size in projection photolithography. On the other hand pixelated grayscale masks use diffraction through many sub-resolution pixels to control the UV dose. These greyscale masks may be written with conventional binary mask technology and therefore are compatible with any plate dimension.
Pixelated masks are less restrictive and allows a simple and low cost solution to vertically pattern photoresist with one single exposure while still using conventional photolithography tools. Therefore I choose pixelated grescale mask techonolgies to slope the side-wall of the SU8 platforms as well as to grade the stifnesss of the P-PDMS around the platforms.

2.3.2 Materials and methods

Three different engineered stretchable substrates were prepared: (i) non optimized, PDMS membrane with cylindrical SU8 platform, (ii) sloped SU8 platforms, PDMS membrane with truncated SU8 cones, and (iii) graded P-PDMS, mechanically graded P-PDMS membrane with cylindrical SU8 platform. In all cases, the elastomeric membrane and SU8 film were 100 μm and 50 μm thick, respectively and the embedded platfrom were arranged in a 3 $\times$ 3 square matrix, with S/D=4 (Fig 2.21).

All engineered substrates were subsequently released from their carrier and cut into 2 $\times$ 4 cm strips for mechanical characterization. Strain mapping of the different substrates, when

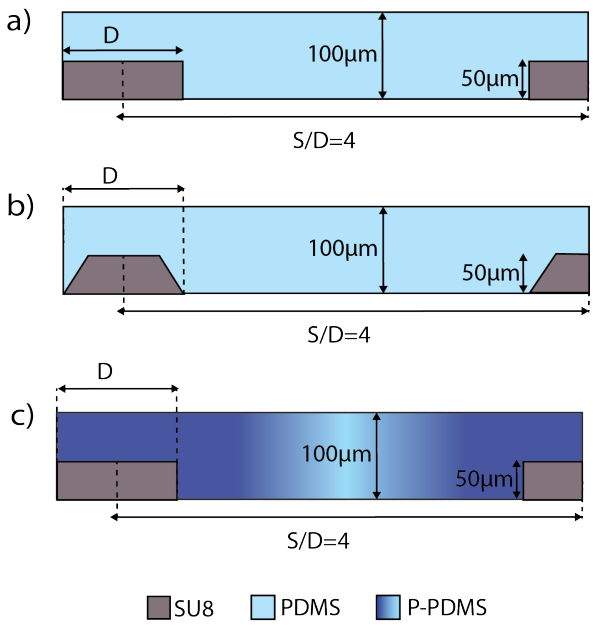


Figure 2.21: Schematic cross sections of three different engineered substrates. SU8 platforms have a diameter D and a thickness of 50 μm. The PDMS or photosensitive P-PDMS membrane is 100 μm thick, and the S/D is equal to 4. a) non optimized structure, b) sloped SU8 platform and c) graded P-PDMS. Proc.

stretched at 20% of strain, have been performed with DIC system as described in the section before. The non optimized structure has been fabricated as described in section2.2.2 ,while the fabrication of the two new structures, sloped SU8 platform and graded P-PDMS, are reported below. Both structures make use of pixelated greyscale mask in order to achieve vertical patterning of the SU8 platform and a continuous grading of the P-PDMS stiffness with a single exposure. All the engineered substrates were manufactured using polymer spin-coating and photolithography using CMi facilities.

Sloped SU8 platform

Since SU8 is a negative photoresist, to manufacture truncated SU8 cones through greyscale photolitography, back exposure is required. Therefore both the support rigid wafer and releasing layer, onto which SU8 is patterned, need to be transparent in order to let the UV light pass trough them and expose the SU8 underneath. Si wafer and Ti/Al releasing layer were replaced by glass wafer and water soluble polymer respectively. The sacrificial material chosen in this study was polyacrylic acid (PAA)because it is transparent, dissolves rapidly in water, which, does not attack the PDMS substrate, but is insoluble in 1-methoxy-2-propanol-acetate (PGMEA), which is developer for epoxy-based SU8. PAA (50 kDa) purchased from Polysciences as a 25% (w/v) solution in water, was neutralized with a saturated solution of NaOH until reaching a pH of 7.5 with a pH indicator band test to improve the wettability of the aqueous solution of PAA on the glass substrates. The solutions was spincoated on the 4

inch glass wafers at 1200 rpm for 30 s, and then cured on a hot plate at 150°C for 15 min. Next, 50 μm thick SU8 2035 (MICRO CHEM) platforms were patterned with a greyscale mask by UV exposure tool (Karl Suss MJB4 contact mask aligner) on the substrate. The wafers were flipped upside down during the exposure in order to produce exposed truncated cone structure on the SU8 layer. Spin speed, soft and post exposure bake temperatures have been optimized in order to avoid cracks formation in the exposed layer. While different exposure doses from 120 to 300 mJ/cm^2 were tested in order to get the desired side-wall slope of the platforms. After development, 100 μm thick PDMS (Sylgard 184, Dow Corning) was spin-coated on the wafers and cured at 150°C for 24 h onto a hot plate. Finally the stretchable substrate was released in DI water.
Figure 2.22 show a schematic of the greyscale photolitography implemented. In the top is represented the greyscale pattern of a single SU8 platform. Since the actual gradient on the Cr mask is the inverse of designed layout, this was designed with a gradient from black to white from the center of the image. The layout was made with Photoshop, which allows to adjust the pixels/centimeter ratio. Four different masks layout have been tested in order to get the desired truncated cone shape with 2 mm bottom diameter D and 0.5 mm side-wall

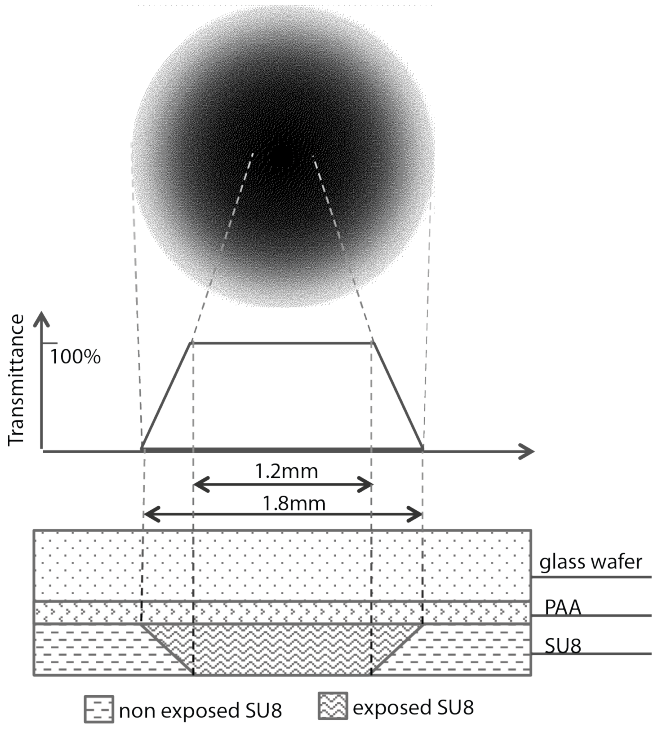


Figure 2.22: Schematic vertical patterning of SU8: on top a particular of the greyscale mask used to pattern sloped SU8 platform, in the middle the exposure fluence required to create truncated cone structure desired through a single exposure process. At the bottom the exposed SU8 structure, flipped upside-down to get the desired shape.

length. The mask layout, which gave resulting patterns closest to the desired ones, was designed using 3900 pixels/centimeter ratio, the maximum for the used software, and it was composed by circular patterns of 2 mm diameter, a black central part of 0.4 mm diameter and a side linear gradient of 0.8 mm. In the middle of figure2.22 energy profile required to produce the sloped SU8 structures is shown. At the edges of the greyscale pattern, no exposure occurs, while at the center the material is fully exposed. The linear gradient of energy from the exposure threshold to 100% of the exposure fluence help in producing sloped side-walls. Resulting exposed structures with truncated cone shape of 1.8 mm bottom diameter D, 0.3 mm side-wall length and 8 mm spacing S were formed in the SU8 layer after development. SU8 platform profiles have been recorded with a mechanical profilometer after development and their morphology was inspected using a Zeiss MERLIN scanning electron microscope (SEM).
Stretch test up to 20% of strain where performed in order to compare the strain distribution among the optimized substrate fabricated with different exposure doses.

Graded P-PDMS

SU8 rigid platforms (1 mm diameter D and 4 mm spacing S) are first patterned with standard photolithography on top of Si wafers with Ti/Al releasing layer, as described in section2.2.2 and then embeeded in a graded P-PDMS membrane. The positive P-PDMS mixture is prepared by mixing the uncrosslinked PDMS (10:1 prepolymer:crosslinker ratio, Sylgard 184, Dow Corning) with benzophenone flakes (3 wt. % of the elastomer mixture; 99% pure, Sigma Aldrich) dissolved in xylene (4.3 wt. % of the elastomer mixture; reagent grade, Fisher Scientific). The P-PDMS was next UV-exposed through a greyscale mask. Since the P-PDMS was not cured yet during the exposure, air gap between the mask and the spincoated polymer was required during UV exposure step. The exposure was implemented with MJB4 mask aligner which allows to set manually the mask-to-P-PDMS air gap ($<$ 1mm). The elastomer was then cured onto a hotplate for 24 h at 150 $^{\circ}C$ and released from aluminum coated Si carrier wafers by anodic dissolution of the metallic film.
Cotton et al. [15] demonstrated that by varying the UV energy absorbed, it is possible to modify the crosslink density of the P-PDMS which leads to adjustment of the polymer elastic modulus. Based on this concept, the P-PDMS membrane was mechanically patterned in order to achieve the highest Young's modulus (non-exposed P-PDMS) above the SU8 platform and the softest E in the region in-between the two platforms (completely exposed P-PDMS). A greyscale mask used to achieve a smooth transition between these two regions was designed employing binary dithering technique. Dither Matlab function was used to convert greyscale square pattern, of 4 mm side with a fully white central circle of 2 mm diameter, into a balck and white image. Here, the density of black dots approximates the average grey level in the original pattern. Figure 2.23 shows on the left the greyscale mask (inverted) pattern and the correspondent fluence transmission which is received by the uncured P-PDMS membrane. Different energy densities from 0 to 18 J/cm^2 were used in order to get an optimal strain

distribution on the top surface.
The linearly graded engineered substrate was then compared with discrete graded one, where P-PDMS is patterned using two concentric binary mask (Fig 2.23 on the right). Three distinct regions of different modulus $E1, E2, E3$, are formed by exposing the P-PDMS with UV light in two steps with exposure energy of 9 J/cm^2 each: first step used a Cr mask M1 with circular 2 mm diameter black regions concentric with the PI platform; step 2 used a similar mask with a larger non exposed region of 3 mm diameter. The resulted patterned elastomer will have a stiff region around the SU8 platform which was never exposed $E1$, a circular contour around it which was exposed with a UV energy dose of 9 J/cm^2, and a softer external region which absorbed a total UV dose of 18 J/cm^2.
Strain map and strain profile of the two graded P-PDMS optimized substrates where measured when a strain of 20% is applied.

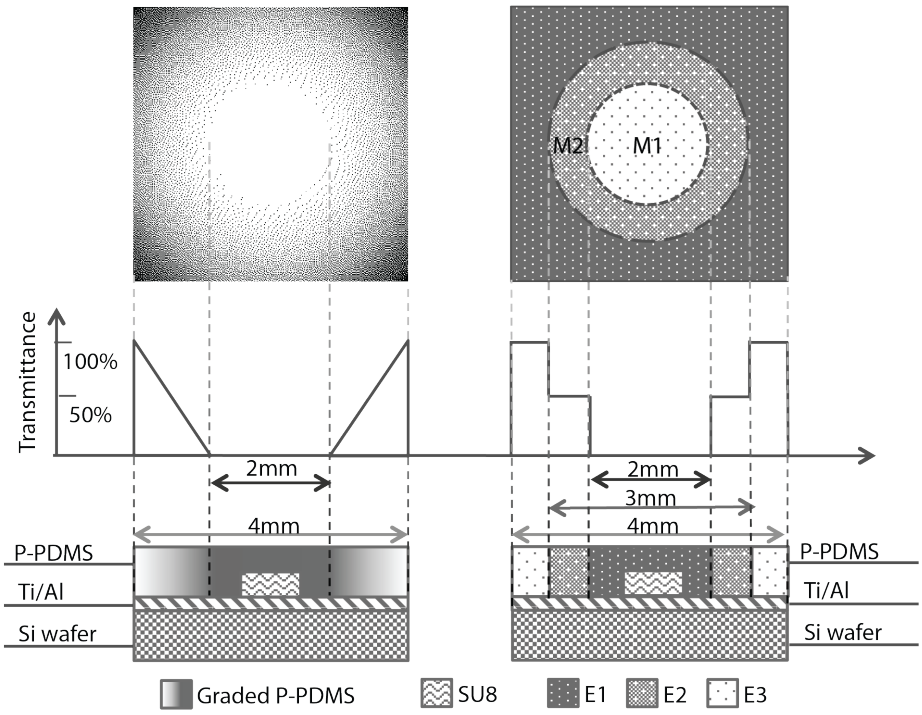


Figure 2.23: Schematic of stiffness patterning of P-PDMS with respectively single exposure greyscale mask and double exposure concentric circle binary mask: (top) detail of the mask pattern corresponding to the platform. At the edges of the pattern the material is fully exposed, while at the center zero exposure occurs. The fluence linear (left) and discrete (right) gradient is required from the exposure threshold to full exposure to grade the stiffness pf the P-PDMS. At the bottom the patterned P-PDMS membranes.

2.3.3 Results and Discussion

Sloped SU8 platforms

The truncated SU8 platforms were prepared with pixelated greyscale mask and three UV exposure energies in order to smooth the sloped side-wall thickness profile of the SU8 platform. The SU8 resist exposed with the larger UV light energy (300 mJ/cm^2) presents the sharpest edge and shortest side-wall length (0.150 mm). Decreasing the UV dose a smoother transition from the rigid to the soft area is achieved as shown in figure 2.24. The platforms exposed with 217 and 120 mJ/cm^2 shown a similar smooth profile. However the measured SU8 platform size does not correspond to the desired one, since they show a

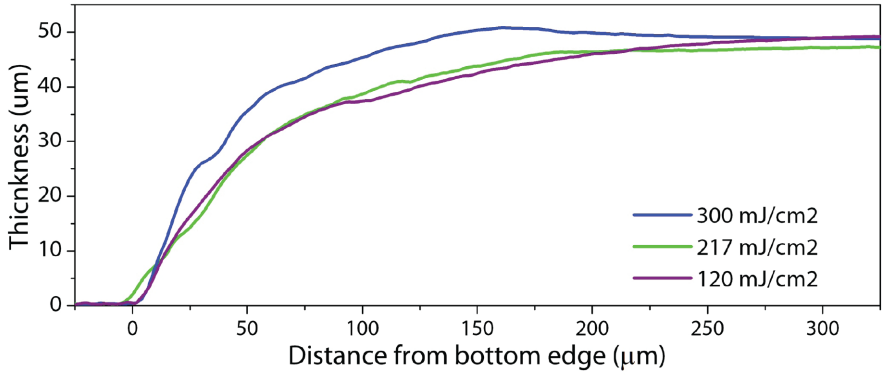


Figure 2.24: Sloped side-wall profiles of truncated SU8 cones platforms patterned with pixelated greyscale mask at different exposure energies.

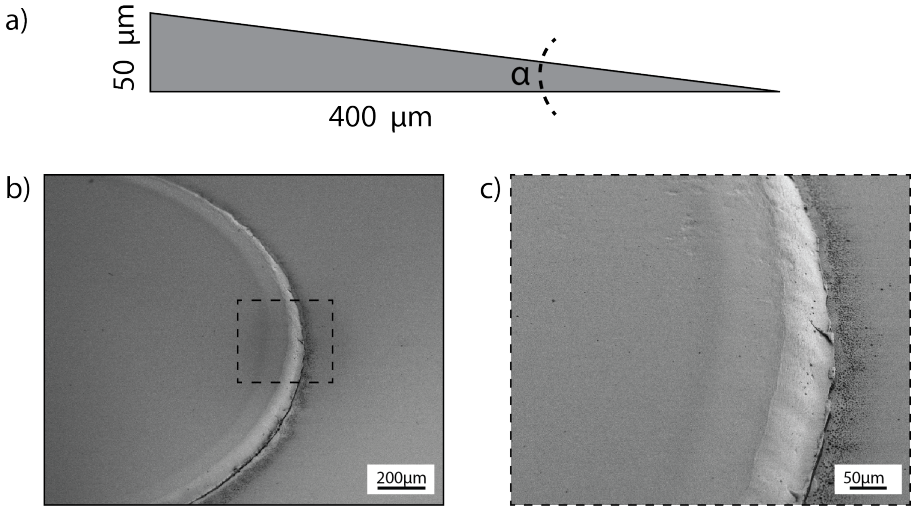


Figure 2.25: Side-wall edge undercut: a) schematic cross section of the side wall, b) SEM image of half truncated SU8 cone platform, c) SEM picture of the undercut side-wall edge detail.

bottom diameter of D=1.8 mm, instead of 2 mm and a side-wall length of 0.3 mm instead of 0.5 mm. These artifacts are possibly due to two different factors. First, the top diameter of the truncated cone d=1.2 mm is much larger thanthe fully exposed central region (0.4 mm diameter). This means that the fluence passing through the initial part of the pixelated gradient is absorbed along all the SU8 layer depth. No slope was produced in the first 0.4 mm of the linear pixelated gradient reducing the desired side-wall length by 0.1 mm per side. Secondly, if we consider the side-wall of the SU8 structure as a right triangle, since the two catheti the length and thickness have different magnitude orders (400 $\mu m \gg 50\mu m$, where the length value have been calculated has the desired one reduced of 0.1 mm as described above) the resulting acute angle is very small ($\alpha \approx 7.11°$) as shown in figure 2.25a. We think that this small angle is undercut during the development step (1^{st} bath PGMEA for 3 min, 2^{nd} bath of PGMEA for 2 min, rinsing in Isopropanol) of approximately 25%. Figure 2.25b and c show SEM images of respectively half truncated SU8 cone platform and a detail of the undercut edge of the side wall, outlined by the dotted line in b. This factor further reduced the side wall length as well as the bottom diameter D of the structure by 0.1 mm per side. Therefore the actual S/D ratio was 4.4.

The exposure energy affects the SU8 platform side-wall, as described above, which consequentially modifies the macroscopic strain distribution on the top surface. Figure2.26 shows the strain profile measured at the top surface when the samples are stretched at 20% of macroscopic strain at different UV exposure dose. Decreasing the exposure energies a smoother transition from the rigid to the soft area is achieved. Alternatively, when the

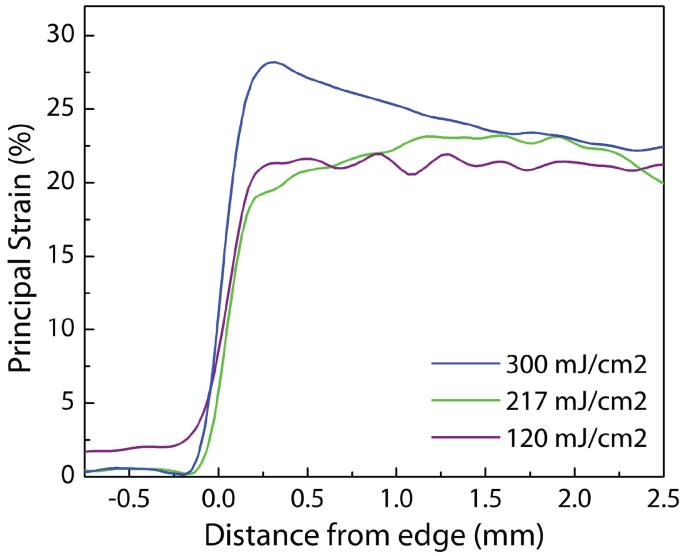


Figure 2.26: Strain profiles taken along the x-axis from the center of the SU8 platform and as function of the total UV exposure energy.

exposure energy was too low (120 mJ/cm^2) the strain above the SU8 platform increases and no safe area (ε <0.5%) is formed. Perhaps the small UV dose affected the stiffness of the photoresist layer and softer SU8 platforms were produced. Substrates prepared with SU8 platforms exposed with 217 mJ/cm^2 UV light energy present the optimal strain profile as no large peak is observed at the interface, the far field strain matches the applied strain, and the rigid surface above the platform is maximal.

Graded P-PDMS

The strain surface analysis was conducted on the engineered substrates prepared with 1mm diameter SU8 platforms embedded in P-PDMS elastomer at different UV exposure energies when a strain of 20% is applied (Fig 2.27).

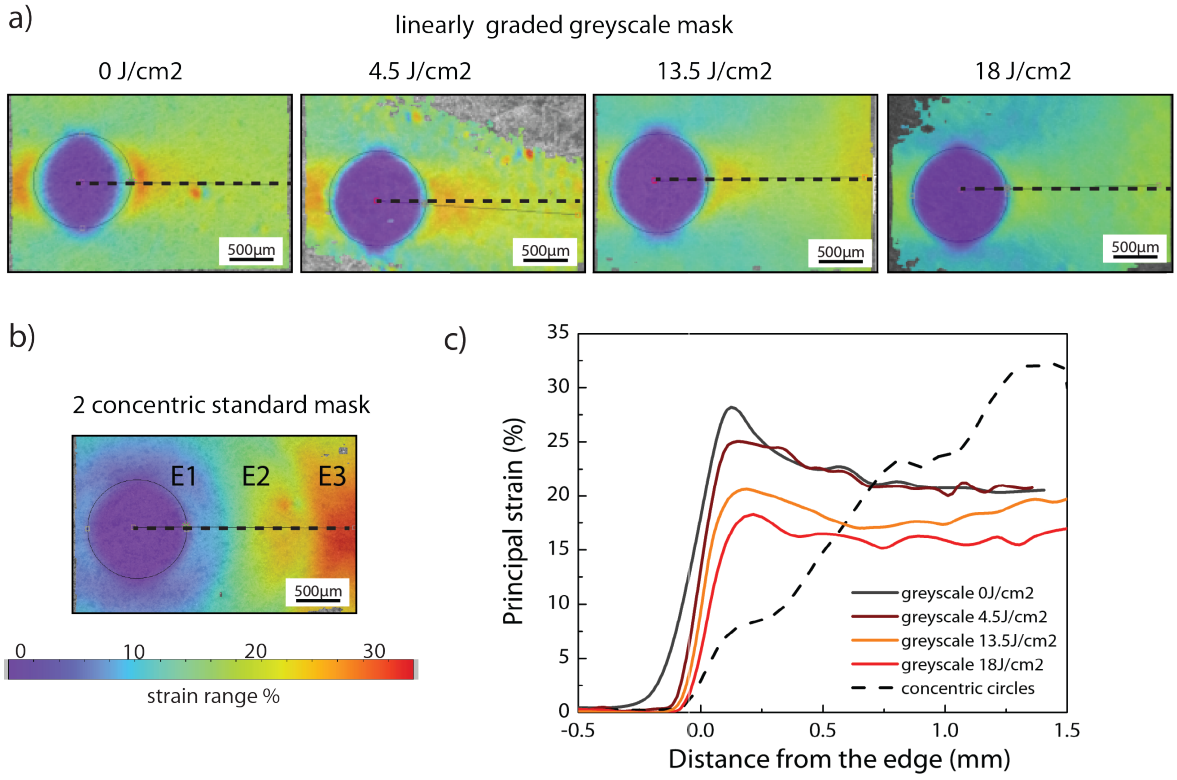


Figure 2.27: Surface strain experimental measurement of stretched engineered substrates prepared with photosensitive P-PDMS when 20% strain is applied across the sample. a) and b) show the strain maps of P-PDMS substrate with respectively continuous patterned compliance with greyscale mask at different exposure energies and 3 moduli patterned compliance with 2 concentric mask; c) strain profiles taken along the x-axis from the center of the SU8 platform and as function of the total UV exposure dose (J/cm^2) and implemented mask.

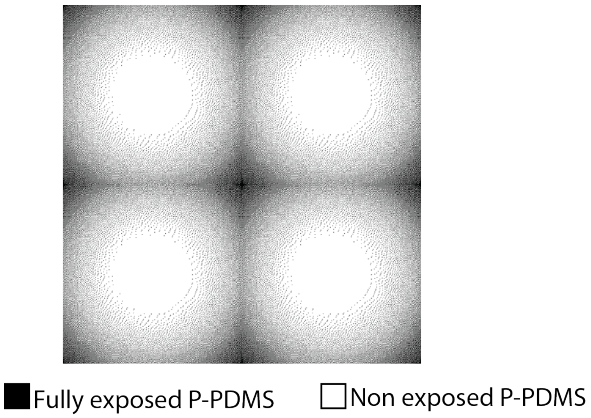


Figure 2.28: Greyscale mask pattern (inverted) used to linearly patter the P-PDMS around 4 platforms. The P-PDMS area of 2 mm diameter around the platform is not exposed and therefore owns an higher Young's modulus, which decrease by moving away from the platform. Softer cross areas are formed at the intersection of 4 platform which accommodate most of the applied strain.

The absorbed UV light energy modify the crosslinking of the photosensitive elastomer and therefore its stiffness. The non-exposed P-PDMS (2 mm diameter area around the SU8 platform) and fully exposed P-PDMS (in between the 2 platforms) had a modulus of $\sim$ 2.35 MPa and $\sim$ 0.79 MPa, respectively (Chapter 4).
Engineered P-PDMS substrates that were not exposed to UV light displayed identical properties to PDMS substrates: the no-strain area above the SU8 is smaller than the SU8 diameter ($\sim 0.5D$), a large peak strain is observed at the edge of the platform (strainpeak $\sim$28%) and the far field strain is slightly larger than the applied strain.

Increasing the UV energy absorbed by the P-PDMS and grading its profile away from SU8 platform using a greyscale mask improves all parameters of the engineered substrate In fact by increasing the exposure dose, the difference in the Young's moduli between the exposed and the non-exposed area increases. For exposure energy of 18 mJ/cm^2, the safe area is covering almost all the area above the platform, the peak strain at the edge is suppressed and a continuous strain, lower than the applied strain, is produced from the edge of the platform to the far field. Here the most part of the strain is accommodated by the softer regions formed at the intersection of 4 greyscale patterns as shown in figure 2.28. The top surface strain of the P-PDMS substrate patterned with two concentric binary masks, show the smoothest profile, but its far field strain raises up to more than 30%. Figure2.27 b shows the strain map distribution of the discrete patterned P-PDMS substrate. Three distinct concentric strain regions are produced which correspond to the tree patterned P-PDMS moduli, $E1$ = 2.35 MPa, $E2$=1.1 MPa. $E3$=0.79 MPa. Most of the strain is accommodated by the softer region, $E3$, this produce a large strain concentration in the area in between two platforms, while the peak of strain is completely suppressed at the rigid-to-soft interface zone.

Therefore the P-PDMS substrate patterned by the greyscale mask with the largest exposure energy offer the optimal solution for the graded P-PDMS strategy, since is able to

suppress the peak of strain above the platform edge while reducing the far field strain.

2.3.4 Conclusions

Figure 2.29 compares the strain line profiles between the 3 different approaches: non optimized engineered substrate, sloped SU8 platforms (exposure energies = 217 mJ/cm^2) and graded P-PDMS (exposure energy = 18 mJ/cm^2).

To some extent, all three allow for a no-stretch area, and moderate strain across the surface with regards to the applied strain. However the optimized P-PDMS and sloped SU8 substrates show improved top surface strain distribution compared to the non optimized one: (i) safe area ($\varepsilon < 0.5\%$) is maximized, its diameter matches that of the SU8 platform and (ii) the strain concentration above the edge of the platform is suppressed. Moreover, with linearly graded P-PDMS substrate is possible to reduce also the far filed strain, which is lower than the applied one. This allows to reduce the strain along the elastic conductors interconnecting electronic devices above the safe areas, without increasing the spacing. Therefore grading the mechanical modulus of the P-PDMS, combined with embedding stiff platforms in the elastomer matrix, provides the most promising mechanical design for engineered substrate with embedded strain relief.

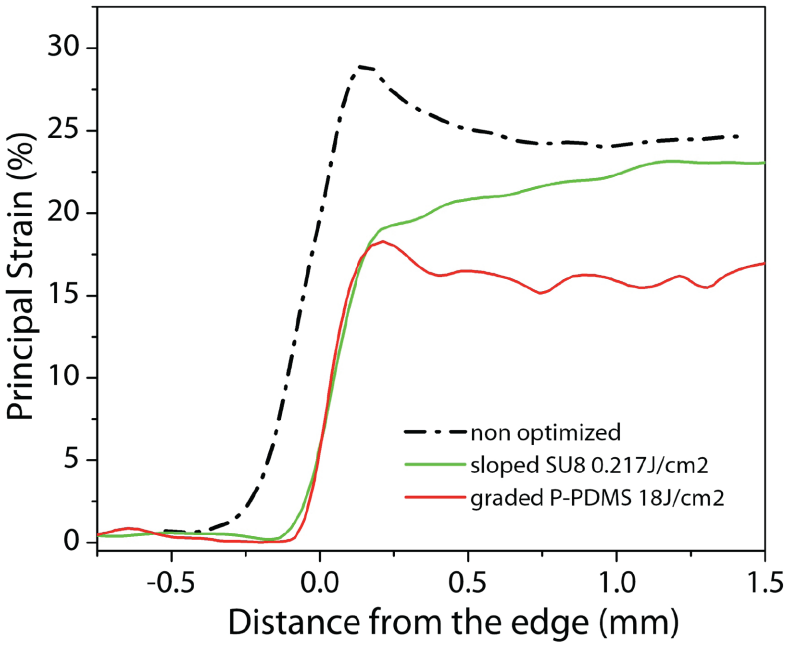


Figure 2.29: Strain profiles for each of the three substrate designs: non optimized, sloped SU8 platform, graded P-PDMS. The profiles are taken along the x-axis from the center of the SU8 platform

2.4 Optimized Engineered Substrate Layout

Mechanical and geometric arguments are of primary importance in designing a stretchable substrate for soft electronic circuits.
In the proposed approachs, engineered substrate with embedded strain relief, embedded platform geometry and density have been adjusted in order to impose a desired strain distribution on the top surface to properly host electronic circuits. Moreover, mechanically grading the elastic modulus of the elastomer surrounding the platforms enables to further optimize the top surface strain, by maximizing the safe area above the platforms, suppressing the peak of strain at the stiff-to-soft interface and reducing the far field strain.

Here I propose a solution to reduce the strain along the potential electrical interconnects location. This latest approach is based on a new arrangement of the SU8 platforms, so that the uni-axial applied strain is not anymore parallel to the platform interconnections direction and therefore the strain along these lines is reduced. To further strengthen these interconnections tracks the elastomer compliance is photopatterned with single exposure, standard binary mask, in order to create stiffer meshes along the interconnection paths. New substrate with rhomboidal and hexagonal layout and their mechanical characterization are presented below.

2.4.1 Materials and Methods

Engineered stretchable substrate was prepared with 10:1 P-PDMS substrate designed with embedded strain relief structures as described in section 2.3.2.

SU8 circular platforms (50 μm thick, 1 mm diameter) were embedded in 100 μm thick P-PDMS membrane. Next, the elastomer was UV-exposed (at 18 J/cm2 energy density) through a chromium mask with rhomboidal and hexagonal non-exposed patterns and cured at 150 $^{\circ}C$ for 24 h. Figure 2.30 illustrate the schematic top view and cross section of the two implemented layouts. The non-exposed patterns of the rhomboidal layout (Fig 2.30 a and b) have a side length L and width W of 3 mm and 1.5 mm respectively. The spacing S between two adjacent platforms in the strain direction is 4 mm, while a fully exposed rhomboidal area, with diagonal of 2.5 mm, is formed in the center of 4 connected platforms. Similarly, hexagonal non exposed patterns having L=2.5 mm, W=1.5 mm and S=4.4 mm, produce fully exposed hexagonal area, of 2.8 mm width, in the center of 6 connected platforms (Fig 2.30 c and d).
For comparison, substrates with rhomboidal and hexagonal SU8 platform layouts were also prepared with standard 10:1 PDMS.
The substrates were then released from aluminum coated Si carrier wafers by anodic dissolution of the metallic film. Sample of 2 $\times$ 4 cm were cut and prepared for mechanical characterization. Uni-axial stretch test up to 20% of strain were performed and strain distribution on the top surface was monitored with DIC system as described in section 2.2.2.

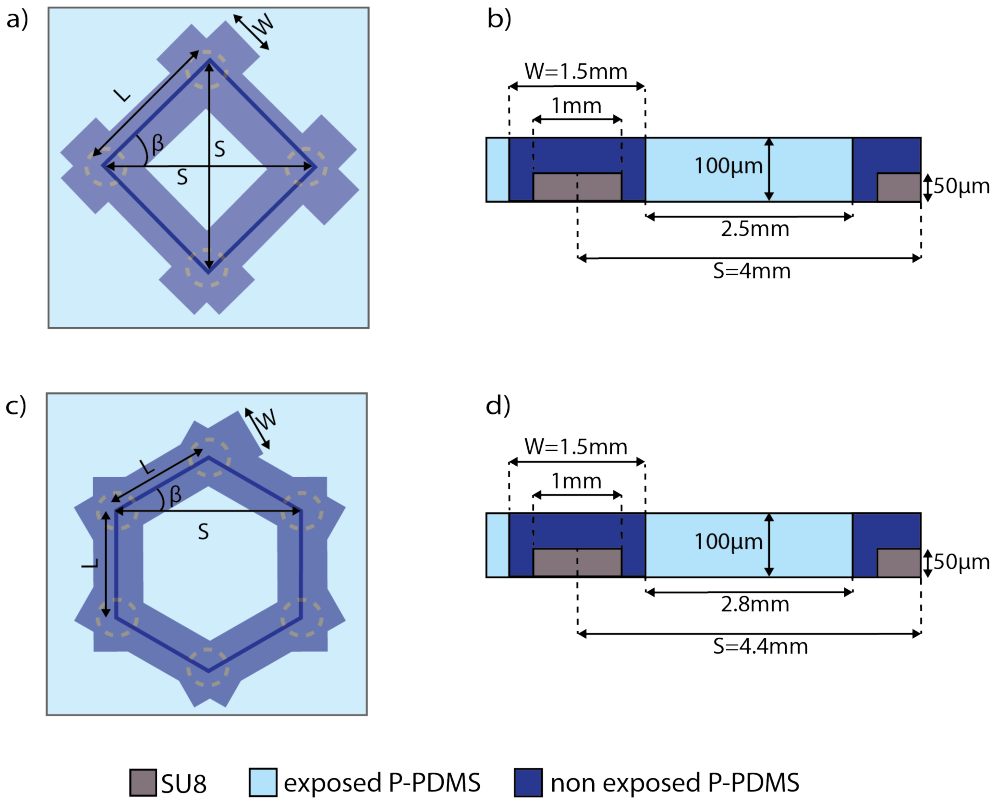


Figure 2.30: Engineered stretchable substrates with optimized layout. The non exposed P-PDMS patterns have side length L, width W and spacing S. a) and b) illustrate the top view and cross section of the engineered substrate design with rhomboidal layout. A fully exposed rhomboidal area of 2.5 mm diagonal is formed in between 4 platforms. c) and d) show the top view and cross section of hexagonal layout. Fully exposed hexagonal of 2.8 mm width is formed in between 6 platforms.

2.4.2 Results and Discussion

The implemented layouts have been chosen in order to decrease the strain along the elastic conductor interconnecting adjacent platforms under uni-axial strain.

Both in hexagonal and rhomboidal disposition the platforms are designed to be interconnected diagonally and/or perpendicularly to the applied strain. Thus the strain on the interconnection line is reduced proportionally to the angle β formed between the applied strain direction (spacing direction) and the interconnection line. If we consider a uniform substrate with homogeneous mechanical properties, applaying a strain in a direction x, ε_x, the resulting strain in a direction z, ε_z, forming an angle β with x is given by the following equation:

$$\varepsilon_z = \varepsilon_x \cdot cos\beta \tag{2.7}$$

Therefore the larger is the angle β the smaller is the resulting strain in direction z.

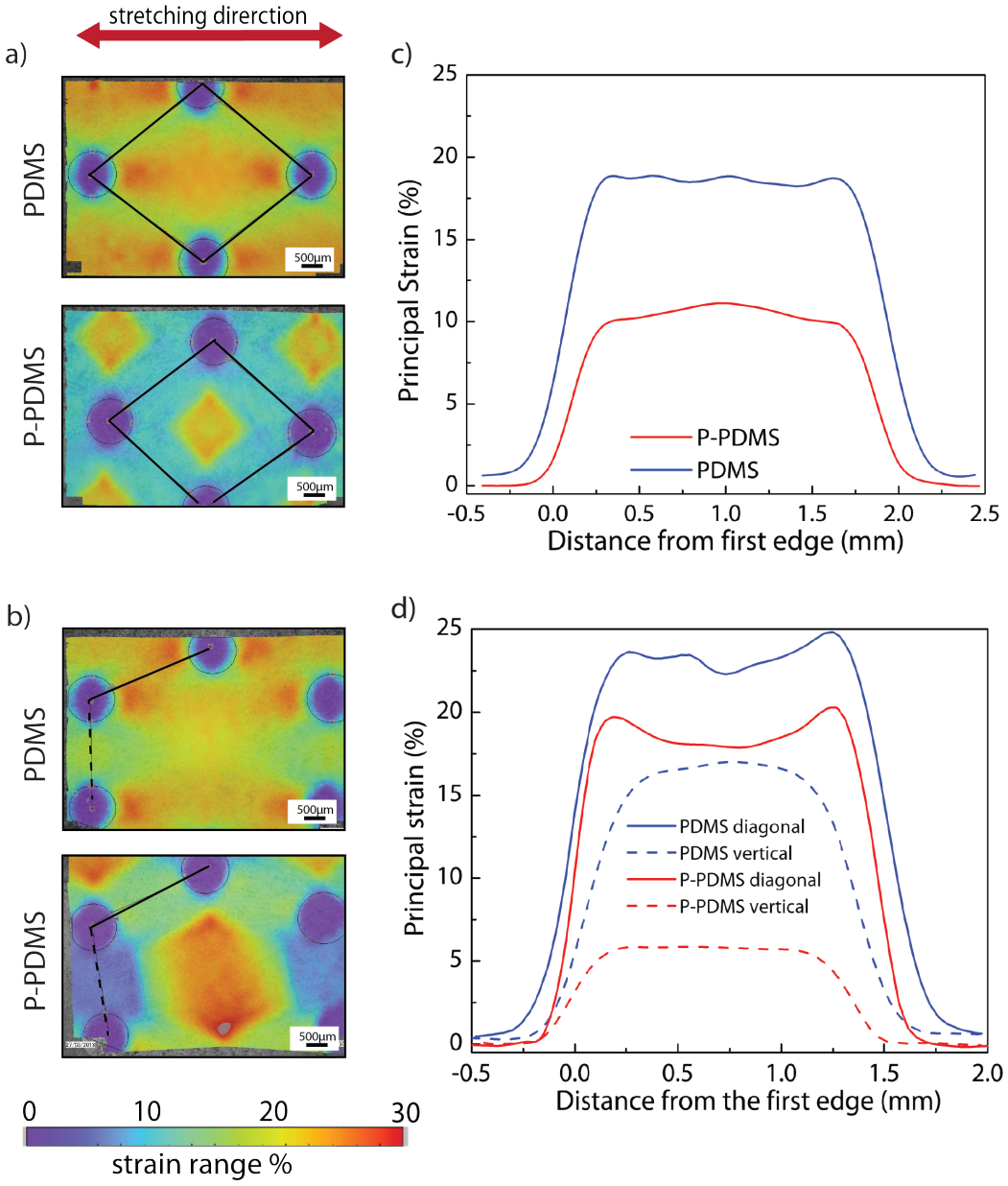


Figure 2.31: Surface strain experimental measurement of stretched engineered substrates prepared with photosensitive P-PDMS when 20% strain is applied across the sample. a) and b) experimental strain maps (principal strain) of the surface of the PDMS (*top*) and P-PDMS (*bottom*) engineered substrate with respectively rhomboidal and hexagonal layout; c) average strain profile along four rhomboidal sides L for both substrate types, d) strain profile along vertical (dotted line) and diagonal (continuous line) hexagonal sides L for both substrate type.

Implemented engineered substrates are characterized by heterogeneous mechanical compliance, thus the resulting strain distribution on the top surface is influenced also by this non uniformity. Strain maps and strain profile of both patterned P-PDMS and bare PDMS substrates with optimized SU8 layouts, stretched at 20% of strain, are shown in figure 2.31. The surface immediately above the SU8 platforms sustained no deformation ($\varepsilon < 0.5\%$) independently of the platforms layout or the elastomeric materials. However this safe area is maximal in the substrate with patterned P-PDMS. As described in the previous section, when the P-PDMS is exposed to UV light, its elastic modulus E decreases proportionally to the absorbed energy. In our experiment non-exposed P-PDMS patterns and fully exposed P-PDMS rhomboidal and hexagonal areas have a modulus of $\sim$2.35 MPa and $\sim$0.79 MPa, respectively. Therefore in the substrate with P-PDMS patternerd compliance, the SU8 platforms are surrounded by stiffer P-PDMS and the no-stretch zone diameter, produced on the top surface, matches that of the SU8 platform. Moreover, compared to the PDMS substrates, the strain across the non-exposed P-PDMS rhomboidal and hexagonal sides is smaller. Zones of high strain (>20%) are concentrated in focal zones in-between the SU8 platforms where softer rhomboidal and hexagonal areas are formed. Figure2.31 (c) and d illustrate the strain profile along the interconnection lines of respectively rhomboidal and hexagonal layout. In both designs the strain along the interconnection directions is smaller than the applied strain independently of the elastomeric material. However, in the substrates with patterned P-PDMS compliance, these strain profile are further reduced. This reduction is constant in the rhomboidal case, where the strain along the four sides is decreased of approximately 50% (β =45°). While, in the hexagonal layout we have two different strain profiles: the vertical profiles, perpendicular to the applied strain direction, shows a very low strain ($\sim$ 5%), and diagonal profiles whose strain is higher than the rhomboidal one, due to the smaller angle (β =30°) as well as shorter side length L.
Therefore the rhomboidal layout of the SU8 platform together with patterned P-PDMS compliance along the interconnections side presents an optimal solution for optimized layout of engineered substrate under uni-axial stretching.

2.4.3 Conclusions

The local softening of the P-PDMS combined with the layout rearrangement of the platforms, significantly improves the strain distribution across the engineered substrate. The non - UV exposed mesh defines the potential location of electrical interconnects running in-between the safe (no-strain) zones.
This approach not only allows to increase the safe area above the SU8 platforms as well as to reduce the strain concentration at the interface, but it enables to further reduce the strain along the interconnection sides between adjacent platform, thus preventing the electrical interconnects to experience large deformation. However this approach is limited only to uni-axial strain. The presented mechanical analysis is valid only if the strain is applied in the x direction, or in the orthogonal one. In order to accommodate multidirectional deformation it would be necessary to implement a further isotropic design.

2.5 Conclusions

In summary, a simple and robust approach to design and manufacture stretchable substrate for soft electronic applications was developed.

The stretchable substrate is based on the "pixelated"architecture, where rigid islands or "pixels"are distributed on the stretchable substrate and interconnected by elastic wiring. The stiff islands can host the electronic devices preventing them form exceeding their fracture strain. When the whole system is stretched, the substrate exposed between the rigid islands, together with the conductors that run across it, accommodate the elastic strain, isolating the rigid islands from the applied macroscopic strain.

Engineered substrates with embedded strain relief are prepared by combining rigid platforms embedded in a silicone membrane, and stretchable thin gold film interconnects. Since the platforms are significantly stiffer than the surrounding rubbery matrix, the elastomer volume immediately above the platform is little strained when the substrate is macroscopically stretched. Therefore intrinsic stiff regions are produced, while maintaining plain and uniform top surface onto which electronic device materials can be directly processed. Non-stretchable safe areas ($\varepsilon < 0.5\%$) are formed on the elastomer top surface, which can host fragile devices and protect them from large mechanical deformations. The proposed strain relief method enables for planar but mechanically engineered heterogeneous elastic substrate compatible with direct fabrication of thin-film devices was developed.

Optimization of the strain distribution on the top surface was performed in order to maximize the non-stretchable area available for the electronic devices and to minimize the strain concentration at the stiff-to-soft interface and in the far field. The achieved results are summarized below:
(i) by changing the thickness and densities of the embedded platform it possible to adjust the penetration depth of the safe area, to smooth strain concentration and the interface and to reduce the far filed strain.
(ii) further grading the mechanical compliance of the elastomeric matrix around the embedded platforms allow for maximizing the safe areas and suppress the peak of strain at the interface.
(iii) combining the local softening of P-PDMS with an optimized interconnected SU8 platforms layout enables to reduce also the strain along the elastic wiring simply running across the different safe areas.

The results described in this chapter highlight the primary importance of mechanical and geometric arguments in designing a stretchable substrate for soft electronic circuits. These results are universally applicable as long as the limit of allowable strain on a device, component or circuit is known, and a suitable elastic wiring technology is available.
Furthermore the compatibility of the proposed planar but mechanically engineered heterogeneous substrate with standard, additive thin-film processing was demonstrated, thereby,

promising low cost manufacturing and scalability.
The proposed engineered elastomeric substrate is therefore a promising carrier for thin-film device materials and metallization. However, it may also be used as a generic elastic substrate for stretchable circuits prepared with alternative technologies, such as transfer-printing or lamination of inorganic thinned devices.

References

[1] S. Wagner and S. Bauer, "Materials for stretchable electronics," *MRS Bull.*, vol. 37, no. 03, pp. 207–213, mar 2012. [Online]. Available:

[2] Z. Suo, "Fracture in Thin Films," *Encycl. Mater. Sci. Technol.*, pp. 1–17, 2001. [Online]. Available:

[3] S. Wagner, "Electronic skin: architecture and components," *Phys. E Low-dimensional Syst. Nanostructures*, vol. 25, no. 2-3, pp. 326–334, nov 2004. [Online]. Available:

[4] J. a. Rogers, T. Someya, and Y. Huang, "Materials and mechanics for stretchable electronics." *Science*, vol. 327, no. 5973, pp. 1603–7, mar 2010. [Online]. Available:

[5] J. W. M. Shi, J. Yoon, S.-I. Park, Z. Liu, and Y. Huang, "Stretchable GaAs Photovoltaics with Designs That Enable High Areal Coverage," *Adv. Mater.*, vol. available, 2011.

[6] S. P. Lacour, "Stretchable Thin-Film Electronics," *Stretchable Electron.*, no. ii, pp. 81–109, 2012.

[7] P. I. Hsu, R. Bhattacharya, H. Gleskova, M. Huang, Z. Xi, Z. Suo, S. Wagner, and J. C. Sturm, "Thin-film transistor circuits on large-area spherical surfaces," *Appl. Phys. Lett.*, vol. 81, no. 9, pp. 1723–1725, 2002.

[8] P. I. Hsu, M. Huang, Z. Xi, S. Wagner, Z. Suo, and J. C. Sturm, "Spherical deformation of compliant substrates with semiconductor device islands," *J. Appl. Phys.*, vol. 95, no. 2, p. 705, 2004. [Online]. Available:

[9] N. Lu, J. Yoon, and Z. Suo, "Delamination of stiff islands on stertchable substrates," *Int. J. Mat. Res.*, pp. 717–722, 2007.

[10] J.-Y. Sun, N. Lu, J. Yoon, K.-H. Oh, Z. Suo, and J. J. Vlassak, "Inorganic islands on a highly stretchable polyimide substrate," *J. Mater. Res.*, vol. 24, no. 11, pp. 3338–3342, 2009.

[11] H. Cheng, J. Wu, M. Li, D.-H. Kim, Y.-S. Kim, Y. Huang, Z. Kang, K. C. Hwang, and J. a. Rogers, "An analytical model of strain isolation for stretchable and flexible electronics," *Appl. Phys. Lett.*, vol. 98, no. 6, p. 061902, 2011. [Online]. Available:

[12] S. Wagner, S. P. Lacour, J. Jones, P.-h. I. Hsu, J. C. Sturm, T. Li, and Z. Suo, "Electronic skin: architecture and components," *Phys. E Low-dimensional Syst. Nanostructures*, vol. 25, no. 2-3, pp. 326–334, nov 2004. [Online]. Available:

[13] S. P. Lacour, S. Wagner, R. J. Narayan, T. Li, and Z. Suo, "Stiff subcircuit islands of diamondlike carbon for stretchable electronics," *J. Appl. Phys.*, vol. 100, no. 1, p. 014913, 2006. [Online]. Available:

[14] I. M. Graz, D. P. J. Cotton, A. Robinson, and S. P. Lacour, "Silicone substrate with in situ strain relief for stretchable thin-film transistors," *Appl. Phys. Lett.*, vol. 98, no. 12, p. 124101, 2011. [Online]. Available:

[15] D. P. J. Cotton, A. Popel, I. M. Graz, and S. P. Lacour, "Photopatterning the mechanical properties of polydimethylsiloxane films," vol. 054905, no. January, pp. 1–6, 2011.

[16] R. M. Erb, K. H. Cherenack, R. E. Stahel, R. Libanori, T. Kinkeldei, N. Münzenrieder, G. Tröster, and A. R. Studart, "Locally Reinforced Polymer-Based Composites for Elastic Electronics." *ACS Appl. Mater. Interfaces*, jun 2012. [Online]. Available:

[17] a. Robinson, a. Aziz, Q. Liu, Z. Suo, and S. P. Lacour, "Hybrid stretchable circuits on silicone substrate," *J. Appl. Phys.*, vol. 115, no. 14, p. 143511, apr 2014. [Online]. Available:

[18] P. Jothimuthu, A. Carroll, A. A. S. Bhagat, G. Lin, J. E. Mark, and I. Papautsky, "Photodefinable PDMS thin films for microfabrication applications," *J. Micromechanics Microengineering*, vol. 19, no. 4, p. 045024, apr 2009. [Online]. Available:

[19] A. Mata and A. J. Fleischman, "Characterization of Polydimethylsiloxane (PDMS) Properties for Biomedical Micro / Nanosystems," *Biomed. Microdevices*, vol. 2, pp. 281–293, 2005.

[20] D. Corning, "Electronics Sylgard Â® 184 Silicone Elastomer," *Prod. Datasheet*, pp. 1–3, 2013.

[21] J. C. McDonald and G. M. Whitesides, "Poly(dimethylsiloxane) as a Material for Fabricating Microfluidic Devices," *Acc. Chem. Res.*, vol. 35, no. 7, pp. 491–499, jul 2002. [Online]. Available:

[22] F. Schneider, T. Fellner, J. Wilde, and U. Wallrabe, "Mechanical properties of silicones for MEMS," *J. Micromechanics Microengineering*, vol. 18, no. 6, jun 2008. [Online]. Available:

[23] A. N. Gent, *Engineering with Rubber - How to Design Rubber Components (2nd edition)*, 2nd ed. Hanser Publishers, 2001.

[24] H. Cong and T. Pan, "Photopatternable Conductive PDMS Materials for Microfabrication," *Adv. Funct. Mater.*, vol. 18, no. 13, pp. 1912–1921, jul 2008. [Online]. Available:

[25] A. A. S. Bhagat, P. Jothimuthu, and I. Papautsky, "Photodefinable polydimethylsiloxane (PDMS) for rapid lab-on-a-chip prototyping." *Lab Chip*, vol. 7, no. 9, pp. 1192–7, sep 2007. [Online]. Available:

[26] V. Seidemann, J. Rabe, M. Feldmann, and S. Büttgenbach, "SU8-micromechanical structures with in situ fabricated movable parts," *Microsyst. Technol.*, vol. 8, no. 4-5, pp. 348–350, 2002.

[27] Gersteltec, "SU8 Gm 1070, Datasheet," pp. 1–9, 2005.

[28] I. M. Graz and S. P. Lacour, "Flexible pentacene organic thin film transistor circuits fabricated directly onto elastic silicone membranes," *Appl. Phys. Lett.*, vol. 95, no. 24, p. 243305, 2009. [Online]. Available:

[29] S. P. Lacour, D. Chan, S. Wagner, T. Li, and Z. Suo, "Mechanisms of reversible stretchability of thin metal films on elastomeric substrates," *Appl. Phys. Lett.*, vol. 88, no. 20, p. 204103, 2006. [Online]. Available:

[30] S. Balslev, T. Rasmussen, P. Shi, and a. Kristensen, "Single mode solid state distributed feedback dye laser fabricated by gray scale electron beam lithography on a dye doped SU-8 resist," *J. Micromechanics Microengineering*, vol. 15, no. 12, pp. 2456–2460, 2005.

[31] M. D. Henry, M. J. Shearn, B. Chhim, and a. Scherer, "Ga(+) beam lithography for nanoscale silicon reactive ion etching." *Nanotechnology*, vol. 21, no. 24, p. 245303, 2010.

[32] V. Kudryashov, X. Yuan, W. Cheong, and K. Radhakrishnan, "G rey scale structures formation in SU-8 with e-beam and UV," vol. 68, pp. 306–311, 2003.

[33] M. Rossi and H. Schulz, "Elements By Direct Laser Writing in Photoresists," vol. 33, no. 11, pp. 3556–3566, 1994.

[34] T. Dillon, A. Sure, J. Murakowski, and D. Prather, "Continuous-tone grayscale mask fabrication using high-energy-beam-sensitive glass," *J. Microlithogr. Microfabr. Microsystems*, vol. 3, no. 4, p. 550, 2004. [Online]. Available:

[35] J. M. Dykes, D. K. Poon, J. Wang, D. Sameoto, J. T. K. Tsui, C. Choo, G. H. Chapman, A. M. Parameswaren, and B. L. Gray, "¡title¿Creation of embedded structures in SU-8¡/title¿," vol. 6465, pp. 64 650N–64 650N–12, jan 2007. [Online]. Available:

[36] B. Electronics, "Fabrication of Fluidic Manifold Systems Using Single Exposure Greyscale Masks," vol. 4404, pp. 231–237, 2001.

[37] C. M. Waits, A. Modafe, and R. Ghodssi, "Investigation of gray-scale technology for large area 3D silicon MEMS structures," *J. Micromechanics Microengineering*, vol. 13, no. 2, pp. 170–177, 2002.

3 Stretchable thin-film trnasistor*

Contents

*Alessia Romeo, Stéphanie P. Lacour , "Stretchable metal oxide thin film transistors on engineered substrate for electronic skin applications," *IEEE-EMBC,* 2015.

3.1 Introduction

Stretchable electronics are integrated circuitry that can stretch, twist and deform into complex curvilinear shapes while maintaining their electrical performance. Stretchable devices provide interesting opportunities, particularly in biomedical applications, where shape adaptability is a highly desirable feature [1, 2].
Two main challenges need to be overcome when implementing direct fabrication of electronic devices on soft substrates:

- integration of stiff (elastic modulus in the GPa range) and brittle (fracture strain <5%) electronic device materials with compliant elastomeric substrates.

- compatibility of stretchable substrates with standard microfabrication technologies, especially the process temperature.

Soft substrate engineered with the strain relief method (presented in chapter2) enables the mechanical integration of stiff materials onto stretchable substrate [3–5].
The next challenge is to direct growth and patterning of the device materials. Device fabrication on such engineered substrate is limited by the high temperature process and solubility in various solvents. Therefore I aimed at manufacturing active devices using low temperature, vapor phase and dry processes.

Thin-film transistors (TFTs) are the basic element for electronic circuits, such as inverters or logic gates. Low temperature TFTs on flexible and stretchable substrates are enabled by a-Si:H or organics semiconductor films but suffer from low mobility and require high driving voltage [3, 6–8]. More recently, transparent oxide semiconductors such as In-Ga-Zn-O (IGZO), have attracted great attention because of their high mobility, large area uniformity and low-temperature process [9–11].

Here, direct integration of a-IGZO TFTs onto a planar but mechanically engineered heterogeneous elastic substrate is presented. Evaluation of the electro-mechanical performance of the soft pixellated system was also performed. The devices were patterned on the non-stretchable regions of the elastomeric substrate, and interconnected with stretchable metallization spanning across the rigid platforms.

This section reviews the standard structures of TFTs and their main mode of operation. Then I focus on the technologies available for low temperatures (<150°C) device materials. Next I report on electro-mechanical performance of metal oxide TFTs prepared on stretchable substrate.

3.1.1 Thin film transistor

TFTs are three terminal field-effect devices in which the active channel layer, gate insulator, and metal contacts are deposited as thin-film layers. The working principle relies on the modulation of the current flowing in a semiconductor placed between two electrode, source and drain. A dielectric layer is inserted between the semiconductor and a transversal electrode, the gate. The current modulation is achieved by the capacitive injection of carriers close to the dielectric/semiconductor interface, known as field effect [12, 13].
TFTs have been in development since their invention in 1930 [14] while the use of transparent conducting oxide (TCO)-like materials for a channel has been used for the last five decade, since 1964 [15].
The following subsections focus on TFT structures and operations.

Device structure

As described above the TFTs contain three basic components: a gate insulator, an active channel layer, and metal contacts. The order in which these components are deposited can result in four different structures, as shown in figure 3.2; staggered top-gate, co-planar top-gate, staggered bottom-gate, and co-planar bottom- gate. Classification of each structure is determined by the location of the gate contact and the position of the source/drain contacts relative to the gate contact. Staggered structures are so named because the source/drain contacts are placed on the opposite side of the channel-insulator interface than the gate contact. Co-planar structures are so named because the source/drain and gate contacts are

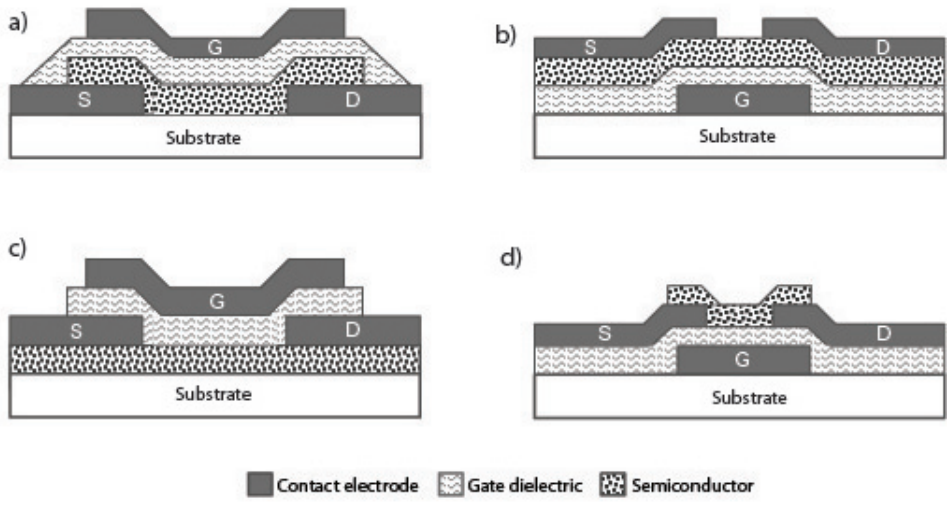


Figure 3.1: Four thin-film transistor structures: a) staggered top-gate, b) staggered bottom-gate, c) co-planar top-gate, d) co-planar bottom-gate.

placed on the same side of the channel-insulator interface. On the other hand, if the gate contact rests above the channel layer, it is known as the top-gate configuration. If the gate contact is positioned below the channel layer, it is known as the bottom-gate configuration.

Staggered bottom-gate structure are employed exclusively within this thesis in order to prevent eventual damage to the active layer during the dielectric deposition and patterning.

Device operation

On applying a bias voltage to the gate terminal (V_{GS}), charge carriers accumulate near the dielectric/semiconductor interface. This charge is equal in magnitude but of opposite sign to that on the gate electrode.
The ideal operation of an n-type TFT depends on the existence of electron accumulation layer at the dielectric/semiconductor interface. This is achieved by applying a positive V_{GS}, which results in accumulation of electrons corresponding to the negative band-bending of the semiconductor close to its interface with the dielectric. For applied gate voltage higher than a certain threshold voltage (V_T), $V_{GS} > V_T$, when a positive drain voltage V_{DS} is applied, current flows between the drain and the source electrodes (I_{DS}). This is regarded as the *on*-state of the TFT. Conversely, when $V_{GS} < V_T$, positive band-bending occurs near the dielectric/semiconductor interface, resulting in low I_{DS}, independently of the applied V_{DS}, which correspond to the off-state.

In the *on*-state, the semiconductor initially acts as a resistor, where I_{DS} increases linearly with the applied drain voltage. With further increase of V_{DS}, the electrons accumulation near the drain starts to decrease and eventually begins to deplete. The voltage at which

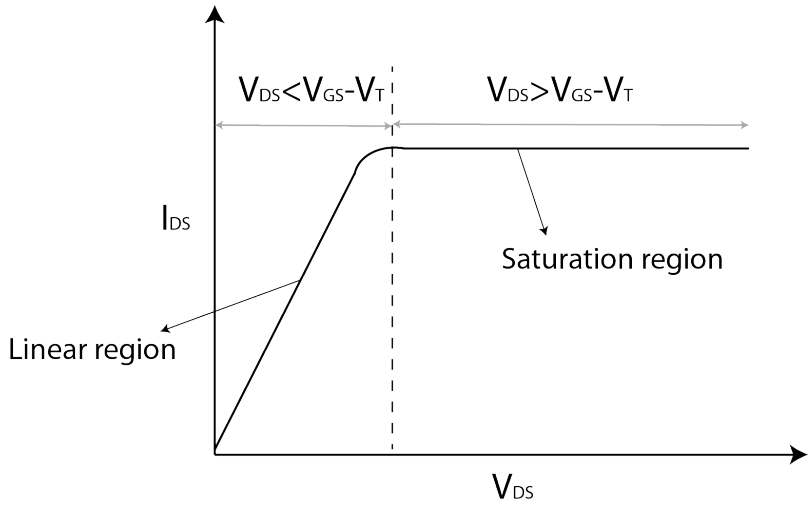


Figure 3.2: Relation of drain-source current versus voltage.

the semiconductor region near the drain is fully depleted of carriers is denoted the pinch-off voltage. V_{DS} higher than the pinch-off voltage leads to a saturation of I_{DS}, which becomes almost constant as shown in figure 3.2.
Depending on the applied V_{DS}, two different operation regimes can be observed [16], as shown in figure 3.2 :

- Linear regime, for $V_{DS} < V_{GS} - V_T$. Here the drain-source current increases linearly with the applied drain voltage. the ideal current-voltage relation in the linear region is shown below:
$$I_{DS} = C_i \, \mu_{FE} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{3.1}$$
where W is the width of the channel region (between the source/drain electrodes), L is the length of the channel, μ_{FE} is the field-effect mobility in the semiconductor, C_i is the gate capacitance per unit area. For very low V_{DS}, the quadratic term can be neglected, yielding a linear relation between the I_{DS} and V_{DS}.

- Saturation regime, for $V_{DS} > V_{GS} - V_T$. In this regime the semiconductor close to drain region becomes depleted, leading to a saturation characteristics of the drain current, being I_{DS} described by:
$$I_{DS} = C_i \, \mu_{sat} \frac{W}{2L} (V_{GS} - V_T)^2 \tag{3.2}$$
where μ_{sat} is the saturation mobility in the semiconductor. I_{DS} is ideally independent of V_{DS}.

The static metrics of TFTs can be accessed by their output (I_{DS} vs V_{DS} at a given V_{GS}) and transfer (I_{DS} vs V_{GS} at a given V_{DS}) characteristics.
From the measured transfer characteristics, the following parameters can be extracted:

- I_{on}/I_{off}: is defined as the ratio of the maximum (*on*-state) and the minimum (off-state) I_{DS}. Large current ratio are normally required for a good working transistor [17].

- Treshold voltage (V_T): is defined as the applied gate voltage at which the channel of mobile carriers begins to form close to the semiconductor/dielectric interface and thus the TFT device begins to switch from 'off' to 'on'.
An n-type TFT can be designed as enhancement or depletion mode depending upon whether V_T is positive or negative respectively [18].

- Sub-treshold swing (S): is defined as the inverse of the maximum slope of the transfer characteristic and indicates the necessary V_{GS} to increase I_{DS} by one decade:
$$S = \left(\frac{dlog(I_{DS})}{dV_{GS}} | max I_{DS} \right)^{-1} \tag{3.3}$$

The lower value of subthreshold slope indicates that TFT can switch from off to on state sharply within the small voltage change [17].

- Mobility μ: is an intrinsic property of the material. The higher the value of mobility, the ease of charge flows which results in higher drain-current. The mobility is affected by the interface trap density, growth of the semiconductor layer. [19]. Mobility can be extracted using different methodologies [20].
  The most widely used term for mobility is field-effect mobility μ_{FE}, which represents the mobility of carriers under the influence of the device structure in field-effect transistors.

3.1.2 Consideration for deposition and patterning room temperature TFTs materials

Engineered substrate with embedded strain relief method, described in chapter 2, enables to overcome the mechanical mismatch between the polymeric soft substrate and the stiff device materials. Integration of active device on engineered stretchable substrates was the consecutive step to demonstrate the strength and the reliability of the proposed method for future integrated stretchable electronics, *e.g.* electronic skin [21].

The direct fabrication of TFTs onto such substrate requires particular considerations on the manufacturing process due to the limits imposed by the polymeric nature of the substrate. PDMS has high coefficient of thermal expansion, while electronic device materials are extremely stable even at high temperature. Moreover, PDMS swells in most of the chemical compounds commonly used for wet etching [22, 23]. Swelling and thermal expansion of the substrate may cause stress in the deposited materials, which can result in wrinkled or cracked films. Therefore special attention is required in the development of all the components that will make up the device. The components include the semiconductor, dielectric, metals, and processes used to fabricate the device structures.
To enable the direct fabrication of the device on top of engineered stretchable substrates, our guiding philosophies for process development were (i) maintaining low process temperatures (∼room temperature) and (ii) patterning of materials implementing only dry steps. Therefore, these two guidelines constrained our choice of semiconductor and dielectric materials, device structure, and deposition and patterning processes during fabrication.
Thin microccracked gold film was the more logical choice for the three metal contacts, since it is already used as stretchable metallization spanning across the rigid platforms (section 2.2.3). It can be deposited by thermal evaporation using low temperature (<50°C). More considerations were made on the choice of the active layer and the gate dielectric materials, since they mainly determine the transistor performance.

In this subsection, the selection and properties of low temperature TFT materials and processing will be discussed.

Room temperature semiconductor: a-IGZO

Currently, hydrogenated amorphous silicon (a-Si:H) is widely used for low temperature inorganic semiconductor material in large area electronics and flexible displays applications. A-Si:H can be deposited uniformly over large area and at a relatively low cost. However, the carrier mobility of a-Si:H is lower by two or three orders of magnitude than that of single-crystalline Si, since its field effect mobility, μ_{FE}, is limited to 1 $cm^2V^{-1}s^{-1}$ [24–26]. The origin of the mobility degradation in a-Si:H TFT is associated with the intrinsic nature of the chemical bonding. Bonding between the directional sp^3 orbitals in amorphous silicon is highly sensitive to angular disorder. Therefore the bond angle fluctuations, due to the amorphous state, give rise to localized tail states that impede carrier transport and degrade mobility.

Over recent years, transparent oxide semiconductors (TOS) have recently attracted much attention as a potential alternative to a-Si:H in TFT applications. TOS are composed of post-transition metal oxides exhibiting n-type carriers [27]. TOS that are attracting the most interest can be broadly divided two categories; polycrystalline oxide semiconductor (POS) such as ZnO [28], and amorphous oxide semiconductors (AOS) including InZnO and InGaZnO [29, 30]. While polycrystalline oxides have limitations for uniformity which affects the grain boundaries that can deteriorate the reproducibility [31], amorphous materials result in uniform layers. Compared to amorphous silicon, amorphous oxide semiconductors also have a better electrically stability, even though deposited at room temperature. Although the amorphous state, the carrier transport properties in AOS are not deteriorated compared with associated crystalline materials.
The most popular AOS choice to date is amorphous InGaZnO (a-IGZO), which holds great promise as a commercial replacement for a-Si:H, thanks to its higher mobility (in the order of 10 $cm^2V^{-1}s^{-1}$) and the ability to be deposited at room temperature without electrical degradation. This is because the chemical bonds are completely different from those of the covalent semiconductors (*e.g.* a-Si:H) characterized by a strong directivity. Conversely in amorphous oxide semiconductors (*e.g.* a-IGZO), electrons are conducting through metal ion's ns orbital with spherical isotropic shape (n is the principal quantum number). Hence, the interaction between two s states only depends on the metal-metal distance and not bond angle. Direct overlap among the neighbouring metal ns orbitals is possible if the radii of these orbitals is made larger than the inter-cations distance, which can be achieved for $n > 4$ [31]. The magnitude of this overlap is insensitive to distorted metal-oxygen-metal chemical bonds that intrinsically exist in amorphous materials [9, 32, 33]. Takagi, et al. found the electronic structure and carrier transport in amorphous indium gallium zinc oxide to be very similar to that in crystalline IGZO [34].

The research on amorphous IGZO is being considered by many groups since its first TFT reported in 2004. [9, 31, 35–37]. Recently, Samsung and LG electronics demonstrated a 55"FHD AMOLED display in 2013 CES conference, flexible displays, and transparent

displays using amorphous IGZO TFTs
Different deposition method have been reported to prepare IGZO-based thin films, including pulsed laser deposition (PLD) [38], magnetron sputtering [39], chemical vapor deposition (CVD) [40],sol-gel [41] or photochemical activation induced by deep-ultraviolet (DUV) [38]. One method in particular, RF sputtering, is widely used to prepare thin metal oxide FETs. One advantage of sputtering is the ability to deposit films at low or room temperatures, which is a fundamental requirement for the implemented stretchable substrate, good adhesion and uniform step coverage. Deposition conditions affect the material properties, like stoichiometry and microstructure, of the sputtered metal oxide, thus influencing its electrical performance [42].
Besides doping, the oxygen vacancies derived from stoichiometry deviations in the deposited films are the main contributors for electrical conduction in amorphous metal oxides. The sensitivity of the film properties to oxygen vacancy concentration offers a wide range of tunability. The variation of O_2 percentage during sputtering is therefore an effective ways to control the electrical properties of oxide semiconductors [11, 43]. The main trend is for resistivity, ρ (Ω/cm) to increase with P_{O_2} due to the reduction of oxygen vacancies. Beyond the oxygen content and deposition conditions, post-annealing is another possible method for improving semiconductor performance. Annealing has proved to be an important postdeposition treatment to enhance the electrical properties. Increasing the annealing temperature (up to 600°C), the carrier concentration became higher, due to the thermally induced oxygen vacancies and this contributes to increase the μ_{SAT} and on-off current ratio, but it also induce a negative shift of theV_T [44].

Because it retains high carrier mobility in amorphous state and electrical stability, RF magnetron sputtered thin film a-IGZO was an attractive choice for a room temperature-deposited FET channel layer in this thesis.

Room temperature dielectric: Parylene

The selection of an appropriate gate dielectric material is critical for the electrical performances of the TFTs, since the carrier transport is heavily dependent on the semiconductor-dielectric interface. By far most of the literature has reported metal oxide TFTs based on inorganic dielectrics, especially oxide dielectric with high dielectric constant (k) such as aluminum oxide Al_2O_3 [12]. Although high-k dielectrics enable to reduce the operating voltage and increase the on-current, their deposition is typically carried out at 150-300°C by atomic layer deposition (ALD) or sputtering [45–48]. The quality of these dielectrics degrades with decreasing deposition temperature, limiting the minimum achievable process temperature.
In contrast to many inorganic dielectrics, organic dielectrics can be deposited at low- or even room-temperature by solution processing, spin-coating, or chemical vapor deposition. While the compatibility of organic dielectrics with oxide semiconductors might be cause for

concern, a few research groups have shown that they can be successfully integrated in hybrid organic-inorganic FETs [49–53]. The disadvantage of the implemented solution-processed or spin-coated dielectrics is they require high cross-linking or annealing temperature (>150°) and wet patterning steps.
Parylene can be deposited from vapour phase at room temperature without the use of solvents or catalyst, which makes it attractive for direct fabrication onto PDMS substrate. Nomura, et al. have implemented $1\mu m$ thick parylene layer as gate dielectric for a-IGZO TFT fabricated on flexible polyethylene terephthalate (PET) substrates [54]. The transistors showed a large I_{on}/I_{off} ratio $> 10^7$ and a saturation mobility of 3.2 $cm^2V^{-1}s^{-1}$.

Parylene, or poly(para-xylylene), is one of the most well-known chemical vapor deposited (CVD) film polymer films [55]. It has been studied since 1947 after Szwarc [56], who first observed the formation of poly-para-xylylene as a product of the pyrolysis of p-xylene. Parylenes were not commercialized until 1965 following the development of a CVD polymerization process by Gorham [57]. Many variants exist with varying substitutions on the benzene ring [58]. These simple chemical changes result in differences in chemical and physical properties as well as deposition kinetics. For this work, parylene-C was chosen as the dielectric material and all references hereafter to "parylene" refer to parylene-C.
Among different advantages, excellent mechanical properties, barrier properties for water, stability toward a wide range of organic and inorganic materials, the ability to form conformal coating and high resistivity [59, 60], thin parylene layers show superior electrical insulation characteristics for the gate dielectric of organic field effect transistors [61].

Parylene vapour deposition process consist of three steps.

- Parylene precursor, in the form of a dimer di-(para-xylylene, is loaded into the vapor-

Table 3.1: *Parylene-C properties [62].*

Property	Unit	Value
Dielectric constant (1KHz)		3.10
Density	g/cm^3	1.289
Young's modulus	GPa	2.8
Yield strength	MPa	55.2
Water Absorption	% after 24h	<0.1
Thermal conductivity		0.084
Melting point	°C	290

ization chamber where it is heated (90-180 °C) until the material sublimes and flow through the pyrolysis chamber which is at 680°C.

- In the pyrolysis chamber, the gaseous dimer decomposes to form a gaseous monomer (para-xylylene).

- The gas then flows into the room temperature deposition chamber containing the substrate to be coated. Upon encountering the substrate, the gas converts into a solid polymer state poly(para-xylylene), which takes the form of a completely conformal transparent polymer film

The entire process takes place in low vacuum (∼0.1 Torr) and the resulting film is smooth and uniform.

Parylene-C conformal coating is a very good candidate as gate dielectric for our process due to its excellent electric bulk properties and the ability to polymerize in gas phase at room temperature.

Room temperature pattering method: shadow mask

Given the importance of the semiconductor-dielectric interface for charge transport in TFTs, the quality of the interface depends not only on intrinsic materials properties but also on device structure and fabrication methods.
One possible fabrication methods for vacuum-deposited semiconductor devices is shadow mask patterning. Shadow mask is a resistless, solvent-free patterning method and it does not involve any heat or chemical treatment of the substrates. Because no solvents or etchants are required, this technique allows for in-situ patterning of the material thin films solely by a micromachined template, the shadow mask. Moreover thanks to the sticky nature of the PDMS engineered substrate, no adhesion tapes are needed to keep the shadow mask in place during different depositions. Yet there are disadvantages to relying on shadow mask patterning, since this method limits feature size and alignment accuracy.

In this thesis, polyimide shadow masks, with smallest feature of 100 μm, have been implemented to pattern the different layers of the TFT stack. The masks were first positioned on top of the substrate, after the alignment, by applying a slight pressure. Then, after deposition, they were easily removed by gently peeling them off with the help of a tweezer. In order to prevent damage to the active layer from dielectric deposition and patterning, TFTs with bottom-gate configuration was selected. A single shadow mask was used to pattern dielectric and semiconductor ,to avoid eventual misalignment. Therefore the TFT stack was built by implementing only three (gate, dielectric and semiconductor, source and drain) PI shadow masks and four different depositions.

3.1.3 Stretchable metal oxide TFTs

Recently, plenty of research has been carried out for the fabrication of a-IGZO based TFTs in flexible electronic applications [29, 63–66], using different flexible polymers or paper as substrate. However, only few groups have explored oxide semiconductor-based TFTs with, the more challenging, stretchable substrates. All the proposed strategies are based on two-step process: the inorganic TFTs are first fabricated on conventional, rigid substrates, to assure high-temperature fabrication process required for good electrical performance, and afterwards transferred onto non-conventional, stretchable substrates.

Park et al. proposed a method to fabricate stretchable metal oxide TFT using a wavy structural configuration [67]. ZnO thin film transistor, with SiO_2 gate dielectric layer, are first fabricated onto carrier substrate using high-temperature fabrication process, then transfer-printed onto pre-stretched (5%) elastomeric membrane. Relaxing the pre-strain led to compressive strain that forms wavy configurations in thin bridges and device regions. The TFTs showed stable electrical performance under an applied strain of up to 5% with a threshold voltage (V_T), field effect mobility (μ_{FET}) and I_{on}/I_{off} ratio of respectively 9 V, 1.15 $cm^2V^{-1}s^{-1}$ and 10^5 [67].
Three years later Sharma et al., improved the previous approach introducing a load-controlled roll method to transfer high electrical performance IGZO TFT arrays on a stretchable substrate [68]. The inorganic devices were fabricated on a conventional Si substrate, then integrated on a pre-stretched rubber substrate using the roll transfer system. The proposed load-controlled method allows for a fully automated and scalable transfer of the IGZO TFTs from a rigid substrate to a non-conventional elastomeric substrate without affecting the electrical performance. The IGZO TFTs could be very well operated in the low-voltage region ($\pm$ 5 V) after the transfer process, showing a V_T of 1.26 V, a μ_{FET} of 12.83 $cm^2V^{-1}s^{-1}$ and a I_{on}/I_{off} ratio of 1.8×10^7. The electrical parameters slightly change when the system is stretched up to 5%.
Münzenrieder, et al. proposed two approaches to develop metal oxide based electronic devices reversibly stretchable to strain values >200% [69]. Here, a-IGZO TFTs, showing V_T of 0.4 V and μ_{FET} of 11.3 $cm^2V^{-1}s^{-1}$, were first fabricated on a rigid substrate and afterwards transferred on both a pres-stretched elastomeric polymer and locally reinforced stretchable substrates. In the first case the stretchability of the system is enabled by the wavy configuration created after releasing the pre-srain, as in the method described above. In the second case the electronic devices are transferred onto mechanically graded patches, embedded in the substrates, exhibiting a gradual and discrete transition of the elastic modulus from 40 to 5150 MPa [70]. Both techniques result in inorganic, metal oxide based devices that can be stretched by more than 200%.

All the presented strategies, however, require complex wavy structure, multi-step and multi-carrier processing.
Graz, et al. demonstrated that stretchable organic thin-film transistors can be fabricated di-

rectly onto the engineered elastomeric substrate [3]. Pentacene thin-film transistors sustained applied strain up to 13% without electrical degradation and mechanical fracture. Here, the direct integration of metal oxide thin-film transistor onto the engineered substrate with strain relief method was explored [4] Room temperature a-IGZO TFTs were patterned, through only planar and standard processing, directly on the non-deformable regions of the engineered substrate, and interconnected with stretchable metallization running across the mechanically patterned elastomer. Their electrical performance was reliable and remains stable when the substrate is uni-axially stretched by 20% strain.
.

3.2 Materials and methods

3.2.1 Fabrication Process

The process flow starts with the preparation of the engineered substrate then continues with the patterning of the interconnected bottom gate IGZO TFTs (Fig.3.3). The engineered substrate is prepared by embedding stiff SU8 platforms into an elastomeric silicone matrix. The strain distribution on the top surface depends on the geometry of these platforms, as described in chapter 2. In this work, the thickness of the SU8 platforms (h) was half that of the PDMS (t); this ensures a smooth stiff-to-soft transition with minimal strain peak. The inter-platform distance (S) was four times their side (D) to minimize the far field strain, i.e. the strain between the platforms. Rounded SU8 squares of 50 μm thickness, 1.5 mm side and 6 mm spacing were patterned in a square matrix by UV lithography on a carrier Si wafer, covered with Ti/Al 5/50 nm thick releasing layer. After development and curing of the SU8 film, silicone (Sylgard 184, 10:1 polymer:crosslinker w:w ratio, Dow Corning) was spin-coated and cured at 150 °C for 24 h to form a 100 μm thick membrane of silicone rubber.
Next, IGZO TFTs were fabricated directly on top of the engineered stretchable substrate . Each TFT stack was hosted above an SU8 platform and its three electrodes are interconnected with stretchable thin-gold film conductors to three contact pads, also patterned above the rigid platforms. This design enabled stable probing contacts despite the applied stretch.
The TFT process begun with the evaporation of 5/30 nm thick Cr/Au film, structured into bottom-gate contacts (Fig.3.3 (c)). To electrically insulate the gate, different solutions were tested, where CVD parylene was standing alone or combined with thin sputtered Al layer oxidized in O_2 plasma, were explored, as described in the following subsection (Fig.3.3 (d)). The IGZO active layer with a thickness of 30 nm was next deposited using an RF magnetron sputter from a ceramic IGZO target with a composition of In:Ga:Zn=1:1:1 mol. (Fig.3.3 (e)). To complete the TFT stack, a 5/30 nm thick Cr/Au film was thermal evaporated for the source and drain contacts (Fig.3.3 (f)). Each thin film was patterned at room temperature using polyimide shadow masks aligned by eye with a shadow mask aligner. The stretchable systems were manufactured using polymer spin-coating, photolithography and thin-film processing using CMi facilities.
After the TFT stack was completed, annealing in air at 120°C for 90 minutes was per-

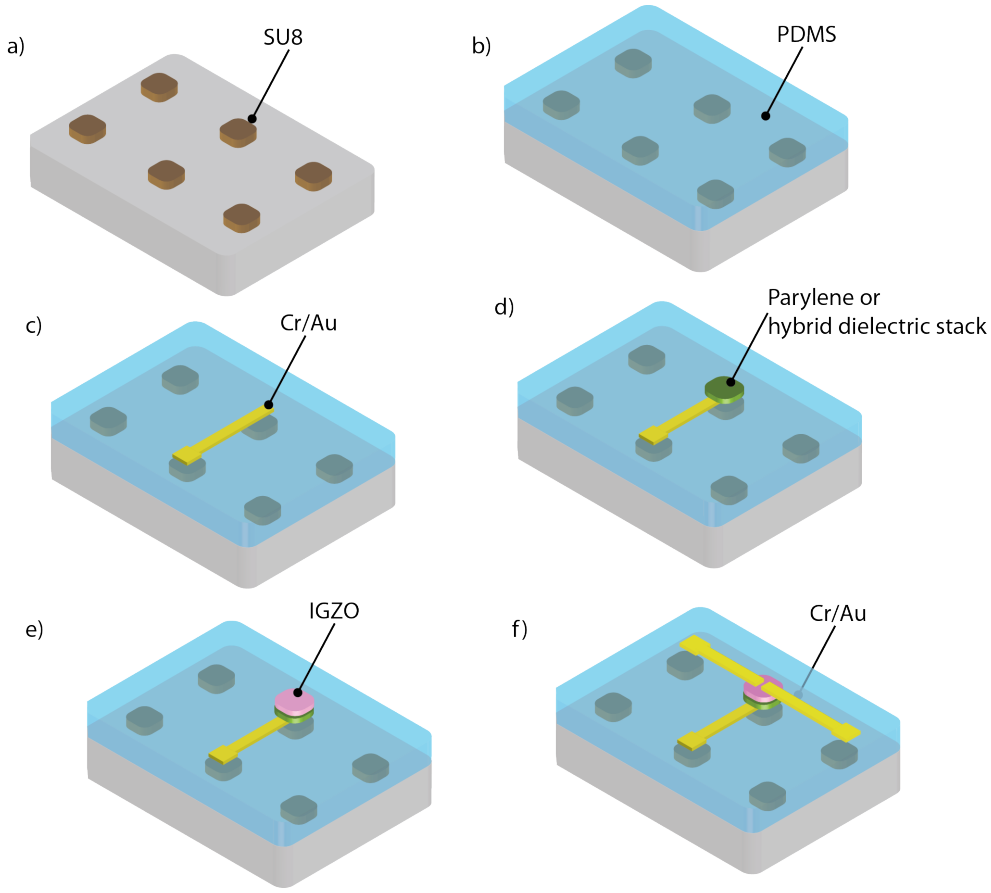


Figure 3.3: Schematic illustration of a stretchable a-IGZO TFT. a) The fabrication process started SU8 platform patterned above Si carrie wafer. b) PDMS was spincoated on top to obtain a 100μm thin layer. c) Cr/Au gate contact pads were thermally evaporated. d) CVD Parylene layer or hybrid dielectric stack were deposited in correspondence of the embedded SU8 platforms e) a-IGZO channel layer was magnetron sputtered above the gate dielectric f) Cr/Au electrodes as S/D contacts were deposited to conclude the TFT stack.

formed. Then, rectangular sample were cut on the elastomeric substrate still attached to the rigid wafer and released together with the TFTs after anodic dissolution of the metal releasing layer. The TFT channels width W and length were respectively 750 μm and 100 μm.

3.2.2 Dielectric structure

In order to improve the electrical performances of the a-IGZO TFTs four different dielectric structure were tested as shown in figure 3.4.

In structure (a) the dielectric was composed by a single 200 nm thick layer of Parylene, while the (b), (c) and (d) presented a hybrid dielectric stack where the 200 μm CVD Parylene

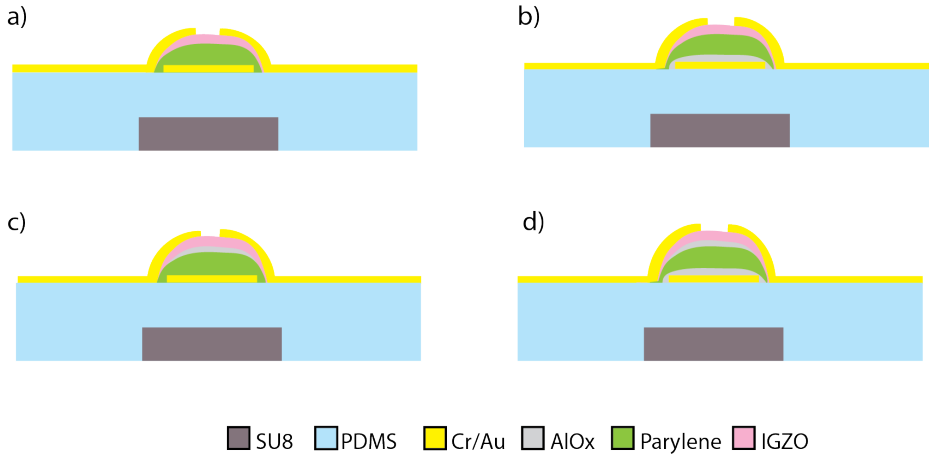


Figure 3.4: Schematic cross section of the four gate dielectric structure. a) 200 nm Parylene b) 3 repeated step of 2 nm aluminum oxidized in O_2 plasma coated with 200 nm Parylene c) 200 nm Parylene covered with 2 nm Al_xO_y oxidized in O_2 plasma d) 200 nm Parylene sandwiched between 3 repeted steps and 1 step of 2 nm aluminum oxidized in O_2 plasma, respectively on the bottom and on the top.

is stacked together with thin aluminum oxide. In structures (b) Aluminum oxide (Al_xO_y) (2 nm of sputtered Al oxidized for 10 min in O_2 plasma repeated for 3 times) was deposited before the Parylene layer. Structure (c) Al_xO_y (2 nm of sputtered Al oxidized for 10 min in O_2 plasma) was sputtered after the Parylene layer. And structure (d) where the Parylene layer is sandwiched between the two aluminum oxide layers. For each structure transfer characteristic was measured before and after the annealing step.

3.2.3 Characterization of substrate mechanics

To mechanically characterize the substrate, strain distribution was monitored on the top surface of released samples using an extensometer equipped with a Digital Image Correlation (DIC) system (LIMESS Messtechnik und Software GmbH, Istra 4D v4.3.0 software) as described in section 2.2.2

Rectangular PDMS samples with embedded 3x3 square matrix of SU8 rounded squares platforms, with diameter D of 1.5 mm side and spacing S of 6 mm, were prepared. Mechanical characterization of the substrate without and with the TFT on top were performed. Figure 3.5 (a) and (b) show the schematic cross sections of the two set of analyzed samples. The regions highlighted by the red rectangle indicate the top surface areas where the strain distribution was characterized.
After releasing from the rigid carrier, the samples were covered with black and white powder and clamped to the jaws of an automated custom built uni-axial stretcher. Tensile stress up to 20% of deformation was applied along the channel length direction. Speckle images (Fig

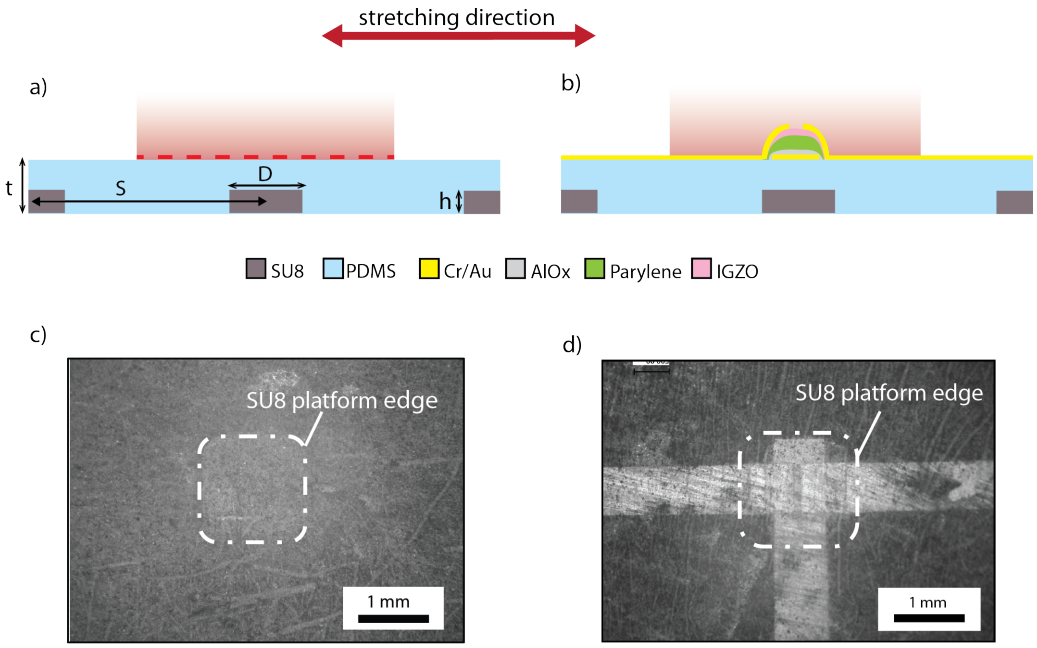


Figure 3.5: Top surface strain characterization of the two sets of samples: engineered substrate without the TFT on the left, and engineered substrate with the TFT stack on the right. A) and b) represent the schematic cross section where D =1.5 mm, S = 6 mm, h = 50 μm,t = 100 μm. The sections highlighted by the red rectangles point out the top surface areas where the strain distribution was monitored. C) and d) are optical speckle images of the correspondent top surface observed area for the two sample with 50x magnification. The white dotted line underline the edge of the embedded platform.

3.5 (c) and (d) taken at different applied strain were analyzed with the above mentioned the DIC system to produce strain distributions across the top surface of the stretched samples.

3.2.4 TFT Electrical characterization

TFTs were electrically characterized under ambient condition during uni-axial stretching using an Agilent technologies B1500 parameter analyzer. The characterizations of the TFTs-stretchable substrate system attached to the carrier wafer were performed by contacting the source, drain and gate with three flexible probe tungsten tips. After releasing, the stretchable electronic system was not flat anymore and it could have been damaged during the positioning of the probe tips above the TFT's electrodes. Therefore, to assure a good electrical contact between the tips and the freestanding soft system, a drop of liquid metal eutectic indium/gallium was poured above each TFT's electrical contacts and the tips were inserted inside the metal drops without touching the substrate.

The transistor transfer characteristics ($I_{DS}vsV_{GS}$) provide a means to quantitatively mea-

sure the performance of the TFT device. Transfer characteristics were taken by applying a constant voltage V_{DS} (in a range from 0 to 5 V)at the drain electrode. In parallel, a sweeping voltage V_{GS} (in a range from -10 to 10 V) is applied at the gate electrode and the drain current I_{DS} is monitored.
Transfer characteristics, with V_{DS}=5 V, were used to extract TFT typical performance parameters such as the apparent mobility μ, the I_{on}/I_{off} ratio, the extrapolated threshold voltages V_T and the inverse sub threshold swing $S.S$.

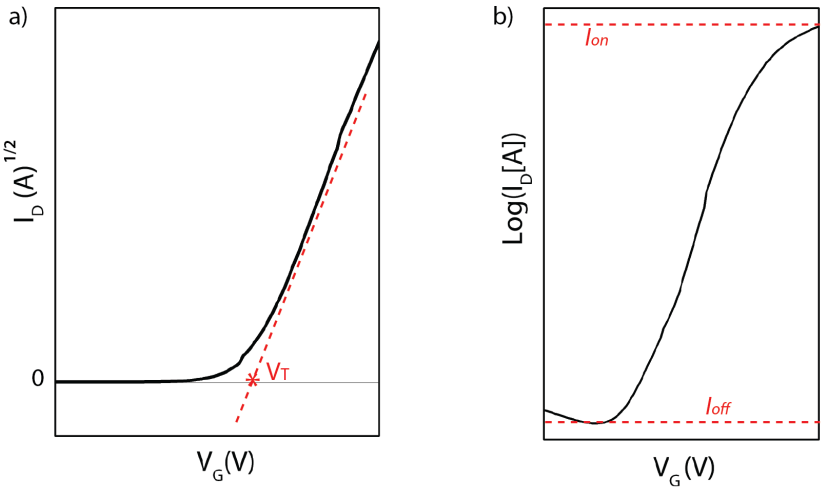


Figure 3.6: TFT performance parameters extrapolation: a) threshold voltage determination by the saturation extrapolation technique, b) I_{on}/I_{off} ratio and substhreshold slope determination.

The saturation extrapolation method was used to measure the threshold voltage, since $V_{DS} > V_{GS} - V_T$. In this method V_T is determined by extrapolating a line tangential to the $\sqrt{I_{DS}}$ vs V_{GS} characteristics of n-channel a-IGZO TFTs at the point of maximum slope. The intercept of this line with the V_{GS} axis yields V_T. Figure 3.6 (a) shows an example of applying this method to determinate V_T.
Saturation mobility μ_{sat}, given in cm^{2}V^{-1}s^{-1} , was calculated as

$$\mu_{sat} = \left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2 \frac{2L}{WC_i} \tag{3.4}$$

where $\frac{d\sqrt{I_{DS}}}{dV_{GS}}$ is the slope of a plot represented in figure 3.6 (a).
C_i was calculated as the average capacitance per unit area of ten, 3 x 3 mm square, capacitors measured at 100 KHz. The capacitors, composed by the dielectric hybrid stack sandwiched between 2 gold electrodes, were fabricated on top of a glass wafer.

The I_{on}/I_{off} ratio was extracted by plotting the drain current I_{DS} of the transfer

characteristics in logarithmic scale. The difference between the TFT's maximum and minimum current is expressed as I_{on}/I_{off} as shown in figure 3.6 (b) . Here, $\log(I_{DS})$ exhibits approximately linear behavior in the $V_{GS} > V_T$ region. The inverse of its slope is the subthreshold swing $S.S$, given in units mV/dec.

3.2.5 TFT Electro-mechanical characterization

Finally, electro-mechanical characterization of an a-IGZO TFT fabricated on top of the engineered substrate was accomplished.

The TFT gate dielectric was composed by a hybrid stack: Al_xO_y thin layer (2 nm of sputtered Al oxidized for 10 min in O_2 plasma repeated for 3 times) coated with 200 nm thick CVD Parylene. Once the device fabrication was completed, the stretchable system was annealed at 120°C for 90 minutes and then, released from the rigid carrier wafer to achieve a freestanding stretchable TFT system.

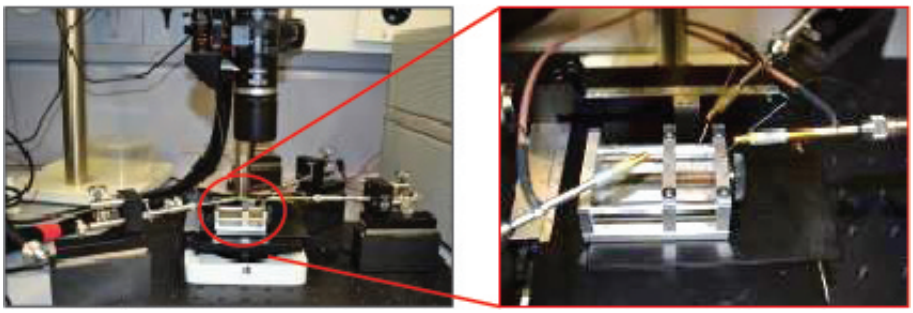


Figure 3.7: TFT electromechanical characterization setup. The stretchable TFT is mounted on a manual stretcher at located at the center of the probe station, to perform electrical characterization of the device while applying different strain.

Transfer characteristics of the device were recorded before and after the annealing as well as after the releasing. Then the sample was mounted on a manual stretched placed at the center of the probe station and stretched up to 20% of strain, as shown in figure 3.7 . Transfer characteristics were measured at 0%, 10%, 15% and 20% of the applied strain. The respective change in the TFT parameters, V_T, μ_{sat}, I_{on}/I_{off} ratio and $S.S$, over the applied strain have been monitored.

3.3 Results and discussions

IGZO TFTs were fabricated directly on top of the engineered stretchable substrate, above the embedded rigid platforms as illustrated in figure 3.8 (a) and (b). The TFTs have bottom gate staggered structure and are manufactured using only dry and room temperature

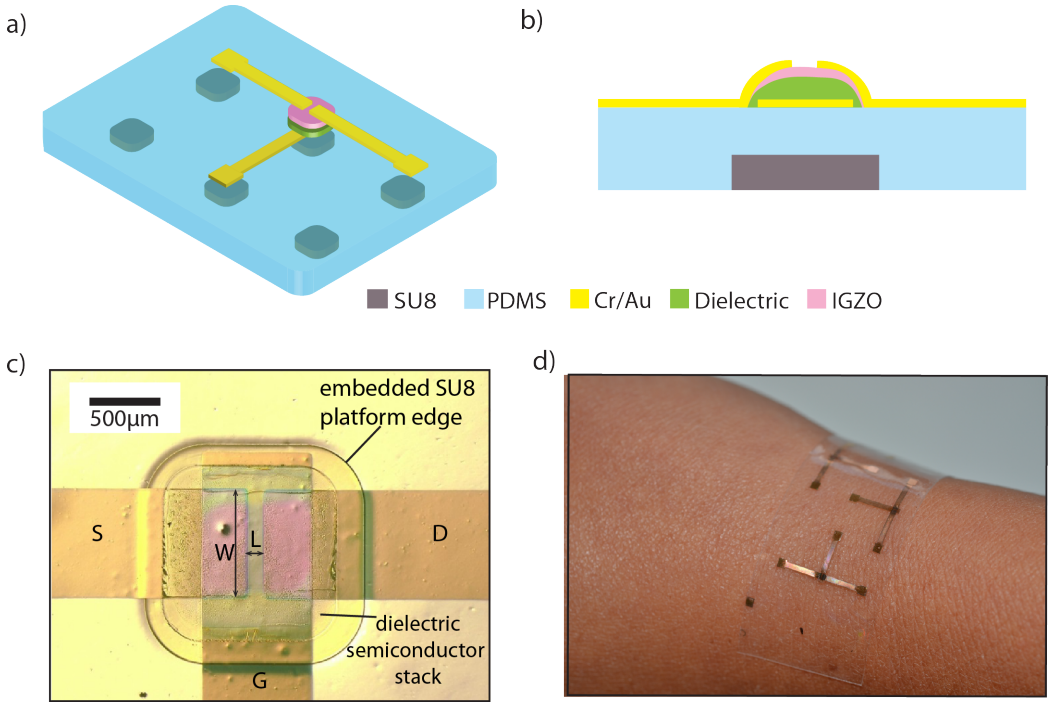


Figure 3.8: IGZO TFT fabricated on top of the engineered substrate: a) 3D schematic, b) schematic cross section, c) TFT top view optical picture and d) photograph of released the stretchable TFTs wrapping wrist's curve.

fabrication step. Figure 3.8 (c) shows the optical top view of an IGZO TFT. The edge of the rounded square embedded platform as well as the edge of the dielectric/IGZO stack are easily distinguishable. The source, drain, and gate metal contact are interconnected with the respective adjacent platforms. The active channel is 750 μm width and 100 μm long.
Figure 3.8 (d) shows a picture of a free-standing stretchable sample wrapped around human wrist, complying with its curved shape.

3.3.1 Dielectric film(s) structure

TFTs with four different dielectric film structures, based on bare Parylene or Al_xO_y/Parylene combined stack, have been fabricated on top of the engineered substrate. 20 TFTs on one wafer were prepared for each of the dielectric stack.

Figure 3.9 shows the transfer characteristics of the best working IGZO TFT per each dielectric structure.
In all cases the $I_{DS} - V_{GS}$ curve before annealing exhibits almost a static behavior, since the *on* current is in the same order than the off current. In fabricating the TFTs, IGZO was

deposited using magnetron sputtering in an only-Ar-reactive gas environment, which may cause excess of oxygen deficiency resulting in a high conductivity of the semiconductor films. This could explain the poor TFT performance.

It has been demonstrated that annealing at high temperature enables to compensate the oxygen deficiencies in IGZO films as well as on TFT devices to reduce the densities of the interface trap between the active layer and insulator [71].
In this work annealing at 120°C for 90 minutes was performed. The annealing temperature was selected to prevent eventual strain formation in the thin film stack due to the thermal expansion of the polymeric substrate. However, even if it is lower than the ones reported in literature (ranging from 200 to 600°C [71, 72]), IGZO TFTs showed improvement in transfer characteristics after thermal annealing, as shown in figure3.9. For all the four dielectric structure TFTs, the channel is more controlled by the gate voltage though the drain current is decreased by 1 or 2 orders of magnitude.
Despite these improvements, the fabricated IGZO TFTs shown poor electrical performance if compared to those reported in literature [10, 66, 73]. Given the fact the devices have organic/inorganic interface it is reasonable to expect the presence of traps at the semiconductor-dielectric interface, which degrade the TFTs performance. Therefore, future works to improve interfaces or reduce the charge trapping are required to enhance the electrical performance of the devices.

Although sputtering and CVD deposition processes, employed for the dielectric and semiconductor films deposition, are usually characterized by large area uniformity, the yield of working transistors was low. In particular, the first two proposed structure, bare Parylene and Al_xO_y/Parylene, exhibit a yield of respectively 40% and 56%. This difference could be explained by the fact that the Al_xO_y thin layer improves the adhesion of the Parylene dielectric films on the substrate. However, the last two structures show only one transistor working over 20, which are shown in figure 3.9 (c) and (d). In both of these structures, oxygen plasma was performed on aluminum coated Parylene. From the poor TFT performance, it was understood that poor coverage of aluminum on Parylene leads to etching of Parylene. It results in degraded Parylene than other stacks shown in Figure (a) and (b).
Since organic and inorganic materials are commonly regarded to form poor interface, dielectric stacks with thin oxide layer between the IGZO semiconductor and the Parylene dielectric were proposed to improve this interface (Fig. 3.9 (c) and (d)). Unfortunately the selected approach damages the Parylene layer underneath, resulting in a nearly null yield of working transistor. One possible solutions could be to invert the TFT structure, using a bottom gate staggered structure. In this case the oxidation of the Aluminum layer would be performed before the Parylene deposition and, at the same time, the Parylene film could act also as passivation layer for the active channel. However, in this solution, the effect of the O_2 plasma on the IGZO electrical performance need to be studied.

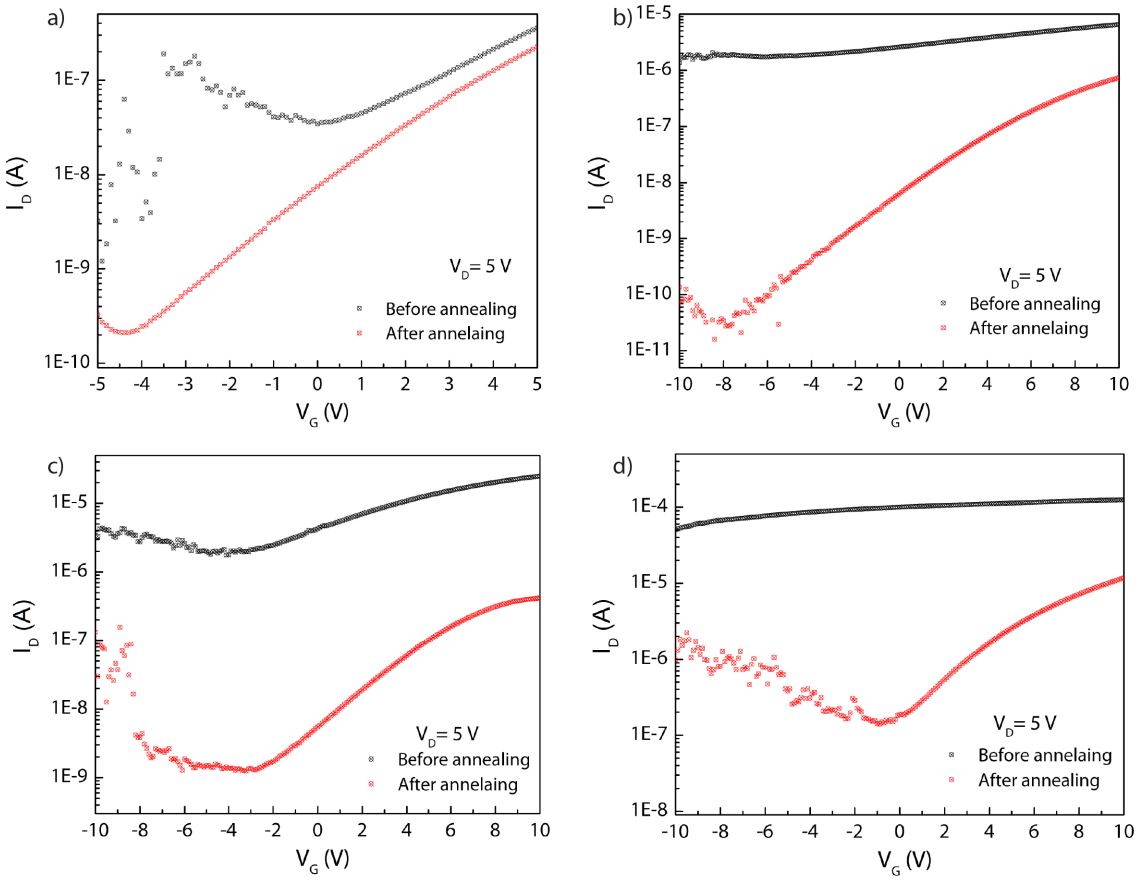


Figure 3.9: Transfer characteristic of IGZO TFTs before and after annealing for 90 min at 120°.C, taken at V_D=5 V with different dielectric films structure: a) 200 nm Parylene, b) Al_xO_y/Parylene, c) Parylene/Al_xO_y d) Al_xO_y/Parylene/Al_xO_y.

Moreover to understand how the soft nature of the substrate influence the yield and quality of the deposited device materials, comparison of the electrical characterization of equivalents TFT structures fabricated onto glass or flexible (*e.g.* Polyimide) substrates is strongly suggested. However, implementing shadow mask patterning technique with non sticky substrates requires particular attentions to keep shadow masks in place with uniform adhesion to the substrate during different depositions. Lift off patterning or could be considered for this purpose.

From these initial results, I decided to proceed with the dielectric films structure that lead the highest working TFT yield. Therefore IGZO TFTs with Al_xO_y thin layer coated with 200 nm Parylene dielectric stack were fabricated for more detailed electro-mechanical characterization.

3.3.2 Substrate mechanical characterization

The surface strain across the engineered substrate, with and without IGZO TFT on top, was monitored during tensile loading to 20% strain. Principal strain distribution was mapped above the embedded SU8 platforms.

Using the analysis and design guidelines described in Chapter 2 a SU8 platform matrix S/D=4 was selected, (where S is the spacing in between two adjacent platform, and D is the diameter of the platform). This value was chosen to minimize the strain along the gold interconnects spanning across the rigid platforms. Moreover rounded square platform were used to maximize the area available for the active TFT channel.

Figure 3.10 and 3.11 provide experimental results on the principal strain distribution when macroscopic strain was applied on engineered substrate respectively without and with the TFT stack on top. In both cases, the strain immediately above the SU8 platform, remains close to 0%; in-between platforms, the strain increases to plateau nearly at the applied strain. No cracks arises on the TFT stack after mechanical stretching. The area at the edges of the platform shows the highest strain (around 25%). This value is lower than strain concentration measured with the same geometrical platforms distribution but with circular shape. With the rounded square shape, the strain is concentrated on the rounded corners of the platform, as shown in figure 3.10 (a), thus minimizing the strain on the metal interconnects at the hard-to-soft interface (Fig. 3.11).

These experimental results validate the engineered stretchable substrate design and its efficiency to protect materials from irreversible cracking upon mechanical deformation.

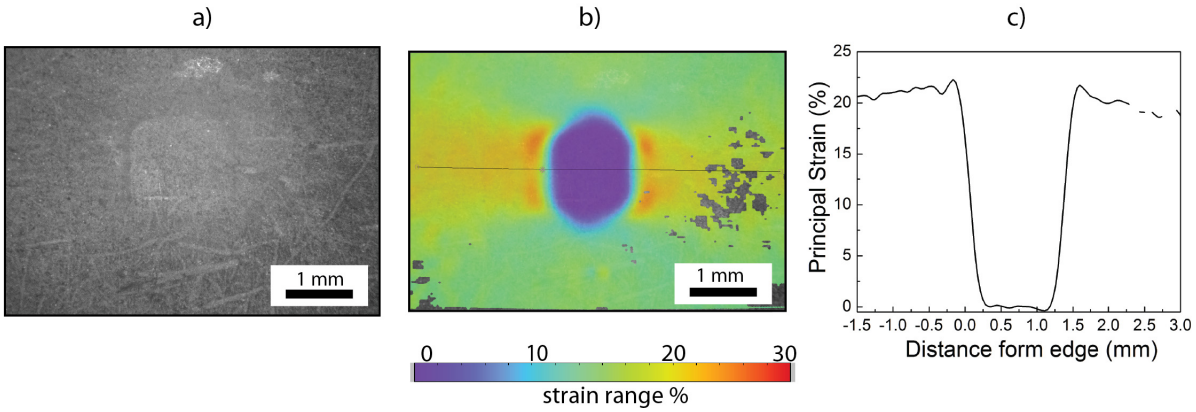


Figure 3.10: Top surface strain distribution on the engineered substrate without the TFT stack when 20% of strain is applied: a) top view optical speckle image, b) strain map and c) extrapolated strain profile taken along the x-axis passing fro the center of the platform.

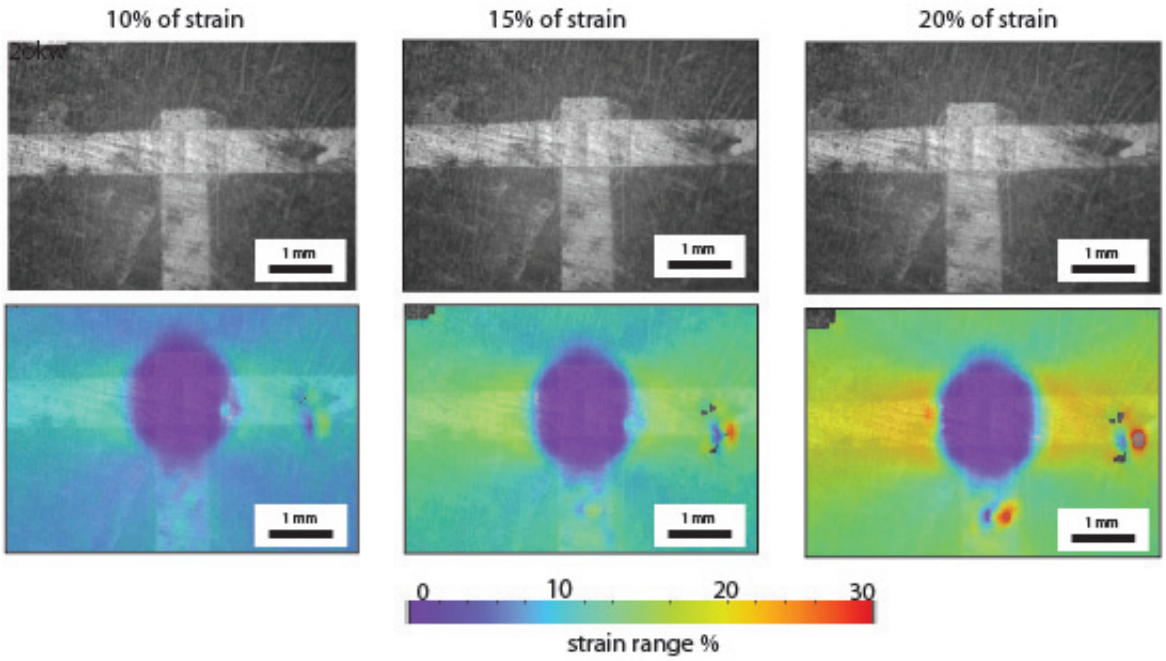


Figure 3.11: Top surface strain distribution on the engineered substrate with the TFT stack when macroscopic strain is applied. On the top, the top view, optical images and and on the bottom the colored strain maps respectively at 10%, 15% and 20% of applied strain.

3.3.3 TFT electro-mechanical characterization

Stretchable IGZO TFTs with Al_xO_y/Parylene dielectric stack were prepared to perform electro-mechanical characterization of the soft system.

Each TFT is hosted above the SU8 platform and its three electrodes were interconnected with stretchable thin-gold film conductors to three contact pads, also patterned above a rigid platform (Fig. 3.8 (a)). Although almost 50% of TFTs fabricated on the same exhibits good transfer characteristic after thermal annealing, only two of them were properly working after the releasing from the carrier wafer. Since the releasing step is performed in salted water, it is most likely that the channel layer is damaged by the absorbtion of H_2O molecules. Park et al. demonstrated that for a-IGZO thin film are very sensitive to the surface adsorption of water [74]. In particular, for IGZO film < 70 nm, the adsorbed water act as acceptorlike trap causing great deterioration of the subthreshold swing and I_{on}/I_{off} ratio.
Due to the physical proximity of the two working transistors, it was possible to perform stretch test only for one of them, whose transfer characteristics and performance parameters are presented below.

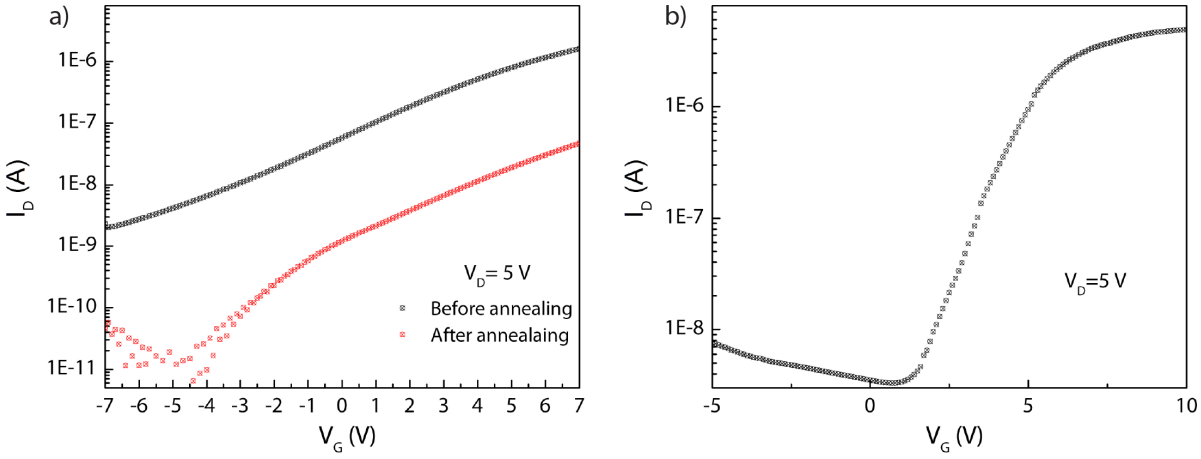


Figure 3.12: Transfer characteristic of soft a-IGZO TFT at $V_{DS} = 5$ V: a) before and after annealing at 120°C for 90 minutes, b) after releasing from the rigid wafer.

First, the dielectric properties of the Al_xO_y/Parylene film was evaluated. Capacitances prepared with Au electrodes sandwiching the hybrid film (Al_xO_y/Parylene) were probed in C(V) setting at 100 kHz. To calculate the capacitance value I supposed that the Al_xO_y layer was 9 nm thick. The resulting capacitance per unit area was C_i =1.4 nF/cm^2, this value was used for subsequent calculation of the saturation mobility μ_{sat} of the TFT.

Figure 3.12 (a) shows the transfer characteristics before and after annealing, taken when V_{DS}= 5 V. 120°C annealing results in less ohmic I_{DS}- V_{GS} curve, with μ_{sat} of 0.33 cm^{2}V^{-1}s^{-1}, a V_T of 2.2 V. The *on* and off currents decrease of two orders of magnitude with respect to the pre-annealing characteristic, as already shown in section 3.3.1. However, the transfer characteristic curve was significantly improved after releasing, as shown in figure 3.12 (b). Here, the TFT exhibits a proper tranistor-like behaviour and a *on* current of 4 μA. The extracted TFT parameters show improved electrical properties, with a μ_{sat} of 2.4 cm^{2}V^{-1}s^{-1}, a V_T of 4.1 V, I_{on}/I_{off} ratio of $\sim 10^3$ and a $S.S$ of 1.4 V/dec. The same electrical improvements were observed in the other TFT properly working after releasing.
After releasing, a drop of liquid metal was poured above the source, drain and gate electrodes in order to electrically connect the probe tips with the contact pads of the free-standing TFT. This solution enabled stable probing contacts despite the applied deformation and it probably offer a better electrical contact between the sample and probe tips system, which could explain the improvements of the TFT performance. This result suggest that an improved electrical contact between the TFT's contact electrodes and the probe tips is required for proper characterization of the active device before releasing.

Then, to assess its robustness, the freestanding IGZO TFT was mounted in a customized

uni-axial stretcher for electro-mechanical characterization when stretched up to 20% strain (stretching direction parallel to the channel length).
The device shows no significant change in electrical properties under an applied strain of up to 20%. Figure 3.13 shows the transfer characteristics at 0%, 10%, 15% and 20% of applied strain ε_{app}. When no strain is applied ($\varepsilon_{app} = 0\%$) the TFT showed a μ_{sat} of 2.24 $cm^2V^{-1}s^{-1}$, a V_T of 4.1 V, I_{on}/I_{off} ratio of $\sim 10^3$ and a $S.S$ of 1.6 V/dec. Little deterioration of performance parameters is observed after clamping the stretchable TFT on the manual stretcher, compared to the ones measured in the freestanding condition.
The TFT response is little affected by the large mechanical deformation (ε_{app}= 20%) with μ_{sat} of 1.31 $cm^2V^{-1}s^{-1}$, and V_T of 4.5 V. The I_{on}/I_{off} ratio and the subthreshold swing showed almost no change over the applied strain. The slight difference in threshold voltage as well as the decreasing of the μ_{sat} may be an artifact from the increasing resistance of the electrode interconnects with strain. The TFT contact pads are located 5 mm away from the transistor stack. When tensile strain is applied in a direction parallel to channel length, source and drain interconnects are subjected to elongation and therefore the resistance increases. The applied V_{DS} resulting on the TFT stack as well as the recorded I_D on the source electrode decrease with the applied strain. This could explain the shifting on the bottom right of the transfer characteristics in figure 3.13. Figure 3.14 plots the saturation mobility and threshold voltage of an IGZO TFT as a function of the applied strain. Both parameters are almost stable over the range of elongation. The slight increasing of the V_T as well as the decreasing

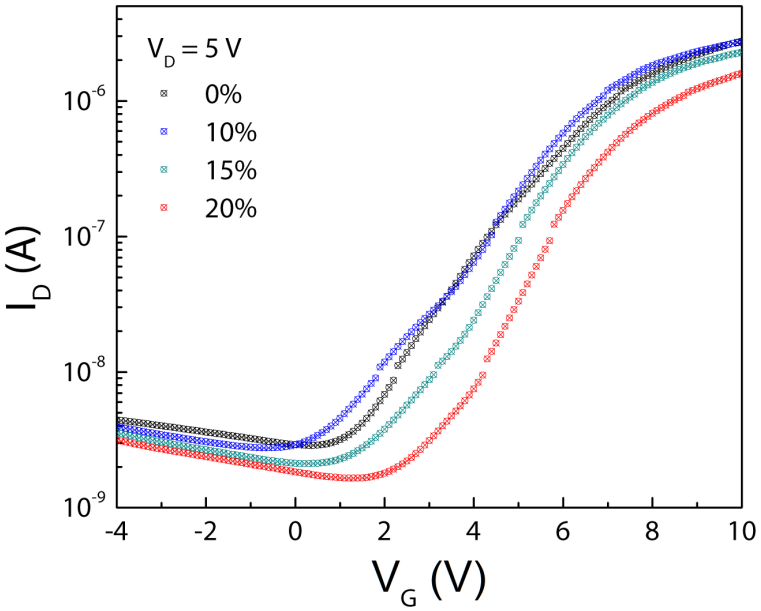


Figure 3.13: Transfer characteristics under stretching recorded at 0% , 10%, 15% and 20% of strain, when $V_{DS} = 5$ V.

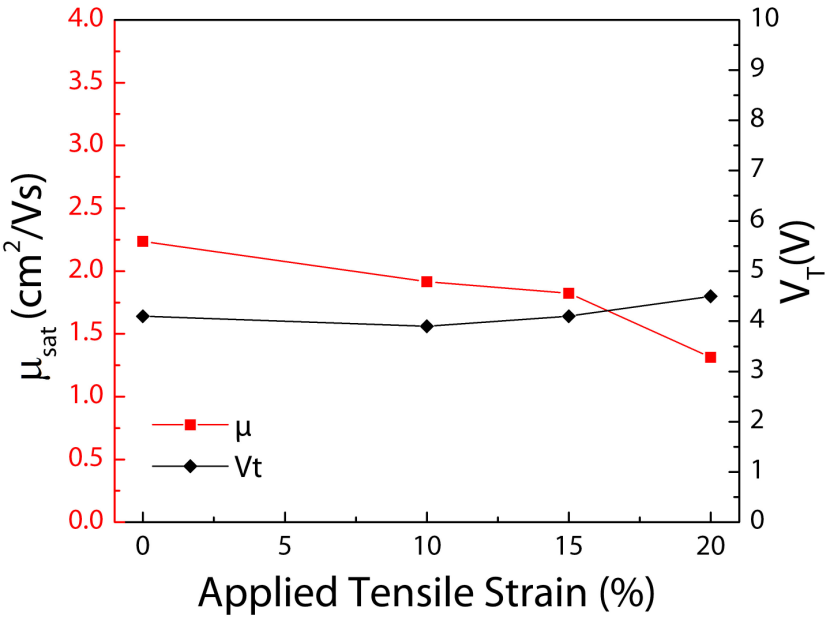


Figure 3.14: Saturation mobility, on the left, and threshold voltage, on the right, as function of the applied strain.

of the μ_{sat} with the applied strain could be caused by the elongation of the source and drain metallization as explained before.

Optical observations of the IGZO TFTs before, during and after the stretching cycles indicate no cracking occurs in the brittle thin film stack (Figure 3.15). Longitudinal extension of the source and drain Au interconnects is visible figure 3.15 b while no shape change occurs on the TFT structure.

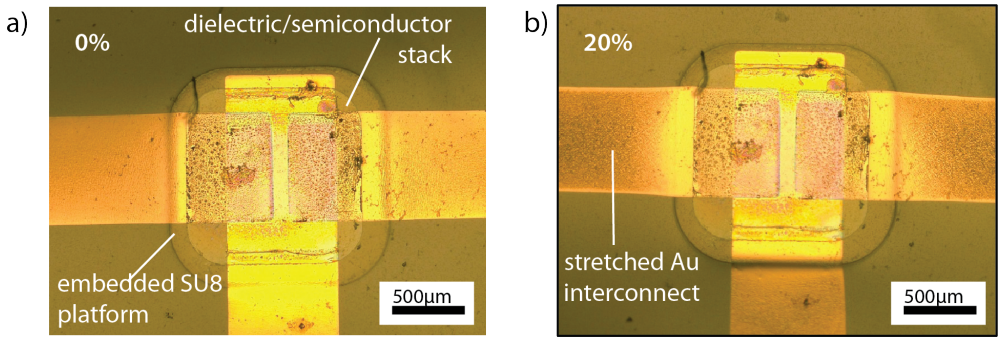


Figure 3.15: Optical picture of the free standing TFT at: (a) 0% of strain and (b) 20% of strain.

The feasibility of direct integration of metal oxide active electronics onto stretchable engineered substrate with embedded strain relief, by means of planar and standard processing was demonstrated. The proposed stretchable substrate enables the electronic devices to maintain their electrical performances even when large deformations are applied (20% of strain).

Despite these promising electro-mechanical results, the yield of fabrication of our stretchable IGZO TFTs remains low, and the electrical parameters are much smaller than those of standard IGZO thin film transistor.
The fabrication yield could be partially be improved by introducing an encapsulation layer before the releasing step, to protect the active channel layer from water absorption. Moreover the electrical characteristic of the IGZO layer is sensitive to the deposition conditions as well as to the history of the sputter target. Because the sputter system is shared by many users and different sputter targets are frequently rotated in and out of the system, the process was not sufficiently controlled. Therefore if optimization of the deposition parameters can improve the electrical performance of the IGZO active layer, a dedicated deposition system not shared with other is strongly suggested to improve the reproducible of the process.
Beside the possible improvements of the device materials directly fabricated on the engineered stretchable substrate, another solution is the employment of transfer fabrication technique. IGZO TFTs fabricated on to glass or plastic substrates having good electrical performance and stability have been largely demonstrated [35, 45, 66, 75–77]. Therefore IGZO TFTs could be first fabricated onto thin plastic substrate attached to a rigid carrier wafer. Afterwards the plastic substrate could be patterned in islands hosting the TFTs and transferred them onto the engineering stretchable substrate substrate in correspondence of the embedded SU8 platforms. Before the transferring step, elastic interconnects are fabricated on the elastomeric substrate to enable electrical contact between the TFTs islands and the stretchable substrate. The proposed method does not suffer anymore form the limitation imposed by the soft substrate. Higher temperature fabrication processes could be implemented, such as ALD deposition of high-k oxide dielectrics or high temperature annealing, which allows for high electrical performance TFTs.

3.4 Conclusions

In summary, I have demonstrated that stretchable metal oxide thin-film transistors can be fabricated directly onto elastomeric engineered substrates. The soft electronics can conform curved structures and stretch while retaining its functionality.
The engineered strain distribution of the heterogeneous substrate prevents the brittle TFT's materials from exceeding their fracture strain when a macroscopic strain is applied. At the same time planar top surface is assured, simplifying the electronic device fabrication process.

A successful direct fabrication of IGZO transistors onto the engineered substrate using

Al_xO_y/Parylene hybrid dielectric stack and stretchable gold metal electrodes was obtained. To ensure minimal or no strain in multilayer of brittle electronic materials, they were patterned above the safe area in correspondence of the embedded SU8 platforms. The fabrication process imply only standard, dry and room temperature steps, compatible with the soft polymeric substrate.
Post-annealing at 120°C for 90 minutes enables improved $I_{DS} - V_{GS}$ characteristics, where the I_{DS} is more controlled by the gate voltage.
Electro-mechanical characterization of a stretchable IGZO TFT was performed. The stretchable transistor with channel lengths and width of respectively, 100 and 750 μm, showed typical transistor-like behavior after releasing from the rigid carrier wafer, with a μ_{sat} of 2.4 $cm^2V^{-1}s^{-1}$, a V_T of 4.1 V, I_{on}/I_{off} ratio of $\sim 10^3$ and a $S.S$ of 1.4 V/dec.
The transistor could sustain large deformation by up to 20% without electrical or mechanical degradation. The electrical measurements of the device showed stable responses under the applied strain. The V_T and the μ_{sat} showed little variation due to the increasing resistance of the electrode interconnects with strain.
Although the promising electro-mechanical results, encapsulation layer and optimization of the IGZO deposition as well as the semiconductor-dielectric interface are needed to increase the fabrication yield and to improve the TFTs performance and make it comparable with that of IGZO TFTs fabricated onto glass or plastic substrate. For the same purpose, different manufacturing techniques which allows for high temperature processing, could be tested, such as substrate transfer approach.

The integration of IGZO transistors on a soft carrier matrix, which guarantees the electronic devices to maintain their electrical performance even when large deformations are applied, are of fundamental importance for future stretchable electronics application. Although the starting point for technology development is the fabrication of single field-effect transistors, these individual devices are the building blocks for integrated stretchable circuits. Combining standard active electronics materials and processing with stretchable and biocompatible substrates to produce large-area, skin-like sensory surfaces provides exciting opportunities, especially in biomedical applications and wearable electronics.

References

[1] T. Sekitani and T. Someya, "Stretchable organic integrated circuits for large-area electronic skin surfaces," *MRS Bulletin*, vol. 37, no. 03, pp. 236–245, Mar. 2012. [Online]. Available:

[2] L. Xu, S. R. Gutbrod, A. P. Bonifas, Y. Su, M. S. Sulkin, N. Lu, H.-J. Chung, K.-I. Jang, Z. Liu, M. Ying, C. Lu, R. C. Webb, J.-S. Kim, J. I. Laughner, H. Cheng, Y. Liu, A. Ameen, J.-W. Jeong, G.-T. Kim, Y. Huang, I. R. Efimov, and J. a. Rogers, "3D multifunctional integumentary membranes for spatiotemporal cardiac measurements and stimulation across the entire epicardium," *Nature Communications*, vol. 5, pp. 1–10, Feb. 2014. [Online]. Available:

[3] I. M. Graz, D. P. J. Cotton, A. Robinson, and S. P. Lacour, "Silicone substrate with in situ strain relief for stretchable thin-film transistors," *Applied Physics Letters*, vol. 98, no. 12, p. 124101, 2011. [Online]. Available:

[4] A. Romeo, Q. Liu, Z. Suo, and S. P. Lacour, "Elastomeric substrates with embedded stiff platforms for stretchable electronics," *Applied Physics Letters*, vol. 102, no. 13, p. 131904, 2013. [Online]. Available:

[5] A. Romeo, Y. Hofmeister, and S. P. Lacour, "Implementing MEMS technology for soft, (bio)electronics interfaces," vol. 9083, p. 90831F, Jun. 2014. [Online]. Available:

[6] S. P. Lacour and S. Wagner, "Thin Film Transistor Circuits Integrated onto Elastomeric Substrates for Elastically Stretchable Electronics," *Film*, vol. 00, no. c, pp. 20–23, 2005.

[7] M. H. Lee, S. T. Chang, Y. C. Wu, M. Tang, and C. Y. Lin, "Mechanical bending cycles of hydrogenated amorphous silicon layer on plastic substrate by plasma-enhanced chemical vapor deposition for use in flexible displays," *Japanese Journal of Applied Physics*, vol. 48, no. 2, 2009.

[8] R. a. Street, "Thin-Film Transistors," *Advanced Materials*, vol. 21, no. 20, pp. 2007–2022, May 2009. [Online]. Available:

[9] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors." *Nature*, vol. 432, no. 7016, pp. 488–92, Nov. 2004. [Online]. Available:

[10] J. Yeon Kwon and J. Kyeong Jeong, "Recent progress in high performance and reliable n-type transition metal oxide-based thin film transistors," *Semiconductor Science and Technology*, vol. 30, no. 2, p. 024002, Feb. 2015. [Online]. Available:

[11] P. Barquinha, L. Pereira, G. GoncÌ§alves, R. Martins, and E. Fortunato, "The Effect of Deposition Conditions and Annealing on the Performance of High-Mobility GIZO TFTs," *Electrochemical and Solid-State Letters*, vol. 11, no. 9, p. H248, 2008.

[12] P. Barquinha, R. Martins, L. Pereira, and E. Fortunato, *Transparent Oxide Electronics. From materials to devices*, Wiley, Ed., 2012.

[13] A. C. Tickle, *Thin - film transistors : a new approach to microelectronics*, I. New York: John Wiley & Sons, Ed., 1969.

[14] J. Lilienfiel, "Method and apparatus for controlling electric currents," 1930. [Online]. Available:

[15] H. A. Klasens and H. Koelmans, "A tin oxide field - effect transistor," *Solid-State Electronics*, vol. 7, no. 701, p. 2, 1964.

[16] D. Neamen, *Semiconductor Physics and Devices: Basic Principles*, M. Hill, Ed., 2003.

[17] J.-H. Lee, D. N. Liu, and S.-T. Wu, *Introduction to Flat Panel Displays*, L. John Wiley & Sons, Ed., 2008.

[18] R. L. Hoffman, B. J. Norris, and J. F. Wager, "ZnO-based transparent thin-film transistors," *Applied Physics Letters*, vol. 82, no. 5, pp. 733–735, 2003.

[19] Y.-j. Yang, *Microelectronics Devices Type of Solid Materials*, McGraw-Hill, Ed., Singapore, 1988.

[20] D. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed., I. John Wiley & Sons, Ed., 2006.

[21] S. P. Lacour, I. Graz, D. Cotton, S. Bauer, and S. Wagner, "Elastic components for prosthetic skin." *Conference proceedings : ... Annual International Conference of the IEEE Engineering in Medicine and Biology Society. IEEE Engineering in Medicine and Biology Society. Conference*, vol. 2011, pp. 8373–6, Jan. 2011. [Online]. Available:

[22] J. N. Lee, C. Park, and G. M. Whitesides, "Solvent Compatibility of Poly(dimethylsiloxane)-Based Microfluidic Devices," *Analytical Chemistry*, vol. 75, no. 23, pp. 6544–6554, 2003.

[23] F. Gubbels and D. Corning, *11 . Silicones in the Electronics Industries*, Seneffe, Belgium, 2007.

[24] S. Wagner, H. Gleskova, I.-C. Cheng, and M. Wu, "Silicon for thin-film transistors," *Thin Solid Films*, vol. 430, no. 1-2, pp. 15–19, 2003.

[25] K. C.R. and A. P., *Thin film transistor*, M. Dekker, Ed., New York, 2003.

[26] C.-S. Yang, L. L. Smith, C. B. Arthur, and G. N. Parsons, "Stability of low-temperature amorphous silicon thin film transistors formed on glass and transparent plastic substrates," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 18, no. 2, p. 683, 2000.

[27] H. Hosono, N. Kikuchi, N. Ueda, and H. Kawazoe, "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples," *J. Non. Cryst. Solids*, vol. 198-200, pp. 165–169, 1996.

[28] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Gonçalves, A. J. S. Marques, R. F. P. Martins, and L. M. N. Pereira, "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature," *Applied Physics Letters*, vol. 85, no. 13, pp. 2541–2543, 2004.

[29] H. Hosono, *Transparent Amorphous Oxide Semiconductors for Flexible Electronics 13*, D. S. Ginley, Ed. Boston, MA: Springer US, 2010. [Online]. Available:

[30] J.-S. Park, H. Kim, and I.-D. Kim, "Overview of electroceramic materials for oxide semiconductor thin film transistors," *Journal of Electroceramics*, Sep. 2013. [Online]. Available:

[31] H. Hosono, "Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application," *Journal of Non-Crystalline Solids*, vol. 352, pp. 851–858, 2006.

[32] N. Mott, "Silicon dioxide and the chalcogenide semiconductors; similarities and differences," *Advances in Physics*, vol. 26, no. 4, pp. 363–391, 1977.

[33] S. Narushima, M. Orita, M. Hirano, and H. Hosono, "Electronic structure and transport properties in the transparent amorphous oxide semiconductor 2 CdOâGeO2," *Physical Review B*, vol. 66, no. 3, pp. 15–16, 2002.

[34] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4," *Thin Solid Films*, vol. 486, pp. 38–41, 2005.

[35] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Materials*, vol. 2, no. 1, pp. 15–22, Jan. 2010. [Online]. Available:

[36] J. Park, S. Wang, M. Li, C. Ahn, J. K. Hyun, D. S. Kim, D. K. Kim, J. a. Rogers, Y. Huang, and S. Jeon, "Three-dimensional nanonetworks for giant stretchability in dielectrics and conductors." *Nature communications*, vol. 3, no. May, p. 916, Jan. 2012. [Online]. Available:

[37] N. Tiwari, H.-p. D. Shieh, and P.-t. Liu, "Structural , optical , and photoluminescence study of ZnO / IGZO thin fi lm for thin fi lm transistor application," *Materials Letters*, pp. 1–4, 2015. [Online]. Available:

[38] X. Su, L. Wang, R. Sun, C. Bao, Y. Lu, and R. Wang, "Amorphous (In2O3)x(Ga2O3)y(ZnO)1âxây thin films with high mobility fabricated by pulsed laser deposition," *Applied Surface Science*, vol. 282, pp. 700–703, 2013. [Online]. Available:

[39] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park, and J. Chung, "Amorphous gallium indium zinc oxide thin film transistors: Sensitive to oxygen molecules," *Applied Physics Letters*, vol. 90, no. 19, 2007.

[40] T. Kawaharamura, T. Uchida, D. Wang, M. Sanada, and M. Furuta, "Enhancing carrier mobility of IGZO TFT fabricated by non-vacuum mist CVD with O 3 assistance," *Physica Status Solidi (C)*, vol. 4, pp. n/a–n/a, Oct. 2013. [Online]. Available:

[41] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, and H. Sirringhaus, "Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a âsolâgel on chipâ process." *Nature materials*, vol. 10, no. 1, pp. 45–50, 2011. [Online]. Available:

[42] H. Q. Chiang, B. R. McFarlane, D. Hong, R. E. Presley, and J. F. Wager, "Processing effects on the stability of amorphous indium gallium zinc oxide thin-film transistors," *Journal of Non-Crystalline Solids*, vol. 354, no. 19-25, pp. 2826–2830, May 2008. [Online]. Available:

[43] H. Pu, Q. Zhou, L. Yue, and Q. Zhang, "Investigation of oxygen plasma treatment on the device performance of solution-processed a-IGZO thin film transistors," *Applied Surface Science*, vol. 283, pp. 722–726, 2013. [Online]. Available:

[44] S. Hwang, J. H. Lee, C. H. Woo, J. Y. Lee, and H. K. Cho, "Effect of annealing temperature on the electrical performances of solution-processed InGaZnO thin film transistors," *Thin Solid Films*, vol. 519, no. 15, pp. 5146–5149, May 2011. [Online]. Available:

[45] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous InâGaâZnâO thin-film transistors," *Science and Technology of Advanced Materials*, vol. 11, no. 4, p. 044305, Aug. 2010. [Online]. Available:

[46] X. Ding, J. Zhang, H. Zhang, H. Ding, C. Huang, J. Li, W. Shi, X. Jiang, and Z. Zhang, "ZrO2 insulator modified by a thin Al2O3 film to enhance the performance of InGaZnO thin-film transistor," *Microelectronics Reliability*, pp. 3–7, Jul. 2014. [Online]. Available:

[47] N. Münzenrieder, S. Member, L. Petti, C. Zysset, T. Kinkeldei, G. A. Salvatore, G. Tröster, and S. Member, "Flexible Self-Aligned Amorphous InGaZnO Thin-Film Transistors With Submicrometer Channel Length and a Transit Frequency of 135 MHz," pp. 1–6, 2013.

[48] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "All oxide transparent MISFET using high-k dielectrics gates," *Microelectronic Engineering*, vol. 72, no. 1-4, pp. 294–298, 2004.

[49] L. Wang, M.-H. Yoon, G. Lu, Y. Yang, A. Facchetti, and T. J. Marks, "High-performance transparent inorganicâorganic hybrid thin-film n-type transistors," *Nature Materials*, vol. 5, no. November, pp. 893–900, 2006. [Online]. Available:

[50] S. Yang, J.-i. Lee, S.-h. K. Park, W.-s. Cheong, D.-h. Cho, S.-m. Yoon, C.-w. Byun, C.-s. Hwang, H.-y. Chu, K.-i. Cho, and T. Ahn, "Environmentally Stable Transparent Organic/Oxide Hybrid Transistor Based on an Oxide Semiconductor and a Polyimide Gate Insulator," *IEEE Electron Device Letters*, vol. 31, no. 5, pp. 446–448, May 2010. [Online]. Available:

[51] C. J. Chiu, S. P. Chang, C. Y. Lu, P. Y. Su, S. J. Chang, J. Ihm, and H. Cheong, "High-Performance a-IGZO Thin-Film Transistor with Organic Polymer Dielectric Layer," vol. 929, no. May, pp. 929–930, 2011. [Online]. Available:

[52] K. Lee, K.-t. Kim, J.-M. Choi, M. S. Oh, D. K. Hwang, S. Jang, E. Kim, and S. Im, "Improved dynamic properties of ZnO-based photo-transistor with polymer gate dielectric by ultraviolet treatment," *Journal of Physics D: Applied Physics*, vol. 41, no. 13, p. 135102, 2008.

[53] J.-H. Choi, H.-S. Seo, and J.-M. Myoung, "Dual-Gate InGaZnO Thin-Film Transistors with Organic Polymer as a Dielectric Layer," p. H145, 2009.

[54] K. Nomura, T. Aoki, K. Nakamura, T. Kamiya, T. Nakanishi, T. Hasegawa, M. Kimura, T. Kawase, M. Hirano, and H. Hosono, "Three-dimensionally stacked flexible integrated circuit: Amorphous oxide/polymer hybrid complementary inverter using n -type a-In-Ga-Zn-O and p -type poly-(9,9-dioctylfluorene-co-bithiophene) thin-film transistors," *Applied Physics Letters*, vol. 96, no. 2007, pp. 10–13, 2010.

[55] W. F. Beach, C. Lee, D. Bassett, J. Wiley, S. New, A. S. Harrus, M. A. Plano, D. Kumar, and J. K. Proceedings, *Encyclopedia of polymer science and engineering Parylene*, 2nd ed., Wiley & Sons, Ed., 1989, vol. 17.

[56] M. Szwarc, "Some remarks on the CH2=CH2 molecule," in *Discussions of the Faraday Society*, vol. 2, 1947, pp. 46–49. [Online]. Available:

[57] W. F. Gorham, "A New , General Synthetic Method for the Preparation of Linear Poly â p â xylylenes," *J. Polym. Sci. Polym. Chem*, pp. 3027–3039, 1966.

[58] Coatings SCS Parylene, "SCS Parylene Properties," 2011. [Online]. Available:

[59] A. Greiner, "Poly (1 , 4-xylylene) s : Polymer Films by Chemical Vapour Deposition," *Trends Polym Sci*, p. 5:12, 1997.

[60] V. Podzorov, V. M. Pudalov, and M. E. Gershenson, "Field-effect transistors on rubrene single crystals with parylene gate insulator Field-effect transistors on rubrene single crystals with parylene gate insulator," vol. 1739, pp. 15–18, 2003.

[61] K. N. N. Unni, S. Dabos-Seignon, J.-M. J.-M. Nunzi, and K. N. Narayanan Unni, "Influence of the polymer dielectric characteristics on the performance of a quaterthiophene organic field-effect transistor," *J. Mater. Sci.*, vol. 41, no. 2, pp. 1866–1871, 2006. [Online]. Available:

[62] "VSI Parylene." [Online]. Available:

[63] Y. Liu, H. Zhou, R. Cheng, W. Yu, Y. Huang, and X. Duan, "Highly flexible electronics from scalable vertical thin film transistors." *Nano letters*, vol. 14, no. 3, pp. 1413–8, Mar. 2014. [Online]. Available:

[64] R. Martins, A. Nathan, R. Barros, L. Pereira, P. Barquinha, N. Correia, R. Costa, A. Ahnood, I. Ferreira, and E. Fortunato, "Complementary metal oxide semiconductor technology with and on paper." *Advanced materials (Deerfield Beach, Fla.)*, vol. 23, no. 39, pp. 4491–6, Oct. 2011. [Online]. Available:

[65] H.-h. Hsu, C.-y. Chang, and C.-h. Cheng, "A Flexible IGZO Thin-Film Transistor With Stacked TiO 2 -Based Dielectrics Fabricated at Room Temperature," vol. 34, no. 6, pp. 768–770, 2013.

[66] G. a. Salvatore, N. Münzenrieder, T. Kinkeldei, L. Petti, C. Zysset, I. Strebel, L. Büthe, and G. Tröster, "Wafer-scale design of lightweight and transparent electronics that wraps around hairs." *Nature communications*, vol. 5, p. 2982, Jan. 2014. [Online]. Available:

[67] K. Park, D.-K. Lee, B.-S. Kim, H. Jeon, N.-E. Lee, D. Whang, H.-J. Lee, Y. J. Kim, and J.-H. Ahn, "Stretchable, Transparent Zinc Oxide Thin Film Transistors," *Advanced Functional Materials*, vol. 20, no. 20, pp. 3577–3582, Oct. 2010. [Online]. Available:

[68] B. K. Sharma, B. Jang, J. E. Lee, S.-h. Bae, T. W. Kim, H.-j. Lee, J.-h. Kim, and J.-h. Ahn, "Load-Controlled Roll Transfer of Oxide Transistors for Stretchable Electronics," pp. 2024–2032, 2013.

[69] N. Münzenrieder, G. Cantarella, C. Vogt, L. Petti, L. Büthe, G. a. Salvatore, Y. Fang, R. Andri, Y. Lam, R. Libanori, D. Widner, A. R. Studart, and G. Tröster, "Stretchable and Conformable Oxide Thin-Film Electronics," *Advanced Electronic Materials*, pp. n/a–n/a, 2015. [Online]. Available:

[70] R. Libanori, R. M. Erb, A. Reiser, H. L. Ferrand, M. J. Su, and R. Spolenak, "with extreme mechanical gradients," pp. 1–9, 2012.

[71] T. T. Trinh, V. D. Nguyen, K. Ryu, K. Jang, W. Lee, S. Baek, J. Raja, and J. Yi, "Improvement in the performance of an InGaZnO thin-film transistor by controlling interface trap densities between the insulator and active layer," *Semiconductor Science and Technology*, vol. 26, no. 8, p. 085012, 2011.

[72] W. J. Hwang, K. T. Eun, K. Y. Park, J. H. Ahn, S. H. Choa, J. Ihm, and H. Cheong, "The mechanical reliability of transparent ZnO TFT transfer printed on the flexible substrate," vol. 879, no. May, pp. 879–880, 2011. [Online]. Available:

[73] K. C. Sanal, M. Majeesh, and M. K. Jayaraj, "Growth of IGZO thin films and fabrication of transparent thin film transistor by RF magnetron sputtering," vol. 8818, pp. 881 814–881 814–7, Sep. 2013. [Online]. Available:

[74] J. S. Park, J. K. Jeong, H. J. Chung, Y. G. Mo, and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water," *Applied Physics Letters*, vol. 92, no. 7, pp. 34–36, 2008.

[75] P. K. Nayak, M. N. Hedhili, D. Cha, and H. N. Alshareef, "High performance solution-deposited amorphous indium gallium zinc oxide thin film transistors by oxygen plasma treatment," *Applied Physics Letters*, vol. 100, no. 2012, pp. 1–5, 2012.

[76] M.-J. Yu, Y.-H. Yeh, C.-C. Cheng, C.-Y. Lin, G.-T. Ho, B. C.-M. Lai, C.-M. Leu, T.-H. Hou, and Y.-J. Chan, "Amorphous InGaZnO Thin-Film Transistors Compatible With Roll-to-Roll Fabrication at Room Temperature," *IEEE Electron Device Letters*, vol. 33, no. 1, pp. 47–49, Jan. 2012. [Online]. Available:

[77] K. H. Cherenack, N. S. Münzenrieder, G. Tröster, S. Member, A. B. Zno, and A. T. F. T. Fabrication, "Impact of Mechanical Bending on ZnO and IGZO Thin-Film Transistors," vol. 31, no. 11, pp. 1254–1256, 2010.

4 Concurrent photopatterning of elastic modulus and structures in photosensitive silicone elastomers *

Contents

*A. Romeo and S. P. Lacour, "Concurrent photopatterning of elastic modulus and structures in photosensitive silicone elastomers", *Extrem. Mech. Lett.*, 2015.

4.1 Introduction

Photosensitive PDMS, P-PDMS, is a new class of silicone whose crosslinking process is sensitive to ultraviolet wavelength. Negative and positive photopatternable PDMS can be achieved by adding to the polymer base a photoinitiator, *e.g.*, 2,2-dimethoxy-2-phenyl acetophenone (DMPA), or a photoinhibitor, *e.g.*, benzophenone. [1–4]. Crosslinking among PDMS monomers will be activated or inhibited through UV light exposure, depending on the photosensitive compound employed.
Photosensitive PDMS has recently received significant interest since it provides a unique combination of properties of bulk PDMS *e.g.* microfabrication compatibility, elasticity, chemical inertness, optical transparency and low autofluorescence, with those of a photoresist in direct definition of microstructures upon UV exposure and development.
They have initially been used for those applications where silicone microstructuring is required (e.g. microfluidics), using P-PDMS as a conventional photoresist in a standard UV photolithography fabrication process. The method offers the advantages of PDMS elastomer, yet simplifies fabrication by eliminating the need for a master [3, 4].
Other groups have then implemented non developed positive P-PDMS to locally modulate the tensile modulus of the elastomer for stretchable electronics [5, 6] and soft cellular interface applications [7]. This technique allow to locally adjust the tensile modulus by direct lithography within a single PDMS rubber film.

A new approach to simultaneously patterning the topography and elasticity of positive P-PDMS film, solely by UV light exposure, without any wet processing, nor mechanical pre-loading of the elastomer is proposed [8]. Single-step photopatterning of silicone rubber may be used to form microfluidic chips and engineered substrates required for the hybrid integration of stretchable electronics and soft robotics.

P-PDMS miscrostructuring, chemistry and elasticity photopatterning and polymer single-step photopatterning will be described in the following section.

4.1.1 PDMS Microstructuirng

The ability to create surface patterns is at the heart of disciplines ranging from microelectronics [9] to cellular biology [10]. Over the last decades, the pool of materials that can be micromachined has significantly widened, with polymers playing a pivotal role in many applications. In particular, elastomeric devices that combine elasticity with biology, electronics or optoelectronics offer exciting new opportunities in microfluidics, soft transducers, stretchable electronics and implantable bioelectronics.

Among elastomers, Polydimethylsiloxane PDMS has become popular in a wide range of alternative applications due to its chemical and physical properties, as described in subsection 2.1.1. Creating surface patterns in a PDMS elastomer is usually performed by

soft lithography [11], dry etching of the elastomer through a mask [12], casting against a micromachined mold [13] or UV lithography of photosensitve PDMS [4]. This subsection focuses on the latest approach which offer a rapid and simple method for elastomer prototyping.

Lotters et al. [14] were the first to successfully demonstrate the patterning of PDMS by addition of DMAP photoinitiator. Exposure to UV light results in PDMS cross-linking of the exposed regions. This technique, however, required special processing conditions to address the oxygen and ambient light sensitivities of the photodefinable PDMS mixture. Nevertheless, Almasri et al [2] used this photodefinable PDMS formulation to fabricate a tunable infrared filter based on PDMS springs ($100\times100\ \mu m^2$ features). Alternatively, Dow Corning has introduced photodefinable silicone PPS products (WL-5000 series) to prepare structures with 15 μm minimum feature size [15, 16]. The product is similar to a conventional negative photoresist in terms of processing and high costs. In other recent work, Tsougeni et al. [17] demonstrated photopatterning of several types of siloxane copolymers with vinyl-methyl siloxane groups as polymerizable units by crosslinking with three photoinitiators (4,4'-bis(diethylamino)benzophenone, 99+%, thioxathen-9-one, 98%, and Igracure 651).
Recently, another PDMS photolithographic process has been reported using benzophenone as photoinibitor [3, 4]. Here the benzophenone is added to PDMS, which is then patterned with UV light exposure, cured and developed. When benzophenone is irradiated with UV light, benzophenone radicals are formed which react with the PDMS monomers inhibiting the cross-linking of the elastomer. During the post-exposure bake the unexposed PDMS is cured and crosslinked, while the exposed PDMS is washed away in toluene. Figure 4.1 illustrates a sketch of P-PDMS behavior under UV exposure. The authors demonstrated fabrication of features, ranging from 200 μm to 1 mm, using benzophenone concentration of 3% (w) for a standard PDMS prepolymer to curing agent ratio of 10:1. Moreover this fabrication process is not sensitive to ambient light, allowing for rapid application in any lab, eliminating the need for a cleanroom. Therefore adding the benzophenone to the elastomer mixture offers a simple and low- cost method for direct patterning PDMS

Positive P-PDMS chemistry

In terms of chemical structure, conventional PDMS consists of repeating *-OSi(CH3)2-* units. The base prepolymer is composed of 60 units terminating with a vinyl *-CH=CH2* group. The curing agent is similar but much smaller, (about ten units), it is methyl terminated and it has periodic silicon hydride *-OSiHCH3-* units. During the curing step, these PDMS monomers cross-link together to establish *Si-CH2-CH2-Si* linkages by reactions between the vinyl groups in the prepolymer and silicon hydride groups in the crosslinker [4, 18, 19]. The density of these linkages determines the mechanical properties of the resulting elastomer. The elastic modulus increase with the cross-link density, up to a certain limit. [20]

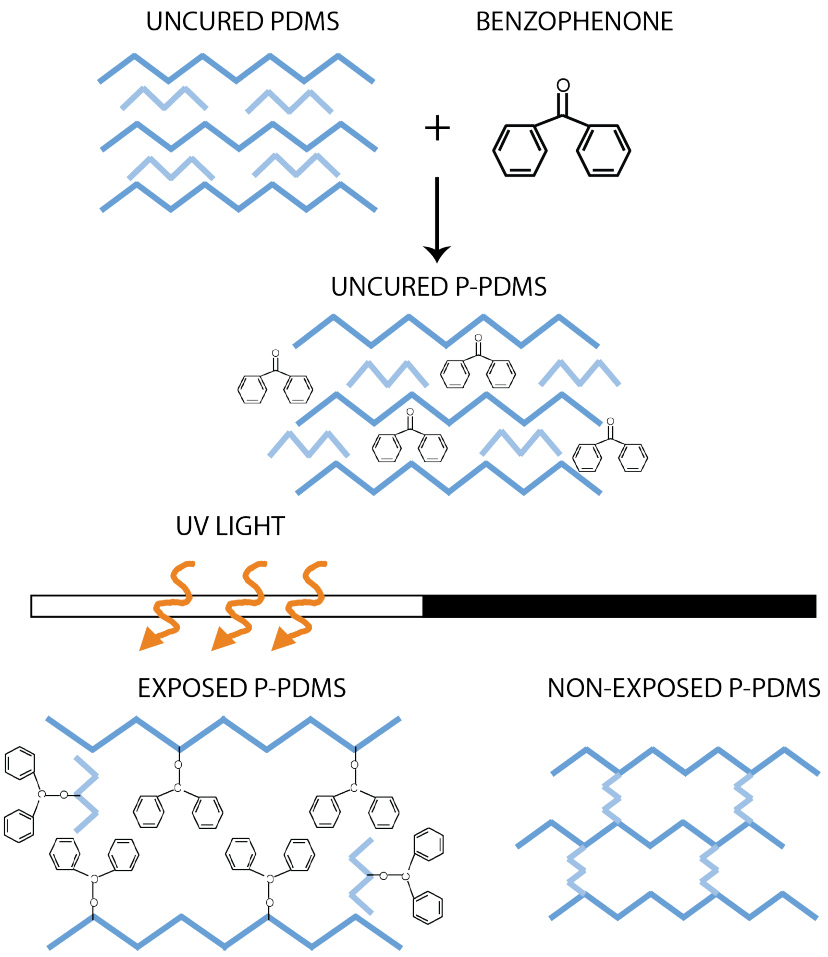


Figure 4.1: Schematic representation of positive P-PDMS under UV ligth exposure: benzhophenone is addedd to PDMS curing angent and prepolymer monomers to form photosensitive PDMS. When exposed with a patternend photomask, in the P-PDMS volume exposed through UV light, benzophenone radicals are formed which react with the binding site of PDMS monomers, preventing them from undergoing the traditional crosslinking reactions. While, in non-exposed portion, no radicals are formed and crosslink of PDMS monomers will occur.

Benzophenone (also known as diphenyl ketone) is a photosensitizer often used to initiate free-radical polymerization. When it is irradiated with UV light ($\sim$ 365 nm), a benzophenone radical is formed which is able to abstract a hydrogen atom from a suitable hydrogen donor [3, 4, 21]. Therefore if benzophenone is added to the uncured P-PDMS mixture, upon UV light, the benzophenone radicals react with both silicone prepolymer and curing agent, preventing them from undergoing the traditional crosslinking reactions.
Jothimuthu et al. [4] proposed a possible reaction mechanism that could account for the

benzophenone's inhibition of crosslinking. The proposed mechanism, based on the reduction of carbonyl groups by hydrosilane, was then validated through Fourier transform infrared spectroscopy (FTIR) investigation. The benzophenone radicals could act to abstract the hydrogen from the silicon hydride reactive groups present in the curing agent. Other radicals could combine with the vinyl terminated (*-CH=CH2*) groups of the base monomer to form short polymer chains. In both cases, the binding sites of the two PDMS components are reduced, limiting the potential cross-link density of the exposed area.
During the post-exposure bake, the unexposed PDMS is fully cured and crosslinked, while the exposed PDMS can be washed away in toluene [3, 4] or can lead to a photo-softening of the elastomer if the development step is omitted [5, 7].

4.1.2 Positive P-PDMS elasticity photopatterning

Spatial control of the elasticity of the patterned material is a more recent need. Tissue engineering designs integrate matrix mechanics and topography to control across scales cell behavior and cell-material interactions [22]. Hydrogels with spatially controlled compliance have been reported to modulate cells behavior [23]. The emergence of stretchable electronics and soft bioelectronics also motivate new design and materials strategies for mechanically heterogeneous structures [6, 24, 25]. Optimization of the soft-to-hard interface calls for local definition of the mechanical properties of the soft carrier and encapsulation materials to protect the fragile device materials.

Materials with patternable mechanical properties are of great importance in these applications. For example, the bulk Young's modulus of PDMS elastomers, could be conveniently controlled by the elastomer cross-linking and processing conditions, such as temperature and bake time. In a recent work, Cotton et al. [5] introduce a simple and straightforward method to locally control the tensile modulus by direct lithography within a single P-PDMS rubber film. When photosensitive PDMS is exposed through a mask to UV light, cross-linking of the UV exposed elastomer is inhibited, leading to softer regions than the surrounding unexposed matrix. If no development step is performed after the soft-exposure bake, photosoftening can be achieved. The authors demonstrated that P-PDMS (benzophenone concentration of 3% (w) of 10:1 PDMS) tensile modulus can be adjusted in the 0.65-2.9 MPa range by decreasing the UV exposure dose, from 24 to 0 J/cm^2. Uniform mechanical properties could be obtained through <200 μm thick P-PDMS film. Tuning of the tensile modulus of embedded 100 μm diameter features in a plain PDMS film was demonstrated. The mechanically patterned substrate was also implemented to engineer strain distributions across elastomeric substrates for stretchable electronics applications [6, 25].
Sun et al. [7] tuned the tensile modulus of the positive photosensitive PDMS for study of mechanoresponsive cellular behaviors. Here the P-PDMS mixture was prepared with a lower concentration benzophenone (1% w) and UV flood-exposed using a portable UV-lamp. A broad range of bulk Young's modulus for P-PDMS from 0.027 to 2.48 MPa was achieved by

modulating the PDMS prepolymer to curing agent ratio (10:1 and 30:1), UV light exposure energy density (0 to 2.7 J/cm^2), and post exposure baking time (20 min to 40 h at 110 °C). The authors demonstrated that the bulk Young's modulus of P-PDMS could impact cell morphology, adhesion formation, cytoskeletal structure, and cell proliferation since the cells could sense and respond to changes of substrate rigidity at a subfocal adhesion resolution.

4.1.3 Single-step photopatterning

Single-step photopatterning has widely been used to fabricated continuous surface relief micro-optical elements. Diffraction grating are made directly by irradiation of the polymeric surface through a phase mask [26] or a focused laser beam [27, 28] without any etching or wet process.The surface profile is directly controlled by the UV exposure dosage and the exposed areas. Grating feature size goes from tens of μm in width and hundred nm to few μm (<10) in depth. Many studies have concentrated on these method since it has significant technological advantages because it involves just a facile, entirely optical single step with no wet chemistry. In particular single-step photopatterninG was used to produce surface-relief gratings, SRGs, in azo-polymers, dry photopolymer films [27], inorganic-organic hybrid materials [26, 29] and polystirene films [30].
More recently Bowman's research group [31–33] introduced mechanophotopatterning of photosensitive elastomer, based on photoinduced stress relaxation due to addition fragmentation chain transfer (AFCT) process. This method enables the ability to manipulate both material shape and surface topography solely by exposure to light. Here, photopatterning of 3D micro-structures (0.41 mm in higth and 0.69 mm in width) in the pre-crosslinked thioene-based elastomer is achieved upon light exposure without any wet chemistry, but pre-stretching of the specimen is required.

In contrast to the latter process, I demonstrated single-step photopatterning of positive photosensitive PDMS films to simultaneously manipulate shape and elasticity of the polymer by simply exposure to UV light, without any pre-stretching or wet process. P-PDMS was prepared by adding benzophenone compound to the silicone polymer. Under UV light exposure benzophenone generates free radicals which inhibit the elastomer cross-linking. Subsequent curing sets topographical and elastic modulus patterns across the elastomeric membrane. Concurrent photopatterning of elastic modulus and structures in P-PDMS films provides an extremely useful and simple fabrication method for applications in stretchable electronics and polymer microstructuring.

4.2 Materials and methods

Photosensitive PDMS with two PDMS prepolymer:crosslinker (w:w) ratios R of 5:1 and 10:1 have been tested. For both ratios R, first the tensile elasticity of the photosensitive elastomer

exposed to different UV light energy density was evaluated. Then P-PDMS patternability against feature, size and spacing was tested. Next the combined topographical and mechanical patterning of P-PDMS was explored. Proof of concept designs using the photosensitive elastomer in microfluidics was also provided.

4.2.1 P-PDMS preparation

The P-PDMS membranes were manufactured using polymer spin-coating and photolithography using CMi facilities.
The positive P-PDMS mixture was prepared as following: first benzophenone flakes (3 wt.% of the elastomer mixture; 99% pure, Sigma Aldrich) dissolved in xylene (4.3 wt.% of the elastomer mixture; reagent grade, Fisher Scientific) for 2h, then PDMS (Sylgard 184, Dow Corning) prepolymer was added and blended overnight. Finally the PDMS curing agent was inserted and the final solution was mixed at 2200 rpm for 2 min.
The fabrication steps were implemented on top of rigid 4 inch Silicon wafer, covered with water soluble releasing layer. First water soluble release layer, poly (4-styrenesulfonic acid) (PSS) (18 wt.% in H_2O, Sigma Aldrich) was spin-coated on Si wafer at 1200 rpm for 30

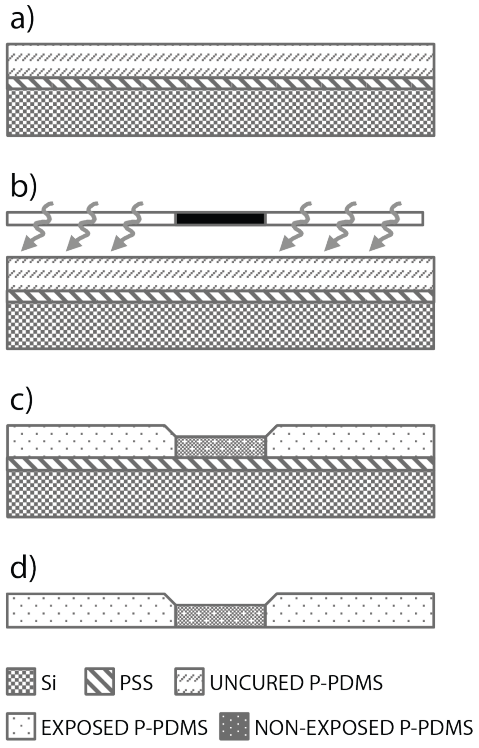


Figure 4.2: Schematic diagram showing the different step of P-PDMS preparation: a) Spin coat P-PDMS mixture, b)UV exposure trough Cr mask c) cure P-PDMS at 150°C, d) free-standing P-PDMS membrane after release in DI water.

s and subsequently cured at 150°$C$for 15 min on a hot plate. Then the P-PDMS mixture is spin-coated onto the coated wafer (500 rpm, 5 s, followed by 680 rpm, 30 s) to obtain a layer of 70 μm thickness. The uncured P-PDMS was UV-exposed (Karl Suss MJB4 contact mask aligner) keeping an air gap between the mask and the spincoated polymer <1 mm. The elastomer was then cured onto a hotplate for 24 h at 150°C and released from Si carrier wafers by after immersion in DI water (Fig 4.2). No development was performed.

4.2.2 Young's modulus characterization

P-PDMS mixture prepared with either PDMS prepolymer: curing agent ratios R (5:1 and 10:1) were spincoated onto rigid substrate and UV flood-exposed with light energy densities of 0, 9 or 18 J/cm2. After exposure they were cured and released from the carrier wafer in deionized water.
The P-PDMS freestanding films were next cut into 10 mm x 30 mm strips in order to perform tensile tests. The rectangular samples were clamped to the jaws of an axial electromechanical testing system (MTS Criterion). The samples were stretched to a maximal strain of 10% with a strain rate of 0.1% × s and stress-strain curves were recorded. Mean values of Young's modulus were calculated for each exposure density and R ratio. The average was calculated as an average over 4 samples with the same exposure density and R, and the single value of E value for each sample was calculated as an average over three repeated tensile tests.

Top surface microstructuring

P-PDMS mixture mixture prepared with either PDMS ratios R (5:1 and 10:1) were spincoated on wafer with on top a water soluble polymer to form 70 μm thick membranes. These uncured P-PDMS membranes were exposed to UV light and patterned through a chromium mask carrying arrays of parallel chromium stripes with different geometrical parameters: length L, width W and spacing S. Two different sets of patterns have been tested, but all of them had the same length L=5 mm: (i) constant stripe width W=0.4 mm separated by increasing spacing S (from 0.4 mm to 6.4 mm), and (ii) constant stripe spacing S=5 mm and increasing width W (from 0.2 mm to 3.2mm) as shown in figure 4.3. The implemented UV exposure density was 18 J/cm^2 for all samples. The P-PDMS was than cured at 150 °C for 24h. Upon polymerization volume rearrangement of the elastomeric film occured, modulating locally the thickness of the film within the UV-shielded and irradiated zones. Top surface profiles have been recorded with a mechanical profilometer (Bruker Dektak XT Profilometer).

Stiffness characterization

Next the combined topographical and mechanical patterning of the photosensitive elastomer was explored. Uncured P-PDMS membranes (with R of 5:1 and 10:1), spincoted onto Si carrier, were UV-exposed (at 18 J/cm^2 energy density) through a chromium mask with hexagonal, transparent patterns. The non-exposed patterns of the this hexagonal layout (

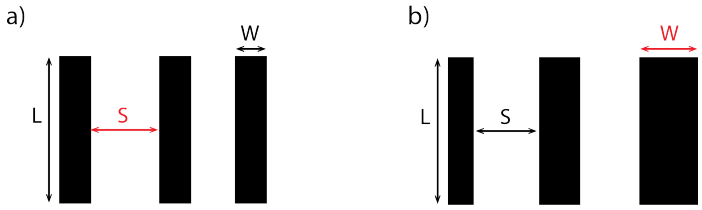


Figure 4.3: Schematic of the stripe non exposed patterns: a) L=5 mm, W = 0.4 mm and S is varying from 0.4 to 6.4 mm; b) L=5 mm, S=5 mm, W is varying from 0.2 to 3.2 mm.

Fig4.4) have a side length L and width W of 5 mm and 1 mm respectively. Fully exposed hexagonal areas were formed in the center. After thermal curing, top surface profiles of the non exposed patterns were recorded with a mechanical profilometer, as described above. Next P-PDMS membranes were cut into samples of 2 cm 2×4 cm and released from the rigid wafers. Each sample was then mounted in a customized uni-axial extensiometer, and stretched to 20% macroscopic strain. Experimental strain maps and strain profile, representing the maximal principal strain, were recorded at the top surface of each sample using a Digital Image Correlation (DIC) system (LIMESS Messtechnik und Software GmbH, Istra 4D v4.3.0 software) as explained in section 2.2.2. The section delimited by the red dotted line in figure4.4, highlights the selected area for strain mapping.

Microfluidics

In Chapter 2 a possible use of positive, mechanically patterned P-PDMS for stretchable electronics application was presented. Here, as proof of concept of concurrent mechanical and topographical photopatterning, single-step photoppaterning was employed to fabricate Y-shaped P-PDMS channels for potential application in microfluidics.
The P-PDMS was prepared with 5:1 prepolymer:curing agent ratio, since it allows for a deeper depression of the non-exposed pattern. 70 μm thick polymer membrane was spin-coated onto

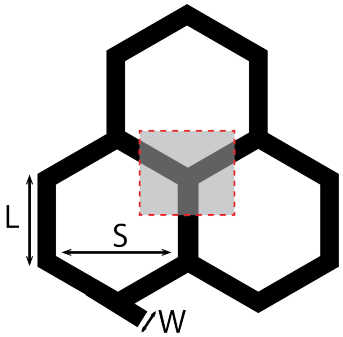


Figure 4.4: Schematic of the hexagonal non-exposed pattern L=5 mm, W= 1 mm, S = ; the red zone highlights the selected area for strain mapping.

Si wafer and exposed to UV light (18 J/cm^2) through a $\sim 60°$ wall angle, Y-shaped features of side width 800 μm), chromium mask. After curing at 150 $°C$ for 24h, a thick slab of PDMS was subsequently bonded to the patterned P-PDMS surface using oxygen plasma. Figure4.5 shows a schematic cross section of the P-PDMS microchannel.

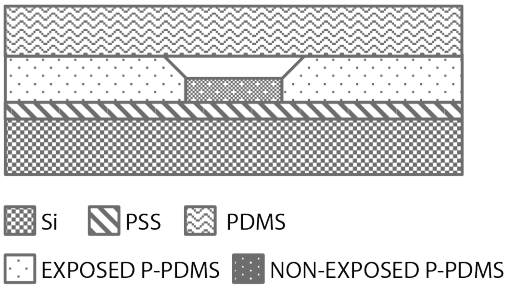


Figure 4.5: Schematic cross-section of a P-PDMS microchannel

4.3 Results and discussions

4.3.1 Young's modulus characterization

As described in subsection4.1.2, when the uncured P-PDMS is irradiated with UV light, benzophenone free radicals are formed, which react with both the curing agent and the prepolymer inhibiting the crosslinking of the elastomer. The mechanical properties of PDMS depends mainly from the the crosslink density. Therefore under UV light, the elastomer softens.

Figure4.6 shows the Young's modulus E of the photosensitive elastomer as function of UV light density absorbed. Pristine P-PDMS films displayed modulus in the range of 2.4 MPa and 3.2 MPa $\pm$ 0.1MPa for the prepolymer: curing agent ratio R of 10:1 and 5:1 respectively. Clearly, higher concentration of curing agent (5:1) in P-PDMS mixtures implies higher crosslinking density, at a given UV exposure energy.
Upon UV light exposure, the elastic modulus decreased for both ratios. To quantify this reduction the variation in the Young's modulus between the bulk, non-exposed, elastomer E_0 and the elastomer exposed with the maximum UV density ($18 J/cm^2$) E_{18} was evaluated. The P-PDMS tensile modulus when R=5:1 could be adjusted in a range between the 3.2 â 2.25 MPa. A reduction in the modulus up to 1.42 times (E_0/E_{18}) that of the non-exposed elastomer was observed. This reduction was doubled in 10:1 P-PDMS, where E_0/E_{18}=3 within a range of 2.4 - 0.79 MPa.
The resulting tensile modulus is inversely proportional to the UV light absorbed, this allows

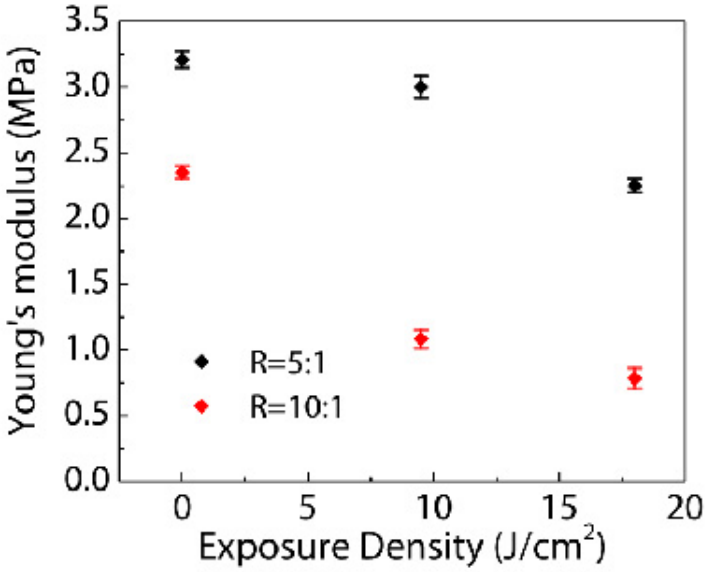


Figure 4.6: Tensile Young's modulus of P-PDMS as a function of UV exposure density for two initial prepolymer:curing agent ratio R (10:1 and 5:1).

for optical tuning of the mechanical properties of a continuous elastomeric membrane. By modulating the PDMS prepolymer to curing agent ratio and UV light exposure energy, it was possible to achieve a broad range of bulk Young's modulus for P-PDMS from 0.079 to 3.2 MPa.
The ability to locally pattern the stiffness of the P-PDMS membrane has been explored in chapter 2, where engineered substrates with distinct non-stretchable zones embedded in a yet elastic matrix were presented.

4.3.2 Top surface microstructuring

Young's modulus of the photopatternable PDMS can be adjusted as function of the UV energy density absorbed. At the same time, upon patterned UV exposure, volume rearrangement of the elastomeric film occurs, modulating locally the thickness of the film within the UV-shielded and irradiated zones. I noticed that in the P-PDMS membranes exposed through chromium rectangular patterns, as described in subsection 4.2.2, depressions appear within the non-exposed P-PDMS. This outcome could be caused by the volume shrinkage as consequence of the higher crosslink density of the non exposed P-PDMS. Both depth and profile of these channels are function of the mask pattern geometry, W and S, and the initial mixing ratio R. Moreover, the shape of the transferred pattern depends on the mask-to-P-PDMS air gap during UV exposure, which was necessary since the P-PDMS film was not cured yet during the exposure. As consequence of the air gap ($< 1mm$) UV light

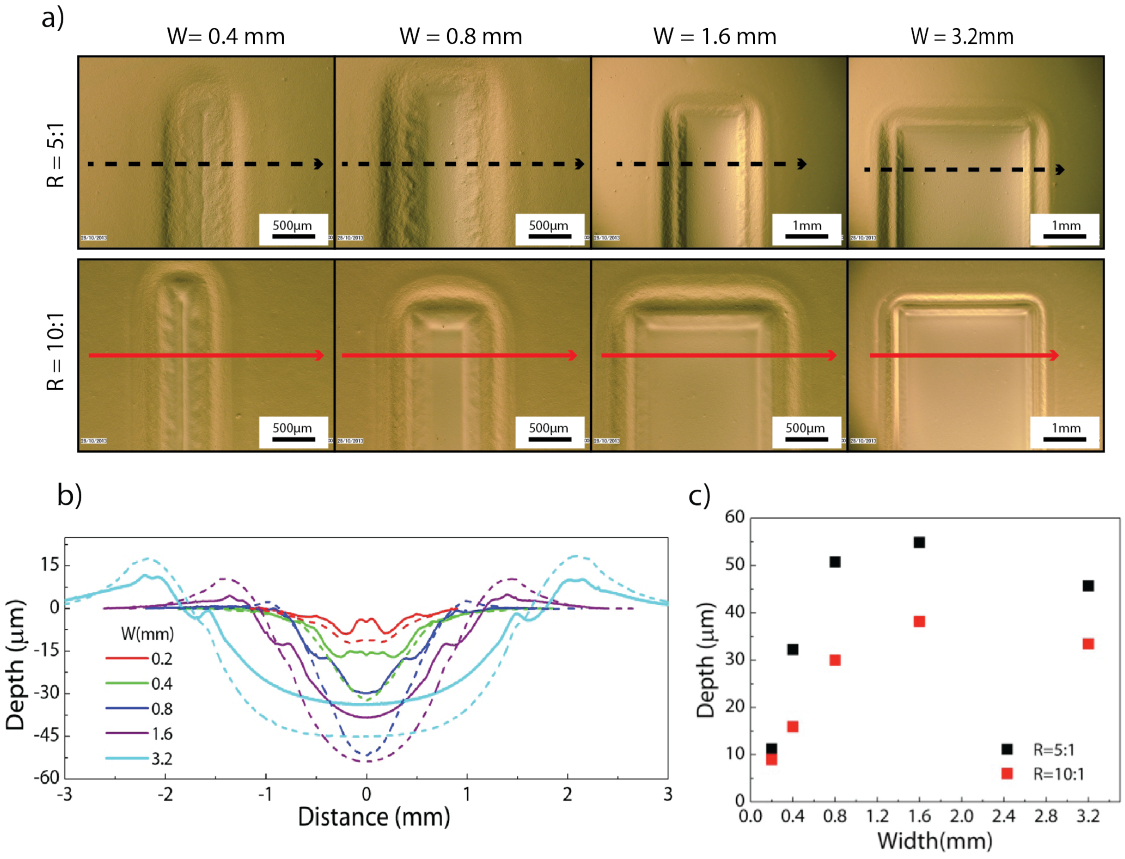


Figure 4.7: Channel profiles as function of the width W: a) Optical picture of the transferred rectangular pattern on the P-PDMS film for both R, 5:1 (*top*) and 10:1 (*bottom*); b) profile of the top surface of each rectangular pattern, the solid and the dashed lines represent the 10:1 and 5:1 prepolymer:crosslinker ratio R, respectively; c) maximum depth of each profile measured at the center of the depression

was diffracted and pattern distortion occurred. An improved control of the gap could help in reducing diffraction bevel and bumps at the pattern edges.

To evaluate the depression depth, top surface profiles were recorded across the entire width of each pattern, from one exposed edge to the opposite one.
Figure4.7 (a) shows optical pictures of the films exposed with rectangular pattern with different W, when S=5mm. Red and black arrows indicate where the depth profile have been taken. Figure4.7 (b) and (c) represent respectively the top surface profile of each pattern and the maximum depth of each profile, measured at the center of the depression, as function of different spacing. The channels deepened with increasing pattern width until W = 1.6 mm. Beyond this value, when W=3.2 mm, shallower channels are formed, accompanied with large bumps along both edges of the line. The height of these lateral protrusions increased

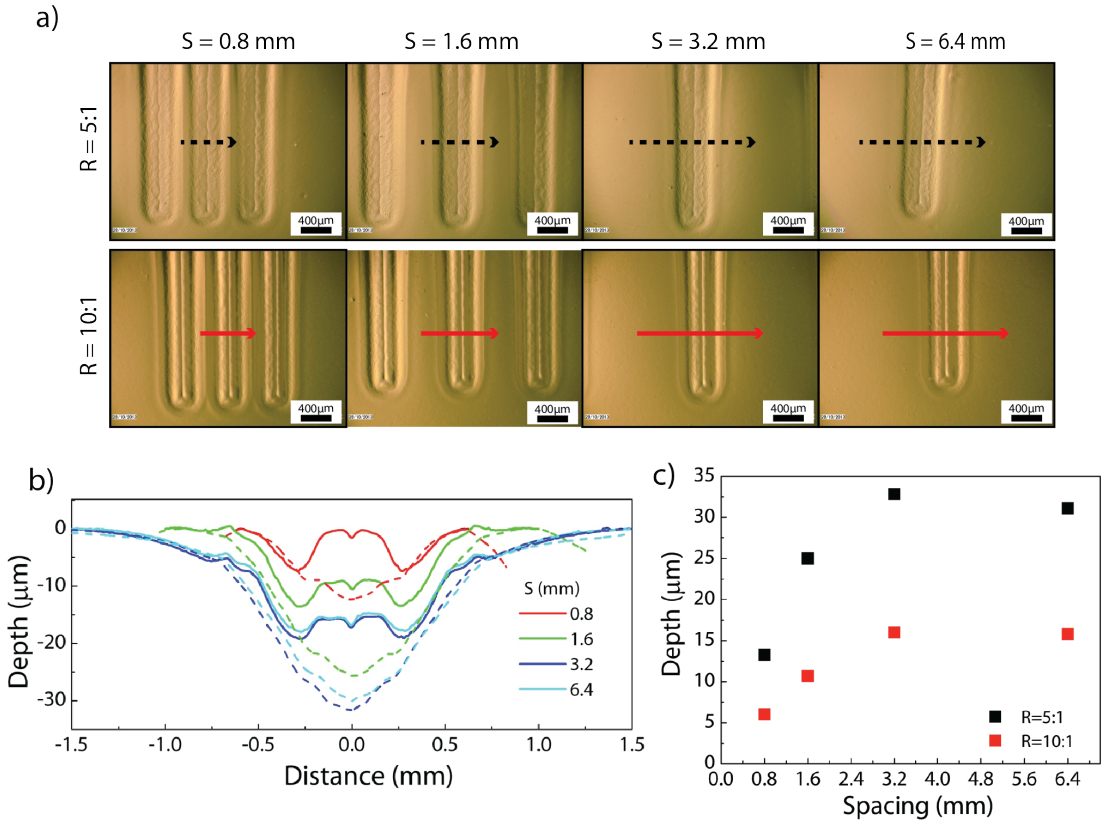


Figure 4.8: Channel profiles as function of the spacing S: a) Optical picture of the transferred rectangular pattern on the P-PDMS film for both R, 5:1 (*top*) and 10:1 (*bottom*); b) profile of the top surface of each rectangular pattern, the solid and the dashed lines represent the 10:1 and 5:1 prepolymer:crosslinker ratio R, respectively; c) maximum depth of each profile measured at the center of the depression

with the depth and the width of the non-exposed pattern. It is then likely that during the curing step at 150°C, material flow from the non-exposed to the irradiated regions is triggered because the diffusivity of the polymer chains is higher in the exposed than in the non-exposed elastomers [29, 30, 34].

Figure4.8 shows optical pictures, depth profiles and maximum depth of the non-exposed patterns with different spacing S, when W= 0.4 mm. For a given line width, the depth of the channels increases with line spacing to reach a plateau when S > 8W. Here, edge bumps were not affected by the spacing.
In all cases, for a given S and W, the patterned P-PDMS membrane with 5:1 initial mixtures showed deeper non-exposed channels than the 10:1 one. Maximum depth of 55 μm was measured in 5:1 P-PDMS membrane when the rectangular pattern was 5 mm in spacing and 1.6 mm in width.
The resulting distinct cross-link densities between the exposed and non-exposed P-PDMS

volumes lead to local softening of the elastomer membrane thereby may also lead to distinct lateral material transfer and structural shrinking of the non-exposed part. The last two structural factors contribute to the final outline of the channels. Therefore patterning of continuous relief structures can be easily achieved by direct UV exposure within a single P-PDMS rubber film and without any development step.

4.3.3 Stiffness characterization

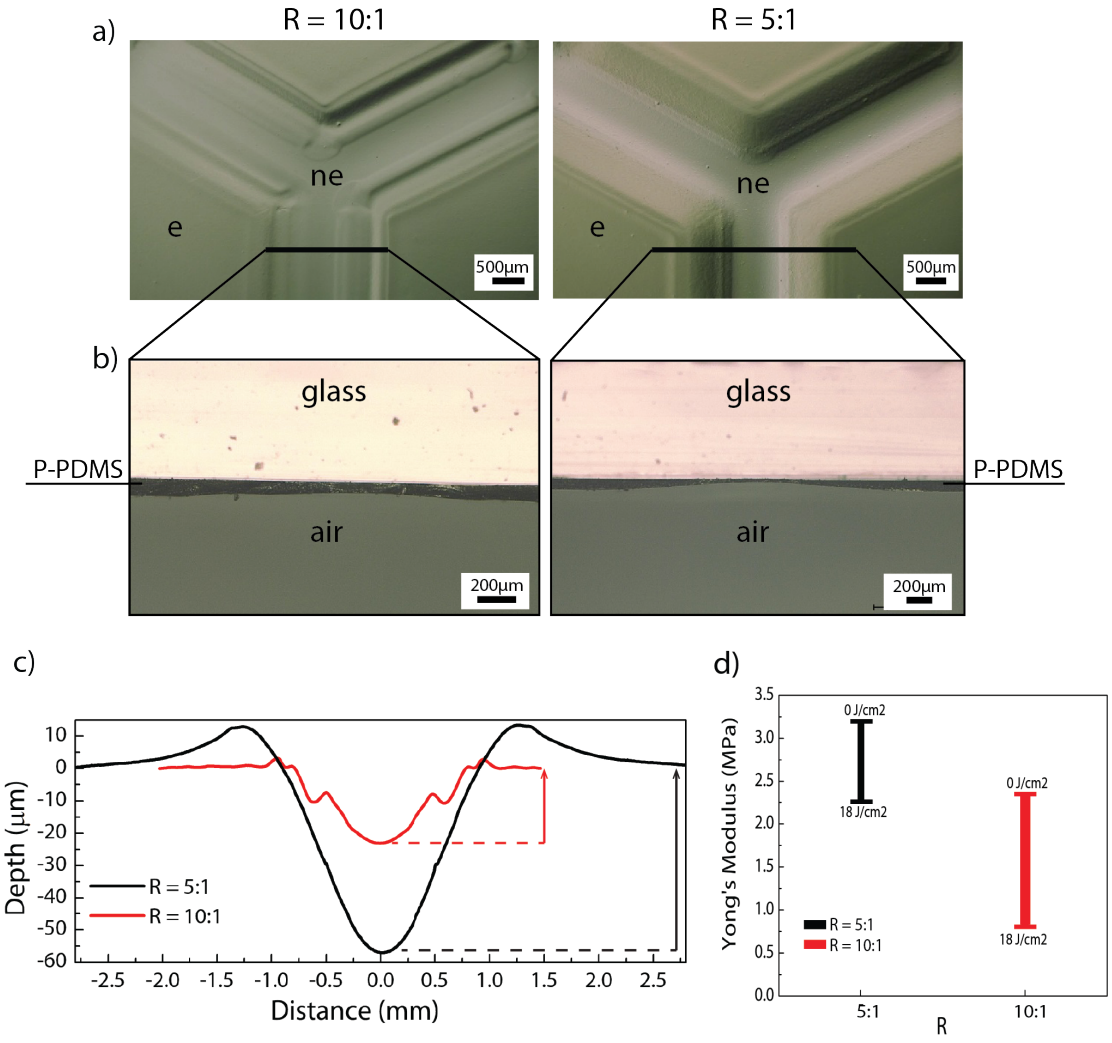


Figure 4.9: Surface characterization of the hexagonal non-exposed (*ne*) patterns for both P-PDMS ratio *R*: a) top view optical images and b) corresponding cross sections of the non exposed channels; c) top surface profiles of the non-exposed channels; and d) corresponding Young's modulus range at different exposure densities (0 and 18 J/cm^2).

Tuning optically the crosslink density affects simultaneously the thickness t and the Young's modulus E of the P-PDMS films was demonstrated. Then, the combined topographical and mechanical patterning of P-PDMS, and how they influence the resulting film stiffness were investigated.

Figure4.9 (a) and (b) show optical images, top view and cross section, of hexagonal mask patterns reproduced in P-PDMS films for both ratios R in samples described in subsection4.2. The non exposed patterns are distinctly visible on the cured film, as well as, the non uniform thickness. Figure4.9 (c) and d display for each R the top surface profiles of non-exposed channels and the Young's modulus change between the exposed and non-exposed P-PDMS. To evaluate the resulting stiffness of the patterned samples two ratios, η and χ, were defined as:

$$\eta = \frac{E_{ne}}{E_e} \tag{4.1}$$

$$\chi = \frac{t_e}{t_{ne}} \tag{4.2}$$

where E_{ne}, t_{ne}, E_e and t_e are the tensile elastic modulus and thickness of non-exposed (0 J/cm^2) and UV exposed P-PDMS (18 J/cm^2), respectively. If $\eta/\chi > 1$, then the effect of the Young's modulus is predominant and the non-exposed pattern is stiffer than the exposed surrounding film. This is the case of 10:1 P-PDMS where η=3 and χ =1.5. Viceversa, if $\eta/\chi < 1$, the relative change in thickness prevails and the non-exposed pattern is softer than the exposed part, even if its Young's modulus is bigger. This is the case of the 5:1 P-PDMS where η=1.42 and χ=3.7.

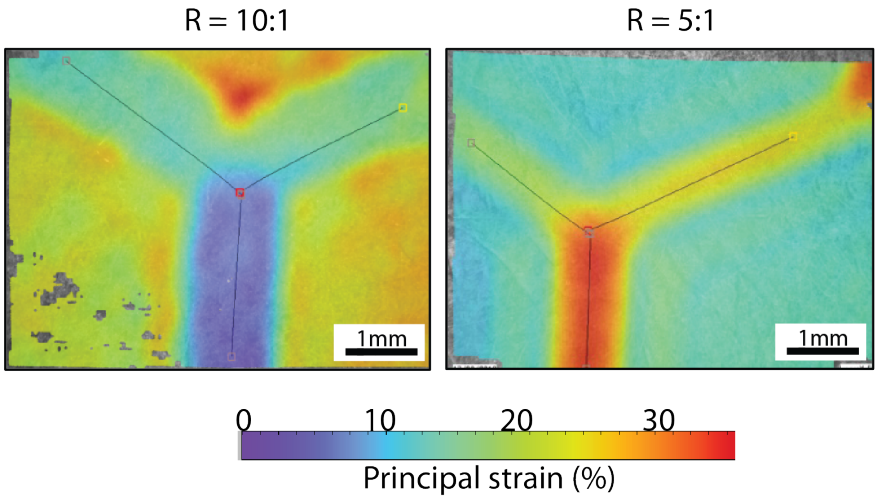


Figure 4.10: Surface strain maps (principal strain) for both P-PDMS ratios (10:1 and 5:1)taken when a 20% macroscopic strain is applied to P-PDMS sample with hexagonal non-exposed patterns.

To demonstrate the different resulting stiffness, the strain distribution in the stretched samples was investigated. Figure4.10 shows that the exposed 10:1 and 5:1 samples display nearly opposite strain maps. At 20% applied strain, the non-exposed, 10:1 P-PDMS is nearly undeformed while the surrounding exposed elastomer stretches to ∼25% strain. Conversely, the UV exposed volume in the 5:1 sample stretches slightly but the non-exposed Y-pattern expands to strain up to 35%. Here, although the tensile elastic modulus of the non-exposed polymer regions is bigger than that of exposed ones, the relative change in thickness in the material is larger than that of the modulus change ($\eta/\chi > 1$). Then, the local stiffness of the non-exposed film is smaller than that of the surrounding film and the non-exposed pattern stretch further.
The combination of locally adjusted elastic modulus and thickness, allows for inverting the mechanical behavior of the UV patterned P-PDMS membrane solely by changing the prepolymer:curing agent ratio.

4.3.4 Microchannels

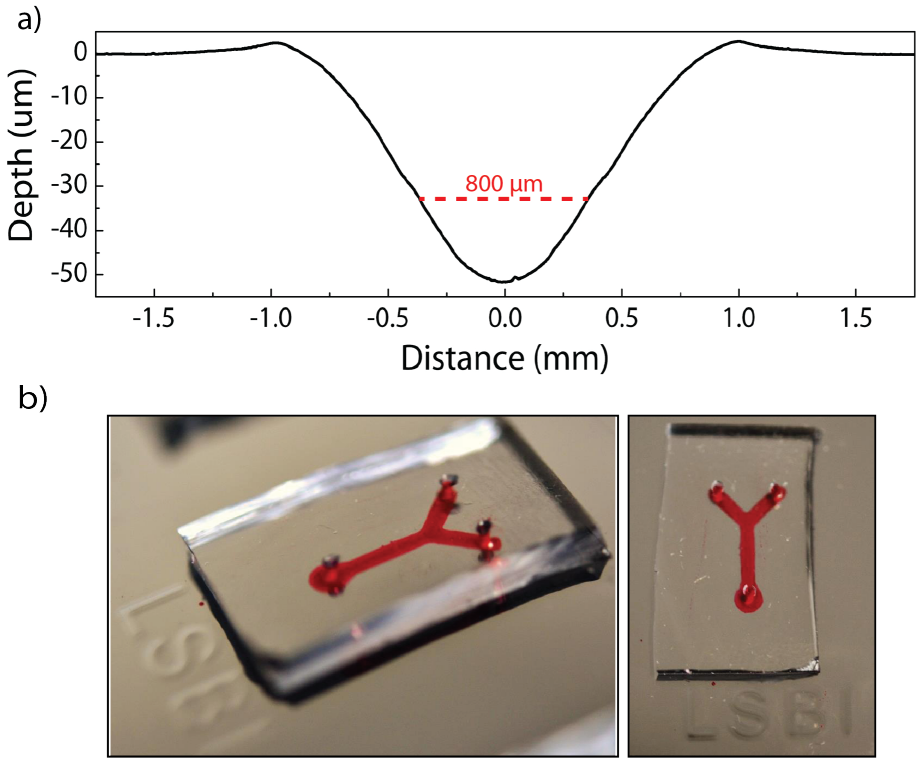


Figure 4.11: Fabrication of microfluidic channel: a) top surface profile of microchannel exposed through a 800 μm wide Y shape pattern Chromium mask. b) Optical pictures of an encapsulated microchannel filled with a red dye.

Microchannels were fabricated to demonstrate a possible applications in microfluidics of P-PDMS single-step photopatterning technique. Microchannels with sub-millimeter cross-section were prepared as described in subsection4.2.2. 800 μm wide Y patterns on the lithography mask lead channels of 2 mm width and 52 μm depth within the P-PDMS. Their profile is displayed in figure4.11 (a). To complete the microchannels the patterned P-PDMS membranes were bonded to a 1 mm thick PDMS slab. The encapsulated channels were then filled with a red dye to demonstrate good channel definition and reliable sealing (Fig.4.11 (b)). An important observation is that even though the P-PDMS contains benzophenone, it still bonded well with the thick PDMS slab. The benzophenone did not affect the quality of the bonding.

Positive P-PDMS microchannel have been fabricated through a direct photopatterning of the elastomer in a process identical to that of thick photoresists [3]. This technique eliminated completely the need for a master. With single-step photpatterning, the fabrication process is further simplified by omitting the development step and proposing an essential "dry"method for P-PDMS microstructuring.

4.4 Conclusion

Photosensitive elastomers are an interesting class of polymers combining within one material the mechanical properties of an elastomer with the features of a photoresist.
Positive P-PDMS may be prepared by adding benzophenone to PDMS prepolymer:crosslinker mixture. Benzophenone acts as a photoinhibitor: under UV exposure bezhophenone radicals are formed which react with both prepolmyer and crosslinker binding site, inhibiting the cross-linking of the elastomer. Therefore modulating the UV ligth absorbed cross-link density of photosensitve PDMS may be adjusted and locally modified. Developed P-PDMS films have been used in a process similar to that of positive photoresist for rapid prototyping PDMS-based lab-on-a-chip LOC system. Whereas, non-developed P-PDMS has been employed to locally adjust the elastomer tensile modulus whitin a continuous membrane for engineering stretchable electronic substrates.
Here I demonstrated that shape and elasticity can be engineered in a single elastomeric membrane using simple UV exposure through standard photolithography mask. Absorption of UV light restricts cross-linking therefore softens the elastomer, but also induces distinct lateral material transfer and structural shrinking of the non-exposed elastomer. The described process eliminates lithography wet development step therefore offers a new technique to PDMS microstructuring.
P-PDMS was made using a benzophenone concentration of 3% (w) dissolved in xylene. P-PDMS photopatterning ability have been investigated as function of UV energy density, prepolymer:curing agent ratio, and patterns size and spacing.
By modulating the PDMS prepolymer to cross-linker and UV light density, a wide range of rigidity change from 0.79 to 3.2 MPa was achieved. The addition of benzophenone to the

PDMS monomers on their own has little impact on the cross-linking ability of the original mixture. However,when the mixed compound is irradiated with UV light, the potential cross-link density is limited and photosoftening is induced in the P-PDMS.
Moreover P-PDMS elastomers responds to patterned UV light by continuously and locally deforming via volume rearrangement, which enables 3D control of its geometry. Rectangular chromium patterns are reproduced in the P-PDMS membrane solely by Uv irradiation, no development step was required. The quality of the reproduced pattern on the elastomer depended on the distance between the photo-mask and the P-PDMS film. Top surface profile showed depressions are produced within the non-exposed areas. The depth and profile of this depression are function of the pattern geometry and prepolymer to crosslinker ratio.Thin films 70 μm in thickness with features ranging from 400 μm to a few millimeters in size were successfully demonstrated. Depression depth increases with the increasing of the width and the spacing of the non-exposed patterns till reaching a plateau. Furthermore, lateral protrusion are formed at the edge of the pattern, whose high is proportional to the compressed volume. Thus, lateral material transfer clearly occurs from the shaded areas to the irradiated ones, enabling the formation of variable surface structure. Rectangular patterns with 1.6 mm in width and 5 mm in depth achieved the maximum depth of 55 μm and edge bumps of $\sim$ 10 μm within a film thickness of 70 μm.
The combined mechanical and topographical patterning of P-PDMS influences the resulting film stiffness. This is function of relative change of both Young's modulus and film thickness between the exposed and the non-exposed zones. Although the tensile elastic modulus of the exposed regions of the elastomer is lower than that of non-exposed regions, if the relative change in thickness in the material is not larger than that of the modulus change, then the local stiffness of the exposed film is larger than that of the surrounding film, and the patterned volumes stretch further. This allows for inverting the mechanical behavior of the UV patterned P-PDMS membrane solely by changing the prepolymer:crosslinker ratio.
Microchannels of sub-millimeter cross-section and millimeter length, were fabricated directly upon the photosensitive PDMS films, and this presents a number of interesting possibilities. In general, PDMS prototyping requires treatments, such as developing and dry or wet etching processes, after irradiation. However, single-step photopatterning of photosensitive PDMS used in this study did not require such additional steps simplifying multi-tiered feature fabrication.
The proposed method allows for the creation of motifs of controlled shapes and elastic moduli within a single elastomer membrane thus presents a rapid prototyping approach for soft MEMS, microfluidics and stretchable electronics.

References

[1] W. Olthuis, P. H. Veltink, and P. Bergveld, "The mechanical properties of the rubber elastic polymer polydimethylsiloxane for sensor applications," *Adv. Packag.*, vol. 7, pp. 145–147, 1997.

[2] M. Almasri, W. Zhang, A. Kine, Y. Chan, J. C. LaRue, and R. Nelson, "Tunable infrared filter based on elastic polymer springs," vol. 5770, pp. 190–198, 2005. [Online]. Available:

[3] A. A. S. Bhagat, P. Jothimuthu, and I. Papautsky, "Photodefinable polydimethylsiloxane (PDMS) for rapid lab-on-a-chip prototyping." *Lab Chip*, vol. 7, no. 9, pp. 1192–7, Sep. 2007. [Online]. Available:

[4] P. Jothimuthu, A. Carroll, A. A. S. Bhagat, G. Lin, J. E. Mark, and I. Papautsky, "Photodefinable PDMS thin films for microfabrication applications," *J. Micromechanics Microengineering*, vol. 19, no. 4, p. 45024, Apr. 2009. [Online]. Available:

[5] D. P. J. Cotton, a. Popel, I. M. Graz, and S. P. Lacour, "Photopatterning the mechanical properties of polydimethylsiloxane films," *J. Appl. Phys.*, vol. 109, no. 5, p. 54905, 2011. [Online]. Available:

[6] I. M. Graz, D. P. J. Cotton, A. Robinson, and S. P. Lacour, "Silicone substrate with in situ strain relief for stretchable thin-film transistors," *Appl. Phys. Lett.*, vol. 98, no. 12, p. 124101, 2011. [Online]. Available:

[7] Y. Sun, L.-T. Jiang, R. Okada, and J. Fu, "UV-modulated substrate rigidity for multiscale study of mechanoresponsive cellular behaviors." *Langmuir*, vol. 28, no. 29, pp. 10 789–96, Jul. 2012. [Online]. Available:

[8] A. Romeo and S. P. Lacour, "Concurrent photopatterning of elastic modulus and structures in photosensitive silicone elastomers," *Extrem. Mech. Lett.*, 2015. [Online]. Available:

[9] "a) M. Madou Fundamentals of Microfabrication and Nanotechnology; Third Edition ed.; CRC Press, 2011 b) Younan Xia,John A. Rogers,Kateri E. Paul,G. M. Whitesides Chemical Reviews 1999, 99, 1823." p. 2014, 2014.

[10] G. M. Whitesides, E. Ostuni, S. Takayama, X. Jiang, and D. E. Ingber, "Soft lithography in biology and biochemistry." *Annu. Rev. Biomed. Eng.*, vol. 3, pp. 335–373, Jan. 2001. [Online]. Available:

[11] Y. Xia and G. M. Whitesides, "Soft Lithography," *Annu. Rev. Mater. Sci.*, vol. 28, no. 1, pp. 153–184, Aug. 1998. [Online]. Available:

[12] J. Garra, T. Long, J. Currie, T. Schneider, R. White, and M. Paranjape, "Dry etching of polydimethylsiloxane for microfluidic systems," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 20, no. 3, p. 975, 2002. [Online]. Available:

[13] D. C. Duffy, J. C. McDonald, O. J. a. Schueller, and G. M. Whitesides, "Rapid prototyping of microfluidic systems in poly(dimethylsiloxane)," *Anal. Chem.*, vol. 70, no. 23, pp. 4974–4984, 1998.

[14] J.C. Lotters, W. Olthuis, P.H. Veltink and P. Bergveld, "The mechanical properties of the rubber elastic polymer polydimethylsiloxane for sensor applications," *J. Micromechanics Microengineering*, vol. 7, pp. 145–147, 1997.

[15] S. P. Desai, B. M. Taff, and J. Voldman, "A photopatternable silicone for biological applications." *Langmuir*, vol. 24, no. 2, pp. 575–581, Jan. 2008. [Online]. Available:

[16] "Dow Corning WL-5000 series Datasheet, Dow Corning, available at www.dowcorning.com."

[17] K. Tsougeni, a. Tserepi, and E. Gogolides, "Photosensitive poly(dimethylsiloxane) materials for microfluidic applications," *Microelectron. Eng.*, vol. 84, no. 5-8, pp. 1104–1108, May 2007. [Online]. Available:

[18] G. C. Lisensky, D. J. Campbell, K. J. Beckman, C. E. Calderon, P. W. Doolan, Rebecca M. Ottosen, and A. B. Ellis, "Replication and Compression of Surface Structures with Polydimethylsiloxane Elastomer," *J. Chem. Educ.*, vol. 76, no. 4, p. 537, 1999. [Online]. Available:

[19] "http://www.dowcorning.com."

[20] A. N. Gent, *Engineering with Rubber - How to Design Rubber Components (2nd edition)*, 2nd ed. Hanser Publishers, 2001.

[21] W. M. Moore, G. S. Hammond, and R. P. Foss, "Mechanisms of Photoreactions in Solutions. I. Reduction of Benzophenone by Benzhydrol," *J. Am. Chem. Soc.*, vol. 1068, no. 2, pp. 2789–2794, 1961.

[22] "D. E. Discher,P. Janmey,Y. L. Wang Science 2005, 310, 1139 b) B. D. Fairbanks,M. P. Schwartz,A. E. Halevi,C. R. Nuttelman,C. N. Bowman,K. S. Anseth Advanced Materials 2009, 21, 5005." *Science*, vol. 310, no. 5751, pp. 1139–43, Nov. 2005. [Online]. Available:

[23] C.-H. R. Kuo, J. Xian, J. D. Brenton, K. Franze, and E. Sivaniah, "Complex stiffness gradient substrates for studying mechanotactic cell migration." *Adv. Mater.*, vol. 24, no. 45, pp. 6059–64, Nov. 2012. [Online]. Available:

[24] A. Romeo, Q. Liu, Z. Suo, and S. P. Lacour, "Elastomeric substrates with embedded stiff platforms for stretchable electronics," *Appl. Phys. Lett.*, vol. 102, no. 13, p. 131904, 2013. [Online]. Available:

[25] A. Romeo, Y. Hofmeister, and S. P. Lacour, "Implementing MEMS technology for soft, (bio)electronics interfaces," vol. 9083, p. 90831F, Jun. 2014. [Online]. Available:

[26] D. J. Kang, J.-u. Park, and B.-s. Bae, "Single-step photopatterning of diffraction gratings in highly photosensitive hybrid sol-gel films," vol. 11, no. 10, pp. 3184–3187, 2003.

[27] J. Neumann, K. S. Wieking, and D. Kip, "Direct laser writing of surface reliefs in dry, self-developing photopolymer films." *Appl. Opt.*, vol. 38, no. 25, pp. 5418–21, Sep. 1999. [Online]. Available:

[28] W. Yu, X. Yuan, N. Ngo, W. Que, W. Cheong, and V. Koudriachov, "Single-step fabrication of continuous surface relief micro-optical elements in hybrid sol-gel glass by laser direct writing." *Opt. Express*, vol. 10, no. 10, pp. 443–8, May 2002. [Online]. Available:

[29] J.-U. Park, W.-S. Kim, and B.-S. Bae, "Photoinduced low refractive index in a photosensitive organicâinorganic hybrid material," *J. Mater. Chem.*, vol. 13, no. 4, pp. 738–741, Mar. 2003. [Online]. Available:

[30] T. Ubukata, Y. Moriya, and Y. Yokoyama, "Facile one-step photopatterning of polystyrene films," *Polym. J.*, vol. 44, no. 9, pp. 966–972, Mar. 2012. [Online]. Available:

[31] C. J. Kloxin, T. F. Scott, H. Y. Park, and C. N. Bowman, "Mechanophotopatterning on a photoresponsive elastomer." *Adv. Mater.*, vol. 23, no. 17, pp. 1977–81, May 2011. [Online]. Available:

[32] D. P. Nair, N. B. Cramer, T. F. Scott, C. N. Bowman, and R. Shandas, "Photopolymerized Thiol-Ene Systems as Shape Memory Polymers." *Polymer (Guildf).*, vol. 51, no. 19, pp. 4383–4389, Sep. 2010. [Online]. Available:

[33] T. F. Scott, A. D. Schneider, W. D. Cook, and C. N. Bowman, "Photoinduced Plasticity in Cross-Linked Polymers," vol. 1615, no. 2005, 2014.

[34] K. G. Yager and C. J. Barrett, "Photomechanical Surface Patterning in Azo-Polymer Materials," *Macromolecules*, vol. 39, no. 26, pp. 9320–9326, Dec. 2006. [Online]. Available:

5 Conclusion and outlook

5.1 Conclusion

In this thesis a simple and robust approach to design and manufacture versatile elastic substrates for stretchable electronic applications has been developed.

The substrate was engineered with the strain relief method combining rigid epoxy SU8 platforms embedded in a silicone matrix. Embedding and distributing SU8 platforms in a PDMS membrane results in a stretchable substrate with intrinsic stiff regions while providing a flat and uniform top surface. This planar but mechanically heterogeneous approach offers two main advantages if compared to the standard *hard-on-soft* pixelated design: (i) electronic materials can be directly processed onto it, and (ii) it prevents issues associated with steep and sharp step coverage.

The proposed strain relief method is efficient to ensure brittle materials are not stretched above their fracture strains and it can be tuned to develop a low strain profile across the elastic thin film interconnects running in-between the rigid elastomeric regions and to maximize the safe area available for the active devices.

The geometrical configuration of the locally reinforced elastomer can be accurately optimized. Using experimental as well as modeling data two geometrical parameter values were selected: platform/elastomer thicknesses ratio (t/h) = 0.5, as good compromise between the penetration depth and the strain concentration at platform edge; and spacing/diameter ratio (S/D) = 4, as good compromise between the far field strain and the spatial resolution of the safe areas.

It was demonstrated that grading the mechanical compliance at the *stiff-to-soft* interface enables to completely suppress the strain localization at this interface, as well as, to maximize the safe areas without compromising the spatial resolution. Mechanical grading can be achieved in two different ways: (i) shaping the SU8 polymer into truncated cones, and (ii) mechanically grading the elastic modulus of the elastomer surrounding the SU8 platforms. Both methods make use of a graded binary photolithographic mask. The first approach implies a more complicated process flow and further improvements to achieve the desired size and shape are needed. For example, the gradient of the greyscale mask should be prepared taking into consideration the logarithmic relation between the photoresist thickness and the UV dose. The second approach, does not require complicated change in the process flow, moreover it allows for reducing the far field strain. Therefore, grading the mechanical modulus of the P-PDMS provides the most promising mechanical design for engineered substrate.

Further reduction of the far field strain can be achieved combining optimized layout of the

embedded platforms with stiffer P-PDMS meshes. It was demonstrated that hexagonal and rhomboidal layouts with non-exposed P-PDMS along the interconnection paths allow for reducing the strain along the elastic conductors interconnecting electronic devices above the safe areas.
Adjustment of the top strain distribution under large applied deformation is of extreme importance for the long-term performance of the stretchable circuit. In the proposed approach, customized elastomeric substrates can be achieved simply by optimizing the local stiffness of the substrate as well as the embedded platforms geometry and layout, without including any special device designs, such as wavy or buckled configurations. Furthermore, the engineered stretchable substrate is prepared on a flat carrier that can then be handled similarly to standard microelectronics wafers yet provide the stretchability required once released from the carrier.

Compatibility of the proposed engineered substrate with standard, additive thin-film processing was demonstrated.
Metal oxide based TFTs were directly patterned on top of the rigid zones of the engineered substrate, using only planar, low temperature (<50°C) and dry fabrication steps.
Direct integration of active device onto stretchable substrate allows for low-cost, simple and straightforward fabrication processing. However this technique limits the materials choice due to the minimal temperature processing imposed by the soft substrate. In this work, an hybrid dielectric stack composed by Parylene and Aluminum oxide was used and optimized.
IGZO TFT with the hybrid dielectric stack was released from the rigid carrier wafer and stretched up to 20 % of strain. After release from the carrier the transistor showed typical transistor-like behavior, with a μ_{sat} of 2.4 $cm^2V^{-1}s^{-1}$, a V_T of 4.1 V, I_{on}/I_{off} ratio of $\sim 10^3$ and a $S.S$ of 1.4 V/dec. The engineered stretchable substrate enables transistor to sustain large applied strain without electrical degradation or mechanical fracture.
The proposed strain relief method enables for engineered stretchable substrate with planar and uniform top surface, onto which electronic device can be directly patterned, yet providing the mechanical requirements to host and protect fragile device's materials when large deformations are applied. The potential of patternable mechanical reinforcement of elastomer substrate with thin-film technology was demonstrated but this approach may also be compatible with transfer-printing and lamination of electronic circuits and component.

Moreover concurrent mechanical and structural photopatterning of photosensitive silicone was discovered.
To date, photosensitive silicones have mainly been implemented in soft lithography or to locally modulate the elasticity of the elastomer.
In this thesis it was demonstrated that patterning of structures and elastic modulus of the elastomer may be achieved simultaneously, solely by UV exposure through standard photolithography mask. P-PDMS tensile modulus can be adjusted in the 0.79-3.2 MPa range by decreasing the UV exposure dose and prepolymer/curing agent ratio. At the same time, de-

pression depth increased with the increasing of the width and the spacing of the non-exposed patterns till reaching a plateau. Maximum depth of of 55 μm and edge bumps of 10 μm was achieved with rectangular patterns with 1.6 mm in width and 5 mm in depth, within contiguous P-PDMS film with prepolymer/ curing agent ratio = 5:1.
The described process eliminates lithography wet development step, nor mechanical preloading of the elastomer, therefore offers a new, simple technique for PDMS microstructuring. Single-step photopatterned P-PDMS was used to form mold-free microfluidic channels, and engineered substrates required for the hybrid integration of stretchable circuits.
Concurrent photopatterning of elastic modulus and structures in photosensitive silicone elastomers provides a simple and low cost approach to create complex topographical features and shape as well as to define mechanical stiffness gradient within the elastomer. This combination of properties opens possibilities in a wide range of application in soft micro-electromechanical systems MEMS, microfluidics and stretchable electronics allowing for rapid prototyping and new mechanical design, only requiring a single material, a casting step and an UV exposure.

5.2 Outlook

The results achieved within this thesis lead to future objectives and open new possibilities to engineered mechanically heterogeneous substrate for the fabrication stretchable circuits.

Stretchable engineered substrate has proven to be compatible with thin-film fabrication techniques. IGZO TFTs can be patterned directly onto rigid regions of the elastomeric substrate and sustain large strain without electrical or mechanical degradation. However, the developed stretchable IGZO TFTs showed poor electical performance if compared to that of their counterparts on flexible plastic foil. Further improvements are therefore required.

- A particular area of concern is the semiconductor-dielectric interface which mostly determine the TFT performance. In this thesis we presented IGZO TFTs with an inorganic/organic active interface which are commonly regarded to form poor interfaces. Most of the fabricated transistors have shown a poor semiconductor-dielectric interface with drain-to-source currents that could not be gate-controlled. A better understanding is needed to mitigate these issues for the reproducible fabrication of oxide TFTs. For example, understanding and controlling the presence of interface states will help in producing oxide TFTs with high electrical performance.
  Moreover the use of high-k dielectrics can increase the gate capacitance and, depending on the deposition method, also improve the interface between IGZO and gate insulator leading to a reduced interface trap density. Therefore adding a thin layer of high-k dilectric, such as Al_xO_y, between the Parylene dielectric and the IGZO semiconductor could improve this interface, and therefore the performance of the transistor. In Chapter 3 a possible solution to this problem was proposed to integrate a thin oxide layer at the IGZO-Parylene interface without compromising the materials quality. Inverting

the TFT structure, therefore using a bottom gate staggered structure, a thin layer of Aluminum can be sputtered above the IGZO layer and oxidized in O_2 plasma before the Parylene deposition. However, this solution requires further studies on the effect of the O_2 plasma on the electrical performance of the IGZO semiconductor

- Systematic studies on the semiconductor deposition should be performed since electrical characteristics of IGZO films depend primarily on the oxygen partial pressure during sputtering but also on the history of the sputter target. Different oxygen partial pressure could be tested to optimize the semiconductor performances. Moreover, a dedicated sputtering machine, not shared with other users, is strongly suggest to improve the reproducibility of the fabrication

- This thesis does not directly address device stability, but stability is already an active area of research and researchers have suggested way to improve device stability such as encapsulation/passivation, or modifying film stoichiometry and/or composition. For example, encapsulation or passivation layer for the TFTs is highly recommended to avoid electrical degradation of the device during the releasing step. Encapsulation of the TFTs could be done by bonding onto the engineered substrate a thin PDMS membrane with patterned openings in order to access source, drain and gate contacts

- Repeated mechanical loading should also be performed, on both channel length and width directions, to asses if the device operates stably, even after n cycles stretching. Moreover it would be nice to investigate the maximum strain that the stretchable device can sustain before fracturing

The proposed approach is not limited to IGZO TFTs and should be easily transferred to other thin-film devices organic or inorganic semiconductors. This opens the possibility for more complex architectures. Stretchable inverters or ring oscillators can be designed by combining p- and n-type semiconductors.
Furthermore, active devices can be integrated with stretchable sensors array onto the optimized engineered stretchable substrate in order to achieve an integrated stretchable active matrix. For example, TFTs could be integrated with strain and pressure sensors to convert their output into a μA current, which could then be applied for nerve stimulation for prosthetic skin applications.

Moreover, concurrent mechanical and structural photopatterning of photosensitive silicone opens possibilities in a wide range of application icludign soft bio-interfaces. Therefore biocompatibility of the photopattenred P-PDMS should be tested and compared with the conventional that of conventional PDMS substrates.

Abbreviations

Al	Aluminum
AlO_x	Aluminum Oxide
A_s	Safe area
Au	Gold
CVD	Chemical Vapour Deposition
Cr	Chromium
D	Rigid platforms diameter
DIC	Digital Image Correlation
E	Young's Modulus
FEM	Finite Elements Modeling
FET	Field Effect Transistor
g	PDMS above the rigid platform thickness
h	Rigid platforms thickness
I_D	Drain current
I_{on}/I_{off}	On-off current ratio
IGZO	Indium Gallium Zinc Oxide
L	Length
p	Penetration depth
P_{O_2}	Oxygen Pressure
PAA	Polyacrylic Acid
PDMS	Polydimethylisoxsane
P-PDMS	Photosensitive PDMS
PI	Polyimide
PSS	Poly 4-Styrenesulfonic Acid
R	Prepolymer: curing agent ratio
t	PDMS thickness
Ti	Titanium
TFT	IThin Film Transistor
S	Rigid platforms spacing

SEM	Scanning Electron Microscope l
V_D	Drain voltage
V_G	Gate voltage
Threshold voltage	
W	Width

Scientific achievements

Journal publications

A. Romeo, Q. Liu, Z. Suo, S.P. Lacour, "Elastomeric substrates with embedded stiff platforms for stretchable electronics", *Applied Physics Letters,* April 2013.

A. Romeo and S. P. Lacour, "Concurrent photopatterning of elastic modulus and structures in photosensitive silicone elastomers", *Extreme Mechanic Letters*, 2015.

Conference publications

A. Romeo, Y. Hofmeister, S.P. Lacour, "Implementing MEMS technology for soft, (bio)electronics inter- faces", *proc. of SPIE DSS, Baltimore*,USA,May 2014.

A. Romeo, S. P. Lacour , "Stretchable metal oxide thin film transistors on engineered substrate for electronic skin applications", *IEEE-EMBC, Engineering in Medicine and Biology Society*, 2015.

Conference talks

A. Romeo, Q. Liu, Z. Suo, S. P. Lacour, 'Design Guidelines for Stretchable Thin-film Electronics ", *MRSspring* , San Francisco, USA, April 2013

A. Romeo and S. P. Lacour., "Stretchable metal oxide thin film transistors on engineered substrate for electronic skin applications", *IEEE-EMBC* , Milan, Italy, August 2015

Conference posters

S. P. Lacour, D. Cotton, I. Graz, and **A. Romeo**, "A technological route to produce stretchable, integrated thin film transistor circuits", *FlexStretch, Berlin*, November 2011

A. Romeo and S.P. Lacour, "Single Step Patterning of Soft Silicone Microstructures ", *MRSspring*, San Francisco, USA, April 2014

A. Romeo and S.P. Lacour, "Patterning of local mechanical stiffness in photosensitive silicone membrane", *MNE Conference*, Lausanne, September 2014

Curriculum Vitae

Name Alessia Romeo
Date of birth 26th of September 1986
Nationality Italian

Education

Jul 2011-Current **PhD in Stretchable Microelectronic,** EPFL, Lausanne, SWITZERLAND
Lab of Soft Bioelectronic Interfaces, LSBI
Thesis director: Prof. Stéphanie Lacour

Sep 2008-Mar 2011 **Master Degree in Biomedical Engineering** PoliMi, Milan, ITALY
GPA: *Grade110/110*

Aug 2009-Feb2010 **Erasmus exchange program** TUT, Tampere, FINLAND

Research and Work Experience

Jul 2011-current **Research Assistant at EPFL**, Switzerland
- Involved in scientific tasks for the ERC project "E-SKIN"
- Design, fabrication, mechanical optimization and characterization of stretchable inorganic TFTs systems
- Fully independent work in a Class 100 cleanroom (https://cmi.epfl.ch/)
- Lecturer and project supervisor for M.Sc. students
- Training of students and collaborators
- Authored 9 scientific contributions in international conferences and journals

Jun 2010-Mar 2011 **Internship at Philips Research** - HTC, Netherlands
- Development of substrate transfer technology for stretchable electronic applications
- Achieved full independence in cleanroom work *(MiPlaza*)

Feb 2010-Jun 2010 **Electronic Technologies and Biosensors Laboratory**, PoliMi, Italy
- Design, prototyping and characterization of a wearable, low-power, wireless EKG system for newborn monitoring at S. Gerardo Hospital (*Monza, IT*)
- PCB design and assembling: analogic front-end, PIC, rechargeable battery, PIC, Xbee
- Development of PIC firmware
- Development of LabView user interface for monitoring the EKG acquired data

Sep 2007-Feb 2008 **Internship at Department of Human Morphology**, UniMi**,** Italy
- Analysis of human motion through optoelectronic systems BTS Smart

Awards and Scholarship

- **Best Poster Award** - EDMI research-day, EPFL, Dec 2012
- **MENSA member**, the high IQ society, Since 2008 *http://mensa.org*
- **Student at *Collegio di Milano***, inter-university campus of excellence, Sep2007-Jul2009 http://www.collegiodimilano.it/web/en/home

Technical skills

- **Cleanroom equipment and electrical characterization**

Soft polymers microfabrication, flexible and stretchable film, thin film transistor processing, photo-lithography on different substrates, chemical vapor deposition (CVD), atomic layer deposition (ALD), dry/wet etching, e-beam/thermal evaporation, sputtering, lift-off, profilometer, scanning electron microscopy (SEM), electro-mechanical material characterization, semiconductor device analyzer

- **Design and modeling**

CleWin, Solid Works, Autocad, Cadence

- **Programming languages, frameworks and tools**

MATLAB, C, C++, LabView, Latex , OriginPro, Adobe Photoshop, Adobe Illustrator, Image J, Mendeley, MS Office, MS Windows, Linux, Mac OS X, iOS

Activities and Volunteering

2011-current	**Active member of "Oltre Food for Brains" ONLUS** • Association operating in Tanzania with the mission of sustaining knowledge development and access to education • Organization of fund-raising and dissemination events • Volunteering work at Ismani Cultural Center	Milan, ITALY Ismani, TANZANIA
2011-2013	**Vice-president of the association "ITALaus"** • Association for the promotion of the Italian culture in Lausanne • Management of several projects and their budgets	Lausanne, SWITZERLAND
2011-2012	**Actor in the theater company "Pourquoi Pas?"** • Theater in Italian language with performances in all Switzerland	Lausanne, SWITZERLAND
2010-2011	**Event specialist at Philips Intern Committee** • Association within Philips Research to provide an environment for professional training, integration and students welcoming • Management and promotion of several events	HTC, Eindhoven, NEDERLANDS

Languages

Italian	**English**	**French**
Mother tongue	Very fluent	Fluent