

3.6 GHz CMOS Ring Oscillator with Low Tune Voltage Sensitivity and Temperature Compensation

Hasene Gulperi Ozsema

Ecole Polytechnique Fédérale de
Lausanne, Lausanne, Switzerland
hasene.ozsema@epfl.ch

Tugba Demirci

Ecole Polytechnique Fédérale de
Lausanne, Lausanne, Switzerland
tugba.demirci@epfl.ch

Yusuf Leblebici

Ecole Polytechnique Fédérale de
Lausanne, Lausanne, Switzerland
yusuf.leblebici@epfl.ch

Abstract—In this paper we present the design of a temperature compensated low-tune-voltage-sensitive CMOS ring oscillator in 40nm standard CMOS technology. The oscillator has an overall frequency range from 3.1 GHz to 3.6 GHz. The effect of temperature variations on the frequency span has been tuned out by an IPTAT (inversely proportional to absolute temperature) current reference. In this work, using a coarse-fine tuning mechanism lowers the tune range sensitivity of the oscillator, which is usually represented as K_{VCO} . The achieved K_{VCO} is around 490 MHz/V with 400 mV tune voltage sweep. The area and the power consumption of the ring oscillator are 0.0056 mm² and 0.9 mW.

I. INTRODUCTION

In integrated circuits, the clock generators have to fulfil various requirements such as achieving a defined frequency range or producing a low noise signal depending on the application. *Phase-locked-loop (PLL)* circuits are widely used in clock generation, and the *voltage-controlled oscillator (VCO)* is a critical sub-block of PLL circuits. Two main oscillator topologies used as VCO are LC oscillator topology and ring oscillator topology. Although ring oscillators have poor phase noise characteristics, they have the advantages of simplicity, availability of multiphase outputs, compactness and wide-range output frequency compared to LC oscillators. Therefore, they are preferred in a number of applications with relaxed noise requirements (e.g. time-interleaved applications) [1], [2].

According to *International Roadmap for Semiconductors (ITRS)*, technology scaling continues along with supply voltage downscaling [3]. Due to reduced supply voltages, circuits designed in modern CMOS technologies have to operate with low voltage swings. This requirement poses a challenge for ring oscillator design, since the frequency of the ring oscillator is controlled by a voltage signal input. Achieving a wide output frequency range with a low swing control voltage degrades the tuning sensitivity of the oscillator, which is a crucial parameter that directly affects the noise performance of the ring oscillators. So, it is essential to keep the tuning sensitivity as small as possible.

In the literature, different methods are proposed to lower the oscillator gain. In [4], a two-step control mechanism is used. In this method, the frequency is firstly set via coarse tuning. Then, the frequency is further adjusted by using fine-tuning. Another method [5] uses a digitally controlled oscillator. In this technique, the frequency is tuned by switching in and out resistors. Coarse-fine tuning mechanism is more

preferable as it avoids switching that may cause instantaneous spikes in the output frequency. On the other hand, both of the methods do not clearly address how they correct the frequency fluctuations caused by temperature variations.

In this work, we present an 8-phase ring oscillator solution in 40nm CMOS technology that utilises a coarse-fine tuning mechanism together with an IPTAT current reference to lower the tune sensitivity. The IPTAT current reference compensates the effects of the temperature variation by adjusting the bias current of the oscillator according to the temperature. The resulting design achieves a wide tuning range, high oscillation frequency that is between 3.1 GHz and 3.6 GHz, and a K_{VCO} value of 490 MHz/V which could be very suitable for a wide range of high-performance applications that require small silicon area.

In Section II, the architecture of the 8-phase ring oscillator and its delay cell are explained. Section III shows the control technique against temperature variations. Section IV is about the designed frequency divider and its building blocks. In Section V, the simulation results are presented. Finally, in Section VI concluding remarks will be given.

II. RING OSCILLATOR DESIGN

The four-stage ring oscillator shown in Fig. 1 is the basic architecture of this work. The delay stages of this oscillator are differential ended, as differential cell based design allows to achieve a better noise performance. In literature, various topologies have been proposed for the design of differential delay cells. Some of them can be found in [6]–[8].

The used cell topology for this design is also represented in Fig. 1. This structure is called as delay stage with adaptive load. It functions by switching differential pair transistors ($M_1 - M_2$), and an active load ($M_3 - M_6$) controls the output swing. The cell has both coarse-tuning and fine-tuning mechanisms. The coarse tuning is controlled by a cascoded current source ($M_8 - M_{11}$). The cascoded architecture is preferred to suppress the effect of channel length modulation and to reduce the copying error in the current mirror. In our design, the coarse-tune current is generated by a 2-bit DAC, and this current is set at the start-up during the calibration. On the other hand, the fine-tuning is achieved by combining a current source (M_{12}) and a negative resistance latch ($M_{13} - M_{14}$). The voltage of the fine-tuning mechanism could be adjusted by the regular operation of a PLL. Thanks to this two-step tuning technique, it is possible to have smaller oscillator sensitivity.

Differential buffers have been placed at the output of each delay cell. These buffers provide equal loading on all outputs

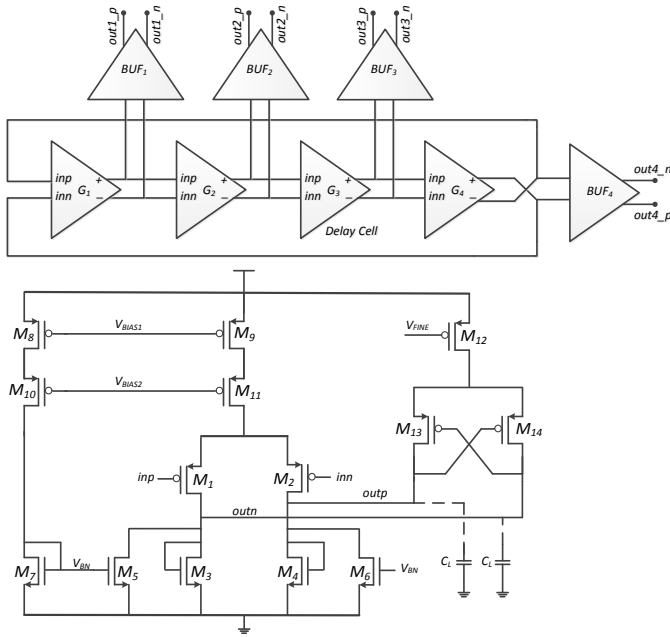


Fig. 1. (Top) Four-stage ring oscillator topology, and (bottom) the schematic of the delay cell

and isolate the ring oscillator from the rest of the circuit. The architecture of the buffers are the same as the delay cells, since the polarities of the inputs and outputs can be changed at no cost in differential gates. But, the buffers don't contain the fine-tuning mechanism. The delay of each cell is governed by the following formula:

$$t_{del} = \frac{V_{SW}C_L}{I_{BIAS}}, \quad (1)$$

where V_{SW} is the output voltage swing, C_L is the output load capacitance, and I_{BIAS} is the total bias current of the cell. Then, the frequency of the four-stage (8-phase) oscillator would be:

$$f_{osc} = \frac{1}{8t_{del}}. \quad (2)$$

The frequency of the oscillator can be tuned by varying the parameters given in Eq. (1). Bias current variation is the preferred method due to its simple implementation: When the bias current is increased, the circuit oscillates faster. However, the increase in the oscillation frequency saturates after a certain point. This limitation occurs due to two reasons. The first reason is that it is not possible to increase the current of the cells without increasing the dimensions of the differential pair, which brings additional load capacitance that counteracts the effect of the bias current increase. Secondly, the channel length of the differential pair transistors can not always be chosen as equal to the minimum value allowed by the technology. Larger channel length values are necessary to keep the variation of the operating point with respect to the overdrive voltage at the minimum. Otherwise, the circuit may become unstable.

Our 4-stage differential ring oscillator is designed based on the mentioned principles. The frequency tuning curves of this oscillator that are obtained from the post-layout simulations

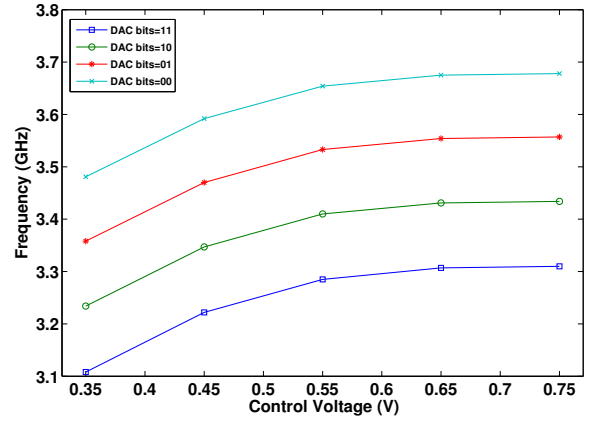


Fig. 2. Simulated tuning ranges of the oscillator versus fine-tune voltage at different DAC configurations

are represented in Fig. 2. According to the graph, the available control voltage swing is between 350 mV and 750 mV. When the borders of the curves are examined, the tuning range of the oscillator is found to be from 3.1 GHz to 3.6 GHz, with K_{VCO} of 490 MHz/V. If we omit the coarse-tuning control and try to achieve the same tuning range with fine-tuning only (keeping the control voltage swing the same), the K_{VCO} would be around 1.25 GHz/V, which is simply too high to be practical. More than a factor of x2 improvement in the sensitivity of the oscillator proves the usefulness of the two-step tuning approach.

III. TEMPERATURE COMPENSATION

Variation of the temperature can lead to a significant drift in the frequency of the oscillator. This drift may drive the oscillator out of the expected operating range. A proper compensation technique is necessary to avoid this problem.

The analyses on our ring oscillator showed that its output frequency is directly proportional to the temperature without any compensation. We found the main reason of the frequency increase to be the decreasing output swing at high temperatures. As expressed in Eq. (1), smaller output voltage swing means smaller gate delay, which in the end increases the oscillation frequency. A simple way to overcome the effects of the temperature variation would be to decrease the bias current of the oscillator as the temperature increases. This idea can be realised by biasing the oscillator by an IPTAT current reference.

The diagram in Fig. 3 represents our temperature compensation structure. The coarse current of the oscillator is generated by an IPTAT current reference and a 2-bit DAC. In order to have well-defined operating points for the current source transistors, the switches of the DAC are placed between the supply and the current source transistors. Such current references can be designed in various ways [9]. The chosen topology employs a bipolar transistor whose base-emitter voltage has a negative temperature coefficient. With $V_{BE} \approx 750mV$ and $T = 300^{\circ}K$, this temperature coefficient is calculated as [10]

$$\frac{\partial V_{BE}}{\partial T} \approx -1.5mV/^{\circ}K. \quad (3)$$

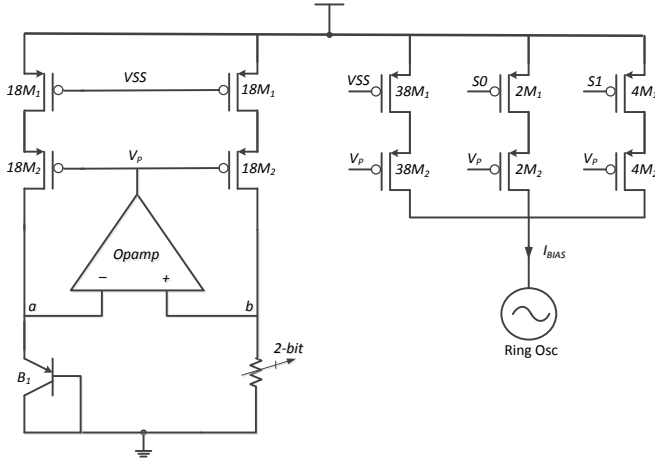


Fig. 3. Circuit schematic of the temperature compensation block and the 2-bit DAC.

Then, the IPTAT voltage is forced across a resistor by an operational amplifier. This amplifier keeps the nodes "a" and "b" at the same potential, hence the IPTAT current is generated. The temperature dependency of the resistor affects the generated current, as well. Here, the chosen resistor has a considerably smaller negative temperature coefficient than the BJT. Furthermore, this topology is suitable for low supply voltage design as it does not contain any stacked transistors. Finally, the change of bias current with respect to temperature at different DAC configurations is shown in Fig. 4.

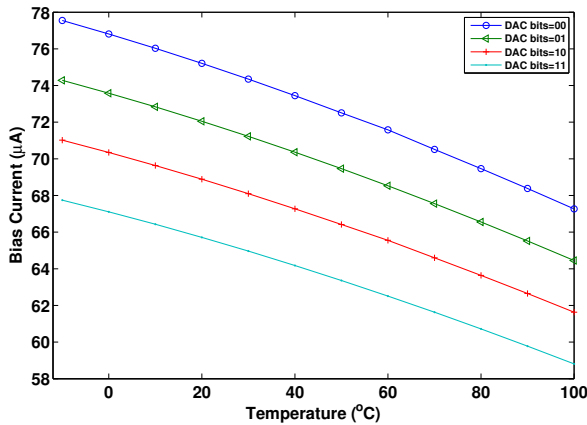


Fig. 4. Bias current variation versus temperature for different DAC configurations

The accuracy of the current reference depends on the matching between the designed and fabricated values of the resistor. In modern technologies, integrated resistors may vary on the order of 10% to 20%. This variation will translate to a change in the bias current, which can shift the frequency tuning curves. However, if the shifts are too large, we might lose continuity of the tuning range. In order to avoid this situation, a digitally controlled resistor is designed. The proper resistor value should be set at start-up based on the initial calibration results.

IV. FREQUENCY DIVIDER

Due to the limitations of the measurement equipment, it is necessary to lower the frequency of the output signals of the ring oscillator. Therefore, the multi-phase outputs of the ring oscillator are followed by dividers and buffers. The divider and its building blocks are shown in Fig. 5. The D flip-flops (DFF) inside the divide-by-2 blocks are constructed with saturated-type latches. This latch topology has been constructed based on the work explained in [7]. It is named as saturated, since the outputs of the gates designed with this idea can swing from rail to rail. This architecture includes a pair of cross-coupled PMOS ($M_7 - M_8$) transistors providing positive feedback, which is helpful to sharpen the transition edges of the output signal and to increase the speed of the gate. The buffers at the outputs of the dividers are also built as saturated-type for achieving good signal shape with rail-to-rail swing. Another advantage of this topology is that it can produce inverting and non-inverting outputs. The input and output waveforms of the divider are shown in Fig. 6.

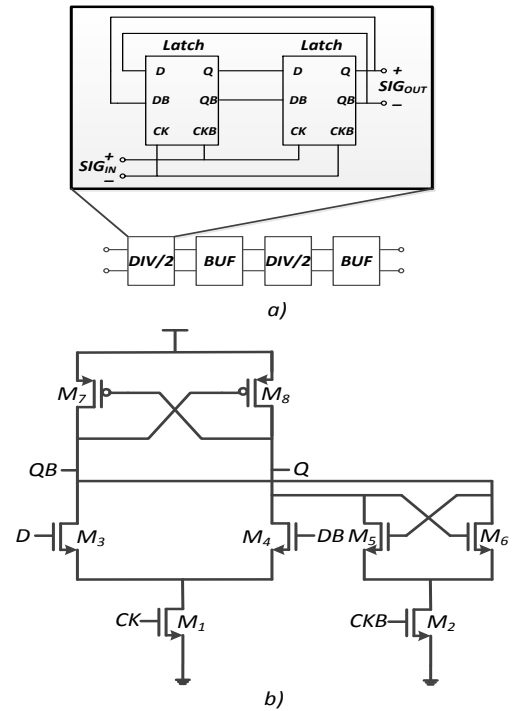


Fig. 5. a) Frequency divider and its building blocks b) Schematic of the saturated-type latch

V. SIMULATION RESULTS

The ring oscillator is designed in 40 nm CMOS technology from Taiwan Semiconductor Manufacturing Company (TSMC). The layout photo is shown in Fig. 7. The layout occupies a silicon area of 0.0056 mm^2 .

The performance of the ring oscillator is summarised in Table I. According to the post-layout simulations, the ring oscillator has a continuous tuning range from 3.1 GHz to 3.6 GHz; and it consumes 0.9 mW power at 0.95-V supply voltage.

The effects of temperature variation has been compen-

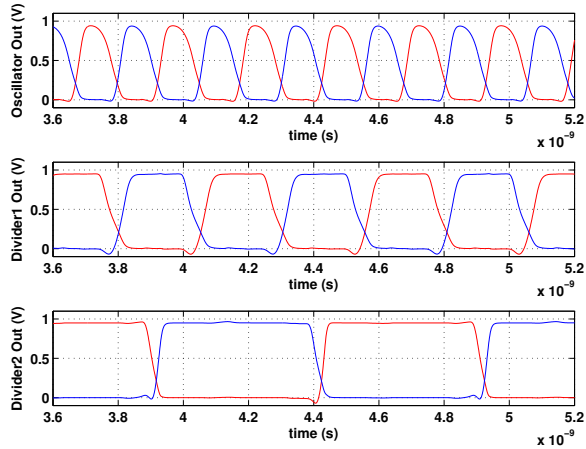


Fig. 6. Simulated input and output waveforms of the divider unit

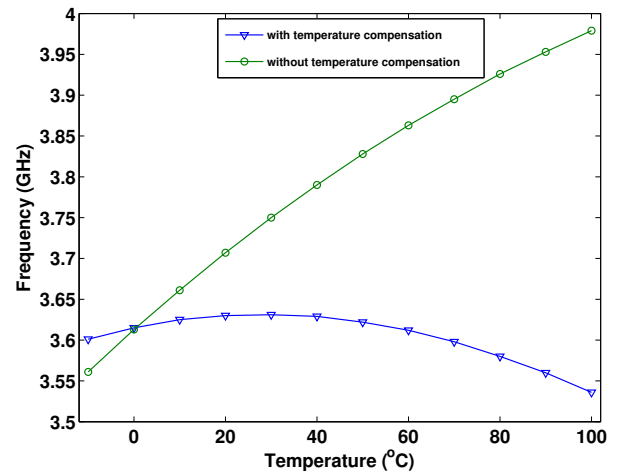


Fig. 8. Simulated performance of the ring oscillator at the maximum output frequency with and without temperature compensation

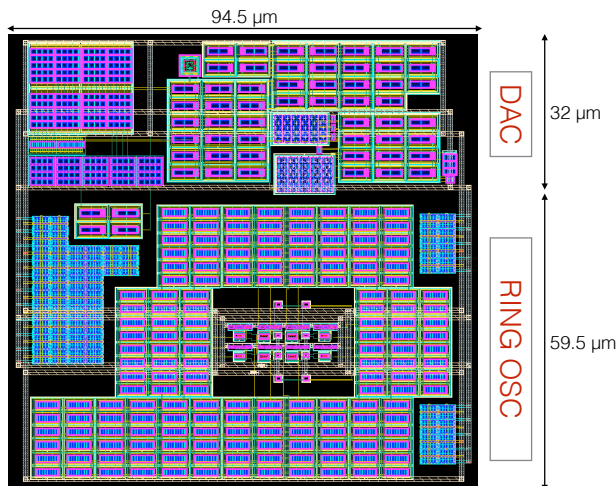


Fig. 7. Layout photograph of the ring oscillator and the DAC

sated by an IPTAT current reference. Fig. 8 illustrates the performance of the ring oscillator at the maximum output frequency with and without temperature compensation. The temperature is swept from $-10\text{ }^{\circ}\text{C}$ to $100\text{ }^{\circ}\text{C}$. Without any temperature compensation mechanism, the frequency deviates significantly from the expected value. It is seen that the presented temperature compensation technique is able to keep the output frequency change due to the temperature variations in an acceptable range.

TABLE I. SUMMARY OF SIMULATED RING OSCILLATOR PERFORMANCE

Technology	40 nm CMOS
Power supply	0.95 V
Frequency Range	3.1-3.6 GHz
K_{VCO}	490 MHz/V
Power Consumption	0.9 mW
Area	0.0056 mm^2

VI. CONCLUSION

In this paper, a multi-phase temperature compensated low-tune-voltage-sensitive CMOS ring oscillator has been presented. The design could be very suitable for time-interleaved applications that require small silicon area. The ring oscillator uses coarse-fine tuning technique to lower the sensitivity and employs an IPTAT current reference biasing to compensate the effects of temperature variation. Simulation results from a 40 nm CMOS design indicates that it can achieve a tuning range of 15%, with 0.9 mW power consumption at 0.95-V supply voltage.

REFERENCES

- [1] L. Wu and W. C. Black Jr, "A low-jitter skew-calibrated multi-phase clock generator for time-interleaved applications," in *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*. IEEE, 2001, pp. 396–397.
- [2] A. H.-Y. Tan and G.-Y. Wei, "Adaptive-bandwidth mixing pll/dll based multi-phase clock generator for optimal jitter performance," in *Custom Integrated Circuits Conference, 2006. CICC'06. IEEE*. IEEE, 2006, pp. 749–752.
- [3] International roadmap for semiconductors (itrs) 2009 edition. [Online]. Available: <http://www.itrs.net/Links/2009ITRS/Home2009.htm>
- [4] B. Ghafari, L. Koushaei, and F. Goodarzi, "An ultra low power and small size pll for wearable and implantable medical sensors," in *Consumer Communications and Networking Conference (CCNC), 2012 IEEE*. IEEE, 2012, pp. 409–412.
- [5] B. Fahs, W. Y. Ali-Ahmad, and P. Gamand, "A two-stage ring oscillator in 0.13-cmos for uwb impulse radio," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, no. 5, pp. 1074–1082, 2009.
- [6] J. G. Maneatis and M. A. Horowitz, "Precise delay generation using coupled oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 28, no. 12, pp. 1273–1282, 1993.
- [7] C.-H. Park and B. Kim, "A low-noise, 900-mhz vco in 0.6- μm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 5, pp. 586–591, 1999.
- [8] D. Z. Turker, S. P. Khatri, and E. Sánchez-Sinencio, "A dcvs1 delay cell for fast low power frequency synthesis applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, no. 6, pp. 1225–1238, 2011.
- [9] P. E. Allen and D. R. Holberg, *CMOS analog circuit design*. Oxford Univ. Press, 2002.
- [10] R. Behzad, "Design of analog cmos integrated circuits," *International Edition*, 2001.