Polarity Control at Runtime: from Circuit Concept to Device Fabrication

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PAR

Michele DE MARCHI

acceptée sur proposition du jury:

Prof. C. Guiducci, présidente du jury
Prof. G. De Micheli, directeur de thèse
Prof. S. Mitra, rapporteur
Dr W. Weber, rapporteur
Prof. Y. Leblebici, rapporteur

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Abstract

Semiconductor device research for digital circuit design is currently facing increasing challenges to enhance miniaturization and performance. A huge economic push and the interest in novel applications are stimulating the development of new pathways to overcome physical limitations affecting conventional CMOS technology.

Here, we propose a novel Schottky barrier device concept based on electrostatic polarity control. Specifically, this device can behave as p- or n-type by simply changing an electric input bias. This device combines *More-than-Moore* and *Beyond CMOS* elements to create an efficient technology with a viable path to *Very Large Scale Integration* (VLSI). This thesis proposes a device/circuit/architecture co-optimization methodology, where aspects of device technology to logic circuit and system design are considered.

At device level, a full CMOS compatible fabrication process is presented. In particular, devices are demonstrated using vertically stacked, top-down fabricated silicon nanowires with gate-all-around electrode geometry. Source and drain contacts are implemented using nickel silicide to provide quasi-symmetric conduction of either electrons or holes, depending on the mode of operation. Electrical measurements confirm excellent performance, showing $I_{on}/I_{off} > 10^7$ and subthreshold slopes approaching the thermal limit, $SS \approx 60\,\text{mV/dec}$ ($\approx 63\,\text{mV/dec}$) for n(p)-type operation in the same physical device. Moreover, the shown devices behave as p-type for a polarization bias (polarity gate voltage, V_{pg}) of 0 V, and n-type for a $V_{pg} \approx 1\,\text{V}$, confirming their compatibility with multi-level static logic circuit design.

At logic gate level, two- and four-transistor logic gates are fabricated and tested. In particular, the first fully functional, two-transistor XOR logic gate is demonstrated through electrical characterization, confirming that polarity control can enable more compact logic gate design with respect to conventional CMOS. Furthermore, we show for the first time fabricated four-transistors logic gates that can be reconfigured as NAND or XOR only depending on their external connectivity. In this case, logic gates with full swing output range are experimentally demonstrated. Finally, single device and mixed-mode TCAD simulation results show that lower V_{th} and more optimized polarization ranges can be expected in scaled devices implementing strain or high-κ technologies.

At circuit and system level, a full semi-custom logic circuit design tool flow was defined and configured. Using this flow, novel logic libraries based on standard cells or regular gate fabrics were compared with standard CMOS. In this respect, results were shown in comparison to CMOS, including a 40% normalized area-delay product reduction for the analyzed standard cell libraries, and improvements of over 2× in terms of normalized delay for regular *Controlled*

Abstract

Polarity (CP)-based cells in the context of Structured ASICs. These results, in turn, confirm the interest in further developing and optimizing CP devices, as promising candidates for future digital circuit technology.

Key words: nanotechnology, emerging technologies, silicon nanowires, Schottky barrier, logic design, multi-level synthesis, gate-all-around, polarity control, beyond CMOS, XOR, device fabrication.

Sommario

L'attuale ricerca sul progetto di circuiti digitali sta incontrando crescenti difficoltà nel tentativo di migliorare prestazioni e miniaturizzazione dei moderni dispositivi a semiconduttore. Una fortissima spinta economica e l'interesse in nuove applicazioni stanno stimolando lo sviluppo verso nuove direzioni di ricerca per superare le limitazioni fisiche che caratterizzano la tecnologia CMOS standard.

In questa tesi consideriamo un nuovo concetto di dispositivo, basato sul controllo elettrostatico della polarità, che consiste in un dispositivo a barriera Schottky che si può configurare elettostaticamente per operare come *tipo n* o *p*. Questo dispositivo combina elementi *More-than-Moore* e *Beyond CMOS* per creare una tecnologia efficiente e con una visione pratica per l'integrazione su larga scala (*Very Large Scale Integration* o VLSI). Qui, proponiamo una metodologia di co-ottimizzazione tra i livelli di dispositivo/circuito/architettura, dove consideriamo aspetti che vanno dalla tecnologia dei dispositivi, al design di circuiti e sistemi.

A livello di dispositivo, presentiamo un processo di fabbricazione completo e compatibile con i processi CMOS standard. In particolare, dimostriamo dispositivi che utilizzano canali composti da nanofili (*nanowire*) di silicio impilati, fabbricati con una metodologia *top-down* e circondati da elettrodi *gate-all-around* per ottenere un'elettrostatica ottimale. I contatti di *Source* e *Drain* sono implementati usando siliciuro di nichel per garantire una conduzione quasi simmetrica di elettroni o lacune a seconda della modalità di conduzione selezionata. Le misure elettriche confermano prestazioni eccellenti, dimostrando $I_{on}/I_{off} > 10^7$ e *subthreshold slope* vicine al limite termico $SS \approx 60\,\text{mV/dec}$ e $\approx 63\,\text{mV/dec}$ rispettivamente nelle modalità *tipo n* e *p*. Inoltre, i dispositivi fabbricati possono essere polarizzati a *tipo p* per polarizzazioni del gate di polarità (*polarity gate voltage*, V_{pg}) di 0 V e *tipo n* per $V_{pg} \approx 1\,\text{V}$, confermando la loro compatibilità con la sintesi di circuiti logici con porte logiche connesse in cascata.

A livello di porta logica, abbiamo fabbricato e collaudato porte composte da due e quattro transistor. In particolare, presentiamo la prima porta logica di tipo XOR composta da soli due transistor, confermando che il controllo della polarità permette il progetto di porte logiche più compatte rispetto alla tecnologia CMOS standard. In aggiunta, mostriamo per la prima volta porte logiche composte da quattro transistor che possono essere configurate come NAND o XOR solo modificando le loro connessioni esterne. In questo caso, porte logiche con output *full-swing* sono state dimostrate sperimentalmente. Infine, presentiamo delle simulazioni effettuate utilizzando TCAD che indicano che una riduzione della tensione di soglia nonché condizioni di polarizzazione ottimizzate possono essere ottenute utilizzando dispositivi più miniaturizzati e utilizzando tecnologie come *strain* o dielettrici *high-*κ.

Sommario

A livello di circuito e sistema, abbiamo definito e configurato un flusso di progetto software *semi-custom* per il design di circuiti in modo automatizzato. Utilizzando questo strumento, abbiamo confrontato delle innovative librerie logiche basate su *standard cell* o matrici regolari di porte logiche con le porte CMOS standard. In particolare, abbiamo ottenuto una riduzione del 40% in termini di prodotto *area-delay* per le librerie di *standard cell* analizzate, e miglioramenti di oltre 2× in termini di *delay* normalizzato nel contesto delle tecnologie *Structured ASIC*. Questi risultati, in definitiva, confermano l'interesse nel continuare lo sviluppo e l'ottimizzazione dei dispositivi con controllo elettrostatico della polarità, affermandoli come ottimi candidati per l'evoluzione delle future tecnologie digitali.

Key words: nanotecnologie, tecnologie emergenti, nanofili di silicio, barriera Schottky, progetto logico, sintesi logica, gate-all-around, controllo elettrostatico della polarità, beyond CMOS, XOR, fabbricazione di dispositivi.

Résumé

Des nos jours, la recherche dans le domaine des circuits numériques est confrontée à des difficultés croissantes dans la tentative d'améliorer les performances et la miniaturisation des dispositifs à semi-conducteur modernes. Une énorme pression économique et l'intérêt pour de nouvelles applications sont en train de stimuler le développement de nouvelles directions de recherche capable de surmonter les limitations physiques qui contraignent la technologie CMOS conventionnelle.

Dans cette thèse, nous considérons un nouveau concept de dispositif, basé sur le contrôle électrostatique de polarité, qui se compose d'un transistor à barrière de Schottky qui peut être configuré pour opérer comme un type *n* ou *p*. Ce dispositif combine des éléments *More-then-Moore* et *Beyond CMOS* pour créer une technologie efficace et crédible pour l'intégration à grande échelle (*Very Large Scale Integration*, ou VLSI). Ici, nous proposons une méthodologie de co-optimisation aux niveaux dispositif/circuit/architecture, où nous adressons des questions partant de la technologie du dispositif, jusqu'à la conception de circuits et systèmes.

Au niveau du dispositif, nous présentons un procédé de fabrication complet et compatible avec les procédés de fabrication standards CMOS. En particulier, nous démontrons des dispositifs qui utilisent un canal composé de nanofils de silicium empilés, fabriqué avec une méthodologie *top-down* et entouré par une grille enrobante afin d'obtenir un contrôle électrostatique optimal. Les contacts de source et de drain sont fabriqués en utilisant du siliciure de nickel afin d'assurer une conduction quasi-symétrique des électrons ou des trous en fonction du mode de conduction sélectionné. Les mesures électriques confirment une excellente performance, montrant un rapport $I_{on}/I_{off} > 10^7$ et une pente sous le seuil près de la limite thermique, de $\approx 60\,\text{mV/dec}$ et $\approx 63\,\text{mV/dec}$ respectivement pour le type *n* et le type *p*. De plus, les dispositifs fabriqués peuvent être polarisés comme type *p* pour une polarisation de la grille de polarité (*polarity gate voltage*, Vpg) de 0 V et comme type *n* pour $V_{pg} \approx 1\,\text{V}$, confirmant leur compatibilité avec la réalisation des circuits logiques avec des portes logiques connectés en cascade.

Au niveau portes logiques, nous avons fabriqué et testé des portes composées de deux et quatre transistors. En particulier, nous présentons la première porte logique XOR constituée de seulement deux transistors, confirmant que le contrôle de polarité permet la conception de portes logiques plus compactes par rapport à la technologie CMOS conventionnelle. De plus, nous montrons pour la première fois des portes logiques composées de quatre transistors qui peuvent être configurées comme NAND ou XOR uniquement en modifiant leurs connexions externes. Dans ce cas, des portes logiques avec sortie pleine-échelle ont été démontrées

expérimentalement. Enfin, nous présentons des simulations TCAD qui indiquent qu'une réduction de la tension de seuil ainsi que des conditions de polarisation optimisées peuvent être obtenues en utilisant des dispositifs plus miniaturisés ainsi qu'utilisant des technologies telles que la contrainte ou des isolants de grille à forte permittivité.
Au niveau circuit et système, nous avons défini et configuré un flot d'outils de conception de projet logiciel de type *semi-custom* pour la conception de circuits de manière automatisée. Grâce à cet outil, nous avons comparé des librairies logiques innovantes basées sur des cellules standards ou des matrices régulières de portes logiques avec des portes CMOS standards. En particulier, nous avons obtenu une réduction de 40% en termes de produit surface délai pour les librairies de cellules standards analysées, et des améliorations de plus de 2× en termes de délai normalisé dans le contexte des technologies de circuits ASIC structurés. Ces résultats, finalement, confirment l'intérêt de poursuivre le développement et l'optimisation des dispositifs avec contrôle électrostatique de polarité, les affirmant comme d'excellents candidats pour le développement des technologies numériques du futur.

Mots clefs : nanotechnologies, technologies émergentes, nanofils de silicium, barrière de Schottky, projet numérique, synthèse numerique, gate-all-around, contrôle électrostatique de polarité, beyond CMOS, XOR, fabrication de dispositifs.

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List of acronyms

Acronym	Definition
ADP	Area × Delay Product
ALD	Atomic Layer Deposition
ALU	Arithmetic Logic Unit
AOI	And-Or-Inverter
ASIC	Application Specific Integrated Circuit
BBDD	Biconditional Binary Decision Diagram
BEOL	Back End Of the Line
BF	Bright Field
BHF	Buffered HF
BisFET	Bilayer pseudospin FET
BOX	Buried OXide
BSG	BoroSilicate Glass
CG	Control Gate
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CNTFET	Carbon NanoTube FET
CNT	Carbon NanoTube
CP	Controlled Polarity
CU	Control Unit
CVD	Chemical Vapor Deposition
D	Drain
DG	Double Gate
DIBL	Drain Induced Barrier Lowering
DRIE	Deep Reactive Ion Etching
DSD	Doped Source and Drain
EBL	Electron-Beam Lithography
EDX	Energy-dispersive X-ray Spectroscopy
EOT	Equivalent gate Oxide Thickness
ERD	Emerging Research Devices
FA	Full Adder
FDSOI	Fully Depleted SOI

List of acronyms

Acronym	Definition
FET	Field Effect Transistor
FG	Front Gate
FIB	Focused Ion Beam
FO4	Fan-Out of 4
FPGA	Field Programmable Gate Array
FTIR	Fourier Transform InfraRed
GAA	Gate-All-Around
GNAND/GNOR	Generalized NAND/Generalized NOR
HAADF	High-Angle Annular Dark Field
HDL	Hardware Description Language
HRTEM	High Resolution Transmission Electron Microscope
HRSEM	High Resolution Scanning Electron Microscope
HSQ	Hydrogen SilsesQuioxane
IC	Integrated Circuit
IMOS	Impact Ionization MOS
ITRS	International Technology Roadmap for Semiconductors
L.S.	Low Stress
LER	Line Edge Roughness
LPCVD	Low Pressure Chemical Vapor Deposition
LUT	Look-Up Table
MBE	Molecular Beam Epitaxy
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NEMS	NanoElectroMechanical Systems
NML	NanoMagnetic Logic
NW	NanoWire
PDSOI	Partially Depleted SOI
PD	Pull-Down
PEC	Proximity Effect Correction
PECVD	Plasma Enhanced Chemical Vapor Deposition
PG	Polarity Gate
PLA	Programmable Logic Array
PMMA	Poly(Methyl MethAcrylate)
PR	PhotoResist
PU	Pull-Up
PVD	Physical Vapor Deposition
RET	Resolution Enhancement Techniques
RTL	Register Transfer Level
S	Source
SAT	boolean SATisfiability
S/D	Source and Drain
SB SiNWFET	Schottky Barrier Silicon Nanowire FET

Acronym	Definition
SB	Schottky Barrier
SCE	Short Channel Effect
SEM	Scanning Electron Microscope
SET	Single Electron Transistor
SiNWFET	Silicon NanoWire FET
SiNW	Silicon NanoWire
SOI	Silicon On Insulator
SoT	Sea-of-Tiles
SRAM	Static Random Access Memory
SS	Subthreshold Slope
STEM	Scanning TEM
Structured ASIC	Structured Application Specific Integrated Circuit
TCAD	Technology CAD
TEM	Transmission Electron Microscope
TFET	Tunnel FET
TG	Transmission Gate
THF	Tetrahydrofuran
VLSI	Very Large Scale Integration
XAS	X-ray Absorption Spectroscopy
XPS	X-ray Photoelectron Spectroscopy

1 Introduction

In the long flow of technological advances that mark ancient and modern history, we have witnessed a logarithmic decrease in the timescale of technological revolutions [1]. Whereas the diffusion of iron tools in ancient civilizations took more than 1000 years starting from 2000 BC, the industrial revolution that started in Great Britain in 1760 took about 100 years before its effects influenced far economies like Japan. Today, with the advent of advanced telecommunications and cheap global shipping services, an individual can propose a new technology worldwide in a matter of days, accessing an exponentially increasing amount of resources and market size.

An interesting consequence of this trend is that, after the development of the integrated circuit in 1958, the time frame of modern industrial revolutions has become shorter than our lives. Today, we can witness first hand the birth of a new technology, and grasp its course of development and stabilization over time. A common effect we can see in our daily lives is that, after a period of fast improvement, a technology will reach a level of fine tuning that requires increasingly costly and risky efforts to bring further improvements.

Conventional nanoelectronic transistor devices, or *Metal Oxide Semiconductor Field Effect Transistors* (MOSFETs), are nowadays the prime example of a technology that is reaching an innovation plateau. Interestingly, however, its industrial development is based on a stable, yet ever unsettling technology. In fact, MOSFETs are the fundamental element of *Complementary Metal Oxide Semiconductor* (CMOS) logic circuits, which lie at the core of all modern digital technologies. As such, their performance and miniaturization advancements, as well as their unit cost reduction, are driven by tremendous economic forces. Due to these dynamics, high performance devices, which may well settle as standard for a number of years, are immediately surpassed and made obsolete by the addition of new techniques (e.g., strain technology) or structural changes, like the recent industrial introduction of FinFET devices [2].

At the same time, transistors manufactured at the most advanced technology nodes (14 nm at present [3]) are facing great improvement challenges due to fundamental physical limitations arising from their intrinsic functioning mechanism and material properties. Nonetheless,

the conventional scaling roadmap envisioned by Gordon Moore back in 1965 and referred to as Moore's law [4] has not yet failed to keep going. It is needless to say that we do not know when this trend will stop. Still, simply due to the discrete nature of atoms, conventional geometrical device downscaling is not any more convenient from a performance standpoint. Recent paradigm changes in industrial transistor development, e.g., the mentioned shift from bulk to FinFETs and the attention to new materials and techniques are a reflection of these fundamental challenges approaching.

1.1 Industrial and research innovation

While Moore's law was originally intended to generally describe transistor integration improvement in terms of cost/performance reduction, the early days of MOSFET scaling were ruled by the idea described by Dennard in 1975 that, so far as the basic physical and material assumptions hold for a reasonably large device, the mere size downscaling of a factor κ, increase in doping concentration as κ and voltage reduction as $1/\kappa$ would bring nothing but benefits to the overall circuit performance [5]. Notably, in this ideal situation, circuit power density would remain constant. After a few technology generations, however, numerous limiting factors arose, first of all the fact that operating voltages could not be scaled indefinitely, mainly due to thermal noise and subthreshold leakage. At the same time, gate oxide thickness could not be reduced further than ≈ 1 nm due to increasing leakage and due to the atoms themselves becoming comparable in size to the insulator thickness. Finally, doping concentrations could not be indefinitely increased, as they increased scattering and the risk of *Source and Drain* (S/D) junction band-to-band tunneling [6].

For these reasons, starting around 2005, other improvement directions were undertaken, such as strain technology, high-κ gate dielectrics and, recently, new transistor geometries, such as multi-gate technology. Noteworthy is the FinFET structure introduced in industrial manufacturing by Intel in 2011 [2]. One common background of these innovations, nonetheless, is the fact that the basic transistor functioning mechanism, based on *Doped Source and Drain* (DSD) silicon channels, has not really changed from its conception in 1954.

1.1.1 Emerging research technologies

While industry invests large efforts in pushing consolidated processes to the limit, the search for a technology that will unlock new spaces for performance improvement at a lower cost is exploding with the invention of a plethora of emerging devices. This invention fecundity is empowered by extremely powerful prototyping tools that have become available and stable technologies, such as *Electron-Beam Lithography* (EBL), controlled thin film deposition processes, such as *Atomic Layer Deposition* (ALD), Sputtering, *Chemical Vapor Deposition* (CVD), and dry (plasma) etching tools. These tools have been providing cutting edge lithographic resolutions below 20 nm and good process control, allowing researchers to rapidly implement and measure state-of-the-art prototypes.

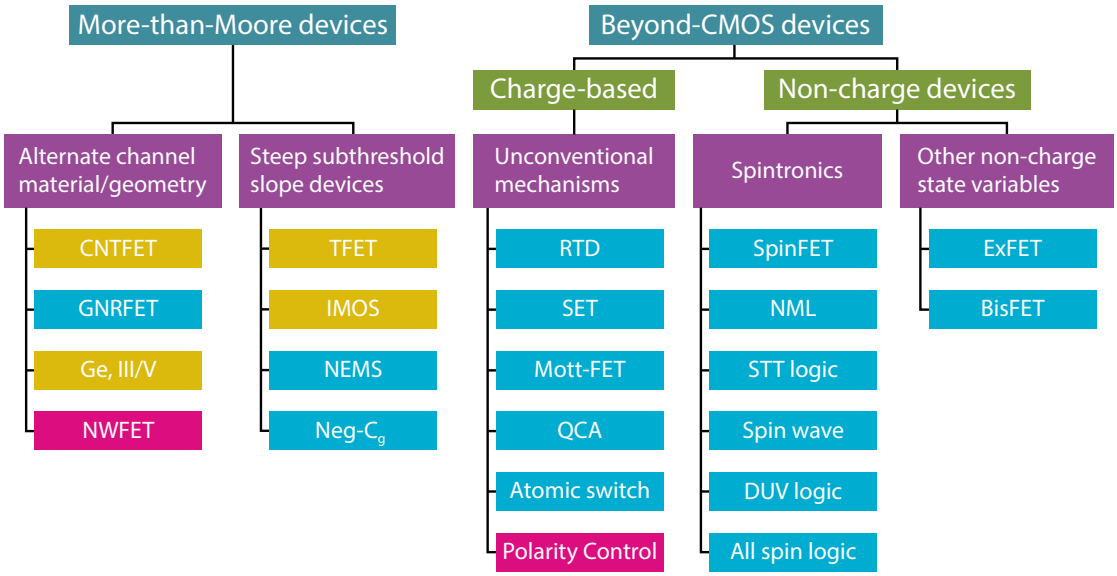

Figure 1.1 – Emerging device universe, categorized as *More-than-Moore* and *Beyond CMOS*. The devices are generally sorted from the more conventional (left) to more exotic structures, based on non-charge mechanisms. *Beyond CMOS* devices enable degrees of freedom and architectures not achievable using conventional CMOS. As a general trade-off, while some devices have been demonstrated and thoroughly characterized (CNTFET, TFET), the more exotic devices are also the most difficult to implement, and devices such as the BisFET [7] are still at a very early research stage. We highlighted in fuchsia the features of the device we will present in the remainder of this thesis. In addition, technologies highlighted in yellow are directly compatible with our device concept. Image adapted from An Chen, IEDM 2012.

Figure 1.1 shows a synoptic chart of emerging device technologies, ranging from the most conventional charge-based devices exploiting new materials and geometries (left) to more and more exotic structures based on unconventional and non-charge based switching mechanisms (right). The first and second columns from the left include devices that act as simple switches, similarly to conventional bulk MOSFETs, although with enhanced properties, such as high mobility, low I_{off} or steep *Subthreshold Slope* (*SS*) [8]. These properties are achieved using novel channel materials, e.g., *Carbon NanoTubes* (CNTs) [9], advanced geometries, like *Gate-All-Around* (GAA) *NanoWires* (NWs) [10] or exploit different switching mechanisms, like band-to-band tunneling (TFET) [11], impact ionization (IMOS) [12] or mechanical activation (NEMS) [13]. In general, we define these technologies as *More-than-Moore* devices, as they can implement conventional CMOS logic circuits without any fundamental paradigm shift at circuit or architecture level.

In order to move out of the boundaries of CMOS, new degrees of freedom have to be introduced at device level. Emerging devices providing these features fall in the *Beyond CMOS* category, and represent a wide range of structures based on charge and non-charge switching mechanisms [14]. For example, special non linear device characteristics are exploited in the *Single Electron Transistor* (SET) [15]. In *NanoMagnetic Logic* (NML), nanoscale magnetic

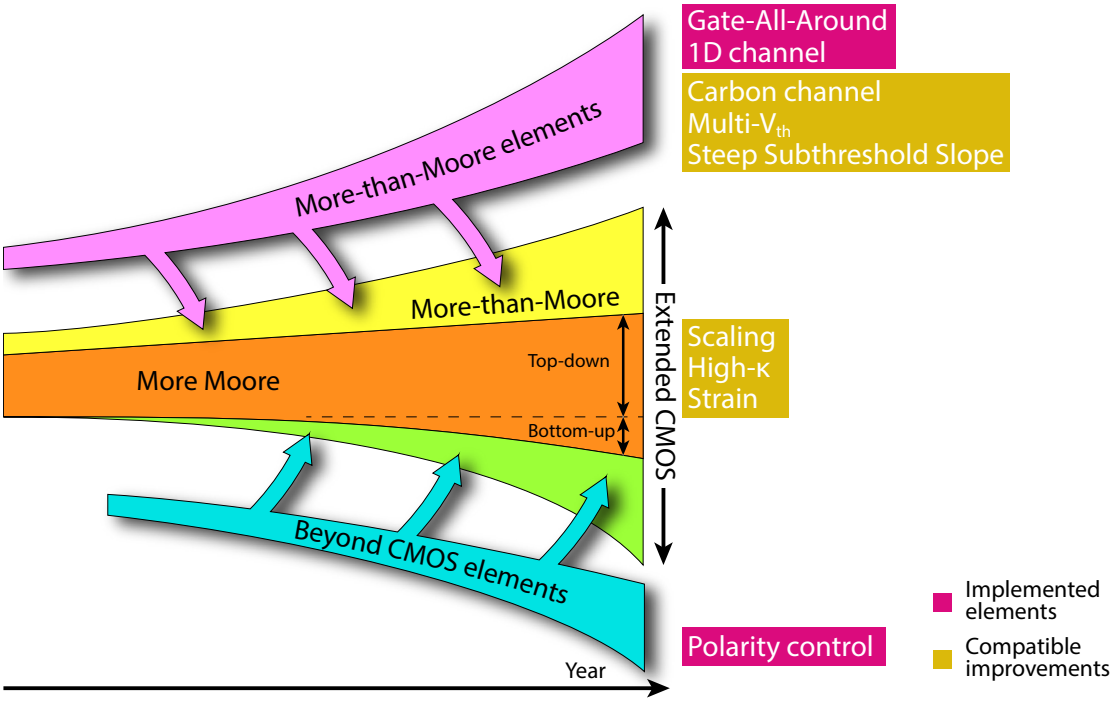

Figure 1.2 – Relationship between technology-defining domains as described in the ITRS ERD chapter. Specifically, the *More Moore* roadmap brings to the extension of conventional CMOS by means of *More-than-Moore* elements, integrating new materials and structures, without enhancing the CMOS paradigm at a higher level, and *Beyond CMOS* elements, adding functional degrees of freedom beyond the capabilities of conventional CMOS. Image adapted from [17].

polarization effects among ferromagnetic domains are exploited to produce efficient logic gates based on polarization, rather than charge [16].

1.1.2 The ITRS roadmap: Beyond-CMOS and More-than-Moore

In this context, the *International Technology Roadmap for Semiconductors* (ITRS) [18] provides a great overview of the trends involving novel device technologies. From 1998, ITRS develops a comprehensive set of documents with the objective of providing a reference and guidance for the continuation and extension of Moore's law in the horizon of the next 15 years.

Figure 1.2 [17] gives a comprehensive view on the relationships between *More Moore*, *More-than-Moore* and *Beyond CMOS* elements, that characterize current device research. Specifically, the relative importance of more-than-Moore elements in the advancement of switching devices for logic and memory applications is expected to grow in the near future, in contrast with a slow-down of the technologies that improve by conventional downscaling, e.g., gate length and *Equivalent gate Oxide Thickness* (EOT).

In this framework, we can then proceed in introducing the device concept developed and implemented in this thesis work.

1.2 The controlled polarity silicon nanowire FET

The main focus of this thesis consists of the development and implementation of a novel device structure combining state-of-the-art *More-than-Moore* and *Beyond CMOS* elements. Namely, our device is fabricated using a vertically stacked silicon nanowire channel structure, comprising two independent GAA electrodes. A first gate electrode, the control gate, acts in the center region of the channel and enables the conventional on/off switching of the device. The second gate electrode, acting on the two side regions of the channel, in proximity of S/D electrodes, enables the selection of the majority carrier type (electrons or holes), effectively determining the device type (n or p) at *runtime*.

In order to contextualize this device in the framework of the ITRS roadmap for emerging research devices, in Figures 1.1 and 1.2, we highlighted in fuchsia the features we implemented and that will be described in detail in the following chapters. Specifically, we envisioned a device providing optimal channel electrostatics by constructing stacked nanowire channels surrounded by GAA structures. At the same time, we embedded the polarity control functionality to enhance the versatility of the device. In particular, this feature represents a new degree of freedom with respect to conventional MOSFET device. Further, when used to implement logic circuits, polarity control enables the design of more area-efficient, faster logic circuits in comparison with conventional CMOS gates.

Balanced, VLSI-compatible fabrication approach

In order to minimize fabrication complexity, and considering the practical limitations of our university cleanroom facilities, our fabrication approach was defined by finding a balance between an advanced 3D nanowire-based channel structure, and the use of simple materials and relaxed fabrication constraints. Moreover, VLSI compatibility is considered as a strong asset in the context of emerging devices, where many bottom-up fabrication techniques (e.g., using CNTs or grown NWs) still find strong limitations to reliable VLSI. Therefore, our devices were fabricated with a fully top-down process flow using low p-doped silicon substrates (bulk and *Silicon On Insulator* (SOI)), with 5-8 nm thick silicon oxide gate dielectrics and intrinsic polysilicon Gate-All-Around electrodes. Device channel length was targeted at around 400 nm, to account for e-beam lithography resolution and alignment accuracy limits. Finally, a structure with these dimensions has proven to be a good compromise to enable high performance characteristics while guaranteeing proper control on the functionality and variability issues.

Device enhancement perspectives

In this device concept, no fundamental constraints limit the application of mainstream device enhancement techniques, as well as more exotic channel materials. Moreover, the GAA/-nanowire geometry is the natural evolution of current industrial Fin-based geometry and, as such, it provides the best possible geometry for the suppression of *Short Channel Effects* (SCEs), therefore allowing the most aggressive dimensional scaling [8]. Moreover, this device can directly benefit from advanced yet industrially available device enhancement technologies, including high-κ-metal gate stacks and strain. At the same time, the polarity control effect is not limited to a specific channel geometry or material. In principle, the same functionality can be achieved using Fins as well as CNTs or other semiconducting materials [19]. For example, a recent work from S. Nakaharai *et al.* [20], demonstrates the applicability of the polarity control approach to novel 2D semiconducting materials. In particular, the authors demonstrate an ambipolar α-$MoTe_2$transistor where promising measured n and p-type characteristics are shown via the electrostatic polarization of the same physical device.

Functionality enhancements and co-integration

Thanks to the efficient electrostatics, and electrostatic doping effect used for the polarization of the device, interesting concepts can be developed starting from the proposed fabrication methodology and device design. Specifically, the polarity gate electrode, which in the presented form consists of two sections acting on the source and drain *Schottky Barriers* (SBs), can be split into two independent electrodes, thus enabling further polarization flexibility at the cost of the addition of one device terminal. With this architecture, demonstrated by J. Zhang *et al.* in [21], smart gates polarization allows the configuration of the devices to high or low threshold voltage (V_{th}) modes for both n and p-type polarizations in the same device. This, in turn, reduces constraints at the circuit level, allowing the fabrication of configurable low power/high performance transistors.

In another work, presented by J. Zhang *et al.* in 2014 [22], we demonstrated a device based on the same architecture exploiting weak impact ionization to achieve state-of-the-art 6 mV/dec *SS* over 5 decades of current, among other high performance features. Note that this device was built using a FinFET (tri-gate) channel structure, obtained by exchanging a single silicon etching step in our presented top-down fabrication process.

Finally, the proposed fabrication approach and design was adapted by F. Puppo *et al.* [23] to implement memristive biosensing devices. These devices effectively exploit the high area/volume ratio provided by nanowires, in conjunction with the simple top-down fabrication approach that does not require complex transfer techniques required for bottom-up fabricated nanowires.

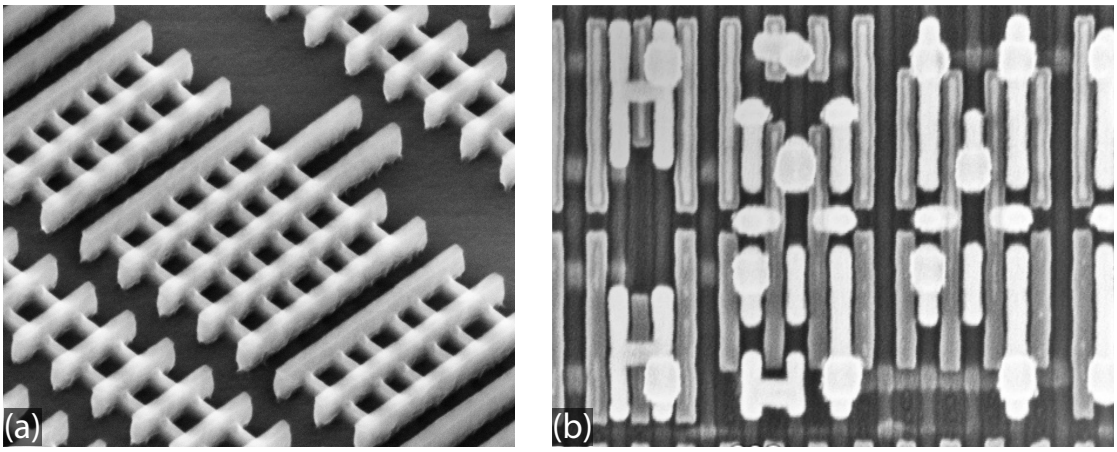

Figure 1.3 – Industrial state-of-the-art FinFET technologies. (a) 22 nm FinFET tilted SEM view. Image source: Intel®. (b) Last generation 14 nm FinFET SEM fabric view. Image source: ChipWorks [24]. In both images, strong regularity is shown in the layout design. Moreover, due to the peculiar geometry of FinFETs, devices with larger channel width are composed of multiple fins in parallel, i.e., width is a quantized quantity in these scaled devices.

1.3 A wider perspective: device/circuit/architecture interactions

Device development at scaled technology nodes (45 nm and beyond) brings improved performance at the cost of increased variability and circuit design constraints. In particular, the need of increased layout regularity (see, e.g. Figure 1.3, showing state-of-the-art industrial Intel® FinFETs) and attention to transistor threshold voltage variability can strongly benefit from a device/circuit/architecture interaction aware design [25].

In the case of emerging device technologies, device non-linearities, unconventional switching mechanisms as well as non-charge internal states are exploited, creating new degrees of freedom not implementable using simple MOSFETs. However, we believe that only by understanding the advantages of these features at circuit level and, further, at architecture level, we can unlock the potential of these novel technologies.

In the specific case of CP devices, we implement devices which require two gate electrodes to operate correctly. Therefore, these devices are slightly more complex than conventional MOSFETs. At the same time, as we will describe in detail in the following chapters, these devices enable the mapping of logic circuits with reduced transistor count as compared to conventional CMOS. Fewer transistors translate into smaller area and critical path delay for large circuits, ultimately allowing the fabrication of more efficient circuits.

The focus of this thesis, therefore, is not limited to device fabrication and characterization. The design of the presented device, in particular, is interleaved with the evaluation of its properties and advantages at circuit and architecture level. Figure 1.4 presents a conceptual overview of the main design abstraction levels. At the bottom, we envision the design of a regular sea-of-wires, with transistors grouped in series and parallel to form efficient basic building blocks

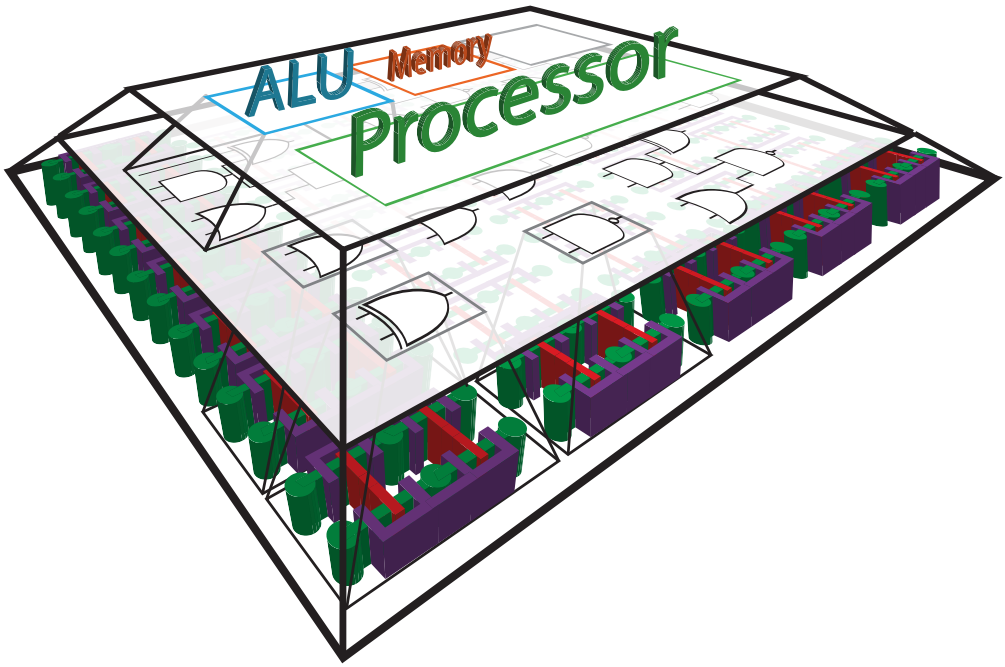

Figure 1.4 – Conceptual representation of a regular sea-of-wires. Tiles are configured to realize logic functions that are part of a complex system such as a processor.

acting as small grain elements to map logic circuits [26]. At the same time, we consider trade-offs at logic gate and architecture level, such as logic gate granularity and regularity for the implementation of *Structured Application Specific Integrated Circuits* (Structured ASICs) and *Field Programmable Gate Arrays* (FPGAs) [27] to better understand the cost and advantages of this methodology.

1.4 Prior art

The results described in this thesis build upon a number of earlier research works which created the base for the presented device and circuit design methodologies. We mention here the most relevant results that directed us to further investigate controlled polarity device behavior and applications, finally leading to an optimized fabrication approach at device and circuit level. Note that, due to the variety of design levels treated in this thesis, more detailed state-of-the-art analyses are proposed in each subsequent chapter.

Polarity control static logic

Static complementary logic circuit design was first introduced by M. H. Ben Jamaa *et al.* in 2009 [28]. In this early work, the idea that Schottky barrier FET devices could be polarized via electrostatic control over the source and drain barriers, by dynamically selecting the majority carriers allowed in the device channel, was exploited as an added degree of freedom with

respect to conventional doped source and drain MOSFETs. Specifically, the first controlled polarity SB FET device was presented by IBM in 2005 [29], and was based on the use of a CNT as channel material (see Section 2.2.2). This device required high voltage biases in order to correctly polarize it to n or p-type, however, it was understood that no particular physical limitations would hinder its further scaling and optimization to obtain low threshold and polarization voltages for the device gate electrodes. Following this seminal work, in [30], as well as in our circuit-level evaluation of the CP logic design paradigm presented in Chapter 5, simulations were based on an adapted *Carbon NanoTube FET* (CNTFET) device model. Nonetheless, all extracted data was normalized to the intrinsic technology delays in order to create a fair comparison to conventional CMOS circuits.

Polarity Control in a single nanowire FET

Stimulated by the interest in developing a simple technology demonstrating polarity control, based on a top-down fabrication approach for VLSI compatibility and an advanced device geometry to obtain high performance characteristics, efforts started towards the creation of a silicon nanowire based structure. This device, presented by D. Sacchetto *et al.* in 2012 [31], demonstrated that it is indeed possible to obtain n or p-type polarization of a nanowire, showing n and p-type characteristics measured in the same physical device. However, this device was fabricated using contact photolithography to obtain 20 μm long Si wires polarized by $\approx 7\,\mu$m long gate electrodes, and further improvements in device structure and scale were needed to obtain the optimal I_{d}–V_{g} characteristics required to build circuits using this technology. Specifically, optimized nanowire etching procedures based on *Deep Reactive Ion Etching* (DRIE) were being developed to obtain smaller and more reliable wires [32, 33]. As described in detail in Chapter 3, some of these techniques are embedded in the optimized fabrication process flow developed in the presented research work.

1.5 Research objectives and contributions

Figure 1.5 presents a complete overview of the research topics covered in this thesis. The main analysis flow for the evaluation and implementation of controlled polarity *Silicon NanoWire FET* (SiNWFET) devices is represented by the blue squares. On this path, we start from device design, fabrication and characterization, down to elements of device physics and functioning mechanism. We then focus on logic gates, fabricated using CP SiNWFETs, and demonstrate their functionality advantages compared to conventional CMOS gates. Further, we perform technology mapping using standard cells at different granularities to evaluate the impact of the higher device flexibility to produce faster and smaller logic circuits compared to CMOS. Note that technology mapping is performed at an higher abstraction level, thus it is applicable to any device technology exhibiting polarity control. Finally, in addition to the main workflow, red and green squares in Figure 1.5 represent the main characterization and modeling methodologies presented along the thesis to, respectively, understand device performance and properties

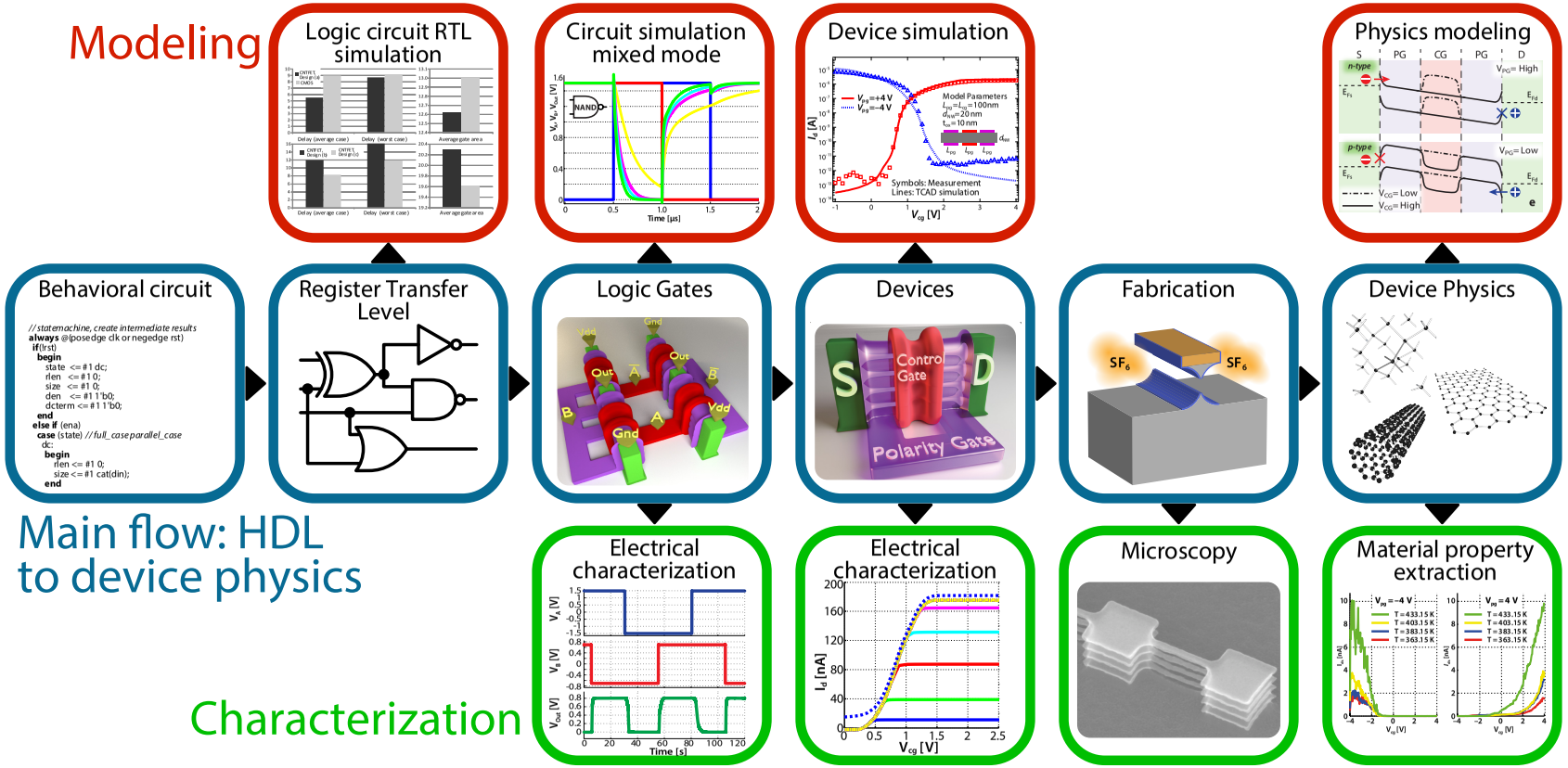

Figure 1.5 – Overview of the presented research work. The blue squares represent the main research flow, from a circuit description in a HDL down to the physics of our implemented CP devices. Starting from an abstract benchmark circuit, we considered its register transfer level mapping, using designed efficient standard cells based on the CP paradigm. Standard cells are fabricated and measured as discrete elements to demonstrate their added functionality with respect to CMOS. Further, devices are designed considering their intrinsic efficiency, evaluated through SS and I_{on}/I_{off} performance. Finally, a full fabrication process flow is implemented to produce the devices and elements of device physics are considered to guarantee correct functionality and performance. Finally, red and green squares show, respectively, the modeling and characterization scenarios considered in this thesis to evaluate and make predictions at different steps of the main research flow.

and to predict performance beyond the limitations of our university fabrication process.

After introducing the range of topics covered in this thesis, we can summarize the objectives and research contributions of the presented research work as follows:

1.5.1 Device design and fabrication

The first and main objective of this work has been to demonstrate a novel device based on polarity control. This device had to be scaled to a dimension enabling high performance characteristics, while being under control in terms of variability sources in our university cleanroom. Moreover, as previously described, we envisioned a device designed in a top-down fashion, to enable future VLSI integration, with a low thermal budget, CMOS compatible fabrication approach.

Results

A full top-down fabrication process flow was developed, demonstrating stacked $\approx 400\,\text{nm}$ long, $20-50\,\text{nm}$ thick nanowires controlled by gate-all-around electrodes for best case channel electrostatics. Measurement results on silicon show $I_{on}/I_{off} > 10^7$ and subthreshold slopes approaching the thermal limit, $SS \approx 60\,\text{mV/dec}$ ($\approx 63\,\text{mV/dec}$) for n(p)-type operation in the same physical device. Moreover, the shown devices behave as p-type for a polarization bias (polarity gate voltage, V_{pg}) of 0 V, and n-type for a $V_{pg} \approx 1\,\text{V}$. Note that this feature is a fundamental requirement to obtain cascadable logic gates with this technology, i.e., logic gates operating with all voltages in the range $0\,\text{V}-V_{dd}$.

1.5.2 Two and four-transistor XOR demonstration

The second objective of this work was the demonstration of the logic gate level features provided by the polarity control degree of freedom. In particular, compact configurable inverter/buffer two-device circuits, ultimately implementing a compact XOR logic function, and XOR/NAND four-transistor reconfigurable logic gates were envisioned to demonstrate the advantage of this technology with respect to conventional CMOS.

Results

Two-transistor logic gates composed of two separate devices were measured, showing the expected compact XOR implementation and showing multi-level logic compatible characteristics, with all positive voltages used as input biases for the polarity and control gates of the devices. In particular, these gates were implemented connecting two physically equal devices, thus showing that only one transistor design is required to implement complementary logic gates. Therefore, we showed that no chemical doping or doping wells were required to fabricate functional complementary logic gates, to the advantage of lower complexity fabrication

and circuit area cost.

Further, XOR/NAND configurable logic gates composed of pre-connected, four-transistor circuits were fabricated and measured, showing configuration as XOR or NAND gate of the same physical circuit, and showing full-swing output for both modes as predicted theoretically by our implemented complementary, pass-transistor based logic design approach.

1.5.3 Large logic circuit level benchmarking

The third objective we envisioned, was the evaluation of the advantage of the polarity control degree of freedom provided at device level, in the design of efficient logic circuits. Here, we consider a comparison with conventional CMOS to understand the advantage of the proposed devices to reduce transistor count, thus area and delay resources, in the technology mapping of large circuit benchmarks.

Results

At the time of this analysis, we employed an adapted device model based on CNTs, to show that reconfigurable medium-grain cell regular fabrics based on polarity control produced a reduction of 47% of area×normalized delay over an optimized, commercial configurable logic block (the Actel ACT1 block), and of 38× over 4-input Look-Up Tables, showing that significant performance advantages over CMOS can be obtained through the higher expressive power of CP logic blocks. In this part of the research, results are normalized to the intrinsic technology delays, in order to produce a fair comparison with conventional CMOS logic gates, and be applicable to other CP-enabled technologies.

1.6 Thesis organization

The presented research work is described over five main chapters, followed by a conclusion. For the sake of clarity, the thesis starts from the fabricate devices characterization and simulation, and follows the flow of Figure 1.5 from right to left, conceptually stepping to higher and higher abstractions to arrive at the circuit level benchmarking in Chapter 5. A further chapter presents ongoing research with more details on advanced fabrication optimization techniques for the device. Note that, due to the wide range of topics covered in the manuscript, specific background and state-of-the-art information is presented chapter-by-chapter.

Chapter 2 – In-Field Controlled Polarity SB FET

In this first chapter, we present the CP SB FET device which will create the conceptual ground for the remainder of the thesis. Specifically, after describing a number of devices from the literature implementing similar properties, we introduce the functioning mechanism for the

proposed structure, and present measured electrical characteristics demonstrating properties and performance of the fabricated devices. Finally, we present simulation results reproducing the measured device characteristics, and expand these simulations to scaled device dimensions, to predict performance and properties when including advanced technologies such as high-κ/metal gate stacks.

Chapter 3 – Device Fabrication

This chapter, strongly related to Chapter 2, gathers all the information on the fabrication process flow and techniques we employed to create the measured devices. After motivating our choices in terms of device geometry and general fabrication approach, we introduce the most common nanowire fabrication methodologies, including top-down and bottom-up techniques, focusing on the DRIE-based approach we used in our process. Then, we proceed to describe in detail all the critical phases characterizing the implemented process flow, with detailed notes on the challenges and advantages of the employed methodologies. Finally, the full process runcard is proposed as reference at the end of the chapter.

Chapter 4 – Polarity control logic gates

In this chapter, we step up from Chapter 2 to describe small circuits composed of two and four transistors working together. Measured input-output characteristics of small fabricated logic gates are discussed demonstrating the advantage of the added degree of freedom enabled by polarity control. Efficient logic cells implementing INV, NAND and XOR operators are demonstrated. Similar to the device-level analysis, fitted mixed-mode *Technology CAD* (TCAD) simulations are presented to show more in detail the operation nuances of the fabricated logic gates, along with some performance predictions at a more advanced technology node.

Chapter 5 – Polarity control circuit level benchmarking

This chapter presents the last step of the device-to-circuit interaction analysis proposed in this thesis to evaluate the advantages of our device design methodology. Specifically, we consider the physical design of regular fabrics with CP FET devices and consider a number standard cells of medium grain size built with this technology. With these standard cells, we perform technology mapping and place and route of a set of benchmark circuits, and compare the results with conventional bulk MOSFET based CMOS and an existent configurable logic cell of medium grain size, the Actel ACT1 logic block, as well as 4-input *Look-Up Tables* (LUTs). Further, for the sake of generality, results included in this chapter are presented after normalization to intrinsic technology model parameters, such as delay and area, to produce evaluations that can be applied to any CP enabled technology.

Chapter 6 – Device technology enhancements

In this final chapter, we showcase some options for future improvement of the SiNWFETs at fabrication level. Specifically, we focus on S/D nickel silicide technology as an enabler for optimized device functionality and performance. First, we describe basic material and electrical characterization of the S/D Schottky contacts produced using the fabrication process of Chapter 3. Then, we introduce a method for S/D contact resistance reduction by S/D contact hollowing and volume silicidation. Due to the increasing need for an enhanced isotropic deposition technique for nickel silicide, and strongly motivated by our fabrication constraints, we then proceed in describing a novel, wet chemical based NiSi deposition technique, that is currently under development in collaboration with the ETH Laboratory of Inorganic Chemistry [34].

Chapter 7 – Conclusions

This chapter concludes the thesis, with some remarks on the challenges and opportunities provided by the presented research work and an outlook on future research directions.

2 In-Field Controlled Polarity SB FET

In this chapter, we comment on a new class of transistors designed to achieve in-field polarity control, while providing compatible gate voltages for operation in multi-level logic circuits. We demonstrate the operation of the devices we designed and fabricated by showing measured characteristics, followed by TCAD simulations we produced to evaluate device performance and scaling perspectives. The presented device will serve as a foundation for the subsequent circuit and architecture performance analyses shown in Chapters 4 and 5. Note that, for the sake of conciseness, details regarding the fabrication process flow and tools are described later in Chapter 3.

In the following, we first illustrate the principle of operation for this device (Section 2.1). We then propose, in Section 2.2, an overview of the main devices from the literature creating the background for our research. In Section 2.3, we introduce the proposed CP *Schottky Barrier Silicon Nanowire FET* (SB SiNWFET) device, describing device functionality requirements in detail, the switching mechanism and device geometry. In Section 2.4, we present the measurement setup and device measurements we performed on fabricated devices showing device-level performance properties and the proposed polarity control functionality. In order to make predictions at device and circuit levels in terms of scalability and technology optimization, in Section 2.5, we present a basic and an optimized TCAD device model with some extracted characteristics. Finally, Section 2.6 concludes the chapter, summarizing the contributions provided by the presented research work.

2.1 Polarity control functionality

In this section, we describe the polarity control functionality concept. We propose an overview on Schottky barrier-based devices, and their interest with respect to conventional doping-based MOSFET devices. Further, we describe their intrinsic ambipolar behavior and how we can harness it to produce the sought electrostatic polarity control.

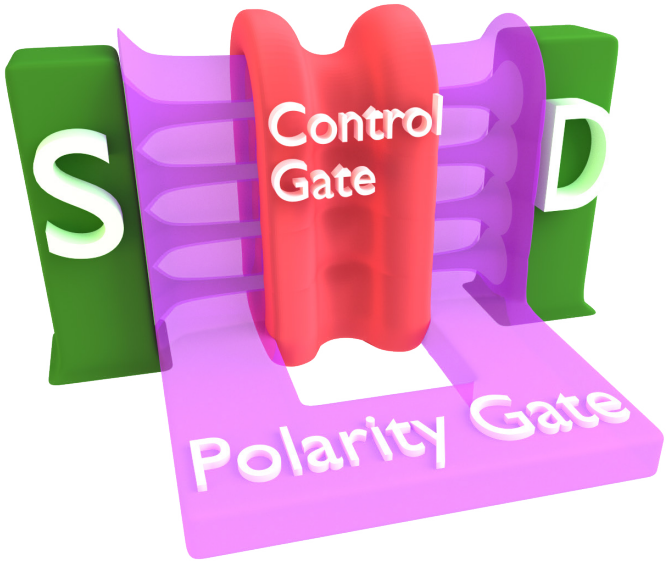

Figure 2.1 – 3D conceptual view of the proposed device. Source/Drain pillars supporting a vertical stack of nanowires are shown in green. The Gate-All-Around polarity gate, covering the side regions of the channel is shown in violet, while the central control gate is shown in red. The model is shown in proportion to the actual fabricated device dimensions.

2.1.1 Generalities

As we introduced in Chapter 1, as device channel lengths approach the nanoscale (45 nm node and beyond), device variability concerns demand less abrupt chemical doping profiles and lower absolute doping concentrations. At the same time, SB FET transistors are receiving increasing attention due to their simpler structure, low S/D access resistances, atomically abrupt junctions and good scalability properties with respect to conventional DSD MOSFETs [35, 36]. Moreover, many novel device channel materials are most effectively embedded as SB transistors, such as NWs, CNTs, graphene and other quasi-2D materials such as MoS_2 monolayers [37, 38, 39, 40].

One peculiar characteristic of SB-based devices is the presence of ambipolar behavior, i.e., the simultaneous conduction of both electrons and holes through the device channel [41, 42]. This effect is typically detrimental to the device functionality, due to the unwanted leakage of minority carriers which in turn increases I_{off}. In extreme cases, as shown in Figure 2.2 [9], the device will present the superposition of visible n and p-type characteristics [43], producing a strongly non-linear characteristics with an on state both at low and high V_{gs} values. In typical circuit applications, ambipolar conduction is an unwanted effect, due to the increased I_{off} leakage and lower device performance. Thus, a large effort has been devoted to reducing it through engineering of materials, doping and device geometry [44].

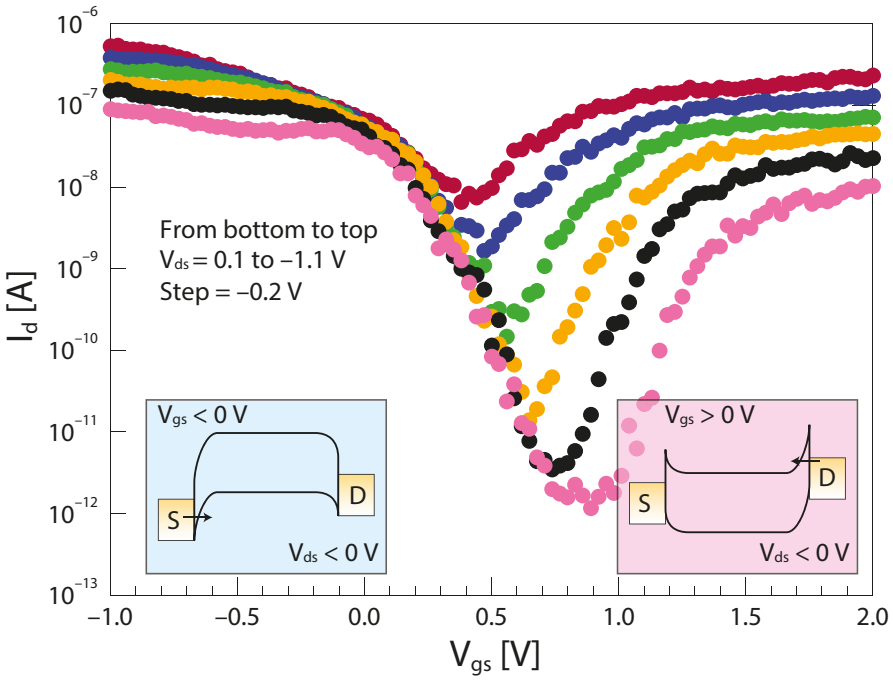

Figure 2.2 – Typical strongly ambipolar device I_d–V_{gs} characteristic. The characteristics show a superposition of n-type and p-type conduction. The characteristics are quasi symmetric around a minimum I_d value. The shift of the minimum I_d to the left for increasing V_d biases is due to the fact that the dominating barrier for carrier injection in the channel changes from the source to the drain side along the characteristics. Therefore, when the barrier is at the source side (light blue inset), the device behaves as a p-type device, and the V_d has no influence on the source side barrier. When the V_{gs} is at high bias, however, the dominating barrier is at the drain side, and V_d has a strong influence on the barrier and thus the I_d. Image adapted from [9].

2.1.2 Ambipolarity as an added degree of freedom

In our case, we exploit ambipolar conduction in a lowly doped device channel by harnessing it via an electrostatic polarization, i.e., we introduce a device controlled by two gate electrodes: the first one, the *Control Gate* (CG), conventionally switches on and off the device. The other electrode, the *Polarity Gate* (PG), acts in proximity of both the source and drain electrodes, determining the device polarization (n or p-type).

The addition of the PG electrode enables a two-fold advantage, in terms of device fabrication and functionality. As we will further describe in Section 2.3.2, no dopant implantation is required to guarantee device functionality, thus reducing complexity with respect to conventional CMOS fabrication processes, in terms of processing steps and number of required lithographic masks. Moreover, due to the dual polarity nature of the proposed devices, there is no need for the separate development of n and p-type devices, to the benefit of fabrication simplicity and device regularity. In terms of functionality, the PG enables runtime control of

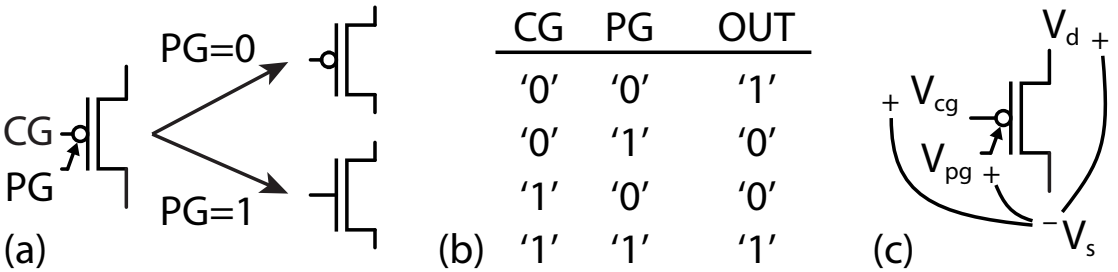

Figure 2.3 – (a) CP FET circuit symbol, with the used polarization convention. (b) Conceptual single device truth table, with inputs following the convention: high V_{pg-s} or V_{cg-s} equals $'1'$; low V_{pg-s} or V_{cg-s} equals $'0'$. Equivalently, for the output, a high I_{ds} equals $'1'$ and a low I_{ds} equals $'0'$, as if the device was connected as pull-down network in a pseudo-logic gate (see Section 4.1). (c) Definitions of the used bias voltages. Unless otherwise stated, all voltages are defined with reference to V_s. Due to the inherent polarization symmetry provided by this device, the source is defined as the electrode at the lowest voltage between the two channel access contacts.

the device polarization, thus a single device can be used to implement both device polarities in a logic circuit.

2.1.3 Embedded binate operation

The ability of the device to change polarity on command enables the two gate polarizations to interact in a fashion precluded to conventional MOSFET devices. Specifically, four different conduction states can be identified, in contrast with the simple on/off states of a conventional MOSFET. To illustrate this concept, in Figure 2.3(b) we present a conceptual table of four the conduction states of a CP FET device. In this table, we assign a logic $'1'$ to a high V_{pg-s} (V_{cg-s}) bias voltage and $'0'$ to a low bias voltage. In terms of output, we associate a low channel resistance—the device in the on state—with logic $'1'$ and a high channel resistance with $'0'$. As we can see from the table, the device output is in the $'1'$ state if and only if both of the inputs are in the same state (CG = PG =$'$ 1$'$ or CG = PG =$'$ 0$'$) and is in the $'0'$ state if the inputs differ. Note that this non-linear behavior is not reproducible by a single conventional MOSFET. If we consider the device as a black box, the truth table of Figure 2.3(b) effectively shows that the device calculates the output of a binate function of two inputs, in this specific case an XNOR function. As we will further discuss in Chapter 5, this effect enables the implementation of complex logic circuits with less area occupation and input-to-output timing delay than conventional CMOS.

As we will see more in detail in Section 2.3.1 and later in Section 4.1, specific device features have to be combined to provide a device that not only changes polarity on command, but allows the creation of functioning logic circuits by assembly of small logic gates, similarly to the conventional CMOS standard cell-based methodology.

2.2 State-of-the-art

In this section, we present a number of relevant works from the literature providing the background for our functionality and fabrication approaches. Table 2.1 provides a comparison between our work and the most important devices presented in the literature [45, 46, 47, 29]. In the following, we review the main properties of some of these devices more in detail.

2.2.1 Ambipolar FET implementing a single transistor XOR logic gate

Among a number of ambipolar devices presented in literature, we showcase here the device presented in [50], due to the logic circuit application devised by the authors. This device exploits for the first time the strongly non-linear ambipolar device characteristic of an intrinsic CNT-based FET to implement a compact single-transistor XOR logic gate. As shown in the schematic in Figure 2.4(a), the V_g is evaluated as the average between two inputs V_{G1} and V_{G2} by means of two equal access resistors, and fed to the CNTFET gate electrode. Due to the presence of two logic inputs, we can consider three input bias values for V_G: $V_G = 7.2\,V$ when G1 and G2 are at logic $'0'$, $V_G = 15\,V$ when G1 and G2 are at opposite logic values $'1'/'0'$ or $'0'/'1'$ and finally $V_G = 20\,V$ when both G1 and G2 are at logic value $'1'$. Due to the ambipolar characteristics of the device, shown in Figure 2.4(b), the device is on when V_G is sufficiently low or sufficiently high, while the channel turns off for intermediate V_G voltages. Using a pull-up resistor to implement a simple pseudo-logic gate, a binate function (XOR) can then be evaluated using a single ambipolar transistor.

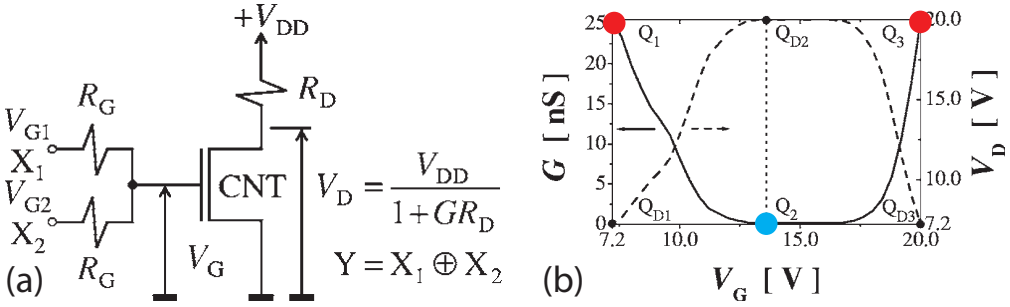

Figure 2.4 – (a) Circuit schematic of a pseudo-logic gate exploiting a single ambipolar CNTFET to calculate an XOR logic function and (b) the ambipolar device characteristics (G–V_g and V_g–V_d) with the highlighted CNTFET on states (red dots) and off state (blue dot). Image adapted from [50].

Besides its interesting logic functionality, this device presents a number of disadvantages, mostly due to the single input device structure:

- The two inputs ($X1$ and $X2$) have to be multiplexed before acting on the gate electrode. This is implemented by averaging them through two resistors at the gate input, leading to static leakage.

Table 2.1 – State-of-the-art for nanowire / nanotube channel devices with full / partial polarity control by means of a polarity gate. Our device shows a high level of symmetry between n and p-type operation in terms of SS, I_{on}/I_{off} and input voltages, combined with a top-down fabrication approach enabling large-scale integration.

Ref.	**Device Type**	**Approach**	**Device length**	**Wire diameter**	V_{pg} **range**	V_{cg} **range**	I_{on}/I_{off}	**Subthreshold Slope**
[45]	Single SiNWFET, Ω-gate (CG), Substrate (BG)	Bottom-up	500nm (gate)	40 to 100nm	−15V (p-type) −5V (off)	−2V to 2V	$\approx 10^7$ (p-type)	≈140mV/dec (p-type)
[47]	Single SiNWFET, Ω-gate (CG), Ω-gate (BG)	Bottom-up	≈1μm (channel) 220nm (gate regions)	20nm	V_{pg} =2V, V_d =2V (n-type) V_{pg} =−2V, V_d =−2V (p-type)	−2V to 2V	$\approx 10^7$ (n-type) $\approx 10^9$ (p-type)	≈150mV/dec (n-type) ≈150mV/dec (p-type)
[46]	Single SiNWFET, Ω-gate (CG), Substrate (BG)	Top-down	28μm (channel) 2μm (gate)	60nm	−10V to 10V	−4V (p-type) 4V (n-type)	$\approx 10^6$ (n-type) $\approx 10^4$ (p-type)	≈80mV/dec (n-type) >2000mV/dec (p-type)
[29]	Single CNTFET, Ω-gate (CG), Substrate (BG)	Bottom-up	300nm (channel)	≈1.4nm	V_{pg} =1.6V, V_d =0.6V (n-type) V_{pg} =−2V, V_d =−0.6V (p-type)	−2V to 2V	$\approx 10^3$ (n-type) $\approx 10^4$ (p-type)	≈63mV/dec (p-type)
[48]	Single SiNWFET, Ω-gate (CG), Substrate (BG)	Top-down	50μm (channel) 5μm (gate)	60 × 90nm	−20V to 20V	−3V to 5V	$\approx 3\times10^8$ (n-type) $\approx 3\times10^6$ (p-type)	≈150mV/dec (n-type) ≈100mV/dec (p-type)
This work [49]	Stacked SiNWs, GAA (CG), GAA (BG)	Top-down	400nm (channel) 100nm (gate regions)	20 to 30nm	−1V to 4V (n-type) −4V to 0V (p-type)	−1V to 4V	$\approx 3.5\times10^7$ (n-type) $\approx 10^8$ (p-type)	≈60mV/dec (n-branch) ≈63mV/dec (p-branch)

- The transistor requires high input operating voltages, since two transitions (on→off→on) have to fit in the I_d–V_g characteristic.

- As previously described, due to minority carrier leakage, the device always shows high V_{ds} in the off state, reducing performance and increasing static power consumption.

- In order to correctly operate, the input voltages V_{G1} and V_{G2} have to be tuned according to the input FET characteristic on → off → on behavior. Therefore, the output of the logic gate would not be compatible with the input of a subsequent logic gate in a more complex logic circuit.

2.2.2 Electrostatic polarity control demonstration in a CNTFET

The work presented by IBM in 2005 [29] proposed for the first time the active control of channel polarization. In the proposed device structure, shown in Figure 2.5(a), the transistor channel, consisting of a single CNT, is controlled by both a conventional gate electrode acting on the center region of the channel, and the substrate, which acts as polarity gate. The addition of a PG to the transistor enables the dynamic polarization of the device to n or p-type, effectively acting as a suppressor of minority carrier leakage during operation. This effect potentially enables high performance characteristics to the ambipolar device, without forgoing by construction (e.g., through chemical doping) the non-linear effect given by ambipolar behavior.

Device characteristics demonstrating the controlled selection of p-type or n-type characteristics in the same physical device are shown in Figure 2.5(b). Similar to the device presented in Section 2.2.1, the device is built exploiting a single CNT as channel material, deposited on an isolated Si substrate after patterning of the central Al gate.

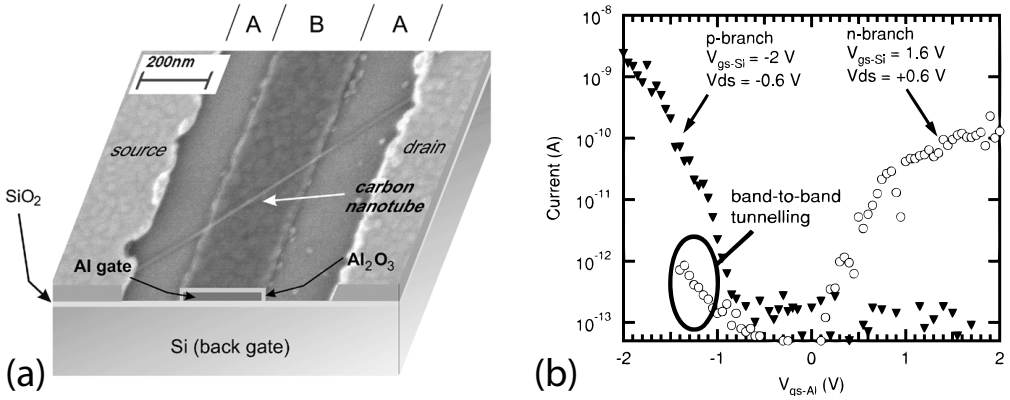

Figure 2.5 – (a) Composite image of the device proposed in [29]. A CNT is laid between two Ti S/D contacts. The substrate is isolated with 10 nm of SiO_2 and acts as back gate, while a second Al gate acts along the center section of the device channel. (b) Measured device subthreshold I_d–V_{gs} characteristics for high and low V_{bg}, showing n-type and p-type behavior. Good suppression of ambipolar conduction is shown. Image adapted from [29].

2.2.3 Voltage-selectable top-down SiNW FET

A second device, presented by F. Wessely *et al.* [48], proposes a similar electrostatic polarization concept, exploiting the back gate bias, V_{bg}, imposed on the substrate of a ultrathin body SOI wafer. A conceptual device cross section is shown in Figure 2.6(a). To fabricate the device, a rectangular-cross section (60 × 90 nm) nanowire is patterned by e-beam lithography on the SOI device layer. This device is built with a top-down approach, depositing a Ω *Front Gate* (FG) structure in the middle section of the nanowire. Figure 2.6 shows measured device I_d–V_{fg} transfer characteristics for the n and p-type characteristics, selected respectively with a V_{bg} of +20 V and −20 V. Good subthreshold control of I_d is shown, although very strong V_{bg} biases are needed to correctly polarize the device due to the relaxed dimensions and device structure.

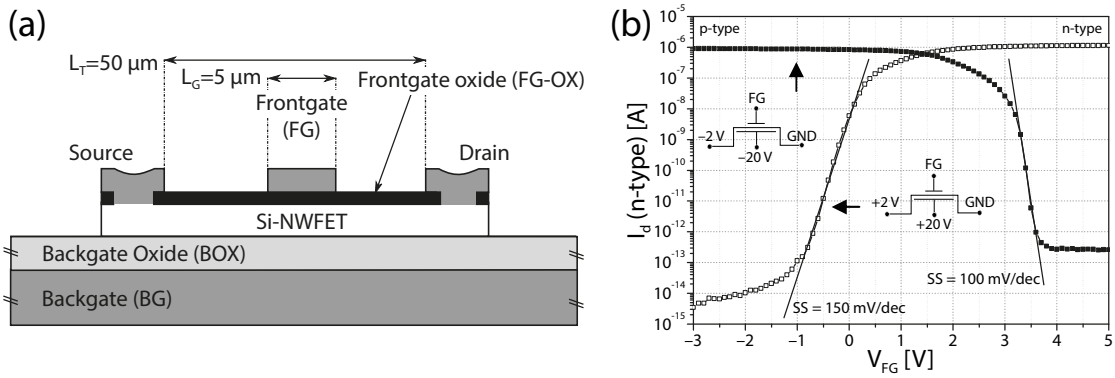

Figure 2.6 – (a) Conceptual cross section of the device proposed in [48], composed of a patterned rectangular nanowire of 60 × 90 nm. (b) I_d–V_{fg} device characteristics measured for V_{bg} = +20 V (n-type) and V_{bg} = −20 V (p-type). Image adapted from [48, 51].

2.2.4 SiNWFET with two independent Ω gate electrodes

The first work exploiting electrostatic polarization with Si nanowires is presented in [52] and further optimized in [47]. The aim of this work is to obtain a configurable universal transistor, able to implement with the same physical structure either an n-type or p-type transistor with symmetric n and p-type performance properties. This device is built with a bottom-up approach, exploiting a single grown Si nanowire transferred on a final substrate, where two Ω-gate structures, as well as the S/D contacts, are patterned last on top of the nanowire. Figure 2.7(a) and (b) show a 3D conceptual view and SEM micrograph of the proposed device, with two Ω-gate structures deposited on top of a bottom-up fabricated nanowire channel, in proximity of S and D metal electrodes.

I_d–V_{G1} transfer characteristics for the p-type (V_{G2} = −3 V) and n-type (V_{G2} = +3 V) polarizations are shown in Figure 2.7(c). The device shows very pure p-type and n-type behaviors for the two modes, with perfect suppression of ambipolar and other types of leakage. Note, however, that each gate acts exclusively on one of the two SB at either the S or D electrodes. Therefore, for a fixed V_{ds}, each gate can create a barrier to only one type of carriers. For

example, G1 can enable or stop only the conduction of electrons, while G2 can allow or stop exclusively the flow of holes. The carrier types are then inverted when V_{ds} is inverted to a negative value. In order to switch the device from p-type to n-type, as shown in Figure 2.7(c), thus, both the V_{ds} and the polarization of the gate at the source side have to be reversed.

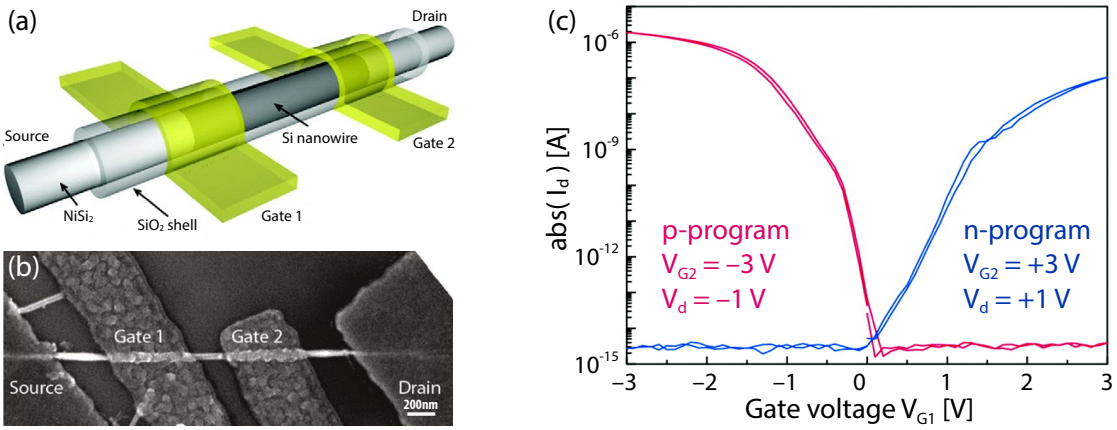

Figure 2.7 – (a) 3D conceptual view of the device proposed in [52], with two Ω-gate structures deposited on top of a bottom-up fabricated nanowire channel, in proximity of S and D metal electrodes. (b) SEM micrograph of a fabricated device and (c) I_d–V_{G1} transfer characteristics for the p-type (V_{G2} = −3 V) and n-type (V_{G2} = +3 V) polarizations. Note that the two characteristics are obtained for opposite V_d polarizations of respectively −1 V and +1 V. Image adapted from [52]

2.3 The proposed CP Schottky barrier nanowire FET device

The devices shown in literature provide interesting insights into the possibilities enabled by the added degree of freedom introduced by polarity control, and the use of advanced materials and geometries to concurrently obtain high device performance. However, further advances in device geometry, fabrication approach and device properties are needed in order to provide a foreseeable logic circuit design compatible and VLSI-capable device.

2.3.1 Device requirements

In the following, we summarize the main device requirements we aimed at fulfilling through our device design and fabrication. Table 2.2 proposes a simplified synopsis of the requirements and their key enablers, with a qualitative comparison of the devices from the state-of-the-art in terms of their closeness to our device concept.

Compatible gate voltages

A major requirement for the correct functionality of a transistor in a logic circuit is the compatibility between power supply voltages and gate voltages (V_{pg}, V_{cg}). Specifically, in a conven-

Requirement	Key Enablers	[45]	[47]	[46]	[29]	[48]	This work
Compatible gate voltages	Midgap S/D silicide, similar PG and CG electrode structure	☹	😐	☹	☹	😐	☺
Run-time polarity configuration	Symmetric PG geometry	☺	☹	☺	☺	☺	☺
Large scale integration	Top-down fabrication	☹	☹	☺	☹	☺	☺
Advanced geometry	Scaling-compatible structure, GAA, low SCEs	😐	☺	☹	😐	☹	☺

Table 2.2 – Synoptic table of the suggested device requirements: key enablers are qualitatively evaluated in the main devices from the literature.

tional logic circuit, the only available voltages for operation of logic gates are the reference V_{GND} and V_{dd}. As further described in the following chapters, the output of a logic gate built withing the complementary logic paradigm, can only range between V_{GND} and V_{dd}. Therefore, the gate electrode of a device fed by the output of a logic gate has to forcefully be driven by a voltage not exceeding this range. In order to allow negative voltages or larger voltage ranges for the gate inputs, voltage shifters have been proposed in literature, often relating to more complex design styles, e.g., ternary logic circuits [53].

In this work, we envision the use of our device in logic circuits where all voltages are compatible, i.e., negative voltages or voltages exceeding V_{dd} are not allowed. Note that no device in the current literature fulfills this requirement, due to the strongly asymmetric gate electrode design (see for example Section 2.2.2) or material tuning. In our work, on the contrary, we create a symmetric device design, with PG gate electrodes at both S and D channel sides, and employ mid-gap nickel silicide NiSi S/D contacts in conjunction with a low p-doped channel to shift the device characteristics in the correct operation ranges.

Large scale integration

While envisioning a roadmap to extend the capabilities of CMOS with a novel controlled polarity transistor, we gave fundamental importance to large scale device integration. As shown in Section 2.2, many devices shown in literature and expected to surpass conventional MOSFET performance are fabricated in a bottom-up fashion, through assembly of previously fabricated advanced channel materials such as nanowires, CNTs and graphene. In our technology, we instead rely on a top-down fabrication approach. In this case, the devices are fabricated all at the same time, starting from a bulk Si wafer (see Chapter 3) on which the devices are patterned in dense arrays.

Channel type	**Characteristic length**	**Value for $t_{Si} = 20\,nm$ and $t_{ox} = 2\,nm$**
Single gate	$\lambda_1 = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} t_{ox}}$	11 nm
Double-gate (FinFET)	$\lambda_2 = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} \left(1 + \frac{\epsilon_{ox}}{4\epsilon_{Si}} \frac{t_{Si}}{t_{ox}}\right) t_{Si} t_{ox}}$	10 nm
Gate-all-around (circular cross section)	$\lambda_\circ = \sqrt{\frac{2\epsilon_{Si} t_{Si}^2 \ln\left(1+\frac{2t_{ox}}{t_{Si}}\right) + \epsilon_{ox} t_{Si}^2}{16\epsilon_{ox}}}$	7.2 nm

Table 2.3 – Natural length λ for different device channel geometries, as defined in [55] and [58], where t_{ox} is the gate oxide thickness and t_{Si} is the channel thickness. For a surrounding gate configuration, the effective gate length can approach the nanowire thickness without suffering strong SCEs.

Advanced Gate-All-Around geometry

The last requirement we envisioned was the optimization of the device channel geometry to obtain the best possible electrostatic control over the channel by the gate electrodes. The natural choice in this case is a GAA structure, where the gate electrode is wrapped around one or more nanowire-shaped channels. This geometry is virtually the best in terms of suppression of SCEs such as *Drain Induced Barrier Lowering* (DIBL) and consequently V_{th} roll-off. A characteristic length λ can be defined for a certain channel geometry, so that if the effective gate length $L_g \gtrsim 5\lambda$, good suppression of SCEs can be guaranteed [54, 55, 56, 57]. Table 2.3 resumes the definitions of λ for typical geometries, ranging from one-gate thin film transistor to two-gate (similar to the FinFET case) to GAA. The example λ values, calculated for the case $t_{Si} = 20\,nm$ and $t_{ox} = 2\,nm$, show that the GAA geometry indeed allows for the most aggressive L_g scaling, with SCEs still well suppressed at $L_g \approx t_{Si}$where t_{Si} in this case equals the wire diameter.

2.3.2 Schottky barrier FET technology

The main reason for selecting a Schottky barrier device as base for our investigation is the peculiar ability of SB FETs to operate both as n-channel and p-channel devices using the same p-type substrate [41, 37, 36]. Specifically, SB junctions can operate with the same injection mechanisms both as inversion or accumulation mode devices, while doped p-n semiconductor junctions will allow carrier injection through thermionic emission only in forward (inversion) biasing mode. The direct consequence of this peculiar SB behavior is the strongly enhanced ambipolarity of a single gate SB FET characteristic. As previously described, we harness this behavior by means of the PG electrode, to obtain a device which performs well as either p-type

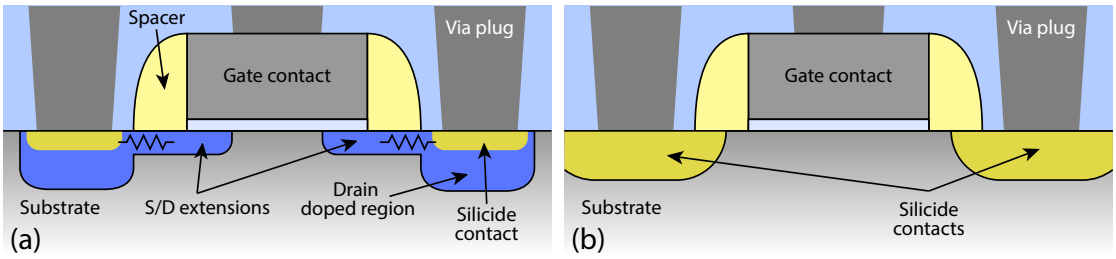

Figure 2.8 – (a) Conceptual cross section of a conventional bulk MOSFET structure. A complex series of lithographically masked dopant implantation/activation process steps are required to produce the S/D contacts. For simplicity, dopant wells and more advanced techniques such as halo regions are not shown in the picture. In (b), the greatly simplified silicided contact process is shown.

or n-type. A further, more general advantage of this effect is that all devices can be effectively built using the same type substrate, without requiring doping wells to produce p-type and n-type devices as is necessary in conventional CMOS processes. This leads to fabrication process simplification and occupied area reduction, since the overhead areas for well isolation and consequent lithographic design rules are relaxed.

In parallel to the functionality advantages provided by SB devices in our application, strong interest is currently given to SB devices as replacement for conventional DSD devices for their promising performance advantages.

The main reason for substituting conventional DSD MOSFETs is their high S/D contact access resistance. As device channel lengths are scaled down to nanometer dimensions (45 nm and beyond), DSD parasitic resistances are becoming more and more dominant with respect to reducing channel resistances. Metallic ohmic contacts, at the same time, are already employed in current industrial processes to contact back-end metal layers to front-end devices at the S/D, through metal via plugs and the use of silicide technology. As shown in Figure 2.8, the logic step towards metal S/D contacts is to eliminate highly doped S/D regions and access directly the device channel through rectifying SB contacts. Although this step requires the optimization of the SBs for correct device operation, we can describe several of advantages it provides with respect to doped S/D contacts:

- **Fabrication process simplification:** as previously stated, no dopant implantation and activation annealing steps are necessary in the silicided SB S/D process. No lithographic masks are required for the n-type and p-type species implantation and no high-temperature annealing (typically around 900 °C) is required, reducing the fabrication thermal budget and reducing constraints on high-κ gate stacks or 3D integration, which typically suffer from high temperature damage.

- **Contact resistance reduction:** as S/D regions shrink in size, in DSD devices, higher and higher dopant concentrations are required, with S/D extensions and halo implants

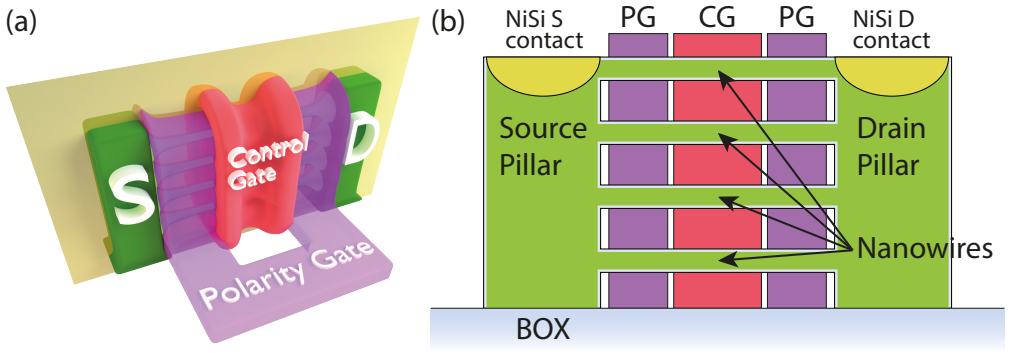

Figure 2.9 – (a) Position of the vertical device cross section. (b) Corresponding conceptual cross section of the device, showing the green S/D pillars sustaining a vertical stack of silicon Nanowires, with GAA PG structures in proximity of S/D electrodes and CG positioned at the middle of the channel.

further needed to guarantee device performance. Metal contacts, in contrast, inherently provide lower access resistance than DSD regions, allowing further and simpler scaling.

- **Junction abruptness and position:** in contrast to n-p semiconducting junctions, SB junctions built by Si bulk silicidation are inherently atomically abrupt, (see Section 6.2) providing the best possible contacts for strongly scaled device channel lengths. Moreover, as described more in detail in Section 6.3, junction position along the channel can be tuned without disrupting adjacent structures because of high temperatures or energetic particle implantation.

Further, at the back-end fabrication level, S/D regions have to be contacted through metal plugs (vias) to higher metal interconnect layers. At the same time, semiconducting S/D regions typically introduce a higher contact resistance than metallic regions. For this reason, state-of-the-art scaled technologies typically include S/D silicidation steps via intrusion of a metallic species in the crystalline silicon, such as nickel or cobalt [59, 60, 61], to minimize contact resistance.

By directly fabricating SB metal contacts, therefore, access resistance is minimized. Moreover, if doped S/D contacts are avoided, all the related masking, implantation and annealing fabrication steps are not necessary, to the benefit of a much simplified fabrication process (see Chapter 3). Interestingly, these relaxed fabrication constraints open possibilities in further integration directions. For its interest, we mention here monolithic 3D integration [62], which is strongly limited by processing temperature budget due to the bottom device layers being easily damaged by high temperatures. Typically, dopant activation in the higher device layers requires high temperature annealings ($\gg 600\,°C$) which in turn increase unwanted dopant diffusion, damage silicided contacts and in general reduce device performance [63]. In our process, no dopant implantation/activation is required, and a thermal budget of $\approx 400\,°C$ can be guaranteed, thus allowing for easier integration in these novel architectures.

Parameter	Symbol	Typical value
NW total length	L_{NW}	400 nm
PG length	L_{pg}	120 nm
CG length	L_{cg}	120 nm
PG to CG gap	L_{gap}	$\approx t_{OX}$
Oxide thickness	t_{OX}	5–8 nm
NW diameter	d_{NW}	20–50 nm
Pillar side length	L_{pil}	100–200 nm

Table 2.4 – Typical fabricated device dimensions.

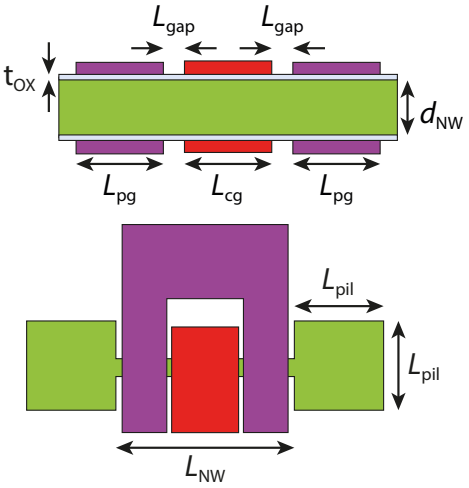

Figure 2.10 – Schematic view of the dimensions of Table 2.4.

2.3.3 CP SiNWFET geometry and switching mechanism

Figure 2.9(a–b) show a conceptual cross section of the proposed device structure. The cross section is vertical and along the length of the nanowires. Thanks to the simple device fabrication process, performed top-down using a tuned DRIE process step (see Section 3.2.1 for more details), an arbitrary number of silicon nanowires can in theory be produced as channel structure. Typically, the number of nanowires can range between 1 and 20 while maintaining good wire size uniformity in the stack. In our process, nonetheless, other limiting factors due to the high 3D topography of large nanowire stacks limit practical channels to 6 nanowires. Typical dimensions for the fabricated devices are summarized in Table 2.4 and Figure 2.10 and will be further discussed in Chapter 3.

The mechanism on which the proposed CP SiNWFET operates is inspired by the devices demonstrated in the literature and is described conceptually in Figure 2.11. The device has four regions of operation, corresponding to the four combinations of high/low bias voltages for each of the gate electrodes, PG and CG. The device is effectively ambipolar, in that electrons and holes both access the channel, although always in separate regions of operation, i.e., no superposition of minority and majority carriers is at any moment allowed in the channel when the device is correctly polarized. Note that the described device is *de facto* symmetric, both in terms of geometry and of polarization, i.e., it can operate both as n-type and p-type without changing any of its physical properties or connection configuration. Therefore, unless explicitly mentioned, in the following we define drain the electrode at the highest voltage between the two channel access contacts, independently of the polarization of the device. Note, specifically, that unlike the device described in Section 2.2.4, the PG electrode acts on both*Source* (S) and *Drain* (D) Schottky barriers simultaneously.

In order to illustrate the four modes of operation, we can first consider the selection of low (Figure 2.11(a)-(b)) or high ((c)-(d)) V_{pg}. In the first case, the bands at the sides of the device

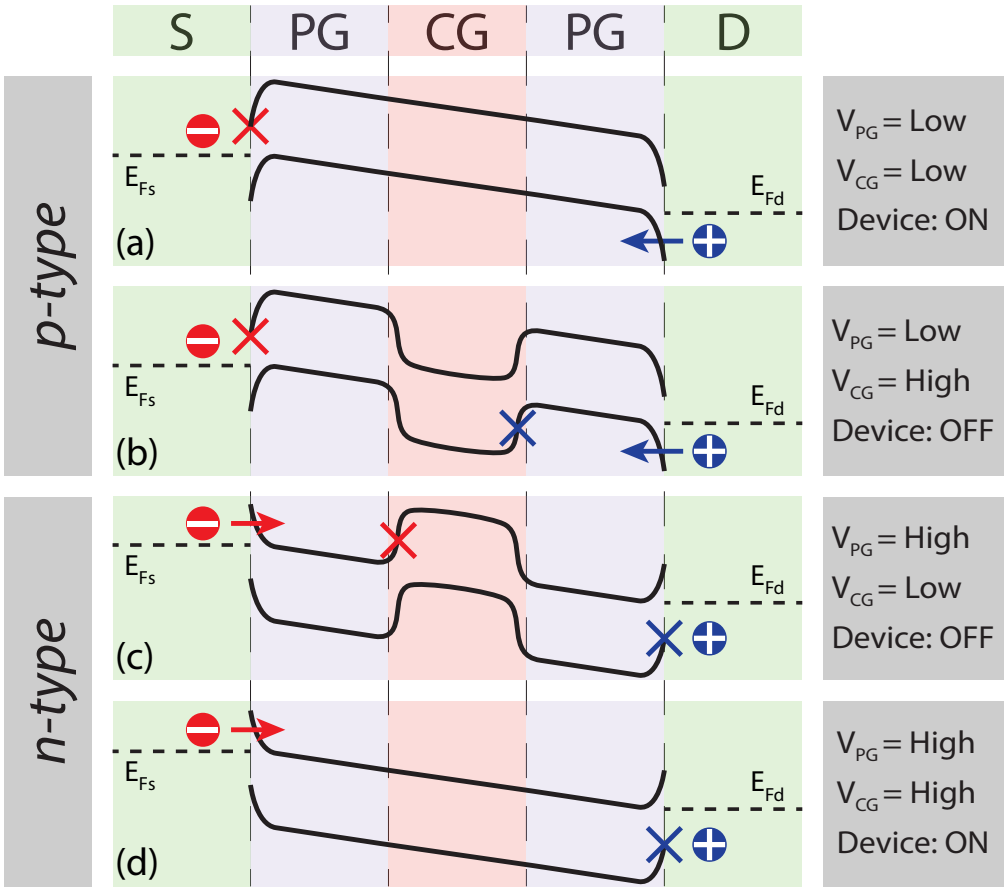

Figure 2.11 – Conceptual band diagrams for the controlled polarity SB FET device. Four cases are shown, describing the four combinations of high / low bias for the polarity gate and control gate of the device. Electron paths are shown with red arrows / crosses, hole paths are shown with blue arrows / crosses. Following the convention of Figure 2.3, the device is shown to embed the XOR functionality.

channel, in proximity of the S/D contacts, are pushed up, allowing holes to enter the channel from the drain electrode. On the other hand, if the V_{pg} is polarized at high voltage, the bands are pushed down, and electrons can access the channel from the source electrode. After the selection of the device polarity, the second gate electrode, the CG , conventionally acts on the middle section of the channel, creating a potential barrier in all similar to a conventional DSD FET device. However, due to the polarization change imposed by the PG , the CG effect will be symmetric in the case of n-type or p-type polarizations. Thus, when the device is set to p-type, a low V_{cg} is required for the channel to turn on. In contrast, when the device is set to n-type, a low V_{cg} will impede electron conduction, and the device will turn on when V_{cg} is high.

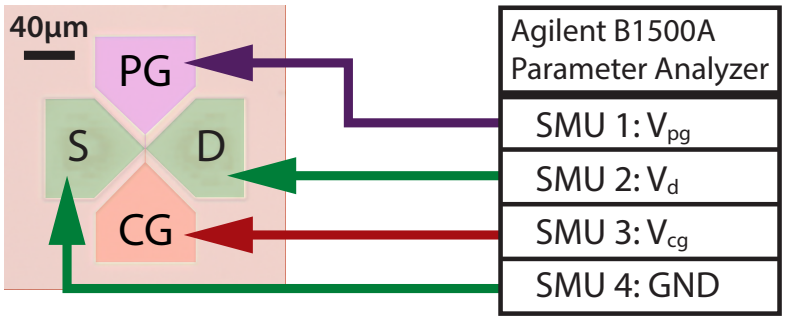

Figure 2.12 – Single device measurement setup. The measurements are performed landing four probes on large ($\approx 80 \times 80\,\mu$m) pads fabricated as extensions of the pillars or gate electrodes.

2.4 Device measurements

The following section reviews the experimental device measurements we performed on the fabricated devices. Particular focus is given on the demonstration of the proposed polarity control functionality. Further, measurements demonstrating the main characteristics of SB S/D contact operation are described.

2.4.1 Measurement setup

Static I–V measurements were performed using a Karl Süss PM8 probe station enclosed in a Faraday cage. Tungsten probes were directly landed on appropriately sized ($\approx 80 \times 80\,\mu$m) contact pads produced as extensions of the four device terminals: S, D, PG and CG . Unless otherwise stated, the wafer substrate as well as the source electrode were biased to GND (common source).

The measurements were acquired using an Agilent B1500 Semiconductor Parameter Analyzer, equipped with four high resolution (B1517A) SMU modules. Figure 2.12 shows an SEM micrograph of a device used for measurements, with the used probe connections.

2.4.2 Polarity control demonstration

In Figure 2.13 we show measured I_{d}–V_{cg} device characteristic for V_{cg} ranging between −1 V and 4 V, performed at various V_{pg} bias voltages, from −2 V and 4 V. Qualitatively, this set of characteristics demonstrate the basic device operation, showing the polarity control effect imposed by the PG electrode. As expected, the device behaves as a conventional n-type FET for high V_{pg}, turning on for high V_{cg} polarizations. This mode corresponds to case (d) in Figure 2.11. At $V_{\mathrm{pg}} = 0$ V, the device becomes p-type, showing increasingly stronger p-type polarization for more negative V_{pg}. Note that the fact of obtaining a p-type polarization for $V_{\mathrm{pg}} = 0$ V is fundamental for satisfying the first requirement described in Section 2.3.1, i.e., the device has to operate at all positive bias voltages. Conceptually, this requirement translates

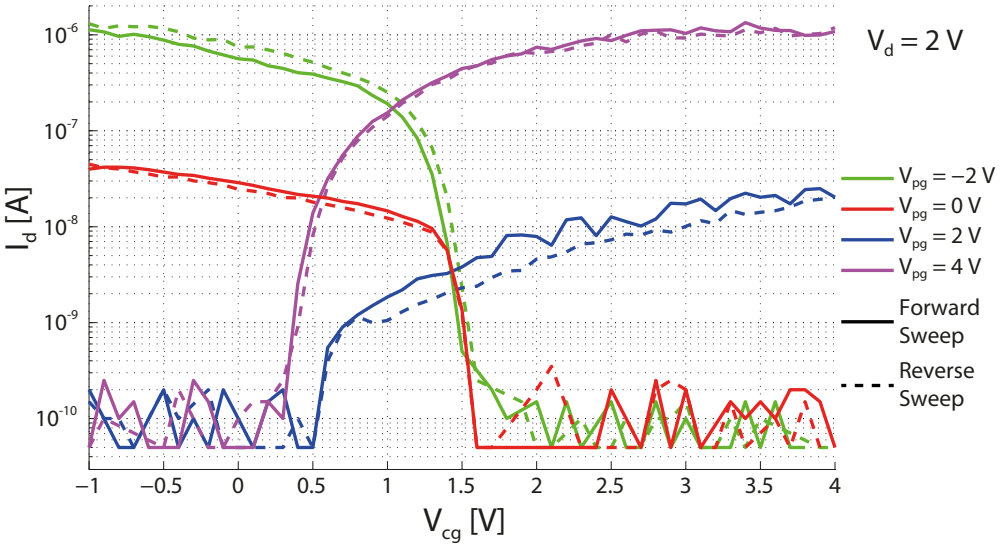

Figure 2.13 – Measured I_d–V_{cg} device transfer characteristic for various V_{pg} bias voltages, at V_d = 2 V. The device behaves as a conventional semiconductor to semiconductor thermionic barrier with respect to V_{cg}, due to the electrostatic doping effect imposed on the channel regions in proximity of S/D by the PG . The device is shown to be p-type up to V_{pg} = 0 V, and switch to n-type for V_{pg} > 0 V. Forward (solid lines) and reverse (dashed lines) sweeps of V_{cg} are shown, demonstrating the absence of relevant hysteresis effects during device operation.

into obtaining the crossover between p and n-type characteristics in the positive voltage range for both the PG and CG polarizations. To further clarify this effect, the equivalent I_d–V_{pg} (V_{pg} = −4 to 4 V) set of characteristics is shown in Figure 2.14 for various V_{cg} bias voltages, ranging from −4 to 4 V. Also in this characteristic, we correctly observe a crossing between p-type and n-type characteristics for V_{pg} > 0 V.

2.4.3 Subthreshold slope and I_{on}/I_{off} performance

Due to the presence of two gate electrodes simultaneously controlling device channel switching behavior, parameter extraction is not as straightforward as in the case of a conventional single-gate device. As introduced in Section 2.3.3 and shown in Figures 2.13 and 2.14, the two gate electrodes modulate channel conduction with different mechanisms. Specifically, the PG electrode acts at the extremities of the device channel, modulating the properties of the S/D Schottky barriers. At the same time, the CG electrode acts at the center of the channel, creating a semiconductor-to-semiconductor barrier, similar to a conventional DSD MOSFET barrier, due to the electrostatic doping effect imposed by the PG . We can thus extract SS and I_{on}/I_{off} values independently for the four operating conditions of Figure 2.11. Best-case SS and I_{on}/I_{off} values are shown in Figures 2.15 and 2.17 for, respectively, I_d–V_{cg} and I_d–V_{pg} characteristics.

The highest subthreshold performance is obtained for a fixed PG polarization, while sweeping

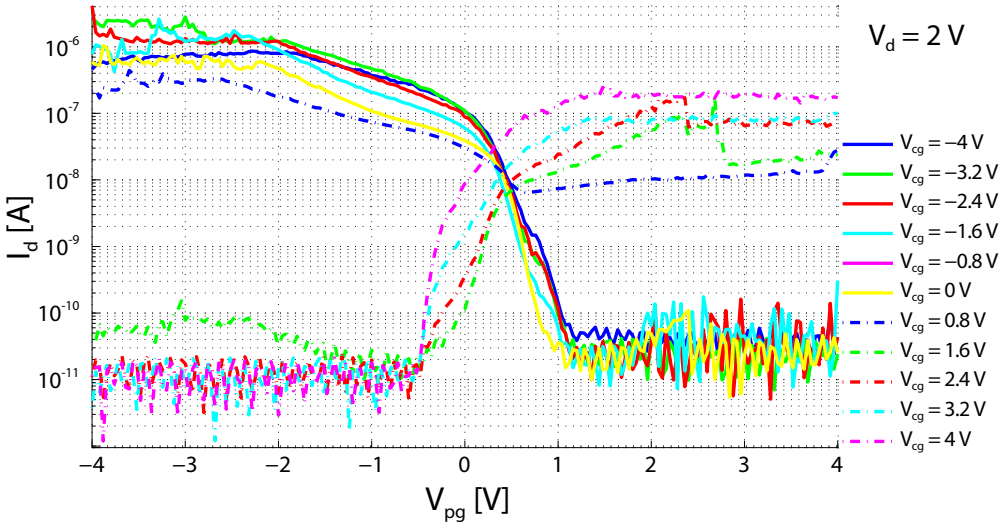

Figure 2.14 – Measured I_d–V_{pg} device transfer characteristic for various V_{cg} bias voltages, at $V_d = 2\,V$. The device is shown to switch between p-type and n-type with a crossing of the characteristics around $V_{pg} = 0.5\,V$. At strong polarizations, the plots show the tri-slope behavior typical of SB FET switching. Note that the device is in the on state for $V_{pg} = V_{cg} = 0\,V$ (yellow line), as expected for correct logic circuit design compatibility.

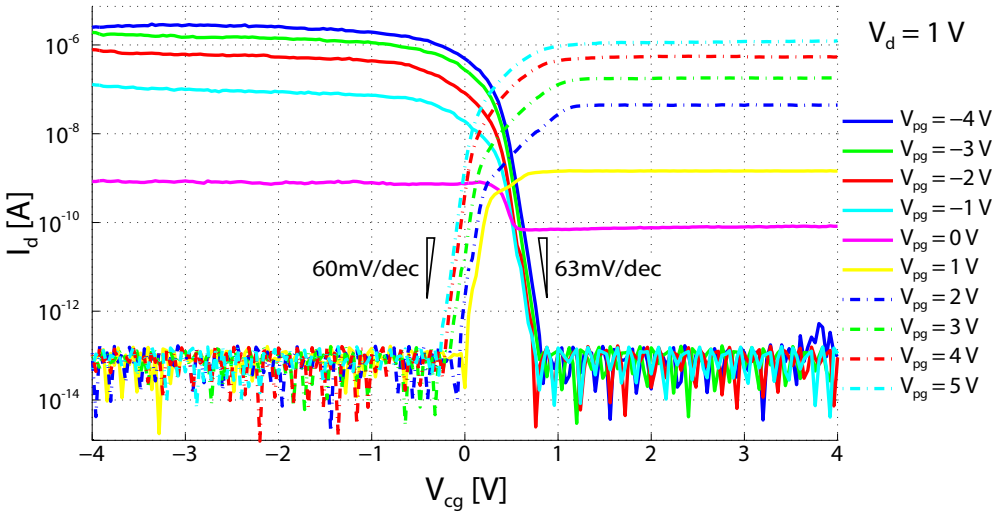

Figure 2.15 – Measured I_d–V_{cg} device transfer characteristic for various V_{pg} bias voltages, at $V_d = 1$,V. Subthreshold slopes are highlighted for the p-type and n-type characteristics. The values are shown for the case $V_{pg} = 4\,V$, with $SS \approx 60\,mV/dec$ and for $V_{pg} = -4\,V$, with $SS \approx 63\,mV/dec$. I_{on}/I_{off} performance reaches 10^8 for $V_{pg} = -4\,V$ and 3.5×10^7 for $V_{pg} = 5\,V$ in the same physical device. Note that I_{off} measurements are limited by our instrument bottom current range.

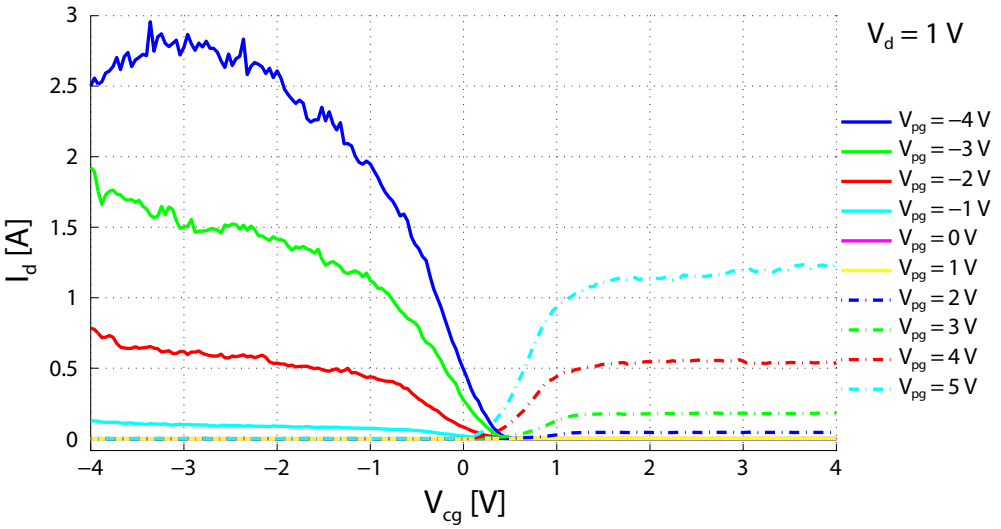

Figure 2.16 – Linear I_d–V_{cg} characteristics corresponding to the semi-log plot of Figure 2.15.

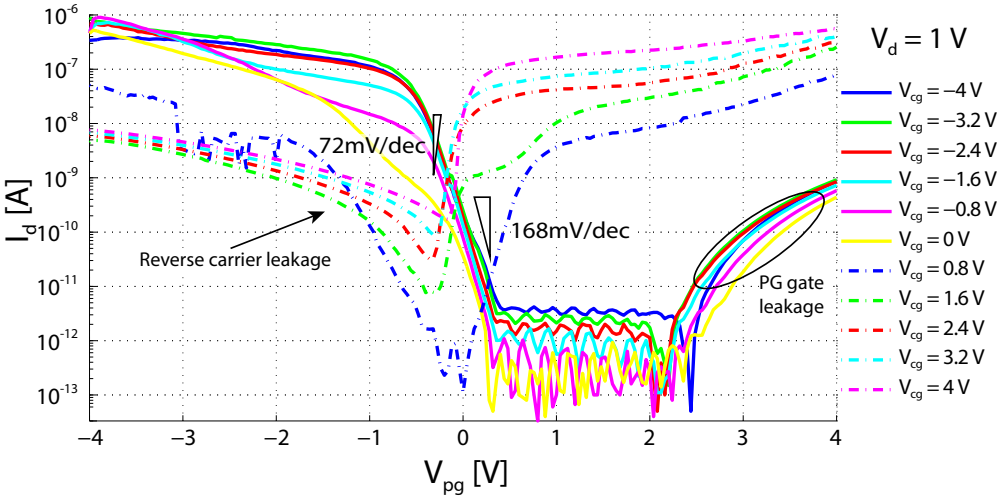

Figure 2.17 – Measured I_d–V_{pg} device transfer characteristic for various V_{cg} bias voltages, at V_d = 1,V. Subthreshold slopes are highlighted for the p-type and n-type characteristics. The values are shown for the case $V_{cg} = 4\,V$, with $SS \approx 72\,mV/dec$ and for $V_{pg} = -1.6\,V$, with $SS \approx 168\,mV/dec$. I_{on}/I_{off} performance reaches 10^6 for $V_{pg} = -0.8\,V$ and 7.5×10^5 for $V_{pg} = 0.8\,V$ in the same physical device. Note that in this device, for negative V_{pg} voltages, the CG does not efficiently suppress reverse leakage of holes from the drain electrode. At the same time, the characteristics for negative V_{cg} (solid lines) show strong leakage for high V_{pg} voltages. This is due to the appearance of parasitic PG gate leakage.

V_{cg}. Specifically, we obtained, for the case $V_{pg} = 4\,V$, an SS approaching the physical limit of $SS \approx 60\,mV/dec$ and for $V_{pg} = -4\,V$, an $SS \approx 63\,mV/dec$. I_{on}/I_{off} performance provides 10^8 for $V_{pg} = -4\,V$ and 3.5×10^7 for $V_{pg} = 5\,V$. Note that these values were all obtained in a single measurement on the same physical device. Moreover, the I_{on}/I_{off} measurements, as can be noticed in Figure 2.15, are limited by the minimum current resolution provided by our

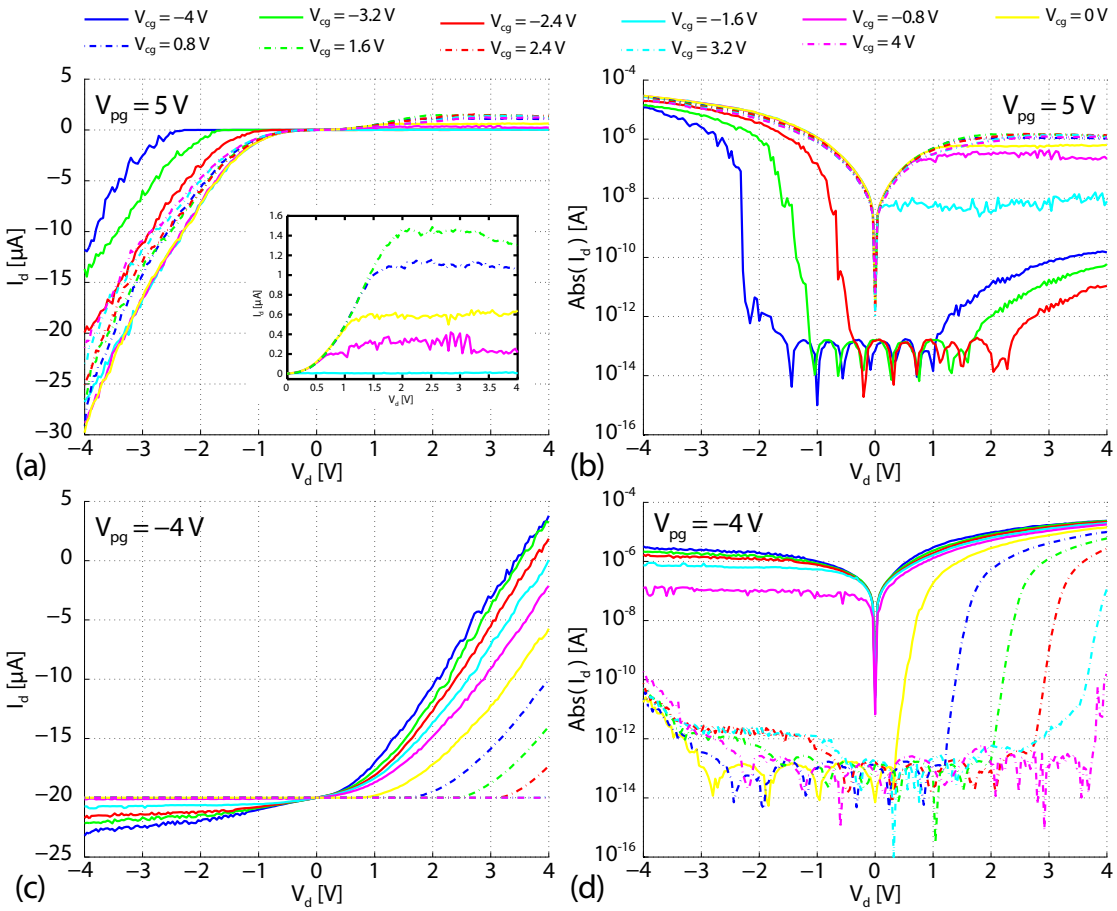

Figure 2.18 – I_d–V_d device output characteristics all measured in the same physical device at various V_{cg} polarizations, ranging from $V_{cg} = -4$ V to +4 V. (a) Linear I_d–V_d for a strong n-type polarization, setting $V_{pg} = 5$ V. The inset shows a zoom-in for positive V_d values. (b) Semi-log plot of the same data. (c) Linear I_d–V_d for a strong p-type polarization, setting $V_{pg} = -4$ V and (c) semi-log plot of the same data.

instrument setup. Finally, these values show that this device can provide high-performance combined with low-leakage (I_{off}), thus low-power aspects. This translates in relaxed constraints in terms of scalability and power consumption, which together summarize the biggest challenges currently faced by scaled CMOS technologies.

In Figure 2.17, SS and I_{on}/I_{off} values are shown for a V_{pg} sweep by fixing V_{cg}. The values are shown for the case $V_{cg} = 4$ V, with $SS \approx 72$ mV/dec and for $V_{pg} = -1.6$ V, with $SS \approx 168$ mV/dec. I_{on}/I_{off} performance reaches 10^6 for $V_{pg} = -0.8$ V and 7.5×10^5 for $V_{pg} = 0.8$ V in the same physical device. The device measured in Figure 2.17 is showcased as it provides good polarity gate SS performance. Nonetheless, in this device, high levels of I_{off} leakage are visible for the n-type characteristics (highlighted as reverse carrier leakage in the figure). Note that this leakage is the effect of minority carriers entering the channel, typically referred to as ambipolar leakage, which is usually observed in SB FET devices [36]. In contrast, in the measurement

presented in Figure 2.14, ambipolar behavior is strongly suppressed, by means of a more efficient CG electrostatic control, and no leakage is observed in the off state in either p or n-type characteristics.

2.4.4 I_d–V_d characteristics

To further evaluate device behavior, we measured I_d–V_d characteristics for p and n-type polarizations for the same physical device. Figure 2.18 shows measured I_d–V_d characteristics in linear (a) and semi-log scale (b) for a strong n-type polarization (V_{pg} = 5 V), and linear (c) and semi-log scale (d) for a strong p-type polarization, (V_{pg} = −4 V). Similarly to the I_d–V_g characteristics previously described, output behavior can be extracted separately for the n and p-type cases in the same device.

First, in Figure 2.18(a–b), we consider the case in which the PG selects electron conduction. For $V_d > 0$ V, normally saturated I_d–V_d characteristics are obtained [46]. Figure 2.19(a) shows a conceptual band diagram of this case, in which the main carrier injection barrier (for e^-) is at the S side of the channel. At increasing V_d, the barrier at the D side is modulated by V_d (symbol ↔ in the figure) creating an increasing e^- exit resistance which produces the saturation effect. If we now reverse V_d to negative values, we obtain a polarization which is normally outside the region of operation of the device, where V_{pg-d} becomes very strong (up to 9 V). Nonetheless, as shown in Figure 2.19(c), now e^- injection in the channel happens at the D electrode and is strongly modulated by V_{pg-d}, thus the characteristics do not saturate.

In the symmetric cases of p-type polarization (Figure 2.18(c–d)), the PG selects hole injection. For $V_d > 0$ V, then, the main barrier for carrier injection in the channel is at the D side (red circle in Figure 2.19(b)) and the barrier height is modulated by V_{pg-d}, thus no saturation is observed. For the case of $V_d < 0$ V, $V_{pg} < 0$ V produces a quite resistive at the D side, which is modulated by V_d and produces a saturation effect.

2.5 TCAD simulations

In order to make predictions about device performance and scaling properties, after measuring the fabricated devices, we built a simplified TCAD model using the same device architecture, considering a single low p-doped Si nanowire terminated by silicided S/D SB contacts. The model was fitted with experimental results and data from the Schottky barrier height extraction (see Section 6.2). Figure 2.20 shows the model-based device characteristic in comparison with the characteristic of an experimental device. Good agreement with the measured data is shown. In Figure 2.20, the p-type device branch (blue color) shows substantial leakage when $V_{cg} > 2$ V. As previously mentioned, we attribute this leakage to the lowering of the PG barrier to electron injection at the source electrode due to coupling of the very positively biased CG to the very negative V_{pg} = −4 V.

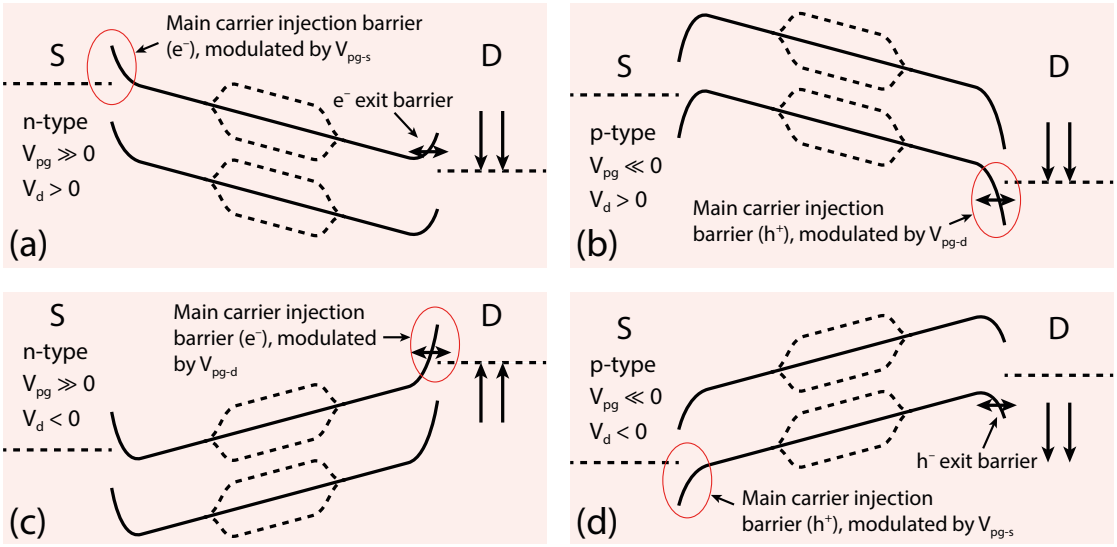

Figure 2.19 – Conceptual band diagrams describing the cases of Figure 2.18. (a) and (c): n-type cases, for $V_{pg} \gg 0\,V$ (see Figure 2.18(a)); (b) and (d): p-type cases, for $V_{pg} \ll 0\,V$ (see Figure 2.18(c)). The main carrier injection barrier is highlighted with a red circle, while a ↔ symbol shows the barrier most strongly modulated by V_{pg}.

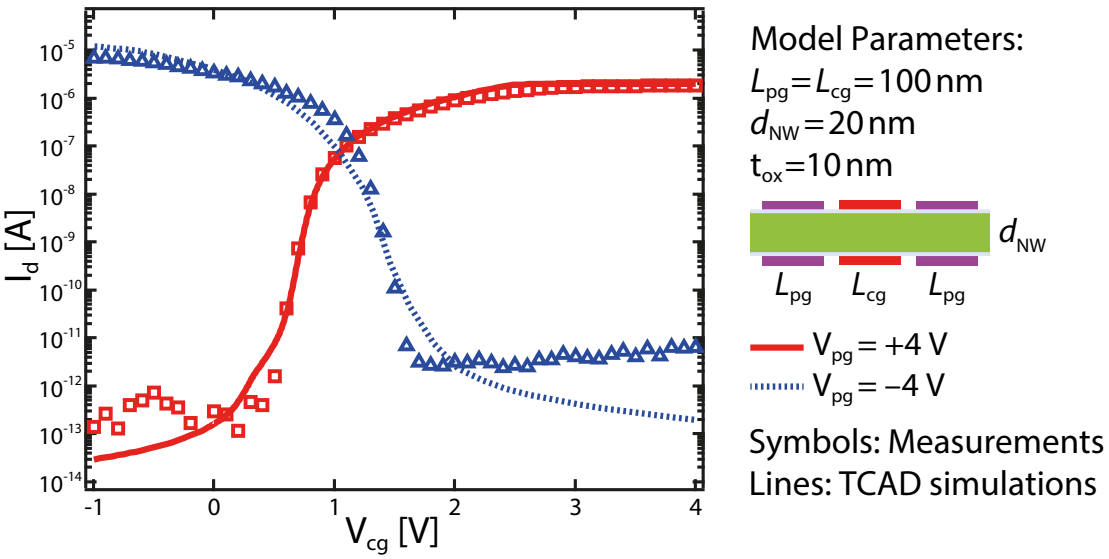

Figure 2.20 – Basic TCAD model fitting for the SiNW device. The model is built considering a single nanowire device channel, with dimensions adapted from the fabricated device parameters, with gated regions of 100 nm in length, nanowire diameter of 20 nm and relaxed gate oxide thickness of 10 nm. In the plot, measured (symbols) and simulated (solid lines) characteristics show good overlap, with the fabricated device presenting quite high reverse leakage in the region for $V_{cg} \gg 0\,V$ due to the very strong $V_{pg} = -4\,V$ polarization. Image adapted from [64].

2.5.1 I_d–V_d characteristics

I_d–V_d characteristics extracted using the fitted model are shown in Figure 2.21. As previously described in Section 2.4.4, output characteristics show a typical SB FET behavior, with a sat-

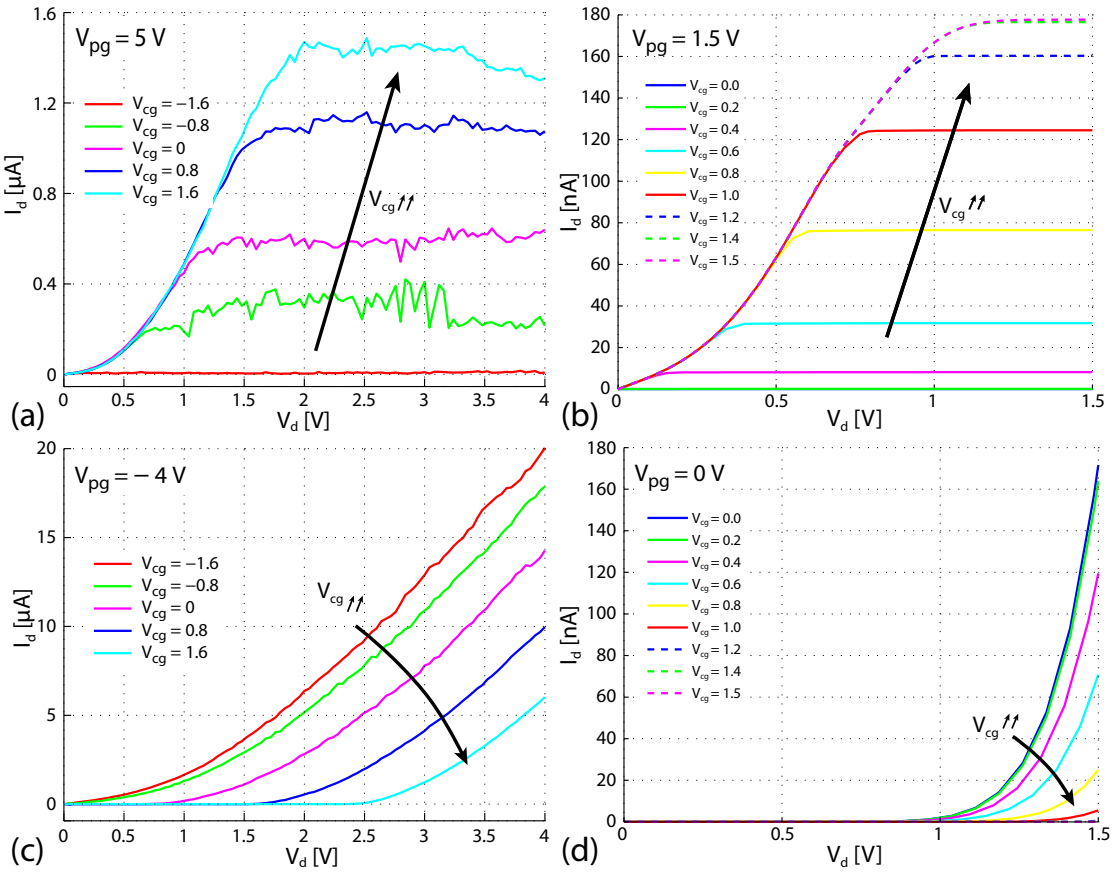

Figure 2.21 – Comparison of measured I_d–V_d device output characteristics with simulated characteristics using the basic TCAD device model described in Figure 2.20. (a) Measured I_d–V_d for $V_{pg} = 5\,V$ (strong n-type polarization) and (b) simulated characteristics for the n-type polarization. (c) Measured I_d–V_d for $V_{pg} = -4\,V$ (p-type) and (d) simulated characteristics for the p-type polarization. Qualitatively similar behavior is observed, with a sublinear region at very low V_d, typical for SB devices [65].

uration effect for the n-type case ($V_{pg} > 0\,V$, shown in Figure 2.21(a)) and no saturation for the p-type case, due to the main injection barrier (for h^+) shifting to the drain side of the channel when $V_{pg} \leq 0\,V$ (figure 2.21(c)). Characteristics simulated with less strong polarizations, respectively $V_{pg} = 0\,V$ and $1.5\,V$ for the p-type and n-type cases, and V_d up to $1.5\,V$ show a qualitatively similar behavior, with saturation in the n-type case (Figure 2.21(b)) and no saturation for p-type (Figure 2.21(d)). The expected sublinear region typical of SB FET devices [65, 36] is visible for very low V_d voltages in the simulated n-type characteristics.

2.5.2 I_d–V_{cg} vs. I_d–V_{pg} switching behavior

Figure 2.22 shows simulated I_d–V_{cg} (a) and I_d–V_{pg} (b) characteristics of the considered devices. In the case of I_d–V_{pg}, the side regions of the channel are polarized to a p-type equivalent

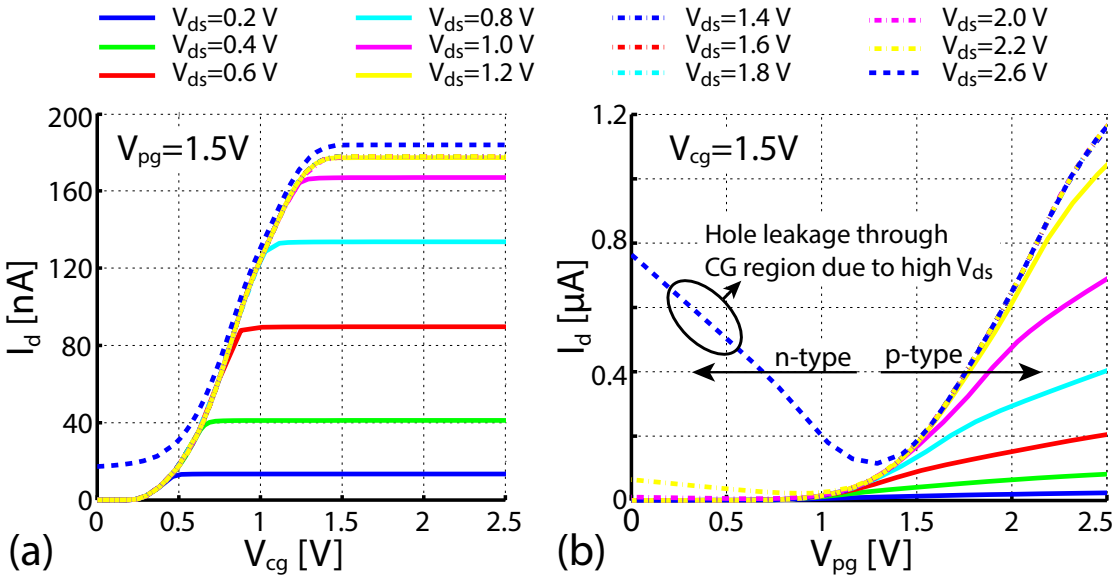

Figure 2.22 – Simulated I_d–V_g plots at different V_{ds}. (a) I_d–V_{cg} characteristics and (b) I_d–V_{pg} characteristics. Due to the asymmetry in geometry, different threshold voltages are expected in the two characteristics. Image adapted from [66].

electrostatic doping by the high (1.5 V) PG bias. Note that the two gate structures (PG and CG) act sequentially on the carrier injection from S/D , with the PG bias first setting the maximum current flowing through the channel, and the CG bias conventionally switching on/off the device. Thus, for increasing V_{cg}, current saturation is observed in Figure 2.22(a) when all the carriers entering the channel at either the source or drain regions are also allowed to flow through the CG region. Nonetheless, at high V_{ds} biases (>2.5 V) and low PG biases (<1.5 V), strong leakage is observed in the channel. This is mainly due to the thinning of the Schottky barrier at the drain, that allows holes to flow through the channel without being stopped by the CG barrier, resulting in a strong ambipolar behavior. In terms of circuit performance, the two gate structures have different influences on the channel, both in terms of geometry (length) and influence on the Schottky barriers. This directly translates into different fingerprints for the two I_d–V_g characteristics, with the $V_{th,pg}$ threshold being significantly higher (≈ 1.4 V) than the $V_{th,cg}$ threshold (≈ 0.5 V).

2.5.3 Optimized device model and simulations

We reduced dimensions and modified material parameters to evaluate performance of the device at a scaled technology node. At the time of this analysis, we considered a node with 45 nm critical dimension [49]. The applied dimensions and materials are summarized in Figure 2.23, along with a conceptual 3D view of the nanowire channel with the three gate regions wrapped along the channel and S/D capping Schottky contacts. Same as for the non-optimized case, in the following simulations we considered a device comprising a single nanowire channel. The optimized structure includes high-κ gate dielectric, metal gates

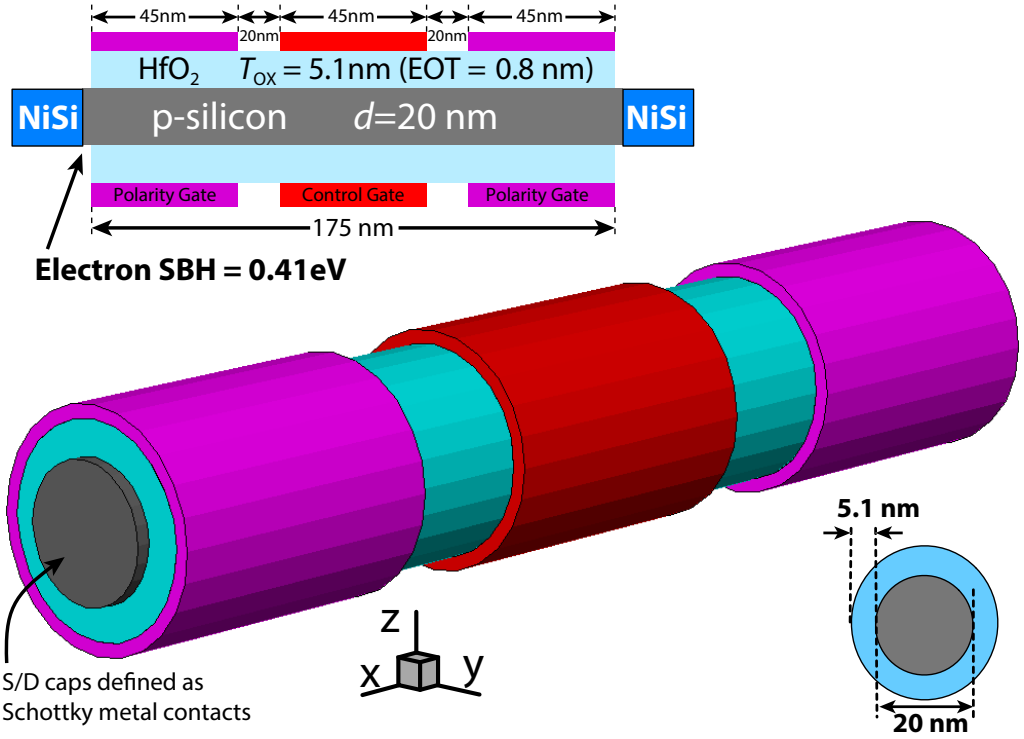

Figure 2.23 – Structure of the optimized controlled polarity SiNW device structure with three, 45 nm-long gate regions. High-κ gate dielectric and metal gate with mid-gap work function are introduced to evaluate device performance after tuning of dimensions and materials. Schottky barrier height $q\Phi_{B_p}$ for electrons is fixed at 0.41 eV at bothS and D electrodes. Image adapted from [64].

with mid-gap work function and 45 nm long gate regions. Schottky barrier height $q\Phi_{B_n}$ for electrons is fixed at 0.41 eV at both source and drain junctions. The I_d–V_{cg} characteristics of the optimized device are shown in Figure 2.24, obtained with hydrodynamic transport and quantization models. Tunneling masses for electrons and holes are set to 0.19 m_0 and 0.16 m_0 respectively, consistent with theory and measurement fitting.

We show in Figure 2.24 the optimized I_d–V_{pg} characteristics for the optimized TCAD model. The characteristics are shown in linear (left) and logarithmic scales (right axis) for both n and p-type polarizations for V_{ds} = 1.2 V. As observed for the non optimized and measured cases, the peculiar device symmetry with p and n-type characteristics crossing at $V_{cg} = 1/2\ V_{ds}$, enable operation at all positive voltages, with compatible V_{cg} and V_{pg} input ranges. Note that the curve crossing in the I_d–V_{cg} plot is shifted to lower V_d, 0.6 V, with respect to the non-optimized case (see Figure 2.20) ($V_d \approx 1.1$ V). This reduction would allow a power supply voltage lowering still providing steep SS and good I_{on}/I_{off} performance. Note that these models, the non optimized as well as the one based on the optimized and scaled structure, will serve as basis for the mixed-mode simulations at logic gate level shown in Chapter 4.

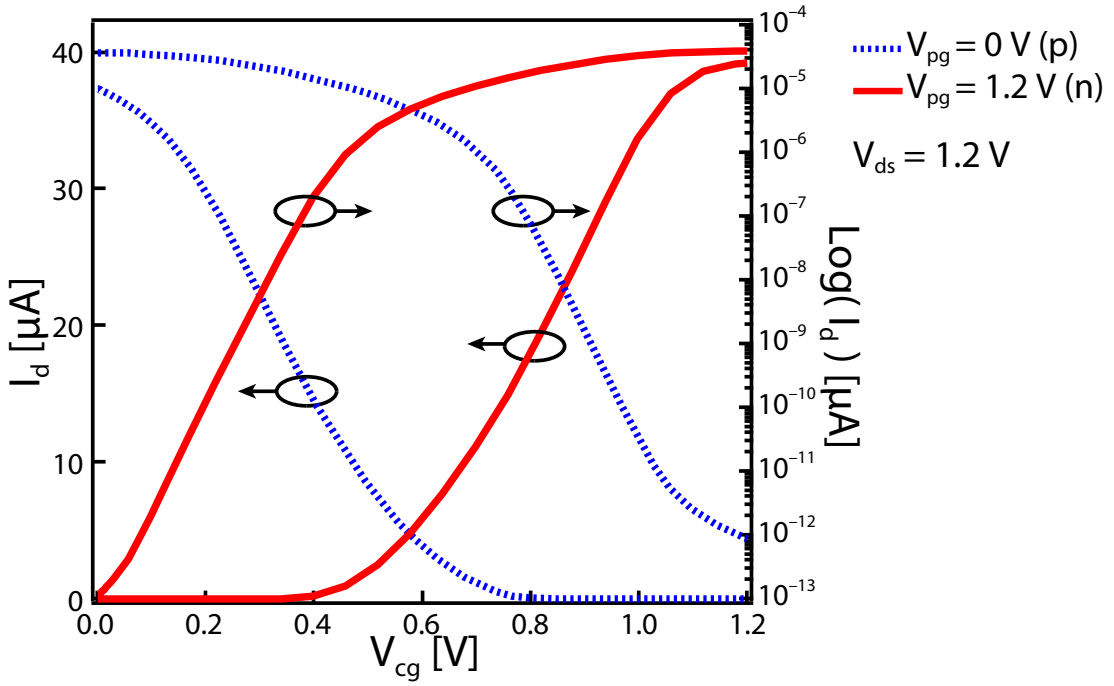

Figure 2.24 – I_d–V_{cg} characteristics of the optimized device as predicted by TCAD simulation. Symmetric characteristics for n-type (blue curves) and p-type (red curves) polarizations are observed, respectively, bat V_{pg} = 1.2 V and V_{pg} = 0 V. For both polarizations, linear (left axis) and logarithmic (right axis) plots are shown.

2.6 Chapter summary and contributions

In this chapter, we introduced the controlled polarity Schottky barrier SiNWFET device which represents the main research contribution presented in this thesis. A novel device was designed to provide in-field electrostatic polarity control at the same time as high performance characteristics.

Specifically, the demonstrated device enables for the first time the combination of three fundamental elements:

Polarity control at compatible gate voltages

The device shows state-of-the-art control of the polarization (n to p-type) for voltage ranges withing 0 V and V_{dd} for both the PG and CG electrodes, enabling straightforward cascading of logic gates built with this technology.

High performance characteristics

The device shows quasi-ideal measured SS steepness of respectively ≈ 60 mV/dec for n-type and ≈ 63 mV/dec for p-type polarizations. At the same time, observed I_{on}/I_{off} performance reaches 10^8 for $V_{pg} = -4$ V and 3.5×10^7 for $V_{pg} = 5$ V all in the same physical device.

VLSI-compatible device design

The device is designed with a best-case 3D GAA based channel geometry, employing top-down fabricated nanowire stacks (see Chapter 3) for large scale fabrication compatibility. Low I_{off} leakage and excellent subthreshold characteristics reduce constraints in terms of prospective scaling potential and low power operation, both of paramount importance for the density requirements of current logic circuit technologies.

Finally, our fabricated devices are the first demonstrated so far to combine remarkable device characteristics with sufficient symmetry and compatible operating voltages to enable complementary multi level logic synthesis.

We consider this work as a proof of concept for the use of *Double Gate* (DG) devices in future circuit design. However, numerous improvements could be implemented in order to improve the device characteristics and reduce dimensions. First, at the technology level, high-κ gate dielectric materials and metal gates, together with channel strain techniques can be directly applied to the presented structure. As shown in the simulations of Section 2.5, these elements would provide further degrees of freedom to better tune device symmetry and control of polarization thresholds.

In the next chapters, we will discuss more in detail the fabrication approach we employed to physically produce the measured device, and their application in constructing small logic gates.

3 Device Fabrication

This chapter provides a detailed description of the process flow developed in this thesis work and implemented to physically fabricate the controlled polarity devices. Characterization at device level is proposed in Chapter 2, while Chapter 4 describes the scale-up of this technology to two- and four-transistor logic gates. As previously described, we chose a top-down, silicon nanowire-based device fabrication approach. In our work, nanowires are fabricated in vertical stacks using a single DRIE etching step. In the following, we describe more in detail the geometry and dimensions of the presented device. First, we introduce the most common NW fabrication methods used in literature and their advantages/disadvantages. We then introduce the complete implemented fabrication process flow with some details on the challenges and methods employed to obtain the final measured devices.

3.1 CP SiNWFET structure motivation

In parallel with the performance and scaling advantages provided by the nanowire GAA channel geometry (see Section 2.3.1), we considered the advantages of top-down fabricated nanowire stacks in terms of simplicity and cost-effective fabrication.

Channel geometry: from bulk to nanowire

The recent years have seen a rapid evolution of FET device channel geometries. The transformation saw at first the shift from bulk to thin-film structures. Specifically, in bulk devices, the channel electrostatic integrity [57] had strong scaling limitations due to the thick channel volume allowing drain-side electrostatics to influence channel conduction. This caused the increase of SCEs to intolerable levels and the risk of channel punch-through at very short gate lengths. *Partially Depleted SOI* (PDSOI) [67] and *Fully Depleted SOI* (FDSOI) [68] transistors then appeared, bringing the possibility to reduce channel doping steps and doping complexity, while at the same time better confining drain electrostatic influence over the channel. This ultimately enables more aggressive scaling and lower channel doping levels, reducing

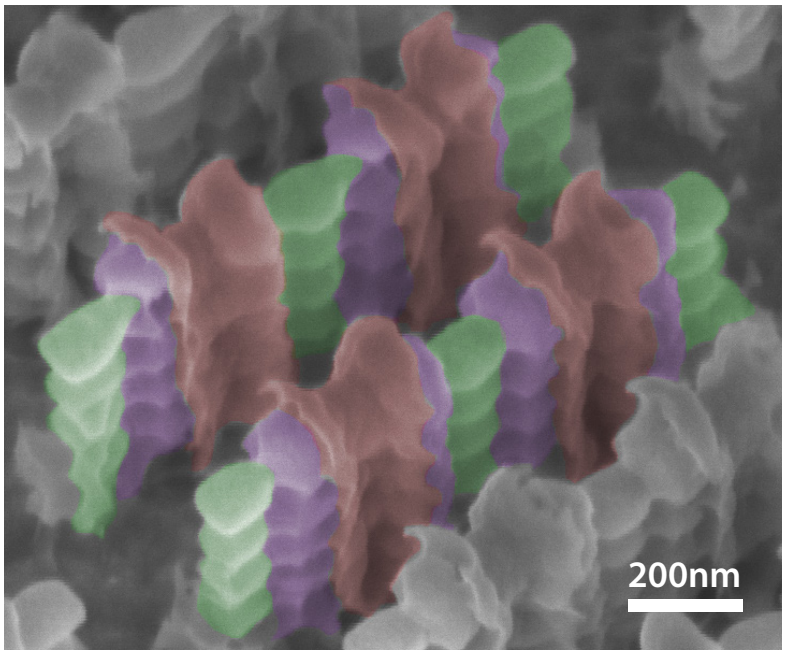

Figure 3.1 – Tilted SEM micrograph of a fabricated four-transistor tile. False colors show the nanowire stack sustaining pillars (green), with Polarity (violet) and Control gates (red) wrapped around the NW channel.

variability among devices. In order to further increase device density and gate electrostatic control over the channel, FinFETs were developed and are currently a mainstream industrial technology for high-performance logic circuit implementations. FinFETs are fabricated in a vertical fashion [8], bringing the device structures into the third dimension. Moreover, in the case of the devices presented by Intel in 2011 [2] and in 2014 [3], the device fins are not isolated via an insulating layer from the bulk substrate, thus effectively not requiring a an SOI substrate to be fabricated.

In-house state-of-the-art nanowire fabrication

In our process, we go one step further, and produce device channels made of a vertical stack of horizontal nanowires. In particular, the proposed devices are based on a single bulk silicon etching procedure (described in detail in Section 3.2.1). Among other state-of-the-art techniques, we chose DRIE due to a number of previous works, carried out in our facilities to target the fabrication of FET devices [33, 31] and dense nanowire arrays [32]. In this context, the process parameters we use in the presented device fabrication is an adaptation of these earlier processes, which created a foundation in terms of reliability and stability using our specific etching equipment.

Relaxed constraints for a delicate process flow

As we will describe further in this chapter, the fabrication approach we employed to create the stacked SiNWFET devices requires the fine-tuning of a number of critical process steps, namely, three e-beam lithography patterning steps, the DRIE-based nanowire and gate electrodes etching step and the final nickel silicidation of the contacts. At the same time, the proposed device dimensions, introduced in Section 2.3.3, stand close to the limits of resolution and performance of the available equipment at our fabrication facility. In this respect, the final device structure reflects our effort in keeping materials simple (e.g., silicon channel and polysilicon gates) and constraints as relaxed as possible (≈ 8 nm gate oxide thickness), as to create an effective equilibrium between device performance and fabrication complexity, which ultimately enabled the fabrication of the first fully functional devices exhibiting the proposed polarity control behavior.

3.2 Nanowire fabrication

A number of techniques have been proposed in literature to fabricate semiconducting nanowires to be used as FET device channels. Due to the inherent discrete object nature of nanowires, these wire-like structures can be fabricated with top-down or bottom-up approaches. With top-down, we intend any methodology where structures are etched out of a whole (e.g., a crystalline substrate), whereas bottom-up means the structures are grown from precursor gases and particles, and subsequently assembled and positioned to create the device channels. We summarize here the main methodologies proposed in literature, highlighting pros and cons of each category. We include bottom-up techniques since the sought polarity control effect is independent from the chosen channel fabrication methodology, and can in principle be applied to any scaled technology, including Fin-based or any wire-like configuration.

Generally, top-down fabrication approaches have several advantages, and are currently employed in all CMOS industrial processes:

- Integration of device in large scale is inherent to these methods, since device shapes are drawn once on a lithographic mask and then transferred by lithography on a substrate. Device-to-device variability can be easily reduced by using dummy structures and advanced patterning techniques. Moreover, device position, density and distribution on a substrate can be controlled by patterning.
- All processes happen on the final substrate. There is no need to add separate processing steps to produce some device parts (e.g., the nanowire channels) which would then have to be transferred to the final substrate with additional risk of increased variability and contamination by unwanted chemical species.
- Channel structure and properties are all equal by construction. Bottom-up fabricated structures normally rely on precursor particles which vary in size and shape, leading to

the fabrication of wires that are always different, in terms of cross-section and length.

Top-down methods allow for a direct and reliable integration of many devices. However, they do not allow the same flexibility in the design of the actual channel structures:

- Top-down fabricated devices rely on lithographic patterning to produce the device channels, typically by etching. Therefore, any irregularity in the lithographic mask and *PhotoResist* (PR) (typically, *Line Edge Roughness* (LER)) will translate into a source of variation at device level. Grown structures can instead be fabricated with atomically smooth surfaces.
- Grown nanowires can be processed to create core-shell radial layers directly in the growth CVD chamber, creating high quality transitions between materials along the wire radius.

3.2.1 Top-down methodologies

Deep reactive ion etching

The methodology implemented in our process flow is based on dry DRIE (or Bosch) process, from the original patent developed in 1996 [69]. DRIE was developed to produce near-vertical walls with high aspect ratios using dry etching. This method consists of alternating a quasi-isotropic etching step, based on SF_6 for silicon, with an organic passivation step based on Octafluorocyclobutane (C_4F_8). Figure 3.2(a–f) shows a schematic view of a DRIE cycle, applied to the fabrication of nanowires. After creating a thin photoresist line on a substrate, the first step of DRIE consists of an isotropic Si etching step, lasting one to a few seconds, creating a groove with a small undercut at the edges of the photoresist pattern. After the etching step, a thin passivation layer is deposited by polymerization of a second precursor, C_4F_8, which effectively inhibits further Si etching on the surfaces shadowed vertically by the photoresist mask. Only the horizontal exposed surfaces are cleaned from the organic layer by the partly physical SF_6 etching. Using this method to fabricate nanowires was originally proposed in 2007 by Ng *et al.* [70] and further developed by Sacchetto *et al.* [33] to fabricate SiNWFET devices . The method consists of reducing a photoresist line width to less than twice the undercut width produced by the isotropic etching step in the DRIE process.

Figure 3.3 shows a SEM image of pillar and nanowire structures patterned and etched in bulk silicon. Scalloping due to the cycling nature of the etching is visible on the sidewalls. Where the pattern width becomes thin enough, the scallops at the two sides of the pattern touch, releasing discrete nanowires. The number of scallops typically indicates the number of etching cycles, although the first isotropic etching step may not result in a visible groove, because of the breakthrough time required to initiate the Si etching at the surface, due to native oxide and residual molecules from the previous photoresist development.

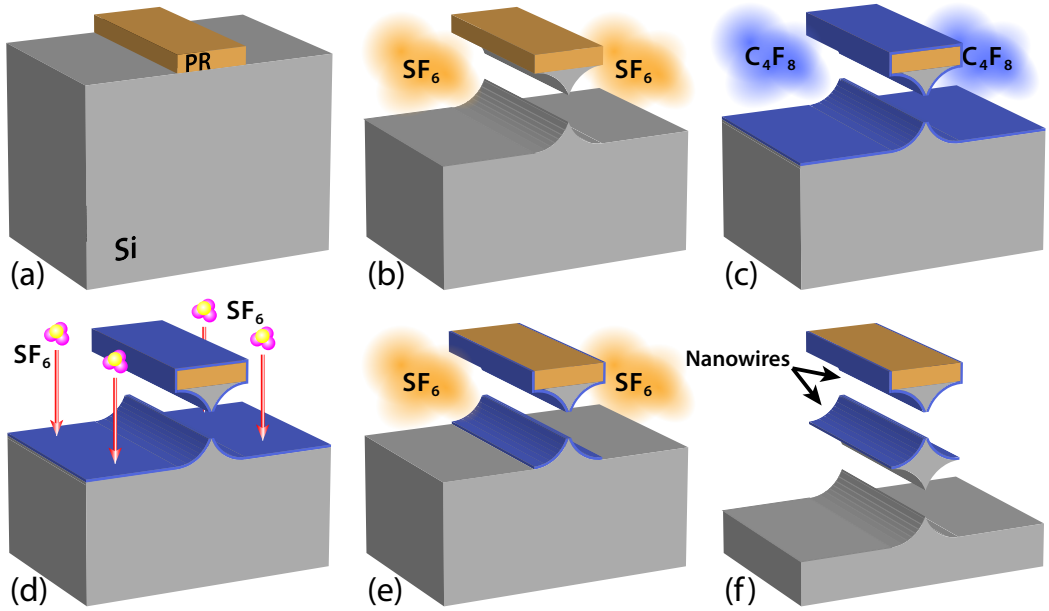

Figure 3.2 – Deep Reactive Ion Etching applied to nanowire fabrication. (a) a photoresist mask is applied on crystalline silicon; (b) physical/chemical SF_6 etching is applied, creating an undercut below the mask pattern; (c) conformal thin passivation is applied using C_4F_8 gas; (d) the vertically accessible surface passivation is readily removed by the partly anisotropic SF_6 etching; (e) finally, a new undercut is produced by chemical etching by the SF_6, leading to (f) a new nanowire.

SiGe superlattice method

A second top-down approach to fabricate Si nanowires exploits the high etching selectivity between Si and SiGe layers to create the nanowires by underetching a SiGe layer below a Si trench. This approach has been implemented in [71] to create twin SiNWFETs, and in [72, 73] to produce Si nanowire stacks. The method steps are depicted in Figure 3.4(a) from top to bottom: a superlattice of multiple pure Si and SiGe alloy layers are grown epitaxially. Then, a photoresist pattern is created on the top surface of the stack, and an anisotropic dry etching step is performed to create a fin-like structure. Finally, the SiGe alloy layers are removed by selective wet etching and rectangular nanowires are released between two supporting pillars.

Compared to the DRIE based method, in this case the process requires the extra cost of fabricating the Si/SiGe superlattice, and employing two different etching methods to produce and release the nanowires. Moreover, nanowire quality depends on the Si layer quality, and seamless monocrystalline nanowires are difficult to fabricate reliably with this method. At the same time, this method also suffers from photoresist LER influencing the nanowire shape as in the case of DRIE.

One advantage of this method, is the possibility to fine-tune nanowire shape, in terms of width and height, and create more freely designed structures such as horizontal beams/fins or

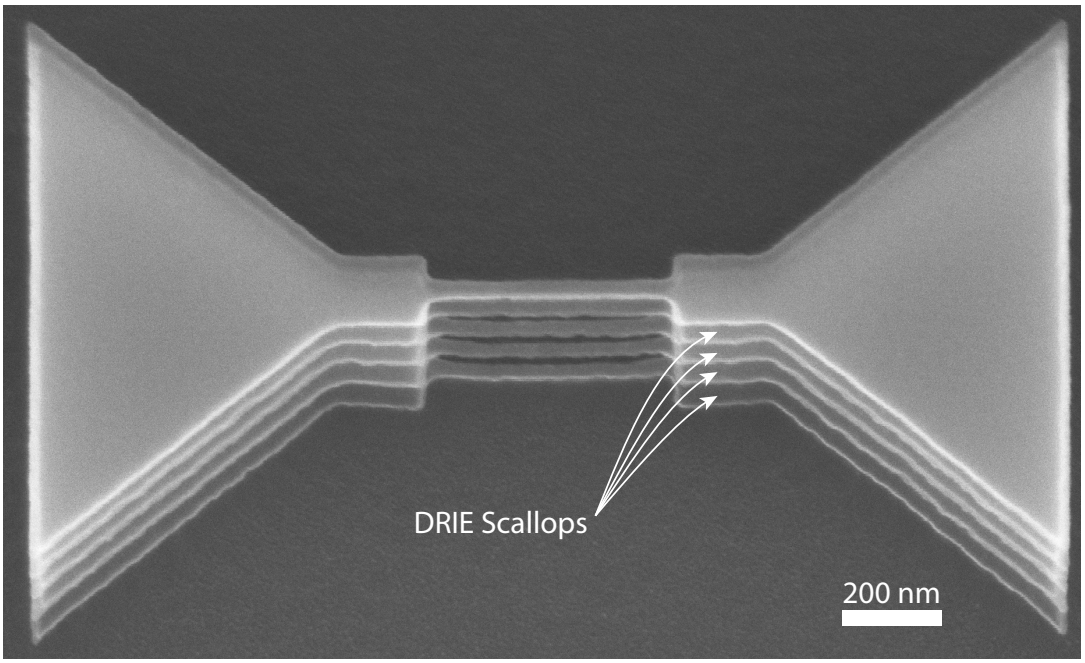

Figure 3.3 – SEM micrograph of a structure etched using DRIE on a silicon bulk wafer. Scalloping due to the cycling nature of the etching is visible on the sidewalls. The number of scallops typically indicates the number of etching cycles, although the first isotropic etching step may not result in a visible groove, due to the surface imperfections, including native oxide, require a breakthrough time.

wires of different thickness. Figure 3.4(b) shows some fabricated structures from the literature, including crystalline nanobeams with a HfO_2 and polysilicon GAA stacks [73], and (c) single nanowire stacks [72].

3.2.2 Bottom-up methodologies

In contrast with top-down fabrication methods, other groups have opted for a bottom-up approach, consisting of fabricating the nanowires as discrete objects via a chemical or physical method [74, 75]. As previously mentioned, an advantage of bottom-up approaches is the possibility to produce nanowires with controlled thickness profiles and different materials, e.g. Ge/Si core/shell NWs. This comes at the cost of the difficulties in selecting, aligning and positioning the nanowires on the final substrate, which are currently the main limitations to large scale integration of devices built with these methods.

Bottom-up methods include a large variety of techniques allowing the growth of nanowires of different lengths, cross-sectional profiles, materials and properties. Typically, growth is initiated using catalyst nanoparticles which are put in a reactive atmosphere containing a silicon (or other elements) precursor species. The precursor reacts with the surface of the nanoparticle depositing the silicon, and a wire grows in a certain direction from the

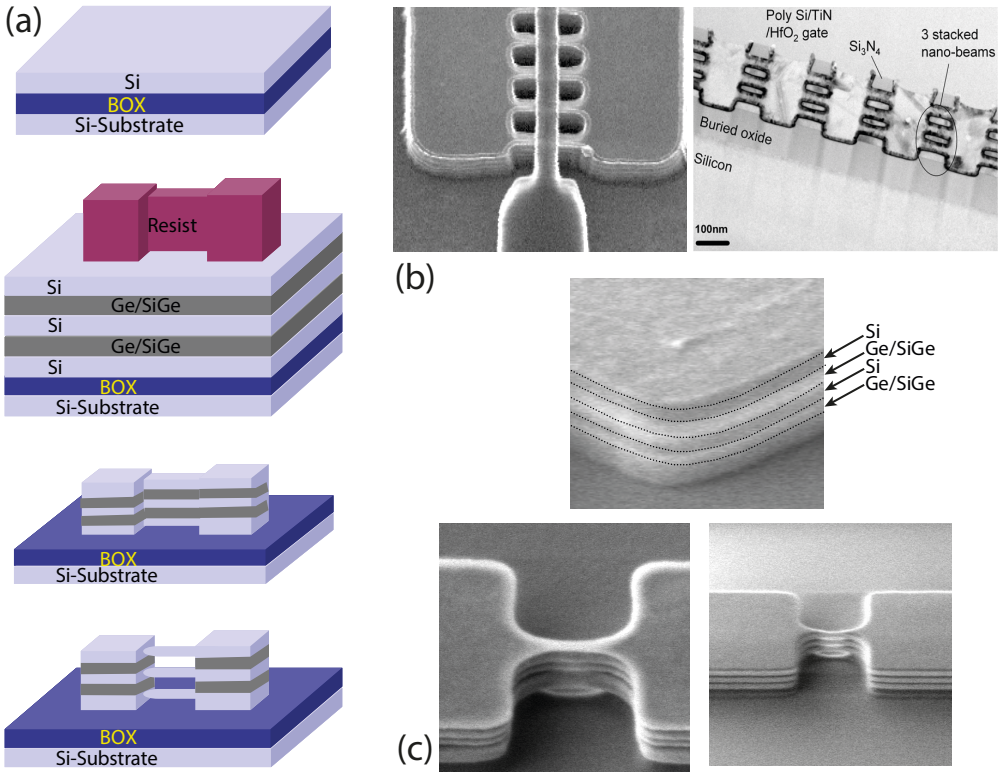

Figure 3.4 – (a) Process flow for Si/SiGe superlattice stacked nanowire fabrication (image adapted from [72]). (b) SEM micrograph and TEM cross section of fabricated densely packed crystalline silicon nano-beams, including conformal HfO_2 and polysilicon GAA electrodes (images adapted from [73]). (c) Etched sidewall of a Si/SiGe epitaxial superlattice, with highlighted layers grown on the BOX of an SOI substrate. In the bottom-left image, the wire structures appearing after SiGe wet etch and in the bottom-right image, the nanowires being released and reduced in diameter after self-limiting oxidation and oxide removal. Images adapted from [72].

particle. Figure 3.5(a–f), shows a schematic view of the the experimental setups of different techniques employed to provide the precursor Si to the catalyst nanoparticle surface and grow the wires. These techniques [76] include CVD, annealing in a reactive precursor-rich atmosphere, evaporation and reaction of SiO_2 as a precursor, *Molecular Beam Epitaxy* (MBE), laser ablation of a precursor target and finally, a wet environment growth, allowing the use of different, non-gaseous precursor molecules.

Directed growth and transfer techniques

Since the nanowires are grown as discrete entities, they need to be transferred on a final substrate to be used as transistor channels. Therefore, literature on nanowire transfer techniques [77] and directed growth [78], allowing to produce as regular and uniform nanowire arrays as possible, is intrinsically related to the growth methods. Moreover, transfer techniques can

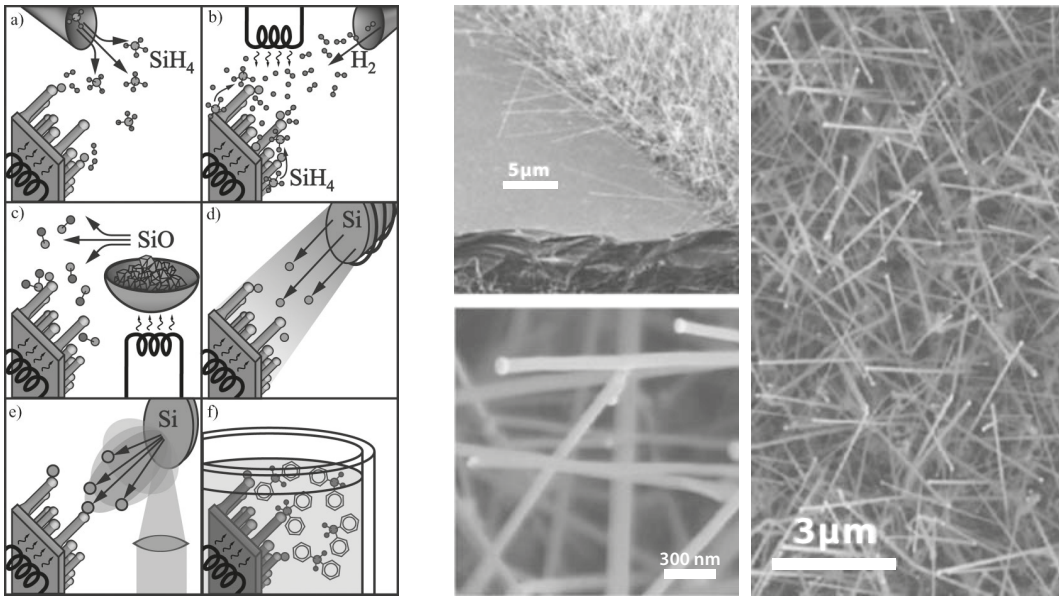

Figure 3.5 – (Left side) Schematics of experimental setups for silicon nanowire growth. a) CVD, b) annealing in reactive atmosphere, c) evaporation of SiO, d) MBE, e) laser ablation, and f) solution-based growth. Image adapted from [76]. (Right side) SEM micrographs of grown nanowires on a substrate. The wires are randomly distributed and oriented, however, smooth sidewalls and large length to width ratios can be attained using bottom-up growth methodologies [82].

be applied to other one-dimensional channel materials such as CNTs [79]. In general, fine control of the final NW/CNT density and position on a final substrate is a strong limiting factor to VLSI integration using these channel materials. Nonetheless, as shown in the device state-of-the-art (Section 2.2), numerous groups have demonstrated very high performance devices using bottom-up NW/CNTs, and larger and larger circuits are being demonstrated using these materials [80, 81].

3.3 The full CP SiNWFET process flow

We describe here the full CP SiNWFET fabrication process flow. We will first describe the main process phases, including some information about the fabrication equipment we employed in our university cleanroom [83] to carry on the process. Figure 3.6 shows an overview of the process, providing conceptual top and cross-section views of the device at various processing steps. Steps are grouped in Phases (1 to 12) for added clarity. Phase numbers correspond between Figure 3.6, the step descriptions (Sections 3.3.2 to 3.3.9) and the detailed runcard (Table 3.3). Due to the repetitive nature of some of the steps (e.g., the PG and CG processing phases), we included more detailed descriptions in the first phases and focused, later on, on the differences between similar process steps.

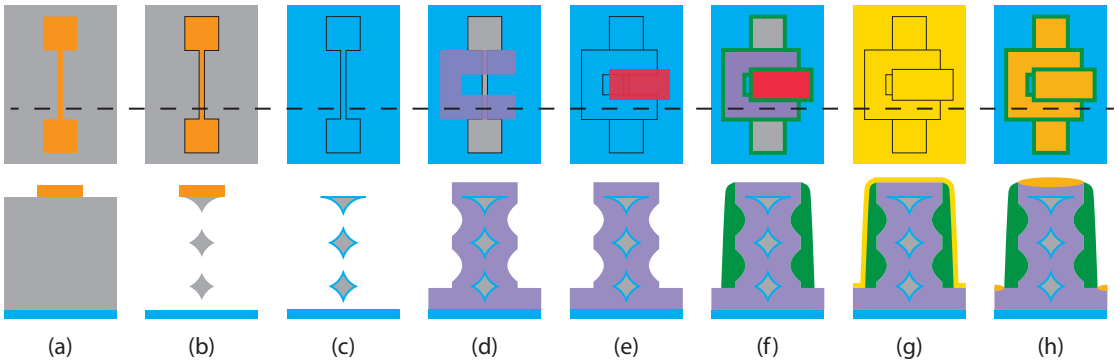

Figure 3.6 – Vertically stacked CP NW process flow conceptual overview. (a-h) Top and cross section views of the main fabrication process steps. (a) The nanowires are patterned by EBL on an SOI substrate with two larger areas at the sides which will form the sustaining pillars (Phase 3); (b) the nanowires are created in a single DRIE (BOSCH) procedure (Phase 4); (c) dry gate oxide is formed by on the nanowires and (d) conformal gate polysilicon is deposited around the nanowires and patterned by EBL (Phases 5–7); (e) a second oxidation and polysilicon deposition is performed. The control gate (red) is patterned by EBL self-aligned to the polarity gate (violet) (Phases 8–10). Finally, (f) low-stress SiN spacers are formed to isolate the structures (Phase 11), (g) nickel is blanket-deposited on all the wafer surface and (h) annealing is performed to produce NiSi S/D and gate contacts, after which excess metallic Ni is removed by wet etching (Phase 12).

3.3.1 Substrate choice for device isolation

Device isolation is a critical feature required for the proper functioning of the fabricated devices. On bulk Si substrates, in the case of nanowire channels supported by small pillars, the parasitic conductive path between the two pillars through the underlying bulk may increase the I_{off} current leakage. Moreover, conductive paths can form on the surface of the underlying bulk Si due to the PG/CG electrodes creating accumulation/inversion layers directly on the bulk surface. These parasitic effects can in practice be eliminated by using a technique employed in state-of-the-art FinFET devices, shown in Figure 3.7(a) [3] and schematically in (b), consisting of filling the gaps between etched fins, or equivalently nanowires, with oxide, and etch down the oxide until the top part of the fins are exposed. Note that, in the case of DSD devices, high channel doping levels require also more complex buried doping layers at the base of the fins to guarantee isolation. In the case of SB devices, low substrate doping limits conductive paths in the bulk between pillars, still simplifying the fabrication process compared to DSD devices.

Nonetheless, in the presented work, due to the added processing complexity required by this method, we opted for the use of SOI substrates. SOI substrates are successfully employed in other industrial FinFET (see Figure 3.7(c)) and FDSOI processes [68] to provide straightforward isolation of the active devices. In our case, despite their higher unit cost compared to plain bulk silicon substrates, SOI substrates allow us to guarantee good I–V device characterization, by forcing all the current injected at the S/D electrodes through the device channel. Nevertheless,

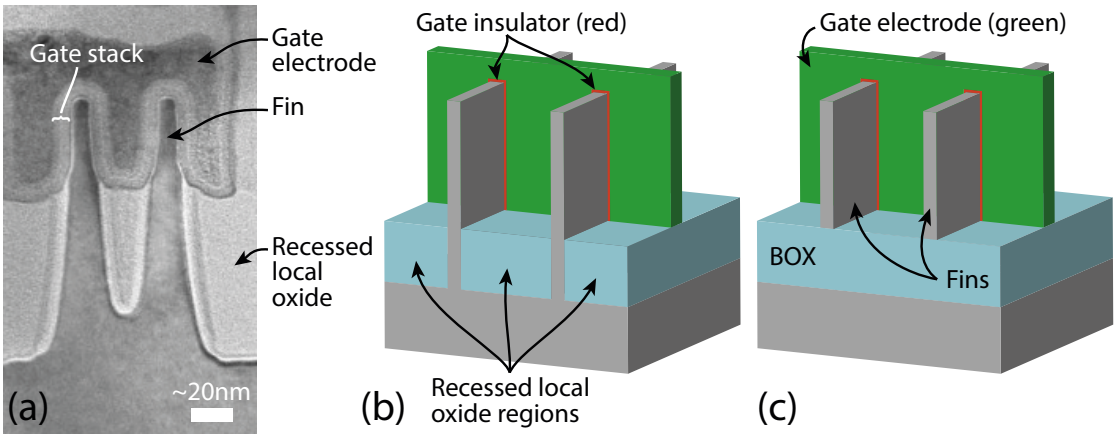

Figure 3.7 – (a) State-of-the-art 14 nm technology node FinFET device cross section from Intel, fabricated on a bulk Si substrate and isolated using recessed local oxide regions that leave only the top, thin fin tip exposed. Image adapted from [3]. (b) Conceptual 3D view of the local recessed oxide isolation on bulk substrates. In this process, after etching the fins, an oxide is deposited on the whole wafer surface and fills the gaps between the fins. Subsequently, CMP is performed to planarize the oxide and blanket oxide etching is performed to etchback the oxide until the fin tips are exposed. (c) The simpler SOI FinFET structures, with BOX isolation. In this case, a single etching of the device layer is sufficient to obtain isolated fins of controlled height.

processing SOIs requires extra care in a number of fabrication steps, mainly due to the presence of the *Buried OXide* (BOX) layer. Specifically the BOX interferes with any process involving charged particles, typically plasma (dry) etching and device imaging through SEM and *Focused Ion Beam* (FIB) analyses. This is due to charging effects, which often reduce or enhance the effect of ions/electrons interacting with the substrate surfaces and structures (see for example Section 3.3.4).

3.3.2 EBL alignment markers definition – Phases 1–2

The proposed process flow exploits multiple subsequent EBL steps to define the various structures composing the device. Same as for optical lithography, alignment patterns are required on the substrate in order to achieve the alignment of the subsequent lithography patterns. Typically, in optical lithography, the alignment markers can be defined at the time of the first mask of the fabrication process. In our case, however, the first actual fabrication step is the nanowire formation, that consists of a shallow (< 500 nm high) silicon etching. Due to the peculiar requirements of our EBL system, a Vistec EBPG5000+ system running at 100 keV [83], markers fabricated with this shallow etch cannot be reliably detected by the system in subsequent patterning steps. Thus, the first phase of the device fabrication process is the definition of alignment patterns on the substrate. Moreover, due to the fine mask-to-mask alignment necessary for the proper implementation of our process (≈ 20 nm), the markers themselves have to be defined by EBL. Specifically, a thick, 550 nm ZEP520 100% photoresist

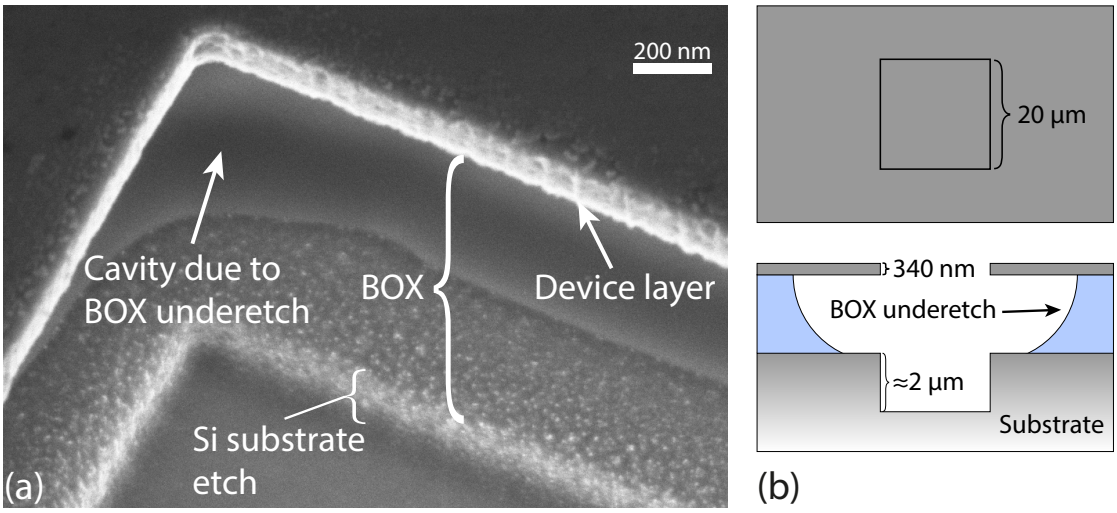

Figure 3.8 – (a) Tilted SEM view (35°tilt) of an etched EBL alignment marker in an SOI substrate, with 2 μm BOX thickness. (b) Conceptual top-view and cross section of the marker after dry etching of the device layer, BHF wet etching of the BOX and further dry etching of the Si substrate.

layer is spin coated at 2000 rpm and exposed with a dose of 220 μC/cm^2.

Subsequently, the markers are created by a deep etching of the substrate. For bulk substrates, this step is straightforward, and consists of a single, $\approx 2.5\,\mu$m deep, anisotropic Si etch (2 min 30 s Si_opto recipe on the CMi Alcatel AMS 200 SE dry etching tool).

In the case of SOI substrates, however, this step is more critical. If only the device layer is etched as marker pattern, the electron beam tool is not able to detect the edges of such shallow (typically, 340 nm) cavity. Moreover, along the fabrication process, the markers are covered with thin films (e.g., the gate polysilicon) multiple times, and their edge positions become less reliable. For these reasons, SOI marker definition includes a first anisotropic etch of the device layer (Si_opto recipe), followed by wet etching in *Buffered HF* (BHF) chemical bath of the BOX and finally a further anisotropic dry etching (using Si_opto) of the Si bulk, down to about 2 μm depth. Figure 3.8(a) shows a tilted SEM view of an etched marker square corner in an SOI substrate and (b) the conceptual top view and cross section of the SOI stack. Wet etching is used to etch through the BOX instead of plasma etching due to the poor selectivity of plasma-based oxide etching to the PR mask, which would result in damaging the PR layer and compromising the deep etching of the substrate below the BOX.

3.3.3 Nanowire mask – Phase 3

Phase 3 is the first actual step required to fabricate the CP *Silicon NanoWire* (SiNW) devices. This phase consists of an EBL step (Phase 3 in Table 3.3) which defines the nanowire thickness and length, as well as the shape of the NW sustaining pillars. In our process, this patterning

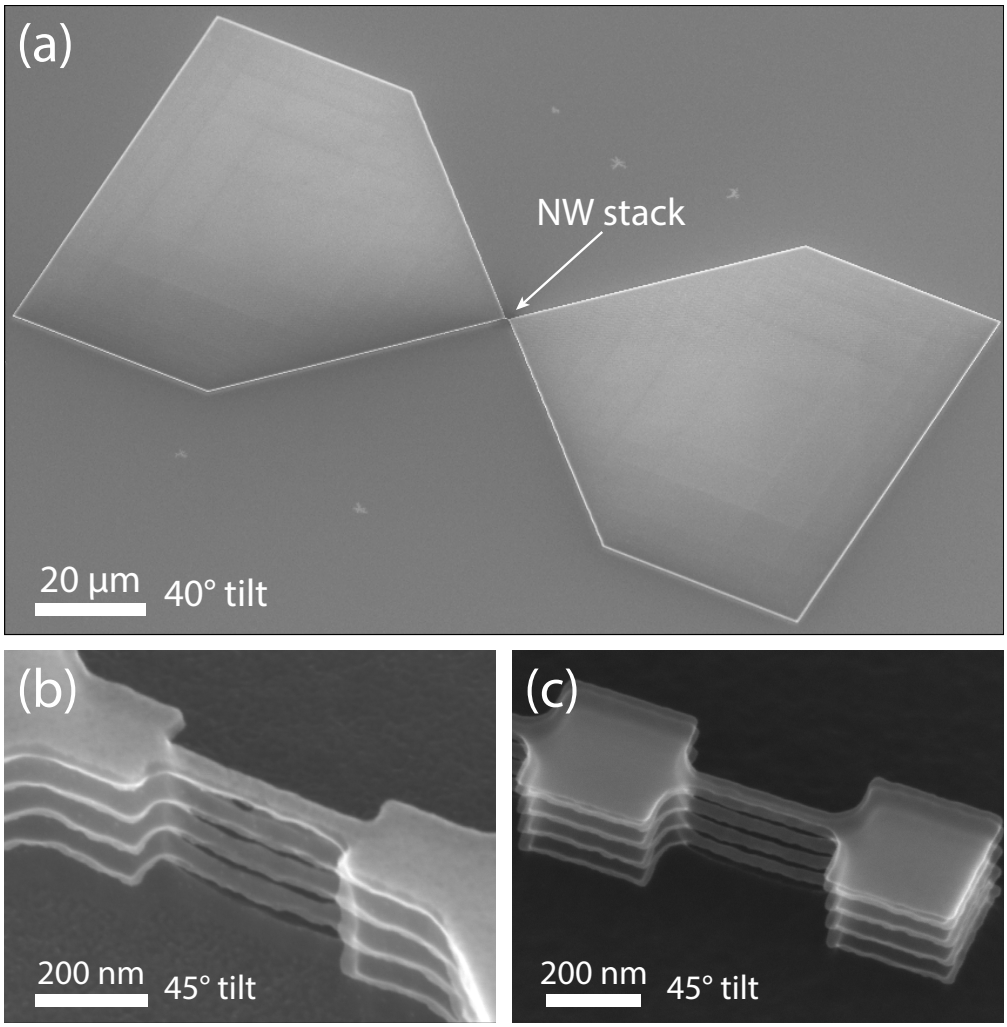

Figure 3.9 – (a) Tilted SEM view of a DRIE-etched nanowire stack with large contact areas for landing probe station needles. (b) Close-up on the device nanowire stack for the large-contact device (50% pattern area fill) and (c) a nanowire stack with small sustaining pillars. In this last case the pattern is much more sparse, and typically lower LER can be obtained in this case.

step has the smallest critical dimension of the three main process layers, i.e., the nanowire pattern width of 40–60 nm. In this mask, we want to etch away most of the wafer surface, maintaining only the nanowires, the sustaining pillars and large contact pads in the case of devices to be characterized with the probe station. For the high resolution and pattern requirements, we chose a negative tone photoresist, namely *Hydrogen SilsesQuioxane* (HSQ) at 2% concentration. This PR has good dry etching selectivity to Si and allows to obtain a thin, ≈ 50 nm layer by spin-coating. Moreover, HSQ allows for a fast exposure (negative tone) and high resolution, which translates into low LER and smoother NW profiles [84].

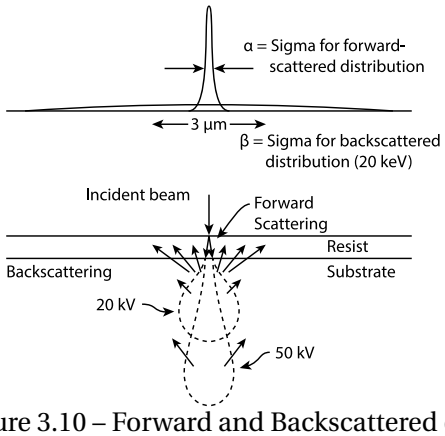

Figure 3.10 – Forward and Backscattered electron influence area for a typical semiconducting substrate coated with a thin PR layer. Image adapted from [85].

Beam energy [keV]	α [μm]	β [μm]	η
5	1.33	[0.18]	[0.74]
10	0.39	[0.60]	[0.74]
20	0.12	2.0	0.74
50	0.024	9.5	0.74
100	0.007	31.2	0.74

Table 3.1 – Electron scattering parameters at increasing beam energies. The values refer to a 0.5 μm thick photoresist film on a bulk silicon substrate. Table adapted from [86].

EBL mask fill-factor and nanowire LER

As introduced in Section 2.4.1, in order to electrically characterize the devices, we employed a setup using a probe station and landing the probes directly on large contacts ($\approx 80 \times 80\,\mu$m) created as extensions of the device electrodes (S/D pillars, PG and CG). These contacts are fabricated close to the device, in order to guarantee low access resistance and reliable contacts to the devices. As shown in Figure 3.9(a), however, these contacts are butterfly-shaped, and fill 50% of the area immediately surrounding the nanowires. Due to electron beam back-scattering in the substrate, these areas provide a background electron exposure of the photoresist where the nanowires are written, ultimately increasing the HSQ nanowire pattern LER and reducing the PR resolution.

Specifically, the normalized exposure dose at a distance r on a photoresist provided by an electron beam incident to the coated substrate can be described by the summation of two Gaussian functions, representing forward and backscattered electron influences [87]:

$$I(r) = \frac{1}{\pi\left(1+\eta\right)}\left[\frac{1}{\alpha^2}e^{-\frac{r^2}{\alpha^2}} + \frac{\eta}{\beta^2}e^{-\frac{r^2}{\beta^2}}\right] \tag{3.1}$$

Note that the dose $I(r)$ is normalized to the clearing dose that would lead to full PR exposure in the middle of a large area. In this equation, α and β parameters represent, respectively, the area of influence of forward scattered electrons (smaller for a more energetic beam) and backscattered electrons (wider for higher energy beams), while η represents the relative influence of backscattered electrons to the main beam intensity. Figure 3.10 shows a conceptual diagram of the forward and backscattered electron influence on a thin photoresist due to the interaction of an incident electron beam of different intensity with a solid substrate. Calculated values for the case of a 0.5 μm PR coating on a bulk Si substrate are presented in Table 3.1. As shown, in our case (100 keV electron beam), a very thin beam can be expected due to very

Gas	Inactive state [sccm]	Active state [sccm]	Priority	Duration [s]
C_4F_8	0	75	1	1.5
SF_6	0	100	2	2.8

(a) Gas flow settings. The total cycle time is 1.5 + 2.8 = 4.3 s.

	Power [W]	Duration [ms]
High	40	10
Low	0	90

(b) Chuck generator pulse settings.

Table 3.2 – DRIE parameters employed for the nanowire etching on bulk and SOI substrates. The parameters are adapted for the Alcatel AMS200 SE dry etcher of EPFL CMi [89]. Note that the parameters refer to a single etching cycle. Multiple cycles are used to fabricate nanowire stacks with a different number of nanowires.

low forward scattering. However, the influence of a beam in an area of the order of 30 μm can be expected in our lithographies, and the $\approx 80 \times 80\,\mu$m pads are well over this size range.

In order to reduce proximity effects, GenISys LayoutBeamer *Proximity Effect Correction* (PEC) software [88] was employed, with parameters $\beta = 30\,\mu$m, $\alpha = 0.005\,\mu$m and η in the range 0.6–1.2. Since the sensitive area in our large pad design is only limited to the device channel, in principle an overall lower exposure dose could be employed to expose the device S/D pads, to limit the effect of background exposure on the nanowire pattern. In this case, however, even if the center areas of the large pads receive the clearing dose, the edges of the pads, including the areas approaching the nanowire sustaining pillars, would be underexposed. PEC on the contrary, consists of fracturing large design areas and varying dynamically the exposure dose, thus minimizing the overall deposited beam energy to write the pad, while preserving sharp pattern edges.

3.3.4 Nanowires DRIE etching – Phase 4

As introduced in Section 3.2.1, after patterning of the HSQ mask for the nanowires, a single etching step comprising a number of DRIE cycles is applied to produce the nanowires. We used the Alcatel AMS 200 SE plasma Si etcher to perform this step, with a 22 s long etching and cycle time of 4.3 s. Figure 3.9 shows DRIE-etched device nanowire stacks (a–b) for the case of large S/D contact pads and (c) in the case of small pillars. In Table 3.2, we summarize the main process parameters defined for the etching.

Figures 3.11(a) and (b) show two SEM/FIB cross sections of the nanowire stacks. In (a), rhombohedral shape wires are shown, surrounded by the 50 nm conformal polysilicon PG gate electrode (see Section 3.3.5). In (b), the nanowire lithography and etching processes were optimized to obtain thinner, more round nanowires. Specifically, lower C_4F_8 gas flow rate will produce more round wires [32], while the nanowire thickness can be tuned by accordingly reducing the original photoresist pattern.

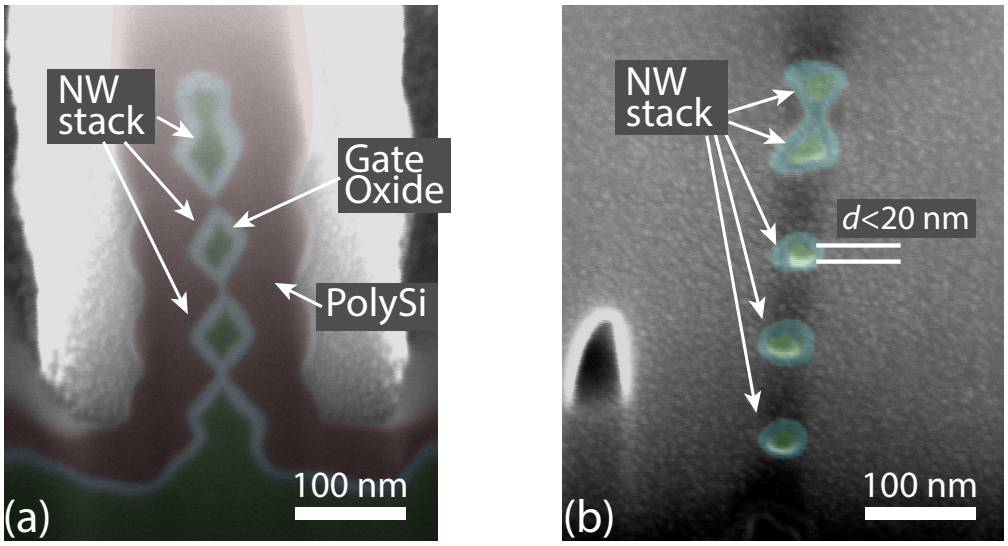

Figure 3.11 – SEM/FIB cross-section views of fabricated nanowire stacks, showing (a) the nanowire stack with 8 nm gate oxide and 50 nm thick conformal polysilicon GAA structure, and (b) an optimized nanowire stack with nanowires of $d < 20$ nm diameter, surrounded by a ≈ 5 nm gate oxide. Image adapted from [64].

Notching effect on SOI

As introduced in Section 3.3.1, due to our measurement requirements, we employed SOI substrates to produce devices to be measured. SOI allow precise definition of the height of the nanowire stack (typically 340 nm in our process), due to the BOX acting as etch stop layer. Nevertheless, as soon as the BOX is exposed to the etching plasma, charging and notching effects can be observed if the etching recipe is too aggressive [90]. Figure 3.12(a) shows damaged structures fabricated on an SOI substrate. Shifted structures can be observed, confirming that the structures are mechanically detached from the BOX surface. Collapsed small pillars are also present on the surface, showing that the etching produced a marked undercut due to notching at the device layer to BOX interface.

3.3.5 Polarity gate stack deposition and lithography – Phases 5–6

The first phase of the PG stack formation consists of creating the gate dielectric and gate electrode. First, the wafer is cleaned from remaining HSQ PR and organic contamination from the DRIE with a 15 s dip in BHF, followed by 5 min in clean hot piranha (H_2O:H_2SO_4:H_2O_2 5:5:1 at 100 °C) and 15 min in standard RCA2 bath (H_2O:HCl:H_2O_2 6:1:1 at 75 °C). Note that RCA1 (H_2O:NH_4OH:H_2O_2 5:1:1) is avoided in this process since it oxidizes too aggressively the silicon surface with risk of damaging the nanowires.

After cleaning, we proceeded with oxidation and polysilicon deposition. In this process, in order to minimize the risk of gate leakage, we opted for a thick ($t_{OX} \approx 8$ nm) gate oxide,

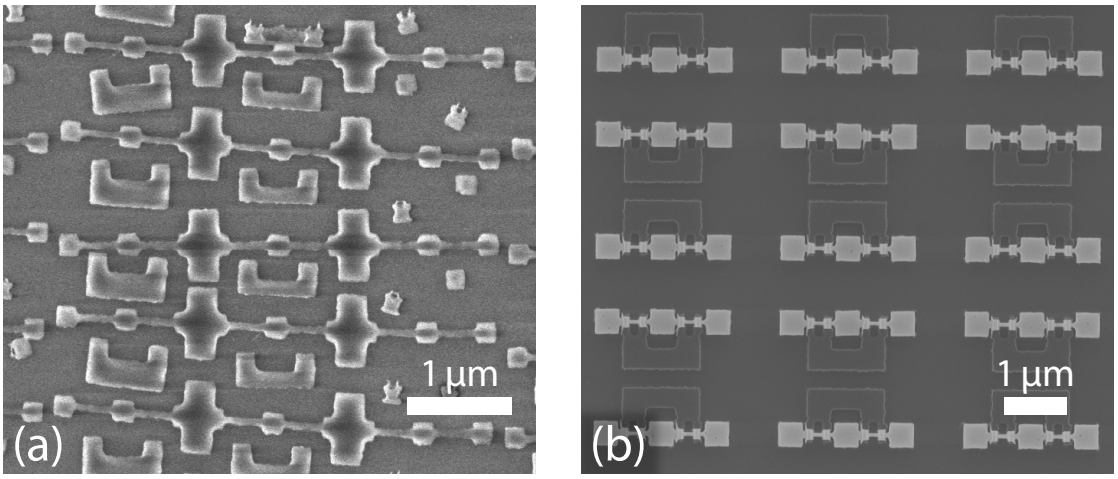

Figure 3.12 – (a) SEM micrograph showing the effect of destructive notching on DRIE-etched structures on an SOI substrate. Due to the charging of the BOX surface, the device layer structures are damaged and detached completely from the BOX. Shifted and collapsed pillars can be observed. (b) Structures etched with a less aggressive DRIE recipe. In this case, no notching and detachment of the structures is observed.

produced using a 60 minutes long bake at 830 °C in O_2 atmosphere. After the gate oxide, a 50 nm polysilicon layer was conformally deposited using *Low Pressure Chemical Vapor Deposition* (LPCVD) (see Figure 3.13(a)). The polysilicon layer thickness was selected in order to maintain a balance between a sufficient layer thickness to allow proper GAA geometry and low enough layer resistivity, while maintaining the PG structure thin enough to be able to properly etch the gate all the way to the BOX (bottom of the nanowire stack). Specifically, a thin, 100 nm gap has to be created in between the two S/D PG sections to allow the fitting of the CG electrode in the subsequent CG stack formation, and 50 nm was found to be a good compromise in terms of aspect ratio compared to the other transistor dimensions.

Perspectives for gate stack optimization

In order to control fabrication complexity and due to equipment limitations, the proposed fabricated devices rely on simple and reliable processing steps for gate stack formation. Nonetheless, many straightforward improvements can be applied to our process, due to its low thermal budget (determined by the nickel silicidation step, at around 450 °C) and top-down fabrication approach, to enable aggressive scaling and optimize device performance. For the sake of completeness, we briefly mention the main technologies used in state-of-the-art devices which could be applied to our process without disrupting its integrity.

- **Self-limiting oxidation:** in our process, nanowire thickness control is mainly delegated to the nanowire mask width and DRIE parameters. In order to obtain reasonable device equivalent channel width and consequently I_{on} performance, we limited our fabrication

to nanowire diameters > 20 nm. The disadvantage of this process choice is the low final NW thickness control, and the resulting roughness of the wires, which can be observed in Figure 3.9. Nevertheless, techniques to further thin the nanowires typically require a first, faster oxidation step, after which the oxide is removed by wet-etching, and a subsequent controlled oxidation to fine-tune the nanowire diameter. This is done by dry oxidation at temperatures below ≈ 900 °C, that are shown to self limit due to the increasing curvature of the nanowire surfaces for decreasing diameters [91]. Using this technique, nanowire diameters below 5 nm can be obtained [92].

- **High-κ dielectric – metal gate:** another established technique, widespread in current industrial processes, is the use of high-κ/metal gate stacks. These technologies allow for strong reductions in EOT, thus further enhancing device performance and enabling aggressive device downscaling. Interestingly, one of the main limitations for obtaining good high-κ dielectrics is high processing temperatures, due to the tendency of some high-performance high-κ materials (e.g., HfO_2) to crystallize when exposed to the high temperatures needed for dopant activation in DSD FET processes. In our process, due to the absence of doping steps, and the relatively low annealing temperatures required for S/D silicidation (≈ 400 °C), high-κ/metal stacks can be in principle applied without interfering with the proposed fabrication steps.

Polarity Gate EBL

Figure 3.13 shows 100% ZEP520 PR patterns covering respectively a couple of devices with small pillars (b) and a device with large contact pads (c). The choice of ZEP520 for this lithography is mainly due to the high topography of the device structures which need to be patterned. Specifically, ≈ 400 nm tall structures have to be covered to guarantee good masking of the areas that have to remain after etching. Low rpm spin coating at 3000 rpm was found to completely cover the structures with good adhesion, producing a PR layer about 500 nm thick. Note that ZEP is a positive PR: therefore, the areas where the polysilicon has to be removed have to be exposed. This requires the exposure mask to be inverted to produce the correct patterns of Figures 3.13(b–c), ultimately requiring long exposure times on the e-beam tool in the case of devices with large contact pads (exposed areas of ≈ $200 \times 200\,\mu m^2$). In this respect, ZEP520 guarantees good etching selectivity and resolution [93] while requiring a relatively low exposure dose (around $220\,\mu C/cm^2$) compared to *Poly(Methyl MethAcrylate)* (PMMA) (requiring about $1000\,\mu C/cm^2$ for the same pattern).

3.3.6 Polarity gate etching – Phase 7

Due to the complex geometry of the proposed device, proper etching of the PG electrode is a critical step to guarantee high performance device functionality while avoiding the risk of damaging the delicate underlying nanowire channels. In particular, the PG electrode has to be cut all the way to the bottom of the SOI device layer, without leaving residual polysilicon

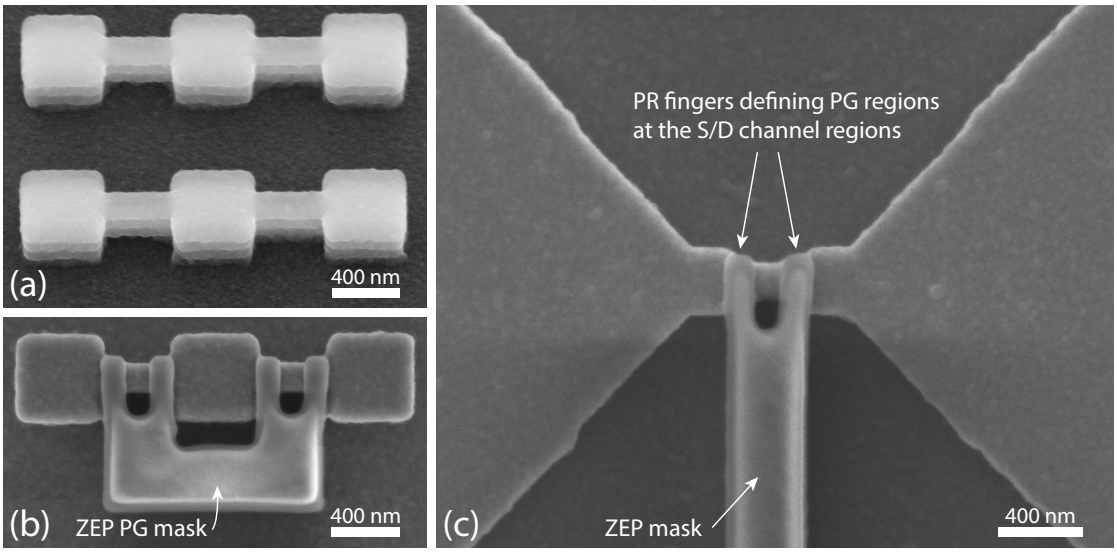

Figure 3.13 – (a) Tilted (40°) SEM view of a nanowire stack after oxidation and deposition of 50 nm conformal LPCVD polysilicon layer (Phase 5). (b) The same nanowire stack tilted at 40°after potoresist coating, e-beam exposure and PR development. (c) The PG mask for the design with large pads. The PG fingers covering the side channel regions are visible, as well as the elongated PG mask leading to the PG large contact pad (not visible in the figure).

areas that could compromise device functionality. Functionality may be disrupted, e.g., in the eventuality that the center region of the channel is covered by a leftover tail of the PG instead of being properly covered by the control gate electrode, thus creating a conductive path regardless of the polarization of the CG. Moreover, compared to the case of a FinFET structure, where the fin sidewalls are less-than-vertical, thus directly accessible vertically via an anisotropic dry etching process, in our case the center region of the nanowires has to be cleared all around the wires, including the small regions *under* the wires.

Figure 3.14(a) shows small-pillar nanowire stacks after etching of the PG electrodes and removal of the leftover PR mask. Clean PG cutting was achieved using a three-step dry etching procedure on the AMS 200 SE Si etcher:

- **3 s SiO2_PR_5:1 –** This step was performed as a break-through step to initiate the etching of the polysilicon layer.
- **26 s DRIE –** This step reproduces exactly the etching parameters used to etch the nanowire stacks in Phase 4 (Table 3.2), with a slightly longer cycle time.
- **4 s Si_ISO_slow –** This step consists of a short isotropic Si etch. The Si_ISO_slow recipe is based on a mostly chemical, pure SF_6 etching, which provides very high selectivity both to PR mask ($> 100:1$) and to SiO_2 ($> 200:1$). Being isotropic and highly selective, we exploit this step to clean the shadowed areas below the nanowires without risking to damage the middle sections which will be covered by the CG electrode.

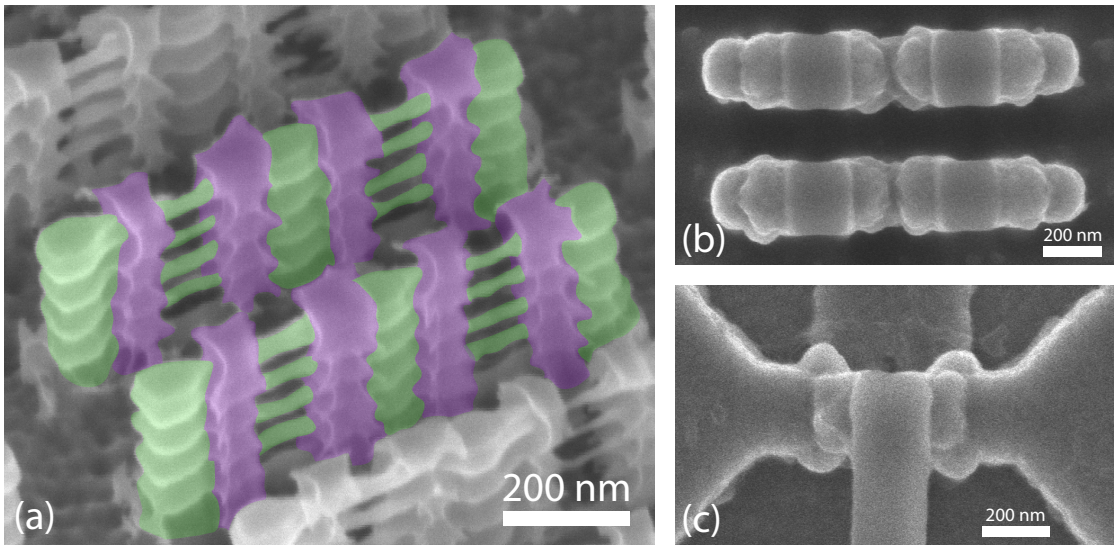

Figure 3.14 – (a) Tilted SEM view with false colors of the nanowire stacks after deposition and etching of the PG structures (Phase 7), showing the PG 100 nm long gate sections (violet) in contact with S/D sustaining pillars (green). Image adapted from [64]. (b) Self-aligned CG ZEP520 PR mask for the small pillar devices: the mask is patterned with an overlap to the underlying PG electrodes. (c) CG mask for the large pillar devices for measurement: in this case the CG structure extends away from the device to form a large contact pad.

3.3.7 Control gate deposition, lithography and etching – Phases 8–10

After fabricating the PG electrodes, Phases 5–7 are repeated using the same recipes in order to produce the CG electrodes. After PG etching, the wafer is cleaned in hot piranha solution, BHF and standard RCA2 bath in order to remove organic and metallic contaminants. Then, a 60 min gate oxidation is performed at 830 °C. This oxidation creates the gate oxide for the center region of the nanowires, and isolates the PG electrode to avoid leakage paths between PG and CG structures. Subsequently, another 50 nm conformal polysilicon deposition is added by LPCVD.

After polysilicon deposition, the CG structures are patterned by EBL using ZEP520, with a 3000 rpm spin coating to guarantee good coverage of the surface topography. Figure 3.14(b) and (c) show respectively CG ZEP520 PR patterns on small and large-contact pad devices after CG polysilicon deposition. Finally, the structures are etched using the same three-step process used for the PG and described in Section 3.3.6.

Self-aligned CG design

As described in Section 2.3.3, our device relies on the electrostatic action imposed by two gate electrodes (PG and CG), ultimately defining three regions of influence over the channel length. Device functionality and reliability is therefore dependent on the good alignment of the two

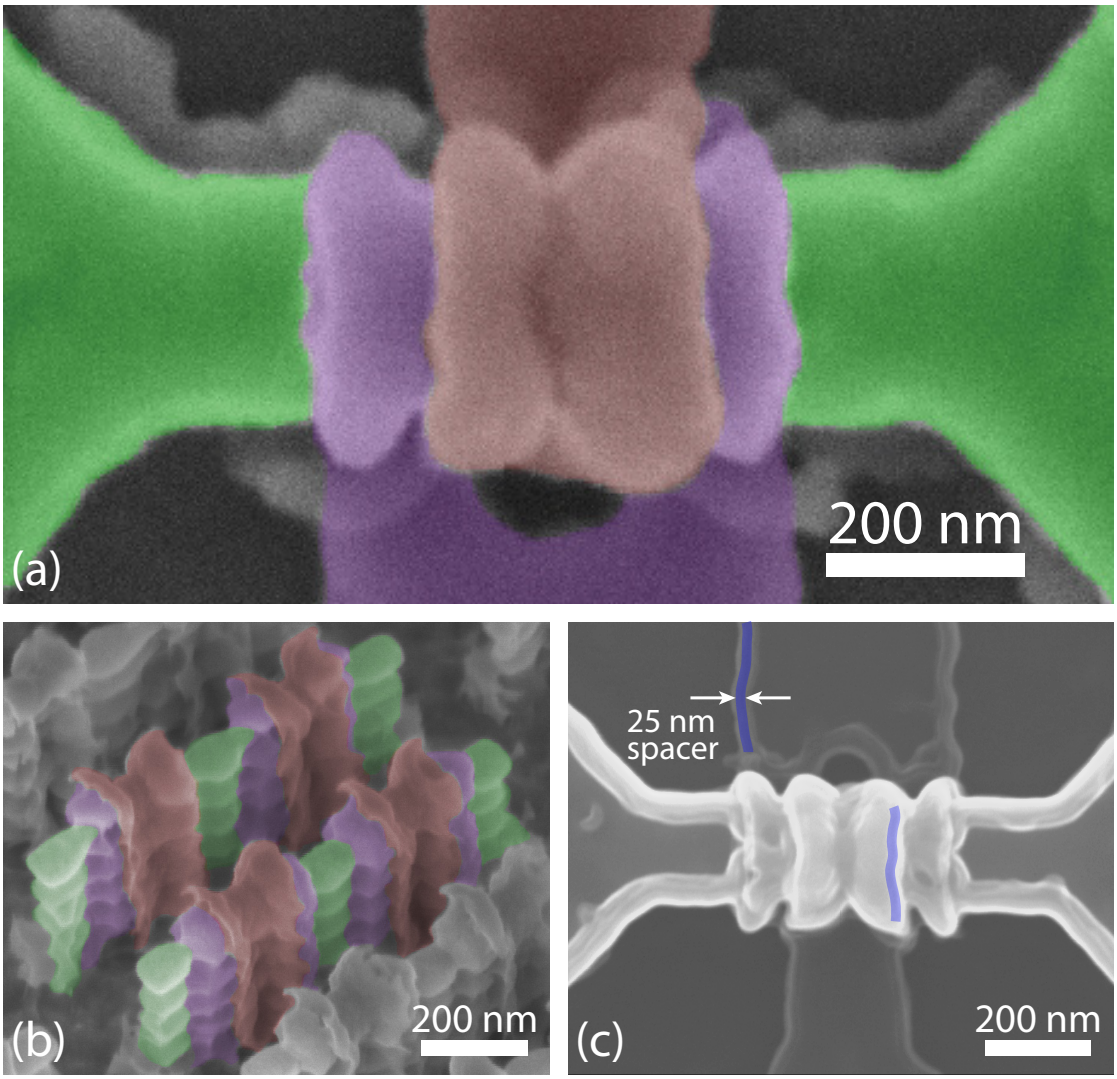

Figure 3.15 – (a) SEM micrograph with false colors of a large-contact pad device with patterned CG and PG electrodes. (b) Tilted SEM view of an array of completed devices. The structures are colored following the convention of Figure 2.1, with green S/D pillars, violet PG and red CG electrodes. (c) A large-contact pad device after definition of the L.S. SiN spacer. The spacer is visible in correspondence of all the vertical step features. In order to facilitate the interpretation of this image, the spacer is highlighted in blue in two regions of the device, one along the PG polysilicon extension (top) and the other between CG and PG electrodes at the top of the nanowire stack (center of the image). The other regions are left without color overlay for improved clarity.

gates. In our process, we opted for a self-aligned masking/etching procedure when adding the CG electrode. This effect is obtained by etching the CG with a small overlap over the PG gate structures. Figure 2.1 conceptually shows this overlap at the interface between PG (violet) and CG (red) electrodes. Figure 3.15(a) and (b) show SEM micrographs of fabricated devices, with respectively large and small contact pads, where the overlap between CG and PG structures

can be observed.

Compared to a process with lithographically defined CG to PG alignment, the self-aligned process has several advantages:

- **Lower constraints at lithography level:** EBL alignment quality strongly depends on alignment markers. As the markers degrade in sharpness due to the subsequent thin film deposition and etching along the process, it becomes more and more difficult to guarantee very precise (< 20 nm) mask alignment for the CG electrode.
- **No ungated nanowire areas:** self-aligned gates rely on the CG gate oxide to determine the thin gap between the areas of influence of the electrodes. Therefore, no ungated nanowire areas are left open to the external atmosphere. This has the advantages of reducing parasitics, such as charge buildup effects and the influence of the environment on the device channel (e.g., incoming light and air humidity). Moreover, in this process, the risk of damaging the nanowires caused by the CG DRIE etching is avoided. Finally, ungated areas increase parasitic resistance of the channel, due to the low doping concentration of the SiNWs.
- **Optimization of device channel length:** lithography defined gate alignment requires the gaps between the two gate electrodes to be large enough to avoid the risk of failure due to mask misalignment. Using a self-aligned process, on the contrary, allows for shorter overall channel lengths, and more compact device structures.

At the same time, one drawback of self-aligned gate electrodes, is the added parasitic capacitance due to the larger surface area where the two electrodes are separated only by the thin gate oxide thickness. This added capacitance has the main effect of increasing delay when the devices are embedded in logic gates. Note that in our process, the separation between PG and CG electrodes along the nanowire channels is determined by the thin gate oxidation. At the same time, by using a controlled self-limiting oxidation of the center region of the nanowires, a different dielectric thickness could be obtained on the wire surface and the PG surface (where the oxidation is not self-limiting), thus allowing a more fine control of the separation between CG and PG electrode regions, including a reduction of the C_{CG-PG} parasitic capacitance. At the same time, minimum mask overlap for the creation of the CG electrode is dictated by the EBL alignment accuracy. In our case, we considered an overlap of around 80 nm, but this figure can be strongly reduced in future processes.

3.3.8 Nitride spacer process – Phase 11

After defining the PG and CG gate electrodes, we defined a silicon nitride spacer in order to prevent short circuit paths between the gate electrodes and between the PG electrode and S/D pillars when performing contact silicidation (see Section 3.3.9). In this step, a 5 nm dry oxide adhesion layer followed by 20 nm *Low Stress* (L.S.) silicon nitride conformal deposition

was performed. Subsequently, a blanket dry etchback step was performed using an SPTS APS dielectric etcher tool. We used the SiO2_PR_1:1 recipe for 7 s which provides smooth etching with good uniformity and similar etching speed for L.S. SiN and SiO_2. Specifically, poor etching selectivity to PR (≈ 1.7 for this recipe) is not critical in this step as the etching has to remove the SiN on all the horizontal surfaces of the wafer.

Figure 3.15 shows a close-up of a device with large contact pads after blanket L.S. SiN spacer etching. Spacer contours are highlighted in blue false coloring along the PG polysilicon contact extension and in correspondence of the step between CG and PG electrodes.

3.3.9 Nickel silicide formation – Phase 12

The last critical step for the completion of the CP SiNWFET fabrication process is the formation of silicided S/D contacts. As described in Section 2.3.1, a mid-gap metal was chosen to produce the S/D regions, to obtain symmetric n and p-type I–V characteristics. To this end, we employed stoichiometric nickel silicide (NiSi) S/D contacts.

In order to fabricate S/D silicided regions, after CG etching and PR removal via oxygen plasma, the exposed Si surfaces are thoroughly cleaned from native oxide in BHF bath for 15 s, and immediately transferred to an Alliance-Concept DP650 sputtering tool. Note that surface cleanness is paramount to the proper reaction of Ni with the underlying Si structures. With this respect, the employed sputtering tool provides the possibility to perform short non-aggressive Ar ion plasma cleaning steps to the substrate to remove any native oxide before the actual metal sputtering without breaking the chamber vacuum. Moreover, to reduce contamination with other metal species, the sputtering target and chamber are primed with a dummy Ni sputtering step, then the substrate is introduced and further cleaned with a 1 min Ar ion plasma etching step prior to Ni deposition. Then, a 25 nm Ni blanket deposition step is performed (see step 12.3 in Table 3.3). Finally, the substrate is processed with a three-step annealing procedure in forming gas (H_2–N_2) atmosphere, with a 25 °C/min ramp-up from room temperature. The temperature is maintained at 200 °C for 20 min, then at 300 °C for 20 min and finally at 400 °C for 20 min. Figure 6.2 shows a plot of the temperature over time in the annealing oven. The 400 °C is the critical step to obtain the stoichiometric Ni_1Si_1 stable phase. In this process, due to the length of the annealing (20 min), the Ni is allowed to fully consume while diffusing in the Si, and the final NiSi layer thickness is determined via the initial metallic Ni layer thickness. For further process control, nonetheless, spike annealing in conjunction with thicker Ni layers can be employed to fine-tune silicidation depth.

3.4 Chapter summary and contributions

In this chapter, we described the full process flow we designed and implemented to fabricate SB CP SiNWFET devices with electrostatic polarity control. We introduced the key technologies required to produce top-down and bottom-up semiconducting nanowires, with a focus on our

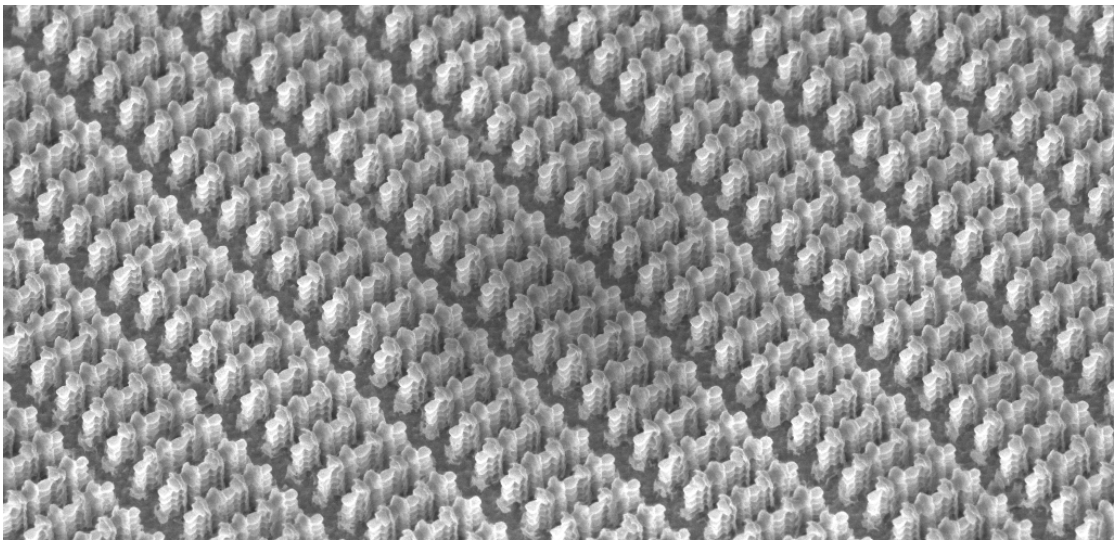

Figure 3.16 – Tilted SEM micrograph of a fabricated dense device array on bulk substrate. The transistors are grouped in four-transistor tiles, with $1.5 \times 0.9\,\mu$m size, for a density of $\approx 3 \times 10^8$ transistors/cm^2.

top-down DRIE-based approach. We described the employed three mask process—based on e-beam lithography—to implement small pillar and large contact pad devices. Specifically the process implements devices with symmetric PG contacts in proximity of S/D electrodes and a self-aligned CG electrode. In general, we can summarize as follows the main requirements we met with this process flow:

- **VLSI compatibility:** the proposed device fabrication relies on a fully top-down, CMOS-compatible process flow, thus allowing straightforward large-scale integration. Figure 3.16 shows fabricated dense device arrays on a bulk substrate, showing $\approx 3 \times 10^8$ transistors/cm^2 using the relaxed device dimensions (roughly compatible with a 90 nm CMOS technology node) used across our process flow.

- **Simple, symmetric device design:** in this fabrication, we chose simple materials (low-doping Si, poly-Si, NiSi, SiN) and non-aggressive processes (e.g., relaxed SiO_2 thicknesses) to fabricate state-of-the-art 3D GAA device structures. Devices fabricated with this process showed excellent performance in electrical measurements (see Chapter 2), while providing ample room for improvement in terms of scaling and material tuning.

- **Low temperature process:** due to the absence of doping implantation/activation steps, the process can be readily adapted to the use of high-κ dielectrics and to 3D monolithic integration technologies.

- **Device isolation:** in this process, we employed SOI substrates to guarantee proper device isolation in the case of large contact pads and produce controlled measurement

results. Nonetheless, since our devices are Schottky barrier-based, bulk isolation techniques based on recessed oxide regions can be applied without substantially modifying the presented process.

Finally, the proposed process demonstrated a sufficient degree of stability to enable the fabrication of four-transistor logic gates that will be presented along with measurements in the next chapter.

Table 3.3 – Process runcard for the fabrication of the DG-SiNWFET devices on an SOI substrate. Typical substrate parameters are: 340 nm-thick boron-doped device layer with ≈ 10 Ω·cm resistivity and 2 μm BOX thickness. *Zn* in the Equipment column refers to the location of the equipment in the CMI cleanroom [83].

Step	Process	Equipment	Recipe
Phase 1	**EBL Mask 1 Lithography – EBL Alignment Markers**		
1.1	Wafer dehydration	Z7/Hot plate	200 °C (180 °C at surface) for 5 min
1.2	ZEP 100% PR spin coating	Z7/ATMsse OPTIspin SB20 manual coater	2000 rpm program (1 min spin time), 600 nm target thickness
1.3	PR pre-bake	Z7/Hot plate	200 °C (180 °C at surface) for 5 min
1.4	e-beam exposure	Z7/Vistec EBPG5000+ EBL tool	Exposure dose: 220 μC/cm^2
1.5	PR development	Z7/Solvent wet bench	n-Amyl Acetate bath for 1 min 45 s
1.6	Substrate rinsing and drying	Z7/Solvent wet bench	9:1 MiBK:IPA bath for 40 s
Phase 2	**Alignment Marker Etching**		
2.1	SOI device layer etching	Z2/AMS200 Si etcher	Si_OPTO for 1 min
2.2	BOX wet etching	Z2/Plade Ox wet bench	Clean BHF bath for 30 min
2.3	Substrate rinsing and drying	Z2/Plade Ox wet bench	FFR + Trickle tank DI water baths, standard recipe
2.4	Bulk etching	Z2/AMS200 Si etcher	Si_OPTO for 1 min
2.5	ZEP removal	Z2/Oxford PRS900	Oxygen plasma, 20 min recipe
Phase 3	**EBL Mask 2 Lithography – Nanowire Pattern Definition**		
3.1	Wafer priming	Z7/Bases wet bench	CD-26 developer bath for 1 min
3.2	Rinsing	Z7/Bases wet bench	Water tank until 15 MΩ/cm resistivity is reached

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Table 3.3 – Table continued from previous page.

Step	Process	Equipment	Recipe
3.3	Wafer dehydration	Z7/Hot plate	200 °C (180 °C at surface) for 5 min
3.4	HSQ 2% PR spin coating	Z7/ATMsse OPTIspin SB20 manual coater	3000 rpm program (1 min spin time), 50 nm target thickness
3.5	E-beam exposure	Z7/Vistec EBPG5000+ EBL tool	Dose: $1500 - 1800\,\mu C/cm^2$. PEC $\eta = 0.6$ for large pads devices, $\eta = 1.2$ for small pillar devices
3.6	PR development	Z7/Bases wet bench	CD-26 developer bath for 2 min
3.7	PR post-bake	Z7/Hot plate	200 °C (180 °C at surface) for 10 min
3.8	PR hardening	Z2/Oxford PRS900	Oxygen plasma 10 min recipe
Phase 4	**Nanowire DRIE Process**		
4.1	SOI layer etching	Z2/AMS200 Si etcher	MM_SOI_ACCU DRIE recipe for 22 s on 340 nm device layer
4.2	HSQ removal	Z2/Plade Ox wet bench	Clean BHF bath for 15 s
4.3	Substrate rinsing and drying	Z2/Plade Ox wet bench	FFR + Trickle tank DI water baths, standard recipe
4.4	Inspection	Z15/SEM Zeiss MERLIN	
Phase 5	**Polarity Gate Electrode Stack Deposition**		
5.1	Organic residues removal	Z2/Piranha wet bench	Piranha clean bath for 5 min
5.2	Rinsing/drying	Z2/Piranha wet bench	Quick dump rinsing + fine rinsing baths, standard recipe
5.3	RCA2 cleaning	Z3/RCA wet bench	RCA2 standard recipe
5.4	Gate oxide	Z3/Dry oxide oven	60 min @ 830 °C
5.5	Polysilicon deposition	Z3/Polysilicon LPCVD	50 nm target thickness

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Table 3.3 – Table continued from previous page.

Step	Process	Equipment	Recipe
Phase 6	**EBL Mask 3 Lithography – Polarity Gate Pattern Definition**		
6.1	Wafer dehydration	Z7/Hot plate	200 °C (180 °C at surface) for 5 min
6.2	ZEP 100% Spin Coating	Z7/ATMsse OPTIspin SB20 manual coater	3000 rpm program (1 min spin time) , 450 nm target thickness
6.3	Post-bake	Z7/Hot plate	200 °C (180 °C at surface) for 5 min
6.4	E-beam exposure	Z7/Vistec EBPG5000+ EBL tool	Dose: $\approx 210\,\mu C/cm^2$. PEC $\eta = 0.6$.
6.5	Development	Z7/Solvent wet bench	n-Amyl Acetate
6.6	Rinsing/drying	Z7/Solvent wet bench	9:1 MiBK:IPA
Phase 7	**Polarity Gate Etching**		
7.1	Polarity Gate etching	Z2/AMS200 Si etcher	SiO2_PR_5:1 for 3 s + MM_SOI_ACCU for 26 s + Si_ISO_slow for 4 s
7.2	Inspection	Z15/SEM Zeiss MERLIN	
7.3	ZEP removal	Z2/Oxford PRS900	Ox plasma 20 min
Phase 8	**Control Gate Electrode Stack Deposition**		
8.1	Organic residues removal	Z2/Piranha wet bench	Piranha clean bath for 5 min
8.2	Rinsing/drying	Z2/Piranha wet bench	Quick dump rinsing + fine rinsing baths, standard recipe
8.3	RCA2 cleaning	Z3/RCA wet bench	RCA2 standard recipe
8.4	Gate oxide	Z3/Dry oxide oven	60 min @ 830 °C
8.5	Polysilicon deposition	Z3/Polysilicon LPCVD	50 nm target thickness
Phase 9	**EBL Mask 4 lithography – Control Gate Pattern Definition**		

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Table 3.3 – Table continued from previous page.

Step	Process	Equipment	Recipe
9.1	Wafer dehydration	Z7/Hot plate	200 °C (180 °C at surface) for 5 min
9.2	ZEP 100% Spin Coating	Z7/ATMsse OPTIspin SB20 manual coater	3000 rpm program (1 min spin time), 450 nm target thickness
9.3	Post-bake	Z7/Hot plate	200 °C (180 °C at surface) for 5 min
9.4	E-beam exposure	Z7/Vistec EBPG5000+ EBL tool	Dose: $\approx 210\,\mu C/cm^2$. PEC $\eta = 0.6$.
9.5	Development	Z7/Solvent wet bench	n-Amyl Acetate
9.6	Rinsing/drying	Z7/Solvent wet bench	9:1 MiBK:IPA
Phase 10	**Control Gate Etching**		
10.1	Control Gate etching	Z2/AMS200 Si etcher	SiO2_PR_5:1 for 3 s + MM_SOI_ACCU for 26 s + Si_ISO_slow for 4 s
10.2	Inspection	Z15/SEM Zeiss MERLIN	
10.3	ZEP removal	Z2/Oxford PRS900	Ox plasma
Phase 11	**Nitride Spacer Definition**		
11.1	Organic residues removal	Z2/Piranha wet bench	Piranha clean bath for 5 min
11.2	Rinsing/drying	Z2/Piranha wet bench	Quick dump rinsing + fine rinsing baths, standard recipe
11.3	RCA2 cleaning	Z3/RCA wet bench	RCA2 standard recipe
11.4	Gate oxide	Z3/Dry oxide oven	standard 5 nm recipe
11.5	Low stress nitride	Z3/Nitride LPCVD	20 nm L.S. SiN recipe
11.6	Spacer etching	Z2/SPTS APS dielectric etcher	SiO2_PR_1:1 for 7 s
11.7	Inspection	Z15/SEM Zeiss MERLIN	

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Table 3.3 – Table continued from previous page.

Step	Process	Equipment	Recipe
Phase 12	**Nickel Silicide Contact Creation**		
12.1	Native oxide removal	Z2/Plade Ox wet bench	Clean BHF for 15 s
12.2	Substrate rinsing and drying	Z2/Plade Ox wet bench	FFR + Trickle tank DI water baths, standard recipe
12.3	Surface plasma cleaning	Z11/DP650 sputtering tool	Standard 1 min RF Ar plasma etching recipe RT_E
12.4	Nickel deposition	Z11/DP650 sputtering tool	25 nm target Ni thickness, recipe RT___Ni_unif for 132 s @ 3.8 Å/s
12.5	Annealing	Z3/Centrotherm furnace	20 min @ 200 °C + 20 min @ 300 °C + 20 min @ 400 °C, 25 °C/min ramp-up
12.6	Piranha excess metallic nickel removal	Z2/Piranha wet bench	2 baths, 5 min per bath
12.7	Rinsing/drying	Z2/Piranha wet bench	Quick dump rinsing + fine rinsing baths, standard recipe

4 Polarity control based logic gates

In this chapter, we present the first demonstration of fabricated, fully-functional, two and four-transistor logic gates exploiting the CP SiNWFET device technology introduced in Chapters 2 and 3. We show measurements for two-transistor logic gates showing functional and cascadable input-output characteristics. We then present measured four-transistor logic gates fabricated as stand-alone circuits with internal connections between the transistor gate electrodes. Finally, we show simulated results to predict performance when considering a low-variability, more mature device structure, and when downscaling dimensions, and to further highlight the differences between the CP-based logic gates with respect to conventional CMOS gates.

In Section 4.1, we introduce the complementary static logic design approach, based on transmission gates, to produce full-swing output, four-transistor XOR logic gates. Section 4.2 presents two relevant works from the literature demonstrating fabricated small logic circuits using NW-based, controlled polarity devices. In Section 4.3, we describe one and two-transistor measured input/output logic gate characteristics, showing for the first time a two-transistor fully functional XOR logic gate. In Section 4.4, we show for the first time fabricated four-transistor logic gates, and show NAND and XOR full-swing output transient characteristics in the same physical circuit. Finally, Section 4.5 presents a number of simulations based on our TCAD device setup, to confirm the measured cell behavior for the two and four-transistor circuits. Section 4.6 concludes the chapter, summarizing the contributions provided by the presented research work.

4.1 Polarity control for logic gate design

In this section, we introduce the complementary static logic gate design approach we implemented to scale up from the single SiNWFET devices to the fabrication and measurement of two and four-transistor logic gates.

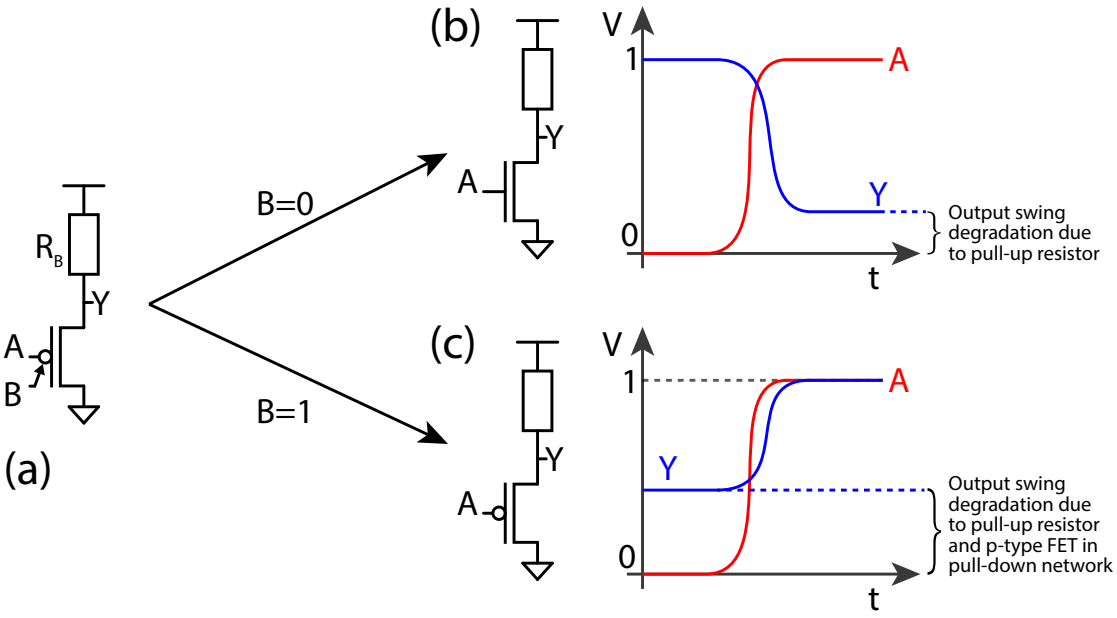


Figure 4.1 – CP FET based pseudo-logic one-transistor gate. When the polarity control gate is driven to logic $'0'$, the transistor becomes n-type and the gate becomes an inverter; if the control gate has value $'1'$, the transistor becomes p-type and the output follows the input value. On the right, qualitative V_{in}–V_{out} characteristics are shown.

4.1.1 One-transistor controlled polarity pseudo-logic gate

Figure 4.1 conceptually illustrates the functioning mechanism of the simplest logic gate which can be built exploiting CP FET devices. Specifically, if we connect a controlled polarity FET to a pull-up resistor as shown in Figure 4.1(a), we obtain a logic gate that can produce either an inverting or non-inverting output, depending on the polarization of the PG electrode of the device. We can then define a convention associating logic values to voltage biases for the logic gate inputs and output. Specifically, we define a low bias voltage for V_{in} or V_{out} (typically, $\leq 0\,V$) as the logic level $'0'$ and a high voltage (typically, V_{dd}) as the logic level $'1'$. Note that, in order to produce cascadable logic gates with this technology, i.e., gates whose inputs can be directly fed by the output of another gate, PG and CG input biases are required to be compatible with V_{dd}, i.e., all voltages have to range between 0 V and V_{dd}. We refer to Section 2.3.1 for a more detailed description of the device level requirements we considered for the fabricated SiNWFETs.

Using the described logic value convention, we can then call the PG and the CG electrode biases, respectively, V_{pg} and V_{cg}, using logic variables (A and B in Figure 4.1). Then, when input B is driven to logic $'0'$, the device in the pull-down network of the logic gate becomes n-type, and a standard pseudo-logic inverter characteristic is obtained (Figure 4.1(b)). On the other hand, when B is controlled to the logic level $'1'$, the device in the pull-down network becomes p-type, and turns on when the input bias for the CG, V_{cg} (represented by logic input A), is low. This induces a buffer behavior, and the output level Y follows the input

value. In other words, if we consider this circuit as a black box, with logic inputs A and B and output Y, we obtain an efficient implementation of an XNOR gate, since $Y =' 1'$ if and only if $(A,B) = ('0','0')$ or $(A,B) = ('1','1')$. As we will see in the next section, this circuit presents strong limitations in output swing and performance. Nonetheless, as shown in Section 4.3, one and two-transistor logic gates allow us to give a first demonstration through measurements the intrinsic functionality embedded in CP devices.

4.1.2 From pseudo-logic to complementary pass-transistor logic gates

As qualitatively shown in Figure 4.1(b–c), the output characteristics of the one-transistor basic gate are strongly degraded both in the inverter and the buffer modes. The first reason for this degradation is the pseudo-logic design: when the pull-down network transistor is in the on state, the supply voltage is ratioed between the transistor resistance and the pull-up network resistance R_B. This limits the minimum output voltage to $V_{DD}R_{on_{n,p}} / \left(R_{on_{n,p}} + R_B\right)$. The natural solution to this problem is the substitution of the pull-up resistor with an active pull-up network, complementary to the pull-down one, similarly to what is done in CMOS logic.

By substituting the pull-up resistor by a network of transistors, we obtain a complementary pass transistor design, shown in Figure 4.2(b). With this configuration, when the CG input B is set to logic level $'0'$, we obtain an inverter with a n-type transistor in the pull-down network and a p-type one in the pull-up network. This inverter provides full swing output and is in all similar to a conventional CMOS inverter. When input B is set to $'1'$, however, the output Y presents a degraded output voltage both for logic value $'1'$ and $'0'$. This is due to the presence of *weak* transistors in the pull-up and pull-down networks.

We define a transistor *weak* using the definition given in [94], i.e., a n(p)-type transistor is weak when it passes, respectively, a logic $'1'$ ($'0'$) across its S/D terminals. In our case, this corresponds to having a n(p)-type transistor operating in the pull-up (pull-down) network of a logic gate. For example, in the simple gate of Figure 4.1, when $B =' 1'$ and $A =' 0'$, the transistor is configured as p-type, and it is in the on state until $V_{GS} = V_A - V_Y < V_{T,p}$. Thus, when $V_A = 0$V, V_Y is limited to a minimum value of $|V_{T,p}|$. In the case of complementary pass transistor logic gates, this limitation appears also for the output high value, which is limited to $V_{T,n}$ when $B =' 1'$, since both transistors are weak.

Transmission Gates

The solution proposed to the problem of weak transistors by M. H. Ben Jamaa *et al.* in [28] is the introduction of *Transmission Gates* (TGs). Figure 4.3 shows a TG and the possible configurations for different values of the CG input B. As we can see, for any configuration one of the transistors is not weak at any time. Thus, by substituting each single CP FET of a logic gate with a TG, full swing outputs can be obtained. Figure 4.2(d) shows the XOR gate which is

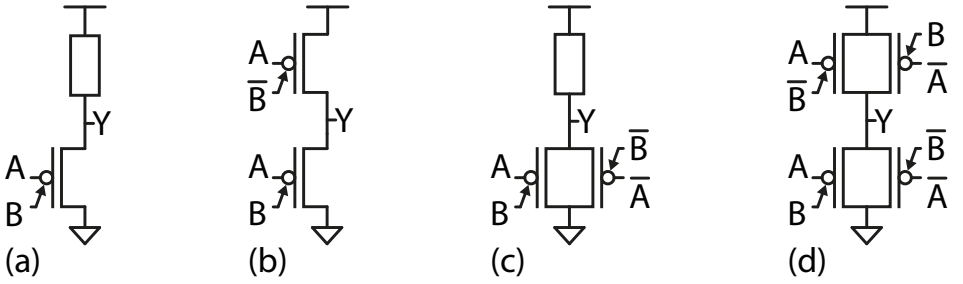


Figure 4.2 – CP FET static logic families; (a) pass transistor pseudo-logic, (b) pass transistor complementary logic, (c) transmission gate pseudo-logic and (d) transmission gate complementary logic.

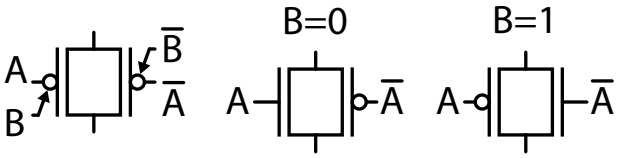


Figure 4.3 – CP based transmission gate structure. At any time, at least one transistor in the structure transfers a strong logic signal, i.e., at any time one transistor is polarized as n-type and the other is polarized as p-type.

obtained from the gate in Figure 4.2(b) by substituting each CP device with a TG.

4.2 State-of-the-art

As described in the introduction of this thesis, in order to go from single device fabrication to circuit-level benchmarking, in this chapter we describe the interaction of a few devices to produce small measured logic gates. Along these lines, we now introduce two relevant works from the literature demonstrating fabricated and measured controlled polarity FET-based logic gates. Note that a number of works exploiting polarity control to produce logic circuits has been described in literature. These works analyze a number of fine and coarse grain logic gates involving either static or dynamic logic approaches (see Section 5.2. Nonetheless, these works rely on cell to circuit level simulations for their analyses. As such, we will introduce these methodologies in Chapter 5, along with our circuit-level benchmarking.

4.2.1 Dopant independent CMOS for reconfigurable logic applications

The first work demonstrating a full inverter characteristic exploiting CP SiNW devices is based on the device described in Section 2.2.3 and was first presented in 2010 by F. Wessely *et al.* [48, 51]. This work exploits the fact that CP devices do not require doping steps along the fabrication process. Using these devices, the authors produce a configurable CMOS-style inverter circuit using two identical CP SiNWFET devices. The devices are configured by PG biasing to behave as p-type ($V_{pg} = -20\,V$) and n-type ($V_{pg} = +20\,V$) respectively in the pull-

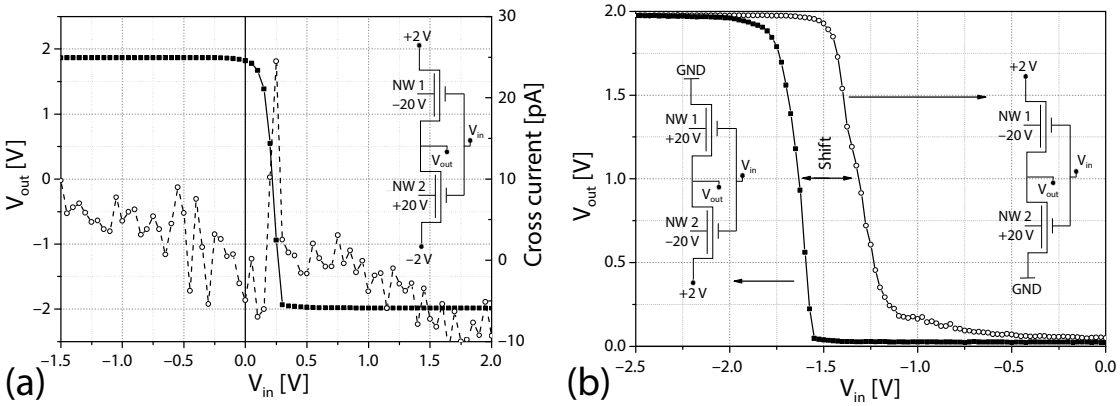


Figure 4.4 – Switching characteristics (solid symbols) of a CMOS inverter circuit fabricated using CMOS NW FETs by applying the appropriate voltages at the back gates (schematic shown as inset). (b) Two traces of the switching characteristics of the voltage selectable CMOS inverter illustrate the versatile programming capability of the NW devices. Filled symbols represent NW FET 1 working as p-fet and NW FET 2 as n-fet. Interchanging back-gate bias and supply voltage polarity, the transistor types are swapped and again a CMOS inverter characteristic (open symbols) is observed. Image adapted from [48].

up and pull-down networks of the logic gate. Figure 4.4(a) presents a measured V_{in}–V_{out} characteristic, for symmetric V_{dd} and V_{ss} of ±2V, showing a typical inverter switching behavior, with the output inverting the input logic value. Further, in Figure 4.4(b), characteristics are shown for $V_{\text{ss}} = GND$ and $V_{\text{dd}} = +2\,\text{V}$, before and after swapping V_{ss} and V_{dd} values, as well as the two PG biases. The superposed characteristics for the two cases show that the devices can both work as n or p-type devices. However, negative V_{in} voltages are required to obtain proper inverter operation when setting a supply voltage $V_{\text{dd}} - V_{\text{ss}} = 2\,\text{V}$.

Note that, as described in Section 2.3.1 and resumed in Table 2.2, this circuit suffers from the asymmetric front and bottom gate electrode geometries. Specifically, although the PG (front gate) is fabricated as an Ω structure, thus providing strong electrostatic coupling to the NW channel, the PG (bottom gate) is separated from the device by a thick back gate oxide (See Figure 2.6). As in our work we aim at designing cascadable logic gates using CP devices, the PG and CG bias voltage ranges have to be as symmetric as possible, and compatible with V_{dd}. Therefore, the asymmetric polarity and control gate structures shown in this device are non-ideal, as shown by the very strong positive and negative voltages (±20V) required to correctly polarized the devices.

4.2.2 Single NW configurable logic gates

The second work combining more than one transistor to produce measured logic gate characteristics was presented by A. Heinzig *et al.* [47] in 2013. The shown logic gates exploit the device structure introduced in Section 2.2.4, comprising a bottom-up fabricated nanowire with two independent gate electrodes acting on the channel source and drain SBs. In this

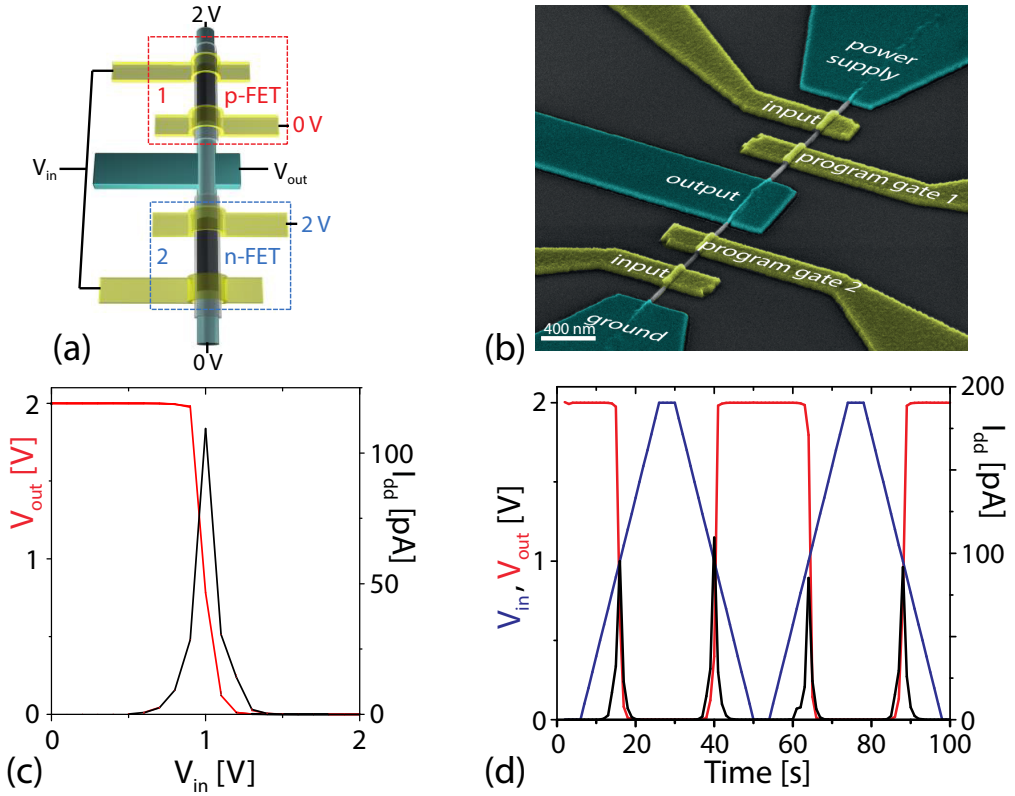


Figure 4.5 – Reconfigurable inverter circuit on a single wire, separated to create two transistors as described in [47]. (a) Conceptual configuration setup for the shown measured characteristics. (b) SEM tilted view with false colors highlighting S/D contacts and Ω gate electrodes for the fabricated two-transistor circuit. (c) Configured inverter transfer characteristic showing switching at $V_{dd}/2$ with steep switching slope and full swing output voltage range. Significant current only flows during switching demonstrating the complementary function. (d) Time domain measured sweeps, showing correct inverter operation. Image adapted from [47].

work, the two gate regions act on each SB independently, allowing the reconfiguration of transistors to operate either as n or p-type. Specifically, full-swing output configurable inverters are demonstrated by employing two transistors with the same exact physical structure built on a shared long SiNW. This reconfigurability enables the construction of CMOS-style complementary logic gates using a single physical transistor structure, thus not requiring chemical doping or doping wells to fabricate complex circuits.

Figure 4.5(a) shows the conceptual structure of such inverter [47], where the devices are configured as a p-fet in the pull-up and n-fet in the pull-down gate networks. Fabricated devices with highlighted S/D regions and gate structures are shown in Figure 4.5(b). In Figure 4.5(c) and (d), measured output characteristics show correct switching operation and very good symmetry in rising and falling V_{out} edges when operating at all positive voltages (i.e., in the range 0 V to $V_{dd} = 2$ V), thanks to the highly symmetric I–V characteristics of the single devices. Nonetheless, due to the fact that the PG electrodes act only on one side of the

channel, these transistors have to be pre-configured to behave as n or p-type before the logic gate is operated, i.e., the transistors cannot change polarity at runtime without modifying their physical routing connections. As a consequence, a circuit as the one shown in Figure 4.5(a) cannot be employed to produce a functional XOR logic gate. In order to create logic gates where some of the PG electrodes can be fed directly by a logic state variable, on the contrary, we need transistors that have an intrinsic structural symmetry with respect to S/D electrodes. As we will show in the following, this effect can be achieved by using a three gate region structure, where the PG electrode acts on both the S and D side SBs.

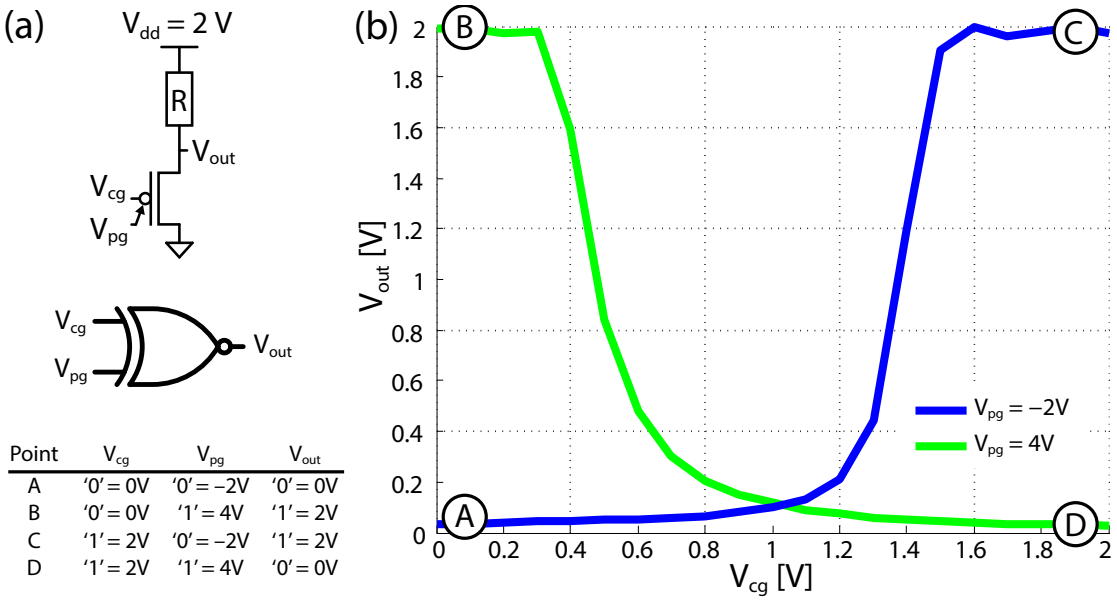
4.3 CP SiNWFET one and two-transistor circuit measurements

In this section, we describe the measurement results obtained by the combination of multiple fabricated CP SiNWFETs to produce small logic gates comprising up to two devices. For the first time, we demonstrate measured two-transistor fully functional complementary XOR logic gates. Specifically, we will first consider an extracted characteristic using a single FET device to demonstrate the XOR functionality produced exploiting the PG bias (V_{pg}) as a logic state variable. Furthermore, we will introduce the two-transistor logic gates built with a complementary structure, including a configurable inverter and the two-transistor cascadable XOR gate.

4.3.1 Single CP SiNWFET embedded as a pseudo-logic XOR gate

According to the circuit design methodology presented in Section 4.1.1, the most basic logic gate which can be demonstrated using our fabricated CP SiNWFET devices is a one-transistor pseudo-logic gate. Figure 4.6 shows the extracted characteristic produced by using a measured single device characteristic, and evaluating the V_{out} value considering a pull-up resistor with $R = 100\,\mathrm{M\Omega}$. Specifically, Figure 4.6(b) shows output characteristics in the case in which the pull-down FET is polarized as n-type (inverter, green curve) or p-type (buffer or non-inverting mode, blue curve). Note that, due to the pseudo-logic gate configuration, the output characteristics cannot reach 0 V, since when the pull-down FET is on, current will flow also through the pull-up resistor (see Section 4.1.1).

To summarize the possible input/output configurations, the table at the bottom of Figure 4.6(a) shows high and low input voltage configurations as applied to the two gate electrodes (V_{pg} and V_{cg}), respectively representing logic values $'1'$ and $'0'$. As previously described, output values show that the output is at high voltage (logic $'1'$) if and only if the two inputs have opposite logic values ($'1'/'0'$ or $'0'/'1'$), thus effectively implementing an XOR logic operator.



Point	V_{cg}	V_{pg}	V_{out}
A	'0' = 0V	'0' = −2V	'0' = 0V
B	'0' = 0V	'1' = 4V	'1' = 2V
C	'1' = 2V	'0' = −2V	'1' = 2V
D	'1' = 2V	'1' = 4V	'0' = 0V

Figure 4.6 – Pseudo-logic XOR characteristic obtained using a single CP SiNWFETs. (a) Circuit schematic for the pseudo-logic gate, logic symbol and truth table for the circuit input-output configurations considering logic values '0' and '1' and their equivalent bias voltages for V_{pg}, V_{cg} and V_{out}. The device in the pull-down network is polarized by means of the PG. (b) Extracted characteristics from a single measured device calculated using a pull-up resistor with $R = 100\,M\Omega$. In the case of the n-type polarization, the characteristic of a pseudo-logic inverter is obtained (green). In the p-type case, a buffer is obtained (blue). As shown in the inset truth table, overall an XOR function can be implemented with a single transistor. Image adapted from [64].

4.3.2 Two-transistor configurable inverter

The next step in the construction of a functional and efficient logic gate consists of substituting the pull-up resistor with a second CP device. Thanks to the configurable nature of the CP devices, and as described in detail in Chapter 2, no chemical doping profiles or doping wells are required to produce n and p-type devices. Therefore, two devices with the same physical structure can be connected and configured to produce any CMOS-like logic gate. In this first example, therefore, we measured a circuit comprising two devices polarized respectively as p (n)-type in the pull-up (pull-down) networks of the logic gate. Note that this circuit was measured connecting two independent devices by landing 8 separate probes on our probe station setup, and creating the connections with appropriate cabling.

Figure 4.7(a) shows the implemented circuit, along with the utilized PG bias voltages, respectively for the transistor in the pull-up ($V_{pg,PU}$) and pull-down ($V_{pg,PD}$) networks, used to polarize the devices. A $V_{dd} = 1\,V$ is used in this circuit, that presents correct 0 V to 1 V full swing output, with the output transition well centered around $V_{cg} = V_{dd}/2 = 0.5\,V$. A slightly negative PG bias voltage $V_{pg} = -0.5\,V$ was chosen to polarize the pull-up transistor to p-type. This value results from a trade-off between using a strongly negative voltage (for better polar-

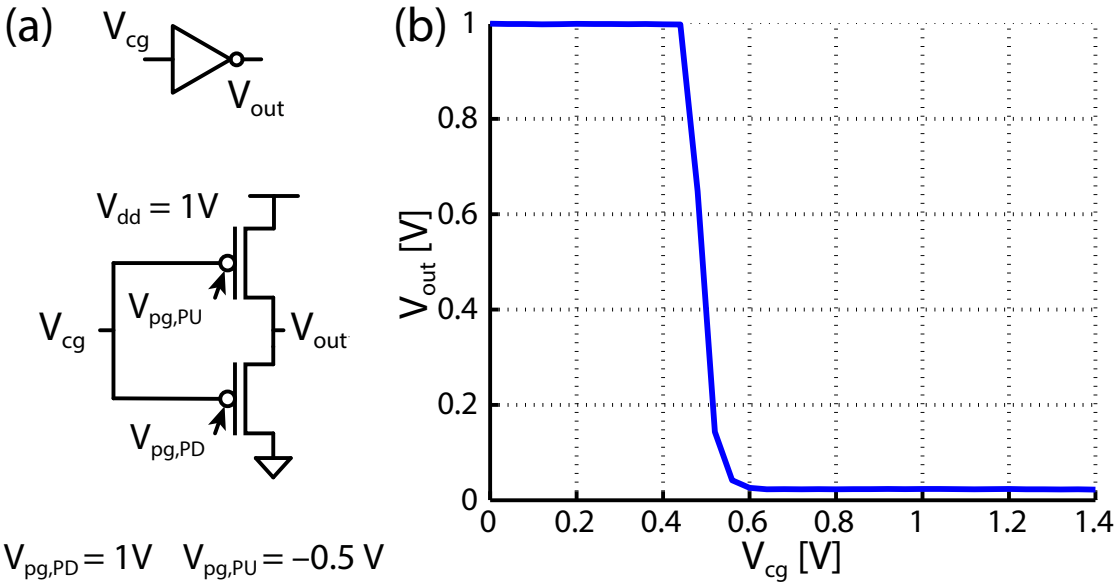


Figure 4.7 – Measured inverter characteristic (b) obtained by connecting two transistors as in the logic gate circuit (a) The polarity gates are biased so as to obtain a CMOS-like inverter, with a p-type transistor in the pull-up network and a n-type transistor in the pull-down network. Image adapted from [64].

ization) and a voltage closer to 0 V, showing that the device is functioning almost in the correct range for multi-level logic circuit compatibility. Note that this value is required to balance the performance of our proof of concept devices. $V_{pg} = 0$ V can be reached with more optimized transistors, as shown in Section 4.5.1.

4.3.3 Two-transistor XOR operation

Instead of using the PG bias as a pre-set configuration signal, the PG input can be utilized as a second logic variable. In this case, the transistor polarity would be dynamically-defined by a logic signal during the circuit operation. As described in Section 4.1.1, such logic gate could act as an inverter or buffer depending on the PG input.

Note that, as previously mentioned, in order to enable multi-level static logic synthesis with this technology, PG and CG input biases are required to be compatible with V_{dd}, i.e., all voltages have to range between 0 V and V_{dd}. Figure 4.8 shows the first demonstration of a measured complementary XOR logic gate exhibiting this feature. In this case, the output characteristic of the buffer branch is degraded, in that full-swing output is not reached, and the switching region is not as steep as for the inverter characteristic of Figure 4.7. However, this effect is due to the presence of the weakly polarized n-type FET in the pull-up network and the p-type FET in the pull-down network. Note that, as shown by the ad-hoc gate simulation described further in this section, this limitation is due to the logic gate circuit topology, and not to an intrinsic device limitation.

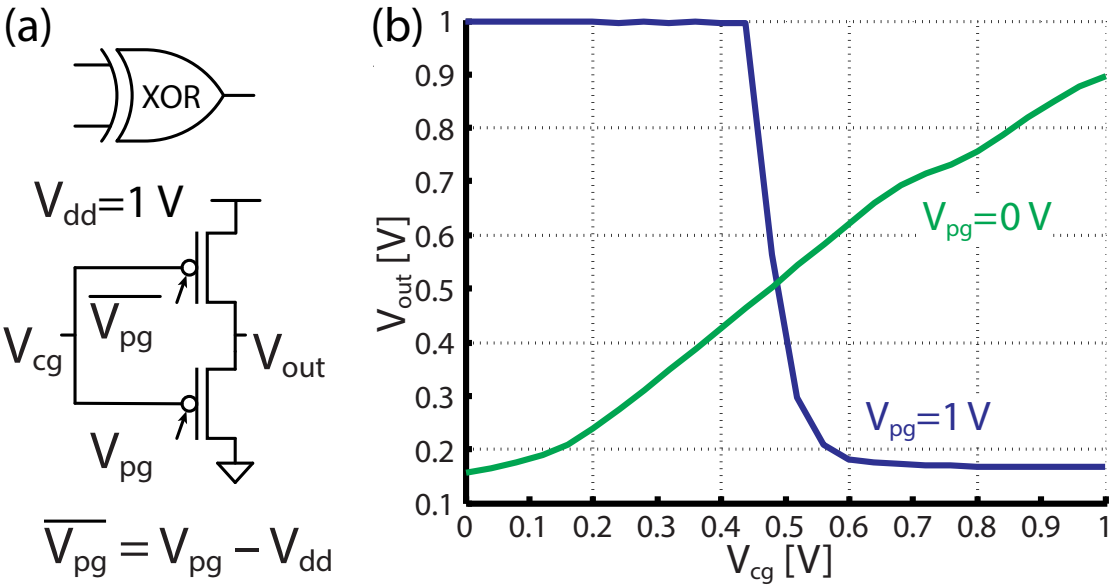


Figure 4.8 – Output characteristic of a two-transistor complementary XOR logic gate. Similar to a two-transistor non-inverting gate, the buffer characteristic is degraded due to the presence of weakly polarized n-type FET in the pull-up network and p-type FET in the pull-down network. Note, however, that control and polarity gate input voltages are compatible with V_{dd} (range from 0 V to 1 V), making this gate fully functional for implementing multi-level static logic. Image adapted from [64].

Finally, in this measurement, the inverter characteristic does not fully reach the correct low output voltage of 0 V. This is due to the pull-up transistor not switching off completely. Nonetheless, control and polarity gate input voltages both range from 0 V to V_{dd} = 1 V, making this gate fully functional for implementing multi-level static logic. As described in Section 4.1.2, the degraded output characteristic of the measurement of Figure 4.8 can be restored by simply using pairs of transistors with opposite polarities, as shown in Figure 4.2(d).

Two-transistor XOR simulation

In order to further elucidate the buffer output degradation, in Figure 4.9, we show a simulated characteristic for the same circuit of Figure 4.8. In this case, we used the optimized device model described in Section 2.5 using a mixed-mode TCAD simulation setup. As expected, this simulation shows no output degradation for the inverter configuration and demonstrates that the output signal degradation for the buffer configuration of the circuit (see Figure 4.8) is indeed due to early switching off of the transistors in the pull-up and pull-down networks and not to degraded device level characteristics.

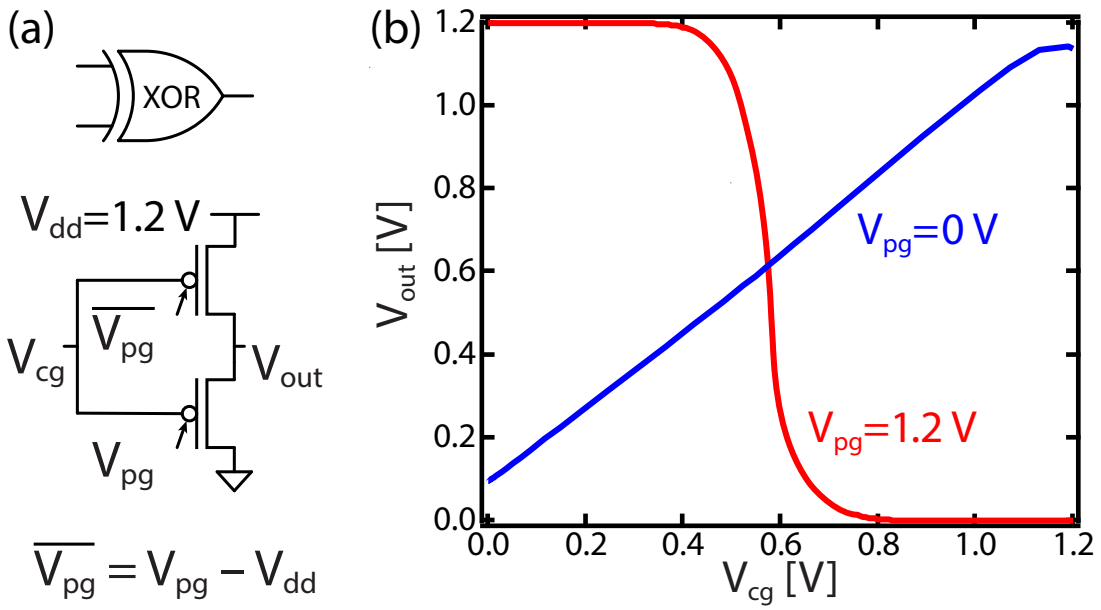


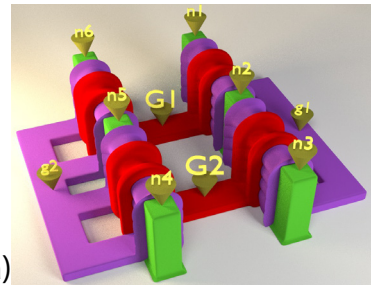
Figure 4.9 – TCAD simulation of the two-transistor XOR gate built with optimized devices corresponding to the measurement in Figure 4.8. Image adapted from [64].

4.4 The fabricated four-transistor logic gates

In order to fulfill the output integrity requirements conceptually described in Section 4.1, i.e., to obtain full swing output characteristics, we stepped up our fabrication process flow by designing monolithic four-transistor logic gates, i.e., circuits where the four transistors are pre-connected by fabrication. Specifically, the transistors are connected by sharing a drain pillar, and by connecting PG and CG electrodes in a parallel/series configuration shown conceptually in Figure 4.10(a). The shown connectivity, as described in the following, allows efficient reconfiguration of the logic gate to implement either a unate two-input (e.g., NAND) or binate function (e.g.,) In particular, thanks to dynamic polarity control, the fabricated single physical circuit with fixed polysilicon lines, consisting of 4 identical transistors, can be configured to implement various logic functions including NAND, XOR, NOR and minority gate (a Full Adder requiring only 8 transistors) [95] by only changing its back-end metal connections. Note that, as previously described, the fabricated devices do not require the use of doping wells, thus reducing constraints at layout design level.

The circuit connectivity to obtain NAND and XOR configurations is shown in detail in Figure 4.10(b). Finally, Figure 4.10(c) shows the used measurement setup, created using a Karl Süss PM8 probe station. The shown SEM micrograph of a circuit is false colored using the same color convention used throughout this document (see Figure 2.1), highlighting red control gates (CG1 and CG2), which are shared between parallel devices, and violet polarity gates (PG1 and PG2), shared between transistor series. In this measurement setup, the Agilent B1500A parameter analyzer was employed to provide static polarization signals to the transistors, and to evaluate the output signal of the logic gates. Positive and negated input signals were

(a)



(b)

PAD	NAND	XOR
PG1	Gnd	¬B
PG2	Vdd	B
CG1	A	¬A
CG2	B	A
S1	Out	Gnd
S2	Out	Vdd
S3	Gnd	Vdd
S4	Out	Gnd
D1	Vdd	Out
D2	---	Out

(c)

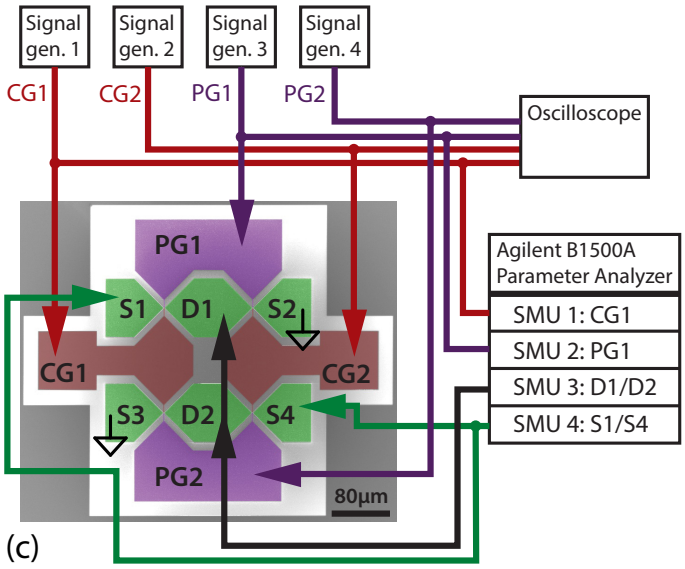


Figure 4.10 – (a) Conceptual model of an unconfigured four-transistor CP FET based circuit. (b) Configuration connectivity table to obtain NAND and XOR logic functions from the unconfigured cell of (a). (c) SEM micrograph overlay of the 10-probe measurement setup. Same as for the single transistor case, measured four-transistor gates are designed including $\approx 80 \times 80 \mu$m pads for probe landing. The false colors follow the convention of Figure 2.1. Image adapted from [66].

provided using four arbitrary waveform generators. Finally, an oscilloscope was employed to produce time domain plots of the logic gate operation.

The time domain measurement of the output response of the tile in the NAND configuration (circuit in Figure 4.11(a) and (b)) for all A and B input combinations is shown in Figure 4.11. The output is at logic $'1'$ (1 V) only when A and B are both at logic $'0'$. This result demonstrates a correct NAND logic behavior. Similarly, Figures 4.12(a) and (b) show the conceptual configuration of the same physical tile to produce an XOR logic function. In this case, the output is shown to be at logic level $'1'$ (0.8 V) only when the inputs signals are different ($A ='0'$, $B ='1'$ or $A ='1'$, $B ='0'$), justifying a correct XOR behavior. For both configurations, the output response shows full swing output voltage levels from logic state $'0'$ (0 V) to $'1'$ (1 V for NAND and 0.8 V for XOR). A batch of more than 20 different four-transistor tiles was characterized, all correctly calculating the output function. Note that, in order to obtain fully cascadable logic gates, only positive voltages would be required as inputs of the CG and PG electrodes. As previously considered in Chapter 2, this would require tuning of process parameters to obtain the desired CG and PG thresholds. Nonetheless, neither exotic materials nor advanced techniques such as strain technology were employed in the presented fabrication process flow. Moreover, these improvements are indeed applicable to the analyzed structures, giving a range of opportunities for device tuning, as shown for example in [47].

Further, note that the CP device geometry imposes a difference in input/output capacitances

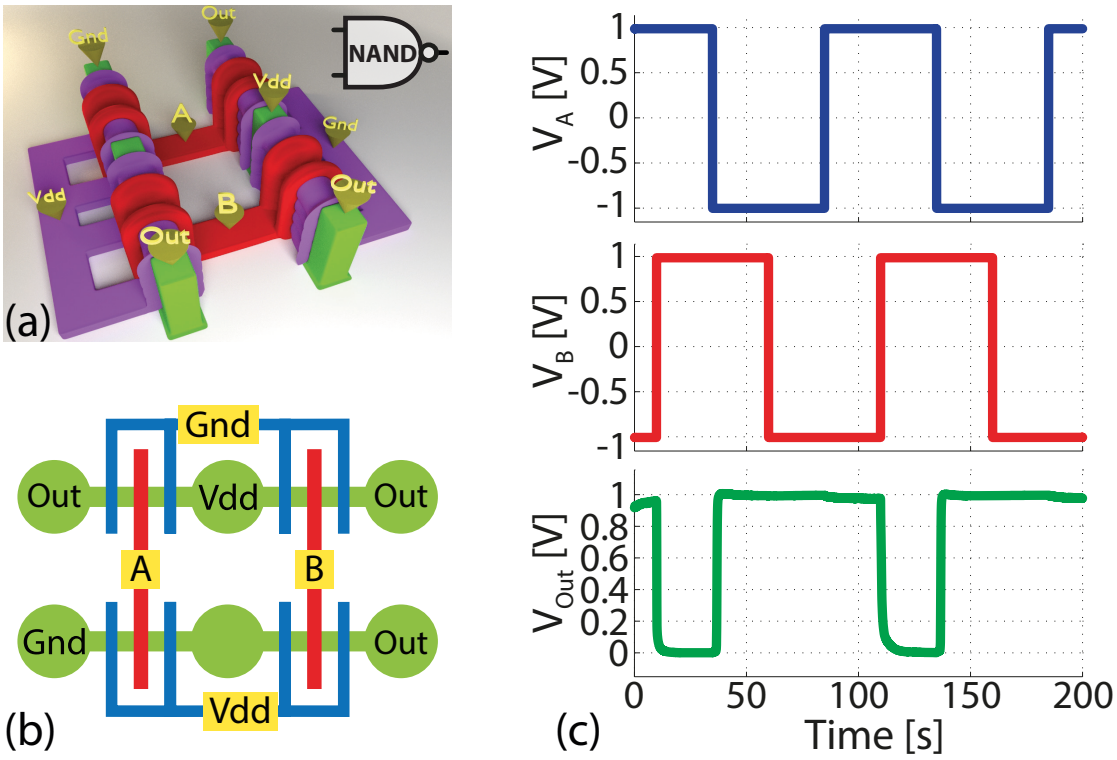


Figure 4.11 – Four-transistor NAND circuit measurement. (a) Conceptual view of the four-transistor tile configured for NAND operation. (b) Conceptual schematic structure of the circuits, with the utilized connectivity. (c) Time domain measurement results for the NAND configuration. Image adapted from [66].

for PG and CG structures, with the PG being more capacitive as it covers a longer channel length. As shown in Section 4.5.1, this translates into two different intrinsic delays for a transistor. The PG capacitance becomes relevant only when the PG is fed by a logic input and not pre-set to a fixed bias voltage, i.e., in the case of binate (e.g., XOR) functions. However, since an XOR/XNOR function is symmetric to its inputs, this effect can be minimized by feeding all PGs by signals on non-critical delay paths and with the lowest switching activity of the two. Moreover, in our implementation, contrarily to standard CMOS, no transistor series are found in the pull-up and pull-down networks of XOR logic gates. Thus, all transistors can be sized to the minimum technology size, directly leading to an overall reduction in transistor sizing and gate capacitance compared to standard CMOS.

4.5 Performance investigation through simulations

In this section, we complement our measurement results with some gate-level simulations we performed to better evaluate logic gate properties and make some performance predictions for large scale circuit applications of the presented devices.

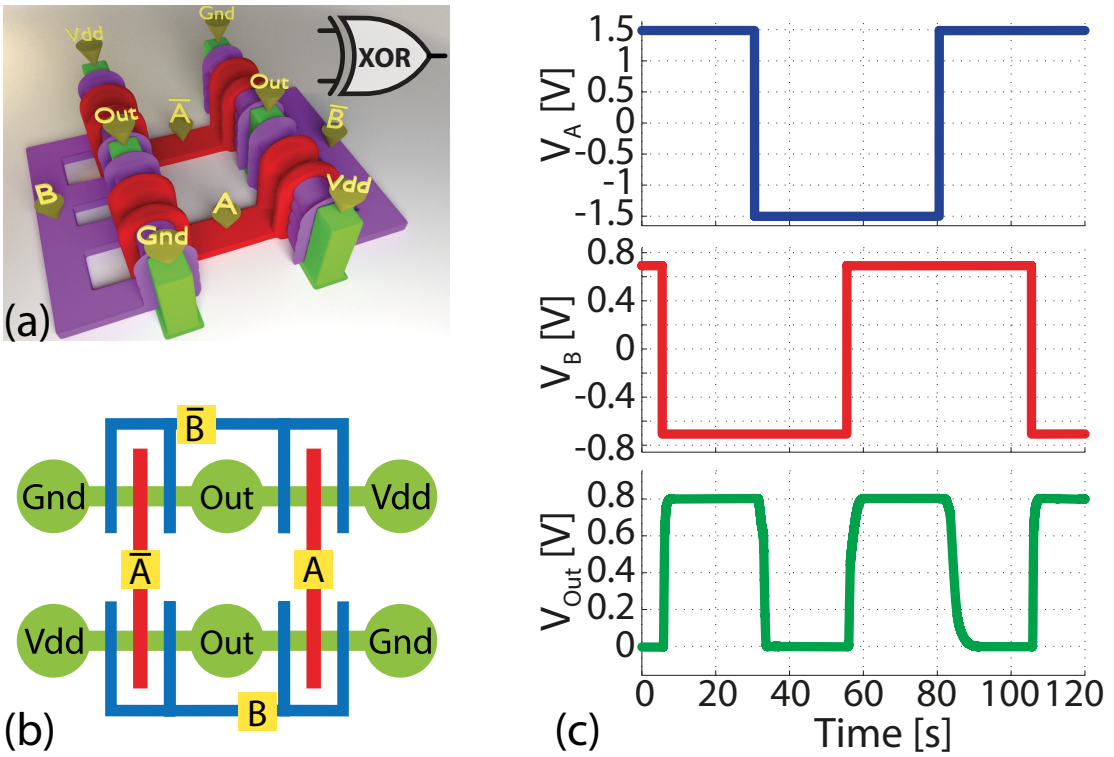


Figure 4.12 – Four-transistor XOR circuit measurement. (a) Conceptual view of the four-transistor tile configured for NAND operation. (b) Conceptual schematic structure of the circuits, with the utilized connectivity. (c) Time domain measurement results for the XOR configuration. Image adapted from [66].

4.5.1 Four-transistor logic gate mixed-mode simulations

In order to predict dynamic performance of the measured circuits, we performed mixed mode simulations of four-transistor logic gates configured to express NAND or XOR logic functions. Due to the computational complexity of these simulations, which comprise four full transistor structures being solved at the same time, in this case we used non-optimized device parameters, with dimensions as described in the following section.

Four-transistor simulation setup

The simulated transistor dimensions are similar to the fabricated devices (see Section 2.5). In this case, we considered three, 120 nm long GAA regions separated by 15 nm gaps but isolated by an optimized 1 nm equivalent gate oxide thickness. The nanowire channel is uniformly lowly p-doped (1×10^{15} cm^{-3}), and source and drain are defined as nickel silicide metal contacts (NiSi) at the nanowire extremities, at a distance of 5 nm from the polarity gate edges. In these simulations, the NiSi work function was set at 4.43 eV, consistently with performed measurements (see Section 6.2) and providing optimal symmetry between n and p-type operation in the simulated device characteristics.

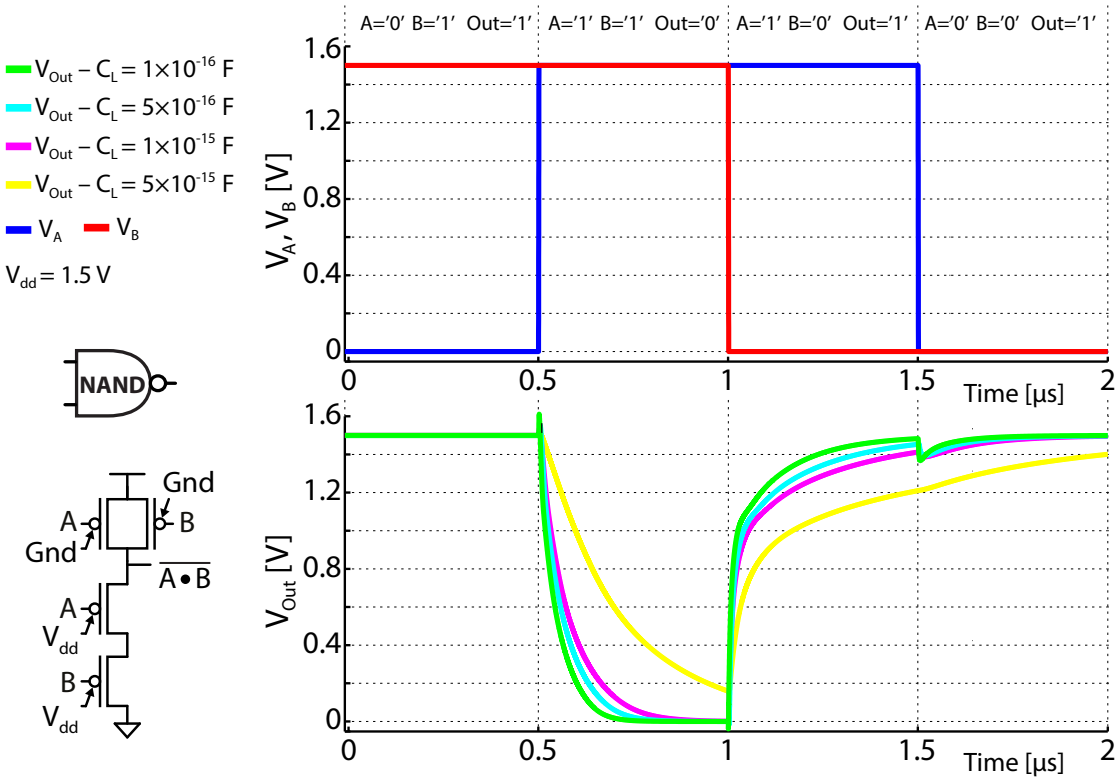


Figure 4.13 – Transient simulation for the four-transistor NAND logic gate with 1 ns input rise/fall times. Image adapted from [66].

Note that, due to the geometry of this device, stray capacitances between the CG and PG gate electrodes will influence performance when driven by the output of another gate. Therefore, we first performed capacitance simulations using 3D Sentaurus TCAD software, obtaining CG to PG capacitances in the range of $[2\times10^{-16}, 7\times10^{-16}]$ for wire diameters between 30 nm and 80 nm and a gate-to-gate polysilicon contact distance of 10 nm.

Simulated waveforms

Figure 4.13 shows the schematic and the output waveforms of a NAND logic gate for output load capacitances in the range $[10^{-16}, 5\times10^{-15}\,\mathrm{F}]$. Calculated delays at 50% V_{dd} for $C_{\mathrm{L}} = 10^{-16}\,\mathrm{F}$ are 31 ns and 9.7 ns for falling and rising transition, respectively. In this case, all transistors are pre-polarized by setting fixed biases to the PGs (V_{dd} for n-type and GND for p-type). Thus, differences in delays are mainly due to the presence of a two-transistor series in the pull-down network as in standard CMOS design. In Figure 4.14, the output waveforms of a XOR logic gate are shown for all input configurations and for the same C_{L} range as for the NAND gate. Significantly lower delays at 50% V_{dd} for $C_{\mathrm{L}} = 10^{-16}\,\mathrm{F}$ are obtained compared to the NAND case, with delays of 2.8 ns for the falling output transition (triggered by switching of the CG biases) and 11 ns for the rising output transition (triggered by a switching of the PG biases). In this case, we attribute the delay difference to the asymmetry in I_{d}–V_{g} characteristics between

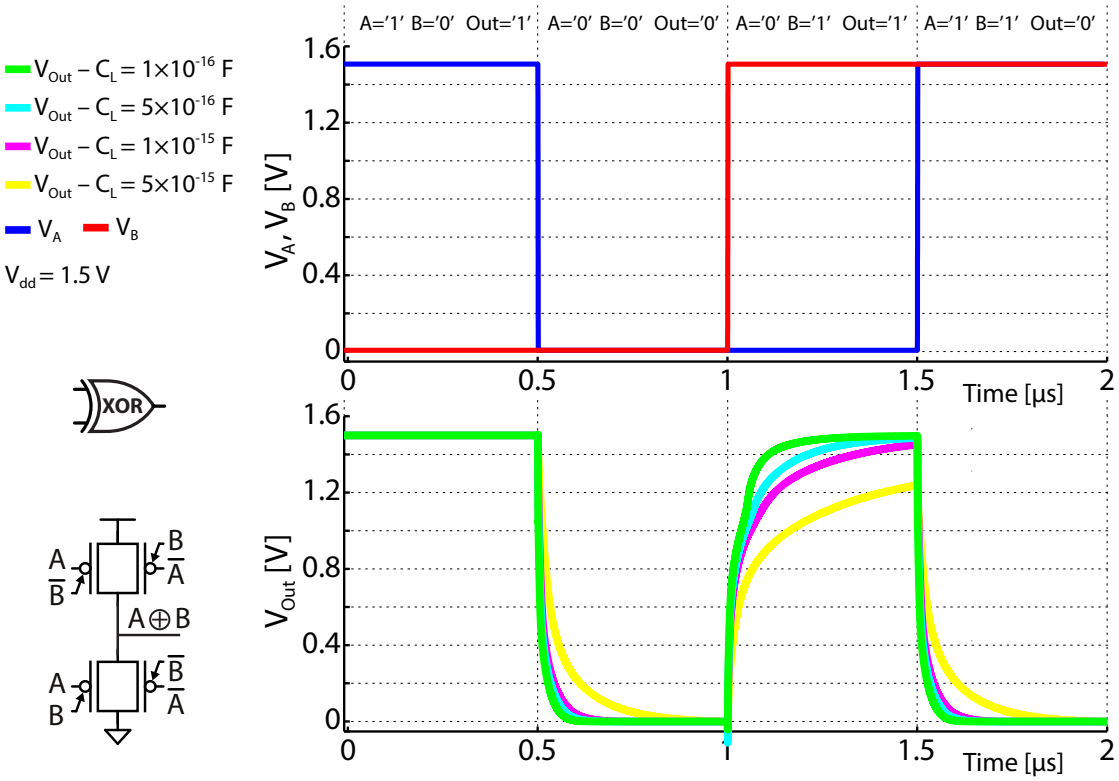


Figure 4.14 – Transient simulation for the four-transistor XOR logic gate with 1 ns input rise/fall times. Image adapted from [66].

the PG and CG inputs, i.e., the different shape of the I_d–V_{cg} and I_d–V_{pg} device curves (see Section 2.5.2).

Furthermore, the XOR circuit exhibits an interesting feature due to the presence of two transistors switching at the same time both in its pull-up and pull-down networks. Specifically, at any time, one transistor is strongly polarized (i.e., it is set as p(n)-type in the pull-up(down) network), correctly driving the output. The other transistor, (n(p)-type, respectively), will also turn on at the beginning of the transition, effectively boosting output switching. Only later, this transistor will see a decreasing V_{pg-s} while V_{out} rises, and will turn off before the end of the transition. Nonetheless, a faster response is observed at the gate output. This can be seen in Figure 4.14(b), where a slope change can be observed when the output approaches its final bias voltage. As a consequence, the simulated XOR is about 3× faster than the NAND, further demonstrating the advantage of this technology over CMOS in implementing complex functions.

4.5.2 Ring oscillator performance

As a last step in our performance evaluation of CP SiNWFETs at gate level, we considered a table model extracted from the single device simulation performed by TCAD for an optimized device

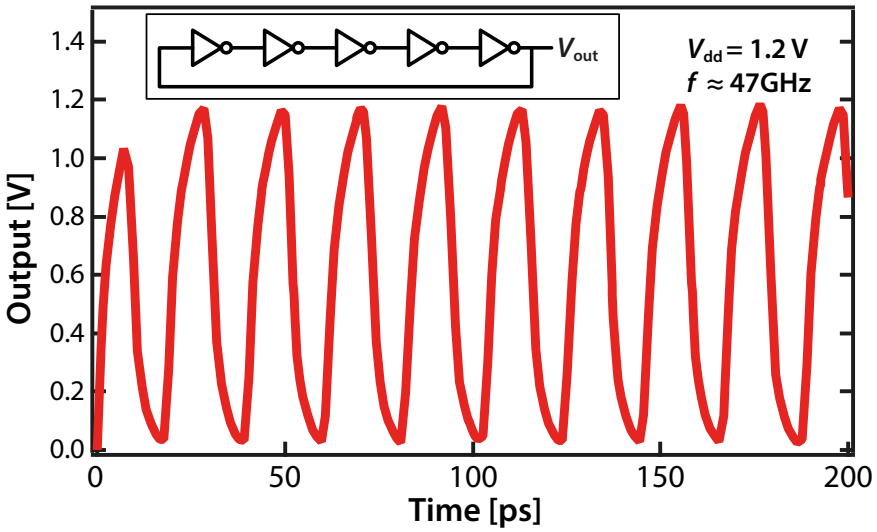


Figure 4.15 – Transient simulation of a 5-stages ring oscillator. The number of vertically stacked nanowires is 6 per device. 0.3 fF load capacitance is included in each stage to explicitly account for parasitics. Frequency reaches 47 GHz.

structure (see Section 2.5.3). This model was used to perform a SPICE transient simulation of a 5-stage ring oscillator. In Figure 4.15, we show a plot of the output of this circuit, forecasting operating frequencies well in the GHz range.

4.6 Chapter summary and contributions

Devices for the *Beyond CMOS* era have to integrate new degrees of freedom which can relax constraints at the physical and design levels. At the same time, many of these novel devices still require fabricated and measured demonstrations of operating circuits. In this chapter, we demonstrated the fabrication and electrical characterization of small logic gates built using the CP SiNWFETs devices first introduced in Chapter 2.

Specifically, we employ CP devices to design small logic gates that take advantage of their intrinsic in-field polarity control degree of freedom:

Basic configurable inverter circuit demonstration

As a first step to benchmark the device polarizability in a circuit, we connect two CP devices to implement and measure a configurable inverter circuit, composed of two transistors with identical physical structure.

First fully functional two-transistor XOR logic gate

Further, we feed both the CG and PG electrodes with logic inputs to demonstrate the first functional XOR logic gate with a complementary circuit structure. This logic gate fulfills the constraint of working at all positive gate voltages, providing a base for a cascadable and efficient *Beyond CMOS* logic technology.

Four transistor NAND/XOR logic gates

After demonstrating two-transistor logic gates, we scale up our design to include monolithic four-transistor circuits, pre-connected via pillar and gate polysilicon interconnections. These gates comprise four physically identical transistors, and show for the first time gates that can be configured to implement NAND (or, equivalently, NOR) and XOR logic operators by reconfiguring the same physical circuit. Moreover, these gates provide the required full-swing output voltage range required for efficient large circuit operation.

Performance evaluation through simulation

After the measurement results, in order to validate and support our fabrication and measurement approach, we performed mixed-mode simulations using two and four-transistor TCAD physical circuit models, showing that the limitations in output swing for the two-transistor XOR gate is embedded in its architecture, and that this limitation can indeed be removed by employing four-transistor circuits. Finally, the four-transistor and ring oscillator transient simulations highlight interesting features of the employed transmission gate structure and underline the potential of this technology for future circuit design.

Finally, our fabricated devices are the first demonstrated so far to combine remarkable device characteristics with sufficient symmetry and compatible operating voltages to enable complementary multi level logic synthesis and fully exploit the advantages of the efficient CP SiNWFET XOR implementation.

Further, as we have shown, more degrees of freedom at device level directly enable more compact and efficient logic gate designs with respect to standard CMOS technologies [27, 96]. At the same time, our top-down fabrication approach can implement CMOS-compatible, highly regular and dense arrays of nanowire stacks. Specifically, device regularity is an extremely important feature to reduce design constraints in current ULSI scaled devices, where double or triple-patterning techniques are employed to minimize device dimensions. In the next chapter, we will present a circuit-level benchmarking simulation flow we employed to evaluate the advantage of the presented logic gates as regular blocks in large logic circuits.

5 Polarity control in logic circuit design

In this chapter, we introduce a logic circuit benchmarking process flow implemented to evaluate the architecture level performance of CP FET devices as compared to conventional CMOS. The presented analysis considers a number of elements contributing to create efficient and reliable logic circuits using CP FET technologies. Specifically, system level aspects such as logic gate granularity, complexity and regularity are considered, showing that reconfigurable devices can provide promising advantages over conventional MOSFETs. Moreover, as mentioned in Section 1.3, the considered regular and reconfigurable architectures go hand in hand with the conservative design requirements of state-of-the-art scaled industrial devices. As a first step in our evaluation, we consider the use of a dedicated logic gate library built using CP FETs, and implement a logic design process flow to map a set of benchmark logic circuits using CP FET as well as conventional bulk MOSFET technology for comparison. Further, architectures such as FPGAs and Structured ASICs, based on LUTs and configurable logic blocks, are considered to evaluate the potential of CP devices in the context of regular fabrics.

In Section 5.1 we first overview the interest in logic circuit design using CP technology, further focusing on the system level advantages that these devices can provide. In Section 5.2, we present three relevant early works from the literature creating the base for our analysis. In Section 5.3, we present the static logic circuit design methodology we employed to build and evaluate CP-based logic gates with respect to CMOS at circuit level, including the selection of efficient gates to be employed for regular fabric architectures. In Section 5.4, we present the simulation tool flow and simulation results we obtained as area and delay performance of the CP-based static logic cells when mapping circuit benchmarks. In Section 5.6, we present some future perspectives and developments, citing a number of references to concurrent and ongoing research that started as a refinement of the presented results. Finally, Section 5.7 concludes the chapter, summarizing the contributions provided by the presented research work.

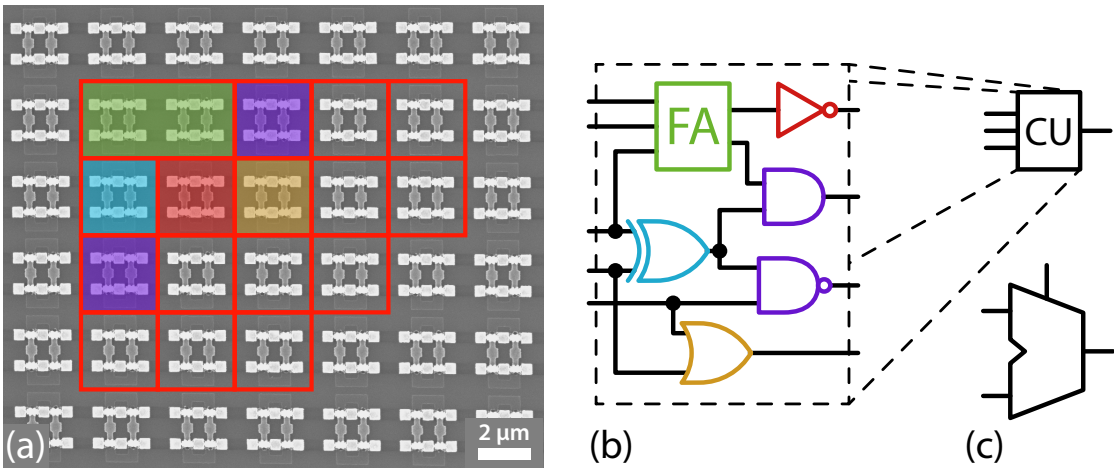


Figure 5.1 – (a) SEM micrograph overlay view of fabricated regular array of four-transistor tiles. The colors refer to the logic gates (b) implementable by configuring the interconnect of one or more of the repeated tiles, e.g. a FA requiring two tiles. In (c), the architecture-level logic blocks, e.g. a processor ALU or CU that are composed of the fine-grain logic gates.

5.1 Background

The current push towards device miniaturization, as mentioned in Chapter 1, is producing more and more stringent requirements to counteract the effects of variability at scaled technology nodes. As described in Chapters 2 and 3, the proposed SiNWFET devices, as well as CP CNTFETs, do not require sharp chemical doping profiles or doping wells. Thus, they permit the use of simplified design rules and more compact layouts. In particular, logic gates constructed using these technologies are particularly suited to implement regular fabrics, due to their intrinsic symmetry and high expressivity [26]. At the same time, the CP paradigm provides a new degree of freedom with respect to conventional DSD transistors, opening the way to interesting system level enhancements.

Specifically, a regular fabric is a layout style where gates and interconnect are designed in a regular manner in order to contrast the problem of increasing variability in scaled technology nodes [97]. Regular fabrics can be implemented at different levels, ranging from the simple application of *Resolution Enhancement Techniques* (RET)-friendly design rules [98] to the construction of inherently regular layouts composed of identical, repeated cells. Figure 5.1 shows a conceptual overview of the regular fabric design methodology. In (a), we show a fabricated regular fabric of repeated identical tiles. In general, these tiles can be fabricated at different granularity, from the single transistor to four-transistor (shown in the figure), to more complex logic blocks including memory elements. In Figure 5.1(b), the logic gates that can be implemented by one or more tiles (e.g., a *Full Adder* (FA) requires two four-transistor tiles in this technology [96]), which in turn compose the architecture-level blocks (c), such as a processor *Control Unit* (CU) or an *Arithmetic Logic Unit* (ALU). Finally, note that although every constraint on the regularity of a circuit will produce a penalty in terms of performance,

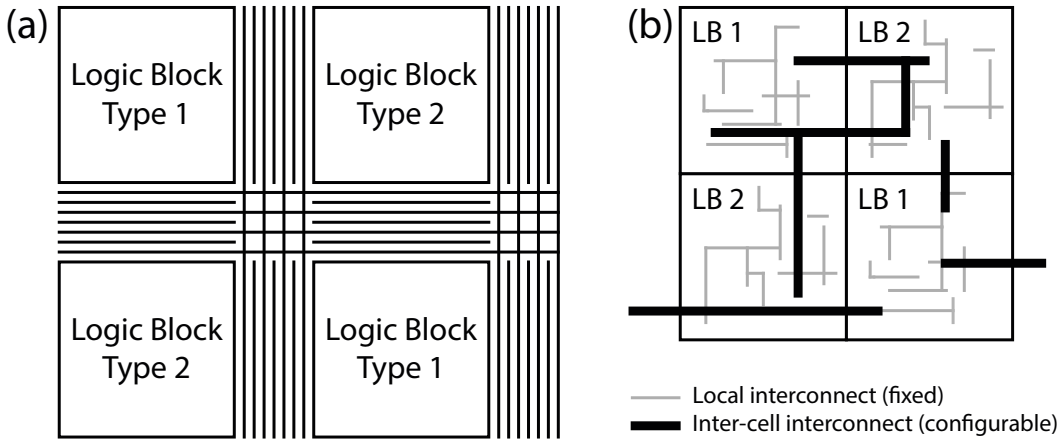


Figure 5.2 – Regular structures with two different alternating logic bricks. (a) Island-style FPGA and (b) Structured ASIC style. Image adapted from [27].

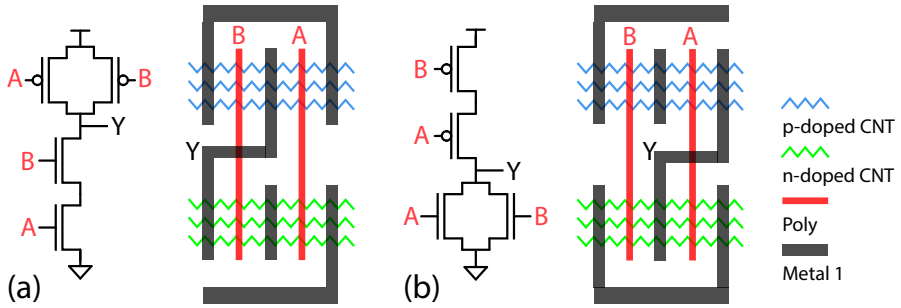


Figure 5.3 – A NOR2 gate layout (b) is derived from a NAND2 layout (a) by simply rotating it by 180°. Image adapted from [27].

regularity can help increase performance predictability, consequently helping to reduce design costs and to increase optimization [99]. At chip level, fabric grain size considerations go in parallel with configuration methodologies to obtain a range of architectures. Specifically, a trade-off is created between performance, overall manufacturing cost and configuration cost. Typically, the fabric can be configured by customizing only the higher level interconnect masks, thus providing a lower cost alternative to full custom ASICs, or using transistors connected to a reconfigurable memory. Figure 5.2 shows two types of regular structure in which these tiles can be embedded. The first one (a) is an island-style FPGA architecture, where logic bricks are interleaved with interconnect channels, that in turn can be configured by means of antifuses or using transistors driven by SRAM memory cells [100]. In FPGAs, the circuit is configured after the manufacturing is complete. The second architecture, shown in Figure 5.2(b), is called Structured ASIC, i.e. the logic cells are tightly packed and pre-structured, and only the higher level masks can are configured by the designer to obtain the desired circuit schematic [101]. Structured ASICs provide an interesting and cost-effective alternative to full-custom ASICs in the case of advanced technologies, due to the high cost of designing and fabricating masks that include increasingly strict design rules.

Regarding design regularity, thanks to the symmetric conductance of n and p-type CNTFETs [102], CNTFET logic gates can be constructed to be inherently symmetric, e.g. a NOR (shown in Figure 5.3(a)) gate can be built from a NAND one (Figure 5.3(b)) by simply rotating its layout by 180°. Moreover, CNTFETs have a channel which is isolated from the substrate, and do not require wells to obtain proper functionality. This enables the construction of a layout consisting of a chessboard-like tiling of dual logic gates, i.e. a logic cell and its dual produced by switching the *Pull-Up* (PU) and *Pull-Down* (PD) networks topology, without significantly reducing the overall macro-regularity of the layout. Note that, from recent results in SiNW technology (see Section 2.2), in particular the demonstration of symmetric n and p-type characteristics for CP SiNWFETs, these design techniques can be directly applied to the use with SiNWs, and could ultimately lead to faster and more efficient logic circuit design [95, 103].

Further, in [28], a design methodology was introduced, consisting of a static complementary logic, where the in-field reconfigurability of CP FETs is exploited to produce logic gates with high expressivity, capable to implement binate functions such as XOR at a low area cost, still providing all the advantages of complementary static logic such as CMOS (see Sections 4.1.2 and 5.2.3). In the following, we will then consider regularity aspects and their conjunction with this novel CP-based gate design methodology.

5.2 State-of-the-art

As previously mentioned, the gate design and circuit level benchmarking proposed in this chapter temporally precedes the device and circuit fabrication works presented in Chapters 2 to 4. As such, in this section we will focus on methodologies developed before or in parallel with our analysis, mostly relying on simulations using simple or more advanced device and circuit-level models and optimization tools.

5.2.1 Circuit design using reconfigurable dynamic logic gates

The first work described in literature utilizing CP devices to design logic circuits, was presented by I. O'Connor *et al.* [104, 105], and exploited the unique polarization feature of these devices to produce configurable dynamic logic blocks. In particular, at this early time of publication (2006–2007), the only demonstrated fabricated devices showing electrostatic polarity control were the devices built by IBM using CNTFETs [19] and bottom-up SiNWFETs [45]. As described in Section 2.2, these devices showed only partial configurability, and high voltage ranges were needed to produce acceptable n or p-type device characteristics. For this reason, at logic design level, CNTFETs were chosen as prime device technology for the presented evaluations. Moreover, device polarization signals were fed by appropriate polarization voltage sources in simulations.

Figure 5.4 shows one of the designed reconfigurable dynamic logic blocks (CNT-DR6F), com-

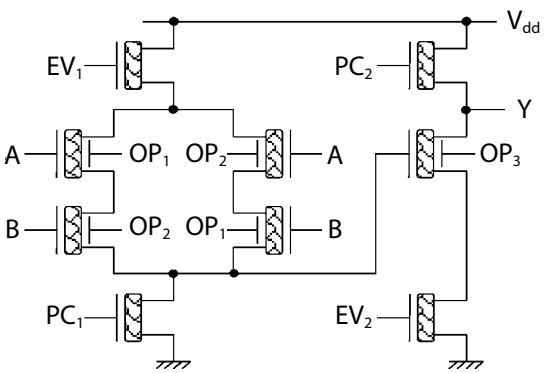


Figure 5.4 – Schematic of the CNT-DR6F reconfigurable 8-function dynamic logic gate. Image adapted from [105].

OP_1	OP_2	OP_3	Y
+V	+V	+V	$\overline{A \cdot B}$
+V	+V	−V	$A \cdot B$
+V	−V	+V	$\overline{A \oplus B}$
+V	−V	−V	$A \oplus B$
−V	+V	+V	$\overline{A \oplus B}$
−V	+V	−V	$A \oplus B$
−V	−V	+V	$A + B$
−V	−V	−V	$\overline{A + B}$

Table 5.1 – 3-input configurations and corresponding eight basic binary logic functions implemented by the CNT-DR6F logic gate. Table adapted from [105].

prising four CP devices in the first logic gate stage, followed by an inverter/buffer stage comprising one further CP device [105]. By selecting a positive or negative voltage for the configuration signals OP_1, OP_2 and OP_3, a number of Boolean functions could be implemented using the same physical circuit. Table 5.1 lists all the possible device configurations, each associated with the corresponding function implemented by the circuit. This early presented gate design is very promising from a reconfigurability standpoint, due to the high number of Boolean functions implemented by a low transistor count—8 functions for 9 transistors—. Nonetheless, due to the *weak* transistor polarization problem (see Section 4.1.2) for negative (−V) polarization signals, for which some transistors are polarized as n-type in the pull-up networks of the gate of Figure 5.4 (or, vice versa, as p-type in the pull-down network), this reconfigurable gate suffered from output swing degradation. For this reason, in subsequent works on dynamic logic, the authors enhance expected cell output quality employing transmission gate structures similar to the approach used in Chapter 4 for static logic gate design [106], at the cost of increased complexity and larger area occupation for the cells (see, e.g., cell 16F-DS-DRLC).

5.2.2 Dynamic Generalized NAND/NOR PLA design

Along the lines of constructing compact reconfigurable dynamic logic gates using CP devices, *Generalized NAND/Generalized NOR* (GNAND/GNOR) gates were proposed by M. H. Ben Jamaa *et al.* in 2008 [107]. Figure 5.5(a) shows the schematic of a GNOR logic gate, where parallel CP transistors are configured by external C_n configuration PG (V_{pg}) biases to behave as n or p-type, and logic inputs A to D feed transistor CGs (V_{cg}). In these gates, in addition to the high/low PG bias voltages (+V, −V) as used in Table 5.1, the authors envision the use of an intermediate V_{pg} polarization for which the device is expected to be always off [108] to expand the capabilities of the GNAND/GNOR gates by arbitrarily excluding input literals from the

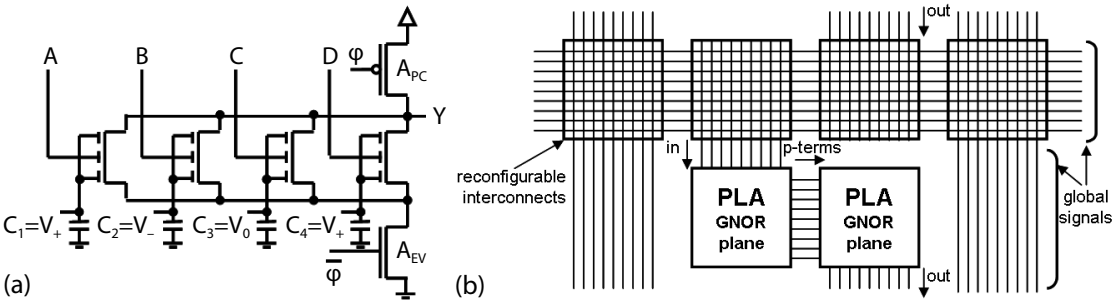


Figure 5.5 – (a) Generalized NOR logic gate configured as $Y = \overline{A \cdot \overline{B} \cdot D}$. (b) Programmable logic array architecture based on configurable GNOR planes. Image adapted from [107].

output calculated functions.

Further, this work proposes the first analysis on the use of configurable gates based on CP technology (using CNTFETs) for the design of regular circuits, in this case using *Programmable Logic Arrays* (PLAs) as underlying fabric for FPGA architectures. In particular, the authors consider technology design rules and performance data for CNTFETs and create a first estimation of the advantage in terms of circuit area and delay for PLA-based FPGA architectures using CP or a comparable conventional MOSFET technology, with design parameters taken from the ITRS. Finally, a performance advantage of about 2× in terms of area × delay is obtained for the proposed GNAND/GNOR architecture. Note, however, that also the designed GNAND/GNOR gates suffer the same limitations in output swing and performance expected for the previous cells of Section 5.2.1, due to the *weak* polarization of transistors in certain V_{pg} configurations. Therefore, further considerations and a more reliable modeling of the designed circuit architectures were required in order to create more accurate predictions on the performance advantages provided by using CP devices.

5.2.3 Polarity control based static logic design

In order to address the limitations and design complexity introduced by the use of dynamic logic, in particular due to the lack of full-swing output for the proposed GNAND/GNOR gates, M. H. Ben Jamaa *et al.* [28] proposed a paradigm shift from dynamic to static complementary logic design. In this further step, the authors describe a library of logic gates based on CP FETs that for the first time provide full-swing output and can be cascaded and directly used to map complex multi-level logic circuits. This improvement is achieved by the introduction of TGs, as described in Section 4.1. With this library, further described in Section 5.3, technology mapping is performed on a set of multi-level benchmark circuits, in order to estimate area and delay performance with respect to a CMOS library. The estimations proposed in this work rely on a simple switch-level RC CNTFET circuit model [94] to calculate *Fan-Out of 4* (FO4) delays for the library logic gates. In this evaluation, after normalization to the intrinsic fan-out of 1 inverter delay, a performance advantage of the CP CNTFET library of 38% in terms of area reduction and performance improvement of 6.9× is obtained with respect to CMOS.

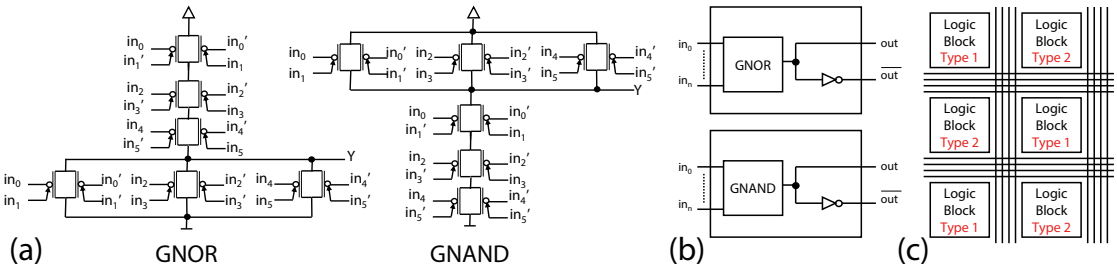


Figure 5.6 – (a) Static GNAND/GNOR logic gates with three TGs in the PU and PD networks. (b) Conceptual logic block containing a GNAND/GNOR gate, providing dual rail output. (c) Envisioned island-style FPGA baseline architecture for the GNAND/GNOR regular fabrics. Image adapted from [28].

5.3 Static logic circuit design with CP devices

The high expressivity given by CP static logic makes it a great choice for constructing configurable gates which can be implemented in arrays to produce regular fabrics. In the following, we present the application of this logic design methodology to introduce a refined set of configurable gates to be used to design regular fabrics.

The complementary static logic design methodology first introduced in [28], exploits the tunable polarity of CP FET devices to produce logic gates which implement binate functions such as XNOR (see Figure 4.2(d)) with low area occupation, thus producing more compact gates with respect to conventional CMOS. In particular, in this work, the authors define a 46-gate library, shown in Table 5.2, by considering all the gates that can be implemented with up to three transistors or TGs in the PD (and, equivalently, the PU) gate networks. As previously stated, only a rough evaluation based on a simple RC transistor model is proposed in this work. In the remainder of this chapter, we then consider the 46-gate library as a base for a more detailed investigation in terms of performance with respect to CMOS, as well as for the selection and evaluation of a number of gates when used to implement regular fabrics. Here, we embed a full SPICE-based CNTFET compact model (see Section 5.4.2) into our tool flow. Specifically, CNTFETs were chosen as a promising and convenient technology, due to the availability of reliable device models and their intrinsic SB device typology. Nonetheless, all presented analyses are presented in a normalized form, and results can be extended to any CP technology. In the following, we first introduce the problem of dual polarity signals required to feed TGs and define three gate design styles that can provide an optimum use of inverters when mapping a circuit. We then make some considerations regarding regular fabric design, i.e., the definition of sets of *sub-functions* used to map a circuit benchmark starting from a repeated logic gate.

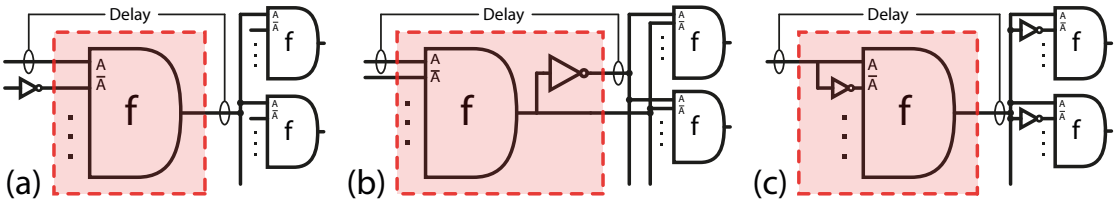


Figure 5.7 – Standard cell polarity-aware design. Shaded areas define the extent of the analyzed cells. Delays are calculated as shown between the slowest input/output of cells, depending on the inverter configurations. (a) Inverters are in independent cells. (b) An inverter is included at the output of each cell. (c) Inverters are included at the input of cells only when dual polarity inputs are required. Image adapted from [27].

5.3.1 Signal-polarity-aware design

As previously mentioned, the implementation of this library includes TGs. For proper operation, these transistor pairs need to be fed by dual polarity inputs. In circuit implementations, this translates into the need of a large number of inverters in the circuit and of dual rail interconnect, i.e., wire couples carrying negated signals. To understand how this requirement affects performance, and to find a design methodology to implement configurable cells for regular fabrics, we analyzed areas and delays under three different input and output conditions, shown in Figure 5.7. In the following, we will refer to these conditions as designs (a), (b) and (c):

(a) FO4 condition, with an output load of 4 unloaded gates equal to the one under measurement

(b) FO4 with an extra inverter at the output of the gate under analysis

(c) FO4 with an inverter at any input which requires both polarities (transmission gates)

Design (a) is the simplest and requires inverter cells to provide the dual rail signals for the TGs. Since cells produce only single rail outputs, a part of interconnect will be single rail and a part dual rail. Design (b) reduces the number of cells by inserting inverters directly at the output of gates. In this case, the size of the inverters which produce the negated signals cannot be optimized at design time. Although the number of cells is reduced with respect to design (a), dual rail interconnect is always necessary. At last, design (c) is a configuration which does not require dual rail interconnect. Even if the number of inverters is larger than in cases (a) and (b), their size is self-optimized since a unit size inverter is added only when needed to drive a gate input. Moreover, since inverters are typically inserted as buffers in regular layouts, we expect their cost in terms of area to be compensated by reduced signal noise and better delay predictability.

Gate	Function	Gate	Function
F00	$\overline{A}$	**F23**	$\overline{A+(B\oplus D)\cdot C}$
F01	$\overline{A\oplus B}$	F24	$\overline{(A\oplus D)+(B\oplus D)\cdot C}$
F02	$\overline{A+B}$	F25	$\overline{A+(B\oplus D)\cdot(C\oplus D)}$
F03	$\overline{A\cdot B}$	F26	$\overline{(A\oplus D)+(B\oplus D)\cdot(C\oplus D)}$
F04	$\overline{(A\oplus B)+C}$	**F27**	$\overline{(A\oplus D)\cdot B\cdot C}$
F05	$\overline{(A\oplus B)\cdot C}$	F28	$\overline{(A\oplus D)\cdot(B\oplus D)\cdot C}$
F06	$\overline{(A\oplus B)+(A\oplus C)}$	F29	$\overline{(A\oplus D)\cdot(B\oplus D)\cdot(C\oplus D)}$
F07	$\overline{(A\oplus B)\cdot(A\oplus C)}$	**F30**	$\overline{(A\oplus D)+(B\oplus E)+C}$
F08	$\overline{(A\oplus B)+(C\oplus D)}$	F31	$\overline{(A\oplus D)+(B\oplus D)+(C\oplus E)}$
F09	$\overline{(A\oplus B)\cdot(C\oplus D)}$	**F32**	$\overline{((A\oplus D)+(B\oplus E))\cdot C}$
F10	$\overline{A+B+C}$	**F33**	$\overline{((A\oplus D)+B)\cdot(C\oplus E)}$
F11	$\overline{(A+B)\cdot C}$	F34	$\overline{((A\oplus D)+(B\oplus D))\cdot(C\oplus E)}$
F12	$\overline{A+B\cdot C}$	F35	$\overline{((A\oplus D)+(B\oplus E))\cdot(C\oplus D)}$
F13	$\overline{A\cdot B\cdot C}$	**F36**	$\overline{(A\oplus D)+(B\oplus E)\cdot C}$
F14	$\overline{(A\oplus D)+B+C}$	**F37**	$\overline{A+(B\oplus D)\cdot(C\oplus E)}$
F15	$\overline{(A\oplus D)+(B\oplus D)+C}$	F38	$\overline{(A\oplus D)+(B\oplus E)\cdot(C\oplus E)}$
F16	$\overline{(A\oplus D)+(B\oplus D)+(C\oplus D)}$	F39	$\overline{(A\oplus D)+(B\oplus E)\cdot(C\oplus D)}$
F17	$\overline{((A\oplus D)+B)\cdot C}$	**F40**	$\overline{(A\oplus D)\cdot(B\oplus E)\cdot C}$
F18	$\overline{((A\oplus D)+(B\oplus D))\cdot C}$	F41	$\overline{(A\oplus D)\cdot(B\oplus D)\cdot(C\oplus E)}$
F19	$\overline{((A\oplus D)+B)\cdot(C\oplus D)}$	**F42**	$\overline{(A\oplus D)+(B\oplus E)+(C\oplus F)}$
F20	$\overline{((A\oplus D)+(B\oplus D))\cdot(C\oplus D)}$	**F43**	$\overline{((A\oplus D)+(B\oplus E))\cdot(C\oplus F)}$
F21	$\overline{(A+B)\cdot(C\oplus D)}$	**F44**	$\overline{(A\oplus D)+(B\oplus E)\cdot(C\oplus F)}$
F22	$\overline{(A\oplus D)+B\cdot C}$	**F45**	$\overline{(A\oplus D)\cdot(B\oplus E)\cdot(C\oplus F)}$

Table 5.2 – The 46-gate static logic library first defined in [28]. In italics, the gates which can be implemented with the same resources and topology in CMOS technology. In bold, the selected configurable logic gates for regular fabrics.

5.3.2 Logic gates for regular fabrics

Each configurable gate is defined by its logic function. In a regular architecture, such as a Structured ASIC, the logic gates are pre-configured and only part of the interconnect can be user-configured. By configuring the interconnect, each input of a gate can be fed by either the output of another gate or by a constant value ($'0'$ or $'1'$). Each configurable gate is thus capable to implement a set of *sub-functions* with a number of inputs smaller or equal to the one of the logic function which represents it. For each gate, we can define a dual gate as the one produced by simply swapping the topologies of its PU and PD networks.

As we have seen in Section 5.1, CP FET static logic is particularly suited to build configurable gates to implement chessboard-like regular fabric layouts with alternating dual cells. Dual cells, used together, provide a higher number of implemented functions than a single gate. Since in the case of CNTFETs or symmetric SiNWFETs, gates can be produced by simply rotating a layout of 180°, it is possible to produce chessboard-like layouts which are more

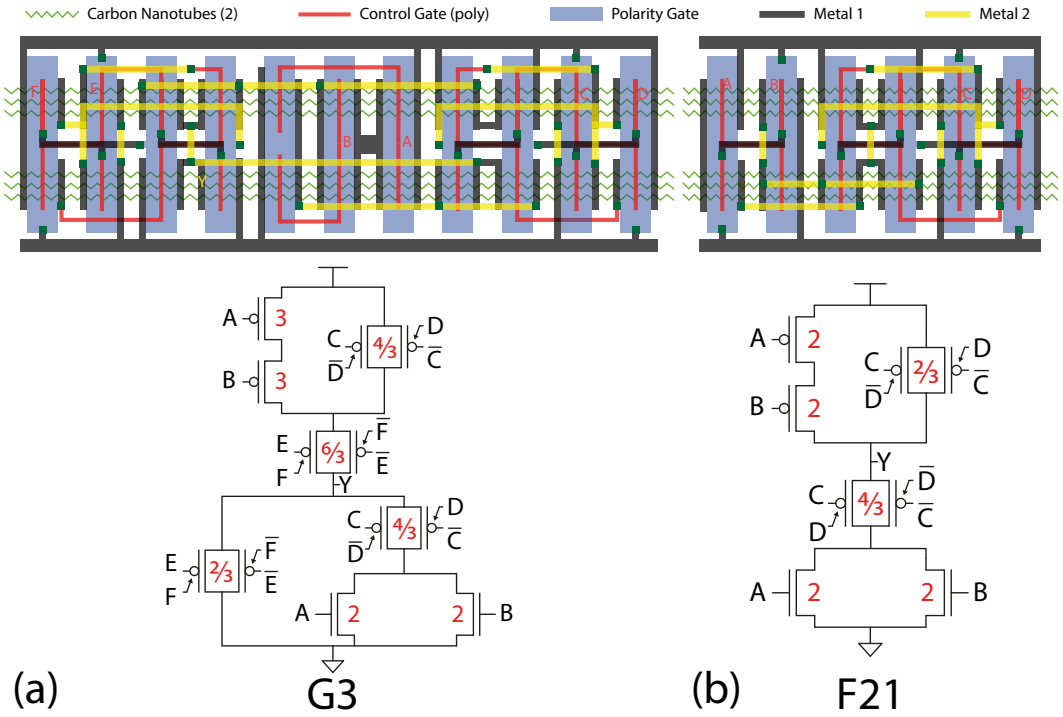


Figure 5.8 – On top, tentative conceptual layout views of CP CNTFET logic gates (a) G3 and (b) F21. At the bottom, the respective circuit schematics, indicating the size of each transistor.

regular than their CMOS counterparts, without modifying transistor sizes to obtain dual gates.

From the 46-gate static logic library, we selected a number of gates which could be used as bricks to design regular fabrics (shown in bold in Table 5.2). We included the gates which: 1) contain at least one transmission gate and 2) cannot be implemented by another logic gate with the same topology by feeding two or more of its inputs by a single signal. For example, function F06 = $\overline{(A \oplus B) + (A \oplus C)}$ can be implemented from F08 = $\overline{(A \oplus B) + (C \oplus D)}$ by feeding inputs A and C by the same external signal.

In order to evaluate gates with larger granularity than those from the 46-gate library, we also include in our analysis four gates (two gates plus their duals) with four transistors or TGs in the PU and PD networks (see Table 5.3). These gates have been arbitrarily chosen on the base of their high number of implemented *sub-functions*, and the concurrent low *redundancy* between a gate and its dual, i.e. the set of implemented *sub-functions* of the gate overlaps in small proportion with that of its dual gate. For example, a layout consisting of both gates G3 and G4 can implement 77% more sub-functions than a layout including only gate G3.

In Figure 5.8 (bottom), we show the schematics of gates F21 and G3, indicating the sizing of each transistor. TG sizing refers to the size of each one of the transistors implementing the TG. Figure 5.8 (top) shows the approximate layouts for the two gates. Since n and p wells are not needed in this technology, layouts can be made more compact than in CMOS. Moreover,

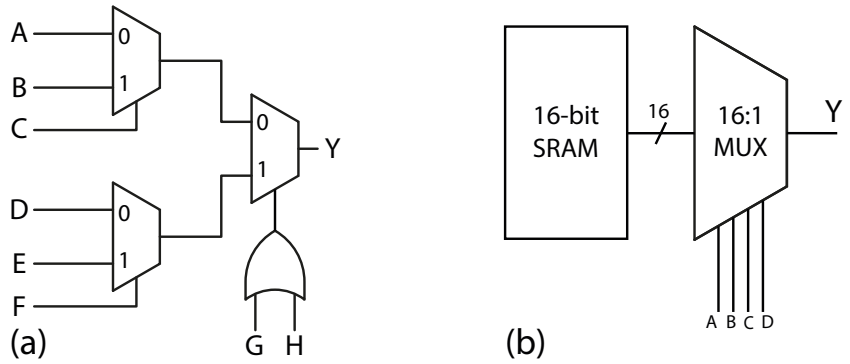


Figure 5.9 – (a) The ACTEL ACT1 configurable logic cell [100]. (b) The considered high-level 4-input LUT structure.

n and p-type transistors do not need to be separated in distinct zones of the cell layouts, which enables more optimized designs.

5.4 Simulation results

This section presents the results of the simulations we performed to evaluate various configurable logic gates. After a preliminary evaluation of the library of 46 gates, we compare the performance of the logic gates when used as bricks to implement regular fabrics. We then compare the most efficient gates with the Actel ACT1 logic block, shown in Figure 5.9(a), and 4-input LUTs (b). Finally, we compare the best regular tiling, F21–F22, with standard cells in the same technology.

5.4.1 Characterization of individual logic gates

For each gate of the library in Table 5.2, we evaluated areas (normalized to the unit size transistor) and delays (normalized to the intrinsic technology delay) in the worst (w) and average (a) cases. This first characterization step is required to produce area and delay information for each individual gate. The results for each individual gate are then assembled in an updated library used for technology mapping (see Section 5.4.2. Note that we normalize all values in

Gate	Function
G1	$\overline{(A\cdot B)+(C\cdot(D\oplus E))}$
G2	$\overline{(A+B)\cdot(C+(D\oplus E))}$
G3	$\overline{((A+B)\cdot(C\oplus D))+(E\oplus F)}$
G4	$\overline{((A\cdot B)+(C\oplus D))\cdot(E\oplus F)}$

Table 5.3 – Selected gates with four TG or transistors in the PU and PD networks. G2 and G4 are respectively the duals of G1 and G3.

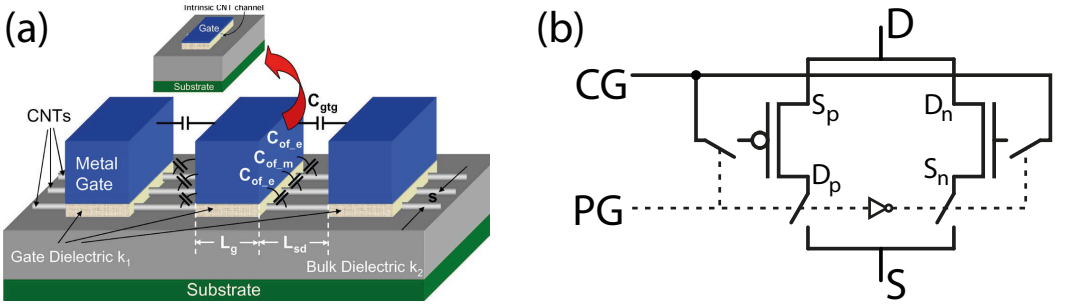


Figure 5.10 – (a) Conceptual view of the Stanford CNTFET model 3D structure and parasitics. Image reproduced from [109]. (b) Adapted CNTFET behavioral model to implement CP CNTFETs for SPICE simulations. The model is inspired from [105].

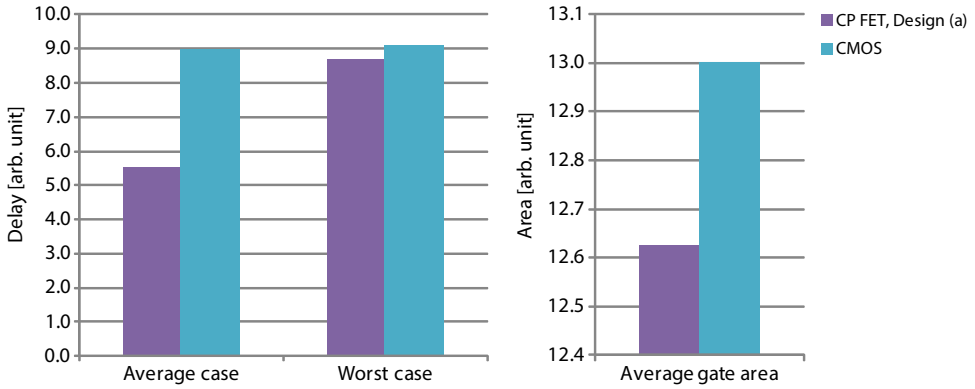


Figure 5.11 – Comparison of average values of area and normalized delay between CP FET design (a) and CMOS.

order to understand and highlight the benefit coming from the intrinsic device polarization degree of freedom, associated with the TG static logic design methodology.

Specifically, we performed SPICE simulations using the Stanford CNTFET model [110, 109, 111], using a minimum feature size of 32 nm for the CNTFETs. The model is adapted to behave as a selectable superposition of an n and a p-type device, similar to the one used in [105]. Figure 5.10(a) shows a conceptual 3D view of the Stanford model structure, including channel region parasitics, e.g., the capacitances between adjacent gates and gate to S/D electrodes. Figure 5.10(b) shows the implemented schematic structure of a CP CNTFET, where the PG selects between n and p-type behavior. Note that, in the shown simulations, the PG-to-output delay is arbitrarily selected as equal to the CG-to-output delay. This choice, in first approximation, is justified by the fact that, due to the intrinsic symmetry of an XOR operator with respect to its two inputs, CG and PG logic inputs can be swapped without changing the circuit functionality. If the logic signals included in the circuit critical path are then always applied to the smallest delay gate electrode, the difference in delay between CG and PG electrodes is not expected to produce a difference in overall circuit delay.

Further, it is very hard to make a fair comparison of the technology described here with other

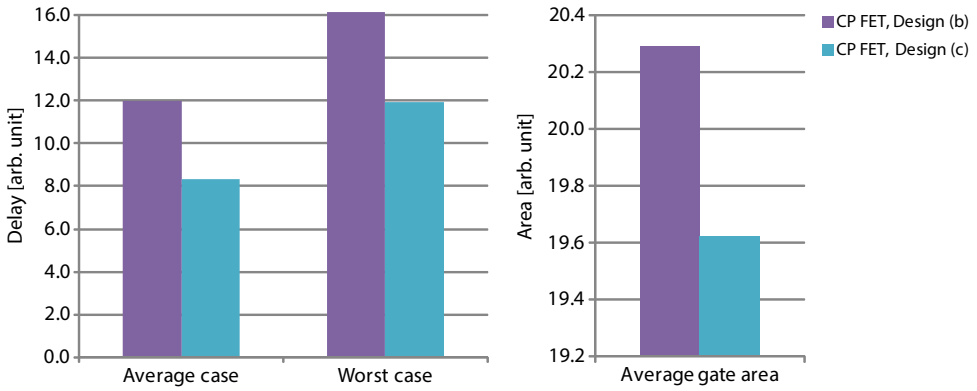


Figure 5.12 – Comparison of area and normalized delay between design (b) and design (c).

existing technologies. For this reason, we present a comparison with normalized 32 nm CMOS for which, even though the devices have a different structure, cells can be compared to those built with CNTFETs in terms of area in first approximation. We constructed a library including the 7 CMOS gates (shown in italics in Table 5.2) which can be built with the same topology as for CNTFETs, with no more than three transistors in every PU and PD network. All CMOS cells were simulated using the 32 nm CMOS *Predictive Technology Model* [112].

In Figure 5.11, we show a comparison of the average values of area and normalized delay calculated over all the individual gates in the library for design (a) and for CMOS. All delays are shown after normalization to the intrinsic technology delay, with $\tau_{\mathrm{CNTFET}} = 0.59\,\mathrm{ps}$ and $\tau_{\mathrm{CMOS}} = 3.0\,\mathrm{ps}$ [113]. Our simulations show a 39% normalized delay reduction for CP CNTFET with respect to CMOS. Even if only 7 gates with this topology can be constructed in CMOS, the average gate area comparison shows how CNTFET cells utilize a similar amount of resources of CMOS to produce a larger number of functions. If we consider the normalized *Area* × *Delay Product* (ADP) (average case), we obtain an improvement of 40% for design (a) over CMOS.

In Figure 5.12, we show the average values of area, normalized delay (average case) and normalized delay (worst case) over the 46-gate library for designs (b) and (c). When comparing these two designs, we observed a reduction of 3.3% in area of design (c) compared to (b). At the same time, we observed a much more efficient exploitation of inverters in design (c), obtaining a reduction of 30.5% in the average and 25.8% in the worst case gate delay. Since inverters in design (b) have a pre-defined sizing (since we cannot know the fan-out of a gate before mapping it in a circuit), even gates with low fan-out will be penalized by the presence of an inverter at the output, thus increasing the average gate area.

5.4.2 Full logic library characterization

After producing a gate library including delay and area information for each gate, we used the ABC logic synthesis system [114] to perform logic minimization and technology mapping over a set of several benchmark circuits taken from the ISCAS'85 set [115]. With the results of

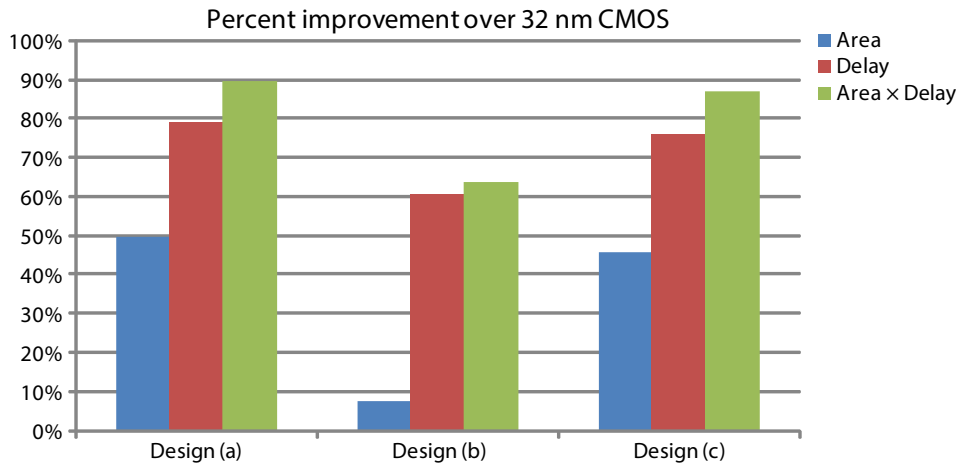


Figure 5.13 – Percent improvement of CNTFET gates over CMOS in terms of area, normalized delay and ADP.

technology mapping, a meaningful comparison can be made among all three design configurations (a), (b) and (c). In Figure 5.13, we see a summary of the percent improvement over 32 nm CMOS in terms of area, normalized delay and normalized ADP for the three design configurations. The percentages represent the average circuit values obtained through technology mapping on a set of benchmark circuits with each design configuration (a), (b) and (c). All the design configurations show a considerable improvement over CMOS in terms of ADP, between ~60% (design (b)) and ~90% (design (a)). If we consider that the average values for the single gates of the library showed an improvement of only 40% in terms of ADP over the CMOS library, we can see how the increased expressive power given by the CP CNTFETs improves performance substantially, when we look at the average performances of mapped circuits for each library.

As we expected, design configurations (a) and (c) give the best results, and the performance of these two configurations is very similar. For the considerations we presented in Section 5.3.1, we can then consider design (c) a valid possibility for the implementation of an efficient library of standard cells using CP CNTFETs.

5.4.3 Characterization of configurable gates

The complete list of configurable logic gates we characterized is shown in Table 5.4. For each gate, we give the number of inputs N_{in}, the number of implemented sub-functions N_f, area and average normalized delays for design configurations (b) and (c) (see Section 5.3.1). We chose to evaluate the performance of gates implemented with design (b) and (c) since design configuration (a) has the limitation of inverters, which we assume not to be available in the regular fabric. Thus, for design (a), a number of cells would have to be used to implement the required inverters, causing a large loss in terms of area.

Function Data			Gate Area [arb. unit]		Average Delay [arb. unit]	
Name	N_{in}	$N_{f(b)}$	**Design (b)**	**Design (c)**	**Design (b)**	**Design (c)**
F04	3	8	15.67	11.67	11.67	9.73
F04–F05	3	12	15.67	11.67	11.67	9.73
F08	4	16	17.33	17.33	9.69	7.01
F08–F09	4	28	17.33	17.33	9.69	7.01
F14	4	12	22.00	18.00	15.22	10.74
F14–F27	4	20	22.00	18.00	15.22	10.74
F17	4	16	20.33	16.33	13.47	9.47
F17–F23	4	20	20.33	16.33	13.47	9.47
F21	4	15	20.67	16.67	10.26	7.15
F21–F22	4	24	20.67	16.67	10.26	7.15
F30	5	28	24.00	24.00	13.89	10.05
F30–F40	5	52	24.00	24.00	13.89	10.05
F32	5	32	21.67	21.67	13.65	9.70
F32–F37	5	52	21.67	21.67	13.65	9.70
F33	5	48	22.00	22.00	11.26	7.91
F33–F36	5	84	22.00	22.00	11.26	7.91
F42	6	47	26.00	30.00	11.52	8.33
F42–F45	6	90	26.00	30.00	11.52	8.33
F43	6	105	23.33	27.33	11.00	7.82
F43–F44	6	105	23.33	27.33	11.00	7.82
G1	5	34	25.33	21.33	14.45	11.20
G1–G2	5	44	25.33	21.33	14.45	11.20
G3	6	105	29.33	29.33	9.01	7.39
G3–G4	6	186	29.33	29.33	9.01	7.39
ACT1	8	702	33.00		16.08	
LUT-4	4	65536	169.00		49.61	

Table 5.4 – Configurable gates for regular fabrics, in single cell configuration or dual cell tiling (e.g. F04F05). Number of inputs N_{in}, number of implemented functions $N_{f(b)}$ for the (b) design case, normalized area and average normalized delays are given for each cell. For the ACT1 and 4-LUT, values are relative to 32 nm CMOS.

Comparison among configurable gates

In Figure 5.14, we present a summary of the total values of normalized ADP obtained by mapping our benchmark circuit set using each one of the logic gates of Table 5.4. Results are shown for every logic gate, with single or dual tiling, for design configuration (c). Note that the x-axis labels in Figure 5.14 refer to the logic cell for the single-gate layout, so for dual-gate layouts, the respective dual cells are also present.

From this plot, we can extract two groups of cells, one group showing high efficiency (F17, F21, F33, G3) and one presenting lower-than-average efficiency (F14, F30, F42). In Table 5.5, we

High Efficiency Gates		Low Efficiency Gates	
Gate	**Function**	**Gate**	**Function**
F17	$\overline{((A \oplus B) + C) \cdot D}$	F14	$\overline{(A \oplus B) + C + D}$
F21	$\overline{(C + D) \cdot (A \oplus B)}$	F30	$\overline{(A \oplus B) + (C \oplus D) + E}$
F33	$\overline{((A \oplus B) + E) \cdot (C \oplus D)}$	F42	$\overline{(A \oplus B) + (C \oplus D) + (E \oplus F)}$
G4	$\overline{((A \cdot B) + (C \oplus D)) \cdot (E \oplus F)}$		

Table 5.5 – Sets of high and low ADP configurable logic gates.

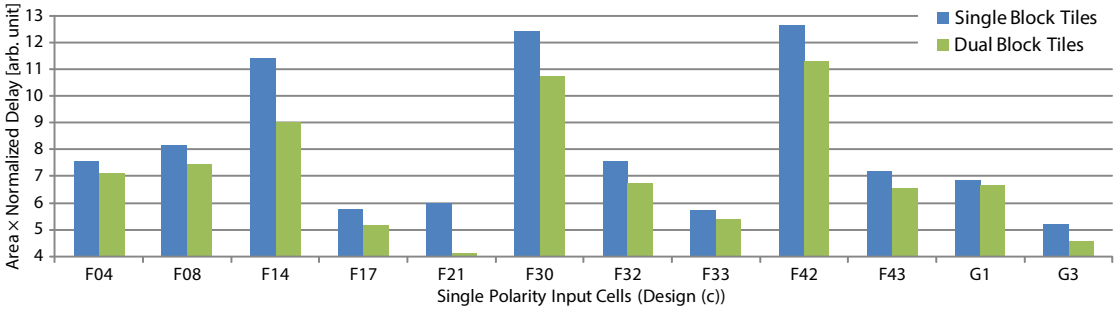


Figure 5.14 – Comparison, in terms of normalized ADP, between single-gate layout and dual-gate layout for the different single input polarity cells (design (c)). x-axis labels refer to the logic cell for the single-gate layout, so for dual-gate layouts, the respective dual cells are also present.

resume the list of these gates with the respective representative function. We do not report here the same results for the gates constructed with design configuration (b), since their performance was on average 30% lower, in terms of normalized ADP, than the one for design (c).

If we consider XORs as if they were single literals, an immediate evidence from these data is that low efficiency gates all share a common function structure, consisting of a disjunction (OR) of three terms, while all efficient gates have an *And-Or-Inverter* (AOI) main structure. This also explains the high performance of the G3–G4 tiling, which is more complex but can implement all *sub-functions* implemented by tilings F21–F22 and F33–F36.

Comparison with standard cells

To better evaluate the potential of CP CNTFET based configurable gates, we compared the regular fabrics with a standard cell circuit implementation in the same technology. In Figure 5.15, we present this comparison for the best CNTFET-based configurable gate, F21. In the plot, we compare the normalized ADP values, on average over a set of mapped benchmark circuits, for all four types of tiling implemented with F21, i.e. single and dual tiling with the gates in either design configurations (b) and (c). For standard cell technology mapping, we give the values for all three design configurations (a), (b) and (c) and for the 32 nm CMOS library.

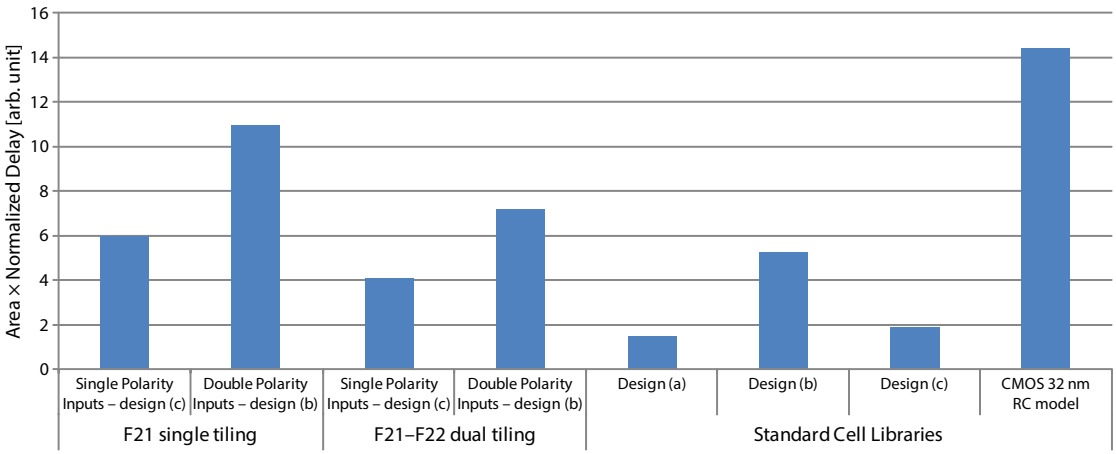


Figure 5.15 – Comparison of normalized ADP for logic gate F21 in single and dual tiling configuration with the Standard Cell libraries produced with design configurations (a), (b) and (c) of Section 5.3.1. Image adapted from [27].

As we can see, every configuration using CP CNTFETs is more efficient than the CMOS library, even considering normalized delays. This gives us a first confirmation of the efficacy of the regular fabrics implementation. As we expected, however, we observe a non negligible loss of performance for the regular tiling. For example, the design (c) standard cell library for CP CNTFETs performs about 2× more efficiently than the F21–F22 tiling in design (c) configuration in terms of normalized ADP, on average over a set of circuits mapped with the respective libraries.

5.5 Place and route process flow for regular fabric evaluation

After performing the general comparison among configurable gates presented in the previous section, we designed a more advanced process flow [116] to further evaluate these cells, including circuit place and route. This flow, shown conceptually in Figure 5.16 includes more efficient technology mapping and cell delays are characterized through simulations of each cell independently considering a range of output load capacitances. In particular, the characterization of the cells was implemented by automatically simulating each of the *sub-functions* implemented by each of the analyzed cells, F17, F21, F33 and ACT1, using Cadence SignalStorm® Library Characterizer (Version 5.20). Moreover, we considered more accurate gate areas, estimating the overhead due to power supply rails and input/output ports. Figure 5.16 shows an overview of the design flow we considered for this second evaluation phase. The initial libraries consist of the list of sub-functions implemented by cells F17, F21, F33 and ACT1. At this stage, 32 nm technology rules of the Stanford CNTFET transistor model [110] were employed to simulate cells F17, F21 and F33. In terms of area information for the library, we designed the basic cells considering the backend design rules available through the open source 45 nm Nangate library (Version 1.3) [117]. Layout techniques which are immune to misaligned CNTs [118] were incorporated while designing the cells. Synopsys Design

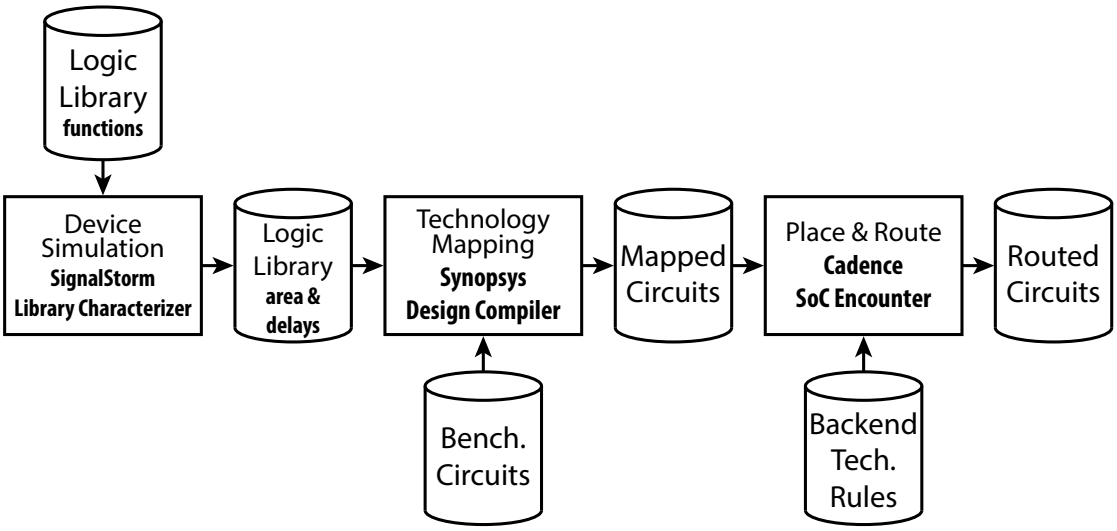


Figure 5.16 – Conceptual logic design process flow for the regular fabric evaluation up to place and route. A logic library of *sub-functions* is characterized for cell delay for a range load capacitances to create a logic library including area and delay information for each library element; subsequently, technology mapping is performed on a set of benchmark circuits and, finally, the circuits are placed and routed using a regular fabric of cells employing the 45 nm Nangate (v1.3) backend technology rules. Image adapted from [116].

Compiler® (B-2008.09-SP3) was used to map the *Register Transfer Level* (RTL) description of the benchmarks onto each target cell library. Cadence SoC Encounter® (Version 07.10) was used as the physical synthesis engine to study the impact of interconnect parasitics associated with the interconnect routing phase of the mapped netlist.

5.5.1 Evaluation results

In Figure 5.17 we report the delay estimation summary for each of the considered cells. Delays are reported as a sum of the delays of a set of benchmark circuits (mostly taken from the ISCAS'85 set) after the technology mapping design step and after the interconnect routing of the circuits. Note that all delays are normalized to the intrinsic technology delays, respectively 0.59 ps for CNTFETs and 3.00 ps [113] for 32 nm MOSFETs used to implement the ACT1 cell.

All three CP CNTFET cells showed better performance than the Actel ACT1 cell in terms of normalized delay. In particular, F2 demonstrated the best results, showing a normalized delay of 47% of the delay of the ACT1 cell after technology mapping and of 48.2% compared to ACT1 after interconnect routing. We attribute the slightly lower performance of the F33 cell to the higher complexity caused by the presence of two transmission gates in its schematic. As observed in [27], gates with two or more transmission gates (or, equivalently, XOR operators) cannot be used for technology mapping as efficiently as smaller gates such as F21. When comparing F17 and F21, finally, we observed that benchmarks can be mapped with a similar number of cells of types F17 or F21. This result is explained by the comparable set of *sub-*

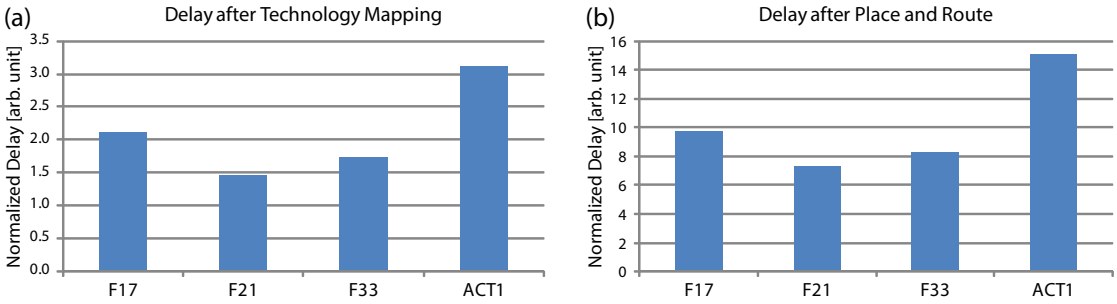


Figure 5.17 – Normalized delays after technology mapping and after routing for the CNTFET cells and ACT1. Image adapted from [116].

functions implemented by the two gates. When looking at delays, however, we see a distinct advantage of F21 over F17. This is mostly due to the lower average delay of cell F21 when compared to F17.

Table 5.6 reports the detailed results of the characterized benchmark circuits. Delays after technology mapping and after interconnect routing steps are provided. Finally, when looking at overall performance in terms of ADP for the CNTFET based cells, we observed performances of 5.9×, 7.7× and 6.6× respectively for F17, F21 and F33 over the Actel ACT1.

5.6 Perspectives for device/circuit co-optimization

As described in Chapter 1, the CP SiNWFET presented in this thesis unlocks new degrees of freedom in terms of device level functionality, that can be compared and appreciated with respect to conventional MOSFETs only when evaluated at larger logic gate and circuit levels. Moreover, as envisioned for modern scaled and *Beyond CMOS* technologies, closing the loop of device/circuit/architecture co-optimization can be highly beneficial to the overall definition and refinement of a technology. In the following, we will thus reference a number of works that were developed after the presented circuit benchmarking and in parallel with our fabrication process development.

5.6.1 Sea-of-Tiles as paradigm for physical regular fabric synthesis

Following our circuit level benchmarking, and after developing the physical SiNWFET fabrication process and characterization results described in Chapters 2 and 3, we take advantage of the simulated gate performance evaluations, and physical device design, to include device structure information for the physical synthesis of regular tiles. In particular, in [26], we envision a physical synthesis methodology based on *Sea-of-Tiles* (SoT), i.e., a layout design methodology where a regular array of small grain tiles, optimized for area and regularity, is repeated to create a die-scale fabric. In this work, the basic tile design is inspired by the fabricated device geometry, comprising sustaining S/D pillars and nanowire stacks in between.

	F1				F2				F3				ACT1			
	Delay		Cells		Delay		Cells		Delay		Cells		Delay		Cells	
Bench	Map	P&R	N.	Area	Map	P&R	N.	Area	Map	P&R	N.	Area	Map	P&R	N.	Area
add16	105.1	364.4	400	287.5	76.8	275.3	434	311.9	74.3	284.3	584	503.7	149.3	605.5	371	1697.9
add32	146.4	532.0	837	601.6	101.0	455.9	859	617.4	107.0	452.7	1012	872.8	212.4	968.6	655	2997.7
add64	175.4	838.1	1991	1430.9	133.9	667.5	1978	1421.6	141.7	968.4	2995	2583.1	250.5	1608.8	2122	9711.5
C1355	105.8	361.2	410	294.7	59.7	216.9	307	220.6	79.5	293.9	375	323.4	144.5	510.6	271	1240.3
C1908	131.4	538.6	579	416.1	86.3	450.8	522	375.2	112.1	392.4	378	326.0	189.9	823.1	253	1157.9
C2670	124.2	558.5	849	610.2	85.3	403.2	899	646.1	83.6	315.2	515	444.2	112.6	367.4	439	2009.1
C3540	173.7	744.1	1200	862.4	114.0	597.3	1213	871.8	140.1	541.8	1033	890.9	242.2	1595.0	726	3322.6
C5315	113.8	586.4	1938	1392.8	80.7	432.4	1960	1408.7	97.5	415.6	1204	1038.4	174.1	900.2	808	3697.9
C6288	435.4	1234.2	2284	1641.5	332.5	1175.8	2299	1652.3	434.0	1234.2	3117	2688.4	818.2	2406.0	2096	9592.6
C7552	122.5	623.4	2581	1855.0	78.4	471.0	2469	1774.5	98.5	547.7	1627	1403.3	165.9	821.4	1058	4842.0
dalu	83.0	443.1	749	538.3	56.1	401.5	788	566.3	75.8	498.3	691	596.0	118.9	759.7	477	2183.0
des	105.8	845.3	3366	2419.1	61.1	458.3	3699	2658.5	77.2	980.0	3197	2757.3	140.7	1401.2	2095	9588.0
i10	175.0	877.5	1883	1353.3	122.3	610.3	1957	1406.5	139.8	761.8	1816	1566.3	256.9	1457.2	1286	5885.5
i8	104.2	1158.8	3194	2295.5	68.9	637.8	3272	2351.6	76.3	577.5	747	644.3	127.0	818.6	578	2645.3
Total	2101	9705	22261	15999	1456	7254	22656	16283	1737	8263	19291	16638	3103	15043	13235	60571
%ACT1	67.7	64.5	168.2	26.4	46.9	48.2	171.2	26.9	56.0	54.9	145.8	27.5	100.0	100.0	100.0	100.0

Table 5.6 – Results after technology mapping and routing for a set of benchmark circuits. Delays are normalized to the intrinsic delays (0.59 ps for F17, F21, F33 and 3.00 ps for ACT1). Total values are also provided as percentage of the ACT1 results. Table adapted from [116].

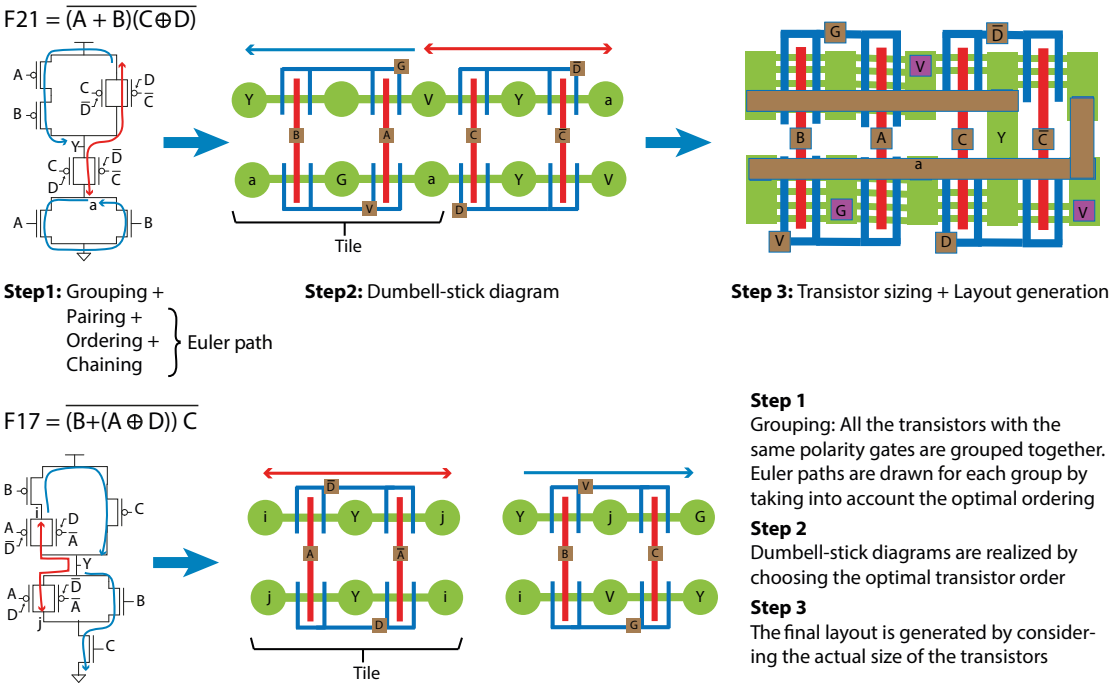


Figure 5.18 – Automatic steps for the generation of complex gate layout topologies. Examples are shown for gates F21 and F17. Image adapted from [26].

Moreover, the fabricated four-transistor structures shown in Figure 4.10 are evaluated as basic building block for the SoT, along with other similar two- to six-transistor tiles. Figure 5.18 shows the conceptual layout topology generation flow employed to design cells including physical layout information.

5.6.2 Further developments and outlook

In this section, we finally refer to a number of works from the literature that have been developed to further explore and analyze specific architectures and tools related to CP devices when employed to design digital circuits.

Cell complexity and power routing

Due to the polarization signal V_{pg} required for proper operation of a CP FET, these devices require a higher number of routing lines with respect to a conventional MOSFET, when embedded in logic circuits. Specifically, the PG has to be polarized either by a logic input or fixed to a supply voltage level. In [119], S. Bobba *et al.* consider intra-cell routing complexity aspects to present a further optimization of tile size for SoTs. Furthermore, in [120], C. Gasnier *et al.* implement a *boolean SATisfiability* (SAT)-based methodology in a tool (SATSoT) to automatically map a netlist of CP devices onto a SoT fabric, while minimizing wiring complexity. Finally, in [121], O. Zografos *et al.* propose an optimized power routing scheme that can be applied to our

CP FET technology and exploit the SATSoT tool to evaluate its efficacy with respect to standard ASIC interleaved horizontal power rails. In this work, the authors report a 26% improvement in speed with only a 17% of area increase trade-off when using CP FET devices with respect to a 22 nm conventional FinFET architecture, still considering the fact that unate logic gates are larger than their CMOS implementation due to the extra gate electrodes required for device polarization.

Architecture-specific advances

From an architecture point of view, after the work presented here on general purpose regular logic blocks, M. H. Ben Jamaa *et al.* [122] propose a further analysis of more complex logic blocks specifically targeted to FPGA implementations. Along these lines, other authors proposed further analyses of more complex configurable logic gates, such as a Universal Logic Module [123], and a universal medium-grain logic circuit including a latch for FPGA applications [124].

Logic minimization and technology mapping

Finally, in [125], L. Amarù *et al.* exploit the SATSoT methodology, together with *Biconditional Binary Decision Diagrams* (BBDDs), a newly developed canonical logic representation form, based on the biconditional operator (in Boolean logic, the XNOR operator), to create a dedicated design automation flow for CP devices. This flow takes advantage of the availability of efficient binate operators provided by CP devices to obtain a more efficient mapping of logic circuits onto a the physical SoT fabric as compared to a commercial synthesis tool flow. In this work, experimental results show that digital circuits based on CP FETs, using SiNW 22 nm technology, optimized by the proposed flow are 22% smaller and 42% faster than the same circuit synthesized by a commercial synthesis tool. Compared to FinFET 22 nm technology, the designed circuits have 2.9× smaller ADP.

5.7 Chapter summary and contributions

The increasing fabrication complexity at scaled technology nodes, and the need to limit device variability by producing more regular and predictable layouts (see, e.g., Figure 1.3), motivates the interest in regular architectures that provide designers with cost effective yet high performance platforms for circuit design. Due to their high expressivity with respect to conventional CMOS, their intrinsic symmetry, as well as the absence of doping wells and isolation structures, CP FETs are an ideal candidate for regular fabric architectures.

In this chapter, we evaluated a novel application of CP devices to produce configurable logic gates for regular fabric design. Moreover, the presented results encouraged the effort in developing a physical fabrication process flow for the SiNWFET devices presented in the

previous chapters. Here, simulation from the logic gate level to circuit place and route was carried out using a SPICE device model and a semi-custom circuit design tool flow:

Detailed static logic library evaluation

Gate-level simulation of a 46-gate static logic library was carried out using an adapted CP CNTFET compact model. The updated library containing delay information was used to perform technology mapping on a set of large circuit benchmarks, obtaining a 40% normalized ADP reduction with respect to their CMOS equivalents. Normalized results of technology mapping were then analyzed in order to select a number of cells, depending on their performance, as possible gates for regular fabric design.

Configurable gate regular fabric evaluation

For each configurable gate, results of technology mapping were compared with a conventional CMOS standard cell library, the Actel ACT1 block and 4-LUT. Gate evaluation showed that an improvement of 47% over the ACT1 block and of about 18× with respect to 4-LUT in terms of normalized ADP can be obtained with an And-Or-Inverter gate architecture. Standard cells, due to their intrinsically efficient full-custom design approach, maintained an advantage of about 2× of normalized ADP compared to the most efficient configurable gate.

Place and route evaluation of selected gates

Furthermore, we chose three medium grain-size configurable cells which we used to create a refined evaluation with respect to CMOS. After technology mapping, placement and routing was performed over regular layouts designed with each analyzed cell. CNTFET-based cells were compared with the Actel ACT1 cell. 32 nm technology rules were chosen for the transistors, while the interconnect was defined using 45 nm back-end design rules. Regular layout evaluation showed improvements of over 2× in terms of normalized delay for the CNTFET cells compared to ACT1. Area × normalized delay values for routed circuits showed performances about 8× better than that of the ACT1 cell.

In conclusion, although a number of technological issues still require to be addressed in order to produce defect-free, large scale integration of CP devices, the presented preliminary analyses of a physical design using these devices showed promising results, on one side motivating the interest in developing a reliable and scalable physical CP technology, on the other side stimulating further research on regular architectures, such as SoTs, Structured ASICs and FPGAs.

6 Device Optimization

In this chapter, we provide more detailed considerations for device optimization directions, focusing in particular on the characterization and improvement of S/D, nickel silicide device contacts. Specifically, S/D contact geometry and material quality are fundamental elements for proper operation of CP FET devices. Moreover, since silicides, and in particular nickel silicides, are currently employed in industrial devices to fabricate high performance, low-resistivity S/D and gate contacts, the methods presented in the following are not limited to use in CP or in general SB devices.

In Section 6.1, we provide some background on nickel silicides, with a focus on stoichiometric Ni_1Si_1 as the material of choice for our CP, SB-based devices. Furthermore, we briefly describe the most common NiSi deposition methods, highlighting some advantages and limitations motivating the need for a more efficient NiSi fabrication methodology. In Section 6.2, we present some material and electrical characterization results describing the S/D SB junctions employed in the fabricated devices. In Section 6.3, we present additional process steps we explored as a methodology to reduce contact resistance and improve channel access uniformity in our fabricated 3D stacked nanowire devices. In Section 6.4, we introduce a novel, wet chemical based methodology for Ni and NiSi conformal deposition on silicon, including some material characterization we performed on early fabricated samples. Finally, Section 6.5 concludes the chapter, summarizing the contributions provided by the presented research work.

6.1 Nickel silicide technology

Due to their interesting material properties, metal silicides, and in particular nickel silicides, have been extensively characterized, and have been used in numerous research and industrial devices [126, 127, 128, 129, 60]. In general, silicides are formed by solid-state reaction of a metal species with silicon, with the metal typically diffusing and creating an alloy when annealed at a certain temperature. Silicides can then provide very abrupt heterojunctions with the underlying silicon, showing very low interface states with respect to sputtered or

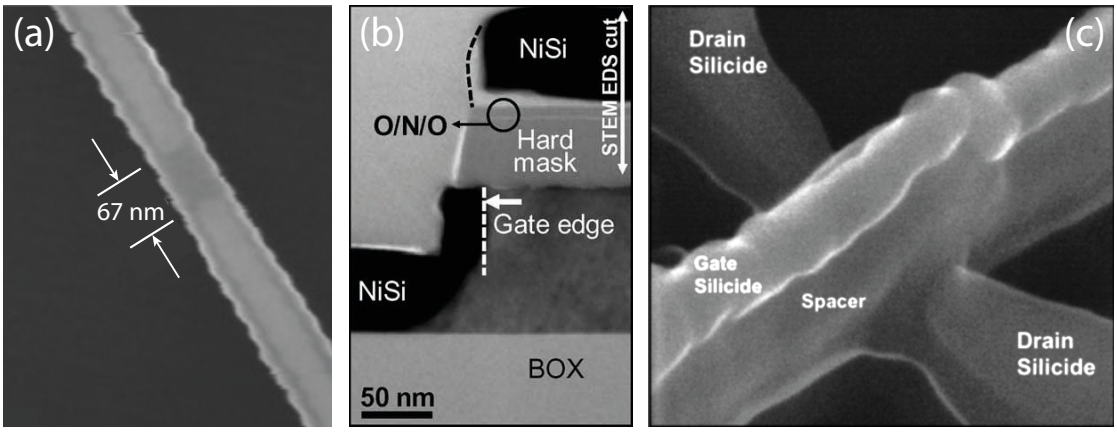


Figure 6.1 – (a) HRSEM view of a suspended SiNW with intruded nickel silicide contacts. Good control of the nickel diffusion in the nanowire is shown, and a barrier to barrier distance of ≈ 67 nm is obtained. Image adapted from [126]. (b) TEM cross section view of a complex FinFET structure with embedded SONOS stack, showing uniform nickel silicidation of S/D and gate contacts. Image adapted from [127]. (c) Tilted SEM view of a 60-nm gate length FinFET exploiting silicidation (in this case, using thin $CoSi_2$) for S/D and gate contact formation. Image adapted from [128].

evaporated metals on silicon. These properties make them a great class of materials for S/D contact resistance reduction in conventional FETs, where they have been successfully employed (examples in Figure 6.1). For the same reasons, silicides are a great choice for the fabrication of SB devices. In addition, the fact that a metal intrudes into the preexisting silicon structure, enables the fabrication of more complex geometries, including NWs with embedded junctions along the wire length (See Figure 6.1(a)). In [128], the authors show a FinFET device fabricated exploiting S/D and gate electrode silicidation (shown in Figure 6.1(c)). In this work NiSi was found to be the best among various Ni and Co based silicides due to its low stress effect when siliciding the deep gate electrode.

Moreover, Ni_xSi_y can be produced in various stable phases, by simple diffusion of Ni in a silicon volume by annealing at different temperatures. Figure 6.2 shows a plot of the main phases obtained by diffusion of Ni in bulk crystalline Si, depending on the annealing temperature [129]. More in detail, stoichiometric Ni_1Si_1 was chosen for a number of advantages it provides with respect to our process requirements:

- **Mid-gap work function:** NiSi provides quasi-midgap work function with respect to Si, thus providing optimal device symmetric behavior between n and p-type characteristics compared to other materials such as Pt–Si and Co–Si [130, 51].
- **Low silicon consumption:** contact silicidation involves diffusion of metallic nickel into the underlying crystalline Si structures (S/D and gate polysilicon layers), to create polycrystalline silicide regions. Due to the solid reaction occurring between nickel and silicon, swelling of the contact areas occurs. This swelling may lead to short circuit

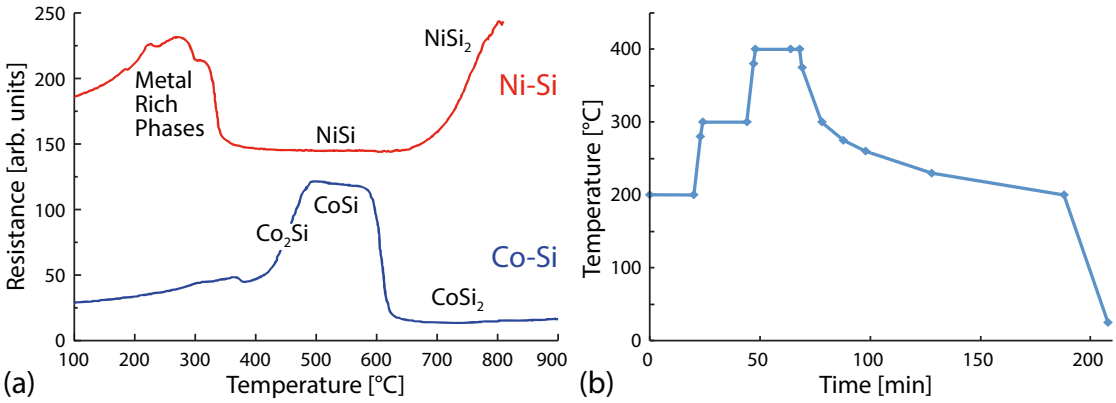


Figure 6.2 – (a) Comparison between Ni-Si and Co-Si alloy sheet resistance properties. After annealing, the measurements were performed on Co and Ni films deposited on polysilicon substrates in inert He atmosphere. Image adapted from [129]. (b) Temperature plot of the anneal used to produce the silicide at the device contacts in our process.

paths in the devices, or risk of damage of the delicate 3D structures. In the case of stoichiometric NiSi, low Si consumption, and consequently low volume expansion, is observed with respect to other silicides like $CoSi_2$ or $TiSi_2$ [129], and risk of structural damage is more contained.

- **Low temperature processing:** as shown in the plot in Figure 6.2(a), the Ni_1Si_1 phase is typically obtained in a wide annealing temperature window of 350 °C to 700 °C [129]. This enables the creation of a stable process with a low temperature budget for the silicidation annealing. Moreover, as mentioned in Section 2.3.2, a low temperature budget enhances compatibility with advanced gate stack technologies, such as high-κ dielectrics, as well as 3D monolithic integration.

- **Low sheet resistance:** among the different stable nickel silicide phases (Ni_2Si, Ni_1Si_1, $NiSi_2$) typically employed in industry, Ni_1Si_1 has the lowest sheet resistance. In particular, Ni_1Si_1 retains low resistance properties, also with respect to platinum and cobalt silicides, when patterned in small confined areas, such as nanowire or ribbon shapes [131, 132].

6.1.1 Nickel deposition methods

Several methods for nickel deposition are employed for the formation of nickel silicides in nanoelectronic devices. We briefly review the most common ones here, including sputtering, i.e., the method used in the device process presented in Chapter 3 and less developed methods including CVD and ALD. Existing limitations in terms of deposition quality and conformality will then serve as motivation for the development of a novel wet-based methodology, which will be further described in Section 6.4.

Physical vapor deposition

Physical Vapor Deposition (PVD) methodologies include metal evaporation and sputtering, and are so far the most common and reliable methodologies for Ni deposition. They are by now part of any conventional CMOS process, and provide high purity and good quality metal layers. In particular, evaporation consists of evaporating metallic Ni by heating a pure metal target. In this case, thanks to the low pressure environment, evaporated metal atoms deposit anisotropically on a substrate surface positioned at a distance, perpendicularly to the metal target. Similarly, in the case of sputtering, nickel atoms are extracted from a target using energetic gas ions and deposit on the substrate. In this case, the substrate is typically positioned closer to the metal target than in the evaporation case, thus enabling better deposition isotropy. Nonetheless, as shown in Figure 6.8(a), sputtering is not adequately conformal for good step coverage and isotropy to enter small cavities.

Chemical Vapor Deposition

This methodology consists of inserting vapor-phase chemical precursors of the desired materials in a chamber where the substrates are positioned. Various enhancements can be included, such as a low pressure environment (LPCVD) and plasma assisted processing (PECVD). In the case of nickel silicide, thermal stability of Ni precursors in gaseous form is a strong concern. In particular, shown methods for NiSi film deposition on silicon using CVD typically exploit intermediate materials, such as NiO, which are deposited at first and then reduced to obtain more pure Ni. As another example, in [133], nitrogen is used to enhance the precursor stability (Bis(N, N'-di-tert-butylacetamidinato)nickel(II) $\mathrm{Ni}\left(\mathrm{MeC}\left(\mathrm{N^tBu}\right)_2\right)_2$ in this case). The shown method is promising, as it provides good nickel silicide layers after annealing. However, agglomeration and layer degradation are observed at thicknesses below 10 nm.

Atomic Layer Deposition

For various materials, ALD is considered to be the most controlled deposition methodology, consisting of a chamber where a substrate is exposed to two or more material precursors in gas form one at a time, each of them providing a self-limiting reaction with the substrate surface. If stable precursors are employed, very good step coverage can be obtained ($> 100:1$) while the layer thickness can be fine-tuned by controlling the precursor cycle count. In the case of nickel and NiSi deposition on silicon, only a limited number of works are available in the literature, due to the unavailability of stable and reliable gaseous Ni precursors at the required deposition temperatures [134, 135].

6.2 Silicide characterization

The first step in our silicidation optimization was the characterization of the basic properties of the silicide produced by annealing in our SiNWFET fabrication process (see Chapter 3). To this end, in the next two sections, we describe material and electrical basic characterizations we performed to confirm the presence of the sought stoichiometric Ni_1Si_1 phase of nickel silicide.

6.2.1 Material characterization

Material analyses were performed using *Scanning TEM* (STEM) *High-Angle Annular Dark Field* (HAADF) imaging and *Energy-dispersive X-ray Spectroscopy* (EDX) component analyses, as well as XPS. Figure 6.3 presents the results of these measurements on a bulk Si surface. Ni deposition and annealing were performed following the same steps as described in Section 3.3.9. Specifically, the employed annealing temperature plot is shown in Figure 6.2(b). This annealing deliberately includes three 20-min long constant temperature phases, and was found to reliably produce good quality stoichiometric Ni_1Si_1. In Figure 6.3(a), a STEM-HAADF image is shown of a SEM/FIB prepared lamella across the fabricated NiSi layer. In this image, NiSi grain boundaries can be observed, forming a smooth junction to the underlying Si bulk. In (b), the same sample portion is analyzed using EDX and confirming the presence of Ni in the intruded layer. In (c) and (d), an X-ray diffraction spectrum and a depth profile produced using *X-ray Photoelectron Spectroscopy* (XPS) are shown, confirming that the observed layer is composed of stoichiometric Ni_1Si_1.

6.2.2 Schottky barrier height extraction

Due to the complex nature of the measurements, and the extensive literature describing the electrical properties of nickel silicides [136, 137, 138], in this work, we limited our analysis to the measurement of the device barrier heights at the S/D contacts.

Schottky barrier height extraction was performed on the device described in Section 2.4. Among different techniques used to measure the Schottky barrier height, we selected the activation energy approach, both for its accuracy and for its independence from the electrically active area. This second aspect makes it particularly well suited to study silicide-semiconductor interfaces. Assuming negligible parasitics resistances, the thermionic emission theory can be applied to the barrier extraction:

$$I = I_0 \left[\exp\left(\frac{qV}{\eta k_B T} \right) - 1 \right]$$

$$I_0 = A A_0 T^2 \exp\left(\frac{-q\Phi_B}{k_B T} \right),$$

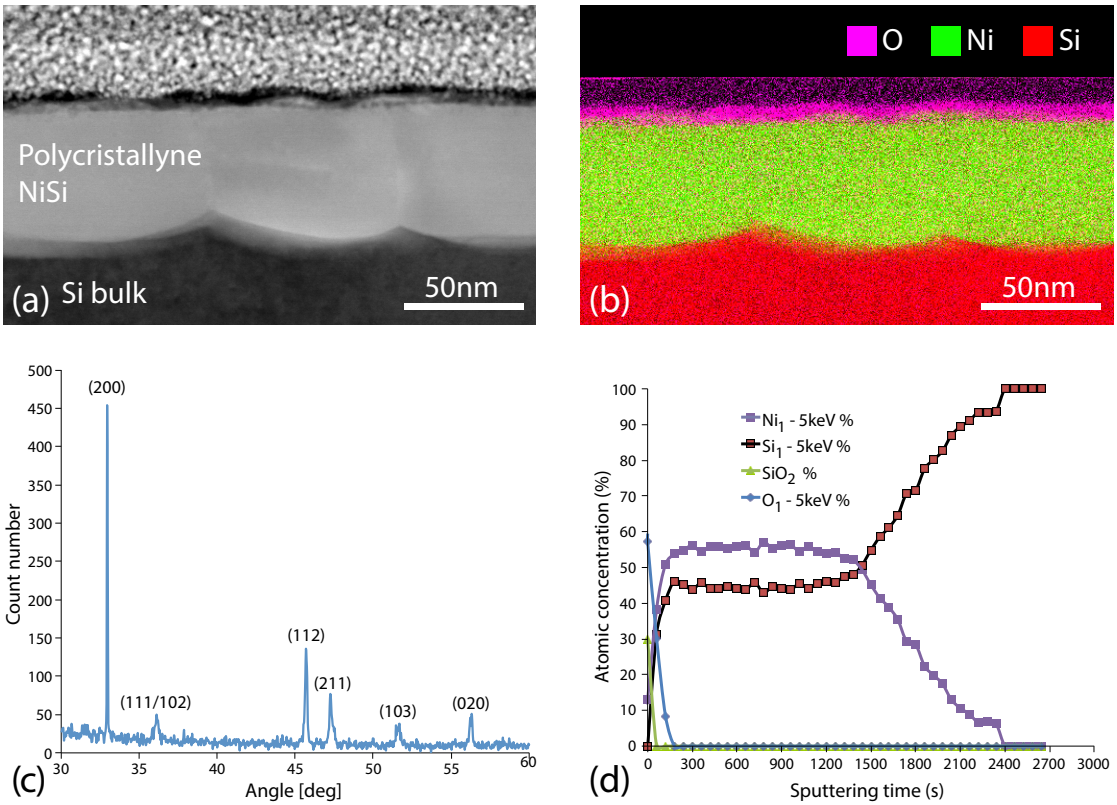


Figure 6.3 – (a) STEM-HAADF image of a stoichiometric polycrystalline Ni_1Si_1 layer produced using the process presented in Section 3.3.9. A continuous layer and grain boundaries can be observed. (b) STEM-EDX image of the same sample portion, showing Ni, Si and O species, and confirming the layer composition. (c) X-ray diffraction spectrum of a silicided sample in $\theta - 2\theta$ configuration. The different peaks represent diffraction from different NiSi crystallographic planes. (d) X-ray photoelectron spectroscopy curve showing the nature of the formed silicide, confirming $\approx 1/1$ Ni/Si atomic ratio.

where A is the contact area of the source to channel junction, A_0 the Richardson constant, q the elementary electron charge, ϕ_B^0 the effective Schottky barrier height, T the temperature, V the applied voltage across the Schottky junction, k_B the Boltzmann constant, and η the ideality factor.

In Figure 6.4, some of the experimental results of I_{ds} current measurements at different temperatures are shown. The linear decreasing slope of the Arrhenius plot in Figure 6.5, fitted within 5% error in experimental data with a measured ideality factor $\eta = 1.84$, indicates thermionic emission regime. Near-midgap Schottky ($q\Phi_{B_p}$) barrier height of 0.45 eV is observed, confirming that the type of silicide is compatible with the expected NiSi, whose barrier height value on p-Si is ~ 0.4 eV. This value is consistent both with literature and simulation results. In the inset of Figure 6.5, the energy-band diagram of metal to p-type semiconductor junction at thermal equilibrium is represented, showing the $q\Phi_{B_p}$ barrier.

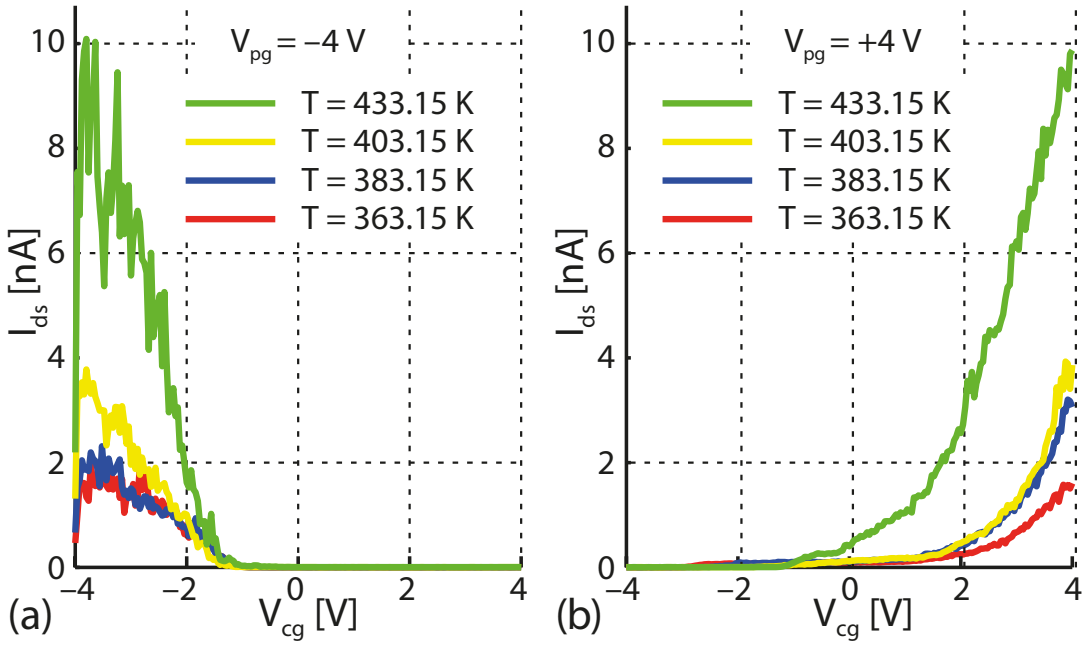


Figure 6.4 – A selection of the performed measurements at different temperatures, used for Schottky barrier height extraction, at V_{ds} = 100 mV and for (a) $V_{\mathrm{pg}} = -4$ V and (b) $V_{\mathrm{pg}} = 4$ V. Quasi-symmetric device operation can be observed.

6.3 S/D access resistance reduction

With the development of fabrication processes in the vertical dimension, such as FinFETs and the proposed stacked nanowire devices, new constraints arise in terms of fabrication. One of these is S/D contact access resistance. Specifically, in our device, high-aspect-ratio channel sustaining pillars determine the presence of increasing contact resistance to the lower nanowires due to the low doping of the Si bulk material. In the process we presented in Chapter 3, we employ a simple approach, where NiSi contacts are created at the top of the S/D pillar structures. Figure 6.6(a) shows a conceptual cross section view illustrating the NiSi S/D contact creation approach used in the device fabrication process. Specifically, removal of the gate SiO_2 layer is performed on the horizontal top surfaces of the S/D pillars. After SiO_2 removal, blanket Ni deposition is performed by sputtering. Figures 6.6(b) and (c) show the NiSi regions created by annealing. In Figure 6.6(b), a short anneal time, or a low amount of available metallic Ni at the surface, will produce a shallow NiSi intrusion, providing good control of the SB position along the topmost nanowire. This first case was employed as it provides good device performance, while not requiring additional process steps, and was successfully applied to obtain the electrical characterizations of Chapter 2.

When using this basic S/D silicidation technique, however, access resistance and junction position to the bottom wires will be very poor. At the same time, in Figure 6.6(c), increasing the available source nickel, will enable the creation of deeper NiSi regions. In this case, while access resistance to the bottom nanowires will be reduced, higher risk of damage of the top

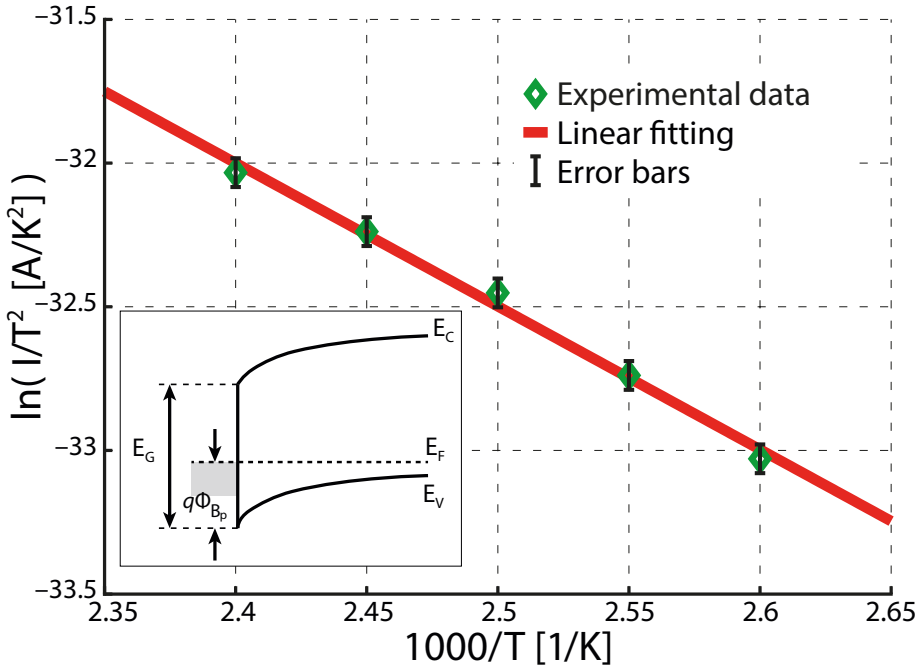


Figure 6.5 – Arrhenius plot extracted from measurements, some of which are represented in Figure 6.4. The linear decreasing slope of the plot, fitted within 5% error in experimental data, indicates thermionic emission regime. $q\Phi_{B_p}$ barrier height of 0.45 eV is observed, confirming that the type of Silicide is compatible with the expected NiSi, whose barrier height value on p-Si is ~0.4 eV. In the inset, energy-band diagram of metal on p-type semiconductor at thermal equilibrium, showing the $q\Phi_{B_p}$ barrier

wires and high variability in the barrier position along the top wires will be encountered.

Therefore, after determining that the fabricated NiSi S/D contacts match the required material and electrical properties for correct polarity control in the implemented devices, in this section we consider a fabrication level improvement that can enable better S/D barrier control and reduced contact access resistance. The proposed improvement is conceptually shown in Figure 6.7 and consists of producing deep vertical cavities (or, possibly, complete Si removal) in the S/D pillar structures. In this case (Figure 6.7(a)), however, a strongly conformal metallic Ni deposition is required. Thanks to this improved geometry, after silicidation annealing, NiSi can be formed in the whole pillar height (Figure 6.7(b)), and even control of the Schottky junctions along all the nanowire stack can be obtained.

Figure 6.8 shows a number of SEM and SEM/FIB cross section micrographs of various performed steps. In Figure 6.8(a), preliminary evaluation of Ni step coverage via sputtering deposition is shown. The image is taken after ≈ 50 nm Ni deposition and 30 s a 450 °C on a bulk Si wafer with vertical 200 nm cavities created by dry anisotropic etching. Poor step coverage can be observed, with a low amount of NiSi forming at the bottom of the cavity.

At the same time, in Figure 6.8(b), we show etched pillar structures with round cavities of

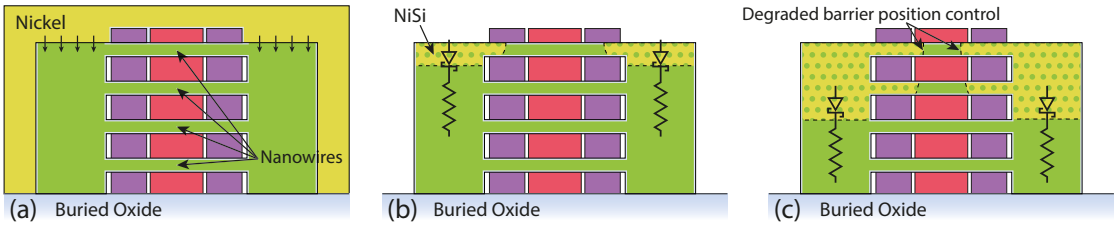


Figure 6.6 – Conceptual cross-section views of the stacked SiNW CP device structure after Ni deposition and annealing steps. (a) The device as fabricated with the process flow described in Chapter 3 just after Ni deposition. In (b) and (c), views after annealing and removal of excess metallic Ni: depending on the silicidation time or metallic Ni availability, the NiSi front proceeds in the Si structure (in green) to form uneven depth SBs along the SiNWs, with the bottom wires experiencing high access resistance.

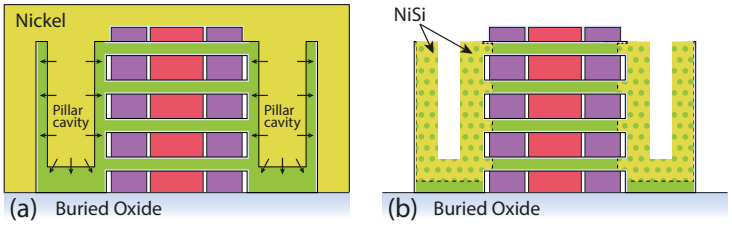


Figure 6.7 – Conceptual cross-section views of the stacked SiNW CP device structure after Ni deposition and annealing steps when using hollowed pillars. (a) Conformal Ni as deposited on hollowed-pillar devices. (b) The device after silicidation and excess Ni removal. In this case, finer control of the SB position along the wires is possible, as well as reduction or elimination of high access resistance to the lower wires in the stack.

about 200 nm in diameter. In Figure 6.8(c), these fabricated nanowire stacks with hollow pillars are shown after Ni coating. A SEM/FIB cross section view of a pillar is then presented in Figure 6.8(d), showing large accumulation of metallic Ni at the top edges of the pillar cavity. A small amount of Ni is observed to deposit at the bottom and on the cavity sides. However, improved step coverage is a critical feature required to guarantee the efficacy of the presented methodology, especially in the effort to scale down pillar dimensions.

Motivated by the more and more stringent requirements arising from the shown device process, and more in general by state-of-the-art scaled DSD as well as SB FETs, we will present in the following section a novel wet nickel silicide deposition technique aiming to overcome these limitations.

6.4 Wet conformal NiSi deposition

As we have described in the previous sections, fine control of the contact silicidation is a fundamental requirement to obtain a stable device fabrication process and low performance variability. In particular, good step coverage and deposited layer purity are fundamental

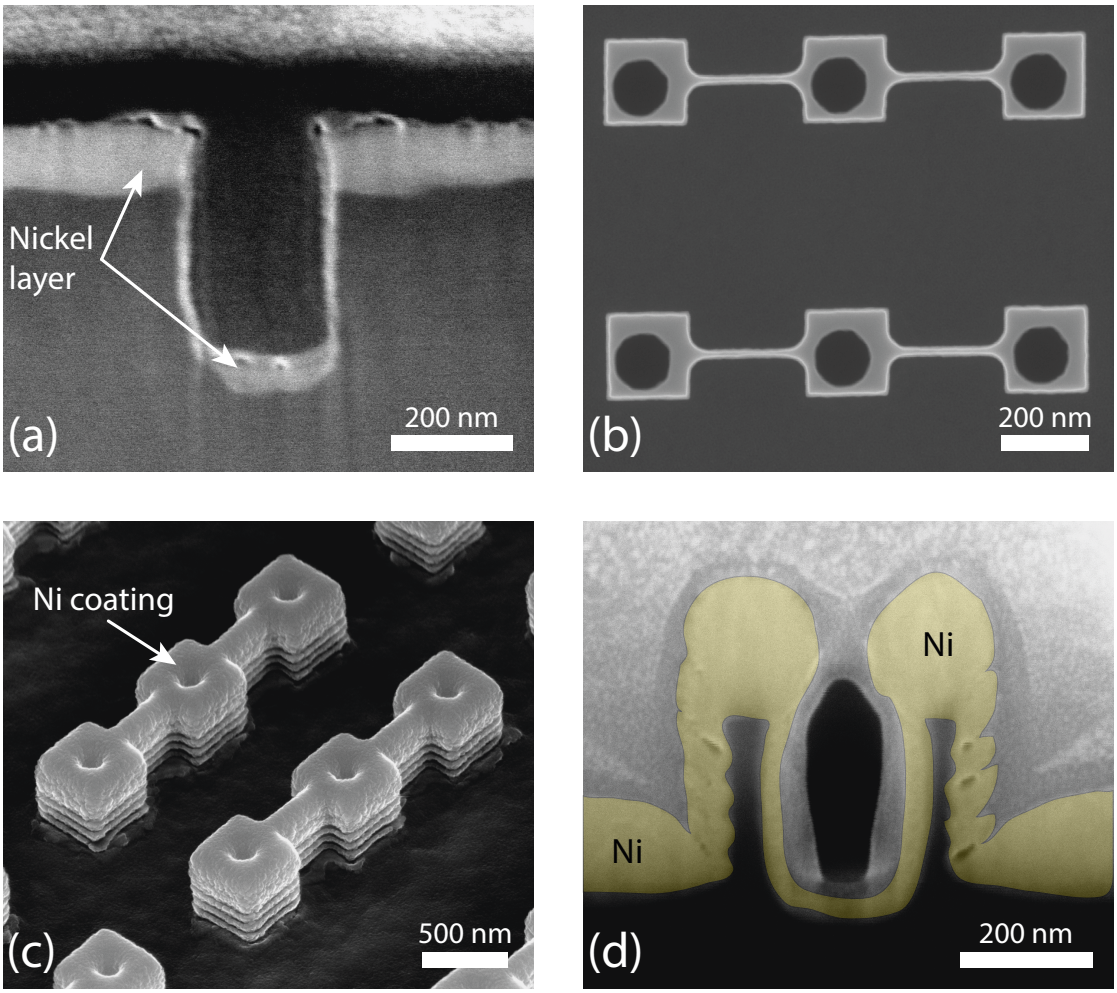


Figure 6.8 – Contact resistance reduction by pillar hollowing. (a) Test cavity SEM/FIB cross section on a bulk Si substrate. After deposition of ≈ 45 nm of metallic Ni by sputtering, followed by 30 s a 450 °C, formed NiSi is shown to cover the cavity bottom, but sidewalls are not well coated. (b) SEM top view of fabricated nanowire stacks with hollowed pillars. A small misalignment between the pillars and the cavities is caused by imperfect alignment during hole definition by e-beam lithography. (c) Tilted and rotated SEM view of hollowed pillars after Ni coating via sputtering of metallic Ni. (d) SEM/FIB cross section of a hollowed pillar after Ni coating, showing a thick accumulation of Ni on the horizontal surfaces at the pillar wall edges.

qualities to enable integration in state-of-the-art devices for CMOS and emerging devices at scales below 100 nm, especially in presence of highly packed, 3D structures. In this section, we describe a novel method for low temperature, conformal nickel or nickel silicide deposition. This method is under development, and is based on a chemical precursor reaction with a silicon surface. Specifically, wet environment reaction offers the potential to produce homogeneous and highly conformal deposition on complex 3D silicon device structures. As such, it is directly applicable to our device fabrication methodology, where it could be

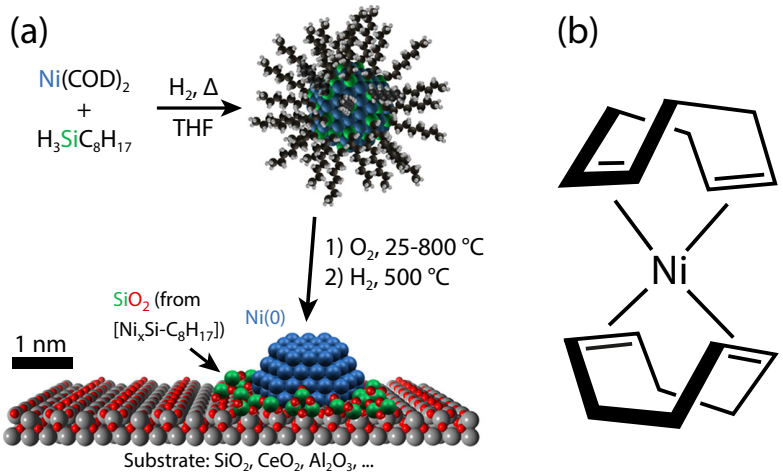


Figure 6.9 – (a) Conceptual view of the synthesis of nickel silicide colloids and their conversion into a substrate for use as Ni catalysts. Image adapted from [140]. In (b), Bis(1,5-cyclooctadiene)nickel(0) [$Ni(COD)_2$], an employed precursor for nickel silicide wet deposition.

employed to produce full NiSi S/D pillars, or used to coat the interior of hollowed sustaining pillars, to obtain low resistance contacts with a low temperature budget.

This project was carried out as a collaboration in the context of the ChemNiSi project[1] with the ETH Laboratory of Inorganic Chemistry [34]. The contribution presented here mainly includes SEM/TEM and EDX analyses performed at the Interdisciplinary center for Electron Microscopy (CIME) at EPFL [139], as well as a diode process flow (see Section 6.4.4) allowing to obtain junction electrical properties for the deposited material layers.

6.4.1 Nickel silicide deposition in wet chemical conditions

Due to the difficulties encountered in gas-phase reaction of nickel containing organometallic precursors, we propose the use of an alternative method based on a wet environment for deposition of conformal, high quality Ni and NiSi layers. This novel methodology takes advantage of recent developments in nickel silicide colloid production as catalyst for fuel gas reforming applications. In particular, in [140], the authors show the production of stable nickel silicide nanoparticles, which can then be exposed to oxygen and then reduced to metallic Ni particles by treatment with H_2. The nanoparticles are produced in mild conditions, i.e., low temperature (55–65 °C) and non aggressive *Tetrahydrofuran* (THF) solvent bath. This method is particularly attractive as it can potentially enable production of nickel silicide layers with high conformality and very low temperature budget. Here, we describe preliminary results of *High Resolution Transmission Electron Microscope* (HRTEM) and STEM-EDX analyses we performed on wet processed samples, showing that nickel silicide layers can be deposited on Si substrates, although further developments are required to reduce carbon and oxygen

[1] Project ChemNiSi: A Chemical Route towards Conformal Low-Temperature Silicide Deposition. Supported by Swiss National Science Foundation grant CR22I2_152955.

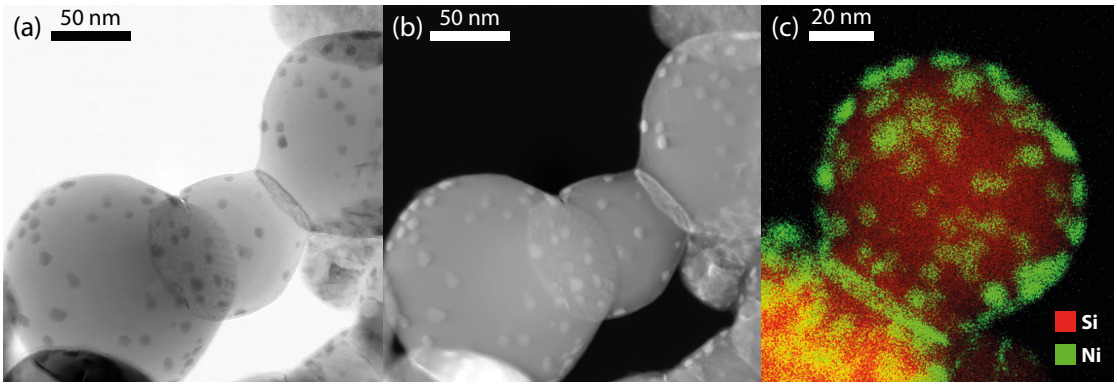


Figure 6.10 – Silicon nanoparticles after wet treatment with $Ni(COD)_2$and silane. (a) STEM-BF and (b) STEM-HAADF views highlighting the presence of ≈ 5 nm dots distributed on the surface of the Si particles. (c) STEM-EDX close-up of a silicon particle, showing the presence of nickel as dots on its surface.

contamination in these layers.

6.4.2 Ni deposition on Si nanoparticles

Due to its manipulation simplicity, Si nanopowder was employed in early tests in order to evaluate the potential of the wet deposition methodology. In particular, nanopowder provides high exposed surface-to-volume ratios, and can be collected and compacted for easy *X-ray Absorption Spectroscopy* (XAS) and *Fourier Transform InfraRed* (FTIR) analyses, providing information on material type (e.g., the presence of a specific silicide phase) and surface reactivity of the material, respectively. In this case, TEM analyses provide information on layer formation and distribution of atoms on the particle surface. Figure 6.10, for example, shows STEM-*Bright Field* (BF)(a) and HAADF(b) of Si nanoparticles after reaction in a high pressure glass reactor. STEM-EDX close-up is shown in Figure 6.10(c), confirming the presence of Ni containing particles of ≈ 5 nm in diameter on the surface of the Si nanoparticles.

6.4.3 Deposition on Si bulk substrate

In subsequent tests, Si (100) substrates were employed to evaluate Ni deposition on a flat surface. Specifically, due to the nature of the surface, with a single crystal plane exposed for reaction, Si nanoparticles are not sufficiently reliable as model for nanoelectronic processing. In Figure 6.11, HRTEM (a), STEM-HAADF (b) and STEM-EDX analyses are shown on a cross section of a first one-pot synthesis test of nickel silicide on a Si die. In this test, the Si die was treated with HF for native SiO_2 removal prior to the layer deposition.

After this first test, various reaction conditions were tested, targeting a stable formation of a continuous and uniform layer of Ni and Si containing material. In general, pyramid formation was observed, indicating a good cleaning of the starting Si surface, but no uniform thin layer of

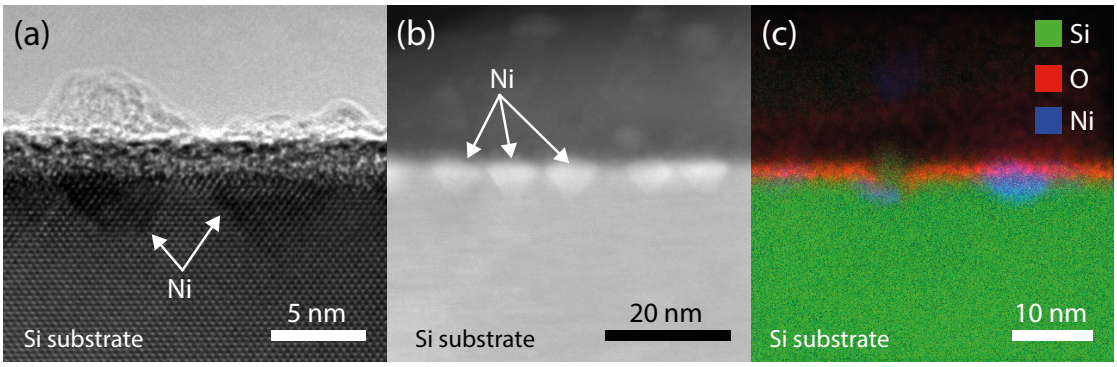


Figure 6.11 – First one-pot synthesis using $Ni(COD)_2$ on silicon (100) die surface. (a) HRTEM view of a tripod method prepared surface cross-section, showing intrusion of Ni into the Si bulk in the form of pyramids, with interfaces along the (111) Si planes. (b) STEM-HAADF view highlighting Ni intrusions and (c) STEM-EDX view showing a Si oxide layer on the Si bulk surface and confirming Ni presence below Si surface.

silicide was yet created on the Si surface. Figure 6.12 shows a sample prepared using the tripod polishing method [141] produced using a more optimized deposition process. In particular, Figure 6.12(a) shows a STEM-HAADF close-up of the deposited layer, showing a uniform, amorphous deposited layer on top of the underlying Si (100) bulk surface. In (b), a STEM-EDX overview of the sample is shown, highlighting the continuous Ni containing layer on both the top and bottom surfaces of the sample sandwich. In (c), a close-up of the formed layer and (d) EDX based atom percent line profile of the species contained in the layer across the Si bulk to deposited layer interface, showing a ≈ 1.5 Si/Ni atom presence in the layer.

Precursor selection

Various Ni organometallic precursors have been employed in the literature for Ni or Ni/Si synthesis. In this work, besides $Ni(COD)_2$, other precursors are being investigated with the objective, e.g., to reduce carbon contamination. This effect is strongly desired, as contamination is one of the limiting factors in alternative Ni and NiSi deposition methods with respect to the high purity Ni obtained using PVD methods. In this context, a number of variables are being explored that can influence the behavior of the selected precursor molecules, including deposition temperature, presence of a post-treatment step and surface properties and materials.

6.4.4 Diode process flow

For the sake of completeness, as a last element for the analysis of the produced NiSi layers on bulk substrates, we describe a dedicated process flow enabling quick electrical testing of deposited layers. This process can be applied to characterize any rectifying junction, in combination with the activation method fitting presented earlier in this chapter. Due to

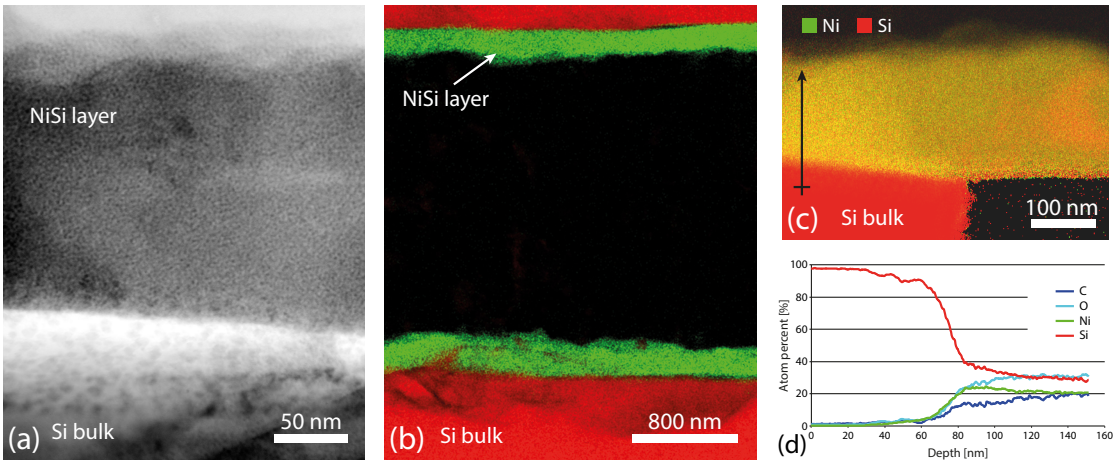


Figure 6.12 – Optimized one-pot synthesis on bulk (100) Si. (a) STEM-EDX close-up of the formed layer, showing good uniformity and no visible layer porosity. Intruded silicide pyramids can be observed as small particles on the Si surface due to the slight sample tilt in the bottom portion of the image. (b) STEM-EDX overview of the tripod-polished sample sandwich, highlighting the continuous Ni containing layer over the Si bulk surfaces. (c) Atom percent calibrated EDX view of the layer, and (d) atom percent line profile along the arrow shown in (c), showing no interface oxide between bulk Si and deposited layer, as well as a ≈ 1.5 Si/Ni ratio in the deposited material. C and O contamination is also shown.

the status of the layer deposition process, this diode process has not been employed yet for electrical measurements, although it is operational and has been tested from a fabrication point of view.

Figure 6.13 shows a conceptual overview of the main fabrication steps of this process. The complete runcard is presented in Table 6.1. In this process, a double side polished, low p-doped substrate is coated with 100 nm L.S. silicon nitride, and ring shaped openings are created by contact photolithography (Figure 6.13(a)) and dry etching. Subsequently, (b) a degenerate boron doping is produced by diffusion of boron from *BoroSilicate Glass* (BSG) through annealing at 1250 °C for 60 min in N_2 atmosphere. After annealing, a second circular opening is created in the nitride layer, leaving an intrinsic Si surface area available for SB contact formation. This is done by deposition of the material under test (Ni or NiSi) (b) and (c). Finally, metal contacts are created on the doped and non-doped Si regions to create ring ohmic contacts as well as to contact the SB created with NiSi, allowing the SB properties to be electrically characterized by means of a standard probe station.

6.5 Chapter summary and contributions

In the transition from conventional bulk MOSFETs to devices growing in the vertical dimension, perfect control of S/D contact formation becomes of paramount importance to guarantee integrity and functionality at highly-scaled technology nodes. In this chapter, we considered

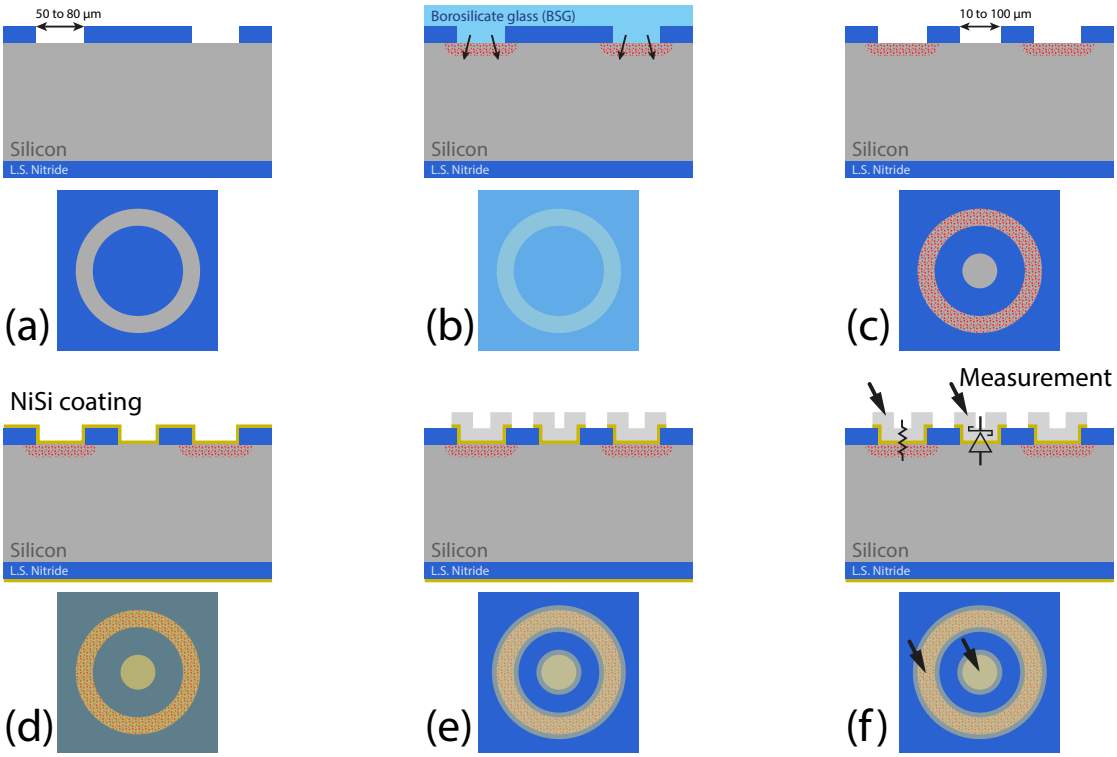


Figure 6.13 – Conceptual overview of process flow described in Table 6.1. for each step, cross section (top) and layout (bottom) views are shown. (a) A double side polished substrate is coated with 100 nm of low stress SiN, and ring patterns of various sizes (50–80 nm width) are created via optical lithography. (b) BSG is deposited and annealing is performed to produce degenerate boron doping areas below the open ring pattern, and create ohmic contacts at the end of the process. (c) BSG is removed by BHF plus dry etching and a second optical lithography step is performed to create center openings in the SiN coating (10–100 nm in size) for SB contact formation. (d) The desired Ni or NiSi deposition under test is performed, and a contact Ni–Si is created at the center opening. (e) Contact creation via metal deposition and lift-off or etching is performed on the ring and center circular patterns. (f) Measurements can be performed using a probe station, isolating the behavior of the center Schottky diode.

elements contributing to the evaluation and improvement of nickel silicide based S/D contact formation, with a focus on material deposition conformality and reduction of access resistance in the case of stacked nanowire devices. In particular, we considered three steps:

Device S/D contact characterization

As a first step, we characterized fabricated devices in terms of material and electrical properties, by producing TEM-based cross section analyses of annealed NiSi layers, and confirming their composition with XPS to guarantee creation of the sought stoichiometric Ni_1Si_1 silicide phase. Further, we performed basic electrical measurements to confirm good symmetry between the source and drain barrier heights, as required for proper functionality of our CP device

paradigm.

S/D access resistance reduction

Due to the peculiar 3D structure of the device presented in Chapter 2, large and uneven access resistances to the lower nanowires in the device stacks are expected to reduce device performance and increase variability. In this second section, we consider the addition of further process steps to the fabrication process presented in Chapter 3 that may reduce this variability by hollowing the device S/D pillar structures and filling the created cavities with Ni before silicidation anneal. Nonetheless, limitations in the pillar silicidation quality were observed due to the imperfect step coverage provided by conventional sputtering PVD of nickel.

Wet chemical NiSi deposition

Motivated by the need of a conformal nickel silicide creation for use in complex 3D device structures as the proposed one, in this last part of the chapter, we introduce a novel NiSi deposition approach. This approach is being developed in a collaboration with organometallic chemistry researchers [34] and consists of a wet chemical path to produce NiSi layers on silicon substrates in mild conditions, i.e., low temperature, non aggressive environment. Preliminary results, mostly in terms of HRTEM and STEM-EDX material analyses, show great potential in terms of material control and quality.

Finally, this chapter highlights the need for high quality nickel silicidation of S/D contacts, proposing fabrication level and material deposition level techniques to increase contact quality. Due to the wide interest and applications of nickel silicides in current scaled devices, including DSD (for ohmic contact creation) as well as SB devices, the described methods provide promising research directions with a large application base.

Table 6.1 – Process runcard for the fabrication of ring SB diodes. Substrate: double side polished, low p-doping Si wafer. Z*n* in the Equipment column refers to the location of the equipment in the CMI cleanroom [83].

Step	Process	Equipment	Recipe
Phase 1	**L.S. Nitride Deposition**		
1.1	RCA cleaning	Z3/RCA wet bench	Full RCA standard recipe
1.2	Low stress nitride	Z3/Nitride LPCVD	100 nm L.S. SiN recipe
Phase 2	**Mask 1 Optical Lithography – Ohmic contact definition**		
2.1	PDMS priming	Z1/PDMS priming oven	Standard recipe
2.2	Photoresist coating	Z1/Rite Track	AZ92xx 2 μm recipe
2.3	Optical lithography exposure	Z6/MA6 mask aligner	9 s exposure at 10 mW/cm^2
2.4	Photoresist development	Z1/Rite Track	AZ92xx 2 μm recipe
Phase 3	**L.S. Nitride Etching**		
3.1	L.S. Nitride Etching	Z2/SPTS APS dielectric etcher	Si3N4 recipe for 40 s
3.2	Photoresist removal	Z6/Remover wet bench	Standard recipe (15 min dirty bath + 15 min clean bath + rinsing)
3.3	Organic residues removal	Z1/Tepla oxygen plasma	1 min recipe
Phase 4	**BSG doping for ohmic contact formation**		
4.1	Native oxide removal	Z1/BHF wet bench	Clean bath for 30 s
4.2	RCA cleaning	Z3/RCA wet bench	Full RCA standard recipe
4.3	BSG deposition	Z3/BSG LPCVD	800 nm Borosilicate glass recipe

Continued on the next page...

Table 6.1 – Table continued from previous page.

Step	Process	Equipment	Recipe
4.4	Annaling	Z3/Centrotherm densification furnace	60 min recipe at 1250 °C in N_2
4.5	BSG excess removal	Z1/BHF wet bench	Contaminated bath for 60 min
4.6	Back side L.S. Nitride Etching	Z2/SPTS APS dielectric etcher	Si3N4 recipe for 40 s
Phase 5	**Mask 2 Optical Lithography – Schottky contact definition**		
5.1	PDMS priming	Z1/PDMS priming oven	Standard recipe
5.2	Photoresist coating	Z1/Rite Track	AZ92xx 2 μm recipe
5.3	Optical lithography exposure	Z6/MA6 mask aligner	9 s exposure at 10 mW/cm^2
5.4	Photoresist development	Z1/Rite Track	AZ92xx 2 μm recipe
Phase 6	**L.S. Nitride Etching and wafer dicing**		
6.1	L.S. Nitride Etching	Z2/SPTS APS dielectric etcher	Si3N4 recipe for 40 s
6.2	Photoresist removal	Z6/Remover wet bench	Standard recipe (15 min dirty bath + 15 min clean bath + rinsing)
6.3	Organic residues removal	Z1/Tepla oxygen plasma	1 min recipe
6.4	Wafer dicing	Hand tool or dicing saw	2 cm× 1 cm dies
Phase 7	**Chemical NiSi deposition**		
7.1	Native oxide removal	Chemical wet bench	Clean BHF bath for 30 s
7.2	Nickel Silicide deposition	Various recipes	
7.3	Annealing	Annealing as required for material testing	

Continued on the next page...

Table 6.1 – Table continued from previous page.

Step	Process	Equipment	Recipe
Phase 8	**Mask 3 – Metal contact definition**		
8.1	PDMS priming	Z1/PDMS priming oven	Standard recipe
2.2	Photoresist coating	Z6/EVG150	AZ1512HS on LOR 1 + 1 μm recipe
2.3	Optical lithography exposure	Z5/MLA150 prototyping direct writer	Dose: 130 mJ/cm^2
2.4	Photoresist development	Z6/EVG150	AZ1512HS on LOR 1 + 1 μm development recipe
6.4	Native oxide removal	Z1/BHF wet bench	Contaminated bath for 30 s
2.3	Substrate rinsing and drying	Z2/Plade Ox wet bench	FFR + Trickle tank DI water baths, standard recipe

7 Conclusions and outlook

Today more than ever, semiconductor device academic and industrial research plays a pivotal role in the development of technologies that fit in every moment of our lives. Be it for entertainment, industrial, research or medical applications, the push for more performance at a lower cost is enormous, not only in terms of mere economic gain, but also thanks to the fascinating variety of applications and synergies that nano device technology can unlock.

In the introduction of this thesis, we presented the concepts of *More-than-Moore* and *Beyond CMOS* development directions, describing how mainstream digital circuit design is becoming more and more multi-faceted, thanks to the integration and diversification of nanoscale devices.

In this exciting turmoil, a plethora of novel devices are being developed at various levels, some being fully mature for production scale-up, some being only at a partial theoretical understanding stage. In the presented research, we chose to undertake a middle way, i.e., we developed and experimentally demonstrated a novel device concept, the CP SiNW based FET, that provides high performance and new functionality while being implementable using CMOS compatible fabrication steps. The peculiar interest in this device is multifaceted, in that it combines both *More-than-Moore* and *Beyond CMOS* aspects, which arise from a smart and combined use of existing technological elements.

Furthermore, in this thesis work, we deliberately wanted to expand the understanding of this device concept through different design levels, from elements of device and material physics, to system-level circuit benchmarking. Specifically, we can resume the objectives at large of this thesis work at two levels:

- **Device proof of concept and benchmarking:** following preliminary research motivating the interest in demonstrating functional and high performance devices exhibiting in-field electrostatic polarity control, our first objective was to create a high quality proof of concept device. Conceptually following this demonstration, scale up to reconfigurable efficient logic gates and circuit level benchmarking were undertaken to

create a comprehensive understanding of the potential of this technology with respect to mainstream CMOS.

- **Device to circuit co-optimization methodology:** we consider the applied research methodology, including device level design, in conjunction with circuit and system level performance analyses, as a benchmark for future *Beyond CMOS* device research. Specifically, we believe the case of CP devices can clearly demonstrate that a system aware device design can produce more net benefits than considering only pure device level performance.

7.1 Summary of contributions

In Chapter 1, we introduced the context of transistor device technology innovation, giving an overview in terms of current and future challenges in the academic and industrial world. After this introduction, we preferred to present chapters that are as much as possible self-contained, each describing a different benchmarking level of SiNW-based CP devices. Specifically, each chapter included a description of the associated state-of-the-art and the peculiar challenges arising from the considered sub-topic, i.e., device performance, fabrication process, logic gate and system levels. In the following, we will briefly review and discuss the most relevant findings arising at each level.

7.1.1 Device fabrication and characterization

The first part of the presented work focused on the stacked SiNW CP device. Device capability to change polarity in the expected bias voltage ranges and exhibit high performance characteristics in both n-type and p-type modes stands as primary objective of this first part of the work.

Due to their intrinsic reconfigurability, CP devices require special attention in terms of characterization. In Chapter 2, we experimentally confirmed correct device programmability to n-type and p-type through ad-hoc I_{d}–V_{cg} measurements, performed for various V_{pg} configurations. We showed, for the first time, that our device is able to operate as p-type for a null V_{pg} bias, and as n-type for a positive V_{pg}, i.e., the required operating regions to enable multi-level logic synthesis are met.

Furthermore, a set of I_{d}–V_{cg} and I_{d}–V_{d} measurements showed that our device can attain record performance of measured SS steepness of respectively $\approx 60\,\mathrm{mV/dec}$ for n-type and $\approx 63\,\mathrm{mV/dec}$ for p-type polarizations. At the same time, observed $I_{\mathrm{on}}/I_{\mathrm{off}}$ performance reaches 10^8 for strong p-type polarization and 3.5×10^7 for strong n-type polarization all in the same physical device, showing that both typical high performance and low-power device features can be obtained with an electrostatically polarized SB-FET device.

In terms of fabrication, in Chapter 3 we described a novel, fully CMOS-compatible process

flow, exploiting top-down fabricated SiNWs. Single devices and large device arrays were fabricated, showing that VLSI can be realized in a straightforward manner using the presented process. In particular, a density of around 3×10^8 transistors/cm^2 was demonstrated using our early process flow, developed applying relaxed design rules that are roughly compatible with a 90 nm CMOS technology node. Furthermore, critical process steps, including S/D contact creation via silicidation annealing, enabled the creation of a low temperature budget process, which is extremely useful in view of the use of high-κ dielectric materials as well as compatibility with 3D monolithic integration.

7.1.2 Reconfigurable logic gate demonstration

Device scale-up to logic gate level has been a second central objective of the presented research. After the demonstration and evaluation at single device level, in Chapter 4, we focus on this second challenge. Specifically, we see this step as crucial for closing the co-optimization loop between the single fabricated device and the more abstract system-level simulations.

In addressing the challenge of creating fabricated circuits using CP devices, we first focused on two-transistor circuits, which were measured by externally connecting two single devices. With this methodology, we demonstrated the first fully functional, cascadable two-transistor XOR logic gate. The consequences of this result are fundamental, as it demonstrates that CP devices can indeed implement more compact logic circuits than conventional CMOS, effectively stepping into the *Beyond CMOS* pathway.

After the demonstration of reconfigurable two-transistor gates, we further concentrated on the fabrication, showing the sought process scale-up to multiple-transistor cells. In this step, we demonstrated four-transistor pre-connected fabricated logic gates, producing measured input-output characteristics, and showing the first four-transistor gate with the ability to calculate either NAND or XOR logic functions without changing its internal transistor connectivity. This gate adds to the previous findings in that it provides full-swing output, and can be employed in larger circuits to implement any complex logic function.

7.1.3 Device and logic gate simulations

As described in Chapters 2 and 4, device level and mixed-mode logic gate level simulations were performed at various stages using TCAD simulation software. We separate this section from the previous two as simulation results have been used mainly as support for the benchmarking and prediction of performance at both single device and small circuit level. Nonetheless, due to the conservative approach employed in our fabrication process, i.e., the use of quite relaxed device dimensions as well as material choice, simulations have proven very useful in predicting performance for scaled device dimensions and use of advanced materials, e.g., high-κ dielectrics. Specifically, in Chapter 2, we showed that in a scaled and more optimized device, we can expect a strong reduction in V_{th}, while maintaining good

symmetry between n-type and p-type I_d–V_{cg} characteristics, further confirming the interest in future applications of this device concept.

At logic gate level, mixed mode simulations served as benchmark to evaluate the response of logic gates to increasing load capacitance. Finally, due to our probe-station based measurement constraints, circuits had to be fabricated with large contact pads. Simulations have then proven to be a useful tool to go beyond practical measurement limitations, to roughly evaluate performance in the case of small scale circuits.

7.1.4 System level benchmarking

As described in the introduction of this chapter, the presented research work was developed not only with the objective to produce high performance devices to address current MOSFET technology challenges. In particular, we believe that the potential of a device including new capabilities has to be evaluated from a larger point of view than with simple device level characterization. Along these lines, the system level benchmarking described in Chapter 5 attempted to evaluate, through the characterization of cell libraries all the way to circuit place and route, the intrinsic advantage enabled by polarity control with respect to conventional CMOS technology.

The analysis carried on at this level included the setup of a semi-custom logic circuit design tool flow. This flow enabled the fast characterization of a predefined cell library, from which basic parameters such as delay and area occupation were extracted. After the creation of test libraries, place and route of a set of benchmark logic circuits was performed to create comparisons of different library types and target architecture. Due to the variety of potential applications of CP devices, aspects of gate granularity and design regularity were considered. In this respect, very encouraging results were shown in comparison to conventional CMOS, including a 40% normalized ADP reduction with respect to CMOS for the analyzed standard cell libraries, and improvements of over 2× in terms of normalized delay for regular CP-based cells compared to the commercial configurable ACT1 logic block.

In general, as in any novel technology simulation based analysis, device model and setup assumptions pose a limit to the accuracy and generality of the extracted results. For this reason, the results presented in Chapter 4, were normalized to intrinsic technology parameters such as delay and transistor sizing. This aspect was considered very important in the effort to produce as fair as possible comparisons among different technologies, and their corresponding design methodologies. Specifically, we expect the estimated efficiency in terms of area and delay with respect to CMOS to be mainly a result of the intrinsic polarity control degree of freedom, and as such the presented results can be expanded without loss of generality to any technology exhibiting the polarity control feature.

7.1.5 Technology refinements

As mentioned throughout this thesis, at such early stage of device process development, numerous opportunities for improvement can be envisioned, in terms of use of materials, device structure and technology enhancers, e.g., strain technology. At the same time, our device is based on extensively studied technologies, such as conventional unipolar SB-FETs, SiNWs and nickel silicidation. For this reason, in the last research chapter of the thesis (Chapter 6), we wanted to privilege more undeveloped research directions, i.e., evaluating a strategy for S/D contact resistance reduction by pillar hollowing, and trying to advance nickel silicide deposition technology via a novel wet chemical method. At present, these methods are not fully stable, nevertheless, we believe that pushing the limits of our fabrication facilities can bring great benefits in terms of vision for future developments and research directions.

7.2 Outlook and future research

Many interrelated elements have to balance out for a technology to proceed to maturity and become stable for large scale applications. In the context of *More-than-Moore* technologies, at first stance, it is fundamental to optimize the trade-off between the advantages of a new technology and its cost, in terms of fabrication complexity and resilience to variability, i.e., process stability.

For the presented CP device, we tried to devise a fabrication process that is intrinsically VLSI compatible, being based on a simple top-down nanowire fabrication methodology. Moreover, the presented fabrication process does not require a high temperature budget, nor complex doping profiles, which are some of the known limiting factors for further state-of-the-art MOSFET scaling. In addition to a scalable process, our device provides the degree of freedom of polarity control, which guarantees an advantage with respect to conventional CMOS, without exploiting exotic materials or non stable complex phenomena to operate.

Finally, our device can directly benefit from the application of conventional technology enhancers such as high-κ dielectrics and strain, as well as advanced lithography techniques, and expect these additions to further highlight the interest in the presented technology.

7.2.1 Catalyst for extended research directions

In terms of added value, the presented device design and process flow, as well as the promising measurement results, have stimulated further research in different directions, from the single device to logic circuit optimization methodologies. Some of these subsequent results have been mentioned in Chapter 1 and included a novel device concept with three independent gates [142] that extends polarity control with the addition of threshold voltage selection for high-performance to low-power reconfigurability. This same device can be optimized to exhibit weak impact ionization and attain record-steep *SS* [22]. At the same time, device

variability analysis specific to the presented SiNW CP device was carried out in [143], as well as a fault modeling study [144].

Moving up to architecture and circuit level research, extensions in the direction of circuit-device co-optimization are presented in [119, 26] as well as applications of CP devices for Structured ASICs [145] and FPGA architectures [146, 147].

Finally, due to the intrinsic capability of controlled polarity devices to express binate logic functions (e.g., XOR) in a compact way, a novel logic minimization paradigm, together with its mathematical framework was developed in [125, 96, 103], further underlining the usefulness of new synergy between device technologies and circuit design techniques.

7.2.2 Future research directions

Numerous directions, in terms of further characterization and optimization of the presented device have been mentioned throughout this thesis. From a research point of view, scaling up of the fabrication process to produce larger circuits, i.e., 10 to 100 devices, is definitely a priority, as it can provide very important results in terms of performance and functionality analysis. In our experience, however, this scale up will require not only the setup of a *Back End Of the Line* (BEOL) process flow, but also a stabilization of the presented process flow to minimize device-to-device variability. Specifically, due to the high 3D topography of the pillar-sustained SiNW stacks, fine tuned planarization and contact creation steps may be particularly challenging in an university cleanroom environment.

At single device level, besides the previously mentioned application of advanced technology enhancers already in use in state-of-the-art industrial technologies, further development of the S/D and Gate contacts material choice can bring great benefits in terms of control of the operating voltage ranges and device performance.

Finally, we would like to mention more visionary developments, including co-integration with memory or sensing elements, as well as 3D monolithic integration, which can be enabled by the presented CMOS-compatible, low temperature budget process.

Finally, the use of promising novel channel materials, such as bottom-up fabricated nanowires or carbon nanotubes, as well as graphene, could possibly bring an even stronger advantage to the CP device concept. At a small scale, these materials have already shown extremely promising characteristics and performance, although a sufficiently reliable scale-up methodology for very large scale integration has not been found so far.

The latest advances in electronic nano device technology are characterized by a stronger then ever push for more performance and more functional diversification. *Beyond CMOS*

as well as *More-than-Moore* roadmaps have been envisioned to expand the current limits of conventional CMOS technology. In this thesis, we proposed a device to system co-optimization methodology, integrating device elements both in the *More-than-Moore* and *Beyond CMOS* realms. Furthermore, we believe the presented techniques, and empirical results, confirm that a physics-to-architecture holistic approach can highlight hidden synergies between different design meta-levels, ultimately guiding faster advances in optimization and device performance.

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Michele De Marchi

nanoelectronics engineer

+41 (0) 78 638 89 60 rte de chavannes 68, 1007 lausanne, switzerland michele.demarchi.85@gmail.com

Strengths

- **Strong nanofabrication, characterization and circuit design tool expertise.**
- **Hands-on problem solving and teamwork on interdisciplinary projects.**
- **Willing to travel. Fluent English.**

Education

École Polytechnique Fédérale de Lausanne **Sep 2015**
Degree: PhD in Microtechnology and Nanoelectronics engineering

University of Udine (Italy) **March 2010**
Degree: Master in Nanoelectronics Engineering
Grade: 110/110 Summa Cum Laude

Scuola Superiore - University of Udine **March 2010**
Degree: Diploma of Advanced Studies
Grade: 110/110 Summa Cum Laude

University of Udine **Oct 2008**
Degree: Bachelor in Electrical Engineering
Grade: 110/110 Summa Cum Laude

AFS Intercultural Programs Returnee **2002/03**
Year abroad program, spent at Maine-Endwell High School, Endwell, NY (www.afs.org)

Skills

Technical

Cleanroom
Strong expertise on all standard nanofabrication techniques (3000 h): full runcard development, e-beam lithography (300 h), photolithography, dry/wet etching, ALD, CMP, evaporation, sputtering.

Microscopy
SEM (300 h), TEM (150 h), HR-TEM, STEM, EDX, AFM, FIB.

Computer

Languages
C/C++ (OOP, data structures), Java, Pascal, Basic, Assembler, Unix scripting.

HW Design
VHDL, Verilog, Spice, Cadence Skill.

Tools
MATLAB, Mathematica, Cadence design suite (500 h), TCAD (200 h), e-beam lithography and proximity correction (150 h).

Publishing
Adobe Illustrator (advanced, 400 h), Latex (advanced user), Blender (80 h), Gimp, AutoCAD, AfterEffects.

Languages

Italian	*native*
English	*bilingual* · C2
French	*advanced* · C1

Publications

- **Polarity controlled transistor** Patent US 20130313524
- **Author** of 15 technical papers on international journals and conferences. Presented as speaker at conferences such as IEDM, ICCAD, Nanoarch.

Work Experience

EPFL **Nov 2010 – Sep 2015**
Research Engineer and Doctoral Candidate

- Beyond-CMOS device fabrication. Developed and implemented a full 3D transistor fabrication process based on top-down silicon nanowires.
- Fabricated nanowire-based FET devices featuring in-field polarity control, showing high device density and state-of-the-art transistor figures of merit.
- Demonstrated the first fully functional two-transistor XOR logic gate. Demonstrated 4-transistor AND, OR and XOR logic gates with the same technology.

University of Udine (Italy) and EPFL
Research Intern **Sep 2009 – Oct 2010**

- Modeling and performance analysis through simulation of Carbon Nanotube (CNT) based ambipolar FETs.
- Implemented full logic design flow with these devices to evaluate circuit performance after place & route.

Awards

- **Work on controlled polarity devices** featured in *Science* magazine 340, 1414 (2013).
- **IEDM** 2012 paper featured in pre-conference press kit.
- **Nanoarch** 2012 Best paper award.
- **Nanoarch** 2010 Best paper award (first author).
- **Graduate of the year** best graduate of Electrical Engineering, University of Udine (2010).

Volunteer work

Student representative (elected): engineering department, University of Udine (2009-2010).

Co-founder (2009) of NeoAteneo student association which won university-wide student elections with overall 60% of votes in the 16'000-student University of Udine.

Treasurer of the EPFL Mountain club (2010-2015). Managed a 20'000 CHF annual budget.

Interests

Rock climbing and mountaineering reached level 7c (5.12d) in 4 years. Coached a number of beginners into improving technical skills and safety techniques.

Long distance bicycling led various team and solo 1000 km trips (e.g., Lausanne – Barcelona).

Graphic design designed a new corporate identity of the LSI university lab (lsi.epfl.ch) and designed the logo of the EPFL mountain club (clubmontagne.epfl.ch).

List of publications

1. M. De Marchi, M. H. Ben Jamaa and G. De Micheli. **Regular Fabric Design with Ambipolar CNTFETs for FPGA and Structured ASIC Applications**. In *Nanoscale Architectures (NANOARCH), 2010 IEEE/ACM International Symposium on*, pages 65–70, 2010. *Best paper award. With presentation.*

2. M. De Marchi, S. Bobba, M. H. Ben Jamaa and G. De Micheli. **Synthesis of Regular Computational Fabrics with Ambipolar CNTFET Technology.** In *Electronics, Circuits, and Systems (ICECS), 17th IEEE International Conference on*, pages 70–73, 2010. *With presentation.*

3. M. H. Ben Jamaa, P.-E. Gaillardon, S. Frégonèse and M. De Marchi, G. De Micheli, T. Zimmer, I. O'Connor and F. Clermidy. **FPGA Design with Double-Gate Carbon Nanotube Transistors**, *in Electrochemical Society Transactions (ECS)*, vol. 34, num. 1, p. 1005-1010, 2011.

4. D. Sacchetto, M. De Marchi, G. De Micheli and Y. Leblebici. **Alternative Design Methodologies for the Next Generation Logic Switch**. In *International Conference on Computer-Aided Design (ICCAD)*, San Jose, California, USA, 2011. *Invited paper. Presentation given by M. De Marchi.*

5. S. Bobba, P.-E. Gaillardon, J. Zhang, M. De Marchi, D. Sacchetto, Y. Leblebici. and G. De Micheli. **Process/Design Co-optimization of Regular Logic Tiles for Double-Gate Silicon Nanowire Transistors**, In *Nanoscale Architectures (NANOARCH), 2012 IEEE/ACM International Symposium on*, pages 55–60, July 2012. *Best paper award.*

6. S. Bobba, M. De Marchi, Y. Leblebici and G. De Micheli. **Physical Synthesis onto a Sea-of-Tiles with Double-Gate Silicon Nanowire Transistors.** In *Proceedings of the 49th Annual Design Automation Conference (DAC)*, pages 42–47, 2012.

7. M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici and G. De Micheli. **Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs.** In *Electron Devices Meeting (IEDM), IEEE International*, pages 1–4, 2012. *With presentation.*

8. P.-E. Gaillardon, L. Amarù, S. Bobba, M. De Marchi, D. Sacchetto, Y. Leblebici and G. De Micheli. **Vertically Stacked Double Gate Nanowires FETs with Controllable Polarity:**

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