A Surface Potential and Current Model for Polarity-Controllable Silicon Nanowire FETs

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***Abstract*—Silicon nanowire FET (SiNWFET) with dynamic polarity control has been experimentally demonstrated and has shown large potential in circuit applications. To fully explore its circuit-level opportunities, a physics-based compact model of the polarity-controllable SiNWFET is required. Therefore, in this paper, we extend the solution for conventional SiNWFETs to polarity-controllable SiNWFETs. By solving the current continuity equation, the potential distribution and drain current is obtained. The model shows good agreement with TCAD simulation. It can be used as the core to develop the complete compact model for polarity-controllable SiNWFETs.**

I. Introduction

As a potential candidate for continuous scaling down, silicon nanowire FET (SiNWFET) provides excellent electrostatic control with its gate-all-around structure [1]. By exploiting metallic contacts, SiNWFET can be fabricated with a dopant-free process, but exhibits ambipolar characteristics. However, by exploiting an additional gate to electrostatically trim the Schottky barriers at source and drain, the polarity of the SiNWFET can be reconfigured dynamically [2]–[5]. Polarity-controllable devices provide new opportunities for circuit design thanks to their enhanced functionalities, and has been extensively studied on fabrication, circuit and architecture design [6]–[9]. Neverthless, as the bridge between technology and design, a physics-based compact model for polarity-controllable SiNWFETs is not yet available.

There are many works on the compact modeling of doped source/drain or Schottky-barrier SiNWFETs [10], [11]. Compared to these devices, polarity-controllable SiNWFETs introduce additional gated regions between source and drain. Therefore, it is necessary to model the potentials of the different regions in order to predict the device characteristics. To address this discontinuity of the gate voltages along the channel, a simple assumption of constant capacitances is proposed in [12] for dual-gate carbon nanotube FET, which has the similar multiple-gate structure as polarity-controllable SiNWFETs. However, the ballistic solution for carbon nanotube FET is difficult to be applied to SiNWFET.

In this paper, we fill the gap in modeling polarity-controllable SiNWFETs by presenting a long-channel model for this device based on the solution of conventional SiNWFETs. Starting from Poisson's equation, the potential distribution and the drain current are obtained by solving the current continuity between Schottky-barrier contacts and the drift-diffusion of both carriers in the channel. The model shows good agreements with TCAD simulation. Advanced physical effects can be easily embedded into the model to develop a complete compact model for polarity-controllable SiNWFETs.

II. Polarity-Controllable SiNWFET Structure

A polarity-controllable SiNWFET is shown in Fig. 1a. Metallic source and drain allow the conduction of both electrons and holes within an intrinsic silicon nanowire channel. The device has three gated regions. The two external gates are connected together to modulate the Schottky barriers. Since this gate determines the type of carriers through the Schottky barriers, it is named *P*olarity *G*ate (PG). For the convenience in the following analysis, the PG close to the source is called PG_S, while the one close to the drain is called PG_D. The gate in the middle of the channel induces a potential barrier to control the current, and is named *C*ontrol *G*ate (CG).

The device has been experimentally demonstrated in [4] by a vertically-stacked nanowire structure. The SEM picture and measured characteristics are reproduced in Fig. 1b. The double-gate SiNWFET shows promising performance in terms of near-ideal subthreshold slope and high I_{on}/I_{off} ratio.

The band diagrams in different configurations are shown in Fig. 1c. In *n*-type configuration, a positive voltage is applied on PG and electrons may tunnel through the thin Schottky barrier at source into the channel. At *on* state, CG is polarized to allow electrons flowing through the channel easily without barriers in the channel. In contrast, at *off* state, the potential barrier induced by CG prevents the current from flowing. The *p*-type operation is similar, but relies on holes tunneling through the barrier at drain.

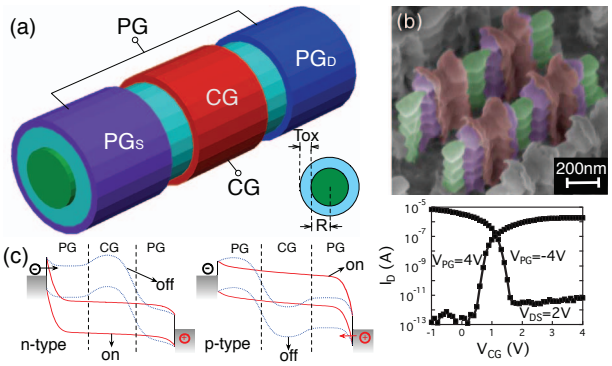

Fig. 1. (a) Conceptual sketch of a double-gate SiNWFET, (b) SEM picture and measured characteristics of the double-gate SiNWFET [4]. (c) Band diagrams of *on*-state and *off*-states in *n*-type and *p*-type configurations.

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III. Model Derivation

In this section, the surface potential is obtained for both *n*-type and *p*-type operations. Then, the expression of drain current is derived at Schottky barriers and in the silicon nanowire channel. By solving the current continuity, the potential distribution and the drain current are finally obtained.

A. Surface Potential Model

In order to capture the transport of both electrons and holes in the model, 1-D Poisson's equation in an intrinsic silicon nanowire channel is written as:

$$\frac{d^2\phi}{dr^2}+\frac{1}{r}\frac{d\phi}{dr}=\frac{qn_{\rm i}}{\varepsilon_{\rm s}}\left(e^{\frac{q(\phi-V_{\rm n})}{kT}}-e^{\frac{q(V_{\rm p}-\phi)}{kT}}\right) \tag{1}$$

where $V_{\rm n}$ and $V_{\rm p}$ are the quasi-Fermi potential of electrons and holes, respectively. Symbols used in this work all refer to their common meanings as in [13] unless specified otherwise.

However, it is difficult to obtain an accurate and explicit solution to (1). Therefore, a piecewise solution is first obtained by only considering electrons or holes according to the bias $V_{\rm geff}=V_G-V_{\rm FB}$ [10]:

$$\phi=\begin{cases}\phi_{\rm n}=V_{\rm n}+\frac{kT}{q}\ln\left(\frac{-8B_{\rm n}}{\delta(1+B_{\rm n}r^2)^2}\right) & \text{if } V_{\rm geff}\gg\frac{V_{\rm p}+V_{\rm n}}{2}\\ \phi_{\rm p}=V_{\rm p}-\frac{kT}{q}\ln\left(\frac{-8B_{\rm p}}{\delta(1+B_{\rm p}r^2)^2}\right) & \text{if } V_{\rm geff}\ll\frac{V_{\rm p}+V_{\rm n}}{2}\end{cases} \tag{2}$$

Then, a single-piece approximation of ϕ is written as:

$$\phi=\sigma_1\cdot\phi_{\rm n}+\sigma_2\cdot\phi_{\rm p} \tag{3}$$

where $\sigma_1=(1+\tanh\alpha)/2$, $\sigma_2=(1-\tanh\alpha)/2$, $\delta=q^2n_{\rm i}/kT\varepsilon_{\rm s}$ and $\alpha=q(2V_{\rm geff}-V_{\rm n}-V_{\rm p})/2kT$. $B_{\rm n}$ and $B_{\rm p}$ are determined by the boundary condition from Gauss's law:

$$C_{\rm ox}(V_{\rm geff}-\phi_{s,0})=\varepsilon_{\rm s}\frac{d\phi}{dr}\Big|_{r=R}=Q_{\rm n}-Q_{\rm p} \tag{4}$$

By substituting (3) into (4), we approximately derived:

$$\frac{q(V_{\rm geff}-V_{\rm n}-\Delta V)}{kT}=\frac{q}{kT}\frac{Q_{\rm n}}{C_{\rm ox}}+\ln\frac{Q_{\rm n}}{Q_0}+\ln\frac{Q_{\rm n}+Q_0}{Q_0} \tag{5a}$$

$$\frac{q(V_{\rm p}-V_{\rm geff}-\Delta V)}{kT}=\frac{q}{kT}\frac{Q_{\rm p}}{C_{\rm ox}}+\ln\frac{Q_{\rm p}}{Q_0}+\ln\frac{Q_{\rm p}+Q_0}{Q_0} \tag{5b}$$

where $Q_0=4(kT/q)(\varepsilon_s/R)$, and $\Delta V=(kT/q)\ln(8/\delta R^2)$. Once the carrier density $Q_{\rm n}$ and $Q_{\rm p}$ are solved from (5), the long-channel surface potential $\phi_{s,0}$ can be obtained by substituting $B_{\rm n(p)}=-Q_{\rm n(p)}/[(Q_{\rm n(p)}+Q_0)R^2]$ into (3).

Eqs. (5) are accurate for calculating the potential and the density of majority carriers, which are important for solving the current. Therefore, (5) is used as a good approximation for following calculations. In addition, we derive a refined expression to calculate the density of minority carriers:

$$\begin{aligned}Q_{\rm n,min}&\approx\frac{qn_{\rm i}}{R}\int_0^R r{\rm e}^{\frac{q(\phi_{\rm p}-V_{\rm n})}{kT}}\,{\rm d}r\\&=\frac{qn_{\rm i}\delta}{48B_{\rm p}^2R}{\rm e}^{\frac{q(V_{\rm p}-V_{\rm n})}{kT}}\left[1-(1+B_{\rm p}R^2)^3\right]\end{aligned} \tag{6}$$

A unified solution valid for all bias conditions is thus given:

$$Q_{\rm n}=\sigma_1\cdot Q_{\rm n,maj}+\sigma_2\cdot Q_{\rm n,min} \tag{7}$$

where $Q_{\rm n,maj}$ is the result of (5a). $Q_{\rm p}$ can be similarly derived.

For Schottky-barrier devices, the potential distribution near the contacts is required in addition to $\phi_{s,0}$ to calculate the tunneling through the Schottky barriers. Therefore, we apply a quasi-2-D solution of the surface potential [11]:

$$\begin{aligned}\phi_s&=\phi_{s,0}+\Delta\phi_{s,S}(y)+\Delta\phi_{s,D}(y)\\ \Delta\phi_{s,S}(y)&=(V_{\rm bi}+V_{\rm S}-\phi_{s,0})\frac{\sinh((L-y)/\lambda)}{\sinh(L/\lambda)}\\ \Delta\phi_{s,D}(y)&=(V_{\rm bi}+V_{\rm D}-\phi_{s,0})\frac{\sinh(y/\lambda)}{\sinh(L/\lambda)}\end{aligned} \tag{8}$$

in which the characteristic length $\lambda=\sqrt{\varepsilon_{\rm s}R/2C_{\rm ox}}$, L is the length of each gate, and $V_{\rm bi}=\chi+E_g/2q-\Phi_m$ is the built-in potential with Φ_m the workfunction of Schottky contacts.

B. Drain Current Model

According to the derived potential model, the potential along the channel can be obtained when the quasi-Fermi potentials $V_{\rm p}$ and $V_{\rm n}$ are known. To obtain $V_{\rm p}$ and $V_{\rm n}$ at each region, the current continuity condition needs to be solved.

For simplicity, here we only discuss the $V_{\rm DS}\geq 0$ case. The results when $V_{\rm DS}<0$ is the same as the device is symmetric. Considering that the quasi-Fermi potentials mostly drop at the contacts and the interfaces between gated regions, we also assume $V_{\rm p}$ and $V_{\rm n}$ keep constant within each region. They are labeled as $V_{\rm n(p),PG_S}$, $V_{\rm n(p),CG}$, and $V_{\rm n(p),PG_D}$. The surface potentials at each region are also labeled as $\phi_{\rm PG_S}$, $\phi_{\rm CG}$, and $\phi_{\rm PG_D}$, respectively.

First we consider the Schottky contacts. Electrons may tunnel through the Schottky barrier from source and holes may tunnel from drain based on the bias conditions. To avoid the complexity of calculating the tunneling probability, the effective Schottky barrier heights $\Phi_{\rm SBeff}$ is applied based on the assumption of the tunneling distance d_t [12], [14]. The tunneling probability is assumed to be unity if the barrier is thinner than d_t and zero otherwise. By solving (8) at $y=d_t$ and $y=L-d_t$, the effective Schottky barriers are given by

$$\Phi_{\rm SBeff,n}=\Phi_{\rm SB,n}-(\phi_{\rm PG_S}-V_{\rm bi}-V_{\rm S})(1-e^{-d_t/\lambda}) \tag{9a}$$

$$\Phi_{\rm SBeff,p}=\Phi_{\rm SB,p}-(V_{\rm bi}+V_{\rm D}-\phi_{\rm PG_D})(1-e^{-d_t/\lambda}) \tag{9b}$$

where $\Phi_{\rm SB,n}=\Phi_m-\chi$ and $\Phi_{\rm SB,p}=\chi+E_g/q-\Phi_m$ are the Schottky barrier heights for electrons and holes, respectively.

In addition to the Schottky barriers, CG may also induce a potential barrier in the middle of the channel as shown in Fig. 1c. This barrier Φ_C can be expressed as:

$$\Phi_{\rm C,n}=(V_{\rm bi}+V_{\rm S}+\phi_{\rm SB,n})-\phi_{\rm CG} \tag{10a}$$

$$\Phi_{\rm C,p}=\phi_{\rm CG}-(V_{\rm bi}+V_{\rm D}-\phi_{\rm SB,p}) \tag{10b}$$

Finally, the barrier height for carriers to overcome is the larger one between $\Phi_{\rm SBeff}$ and $\Phi_{\rm C}$ [12]:

$$\Phi_{\rm eff,n(p)}=\max[\Phi_{\rm SBeff,n(p)},\Phi_{C,n(p)}] \tag{11}$$

Therefore, the current through this barrier is given by

$$I_{\rm T,n(p)}=\pi R^2A^*_{\rm n(p)}T^2exp(-q\Phi_{\rm eff,n(p)}/kT) \tag{12}$$

in which $A^*_{\mathrm{n(p)}}$ is the effective Richardson's constant for electrons (holes).

After coming through the Schottky barriers, the carrier transport in the channel is described by the drift-diffusion model. Therefore, the inner part of the device operates like a conventional single-gate SiNWFET, which uses CG as the gate and PG-controlled regions as doped source and drain.

Based on this assumption, the drift-diffusion current in the channel is derived from (5) following the method in [10]:

$$\begin{aligned} I_{\mathrm{DD,n}} &= \mu_{\mathrm{n}} \frac{2\pi R}{L_{\mathrm{eff}}} \left[G(Q_{\mathrm{n,S}}) - G(Q_{\mathrm{n,D}})\right] \\ I_{\mathrm{DD,p}} &= \mu_{\mathrm{p}} \frac{2\pi R}{L_{\mathrm{eff}}} \left[G(Q_{\mathrm{p,D}}) - G(Q_{\mathrm{p,S}})\right] \\ G(Q) &= 2\frac{kT}{q}Q + \frac{Q^2}{2C_{\mathrm{ox}}} - \frac{kT}{q}Q_0 \ln \frac{Q_0 + Q}{Q_0} \end{aligned} \tag{13}$$

$Q_{\mathrm{n(p),S(D)}}$ is obtained by solving (5) with $V_G = V_{\mathrm{CG}}$ and $V_{\mathrm{n(p)}} = V_{\mathrm{n(p),PG_S}}$ at source or $V_{\mathrm{n(p)}} = V_{\mathrm{n(p),PG_D}}$ at drain.

If the recombination of carriers in the channel is neglected, the current continuity in the device gives

$$I_{\mathrm{T,n(p)}} = I_{\mathrm{DD,n(p)}} \tag{14}$$

In conventional MOSFET, the quasi-Fermi potential mostly drops at the drain side. Thus, we get

$$V_{\mathrm{n,CG}} = V_{\mathrm{n,PG_S}}, \qquad V_{\mathrm{p,CG}} = V_{\mathrm{p,PG_D}} \tag{15}$$

When reaching the other side of the channel, the carriers need to come over the other Schottky barrier. The corresponding currents are modeled as:

$$I_{\mathrm{T,n}} = \pi R^2 A^*_n T^2 exp(-\frac{q\Phi_{\mathrm{SB,n}}}{kT})(e^{\frac{q(V_{\mathrm{D}} - V_{\mathrm{n,PG_D}})}{kT}} - 1) \tag{16a}$$

$$I_{\mathrm{T,p}} = \pi R^2 A^*_p T^2 exp(-\frac{q\Phi_{\mathrm{SB,p}}}{kT})(e^{\frac{q(V_{\mathrm{p,PG_S}} - V_{\mathrm{S}})}{kT}} - 1) \tag{16b}$$

Combining both (16) and (12) yields to:

$$V_{\mathrm{n,PG_D}} = V_{\mathrm{D}} - \frac{kT}{q} \ln \left[1 + exp\left(\frac{q(\Phi_{\mathrm{SB,n}} - \Phi_{\mathrm{eff,n}})}{kT}\right)\right] \tag{17a}$$

$$V_{\mathrm{p,PG_S}} = V_{\mathrm{S}} + \frac{kT}{q} \ln \left[1 + exp\left(\frac{q(\Phi_{\mathrm{SB,p}} - \Phi_{\mathrm{eff,p}})}{kT}\right)\right] \tag{17b}$$

By solving (14), (15) and (17), the quasi-Fermi potentials and thereby surface potentials and current are obtained.

In the above analysis, the Schottky barriers and the nanowire channel are separately modeled. Therefore, advanced physical effects associated with Schottky barriers and the channel can be easily integrated into the proposed core framework. We do not address these questions in this work due to the page limit.

IV. Results and Discussions

First, we verify the model of electrostatic potential with respect to numerical solution of Poisson's equation (1) using a finite element method. In the demonstrated device, an undoped silicon nanowire with a diameter of 30 nm is used as the channel, unless specified otherwise. The thickness of SiO_2 is 2 nm. The potential at the surface and the center of the nanowire as well as the potential distribution along the radial direction are

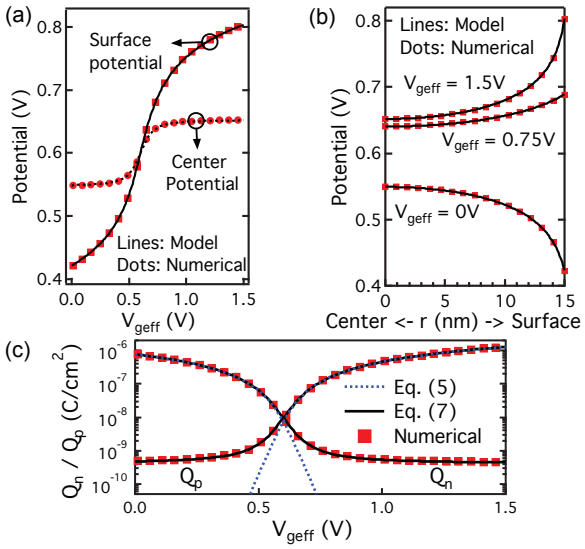

Fig. 2. (a) Surface potential and center potential, (b) potential distribution along the radius direction in the silicon nanowire. (c) The carrier density. Quasi-Fermi potentials V_{n} and V_{p} are set to 0.2 V and 1.0 V, respectively.

shown in Figs. 2a and 2b with given quasi-Fermi potentials. As observed from the figures, the proposed potential model agrees well with numerical solution and provides a smooth transition between different gate voltages. Fig. 2c shows the calculated carrier densities with the numerical solution. Although (5) is accurate for calculating majority carriers, it cannot accurately model minority carriers. In contrast, the unified solution (7) presents a good match with numerical solution.

In order to further verify the whole model, a double-gate SiNWFET as illustrated in Fig. 1a is simulated using Synopsys Sentaurus [15]. In the 3-D simulation, the coupled Poisson's equation and drift-diffusion model are self-consistently solved. The length of each gate is set to be 200 nm. Metal gates with mid-gap workfunction and Schottky barrier contacts with the workfunction of 4.45 eV are applied. WKB approximation is used to calculate the tunneling at Schottky contacts and a constant mobility model is applied in the channel.

According to the analysis in Sec. III, the device can be described by three components in series as shown in the inset of Fig. 3. The Schottky contacts together with PG can be considered as back-to-back Schottky diodes with an additional modulation by PG. CG modulates the barrier in the middle of the channel as in conventional MOSFETs.

The surface potential distribution along the channel for *n*-type configuration is shown in Fig. 3 by fixing V_{PG} at 1.5V. When increasing V_{CG}, not only ϕ_{CG}, but also $\phi_{\mathrm{PG_S}}$ increases due to the change of quasi-Fermi potentials.

With a fixed V_{PG}, the device behaves in the deep subthreshold region as a conventional MOSFET. As observed in Fig. 4a, the *S*ubthreshold *S*lope (SS) is approaching the ideal value, since the effective barrier height is determined by (10). Beyond this region, the current starts to be dominated by the effective Schottky barriers as described in (9), limiting SS. Note that,

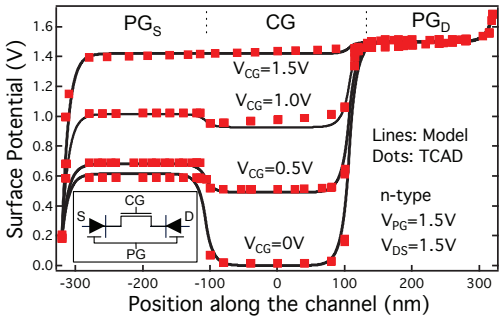

Fig. 3. Surface potential distribution along the channel with $V_{PG} = V_{DS} = 1.5V$ (n-type). Inset: equivalent circuit symbol of the double-gate SiNWFET.

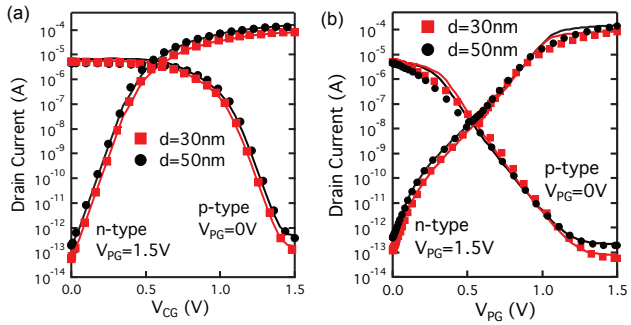

Fig. 4. The predicted drain current with different nanowire diameters under (a) a fixed V_{PG} and (b) a fixed V_{CG} for both n-type and p-type configurations. $V_{DS} = 1.5V$ (lines: model, dots: TCAD simulation).

the electron current also contributes to the leakage in p-type configuration, resulting in a degraded gate control over the leakage current near $V_{CG} = 1.5V$.

In contrast, when varying V_{PG} while applying a fixed bias on CG, the drain current is determined by the Schottky barriers within the whole subthreshold region. In this case, the SS is worse than varying V_{CG} as shown in Fig. 4b. However, in the deep subthreshold region of n-type characteristics, $\phi_{PG_S} < V_{bi} + V_S$. Thus, the effective barrier height is determined by ϕ_{PG_S}. This effect is included in the model by replacing ϕ_{CG} by $\min[\phi_{CG}, \phi_{PG_S}]$ in (10a). The resulted different regimes of SS in n-type configuration can also be observed in Fig. 4b.

The simple assumption of λ in the model does not perfectly capture the effect of the induced carriers, thus causing slight difference between the prediction and TCAD simulation when the device completely turns *on*. However, it can be addressed by introducing a unified λ as in [11]. For simplicity, the modeling of the bias-dependent λ is not discussed in this work.

If PG and CG are connected together, the device works as a single-gate Schottky-barrier MOSFET. The ambipolar characteristics are shown in Fig. 5a. While Schottky-barrer devices are appealing because they do not require chemical doping, they also suffer from low I_{on}/I_{off} ratio with poor subthreshold slope due to the ambipolar behavior. In this work, we exploit electrostatic control of the Schottky barriers with an additional gate to achieve high I_{on}/I_{off} ratio as well as near-ideal subthreshold slope as demonstrated by both the

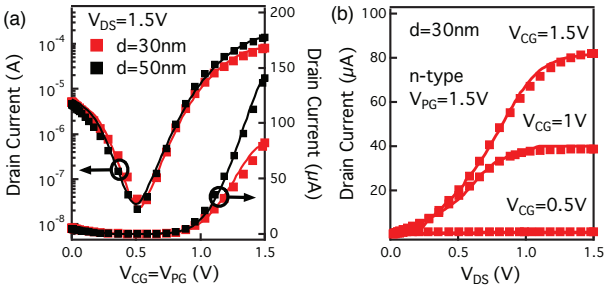

Fig. 5. (a) Ambipolar characteristics by applying the same V_{CG} and V_{PG}, (b) output characteristics with a fixed V_{PG}. (lines: model, dots: TCAD)

experiments [4] and compact modeling. Fig. 5b shows the output characteristics with a fixed polarity-gate voltage.

V. Conclusions

This paper presents a physics-based potential and drain current model for polarity-controllable SiNWFETs with a double-gate structure. By solving both carrier tunneling at Schottky contacts and the drift-diffusion in the channel, the potential distribution and drain current are obtained. The proposed model show good agreements with TCAD simulation for different bias configurations. A complete and more accurate model can be built based on the presented framework, and used for the exploration of functionality-enhanced devices.

Acknowledgment

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