

Response to “Comment on ‘Assessment of field-induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field-effect transistor’” [Appl. Phys. Lett. **106, 026102 (2015)]**

J. L. Padilla, C. Alper, F. Gámiz, and A. M. Ionescu

Citation: [Applied Physics Letters](#) **106**, 026103 (2015); doi: 10.1063/1.4905866

View online: <http://dx.doi.org/10.1063/1.4905866>

View Table of Contents: <http://scitation.aip.org/content/aip/journal/apl/106/2?ver=pdfcov>

Published by the [AIP Publishing](#)

Articles you may be interested in

[Comment on “Assessment of field-induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field-effect transistor” \[Appl. Phys. Lett. **105**, 082108 \(2014\)\]](#)

Appl. Phys. Lett. **106**, 026102 (2015); 10.1063/1.4905865

[Impact of field-induced quantum confinement on the onset of tunneling field-effect transistors: Experimental verification](#)

Appl. Phys. Lett. **105**, 203507 (2014); 10.1063/1.4902117

[Assessment of field-induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field-effect transistor](#)

Appl. Phys. Lett. **105**, 082108 (2014); 10.1063/1.4894088

[Tensile strained Ge tunnel field-effect transistors: k-p material modeling and numerical device simulation](#)

J. Appl. Phys. **115**, 044505 (2014); 10.1063/1.4862806

[Modeling of a vertical tunneling graphene heterojunction field-effect transistor](#)

Appl. Phys. Lett. **101**, 033503 (2012); 10.1063/1.4737394

The logo for Applied Physics Letters (AIP) is displayed in a white font on an orange background. The letters 'AIP' are large and bold, followed by a vertical bar and the words 'Applied Physics Letters' in a smaller font.

Meet The New Deputy Editors



Alexander A.
Balandin



Qing Hu



David L.
Price

Response to “Comment on ‘Assessment of field-induced quantum confinement in heterogate germanium electron–hole bilayer tunnel field-effect transistor’” [Appl. Phys. Lett. 106, 026102 (2015)]

J. L. Padilla,^{1,a)} C. Alper,¹ F. Gámiz,² and A. M. Ionescu¹

¹Nanoelectronic Devices Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne CH-1015, Switzerland

²Departamento de Electrónica y Tecnología de los Computadores, Universidad de Granada, Avda. Fuentenueva s/n, 18071 Granada, Spain

(Received 27 November 2014; accepted 31 December 2014; published online 15 January 2015)

[<http://dx.doi.org/10.1063/1.4905866>]

In our letter,¹ we demonstrated that the inclusion of field-induced quantum confinement in the analysis of the Ge Electron–Hole Bilayer Tunnel Field–Effect Transistor (EHBTFET) led to the appearance of undesired lateral tunneling which degraded the so far reported outstanding switching behavior of these devices.² We showed that a heterogate configuration (HG-EHBTFET) with different work-functions for the overlap and underlap sections of the top gate, ϕ_{tg1} and ϕ_{tg2} , respectively (see Fig. 1(c) in Ref. 1), proved to be appealingly efficient to suppress this parasitic tunneling at $V_D = 0.5$ V and restore the steepness of the $I_D - V_{TG}$ curves. The main point of the comment raised by Hsu *et al.*³ was to elucidate the potential drawbacks that the proposed work function difference might cause at low drain voltages. They showed that no deleterious effects arise in that scenario by analyzing the electron eigenenergy difference for the first subbands in the overlap and underlap regions, ΔE , for $V_D < 0.5$ V and concluded that a heterogate configuration is also quite advisable at low V_D . Furthermore, they showed (Fig. 1(b) in Ref. 3) that there exists an optimized value of ϕ_{tg2} for which ΔE turns out to be approximately independent of V_D . Our response seeks to explain the interesting behavior of the $\Delta E(V_D)$ curves depicted in Fig. 1(b) of the comment by Hsu *et al.*³ for better understanding of the effect that heterogate configuration has on the performance of these devices. The results herein presented were obtained employing the simulation approach used in our original letter¹ with the device structure considered by Hsu *et al.*³

First, the increasing behavior of ΔE at very low V_D for $\phi_{tg2} = 4.3$ eV (Ref. 3) is due to the tighter control that the drain exerts over the first electron subband in the overlap, $E_{e1,OL}$ compared to that in the underlap, $E_{e1,UL}$, as seen in Fig. 1 where we plot the derivative of E_{e1} with respect to V_D . Second, the almost constant behavior of ΔE for $\phi_{tg2} = 4.2$ eV (Ref. 3) follows from the similar pattern of the $E'_{e1}(V_D)$ curves in both regions. Third, the saturation of the decreasing pattern of ΔE observed for $\phi_{tg2} = 4.1$ eV (Ref. 3) that starts at $V_D \approx 0.18$ V comes from the depinning of $E_{e1,UL}$. As displayed in the inset, we can estimate the point at which this depinning takes place by means of the maximum

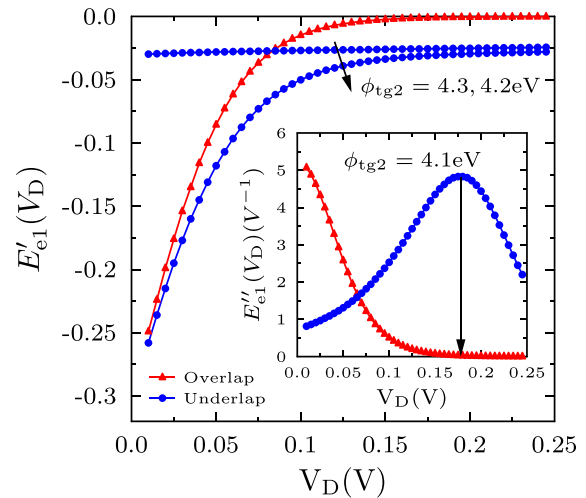


FIG. 1. First derivative and second derivative (inset) of the energy of the first subbands for electrons as a function of the drain voltage in both overlap and underlap regions corresponding to the structure depicted in Fig. 1(a).³

of second derivative⁴ of $E_{e1}(V_D)$ and confirm that it occurs at a value of $V_D = 0.18$ V. For $V_D > 0.18$ V the depinning implies that the top gate recovers the control over $E_{e1,UL}$ and therefore when we increase ϕ_{tg2} by 0.2 eV from 4.1 to 4.3 eV, ΔE behaves practically likewise (Fig. 1(b) in Ref. 3).

This response complements the pertinent comment by Hsu *et al.*³ reinforcing the HG-EHBTFET reliability at low drain voltages and provides an explanation for the observed behavior of the eigenenergy difference between the first bound states for electrons in the overlap and underlap regions when increasing ϕ_{tg2} .

¹J. L. Padilla, C. Alper, F. Gamiz, and A. M. Ionescu, *Appl. Phys. Lett.* **105**, 082108 (2014).

²L. Lattanzio, L. De Michielis, and A. M. Ionescu, *IEEE Electron Device Lett.* **33**, 167 (2012).

³W. Hsu, J. Mantley, L. F. Register, and S. K. Banerjee, *Appl. Phys. Lett.* **106**, 026102 (2015).

⁴J. L. Padilla, F. Gamiz, and A. Godoy, *IEEE Trans. Electron Devices* **59**, 3205 (2012).

^{a)}Electronic mail: jose.padilladelatorre@epfl.ch