3-Dimensional Devices:
Models and Design Tools

Giovanni De Micheli
The emerging nano-technologies

- *Enhanced* silicon CMOS is likely to remain the main manufacturing process
  - The 10nm and 7nm technology nodes are planned
- What are the candidate technologies for the 5nm node and beyond?
  - Tunneling FETs (TFET)
  - Silicon Nanowires (SiNW)
  - Carbon Nanotubes (CNT)
  - 2D devices (flatronics)
- What are the common denominators from a design standpoint?

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22 nm Tri-Gate Transistors

32 nm Planar Transistors

22 nm Tri-Gate Transistors

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[Courtesy: M. Bohr]
From FinFET to Nanowire FET

FinFET  NW FET
Vertically-aligned Nanowire FETs

NW FET

Gate-All-Around
- Electrically program the transistor to either p-type or n-type
- Field-effect control of the Schottky barrier
Silicon Nanowire Transistors

- Gate all around transistors
- Double gate to control polarity

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[Courtesy: De Marchi, EPFL]
Silicon Nanowire Transistors

- Gate all around transistors
- Double gate to control polarity

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[Courtesy: De Marchi, EPFL]
Device cross sections

- NW stack
- Gate Oxide
- PolySi

100nm

- NW stack
- d<20nm

100nm
Device working principle

PG = 1 → n-type
CG = 0

PG = 1 → n-type
CG = 1

PG = 0 → p-type
CG = 1

PG = 0 → p-type
CG = 0
Device $I_d/V_{cg}$

[Image: A graph showing the relationship between $V_{cg}$ and $Log(I_d)$ for different values of $V_{pg}$. The graph includes lines for $V_{pg} = -4V$, $-2V$, $0V$, $2V$, and $4V$. The graph highlights the difference in slope for $V_{pg} = 0V$ with a 64mV/dec decrease and $V_{pg} = -4V$ with a 70mV/dec decrease.]

[Courtesy: De Marchi, IEDM 12 EPFL]
Similar devices

- Controlled devices can be realized with various materials and shapes (e.g., FINFET)
- SiNW controlled-polarity devices can be made with one polarity gate on one side [Heinzig]
- Polarity-gate bias can enable:
  - Steep Subthreshold
  - Multiple threshold voltages
Steep subthreshold slope devices

- Polarity gate at fixed voltage to create potential wells
- Barrier lowering due to carrier generation by impact ionization and accumulation in S/D well areas

![Graph showing drain current versus gate voltage for different drain voltages.](image)

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[Zang –IEDM 14]
Average Subthreshold slope

- 6 mV/decade over 5 decades of current
Three-independent-gate SiNWFET

- **Structure**
  - Vertically stacked nanowires
  - 3 independent gate regions
  - Schottky barrier contacts at S/D
  - Polarity and Vt controllability

- **Electrostatic control**
  
<table>
<thead>
<tr>
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<th>CG</th>
<th>PGD</th>
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Library cell design for double-gate SiNWFETs

- Exploit complementary to achieve full swing
- Require smart local routing to compensate for extra input
- Major advantage is handling binate logic functions well (e.g., XOR)

<table>
<thead>
<tr>
<th>Negative Unate functions</th>
<th>Binate functions</th>
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<tbody>
<tr>
<td>INV</td>
<td>XOR2</td>
</tr>
<tr>
<td>NAND2</td>
<td></td>
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</table>

Similar to regular CMOS

Only 4 transistors when compared to 8 transistors with a regular CMOS

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[Courtesy: H. Ben Jamaa, '08]
2 FET inverter configuration

IN \rightarrow \text{OUT}

PG-PU

PG-PD

Vdd = 1V
PG-PD = 1V
PG-PU = -0.5V
2 transistor XOR circuit

![Diagram of 2 transistor XOR circuit with input A, input B, XOR gate, and output OUT.]

![Graph showing the output voltage (OUT) versus input voltage (A) with two curves. One curve represents Vdd=1V and the other represents B=0V, B=1V.]
Full swing XOR circuit
Dumbbell-stick diagrams

Transistor pairing

Control gates connected together

Transistor grouping

Polarity gates connected together
Layout abstraction and regularity with *Tiles*

Two transistor pairs grouped together

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[Courtesy: Bobba, DAC 12]
Logic level abstraction

- Three terminal transistors are switches
  - A loaded transistor is an *inverter*
- Controllable-polarity transistors compare two values
  - A loaded transistor is an *exclusive or* (EXOR)
- The intrinsic higher computational expressiveness leads to more efficient data-path design
- The larger number of terminals must be compensated by smart wiring
**Biconditional Binary Decision Diagrams**

- Native **canonical** data structure for logic design
- **Biconditional** expansion:
  \[
  f(v, w, \ldots, z) = (v \oplus w)f(w', w, \ldots, z) + (v \oplus w)f(w, w, \ldots, z)
  \]

- Each BBDD node:
  - Has two branching variables
  - Implements the **biconditional** expansion
  - Reduces to Shannon’s expansion for single-input functions
The BDD counterparts for these examples have about 50% more nodes!
Efficient Direct Mapping of BBDD Nodes

BBDD node

MUX driven by a XNOR

Controlled-polarity

CMOS
The BBDD optimization tool

- Unique table to store BBDD nodes
- Recursive formulation of Boolean operations
- Performance-oriented memory management
- Chain variable reordering

http://lsi.epfl.ch/BDD
Experimental results

- We implemented a BBDD package in C language
  - Comparison with CUDD (BDD)
- Both CUDD and BBDD first build the DDs and then apply sifting (no dynamic reordering)

Also 1.63x speedup for arithmetic intensive circuits
Modeling various emerging nanogates

CNFETs

SiNWFTs

Graphene FETs

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Reversible Logic

6T Nanorelays

4T Nanorelays
Conclusions

- The FINFET is the first successful 3D transistor
- FINFET evolution comprises variations:
  - Multi filament devices (NanoWires)
  - Multi gate devices
- Additional gate biasing can be used to enhance logic functionality and/or performance of devices
- Device effectiveness in constructing logic cells depends significantly on physical design
- New logic design tools are key to assess the potential use of these technologies

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Thank you

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