Leakage mechanisms and contact technologies in InAlN/GaN high electron mobility transistors

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This thesis is dedicated to my family
and to Laura

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Abstract

GaN based electronic devices have progressed rapidly over the past decades and are nowadays starting to replace Si and classical III-V semiconductors in power electronics systems and high power RF amplifiers. AlGaN/GaN heterostructures have been, until recently, the materials system of choice for nitride based electronics. The limits of AlGaN/GaN technologies are now known and alternative routes able to overcome them are actively investigated. Nearly lattice-matched InAlN/GaN heterostructures have emerged as viable solutions for extending the frequency range achievable by GaN based devices. These heterostructures have also proven a very high thermal stability, becoming of high interest for extreme environment applications. However, despite those great potentials, InAlN/GaN based devices, in particular high electron mobility transistors, have suffered from high leakage currents, strong short channel effects and low breakdown voltage that made them not competitive with respect to AlGaN/GaN technologies.

The goal of this thesis is to investigate, understand and control the mechanisms that limit the performance of InAlN/GaN based transistors. Particular attention in this thesis will be given to leakage currents, having gate or buffer origin. Concerning gate leakage currents, an accurate model for InAlN/GaN heterostructures will be established and the expected presence of deep levels will be confirmed by means of photocapacitance spectroscopy. Based on these results, it will be shown that two conduction mechanisms contribute to gate leakage currents. A first mechanism dominates in heterostructures with thin (≤ 7 nm) InAlN barriers, while a second mechanism related to the appearance of degraded region becomes dominant in heterostructures with thicker barriers.

Two approaches will be developed for the reduction of buffer leakage currents. A first approach consists in the growth of high quality heterostructures with extremely thin (50 nm) GaN buffer. It will be shown that thanks to this method high electron mobility transistors (HEMTs) with ON/OFF current ratios as high as 5×10^9 can be obtained. This approach will prove effective for the achievement of transistors able to display high performance at temperatures as high as 600 °C. A second approach, which will be developed for microwave transistors, makes use of heterostructures implementing an $Al_{0.04}Ga_{0.96}N$ back-barrier .

The reduction of ohmic contact resistivity will be also considered and the achievement of regrown ohmic contacts by NH_3-MBE will be discussed. A last topic covered will be the thermal stability of InAlN based heterostructures at very high temperatures (850 °C). It will be shown that the stability can be greatly improved by appropriately capping InAlN with a thin GaN layer. This technique will be exploited for the achievement of state of the art InAlN/GaN

heterostructures incorporating an *in situ* SiN passivation. To conclude, the performance of InAlN/GaN based transistors for both microwave and high temperature applications will be presented and discussed, demonstrating that these devices can now seriously compete with AlGaN/GaN based technologies.

Keywords: GaN, InAlN, 2 Dimensional Electron Gas, High Electron Mobility Transistor, Leakage Current, Deep Levels, Schottky Contact, Ohmic Contact, Passivation, Back-Barrier, High Temperature Electronics, Microwave Transistors

Résumé

Au cours des deux dernières décennies, les dispositifs électroniques à base de GaN ont progressé rapidement et commencent maintenant à remplacer le silicium et les semi-conducteurs III-V classiques dans certains systèmes d'électronique de puissances et amplificateurs RF. Les hétérostructures AlGaN/GaN ont été, jusqu'à maintenant, la plateforme de choix pour l'électronique à base de nitrures. Les limites des technologies AlGaN/GaN sont maintenant connues et des alternatives capables de surmonter ces limites sont activement étudiées. Les hétérostructures InAlN/GaN en quasi accord de maille ont émergé comme une alternative viable pour étendre le spectre de fréquences des dispositifs à base de GaN. Ces hétérostructures ont aussi démontré une très grande stabilité thermique, devenant ainsi intéressantes pour des applications sous environnements extrêmes. Cependant, malgré ce potentiel, les dispositifs à base d'hétérostructures InAlN/GaN et en particulier les transistors à haute mobilité électronique, souffrent de courants de fuite élevés, de forts effets de canal court et de basses tensions de claquage qui ne les rendent pas compétitifs par rapport aux technologies AlGaN/GaN.

L'objectif de cette thèse est d'étudier, comprendre et contrôler les mécanismes qui limitent les performances des transistors InAlN/GaN. Une attention particulière sera portée aux courants de fuite, soient ceux générés sous l'électrode de grille, soient ceux générés dans la couche tampon de GaN. Pour ce qui concerne les courants de fuite provenent de la grille, une modélisation des hétérostructures InAlN/GaN sera conduite, et la présence attendue de niveaux profonds dans l'InAlN sera explorée à l'aide de la spectroscopie de photocapacité. En se basant sur ces résultats, il sera montré que deux mécanismes de conduction contribuent aux courants de fuite. Un premier mécanisme est préponderant pour les hétérostructure avec une barrière d'InAlN très fine (≤ 7 nm), alors qu'un deuxième mécanisme, lié à l'émergence de régions dégradées en surface, domine dans les hétérostructures à barrière plus épaisse.

Deux approches seront développées pour la réduction des courants de fuites originaires de la couche tampon. Une première approche consiste à réaliser des hétérostructures de bonne qualité comprenant une couche tampon de GaN extrêmement fine (50 nm). Grâce à cette approche, il sera montré que des transistors avec un rapport de courants ON/OFF atteignant 5×10^9 peuvent être fabriqués. Cette approche permet aussi la réalisation de transistors capables de hautes performances à des températures de 600 °C. La seconde approche, utilisée pour des transistors destinés aux applications microondes, se base sur des hétérostructures comprenant une "back-barrier" d'$Al_{0.04}Ga_{0.96}N$.

La réduction de la résistivité des contacts ohmiques sera aussi mise en oeuvre et la réalisation de contacts ohmiques par recroissance avec NH_3-MBE sera discutée. Une dernière thématique

traitée sera celle de la stabilité thermique (850 °C) des hétérostructures à base d'InAlN. Il sera démontré que la stabilité peut être fortement augmentée en protégeant la surface d'InAlN avec une très fine couche de surface de GaN. Cette technique sera exploitée pour la réalisation d'hétérostructures InAlN/GaN incorporant une passivation SiN déposée *in situ* et ayant des propriétés de transport rivalisant avec l'état de l'art. Pour conclure, les performance des transistors à base d'hétérostructures InAlN/GaN pour applications microondes et très hautes températures seront présentées et discutées, montrant que ces dispositifs peuvent maintenant sérieusement rivaliser avec ceux à base d'hétérostructures AlGaN/GaN.

Mots clefs : GaN, InAlN, Gaz Bidimensionnel d'Électrons, Transistor à Haute Mobilité Électronique, Courants de Fuite, Niveaux profonds, Contact Schottky, Contact Ohmique, Passivation, Back-Barrier, Électronique à Haute Température, Transistors Microondes.

Riassunto

Durante gli ultimi vent'anni, i dispositivi elettronici basati su GaN hanno progredito rapidamente in quanto a prestazioni e cominciano a sostituire i dispositivi basati su silicio e sui semiconduttori III-V classici in alcuni sistemi di elettronica di potenza e amplificatori RF. Le eterostrutture AlGaN/GaN sono state finora la piattaforma preferenziale per l'elettronica basata sui nitruri. I limiti di questa tecnologia sono però diventati evidenti e delle soluzioni alternative capaci di migliori prestazioni sono studiate intensamente. Le eterostrutture InAlN/GaN quasi lattice-matched sono emerse come una valida alternativa per estendere lo spettro di frequenze di operazione dei dispositivi a nitruri. Queste eterostrutture hanno inoltre dimostrato un'altissima stabilità termica, diventando di conseguenza interessanti anche per applicazioni in ambienti estremi. Ciononostante, malgrado il loro grande potenziale, i disposivitivi basati su eterostrutture InAlN/GaN ed in particolare i transitor ad alta mobilità elettronica, hanno a lungo sofferto di forti correnti parassite, effetti di canale corto e basse tensioni di rottura che li rendevano non competitivi rispetto alle tecnologie AlGaN/GaN.

L'obiettivo di questa tesi è di studiare, comprendere e controllare i meccanismi che limitano le prestazioni dei transistor InAlN/GaN. Un'attenzione particolare sarà data alle correnti parassite, sia quelle provenienti dal gate, sia quelle di buffer. Per quanto riguarda le correnti parassite provenienti dal gate, verrà sviluppato un modello per le eterostrutture, e la presenza di trappole elettroniche profonde sarà esplorata per mezzo della spettroscopia fotocapacitiva. Sulla base di questi risultati, verrà dimostrato che due meccanismi contribuiscono a questo tipo di correnti parassite. Un primo meccanismo è dominante nelle eterostrutture aventi una barriera di InAlN molto fine (≤ 7 nm), mentre un secondo meccanismo, legato alla presenza di piccole regioni degradate, diventa dominante nele eterostrutture con barriere più spesse.

Due approcci saranno sviluppati per la riduzione delle correnti parassite di buffer. Un primo approccio consiste nella realizzazione di eterostrutture di buona qualità integranti un buffer di GaN estremamente sottile (50 nm). Grazie a questo metodo, verrà dimostrato che dei transistor con rapporti di corrente ON/OFF fino a 5×10^9 possono essere fabbricati. Questo approccio si dimostrerà utile anche per la realizzazione di transistors capaci di ottime prestazioni a temperature elevate, in particolare fino a 600 °C. Per i transistor destinati ad appliazioni nelle microonde verranno invece sviluppate delle eterostrutture comprendenti una back-barrier di $Al_{0.04}Ga_{0.96}N$.

La riduzione della resistività dei contatti ohmici sarà inoltre trattata e la realizzazioni di contatti ohmici per ricrescita con NH_3-MBE sarà discussa. L'ultima tematica che verrà analizzata sarà quella della stabilità ad altissima temperatura (850 °C) delle eterostrutture basate su InAlN.

Dimostreremo che un'ottima stabilità può essere ottenuta proteggendo la superficie dell'InAlN con un cap molto sottile di GaN. Questa tecnica sarà sfruttata per ottenere delle eterostrutture InAlN/GaN integranti una passivazione *in situ* di SiN e caratterizzate da proprietà di trasporto ottimali. Per concludere, le prestazioni dei transitor InAlN/GaN per applicazioni nelle microonde e ad alta temperatura saranno presentate e discusse, dimostrando che questi dispositivi possono ora competere seriamente con quelli basati su eterostrutture AlGaN/GaN.

Parole chiave : GaN, InAlN, Gas Bidimensionale di Elettroni, Transistor ad Alta Mobilità Elettronica, Correnti Parassite, Trappole Elettroniche Profonde, Contatto Schottky, Contatto Ohmico, Passivazione, Back-Barrier, Elettronica ad Alta Temperatura, Transistor per Microonde.

Table of Contents

Acknowledgements **i**

Abstract (English/Français/Italiano) **iii**

Contents **ix**

Introduction **1**

1 Basic properties and advantages of InAlN/GaN HEMTs **5**
1.1 Basic properties of III-nitride semiconductors 5
1.1.1 Band structure and lattice constant of III-nitride semiconductors 5
1.1.2 Spontaneous and piezoelectric polarization 7
1.2 Advantages of III-nitrides for electron devices 9
1.3 Polarization induced 2 dimensional electron gases 12
1.3.1 Ungated 2 dimensional electron gas 12
1.3.2 Gated 2 dimensional electron gas 14
1.3.3 Transport properties of the 2 dimensional electron gas 15
1.4 High electron mobility transistors 18
1.4.1 Static behavior 18
1.4.2 Dynamic behavior 21
1.5 AlGaN/GaN HEMTs: state of the art and technological limits 25
1.6 InAlN/GaN HEMTs: beyond AlGaN/GaN HEMTs limits 27
1.6.1 State of the art of InAlN/GaN HEMT technologies 27
1.6.2 Issues of InAlN/GaN HEMTs 29

2 Physics of InAlN/GaN heterostructures **33**
2.1 Experimental techniques 33
2.1.1 Measurement of transport properties 33
2.1.2 Electrochemical capacitance-voltage 34
2.1.3 Schottky diode fabrication on thick InAlN layers 35
2.1.4 Photocapacitance spectroscopy 36
2.2 Electron mobility of InAlN/GaN 2DEGs 36
2.2.1 General electron mobility theory 36
2.2.2 Scattering mechanisms in InAlN/GaN heterostructures 38

2.2.3 Modeling of InAlN/GaN 2DEG electron mobilities 41
2.3 InAlN physical parameters 43
2.4 Deep levels in InAlN 48
2.4.1 Photocapacitance spectroscopy of InAlN 49

3 Growth of InAlN/GaN heterostructures 57
3.1 Experimental techniques 57
3.1.1 Metal organic vapor phase epitaxy 57
3.1.2 X-ray diffraction 59
3.1.3 Atomic force microscopy 61
3.2 Growth of InAlN alloys 61
3.3 Growth of InAlN/GaN HEMTs on sapphire 62
3.3.1 Standard InAlN/GaN HEMTs on sapphire 63
3.3.2 InAlN/GaN HEMTs with thin buffers 65
3.4 InAlN/GaN HEMTs on SiC 72
3.5 InAlN/GaN HEMTs on Si 73

4 InAlN/GaN HEMTs: building blocks 77
4.1 Experimental techniques 77
4.1.1 Schottky diode fabrication 77
4.1.2 Molecular beam epitaxy of regrown contacts 78
4.2 Ohmic contacts 79
4.2.1 Annealed contacts 80
4.2.2 Regrown contacts 81
4.3 Schottky contacts 85
4.3.1 Trap assisted tunneling currents 88
4.3.2 Direct tunneling currents 92
4.4 *in situ* SiN passivation 95
4.5 Back-barriers 101

5 Performances of InAlN/GaN HEMTs 105
5.1 HEMTs with thin buffers for high temperature electronics 105
5.2 InAlN/GaN HEMTs for high frequency applications 107
5.2.1 InAlN/GaN HEMTs on SiC for large signal operation at 40 GHz 108
5.2.2 InAlN/GaN HEMTs on Si for large signal operation at 94 GHz 111
5.2.3 Considerations about the potentials of InAlN/GaN HEMTs 114

6 Conclusions 117
6.1 Summary of the results 117
6.2 Outlook 119

A The Fang-Howard approximation 121
A.1 The Fang-Howard wavefunction 121
A.2 The modified Fang-Howard wavefunction 122

Bibliography **125**

Acronyms **141**

Curriculum Vitae **143**

Introduction

Since the first reports of GaN based field effect transistors [1,2] in 1993, the field of GaN based electronics has grown significantly and has gained a considerable interest for a number of applications, in particular those where high power levels are involved. This is due to the large band gap of GaN and of most III-nitride semiconductors, which allow for high breakdown voltages, and at the same time to the high density of the polarization induced 2 dimensional electron gas (2DEG) achievable at the interface between III-nitride materials, which results in high current densities. Therefore, GaN based transistors emerged as interesting candidates for replacing classical III-V semiconductors or Si in power electronics applications and in power RF amplifiers. During the past two decades, AlGaN/GaN high electron mobility heterostructures dominated the field of III-nitride based electronics and AlGaN/GaN based devices have nowadays reached a certain technological maturity, moving from research to the production stage (see for example [3,4]). The limits of AlGaN/GaN technologies have been reached now, in particular for those concerning the frequency bands they can cover. The bottom part of the mm-wave spectrum (30-300 GHz) seems at present the maximum frequency range achievable by AlGaN/GaN devices without incurring in complicated processing methods. Furthermore, the unavoidable strain caused by the lattice mismatch between GaN and AlGaN limits the Al content of the barrier to about 30% and therefore the 2DEG density to $\sim 10^{13}$ cm^{-2}. As a consequence, the maximum current density is limited to ~ 1 A/mm. The presence of strain has been identified as a source of failure for these devices [5,6].

First proposed by Kuzmík in 2001 [7], nearly lattice-matched InAlN/GaN high electron mobility heterostructures present several advantages with respect to their AlGaN/GaN counterparts. They allow in particular for a more efficient downscaling of the transistor dimensions, making easier the achievement of devices with cutoff frequencies > 200 GHz [8]. Furthermore, transistors based on this material system have been shown to produce current densities in excess of 2 A/mm [9], which is a great asset for the achievement of high power densities. Therefore, InAlN/GaN based devices are ideal candidates for power applications at frequencies as high as 100 GHz or more. Additionally, the lattice-matching condition allowed by InAlN alloys eliminates strain related issues, potentially enhancing the reliability [10].

Besides remarkable potentials for high frequency electronics, InAlN/GaN heterostructures have also demonstrated an exceptional thermal stability. Devices could be in fact operated in vacuum at temperatures as high as 1000 °C [11]. Therefore, high temperature electronics is a

second field of application where InAlN/GaN based devices may find interesting applications.

However, despite the great potentials of the technology, before this thesis work InAlN/GaN high electron mobility transistors (HEMTs) were suffering from several major issues that made them not competitive with respect to their AlGaN/GaN counterpart. In particular, high gate leakage currents and consequently low breakdown voltages were often reported [12], as well as strong short channel effects [13]. Ohmic contacts were also characterized, in best cases, by a still not optimal contact resistivity of $\sim 0.3\ \Omega\cdot$mm [13]. Devices for high temperature operation suffered on the other hand from high buffer leakage which strongly degraded their high temperature performances [9]. Finally, high performance devices were reported only on SiC.

Objectives and outline of this thesis

The objectives of this thesis are the understanding and control of parasitic leakage currents in InAlN/GaN heterostructures with the aim of improving InAlN/GaN HEMTs performances, both for high frequency and for high temperature operation. The achievement of ohmic contacts with lower resistivity is also part of the objectives of this thesis, as well as the achievement of heterostructures with reduced short channel effects. Finally, a last goal is the growth of high quality heterostructures on Si and to establish their benchmark with respect to heterostructures on SiC for high frequency applications.

Chapter 1 will introduce the most relevant III-nitride materials properties. The role played by polarization in the formation of high density 2DEGs will be treated with particular attention. High electron mobility transistors will be then introduced, and the state of the art of AlGaN/-GaN will be briefly reviewed. InAlN/GaN HEMTs will be then introduced and discussed.

Chapter 2 will deal with the physical properties of InAlN/GaN HEMTs. An accurate model for the prediction of the barrier thickness and bias dependences of the 2DEG will be developed based on experimental data. For this purpose, several relevant InAlN related parameters will be determined. The scattering mechanisms limiting the electron mobility will be also described and their relative importance discussed. Finally, deep levels in InAlN will be tackled, and experimental evidence for the presence of a broad band of deep levels will be given by means of photocapacitance measurements. In particular, the deep levels are characterized by an optical ionization energy centered around 1.7 eV and a broadening parameter of 0.38 eV.

Chapter 3 will describe the growth of InAlN/GaN heterostructures by metal-organic vapor phase epitaxy. The growth on three different substrates will be treated, namely sapphire, SiC and Si. Concerning sapphire substrates, it will be demonstrated the possibility of achieving high quality heterostructures with extremely thin (50 nm) GaN buffers. Particular attention will be also given to heterostructures on Si. In particular, it will be discussed how to achieve crack-free heterostructures by means of a graded AlGaN strain management layer.

Chapter 4 will focus on several building blocks of advanced InAlN/GaN HEMTs. Ohmic contacts will be discussed first, and low resistivity ohmic contacts by ammonia molecular beam epitaxy will be demonstrated. Schottky contacts will be then studied, with particular attention given to leakage currents. Thanks to the model developed in chapter 2, it will be shown that the deep levels around 1.7 eV evidenced by photocapacitance spectroscopy are responsible for leakage currents in heterostructures with thin InAlN barriers ($\leq$ 7 nm), while for thicker barriers a second mechanism related to the appearance of degraded highly doped regions becomes dominant. The possibility of increasing the thermal stability of InAlN/GaN heterostructures by an appropriate cap layer will be then discussed and the achievement of *in situ* SiN passivated heterostructures. The final topic of this chapter will be the growth of InAlN/GaN heterostructures with AlGaN back-barriers on sapphire, SiC and Si substrates.

Chapter 5 will deal with InAlN/GaN HEMTs processed out of the various heterostructures described in the previous chapters. HEMTs on sapphire with ultrathin buffers will be discussed first, showing that they allow for a very high ON/OFF current ratio of 5×10^9 at room temperature. Their suitability for high temperature (up to 600 °C) electronics will be then considered. Two devices for high frequency operation will be then examined. First, an HEMT designed for large signal operation at 40 GHz will be presented, followed by one on Si designed for large signal operation at 94 GHz. Both devices allow for large power density, namely 5.85 W/mm for the former and 1.3 W/mm for the latter.

Finally, **Chapter 6** will review the results achieved and will conclude this thesis by a short outlook.

1 Basic properties and advantages of InAlN/GaN HEMTs

This chapter introduces the basic physical elements needed for understanding InAlN/GaN HEMTs. We will start with a general analysis of the basic properties of III-nitride semiconductors, followed by a short analysis of their advantages for high power applications. We will then introduce the topic of polarization induced 2DEGs and high electron mobility heterostructures, which form the basis of HEMTs. Finally, we will analyze the state of the art of AlGaN/GaN HEMTs and the main advantages offered by InAlN/GaN HEMTs.

1.1 Basic properties of III-nitride semiconductors

III-nitride materials are a class of compound semiconductors comprising AlN, GaN and InN. To the same family belong also the ternary alloys $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $In_xAl_{1-x}N$ and the quaternary alloy $In_xAl_yGa_{1-x-y}N$. GaN is the most important member of this family, as it can be grown with high quality to thicknesses easily exceeding 1 μm on a large variety of substrates such as sapphire, SiC and Si. Free standing bulk GaN substrates are also available and provide the best material quality. This has set GaN as the main building block of a wide range of nitride-based devices, such as field effect transistors, light emitting diodes or laser diodes. GaN is also the III-nitride semiconductor whose doping is best controlled. However, GaN alone is in general not sufficient for creating devices. GaN-based heterostructures including AlN, AlGaN, InGaN, InAlN or InAlGaN layers give a much larger design freedom and allow for functional electronic or optoelectronic devices. In this section, we review the main physical properties of III-nitride semiconductors, in particular the most relevant ones for electronic devices.

1.1.1 Band structure and lattice constant of III-nitride semiconductors

As a consequence of the strength of the metal-nitrogen bonds, the III-nitrides are characterized, except for InN, by larger band gaps and shorter lattice constants compared to other III-V compound semiconductor families, like arsenides, phosphides, antimonides and their alloys.

Table 1.1: Room temperature band gap E_g and a and c lattice constants of binary nitride materials, together with the bowing parameter b of ternary nitride alloys. Eventual dependence of the b over alloy composition is discussed in the text. The values marked with † and ‡ are taken from [20] and [14], respectively.

Material	E_g (eV)†	a (Å)†	c (Å)†	Alloy	b (eV)
AlN	6.14	3.112	4.982	AlGaN	0.7
GaN	3.42	3.189	5.185	InGaN	1.4
InN	0.64	3.545	5.703	InAlN	5.36‡

The band gaps and lattice constants of binary nitrides are listed in Table 1.1, while the band gaps and lattice constant of nitride semiconductors alloys are shown in Fig. 1.1, together with a comparison with other III-Vs. The band gaps E_g of $Al_xGa_{1-x}N$, $In_xGa_{1-x}N$ and $In_xAl_{1-x}N$ are not simply a linear interpolation between the band gaps of the two binary constituents, but are given by a more complex relationship involving a quadratic term:

$$E_{g,A_xB_{1-x}N} = xE_{g,AN} + (1-x)\,E_{g,BN} - b_{ABN}x\,(1-x) \tag{1.1}$$

Here A and B stand for Al, Ga or In, depending on the compound considered, and b is the so called bowing parameter. The values of b for ternary III-nitride alloys are given in Table 1.1. Concerning InAlN, the reported b values are somewhat scattered in the 5-6 eV range [14–17]. The value of 5.36 eV proposed by Sakalauskas *et al.* [14] is the one in best agreement with reported experimental values for the band gaps. However, as InAlN is the III-nitride alloy which spans the largest band gap range, a more accurate description is obtained by introducing a composition dependent bowing parameter [14]:

$$b_{InAlN}(x) = \frac{A}{1+Cx^2} \tag{1.2}$$

where $A = 6.43 \pm 0.12$ eV and $C = 1.21 \pm 0.14$ eV. Iliopoulos *et al.* [18] has introduced a different but closely related expression

$$b_{InAlN}(x) = \frac{A_1}{1+A_2x} \tag{1.3}$$

where $A_1 = 15.3 \pm 1.6$ eV and $A_2 = 4.81 \pm 0.95$ eV. The need for a composition dependent bowing parameter has been also pointed out by Schulz *et al.* [19] on the basis of tight-binding calculations.

A second distinctive feature of III-nitrides with respect to classical III-Vs is their crystal structure. III-nitrides adopt the wurtzite structure, which is the stable phase, whose main characteristics are the hexagonal symmetry and the lack of an inversion centre. The basic wurtzite cell is illustrated in Fig. 1.2. Classical III-Vs share instead the more symmetric, cubic zincblende structure. The a and c lattice constants describing the unit cell of binary III-nitrides are reported in Table 1.1. The lattice constants of the alloys can be easily obtained by linear

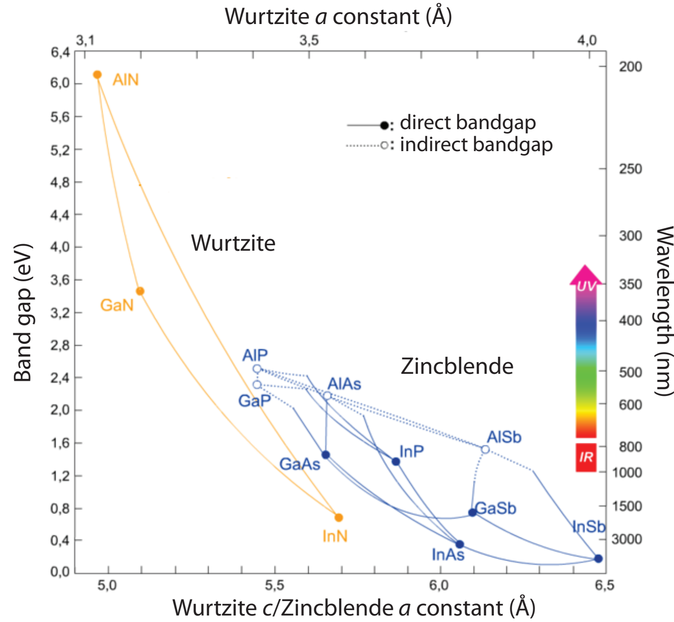

Figure 1.1: Band gap as a function of lattice constants for wurtzite III-nitrides (yellow symbols) and classical zincblende III-V semiconductors (blue symbols).

interpolation of the corresponding binary compounds, without the need of introducing any bowing parameter. As III-nitride devices and heterostructures are generally grown along the c-axis, the a lattice constant is the most meaningful one when considering heterostructures. A closer look to Fig. 1.1 reveals that the only ternary III-nitride semiconductor lattice-matched to GaN is InAlN. From the analysis of the lattice constants the lattice-matching (LM) condition is achieved for an In content of 17-18% [21]. AlGaN alloys and Al-rich InAlN (In$<$ 17%) have a lattice constants smaller than GaN, which implies that layers with such composition are subject to tensile stress when grown pseudomorphically on GaN. On the other hand, InGaN alloys and In-rich InAlN (In$>$ 17%) are subject to compressive stress when grown pseudomorphically on GaN. As we will see in the next paragraphs, the lattice-matched, strain-free condition of $In_{0.17}Al_{0.83}N/GaN$ heterostructures is one of their key advantages. Using the bowing parameter listed in Table 1.1 or the one from Eq. 1.2, we calculate a band gap of $\approx$ 4.5 eV for LM-InAlN, while Eq. 1.3 leads to a lower value of 4.0 eV. We will use the larger value, which has a better agreement with experimental data [14].

1.1.2 Spontaneous and piezoelectric polarization

One of the main consequences of the wurtzite structure, which is not isotropic, is that III-nitrides are strongly polar materials. The relatively low symmetry of the wurtzite structure gives rise to a spontaneous polarization, denoted hereafter P^{SP}, directed along the c-axis. The magnitude of the spontaneous polarization for the whole nitride family has been calculated

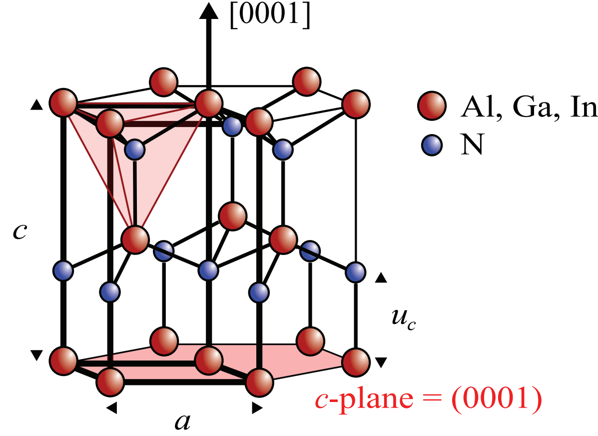

Figure 1.2: Wurtzite hexagonal unit cell. The *a* and *c* lattice constants are indicated, together with the *c*-axis direction and the basal *c*-plane. Image source: Wikipedia.

by Ambacher *et al.* [22] and is given by (in C/m^2):

$$\mathbf{P}^{SP}_{Al_xGa_{1-x}N} = [-0.090x - 0.034(1-x) + 0.021x(1-x)]\,\hat{z} \tag{1.4a}$$
$$\mathbf{P}^{SP}_{In_xGa_{1-x}N} = [-0.042x - 0.034(1-x) + 0.037x(1-x)]\,\hat{z} \tag{1.4b}$$
$$\mathbf{P}^{SP}_{In_xAl_{1-x}N} = [-0.042x - 0.090(1-x) + 0.070x(1-x)]\,\hat{z} \tag{1.4c}$$

where $\hat{z}$ is a unit vector aligned to the *c*-axis and oriented towards the [0001] direction, as shown in Fig. 1.2. The [0001] direction is commonly referred to as the Ga-polar direction, while the $[000\bar{1}]$ one is normally called the N-polar direction. When considering pseudomorphic heterostructures where one layer is under tensile or compressive stress, a piezoelectric component P^{PZ} has to be added to the polarization. This term comes from the fact that bond lengths are modified by the applied stress, and this in turn affects the polarization. The piezoelectric polarization term can take complicated forms depending on which kind of stress is applied to a layer. However, in this thesis we will consider exclusively the relatively simple case of heterostructures grown pseudomorphically on relaxed GaN along the *c*-axis with Ga-polarity. In this case, GaN has no piezoelectric polarization, while for the other nitrides P^{PZ} is given by (in C/m^2) [22]:

$$\mathbf{P}^{PZ}_{Al_xGa_{1-x}N} = [-0.0525x - 0.0282x(1-x)]\,\hat{z} \tag{1.5a}$$
$$\mathbf{P}^{PZ}_{In_xGa_{1-x}N} = [0.148x - 0.0424x(1-x)]\,\hat{z} \tag{1.5b}$$
$$\mathbf{P}^{PZ}_{In_xAl_{1-x}N} = [0.148x - 0.0525(1-x) + 0.0938x(1-x)]\,\hat{z} \tag{1.5c}$$

The total polarization $\mathbf{P} = \mathbf{P}^{SP} + \mathbf{P}^{PZ}$ for nitrides pseudomorphic to GaN is summarized in Fig. 1.3.

According to Maxwell's laws, a spatial variation of the polarization P is associated to a fixed

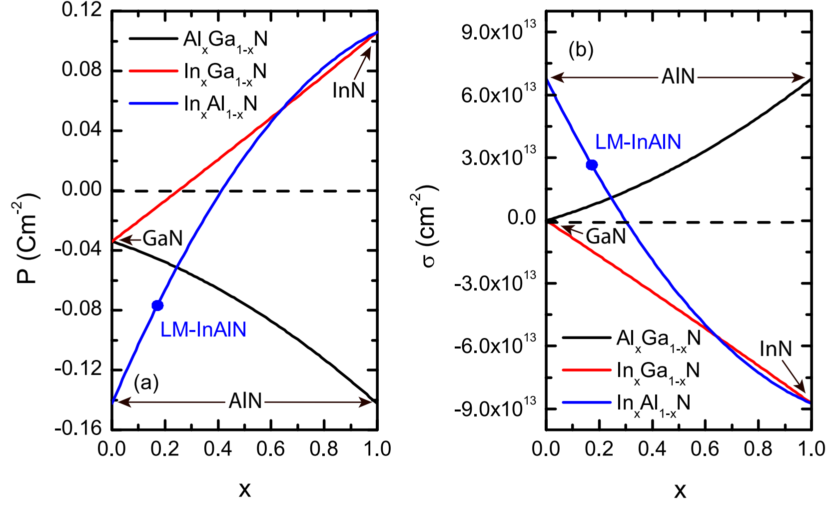

Figure 1.3: (a) Total polarization $\left(P^{SP}+P^{PZ}\right)$ for III-nitride materials grown pseudomorphically on Ga-polar *c*-plane GaN and (b) corresponding interface polarization charge density. Data from [22].

charge density ρ, given by the gradient of $\mathbf{P}$:

$$\rho = -\nabla \cdot \mathbf{P} \tag{1.6}$$

In heterostructures, the polarization undergoes abrupt variations at interfaces. As a consequence, interfaces between III-nitride materials are associated with a sheet density of fixed interface charges σ. For heterostructures grown along the Ga-polar direction, the magnitude of σ is simply given by the polarization difference ΔP between the two materials:

$$e\sigma = -\Delta P \tag{1.7}$$

The interface sheet charge density for III-nitride materials grown on GaN is summarized in Fig. 1.3.

1.2 Advantages of III-nitrides for electron devices

Among the large family of semiconductor materials, the nitrides have several peculiar features that make them of great interest for a variety of electronic applications where compact devices are required to efficiently handle high power levels. The wide band gap of GaN and III-nitride alloys makes the breakdown voltage of III-nitride based devices generally higher than analogous devices of the same size fabricated with Si or classical III-Vs. At the same time, with respect to other wide band gap materials like SiC, GaN is characterized by a higher saturation velocity, which means that parasitic resistances can be reduced, making the devices more energetically efficient. A final strength of III-nitride semiconductors is that they easily allow

Table 1.2: Room temperature material properties relevant for power performances and corresponding Baliga's and Johnson's figures of merit. Data from [23]. The figures of merit are normalized with respect to Si.

Material	E_g (eV)	ϵ_r	E_{BR} (MV/cm)	μ (cm^2/Vs)	$v_{sat}(cm/s)$	BFOM	JFOM
Si	1.1	11.8	0.3	1350	1.0×10^7	1	1
GaAs	1.42	13.1	0.4	8500	1.0×10^7	16	2.7
4H-SiC	3.26	10	3.0	700	2.0×10^7	440	20
GaN	3.39	9.0	3.3	1200	2.5×10^7	900	27.5
Diamond	5.5	5.5	5.6	1900	2.7×10^7	4250	50

for heterostructure based devices. Therefore, it is possible to play with band engineering for improving device performance, as for classical III-Vs, for example through the introduction of quantum wells (QW) or 2DEGs, while this is not possible for SiC or diamond based devices. As a consequence of their properties, GaN-based electron devices have found applications mainly in two fields: power electronics and microwave transistors.

In the field of power electronics, GaN has allowed the realization of devices with high breakdown voltage (V_{BR}) and very low specific ON-resistance (R_{ON}). While a high V_{BR} is required to the device handling high power densities, a low R_{ON} is necessary to minimize power dissipation in the ON-state. The figure of merit that best measures the potentials of a semiconductor for power electronics applications is the Baliga's figure of merit (BFOM) [24]:

$$BFOM = \epsilon\mu E_{BR}^3 \tag{1.8}$$

where ϵ is the semiconductor dielectric constant, μ the electron mobility in the drift region and E_{BR} the critical electric field for breakdown. As BFOM describes the best possible trade-off between V_{BR} and R_{ON}, an equivalent expression, more suitable for comparing real devices, is the following one:

$$BFOM = \frac{V_{BR}^2}{R_{ON}} \tag{1.9}$$

The theoretical BFOM for the principal semiconductors are listed in Table 1.2 and a summary of V_{BR} and R_{ON} data for published devices is presented in Fig. 1.4(a). From this it can be seen that both theoretically and practically, GaN based power devices largely surpass the limits of Si and have also outperformed SiC in terms of performance. For a given V_{BR}, GaN based devices offer reduced R_{ON} and thus lower dissipation. At present, high performance GaN based p-n diodes have been demonstrated with breakdown voltages as high as 3.7 kV [25], and GaN based vertical transistors with low specific on-resistance and breakdown voltage as high as 1.5 kV have been achieved [26]. This indicates that GaN holds great potential for low/medium-voltage power circuits and is being considered seriously for improving the effciency of DC-DC converters [27], LED [28] and motor [29] drivers, etc.

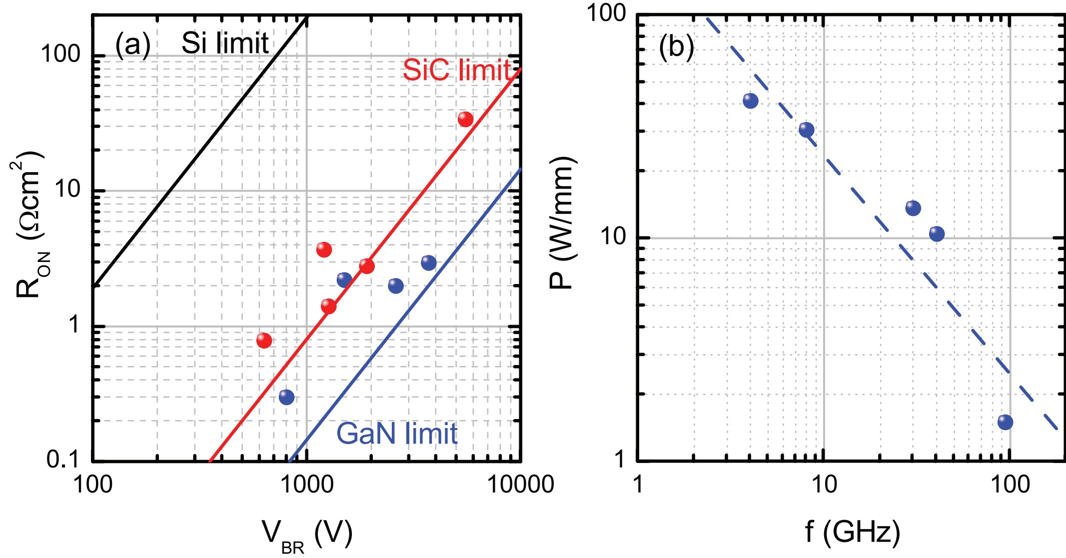

Figure 1.4: (a) Dots: specific ON-resistance vs breakdown voltage for SiC (data from [30–33]) and GaN devices (data from [25, 26, 28, 34]), lines: theoretical limits for Si, SiC and GaN. (b) Best reported output power density at various microwave frequencies for AlGaN/GaN HEMTs (data from [35–39]).

For microwave transistors, which are the subject of this thesis, GaN is an interesting material as it combines a high breakdown strength and at the same time a high saturation electron velocity. Analogously to power devices, a high breakdown voltage is fundamental for increasing the power density a transistor can handle. A high saturated electron velocity is instead advantageous to reduce the electron transit time under the gate electrode or across the base region, and therefore the switching time (Sec. 1.4.2). Combining these two features, GaN based microwave transistors and amplifiers hold the promise of delivering very high output power levels and at the same time high cutoff frequencies. The suitability of a material for power microwave applications can be measured by means of the Johnson's figure of merit (JFOM) [40]:

$$JFOM = \frac{E_{BR} v_{sat}}{2\pi} \tag{1.10}$$

where v_{sat} is the saturated electron velocity. JFOM quantifies the best trade-off between V_{BR} and device speed, which is quantified by the cutoff frequency f_t (see Sec. 1.4.2 for a definition of this parameter). Thus, an equivalent definition suitable for comparing devices is the following one:

$$JFOM = V_{BR} f_t \tag{1.11}$$

The JFOM for the principal semiconductors are listed in Table 1.2. It can be seen that GaN JFOM is ten times that of GaAs and is surpassed only by diamond. However, if we consider that diamond is not easy to dope and does not easily allow for heterostructures, GaN emerges

as the ultimate semiconductors for RF applications. GaN based high electron mobility heterostructures have been used for the realization of 2DEG based devices, in particular HEMTs, which have demonstrated in the last 15 years breakdown voltages much higher than III-V based HEMTs or bipolar transistors [23]. As a direct consequence, nitride based HEMTs have reached record power outputs and efficiencies, and are currently available on the market for RF systems requiring high power levels, like cellular base stations. Figure 1.4(b) summarizes the highest power levels reached by AlGaN/GaN HEMTs, which have been the workhorse for the GaN RF community in the past years. The physical basis of high electron mobility heterostructures and the state of the art of devices based on them will be clarified in the following paragraphs.

1.3 Polarization induced 2 dimensional electron gases

The presence of polarization induced interface charges has a strong impact on the band profile and charge distribution of III-nitride heterostructures. The strong electric fields induced by the charged planes can indeed be several MV/cm and are therefore responsible for strong band bending effects. This is exploited in high electron mobility heterostructures for creating a 2DEG at the interface. More in detail, a 2DEG can be formed by growing, along the c-axis, on top of GaN a barrier layer whose band gap is wider than the GaN one and whose polarization is such to induce a positive polarization charge at the interface. Suitable barrier materials are therefore AlGaN and InAlN with an In content <30% (Fig. 1.3(b)). The bands in the barrier region are bent by the polarization induced electric field and, if the barrier layer is thick enough, the GaN conduction band edge is pushed below the Fermi level. Electrons accumulate at the heterointerface as a consequence of electrostatic attraction. The confining potential is strong enough to make quantum confinement effects not negligible. This means that the 2DEG is best described as electrons occupying one or more subbands, whose wave function is strongly localized in the direction perpendicular to the heterointerface and delocalized in the directions parallel to the heterointerface. We will describe more in detail the wave function of 2DEG electrons in Appendix A. A second important point to stress is the fact that no doping is necessary for 2DEG formation, and this is one of the most important differences with respect to classical III-Vs based 2DEGs. The typical band profile of a nitride-based high electron mobility heterostructure is depicted in Fig. 1.5. In the following sections, we will explore the basic physical properties of 2DEGs.

1.3.1 Ungated 2 dimensional electron gas

The density of the 2DEG, n_s can be calculated from the following energy balance equation:

$$\Phi_B - eF_B d_B - \Delta E_c + (E_F - E_{bott}) = 0 \tag{1.12}$$

where Φ_B is the surface potential, e the electron charge, F_B the electric field in the barrier, d_B the thickness of the barrier, ΔE_c the conduction band offset at the heterointerface, E_F the

Fermi energy and E_{bott} the energy of the bottom of the GaN conduction band. Assuming that the electric field in the GaN channel vanishes far from the heterointerface, the application of the Gauss's theorem allows to calculate F_B:

$$F_B = \frac{e(\sigma - n_s)}{\epsilon_0 \epsilon_B} \tag{1.13}$$

where ϵ_0 is the vacuum permittivity and ϵ_B the barrier's relative permittivity. Concerning the $(E_F - E_{bott})$ term, it is useful to rewrite it as the sum of two physically distinct terms:

$$E_F - E_{bott} = (E_F - E_0) + (E_0 - E_{bott}) \tag{1.14}$$

where E_0 is the energy of the bottom of the first subband. If the 2DEG is not too dense, only the first subband is occupied and standard textbook formulas give [41]:

$$E_F - E_0 = \frac{\pi \hbar^2 n_s}{m_{GaN}} \tag{1.15}$$

where $\hbar$ is the reduced Planck's constant and $m_{GaN} = 0.2 m_0$ the GaN electron effective mass, whit m_0 the free electron mass. The precise evaluation of the $E_0 - E_{bott}$ term requires self-consistent quantum mechanical calculations. However, approximate values for this term can be obtained in the framework of the Fang-Howard approximation, which is treated in Appendix A:

$$E_0 - E_{bott} = \left(\frac{9\pi \hbar e^2 n_s}{8\epsilon_0 \epsilon_{GaN} \sqrt{8 m_{GaN}}} \right)^{2/3} \tag{1.16}$$

Plugging Eq. 1.16, 1.15, 1.14 and 1.13 into Eq. 1.12 gives an equation that can be solved numerically once Φ_B, ΔE_c, σ, ϵ_B are known and d_B is specified:

$$\Phi_B - \Delta E_c - \frac{e^2 \sigma d_B}{\epsilon_0 \epsilon_B} + \left(\frac{e^2 d_B}{\epsilon_0 \epsilon_B} + \frac{\pi \hbar^2}{m_{GaN}} \right) n_s + \left(\frac{9\pi \hbar e^2 n_s}{8\epsilon_0 \epsilon_{GaN} \sqrt{8 m_{GaN}}} \right)^{2/3} = 0 \tag{1.17}$$

From this last equation it can be seen that in order to have a non-vanishing n_s, the barrier thickness must exceed a critical value:

$$d_B > \frac{\epsilon_0 \epsilon_B (\Phi_B - \Delta E_c)}{e^2 \sigma} \tag{1.18}$$

while in the limiting case $d_B \to \infty$ we have $n_s \to \sigma$. Fig. 1.5 shows the barrier thickness dependence of n_s for several barrier materials. The curves shown have been obtained by numerically solving the band profile using the *nextnano* simulator [42] in order to accurately describe the high density cases, where not only the first subband is occupied. The material parameters used for the simulations have been taken from [22] for AlGaN/GaN heterostructures, while for LM-InAlN/GaN heterostructures we used the ones that are derived in Chapter 2. From Fig. 1.5 it can be seen that, as a rule of thumb, the highest the Al content in the barrier, the highest the 2DEG density and the lowest the minimum barrier thickness for 2DEG formation.

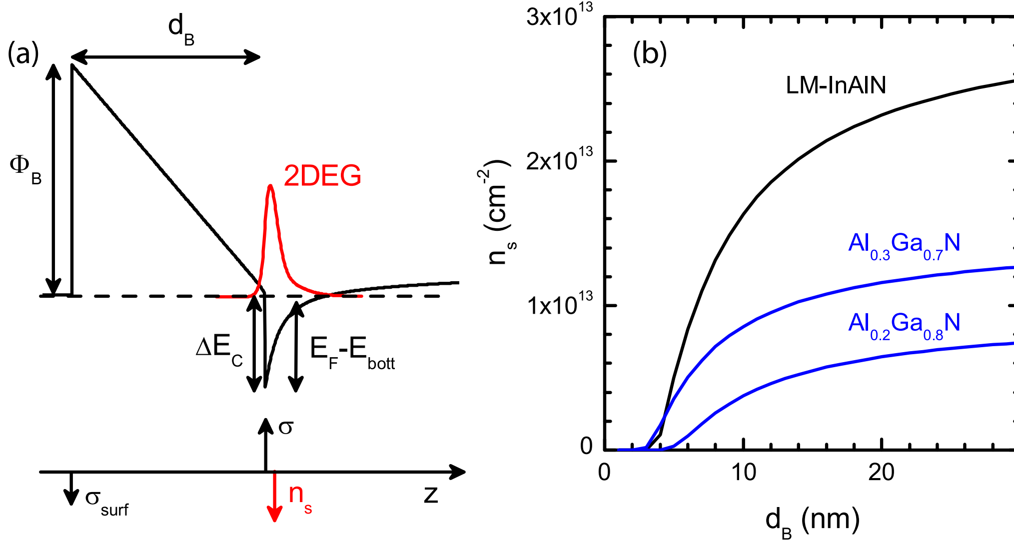

Figure 1.5: (a) Generic conduction band profile for a III-nitride based HEMT, together with the 2DEG density profile. (b) 2DEG density as a function of the barrier layer thickness d_B for LM-InAlN/GaN, $Al_{0.3}Ga_{0.7}N$/GaN and $Al_{0.2}Ga_{0.8}N$/GaN heterostructures.

The reduction of these surface related depletion effects in InAlN/GaN heterostructures with respect to AlGaN/GaN ones is one of the main strengths of InAlN.

1.3.2 Gated 2 dimensional electron gas

The 2DEG density in a high electron mobility heterostructure can be controlled not only with the composition and the thickness of the barrier layer, but can be also modulated electrically by applying an electric field across the barrier. This can be obtained by means of a Schottky contact or by forming a metal insulator semiconductor (MIS) structure and is one of the key features allowing to build field-effect transistors. When a potential difference V is applied across the barrier, the electric field in the barrier region is modified and this affects n_s. The equation governing the dependence of n_s on V can be obtained by slightly modifying Eq. 1.12:

$$\Phi_S - eV - eF_B d_B - \Delta E_c + (E_F - E_{bott}) = 0 \tag{1.19}$$

where Φ_S is the Schottky barrier and the $(E_F - E_{bott})$ term is calculated as in the previous paragraph. From this equation, it can be worked out that a positive voltage increases n_s, while a negative one depletes the 2DEG. A sufficiently negative voltage can cause complete depletion of the 2DEG. Using calculations similar to the ones of the previous paragraph, we

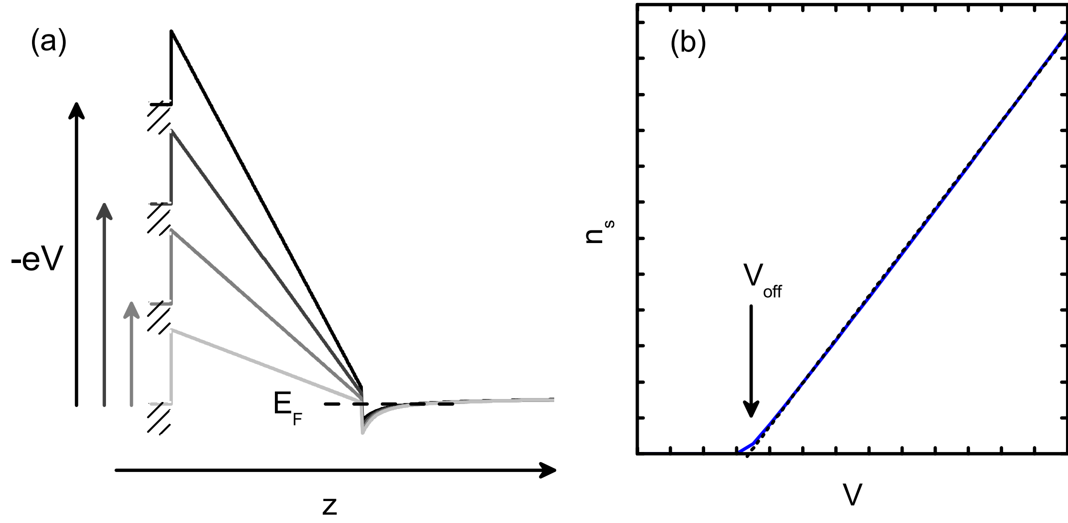

Figure 1.6: (a) Conduction band profile for a III-nitride based HEMT at equilibrium (light gray) and subject to different voltages (dark gray) (b) 2DEG density as a function of the applied bias. The blue line is a numerical calculation, while the dotted line represents the approximation of Eq. 1.21.

obtain the critical voltage for total 2DEG depletion, the so called pinch-off voltage, V_{off}:

$$V_{off} = \frac{1}{e}\left(\Phi_S - \Delta E_c - \frac{e^2 \sigma d_B}{\epsilon_0 \epsilon_B}\right) \tag{1.20}$$

For $V > V_{off}$, n_s can be quite accurately approximated as linearly dependent on V:

$$n_s = \left(\frac{e d_B}{\epsilon_0 \epsilon_B} + \frac{\pi \hbar^2}{m_{GaN}}\right)^{-1} \left(V - V_{off}\right) = \frac{1}{e} C_B \left(V - V_{off}\right) \tag{1.21}$$

where C_B is the specific barrier capacitance. The accuracy of this approximation can be checked in Fig. 1.6, where a numerical calculation of the voltage dependence of the 2DEG density is compared with the approximation of Eq. 1.21.

1.3.3 Transport properties of the 2 dimensional electron gas

In the previous section we have seen that an electric field perpendicular to the 2DEG plane modulates the 2DEG density. When the applied electric field is instead parallel to the 2DEG plane, an electric current is induced. If $F_{\parallel}$ is the longitudinal electric field and $v(F_{\parallel})$ the mean electron velocity induced by the field, the current density J is given by:

$$J = e n_s v(F_{\parallel}) \tag{1.22}$$

The $v(F_{\parallel})$ relation for electrons in GaN is shown in Fig. 1.7. It can be seen that if the electric field is weak, $v(F)$ can be approximated with a linear relationship:

$$v(F_{\parallel}) = \mu F_{\parallel} \tag{1.23}$$

where μ is the electron drift mobility. The introduction of μ allows to define the sheet resistivity ρ_s of a 2DEG:

$$\rho_s = \frac{1}{e n_s \mu} \tag{1.24}$$

μ is one of the most important parameters describing the transport properties of a 2DEG and in general of a conductor. For transistor applications, high electron mobilities are desired in order to reduce parasitic resistances and the transition time under the gate electrode (see Sec. 1.4.2). The main interest of 2DEGs comes from the fact that they allow high carrier densities and high electron mobilities at the same time. In bulk semiconductors, doping is the only way to control the conductivity. Thus, as ionized dopants are scatterers, their presence decreases the low-field electron mobility. Therefore, in bulk semiconductors the carrier mobility gets low at high carrier densities. If the mobile carriers are however spatially separated from ionized impurities, like in 2DEGs, the mobility remains high even at high carrier densities. The very high carrier densities achievable in 2DEGs has the additional advantage of screening very effectively any other scattering mechanism coming from charged centers, for example dislocations, increasing further the mobility. Electron mobilities much higher than the best bulk mobilities are currently achievable in 2DEGs [43]. In the case of III-nitrides, the best electron mobilities for bulk GaN are, at room temperature, ~ 1200 cm^2/V·s [34, 44], while GaN based 2DEGs can easily have room temperature mobilities > 1500 cm^2/V·s, with best values in the 2200 cm^2/V·s range [45]. 2DEGs are however subject to scattering mechanisms that are not present in bulk semiconductors, like interface roughness scattering, that if not properly managed can act as a major limiting factor [43]. There are finally several scattering mechanisms that are common to both bulk semiconductors and 2DEGs. These are mainly phonon related scattering mechanisms. In particular, optical phonon scattering is by far the most important phonon related scattering mechanisms in III-nitride based systems and becomes the mobility limiting factor above room temperature. In Sec. 2.2 we will describe in detail the various scattering mechanisms that determine the electron mobility in InAlN/GaN based 2DEGs, we will analyze their temperature dependence and their relative strength.

The temperature dependence of the electron mobility of 2DEGs is also quite different from bulk semiconductors. In bulk semiconductors, the temperature dependence of the mobility is determined essentially by charged impurity scattering and optical phonon scattering. Charged impurity scattering is very strong at low temperature and becomes weaker as the temperature raises. On the opposite, optical phonon scattering is negligible at low temperature and becomes more and more effective as temperature increases. The net effect is an electron mobility which is low both at high and low temperatures, with a maximum at intermediate temperatures [44, 47]. 2DEGs, on the other hand, suffer much less from charged impurity

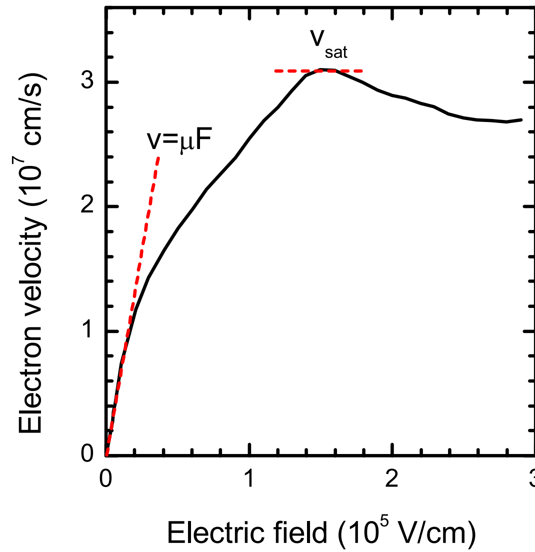

Figure 1.7: Electron velocity as a function of the applied electric field in bulk GaN at 10^{18} cm^{-3} doping level. The low field linear approximation leading to the definition of μ and the saturation velocity v_{sat} are highlighted. Data from [46].

scattering. Therefore, their electron mobility gets higher and higher as the temperature is lowered [43]. 2DEGs are thus highly conductive at low temperatures, which is a very distinctive feature with respect to bulk semiconductors. We will see examples of the temperature behavior of μ for InAlN/GaN based 2DEGs in Sec. 2.2.

While the low-field transport properties of 2DEGs are very different from bulk semiconductors, the high-field behavior is on the other hand the same. As the applied electric field is increased, the electron velocity starts to deviate from the linear behavior of Eq. 1.23 and increases in a sublinear way. This is due to the onset of other scattering mechanisms, for example phonon emission. At a certain electric field, v reaches a maximum, called saturation velocity (v_{sat}), and then decreases. The appearance of negative differential resistance at high fields is caused by the onset of scattering to other conduction band valleys [46].

The low-field electron mobilities and saturation electron velocities are compared in Table 1.2 for the principal bulk semiconductors. It can be seen that low band gap semiconductors are generally characterized by superior low-field transport properties, i.e. they have higher electron mobilities, which is related to the lower effective mass. Wide band gap semiconductors on the other hand have much higher saturation electron velocity. We will see in the next sections how μ and v_{sat} influence the performance in HEMTs.

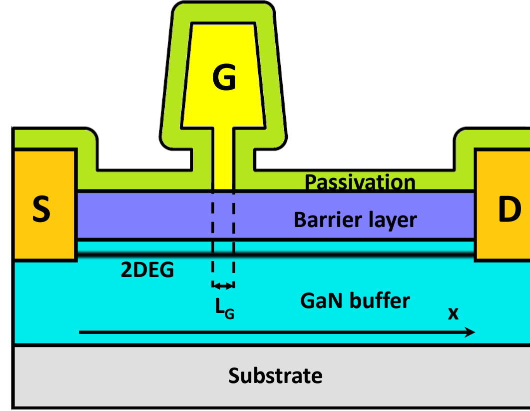

Figure 1.8: schematic cross section of a generic III-nitride based HEMT. S, D, and G stand for source, drain and gate contacts, respectively.

1.4 High electron mobility transistors

1.4.1 Static behavior

HEMTs are field effect devices based on a 2DEG as current channel. According to the general field effect transistor architecture, they are constituted by two ohmic contacts to the 2DEG, called the source and the drain contacts, and a Schottky contact, called the gate contact, placed in the source-drain spacing. A schematic drawing of an HEMT is shown in Fig 1.8. The role of the gate electrode is to control the current flowing between the source and drain electrodes through the 2DEG.

When a voltage V_{DS} is applied to the drain electrode with the source electrode grounded, a current I_{DS}, whose magnitude depends on the total resistivity of the 2DEG channel, flows between the two electrodes. The gate electrode, by acting on the 2DEG density below it, modulates the channel resistivity and thus I_{DS}. The $I_{DS} - V_{DS}$ characteristics, also known as the output characteristics, can be obtained by imposing the constant current condition along the channel at a given gate voltage V_{GS}. Let's call x the direction along the channel, $F(x)$ the position dependent longitudinal electric field, $n(x)$ the position dependent 2DEG density and μ the electron mobility. As we are interested only to understand the main features of the $I_{DS} - V_{DS}$ characteristic, we do not consider any field dependence of μ. We therefore have:

$$I_{DS} = Wen(x)F_{\parallel}(x)\mu \tag{1.25}$$

where W is the gate width. According to Eq. 1.21, $n(x)$ in the gate region can be expressed as a function of the channel potential $V(x)$:

$$n(x) = \frac{1}{e}C_B\left(V_{GS} - V(x) - V_{off}\right) \tag{1.26}$$

Considering that $F(x) = dV(x)/dx$, Eq. 1.25 can be rewritten in the following form:

$$I_{DS} = W\mu C_B \left(V_{GS} - V(x) - V_{off}\right) dV(x)/dx \tag{1.27}$$

Integrating this equation over the gate length, we finally obtain a relation between I_{DS} and V_{DS}:

$$I_{DS} = \frac{W\mu C_B}{2L_g}\left[\left(V_{GS} - V_{off}\right)^2 - \left(V_{GS} - V_{off} - V_{DS}\right)^2\right] \tag{1.28}$$

This equation is valid for $V_{DS} < V_{GS} - V_{off}$ and for $V_{GS} > V_{off}$, i.e. in the so-called linear regime. At $V_{DS} = V_{GS} - V_{off}$ the channel at the drain edge is fully depleted. For higher V_{DS} values, part of the channel gets depleted. In this case, the current does not increase further with V_{DS} and remains approximately constant. This is the saturation regime. Finally, for $V_{GS} < V_{off}$ the channel is completely depleted whatever V_{DS} and the device is in the pinch-off state. Based on these considerations, the output and transfer characteristics of the transistor can be worked out. The output characteristics describe the $I_{DS} - V_{DS}$ dependence at fixed V_{GS} and are shown in Fig. 1.9(a). The transfer characteristic describes on the other hand the $I_{DS} - V_{GS}$ dependence at a fixed V_{DS}, usually in the saturation regime, and is shown in Fig. 1.9(b). In ideal devices, where in the saturation regime V_{DS} has no effect on I_{DS}, a unique curve is sufficient. A third parameter of interest is the transconductance, g_m, defined as:

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=cst} \tag{1.29}$$

As for the output characteristic, what is usually represented is the V_{GS} dependence of g_m in the saturation regime (Fig. 1.9(b)). In an ideal HEMT, both I_{DS} and g_m increase indefinitely with V_{GS}. In real devices, however, several nonidealities contribute to modify the output and transfer characteristics.

A first effect comes from the fact that μ depends on the longitudinal electric field, in particular it decreases as the field increases (Fig. 1.7). This reduces the current the transistor can handle in the saturation regime. A second important effect comes from the presence of an access and an output region on the source and drain side of the gate, respectively. The resistance of these two regions, which is composed of the contact resistance and the resistance of the 2DEG portion connecting the source or drain electrode to the gate region, increases the on-resistance of the device. As a consequence, the saturation regime is reached for V_{DS} values higher than $V_{GS} - V_{off}$. Source and drain resistances induce furthermore a significant reduction of the saturation current, the effect becoming stronger with higher resistances.

A second important phenomenon in GaN based HEMTs is an increase of the access and output resistances with increasing current levels [48, 49]. This is due to the nonlinear velocity-field characteristic of GaN (Fig. 1.7), and its major consequence is a sublinear increase of I_{DS} with V_{GS}. The result is a transconductance having a peak and then decreases at high V_{GS} (Fig . 1.9(b)). V_{GS} is finally limited by the onset of forward conduction in the Schottky contact, which

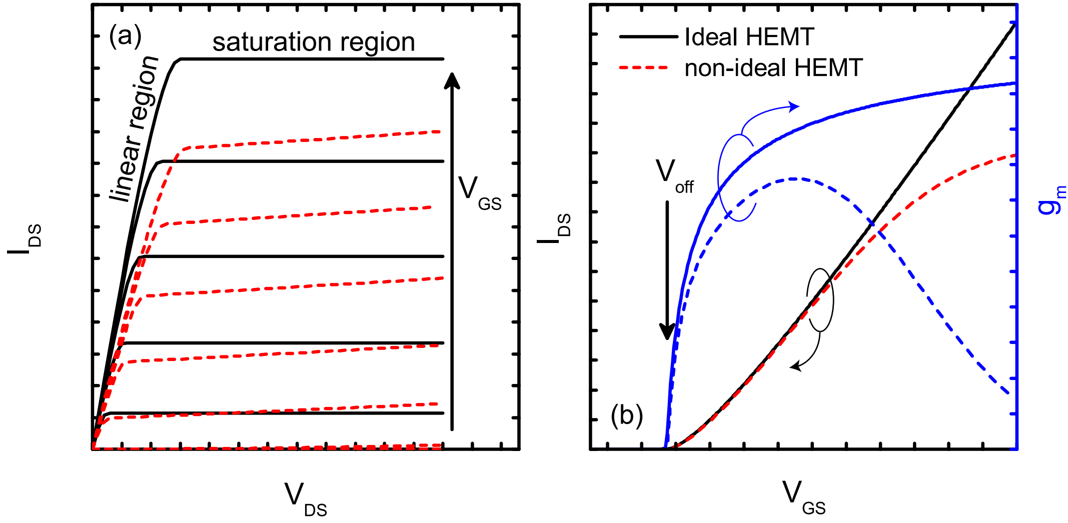

Figure 1.9: (a) Output and (b) transfer characteristics of ideal (continuous line) and real (dashed line) HEMTs. Panel (b) additionally shows the transconductance for the two devices.

usually takes place for $V_{GS} > 1$ V.

Short channel effects can be also very important causes of non-ideal behavior. If the gate does not have a very strong electrostatic control over the channel, the drain voltage can still strongly influence the drain-source current even in the saturation regime. This happens in particular when the gate to channel distance, i.e. the barrier thickness, is not negligible with respect to L_g. Short channel effects manifest themselves in the output characteristics as an increase of I_{DS} with increasing V_{DS} even in the saturation region, as shown in Fig. 1.9(a). Short-channel effects have a strong effect in the pinch-off region. At high V_{DS}, the gate can no longer block the current flow and a non-negligible I_{DS} can appear. Short channel effects can be therefore assimilated to a V_{DS} dependent V_{off} and are measured through the drain induced barrier lowering (DIBL) parameter:

$$DIBL = \frac{\partial V_{off}}{\partial V_{DS}} \tag{1.30}$$

In order to keep short channel effects to acceptable levels, L_g should be at least 5 times d_B or even more [50]. This imposes a limit to the scaling of the transistor dimensions. However, it is important to stress that the higher the power the transistor is tailored to operate at, the higher V_{DS} will be, strengthening short channel effects. Therefore, transistors for high power applications generally require longer gates to keep the DIBL low. We will see in Sec. 4.5 how to reduce short channel effects through the use of back-barriers.

Thermal effects can be also important. With increasing I_{DS} and V_{DS}, the transistor dissipates more and more power in the form of heat. If the heat is not evacuated efficiently, the device temperature increases significantly, reducing the electron mobility and thus I_{DS}. This phenomenon, known as self-heating, manifests as a decreasing I_{DS} with increasing V_{DS} in

the saturation region. It can be attenuated with a proper thermal management of the device. It is in particular important to grow the nitride stack on a substrate with high thermal conductivity. SiC substrates are the most suitable for this purpose, as they have a very high thermal conductivity of 390 W/mK. Sapphire, although being the most popular substrate for III-nitrides epitaxy, is characterized by a much lower thermal conductivity of 42 W/mK and cause therefore strong self-heating effects. Si has an intermediate thermal conductivity of 148 W/mK, but can be thinned much more easily than SiC to reduce the thermal resistance and its much lower cost makes it a very attractive substrate. Diamond is another possible substrate, theoretically the best from the thermal point of view, especially in its single crystalline form. However, diamond substrates are only available in very small size and are quite expensive. Furthermore, III-nitride epitaxy on diamond is quite challenging. Therefore, SiC is now the established substrate for high power applications, together with Si which is attracting more and more interest.

1.4.2 Dynamic behavior

We will now consider the dynamical properties of HEMTs, in particular their behavior as amplifiers. The most common configuration for HEMT based amplifiers is the common source one, where the source is grounded, the signal to be amplified is applied to the appropriately biased gate electrode and the amplified signal is collected by a load impedance at the appropriately biased drain electrode. For a sinusoidal signal applied to the gate, the drain current and voltage change over time in a sinusoidal way too, as shown in Fig. 1.10. In particular, the drain current and voltage follow the so called load line, which is determined by the load impedance and is generally elliptical, reducing to a line in the case of a purely resistive load, which is the case of Fig. 1.10(b). The transistor works as a current(power) amplifier if the current(power) of the outcoming signal is higher than the current(power) of the incoming signal. The ratio between current(power)of the output and incoming signals defines the gain. The frequency dependence of the current and power gain are among the most important parameters describing the transistor frequency performance.

The simplest way for understanding the evolution of the transistor properties with frequency is to start with its behavior under small signal conditions. In this case, the transistor behaves linearly and can be represented by an equivalent circuit, as shown in Fig. 1.11. The elements that constitute this relatively complicated circuit have in most cases a simple physical origin. So R_S and L_S are the resistance and inductance of the source electrode and access region. Analogously, R_D, R_G, L_D and L_G are the resistances and inductances of the drain and gate electrodes. C_{GS}, C_{GD} and C_{DS} are, respectively, the gate-source, gate-drain and drain source capacitances. R_{DS} is the drain-source resistance and is related to short channel effects and buffer conductivity. R_{GS} has a less evident physical origin, it has been introduced mainly for improving the agreement between the circuit model and experimental data. However, it induces minor corrections. Among all these components, the most important ones are by far g_m and C_{GS}. The other components are less important and can be considered as parasitic

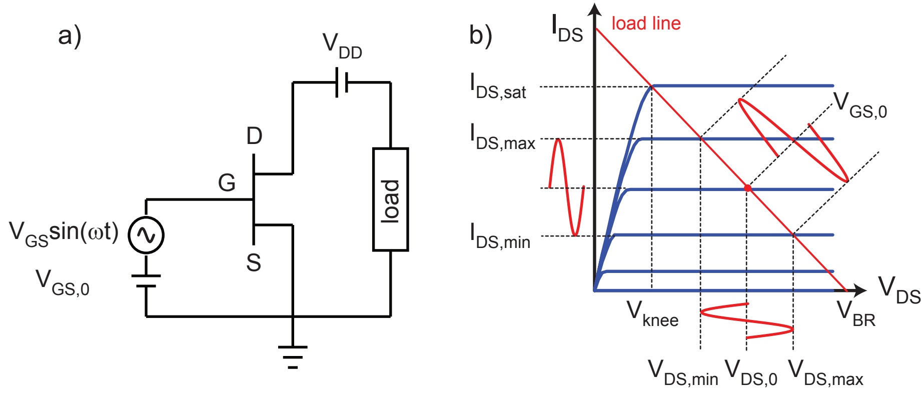

Figure 1.10: (a) Common source configuration for an HEMT based amplifier. (b) Corresponding loadline superposed on the HEMT's output characteristic. This graph shows the drain-source voltage and current evolution during a sinusoidal gate voltage sweep.

components. If these parasitic components are negligible, the current gain G_I can be easily worked out:

$$G_I = \frac{g_m}{2\pi f C_{GS}} \tag{1.31}$$

where f is the frequency. From this equation, we see that the current gain decreases with frequency. If expressed in dB, the gain is found to decrease at a rate of 20 dB/decade and becomes unity at the transition frequency f_t:

$$f_t = \frac{g_m}{2\pi C_{GS}} \tag{1.32}$$

Therefore, for $f > f_t$, the transistor no more amplifies the current. In the ideal case, all the gate-source capacitance is used to modulate the 2DEG electrons. If $\langle v_e \rangle$ is the mean electron velocity under the gate electrode, we have $g_m = C_{GS}\langle v_e \rangle L_g$. Writing now $\langle v_e \rangle = L_g/\tau$, where τ is the transit time for electrons under the gate, we obtain:

$$f_t = \frac{1}{2\pi\tau} \tag{1.33}$$

Therefore, the faster the electrons transit under the gate, the higher f_t will be. High f_t can be thus obtained by reducing L_g and by increasing the electric field under the gate so that electrons reach their saturation velocity. The highest possible value for f_t is therefore

$$f_{t,max} = \frac{v_{sat}}{2\pi L_g} \tag{1.34}$$

Considering that for GaN $v_{sat} = 2.5 \times 10^7$ cm/s, and taking 10 nm as the lower bound for L_g, transition frequencies in excess of 1 THz can be theoretically reached. In real devices, however, C_{GS} contains also fringing parasitic components that lower the g_m/C_{GS} ratio [51]. A second point is that the electron velocity can not be v_{sat} under the whole gate. Electrons enter the

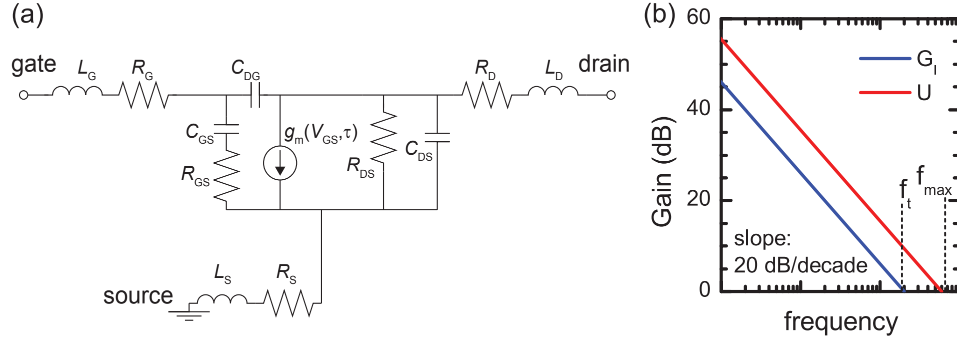

Figure 1.11: (a) Small signal equivalent circuit of an HEMT. (b) Frequency dependence of the current (G_I) and power (U) gain. The cutoff frequencies f_t and f_{max} are indicated.

gate at relatively low velocities and are accelerated to v_{sat} only at the right side of the gate. This further lowers the maximum value of f_t. Furthermore, the effect of the other parasitic elements is not completely negligible. An expression for f_t taking into account the parasitic components is the following one [52]:

$$f_t = \frac{g_m}{2\pi} \frac{1}{(C_{GS}+C_{GD}) + \left(\frac{R_S+R_D}{R_{DS}}\right)(C_{GS}+C_{GD}) + g_m C_{GD}(R_S+R_D)} \tag{1.35}$$

If not managed properly, parasitic components can have a significant impact on f_t, especially in deeply scaled transistors where the low L_g makes C_{GS} small, enhancing the effect of the parasitic source and drain resistances.

Regarding the power gain, the situation is more complicated as many definitions have been given for this parameter. The Mason's unilateral power gain U is the most commonly used and is defined as the power gain when the drain to gate feedback is suppressed. Its frequency behavior is not different from the current gain. It also decreases with frequency at a rate of 20 dB/decade and becomes equal to one at a frequency indicated as f_{max}. Therefore, as for the current gain, the higher f_{max} is, the higher the gain at a given frequency will be. However, f_{max} can be quite different from f_t [53]:

$$f_{max} = \frac{f_t}{2\sqrt{\frac{R_S+R_G+R_{GS}}{R_{DS}} + 2\pi f_t C_{GD} R_G}} \tag{1.36}$$

For power amplifier applications, f_{max} is more critical than f_t as amplifiers have to amplify power rather than current. In order to obtain a high f_{max}, it is required to have a high f_t and low parasitic resistances. In particular, the gate resistance R_G plays a major role and is usually minimized by using T-shaped gates (Fig. 1.8), where a small gate foot, necessary for high f_t, can be combined with a large gate head, which minimizes R_G.

In conclusion, good transistors for small signal regime applications are characterized by high cutoff frequencies, which is obtained with short electron transit times, low access and output

resistances and low gate resistances. The electron transit time is minimized by a high electron mobility and saturation velocity and at the same time a low L_g. Therefore, very thin barriers are required, as short channel effects limit the lowest possible L_g to $\sim 5d_B$. Low R_S and R_D can be obtained with low resistivity ohmic contacts and short source-to-gate and gate-to-drain distances. Low R_G are finally obtained with T-shaped gates. At present, the best reported values for f_t and f_{max} are 453 GHz and 554 GHz, respectively, obtained in AlN/GaN ultrascaled HEMTs (20 nm L_g) with self-aligned ohmic contacts [54].

Let's consider now the large signal behavior, which is the most relevant one if the transistor has to be integrated in a power amplifier. The situation is well described by Fig. 1.10. Increasing the input power, which is equivalent to increasing the gate voltage swing, has the consequence of increasing the drain voltage and current swing. Therefore, the output power increases linearly with the input power. However, the output power is limited. The maximum power is reached when the voltage swing at the gate is large enough to bring the device, during the same sweep, from pinch-off to the maximum possible drain-source current. If $V_{DS,max}$ and $V_{DS,min}$ are the maximum and minimum drain-source voltages reached during the sweep and $I_{DS,max}$ and $I_{DS,min}$ the maximum and minimum current attained during the sweep (Fig. 1.10), the output power is $P_{out} = \left(I_{DS,max} - I_{DS,min}\right)\left(V_{DS,max} - V_{DS,min}\right)/8$. The maximum possible power P_{max} is attained if the load impedance is such to make $V_{DS,min} = V_{knee}$ and $V_{DS,max} = V_{BR}$. Here, V_{knee} is the knee voltage, which is the drain voltage where I_{DS} starts saturating at its maximum possible value, and V_{BR} is the breakdown voltage. Therefore:

$$P_{max} = \frac{I_{DS,max}\left(V_{BR} - V_{knee}\right)}{8} \tag{1.37}$$

Therefore, a high output power can be attained if the breakdown voltage is high and if the ON-resistance is minimized in order to have a small V_{knee}. A high 2DEG density is also desirable because it translates in a high $I_{DS,max}$. It is important to stress the fact that V_{BR} depends critically on the transistor geometry. In particular, short gate lengths and short gate-drain distances reduce V_{BR} as a consequence of the increase of the peak electric field at the drain side of the gate. Thus, transistors designed for operation at high frequency can reach lower power densities if compared to the ones operating at lower frequencies. This is well illustrated in Fig. 1.4(b), where it can be clearly seen that the maximum power density achievable in AlGaN/GaN based HEMTs decreases as the frequency of operation gets higher.

The last parameter of interest for the characterization of high power transistors is the power added efficiency (PAE), which measures the efficiency of the transistor as an amplifier:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1.38}$$

where P_{in} and P_{out} are the input and output power, respectively, and P_{DC} is the DC power necessary for biasing the transistor at its work point. A high power gain is important for getting a high PAE because it is proportional to the $P_{out} - P_{in}$. The PAE increases also if $V_{DS,max}$ is high with respect to $V_{DS,min}$. Therefore, the higher the breakdown voltage and the lower the

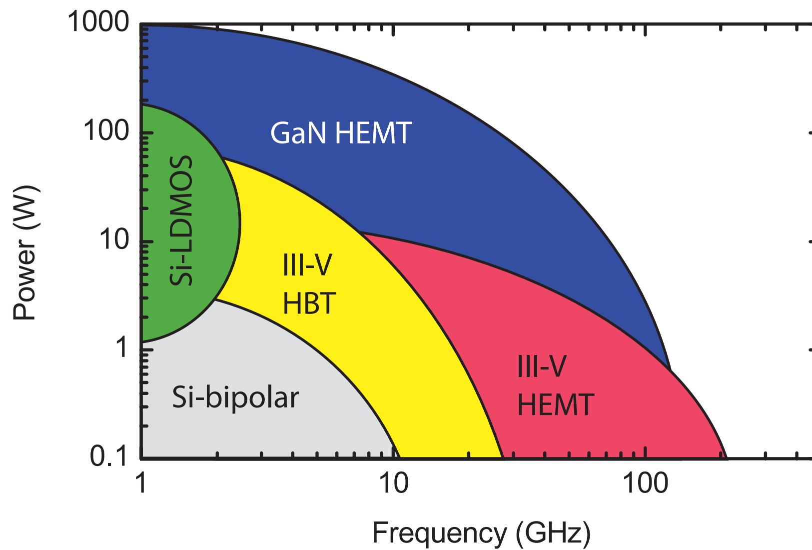

Figure 1.12: Power output as a function of frequency for different semiconductor technologies. GaN based HEMTs distinguish themselves for covering the whole microwave spectrum and for delivering higher power with respect to other semiconductors.

ON-resistance, the higher are the chances to obtain very high PAE. The limiting PAE is reached in the ideal case where the power gain is infinite and V_{knee} is zero, which gives maximum PAE ranging between 50% and 78.5% for class of operation A and B, respectively.

Summarizing, HEMTs for power amplifier applications at frequency f should have cutoff frequencies f_t and f_{max} well above f in order to guarantee a high gain. A high saturated current density, a high breakdown voltage and a low knee voltage (i.e. a low ON-resistance) are also required in order to reach a high power density and PAE. From these considerations, nitride based HEMTs emerge as the best candidates for microwaves and millimeter wave applications. As explained in the previous sections, they allow for higher breakdown voltages with respect to GaAs or Si based transistors as a consequence of their large band gap. The high 2DEG density of GaN based HEMTs allow furthermore to reach easily current densities > 1 A/mm. In the case of InAlN/GaN HEMTs, currents > 2 A/mm can been achieved [13], which is well above the limits of GaAs or InP based transistors. Furthermore, the high electron mobility of the 2DEG and the high v_{sat} of GaN allow for cutoff frequencies that vary, depending on the transistor geometry, in the 10-500 GHz range. Therefore, GaN based HEMTs can reach power densities far above those achievable in narrow band gap devices for the whole microwave range. Fig. 1.12 summarizes the power-frequency areas for the most important semiconductors, clearly showing how nitrides measure up against Si and classical III-Vs based technologies.

1.5 AlGaN/GaN HEMTs: state of the art and technological limits

AlGaN/GaN heterostructures have been the first GaN based high electron mobility heterostructures achieved [55] and are at present the best understood ones. AlGaN/GaN HEMTs are the

most developed GaN electron devices as they have been studied for 20 years. In this paragraph, we will analyze the state of the art of AlGaN/GaN technologies and will discuss their limitations.

We have seen in Sec. 1.3 that the higher the Al content in the AlGaN barrier, the higher the interface polarization charges are, which leads to higher 2DEG densities. At the same time, it is important to keep the thickness of the AlGaN barrier high enough to avoid surface related depletion effects (Fig. 1.5). However, AlGaN layers cannot be grown pseudomorphically on GaN for any composition and thickness. As can be inferred from Fig. 1.1 and Table 1.1, AlGaN can never be grown lattice matched on GaN: whatever its composition, it will always be under tensile strain. Therefore, AlGaN layers will accumulate strain energy as they are grown thicker and, above the so called critical thickness, part of this energy will be relaxed through the formation of dislocations. The higher the Al content of the AlGaN barrier, the lower the critical thickness. An obvious way of avoiding relaxation is to limit the AlGaN thickness below the critical thickness. However, as illustrated in Fig. 1.5, surface related depletion effects reduce the 2DEG density in thin barrier heterostructures. Therefore, a compromise has to be reached between barrier thickness and Al composition. In most cases, AlGaN/GaN heterostructures have Al compositions in the 20-30% range and barrier thicknesses ranging between 20 and 30 nm. Higher compositions and thicknesses lead to strain relaxation issues, while lower ones reduce too much the 2DEG density. This leads to n_s values ranging between $\sim 5 \times 10^{12}$ and $\sim 1 \times 10^{13}$ cm^{-2}. The room temperature electron mobility ranges between 1000 and 2500 cm^2/Vs, depending on the 2DEG density and on the heterostructure quality [43] (see Sec. 2.2 for a quantitative analysis of the electron mobility). As a consequence, apart some exceptional reports of record sheet resistivities below 200 Ω/□ [56, 57], the typical values for room temperature ρ_s lie in the 300-500 Ω/□ range [37, 43, 58–60].

Let's now consider AlGaN/GaN based HEMTs. The 2DEG densities achievable with AlGaN/GaN heterostructures translates in transistors with maximum current densities typically close to 1 A/mm [61]. Even ultra-scaled devices with self-aligned contacts cannot improve much on this value [62]. Transconductance values are generally well below 500 mS/mm. The barrier thickness, on the other hand, constitutes a limit to the scaling of the transistor. In order to avoid strong short-channel effects, the gate length is tipically limited to ~ 100 nm, which in turn sets a limit on f_t. A method to overcome this limitations is to perform a gate recess, i.e. to remove part of the AlGaN barrier in the gate region before depositing the gate electrode. Gate recessed HEMTs benefit therefore from a short gate to channel separation without the need of thin barriers, which prevents a deleterious increase of the access and output resistances. Gate recessing has allowed AlGaN/GaN HEMTs to implement sub-100 nm gate lengths and to reach cutoff frequencies beyond 100 GHz. Examples of record cutoff frequencies obtained with this technique are f_t/f_{max} of 130/170 GHz [37], 225/120 GHz [63], and 70/300 GHz [45]. However, gate recessing involves many challenges. As wet chemical etching methods are not available for III-nitrides, dry etching techniques have to be used. Removing a few nm of material by dry etching in a reproducible and uniform way is a tough task [64]. Additionally, the process can introduce trapping centers and implant charged ions in the gate region [65]. In conclusion,

AlGaN/GaN HEMTs are perfectly suitable for applications up to ~ 40 GHz, where gate recessing is not strictly necessary. Gate recessed AlGaN/GaN HEMTs have shown nevertheless high power densities and efficiencies up to 100 GHz. However, for such high frequencies the need of gate recessing comes at the price of an increased technological complexity.

In the 1 to 40 GHz range, AlGaN/GaN HEMTs have demonstrated very high power densities, well above 1 W/mm, reaching in some case very impressive values like 40 W/mm at 4 GHz [36] or 30 W/mm at 8 GHz [35]. These remarkable results have been obtained thanks to the implementation of field plates for electric field management, which have allowed to bias the transistors at voltages as high as 135 V [36], demonstrating the great power handling capabilities of GaN based HEMTs. With increasing frequency, however, the maximum power achievable decreases due to inevitable breakdown voltage lowering associated to device downscaling. Thus, the best power density achieved is 10.5 W/mm at 40 GHz [37] and 1.5 W/mm at 94 GHz [39]. The maximum power densities achieved in AlGaN/GaN HEMTs are summarized as a function of frequency in Fig. 1.4. High power added effciencies have been also obtained, especially at low frequency where biasing at very high voltages is possible. Up to 10 GHz, PAE values are in most cases above 40%, and record devices with PAE of 60% have been reported [23]. With increasing frequency, the lower bias voltages are associated to lower PAE. Thus, the best reported PAE at 40 GHz is 33% [37], reducing to 24% at 94 GHz [39]. These excellent results have proved that GaN based HEMTs surpass any other solid state based microwave technology in terms of power density and efficiency.

The high performances of AlGaN/GaN HEMTs have pushed the developement of monolithic microwave integrated circuits (MMICs) integrating them as active devices. In particular, compact and efficient power amplifiers have been successfully developed up to 100 GHz with high output power [23, 66]. Results are especially impressive at low frequencies. For example, an outstanding power-efficiency combination of 550 W and 66% has been obtained at 3.45 GHz [67]. This and other results have highlighted GaN based amplifiers as very attractive candidates for replacing Si laterally diffused metal oxide semiconductor based amplifiers in cellular and Wi-Max architectures. AlGaN/GaN based amplifiers are at present a rather mature technology and constitute the state of the art for a large part of the microwave spectrum. However, their application to millimeter wave technologies, which span the 30 to 300 GHz range, is challenging and other GaN-based technologies are emerging that allow for an easier downscaling of the transistor gate length. InAlN/GaN HEMTs are the most promising for this purpose. Their advantages are illustrated in the following section.

1.6 InAlN/GaN HEMTs: beyond AlGaN/GaN HEMTs limits

1.6.1 State of the art of InAlN/GaN HEMT technologies

InAlN/GaN based HEMTs have been proposed for the first time by Kuzmík in 2001 [7] and high quality InAlN/GaN 2DEGs have been realized experimentally for the first time by Gonschorek

et al. in 2006 [68]. With respect to AlGaN, LM-InAlN presents two major advantages. The first one comes from its lattice matching condition with GaN, which eliminates strain related issues in the growth of InAlN/GaN heterostructures. Secondly, interface polarization charges in LM-InAlN are 2 to 3 times higher than in typical AlGaN/GaN heterostructures (Eq. 1.5 and Fig. 1.3). Therefore, InAlN/GaN heterostructures can reach 2DEG densities well above the ones available in their AlGaN/GaN counterparts. 2DEG densities $> 2 \times 10^{13}$ cm^{-2} are indeed currently reported [69]. The consequences of such high n_s values are sheet resistivities in the $200 - 300\ \Omega/\square$ range, i.e. well below those typically achievable in AlGaN/GaN based 2DEGs. A close look to Fig. 1.5 shows also that high n_s values can be obtained even in heterostructures with extremely thin barriers. For example, $n_s > 10^{13}$ cm^{-2} can be obtained with InAlN barrier thicknesses as low as 5 nm. For similar thicknesses, AlGaN/GaN heterostructures can only provide 2DEG densities $< 5 \times 10^{12}$ cm^{-2}.

The fact that InAlN/GaN heterostructures can provide 2DEGs with high density even with very thin barriers provides two major advantages. First, the high n_s means that InAlN/GaN based HEMTs can reach current levels which largely surpass those achievable in AlGaN/GaN HEMTs. Current densities exceeding 2 A/mm have been indeed rapidly obtained since their introduction and values approaching 3 A/mm have been also reported [9]. Therefore, InAlN/-GaN HEMTs have the chance of providing higher power densities with respect to AlGaN/GaN HEMTs, if comparable breakdown voltages can be attained. The second advantage is related to the barrier thickness. In InAlN/GaN HEMTs, sub-10 nm barriers are still able to provide high current densities, therefore downscaling the transistor dimensions is easier with respect to AlGaN/GaN case. In particular, shorter gate lenths and higher cutoff frequencies can be reached without the need of a gate recess. Fig. 1.13 summarizes the reported cutoff frequencies of InAlN/GaN HEMTs as a function of the gate length. It can be seen that both f_t and f_{max} have exceeded 300 GHz and f_t as high as 400 GHz has been obtained. These values are well above those achieved with AlGaN/GaN technologies. Therefore, InAlN/GaN HEMTs are ideal candidates for the fabrication of GaN-based millimeter wave power amplifiers in the 30-300 GHz range. Chapter 5 of this thesis will present several examples of InAlN/GaN based power HEMTs operating in this frequency range.

Another point worth discussing concerns reliability issues. Nitride materials display the reverse piezoelectric effect, i.e. a strain is generated in the barrier when an electric field is applied. In AlGaN/GaN HEMTs, this adds to the already significant strain resulting from the lattice mismatch of the AlGaN barrier with respect to the GaN buffer. The most critical point is the drain side edge of the gate, which is subjected to the highest electric fields. Here, at high voltage operation, the stress can become so high to trigger the formation of defects, in particular microcracks [5, 6]. In LM-InAlN/GaN HEMTs, the absence of built in strain makes reverse piezoelectric effects less critical. Therefore, LM-InAlN/GaN HEMTs may provide improved reliability [10].

A last very interesting feature of InAlN/GaN heterostructures is their high stability at high temperatures. Since the beginning of their development, InAlN/GaN based HEMTs have

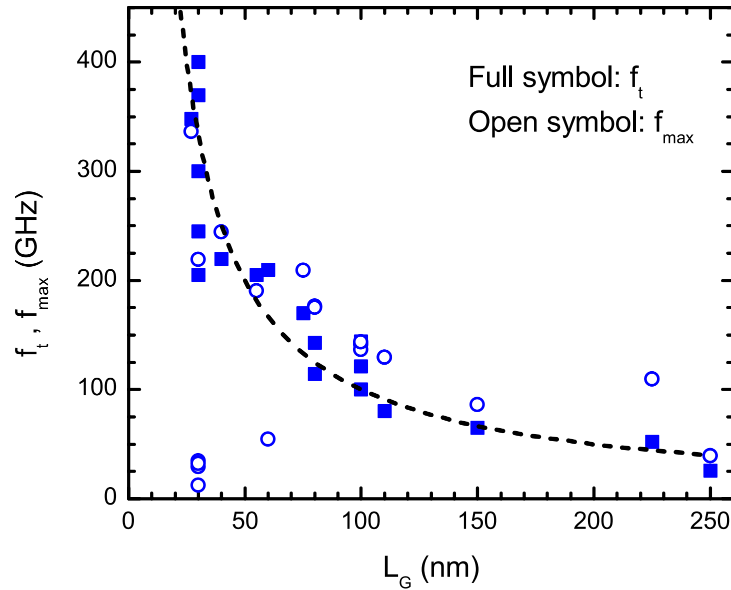

Figure 1.13: Published f_t (full symbols) and f_{max} (open symbols) values for InAlN/GaN HEMTs. Data from [8, 13, 51, 70–85].

proven a formidable resistance to high temperatures. It has been reported that such transistor can be operated in vacuum without permanent damage at temperatures as high as 1000°C [9], which is a temperature far above the maximum temperature sustainable by any other known semiconductor technology [11]. The very high thermal stability of these heterostructures can be attributed to the high Al content of the barrier and to their strain-free condition. This opens up new interesting applications of InAlN/GaN HEMTs. Besides millimeter-wave technologies, the fields of high temperature electronics and harsh environment sensing may significantly benefit from InAlN/GaN heterostructures [86]. However, before this thesis most of the work about the thermal stability of InAlN/GaN HEMTs concerned experiments performed in vacuum [9, 86–88]. Chapter 4 will present the key elements needed to extend the exceptional stability of these heterostructures to more realistic conditions.

1.6.2 Issues of InAlN/GaN HEMTs

Despite the extraordinary opportunities offered by InAlN/GaN HEMTs, these devices suffer from several issues that is necessary to address to make this technology really compelling for high frequency microwave applications. These include gate leakage currents, short channel effects, poor breakdown and dispersion effects.

Gate leakage currents are parasitic currents originating from the gate electrode. In ideal devices such currents should be completely absent. Gate leakage currents are particularly strong in InAlN/GaN HEMTs [12]. They can indeed be higher that 1 mA/mm even at relatively low drain-source voltages [89]. The presence of such high leakage currents strongly degrades

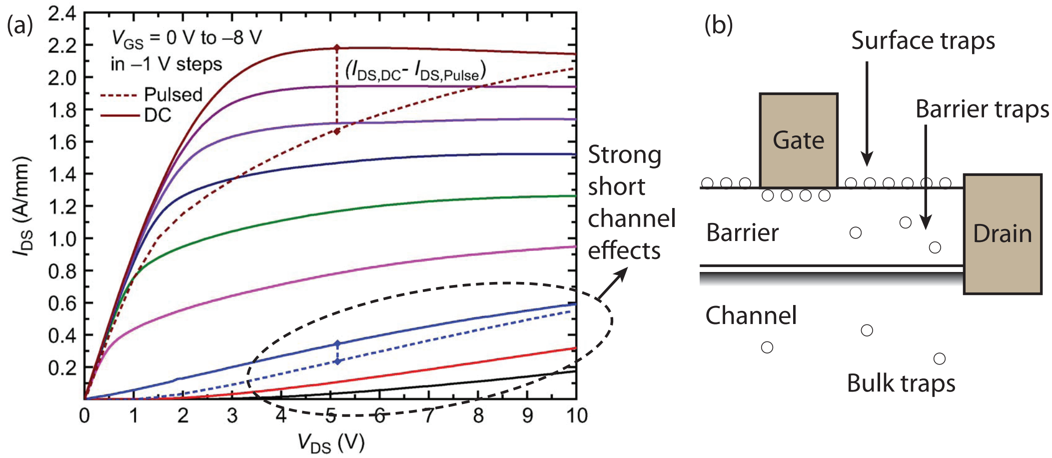

Figure 1.14: (a) Output characteristics of an InAlN/GaN HEMT with 30 nm gate length. Short channel effects are clearly observed for $V_{DS} > 4$ V. The dotted lines are obtained from pulsed measurements and show the importance of dispersion effects. The data are taken form Ref. [13]. (b) Schematic representation of trap distribution in GaN based HEMTs.

the off-state of the transistor, reduces the ON/OFF current ratio and can induce premature breakdown of the device. The most effective way to reduce gate leakage currents is to introduce an insulating layer between the InAlN barrier and the Schottky metal, thus implementing a metal-insulator-semiconductor HEMT (MIS-HEMT) structure. Several oxides have been tested, including Al_2O_3 [90], HfO_2 [91], ZrO_2 [91, 92] and $GdScO_3$ [93]. This approach has proven to be very effective and has allowed $> 10^4$ parasitic leakage reduction. However, the insertion of an insulating layer between the barrier and the gate metal inevitably increases the gate-to-channel separation, enhancing short channel effects. This solution is thus well suited for long gate length devices, but not for deep sub-μm HEMTs intended for high-frequency operation. An alternative and very interesting method to produce InAlN/GaN based MIS-HEMTs consists in oxidizing selectively under the gate region part of the InAlN barrier, which is converted to Al_xO_y [89]. This method has the advantage of decreasing significantly leakage currents without increasing gate-channel separation. However, the threshold voltage of the transistor is modified by the oxydation. A low leakage Schottky contact would be preferrable, as it would be associated with the lowest short channel effects and to a simpler fabrication process. In order to reduce these currents, however, it is important to well understand the origin of the conduction mechanisms. This topic has been deeply investigated during this thesis work and the results are presented in Sec. 4.3.

Short channel effects are a second important factor responsible for the degradation of the OFF-state of InAlN/GaN HEMTs. They are responsible in particular for the onset of parasitic conduction through the buffer at high source-drain voltages (Sec. 1.4.1). Short channel effects are not related directly to InAlN materials issues, but rather to a non optimal 2DEG confinement and management of the electric fields in the gate region. A clear example of the strength of short channel effects in short gate length InAlN/GaN HEMTs is given by Fig. 1.14(a).

Increasing the 2DEG confinement has proven very effective in reducing short channel effects in AlGaN/GaN HEMTs. This could be obtained in particular by introducing a back barrier, which avoids 2D electrons to spill out from the quantum well under high voltage operation. Two types of back barriers have been investigated: the InGaN QW [94] and the low Al content AlGaN buffer (x_{Al} < 10%) [95]. The implementation of back-barriers in InAlN/GaN HEMTs will be discussed in detail in Sec. 4.5, together with a discussion of the physical principles behind them.

Dispersion effects are another major issue of InAlN/GaN HEMTs. They originate from the presence of an high density of traps located at or near the surface of the heterostructure, which is a general feature of GaN based HEMTs (Fig. 1.14 (b)). As a consequence of the high fields in the gate region, which can become very strong under high bias operation, these traps can be populated with electrons and become charged. Once charged, the traps act as a "virtual gate" wich has a slow response time due to the relatively long emission time τ of the traps [96]. Under high frequency modulation, i.e. when $f \gg \tau^{-1}$, this "virtual gate" cannot follow the AC modulation and remains permanently charged. The available 2DEG density in the gate region is thus reduced as well as I_{DS}. For this reason, dispersion effects are also referred to as current collapse. Their effect tends to increase with increasing drain voltage as a consequence of the higher electric field strength. Dispersion phenomena are usually evidenced by means of pulsed measurements. In these measurements, the transistor is biased at a quiscent point in the OFF-state, with $V_{GS} < V_{off}$ and relatively high V_{DS}, and then is suddenly passed to a second bias point for a very short time and the current is measured. The measurement is then repeated until the output characteristics are fully represented. As the pulse duration is very short, the output characteristics obtained are representative of the trap filling state corresponding to the quiescent bias. An example of such measurement is given in Fig. 1.14 (a), where the dotted lines correspond to the output characteristics measured in the pulsed mode. The decrease in source-drain current due to the "virtual gate" effect is well visible. Dispersion effects are especially deleterious for large signal operation, since they indeed increase V_{knee} and reduce $I_{DS,max}$. The direct consequence is a lower maximum output power and power added efficiency. In order to suppress the very strong dispersion effects related to surface traps, a passivation of the heterostructure surface with SiN has proved to be a very effective solution [97]. Usually, the SiN passivation is deposited at the end of the HEMT fabrication process by plasma enhanced chemical vapor deposition (PECVD). Other *ex situ* deposition techniques have been investigated, for example catalitic chemical vapor deposition [98], as well as the *in situ* deposition of the SiN passivation immediately after the growth of the heterostructure [99]. Others materials have been also tested, for example SiO_2 [100] and Al_2O_3 [101]. While a considerable amount of work has been done in this sense for AlGaN/GaN HEMTs, much less ha been done for InAlN/GaN HEMTs. In Sec. 4.4 we will study the possibility of achieving *in situ* passivated InAlN/GaN heterostructures. However, surface traps are not however the only possible sources of dispersion. Traps located in the barrier as well as in the GaN channel may play a significant role [102]. The understanding of the different traps in InAlN based heterostructures is therefore important in this sense. Results

concerning this topic will be presented in Sec. 2.4.

2 Physics of InAlN/GaN heterostructures

This chapter treats the main physical properties of InAlN/GaN heterostructures. After a brief description of the experimental techniques necessary for the measurements, we will treat the topic of InAlN/GaN 2DEG mobility in Sec. 2.2. The theory used for mobility modeling will be described and then used for the modeling of experimental data. The main scattering mechanisms limiting the mobility will be discussed. Sec. 2.3 will deal with the experimental determination of several critical InAlN related physical parameters. These parameters will then be used for the modeling, via Schrödinger-Poisson calculations, the band profile of InAlN/GaN heterostructures. Finally, Sec. 2.4 will treat the topic of deep levels in InAlN. By means of admittance spectroscopy and photocapacitance spectroscopy techniques, we will show the existence of several deep levels in InAlN. The ensemble of the results presented in this chapter constitute the basis for the understanding of a number of different phenomena described in the following chapters.

2.1 Experimental techniques

2.1.1 Measurement of transport properties

The transport properties of interest for InAlN/GaNheterostructures are the density n_s, the mobility μ and the resitivity ρ_s of the 2DEG. These quantities are obtained by means of standard van der Pauw and Hall measurements. The van der Pauw method is a 4-point measurement technique which allows the extraction of the sheet resistivity of the sample under test [103]. The measurement are generally performed on an approximatively square sample, which is contacted at four points over its periphery as shown in Fig. 2.1(a). The measurement principle consists in injecting a certain current between two adjacent electrodes, and measuring at the same time the voltage between the remaining two electrodes. From these values, a resistance is calculated. This is repeated over the four possible permutations of this configuration, and from the four resistances the sample's sheet resistance is finally calculated. The van der Pauw method, being a 4-point technique, is not sensitive to the contact resistance. Accurate results can be thus obtained without the need of complex processing techniques for

low resistivity Ohmic contact fabrication.

Hall effect measurements can be performed at the same time of van der Pauw measurements if a magnetic field is applied to the sample in the direction perpendicular to its surface [104]. The measurement consists in injecting a current between two opposite contacts and measuring the voltage induced between the two other contacts by the magnetic field. The direct output of Hall effect measurements is the Hall coefficient R_H:

$$R_H = -\frac{r_H d_0}{e n_s} \tag{2.1}$$

where d_0 is the unit thickness (usually 1 cm) and r_H is the Hall factor, which depends on the main scattering mechanism limiting the 2DEG mobility. r_H is thus not a constant but varies from case to case. However, it is generally only slightly higher than 1, so that $r_H = 1$ is generally a very good approximation. It must be beared in mind that the Hall carrier density obtained in this way, n_H, is slightly lower than n_s. Once n_H is known and ρ_s has been determined via van der Pauw measurements, it is possible to calculate the Hall mobility μ_H:

$$\mu_H = \frac{1}{e n_H \rho_s} = r_H \mu_{drift} \tag{2.2}$$

μ_H is slightly higher than the drift mobility μ_{drift} as a consequence of the Hall factor. During this work, however, we have assumed $r_H = 1$, thus making no distinction between μ_H and μ_{drift}.

A further discrepancy between μ_{drift} and μ_H raises in the case where multiple subbands are occupied. In this case, if $r_H = 1$, we have [105]:

$$\mu_{drift} = \frac{\sum n_i \mu_i}{\sum n_i} \qquad \mu_H = \frac{\sum n_i \mu_i^2}{\sum n_i \mu_i} \tag{2.3}$$

Nevertheless, even in the case of large discrepancy between different subband mobilities, the difference between μ_{drift} and μ_H remains limited to a few percent. Therefore, μ_H can be always taken as a very good approximation of the real mobility, without the need of corrections.

For practical measurements, we used a PhysTech RH-2010 system equipped with an electromagnet generating a magnetic field of ±0.4 T. The system is also equipped with a closed cycle He cryostat operating in the 10-300 K temperature range, which allows to measure the temperature dependence of the transport properties.

2.1.2 Electrochemical capacitance-voltage

Electrochemical Capacitance-Voltage (ECV) is a useful technique for recording the Capacitance-Voltage characteristic of HEMT heterostructures without the need of processing Schottky diodes on them. In ECV, the Schottky contact is replaced by an electrolyte which wets the heterostructure surface. In order to perform the CV measurement, both the DC and AC bias

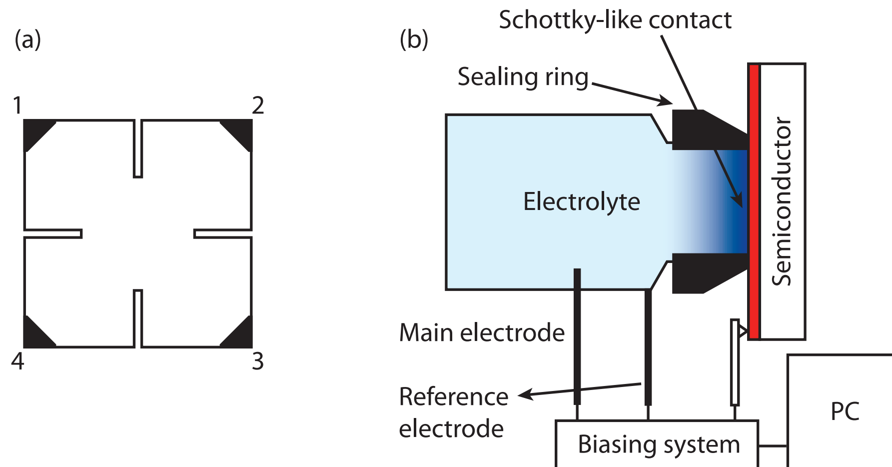

Figure 2.1: (a) Schematic representation of a sample for Hall effect measurements. The black corners represent the contacts and are numbered. (b) Schematic representation of the electrochemical Capacitance-Voltage setup.

are applied by means of an electrode. A schematic of an ECV setup is shown in Fig. 2.1(b). For more details about ECV techniques, we refer the reader to the review of Blood [106].

In this thesis, we used a Dage CVP21 system for ECV measurements, using a ~ 0.1% H_3PO_4 solution as electrolyte. The AC voltage frequencies are in the kHz range, and the system automatically eliminates the effect of series resistance by measuring the impedance at three different frequencies. This constitutes a great advantage with respect to conventional CV techniques, which are usually performed in the MHz range. There, the high frequencies used enhance the effect of series resistances, making the measurements less accurate.

2.1.3 Schottky diode fabrication on thick InAlN layers

A detailed description of InAlN based Schottky diodes fabrication process will be given in Sec. 4.1.1, where a thorough discussion of Ohmic and Schottky contacts will be undertaken. For the purpose of this chapters, it is sufficient to say that Schottky diodes on thick (≥ 100 nm) InAlN layers proceeds as follows. A mesa is first defined by optical lithography and Cl_2 based etching up to the GaN buffer, which is in these cases highly n-doped, contrary to HEMT heterostructures with thin InAlN barriers and semi-insulating buffers. A Ti/Al/Ni/Au stack is then deposited on the GaN buffer and annealed for 30 s at 850 °C under N_2 to form an ohmic contact. Finally, circular Ni/Au Schottky contacts with diameters ranging between 50 μm and 400 μm are evaporated on top of the InAlN layer, thus completing the diode fabrication.

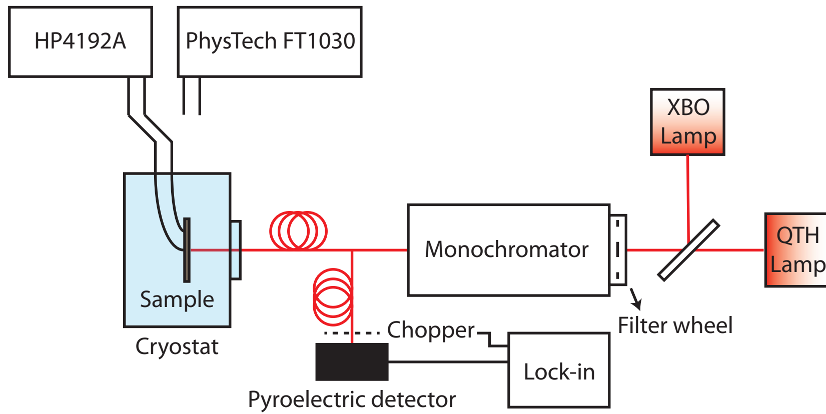

Figure 2.2: Schematic representation of the photocapacitance setup.

2.1.4 Photocapacitance spectroscopy

Photocapacitance spectroscopy is a technique aimed to the characterization of deep levels in semiconductors by means of light induced capacitance transients. In this work, a home made setup [107] was used, shown in Fig. 2.2. The system is equipped with two light sources. A 100 W quartz tungsten halogen (QTH) lamp is used for photon energies < 2 eV, while a 75 W Xe high pressure lamp (XBO lamp) is used for higher energies. Monochromatic light is generated by a Cornerstone 260 1/4m monochromator equipped with three gratings. Five appropriate long-pass filters mounted on a filter wheel block the higher orders diffractions of the monochromator. About 10% of the monochromatic beam is sent to a pyroelectric detector in order to measure the beam power, while the rest is sent via an optical fiber bundle to the sample, which is mounted in a closed cycle He cryostat in the 10-300 K temperature range. The cryostat is equipped of a Suprasil windows for high transmission both in the UV and IR parts of the spectrum. The sample is a Schottky diode illuminated from the back through the sapphire substrate. A focusing microscope objective allows to obtain a 500 μm illuminating spot. The Schottky diode can be electrically connected either to an HP 4192A LF impedance analyzer, either to the transient recorder of a PhysTech FT1030 DLTS system. The former is used for steady state photocapacitance measurements, where long transients have to be measured and a high time resolution is not necessary ($\Delta t = 2$ s). The latter offers on the other hand a very high time resolution and is adopted for optical cross section measurements.

2.2 Electron mobility of InAlN/GaN 2DEGs

2.2.1 General electron mobility theory

The calculation of the low-field electron mobility of InAlN/GaN 2DEGs follows the general treatment of the relaxation time approximation. According to this approximation, the electron

mobility is expressed as follows:

$$\mu = \frac{e\langle\tau\rangle}{m^*} \tag{2.4}$$

where m^* is the electron effective mass and $\langle\tau\rangle$ is the average relaxation time. The relaxation time depends on the electron energy. The relation connecting $\langle\tau\rangle$ and the energy dependent relaxation time $\tau(E)$ is derived from the Boltzmann's transport equation and takes the following form [43]:

$$\langle\tau\rangle = \frac{\int \tau(E) E \frac{\partial f_0(E)}{\partial E} \mathrm{d}E}{\int E \frac{\partial f_0(E)}{\partial E} \mathrm{d}E} \tag{2.5}$$

where $f_0(E)$ is the Fermi-Dirac distribution. Several scattering mechanisms contribute to the relaxation process and each of them is characterized by its own relaxation time $\tau_j(E)$. The different relaxation times sum up according to the following rule:

$$\tau(E) = \left(\sum \tau_j^{-1}(E)\right)^{-1} \tag{2.6}$$

The calculation of the different relaxation times can be performed in the framework of the scattering theory [41]. Let us consider an electron with wavevector $\mathbf{k}$, energy $E = \hbar^2 k^2/2m^*$ and wave function $\Psi(z,\mathbf{r}) = A^{-1/2}\psi(z)e^{i\mathbf{k}\cdot\mathbf{r}}$. In the presence of a scattering potential $V_j(z,\mathbf{r})$, the electron can be elastically scattered to a new wavevector $\mathbf{k}' = \mathbf{k}+\mathbf{q}$. The matrix element for the transition is

$$M_j(E,\mathbf{q}) = \frac{1}{A}\int \psi^*(z)\left[V_j(z,\mathbf{r})e^{-i\mathbf{q}\cdot\mathbf{r}}\right]\psi(z)\mathrm{d}^2\mathbf{r}\mathrm{d}z \tag{2.7}$$

Then, the relaxation time can be calculated:

$$\frac{1}{\tau_j(E)} = \frac{A}{2\pi\hbar}\int\left(\frac{M_j(E,\mathbf{q})}{S(q,T)}\right)^2 (1-\cos\theta)\delta(E_{k'}-E)\mathrm{d}^2\mathbf{k}' \tag{2.8}$$

where θ is the angle formed by $\mathbf{k}$ and $\mathbf{k}'$ and can be obtained from $\mathbf{q}$: $1-\cos\theta = \hbar^2 q^2/4m^*E$. The term $\delta(E_{k'}-E)$ guarantees that only elastic scattering events contribute to $\tau_j(E)$. In case of phonon absorption or emission, this term should be replaced by $\delta(E_{k'}-E \mp E_{ph})$, where E_{ph} is the phonon energy. $S(q,T)$ is the screening function, accounting for the screening effect of 2DEG electrons on the scattering potential:

$$S(q,T) = 1 + \frac{e^2 G(q)\Pi(q,T,E_F)}{2\epsilon q} \tag{2.9}$$

Here, $G(q)$ is the form factor:

$$G(q) = \iint \psi^2(z)\psi^2(z')e^{-q|z-z'|}\mathrm{d}z\mathrm{d}z' \tag{2.10}$$

and $\Pi(q,T,E_F)$ the polarizability function:

$$\Pi(q,T,E_F) = \frac{m^*}{4\pi\hbar^2 k_B T}\int_0^\infty \frac{1-\Theta(q-2k_F)\left[1-(2k_F/q)^2\right]^{1/2}}{\cosh^2\left[(E_F-E)/2k_B T\right]}\mathrm{d}E \tag{2.11}$$

where E_F and k_F are the Fermi energy and wavevector, respectively, and $\Theta(x)$ is the Heaviside step function.

Eq. 2.6 to 2.11 can be used for the calculation of the electron mobility at a given temperature and 2DEG density once the different scattering potentials are defined and the wave function $\psi(z)$ is known. The wavefunction $\psi(z)$ should be numerically calculated separately. Although this is a very accurate way for calculating the mobility, it requires a considerable amount of calculations and the trends related to the effects of diferrent parameters cannot be extracted. Furthermore, in highly dense 2DEGs, where not only the fundamental subband is populated, intersubband scattering events should be taken into account, increasing the complexity of the problem. Analytical expressions for the electron mobility would be far more useful, although not so accurate, especially if some parameters defining the scattering potential are not known and have to be extracted by fitting experimental results. As we are here interested in studying the effect of several parameters on μ, we will make use of a simplified theory allowing for a better understanding of the low-field transport properties of InAlN/GaN 2DEGs.

As InAlN/GaN HEMTs are degenerate up to temperatures well above room temperature as a consequence of their high density, it is reasonable to replace $\langle\tau_j\rangle$ with $\tau_j(E_F)$. Indeed, the $\partial f_0(E)/\partial E$ term in Eq. 2.5 peaks at E_F. This leads directly to the Matthiessen's rule, which states that μ can be written as the sum of individual mobilities, each associated to a specific scattering mechanism and relaxation time:

$$\frac{1}{\mu} = \sum_j \frac{1}{\mu_j}, \quad \text{with} \quad \mu_j = \frac{e\tau_j(E_F)}{m^*} \tag{2.12}$$

The second important simplification comes from the use of Fang-Howard wavefunctions (see Appendix A for their formulation) instead of numerically calculated wavefunctions for the calculation of the matrix elements (Eq. 2.7) and the form factor (Eq. 2.10). The use of analytical wavefunctions constitutes a great advantage, as without them no analytical formula for the mobility can be obtained. This set of approximations allows for analytical convenient expressions of μ_j that will be used hereafter.

2.2.2 Scattering mechanisms in InAlN/GaN heterostructures

The main scattering mechanisms affecting the mobility of GaN based 2DEGs are associated to acoustic and optical phonons, alloy disorder, interface roughness, background ionized impurities and charged dislocations. As we will see in this section, optical phonons, interface roughness and alloy disorder are by far the dominant scattering mechanisms in InAlN/GaN based heterostructures. The equations presented here have been given by Jena [108] on the

basis of previous theories [109].

Acoustic phonon relaxation time can be expressed as:

$$\frac{1}{\langle \tau_{ap} \rangle} = \frac{3m^*_{GaN} b a_c^2 k_B T}{16 \rho v_s^2 \hbar^3} \tag{2.13}$$

where $b = \left(33 m^*_{GaN} e^2 n_s / 8\hbar^2 \epsilon_0 \epsilon_{GaN}\right)^{1/3}$ is the Fang-Howard variational parameter, discussed in more detail in Appendix A, $a_c = 9.1$ eV is the Γ-valley conduction band deformation potential, $\rho = 6.15$ g/cm^3 is the GaN mass density and $v_s = 8 \times 10^5$ cm/s is the GaN sound velocity. The associated mobility μ_{ac} is thus proportional to T^{-1} and to $n_s^{-1/3}$. **Optical phonon** relaxation time takes the following form:

$$\frac{1}{\langle \tau_{op} \rangle} = \frac{e^2 \omega_0 m^*_{GaN} N_B(T) G(q_0)}{2\epsilon^* q_0 \hbar^2 F(y)} \tag{2.14}$$

where $\hbar\omega_0$ is the polar optical phonon energy, $q_0 = \sqrt{2m^*_{GaN}\omega_0/\hbar}$ the polar optical phonon wavevector, and $\epsilon^* = \epsilon_{LF}\epsilon_{HF}/(\epsilon_{LF}+\epsilon_{HF}) = 3.3$, with ϵ_{LF} and ϵ_{HF} the GaN low and high frequency dielectric constants, respectively. $N_B(T) = 1/\left(e^{\hbar\omega_0/k_B T} - 1\right)$ is the Bose-Einstein distribution factor. $F(y) = 1 + (1 - e^{-y})/y$, with $y = \pi\hbar^2 n_s / m*_{GaN}\, k_B T$. $G(q_0) = (2\eta^3 + 3\eta^2 + 3\eta)/8$, with $\eta = b/(b+q_0)$, is the form factor calculated in the framework of the Fang-Howard approximation. The optical phonon limited mobility μ_{op} decreases exponentially with temperature as a consequence of the $N_B(T)$ term and is furthermore reduced at high 2DEG densities as a consequence of the $G(q_0)$ and $F(y)$ terms. μ_{op} becomes the limiting mobility component at room temperature and above.

Interface roughness scattering is another important scattering mechanisms in InAlN/GaN 2DEGs. The corresponding relaxation time can be written as:

$$\frac{1}{\langle \tau_{ir} \rangle} = \frac{\Delta^2 L^2 m^*_{GaN} n_s^2}{8\epsilon^2_{GaN}\hbar^3} \int_0^1 \frac{u^4 e^{-k_F^2 L^2 u^2}}{\left(u + G(2k_F u)\frac{q_{TF}}{2k_F}\right)^2 \sqrt{1-u^2}} \mathrm{d}u \tag{2.15}$$

where Δ and L are the surface rms roughness and correlation length, respectively, and $q_{TF} = e^2 m^*_{GaN}/2\pi\hbar^2\epsilon_0\epsilon_{GaN}$ is the Thomas-Fermi screening wavevector. The associated mobility μ_{ir} is heavily dependent on the 2DEG density due to the n_s^2 term and the strong dependence of the integral on k_F. In particular, μ_{ir} decreases with increasing n_s. Physically, this results from the fact that with increasing n_s, the electron distribution shifts progressively closer to the GaN/barrier interface, enhancing the effect of interface roughness. On the other hand, μ_{ir} is temperature independent. The surface rms roughness Δ can be easily obtained form atomic force microscopy (AFM) measurements. The correlation length L can be in principle obtained from AFM images too. However, it is a often hard to obtain L from AFM images and is more convenient to keep it as fitting parameter.

Background impurity scattering and **dislocation scattering** share several features as they

both concern scattering events caused by the Coulomb potential of either charged impurities or dislocation lines, respectively. Background impurities are associated to the following relaxation time:

$$\frac{1}{\langle\tau_{imp}\rangle} = N_{imp}\frac{m^*}{2\pi\hbar^3 k_F^3}\left(\frac{e^2}{2\epsilon_0\epsilon_{GaN}}\right)^2 \tag{2.16}$$

where N_{imp} is the background impurity concentration, typically 10^{16} to 10^{17} cm^{-3} for GaN based heterostructures. Dislocation scattering gives instead rise to the following relaxation time:

$$\frac{1}{\langle\tau_{disl}\rangle} = \frac{N_{disl}m^*e^2\lambda_L^2}{4\pi\hbar^3\epsilon_0^2\epsilon_{GaN}^2 k_F^4}\frac{\sqrt{1-a^2}+a^2\ln\frac{1-\sqrt{1-a^2}}{a}}{a(1-a^2)^{3/2}} \tag{2.17}$$

where N_{disl} is the dislocation density, λ_L is the linear charge density of a dislocation and $a = q_{TF}/2k_F$. The dislocation limited mobility μ_{disl} can be written in a simpler form:

$$\mu_{disl} \sim 43365\left(\frac{10^8 cm^{-2}}{N_{disl}}\right)\left(\frac{n_s}{10^{12}cm^{-2}}\right)^{1.34}\left(\frac{1}{f^2}\right) \tag{2.18}$$

where f is the dislocation filling factor, i. e. the fraction of the states induced in the gap which are charged. Both μ_{imp} and μ_{disl} are temperature independent and increase with the 2DEG density, contrary to μ_{op} and μ_{ir}.

The final scattering mechanism worth discussing is **alloy disorder scattering**. This scattering mechanism has its roots in the randomly varying alloy potential in the barrier and is supposed to be particularly strong in InAlN/GaN 2DEGs due to the strong difference between In and Al atomic number. Alloy scattering affects the electron mobility if the electron wavefunction overlaps with the barrier material. For this reason, a modified Fang-Howard function, detailed in Appendix A, has to be used. The relaxation time associated to this mechanism is given by:

$$\frac{1}{\langle\tau_{alloy}\rangle} = \frac{m^*\Omega_0(V_{In}-V_{Al})^2 x(1-x)}{2e^2\hbar^3}\kappa_b P_b^2 \tag{2.19}$$

where x is the alloy composition, Ω_0 is the InAlN unit cell volume, $(V_{In} - V_{Al})$ is the alloy scattering potential that results by replacing an Al with an In atom. $(V_{In} - V_{Al})$ can be estimated as the conduction band offset between AlN and InN, which is 4 eV [110]. κ_b is a parameter entering in the modified Fang-Howard function (see Appendix A) and P_b is the probability of finding the electron in the barrier. Alloy scattering has been a critical issue of InAlN/GaN heterostructures at the beginning of their development. The very strong alloy scattering potential results indeed in very low room temperature electron mobility, typically around 500 $cm^2/V{\cdot}s$, hindering the development of efficient electron devices [111, 112]. However, Eq. 2.19 shows that if the penetration of the wavefunction in the InAlN barrier is minimized, the deleterious effect of alloy scattering can be considerably reduced. The introduction of a ~ 1 nm AlN spacer between the GaN channel and the InAlN barrier proved very effective in this

sense [68]. The spacer, being a binary material, does not introduce alloy scattering events and at the same time reduces the overlap of the 2DEG wavefunction with the InAlN barrier to negligible values. The 1 nm AlN spacer is therefore a fundamental component of high quality InAlN/GaN heterostructures and its presence makes alloy scattering negligible. Thanks to it, room temperature electron mobilities well above 1000 $cm^2/V{\cdot}s$ can be easily obtained.

In conclusion, for InAlN/GaN heterostructures having an AlN spacer for high electron mobility, μ can be written as:

$$\frac{1}{\mu} = \frac{1}{\mu_{ap}} + \frac{1}{\mu_{op}} + \frac{1}{\mu_{ir}} + \frac{1}{\mu_{imp}} + \frac{1}{\mu_{disl}} \tag{2.20}$$

where the various terms can be calculated thanks to the help of Eq. 2.13 to 2.18. We will see in the following paragraph the application of this theory to the modeling of experimental InAlN/GaN 2DEG mobilities.

2.2.3 Modeling of InAlN/GaN 2DEG electron mobilities

Identifying the relative importance of the different scattering mechanisms determining the final electron mobility is of high importance as the result of this analysis can be used to rationally improve the heterostructure design and growth. A good example in this sense has been the suppression of alloy scattering thanks to the introduction of the AlN spacer. The separation of the different mechanisms can be done by looking at the temperature dependence of the mobility. This allows to evaluate precisely the contribution of optical and acoustic phonons, while the other mechanisms, which are temperature independent, require additional experimental data for their evaluation. In particular, the correct evaluation of background impurity and dislocation limited mobilities requires the knowledge of background impurity and dislocation concentrations, respectively. The main impurities in high resistivity GaN used normally for HEMT applications are oxygen and carbon. Their concentrations are typically in the high 10^{16} range (see Sec. 4.2.2 for a deeper discussion about their quantification). Therefore, a background concentration value of 10^{17} cm^{-3} is appropiate for mobility evaluations. The dislocation density lies typically in the $10^8 - 10^{10}$ cm^{-2} range and can be evaluated by means of X-ray diffraction. Its quantification will be treated in more detail in Sec. 3.1.2. Finally, interface roughness limited mobility requires the knowledge of both interface rms roughness and correlation length. While Δ can be approximated by the surface rms roughness obtained from AFM images (see Sec. 3.1.3 for more details), L can be taken as a fitting parameter.

Fig. 2.3 compares the temperature dependence of μ for two InAlN/GaN heterostructures. The first sample (panel (a)) is grown on SiC and has an electron density of 1.5×10^{13} cm^{-2}. The second sample (panel (b)) is on the other hand grown on sapphire and has an electron density of 1.0×10^{13} cm^{-2}. Both samples are characterized by a similar dislocation density of $\sim 10^9$ cm^{-2}. Their surface rms roughness are 1.5 nm and 0.8 nm, respectively. The fitted data have been obtained by using a correlation length $L = 3.5$ nm. As can be seen, the model

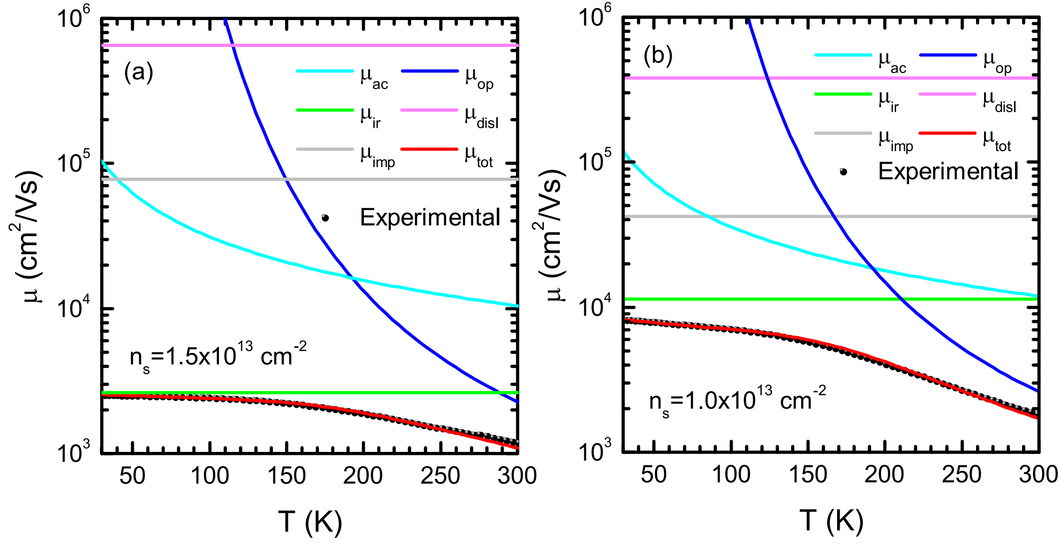

Figure 2.3: Experimental (dots) and calculated (red line) temperature dependent electron mobility for (a) an heterostructure grown on SiC having $n_s = 1.5 \times 10^{13}$ cm^{-2}, $\Delta = 1.5$ nm, $L = 3.5$ nm and (b) an heterostructure grown on sapphire having $n_s = 1.0 \times 10^{13}$ cm^{-2}, $\Delta = 0.8$ nm. Both graphs show the different components of the mobility.

described in the previous section accurately describes the temperature dependence of μ despite its relative simplicity. The two sets of data allow furthermore a deeper discussion of the relative importance of the different scattering mechanisms. First, it is clear that optical phonon scattering and interface roughness scattering are the two principal mechanisms limiting the mobility. In particular, μ_{ir} definitely dominates μ at low temperature, while μ_{op} becomes progressively more important at higher temperature. At room temperature, both μ_{ir} and μ_{op} dominate the mobility. Acoustic phonon scattering has a less important role, becoming significant only around room temperature. Dislocation and background impurity scattering are finally almost negligible in the whole temperature range, being normally more than one order of magnitude lower than the other terms. The small impact of dislocations and background impurities on μ can be attributed to the very efficient screening provided by the high 2DEG density. n_s plays a very important role in determining the final electron mobility. This can be worked out again by comparing the two panels of Fig. 2.3. The sample with the lower density shows indeed a markedly higher mobility over the whole temperature range. μ_{ir} is indeed significantly higher for the lower density sample. This is partly due to its lower rms roughness, but principally to its lower n_s (Eq. 2.15). As a consequence, the 30 K mobility is 2500 cm^2/V·s for the heterostructure with $n_s = 1.5 \times 10^{13}$ cm^{-2}, and 8400 cm^2/V·s for the heterostructure with $n_s = 1.0 \times 10^{13}$ cm^{-2}. Optical and acoustic phonon scattering are also alleviated at low n_s (Eq.2.13 and 2.14), which makes that the room temperature mobility is 1180 cm^2/V·s for the heterostructure with $n_s = 1.5 \times 10^{13}$ cm^{-2}, and 1820 cm^2/V·s for the heterostructure with $n_s = 1.0 \times 10^{13}$ cm^{-2}. It is finally interesting to note that, contrary to phonon and interface roughness scattering, dislocation and background impurity related scattering worsen at low n_s. This is a consequence of the lower screening provided by lower

density 2DEGs.

In conclusion, the different mechanisms contributing to InAlN/GaN 2DEG mobility are well understood. Interface roughness and optical phonon scattering are the dominant mechanisms limiting μ, both at low and room temperature. The 2DEG density has a strong effect on the different scattering mechanisms, and 2DEGs with lower n_s are generally characterized by higher mobilities.

2.3 InAlN physical parameters

Besides a correct modeling of the 2DEG mobility, it is of fundamental importance to dispose of an accurate prediction of the dependence of the 2DEG density on the barrier thickness and gate bias voltage. For this, Schrödinger-Poisson simulations are the most appropriate tool. However, such simulations can be performed on the condition that a certain number of physical parameters are known. These include the static dielectric constant of the different materials constituting the heterostructure, electron effective masses, polarization induced interface charges, band offsets and the surface potential or Schottky barrier, depending if ungated or gated heterostructures are considered, respectively.

For AlN and GaN, which are well known materials, literature values have been used. For the AlN/GaN interface, we took a conduction band offset $\Delta E_{c,AlN/GaN} = 1.7$ eV according to the work of Tchernycheva *et al.* [113]. For the same interface, a polarization induced interface charge density $\sigma_{AlN/GaN} = 6.64 \times 10^{13}$ cm^{-2} was calculated according to Ambacher *et al.* [22]. Concerning the static dielectric constants, we took $\epsilon_{GaN} = 9.5$ and $\epsilon_{AlN} = 8.5$ for GaN and AlN, respectively [114]. Electron effective masses of $m^*_{GaN} = 0.20 m_0$ and $m^*_{AlN} = 0.32 m_0$ were taken [20], respectively, where m_0 is the free electron mass. When coming to InAlN related parameters, however, literature values are much more scarce. Regarding band offsets, Akazawa *et al.* [115] have reported X-ray photoelectron spectroscopy measurements giving a 0.2 eV valence band offset between InAlN and GaN. Taking 4.5 eV as the bandgap for $In_{0.17}Al_{0.83}N$ (see Sec. 1.1), this leads to an InAlN/GaN conduction band offset $\Delta E_{c,InAlN/GaN} = 0.9$ eV. However, in our heterostructures we are not dealing with InAlN/GaN interfaces, but with InAlN/AlN ones. For the latter, no data has been reported so far. We therefore make the assumption $\Delta E_{c,InAlN/AlN} = \Delta E_{c,AlN/GaN} - \Delta E_{c,InAlN/GaN} = 1.7 - 0.9 = 0.8$ eV. Passing now to InAlN electron effective mass, no experimental reports are available. A first approximation would be to take the linear interpolation between AlN and InN electron effective masses, which gives $m_{InAlN} = 0.28 m_0$. However, the large difference between AlN and InN effective masses makes this value questionable. A better approach is to take the effective mass of the AlGaN alloy having the same band gap of LM-InAlN. This leads to $m_{InAlN} = 0.25 m_0$. We chose to keep this last value. The last InAlN related parameters, namely its static dielectric constant ϵ_{InAlN}, InAlN/AlN interface polarization charge density $\sigma_{InAlN/AlN}$, surface potential Φ_B and Schottky barrier Φ_S have been evaluated experimentally.

The extraction of ϵ_{InAlN}, $\sigma_{InAlN/AlN}$ and Φ_B was done by studying the electrochemical CV

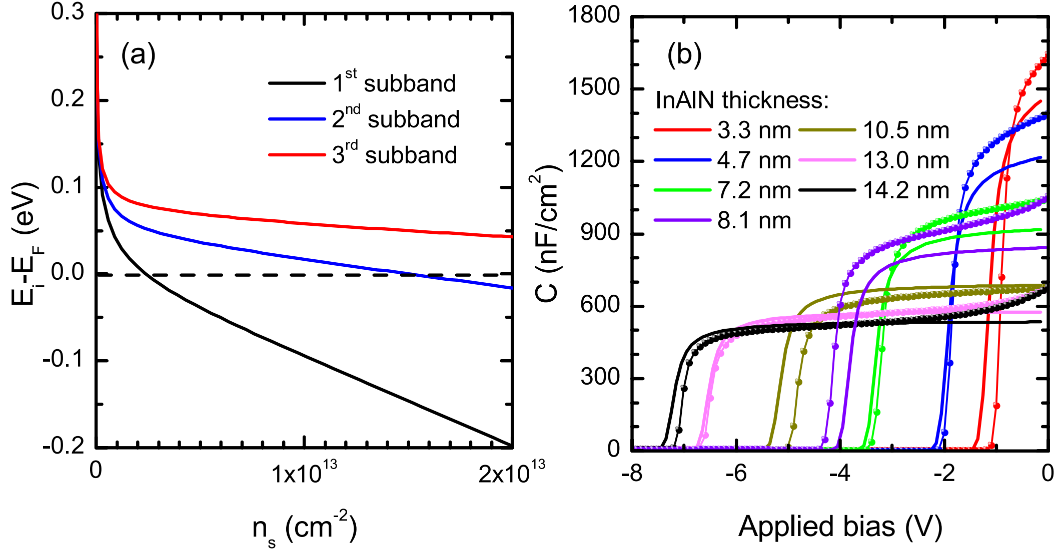

Figure 2.4: (a) Energy of the bottom of the first three subbands of InAlN/GaN 2DEGs as a function of n_s. The energy zero is taken at the Fermi level. (b) Experimental (dots) and simulated (lines) electrochemical capacitance-voltage curves for the ensemble of samples used.

characteristics of a series of InAlN/GaN heterostructures. The basis of this study is constituted by the equations we have already seen in Sec. 1.3. The presence of the AlN spacer requires however their slight modification. The balance equation becomes, therefore:

$$\Phi_{B/S} - eV - eF_{InAlN}d_{InAlN} + \Delta E_{c,InAlN/AlN} - eF_{AlN}d_{AlN} - \Delta E_{c,AlN/GaN} + \\ + (E_0 - E_{bott}) + (E_F - E_0) = 0 \tag{2.21}$$

where $\Phi_{B/S}$ is either the surface (Φ_B) or Schottky (Φ_S) barrier, and d_{InAlN} and d_{AlN} the InAlN and AlN thickness, respectively. F_{AlN}, the electric field in the AlN barrier, can be written similarly to Eq. 1.13:

$$F_{AlN} = \frac{e(\sigma_{AlN/GaN} - n_s)}{\epsilon_0 \epsilon_{AlN}} \tag{2.22}$$

The electric field in the InAlN layer writes, according to Gauss' Law:

$$F_{InAlN} = \frac{e(\sigma_{InAlN/AlN} + \sigma_{AlN/GaN} - n_s)}{\epsilon_0 \epsilon_{InAlN}} \tag{2.23}$$

Finally, $(E_0 - E_{bott})$ and $(E_F - E_0)$ have been already given in Eq. 1.15 and 1.16, assuming that only a single band is occupied.

Eq, 2.21 is the basis for the modeling of CV measurements. The heterostructure specific

Table 2.1: Barrier thickness, In composition and transport properties of the set of samples used for InAlN physical parameters extraction.

d_{InAlN} (nm)	[In] (%)	n_s (cm^{-2})	μ (cm^2/V·s)	ρ_s (Ω/□)
3.3	17	1.05×10^{13}	1380	433
4.7	16	1.66×10^{13}	1220	307
7.2	17	2.09×10^{13}	1240	241
8.1	17	2.43×10^{13}	1040	246
10.5	17	2.32×10^{13}	1220	221
13.0	18	2.51×10^{13}	880	283
14.2	18	2.28×10^{13}	1070	255

capacitance C is defined in the following way:

$$\frac{1}{C} = \frac{\partial Q}{\partial V} = e\frac{\partial n_s}{\partial V} \tag{2.24}$$

Thanks to Eq. 2.21, this can be rewritten in the following way:

$$\frac{1}{C} = \frac{d_{AlN}}{\epsilon_0 \epsilon_{AlN}} + \frac{d_{InAlN}}{\epsilon_0 \epsilon_{InAlN}} + \frac{\pi \hbar^2}{e^2 m_{GaN}} + \left(\frac{\sqrt{3}\pi\hbar}{8e\epsilon_0\epsilon_{GaN}\sqrt{m_{GaN}}} \right)^{2/3} n_s^{-1/3} \tag{2.25}$$

Eq. 2.25 shows that the heterostructure capacitance is composed of the AlN spacer capacitance, the InAlN barrier capacitance, and a quantum capacitance term dependent on the 2DEG density. It is therefore possible to extract ϵ_{InAlN} by studying the variation of the reverse of the capacitance with d_{InAlN} at fixed n_s:

$$\left.\frac{\partial 1/C}{\partial d_{InAlN}}\right|_{n_s=cst.} = \frac{1}{\epsilon_0 \epsilon_{InAlN}} \tag{2.26}$$

In order for this equation to be accurate, n_s should be low enough to have just one subband occupied. Fig. 2.4(a) shows the position of the bottom of the various subbands as a function of n_s. It can be seen that for $n_s < 10^{13}$ cm^{-2} only the first subband is significantly populated.

In this study, we considered a series of 7 standard nearly LM-InAlN/GaN heterostructures grown on sapphire (see chapter 3 for a detailed description of their growth) having a 1 nm AlN spacer and an InAlN barrier thicknesses ranging between 3.3 nm and 14.2 nm. The barrier thickness and In composition have been precisely determined by X-ray diffraction for each sample (see Sec. 3.1.2 for more details) and are summarized in Table 2.1, together with their transport properties. The electrochemical CV characteristics for the whole set of samples has been recorded and is shown in Fig. 2.4(b). For the extraction of ϵ_{InAlN}, we chose to study the heterostructure capacitance for $n_s = n_{s0} = 8 \times 10^{12}$ cm^{-2}. For this, it was necessary to determine for which bias the 2DEG density reaches n_{s0}. The voltage dependent n_s could be

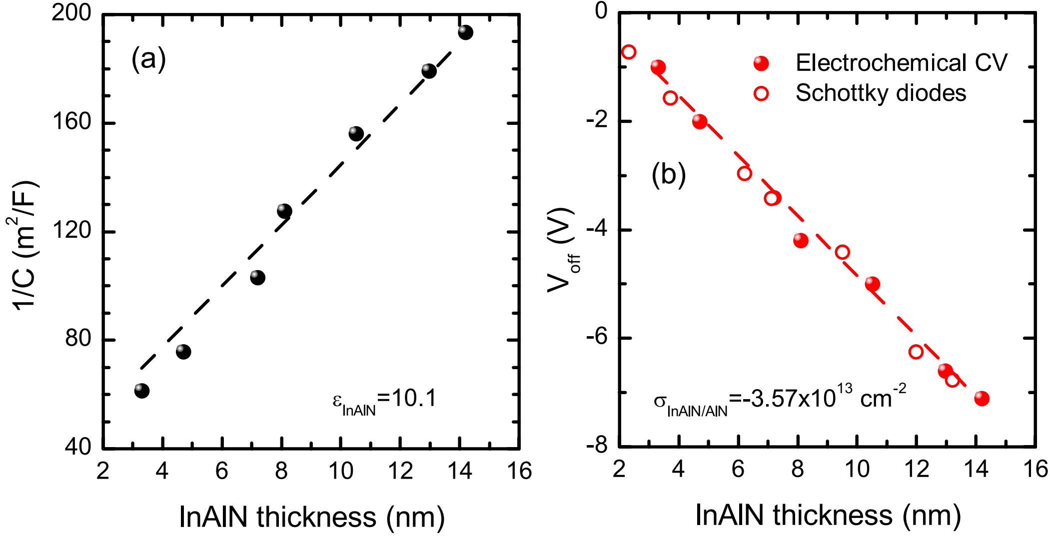

Figure 2.5: (a) Plot of the inverse heterostructure capacitance as a function of the InAlN barrier thickness. The capitance values refer to a 2DEG density of 8×10^{12} cm^{-2}. From the fitting ϵ_{InAlN} is extracted. (b) Pinch-off voltage as a function of InAlN thickness obtained from electrochemical CV measurements on as grown heterostructures (full dots) and from Schottky diodes (open circles). From the fitting $\sigma_{InAlN/AlN}$ is extracted.

evaluated from the CV curves in the following way:

$$n_s(V) = \frac{1}{e}\int_{V_{off}}^{V} C(V)\mathrm{d}V \tag{2.27}$$

where V_{off} is the pinch-off voltage. V_{off} can be identified as for $V = V_{off}$ the capacitance falls to zero. Thanks to Eq. 2.27 we could therefore identify, for each heterostructure, the voltage for which $n_s = n_{s0}$ and the corresponding capacitance. We could therefore build the $1/C|_{n_s=n_{s0}}$ vs d_{InAlN} graph of Fig. 2.5(a). By fitting its slope, we obtained $\epsilon_{InAlN} = 10.1$. This value is similar to the one of 11.3 previously obtained by Gonschorek *et al.* [116]. However, the latter value has not been derived independently from other parameters. Therefore, $\epsilon_{InAlN} = 10.1$ is a more reliable result.

We now turn to the determination of interface polarization charges. This can be done by studying the dependence of V_{off} on d_{InAlN}. V_{off} can be calculated from Eq. 2.21 by setting $n_s = 0$. We thus have:

$$V_{off} = \frac{1}{e}\left(\Phi_{B/S} + \Delta E_{c,InAlN/AlN} - \Delta E_{c,AlN/GaN}\right) - e\left(\frac{\sigma_{InAlN/AlN} + \sigma_{AlN/GaN}}{\epsilon_0\epsilon_{InAlN}} d_{InAlN} + \frac{\sigma_{AlN/GaN}}{\epsilon_0\epsilon_{AlN}} d_{AlN}\right) \tag{2.28}$$

Table 2.2: Physical relevant parameters used for InAlN/GaN heterostructure modeling.

$\Delta E_{c,InAlN/AlN}$	0.8 eV	ϵ_{InAlN}	10.1	m^*_{InAlN}	$0.25m_0$
$\Delta E_{c,AlN/GaN}$	1.7 eV	ϵ_{AlN}	8.57	m^*_{AlN}	$0.32m_0$
$\sigma_{InAlN/AlN}$	-3.57×10^{13} cm^{-2}	ϵ_{GaN}	9.5	m^*_{GaN}	$0.20m_0$
$\sigma_{AlN/GaN}$	6.64×10^{13} cm^{-2}	Φ_B (=Φ_S)	2.8 eV		

Therefore, by plotting V_{off} vs d_{InAlN} a linear relationship is expected with slope

$$\frac{\partial V_{off}}{\partial d_{InAlN}} = -e\frac{\sigma_{InAlN/AlN} + \sigma_{AlN/GaN}}{\epsilon_0 \epsilon_{InAlN}} \tag{2.29}$$

As $\sigma_{AlN/GaN}$ and ϵ_{InAlN} are known, $\sigma_{InAlN/AlN}$ can be extracted. From electrochamical CV extracted V_{off} values (Fig. 2.5(b)) we obtained $\sigma_{InAlN/AlN} = -3.57 \times 10^{13}$ cm^{-2}, in relatively good agreement with the value of 3×10^{13} cm^{-2} calculated from Eq. 1.4 and 1.5. The intercept of the fitted line can be used to extract Φ_B, which turns out to be 3.0 eV. However, we prefer to adopt for Φ_B the value that gives the best fit of the ensemble of the electrochemical CV curves of Fig. 2.4(b). We therefore simulated by means of a Schrödinger-Poisson solver the bias dependent capacitance for the whole set of samples, using the heterostructure parameters discussed before and varying Φ_B to find its optimum value. Best fits were obtained with $\Phi_B = 2.8$ eV, which is slightly lower than the value obtained from Fig 2.5(b). The simulated CV curves are compared to the experimental data in Fig. 2.4(b). It can be noted that the simulated curves do not always perfectly fit the experimental data. Better fits could be obtained by adjusting the simulation parameters for each heterostructure. However, as we are interested in values suitable for InAlN/GaN heterostructures in general, we kept the values that best describe the ensemble of our samples rather than a particular heterostructure. The physical parameters necessary for Schrödinger-Poisson simulations are summarized in Table 2.2.

Thanks to the parameters listed in Table 2.2, it was possible to calculate the dependence of n_s on the InAlN barrier thickness via Schrödinger-Poisson simulations. The calculated band profile and electron density distribution for a series of heterostructures with $d_{AlN} = 1$ nm and d_{InAlN} ranging between 3 and 15 nm are shown in Fig. 2.6(a). Fig. 2.6(b) shows the calculated dependence of n_s on d_{InAlN}, which is in agreement with experimental data, strengthening once more the validity of our model.

Concerning the modeling of gated InAlN/GaN heterostructures, the approach is identical to the modeling of ungated heterostructures, except that the surface potential Φ_B must be replaced with the Schottky barrier height Φ_S. In this thesis, we considered only Ni as Schottky metal. Ni/InAlN/GaN Schottky diodes have been fabricated for the whole set of samples considered above and their V_{off} vs d_{InAlN} is reported in Fig. 2.5(b). As explained in Sec. 4.2.1, the InAlN thickness is reduced of 1 nm by the Schottky fabrication process and for this reason the points in Fig. 2.5(b) corresponding to the Schottky diodes are shifted with respect to the ones corresponding to electrochemical CV measurements. Interestingly, the two series of

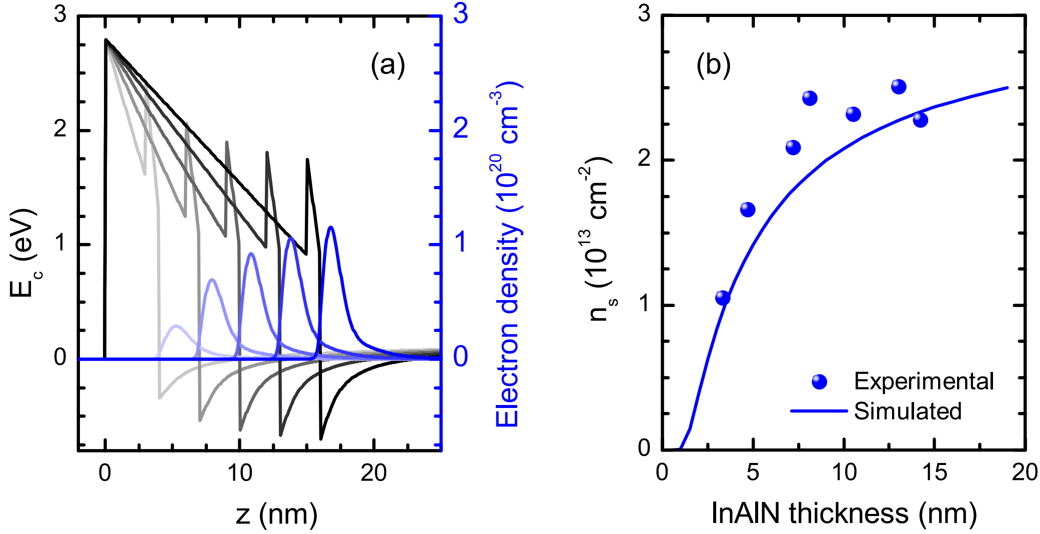

Figure 2.6: (a) Conduction band profile (gray curves) and electron density distribution (blue curves) for InAlN/GaN heterostructures having d_{InAlN} ranging between 3 and 15 nm. (b) Experimental (dots) and calculated (line) n_s as a function of d_{InAlN}.

points are well fitted by the same line. This means first that Schottky diode processing does not alter interface charges and dielectric constants, and that the Schottky barrier height is equal to the surface potential of 2.8 eV found above. It is also interesting to compare our experimental result with the value derived in the framework of the Schottky model from the difference between the Ni work function W_{Ni} and the InAlN electron affinity χ_{InAlN}. Using $\chi_{InN} = 4.7$ eV [117] and $\chi_{AlN} = 2.1$ eV [118], we estimate $\chi_{InAlN} = 2.5$ eV through the Vegard's law. Taking $W_{Ni} = 5.1$ eV, we calculate $\Phi_S = W_{Ni} - \chi_{InAlN} = 2.6$ eV which agrees quite well with our results.

2.4 Deep levels in InAlN

Deep levels play an important role in GaN based electronic devices. In particular, electrically active traps are responsible for dispersion effects, which negatively impact transistor performance (Sec. 1.6.2 and 5.2), and we will show in Sec. 4.3 that deep levels are responsible for gate leakage currents in InAlN/GaN HEMTs. It is thus of high interest to study deep levels in InAlN. Their understanding is not only useful for InAlN based HEMTs, but generally for any application which makes use of InAlN layers. Some results concerning deep levels in InAlN/GaN HEMTs have been published recently. Johnstone *et al.* [119] found, on thick InAlN layers, a level with 0.164 eV activation energy by deep level transient spectroscopy (DLTS) and a second one with 0.35 eV activation energy by admittance spectroscopy. By DLTS, Chen et al. [120] concluded about the presence of three levels with activation energy 0.351 eV, 0.404 eV and 0.487 eV. Chikhaoui *et al.* [121] reported a 0.37 eV trap by current DLTS on InAlN/GaN HEMTs. There is however no general agreement about the validity of trap levels deduced from current-DLTS

on HEMTs. In fact, in contrast to the results of Chikhaoui *et al.*, Sasikumar *et al.* [102] found by the same technique a level with 0.57 eV activation energy, which was however attributed to the GaN buffer from its close signatures with those one found in AlGaN/GaN HEMTs. The traps observed by current-DLTS on HEMTs may also originate from surface states. Other traps have been furthermore proposed to fit trap related leakage models in InAlN based structures. In particular, Arslan *et al.* [122] proposed the presence of a 0.12 eV deep level in order to explain gate leakage currents in InAlN/GaN HEMTs by Poole-Frenkel emission. Ganguly *et al.* [123], on the other hand, had to use a trap energy of 0.48 eV for fitting the current-voltage characteristics of InAlN/GaN Schottky diodes with the Poole-Frenkel model. It is however important to note that in the latter studies only a limited part of the current-voltage characteristic of InAlN based devices could be fitted, which can pose some doubt about the validity of the trap energies deduced. The investigation of deep levels in InAlN remains therefore a debated topic of high interest for which investigations on thick, more bulky layers than the ones used in HEMTs are necessary. A significant step in this sense has been done by Py *et al.* [124]. In this work, deep levels were investigated in 200 nm thick InAlN layers by means of admittance spectroscopy, which is a technique more suitable than DLTS for the investigation of deep levels with high concentrations. Py *et al.* demonstrated the presence of two levels, a first one with activation energy of about 68 meV and capture cross section 9.7×10^{-17} cm^{-2}, and a second one with activation energy 290 meV and capture cross section 6.2×10^{-15} cm^{-2}. The two levels were unambiguously attributed to the bulk of the InAlN layer and it could be proven [125] that they originate from the same impurity, probably oxygen, behaving like a DX-center. The level with 68 meV activation energy would thus correspond to a donor-like, hydrogenic configuration of oxygen in a substitutional nitrogen site, while the deeper level with 290 meV activation energy would correspond to a lattice distorted configuration with acceptor character.

Admittance spectroscopy and DLTS are investigation methods based on thermal emission of carriers from deep levels. However, very deep levels are generally characterized by very low thermal emission rates, even at high temperatures. Their detection can be nevertheless achieved by stimulating carrier emission with light of sufficient energy. The investigation of deep levels in InAlN by means of photocapacitance spectroscopy is the main topic of this section.

2.4.1 Photocapacitance spectroscopy of InAlN

Photocapacitance spectroscopy measurements were performed on InAlN based Schottky diodes. The 100 nm thick InAlN layer had an In content of 16.4% and was grown on a 2 μm thick n^+-GaN buffer on sapphire by MOVPE. Schottky diodes were processed according to the method of Sec. 2.1.3 and loaded in the cryostat described in Sec. 2.1.4 for photocapacitance measurements. A first series of measurements was performed in order to extract the energy dependence of the optical cross section. For this purpose, the Schottky diodes are held at a quiescent bias of -1 V. Assuming that thermodynamic equilibrium is reached, the corresponding electron and deep levels occupancy distribution are shown in Fig. 2.7(a). The voltage is then

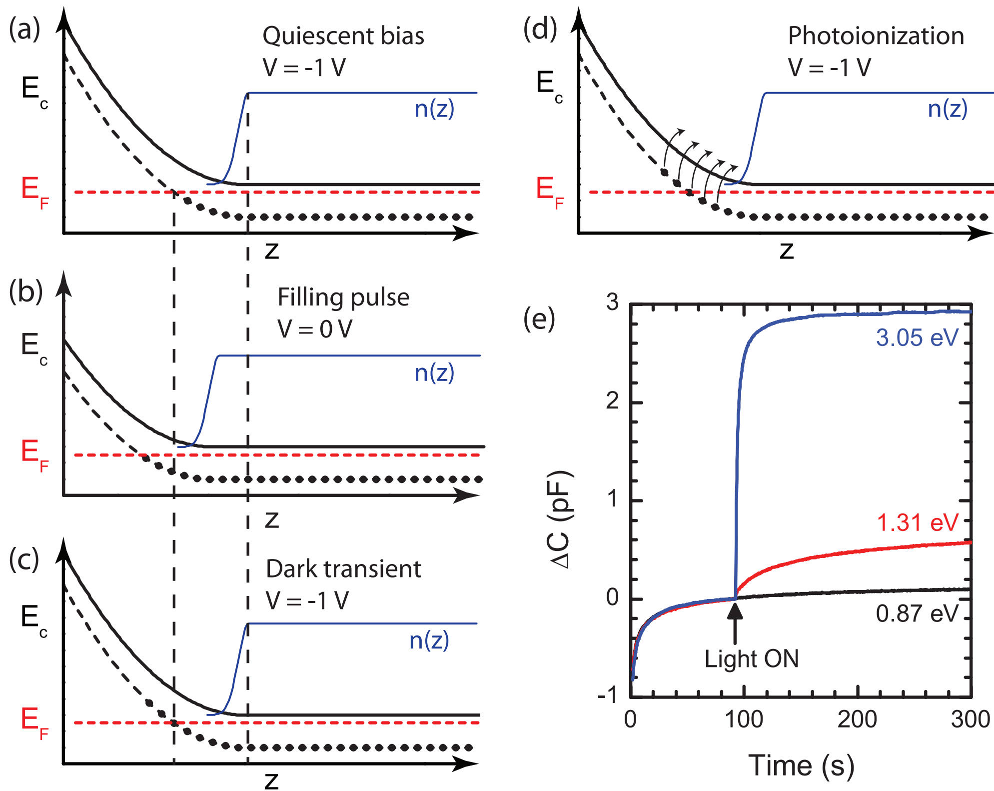

Figure 2.7: Photocapacitance measurement method: (a) From a quiescent bias state the voltage is pulsed (b) to higher values in order to fill some empty traps. The bias is then set back to the quiescent value (c) for a time sufficient for the thermal ionization of shallow levels. The light is then switched on (d) to ionize deep levels. Some representative phototransients at various photon energies recorded on InAlN are shown in (e).

pulsed to a higher value for a certain time, in our case 0 V during 10 s, in order to fill some of the deep levels that were unoccupied under quiescent bias. If the pulse duration is long enough to reach thermal equilibrium, the corresponding trap distribution at the end of the pulse is shown in Fig. 2.7(b). Note however that, for very deep levels, the traps closest to the Fermi level lie far from the tail of the electron distribution. Here, the small electron density makes the capture rate very low. Therefore, at the end of the pulse the traps which lie close below the Fermi level may be not completely filled. Anyway, once the pulse terminated, the voltage is set back to the quiescent value (Fig. 2.7(c)). In order to come back to thermal equilibrium, the deep levels that have been filled during the pulse voltage will need to emit their electrons. While relatively shallow levels can thermally emit the trapped carriers, giving rise to a thermal capacitance transient, very deep levels are characterized by too low thermal emission rates, which inhibits carrier emission. Therefore, after having set the bias back to the quiescent value, the sample is kept in dark for a certain time (90 s in our case) to allow thermal emission from the relatively shallow levels. Then, the sample is illuminated with a monochromatic beam of light, which triggers the ionization of deep levels having an optical ionization energy lower or equal to the photon energy, resulting in a photocapacitance transient (Fig. 2.7(d)). Some

examples of transients recorded with this method at a frequency of 1 MHz using different photon energies are shown in Fig. 2.7(e). The sign of the transient capacitance indicates that electron traps are observed. Note that the thermal transient amplitude is the same in all cases. The photocapacitance transient amplitude on the other hand is not constant. For too low photon energies no transient is induced, while the photocapacitance transient amplitude increases with increasing photon energy. We will discuss the photon energy dependence of the transient amplitude later on. The optical cross section $\sigma(h\nu)$ is extracted from the slope of the capacitance transient according to the method first proposed by Chantre *et al.* [126]. More precisely, the slopes just before (s_{before}) and just after (s_{after}) illumination are extracted, the difference Δs between the two being simply proportional to the product between $\sigma(h\nu)$ and the photon flux $\Phi(h\nu)$:

$$\Delta s \propto \sigma(h\nu)\Phi(h\nu) \tag{2.30}$$

The optical cross section can be thus easily determined, as $\Phi(h\nu)$ is known for each photon energy. The results of this analysis performed in the 0.8-3.0 eV photon energy range and at temperatures of 100 K, 170 K and 250 K are shown in Fig. 2.8. There, $\sigma(h\nu)$ is reported both in linear (Fig. 2.8(a)) and logarithmic scale (Fig. 2.8(b)). From the linear plot it can be recognized that the optical cross section has a threshold around 1.7 eV, but at the same time the logarithmic plot shows that there is a broad tail for lower photon energies. It is furthermore interesting to note that the optical cross sections recorded at 100 K and 170 K superpose very well, while the one recorded at 250 K decreases more rapidly at lower photon energy. The broad tail of the optical cross section indicates that the experimental observations cannot be interpreted by simply stating that a level with depth 1.7 eV is present in the InAlN layer. In that case and as shown in Fig. 2.8, the optical cross section should vanish for photon energies lower than the level depth, as derived by Lucovsky [127]:

$$\sigma(h\nu) \propto \frac{(h\nu - E_t)^{3/2}}{(h\nu)^3} \tag{2.31}$$

where E_t is the trap depth.

Tails in the optical cross section are on the other hand predicted in the case of traps for which the trapping of a carrier induces a large lattice relaxation. In this case the optical ionization energy E_{opt} is higher than the trap depth E_t by an amount called Franck-Condon shift (d_{FC}: $E_{opt} = E_t + d_{FC}$), which is due to the fact that light induces vertical transitions between the two states that do not share the same lattice configuration. In that case, the measured optical cross section is the convolution of several transitions between different phonon states and E_{opt} corresponds to the transition with the highest probability. Jaros [128] and Chantre *et al.* [126] have treated mathematically the problem, giving formulas for the optical cross section that can be essentially interpreted as a convolution of Lucovsky-like functions with a gaussian broadening term which account for the effect of the Franck-Condon shift. The two authors have derived slightly different formulas, which are however nearly equivalent. Chantre *et al.* proposed furthermore different formulas which lead to somewhat different behaviors for

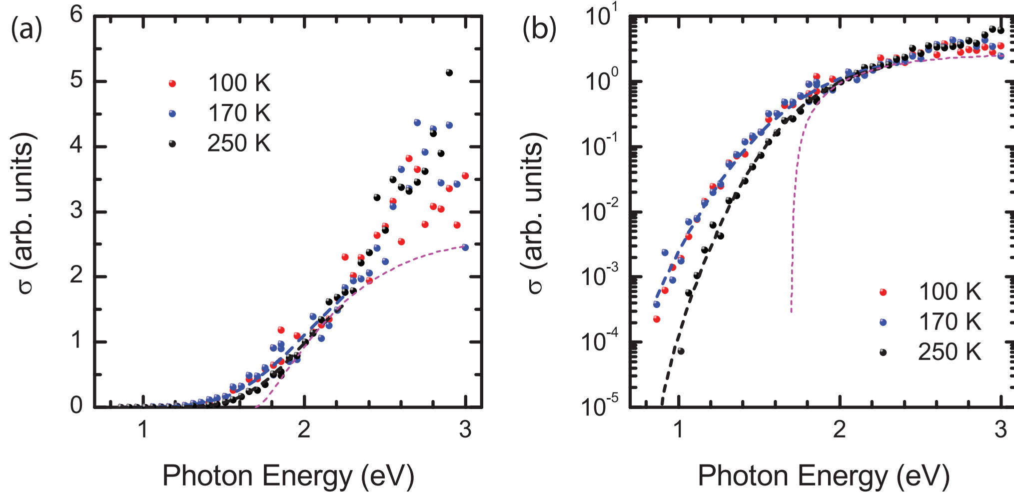

Figure 2.8: (a) Linear and (b) logarithmic scale optical cross section for deep level photoionization in InAlN at 100 K, 170 K and 250 K. Fitted curves are displayed as dashed lines. The magenta line shows the shape of a Lucovsky function.

$h\nu > E_{opt}$. However, the differences are not dramatic and most importantly they are negligible in the low energy tail, which is the most interesting energy domain. Here, we will make use of the formula given by Chantre *et al.* which in closest agreement with the one derived by Jaros [128]:

$$\sigma(h\nu) \propto \frac{1}{h\nu\sqrt{4k_B T d_{FC}}} \int_{E_{opt}}^{+\infty} \frac{\left(E - E_{opt}\right)^{3/2}}{\left(E - E_{opt} + E^i\right)^2} e^{-\frac{(h\nu - E)^2}{4k_B T d_{FC}}} \mathrm{d}E \tag{2.32}$$

where E^i is an energy parameter dependent on the wavefunction of the deep level which can be approximated with E_t. What is worth noting in Eq. 2.32 is that the gaussian broadening term is temperature dependent. In particular, the optical cross section should get broader as the temperature is increased. This is illustrated in Fig. 2.8(b) which shows the evolution of $\sigma(h\nu)$ expected in the case of a large Franck-Condon shift. Attempts to fit the data of Fig. 2.8 with Eq. 2.32 failed for two reasons. First, in order to fit the optical cross section, $d_{FC} > E_{opt}$ was needed at 100 K and 170 K, which seems unphysical. Secondly, a set of fitting parameters suitable for a certain temperature was not at all adapted for other temperatures, which is not surprising considering that the temperature evolution of the cross section broadening is opposite to the one predicted by Eq. 2.32.

An alternative explanation of the broadening of $\sigma(h\nu)$ may be the presence of not just a single deep level, but rather of a band of deep levels with gaussian distribution. In an alloy like InAlN it would not be surprising to have a great variety of local environments for the trap, giving rise to different energy levels. In this case, assuming no thermal activation fot $\sigma(h\nu)$, the experimental optical cross section would be the convolution of the individual cross sections

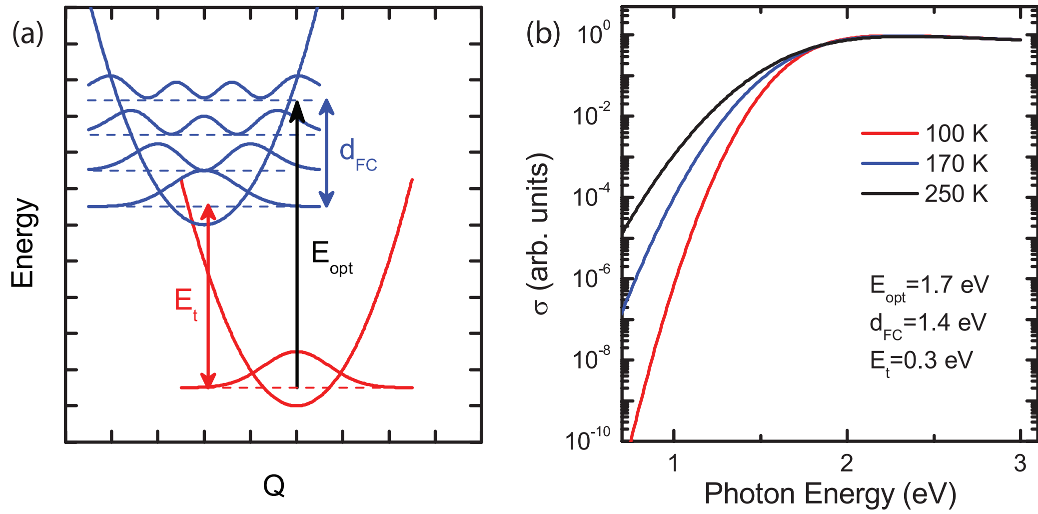

Figure 2.9: (a) Schematic energetic diagram illustrating the Franck-Condon effect. The red and blue lines reprent the ground state and the ionized state of the trap as a function of the lattice distortion Q. Also shown are phonon wavefunction. The graph clarifies also the parameters E_{opt}, d_{FC} and E_t. (b) Simulated optical cross section at different temperatures in the case of large Franck-Condon shift. The graph demonstrates the incompatibility of the model with the experimental data of Fig. 2.8.

with the gaussian distribution term, which is now temperature independent:

$$\sigma(h\nu) \propto \int_0^{+\infty} \frac{(h\nu - E)^{3/2}}{(h\nu)^3} e^{-\left(\frac{E-E_0}{\Delta E}\right)^2} \mathrm{d}E \tag{2.33}$$

where E_0 is the central energy of the Gaussian distribution and ΔE quantifies the broadening. In this model, the low energy tail of $\sigma(h\nu)$ is due to the low energy tail of the trap distribution. Eq. 2.33 allowed a good fitting of the optical cross section up to 2.2 eV at 100 K and 170 K, reported in Fig. 2.8. The parameters used are E_0 = 1.7 eV and ΔE = 0.38 eV. The value of ΔE may be affected by the energy resolution of the light beam. However, as beams with maximum broadening of 20 meV were used, this effect can be neglected. The data at 250 K could be fitted with the same E_0 but a lower broadening ΔE = 0.30 eV, which suggests that at this temperature the shallowest levels are thermally ionized during the 90 s dark period before illumination. It is also possible that, in addition to the energy broadening, the traps are also characterized by a small Franck-Condon shift. Simulation showed, however, that in order to be compatible with experimental data the value of d_{FC} should be $<$ 0.3 eV, otherwise the temperature dependence of $\sigma(h\nu)$ becomes too high. The analysis of the optical cross section is not carried out beyond 2.2 eV. The reason is that for photon energies higher than half of the InAlN band gap (4.5 eV), transitions involving both the conduction band and the valence band have to be taken into account, which complicates significantly the analysis.

Besides the optical cross section, the amplitude of the capacitance transient is another interesting feature and is the object of steady-state photocapacitance studies. In the ideal case,

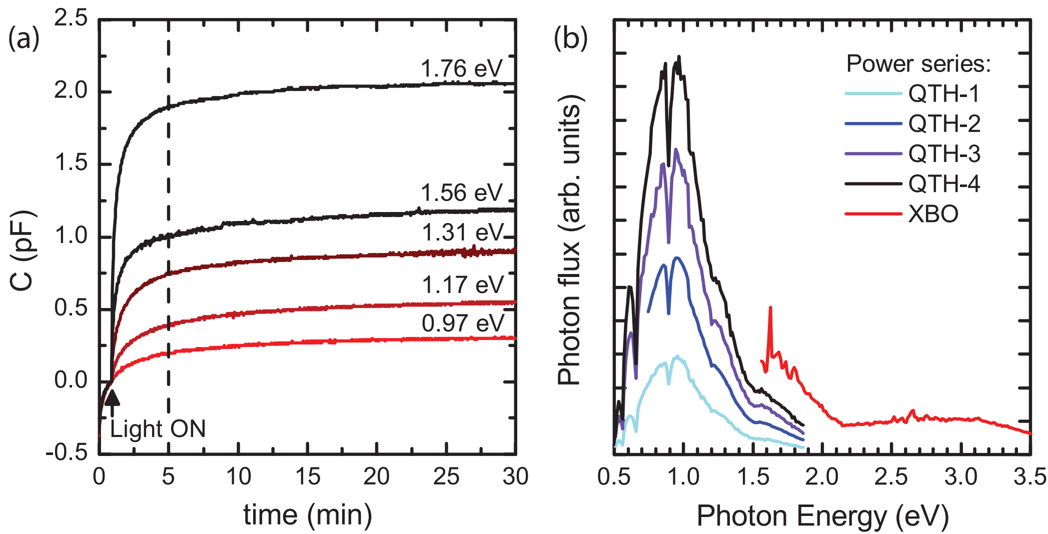

Figure 2.10: (a) Photocapacitance transients recorded over 30 min for some photon energies at 170 K. (b)Spectral dependence of the photon fluxes used for steady state photocapacitance measurements. The QTH-4 power series is the one used for the measurements shown in (a).

the light ionizes completely the traps occupied during the filling pulse, independently of the photon flux, if enough time is given to the system to reach a steady state. In this case, the transient amplitude can be considered directly proportional to the concentration of traps with depth lower or equal to the photon energy. In the case of a deep level with a well defined energy, the transient amplitude should be a step function. In the case of a gaussian distribution of deep levels, as is our case, the amplitude should increase more smoothly. The first step to take for the analysis of the transient amplitude is to determine how much time the illumination should last in order to obtain a saturated transient. The most critical transients are those recorded at low photon energies, as due to the dominant low optical cross section, a long time may be necessary to reach the steady state. For this purpose, 30 min long transients were recorded at 170 K for photon energies in the 0.9-1.8 eV range, as shown in Fig. 2.10(a). The quiescent bias, pulse voltage and pulse duration are identical to the ones used for the determination of the cross section. From the measurements it can be seen that the transients can be considered essentially saturated after 4 min. from illumination, even for the lower energies. This transient duration was therefore chosen for the measurement of the transient amplitude in the 0.5-3.5 eV range, with steps of 12 meV. As the measurements were done using the HP 4192 A LF instrument for capacitance measurements, the capacitance could be measured at 10 kHz. As pointed out by Py *et al.* [124], this relatively low frequency enhances the capacitance, making the transient larger and thus increasing the sensitivity. Measurements were also carried on for different photon fluxes, shown in Fig. 2.10(b), in order to assess the effect of illumination intensity. Five intensity series were used: four for the 0.5-1.9 eV range (QTH-1, QTH-2, QTH-3, QTH-4) and one for the 1.6-3.5 eV range (XBO). The light intensity could be modulated by manually acting on the monochromator slits. The transients shown in Fig. 2.7(e) and 2.10(a) have been taken using light intensities corresponding to the QTH-4 and

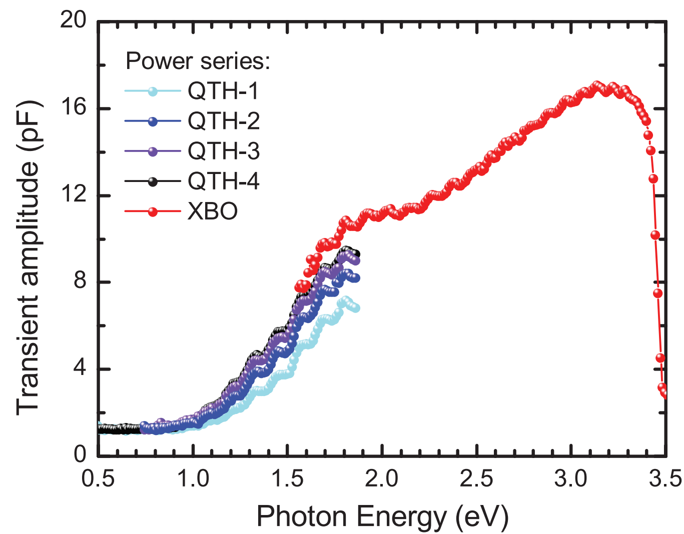

Figure 2.11: Steady-state photocapacitance spectrum of InAlN measured with different photon flux series. The amplitude of the transient is measured after 4 minutes from illumination.

XBO series. The resulting steady-state photocapacitance spectra are displayed in Fig. 2.11. As can be seen, the transient amplitude increases smoothly between ~ 0.8 eV and ~ 2 eV despite the decreasing photon flux, which is in agreement with a broad distribution of traps around 1.7 eV. A second increase in amplitude is observed for energies > 2.2 eV, which is in agreement with the increase in optical cross section above this energy (Fig. 2.8). However, as these transitions involve photon energies higher than half of the bandgap, caution must be taken for their interpretation, as mentioned above. In fact, for such energies not only transitions involving the conduction band are possible, but the valence band may participate too. Furthermore, for energies above 3.0 eV, or even slightly below, absorption in GaN is no more negligible, and measurements become impossible above 3.4 eV. It is finally interesting to note that, despite enough time was given to the system for reaching a quasi steady state, the transient amplitude depends on the photon flux. The dependence is sublinear, as a fourfold increase in photon flux resulted in only a 30% increase in transient amplitude, and is furthermore evidenced by the interference fringes visible all over the graphs of Fig. 2.11. A possible explanation for this behavior may be the ionization of traps below the Fermi energy. As shown schematically in Fig. 2.7(d) for the simpler case of a well defined trap energy, there is a transition region in the space-charge region where deep levels are occupied and the electron distribution has a tail due to band bending. When the light is switched on, these deep levels will be ionized, but at the same time will recapture electrons in this region [129, 130]. With increasing photon flux, the amount of traps that will be ionized in the steady state will increase, in turn increasing the amplitude of the transient. It is however important to note that, despite this dependence on the illumination intensity, the overall shape of the steady-state photocapacitance graphs is always the same. Therefore, even if a quantitative analysis is precluded, the qualitative statement expressed above that the steady-state photocapacitance spectrum is in agreement with the broad trap distribution inferred from the analysis of the cross section remains valid.

To conclude this section, it is interesting to note that Ooyama *et al.* [131] found a level with 1.52 eV optical ionization energy in $Al_{0.60}Ga_{0.40}N$, which has a band gap of 4.9 eV, close to the one of nearly lattice-matched InAlN. The two levels may thus have similar origin. Possible sources of the level were suggested by Ooyama *et al.* as Al-vacancies or oxygen impurities, as well as complexes of these defects with nitrogen vacancies. It is also worth mention that both Hacke *et al.* [132] and Klein *et al.* [133] found in GaN a broad level with ~ 2 eV optical ionization energy and large broadening, but could not assign it to any specific defect. Finally, a broad deep level with 1.3 eV optical ionization energy was found by McCluskey *et al.* [134] in $Al_{0.39}Ga_{0.61}N$ and attributed to oxygen. However, as oxygen was identified there as a DX-center, the broadening was attributed in that case to a large Franck-Condon shift, but the temperature dependence of the optical cross section was not explored. The nature of the deep levels band around 1.7 eV in nearly lattice-matched InAlN remains therefore quite uncertain.

3 Growth of InAlN/GaN heterostructures

This chapter deals with the growth of InAlN/GaN heterostructures. We will start with a description of the experimental techniques used for the growth and characterization of III-nitride based epilayers, and then pass to a detailed explanation of the growth of InAlN alloys in Sec. 3.2. The following sections will treat the growth of InAlN/GaN heterostructures on sapphire (Sec. 3.3), SiC (Sec. 3.4), and silicon (111) (Sec. 3.5) substrates.

3.1 Experimental techniques

3.1.1 Metal organic vapor phase epitaxy

Metal-organic vapor phase epitaxy (MOVPE) is the most widespread technique used for the growth of III-nitride based heterostructures. In MOVPE, the substrate on which the growth is performed is introduced in a reactor chamber and heated at the desired temperature. The metal-organic precursors of the elements that will constitute the growing crystal are then introduced by means of a carrier gas, usually H_2 or N_2. H_2 is the most widely used carrier gas, while pure N_2 is usually used for the growth of In-containing materials to avoid H_2 related In desorption phenomena. Trimethylgallium (TMGa), trimethylindium (TMIn) and trimethylaluminum (TMAl) are the most commonly used metal precursors. Nitrogen source is ammonia (NH_3). The precursors, as they reach the hot substrate surface, are decomposed in the corresponding elements or in smaller radicals that are adsorbed on the surface, and the elements are finally incorporated in the growing crystal while byproducts (methyl radicals, hydrogen atoms etc.) are eliminated. The growth rate and the composition of the growing material can be controlled by acting on the precursors flow and temperature. NH_3, being a gas, can be easily supplied from an appropriate bottle, and its flux can be directly controlled with a gas flow meter. On the other hand, the metal-organic precursors are liquid or solid at room temperature. Therefore, they are stored into special bottles called bubblers, where the carrier gas is introduced and gets saturated with the metal-organic vapor before coming out of the bottle and being injected in the reactor. The metal-organic precursor flow can be thus controlled by simply adjusting the flux of carrier gas passing in the bottle. The bubbler

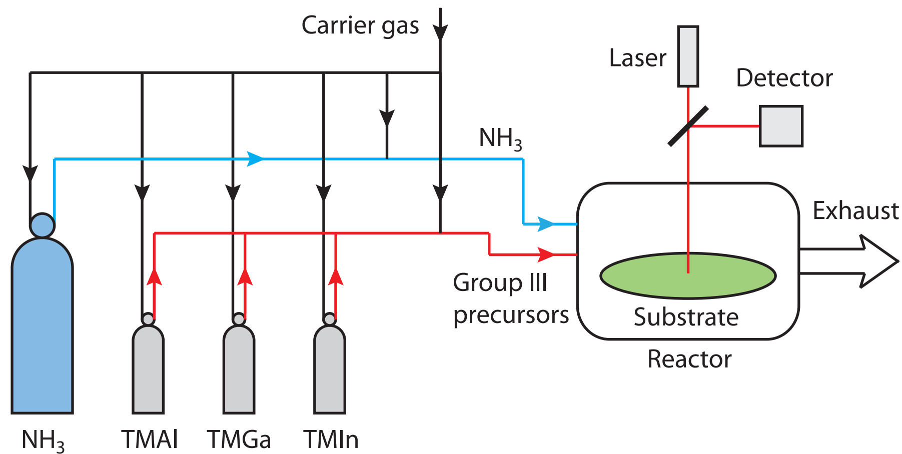

Figure 3.1: Schematic representation of the MOVPE reactor.

temperature must be controlled by means of a thermostatic bath in order to keep the metal-organic vapor pressure constant. Usually, the V/III ratio is kept to very high values because NH_3 has a low cracking efficiency and to prevent the decomposition of the crystal. It is finally important to notice that some impurity atoms, such as C, H, O and Si, will be inevitably incorporated in the crystal as they are released from the decomposition of the precursors (C for example) or from deposits present on the reactor walls (Si for instance) or are already present as impurities in the precursors (for example O, especially in TMAl) or in the carrier gas.

The growth temperature is a very important parameter in MOVPE. The temperature must be sufficiently high to allow for an efficient decomposition of the precursors, in particular NH_3, for an easy desorption of reaction byproducts and for a sufficient diffusion of the adsorbed species. On the other hand, a too high growth temperature will cause precursor decomposition before their arrival at the surface, and their desorption from the growth surface, thus reducing the growth rate. For these reasons, the typical growth temperature of III-nitrides lies between 700 °C for high In content alloys and 1200 ° for AlN. A last important parameter is pressure. MOVPE is usually performed at moderate pressures (50-200 mbar). While high pressures are desirable for high growth rates and reduced crystal decomposition, lower pressures are preferred for Al containing materials in order to limit gas phase parasitic reactions involving TMAl.

The samples described in this thesis have been grown with an AIXTRON 200/4 RF-S MOVPE system, which can handle wafers with 2 inch maximum diameter. The group-III precursors are introduced in the reactor separated from NH_3 in order to minimize parasitic gas phase reactions. The system is equipped with a laser reflectivity monitoring setup which allows to control *in situ* the thickness of the growing layer. A schematic of the system is presented in Fig. 3.1.

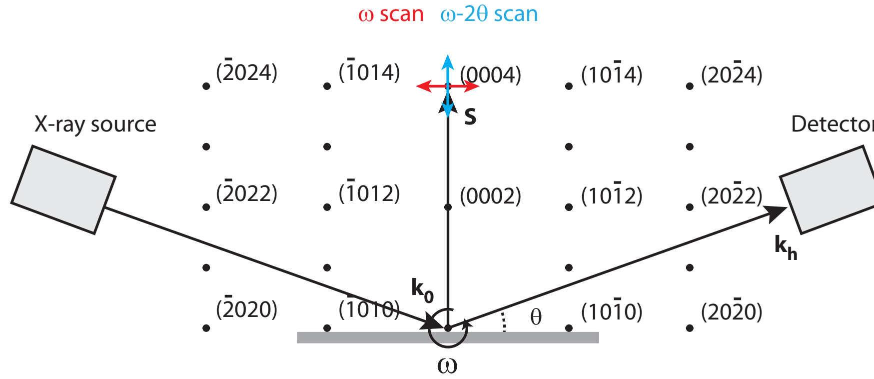

Figure 3.2: Schematic representation of X-ray diffraction experiments. $\mathbf{k}_0$, $\mathbf{k}_h$ and **S** represent the incident, diffracted and scattering wavevectors, respectively.

3.1.2 X-ray diffraction

X-ray diffraction (XRD) is a very powerful technique for the characterization of epitaxial layers and has been extensively used throughout this thesis work, in particular to measure the composition, thickness, and defect density of the epilayers grown by MOVPE. The instrument used is a Brucker New D8 Discovery. The principle of XRD is shown in Fig. 3.2. In XRD, an X-ray beam is generated by an X-ray tube and is sent to the sample, which diffracts the beam. A mobile X-ray detector collects the diffracted beam and measures its intensity. The instrument used in this work is furthermore equipped with an X-ray mirror for focusing the incident beam and with a set of monochromators for increased resolution. Both the sample and the detector can be moved. In particular, the sample can be tilted around the ω axis while the detector is moved in order to change the θ angle. Fig. 3.2 shows, together with the sample and the instrument's X-ray source and detector, the reciprocal space of the crystal under study and the incident ($\mathbf{k}_0$), diffracted ($\mathbf{k}_h$) and scattering (**S**) vectors. $\mathbf{k}_0$ and $\mathbf{k}_h$ have magnitude $1/\lambda$, where λ is the wavelength of the X-rays used ($\lambda = 1.54$ Å in our case). $\mathbf{S} = \mathbf{k}_h - \mathbf{k}_0$. The detector will register a non zero signal when the Bragg diffraction condition is fulfilled, i.e. when **S** points to a reciprocal space node or, equivalently, when $n\lambda = 2d\sin\theta$, where n is an integer and d is the separation between the planes of atoms corresponding to the diffraction spot observed.

Several types of XRD measurements can be performed. ω scans are measurements where the detector is kept fixed, while the sample is rotated around the ω axis. Such measurement configuration allows to explore the broadening of the diffraction spots in a direction perpendicular to the scattering vector. For $(000l)$ reflections, the FWHM of the diffraction peak is related to the tilt angle (β_{tilt}) between the grains constituting the crystal, while For $(l0\bar{l}0)$ reflections it is related to the twist angle (β_{twist}) between the grains. The broadening of other reflections is a combination of β_{tilt} and β_{twist} [135]. If the two angles are known, the screw and edge

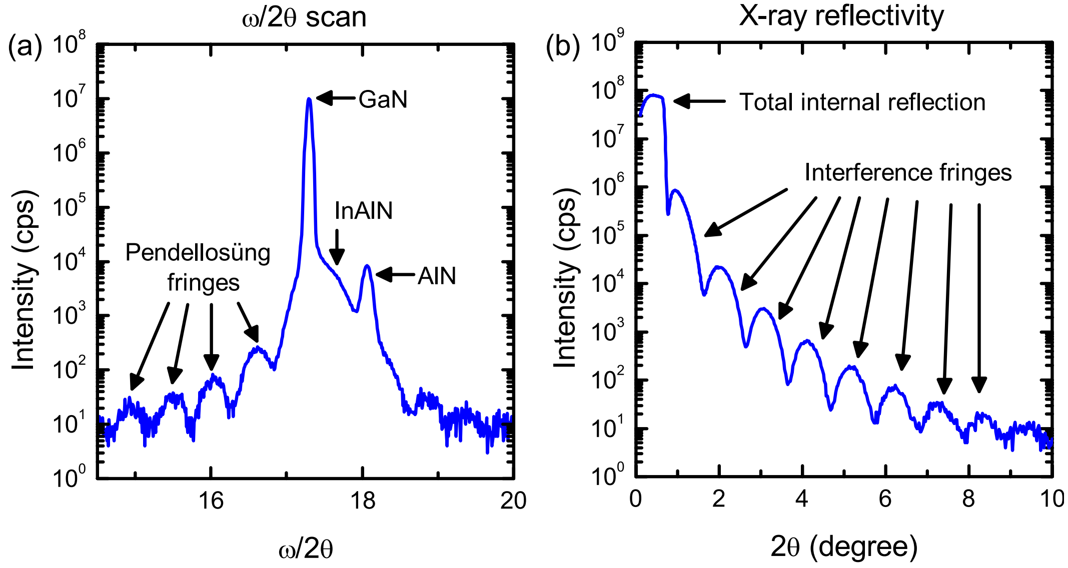

Figure 3.3: (a) $\omega - 2\theta$ spectra of the (0002) reflection of an InAlN/GaN heterostructure on sapphire with 8 nm total (AlN + InAlN) barrier thickness. (b) X-ray reflectivity spectra of the same layer.

dislocation densities (DD) can be extracted using the formulas of Dunn and Kogh [136]:

$$[\text{Screw} \quad \text{DD}] = \frac{\beta^2_{tilt}}{4.35 b_s^2} \qquad [\text{Edge} \quad \text{DD}] = \frac{\beta^2_{twist}}{4.35 b_e^2} \tag{3.1}$$

where $b_s = 5.185$ Å and $b_e = 3.189$ Å are the Burgers vector lengths for edge and screw dislocations, respectively. We will see in Sec. 3.3.2 a rigorous method for the extraction of the tilt and twist angles. However, this method has the drawback of being quite time consuming and furthermore the recording of $(l0\bar{l}0)$ ω scans requires a dedicated instrument for in plane XRD. These measurements have been performed at the University of Magdeburg in the group of prof. Alois Krost. Alternatively, we verified experimentally that a very good approximation of β_{tilt} and β_{twist} are given by the FWHM of the (0002) and $(2\bar{1}\bar{1}2)$ reflections, respectively. This method has been thus employed to obtain a quick and reliable estimation of the dislocation densities.

A second type of XRD measurement are $\omega - 2\theta$ scans, which consist in varying simultaneously and by the same amount the ω and the θ angles. This kind of measurement allows exploring the reciprocal space in the direction parallel to the scattering vector, as shown in Fig. 3.2. During this work, $\omega - 2\theta$ scans have been recorded only for the (0002) reflection. The result of a scan over an InAlN/GaN heterostructure on sapphire having 8 nm total (AlN + InAlN) barrier is shown in Fig. 3.3(a). The spectra is composed of several peaks, corresponding to the various materials constituting the multilayer. The GaN and AlN peaks are easily distinguished and their separation is due to the difference in c lattice parameters. InAlN, on the other hand,

gives rise to a broad peak with several interference fringes on both sides. These fringes, called Pendellosüng fringes, are due to the the low thickness of the barrier. From the period $\Delta\theta$ of the fringes the total thickness T of the barrier can be calculated:

$$T = \frac{\lambda}{2\Delta\theta\cos\theta} \tag{3.2}$$

The average composition of the barrier can be on the other hand obtained from the position of the main peak, in particular from its distance to the GaN peak. The GaN buffer can be indeed considered in most cases relaxed, and is taken thus as a reference for the calculation of the InAlN c parameter, from which the composition is extracted using Vegard's law (Sec. 1.1.1).

The last kind of measurement performed in this work is X-ray reflectivity. This measurement can be thought as an $\omega - 2\theta$ scan of the (0000) peak. The θ angle is therefore scanned around very low values, usually from 0° to 5°. The X-ray reflectivity spectra for the same InAlN/GaN heterostructure of Fig. 3.3(a) is shown in Fig. 3.3(b). For angles higher than the angle of total internal reflection, interference fringes can be observed. These fringes are due to the finite thickness of the barrier stack and their period $\Delta\theta$ can be used to determine the barrier thickness: $\Delta\theta = \lambda/2T$. There might be however a difference between the barrier thickness determined from the period of the Pendelosüng fringes and the one determined from X-ray reflectivity. The former corresponds indeed to just the thickness of the crystalline material, while the latter comprises any layer on top of the GaN buffer, crystalline or amorphous. By comparing the two thicknesses we can thus detect the presence of amorphous layers at the surface. We will see examples of this in chapter 4.

3.1.3 Atomic force microscopy

In AFM, a cantilever with a sharp tip is scanned over the surface of the sample, and the force between the surface and the cantilever is used to extract the desired information. Several types of measurement methods have been developed and a large variety of physical and chemical data can be extracted by AFM. In this work, we are only interested in the topography of the surface of InAlN/GaN heterostructures. For this, we used a Digital Instruments Nanoscope microscope in tapping mode. This measurement technique consists in probing the variations of the oscillation amplitude and phase of the cantilever as it scans the surface. From the data collected, the topography of the sample is reconstructed with sub nm precision in the direction perpendicular to the surface and the surface rms roughness is calculated. We will see throughout this chapter several examples of AFM images of the surface of InAlN/GaN heterostructures.

3.2 Growth of InAlN alloys

The growth of high quality InAlN alloys is a notoriously challenging task due to the strong difference in growth conditions between InN and AlN. The growth of InAlN has been mainly

explored by MOVPE. Much less work has been done regarding the growth of InAlN by molecular beam epitaxy (MBE). In this thesis, we considered the growth of InAlN based heterostructures exclusively by MOVPE.

The great difference between typical growth temperature of AlN (~1000° C) and InN (~600° C) is the main challenge in InAlN growth. An intermediate temperature is needed, but this has two main consequences. First, the Al adatom mobility is greatly reduced, while In adatom desorption is still high. The strong temperature dependence of In desorption rate on temperature makes the growth temperature the key parameter to control InAlN composition. Lowering the growth temperature results indeed in enhanced In incorporation, while Al rich alloys are obtained by increasing the growth temperature. Typically, the lattice-matching condition is obtained for growth temperatures of ~ 800° C, depending on the specific growth conditions used. A 10° C decrease in growth temperature translates into a 2% increase in In content [137]. The other growth parameters have a less important effect. Increasing the In flow results in increased In incorporation, but not indefinitely [138, 139]. This can be explained by means of a Langmuir like model, which predicts a saturation of the surface by In containing species for high TMIn fluxes, in analogy to what is observed for MBE [140]. It has been also found that an increased Al flux results in an increased In incorporation too [141]. This was attributed to an increased InAlN growth rate and a reduced In desorption rate. A high V/III ratio is furthermore important in order to avoid surface morphology degradation [138]. The carrier gas used for InAlN growth is generally pure N_2, as H_2 strongly decreases In incorporation [142].

Throughout this thesis, we performed the growth of nearly lattice-matched InAlN using the growth conditions developed by Carlin *et al.* [143]. The growth is performed under N_2, at a temperature of ~ 800° C, which is adapted from growth to growth in order to finely tune the In composition. The pressure was 75 mbar. This low pressure is necessary in order to avoid excessive TMAl parasitic reactions and it has been show that it helps reducing carbon incorporation [141]. A V/III ratio of 800 is used to maximize the alloy quality and the growth rate is 200 nm/h. In some cases, a reduced growth rate of 60 nm/h has been used, but no change in the properties of InAlN based heterostructures could be observed. It is finally worth noting that no unintentional Ga incorporation in the InAlN layer takes place in our case [144, 145], contrary to what can happen in certain reactors [146].

3.3 Growth of InAlN/GaN HEMTs on sapphire

The growth of high quality InAlN/GaN 2DEG heterostructures has been obtained for the first time using sapphire as substrate [68]. Although sapphire is not the best possible substrate for HEMT applications due to its low thermal conductivity, it is a very convenient substrate for III-nitride growth. Sapphire substrates are indeed available at low cost and are extremely electrically insulating. Thus, if power applications are not targeted, sapphire can still be a very interesting substrate for HEMT epitaxy. It is furthermore worth noting that sapphire is the standard substrate for GaN based LEDs, and the early development of both AlGaN/GaN and

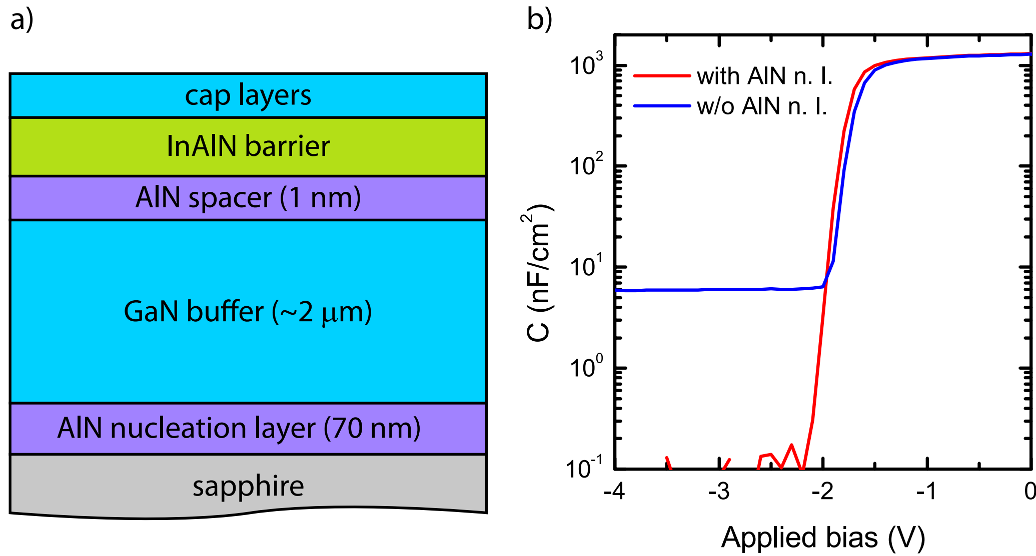

Figure 3.4: (a) Schematic structure of an InAlN/GaN heterostructure on sapphire. (b) Electrochemical CV measurement of two InAlN/GaN heterostructures with identical barrier stack. One is grown with an AlN nucleation layer (red line) and the other without (blue line).

InAlN/GaN based transistors has been mostly accomplished on sapphire substrates. Finally, sapphire is widely used for very high temperature and harsh environment applications due to its exceptional thermal and chemical stability.

3.3.1 Standard InAlN/GaN HEMTs on sapphire

Throughout this thesis, sapphire has been used as substrate for the growth of the InAlN/GaN based heterostructures that have been used for studying InAlN physical properties (results presented in Sec. 2.3), gate leakage currents (results presented in Sec. 4.3), as well as for the development of heterostructures integrating back barriers (Sec. 4.5) or *in situ* SiN passivation layers (Sec. 4.4). All these heterostructures share a common structure, which is shown schematically in Fig. 3.4(a). It consists, starting from the substrate, of an AlN nucleation layer, a GaN buffer layer, a 1 nm AlN spacer, a nearly lattice matched InAlN barrier and, in some cases, some cap layers.

Before starting the growth, the sapphire substrates are cleaned *in situ* by means of a 20 min annealing performed at 1200 °C under H_2. The AlN nucleation layer is then deposited with a two step method. First, 20 nm of AlN are deposited at 800 °C under H_2. The temperature is then raised to 1180 °C and the deposition of the AlN is continued up to a thickness of usually 70 nm. The use of an AlN nucleation in HEMT heterostructures instead of a low temperature GaN nucleation layer, which is quite standard for optoelectronic applications [147], is motivated by the need of a very insulating buffer and beneath layers. Low temperature GaN nucleation

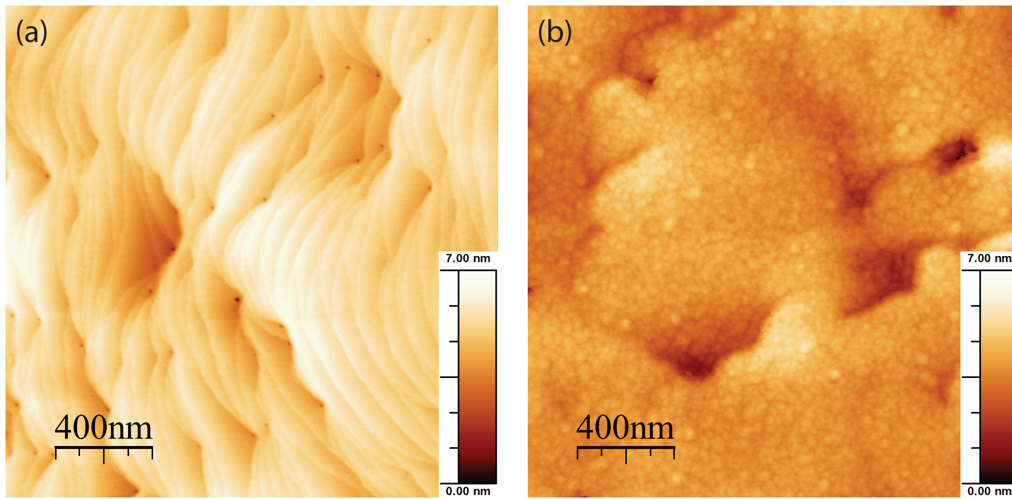

Figure 3.5: (a) 2 × 2 μm^2 AFM image of the surface of a 2 μm thick GaN buffer grown on sapphire. (b) AFM image of the surface of an InAlN/GaN heterostructure grown on sapphire.

layers on sapphire are indeed associated with the presence of parasitic mobile charges at the GaN/sapphire interface [105], which may degrade the insulating character of the buffer. The presence of such charges is evidenced by the electrochemical CV measurement presented in Fig. 3.4(b). For voltages lower than the pinch-off voltage, the capacitance does not fall to zero, but rather to a finite value which is consistent with the modulation of charges located at the GaN/sapphire interface. On the other hand, when an AlN nucleation layer is used, the capacitance falls beyond the instrument detection limit, demonstrating that no parasitic conductive charges are present at the interface with the substrate.

Once the nucleation layer completed, the buffer layer is deposited. In most cases, a 2 μm undoped GaN layer is used, grown under H_2 at 1060 °C at a rate of 2 μm/h. The quality of this layer is crucial for the 2DEG transport properties. In particular, the buffer layer determines the final surface rms roughness and the amount of threading dislocations that will cross the 2DEG. An AFM image of a typical GaN buffer is shown in Fig. 3.5(a). Steps are clearly visible, and the rms roughness is 0.5 nm, which is sufficiently low for guaranteeing high electron mobilities. The typical threading DD of such buffers is a few 10^9 cm^{-2}, with small run to run variations.

Once the buffer completed, the barrier stack is deposited. This starts with a 1 nm AlN spacer, necessary to avoid 2DEG mobility degradation due to alloy scattering (see Sec. 2.2.2), followed by the growth of an InAlN barrier of variable thickness. The InAlN growth is performed according to the conditions described in Sec. 3.2. Finally, a cap layer can be deposited. We will see examples of cap layer fabrication and use in Sec. 4.4. Fig. 3.5(b) shows the AFM image of the surface of an uncapped InAlN/GaN heterostructure on sapphire. If compared to the GaN buffer morphology of Fig. 3.5(a), we can't see steps any more, but rather small hillocks which are typical for InAlN surfaces. The the overall morphology is however comparable. The rms roughness is indeed 0.6 nm, very similar to the one of the GaN buffer. This shows that the

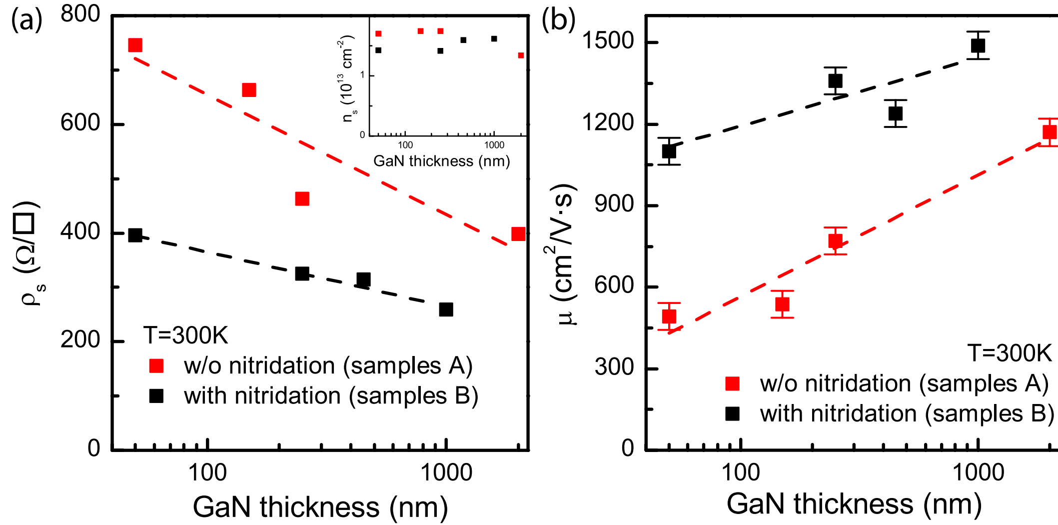

Figure 3.6: (a) Sheet resistivity and (b) Hall electron mobility for InAlN/GaN heterostructures variable GaN buffer thickness grown without (red squares - series A samples) or with (black squares - series B samples) sapphire nitridation. The inset of (a) shows the 2DEG density as a function of the GaN buffer thickness. The lines are guides for the eyes.

surface rms roughness can be taken as a good approximation of the interface roughness.

3.3.2 InAlN/GaN HEMTs with thin buffers

In most cases, GaN based HEMTs are grown on GaN buffers typically 2 μm thick. Such thick buffers are required in order to improve the GaN surface rms roughness and reduce the dislocation density. However, the degree of electrical insulation provided by undoped GaN is not optimal, resulting in buffer leakage currents. The resistivity of thick buffers can be increased by means of Fe-doping [35], C-doping [148] or through the introduction of AlGaN back barriers [149]. Another possible approach for reducing buffer leakage currents is to reduce the buffer thickness, as in thin buffer heterostructures the AlN nucleation layer acts as a back barrier. Furthermore, heterostructures with reduced total thickness can be easily etched down to the sapphire substrate. This constitutes an additional advantage as mesa isolation performed this way constitutes the best possible device isolation strategy [150]. Indeed, in this case the contact pads can be placed directly on the sapphire substrate, reducing buffer related leakage. The main challenge associated to the growth of heterostructures with reduced buffer thickness is however to assure good 2DEG transport properties.

The possibility of growing high quality InAlN/GaN heterostructures with thin buffers has been investigated by growing samples with buffer thickness varying between 50 nm and 2 μm. The growth scheme is analogous to the one used for standard heterostructures, described in the previous paragraph, and the total barrier thickness (AlN spacer + InAlN barrier) was kept constant to 6 nm. Particular attention was given to the early moments of the GaN growth on

the AlN nucleation layer. In particular, the GaN growth conditions were carefully optimized in order to ensure a fast coalescence of the growing GaN layer, which is of crucial importance if smooth GaN surfaces are desired together with thin buffer thicknesses. Furthermore, the control of the sapphire surface chemistry was found to be of critical importance for the realization of high quality 2DEGs, especially when using an AlN nucleation layer. This was evidenced by growing two series of samples with different reactor preparation procedures prior to the growth. In the first series (samples A) the MOVPE reactor and the sample holder were cleaned between two consecutive growths by means of a 20 min long bake at 1200 °C under H_2, while in the second series (samples B) the cleaning of the reactor was omitted and the AlN nucleation layer was grown on the sapphire substrate directly after the previous run. In this case the susceptor plate and the surrounding walls were coated by a thin layer of deposits. The room temperature Hall electron mobility and sheet resistivity for the two series of samples are shown in Fig. 3.6. An increase in the mobility with the thickness of the buffer layer can be observed in both series of samples, and a clear improvement of the transport properties is obtained for samples B. In this latter case, the mobility reaches 1100 $cm^2/V{\cdot}s$ at a GaN buffer thickness of only 50 nm, which is slightly lower than the state of the art value of 1490 $cm^2/V{\cdot}s$ achieved for the sample with 1 μm thick GaN buffer and more than twice the 490 $cm^2/V{\cdot}s$ measured on the sample A series. The corresponding 2DEG resistivity ρ_s is 356 $\Omega/\square$, and the sheet electron density is 1.56×10^{13} cm^{-2}. The sheet electron density for the whole set of samples is plotted in the inset of Fig. 3.6(a). Interestingly, the electron sheet density is nearly constant for all the samples, with an average value of 1.58×10^{13} cm^{-2}, fluctuations being not correlated to buffer thickness. The constancy of the 2DEG density is attributed to the constant barrier thickness, while the modest scattering of the values can be ascribed to variations of about 0.5 nm of the InAlN layer thickness, as InAlN/GaN heterostructures with sub-10 nm barriers are strongly sensitive to barrier thickness fluctuations.

In order to clarify how the reactor state can affect the sapphire surface chemistry, X-ray photoemission spectroscopy (XPS) experiments were performed on sapphire substrates that were annealed in the baked and unbaked reactor. The XPS spectra were obtained using the Al Kα line for excitation and are reported in Fig. 3.7. The Al_{2s} and Al_{2p}, the C_{1s} and the O_{1s} peaks can be clearly identified in both samples, together with a broad oxygen Auger O KLL line in the high energy part of the spectra. The N_{1s} peak could be found only in the sample annealed in the unbaked reactor, while no N related peak is discerned for the sample annealed in the baked reactor. These observations indicate that unexpected nitridation of the surface has occurred without NH_3 supply for the wafer annealed in the unbaked reactor. This suggests that nitridation of the sapphire surface occurs due to the release of N or N-containing species from the reactor walls when the wafer/susceptor is heated to high temperatures [151]. The impact of sapphire surface nitridation on the improvement of GaN material quality is well known [152]. The present results confirm the critical importance of sapphire surface chemistry and therefore the need for a perfectly well-controlled nitridation procedure. Considering these results, the two series of samples will be hereafter referred to as without or with nitridation.

The fundamental role of sapphire nitridation being established, it is necessary to clearly

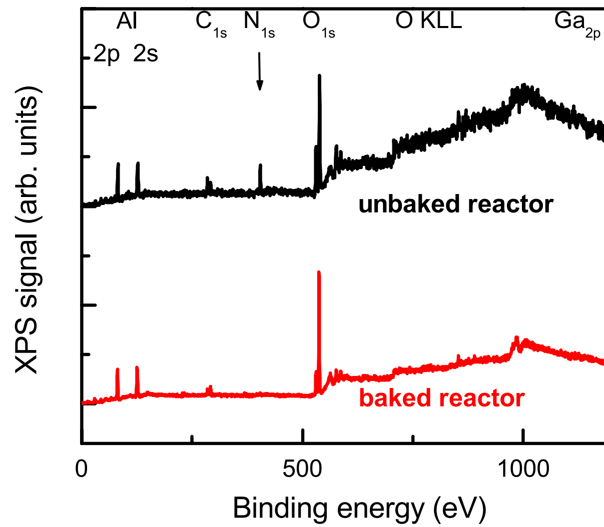

Figure 3.7: XPS spectra of the sapphire substrates annealed for 10 min at 1200 °C under H_2 in a baked (red curve) and unbaked (black curve) reactor. The N_{1s} peak, signature of sapphire nitridation, is found only in the latter spectrum.

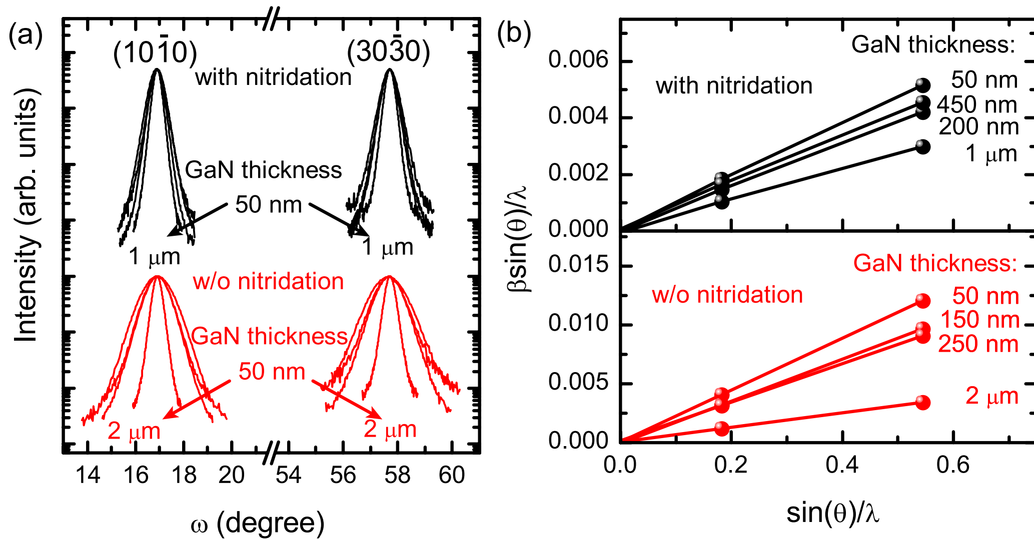

Figure 3.8: (a) ω scans, recorded in grazing incidence geometry, for the $(10\bar{1}0)$ and $(30\bar{3}0)$ reflections of GaN. Data are presented for both series of samples. (b) Corresponding Williamson-Hall plots [153] for the two series of samples. The twist angle is extracted from the slope of the lines. The negligible intercept of the fitted lines indicates that the broadening is completely dominated by the twist between grains, while the effect of finite grain size can be neglected.

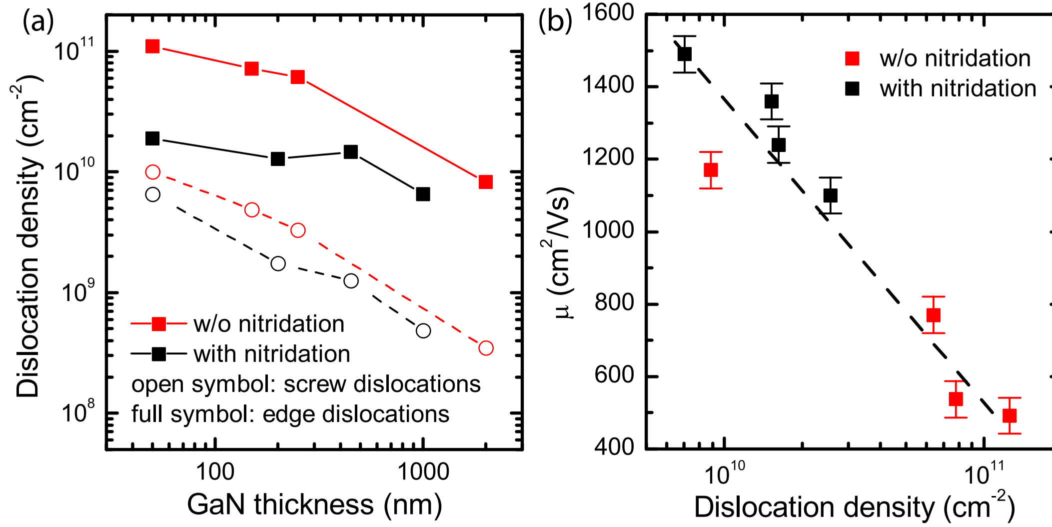

Figure 3.9: (a) Edge (full symbol) and screw (open symbol) dislocation density for the samples grown with and without sapphire nitridation as a function of the GaN buffer thickness. For both series of samples, the dislocation density diminishes as the buffer thickness increases. No significant difference in terms of screw dislocations is found between the two series of samples, while edge dislocations are significantly reduced by sapphire nitridation. (b) 2DEG electron mobility against the total (edge + screw) dislocation density.

understand what determines the difference in mobility between the various samples. We have seen in Sec. 2.2.2 that several mobility limiting scattering mechanisms are strongly dependent on the 2DEG density. Thanks to the low dispersion in electron density between the samples and the identical barrier composition, we can assume that phonon, alloy, and background impurity related scattering are constant at room temperature for all the heterostructures. On the opposite, the different GaN buffer thickness and sapphire preparation procedures are supposed to result in significant differences in DD and interface roughness. These two parameters constituted therefore the focus for the analysis of the room temperature electron mobility.

Edge and screw threading dislocation density were quantified from the twist and tilt angles extracted from XRD measurements. In particular, the twist angle was extracted from the FWHM of $(l0\bar{l}0)$ reflections ($l = 1,3$) measured in the grazing incidence geometry, while the tilt angle was extracted from the FWHM of symmetric $(000l)$ reflections ($l = 2,4,6$). Fig. 3.8(a) shows for example the $(10\bar{1}0)$ and $(30\bar{3}0)$ scans for the two series of samples considered. In order to to separate the contribution of the twist/tilt angle and the broadening due to the finite grain size to the FWHM of the diffraction lines, we performed in both cases a Williamson-Hall analysis [153]. The analysis consists in plotting $\beta \sin\theta/\lambda$, where β is the FWHM of the reflection and θ the corresponding Bragg diffraction angle, versus $\sin\theta/\lambda$ for the different reflections considered. The data are fitted with a straight line and the slope gives directly the twist/tilt angle if $(l0\bar{l}0)$ or $(000l)$ reflections are considered, respectively. Fig. 3.8(b)

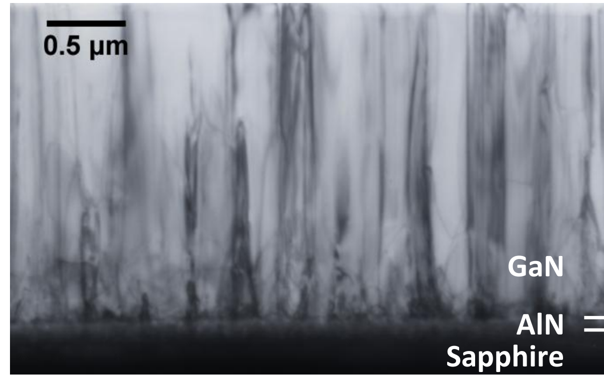

Figure 3.10: Cross sectional TEM image of the sample having a 2 μm thick GaN buffer grown without sapphire nitridation. The image is taken under two-beam diffraction condition with $\mathbf{g} = 01\bar{1}0$ in order to evidence edge component dislocations.

shows the Williamson-Hall plots built from the data of Fig. 3.8(a), from which the twist angle is extracted. It is worth noting that the intercept of the fitted line is zero with good approximation. Indeed, the FWHM of $(10\bar{1}0)$ and $(30\bar{3}0)$ reflections were nearly identical. This shows that the broadening is completely dominated by the twist angle, while the effect of finite grain size can be neglected. The same conclusion could be drawn for (0002) reflections. Once β_{twist} and β_{tilt} known, the threading dislocation density was extracted using Eq. 3.1.

The DD values are summarized in Fig. 3.9(a) as a function of the GaN buffer thickness for both series of samples. As can be observed, screw dislocations are approximately one order of magnitude less dense than edge dislocations, and both types decrease as the buffer thickness increases. Furthermore, a marked reduction in edge DD is observed in the series of samples grown on nitridated sapphire substrates, confirming the beneficial role of sapphire nitridation for the growth of high quality nitride layers. The effect is maximum in the heterostructures with the thinnest, 50 nm buffers, where the edge DD is decreased by nearly one order of magnitude, from 1.1×10^{11} to 1.9×10^{10} cm^{-2}. On the opposite, there is no marked difference in screw DD between the two series of samples. As the estimate of the DD from XRD data may be significantly affected by correlation between dislocations [154], cross sectional transmission electron microscopy (TEM) imaging was performed on the 2 μm thick sample grown without nitridation. More in detail, two-beam diffraction conditions were used, with $\mathbf{g} = 01\bar{1}0$ in order to evidence edge component dislocations. The corresponding image is shown in Fig. 3.10. The amount of dislocations crossing the top part of the GaN buffer, where the 2DEG is located, is quantified based on the estimated thickness of the TEM sample of ~ 300 nm. A density ~ 10^{10} cm^{-2} is extracted, in good agreement with the value of 8×10^{9} cm^{-2} obtained from XRD measurements. Furthermore, a higher DD can be observed in the lower part of the buffer, which agrees with the increase of about one order of magnitude deduced from XRD measurements. Therefore, the TEM analysis fully confirms the accuracy of our XRD experiments.

Fig. 3.9(b) shows the electron mobility of our samples against the total DD. A good correlation

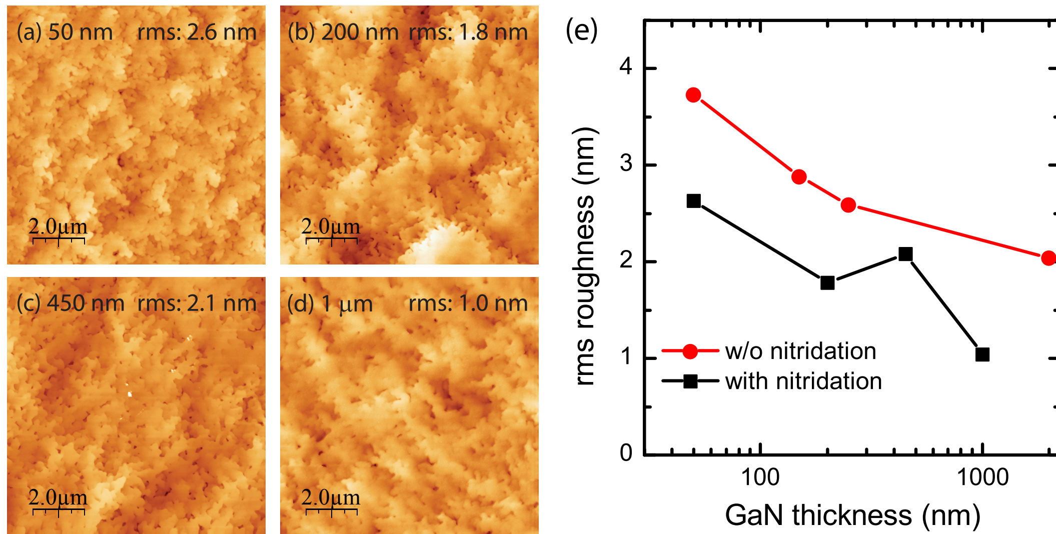

Figure 3.11: (a)-(d) 10×10 μm^2 AFM images of the surface of the samples grown with sapphire nitridation. Each figure reports the GaN buffer thickness and the surface rms roughness. (e) Surface rms roughness as a function of the GaN buffer thickness for the two series of samples.

is observed, with the electron mobility decreasing smoothly as the DD increases. Similar trends have been recently reported by Kaun et al. [57] in AlGaN/GaN heterostructures. At a first glance, these results seem to point out a decisive role of charged dislocations in the determination of the mobility, which contrasts markedly with the results of Sec. 2.2.3. However, it must be noted that interface roughness is one of the most important mobility limiting factors in high density 2DEGs, and that a correlation may exist between DD and interface roughness. The relationship between room temperature electron mobility and interface roughness was therefore investigated in order to get a deeper understanding of these heterostructure properties. Interface roughness was estimated here looking at the surface rms roughness deduced from AFM. Figs. 3.11(a)–3.11(d) show 10×10 μm^2 AFM images of the surface of samples grown on nitridated sapphire. A rough surface is observed, which for a buffer thickness of 50 nm is likely caused by the large amount of threading dislocations and the proximity of the coalescence area (rms roughness of 2.6 nm). A progressive surface smoothening occurs as the buffer gets thicker, with the surface roughness reaching 1 nm for the 1 μm thick sample. Fig. 3.11(e) displays the surface rms roughness against the GaN buffer thickness for both series of samples, showing that the samples grown on a nitridated substrate have smoother surfaces. Fig. 3.12(a) displays the measured surface roughness as a function of the DD, showing that there is a tight relation between the two parameters: at higher DD the surface roughness gets larger. The room temperature electron mobility for the whole set of samples is displayed as a function of the surface roughness in Fig. 3.12(b), showing a monotonous decrease of the electron mobility as the interface roughness increases. Considering the pretty good correlation between room temperature electron mobility, DD, and surface roughness, a modeling of the scattering mechanisms was necessary in order to establish which between the two parameters dominates the evolution of the electron mobility. According to Matthiessen's rule (Eq. 2.12),

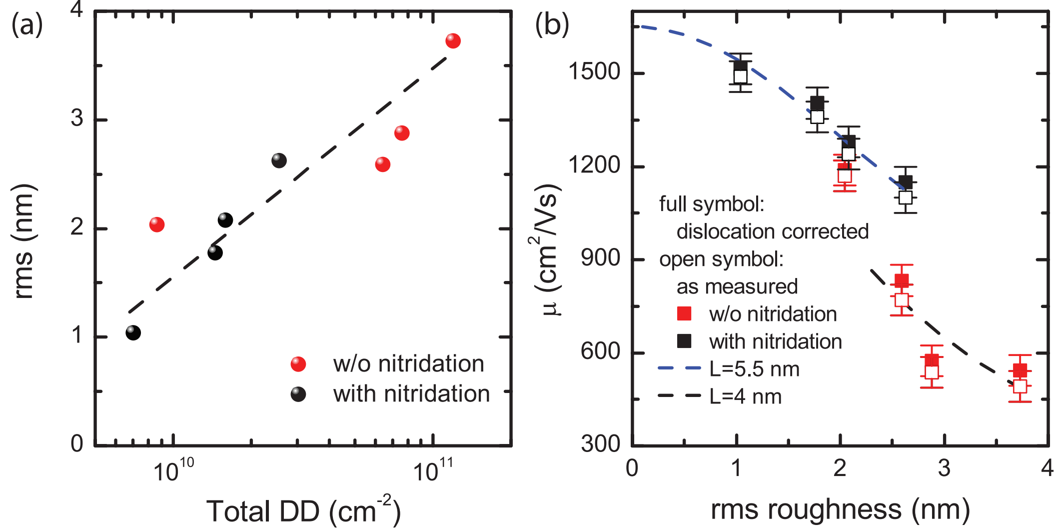

Figure 3.12: (a) Correlation between surface roughness and total dislocation density. (b) 2DEG electron mobility plotted against the surface rms roughness. Open symbols represent experimental values, showing a monotonous decrease of the 2DEG mobility as the surface rms roughness increases. Full symbols represent the mobility values after subtraction of the scattering by charged dislocations contribution. The last set of data is fitted using a surface correlation length of 5.5 nm (blue line, lower rms values) and 4 nm (black line, higher rms values).

the room temperature mobility μ can be written as

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_{disl}} + \frac{1}{\mu_{ir}} \tag{3.3}$$

where μ_{disl} is the dislocations limited mobility, μ_{ir} is the interface roughness limited mobility, and μ_0 is the sum of phonon, alloy, and background impurity scattering limited mobility which, as discussed previously, can be considered constant for our samples, thanks to the low dispersion of the electron density. As discussed in Sec. 2.2.2, alloy scattering is negligible, thanks to the presence of the AlN spacer. Taking into account an average electron density of 1.58×10^{13} cm^{-2} and a background impurity level of 10^{16} cm^{-3}, we calculate $\mu_0 = 1650$ cm^2/V·s by means of Eq. 2.13, 2.14, 2.16. μ_{disl} was calculated using Eq. 2.18 as the total DD was known for each sample. Concerning the calculation of μ_{ir} (Eq. 2.15), all the necessary parameters are known except for L. Therefore, in order to determine the relative importance of μ_{disl} and μ_{ir}, we used the following approach: we first calculate μ_{disl} for our set of samples and subtract its contribution from the experimental mobility via the Matthiessen's rule, obtaining a "dislocation corrected" mobility that is plotted against the surface rms roughness in Fig. 3.12(b). As can be seen, the obtained values are just slightly higher than the experimental ones, confirming that scattering by charged dislocations is playing a minor role even for the layers with the largest amount of dislocations. The corrected mobilities are then fitted by combining through the Matthiessen's rule μ_0 and μ_{ir}. As reported in Fig. 3.12(b), $L = 5.5$ nm

fits quite well the mobility of the samples with the lower roughness, while for rougher samples a lower correlation length of 4 nm is found. While a lower correlation length is consistent with rougher surfaces, additional scattering mechanisms may play a role in 2DEGs with very rough surfaces. For example, strong piezoelectric fields are expected to be present at step edges, causing significant carrier scattering. In any case, the present results clearly show that in our set of heterostructures the evolution of the 2DEG mobility is strongly dominated by interface roughness scattering, while scattering by charged dislocation has a minor importance. However, a strong correlation between DD and 2DEG mobility is observed, which is due to the increased interface roughness in highly dislocated layers.

In conclusion, the results presented in this section clearly show the decisive role of interface roughness on the transport properties of InAlN/GaN based 2DEGs. A reduction of the DD is fundamental for the improvement of interface roughness and thus of the electron mobility. A proper control of the initial growth steps is therefore essential for obtaining heterostructures with reduced threading dislocation densities and high mobilities, especially if layer stacks with thin buffers are desired.

3.4 InAlN/GaN HEMTs on SiC

The growth of InAlN/GaN heterostructures on SiC substrates presents many analogies with the growth on sapphire substrates. The heterostructures share indeed in most cases the same layer sequence. The growth starts therefore with the deposition of an AlN nucleation layer, followed by the growth of the GaN buffer and finally by the deposition of the barrier stack. During this thesis, only 2 μm thick buffers have been considered for growth on SiC. However, despite the analogies with heterostructures grown on sapphire, heterostructures grown on SiC substrates are generally characterized by smoother surfaces. Fig. 3.13(a) shows the surface morphology of a GaN capped heterostructure on SiC. The barrier stack is composed of 1 nm AlN spacer, 3 nm InAlN barrier and 2 nm GaN cap. The surface is very smooth (rms roughness = 0.2 nm). If compared to the surface of the heterostructure on sapphire discussed in the previous section, the better quality offered by SiC is evident.

Fig. 3.13(b) shows the X-ray diffraction spectra relative to the (0002) and $(2\bar{1}\bar{1}2)$ reflections. From the FWHM of the two ω scans, screw and edge dislocation densities of 1.3×10^8 and 1.1×10^9 cm^{-2}, respectively, are evaluated. The total DD is thus 1.2×10^9 cm^{-2}. The relatively low DD obtained on SiC is thus probably at the origin of their better surface morphology. The layer presented here is characterized by a sheet electron density of 1.63×10^{13} cm^{-2}, an electron mobility of 1470 cm^2/V·s and a sheet resistivity of 260 $\Omega/\square$. This is comparable to the best heterostructures on sapphire, despite the better surface morphology and the lower DD. However, this is not surprising. Indeed, as can be inferred from Fig. 3.12(b), for rms roughness < 1 nm an improvement in surface morphology does not lead to important improvements in electron mobility. Nevertheless, the superior thermal conductivity of SiC makes it the platform of choice for the realization of high performance GaN based HEMTs.

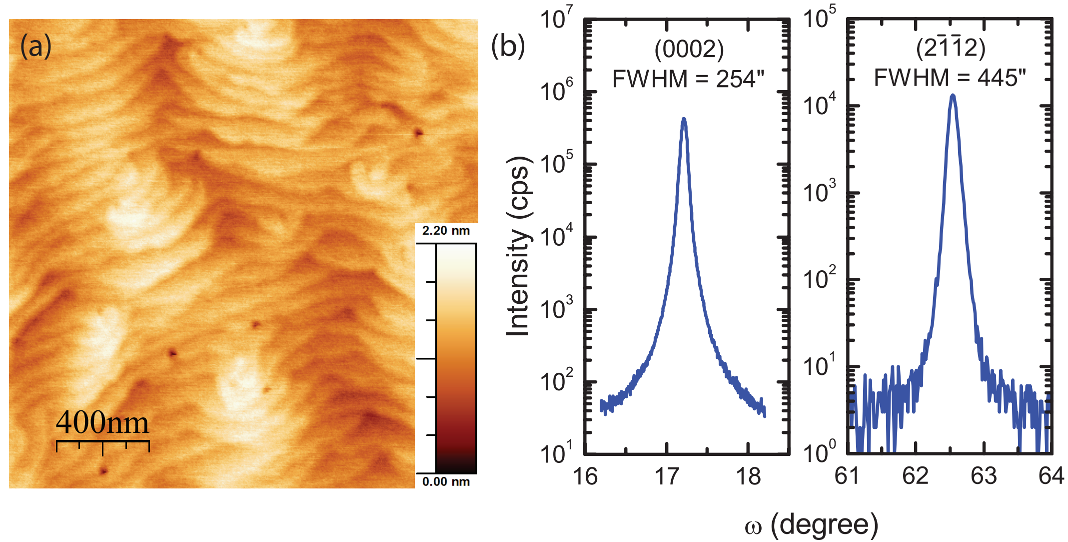

Figure 3.13: (a) $2 \times 2\ \mu m^2$ AFM image of the surface of a GaN capped InAlN/GaN heterostructure grown on SiC. (b) ω scans of the (0002) and (2$\bar{1}\bar{1}$2) reflections of the same layer with their FWHM.

3.5 InAlN/GaN HEMTs on Si

The growth of GaN based epilayers on Si(111) substrates is notoriously challenging due to several factors. The large difference in lattice constant between Si and GaN is the cause of very high threading dislocation densities, while the large difference in thermal expansion coefficients between the two materials is associated to cracking issues. Indeed, during the cooling step from growth temperature to room temperature, the nitride layers are put under strong tensile stress as their thermal expansion coefficient is higher than the one of Si. Therefore, if appropriate strain management techniques are not adopted, the epilayers tend to relax the tensile strain by cracking. An example of a cracked nitride on Si layer is shown in Fig. 3.14(a). It is therefore imperative to contrast the build up of such important strain in order to avoid cracking. Several approaches have been developed, all with the aim of introducing a compensating compressive stress in the nitride stack. In all cases, this is obtained by growing the GaN buffer on a strain management layer comprising one or more AlN or Al-rich layers. The simplest technique consists in growing the GaN buffer on an AlN layer, analogously to what is currently done for the growth on sapphire or SiC. The smaller lattice constant of AlN with respect to GaN puts indeed the GaN buffer under compression. However, the strain is progressively relaxed as the buffer is grown thicker, and the maximum buffer thickness that we could reach without incurring in cracks is ~ 500 nm. The limited buffer thickness results thus in high threading DD and in rough surfaces, which ultimately lead to non optimal transport properties, analogously to the case of Sec. 3.3.2. Fig. 3.14(b) shows an AFM image of the surface of a layer of that kind. Thicker, crack free layers with better crystal quality can be obtained by inserting low temperature AlN interlayers in the GaN buffer [155], or by means

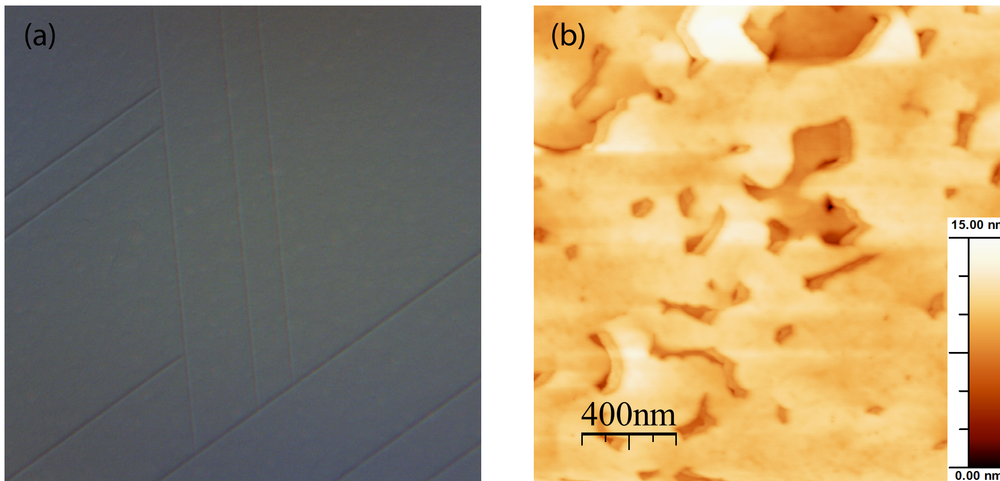

Figure 3.14: (a) Optical microscopy image of a cracked GaN layer on Si. (b) 2×2 μm^2 AFM image of the surface of an InAlN/GaN heterostructure on Si with 500 nm GaN buffer.

of short period AlN/GaN superlattices [156]. However, the high polarization induced sheet charge densities associated with AlN/GaN interfaces have the main drawback of introducing parasitic mobile carriers in the buffer, degrading its semi-insulating character.

An alternative approach makes use of a continuously or step graded AlGaN layer as strain management layer [157]. This approach has the advantage of allowing at the same time the growth of thick enough GaN buffers while the composition gradient is associated to negative fixed polarization induced charges which are equivalent to a compensating p-type doping. The wide band gap of the AlGaN constituting the strain management layer can furthermore act as a back barrier. Such technique could be applied with success, during this thesis, for the realization of InAlN/GaN heterostructure with good transport properties. The continuously graded AlGaN strain management layer gave the best results. The typical layer stack adopted is shown in Fig. 3.15(a). The growth starts with a ~ 50 nm AlN nucleation layer, necessary as the direct growth of GaN on Si is not possible due to the Ga melt back etching phenomena happening when Ga comes in contact with Si. For the same reason, the reactor is baked prior to each growth in order to remove Ga containing species from the reactor walls. If the reactor is not baked, some Ga can be released from the reactor walls during the heat up phase, coming in contact with the virgin Si surface and triggering undesired reactions. Once the AlN nucleation layer completed, the AlGaN graded layer is grown. The best results were obtained with a 1 μm thick AlGaN layer uniformly graded from pure AlN to pure GaN. Then, the GaN buffer is grown using standard growth conditions. The maximum possible thickness allowing for crack-free layers is 2 μm, i.e. a total nitride stack thickness of 3 μm. However, a 1 μm GaN buffer is sufficient for good transport properties, thicker buffers do not lead to better results. The growth is then completed with the deposition of the barrier layer stack.

Fig. 3.15(b) shows the AFM image of the surface of a GaN capped InAlN/GaN on Si heterostructure with 2 μm total nitride stack thickness. For this particular heterostructure, the total barrier

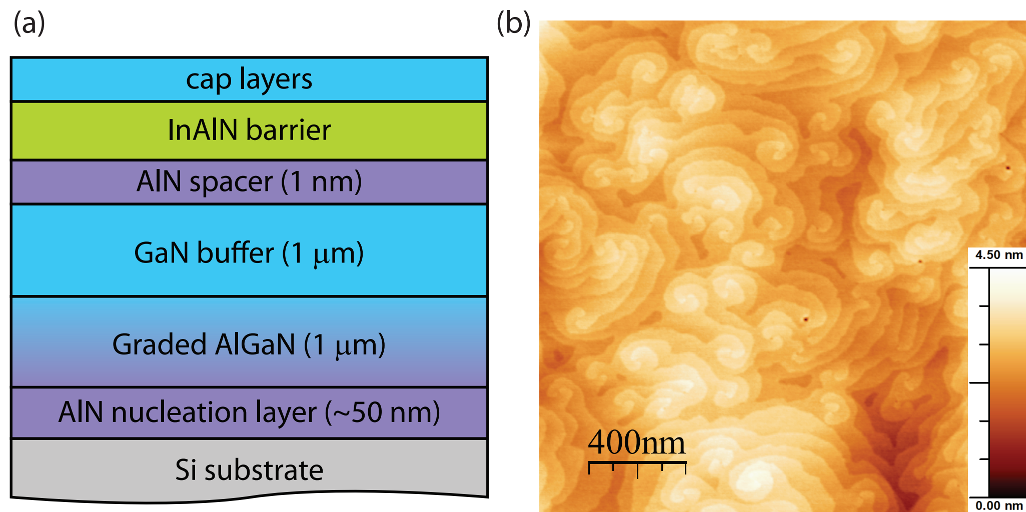

Figure 3.15: (a) Schematic structure of an InAlN/GaN heterostructure on silicon with graded AlGaN strain management layer. (b) 2×2 μm^2 AFM image of the surface of an InAlN/GaN heterostructure on Si of that kind.

thickness is 6 nm, and the layer can be thus compared directly with the one on SiC presented in the previous paragraph. Compared with the layer on SiC of Fig. 3.13(a), the surface is clearly rougher (rms roughness = 0.7 nm), and a higher threading DD can be inferred. The higher defect density is confirmed by the high FWHM of (0002) and $(2\bar{1}\bar{1}2)$ rocking curves, 731" and 1735", respectively, corresponding to a total DD of 1.7×10^{10} cm^{-2}. As expected, this translates in lower transport properties with respect to analogous layers on SiC. The sheet electron density is 1.6×10^{13} cm^{-2}, well comparable to the one of the SiC based layer. We have indeed seen in Sec. 3.3.2 that the 2DEG density is not affected by the materials quality. The electron mobility is instead significantly lower: 1190 cm^2/V·s, to be compared to the 1470 cm^2/V·s of the layer on SiC, which can be thus attributed to the higher interface roughness associated to the higher threading DD. However, the mobility is lower than the one predicted by Fig. 3.12(b). A possible explanation may be a lower correlation length. The sheet resistivity is 320 $\Omega/\square$. A better mobility and thus a sheet resistivity comparable to the one of 2DEGs grown on sapphire or SiC may be therefore possible if the threading DD could be reduced by ~ 1 order of magnitude. However, as we will see in chapter 5, despite their lower transport properties, InAlN/GaN HEMTs on Si achieved performance equivalent to SiC based devices.

Other experiments with different AlGaN layer thicknesses or non uniform composition gradings were attempted, but with worse results. Step graded AlGaN layers were also explored, but with inferior results. However, excellent results with such step graded layers have been obtained by other groups [158], meaning that further optimizations are worth investigation.

4 InAlN/GaN HEMTs: building blocks

After having treated the growth of InAlN/GaN heterostructures, this chapter will deal with the physics of the principal building blocks of InAlN/GaN HEMTs. We will begin by treating the metal-semiconductor contacts found in HEMTs. The focus will be first on ohmic contacts, which constitute the source and drain contacts. Two types of ohmic contacts will be described and compared, namely annealed and regrown ohmic contacts. The second type of metal-semiconductor contacts covered will be Schottky contacts, which are the ones used for the gate electrode. Much of the discussion will deal in particular with the modeling of reverse bias leakage currents which are at the origin of gate leakage currents. Once the metal-semiconductor contacts covered, we will study the issues related to the growth of *in situ* SiN passivated heterostructures. In particular, the stability of InAlN/GaN heterostructures under SiN MOVPE deposition conditions will be discussed and the fundamental role of appropriate capping techniques for the achievement of *in situ* passivated heterostructures with state of the art transport properties will be discussed. Finally, the last section will cover the integration of back-barriers for enhanced 2DEG confinement. We will in particular treat the growth strategies needed for obtaining heterostructures with high electron mobilities. The results treated in this chapter constitute the basis of the InAlN/GaN HEMTs discussed in the next chapter.

4.1 Experimental techniques

4.1.1 Schottky diode fabrication

Schottky diodes are two terminal devices where one of the contacts to the semiconductor is an ohmic contact, while the other is a Schottky contact. The details concerning the physics of ohmic and Schottky contacts are discussed in Sec. 4.2 and 4.3. The fabrication of Schottky diodes on InAlN/GaN heterostructures proceeds as follow. First, the heterostructure surface is cleaned with acetone and isopropanol in order to remove organic contaminants. A second cleaning with buffered HF and HCl is then performed in order to remove surface oxides. Once the surface cleaned, the ohmic contact pattern is formed by standard photolitography, the

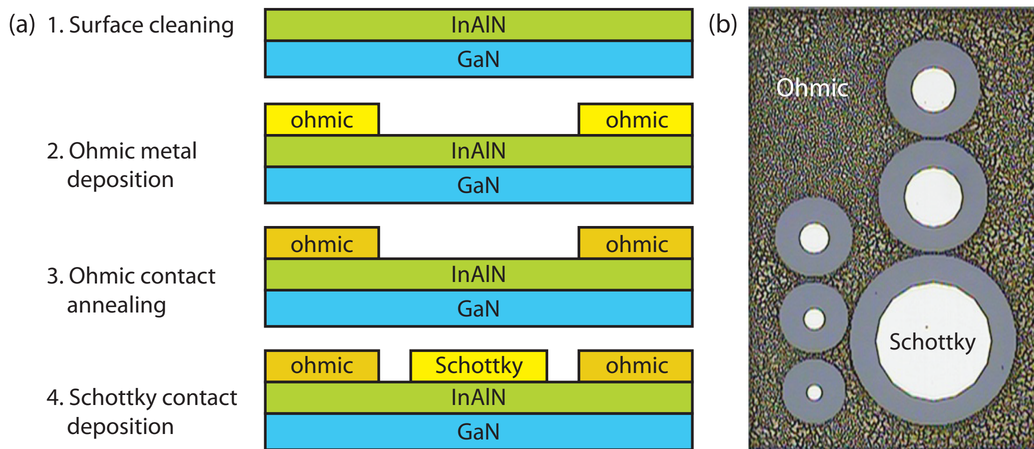

Figure 4.1: (a) Schottky diode fabrication steps and (b) optical microscope image of a fabricated Schottky diode set.

surface is deoxidized with diluted HCl and the Ti/Al/Ni/Au ohmic stack is deposited by e-beam evaporation. After metal lift-off, ohmic contacts are formed by rapid thermal annealing (RTA) of the ohmic stack at 850 °C for 30 s under N_2 in a Jipelec Jetfirst instrument. The diodes are finally completed by forming the Ni/Au Schottky contact. The contact are patterned by photolitoghraphy, the surface is deoxidized by diluted HCl and finally the Ni/Au bilayer is deposited by e-beam evaporation. The fabrication procedure is sumarized in Fig. 4.1(a). In this work we used circular Schottky contacts with diameters in the 50-400 μm range. An optical microscope picture of a fabricated Schottky diodes set is shown in Fig. 4.1(b).

4.1.2 Molecular beam epitaxy of regrown contacts

MBE is a growth technique where molecular or atomic beams of the elements constituting the growing crystal are evaporated from Knudsen cells and then reach the substrate where they condense and react, incorporating the growing crystal. The substrate temperature, also referred to as growth temperature, is thus sensitively lower than the cell temperature. The pressure in the growth chamber must be also low enough to make the mean free path of the evaporated elements longer than the cell-substrate separation. This is achieved under ultra-high vacuum conditions ($P < 10^{-8}$ mbar) and is a fundamental requirement to avoid parasitic reactions in the gas phase. The high vacuum conditions of MBE furthermore allow the use of *in situ* characterization tools which are not compatible with MOVPE. In particular, reflection high-energy electron diffraction (RHEED) can be be performed allowing the monitoring of the growth rate and the surface morphology with monolayer precision.

MBE of III-nitrides differentiates markedly with respect to MBE of classical III-V semiconductors as nitrogen atoms can not be supplied by evaporating a solid source. Two solutions to this issue have been developed, giving birth to two different MBE techniques. In ammonia MBE (NH_3-MBE) NH_3 is the nitrogen source, and nitrogen atoms are supplied by the

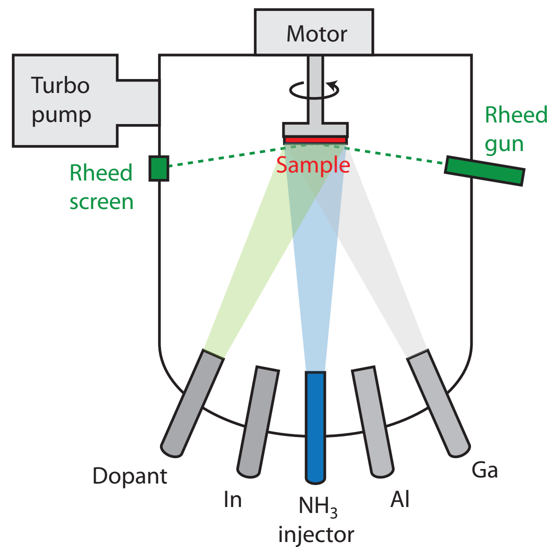

Figure 4.2: Schematic representation of an NH_3-MBE system.

pyrolysis of NH_3 at the hot substrate surface. In order for this reaction to be efficient, the growth temperature must be higher than 500 °C. At lower temperatures the NH_3 cracking efficiency is negligible, while at higher temperatures it increases and saturates to ~ 4% above 600 ° [159]. The typical growth temperatures for GaN by NH_3-MBE are in the 700-900 °C range. For higher temperatures, GaN evaporation is no more negligible. A schematic representation of an NH_3-MBE system is shown in Fig. 4.2. In Plasma-assisted-MBE (PAMBE) nitrogen atoms are on the other hand generated by a N_2 plasma cell, where the N_2 molecules are broken in the constituent atoms. With respect to NH_3-MBE, PAMBE can be performed at lower temperatures as the constraints related to the pyrolysis of the nitrogen precursor are absent. Therefore, the growth of GaN can be performed by PAMBE at temperatures as low as 500 °C. A second difference between NH_3-MBE and PAMBE is that NH_3-MBE is generally performed under N-rich conditions, while PAMBE under Ga-rich conditions. In this thesis, NH_3-MBE has been used as the growth tool for the achievement of regrown ohmic contacts. The results are discussed in Sec. 4.2.2.

4.2 Ohmic contacts

Ohmic contacts are an essential part of HEMTs as they provide electrical access to the 2DEG. They therefore contribute, in most cases significantly, to the source and drain resistance and for this reason the main parameter used for their characterization is the contact resistivity. We will see in this section two methods for the fabrication of ohmic contacts, comparing their advantages and disadvantages.

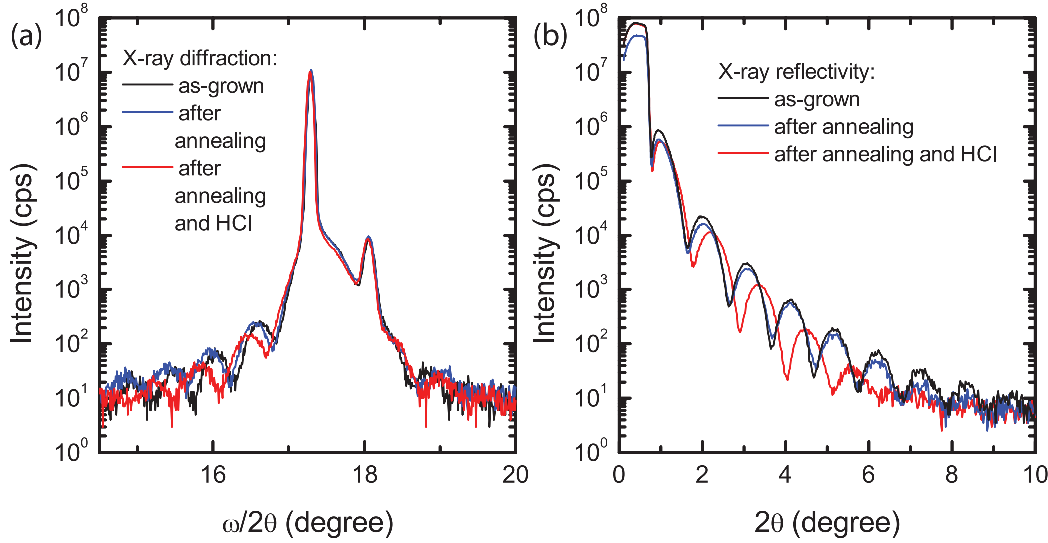

Figure 4.3: (a) $\omega/2\theta$ scans of the (0002) reflection and (b) X-ray reflectivity of an heterostructure with 8 nm total barrier thickness at different processing steps.

4.2.1 Annealed contacts

The simples and most widespread method for ohmic contact formation on GaN based heterostructures consists in depositing a Ti/Al based metal stack which is then annealed at high temperatures (800-900 °C) for a short time (< 1 min) [160]. A Au layer is usually deposited on top of the metal stack to prevent Al oxidation and a refractory metal is often inserted between the Ti/Al bilayer and the Au top layer in order to prevent intermixing [161–164]. In this work we used a Ti/Al/Ni/Au multilayer (16/64/40/50 nm) annealed under N_2 for 30 s at 850 °C. The resulting contact morphology is quite rough, as can be seen from the optical image of Fig. 4.1(b) and the typical contact resistivity is 0.6 Ω·mm. It is important to note that by careful optimization of the annealing conditions other groups could obtain much lower contact resistivities of ~ 0.3 Ω·mm. However, such optimizations have been already extensively discussed and are beyond the scope of the present work. A point that has not been not investigated in depth is the effect of the high temperature annealing on InAlN/GaN heterostructures. Therefore, X-ray diffraction and reflectivity measurements were performed after Ohmic contact processing steps in order to reveal any effect on the crystal quality. The results are presented in Fig. 4.3. Fig. 4.3(a) presents $\omega/2\theta$ scans of the (0002) reflection, while Fig. 4.3(b) shows the corresponding X-ray reflectivity spectra. The heterostructure examined was an InAlN/GaN one with 8 nm total barrier thickness and no cap layer. The top layer was therefore InAlN. The main feature of interest of the spectra of Fig. 4.3 is the period of the interference fringes. As already discussed in Sec. 3.1.2, the period of the Pendellösung fringes in $\omega/2\theta$ scans gives the thickness of the crystalline material constituting the barrier, while the period of interference fringes of X-ray reflectivity spectra gives the total thickness of the barrier stack, including any amorphous layer. For the as-grown layer, the two thicknesses are in perfect agreement and equal to 8.2 nm. After the ohmic annealing step, however, some difference could be detected.

While the X-ray reflectivity determined thickness did not change, the one obtained from $\omega/2\theta$ scans was lower by 0.5 nm, as can be inferred from their wider spacing. This shows that the high temperature annealing, although performed in inert atmosphere, induces the formation of a thin amorphous layer at the surface. This layer is completely removed by a 1:1 HCl:H_2O treatment. Indeed, after this wet treatment the barrier thicknesses determined with the two methods are again in agreement and equal to 7.2 nm. Therefore, in the Schottky contact processing of Sec. 4.1.1, the Schottky metal is deposited on a clean and crystalline InAlN surface.

These results indicate that annealed Ohmic contacts, despite being relatively simple to fabricate, can have an impact on the InAlN/GaN heterostructure. Furthermore, the contact resistivity that can be achieved by careful optimization of the annealing conditions is usually limited to about 0.3 Ω·mm. Overcoming this limit is the main motivation for the implementation of regrown ohmic contacts.

4.2.2 Regrown contacts

We have seen in Sec. 1.4.2 that the access and output resistance limit HEMT performance (Eq. 1.35 and 1.36) and as contact resistivity is a major part of such parasitic resistances, its reduction is highly desirable. The regrown contact method, first proposed by Shinohara *et al.* [165], has not only allowed a significant reduction of the contact resistivity down to 0.1 Ω·mm, but has also made possible the achievement of HEMTs with source-drain spacing as short as 140 nm [83]. The 2DEG contribution to the access and output resistance is thus further reduced and HEMTs with cutoff frequencies exceeding 400 GHz have been achieved this way [54]. Regrown ohmic contacts have thus become a requirement for ultrafast GaN based HEMTs. The regrowth scheme consists in selectively etching the barrier in the contact region and a few tens of nm of the GaN buffer, followed by the regrowth of heavily n-doped GaN ($\sim 10^{20}$ cm^{-3}), which is then easily contacted with metals. Before this work, the only reports available were all dealing with PAMBE as growth technique. No high quality regrown contacts have been obtained by MOVPE yet. This might be related to higher growth temperatures, which impose a higher thermal budget to the underlying structures. With respect to these two techniques, NH_3-MBE is an attractive alternative, as it combines the advantages of both PAMBE and MOVPE. Contrary to PAMBE, it is characterized by stable and reliable N-rich growth conditions like MOVPE and at the same time features low growth temperatures, which is a key advantage for regrowth technologies. The achievement of low resistivity regrown ohmic contacts by NH_3-MBE is the topic of this section.

The first step towards the realization of low resistivity regrown ohmic contacts was to found the appropriate growth conditions for highly doped, low resistivity n^+-GaN. This has been done by growing 90-100 nm thick n^+-GaN layers by NH_3-MBE on semi-insulating GaN-on-sapphire templates previously grown by MOVPE. The transport properties of such layers were then studied by Hall effect in order to obtain the carrier density n, their mobility μ and the

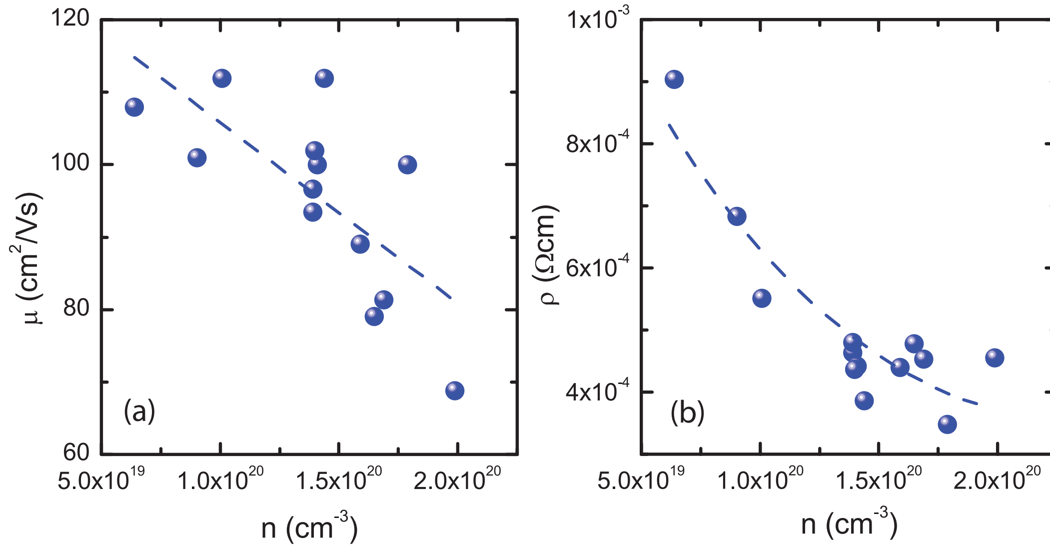

Figure 4.4: (a) Mobility and (b) resistivity of highly Si-doped GaN layers grown by NH_3-MBE as a function of carrier density. Dashed lines are guides to the eyes.

bulk resistivity ρ. The growth conditions were optimized for a growth temperature of 700 °C, which was chosen for two reasons. On one hand, this temperature is sufficiently high to ensure a sufficient NH_3 cracking efficiency and adatom mobility [159]. On the other hand, it is sufficiently low to avoid thermal damage to HEMT layers. We will see indeed in Sec. 4.4 that a high temperature annealing can cause degradation of InAlN/GaN based 2DEGs, which motivates the use of low growth temperatures. An NH_3 flux of 50 sccm was used for all growths and ensured N-rich conditions, i.e. a Ga flux limited growth rate and stable growth conditions with no risk of Ga droplets. The main parameters used to control the doping level of NH_3-MBE grown GaN were thus the Si and Ga cell temperatures. Increasing the Si cell temperature results in increased Si effusion and thus higher Si incorporation. For what concerns the Ga cell temperature, it is used to directly control the GaN growth rate: higher Ga cell temperatures translate in higher GaN growth rates. At a fixed Si impinging rate, lowering the GaN growth rate results in higher doping levels as the ratio between the impinging Si and Ga atoms increases. Therefore, highly doped GaN is obtained with high Si cell temperatures and low GaN growth rates. In this specific case, doping levels $> 5\times10^{19}$ cm^{-3} could be obtained with Si cell temperatures ranging between 1240 and 1285 °C and growth rates as low as 80 nm/h. The electron mobility and resistivity of the grown layers are shown in Fig. 4.4 as a function of the carrier density, which varies between 5×10^{19} cm^{-3} and 2×10^{20} cm^{-3}. The electron mobility is between 69 and 112 cm^2/V·s and decreases at higher doping. ρ follows the same trend and reaches a value of 3.5×10^{-4} Ω·cm for a doping level of 1.8×10^{20} cm^{-3}. The resistivity tends to saturate around this value for very high doping levels due to impurity scattering that affects the mobility. Those results are consistent with published data on highly Si-doped PAMBE [166] and NH_3-MBE [44] grown GaN bulk layers.

For the structure with the lowest resistivity, we performed secondary ion mass spectrometry

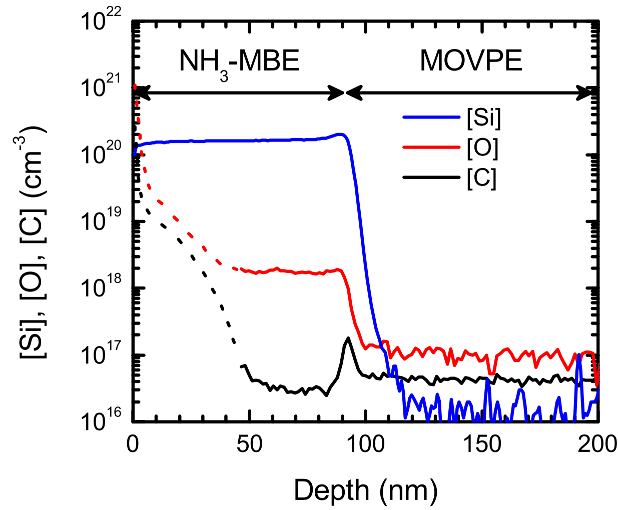

Figure 4.5: [Si], [O] and [C] profile measured by SIMS on the layer with the lowest resistivity ($\rho = 3.5 \times 10^{-4}$ Ω·cm, $n = 1.8 \times 10^{20}$ cm^{-3}, $\mu = 100$ cm^2/V·s). [O] and [C] for depths below 50 nm are affected by surface artifacts and are therefore represented by dotted lines.

(SIMS) analysis in order to access the impurity profile, which is shown in Fig. 4.5 for Si, C and O. It can be seen that the Si profile is flat in the doped region and the measured [Si]=1.7×10^{20} cm^{-3} is consistent with the 1.8×10^{20} cm^{-3} carrier concentration measured by Hall effect. The Si concentration decreases sharply at the regrowth interface and approaches the detection limit of $\sim 10^{16}$ cm^{-3} in the semi-insulating GaN layer. O and C concentrations in the highly doped region are $\sim 2 \times 10^{18}$ cm^{-3} and $\sim 3 \times 10^{16}$ cm^{-3}, respectively. These values refer to the depths in the 50 to 90 nm range, as for lower depths the measurement is affected by surface artifacts (dotted lines). Interestingly, [C] does not change significantly when passing from semi-insulating GaN grown by MOVPE to highly doped GaN deposited by NH_3-MBE. However [O] increases significantly. This value is much higher than the residual concentration (typically a few 10^{17} cm^{-3}) measured in undoped GaN grown by NH_3-MBE with standard growth conditions (growth temperature > 800 °C) [159]. One reason could be the combination of lower growth temperature and the high temperature of the Si cell, leading to O-containing species outgassing.

Once the NH_3-MBE growth conditions were optimized, they were applied to the realization of regrown ohmic contacts on InAlN/GaN heterostructures. For this purpose, the heterostructure used was grown on SiC by MOVPE as described in Sec. 3.4 and was composed of an AlN nucleation layer, a 2 μm thick GaN buffer and a barrier stack consisting of a 1 nm AlN spacer, a 3 nm InAlN barrier and a 2 nm GaN cap. The sheet electron density was 1.6×10^{13} cm^{-2}, the electron mobility 1500 cm^2/V·s and the sheet resistivity 260 $\Omega/\Box$. The contacts were processed for transmission line measurements (TLM) in order to extract the different components of the contact resistance. Two types of TLM structures were fabricated, shown in Fig. 4.6. The first structure (Fig. 4.6(a)) was processed starting with mesa definition by Cl_2 based dry etching. Then, a SiO_2 mask was deposited by plasma enhanced chemical vapor deposition

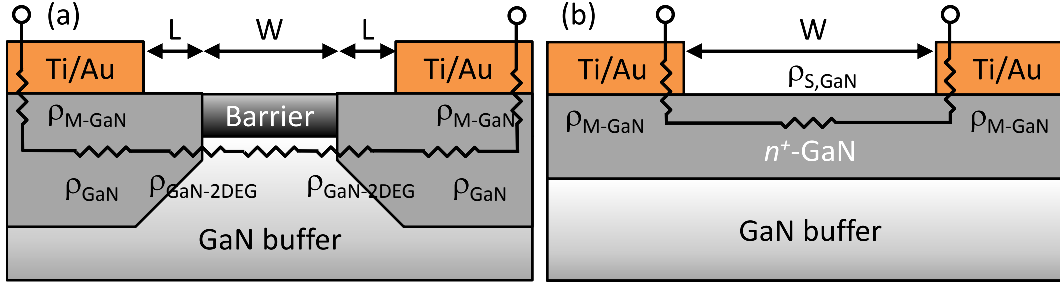

Figure 4.6: (a) Schematic of the TLM structures used for the extraction of ρ_{TOT}. (b) Structure used for the extraction of ρ_{M-GaN} and $\rho_{s,GaN}$.

(PECVD), followed by the opening of the TLM pattern by optical lithography and SF_6-based dry etching. The heterostructure was finally recessed in the contact region by Cl_2-based dry etching. First, we tried to perform the regrowth directly after the contact region recess etching and standard cleaning with organic solvents. This resulted in a very rough surface, as shown in the SEM picture of Fig. 4.7(a), and a very poor contact to the 2DEG. Therefore, wet surface preparation methods were tested. Best results in terms of surface morphology and electrical contact have been obtained with a 10 min piranha solution (1:4 H_2O_2:H_2SO_4) treatment followed by water rinsing. A typical, 90 nm thick, regrown layer implementing this surface preparation procedure is shown in Fig. 4.7(b). As can be seen, the GaN surface is smooth, and the regrowth is very selective, as no GaN growth on the SiO_2 mask could be detected. The GaN surface is smooth and the regrown material nicely contacts the borders, which are the most critical region as they constitute the interface with the 2DEG. Some small pits are however still visible, indicating that there is room for improvement, especially regarding surface preparation methods. After regrowth, the SiO_2 mask was removed with diluted HF and the TLM structure was completed with the evaporation of Ti/Au metal pads. The spacing L between the metal and the 2DEG was here 1 μm, while the contact spacing W is varied in order to allow the extraction of the the contact resistivity, which was 0.25 Ω·mm. Here, the contact resistivity ρ_{TOT} is the sum of the metal/n^+-GaN resistivity (ρ_{M-GaN}), the resistivity of the n^+-GaN layer connecting the metal to the 2DEG (ρ_{GaN}), and the n^+-GaN/2DEG interface resistivity ($\rho_{GaN-2DEG}$): $\rho_{TOT} = \rho_{M-GaN} + \rho_{GaN} + \rho_{GaN-2DEG}$. From this TLM structure it is therefore not possible to obtain the individual components of the contact resistivity. The second TLM structure, shown in Fig. 4.6(b), allows to obtain the values necessary for the decomposition. The structure is obtained by first etching the barrier stack everywhere, exposing thus the buffer over which the regrowth takes place. The final Ti/Au metallization with variable spacing W is finally deposited. This structure allows to extract ρ_{M-GaN} and the sheet resistivity of the regrown GaN layer ($\rho_{s,GaN}$). The measured ρ_{M-GaN} = 0.08 Ω·mm compares well with previous reports [166], and the obtained $\rho_{s,GaN}$ = 60 Ω/□ is consistent with the bulk resistivity of n^+-GaN described above. We have now sufficient elements in order to calculate the remaining components of ρ_{TOT}. ρ_{GaN} is evaluated to 0.06 Ω·mm considering the values of $\rho_{s,GaN}$ and L. We can thus finally obtain $\rho_{GaN-2DEG} = \rho_{TOT} - \rho_{GaN} - \rho_{M-GaN}$ = 0.11 Ω·mm. This value is close to published data obtained by PAMBE [167] and proves the feasibility of low

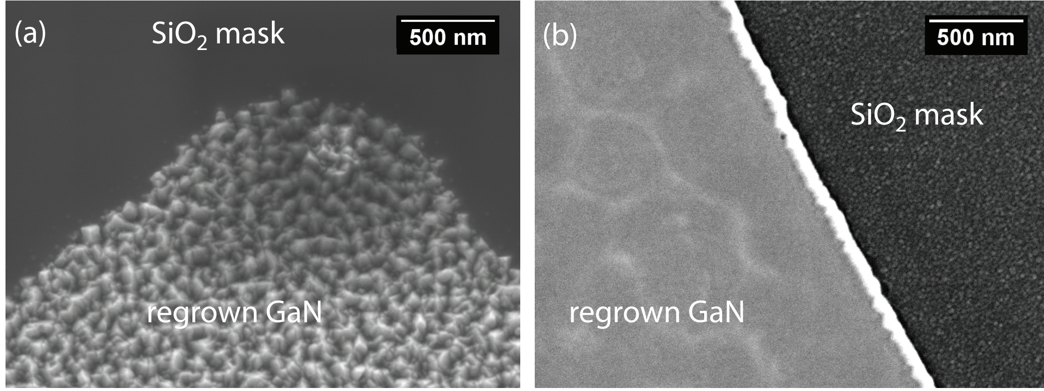

Figure 4.7: Regrown n^+-GaN morphology (a) without any surface preparation after contact region recess etching, and (b) in the case of surface preparation with piranha solution prior to regrowth.

Table 4.1: Components of the contact resistivity extracted from TLM measurements

ρ_{M-GaN}	0.08 Ω·mm
ρ_{GaN}	0.06 Ω·mm
$\rho_{GaN-2DEG}$	0.11 Ω·mm
ρ_{TOT}	0.25 Ω·mm

resistivity contacts by NH_3-MBE. The different components of ρ_{TOT} are summarized in Table 4.1. ρ_{TOT} could be improved by a self aligned process as this would reduce drastically the ρ_{GaN} contribution. The $\rho_{GaN-2DEG}$ term may be also reduced with some improvement of the surface preparation procedure. Therefore, total contact resistivities < 0.2 Ω·mm are a realistic future goal. Finally, we also performed post regrowth Hall effect measurements in order to assess potential impact on the 2DEG transport properties. We measured a 2DEG density of 1.8×10^{13} cm^{-2}, a mobility of 1460 cm^2/V·s, and a sheet resistivity of 240 Ω/□. The nice agreement with the pristine 2DEG properties indicates that the regrowth process did not harm the heterostructure quality. Examples of HEMTs integrating regrown ohmic contacts by NH_3-MBE will be presented in chapter 5.

4.3 Schottky contacts

The gate electrode in HEMTs is essentially a Schottky contact, i.e. a metal-semiconductor junction with blocking characteristic. The role of the gate electrode has been described in chapter 1, where the deleterious effect of gate leakage currents have been also discussed. The aim of this section is to investigate the origin of such parasitic currents. It is important to note that other reports have been published concerning gate leakage currents in InAlN/-GaN heterostructures. Song *et al.* [168] invoked In segregation around screw-component dislocations as the cause of gate leakage but without presenting any quantitative conduction

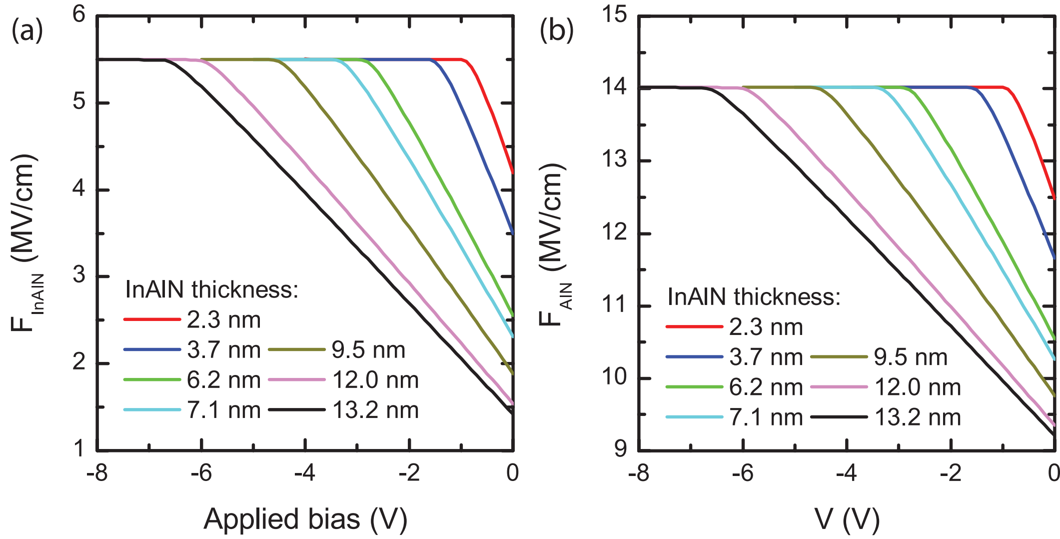

Figure 4.8: Calculated electric field in (a) the InAlN barrier and (b) in the the AlN spacer as a function of the applied voltage for the set of samples considered.

model. Arslan *et al.* [122] and Chikhaoui *et al.* [121] proposed instead Poole-Frenkel emission, with activation energy of 0.13 eV, from a deep level to a continuum of dislocation associated states located 0.37 eV below the InAlN conduction band edge. However, their model allowed fitting the reverse bias current-voltage curve only at low voltages. More recently, Ganguly *et al.* [123] successfully modeled the whole reverse bias current-voltage characteristic but using two different mechanisms for the low and high voltage portion. In particular, they used a modified Poole-Frenkel model for low reverse bias and Fowler-Nordheim tunneling for the higher voltages. A prominent role of tunneling has been also underlined by Arslan *et al.* [169] and Donoval *et al.* [170] for conduction under forward bias. It is important to stress the fact that in all these reports only a single heterostructure was considered each time, and in some cases only a portion of the reverse current-voltage characteristics is examined. This motivated a deeper study which is presented in this section.

Gate leakage currents were studied through the analysis of the reverse bias current-voltage characteristic of Ni/InAlN/GaN Schottky diodes fabricated on the InAlN/GaN heterostructures that have been used in Sec. 2.3 for the extraction of several InAlN related physical parameters. The barrier thickness, In composition and transport properties of such heterostructures have been presented in Table 2.1. It is important to note that the processing of Schottky diodes, in particular the ohmic contact annealing step, induced a loss of 1 nm InAlN, as detailed in Sec. 4.2.1. The thicknesses of the InAlN barrier layers were therefore not the ones of Table 2.1 bur rather 2.3, 3.7, 6.2, 7.1, 9.5, 12.0 and 13.2 nm. The pinch-off voltage of these Schottky diodes has been already presented in Fig. 2.5(b) as a function of the barrier thickness and has been used for the evaluation of the Schottky barrier Φ_S, which turned out to be 2.8 eV. The physical parameters derived in Sec. 2.3 constitute the basis of gate leakage current modeling. Indeed, modeling of the current-voltage characteristics of Schottky diodes relies on the knowledge of

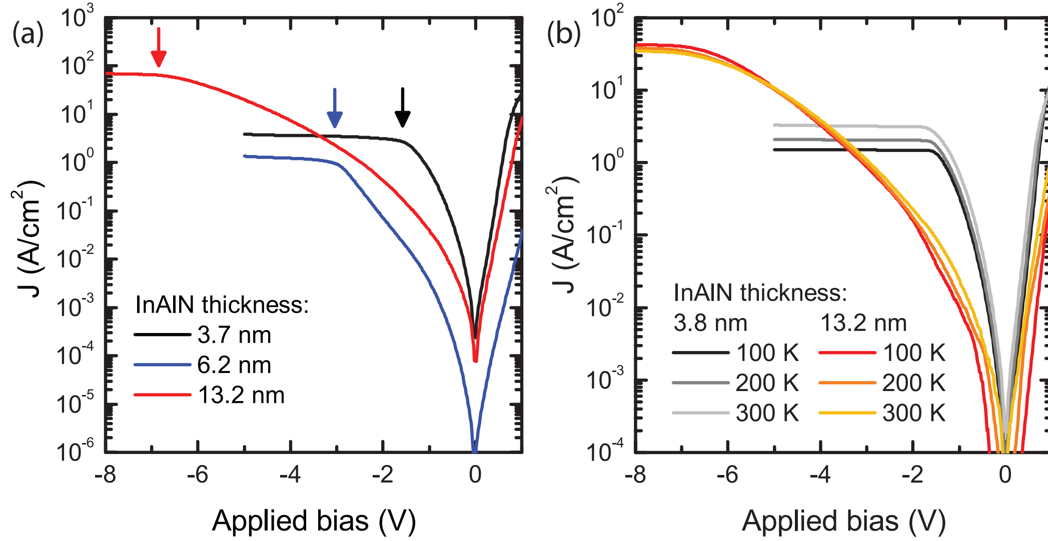

Figure 4.9: (a) Representative room temperature current-voltage characteristics for the different classes of devices. The first class of diodes (2.3, 3.7, and 7.1 nm InAlN thicknesses) is represented by the black curve and shows a steep, nearly exponential increase of the current under reverse bias. The second class of devices (9.5, 12.0, and 13.2 nm InAlN thicknesses) is represented by the red curve and has a much more curved current-voltage characteristic. In both cases, the current saturates at pinch-off (marked by the arrows). The blue curve corresponds to the diode with 6.2 nm thick InAlN barrier and shows the dominance of the first conduction mechanism for $-3 < V < -2$ and of the second mechanism for $-2 < V < 0$. (b) Temperature dependent current-voltage characteristics for the devices with 3.7 and 13.2 nm InAlN barriers recorded between 100 and 300 K.

the conduction band profile and electric field in the barrier as a function of the applied bias. These parameters have been thus calculated by means of the *nextnano* software [42]. The calculated bias dependent electric fields in the InAlN barrier (F_{InAlN}) and in the AlN spacer (F_{AlN}) for the seven diodes are plotted in Fig. 4.8(a) and 4.8(b), respectively. It is worth noting that at zero applied voltage, F_{InAlN} decreases as the InAlN gets thicker, which is a consequence of the higher 2DEG density (Eq. 2.23). For a bias lower than the pinch-off voltage, the 2DEG is no more present and the electric field is therefore no more confined in the barrier but can penetrate inside the GaN buffer. The main consequence is that after pinch-off the electric field in the barrier varies much more slowly as the bias is increased and can be considered practically constant. As a consequence, the current remains constant for voltages lower than the pinch-off voltage.

Within the ensemble of the diodes considered, two classes of devices could be discriminated, showing characteristic I-V curves of different nature. Fig. 4.9(a) shows a representative current-voltage characteristic for each device class. For the first class of devices, corresponding to the thinnest InAlN barriers, the current raises almost exponentially under reverse bias and then saturates at the pinch-off voltage. For the second class of devices, corresponding to the thicker InAlN barrier, the current rises instead more slowly and the current-voltage

characteristic is significantly more curved. There are therefore two different conduction mechanisms, which may even coexist in heterostructures with intermediate InAlN thickness, as is the case for the third device presented in Fig. 4.9(a). A first insight into the nature of those conduction mechanisms can be obtained from temperature dependent current-voltage measurements. The current-voltage characteristic at temperatures between 100 and 300 K for the representative devices of Fig. 4.9(a) are shown in Fig. 4.9(b). As can be seen, the temperature has marginal influence on the reverse-bias current in both cases. The current varies by just a factor 3 maximum when going from 100 to 300 K for both structures, too low for a thermally activated process like Poole-Frenkel or thermionic emission. The data instead strongly suggest that tunneling is at the origin of both conduction mechanisms. However, direct tunneling through the barrier did not prove to correctly model the current-voltage characteristic of neither class of devices. The currents predicted by direct tunneling are indeed more than one order of magnitude lower that the ones measured at any voltage and for any InAlN barrier thickness, which is not surprising considering the high Schottky. Other tunneling-based conduction mechanisms able to predict stronger currents were therefore considered. In particular, the mechanisms examined were trap-assisted tunneling (TAT), [171, 172], where the tunneling rate is enhanced by a deep level, and patch models [172], where leakage currents are associated to a small but highly conductive fraction of the heterostructure surface.

4.3.1 Trap assisted tunneling currents

TAT has been applied successfully by Sathaiya and Karmalkar to predict the current-voltage characteristic of AlGaN/GaN Schottky diodes [171]. The mechanism is sketched in Fig. 4.10(a) and consists in two elastic tunneling steps. The first one, hereafter referred to as trapping, consists in an electron tunneling from the metal electrode to a trap level in the InAlN barrier, followed by the second tunneling step, called detrapping, from the trap level to the 2DEG region. A rigorous formulation of the TAT current has been given by Jos [172]. Let's denote N_t the trap concentration and $n_t(W)$ the occupied trap concentration at a depth W. Denoting $P_1(W)$ and $P_2(W)$ the corresponding trapping and detrapping rates, we can write the following rate equation:

$$\frac{\mathrm{d}n_t(W)}{\mathrm{d}t} = f_{FD}P_1(W)\left[N_t - n_t(W)\right] - P_2(W)n_t(W) \tag{4.1}$$

where f_{FD} is the Fermi-Dirac distribution in the metal, accounting for the amount of available electrons for the trapping process. In steady state $\mathrm{d}n_t(W)/\mathrm{d}t = 0$ and thus

$$n_t(W) = N_t \frac{f_{FD}P_1(W)}{f_{FD}P_1(W) + P_2(W)} \tag{4.2}$$

The traps located at a depth W will contribute to the TAT current J_{TAT} by an amount $\mathrm{d}J_{TAT} =$

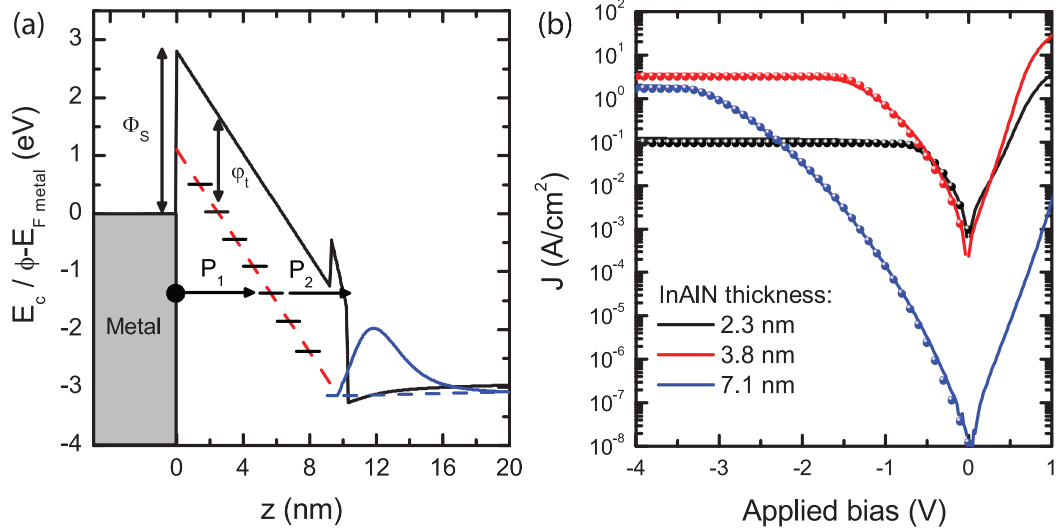

Figure 4.10: (a) Schematic representation of the TAT conduction model, where the tunneling from the metal electrode to the 2DEG region is assisted by a trap level. (b) Experimental (lines) and simulated TAT (dots) currents for the devices having a thin InAlN barrier.

$en_t(W)P_2(W)\mathrm{d}W$. After simple manipulation, we obtain finally:

$$J_{TAT} = eN_T \int_0^{d_{InAlN}} \left(\frac{1}{f_{FD} P_1(W)} + \frac{1}{P_2(W)} \right)^{-1} \mathrm{d}W \tag{4.3}$$

The integral in W is performed only over the InAlN barrier and not over the AlN spacer as only traps in the InAlN barrier are considered. For an electron with kinetic energy ϕ in the metal, the trapping rate P_1 is calculated in the framework of the Wentzel-Kramers-Brillouin approximation according to the model of Lundström and Svensson [173] and is given by

$$P_1(W) = \frac{4\hbar m_m^*}{m_{InAlN}^{*2}} \frac{\alpha}{\alpha^2 + k_0^2} \int_0^{k_0} e^{-2\int_0^W \sqrt{\frac{2m_{InAlN}^*}{\hbar^2}(E_c(z) - \phi_{tunn})}\mathrm{d}z} k_z k_\parallel \mathrm{d}k_\parallel \tag{4.4}$$

where m_m^* is the metal electron effective mass, taken here as $0.1m_0$, $k_0 = \sqrt{2m_m^*\phi/\hbar^2}$ is the electron wavevector in the metal, $\alpha = \sqrt{2m_{InAlN}^*\varphi_t/\hbar^2}$, with φ_t the depth of the trap below the InAlN conduction band edge, $k_z = \sqrt{k_0^2 - k_\parallel^2}$ is the component of the wavevector perpendicular to the metal-semiconductor interface, and $\phi_{tunn} = \phi - \hbar^2 k_\parallel^2 / 2m_{InAlN}^*$ is the tunneling energy. $E_c(z)$ is the InAlN conduction band edge, which can be written $E_c(z) = E_{F,metal} + \Phi_S - eF_{InAlN}z$. Thanks to this last equation, the trap position W can be linked to the electron energy ϕ:

$$W = \frac{\Phi_S - \varphi_t - \phi + E_{F,metal}}{eF_{InAlN}} \tag{4.5}$$

where $E_{F,metal}$ is the metal Fermi level. The detrapping process produces a free electron in the GaN channel with kinetic energy $\phi' = \phi - E_{F,metal} - eV$ and wavevector $k_0' = \sqrt{2m_{GaN}^*\phi'/\hbar^2}$.

The detrapping rate is thus calculated, analogously to P_1, as

$$P_1(W) = \frac{4\hbar}{m^*_{InAlN}} \frac{\alpha}{\alpha^2 + k_0'^2} \int_0^{k_0'} e^{-2\int_W^t \sqrt{\frac{2m^*(z)}{\hbar^2}(E_c(z)-\phi'_{tunn})}\mathrm{d}z} k_z' k_\parallel \mathrm{d}k_\parallel \tag{4.6}$$

where $\phi'_{tunn} = \phi' - \hbar^2 k_\parallel^2 / 2m_{InAlN}$, $k_z' = \sqrt{k_0' - k_\parallel^2}$, $m^*(z)$ is the position-dependent electron effective mass, and t is the extreme of the tunneling region, i.e. the point where $E_c = \phi'_{tunn}$. The need of a position dependent effective mass is motivated by the fact that for some trap levels, the electron, during detrapping, has to tunnel not only through the InAlN barrier but also through the AlN spacer, which is characterized by a different effective mass. Thanks to Eq. 4.3, 4.4 and 4.6 the TAT current can be calculated with the help of the simulated bias dependent electric fields shown in Fig. 4.8(a) and 4.8(b).

According to the theoretical framework just presented, it was possible to determine that in order to produce current levels compatible with the experimental ones, the trap depth should lie between 1.4 and 2.2 eV. For shallower or deeper traps the capture or emission rate, respectively, becomes indeed very slow, and trap concentrations well in excess of 10^{20} cm^{-3} are needed in order to produce current levels compatible with the experimental ones. In Sec. 2.4 we have seen that in InAlN deep level actually exists in this energy range. More precisely, there is a band of deep levels centered around 1.7 eV below the InAlN conduction band edge. In order to avoid excessive complications due to a distribution of energy levels, the approximation of a single level with 1.7 eV depth was made. This value was thus taken as the value of φ_t for TAT current simulation. The only parameter remaining for fitting the experimental data is thus the trap concentration. The TAT model provided excellent fits for the reverse bias current-voltage characteristics of the Schottky diodes with the thinnest barriers, which are shown in Fig. 4.10(b). The N_T values used for the diodes with 2.3, 3.7, and 6.2 nm InAlN barriers are 5×10^{17}, 1.5×10^{19} and 1.0×10^{19} cm^{-3}, respectively. The increase in the trap density with increased InAlN thickness can be interpreted as a degradation of the InAlN quality with increasing thickness. We will come back to this point in the next section, once the second family of diodes will be modeled. Note also that the saturation of the reverse bias current beyond pinch-off is naturally accounted for by the saturation of the simulated electric fields (Fig. 4.8).

Now that the TAT model is complete, the conduction process can be analyzed more deeply. In particular, the relative importance of the trapping and detrapping process and their dependence on the electron energy can be worked out. Fig. 4.11(a) shows the two rates as a function of the electron energy for an heterostructure with 3.7 nm InAlN barrier at a bias of -3 V. The trapping rate P_1 is multiplied by the Fermi-Dirac distribution in the metal in order to display the actual rate of incoming electrons. Trapping is always the slowest rate. It is therefore the limiting process controlling conduction and peaks around the metal Fermi energy. For electrons in the metal having low energies, the tunneling rate is reduced by the increased distance the electron has to travel in order to reach the trap, while at higher energies the process is limited by the decreasing number of available electrons in the metal. This is

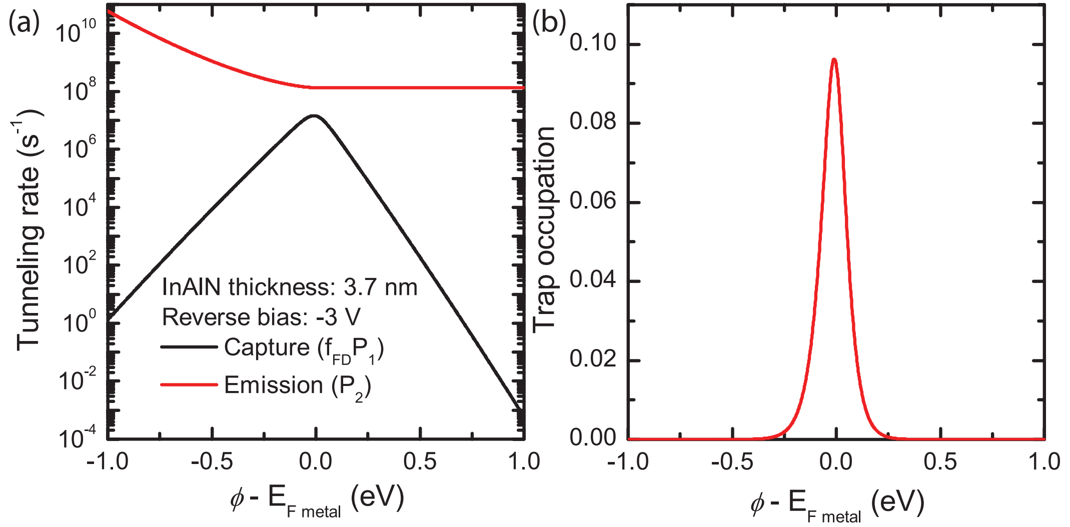

Figure 4.11: (a) Energy dependent trapping and detrapping rates for an heterostructure with 3.7 nm InAlN barrier at a bias of -3 V and (b) corresponding trap occupation factor.

reflected in the trap occupation factor n_t/N_t, shown in Fig. 4.11(b) as a function of the trap level position and calculated according to Eq. 4.2, which is maximum for the traps aligned to the metal Fermi level. The fact that the main contribution to the TAT current is given by electrons close to the metal Fermi energy allows us to simplify considerably the formulation of the TAT current. The dominant role of the trapping step allows us to neglect the $1/P_2$ term in Eq. 4.3, while the fact that only electrons close to the metal Fermi level contribute significantly to the current allows us to avoid the integration over the trap energies and to consider only those which are resonant to the metal Fermi level. P_1 may be further simplified by considering only wavevectors perpendicular to the metal-semiconductor interface. In this case, we obtain

$$J_{TAT} \propto e^{-\frac{8\pi\sqrt{2m^*_{InAlN}}\left(\Phi_S^{3/2}-\varphi_t^{3/2}\right)}{3heF_{InAlN}}} \tag{4.7}$$

This equation is very close to the one for Fowler-Nordheim tunneling (Eq. 4.9). Eq. 4.7 can be indeed cast in the Fowler-Nordheim form by just replacing $\left(\Phi_S^{3/2}-\varphi_t^{3/2}\right)$ with $\Phi_{FN}^{3/2}$, where Φ_{FN} is the fictive Fowler-Nordheim barrier: $\Phi_{FN} = \left(\Phi_S^{3/2}-\varphi_t^{3/2}\right)^{2/3}$. By inserting the experimental values, we calculate Φ_{FN} = 1.8 eV. It is interesting to compare this value with the results of Ganguly *et al.* [123], who could model the high voltage portion of their current-voltage characteristics with the Fowler-Nordheim model. They found a value of Φ_{FN} = 1.56 eV, quite close to the 1.8 eV found here. Our results are therefore consistent with their findings, with the difference that the TAT model describes quantitatively the whole reverse bias characteristic for heterostructures with thin barriers ($d_{InAlN} \leq 7$ nm).

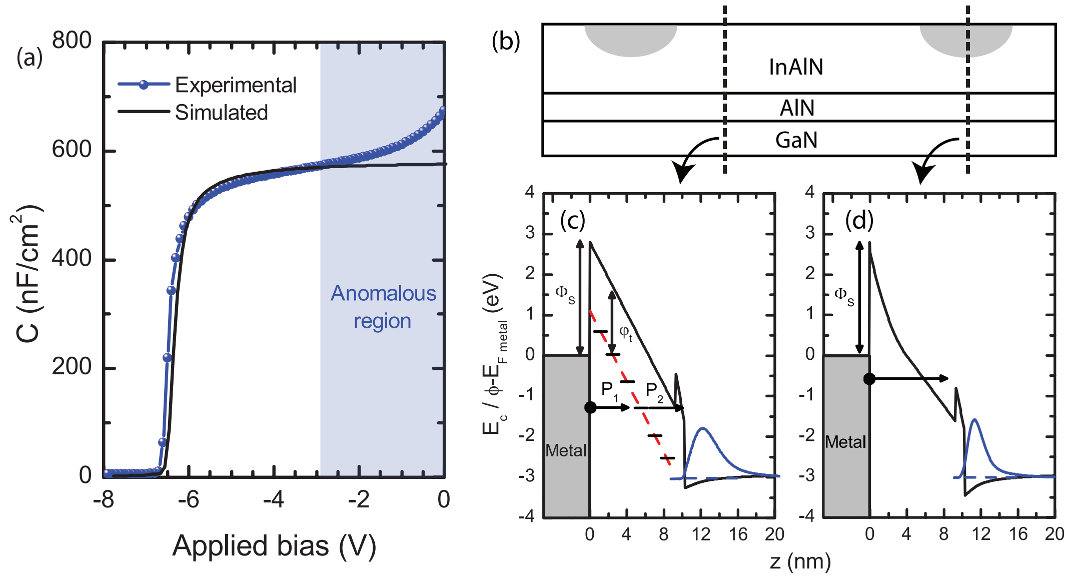

Figure 4.12: (a) Electrochemical capacitance-voltage characteristic of the heterostructure with 13 nm InAlN barrier. The anomalous region where the experimental capacitance deviates significantly from the simulated one is highlighted. (b) Schematic cross section of an InAlN/GaN heterostructure where the critical thickness for the formation of highly doped regions (grey spots) has been exceeded. Two conduction mechanisms therefore coexist: (c) in undoped regions we have a TAT mechanism, while (d) in highly doped regions, electrons tunnel directly through the InAlN barrier.

4.3.2 Direct tunneling currents

If the TAT model describes successfully the current-voltage characteristic of thin barrier devices, it fails modeling the thicker barrier devices, even if traps outside the 1.4–2.2 eV energy window are considered. A different mechanism had to be considered for those heterostructures, and some insights could be obtained from a careful examination of their capacitance-voltage curve. Fig. 4.12(a) shows the representative example of the heterostructure with 13.0 nm (12.0 nm after processing) InAlN barrier thickness. Similar features are found for the other samples with thick InAlN barrier (see Fig. 2.4(b)). At low reverse voltages we observe an anomaly in the capacitance, i.e., the capacitance decreases rapidly, much more that what is expected for a 2DEG. Indeed in this voltage region the simulated capacitance is significantly lower that the experimental one. This behavior indicates carrier modulation inside the InAlN barrier, i.e., of a significant residual doping in the InAlN layer. However, it is worth noting that in order to observe carrier depletion in the barrier in this voltage region, the zero-voltage depletion region must be thinner than the InAlN barrier, which would imply a zero-voltage capacitance much higher than the measured one. Furthermore, the residual doping level required would be much higher than 10^{19} cm^{-3}, and in this case the 2DEG pinch-off voltage would no more scale linearly with the InAlN thickness but rather quadratically, which is not our case. A possible explanation for this apparent contradiction would be that just a little

portion of the material is actually highly doped. In this case, the heterostructure capacitance would be described as the parallel combination of two capacitors, one for the highly doped portion and the other for the undoped part. In this case, the pinch-off voltage would continue scaling linearly with the InAlN thickness and the capacitance anomaly at low reverse voltage would be explained. From the value of the zero-voltage capacitance, it can be estimated that the highly doped region accounts for a few percent of the heterostructure. It is interesting to note that this capacitance anomaly gets stronger as the InAlN thickness increases, and is absent in the thinnest devices. It is therefore likely that the appearance of the highly doped regions is related to some process of degradation of the growing InAlN layer, which can be tentatively ascribed to the early stages of the In segregation related morphological degradation described by Perillat-Merceroz *et al.* [174]. The appearance of a conduction mechanism other than TAT in the thicker samples is therefore associated with the appearance of these highly doped regions, in particular direct tunneling through their thin depletion region. The model is depicted schematically in Fig. 4.12(b).

Tunneling through the highly doped regions was modeled by making the simplifying assumption of a constant electric field throughout the depletion region. In this case, the barrier can be approximated to a triangular one and simple analytic formulas based on Fowler-Nordheim tunneling can be derived for the current-voltage characteristic. The corresponding band profile is sketched in Fig. 4.12(d). We also assume that the depletion region width can be considered independent of the applied voltage, mainly because the high Schottky barrier height mitigates the influence of the applied voltage. The electric field is, therefore,

$$F_{InAlN} = \frac{\Phi_S/e - V}{d} \tag{4.8}$$

where d is the width of the depletion region, which is directly related to the doping N_d: $d = \sqrt{2\epsilon_{InAlN}\epsilon_0\Phi_S/N_d e^2}$. Neglecting the image charge correction terms, the Fowler-Nordheim current reads

$$J_{FN} = \Sigma \frac{e^3 F_{InAlN}^2 m_0}{8\pi h m_{InAlN}\Phi_S} e^{-\frac{8\pi\sqrt{2m_{InAlN}^*}\Phi_S^{3/2}}{3heF_{InAlN}}} \tag{4.9}$$

where Σ is the heterostructure fraction occupied by the highly doped regions. If we now replace Eq. 4.10 in Eq. 4.9 and take the logarithm of both sides, we obtain

$$\ln J_{FN} = \Gamma - \frac{\Theta}{\Phi_S - eV} \tag{4.10}$$

where $\Theta = 8\pi\sqrt{2m_{InAlN}^*}\Phi_S^{3/2}d/3h$ and $\Gamma = \ln\left[\Sigma e^2 m_0 (\Phi_S - eV)^2/8\pi h m_{InAlN}^*\Phi_S d^2\right]$. Γ has a weak logarithmic dependence on the applied voltage and can therefore be considered as a constant in a first approximation. The plot of $\ln(J_{FN})$ as a function of the applied voltage should therefore be fitted with a hyperbola. After pinch-off, we assume that the conduction band profile does not change significantly, in analogy with the TAT case, and the current is therefore supposed to stay constant in this voltage region. Fig.4.13(a) shows that, despite

Table 4.2: Fitting parameters for reverse bias current modeling for the whole set of samples considered in this study. For each sample, the parameter listed are the InAlN thickness d_{InAlN}, the deep trap concentration N_t, the effective Schottky barrier Φ_S, doping concentration N_d, and surface occupation fraction Σ of the highly doped regions.

d_{InAlN} (nm)	N_t (cm^{-3})	Φ_S (eV)	N_d (cm^{-3})	Σ
2.3	5.0×10^{17}	2.8	...	0
3.7	1.5×10^{19}	2.8	...	0
6.2	5.0×10^{18}	1.0	5×10^{19}	1×10^{-7}
7.1	1.0×10^{19}	2.8	...	0
9.5	...	1.2	8×10^{19}	6×10^{-5}
12.0	...	2.1	2×10^{20}	2×10^{-5}
13.2	...	2.8	4×10^{20}	2×10^{-4}

the strong approximations used, the current-voltage characteristics of the heterostructures with thick InAlN barriers can be nicely fitted by our simple model. The fitting parameters are reported in Table 4.2. We observe that the Schottky barrier height Φ_S and the doping N_d are not constant, with Φ_S and N_d increasing as the InAlN thickness increases. It is worth noting that Φ_S reaches 2.8 eV for the thicker InAlN layer. It is possible that the increasing doping observed in thicker layers is due to a non-uniform residual doping distribution inside the highly doped regions, with the residual doping becoming more and more important as we move from the GaN/InAlN interface towards the InAlN surface. A similar argument has been used to explain the current-voltage characteristic of AlGaN Schottky diodes [175], where an exponential decay of the donor concentration inside the layer was found to better fit the experimental results. It is therefore possible that the depletion widths are actually larger than the ones expected in the case of uniform doping. In the thinner layers, the depletion region may therefore extend up to the AlN spacer, and this may in turn significantly affect the zero-voltage electric field in the barrier, giving rise to a low effective Φ_S. It is also possible that trap assisted tunneling contributes significantly to the current, and according to Eq. 4.7 it will give rise to an apparent low barrier. We also note that Σ takes very low values, well below the estimation of a few percent obtained from CV measurements. This may be also explained by a non-uniform doping level within the highly doped regions. As the tunneling current increases exponentially with the doping level, the regions with the highest doping will dominate conduction, even if they represent a minor part of the InAlN surface. Finally, we turn to the device having an InAlN barrier thickness of 6.2 nm and showing both conduction mechanisms. We could fit quite well its whole reverse bias current-voltage characteristic by superposing the TAT and the direct tunneling current

$$J = \Sigma J_{FN} + (1 - \Sigma) J_{TAT} \tag{4.11}$$

Trap concentration $N_t = 5 \times 10^{18}$ cm^{-3} was used for TAT current calculation, while effective barriers $\Phi_S = 1.0$ eV, doping level $N_d = 5 \times 10^{19}$ cm^{-3} and $\Sigma = 1 \times 10^{-7}$ were taken for direct tunneling current simulation. The results of the calculations are shown in Fig. 4.13(b).

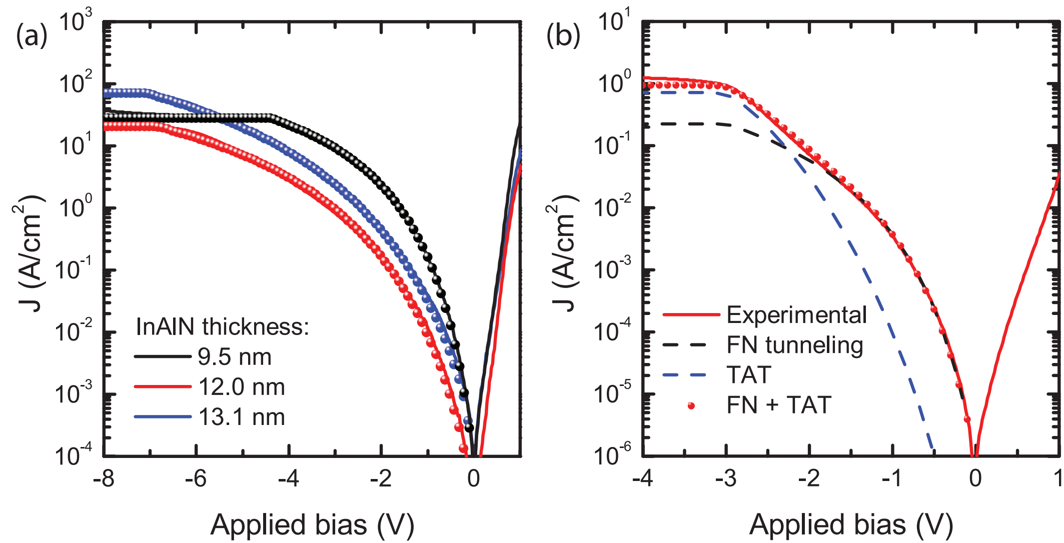

Figure 4.13: Experimental (lines) and simulated (dots) direct tunneling currents for (a) the devices having a thick InAlN barrier and (b) for the sample having a 6.2 nm thick InAlN barrier. In the latter, the current results from the superposition of a TAT (blue curve) and a direct tunneling (black curve) component.

4.4 *in situ* SiN passivation

The passivation of GaN based transistors is one of the most critical steps of their fabrication. The passivation has the very important task of limiting the amount of electrically active traps that cause the dispersion effects described in Sec. 1.6.2. As already mentioned there, while the passivation of AlGaN/GaN heterostructures has been extensively studied, the one of InAlN/GaN HEMTs has been much less explored and remained confined to *ex situ* deposition methods. The *in situ* deposition of a passivating layer may however present interesting advantages. Indeed, in the *in situ* scheme the semiconductor surface never comes in contact with air or liquids, thus avoiding any oxidation or uncontrolled surface chemical process. *In situ* passivation with SiN has been already shown beneficial in other III-nitride HEMT systems [39, 99, 176] and its extension to InAlN/GaN HEMTs is therefore of interest. The realization of *in situ* SiN passivated InAlN/GaN heterostructures is the subject of this section.

A fundamental requirement for the realization of *in situ* passivated layers with state of the art transport properties is that the heterostructure remains stable during the SiN deposition. The thermal stability of MOVPE grown InAlN has been already made the topic of several papers from other research groups, but results are scattered. On one side, InAlN/GaN HEMTs have shown impressive stability at temperatures as high as 1000 °C under vacuum [9, 11, 88]. However, these data concern processed layers, which have been already subjected to high temperature treatments, in particular Ohmic contact annealing, which as we know from Sec. 4.1.1 produces a 1 nm oxide on top of the InAlN layer. Furthermore, in these studies the surface was often protected by a thick *ex situ* passivation layer. On the other side, Yu *et al.* [177] studied

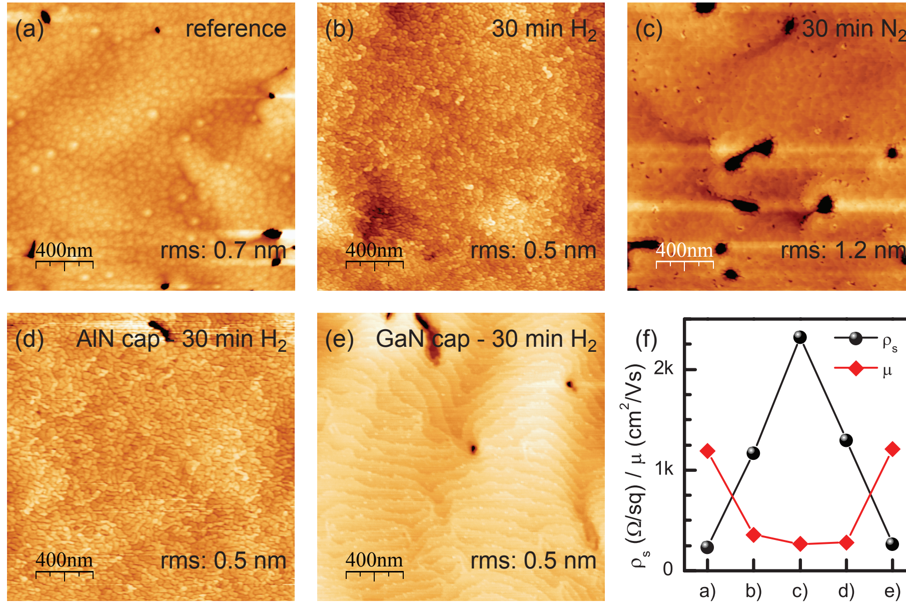

Figure 4.14: AFM image of (a) a reference, unannealed InAlN surface, (b) the same surface annealed *in situ* for 30 min at 850 ° under H_2 and (c) under N_2. (d) and (e) show the AFM image of the surface of AlN and GaN capped heterostructures, respectively, annealed under H_2 for 30 min. (f) Transport properties of the various layers.

the thermal stability of virgin layers and reported that a long *ex situ* annealing time (30 min) at temperatures up to 800 °C under N_2 can harm significantly the quality of the 2DEG. Similarly, Behmenburg *et al.* [178] reported that Ohmic contact annealing at 850 °C on unpassivated heterostructures increased significantly the 2DEG resistivity. On the opposite, Gadanecz and coauthors [179] found a very high stability for lattice-matched InAlN up to 960 °C under N_2. It is worth noting that this whole set of experiments concern *ex situ* InAlN thermal stability. The *in situ* thermal stability of InAlN layers under MOVPE conditions was not investigated before this work. The stability of InAlN/GaN heterostructures at temperatures > 800 °C in MOVPE environments was therefore studied in order to to determine if they are suitable or not for *in situ* passivation.

First, the effect of a 30 min *in situ* annealing at 850 °C on heterostructures with an InAlN top layer (i.e. without any capping layer) was studied. A strong effect of the annealing both on surface morphology and on 2DEG transport properties was found. Fig. 4.14(a) shows the AFM image of the surface of an unannealed InAlN reference surface. The typical hillocks morphology of thin InAlN layers is observed [174], together with larger scale features which reflect the morphology of the GaN buffer. This heterostructure has a barrier stack composed of a 1 nm AlN spacer plus 5 nm InAlN, for a total barrier thickness of 6 nm. The 2DEG is characterized by a low resistivity $\rho_s = 234\ \Omega/\square$, a sheet electron density $n_s = 2.2 \times 10^{13}$ cm^{-2} and a mobility $\mu = 1200$ cm^2/V·s (Fig. 4.14(f)). Figs. 4.14(b) and 4.14(c) show instead the surface morphology of HEMT heterostructures after annealing under H_2 and N_2, respectively. The surface rms roughness is reported for each image and we can note that the annealing

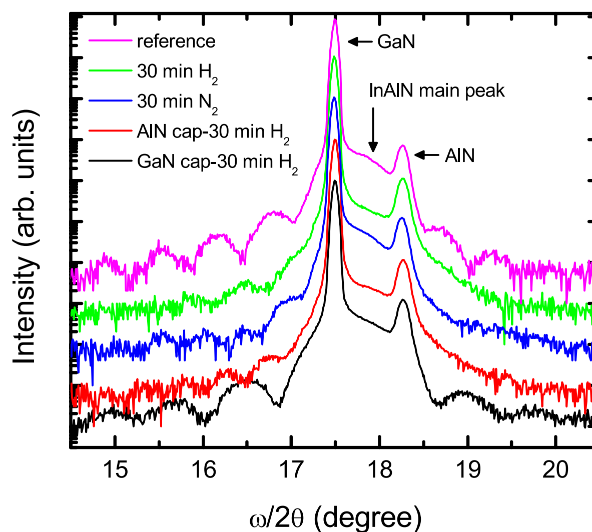

Figure 4.15: $\omega/2\theta$ scans of the (0002) reflection for the reference and *in situ* annealed heterostructures of Fig. 4.14.

does not cause significant roughening for the H_2 annealed layer, while for the N_2 annealed layer the surface rms roughness is increased to 1.2 nm. Strong morphological changes are furthermore evidenced in both cases. In the case of the H_2 annealing, the surface reorganizes in small islands, while for N_2 annealing small pits appear and atomic steps become visible. A similar morphology has been already observed for H_2 annealed InAlN and attributed to the microcracking of an Al rich surface layer formed as a consequence of In desorption [180]. The morphology of the N_2 annealed heterostructure is instead quite different, and the appearance of steps at the surface suggests that surface diffusion phenomena may have taken place. In both cases, we observe a very strong degradation of the sheet resistivity, which increases to 1170 and 2320 $\Omega/\square$, respectively. Most of the degradation is due to a reduction in electron mobility, which after annealing reaches values of 355 and 264 $cm^2/V{\cdot}s$, respectively, very low if compared to the reference sample. The electron density reduces as well, passing from 2.2×10^{13} cm^{-2} for the reference sample to 1.5×10^{13} cm^{-2} and 1.0×10^{13} cm^{-2} , respectively. In order to gain more insights in the degradation mechanism, XRD measurements were performed on these layers to assess eventual changes of the structural properties. The $\omega-2\theta$ scans of the (0002) reflections are presented in Fig. 4.15 and show a strong reduction of the Pendellösung fringes on both sides of the InAlN main peak for the annealed layers. Considering that the roughening evidenced by AFM is not drastic, the loss in fringe intensity must be due to a loss of crystal quality. The significant changes in surface morphology revealed by AFM furthermore suggest that significant compositional inhomogeneities may form within the InAlN layer during high temperature annealing as a consequence of desorption or diffusion phenomena, especially at the surface. This picture is supported by the strong reduction of the electron mobility in the annealed layers. Compositional inhomogeneities cause indeed fluctuations in the confining potential, which have a detrimental effect on 2DEG mobility.

With the aim of making the heterostructures stable against high temperature annealing, the effect of a capping layer on the thermal degradation of InAlN based heterostructures was explored. Both an AlN and a GaN cap were tested. While GaN could be grown without thickness related strain issues, pseudomorphic AlN layers are subject to a strong tensile stress and undergo plastic relaxation if thicker than ~ 1.5 nm, introducing defects that affect the 2DEG transport properties. As a consequence, in order to avoid spurious effects due to AlN relaxation, the AlN cap thickness was kept to 1 nm. The GaN cap was instead 2 nm thick. In both cases, the total barrier thickness (AlN spacer + InAlN barrier + cap) was kept to 6 nm. The 30 min annealing was performed under H_2. The resulting surface morphologies are shown in Figs. 4.14(d) and 4.14(e), while the corresponding values of resistivity and mobility are reported in Fig. 4.14(f). The results for the AlN capped layer are quite similar to the ones for the uncapped layer, both in terms of surface morphology and transport properties. The GaN capped layer instead presents a nice and smooth surface, with clearly visible steps and its sheet resistivity and mobility compare perfectly with the reference sample. The XRD measurements performed on these layers (Fig. 4.15) confirm these results. Weak Pendellösung fringes are indeed found for the AlN capped layer, evidencing crystal degradation, while the GaN capped layer maintains strong and well defined interference fringes. It is therefore possible to achieve extreme stability against high temperature annealing by appropriately capping the InAlN surface with a thin GaN layer. The highly beneficial effect of an appropriate capping layer furthermore supports the hypothesis that the degradation process takes place at the InAlN surface.

The results just described concerning the thermal stability of differently capped heterostructures have been then applied to the growth of *in situ* SiN passivated layers. First, the possibility of growing SiN on uncapped heterostructures in the MOVPE reactor was investigated. The SiN deposition was performed immediately after the growth of the heterostructure, at a temperature of 850 °C and 75 mbar reactor pressure. SiH_4 and NH_3 were used as Si and N precursors, respectively. As only a diluted SiH_4 source was available, the maximum SiH_4 flow that could be used was 0.45 μmol/min. The V/VI ratio was therefore very high: 2200. This resulted in a very low SiN growth rate of 2.5 nm/h. Very long SiN deposition times are therefore necessary, which according to the results presented above may result in 2DEGs with reduced transport properties. The effect of SiN depositions of different duration (15, 30 and 60 min) were tested in order to study their effect on the 2DEG quality. The transport properties of such layers are shown in Fig. 4.16(a). As can be seen, a relatively short growth time of 15 min at 850 °C does not harm the 2DEG transport properties. A layer having a low sheet resistance of 252 Ω/□ and high electron mobility of 1030 $cm^2/V{\cdot}s$ was indeed obtained in this case, which compares quite well with the transport properties of the reference sample. However, such a short SiN deposition time leads to extremely thin (0.7 nm) SiN layers. With increasing growth time, necessary for achieving thicker SiN passivations, the 2DEG starts to be severely degraded. The effect is particularly strong on the electron mobility, which reduces down to 440 $cm^2/V{\cdot}s$ for a SiN growth time of 60 min, giving a sheet resistance of 670 Ω/□. The $\omega/2\theta$ scans and X-ray reflectivity spectra of such layers are presented in Fig. 4.17(a) and 4.17(b), respectively

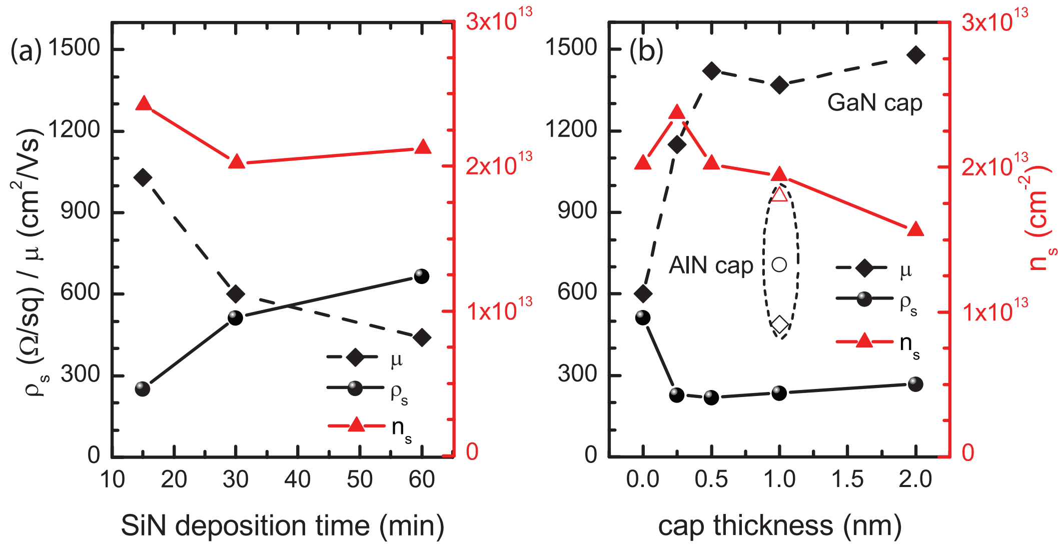

Figure 4.16: (a) Transport properties of *in situ* passivated uncapped heterostructures as a function of SiN deposition time. (b) Transport properties of *in situ* passivated InAlN/GaN heterostructures with GaN (closed symbols) or AlN (open symbols) cap layer. This plot shows also, for comparison, the transport properties of an *in situ* passivated but uncapped (i.e. zero cap thickness) layer. For both (a) and (b) panels, the SiN deposition is performed at 850 °C for 30 min.

(black lines). $\omega/2\theta$ scans are characterized by very weak or absent Pendellösung fringes in every case, which shows that the SiN deposition triggers crystal degradation even for short deposition times. X-ray reflectivity spectra on the other hand are characterized by well visible interference fringes. This shows that even if degradation occurs, no significant roughening takes place, consistently with the AFM observations of Fig. 4.14(a)-(c). An attempt was also made to obtain thicker SiN layers with relatively short deposition times by implementing a two step passivation procedure consisting in a first deposition of SiN at 850 °C for 8 min followed by 16 min SiN growth at 950 °C. The higher temperature of the second step increases the SiN growth rate, which results in a total SiN thickness of 3 nm for a total deposition time of 24 min. However, despite its relatively short duration, this two-step method resulted in a very severe 2DEG degradation. The mobility was indeed reduced to 377 $cm^2/V{\cdot}s$ and the sheet resistance increased to 880 Ω/□. These results may seem to contrast with the results of Behmenburg *et al.* [178], who could obtain damage-free *in situ* passivated heterostructures. However, in that work a high SiN growth rate was used, which allows for very short deposition times and thus very limited damage to the 2DEG transport properties. Nevertheless, the results of this section indicate that InAlN terminated heterostructures are not well suited for *in situ* passivation with SiN, as the growth conditions of the latter trigger InAlN degradation.

We then tested the effect of a thin (≤ 2 nm) cap layer on the stability of our layers, considering both AlN and GaN as cap materials. As before, the capped heterostructures were grown with a total barrier thickness of 6 nm, while the deposition of the *in situ* SiN passivation layer was

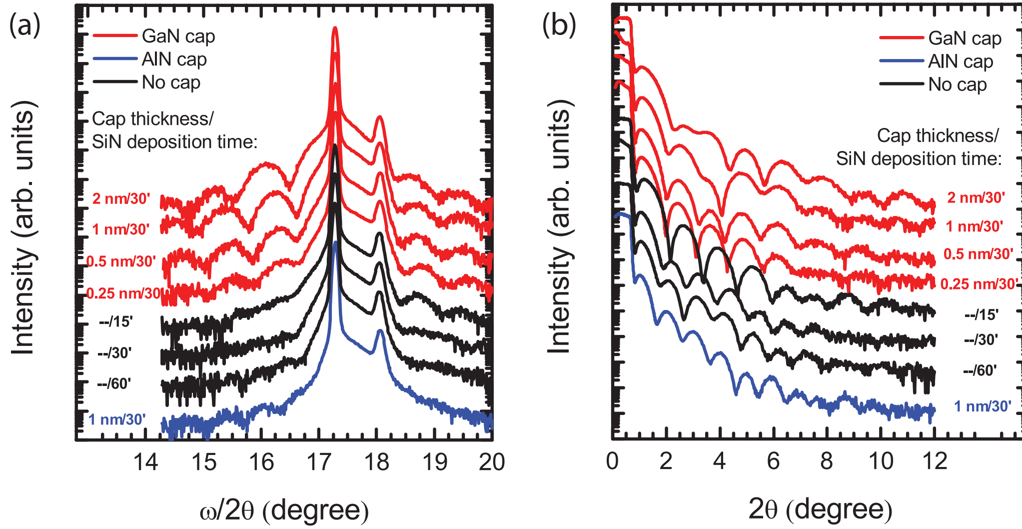

Figure 4.17: (a) $\omega/2\theta$ scans of the (0002) reflection for the *in situ* SiN passivated heterostructures studied. (b) X-ray reflectivity spectra for the same layers. In both cases the cap thickness and the SiN deposition time is specified for each sample.

performed at 850 °C for 30 min, which according to the results on uncapped heterostructures is long enough to evidence an eventual degradation of the 2DEG transport properties. The AlN cap thickness was fixed to 1 nm due to the already mentioned strain issues, while several GaN cap thicknesses were tested, ranging between 2 and 0.25 nm. The transport properties of these layers are summarized in Fig. 4.16(b). The AlN capped layer was found to be severely degraded, consistently with the results obtained in absence of SiN deposition. In particular, it shows a very low mobility of 490 $cm^2/V{\cdot}s$ and a high resistivity of 710 $\Omega/\square$. The degradation is confirmed by the very weak Pendellösung fringes of its $\omega/2\theta$ scan shown in Fig. 4.17(a) (blue line). Note however that, as for the other layers, the X-ray reflectivity spectra presents once again clear fringes, meaning that no roughening takes place. On the other hand, a GaN cap layer is highly beneficial for the thermal stability, as expected from the results of Fig. 4.14. Heterostructures with state of the art transport properties are indeed obtained for GaN cap layers down to 0.5 nm. In these layers, the sheet resistance is $< 270\ \Omega/\square$ for the 2 nm GaN cap and improves to 218 $\Omega/\square$ for a 0.5 nm cap thickness. The effect is ascribed to a higher 2DEG sheet density for thinner cap thickness. In this set of samples, we kept indeed the total barrier thickness constant, meaning that a reduction of the cap thickness is compensated by an increased InAlN thickness, which is at the origin of the higher 2DEG sheet density (see Sec. 2.3). The electron mobility, on the other hand, does not change significantly and lies in the range 1370–1480 cm^2/V·s. For the thinnest GaN cap (0.25 nm), we observe instead a lower mobility of 1150 cm^2/V·s, which could be due to an incomplete covering of the surface. These results are well supported by the $\omega/2\theta$ scans of Fig. 4.17(a), which show strong Pendellösung fringes for the GaN capped layers, exept for the 0.25 nm GaN cap where the fringes intensity is reduced. Finally, for zero cap thickness, i.e., for uncapped heterostructures, the degradation is as expected much more pronounced. In these last two samples, ρ_s follows a consistent

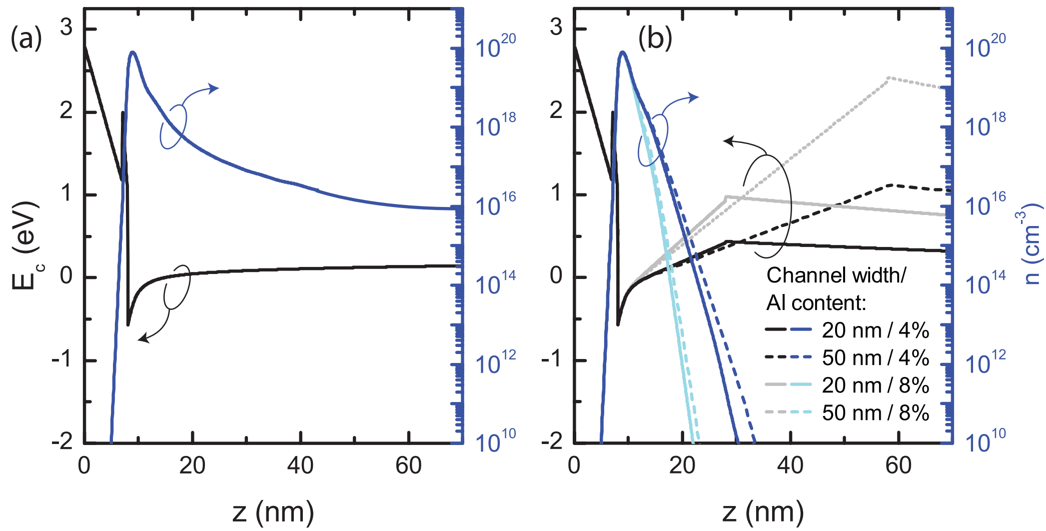

Figure 4.18: (a) Conduction band profile and electron density for (a) an InAlN/GaN heterostructure without back-barrier and (b) with $Al_xGa_{1-x}N$ backbarrier. In the latter case, backbarriers with 4% and 8% Al content are compared, as well as channel widths of 50 and 70 nm for each composition.

trend: it increases slightly to 230 Ω/□ for a 0.25 nm cap and reaches 510 Ω/□ when the cap is removed. The high stability of GaN capped heterostructures is furthermore not only limited to a SiN growth temperature of 850 °C. The use of the two-steps passivation procedure on a 2 nm GaN capped heterostructure indeed resulted in a layer with $\rho_s = 280$ Ω/□, $n_s = 1.73 \times 10^{13}$ cm^{-2}, and $\mu = 1280$ cm^2/V·s, which compares very well with the values of the sample with identical structure but the single step passivation.

4.5 Back-barriers

The last building block that has been considered are back-barriers. These are part of the nitride epitaxial structure and are intended to provide a better confinement of the 2DEG with respect to heterostructures with a standard GaN buffer. This would be desirable in order to reduce short channel effects, especially in HEMTs with deep sub-μm gatelengths, which are detrimental for high-voltage operation. As already mentioned in Sec. 1.6.2, two back-barrier architectures have been developed. The first one consists in introducing an InGaN QW below the 2DEG region [94]. The polarization induced electric field in the InGaN QW induces a step in the conduction band profile which acts as a barrier for 2D electrons. A more effective confinement can be however achieved with the second back-barrier architecture, which consists in using a low Al-content $Al_xGa_{1-x}N$ buffer and a GaN channel [95]. The Al-content of the AlGaN back-barrier is usually < 10% mainly for two reasons. On one side, a too high Al-content would give rise to an excessive stress in the GaN channel, resulting in the relaxation of the latter with the formation of a large amount of defects. On the other

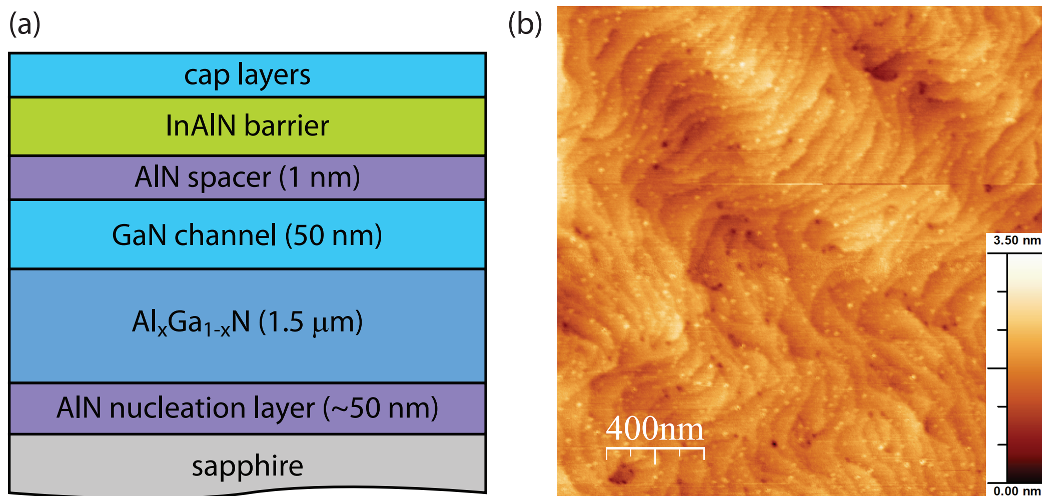

Figure 4.19: (a) General structure of InAlN/GaN heterostructures with back-barrier. (b) 2×2 μm^2 AFM image of an $Al_{0.07}Ga_{0.93}N$ back-barrier.

side, we verified that the growth of thick AlGaN layers with high Al-content often results in rough surfaces, which has to be avoided as this would impact the 2DEG mobility. The AlGaN back-barrier not only introduces a conduction band step due to the larger band gap of AlGaN, but at the GaN/AlGaN interface negative polarization charges are formed, which increase the confinement by electrostatic repulsion. The enhanced confinement provided by AlGaN back barriers is shown in Fig. 4.18. The strong confinement of the 2DEG provided by the back-barrier can be easily seen by comparing Fig. 4.18(a), which shows an heterostructure without back-barrier, and Fig. 4.18(b), which shows four heterostructures with AlGaN back-barriers. The latter differ in the GaN channel width (20 nm and 50 nm) and in the Al content of the back-barrier (4% and 8%). It is evident from Fig. 4.18(b) that the enhanced confinement is mainly due to the negative polarization induced charges at the GaN/AlGaN interface, rather than to the conduction band discontinuity due to band offset. These charges introduce a significant band bending, thus creating a very high barrier whose height increases with the Al content of the back-barrier and the channel width. The back-barrier height does not increase however indefinitely with the channel width as in thick channels the polarization induced charges get screened by the channel residual doping.

The growth of InAlN/GaN heterostructures comprising an AlGaN back-barrier has been optimized on sapphire substrates. The general layer stack of the heterostructures grown is shown in Fig. 4.19(a). The AlN nucleation layer, the GaN channel and the barrier are grown as described in Sec. 3.3.1. Sapphire nitridation is performed before growth in order to improve the crystal quality (Sec. 3.3.2). The 1.5 μm AlGaN buffer constituting the back-barrier is grown under conditions very close to the ones used for standard GaN buffers. The growth temperature is 1060 °C, the growth pressure 75 mbar and the growth speed 1.5 μm/h. The surface morphology of a 1.5 μm thick $Al_{0.07}Ga_{0.93}N$ grown this way is shown in Fig. 4.19(b). Steps are clearly visible, the surface rms roughness is 0.3 nm and the the surface does not

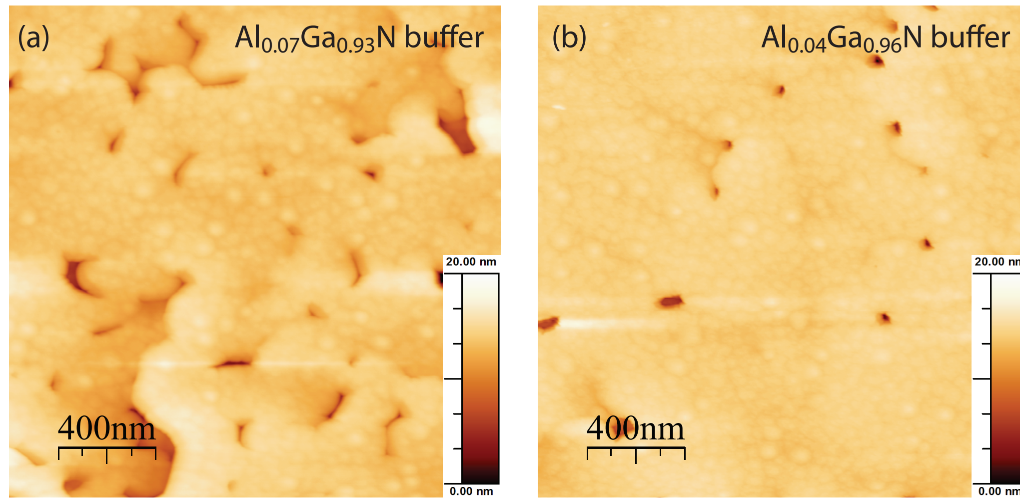

Figure 4.20: 2×2 μm^2 AFM image of an InAlN/GaN heterostructure with (a) an $Al_{0.07}Ga_{0.93}N$ back-barrier and (b) an $Al_{0.04}Ga_{0.96}N$ back-barrier.

differ significantly from the GaN buffer surface of Fig. 3.5(a). The first attempt to grow an heterostructure with back-barrier was therefore based on such buffer. More in detail, the heterostructure incorporated a 50 nm GaN channel and a barrier stack constituted by a 1 nm AlN spacer and 6 nm InAlN. The room temperature transport properties of the 2DEG, measured by Hall effect, are: $n_s = 1.84 \times 10^{13}$ cm^{-2}, $\mu = 1070$ cm^2/V·s and $\rho_s = 317$ Ω/□. The low mobility, which is responsible for the relatively high sheet resistivity, is probably due to the rough heterostructure surface, as can be seen form the AFM image of Fig. 4.20(a). Considering that the underneath AlGaN buffer is quite smooth, the poor morphology is attributed to a partial relaxation of the GaN channel due to the lattice mismatch with the AlGaN buffer. In order to prevent this deleterious phenomenon, a new heterostructure was grown. This heterostructure was nearly identical to the one just described, except for the AlGaN buffer composition, which was set to 4% Al content. The lower Al content of the buffer induces a lower strain in the GaN, resulting in a definetely improved surface morphology (Fig. 4.20(b)). In particular, the amount of pits is reduced by a factor 4. The transport properties of such heterostructure are also improved, as expected, and in line with state of the art heterostructures without back-barrier: $n_s = 2.12 \times 10^{13}$ cm^{-2}, $\mu = 1160$ cm^2/V·s and $\rho_s = 254$ Ω/□. It is therefore possible to obtain heterostructures with back-barriers having excellent transport properties and at the same time a good 2DEG confinement. The barrier provided by the 4% AlGaN back-barrier, although lower than the one provided by the 7% AlGaN back-barrier, is indeed still quite high (~ 1 eV).

The growth scheme developed on sapphire was easily transferred to SiC substrates. The 2 μm GaN buffer is simply replaced by the 1.5 μm $Al_{0.04}Ga_{0.96}N$ buffer just described plus a 50 nm GaN channel. It was also possible to integrate to the structure a SiN passivation. A representative example is given by an heterostructure comprising a back-barrier, a barrier stack with 6 nm total thickness composed of a 1 nm AlN spacer, 3 nm InAlN and 2 nm GaN cap, and a 1 nm *in situ* SiN passivation grown according to the method described in Sec. 4.4.

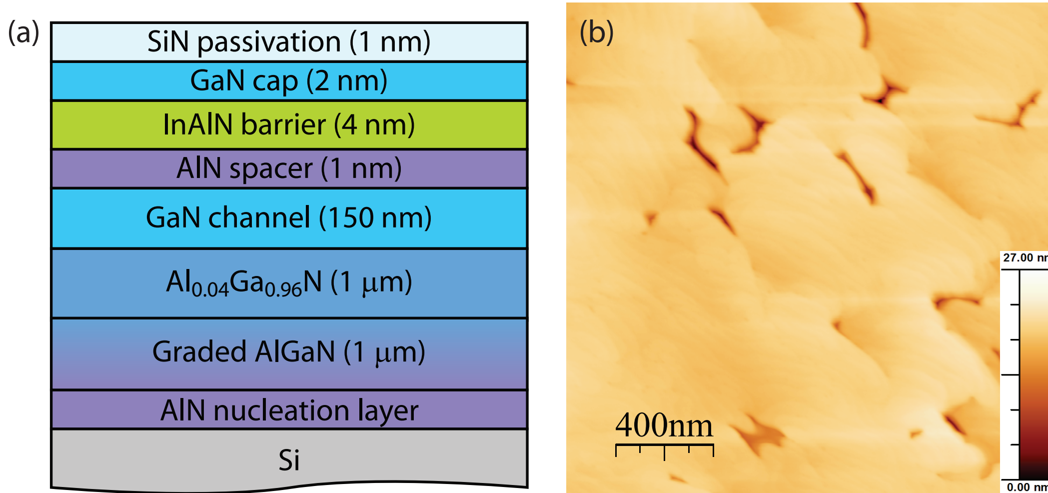

Figure 4.21: (a) layer stack of the InAlN/GaN heterostructure on Si with back-barrier and *in situ* SiN passivation. (b) 2×2 μm AFM image of the surface of the same layer.

The transport properties of such heterostructures are: $n_s = 1.61 \times 10^{13}$ cm^{-2}, $\mu = 1500$ cm^2/V·s and $\rho_s = 260$ $\Omega/\square$. Compared with a standard heterostructure on SiC with same barrier stack but withouth neither back-barrier nor cap (Sec. 3.4), no appreciable difference can be detected. This shows once more that back-barriers and *in situ* passivation can be introduced while preserving state of the art transport properties. Similarly, InAlN/GaN heterostructures on Si could be obtained comprising a back-barrier and *in situ* passivation. The growth of such structures was performed starting with an AlN nucleation layer, followed by a 1 μm graded AlGaN strain management layer which was graded from pure AlN to $Al_{0.04}Ga_{0.96}N$. The $Al_{0.04}Ga_{0.96}N$ growth was then prolonged in order to obtain a 1 μm thick back-barrier on top of which the GaN channel, the barrier stack and the *in situ* passivation were grown. The back-barrier thickness was limited to 1 μm to avoid crack formation. On the other hand, the GaN channel thickness was increased to 150 nm with respect to the previous examples in order to obtain a smooth enough surface. The barrier stack has total thickness of 7 nm and is composed of a 1 nm AlN spacer, 4 nm InAlN and 2 nm GaN cap. Finally, the *in situ* SiN passivation is 1 nm thick. The layer stack is shown in Fig. 4.21(a), while an AFM image of the surface is shown in Fig. 4.21(b). The room temperature transport properties measured by Hall effect are: $n_s = 1.7 \times 10^{13}$ cm^{-2}, $\mu = 1270$ cm^2/V·s and $\rho_s = 280$ $\Omega/\square$. These excellent results confirm that the back-barrier scheme can be applied, together with *in situ* passivation, also to Si based heterostructures without introducing any degradation of the transport properties.

5 Performances of InAlN/GaN HEMTs

This last chapter focuses on the application of InAlN/GaN heterostructures to the achievement of InAlN/GaN HEMTs. We will cover two device applications of InAlN/GaN heterostructures. The first one, treated in Sec. 5.1, concerns the use of InAlN/GaN heterostructures with thin buffers for the achievement of HEMTs able to operate at temperatures as high as 600 °C. The second application, treated in Sec. 5.2, regards on the other hand the use of InAlN/GaN heterostructures for the fabrication of HEMTs for millimeter-wave power applications. We will describe in particular two devices designed for operation at 40 GHz and 94 GHz, respectively. Finally, we will conclude with some considerations about the main performance limiting factors for InAlN/GaN HEMTs and will discuss some future strategies for their improvement.

5.1 HEMTs with thin buffers for high temperature electronics

The InAlN/GaN heterostructures grown on sapphire with ultrathin buffers described in Sec. 3.3.2 have been used for the fabrication of HEMTs that showed exceptional ON/OFF current ratios and good performance when operated at elevated temperatures. As already anticipated, in such ultrathin structures where the GaN channel thickness has been reduced down to 50 nm, the AlN nucleation layer acts as a back-barrier, resulting in a very good 2DEG confinement and strongly reduced buffer leakage currents. The processing of these heterostructures in HEMT devices has been performed by the University of Ulm. The HEMTs have been designed with particular attention to the suppression of leakage currents. The processing started with deep mesa etching down to the sapphire substrate, achieved by Ar/BCl_3/Cl_2 plasma in a RIE reactor. Ti/Al/Ni-based Ohmic contacts were deposited by e-beam evaporation and alloyed for 30 s at 800 °C in N_2 atmosphere. Prior to the formation of the 0.25 μm long Cu/Pt gates by electron beam lithography and metal evaporation, the samples surface was thermally oxidized at 800 °C in O_2-rich environment with the aim of reducing as much as possible the gate leakage currents [89]. Finally, contact pads were evaporated. Thanks to the mesa etching technology employed, the contact pads were evaporated on the sapphire substrate, avoiding thus buffer leakage currents originating from the large contact pads. The devices were left unpassivated. The drain-source and gate-source distance were 3 μm and 1 μm, respectively, while the gate

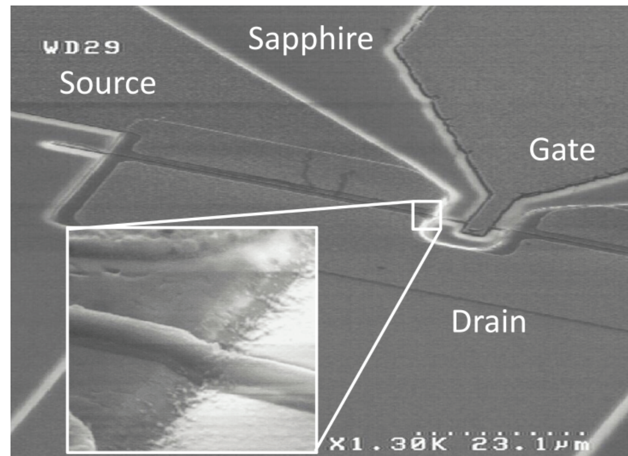

Figure 5.1: SEM micrograph of a HEMT processed out of an heterostructure with 50 nm GaN buffer. The inset shows a magnification of the mesa periphery.

width was 50 μm. A representative SEM picture of an HEMT with 50 nm GaN channel is shown in Fig. 5.1.

We will concentrate here only on the HEMTs with 50 nm GaN buffer thickness, as these are the transistors that showed the best ON/OFF current ratio. The two heterostructures grown with and without sapphire nitridation are compared, in order to link the effect of sapphire nitridation on 2DEG transport properties with HEMT characteristics. The output and transfer characteristics of the two HEMTs are compared in Fig. 5.2(a) and 5.2(b), respectively, showing markedly improved characteristics for the HEMT grown with sapphire nitridation. The maximum drain-source current $I_{DS,max}$ recorded at a gate-source voltage V_{GS} of 2 V is in fact increased from 0.24 A/mm to 0.36 A/mm, i.e. by 50%. It is important to note that the relatively low values of the maximum drain currents are due to several factors not directly related to the heterostructure quality. The InAlN oxydation, necessary for gate leakage current reduction, reduces the thickness of the barrier, which in turn lowers the 2DEG density to 8×10^{12} cm^{-2}. Therefore, even if the electron mobility was not degraded, the sheet resistivity is inevitably increased to 710 $\Omega/\square$. Furthermore, the Au-free ohmic contacts employed are characterized by a high contact resistivity of 4.5 Ω·mm. This, together with the long source-drain separation, gives rise to very high access and output resistances which reduce furthermore $I_{DS,max}$. The drain current ON/OFF ratio, extracted from the transfer characteristics of Fig. 5.2(b), is improved from 4×10^7 in the sample grown without nitridation to 5×10^9 in the sample grown with nitridation. These excellent values are in line with the improvement of the 2DEG transport properties and confirm that remarkable isolation can be achieved by the ultrathin buffer technology. The subthreshold swing is 90 mV/dec for both devices and is close to the values reported for other high quality InAlN/GaN HEMTs [181].

The effectiveness of the thin buffer technology in providing a strong control on 2D electrons and in suppressing leakage currents has been confirmed by testing the devices at high tempe-

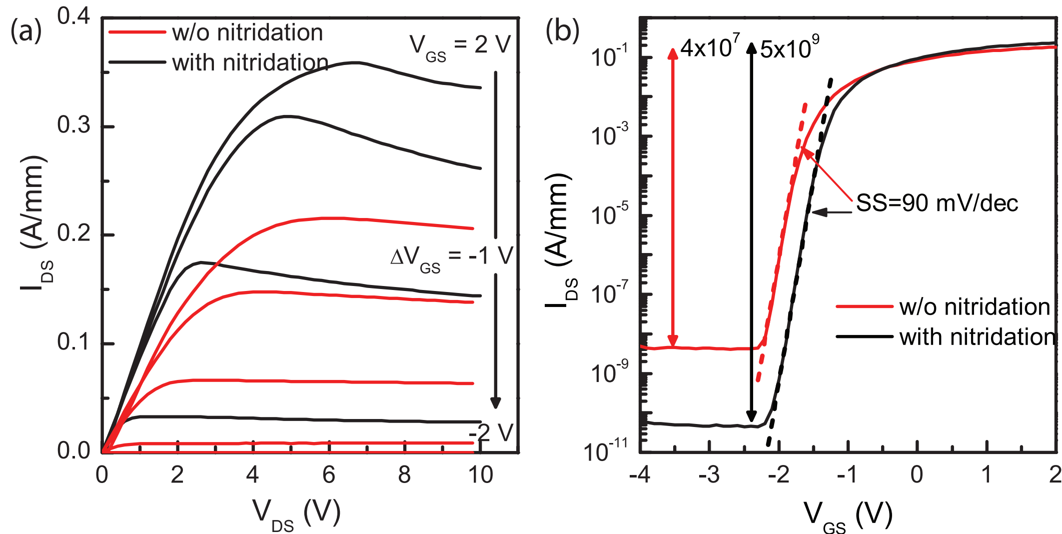

Figure 5.2: (a) Output characteristics of HEMTs fabricated on heterostructures with 50 nm GaN buffers grown with (black curves) and without (red curves) sapphire nitridation. The gate voltage is varied from +2 to −2 V, with steps of 1 V. (b) Semi-logarithmic transfer characteristic recorded at $V_{DS} = 6$ V for the same devices.

rature. The output and transfer characteristics recorded at room temperature and at 600 °C for the device grown with sapphire nitridation are shown in Fig. 5.3(a) and 5.3(b), respectively. The sheet resistance of the processed layer is increased from 710 Ω/□ to 1383 Ω/□ when passing from room temperature to 600 °C, which is due to a lowering of the electron mobility from increased optical phonon scattering, resulting in an increase of the ON-resistance from 8.7 Ω·mm to 11.6 Ω·mm. However, despite the increased ON-resistance, the saturated current measured at high drain-source voltage remains essentially the same, which may be explained by the rather temperature insensitive drift saturation velocity of GaN [182]. The high performance of the device at high temperature are furthermore confirmed by the tranfer characteristics, where we can see that the ON/OFF current ratio remains as high as 10^6 at 600 °C. Altough the current ON/OFF ratio is reduced by 4 orders of magnitude with respect to room temperature, it is important to stress that previous tests at high temperature of InAlN based HEMTs with thick buffers revealed a much stronger degradation of the ON/OFF current ratio and a very important shift of the threshold voltage [9]. This was ascribed to an increased conductivity of the GaN buffer, presumably due to activation of deep levels. The very thin GaN buffer of the devices described here reduces significantly these effects, assuring high performance even at such high temperatures.

5.2 InAlN/GaN HEMTs for high frequency applications

The main opportunity offered by InAlN/GaN HEMTs are high power, high frequency applications. HEMTs targeting such applications require high cutoff frequencies, in particular f_{max},

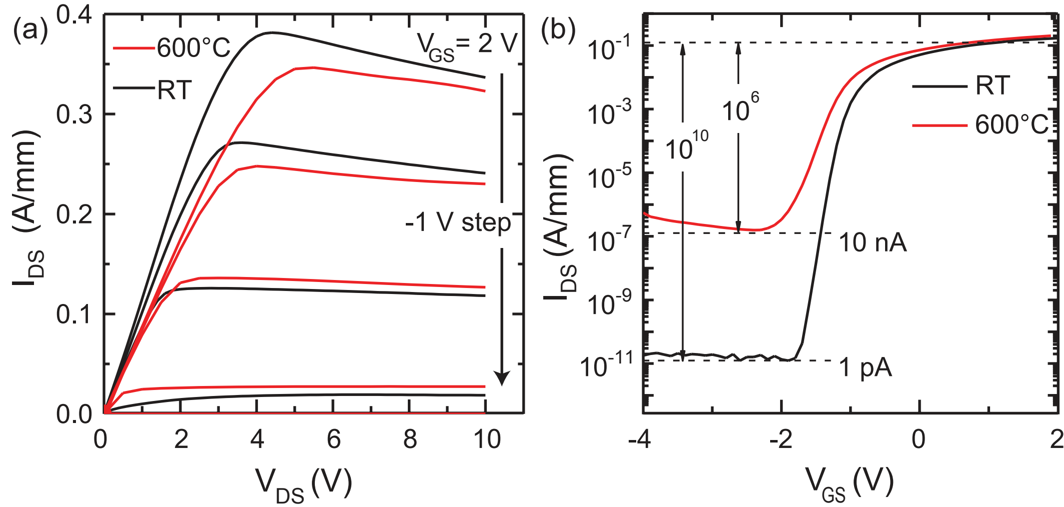

Figure 5.3: (a) Output characteristics at room temperature (black) and 600 °C (red) measured on a device with 50 nm GaN channel grown with sapphire nitridation. (b) Corresponding output characteristics measured at V_{DS} = 6 V.

high current densities and high breakdown voltages. Therefore, high electron mobilities and low 2DEG sheet resistivities are a fundamental requirement. Low contact resistivity is also very important for reduced access and output resistances. T-shaped gates have to be used in order to lower the gate resistance, which is a fundamental requirement for the achievement of high f_{max} values. On the other hand, the gate footprint is kept short as a high f_t is desired. Finally, the devices need to be passivated in order to limit as much as possible the phenomenon of current collapse. It is thus evident that such devices require a completely different approach with respect to the one adopted in the previous paragraph. The heterostructures intended for these applications need to be grown on SiC or Si substrates to limit self heating effects, and the buffer thickness is usually high (~ 2 μm) to provide the highest possible mobility. In this section we will cover two examples of InAlN/GaN HEMTs for high power, high frequency applications. The first case will be that of an HEMT on SiC designed for operation at 40 GHz, the second that of an HEMT on Si designed for 94 GHz operation. These devices have been fabricated and characterized by the group of prof. Bolognesi at ETH Zürich on InAlN/GaN heterostructures provided by EPFL.

5.2.1 InAlN/GaN HEMTs on SiC for large signal operation at 40 GHz

The HEMT presented in this section is based on an InAlN/GaN heterostructure on SiC whose layer stack is the following: AlN nucleation layer (100 nm) / GaN buffer layer (2 μm) / AlN spacer (1 nm) / InAlN barrier (3 nm) / GaN cap (2 nm). The growth of this layer has been described in Sec. 3.4. Hall effect measurements revealed an electron density of 1.6×10^{13} cm^{-2}, an electron mobility of 1470 cm^2/V·s and a sheet resistivity of 260 Ω/□. The pinch-off voltage, measured by ECV, is -1.7 V. HEMTs were fabricated starting with Ti/Al/Mo/Au (16/64/30/50

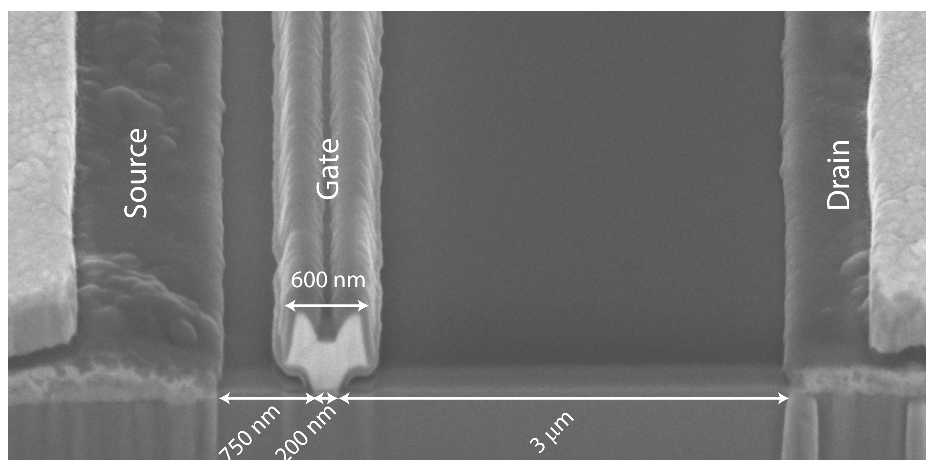

Figure 5.4: Cross sectional SEM micrograph of an InAlN/GaN HEMT designed for large signal operation at 40 GHz. Courtesy of Stefano Tirelli (ETH Zürich).

nm) ohmic contact deposition and rapid thermal annealing, which resulted in a contact resistivity of 0.3 Ω·mm. The post-processing sheet resistivity is 265 Ω/□, very close to the as-grown value, which shows that the layer did not degrade as a consequence of the ohmic annealing step. Device isolation was then achieved by mesa etching with Cl-based reactive ion etching. 2 × 50 μm T-shaped gates could be then fabricated by e-beam lithography and evaporation of Ni/Au (35/350 nm). The gate foot was 200 nm, the stem heigth 200 nm and the gate head size 600 nm. As the source-drain spacing was 4 μm, the gate electrode was offset towards the source, for a source-gate spacing of 750 nm. Finally, after deposition of a 70 nm PECVD SiN passivation layer, contact openings were patterned and etched, a Ti/Cu/Au metal stack was evaporated and lifted off to provide measurement pads. A cross section of a fabricated device is shown in Fig. 5.4. Note that this process has been developed before the achievement of *in situ* passivated hetestructures, which is the reason of the use of PECVD SiN.

The output characteristics for such device are shown in Fig. 5.5(a). The maximum current density, measured at $V_{GS} = 0$ V, is 0.86 A/mm. Compared to record values >2 A/mm obtained in other works for ultrascaled devices [13], the relatively low current density obtained is explained by the relatively long gate and the high source-drain separation which increase the access and output resistances. The device dimensions, which are well above the sub-μm and sub-100 nm values usually adopted for ultrafast HEMTs, have been chosen as such because in this case we are not targeting extremely high frequencies. For 40 GHz applications it is not interesting to aggressively scale-down the transistor dimensions. A reduction of the gate-drain spacing causes in fact a reduced breakdown voltage, while a short gate length enhances short channel effects. There is therefore a trade-off between the maximization of the cutoff frequency and the maximum power an HEMT can handle. For the device considered here, f_t and f_{max} measured at V_{GS} corresponding to peak transconductance are higher than 50 GHz and 150 GHz, respectively, over a wide range of V_{DS}, as shown in Fig. 5.5(b). The OFF-state breakdown voltage is, on the other hand, ~ 40 V. The chosen design could therefore guarantee

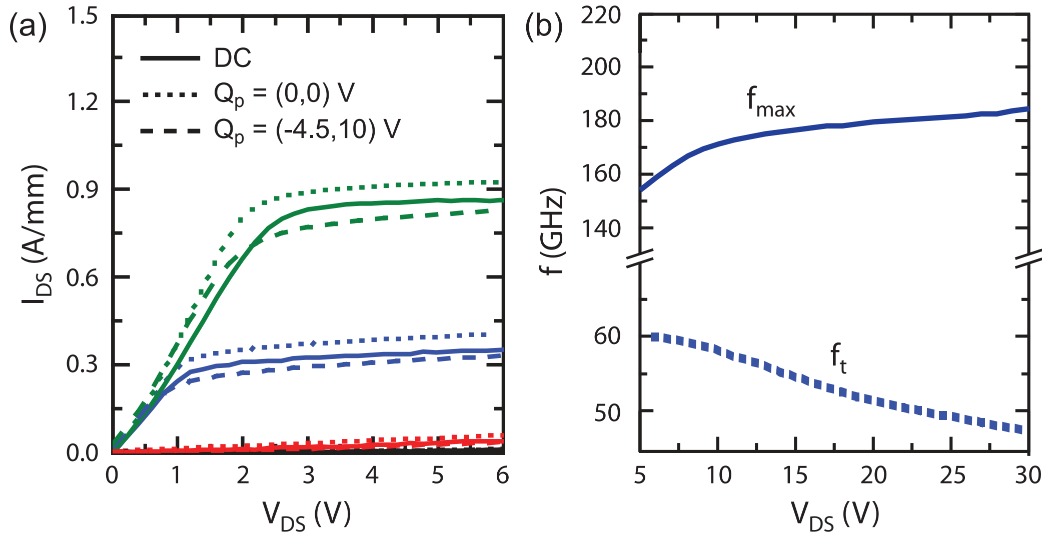

Figure 5.5: (a) Output characteristics measured under DC and pulsed conditions with two different quiescent bias points. V_{GS} is varied from 0 to -3 V in steps of 1 V. (b) V_{DS} dependence of f_t and f_{max} measured at peak transconductance.

a sufficiently high gain at 40 GHz and a relatively large breakdown voltage. Gate leakage currents, measured at $(V_{GS}, V_{DS}) = (-5, 0)$ V, amount to 160 μA/mm, which correspond to a current density of 80 A/cm^2 under the gate. Compared to the maximum current densities of a few A/cm^2 observed in Schottky diodes having similar barrier thickness (Fig. 4.10(b)), the value is larger by more than one order of magnitude. This is explained by the fact that at gate edges the electric field is strongly enhanced with respect to large diodes, resulting in higher currents. Experiments on FAT-FETs processed out of the same heterostructure revealed in fact gate current densities perfectly comparable with the ones reported in Sec. 4.3.1 for Schottky diodes. To further investigate the suitability of the device for large signal operation, pulsed measurements were performed to quantify the amout of current collapse. Fig. 5.5(a) shows the results of pulsed measuremets obtained in two different ways. In the first measurement, the quiescent bias is $(V_{GS}, V_{DS}) = (0, 0)$ V, while in the second measurement the quiescent bias is $(V_{GS}, V_{DS}) = (-4.5, 10)$ V. The difference between the two current levels is due to current collapse, which is generally lower than 20 %.

The large signal behavior of the transistor is reported in Fig. 5.6. The measurement are taken under optimal load conditions in order to maximize the power output. Class A-B conditions were adopted with quiescent bias chosen to give a quiescent drain current ~ 7% of the maximum drain current. The quiescent bias is $(V_{GS}, V_{DS}) = (-2.6, 35)$ V. The maximum power output is 27.5 dBm, corresponding to a power density of 5.85 W/mm. At the time of publication of the results [183], this constituted the highest power density ever reported for InAlN/GaN HEMTs at 40 GHz. The peak gain and PAE are 6 dB and 15.6%, respectively. The relatively low value of the PAE deserves some discussion. On one side, the peak of the PAE is obtained under strong gain compression. The peak gain is in fact obtained at an input power

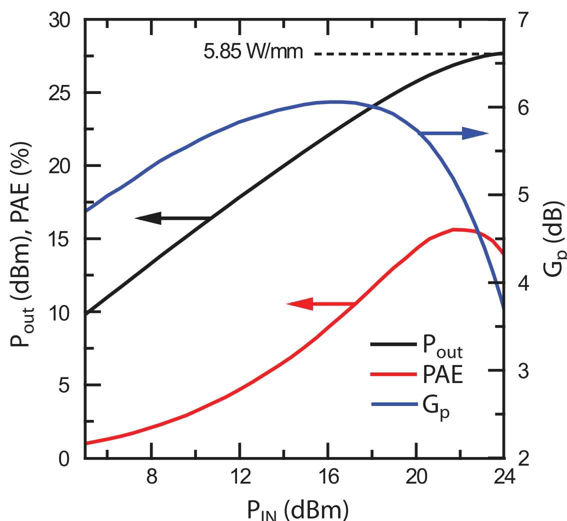

Figure 5.6: Large signal measurement at 40 GHz. The InAlN/GaN HEMT was biased at $(V_{GS}, V_{DS}) = (-2.6, 35)$ V.

lower with respect to the one for peak PAE. At peak PAE, the gain reduces to 5 dB, which means that the input power amounts to 32% of the output power. This fact alone already reduces the PAE to 68% of the maximum theoretical value. Furthermore, loadline analysis revealed that the drain bias sweeps between maximum and minimum values of $V_{max} = 51$ V and $V_{min} = 18$ V. The high value of V_{min} indicates that a very pronounced knee voltage walkout takes place during RF operation, probably as a consequence of the very high drain bias applied. As stated in Sec. 1.4.2, a poor V_{min}/V_{max} ratio is very deleterious for both the PAE and the power density. This means on one hand that devices performance are still hampered by strong dispersion effects, but at the same time this shows that if the dispersion could be attenuated, both the PAE and the saturated power density will be increased substantially.

5.2.2 InAlN/GaN HEMTs on Si for large signal operation at 94 GHz

We now turn our attention to Si-based InAlN/GaN HEMTs. We have seen in Sec. 3.5 that with respect to SiC substrates Si offers an inferior crystal quality and a poorer thermal dissipation. On the other hand, Si substrates are at least 10 times cheaper than SiC substrates, and when coming to MMIC applications they offer the advantage of allowing a much easier wafer thinning and via hole drilling with respect to SiC. It is therefore quite interesting to test the performance of Si based InAlN/GaN HEMTs, especially in the microwave W-band (75-110 GHz) and in particular at 94 GHz, as this frequency band is for the moment the upper limit of GaN based technologies.

HEMTs for W-band power amplification have been fabricated from the InAlN/GaN heterostructure grown on Si as described in Sec. 3.5. The layer sequence comprises an AlN nucleation layer, a 1 μm graded AlGaN strain management layer, a 1 μm GaN buffer and the barrier

stack which is constituted by a 1 nm AlN spacer, a 3.5 nm InAlN layer and a 2 nm GaN cap. Measurement of the room temperature transport properties by Hall effect revealed an electron density of 1.6×10^{13} cm^{-2}, an electron mobility of 1190 cm^2/V·s and a sheet resistivity of 320 Ω/□. With respect to the device studied in the previous section, power amplification at 94 GHz requires a downscaling of the transistors dimensions. The gate length needs to be reduced for higher cutoff frequency, as well as the source-drain separation. To reduce the access and output resistances, regrown ohmic contacts were integrated to the device. Transistor fabrication starting with mesa isolation by Cl-based RIE, followed by the deposition of a SiO_2 hard mask by PECVD which was patterned by optical lithography and SF_6-based dry etching to define the ohmic contact regions. A second dry etching step was performed to remove the barrier stack and a few nm of the GaN buffer from the same regions. Ohmic contacts were then regrown by NH_3-MBE at EPFL according to the method discussed in Sec. 4.2.2. After regrowth, the SiO_2 mask was removed with hydrofluoric acid and ohmic contacts were completed by e-beam evaporation of Ti/Pt/Au pads. The source-drain spacing is 2 μm. TLM measurements revealed a contact resistivity of 0.22 Ω·mm, which compares well with the one obtained in Sec. 4.2.2. With respect to the annealed contacts of the previously described device, regrown ohmics allowed for a ~ 30% reduction in contact resistivity. Once the ohmic contacts completed, 2 × 50 μm T-shaped gate electrodes were formed by e-beam lithography and Ni/Pt/Au metal evaporation. The gate length is 50 nm, the stem height 200 nm and the gate head 500 nm wide. The gates were offset towards the source, resulting in a gate-source spacing of 500 nm. The devices were then passivated with 75 nm of PECVD SiN, which was finally patterned for Ti/Au pad formation.

The DC output and transfer characteristics for the fabricated device are shown in Fig. 5.7(a) and 5.7(b), respectively. The maximum drain-source current at $V_{GS} = 2$ V is 1.6 A/mm, while the peak transconductance, measured at $(V_{GS}, V_{DS}) = (-1.5, 5)$ V, is 650 mS/mm. The output characteristic shows the presence of self-heating effects, which manifest in the form of an apparent negative differential resistance at high current densities. Output characteristics free of self-heating effects have been obtained by pulsed measurements using $(V_{GS}, V_{DS}) = (0, 0)$ V as quiescent bias point (dotted lines in Fig. 5.7(a)). In this case, the maximum current density reaches 2 A/mm, which compares quite well to the performance of the best SiC based devices [13]. The same measurement allow furthermore a more objective evaluation of short-channel effects. In fact, short channel effects manifest themselves as an increased I_{DS} with increasing V_{DS} in the saturation region, and can be masked by self-heating effects. The analysis shows that short channel effects are well present, which is a consequence of the short gate length. It is interesting to make a comparison with the device of Sec. 5.2.1, which had a 200 nm long gate and thus suffered of much weaker short channel effects. To complete the DC characterization, new pulsed measurements were performed using $(V_{GS}, V_{DS}) = (-4, 15)$ V as quiescent bias point to study the strength of current collapse phenomena. The results are shown as dashed lines in Fig. 5.7(a). It can be seen that dispersion phenomena are present and result in a reduced current density with respect to pulsed measurements taken with $(V_{GS}, V_{DS}) = (0, 0)$ V as quiescent bias point. However, the current is not reduced with respect

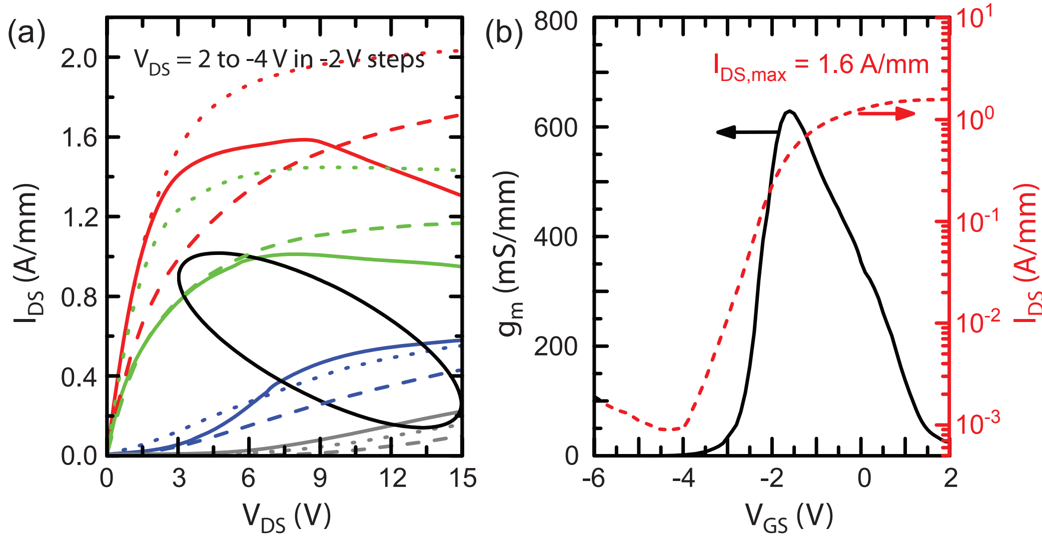

Figure 5.7: (a) Output characteristics of the InAlN/GaN HEMT on Si for 94 GHz large signal operation. Solid lines: DC masurements. Dotted lines: pulsed measurements with quiescent bias $(V_{GS}, V_{DS}) = (0,0)$ V. Dashed lines: pulsed measurements with quiescent bias $(V_{GS}, V_{DS}) = (0,0)$. $(V_{GS}, V_{DS}) = (-4,15)$ V. Pulse width: 500 ns. The black elliptical curve represents the reconstructed dynamic load line under large signal operation at 94 GHz. (b)DC transfer characteristic for the same device.

to DC values. Knee voltage walkout is also present as the maximum current density is reached at higher V_{DS} values if compared to the DC case. Finally, gate leakage currents, measured at $(V_{GS}, V_{DS}) = (-5,0)$ V, correspond to 250 μA/mm, higher with respect to the device of the previous section but still < 1 mA/mm.

The small signal performance of the device is shown in Fig. 5.8(a), where both f_t and f_{max}, measured at $V_{GS} = -1.25$ V, are displayed as a function of V_{DS}. The peak values of f_t and f_{max} are 118 and GHz and 210 GHz, respectively, which after pad de-embedding are improved to 141 GHz and 232 GHz. The high cutoff frequencies obtained here in comparison to the device of the previous section are due to the short gate length. The large signal performance under class A operation at 94 GHz are on the other hand presented in Fig. 5.8(b). The measurements are taken at a quiescent bias point $(V_{GS}, V_{DS}) = (-1.2, 9)$ V, which was chosen as the best trade-off between maximizing V_{DS} and keeping dispersion phenomena to acceptable levels. The maximum power gain is 6 dB, but is however reduced as the input power is progressively increased. The peak power added efficiency is 12%, corresponding to a gain of 4 dB and to an output power of 1 W/mm. For higher input powers, a saturated output power of 1.35 W/mm is achieved. Useful insight about the behavior under large signal operation are given by the reconstructed dynamic load line corresponding to the maximum output power, displayed as a black line in Fig. 5.7(a). The dynamic load line is not a straight line but has rather an elliptical shape due to the fact that the output impedance has both a real and an imaginary component. The critical role of dispersion in limiting the power output is well illustrated by

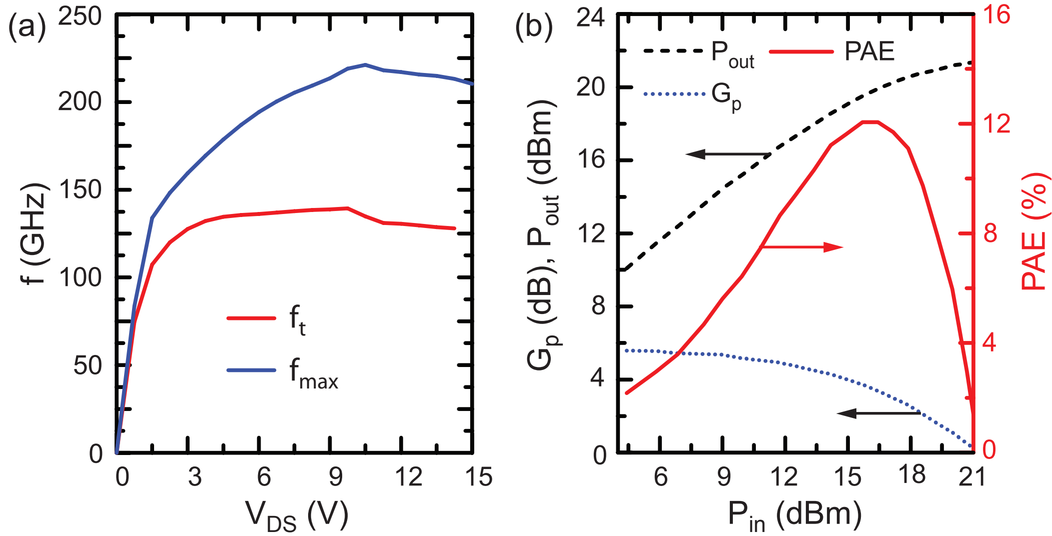

Figure 5.8: (a) V_{DS} dependence of the cutoff frequencies f_t and f_{max} for the InAlN/GaN HEMT on Si device. (b) Large signal measurement at 94 GHz. The InAlN/GaN on Si HEMT was biased at $(V_{GS}, V_{DS}) = (-1.2, 9)$ V.

the graph, as the load line is contained in the output characteristic recorded under pulsed conditions with quiescent bias $(V_{GS}, V_{DS}) = (-4, 15)$ V, which evidence dispersion phenomena, and not by the other ones. With respect to the device shown in the previous section, the pulsed measurements have been taken at a quiescent bias close to the one used for large signal measurements, making them a realistic representative of the device characteristics under large signal conditions.

5.2.3 Considerations about the potentials of InAlN/GaN HEMTs

The results reported in Sec. 5.2.1 and 5.2.2 constitute an interesting benchmark of the potentials of InAlN/GaN HEMTs for high power applications at high frequency. The devices presented set in fact the record in terms of power density for InAlN/GaN HEMTs at 40 GHz and 94 GHz. The data of Sec. 5.2.2 furthermore constituted, at the time of publication [189], the first report of large signal operation at 94 GHz for any GaN-based HEMT on Si. The power performance of InAlN/GaN HEMTs developed so far by the EPFL-ETHZ collaboration are reported in Fig. 5.9. The graph reports also the best power densities obtained by EPFL and ETHZ at 10 GHz and 94 GHz for InAlN/GaN HEMTs on SiC [183, 190]. The data are furthermore compared with the best results obtained for other GaN-based technologies. From the comparison it can be seen that InAlN/GaN HEMTs on SiC are superior to AlN/GaN HEMTs and are starting to seriously compete with AlGaN/GaN HEMTs for frequencies up to 40 GHz. What is most interesting is however the analysis of the performance at 94 GHz. First, it is important to note that InAlN/GaN based HEMTs from EPFL-ETHZ have already a maximum power output which is perfectly comparable with the state of the art of AlGaN/GaN HEMTs.

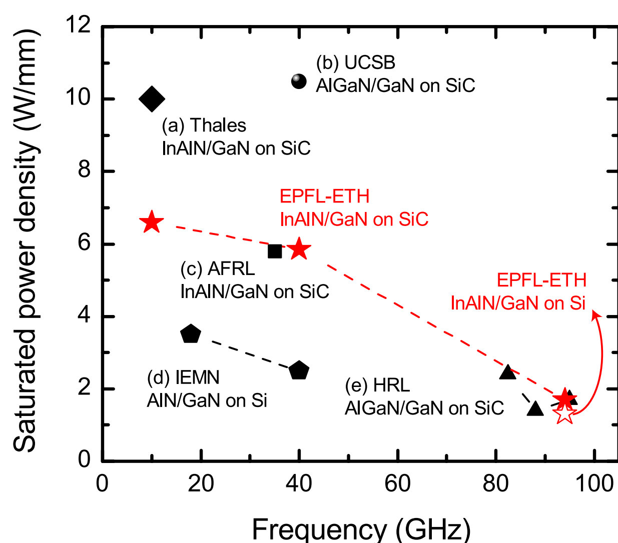

Figure 5.9: Saturated power density for GaN-based HEMTs at high microwave frequencies. Literature values are taken from: (a) [184], (b) [37], (c) [185], (d) [186], (e) [39, 187, 188].

Secondly, the highest reported power density for GaN-based HEMTs on SiC working at the same frequency is 1.7 W/mm [39], which is only slightly higher than the result reported here for Si based HEMTs. This shows that InAlN/GaN HEMTs on Si have all the potentials to provide a new platform for state of the art W-band power technologies.

The main issue of InAlN/GaN based HEMTs, being them grown on SiC or Si, remains a relatively low PAE which is mainly caused by strong dispersion phenomena. The nature and location of the traps determining dispersion is still unknown, but it is interesting to note that the amount of current collapse was similar for the two devices of Sec.s 5.2.1 and 5.2.2. Therefore, it seems that the amount of traps determining dispersion effects is not directly correlated with the substrate material or the dislocation density. A possible origin of such traps may be the InAlN layer itself. We have seen in Sec. 2.4 that the room temperature emission rate of oxygen-related levels ranges between 10^7 s^{-1} and 10^8 s^{-1}, which is well below the typical operation frequency of these devices. The trapping and detrapping rates of the deep levels involved in gate leakage currents are low too (see Fig. 4.11), making this trap level another possible candidate. However, it is important noting that the InAlN based devices reported in [184] and [185] have lower dispersion levels and PAE closer to the theoretical values. Therefore, it is more likely that the important current collapse observed in our devices is due to a not optimal passivation. The use of refined passivation methods like *in situ* SiN passivation or the implementation of different passivating materials like Al_2O_3 [191] may therefore constitute interesting strategies for achieving higher PAE and consequently higher output power densities. The suppression of short channel effects, which as we have seen are still important in devices with short gate lengths, is also important for the improvement of the transistor performance. In particular, the suppression of short channel effects will increase the device transconductance and the drain-source resistance, which will enhance both cutoff frequencies f_t and f_{max}, according

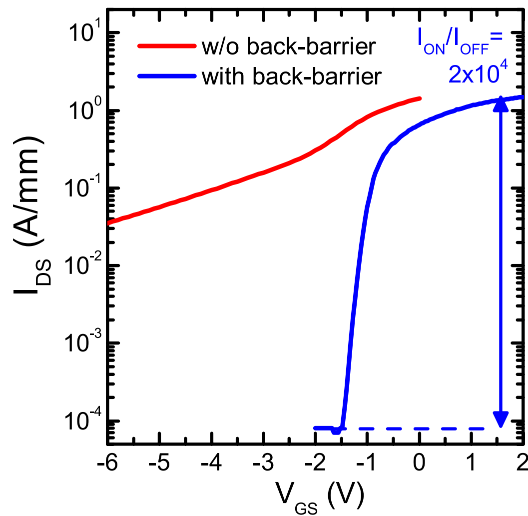

Figure 5.10: Comparison of the DC transfer characteristic of two InAlN/GaN based HEMTs on SiC with identical barrier stack (total thickness of 6 nm) and gate length of 75 nm but different buffer composition. While one device has a simple GaN buffer (red line), the other has an $Al_{0.04}Ga_{0.96}N$ back-barrier and a 50 nm GaN channel (blue line).

to Eq. 1.35 and 1.36. The device will therefore benefit from a higher power gain, resulting in better PAE. Some preliminary results concerning the effect of a back-barrier on InAlN/GaN HEMTs on SiC is shown in Fig. 5.10. The graph compares the transfer characteristics of two HEMTs having a 75 nm long gate and a barrier with total thickness of 6 nm (1 nm AlN spacer / 3 nm InAlN barrier / 2 nm GaN cap). The difference between the two devices resides in the fact that one has a standard GaN buffer, while the other has an $Al_{0.04}Ga_{0.96}N$ buffer and a 50 nm GaN channel. The growth of the two layers has been described in Sec. 3.4 and 4.5, respectively. As can be seen, the back-barrier improves significantly the transfer characteristic, reducing by 3 orders of magnitude the OFF-state current. The maximum drain current, on the other hand, is not reduced and is ~ 2 A/mm for both devices. These results show that back-barriers can effectively improve the electrostatic control of the 2DEG in short-gate InAlN/GaN HEMTs. Therefore, it is likely that back-barriers will play a role in the developement of efficient InAlN/GaN power HEMTs.

6 Conclusions

6.1 Summary of the results

An accurate model for the description of band profiles in InAlN/GaN heterostructures and Schottky diodes has been established based on experimental electrochemical CV measurements on a series of heterostructures with different barrier thicknesses and Schrödinger-Poisson simulations. In particular, InAlN/AlN polarization induced interface charge density, InAlN dielectric constant, surface potential and Schottky barrier height in Ni/InAlN Schottky contacts were dermined. These parameters, together with other additional ones already known, allowed the modelization through Schrödinger-Poisson simulations of the 2DEG density, pinch-off voltage and bias dependent electric fields in the barrier.

Very deep levels in InAlN were investigated by means of photocapacitance spectroscopy, extending the range of energy levels investigated by admittance spectroscopy. The study was carried out on thick InAlN layers rather than on HEMT heterostructures in order to avoid spurious effects caused by surface states or states in the GaN buffer. A gaussian distribution of traps with optical ionization energy centered around 1.7 eV and broadening parameter $\Delta E = 0.38$ eV was identified, explaining the dependence of the optical cross section on both photon energy and temperature.

Thanks to band profile simulations and the knowledge of the presence of deep levels in InAlN, it could be proven that gate leakage currents in InAlN/GaN HEMTs with thin barriers originate from a trap assisted tunneling mechanism involving the deep levels located 1.7 eV below the InAlN conduction band edge. The model allowed an accurate fitting of the whole reverse-bias current-voltage-temperature characteristic of InAlN/GaN based Schottky diodes with InAlN barrier thickness ≤ 7 nm. For thicker layers, the emergence of a different conduction mechanism was observed. This second mechanism could produced leakage currents as high as 100 A/cm^2 and was linked to the appearance of anomalous features in the electrochemical CV characteristic. It could be thus concluded that small, degraded, highly doped regions form within the InAlN layer. There, the strong band bending induced by the high doping makes direct tunneling very efficient, which finally results in high leakage currents. Therefore, an

efficient method to keep gate leakage currents to low levels is to use heterostructures with thin InAlN barriers.

Besides Schottky contacts, ohmic contacts were also studied. In particular, it was explored the possibility of obtaining low resistivity regrown ohmic contacts by NH_3-MBE. For this purpose, it turned out that an appropriate surface preparation procedure before regrowth is a critical step for the achievement of a smooth regrowth surface and a good contact between the regrown material and the 2DEG. The optimized process allowed for ohmic contacts with specific resistivity as low as 0.2 Ω·mm without the need of annealing, to be compared with the ~ 0.3 Ω·mm usually obtained with standard annealed contacts. Annealed contacts have the additional disadvantage of inducing the formatin of a 1 nm thick amorphous layer at the InAlN surface, which is avoided in the case of regrown ohmics.

Concerning the growth of InAlN/GaN heterostructures, it was explored on three different substrates. The usual sapphire substrates, cheap and with well established nitride growth procedures, have been used not only for the growth of standard heterostructures, but have been also chosen for the growth of InAlN/GaN heterostructures with ultrathin buffers. Thanks to a careful optimization of the growth conditions and to the identification of the importance of appropriate sapphire nitridation prior to growth, the buffer thickness could be reduced to just 50 nm while at the same time keeping a > 1000 $cm^2/V \cdot s$ electron mobility. The main parameters affecting electron mobility in this kind of heterostructures was investigated and it was demonstrated that interface roughness, and not dislocation related scattering, is the main electron mobility mechanism. HEMTs were processed out of InAlN/GaN heterostuctures with 50 nm GaN buffer. Thanks to the very efficient isolation allowed by the thin buffer technology and the back-barrier effect of the AlN nucleation layer, the devices showed a very high ON/OFF current ratio of 5×10^9 and 10^6 at room temperature and at 600 °C, respectively. These results show that InAlN/GaN HEMTs with thin buffers hold a great potential for high temperature electronics. The high thermal stability of InAlN based heterostructures could be furthermore increased by adding a very thin (≥ 0.5 nm) GaN cap layer on top of the InAlN barrier. With this technique, heterostructures could be made stable for temepratures up to 850 °C in MOVPE environments, which allowed the achievement of damage-free *in situ* SiN passivated heterostructures with state of the art transport properties.

The second substrate adopted for InAlN/GaN heterostructure growth was SiC. This substrate allowed for state of the art transport properties and was used for the fabrication of HEMTs for large signal operation at 40 GHz. These devices achieved a record power density of 5.85 W/mm at this frequency.

The last substrate used was Si. The growth on this substrate required the development of an appropriate growth scheme to avoid cracking due to thermal expansion related issues. Crack-free heterostructures with high electron mobility could be achieved with the use of a 1 μm graded AlGaN strain management layer. These structures were used for HEMT fabrication, implementing regrown contacts too, and tested under large signal operation at 94 GHz. A

saturated power density of 1.3 W/mm was obtained, together with a peak PAE of 12%.

Finally, InAlN/GaN heterostructures implementing an $Al_{0.04}Ga_{0.96}N$ back-barrier for increased electrostatic control over the 2DEG could be achieved on sapphire substrates while at the same time preserving state of the art transport properties. The back-barrier technology could be easily transferred to SiC and Si substrates.

6.2 Outlook

The results obtained during this work pointed out the great potentials of InAlN/GaN HEMTs for different applications. On one hand, it has been demonstrated that InAlN/GaN HEMTs are capable of good performances at very high temperatures and that appropriately designed InAlN/GaN heterostructures can be made very stable at temperatures as high as 800 °C. However, operation at these extreme environments is not only challenging for the semiconductor, but also for the metal contacts. A further step in this direction may be the design and implementation of devices with refractory metal contacts. This may be difficult for ohmic contacts, but the regrowth technology may help in this sense. The high temperature stability of these devices should be tested over longer periods with respect to the ones explored in this work. Devices of this kind would not be only interesting as RF emitters, but also as sensors for extreme environments.

Concerning mm-wave applications, the main challenge presently faced by InAlN/GaN HEMTs is still a low PAE. In this sense a better understanding of the nature of the traps involved in current collapse phenomena would be highly beneficial. In particular, it will be necessary to clarify if surface traps or rather traps in the InAlN barrier are responsible for dispersion phenomena. In the former case, better surface passivation may be the solution, while in the latter case it will be probably useful to act on the growth conditions of InAlN. A better PAE, coupled to the very high power densities achievable by InAlN/GaN HEMTs for frequencies up to 100 GHz, will make these devices a very serious alternative to GaAs or InP based amplifiers, as they will allow for a reduced chip size. Millimeter-wave monolithic microwave integrated circuits will likely integrate regrown contacts and the possibility of having good devices on Si will make their process cheaper and easier with respect to SiC based devices. This would pave the way to the integration of InAlN/GaN based devices in millimeter-wave systems such as high resolution radars or E-band communication systems.

A The Fang-Howard approximation

A.1 The Fang-Howard wavefunction

The wavefunction of a 2D electron gas can be written, thanks to the invariance of the confining potential in the direction parallel to the heterointerface, as $\Psi(z,\rho) = \psi(z)e^{i\mathbf{k}_{\parallel}\cdot\rho}$, where z and ρ are, respectively, the coordinates in the directions perpendicular and parallel to the heterointerface, and $\mathbf{k}_{\parallel}$ is the electron wavevector. $\psi(z)$ is obtained from the Schrödinger-Poisson equation:

$$\left[-\frac{\hbar^2}{2}\frac{\mathrm{d}}{\mathrm{d}z}\left(\frac{1}{m^*(z)}\frac{\mathrm{d}}{\mathrm{d}z}\right)+V(z)\right]\psi(z)=E\psi(z) \tag{A.1}$$

where $m^*(z)$ is the position dependent effective mass and $V(z)$ is the potential, which comprises contributions coming from conduction band offsets, fixed charges (ionized dopants, polarization charges etc.) and the electrical potential generated by the electron distribution itself. Eq. A.1 must be therefore solved self-consistently. $\psi(z)$ can be evaluated numerically by means of Schrödinger-Poisson simulators, but having an analytical approximation of $\psi(z)$ is more advantageous. For example, the calculation of the electron mobility of a 2DEG requires the explicit knowledge of the electron wavefunction $\psi(z)$ as the latter is needed for the evaluation of the form factor $G(q)$ (Eq. 2.10). The most convenient approximation is the one given by the Fang-Howard wavefunction:

$$\psi_{FH}(z)=\begin{cases}0 & z<0\\ \sqrt{\frac{b^3}{2}}ze^{-bz/2} & z\geq 0\end{cases} \tag{A.2}$$

where b is a variational parameter. The zero of the z coordinate has been put here at the heterointerface. The optimum value of b is [108]:

$$b=\left(\frac{33m^*e^2n_s}{8\hbar^2\epsilon_0\epsilon_b}\right)^{1/3} \tag{A.3}$$

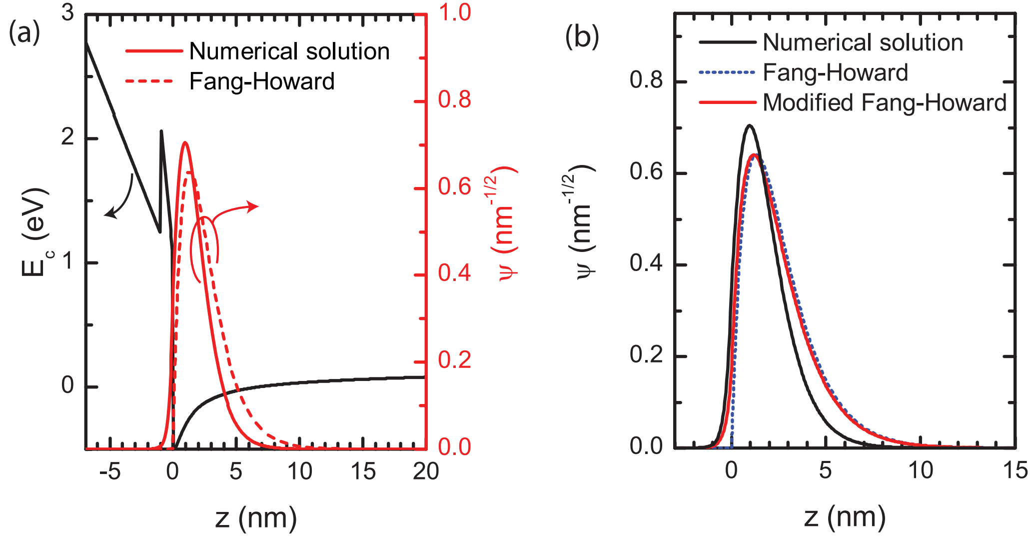

Figure A.1: (a) Comparison between the numerically calculated and the Fang-Howard ground state wavefunction of an InAlN/GaN heterostructure with 1.6×10^{13} cm^{-2} sheet electron density. (b) Comparison between the Fang-Howard and the modified Fang-Howard wavefunction for the same heterostructure.

A comparison between the Fang-Howard wavefunction and the numerically calculated one for a 2DEG with 1.6×10^{13} cm^{-2} sheet electron denisty is shown in Fig. A.1(a).

The Fang-Howard approximation allows to extract analytical expressions of several parameters of interest. The energy of the ground state with respect to the minimum of the conduction band, which has been used in Eq. 1.16, turns out to be:

$$E_0 = \left(\frac{9\pi\hbar e^2 n_s}{8\epsilon_0\epsilon_{GaN}\sqrt{8m_{GaN}}} \right)^{2/3} \tag{A.4}$$

The form factor entering electron mobility calculations can be also obtained:

$$G(q) = \iint \psi^2(z)\psi^2(z')e^{-q|z-z'|}\mathrm{d}z\mathrm{d}z' = \frac{1}{8}\left(2\eta^3 + 3\eta^2 + 3\eta\right) \tag{A.5}$$

where

$$\eta = \frac{b}{b+q} \tag{A.6}$$

A.2 The modified Fang-Howard wavefunction

The wavefunction of Eq. A.2, altough being very practical for most of the relevant mobility related calculations, has the drawback of being zero in the barrier region. This is equivalent

to consider the barrier as infinitely high. However, alloy scattering is a mobility limiting mechanism intrinsically related to the penetration of the electron wavefunction in the barrier region. This difficulty can be overcome by using a modified Fang-Howard function:

$$\psi_{M-FH}(z) = \begin{cases} Me^{\kappa_b z/2} & z < 0 \\ N(z+z_0)e^{-bz/2} & z \geq 0 \end{cases} \tag{A.7}$$

where b is the same as in Eq. A.3 and $\kappa_b = 2\sqrt{2m_B^* \Delta E_c/\hbar^2}$ is the wavevector characterizing the wavefunction penetration into the barrier. ΔE_c is the conduction band offset between the GaN channel and the barrier material, while m_b^* is the electron effective mass in the barrier. z_0, N and M are on the other hand constants whose values are derived from normalization and continuity conditions:

$$\begin{aligned} z_0 &= \tfrac{2}{b+\kappa_b m_B/m_{GaN}} \\ N &= \sqrt{\tfrac{b^3}{2}}\left(1 + bz_0 + \tfrac{1}{2}b^2 z_0^2\left(1+\tfrac{b}{\kappa_b}\right)\right)^{-1/2} \\ M &= Nz_0 \end{aligned} \tag{A.8}$$

The standard and modified Fang-Howard functions are compared in Fig. A.1(b). Based on Eq. A.7, the probability P_b of finding the electron in the barrier can be calculated:

$$P_b = \frac{N^2 z_0^2}{\kappa_b} \tag{A.9}$$

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Acronyms

2DEG	2 dimensional electron gas
AFM	atomic force microscopy
BFOM	Baliga's figure of merit
CV	capacitance-voltage
DD	dislocation density
DIBL	drain induced barrier lowering
DLTS	deep level transient spectroscopy
ECV	electrochemical capacitance-voltage
HEMT	high electron mobility transistor
JFOM	Johnson's figure of merit
LM	lattice-matched
MBE	molecular beam epitaxy
MIS	metal insulator semiconductor
MIS-HEMT	metal insulator semiconductor high electron mobility transistor
MMIC	monolithic microwave integrated circuit
MOVPE	metal organic vapor phase epitaxy
NH_3-MBE	ammonia molecular beam epitaxy
PAE	power added efficiency
PAMBE	plasma assisted molecular beam epitaxy
PECVD	plasma assisted chemical vapor deposition
RHEED	reflection high energy electron diffraction
RTA	rapid thermal annealing
SIMS	secondary ion mass spectrometry
TAT	trap assisted tunneling
TEM	transmission electron microscopy
TLM	transmission line measurement
QTH	quartz tungsten halogen
QW	quantum well
XBO	Xenon arc lamp
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

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Education

2011-2015	**Ph.D. in Photonics** – École Polytechnique Fédérale de Lausanne
2008-2010	**Master's degree in Materials Science** – University of Pisa, Italy**.**
2005-2008	**Bachelor's degree in Chemical Sciences and Technologies** – University of Pisa, Italy (3 months internship at Université Paris Diderot, France)
2005-2010	**Fellow student, Scuola Normale Superiore di Pisa**, class of sciences

Skills

Semiconductor technologies: metal organic chemical vapor deposition, photolithography, dry etching, metal deposition, rapid thermal annealing

Materials characterization: X-ray diffraction, atomic force microscopy, scanning electron microscopy, photoluminescence

Device characterization: current-voltage, capacitance-voltage, deep level transient spectroscopy, admittance spectroscopy

Numerical modeling: Matlab, numerical resolution of differential equations, Schrödinger-Poisson simulations

Computing: Origin, Adobe suite products, LaTeX, Microsoft Office suite

Team work and project management: work in international teams and environments, time management, respect of deadlines and financial constraints, maintain of communication and collaboration between two research teams

Communication: oral and poster presentations at international conferences, writing of project reports, publication of 7 articles in high impact scientific journals

Projects

2011-2015 **École Polytechnique Fédérale de Lausanne** – Ph. D. project – *"Leakage mechanisms and contact technologies in InAlN/GaN high electron mobility transistors"*

- Growth and characterization of GaN based heterostructures
- Numerical modeling of leakage currents in InAlN/GaN based transistors
- Fabrication and modelization of InAlN/GaN based Schottky diodes
- **Main objectives**: development of nitride based devices for harsh environment electronics and achievement of compact and efficient microwave power sources
- **Main achievements**: transistors suitable for very high temperature operation (up to 600°C), record power density (5.85 W/mm) for InAlN/GaN transistors at 40 GHz

09-12/2014 **Venturelab** – Venture challenge: a team based business course focused on startup creation

- Proposition of a startup project and coordination of the team in charge of the project
- Elaboration and presentation of a business plan

2009-2010 **NEST Laboratory – Scuola Normale Superiore** – Master project – *"Growth and structural study of InAs-InSb heterostructured nanowires"*

- Investigation of the growth mechanism of InSb nanowires
- **Main achievements**: synthesis of defect-free InSb nanowires, elaboration of a growth model for InSb nanowires

05-07/2008 **Laboratoire MPQ - Université Paris Diderot** – Bachelor project – *"Design and processing of quantum cascade laser waveguides for THz transfer onto optical carriers"*

- Fabrication of THz quantum cascade lasers with high modulation frequency
- **Main achievements**: minimization of parasitic elements and improvement of the maximum modulation frequency from 13 to 24 GHz.

Publications

Peer reviewed articles:

D. Marti, S. Tirelli, V. Teppati, **L. Lugani**, J.-F. Carlin, M. Malinverni, N. Grandjean, and C. R. Bolognesi, "94-GHz large-signal operation of AlInN/GaN high-electron-mobility transistors on silicon with regrown ohmic contacts", *IEEE Electron Device Lett.* **36**, 17 (2015)

L. Lugani, M. Malinverni, S. Tirelli, D. Marti, E. Giraud, J.-F. Carlin, C. R. Bolognesi, and N. Grandjean, "n^+-GaN grown by ammonia molecular beam epitaxy: Application to regrown contacts", *Appl. Phys. Lett*. **105**, 202113 (2014)

M. A. Py, **L. Lugani**, Y. Taniyasu, J.-F. Carlin, and N. Grandjean, "Shallow donor and deep DX-like center in InAlN layers nearly lattice-matched to GaN", *Phys. Rev. B* **90**, 115208 (2014)

L. Lugani, J.-F. Carlin, M. A. Py, and N. Grandjean, "Thermal stability and *in situ* SiN passivation of InAlN/GaN high electron mobility heterostructures", *Appl. Phys. Lett.* **105**, 112101 (2014)

L. Lugani, M. A. Py, J.-F. Carlin, and N. Grandjean, "Leakage mechanisms in InAlN based heterostructures", *J. Appl. Phys.* **115**, 074506 (2014)

S.Tirelli, **L. Lugani**, D. Marti, J.-F. Carlin, N. Grandjean, and C. R. Bolognesi, "AlInN-based HEMTs for large-signal operation at 40 GHz", *IEEE Trans. Electron Devices* **60**, 3091 (2013)

S. Tirelli, D. Marti, **L. Lugani**, J.-F. Carlin, N. Grandjean, and C. R. Bolognesi, "AlN-capped AlInN/GaN high electron mobility transistors with 4.5W/mm output power at 40 GHz", *Jpn. J. Appl. Phys*. **52**, 08JN16 (2013)

L. Lugani, J.-F. Carlin , M. A. Py, D. Martin, F. Rossi, G. Salviati, P. Herfurth, E. F. Kohn, J. Bläsing, A. Krost, and N. Grandjean, "Ultrathin InAlN/GaN heterostructures on sapphire for high on/off current ratio high electron mobility transistors", *J. Appl. Phys.* **113**, 214503 (2013)

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