Functional Description and Control Design of Modular Multilevel Converters - Towards Energy Storage Applications for Traction Networks

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Abstract

Following the permanent increase in mobility and passenger traffic, the security of supply is progressively becoming an important concern of the energy supply of most railway networks. This problem is particularly important in the networks supplied with a special frequency of 16.7 Hz, because these networks often suffer from a relative seclusion from the conventional 50 Hz grid and possess very limited opportunities of expansion with respect to both the production and transport of electricity. This situation calls for the improvement of the interconnection with the 50 Hz network and also creates a need for *ancillary services*, particularly in relation to power quality concerns.

In both perspectives, Modular Multilevel Converters (MMC) are highly attractive as they constitute a technology that is ideally suited for the corresponding voltage and power levels and are also sufficiently versatile to easily adapt to the numerous applications affected by these needs, still emerging and hence only partially identified.

Furthermore, this attractiveness is even further increased in case energy storage is integrated inside the converters, which are then capable of providing a very broad range of ancillary services. Practically, such a perspective is enabled by the fact that the submodules can be directly used to integrate storage in a distributed manner, essentially limiting the stakes of the design of such a facility to control issues.

At the end of 2014, and in barely more than a decade, MMCs (or their variants) have been adopted by most of the major power electronics manufacturers (ABB, Siemens, Alstom, etc.) and constitute a rapidly expanding topic, catching the attention of more than seventy academic research groups worldwide. This clearly illustrates the breakthrough represented by this technology, which is notably due to the fact that their modular nature imposes operating principles that are fundamentally different from those of conventional structures, but what also allows unprecedented flexibility and scalability.

With no less than 13 ongoing MMC projects related to frequency conversion facilities for railway networks – counting only those already held by Siemens – the relevance of this technology in these applications is largely proven. However, the integration of distributed storage (or *split storage*) in MMCs has still received only little attention. This thesis will even propose the use of *hybrid* split storage, which has apparently not been

studied at all. In both cases, the development of *energy management* mechanisms has apparently not been addressed yet and the control design as a whole is also limited to few developments only. On the other hand, there are already numerous control solutions adapted to the cases without storage, among which it is sometimes difficult to make wise choices. In this context, before adding energy storage (and its associated management mechanisms) to already complex control problems, it is important to rely on a sound basis. This is the main motivation for this thesis to search for a set of *analysis tools* that can allow to take a step back on the control design in general.

Firstly, this thesis develops different representations of MMCs, providing a macroscopic view of their intrinsic behavior and allowing a new interpretation of their basic principles of operation. As it will be seen, these results are useful for control design purposes as well as system engineering in general. Secondly, using the principles of the Energetic Macroscopic Representation (EMR), this work presents a methodology for the systematic control design of MMCs, based on the principle of functional inversion of a system model. Finally, the obtained results are applied and validated on known structures before being extended to other converter systems including energy storage. In parallel to these developments, several digressions are also made to comment on the issues related to the control hardware design and on the possible applications of energy storage in railways.

In the end, these developments are expected to contribute to the improvement of the modularization of the control in general, which is one of the possible ways to provide maximum flexibility, speed and effectiveness in the overall design of MMC systems for all types of applications.

Keywords: Modular Multilevel Converters, Energy storage, Energetic Macroscopic Representation, Functional description, Inversion-based control, Hybrid split storage, Unbalanced grid conditions, Circulating current, Frequency conversion, Power quality, Network intertie, Ancillary services, Railway network, Systemic analysis, Battery-based energy storage, Supercapacitors.

Résumé

Suite à l'augmentation de la mobilité et à l'accroissement du trafic, la sécurité d'approvisionnement en énergie des réseaux électriques ferroviaires devient de plus en plus difficile à garantir. Cette problématique est particulièrement importante dans les réseaux alimentés en 16.7 Hz, qui souffrent souvent d'un certain isolement vis-à-vis du réseau 50 Hz conventionnel et sont pratiquement condamnés au status-quo en termes de capacités de production et de transport d'énergie. Cette situation exige un accroissement du niveau d'interconnexion avec le réseau 50 Hz et crée également un besoin en *services système*, notamment par rapport à des problèmes de qualité de la tension.

Dans ces deux perspectives, les Convertisseurs Modulaires Multiniveaux (MMC) ont sans doute une belle carte à jouer car ils constituent une technologie à la fois idéalement adaptée aux niveaux de tension et de puissance concernés, mais sont également suffisamment versatiles pour s'adapter facilement aux nombreuses variantes d'applications concernées par ces besoins, encore naissants et ainsi relativement mal définis.

Par ailleurs, l'intérêt de cette technologie est encore accru si l'on envisage d'intégrer directement du stockage d'énergie au sein des convertisseurs, qui deviennent ainsi capables de fournir une large palette de services système. Concrètement, une telle perspective est rendue possible par le fait que les sous-modules peuvent être directement exploités afin d'intégrer du stockage de manière distribuée, limitant ainsi essentiellement les enjeux d'une telle installation à des problématiques de contrôle.

À fin 2014, et en à peine plus de dix ans, les MMCs (ou leurs variantes) ont été adoptés par la plupart des acteurs majeurs de l'électrotechnique (ABB, Siemens, Alstom, etc.) et constituent un sujet en pleine expansion, dans lequel plus de septante groupes de recherche académiques sont actuellement impliqués dans le monde. La petite révolution que représente cette technologie est en majeure partie liée au fait que sa nature modulaire impose des principes de fonctionnement qui sont fondamentalement différents de ceux des structures conventionnelles, mais autorise également une très grande flexibilité, qui est également nouvelle.

Avec pas moins de 13 projets de MMC – rien que chez Siemens – pour des convertisseurs de fréquence liés aux réseaux ferroviaires, la pertinence de cette technologie dans ces applications n'est plus à prouver. En revanche, l'intégration de stockage dis-

tribué (ou *split storage*) dans les MMCs reste encore peu étudiée. La présente thèse proposera même le recours à du stockage distribué *hybride*, qui n'a apparemment fait l'objet d'aucune étude antérieure. Dans ces deux cas, le développement de mécanismes de gestion énergétique (*energy management*) n'a apparemment pas encore été abordé et le *control design* dans son ensemble reste également limité à un état embryonnaire. D'un autre côté, il existe déjà de très nombreuses solutions de contrôle adaptées au cas sans stockage, entre lesquelles il est parfois difficile de faire des choix avisés.

Dans ce contexte, avant de rajouter du stockage d'énergie (et les mécanismes de gestion associés) à des problèmes de contrôle déjà complexes, il convient de s'assurer que l'on dispose de bases saines, c'est pourquoi cette thèse vise à fournir un ensemble d'outils d'analyse permettant de prendre un certain recul sur le control design en général.

En premier lieu, cette thèse développe différentes représentations offrant un point de vue macroscopique sur le fonctionnement des MMCs et permettant une interprétation nouvelle de leur fonctionnement. Comme on le verra, ces résultats sont utiles au control design ainsi qu'au system engineering en général. En second lieu, en utilisant les principes de la Représentation Énergétique Macroscopique (REM), ce travail présente une méthodologie de control design systématique reposant sur le principe de l'inversion fonctionnelle d'un modèle du système. Finalement, les résultats obtenus sont appliqués et validés sur des structures connues, avant d'aborder comment ils peuvent être exploités dans le cas des systèmes avec stockage. En parallèle à ces développements, plusieurs digressions sont également faites afin de commenter les enjeux du développement du hardware de contrôle, ainsi que les applications du stockage d'énergie dans le domaine ferroviaire.

Au final, ces différents développements sont appelés à contribuer à l'amélioration de la modularisation du contrôle en général, qui est une des pistes possibles afin d'offrir un maximum de flexibilité, de rapidité et d'efficacité dans la conception de solutions de conversion statique pour tout types d'applications.

Mots clés : Convertisseurs modulaires multiniveaux, Stockage d'énergie intégré, Représentation énergétique macroscopique, Description fonctionnelle, Contrôle basé sur l'inversion, Stockage distribué hybride, Réseau déséquilibré, Conversion de fréquence, Services système, Réseaux électriques ferroviaires, Analyse systémique.

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GENERAL CONTEXT AND MOTIVATIONS

Abstract – This chapter introduces the context in which this thesis has emerged and presents its motivations with respect to the recent and future technical evolution of the electrical grids. Furthermore, it introduces the Modular Multilevel Converter family as a very attractive solution to these various challenges and describes its main characteristics, applications and benefits.

1.1 THE EVOLUTION OF THE ELECTRICAL GRIDS

1.1.1 THE GREEN INCENTIVES

Recently, with the forecasted shortage of traditional fossil energy sources, an increasing sensitivity to the ecological cause is emerging. This results in an growing will and need to reduce the ecological footprint related to the production and consumption of energy. In this context, the recent events in Fukushima during winter 2011 have reinforced some opinions and many countries have resolved to phase out nuclear power generation, such as Germany until 2022 and Switzerland until 2034. Technically, in the case of Switzerland, this corresponds to 3.2 GW of capacity to find in another form, while solving the related economical and sociopolitical concerns.

Fig. 1 illustrates the recent evolution of the worldwide nuclear-based electricity production, which is opposed to the total electricity consumption depicted in Fig. 2:

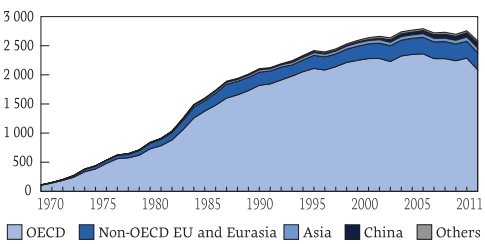


Fig. 1. Worldwide nuclear-based electricity production by region (TWh). Source: IEA [1].

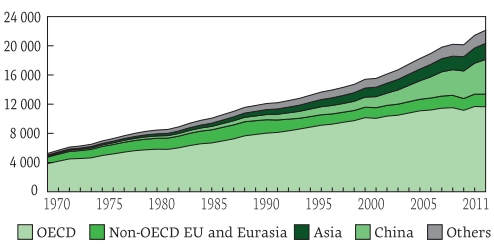


Fig. 2. Total worldwide electricity consumption by region (TWh). Source: IEA [1].

Obviously, the adequacy between production and consumption is becoming increasingly difficult to guarantee. Moreover, it is rather unlikely that opportunities to save energy will generate changes that cannot only slow down the increase of the energy consumption, but also induce an actual reduction of the latter by several tens of percents. Therefore, the development of substitutive solutions in order to replace these unwanted resources with cleaner alternatives seems indispensable and of utmost importance.

However, such a transition represents a formidable challenge. As an example, a simple calculation reveals that reaching the objective of producing 20% of the Swiss electricity from renewable energy sources (RES) by the end of 2020[1] requires to replace about half of the present nuclear-based generation by cleaner resources. Besides, in terms of capacity, this represents no less than 10 GW of capacity to be installed.[2,3] This corresponds to more than 10'000 wind turbines of 1 MW each or 50-100 km^2 of PV panels of 100-200 W/m^2 (a surface equivalent to the city of Paris or the entire lake of Zürich).

This urging need for quite a revolution explains that numerous incentives are already supporting the implementation of a more widespread use of renewable ressources. In turn, some significant changes are already in progress : according to Bloomberg Energy Finance cited in [2], the worldwide investment in new RES-based capacity in 2012 was 244 billion dollars, what contributed to double the corresponding capacity since 2000. Among the latter, the wind-powered capacity increased by a factor of nearly 16 while solar-based electricity production was multiplied by 49 [3].

As a result of such efforts, and even if the corresponding changes probably require quite some time, it is undeniable that the share of renewables in the mix of electricity production is deemed to increase. This is particularly true for the *new* –and non-dispatchable– renewables such as wind and sun, simply because mountains and water are not ubiquitous!

1.1.2 THE DECENTRALIZATION OF THE PRODUCTION

A general trend induced by the increasing penetration of the *new* renewables is the decentralization of the energy production, which mixes with the places of consumption and directly enters distribution networks. This is generally associated to the concept of *distributed generation* (DG), which is precisely characterized by the coexistence of producers and consumers in the local and regional electricity grids.

This so far unusual cohabitation as well as an increased number of decentralized actors result in a growing need for improved coordination mechanisms, from both technical and managerial perspectives. The term *smart-grid* often appears in this context, referring to the additional information technology (IT), measurement and communication means taking place between these various actors.

Furthermore, apart from the coordination issues, another key element related to the distributed generation is the difficult storage of energy, which aims to mitigate the effects of the non-predictability and non-dispatchability of the production and the consumption and thus to help guaranteeing the necessary balance between demand and offer at all times. In practice, the current situation still requires considerable effort :

– On the production side, the use of non-dispatchable RES currently results in a largely sub-optimal situation : the capacity factor of wind-powered electricity generation in Europe between 2003 and 2007 was only 20-25% [4]. For solar-based generation, capacity factors are usually even lower, typically around 10 %.
– Conversely, on the consumption side, the mitigation of the load variations is also a key concept, often referred to as *demand-side load management*. Here again, many

1. This corresponds to achieving the 20/20/20 objectives of the European Union.
2. Assuming a capacity factor of 15% (ratio of yearly average output power over rated power).
3. Currently, the share of non-hydro renewables in the Swiss electricity production in 2012 was 3% (1.9% of biomass and 1.1% of wind and solar) Source: SFOE / OFEN.

applications of energy storage have been foreseen in order to improve the overall load factors, but only few of them have been extended beyond the pilot stage yet.

That said, experts seem to agree on the fact that, where the electrical grids are well established and stable, the integration of non-dispatchable resources is most generally achievable as of today without a massive use of energy storage [5], [6]. Besides, the economical profitability of the latter remains highly dependent on regulations and subsidies, which are subject to significant changes and improvements.

Nevertheless, for the higher penetration ratios that will be necessary in order to fully cease nuclear power generation, energy storage will sooner or later become indispensable, either on the production or the consumption side, or more likely on both. Hence, an increased need for flexibility and controllability will most certainly take place in the grids that will be most affected by these changes, i.e. the distribution grids. Consequently, it can reasonably be expected that electrical energy storage systems will be subject to a continuously increasing interest, above all when used in association with modern power electronic systems.

1.1.3 THE CASE OF THE RAILWAY GRIDS

The electrical networks that are responsible for supplying energy to the railways are an interesting particular case because some of them are already facing today most of the technical challenges that are only foreseen in the medium-term in 50 Hz distribution grids. They are thus called to be somehow the witnesses and precursors of the energy turnaround, and this for several reasons :

- Some of them are employing a specific frequency of 16.7 Hz, one third of 50 Hz (among others : Switzerland, Germany, Austria, Sweden, Norway). This feature is a historical legacy [7] and implies that the entire chain of production–transport–consumption is made through electrical networks that are essentially independent from the European 50 Hz energy grid. This relative seclusion is giving rise to a rather limited security of supply, what is already setting these networks in critical situations in case of defective elements along the energy supply chain.[4]
- Most railway grids are sharing several common characteristics with 50 Hz medium-voltage distribution networks, such as *i)* demanding load profiles, *ii)* relatively low load factors and *iii)* relatively high line impedances.
- Finally, but unlike 50 Hz medium-voltage networks, railway grids are already penetrated by a high number of actors that are capable of both producing and consuming energy – the trains themselves ! – hence constituting an already complex distributed generation problem.

Additionally, the importance of all these characteristics and issues is exacerbated by the fact that these networks are expected to undergo a significant load increase within the next few years : the Swiss federal railways (SBB) are forecasting a 50 % load increase until 2020, while the SNCF is anticipating a 18% increase in the same period in the Paris area.[5] Last but not least, since most of the consumption is due to traction-related requirements, opportunities for energy savings are relatively limited.

4. Exemplarily, a fire accident in the Simplon tunnel in 2011 reduced by 50 % the supply capacity on its south side, which bears one of the steepest and most heavily loaded ramp of the Alps. This forced SBB to quickly set-up a 12 MVar voltage support system using two locomotives parked on a service line in order to restore the full transport capacity of the line [8].
5. Sources: SBB, SNCF.

This particular context is exemplified below by the case of Switzerland, where two relatively independent networks are present on the same area:

– The 50 Hz transmission and distribution grid (Fig. 3), operated by *SwissGrid* and local utilities and interconnected with the European ENTSOE grid.
– The 16.7 Hz grid (Fig. 4) owned and operated by the *Swiss federal railways (SBB)* and powered by a mix of autonomous generation and network interties (see Fig. 5).

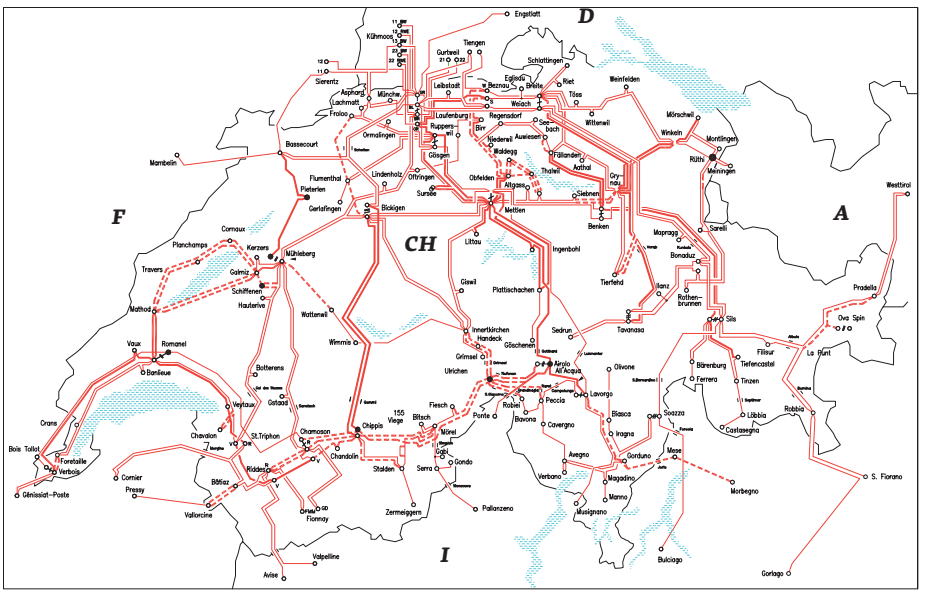


Fig. 3. Swiss 50 Hz network. Bold lines are those being upgraded to 380 kV. Source: SFOE 2008 [6].

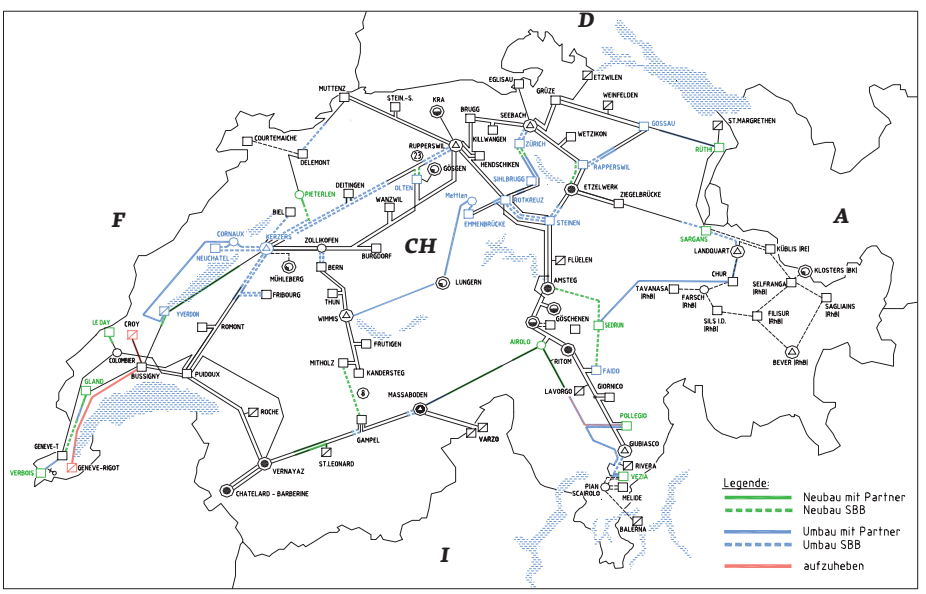


Fig. 4. Swiss 16.7 Hz railway supply grid operated by SBB. Source: SFOE 2008 [6].

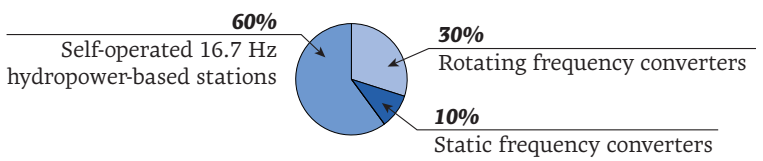


Fig. 5. Production capacity mix of SBB in 2012 for a total installed of about 1 GW. Source: SBB.

Owing to this situation, the improvement of the supply capacity and flexibility appears as essential. However, it seems extremely difficult to significantly increase the existing autonomous production capacity due to the limited amount of clean resources as well as sociopolitical and ecological concerns. Besides, the procurement and maintenance of 16.7 Hz electrical machines seem to be no longer possible as it represents an excessively small market segment for the corresponding manufacturers [9]. Therefore, the interconnection with the 50 Hz grid appears as the only viable option, although it is only pushing the true problem of electricity production one step further.

In turn, despite the strategic advantage that was historically constituted by the vertical integration and independent operation of the entire energy supply chain in 16.7 Hz networks, various benefits can be expected from an increased (inter)dependency of these networks with respect to the ENTSOE energy grid :

– Increased "production" capacity for railway grid operators.
– Possible and *monetizable* mutual exchanges of ancillary services, such as :
  » *Control reserves.* Due to their harsh load profiles, railway grids require and possess relatively large amounts of control reserves. Their participation to the services market may be attractive from both user and producer perspectives.
  » *Security of supply.* Both networks would surely benefit from an improvement.
  » *Blackstart capability.* This capability would be particularly useful in case part of the railway network is accidentally islanded.
  » *T&D capacity.* The relatively low network usage of the railway grids could be used to extent the capacity of the 50 Hz grid.

Concretely, due to the disappearance of 16.7 Hz electrical machines, rotating frequency converters seem to be no longer an option [9], leaving static converters as the only feasible choice for the implementation of network interties. That said, the most recent technologies can not only provide the exact same set of services as rotating converters, but can also inherently provide additional *"advanced" ancillary services* that are potentially highly beneficial to the railway supply grids, as they can address specific weaknesses, some which will be presented below.

1.1.3.1 "ADVANCED" ANCILLARY SERVICES

Harmonic distortion and power quality concerns have been long known as causing significant trouble on railway networks [7], [9]-[11]. These perturbations are mainly related to the interaction between the locomotives' front-ends – which generate high amounts of harmonics – with the supply lines [10]. Besides, due to the movement of trains, the line impedance of the supply system is varying over time, giving rise to undesired resonances that are difficult to locate and prevent [10], [12]. Furthermore, these resonance issues are even worsened due to the closed-loop control algorithms present in the locomotives, which generally have a negative impact on the damping of these phenomena (as they induce a line-side input impedance whose real-axis value may be negative for some frequencies [11], [13]). Ultimately, all these effects may not only limit the power transferred to the locomotives (lower the RMS system voltage), but also potentially trip the protective features and lead to system shutdown [15].

As a matter of fact, it is fortunately possible to fight against these problems using appropriate designs for the locomotive front-ends. Modern designs such as [13]-[14], are indeed already going in that direction. However, with older rolling stock, this is

not always possible and additional stationary systems may be necessary, such as by implementing dedicated passive or active filters and STATCOMs.

Alternatively, such services can also be directly integrated in the static network interties, provided that the latter offer sufficient flexibility and performance. Interestingly, this leads to little additional costs compared to the case where the transfer of energy is the only provided service. Going further, provided that active power exchanges are enabled by some energy storage capability –and/or a network linkage– it becomes possible to further extend the available set of ancillary services as to include:

- *Voltage quality* applications such as harmonic filtering, active resonance damping, sags compensation, fault ride-trough capability, etc. are good examples of existing needs that are best fulfilled with some active power supply exchange capability.
- *UPS-like or emergency supply* applications may be attractive in special cases in order to facilitate the evacuation of a tunnel in case of accident or similar scenarios.
- *Load-leveling* or *peak-shaving* applications may be applicable in order to limit the load variations, provided that cost-competitive energy storage is available.[6]

Overall, these elements show that various needs are emerging in railway networks relatively to *distributed generation* concerns. These issues are all the more important that some of them are similar to those that can be expected to take place in 50 Hz distribution networks in a more or less near future.

Technically, ancillary services can meet most of these needs and can be, for instance, advantageously integrated directly in the network interties, whose further dissemination is made anyway necessary by the forecasted increase of load. Moreover, as mentioned above, such a combined approach may be taken even further, provided that the corresponding facilities can admit active power exchanges. That said, flexible and state-of-the-art converter technologies adapted to utility-scale applications are in any case necessary, what makes of Modular Multilevel Converters a naturally privileged candidate for the implementation of the corresponding facilities.

1.1.4 THE DREAM OF THE DC GRID(S)

Still in the context of the energy transition, another technology that is attracting a lot of attention is that of high voltage direct current (HVDC) transmission. Indeed, the latter has long been recognized as a very attractive solution for the long-distance aerial transmission of energy (> 800 km) or underground / subsea systems, which are often seen as key to the evolution of the electrical grid(s).

In particular, HVDC is an attractive solution in order to upgrade the capacity of existing transmission systems, which are relatively unlikely to evolve significantly anymore. In turn, using the same lines, pylons and insulation, an improvement of several tens of percent of the capacity can be achieved using HVDC instead of HVAC. Besides, the capacity upgrade may be as high as 350 % with limited changes on the pylons [16].

Furthermore, initiatives such as *Desertec* also rely on HVDC in order to build a "supergrid" that could help transporting energy from the solar-based production centers in the sunny areas of the North-African deserts up to the main areas of consumption – such as the largest European cities – and the hydropower-based energy storage facilities located in the mountain areas. Alternatively, medium and high voltage DC

6. A detailed case study will be presented in section 5.2.1.

systems have also been suggested as collection grids for wind or solar farms, or in urban areas [15]. That said, in any case, such perspectives undoubtedly imply major changes in the way the electrical grid(s) are operated and managed and are also setting tremendous technical and political challenges for the most ambitious projects.

Overall, as the transport of DC quantities inevitably relies on power electronics, flexible and scalable converter systems suited for very high power and high voltage applications are the *de facto* key technology enabling such perspectives, what is further extending the already wide range of applications of Modular Multilevel Converters already outlined in the previous paragraphs.

1.2 TECHNICAL TRENDS IN POWER ELECTRONICS

Historically, the use of power electronics in high voltage and high power applications has long been hampered by the limited blocking voltage of the semiconductor switches, in the order of few kilovolts.

This obstacle has first been overcome using series-connected thyristors and GTOs, as it is still typically used in high power load-commutated current source converters (CSCs). Besides, the possibility to synchronously operate IGCTs and IGBTs nowadays also allows the use of PWM-operated voltage-source converters (VSCs) in such applications, with numerous benefits over their current-source counterparts : *i)* reduced harmonic filters, *ii)* capability to freely adjust the amount of exchanged reactive power, *iii)* smaller ground footprint, *iv)* operability in weak grids (low short-circuit ratio) and *v)* autonomous startup (blackstart) [54].[7,8]

The alternative to the series connection of switches is the implementation of *multilevel converters*, which are distributing the blocking voltage among several sub-systems and are switching only one (or few) sub-voltages at once. In such a case, the synchronous operation of the switches becomes dispensable and multiple output voltage levels are obtained. This also results in several other characteristics, which are briefly outlined in the next section.

1.2.1 CONVENTIONAL MULTILEVEL TECHNOLOGIES

Multilevel converters are defined by the fact that the global blocking voltage is divided into several fractions that are typically clamped by capacitive elements. In such a case, the switched voltages are smaller, leading to an improved harmonic performance for the same actual switching frequency. The key benefits such as reduced filtering requirements and potentially better efficiency are however coming at the expense of a significant increase of the control complexity (the voltage sub-division must generally be actively controlled) as well as a possible reduction of the global reliability (unless compensated by redundancies).

Authors of [17] and [18] provide broad reviews of conventional and more novel multilevel topologies. That said, among all the presented research as well as more generally, it is relatively widely accepted that only few multilevel topologies are truly attractive from an industrial point of view. Among them, the most common ones are :

7. Additionally, the power flow can be reversed without inverting the polarity of the DC bus, enabling the implementation of multi-terminal DC systems.
8. Despite a higher vulnerability to DC short-circuit faults and a lower efficiency.

– *Neutral-point clamped (NPC) converters.* Introduced simultaneously by Baker [19] and Nabae et. al. [20], the NPC is the most well known and widespread multilevel topology. NPC converters offer very attractive performances with a limited complexity. Unfortunately, the number of levels is generally limited to N=3 due to a complex design (presence of non symmetrical elements) for a higher number of levels.
– *Floating capacitor converters.* Introduced by Meynard and Foch [21], this topology has attracted a lot of academic interest in the last two decades but reveals to be rather complex to balance and suffers from the same handicap as the NPC topology. A variant named S*tacked Multi-Cell (SMC)* has been proposed in [22], offering a reduced amount of embedded energy. However, this variant reveals to be excessively complex to operate in redundant conditions.
– *Cascaded H-bridges converters.* Proposed by Baker et. al. in 1974 [23], CHBs only attracted significant industrial interest in the mid 1990's (Peng and Lai [24], Hammond [25]) for motor drives and utility applications. However, despite the excellent modularity of their power electronic parts, the necessity to provide isolated supplies to the H-bridges is posing significant challenges to the transformer design, particularly when high insulation voltages are required.

  In case the H-bridges are not supplied on their DC sides, the operating principles are significantly changed. First discussed by Ainsworth et. al. [26] in 1998, this alternative approach has been used in pioneering utility-scale STATCOM applications in the early 2000's [27]. As a matter of fact, the latter variant may be considered today as a proper member of the Modular Multilevel Converter family, with whom it shares many features (see §1.3).

Fig. 6 shows one phase of each of the above-described topologies :

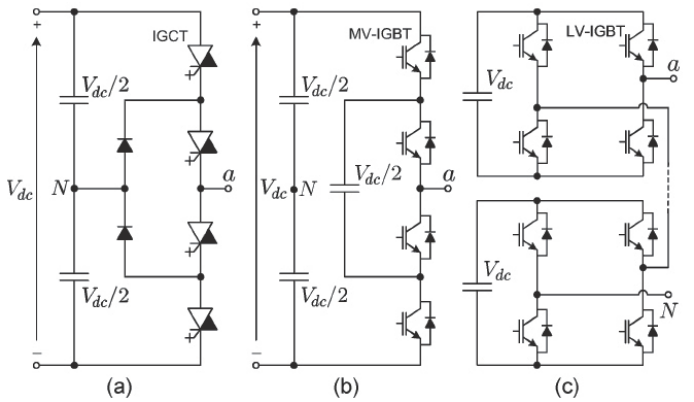


Fig. 6. Conventional multilevel converter topologies (with only one phase shown). *a)* 3L-NPC featuring IGCTs, *b)* 3L-FC featuring IGBTs, *c)* 5L-CHB featuring IGBTs. Source: [18].

1.2.2 CONVENTIONAL RAILWAY INTERTIES

Conventional static frequency conversion interties are generally similar to the structure depicted in Fig. 7. They make use of step-down transformers at both sides and interconnect several conventional (multilevel) converters through a double DC-bus. Besides, one of the key elements of this structure is the 16.7 Hz multi-winding transformer, which is not only complex, noisy and heavy, but also represents a quarter of the capital costs and a quarter of the losses [28].

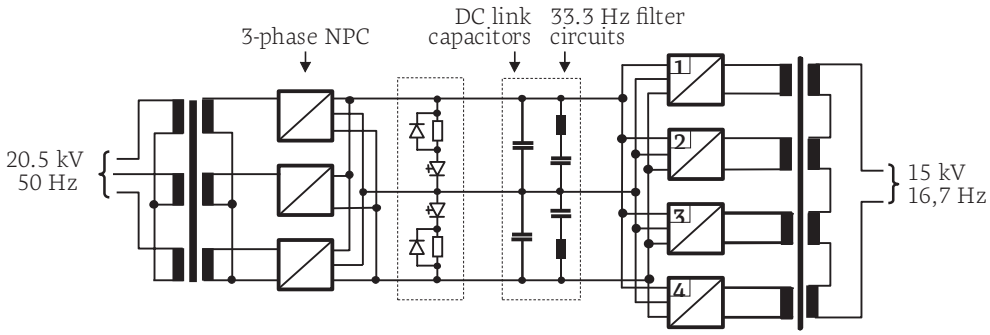


Fig. 7. Conventional frequency converter for the supply of 16.7 Hz railway systems. Source [28].

Owing to these facts, strong interests have emerged for solutions that can make the 16.7 Hz transformer dispensable.[9] That said, since in such a case the typical catenary voltage of 15 kV requires a DC-bus voltage in the order of 25-28 kV, a transformerless implementation is not possible unless series-connected switches are used or, alternatively, a Modular Multilevel Converter topology is employed.

1.3 THE MODULAR MULTILEVEL CONVERTER FAMILY

1.3.1 MOTIVATIONS AND BENEFITS

Modular Multilevel Converters (MMCs) constitute a technology whose authorship is generally attributed to R. Marquardt, relatively to a patent filed in 2001 [34] and publicly presented in 2002 [35].

From that moment, the use of MMCs was rapidly seen as attractive in a broad variety of applications, ranging from HVDC systems to variables-speed drives, but also including railway interties and advanced grid-tied applications. In all these cases, the presented motivations are related to the numerous benefits that this converter technology is offering over conventional multilevel converters. Indeed, as the number of produced voltage levels is generally high (tens to several hundreds), all the benefits of multilevel converters are exacerbated, with three fundamental advantages :

– The *excellent quality* of the produced waveforms makes the bulky and costly AC filters generally entirely dispensable.
– Owing to a strict modularity, MMCs possess a virtually infinite *scalability* (practically only limited by the achievable insulation voltage and the control complexity). This allows transformerless implementations at the medium and high voltage levels, such as in all the above-mentioned grid-tied applications.
– The actual average switching frequency per switching device can be very low compared to the overall apparent switching frequency, thereby greatly reducing the switching losses and improving the overall *converter efficiency*.

Besides, MMCs rely on a submodules-based *modular* design that offers significant additional benefits :

– The sinusoidal and continuous (i.e. non-chopped) nature of the arm currents authorizes the various arm elements to be interconnected with standard wire (without low-inductance busbars). This significantly eases the mechanical design and is the

9. A 50 Hz standard transformer is generally kept for galvanic insulation purposes.

key of the true scalability that other multilevel technologies are missing. Besides, the current commutation loops are confined inside the submodules with reduced *di/dt* and *du/dt*, what significantly improves the overall *EMI performance*.

– The numerous submodules offer natural redundancies that can be easily exploited in order to guarantee a *high reliability*.

Finally, as this work will further address, one of the key distinctive features of MMCs is that their internal power flows are made of low-frequency modulation products (products of sine functions). Compared to conventional technologies, this implies that relatively large amounts of embedded capacitive energy are required and calls for complex control techniques, but is also related to unique capabilities that other converter topologies are not able to provide.

1.3.2 CONVERTER TOPOLOGIES

The first member of the MMC family is generally considered to be that originally proposed by Marquardt in [34]-[35]. This family was quickly completed by a variant using voltage-reversible arms, introduced by the same research group in [36]-[38].

Today, although the exact extent of the MMC family remains somewhat vague [39], their common characteristics are now widely accepted as a *de facto* definition of the MMC family, that is: structures constituted by several arms, each of them being made of series-connected strictly identical cells (submodules), plus an inductor.[10]

Inside the arms, each submodule is constituted by an energy storage element, generally a capacitor, an elementary power conversion structure as well as the necessary gate drive, protection, measurements and power supply circuits. These submodules can be used to build various topologies, some of which are depicted in Fig. 8:

– *Double-star connected converters*, Fig. 8 *a)*. These structures were the first to be labeled as MMCs and correspond to those first described by Marquardt in [35]. Depending on the application, different types of submodules can be used:
  » Typically half-bridges[11] in case of *DC/AC conversion structures* such as three- or poly-phase inverters and rectifiers [34]-[36].
  » Typically H-bridges in case of *direct AC/AC conversion structures* such as from single-phase to single-phase conversion (Glinka, [37]) or single-phase to three-phase systems (Winkelnkemper, [72]).
– *STACOMs aka single-star or -delta connected converters*, Fig. 8 *b)* and *c)*. Since the voltage reversibility of the arms is compulsory in this case, these structures are based on H-bridges and are strictly identical to the previously existing cascaded H-bridges structures, without separate DC link supplies (§1.3.1).
– *Matrix converters (full or sparse matrices)*, Fig. 8 *d)* and *e)*. The main structure of Fig. 8 *d)* was originally suggested by Erickson et. al. in 2001 [40].[12] Alternatively, the sparse matrix converter of Fig. 8 *e)*, known as hexverter, was recently proposed by Barushka in [81]. The main applications of such topologies lie in direct multi-phase frequency conversion systems such as low- and variable speed drives [82].

10. The original schematics shown in [35]-[38] did not comprise any arm inductor. Nevertheless, it is yet widely accepted that these elements are highly beneficial to the converter design and operation and constitute a clearly distinctive feature of MMCs.
11. More complex structures may be used as well. This topic will be further detailed in §1.3.4.
12. Without arm inductors, which were introduced by Oates in 2011 [79].

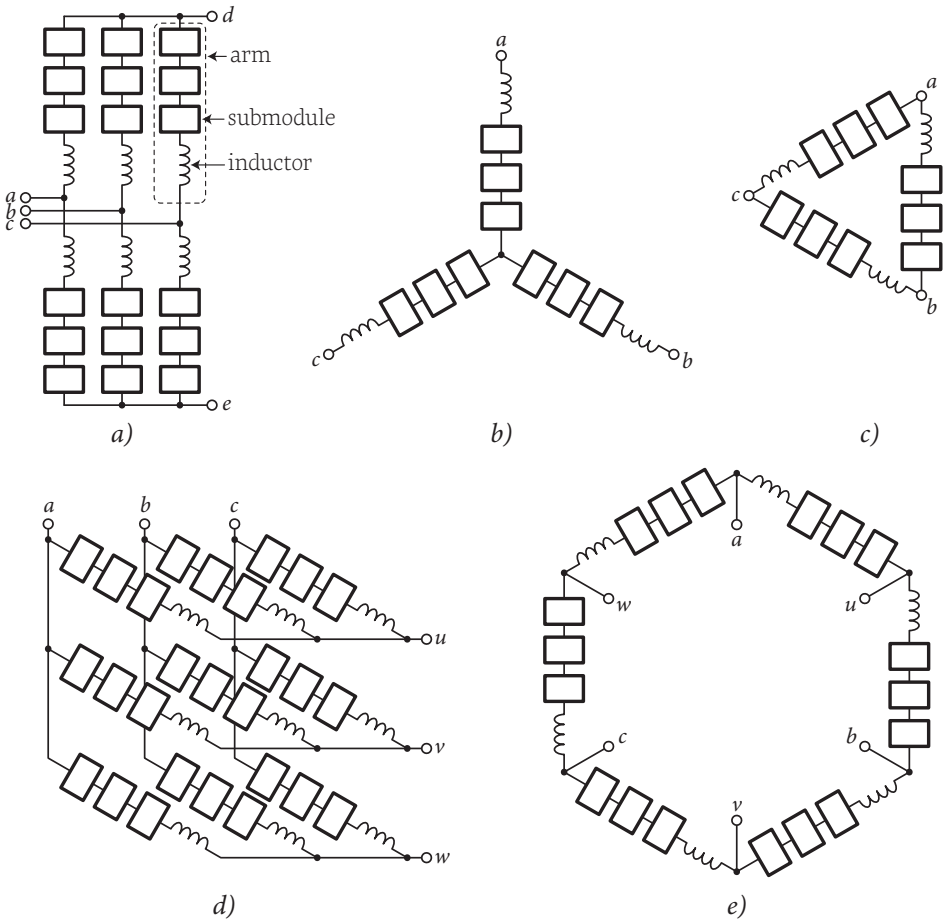


Fig. 8. Main Modular Multilevel Converter (MMC) topologies: *a)* 3-phase DC/AC or 1-phase to 3-phase direct AC/AC converter, *b)* 3-phase star-connected STATCOM, *c)* 3-phase delta-connected STATCOM, *d)* 3-phase full matrix converter and *e)* 3-phase sparse matrix converter (hexverter).

Additionally, compound or hybrid structures have also been developed, such as:

- The *Alternate-Arm Converter (AAC)*, Fig. 9 *a)*, developed by Alstom Grid [83], uses full-bridge submodules and implements additional soft-switched *director switches* in series with the arms in order to reduce the necessary number of cells and provide an excellent DC-fault blocking capability. Besides, the AAC distinguishes due to its bus-side behavior which is rather similar to a conventional VSC than a MMC, hence requiring some DC-bus capacitance for proper operation.
- MMC-based *DC/DC isolated structures*, Fig. 9 *b)*, with power electronic-based step-up/step-down have been proposed for use in DC collection grids (Kenzelmann et. al. [15], [84]). With such a topology, high step-up/step-down ratios can be offered with a simple 1:1 medium-frequency transformer that can be relatively small and simple.
- Targeting vehicular applications, the *Configurable MMC (CMMC)*, Fig. 10 *a)* proposed by Rufer et. al. [85] is making use of the two halves of the motor's stator windings as arm inductors and integrates the converter in a distributed manner inside the battery pack. Hence, AC and DC fast charging possibilities are provided without any hardware addition to the normal power train.
- Other topologies rely on additional converters in the submodules in order to add a third power port to the converters. Among several examples, the *Modular High-*

Frequency converter (MHF) in Fig. 9 *c)* uses additional DC/AC converters to directly supply the windings of a polyphase machine (Marquardt et. al. [86]). Alternatively, by adding split storage and aggregating the cells using DC/DC isolated converters, the *ultra-fast electric vehicle charging station* depicted in Fig. 10 *b)* can be directly tied to the medium-voltage grid (Rufer et. al. [87]).

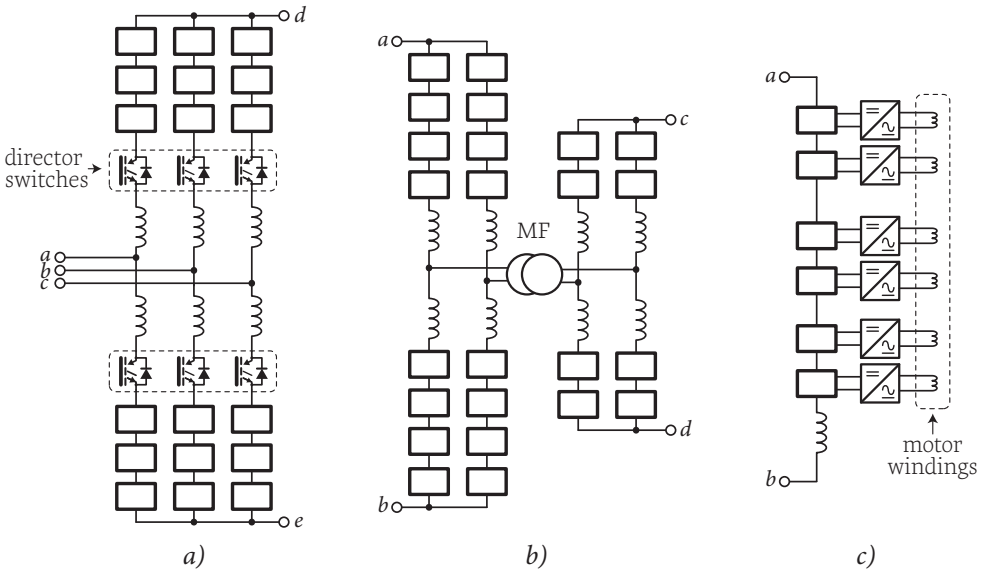


Fig. 9. Alternative Modular Multilevel Converter topologies: *a)* Alternate Arm Converter, *b)* Isolated DC/DC with power electronic-based step-up/down, *c)* Modular High-Frequency converter.

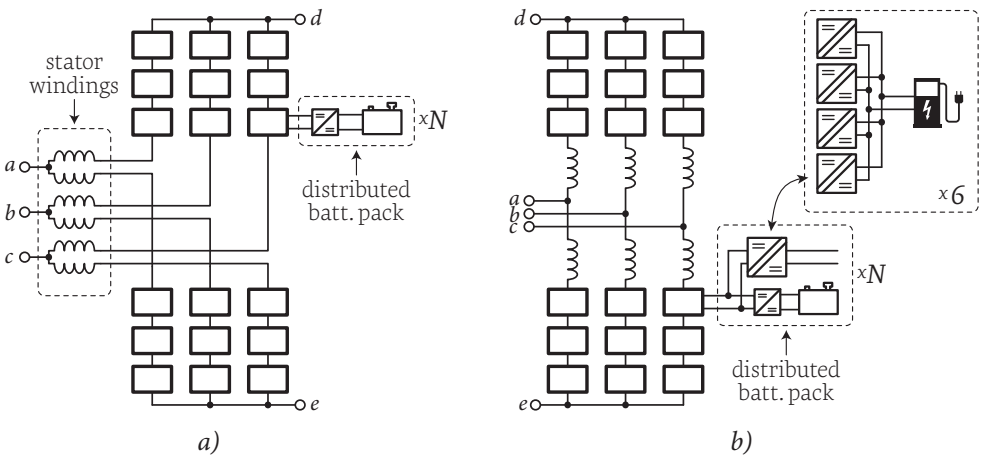


Fig. 10. Alternative Modular Multilevel Converter topologies: *a)* MMC for vehicular applications with integrated split storage and *b)* MMC-based ultra-fast electric vehicle charging station.

1.3.3 APPLICATIONS

Apart from their initial target applications related to HVDC systems, MMCs were early identified as an excellent solution for various other needs. In [54], engineers from Siemens already foreseen applications in *i)* HVDC cable transmission and back-to-back arrangements, *ii)* FACTS, such as STATCOM, *iii)* severely unbalanced networks, *iv)* large single-phase loads and *v)* multi-terminal HVDC systems. A slightly different classification is presented in the following paragraphs:

a) HVDC systems

The attractiveness of MMCs for HVDC applications lies in the fact that they possess all the benefits of VSCs while providing ratings and efficiencies similar to CSCs. This makes them the best technical choice in order to overcome the numerous challenges posed by the implementation of large-scale multi-terminal DC systems [58]-[60]. Indeed, unlike for back-to-back installations, the capability to control and reverse power flows by controlling currents, without change of polarity is absolutely crucial. Besides, the attractive DC-fault blocking capabilities inherent to MMCs are also constituting a key advantage compared to existing technologies [46], [83].

The first commercial HVDC-MMC facility was commissioned by Siemens in San-Francisco in November 2010 as a sub-sea ±200 kV DC link (400 MW / 85 km). Some information about the facility was first disclosed in 2007 [54], with more details given later in [55]. Variants from other companies are being implemented : Altsom Grid uses the Alternate Arm Converter of Fig. 10 *a)*, while ABB employs the so-called Cascaded Two-Level structure[13] under the name *HVDC Light Generation 4* [56]-[57]. Table 1 shows a list of some of the largest MMC-based HVDC projects worldwide.

Project	Supplier	Capacity	Project	Supplier	Capacity
BorWin2	*Siemens*	*800 MW*	*DolWin1*	*ABB*	*800 MW*
BorWin3	*Siemens*	*900 MW*	*DolWin2*	*ABB*	*924 MW*
HelWin1	*Siemens*	*576 MW*	*DolWin3*	*Alstom*	*900 MW*
HelWin2	*Siemens*	*690 MW*	*INELFE (E)/(F)*	*Siemens*	*2000 MW*
SylWin	*Siemens*	*864 MW*			

Table 1. Largest MMC-based HVDC facilities being implemented worldwide.

b) Frequency conversion applications

MMCs were also early considered for medium-voltage network linkage applications, using back-to-back (Marquardt, [35]) or direct conversion structures (Winkelnkemper, [72]). As for HVDC, Siemens turns out to be leading the way in this field, relying on its so-called *Sitras SFC+* technology, dedicated to railway supply applications. As of spring 2014, numerous projects of MMC-based network interties are already under progress, mostly attributed to Siemens. Fig. 11 shows a map of the latter projects :

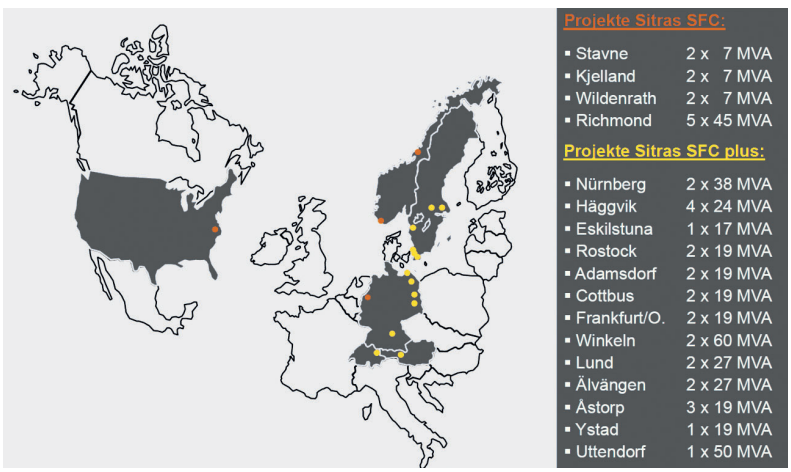


Fig. 11. Currently planned and under progress MMC-based frequency conversion facilities built by Siemens. Source: R. Gruber, ETG Fachtagungen, Spiez, August 2013.

13. The CTL is nothing else than a MMC with flipped submodules in the positive arms.

c) Motor drive applications

MMC-based low- and variable-speed motor drives have attracted a lot of academic and industrial interest in the past decade, particularly for applications in the medium-voltage range. First proposed simultaneously by Hagiwara et. al. [67] and engineers from Siemens [68], motor drive applications are particularly challenging at very low speed due to the difficult control of the phase power pulsation (see §3.2.2.2). As recently commented by Ilves [69], the matrix structures such as in Fig. 8 *d)* and *e)* are on numerous aspects particularly attractive choices for such applications. However, MMCs seem not to have entirely penetrated this market segment yet.[14] More detailed information about the state of the art of MMC-based drives can be found in [125].

d) Smart-grid applications

Finally, as already suggested earlier, the excellent flexibility and controllability of MMCs make them a perfect choice for grid-tied applications where the supply of ancillary services is required. This applies to all kinds of weak networks that are extensively penetrated by renewables and, more generally, all types of applications related to smart-grids. In [88], Bina et. al. suggested to use MMCs as STATCOMs, aiming to reactive power and unbalance compensation, voltage regulation and harmonic cancellation. Later on, Maharjan et. al. [189] introduced split energy storage inside the converter in order to provide load-leveling capabilities with a focus on renewables integration. To the best of the author's knowledge, no such system seems to be in commercial operation yet.

Overall, it can be seen that the high number of applications for which MMCs are well suited explains the high attractiveness of this technology with respect to high power and medium to very high voltage applications. This comment also shows why MMC is also often considered as one of the most promising technology in modern static power conversion applications.

1.3.4 SUBMODULES STRUCTURES

As illustrated in Fig. 8-Fig. 10, MMC topologies employ strictly identical submodules as the common building blocks to all these structures. Fig. 12 depicts some of the main cell circuits, which are described in the sequel :

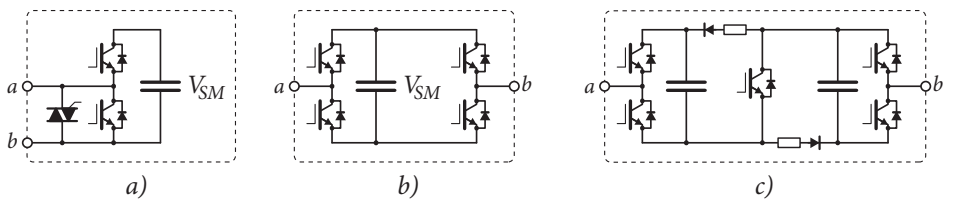


Fig. 12. Main submodule implementations: *a)* half-bridge, *b)* full-bridge, *c)* clamped double submodule.

a) Half-bridge submodules

This structure is the most evident choice for DC/AC applications, where only unipolar arm voltage are required. It is simultaneously the simplest option and the one that features the lowest conduction losses. However, the antiparallel diodes are creating an uncontrollable current path in case of a DC-bus short circuit fault, what leads to a unsatisfying behavior under such conditions, as for any other VSC topology.

14. Exemplarily, the SM-120 drive features a well-mastered NPC converter on its motor side [70].

In turn, this issue is all the more important that, with the emerging interest for multi-terminal DC grids, the existing fault-clearing method consisting in tripping the AC breakers becomes unacceptable as it implies de-energizing the entire grid [62]-[64]. DC circuits breakers would allow for the fast isolation of the faulty grid segment, but current state-of-the-art devices remain both expensive and lossy when compared to the converters themselves [65], [66]. As a matter of fact, with MMCs and appropriate cells structures, a high-voltage DC fault breaking capability can be directly embedded in the converters themselves, thus benefitting from the existing infrastructure so as to provide the necessary redundancy, HV-isolation, cooling, etc. without additional costs [46]. Hence, this opportunity is turning MMCs into one of the most appropriate technology for the implementation of multi-terminal DC systems.

b) Full-bridge submodules

Obviously, in applications that require bipolar arm voltages (such as direct AC/AC or matrix topologies), voltage-reversible submodules are necessarily employed, what constitutes the primary reason to use full-bridges.

That said, since full-bridges can actively break arm currents by imposing appropriate voltages in the arms, their use can be beneficial in unipolar applications as well, owing to the so-constituted DC short-circuit current breaking capability. However, the double number of power switches almost doubles the conduction losses [115], what seriously restrains their attractiveness for DC/AC applications and is the main motivation for the development of the clamped double submodules.

c) Clamped double submodules

This cell structure was proposed by Marquardt in 2010 [46] as a specific answer to DC short circuit protection issues. In fact, with an additional switch that can temporarily reconfigure two half-bridges as one full-bridge, the converter arms can impose counter-voltages up to half their nominal blocking voltage [83].[15] Besides, since the additional switch is not operated in normal conditions, it can be chosen such as to have good conduction characteristics and hence, contribute only marginally to the conduction losses (Modeer et. al. [115]).

d) Other submodule topologies

Alternative structures have also been presented, using either multilevel topologies (such as NPC or FC structures) or series series-connected switches [56]. Besides, the cross-connected cell circuit of [33] has been recently applied to MMCs in [49], offering similar performance as the clamped double submodule. A variant featuring some sort of parallel connection has also been recently proposed in [50].

1.3.5 MODULATION AND CELL BALANCING

The key issue relatively to the PWM or stair-case modulation of MMCs is the trade-off between switching losses, quality of the cell balancing and quality of the produced waveforms, while guaranteeing a simple and reliable implementation of the corresponding mechanisms. Most generally, among the existing cell-level balancing techniques, one can essentially distinguish two opposed paradigms :

15. According to Merlin et.al. [83], this voltage remains insufficient to fully control the fault current (unless more modules are employed), what is the main motivation presented by Alstom Grid to substantiate the development of the AAC topology.

a) Marquardt-type or sort-and-select-based modulation and balancing

In this case, after the desired arm voltage has been synthesized using a multilevel modulation approach (typically, such as proposed by Rohner [43]), the switching events are dynamically routed to the appropriate cells, depending on their charge level (Lesnicar, [35]). Consequently, the balancing is directly integrated within the modulation itself. Fig. 13 illustrates this principle of operation:

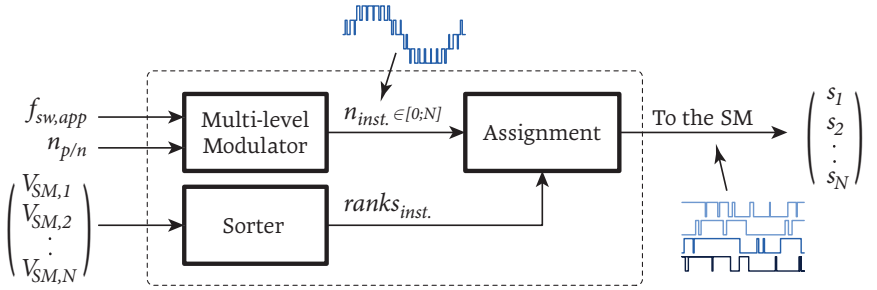


Fig. 13. Basic operating principle of the Marquardt-type (sort and select) modulation approach.

With such a technique, the main issue is to guarantee that no commutations are made without effectively contributing to the output voltage waveforms. Mathematically, this condition pushes (1) towards the equality:

$$f_{sw,\text{avg.}} \geq \frac{1}{N} f_{sw,app} \tag{1}$$

In turn, the equality of (1) can be easily enforced by operating only one cell at a time (in a given arm) and switching only when a actual change of level is required by the desired output voltage waveform. This hence guarantees that the result of the sorting algorithm is not introducing additional switching events – irrespectively of its refreshing rate – that cannot be "seen" on the output voltage.

Finally, it is worth noting that this approach is suited to produce both PWM-type or staircase voltage waveforms. Indeed, as first initiated and reported by [47]-[48], for a high number of submodules per arm, sufficient harmonic performance can be achieved with fundamental frequency switching approaches. The latter are also particularly attractive when the ratio between output frequency and carrier frequency is reduced (e.g. with drives), motivating a continuing research on this topic.

b) Akagi-type or multiple-carriers-based modulation and balancing

This second approach is inspired by the classical carrier-based modulation techniques previously used in CHB converters (Akagi, [42]). This approach is illustrated in Fig. 14:

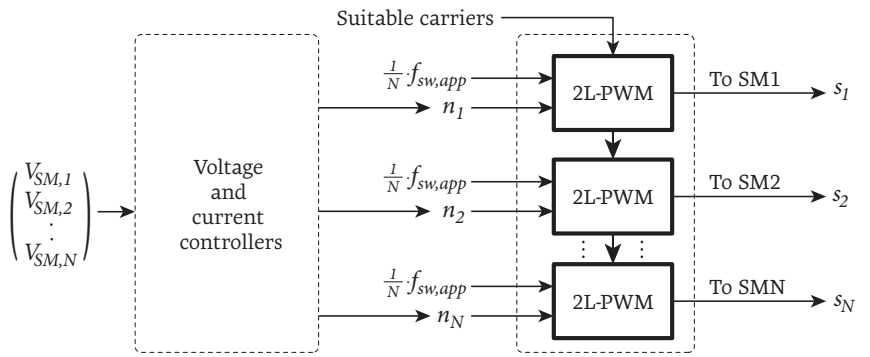


Fig. 14. Basic operating principle of the Akagi-type (distributed modulation) approach.

In this second case, N voltage references must be generated by a closed loop control mechanism (for the capacitor voltages) which ensures the balancing independently from the modulation. The main advantage over *Marquardt-type balancing* is that modulators can be implemented in a distributed manner, resulting in an easier control hardware paralleling (implementation of redundancies, distribution of computational burden, etc.). In this case, the main challenge is to properly synchronize the PWM carriers between the different submodules. This comment also holds when a submodule failure is detected and thus, the PWM patterns must be updated.

1.3.6 COMPONENTS SIZING

The overall dimensioning of MMCs may be considered as mostly defined by that of its passives. Indeed, the sizing of the switches being tightly bound to the shaping of the partial bus currents (see §3.2.1) and hence to the sizing of the submodule capacitors, both can be regarded as a unique problem, as presented below.

1.3.6.1 SUBMODULES CAPACITORS

The main degree of freedom in the sizing of the submodule capacitors is the choice of the related voltage ripple : more ripple allows for reduced embedded energy requirements but involves increased blocking voltages requirements and increased switching losses. Besides, the allowable voltage ripple is constrained by two extrema : the required AC voltage on the minimum side (including some margin) and the maximum operable voltage (limited by the silicon blocking voltage) on the maximum side. Generally, typical voltage ripples are chosen between 5-15%.

An analytical expression for the capacitor sizing has been published in the very first research results by Marquardt et. al. [35], [92]. However, this assumes plain DC partial bus currents (no circulating currents), what strongly limits its applicability. Alternatively, the detailed modeling of the capacitor voltage ripple developed by Vasiladiotis [126] or the frequency-domain approach of Norrga et. al. [105], can be used for sizing purposes as well. However, with respect to that particular objective, these methods are neither significantly faster no simpler than time-domain simulations.

Besides, more empirical and pragmatic approaches can also provide satisfying results. In [56], Jacobson et. al. mention that about 30-40 kJ/MVA of embedded energy corresponds to a good rule of thumb. Besides, Vasiladiotis et. al. have shown in [140] that, provided that the operation under strong grid asymmetries must be made possible, sizings cannot be significantly optimized through second-order harmonic injection or similar techniques. This latter result is illustrated by Fig. 15 :

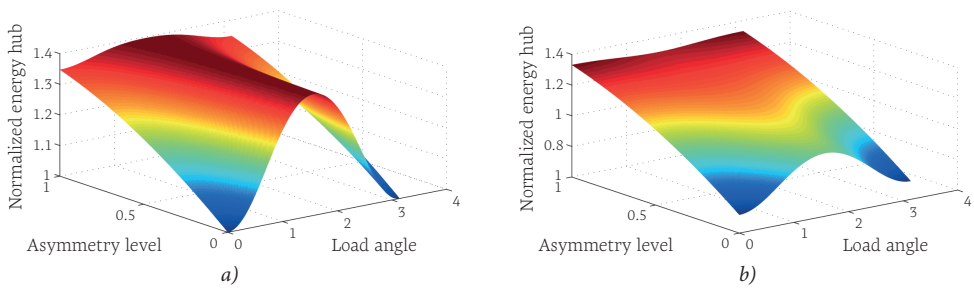


Fig. 15. Arm energy variation (proportional to squared voltage ripple) as a function of the current angle and the asymmetry level (0: no asymmetry, 1: full phase loss) when symmetric line currents are enforced: *a)* without 2nd harmonic injection and *b)* with 2nd harmonic injection. Source: [140].

1.3.6.2 ARM INDUCTORS SIZING

Surprisingly, despite the fact that the arm inductors are key elements of the MMC structures, their design seems to have received little attention from the academic domain. This is all the more remarkable that their *function* has partly evolved over time and may be subject of numerous discussions. Indeed, if at first no inductor was purposely added to the converter arms, these elements were quickly introduced in order to help absorbing the slight voltage differences that are due to the swapping of submodules with different charge-levels (e.g. Antonopoulos [90] and Mohammadi [109]). Typical values were in this case below 1 %. Later on, as reported by Allebrod [44] and Dorn [54], the role of the arm inductors was further identified as a combination of both protection and control purposes, leading to larger inductors, up to several tens of % p.u. Overall, it was recently observed in [112] that the employed values vary on several orders of magnitude for similar applications, what illustrates the absence of consensus with respect to both the function and the parameter design of these elements.

Besides, the *structure* of these inductors has not raised much attention either. For instance, the use of coupled inductors as introduced by Hagiwara et. al. [42] may be beneficial in terms of volume and weight for some design cases, but seems to be only rarely used. Furthermore, the use of non-coupled arm inductors allows to distribute the corresponding inductance among the submodules, what may significantly improve the strict modularity of the converter design, but this approach does not seem to have been much considered either.

Nevertheless, a few references are proposing some leads in order to size and design these elements. For instance, the work of Tu and Xu [111] was the first to address their sizing analytically. Two sizing criteria are proposed, corresponding to *i)* protective requirements as well as *ii)* the limitation of the voltage ripple on the submodule capacitors. Alternatively, Zygmanowski et.al. recall in [112] that the values of C_{SM} and L_{arm} potentially involve resonant frequencies close to the first line-frequency harmonics and therefore recommend to select inductor values so as to avoid these critical frequencies. That said, in both works, the proposed criteria are only applicable when the branch currents are not explicitly controlled, what dramatically reduces the scope of these approaches.

Among the design approaches applicable to more realistic operating conditions, Kolb and Kammerer proposed in [113] to size the arm inductors according to the switching ripple present on the line current. The authors provide an analytical formula depending to the chosen modulation pattern, but did not consider the ripple present on the corresponding partial bus current (corresponding to its own modulation pattern), nor any kind of control or protection criteria. Alternatively, Cherix attempted in [114] to provide a systematic framework in order to successively apply multiple criteria to each type of current involved in the converter's operation (line currents, total bus current and circulating currents). Practically, the author proposed to identify the RLC parameters of each of the corresponding current loops, which can be subsequently used to compute the current rise rate and/or maximum peak current value for different possible failures (submodule failure, line-to-line fault, DC short circuit fault, etc.), using a similar *protection criterion* as in [111]. Besides, a basic *control criterion* can be applied to each of these loops in order to guarantee the adequacy between the

control bandwidth and the time constants of the corresponding RL circuits. However, no *criteria* related to the *switching ripple* was presented, even though that of [113] could have been used in a straightforward manner. In the end, it is proposed to retain the most demanding values for each of the corresponding inductances, which can be subsequently implemented using a combination of line reactors, bus reactors and arm reactors.

1.4 MOTIVATIONS OF THE THESIS

1.4.1 INDUSTRIAL BACKGROUND

The research project surrounding this thesis aims to study the possible interactions between the 16.7 Hz Swiss railway grid and the 50 Hz grid. Three parts are considered:

- The possible use of rolling stock for reactive-power-based voltage support using reactive power injection. The main outcome is constituted by the work of Bahrani [30]-[31] which focuses on control techniques tailored for single-phase systems with time-variant parameters.
- Static converter usage for the supply of ancillary services to the railway network, which constitutes the specific context of the present work.
- The optimal allocation of ancillary services between the European 50 Hz grid and the 16.7 Hz grid. First results have already been published by Bozorg in [32].

Hence, the present work is substantiated by existing industrial interests for the supply of ancillary services to the railway network, as well as to the 50 Hz grid in case network interties are considered. This is why, one of the underlying objectives of the present work is to set-up a catalogue of solutions that are simultaneously applicable to single- and three-phase systems as well as the interconnection of the two latter. More specifically, various applications scenarios are taken into consideration:

a) Network interties

Already presented in §1.1.3, this scenario aims to improve the "supply capacity" of the railway grid. In this case, both the direct AC/AC and the back-to-back AC/DC/AC converter structures may be considered.[16] Besides, "transformerless" implementations are possible in the sense that the 16.7 Hz transformer can be avoided.

Theses applications are shown in Fig. 16, interfacing both grids at the transmission level, hence resulting in relatively large facilities (typically in the hundred MW range).

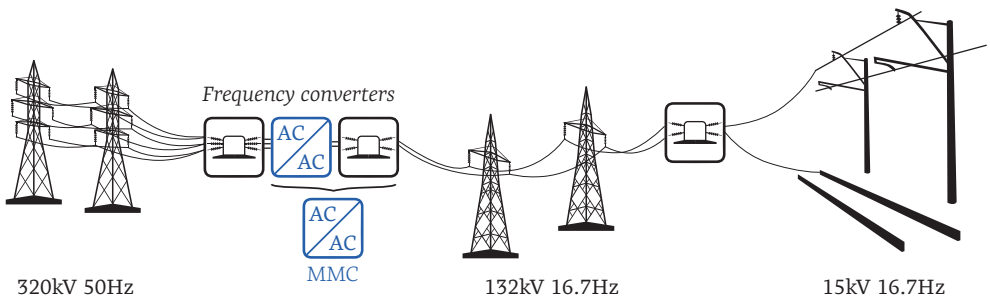


Fig. 16. Possible use of Modular Multilevel Converters in direct network interties.

16. That said, as mentioned by Winkelnkemper et.al. [72] and Gruber et.al. [71], the direct converter structure is likely to be preferable.

b) HVDC upgrade

In 16.7 Hz systems, as energy transport generally relies on two-phases lines, the latter are also ideally suited for bipolar HVDC transmission. A possible capacity upgrade scenario is shown in Fig. 17, using existing lines but based on DC current transmission. In some cases, transformerless converter implementations as possible as well.

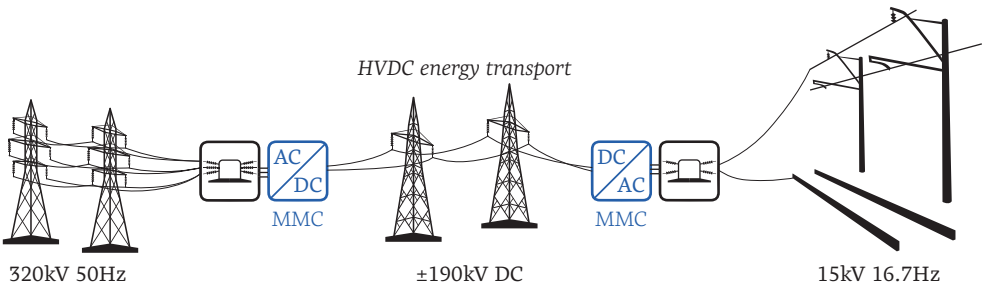


Fig. 17. Possible upgrade of two-phase 16.7Hz transmission lines to bipolar HVDC links.

c) Enhanced STATCOMs

Focusing on particularly weak points of the railway grid, an extended range of ancillary services can be provided by the newest static converters such as MMCs, especially if some energy storage capacity can be installed inside them. As illustrated by Fig. 18, such systems may be implemented at any network level, possibly using transformerless techniques as well :

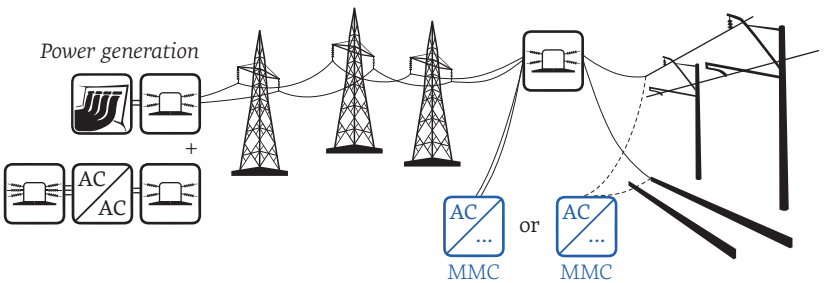


Fig. 18. Possible use of MMCs as STATCOMs (+possibly with energy storage) inside the railway grid.

Finally, although these applications are here described in a 16.7 Hz railway context, perspectives related to the supply of ancillary services can also be seen in 50 Hz single- and three-phase networks, in particular with respect to STATCOMs, network rebalancers, active filters, etc. which correspond to similar needs and may also benefit from an additional energy storage capability.

1.4.2 ACADEMIC BACKGROUND

Although barely older than a decade and still emerging on the industrial market, MMCs have rapidly benefited from a wide adoption among the academic community, resulting in an intense publishing activity, illustrated by Fig. 19.

On the downside of this success, the existing literature reveals to be rather exuberant, which is why, despite some very recent literature surveys [51]-[53], it is relatively uneasy to get the big picture out of the present knowledge. Furthermore, as recently commented by Kolb and Kammerer in [125], holistic approaches remain relatively scarce.

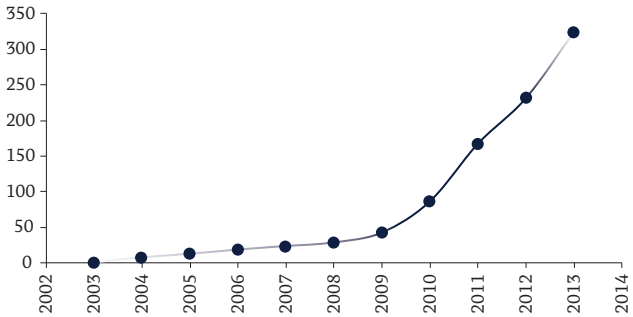


Fig. 19. Statistics of the number of search results available on the IEEE Xplore database containing the words "Modular Multilevel Converter" in the publication title.

Owing to these observations, there somehow exists some free room for contributions that attempt to introduce tools in order to take a step back with respect to the state of the art itself. Moreover, in the perspective to provide energy-related ancillary services from a MMC-based system, it can be noted that the topic of split energy storage has raised a clear academic interest, but has not been extensively studied. In particular, neither structural issues, nor energy-management-related issues haven been fully solved yet.

1.4.3 THESIS OBJECTIVES

As presented earlier, this work is motivated by a context which aims to improve the interconnection of the 16.7 Hz networks with the 50 Hz energy grid, as well as to provide energy-based ancillary services to both types of networks.

That said, being given the power and energy ratings at stake, it is possible to anticipate on the fact that such objectives involve major technical challenges that are reaching the limits of today's energy storage technologies. Hence, legitimate questions arise with respect to the feasibility of such applications : Where are the boundaries between feasible things and those that shall still be considered as aspirations ? How can realistic applications be identified ? Can something attractive be done by mixing two (or more) different types of energy storage technologies ?

Beyond these fundamental issues, another important and very concrete question also arises: assuming that such applications are realistic, how can the corresponding facilities be controlled and operated ? This issue is particularly relevant in case a Modular Multilevel Converter is coupled to a built-in storage, potentially involving mixed energy storage technologies. This thus represents an already complex topology, to which further control difficulties are added.

Consequently, in the perspective of the control design of such complex systems, it is necessary to first address some questions of methodology as to ensure to build on a sound basis and to take into account –as extensively as possible– the existing knowledge, shared among a dense literature. These observations are the main motivations encouraging the development of new tools, enabling to get some perspective on the state of the art itself. This postulates the use of strict formalisms and analysis tools that are as systematic as possible. Furthermore, a more "energetic" approach could have an interesting added value, particularly since the ultimate goal is precisely to manage energy exchanges between different sources and different energy storage technologies (hybridization).

In a second step, the objective is naturally to exploit the developed tools in order to provide some answers to the above questions as well as to help with the design of the corresponding facilities. Here again, the development of a systematic approach seems of high interest as it is expected to offer the necessary flexibility and reusability to apply the corresponding know-how to the numerous variants of systems considered in the presented industrial background.

Going further and ideally, the formalization of the control design of MMCs should also facilitate the modularization and the layerization of the "physical" control hierarchy, what is a true challenge with MMCs. Indeed, it would be desirable to be as flexible and modular with the control algorithmic as MMCs intrinsically are in terms of hardware (power and control). In other words, the flexibility of the power and control sections shall ideally not be undermined by a complex control design. Of course, the latter is inevitably tailored and application-specific, but could nevertheless be potentially modular and deductible in a systematical manner, thereby reinforcing the "universalizing" nature of MMCs.

Concretely, owing to these motivations, this thesis proposes to review the description and the control design of MMCs using so-called functional formalisms and especially the principles of the Energetic Macroscopic Representation (EMR) in order to:

- Highlight the basic principles of operation of MMCs as well as some of their intrinsic characteristics in a macroscopic and energy-oriented perspective.
- Provide tools in order to analyze and develop in a systematic and rational way the control of this family of converters. In particular, so-called model-based or inversion-based control design techniques are considered.
- Open various perspectives related to the design and control of MMCs with built-in energy storage, particularly in case multiple technologies are used.

1.5 SUMMARY AND THESIS OUTLINE

In the light of the emerging needs mentioned in the previous pages, Modular Multilevel Converters appear to be a key enabling technology, offering significant incremental benefits over previous technologies in fields of applications. In particular, this converter technology is very well suited to the supply of numerous ancillary services, what is of raising importance in railway networks.

As presented, owing to their relative seclusion from the 50 Hz grid and the already high proportion of regenerative loads, the latter networks are already facing most of the *distributed generation* issues that are only foreseen in the medium term in 50 Hz medium-voltage networks. Hence, these networks are to some extent today's witnesses of the changes and needs that are called to take place during the energy transition, especially in relation to the increasing penetration of renewables.

Owing to this context, this work focuses on grid-tied applications and on the supply of ancillary services. To that end, being given the large variety of the considered applications as well as the numerous scientific contributions that are already available, this thesis proposes to develop methodological tools aiming to enable a *more systemic* view of MMCs. Among other benefits that thesis will attempt to demonstrate, such tools enable to conduct the control design of such converters in a rigorous and systematical manner, hence facilitating its reuse.

The presented approach consists in reconsidering most of the modeling and representation effort of MMCs, even if it means re-addressing some proven prior knowledge. As it will be shown in Chapter 2, the passage to a functional approach brings a clear added value by offering several unusual but simple and insightful interpretations of MMCs' basic principles of operation.

Subsequently, in Chapter 3, the goal is to develop a methodology for the model-based control design of MMCs by making as much as possible abstraction of the existing literature. The aim is to be capable of assessing what was done by others in order to re-position the obtained results in the light of the state of the art. Finally, it will be attempted to identify prospective improvements.

Chapter 4 primarily aims to validate the presented developments by implementing the control schemes of Chapter 3 on a downscaled laboratory prototype. It also serves to highlight various issues related to the practical implementation of such converters, particularly with respect to the hierarchization of their control hardware and the implementation of the modulation techniques.

Finally, Chapter 5 discusses the integration of energy storage in MMCs as a future perspective to this work. Having highlighted some limits of feasibility in contexts as demanding as those posed by railway applications, this chapter will present how the functional and model-based approach can be used for the control design, especially in the perspective to embed hybrid energy storage technologies into these converters. As it will be shown, this opens interesting doors with respect to the future and necessary development of energy management strategies in such facilities.

2 FUNCTIONAL MODELING AND REPRESENTATION

Abstract – This chapter develops functional representations of Modular Multilevel Converters using the principles of the so-called Energetic Macroscopic Representation (EMR) as well as functionally equivalent schematics. These results aim to better highlight the inner converter dynamics in order to improve the understanding of the converter's intrinsic behavior. Besides, this approach is also expected to ease the assessment of existing control techniques and to provide means in order to deduce model-based control schemes, which will be specifically addressed later in Chapter 3.

2.1 BACKGROUND

Before describing the *model* that is used throughout this work as well as developing possible *representations*, this section briefly defines these two distinct concepts and introduces the so-called EMR formalism. Besides, section 2.2 will quickly review the challenges and the current state of the art of MMC's modeling and representation.

2.1.1 MODELING VERSUS REPRESENTATION

During the development of a plant and/or its control, some effort is always devoted to a relatively abstract analysis of its behavior, which may be generally be subdivided into several phases:

1) *Modeling:* A model is essentially defined by a *set of several assumptions* which aim to attribute known characteristics to some properties or to simplify the analysis of a system with an acceptable loss of fidelity. Moreover, the interactions between a system and its environment being often a central object of analysis, the modeling effort also aims to draw a clear line between the system and its environment, which is also subject to certain assumptions.
2) *Representation:* Often achieved intuitively and/or absorbed in the modeling effort, the representation effort aims to *organize a model and highlight its key elements* with respect to a given objective. A representation may be algebraic, graphical, numerical, etc. It is intended to illustrate functional characteristics (operating principle, transfer functions, energy flow), structural characteristics (hierarchical organization, mechanical layout) or abstract characteristics (states, etc.).
3) *Simulation:* This is an independent and dispensable step. It is often associated with additional assumptions related to the discretization or linearization of the model, depending on it operating points and main time constants.

Overall, modeling and representation are obviously inseparable. It is indeed very difficult to describe a model without a way to represent it and the establishment of any representation requires the existence of an underlying model. That said, multiple rep-

resentations of the same model are of course possible, provided that they are subject to the same set of assumptions.

Historically, various types of representations have been formalized through clear rules as well as standardized notations and representation techniques. Hence, for the same model, different representations may be more or less beneficial depending on the pursued objectives :

– Typically, the *state-space formalism* imposes clear rules to the algebraic representation of the studied system and leads to standardized mathematical descriptions that can be easily used for control design purposes.
– Alternatively, more graphical representations are obtained following the rules of *bond-graphs*, which are most useful in the study of multi-physical systems by setting the focus on the power flow paths between the various (sub)systems [152]-[154].
– A third example is given by *causal-ordering graphs,* which have been proposed in order to highlight the causality of the interactions between the various subsystems and deduce possible control schemes through a simple inversion of the relevant chains of causal relationships [155]-[157].

2.1.2 THE EMR FORMALISM

An alternative to these formalisms has emerged under the name of the Energetic Macroscopic Representation (EMR). The latter was first introduced by the automatic control group of the L2EP laboratory in Lille, France [158].[1] As suggested by its name, its purpose is mainly related to representation concerns, as opposed to modeling ones.

EMR has proved its attractiveness for the *control design* of complex or highly coupled electromechanical systems and has been successfully applied in research on wind turbines [159]-[160], advanced drives [161], hybrid electric vehicles [162]-[164] and railway-traction systems [165]. Practically, EMR relies on standardized graphical representations based on few symbolic elements, such as those represented in Fig. 20. These elements are then assembled using arrows, which describe their causal relationships.

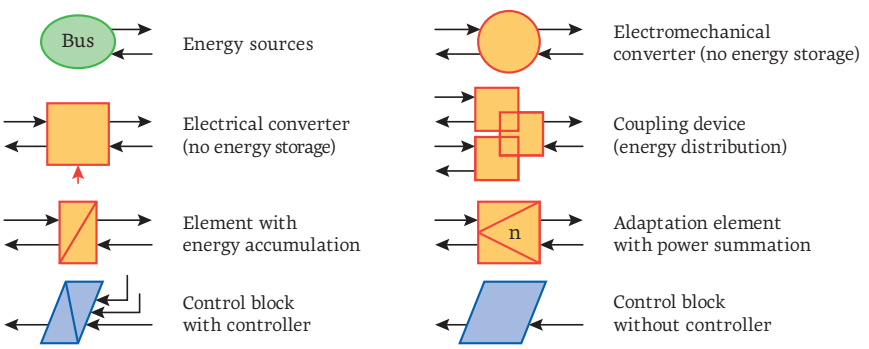


Fig. 20. Standard pictograms used in Energetic Macroscopic Representations.

The attractiveness of EMR is generally substantiated by the fact that it reuses some of the most attractive features of the above-described formalisms :

– Similarly to causal-ordering graphs and bond-graphs, EMR relies on the action-reaction principle and organizes the system as interconnected subsystems according to *causal relationships* [160]. However, EMR distinguishes by focusing on *power*

1. Now actively supported by a growing community. See http://www.emr-website.org

flows and highlighting the relations between the state variables from a *macroscopic point of view*, namely: exchanges of energy.

– Besides, EMR shares with causal-ordering graphs and state-space representations the fact that it is *invertible*, meaning that cascaded control schemes can be easily derived by following simple control design rules. This is all the more true that EMR is an essentially *visual formalism*, and is hence relatively intuitive.

Owing to these characteristics, EMR is particularly well suited to highlight the *functional behavior* of a given system. A typical example of this approach is given by the EMR of a parallel hybrid electric car and its corresponding inversion-based control scheme. The considered system is outlined in Fig. 21 while the obtained representation and control scheme are depicted in Fig. 22:

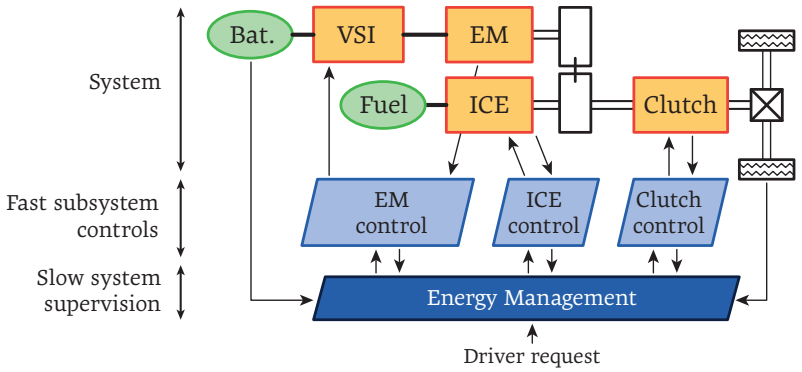


Fig. 21. Typical control structure of a parallel hybrid electric vehicle using an inversion-based control design approach relying on EMR. Original scheme: A. Bouscayrol, University of Lille.

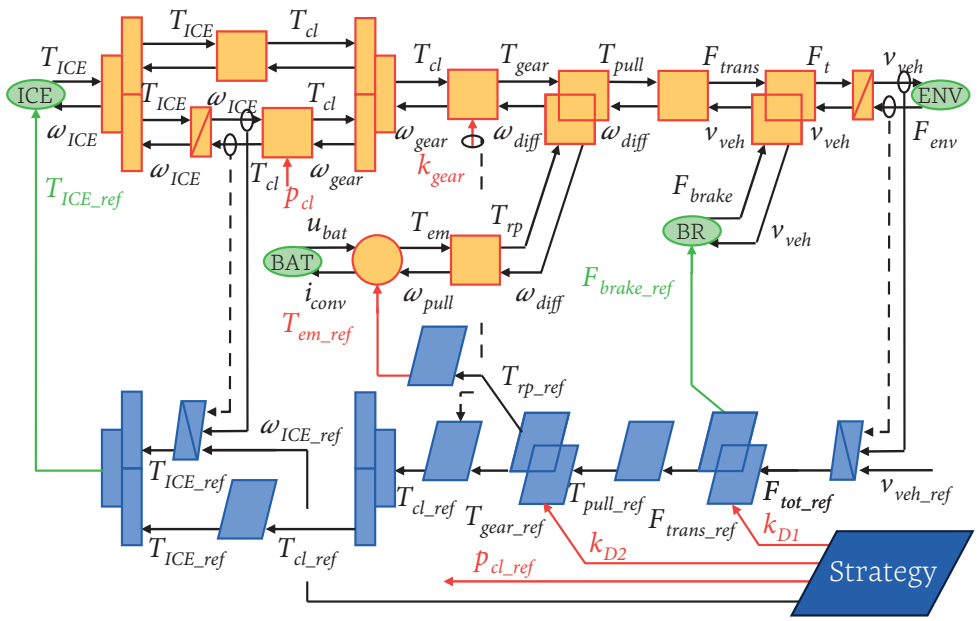


Fig. 22. EMR and inversion-based control scheme of the parallel hybrid electric vehicle of Fig. 21. Source and original scheme: W. Lhomme, University of Lille.

As can be seen from the figures, the causal relationships between the various subsystems are clearly highlighted by the action/reaction mechanisms shown by the arrows. Besides, the various power flow paths are made obvious as well, since the product of two adjacent arrows always results in the corresponding instantaneous power.

Thanks to these properties, the control of each subsystem (in blue) is easily obtained by a mirrored version of its representation (in orange) along the considered causal path(s). Furthermore, the local control loops are well separated from the strategy-level control block(s) which typically embed the energy management mechanisms (in dark blue).

Therefore, and more generally, the main benefits of EMR are certainly related to its high propensity to help developing and organizing a well layered and hierarchized control scheme. Indeed, as shown by the previous example, once the model is properly set and represented, the control loops can be easily identified and hierarchized. Besides, the remaining degree of freedom available for prospective optimizations are clearly highlighted and assigned to strategic and supervisory concerns.

2.1.3 PERSPECTIVES OF THE CHAPTER

Overall, thanks to its above-mentioned qualities and its successful use in the control design of complex systems, EMR can be expected to offer interesting benefits in the context of MMCs as well. Three main reasons are motivating this ascertainment :

- The understanding of the particular behavior of MMCs may be improved thanks to the increased focus set on the causality of the interactions between the subsystems.
- The control hierarchization / layerization shown in the literature may be yet considered as relatively difficult to apprehend on some particular points (and hence, clarified or even improved). Examples are :
  - » The "open-loop control scheme" proposed by Antonopoulos et. al. (see §3.2.1.1), where the roles of estimators, current controllers and voltage controllers are somehow joining and overlapping.
  - » The arm current and capacitor voltage shaping (see §3.2.1-3.2.2) objectives are generally mixing control implementation issues and energy management concerns (optimization of the amount of embedded energy).
  - » The comparative assessment of the various existing closed-loop capacitor voltage control strategies is made difficult by the fact that they depend on the utilized modulation method (see §3.2.2 and §4.2).
- The perspective to integrate energy storage inside the converters encourages the development of more macroscopic representation of the power flows in order to facilitate the future design of the energy management mechanisms.

Therefore, the main objective of the present chapter is to develop energetic macroscopic representations of MMCs as well as other functional representations that can offer some new and interesting interpretations of the basic principles operation of this converter family. Focusing on known topologies, these developments attempt to set up a rigorous and systematic method of analysis. Subsequently, by comparing these results with existing approaches, their attractiveness can be challenged, before being used in the following chapters in order to *i)* help the assessment of existing control techniques and *ii)* provide means to develop model-based control schemes.

2.2 STATE OF THE ART OF THE MODELING AND REPRESENTATION OF MMCS

Some modeling efforts and theoretical analysis can be found in almost every research on MMCs. On the other hand, the developed models can vary significantly depending on the pursued objectives, i.e. on the physical phenomena that are desired to be highlighted and on the required level of detail/granularity. Furthermore, the representations made of these models may also vary significantly. This section thereby briefly overviews the current state of the art of the modeling and representation of MMCs, as a function of the corresponding goals and usage.

2.2.1 KEY QUANTITIES AND DESIGNATIONS

As varying terminologies and definitions exist in the literature, Fig. 23 illustrates some of the main terms and designations used throughout this document. These definitions are here related to the DC/3-AC configuration, but also apply similarly to other topologies.

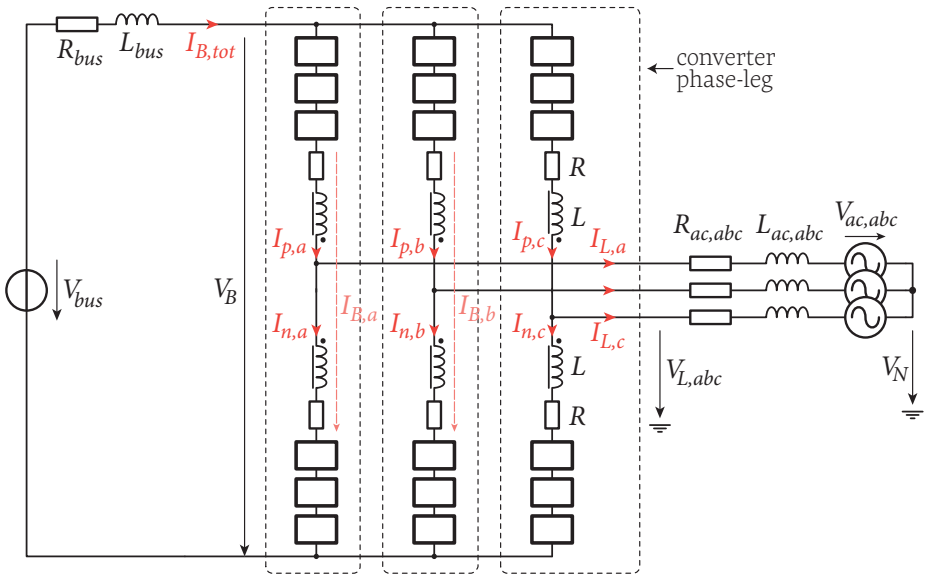


Fig. 23. Structural representation of a DC/3-AC or a direct 1-AC/3-AC converter.

In particular, the following conventions will be used with respect to the various currents components existing in these converter topologies:

- $I_{B,tot}$ denotes the *total bus current*. It is presumably constant in DC/AC systems or essentially sinusoidal in direct AC/AC systems (in which V_{bus} is sinusoidal as well).
- $I_{L,x}$ with x=*a,b,c* are the *line currents*.
- $I_{B,x}$ with x=*a,b,c* are the *partial bus currents* and are freely defined as:

$$I_{B,x}(t) = \tfrac{1}{2} I_{p,x}(t) + \tfrac{1}{2} I_{n,x}(t) \tag{2}$$

  As they correspond to the common-mode current between the positive and negative arms, they can be interpreted as flowing through the entire phase-legs and the bus-side. Besides, their sum corresponds to the total bus current $I_{B,tot}$.
- The differences between the $I_{B,x}$ are the *circulating currents*. They may be thus perceived as flowing in the loops formed between the phase-legs (hence their name!)

Furthermore, the following elements can be defined :

- L and M denote the arm self- and mutual- inductances, respectively. The sign of M defines the direction of the coupling (windings). In case the arm inductors are not coupled, M may be negligible.
- R denotes the average value of the arm resistance (see §2.2.3 *a)* on the next page).
- R_{ac} and L_{ac} are the parameters that model the line-side inductors (if present) or the transformer leakage inductance (if present). In any case, the voltage V_{ac} is assumed to be the point of common coupling and is considered as measurable. When applicable, the source V_{ac} may also embed a Thevenin-equivalent source impedance.
- R_{bus} and L_{bus} denote the impedance parameter that model the DC bus. Alternatively, in case of direct AC/AC conversion, these elements model the single-phase line-side parameters similarly to R_{ac} and L_{ac}. They may be of negligible values or intentionally implemented for protection and control purposes (see the Appendix). In any case, the voltage V_{bus} corresponds to the point of common coupling and is assumed to be measurable.

2.2.2 KEY PHENOMENA

Regarding the modeling of MMCs, most of the challenges are related to few key phenomena that are specific to this converter family and offer unique design or control optimization opportunities. Among them, particular attention has been given to :

a) Circulating currents

Regardless of their definition, it was early reported that these currents are related to additional degrees of freedom (in terms of both control and design), that do not exist in other topologies. Besides, the presence of arm inductors raised legitimate questions with respect to the understanding of this uncommon structure. Furthermore, opportunities of decoupled power control and sizing optimizations were reported in numerous publications, substantiating a need for suitable models and representations.

b) Capacitor voltage dynamics

During the normal operation of any type of MMC, some ripple is unavoidably present on the submodule capacitor voltages, with several low-order harmonics of the line frequency. As a matter of fact, since the presence of these harmonics is directly impacting both the control design and the dimensioning of MMCs, one of the key modeling objectives is to describe and analyze this particular phenomena.

Lesnicar [92], Antonopoulos [90] and Tu and Xu [119] first showed some of the main characteristics of this mechanism. However, and very generally in the first publications, aspects of causality have long remained relatively vague. This is particularly true with respect to the relationship between the arm currents and the capacitor voltages, whose interpretation sometimes forgets that the latter is essentially a consequence of the former (and not the other way around !). Anyway, the understanding of these mechanisms has not been achieved instantly, what justifies the modeling and representation efforts dedicated to this specific topic.

Furthermore, as reported Münch [94], the consideration of the capacitors voltages as part of the MMC control problem increases the number of independent state variables.[2] Simultaneously, Antonopoulos et. al. reported in [90] about the role of the par-

2. There are typically 5 currents and 6 voltages in the DC/3-AC configuration).

tial bus currents in the control of the arm energies, which are a direct image of these voltages. The authors also showed the possible action paths that can be used to control these quantities. Overall, a general consensus can nowadays be observed on the fact that all these quantities must be actively controlled, motivating modeling efforts in the direction of *control design* perspectives.

Finally, since the amplitude of these voltage oscillations is a key design parameter that directly impacts on the sizing of the submodule capacitors, interests have raised regarding the control of the *shape* –i.e. the harmonic content– of these oscillations in order to facilitate the development of optimized design and control techniques.

2.2.3 ASSUMPTIONS AND APPROXIMATIONS

Generally, the main assumptions related to the modeling of MMCs aim to simplify the arm behavior with an equivalent circuit. Several properties are addressed:

a) Equivalent arm resistance

Very commonly, as first suggested by Rohner [91], an equivalent arm resistance is introduced. The latter is intended to model all the resistive elements of the entire arm and generally encompasses all the parasitic resistances of the whole arm (wiring, contact and inductor). Additionally, this resistance may also model approximately the semiconductor conduction losses, as well as the average value of the total ESR of all capacitors. Importantly, although very common, this latter assumption is however only valid as long as the time-varying nature of the total ESR (the number of inserted cells does vary!) is not significantly affecting the arm resistance (Cherix, [104]).

b) Equivalent arm electromotive force (EMF)

Provided that all submodules are identical and behave identically, their capacitor voltages are expected to be almost identical as well. This hypothesis corresponds to assume that some mechanism is achieving a *sufficiently* accurate balancing of the voltages and produces *similar* PWM signals. This hypothesis is easily verified a posteriori, because it is a general requirement for the proper operation of MMCs. Accordingly, an equivalent arm electromotive force can be defined, such that equation (3) can be simplified into eq. (4) with an acceptable loss of accuracy:

$$E_{p/n}(t) = \sum_{k=1}^{N} m_k(t) \cdot V_{SM,k}(t) = \underbrace{\frac{1}{N}\sum_{k=1}^{N} m_k(t)}_{m_{arm,p/n}(t)} \cdot \underbrace{\sum_{k=1}^{N} V_{SM,k}(t)}_{V^{\Sigma}_{p/n}(t)} \tag{3}$$

$$E_{p/n}(t) = m_{arm,p/n}(t) \cdot V^{\Sigma}_{p/n}(t) \tag{4}$$

where $E_{p/n}(t)$ are the total electromotive force (EMF) generated by the positive or negative arm of submodules, $m_k(t)$ is the switching functions of the k-th submodule and $V_{SM,k}$ is the capacitor voltages of the same submodule.

Using this assumption, several equivalent arm circuits have been proposed, which are represented in Fig. 24 on the next page:

– The simplest solution, as in Fig. 24 *b)*, is to directly use the total arm EMF as a fictive and ideal voltage source (Lesnicar, [92]). However, this approach cannot account for the limited amount of embedded energy nor for the capacitor voltage dynamics, since the corresponding state variables are disregarded.

– Alternatively, Antonopoulos et. al. proposed in [90] a model that accounts for the finite amount of embedded energy. However, the presented scheme, shown in Fig. 24 *c)*, fails at separating the total arm EMFs from the capacitor voltage dynamics and hence does not entirely correspond to the developed mathematical model.
– Finally, the addition of the transconductive elements as in Fig. 24 *d)*, introduced by Ludois in [95] and recently improved in [96], allows for a clear separation of the two above-mentioned voltages without neglecting any state variable. A similar result is also obtained using a unique equivalent submodule as suggested by Rohner [99] and, since then, widely adopted.

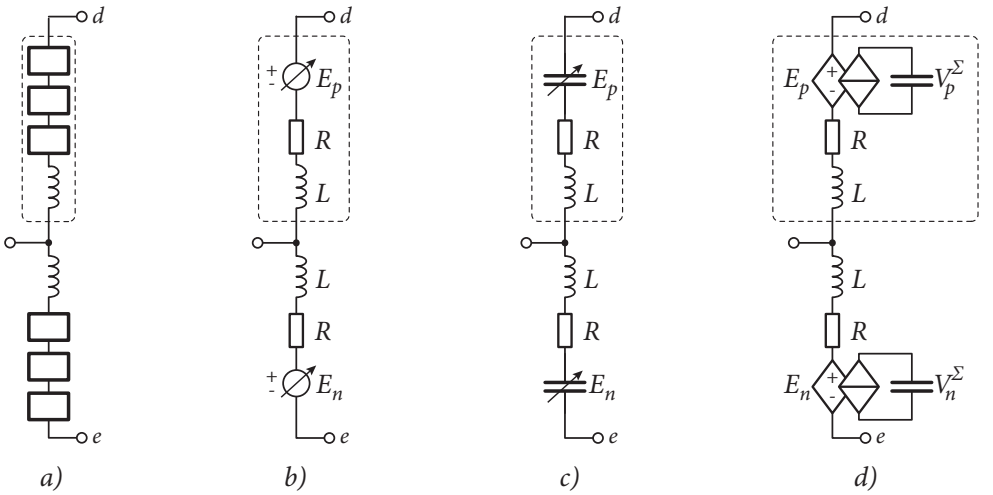


Fig. 24. Various phase-leg models corresponding to *a)* using an equivalent arm resistance as well as *b)* controllable voltage sources, *c)* variable capacitors and *d)* transconductive elements.

As first reported by Antonopoulos [90] and Münch [94], provided that the number of cells and/or the apparent switching frequency are *sufficiently high*, modulation-related effects may be neglected. Consequently, the term $m_{arm}(t)$ in eq. (3) becomes a smooth and essentially sinusoidal function. That said, it is worth noting that, despite its widespread use, this assumption is *not* required in order to develop any of the equivalent arm models in Fig. 24. Indeed, $m_{avg}(t)$ can obviously be defined such that it truly represents the multilevel PWM waveform of $E_p(t)$ and $E_n(t)$. Fig. 25 illustrates this concept, rather ignored in the literature:

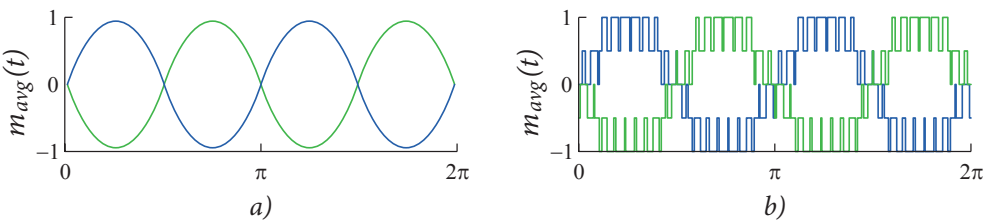


Fig. 25. Typical waveforms of the generated arm-level EMFs using *a)* switching-averaged modeling or *b)* an arm-equivalent PWM modulation.

Overall, when used along with the model of Fig. 24 *d)*, switching-averaged approaches are made very attractive due to their excellent computational speed and the accurate modeling of all low-order harmonics, owing to the consideration of every state variable. In addition, assuming that the equivalent arm EMF is modeled as in Fig. 25 *b)*, even the switching harmonics may be accounted for. In contrast, the individual behav-

ior of the submodules is unavoidably lost, making the analysis of the losses, internal faults and cell-level balancing issues impossible.

c) Alternative approaches

An interesting trade-off between structural switch-level models and arm-equivalent switching-averaged models has been introduced by Gnanarathna [97] and was further developed by engineers from Hydro-Québec [98]. In the reported works, Thevenin, respectively Norton equivalent sources are established, corresponding to each converter arm.

The main difference with the models deduced from an arm-equivalent switching function as in Fig. 24 is that the individual cell voltages are not disregarded. Using this approach, since all the internal nodes are removed from the nodal equation system, already significant improvements are provided in terms of computational complexity [97]. Besides, this method allows to account for the cell-balancing mechanism or internal faults and is well suited for the paralleling of tasks as required by Hardware-in-the-Loop (HIL) simulations [98].

2.2.4 REPRESENTATION TECHNIQUES

Regardless of the utilized representation formalism, the description of the inner converter quantities (circulating currents and summed capacitor voltages), is strongly influenced by the reference frame in which the currents and voltages are chosen to be decomposed and represented:

- Marquardt and Lesnicar proposed to view the arm currents as the superposition of a plain DC component and inner loop currents (circulating currents, *kreisströme* [92]), what is a choice also originally supported by Hiller [68].
- Akagi and his team chose to represent this phenomena using loops the partial bus currents [42] (see §2.2.1), except that the authors are referring to them as *circulating currents* (hence using a different definition of the latter).
- Münch [94] and Kolb [74] make use of the ***αβo*** and ***dqo*** reference frames in order to decompose both the arm currents and the summed capacitor voltages. This is identical to what was also proposed by Perez in [100]. Importantly, this only resembles Lesnicar's decomposition in case the sum of the partial bus currents is a plain DC value, what is not necessarily the case.
- Korn proposed in [124] to exploit basic properties of linear algebra in order to project the arm current in orthogonal vector spaces as to fully decouple inner- and outer-quantities, by construction. This lead to similar results as the ***αβo*** decomposition for the three-phase topologies.

In all these cases, these representations choices are essentially used in the context of mathematical descriptions. However, purely mathematical descriptions have their limits. Exemplarily, important efforts have been made to describe the inner converter dynamics in [90], [93] and [101]. However, no clear formalism is emerging and consequently, no clear methodology is able to help deducing control schemes from the equations, what requires both some intuition and expertise. Therefore, despite the high value of the presented analysis, such works are not best suited for understanding purposes and finally, not so appropriate for model-based control design either.

Alternatively, Münch et. al. [94] were first to use the state-space formalism to describe the behavior of MMCs, reused by Rohner in [99]. Their developments result in mathematical representations using ordinary differential equations. This relatively strict formalism benefits from well-known methodologies intended to develop model-based multivariable control schemes. However, this type of black-box representations is uneasy to interpret in the sense that it barely helps understanding the underlying physics.

Towards the latter purpose, the use equivalent schematic representations is a technique commonly used to ease the interpretation of any converter structure and its behavior. However, the development of such representations is not always trivial and usually also relies mostly on intuition and experience, with the risk that the obtained result is featuring a twisted view of the reality.[3] On that matter, innovative contributions were first reported by Zhao and Tang [103], who presented insightful equivalent schematics, reused later on by Norrga et. al. [105].

Alternatively, Cherix et. al. [106] first reported about the use of the EMR formalism in the context of MMCs and the presented work already contained partial results of the present thesis. More recently, EMR was also used by Delarue [106] and applied to three-phase inverter structures. However, since the developed representations are making use of a vectorial notation for the capacitor-related state variables, most of the arm-level balancing issues is masked, thereby preventing these representations from possessing a true added value for control design purposes.

Finally and regrettably, most of the existing graphical representations fail at highlighting the harmonic components present in the arm currents and capacitor voltages, what is nonetheless truly essential to the understanding of MMCs (see §2.6). Making a similar comment, Norrga et. al. [105] have introduced a frequency-domain modeling of MMC, that extended the work previously published in [101]. The authors iteratively combined the current, modulation indices and capacitor voltages in order to converge to a consistent description of all frequency components and showed that interesting strategies can be deduced in order to extend the converter's safe-operating area.

2.2.5 EXISTING USAGE AND PURPOSES

Very naturally, modeling and representation efforts are generally directly linked to the pursued objectives, which may be classified as:

a) Understanding purposes

Generally speaking, the way the operation of MMCs is perceived and understood seems to be rather a matter of representation than of modeling effort. Hence, equivalent functional representations such as in [103]-[106] are typically aiming for such perspectives, which are key to the analysis and control design of any system.

b) Simulation purposes

As reported by numerous authors, the simulation of MMCs requires unrealistic computation times if simplifying assumptions are not made at the modeling stage. However, provided that the cell balancing is out of the scope of interest, any of the arm-equivalent models presented in §2.2.3 provides an excellent trade-off between accuracy and computational speed.

3. Exemplarily, Fig. 24 *c)* is obviously inaccurate as the arm embedded energy amounts are not a direct image of the produced EMFs.

An interesting review is provided in [98], where the dynamic performance of the two variants of the arm-level EMFs of Fig. 25 are compared to several switch-level models, using non-ideal and non-ideal IGBTs as well as the approach from Gnanarathna [97]. The presented results show a satisfying agreement[4] of the arm-equivalent-based models with the switch-level models. Besides, with the approach of [97], a drastic reduction of the model complexity is observed, with a division of the corresponding simulation times (compared to structural simulations) by about 10-40x for the aggregated Thevenin sources of [97] and about 100-500x for the full switching-averaged models.

Such simplified models are particularly useful in large-scale or grid-level simulations where only the macroscopic behavior of the converter is relevant and computational speed is key. Besides, it also appears that simulation is thus generally not a very critical issue since a wide – and probably sufficient – range of granularity is already existing and can be tuned as a function of the objectives.

c) Control design purposes

Deducing a control diagram directly from the model using a systematic methodology is not a trivial thing. That said, as already mentioned, most authors seem to draw their implementation choices out of their understanding of the converter's basic principles of operation, supported by diverse mathematical developments. In this context, the works of Münch [120] and Korn [124] are worth being highlighted as they are the first examples of systematic control design approaches.

2.3 REFERENCE MMC MODEL

In the following, the employed MMC model is introduced. It relies on an arm-equivalent model and hence uses switching-averaged or PWM-type arm-level EMFs (see §2.2.3). Besides, a conventional and reasonable set of assumptions is employed:

- The equivalent serie resistance (ESR) of the submodule capacitors is neglected. Instead, an arm resistance is used, modeling the parasitic resistance of the inductor and all the contact and wiring resistances as well as the average value of the total ESR of the capacitors.[5]
- A suitable mechanism is assumed to be present in order to guarantee that the cell capacitor voltages are balanced around the same average value. Therefore, all cells are assumed to bear essentially identical behaviors.

These assumptions lead to the converter model illustrated in Fig. 26, which corresponds to a modified version of Fig. 23, accounting for these assumptions. Under the latter, as shown in Fig. 26, the cell strings of each arm are considered to be equivalent to a single fictive converter which relates a unique capacitor of voltage $V^{\Sigma}_{p/n}$[6] to the total arm electromotive force $E_{p/n}$. Thus, $E_p(t)$ and $E_n(t)$[7] are related to V^{Σ}_p and V^{Σ}_n by the modulation indices $m_p(t)$ and $m_n(t)$ such that:

$$E_p(t) = m_p(t) \cdot V^{\Sigma}_p(t) \qquad E_n(t) = m_n(t) \cdot V^{\Sigma}_n(t) \tag{5}$$

4. Apart from the reported DC fault case, which lacks the modeling of the arm inductors.
5. The validity limits of these assumptions are discussed in §2.2.3.
6. Hereafter referred to as summed capacitor voltages.
7. In Fig. 26 and throughout this work, subscripts p and n denote the positive and negative converter arms.

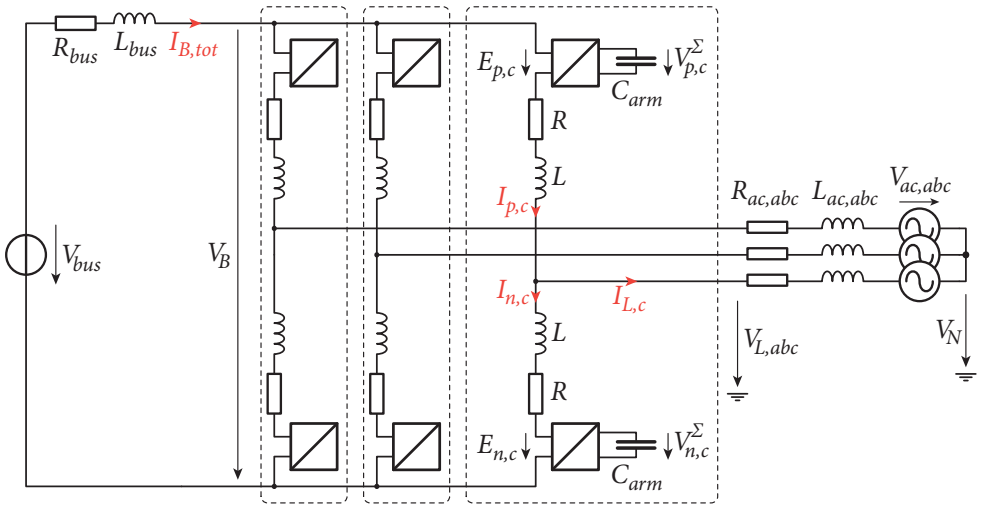


Fig. 26. Structural representation of a DC/3-AC or a direct 1-AC/3-AC converter.

It is important to note here that this model is simultaneously applicable to both DC/3-AC and 1-AC/3-AC configurations, owing to the fact that the only difference between them lies in the bipolar nature of the bus voltage (and hence in the voltage reversibility of the submodules). Indeed, even if the graphical representations are suggesting a DC/AC application, no assumption has been made regarding the actual nature of the voltages and currents. Exemplarily, the total bus current $I_{B,tot}$ is not necessarily a pure constant, but can be a pure AC quantity in case of direct AC/AC conversion. Hence, there is no loss of generality in the above-presented model, as long as it is admitted that V_B, I_B, V_{bus} and $I_{B,tot}$, can contain partially –or uniquely– alternating quantities.

2.4 FUNCTIONAL REPRESENTATIONS OF THE MMC PHASE-LEGS

This section aims to present two novel approaches in order to graphically illustrate the operation of MMCs, using EMR as well as equivalent schematics.

As a first step towards these objectives, the converter phase-legs are analyzed as an independent subsystem. This choice is motivated by the fact that it corresponds to the simplest structure that is common to all double-star-type MMC topologies[8] and features all the specificities of this converter family.[9] This subsystem is represented in Fig. 28 using a conventional schematic derived from Fig. 26. As illustrated, the boundaries of the considered system are modeled by two external voltage sources. Accordingly, with respect to EMR, this choice implies that the *to-be-deduced* representations desirably comply with the top-level concept of Fig. 27 :

Fig. 27. Toplevel "black-boxed" representation of a MMC phase-leg.

8. See §1.3.2 and reference [39] for more information about the employed classification.
9. The relevance of this choice will also be proven *a posteriori*, showing that MMCs are essentially single-phase converters.

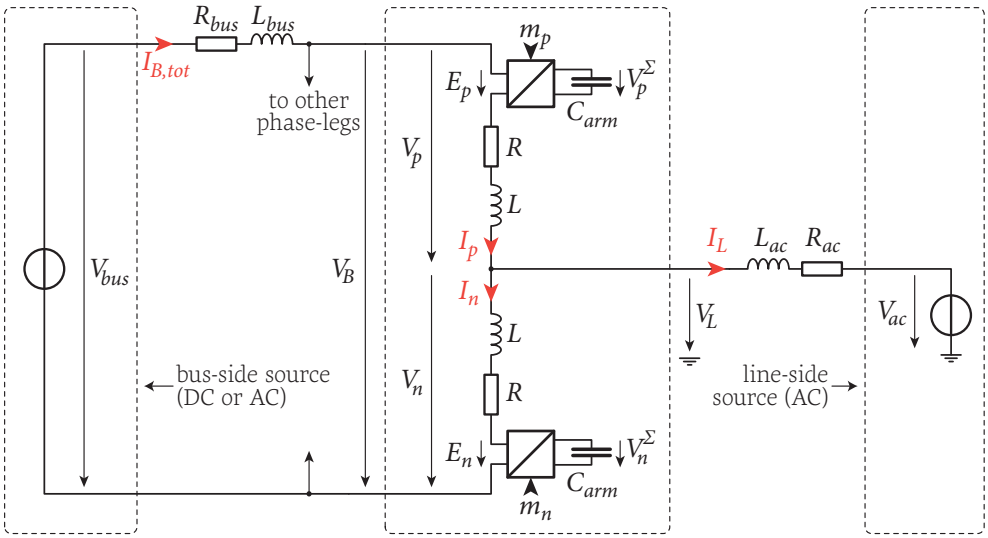


Fig. 28. Structural representation of the utilized model of the MMC phase-leg.

Hence, the respect of the action-reaction principle imposed by EMR [160]-[162] implies that each phase-leg must be considered as a current sources on both its sides, producing the currents I_L and I_B, to which the external sources are counter-acting by imposing the voltages V_{ac} and V_{bus}, respectively.

As a matter of fact, this perspective and representation objective is crucial, as it will impose several of mathematical manipulations shown in the following sections.

2.4.1 DIRECT REPRESENTATIONS

Analyzing the above model, the behavior of each phase-leg can be described by a set of ordinary differential equations. Indeed, by not neglecting the possible couplings between the arm inductors, the direct application of Kirchoff's voltage law results in:

$$\begin{pmatrix} V_p \\ V_n \end{pmatrix} = \begin{bmatrix} L & M \\ M & L \end{bmatrix} \begin{pmatrix} \dot{I}_p \\ \dot{I}_n \end{pmatrix} + \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{pmatrix} I_p \\ I_n \end{pmatrix} + \begin{pmatrix} E_p \\ E_n \end{pmatrix} \tag{6}$$

Subsequently, introducing the reduced values of (7):

$$L' = \left(L^2 - M^2\right)/L \qquad M' = \left(L^2 - M^2\right)/M \tag{7}$$

the dynamics of the positive and negative arm currents and summed capacitor voltages can be easily described, as shown in equations (8) and (9):

$$\begin{pmatrix} \dot{I}_p \\ \dot{I}_n \end{pmatrix} = -\begin{bmatrix} R/L' & -R/M' \\ -R/M' & R/L' \end{bmatrix} \begin{pmatrix} I_p \\ I_n \end{pmatrix} + \begin{bmatrix} 1/L' & -1/M' \\ -1/M' & 1/L' \end{bmatrix} \begin{pmatrix} V_p - E_p \\ V_n - E_n \end{pmatrix} \tag{8}$$

$$\begin{pmatrix} \dot{V}_p^{\Sigma} \\ \dot{V}_n^{\Sigma} \end{pmatrix} = \frac{1}{C_{arm}} \begin{bmatrix} m_p & 0 \\ 0 & m_n \end{bmatrix} \begin{pmatrix} I_p \\ I_n \end{pmatrix} \tag{9}$$

Besides, these dynamics are also related to the external sources through:

$$\begin{pmatrix} \dot{I}_L \\ \dot{I}_B \end{pmatrix} = -\begin{bmatrix} R_{ac}/L_{ac} & 0 \\ 0 & R_{bus}/L_{bus} \end{bmatrix} \begin{pmatrix} I_L \\ I_B \end{pmatrix} + \begin{bmatrix} 1/L_{ac} & 0 \\ 0 & -1/L_{bus} \end{bmatrix} \begin{pmatrix} V_L - V_{ac} \\ V_B - V_{bus} \end{pmatrix} \tag{10}$$

By doing so, equations (8)-(10) infer a system of six differential equations that are not independent. Indeed, the four currents are tightly related by Kirchoff's current law applied to the mid-point of the phase leg. Similar results and comments have also been reported in the literature, such as by Perez et. al. [100], Münch [94], [120] or Kolb and Kammerer [74], [80].

2.4.1.1 EMR OF THE CONVERTER ARMS

The above-presented model can be easily turned into a functional graphical representation of the converter arms using EMR. First, in order to illustrate the basic pinciples, the representations of the arms are developed with non-coupled inductors:

First, equations (8)-(9) reveal two types of state variables that physically correspond to two energy storage elements, namely the arm inductor L and the fictive capacitor C_{arm}. According to the principle of integral causality [160], their constitutive equations are directly derived from the model and described as in equation (11):

(11)
$$I_p = \frac{1}{sL+R}(V_p - E_p) \qquad V_p^{\Sigma} = \frac{1}{s \cdot C_{arm}} I_p$$

Subsequently, the EMR of each converter arm is easily derived as shown in Fig. 29. It also features an electrical conversion block corresponding to eq. (5). By doing so, the equivalent capacitor is represented as an energy tank whose voltage is influenced by the current that flows into it. Similarly, the arm inductor is producing a current which is influenced by the voltage across its terminals.

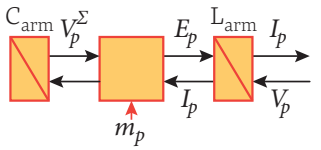


Fig. 29. EMR of a complete MMC arm (here: upper arm).

Represented as such, the underlying choice of action and reaction quantities implies that each converter arm is thereby considered as a current source, which is influenced by the voltage difference between V_p or V_n and the corresponding EMF. This latter interpretation resembles the one proposed by Oates in [45].

Finally, a simple application of Kirchoff's current and voltage laws then easily leads to the representation of the couplings at the mid-point of the phase-leg as in (12) and depicted in Fig. 30:

(12)
$$\begin{cases} V_p = -V_L + \frac{1}{2}V_B \\ V_n = V_L + \frac{1}{2}V_B \end{cases} \qquad \begin{cases} I_L = I_p - I_n \\ I_B = \frac{1}{2}I_p + \frac{1}{2}I_n \end{cases}$$

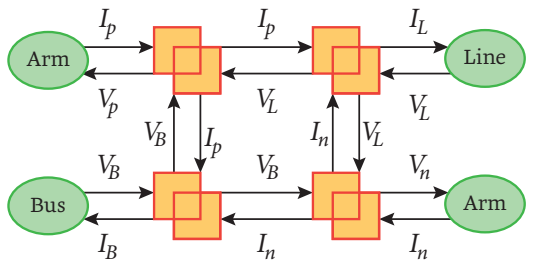


Fig. 30. EMR of the couplings at the inductive node. Each blocks represents an equation of (12).

Unfortunately, using this step-by-step approach, difficulties arise when the EMR is extended to the entire model. Indeed, the external inductors L_{bus} and L_{ac} cannot be included without inducing *conflicts of association*.[10] The same issue also occurs when the mutual inductances must be accounted for. This is illustrated in Fig. 31:

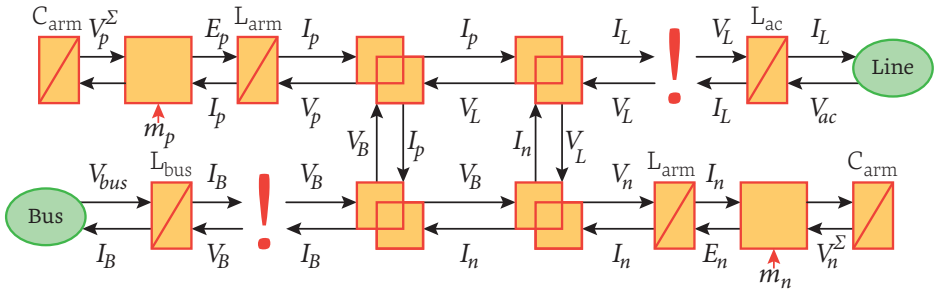


Fig. 31. Conflict of association appearing when it is attempted to include the subsystem representing the inductance of the external AC source.

In fact, in order to overcome these issues, distance must be taken from this approach. In the present case, the *conflicts of associations* simply reveal that these four currents cannot be represented as independent state variables. Therefore, additional mathematical developments are necessary before a satisfying EMR can be built. The latter are presented in the following section.

2.4.2 DECOUPLED REPRESENTATIONS, FIRST STEP

Assuming that the developed assumptions hold true (see §2.3), a simple change of coordinates (isomorphism) decomposing the two arm currents in *common-mode* and *differential-mode* terms highlights interesting properties. Indeed, introducing the $\mathbf{T}_1$ and $\mathbf{T}_2$ matrices such as in (13), the *common-mode* and *differential-mode* currents of I_p and I_n can be described in a decoupled manner shown in eq. (14).

$$\begin{pmatrix} V_L \\ V_B \end{pmatrix} = \mathbf{T}_1 \begin{pmatrix} V_p \\ V_n \end{pmatrix} = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2} \\ 1 & 1 \end{bmatrix} \begin{pmatrix} V_p \\ V_n \end{pmatrix} \qquad \begin{pmatrix} I_L \\ I_B \end{pmatrix} = \mathbf{T}_2 \begin{pmatrix} I_p \\ I_n \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{pmatrix} I_p \\ I_n \end{pmatrix} \tag{13}$$

This decomposition is particularly interesting since the transformed variables happen to possess a very useful physical meaning:

- The differential-mode current corresponds to the line current I_L, *by construction*, as it is the direct result of Kirchoff's current law applied at the mid-point of the phase-leg.
- The common-mode current corresponds to the partial bus current I_B, *by defintion* of the partial bus current.

With this approach, the dependent state variables of (8) and (10) are explicitly related, what results in a decoupled state space representation for the equivalent currents, represented in transformed coordinates. The resulting equations are given by (14):

$$\begin{pmatrix} \dot{I}_L \\ \dot{I}_B \end{pmatrix} = \begin{bmatrix} \frac{\frac{1}{2}R + R_{ac}}{\frac{1}{2}(L-M)+L_{ac}} & 0 \\ 0 & \frac{2R+R_{bus}}{2(L+M)+L_{bus}} \end{bmatrix} \begin{pmatrix} I_L \\ I_B \end{pmatrix} + \begin{bmatrix} \frac{-1}{\frac{1}{2}(L-M)+L_{ac}} & 0 \\ 0 & \frac{1}{2(L+M)+L_{bus}} \end{bmatrix} \begin{pmatrix} V_{ac} - E_L \\ V_{bus} - E_B \end{pmatrix} \tag{14}$$

10. This term refers to a specific meaning in the usual EMR-related terminology, meaning that two blocks cannot be connected as they share the same action and reaction quantities.

where the coordinate transformation defined by (13) has been used to introduce equivalent electromotive forces $E_L(t)$ and $E_B(t)$ as in:

$$\begin{pmatrix} E_L \\ E_B \end{pmatrix} = \mathbf{T}_1 \begin{pmatrix} E_p \\ E_n \end{pmatrix} \tag{15}$$

Additionally, (14) can be further simplified by also introducing equivalent line-side and bus-side impedances, such as in:

$$\begin{cases} L_B = 2(L+M) \\ L_L = \frac{1}{2}(L-M) \end{cases} \quad \begin{cases} L_{B,tot} = L_B + L_{bus} = 2(L+M) + L_{bus} \\ L_{L,tot} = L_L + L_{ac} = \frac{1}{2}(L-M) + L_{ac} \end{cases} \tag{16}$$

Hence, the complete description of the phase-leg dynamics is given by (17)-(18), featuring only linearly independent state variables and equivalent parameters :

$$\begin{pmatrix} \dot{I}_L \\ \dot{I}_B \end{pmatrix} = \begin{bmatrix} R_{L,tot}/L_{L,tot} & 0 \\ 0 & R_{B,tot}/L_{B,tot} \end{bmatrix} \begin{pmatrix} I_L \\ I_B \end{pmatrix} + \begin{bmatrix} -1/L_{L,tot} & 0 \\ 0 & 1/L_{B,tot} \end{bmatrix} \begin{pmatrix} V_{ac} - E_L \\ V_{bus} - E_B \end{pmatrix} \tag{17}$$

$$\begin{pmatrix} \dot{V}_p^{\Sigma} \\ \dot{V}_n^{\Sigma} \end{pmatrix} = \frac{1}{C_{arm}} \begin{bmatrix} \frac{1}{2}m_p & m_p \\ \frac{-1}{2}m_n & m_n \end{bmatrix} \begin{pmatrix} I_L \\ I_B \end{pmatrix} \tag{18}$$

Owing to the fact that both matrices of (17) contain only diagonal terms, these equations proves that I_B and I_L can be controlled in an independent manner by mastering the equivalent electromotive forces E_B and E_L, respectively. This conclusion has been first clearly demonstrated by Tu and Xu in 2010 [119] and can be illustrated graphically by representing the two independent circuits as in Fig. 32:

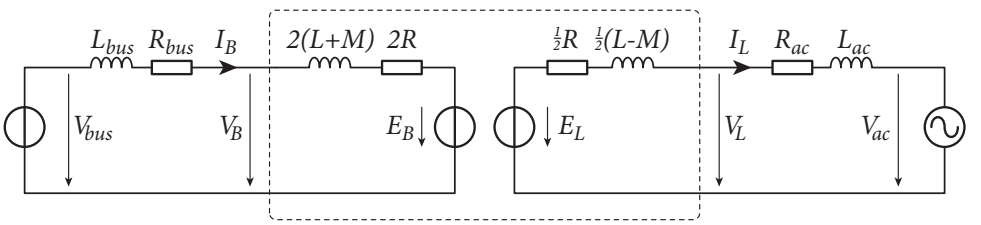


Fig. 32. Simplified equivalent functional representation of an MMC phase-leg.

Importantly, this possibility to separate the two current loops can be interpreted as the means to control independently the two *"sides"* of each phase-leg. In terms of power flows, this implies that the instantaneous power that each phase-leg is exchanging with the bus is *intrinsically* independent from the line-side power flow.

This result has also been reported by several authors and is yet widely recognized as a key feature of modular multilevel converters. However, it is worth reminding here that this possibility to decouple these power flows is tightly bound to the assumption that the arm impedances are *symmetrical* and *constant* over time (see §2.3). It is hence important to make sure that the varying number of inserted submodules does not *significantly* influence the arm impedances. Equation (19) summarizes this condition:

$$\left| Z_{L_{arm}} \right| \gg \left| Z_{ESR,tot(t)} \right| \tag{19}$$

In case this assumption does not hold, additional cross-coupling terms are appearing in the matrices of (17) and must obviously be accounted for [106].

2.4.2.1 ENERGETIC MACROSCOPIC REPRESENTATION

Relying on the transformed equations of (17)-(18), an EMR of the complete phase-leg can be established, as shown by Fig. 33:

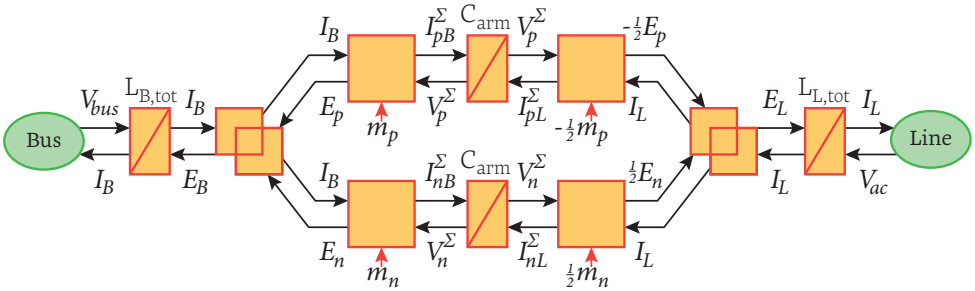


Fig. 33. EMR of the complete phase-leg based on the mathematical description of (17)-(18).

As depicted, each phase-leg is hence entirely defined by four mono-physical conversion elements, two coupling equations and four energy storage elements. On the other hand, although they are depicted several times, only two *tuning variables*[11] are available to control the whole phase-leg, namely the modulation indices $m_p(t)$ and $m_n(t)$.

Importantly, this representation also illustrates that four individual power flow paths are present inside each phase-leg, which must be balanced *in averaged values* in order to guarantee stable energy levels. This clearly concretizes the challenges constituted by the inner control of MMCs:

- The instantaneous *"input"* power flow constituted by $E_B \cdot I_B$ must be compensated on the long run by the line-side *"output"* instantaneous power $E_L \cdot I_L$. Failure to do so induces the long-term charging or discharging of both fictive capacitors. This well-know phenomena is generally reported to as *total energy control* of the phase-legs. Furthermore, since both these power flows can be controlled independently, each phase-leg can be interpreted as being essentially an energy buffer between these two controllable instantaneous power flows.
- By symmetry of the two arms, the global energy transfer is expected to split equally between the two arms. However, dedicated mechanisms could be –and are indeed!– necessary in order to enforce the *vertical balancing* between them.

2.4.3 DECOUPLED REPRESENTATIONS, SECOND STEP

Despite the meaningful information carried by (17)-(18) and their graphical representations in Fig. 33, the dynamics of the summed capacitor voltages remain difficult to analyze due to the presence of the cross-coupled terms in (18). Owing to these motivations, a second mathematical manipulation can provide interesting results. By introducing fictive modulation indices such as:

$$m_{\Delta} = \tfrac{1}{2}m_n - \tfrac{1}{2}m_p \qquad m_{\Sigma} = m_n + m_p \tag{20}$$

as well as decomposing the summed capacitor voltages $V^{\Sigma}{}_p$ and $V^{\Sigma}{}_n$ in their sum and difference terms $V^{\Sigma}{}_{\Sigma}$ and $V^{\Sigma}{}_{\Delta}$, such as in:

$$\begin{pmatrix} V_{\Delta}^{\Sigma} \\ V_{\Sigma}^{\Sigma} \end{pmatrix} = \mathbf{T}_1 \begin{pmatrix} V_p^{\Sigma} \\ V_n^{\Sigma} \end{pmatrix} = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2} \\ 1 & 1 \end{bmatrix} \begin{pmatrix} V_p^{\Sigma} \\ V_n^{\Sigma} \end{pmatrix} \tag{21}$$

11. According the terminology commonly used with EMR, a *tuning variable* is a plant input variable that can be actuated in order to control its behavior (i.e. a manipulated variable).

it is finally possible to transform (17) and (18) into an equivalent set of equations, which describes the dynamics of all state variables and parameters in modified coordinates:

$$\begin{pmatrix} \dot{I}_L \\ \dot{I}_B \end{pmatrix} = \begin{bmatrix} R_{L,tot}/L_{L,tot} & 0 \\ 0 & R_{B,tot}/L_{B,tot} \end{bmatrix} \begin{pmatrix} I_L \\ I_B \end{pmatrix} + \begin{bmatrix} -1/L_{L,tot} & 0 \\ 0 & 1/L_{B,tot} \end{bmatrix} \begin{pmatrix} V_{ac} - E_L \\ V_{bus} - E_B \end{pmatrix} \tag{22}$$

$$\begin{pmatrix} 2C_{arm} \cdot \dot{V}_\Delta^\Sigma \\ \frac{1}{2}C_{arm} \cdot \dot{V}_\Sigma^\Sigma \end{pmatrix} = \begin{bmatrix} \frac{-1}{2}m_\Sigma & 2m_\Delta \\ \frac{-1}{2}m_\Delta & \frac{1}{2}m_\Sigma \end{bmatrix} \begin{pmatrix} I_L \\ I_B \end{pmatrix} \tag{23}$$

This result leads to interesting functional representations. First, Fig. 34 shows another EMR of the MMC phase-leg, developed from (22)-(23):

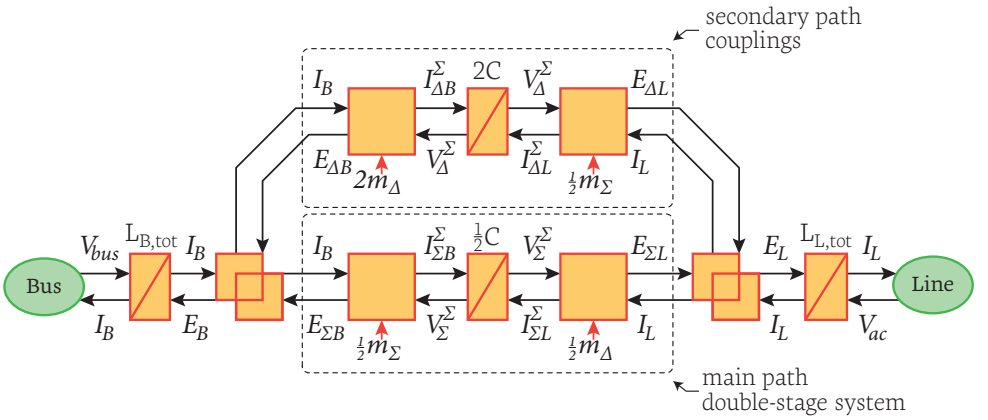


Fig. 34. EMR of the complete phase-leg based on the mathematical description, based on (22)-(23).

Additionally, this result can also be interpreted schematically, using a functionally equivalent, but fictive, circuit schematic, depicted in Fig. 35:

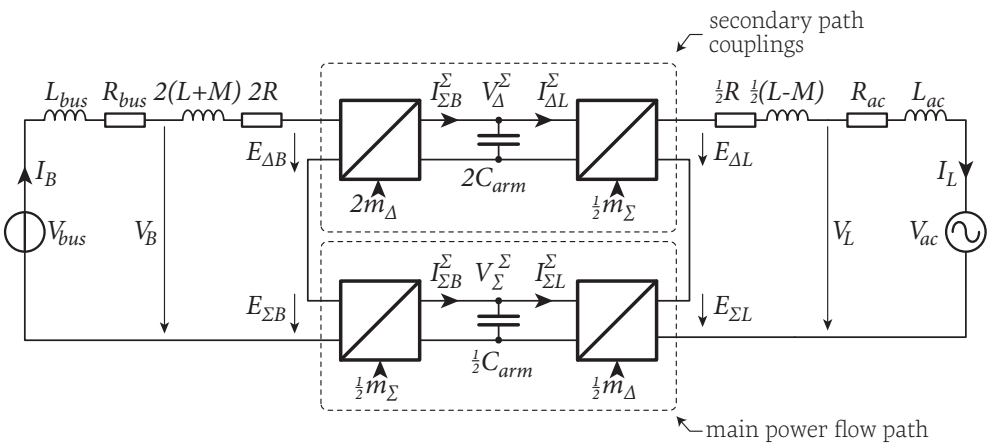


Fig. 35. Functionally equivalent electrical scheme of the MMC phase-leg, based on (22)-(23).

When compared to Fig. 32 and other existing schematic representations (see §2.2.4), these two functional representations provide important informations that were indeed missing in previous equivalent schematics:

- It graphically accounts for all state variables (i.e. those considered in the model).
- It explicitly illustrates how the two sides of the phase-leg are related in terms of energy exchanges and clearly shows that two types of input-output interactions are superposed.

Indeed, in these representations, two *fictive* arms are represented: a first arm containing the common-mode terms (Σ) and the second arm containing the differential-mode terms (Δ). This approach is somehow similar to what was first presented by Antonopoulos et. al. in [90]. Its main benefit is that is clearly highlights the dynamics of the total arm energy (related V^{Σ}_{Σ}), as well as the energy unbalance between the arms (related to V^{Σ}_{Δ}).

Additionally, a careful observation of Fig. 34 reveals a fundamental characteristic of the behavior of MMCs, which has apparently only been highlighted in [106]: the Σ arm can be considered as the *main power flow path*, while the Δ arm is essentially a *perturbation path*, related to the existing couplings between the two sides of the phase-leg.

This ascertainment is substantiated by the fact that the average value of V^{Σ}_{Σ} is necessarily at least twice $V_{bus,pk}$,[12] while the average value of V^{Σ}_{Δ} is generally desired to be zero. Hence, the power flows involved in the Σ arm are typically in the order of magnitude of the transferred active power, while the power flows in the Δ arm have zero average values (and involve only reactive power exchanges).

Hence, Fig. 34 and Fig. 35 are pushing further the results of Fig. 33 and offer a new interpretation of the basic operation principles of MMCs as they clearly show that MMC phase-legs are functionally equivalent to double-stage conversion systems, constituted by two superposed power flow paths:

- A *main power flow path* Σ, whose EMR is identical to a back-to-back power conversion system with an intermediate DC bus of voltage V^{Σ}_{Σ} and two equivalent converters controlled by $\frac{1}{2}m_{\Sigma}$ and $\frac{1}{2}m_{\Delta}$.
- A *perturbation path* Δ, which behaves similarly to the main path Σ but with an AC voltage on its intermediate fictive bus V^{Σ}_{Δ}. This second path describes couplings between the bus and line sides, which somehow embody the non-idealities of the double-stage nature of MMCs.

Hence, the control of V^{Σ}_{Σ} corresponds *by construction* to the control of the common-mode energy between the two arms (what is a direct image of the total energy stored within a phase-leg) while the control of V^{Σ}_{Δ} embodies the control of the vertical energy imbalances. Chapter 3 will demonstrate how this rather new point of view can be used in the context of control design. Besides, this result will also be exploited in Chapter 5, which addresses the integration of energy storage into MMCs.

Finally, it is worth reminding here that, since no assumption has been made regarding the actual components of all voltages and currents, all the presented representations apply to both DC/AC and AC/AC conversion structures. Besides, the representations of multi-phase systems can be easily extrapolated from these results, what is the objective of the following sections.

12. This is directly imposed by the submodules' structure as the diodes would start conducting otherwise.

2.5 FUNCTIONAL REPRESENTATIONS OF THREE-PHASE CONVERTERS

This section develops the representations of the converter structure of Fig. 26, relying on the results of §2.4. It corresponds to a three-phase inverter/rectifier or to a single-phase to three-phase direct AC/AC converter.

Among the pursued objectives, this section aims to highlight several features that the developments of §2.4 could not accurately represent, such as the arm-level voltage balancing between the phase-legs (horizontal balancing), as well as the dynamics of the circulating currents. These developments will be reused in Chapter 3 and in the Appendix, focusing on control design and component dimensioning, respectively.

Practically, the goal is to clearly separate the topology-independent issues – for which existing and non-MMC-specific knowledge inherently applies – from topology-dependent and MMC-specific issues, which much be addressed separately. That is:

- The external/terminal quantities, forming the *outer dynamics* and involving most of the active power flows. In the light of §2.4.3, this part is not MMC-specific in the sense that it is similar to a conventional two-stage power conversion system.
- The MMC-specific properties such as circulating currents and summed capacitor voltages, forming the *inner dynamics* and the arm-level balancing problem.

This objective can be summarized by Fig. 36:

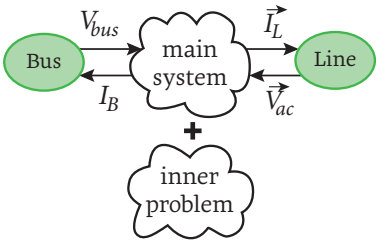


Fig. 36. Desired toplevel "black-boxed" representation of a multi-phase MMC topology.

2.5.1 REPRESENTATIONS IN *abc* REFERENCE FRAME

It is relatively straightforward to establish three-phase representations based on the results of §2.4 by assembling three phase-legs. The only important modification is to account for the dependencies between the line currents in a three-wire configuration (i.e. without a neutral conductor). Indeed, the zero-sequence current being structurally identical to zero ($I_{L,a}+I_{L,b}+I_{L,c}=\emptyset$), only two independent state variables should be represented for the line currents. Hence, applying the Clarke transformation to the line-side currents lead to (24)-(25):

$$\begin{pmatrix} \dot{I}_{L,\alpha} \\ \dot{I}_{L,\beta} \end{pmatrix} = -\begin{bmatrix} R_{ac}/L_{ac} & 0 \\ 0 & R_{ac}/L_{ac} \end{bmatrix}\begin{pmatrix} I_{L,\alpha} \\ I_{L,\beta} \end{pmatrix} + \begin{bmatrix} 1/L_{ac} & 0 \\ 0 & 1/L_{ac} \end{bmatrix}\begin{pmatrix} V_{L,\alpha} - V_{ac,\alpha} \\ V_{L,\beta} - V_{ac,\beta} \end{pmatrix} \tag{24}$$

$$\begin{cases} V_{L,0} = V_{ac,0} + V_N \\ I_{L,0} = 0 \end{cases} \tag{25}$$

Consequently, a possible EMR of the studied converter structure is given by Fig. 37, which may be simplified as in Fig. 38 using a vectorial notation:

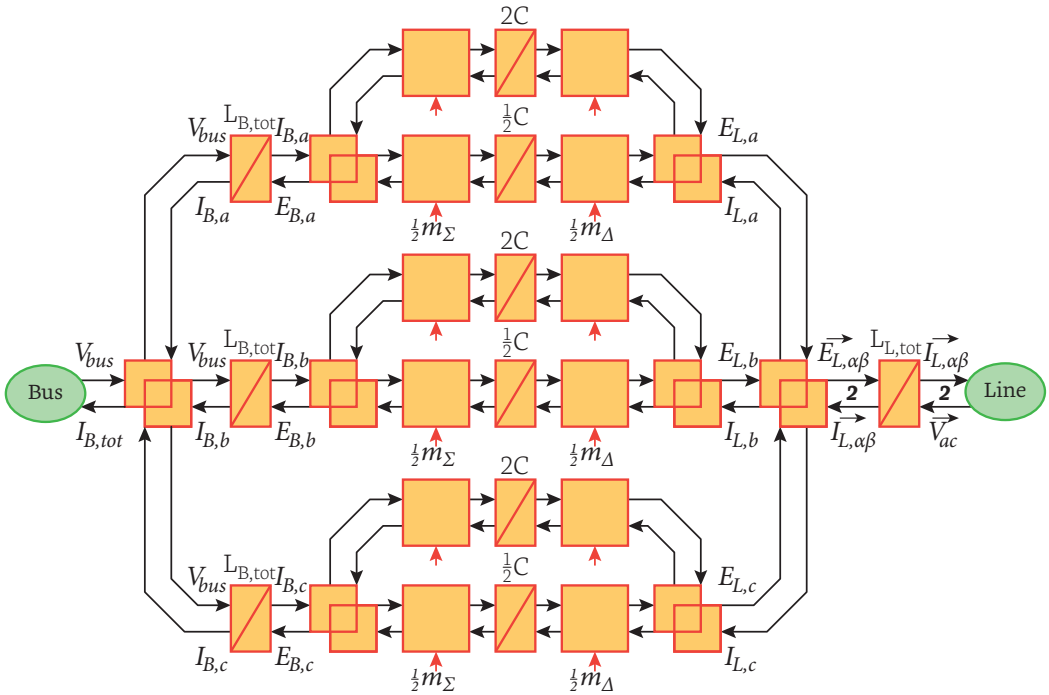


Fig. 37. Extension of the EMR of Fig. 34 to the entire DC/3-AC or 1-AC/3-AC converter structures.

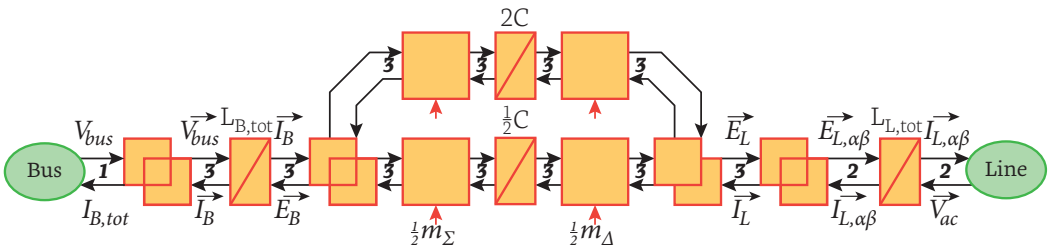


Fig. 38. Extension of the EMR of Fig. 34 to the entire DC/3-AC or 1-AC/3-AC converter structures.

Alternatively, the simplified schematic of Fig. 32 can be extended as in Fig. 39, which only depicts the current state variables, but not the summed capacitor voltages:

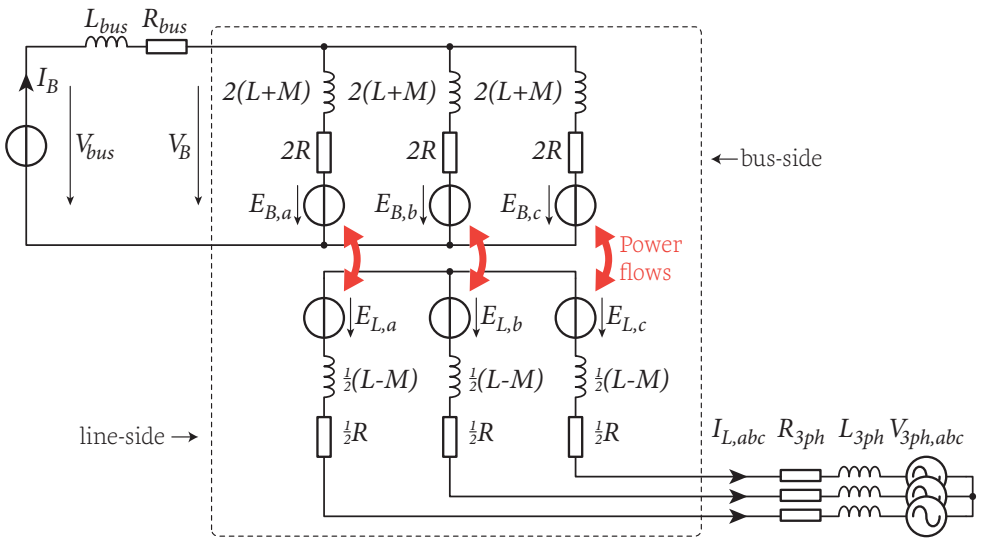


Fig. 39. Simplified equivalent scheme of the entire DC/3-AC or 1-AC/3-AC converter.

Importantly, these representations show that couplings are present between inputs and outputs, but not between phases. Indeed, the only link between the latter appears at *i)* the connection point on the bus-side (where the partial bus currents are summing up) and *ii)* on the line-side, due to the 3-wire connection. In other words, it can be concluded that the intermediate fictive busses are independent from each other.

Consequently, the operation of the three-phase MMC of Fig. 26 is, *from a functional point of view*, much closer to the operation of three double-stage single-phase converters, than a unique three-phase converter. Fig. 40 illustrates this reasoning and depicts a functionally equivalent power conversion circuit, neglecting the secondary/perturbation power flow path of Fig. 35:

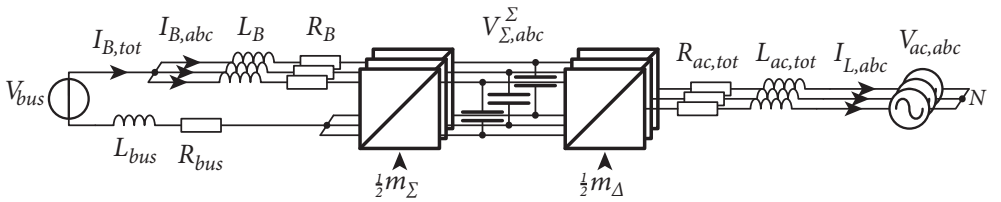


Fig. 40. Simplified equivalent scheme corresponding to the EMR of Fig. 37/Fig. 38, neglecting the secondary perturbation path. The double-stage nature of the MMC operation is clearly highlighted.

Finally, as it was shown by Fig. 37, the considered structure involves 11 independent state variables and 6 *tuning variables*. Hence, numerous power flow paths are present, which are not necessarily very intuitive, because their interactions are physically superposed. In particular, towards control design perspectives, it is difficult to identify the best choices of *tuning paths*[13] in order to control all state variables. This is especially true with respect to the summed capacitor voltages.

These comments are the main motivation for the development of representations that make use of alternative reference-frames, such as developed in the next section.

2.5.2 REPRESENTATIONS IN *αβø* REFERENCE FRAME

Following the mathematical developments of Münch [94], [120] as well as Kolb and Kammerer [74], [80] alternative reference-frames may be used in order to better highlight the corresponding phenomena. Concretely, by combining equation (10) and (17) and simply applying the Clarke transform, the *αβø* description of the bus currents can be obtained, as in equation (26), what leads to the equivalent scheme of Fig. 41 and the EMR of Fig. 42.

$$\begin{cases} 0 = E_{B,\alpha} + 2R \cdot I_{B,\alpha} + 2L \cdot \dot{I}_{B,\alpha} \\ 0 = E_{B,\beta} + 2R \cdot I_{B,\beta} + 2L \cdot \dot{I}_{B,\beta} \\ V_{bus} = E_{B,0} + (2R + 3R_{bus}) \cdot I_{B,0} + (2L + 3L_{bus}) \cdot \dot{I}_{B,0} \end{cases} \tag{26}$$

Interestingly, Fig. 41 offers the valuable benefit of fulfilling the pursued objective to separate the inner and outer converter dynamics (as in Fig. 36). However, it is of little help for the study of the voltage balancing mechanisms and for the design of suitable control schemes, because the inner power flows remain essentially unexposed.

13. According to the EMR terminology, a *tuning path* refers to a chosen power flow path that links a *tuning variable* to a *state variable*. In other words, it designates a causal path that, by way of consequence, allows to control a state variable from a manipulated input.

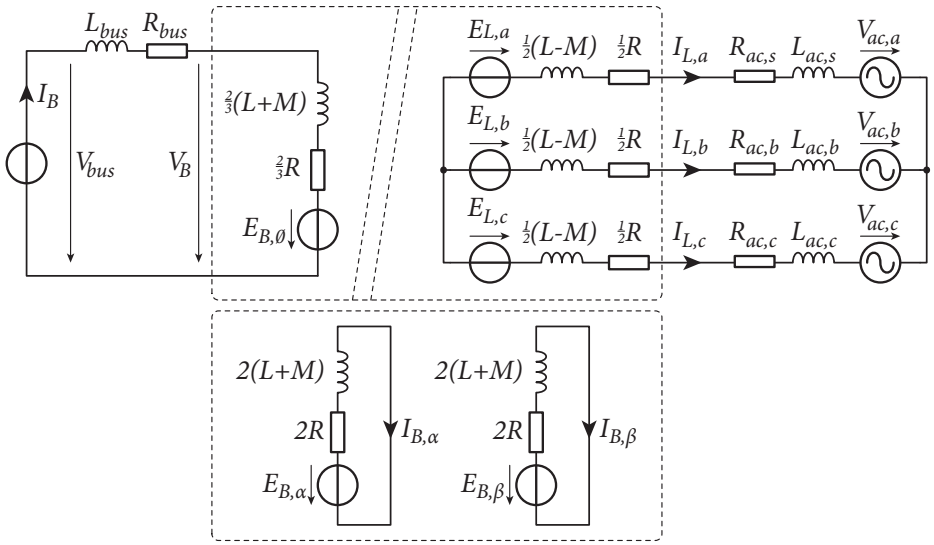


Fig. 41. Simplified equivalent scheme of the 3-phase converter of Fig. 26.

On the other hand, the EMR of Fig. 42 is achieving the same objective, while simultaneously highlighting all the relevant informations:

- The bus and line currents are represented in $\alpha\beta\emptyset$ reference-frame, what allows to clearly identify the total bus current (which is a direct image of $I_{B,\emptyset}$) as well as to highlight the fact that the zero-sequence line current $I_{L,\emptyset}$ is identically equal to zero in a 3-wire configuration.
- The sums of the two summed capacitor voltages are represented in $\alpha\beta\emptyset$ reference-frame in order to separate the horizontal voltage imbalances (α and β axes) from the total converter energy control ($\emptyset$ axis).
- The differences of the two summed capacitor voltages (vertical voltage imbalances) are kept in *abc* reference-frame as it is the most meaningful type of representation (since the phase-legs are inherently independent on that regard).

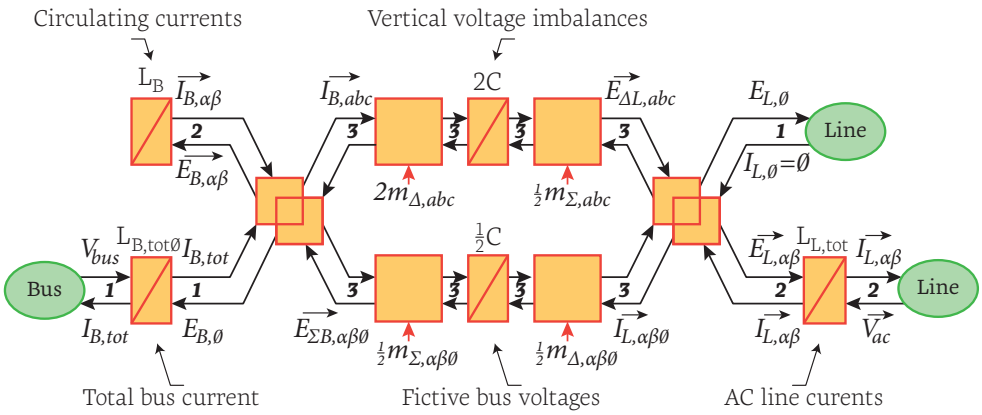


Fig. 42. Complete EMR of the 3-phase converter of Fig. 26.

As a matter of fact, for this topology, the choice of the coordinate transformation that achieves the relevant separation of the arm quantities is relatively obvious: the Clarke transform is already ideally suited to that end. However, most generally, decoupling these quantities requires to find a projection into separate vector sub-spaces that are

orthogonal between each other. This concept was first presented by Korn [124] and may be applied to develop representations of virtually any converter topology.

Interestingly, these results can also be compared to the EMR proposed by Delarue [106], which applies to the same converter topology and relies on a similar model. This alternative EMR is reproduced in Fig. 43 with edited designations. By comparing Fig. 42 and Fig. 43, it appears that both approaches are considering the same state variables for the currents. However, the EMR of [106] neither distinguishes the common-mode and differential-mode power flows, nor highlights the double-stage-type nature of the phase-legs, which are nevertheless crucial elements as to properly deduce a control scheme for the summed capacitor voltages. Chapter 3 will further address these issues.

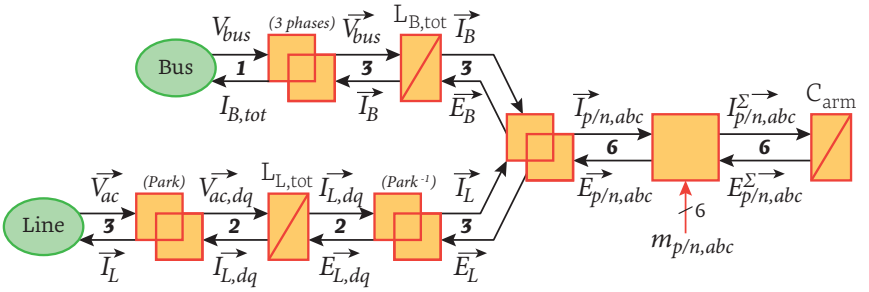


Fig. 43. EMR of the MMC phase-leg as proposed by Delarue et. al. Source: [106].

Overall, with respect to the original representation objective illustrated by Fig. 36, none of the proposed representations are offering a close match. In turn, these results are revealing a slightly different toplevel abstract concept, shown in Fig. 42:

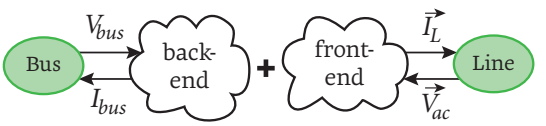


Fig. 44. Resulting "black-boxed" representation of the converter structure of Fig. 26.

While this may appear at first as somehow disappointing, it is nevertheless unavoidable as it is a logical consequence of the intrinsic behavior of MMCs, which is more naturally decomposed as in Fig. 44, rather than as in Fig. 36. Hence, rather than interpreting the behavior of MMCs as a conventional converter plus an additional inner control problem, this work suggests that it should be interpreted as a double-stage power conversion system constituted by several single-phase converters.

Of course, this interpretation of the intrinsic behavior of MMCs is valid for all the double-star-type topologies. However, since the single-star-type topologies obviously possesses only one controllable current per phase-leg, they shall thus be assimilated, *from a functional point of view*, to single-stage conversion systems only.

Finally, these development also allow to conclude that MMCs should be neither considered as VSCs, nor CSCs. Indeed, being intrinsically inductive on both their bus and line sides (and hence, current-controllable on both sides), MMCs naturally combine the two classes of topologies into one: *they are both VSCs and CSCs at the same time!* In other words, it can be concluded that MMCs possess all the assets of dual-stage conversion systems, but with the efficiency and the structure of a single-stage system, what is another way to explain their high technical attractiveness.

2.5.3 ILLUSTRATIVE SIMULATIONS

2.5.3.1 COMPARATIVE PARALLEL SIMULATION

In order to validate the developed representations along with their underlying model, comparative simulations of the operation of the three-phase inverter of Fig. 26 have been conducted on MATLAB/Simulink and PLECS.

Practically, in order to provide means of comparison, the signals produced by the closed-loop controller implemented on a conventional structural-type description are simultaneously fed to an EMR-based simulation file, in an open-loop fashion. Fig. 45 summarizes the implemented parallel simulation approach:

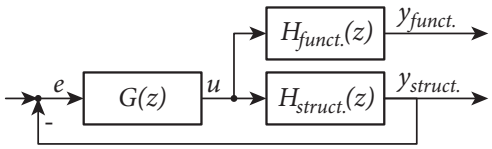


Fig. 45. Principle used to compare the EMR-based simulation versus structural-type simulation.

More precisely, the elements of Fig. 45 have been implemented as follows:

- *G(z)* is very similar to the closed-loop control scheme of Fig. 63, page 79. It corresponds to a possible control scheme of the DC/3-AC converter with the corresponding current control and superposed voltage/energy control loops.
- $H_{struct.}(z)$ is a structural –schematic-type– description of the converter using all submodules (ideal switches) and a Marquardt-type cell-level balancing algorithm.
- $H_{funct.}(z)$ is a functional description of the same converter based on the simplifying assumptions presented in §2.3, page 35 and built as in the EMR of Fig. 37. Of course, each of the blocks constituting the EMR contains the Laplace-domain equation(s) that describe(s) the behavior of the corresponding subsystem. Besides, the arm-level EMFs are generated such that they account for the multilevel modulation waveforms (see Fig. 25 *b.*) in order to offer a close match to $H_{struct.}(z)$.

On the next page, Fig. 46 shows the simulation results based on $H_{struct.}(z)$ while Fig. 47 shows the results obtained with $H_{funct.}(z)$. Both simulations are based on the exact same parameters given in Table 2, which also correspond to the laboratory prototype:

Nominal power	P	*4.1 kVA*	*Bus voltage*	V_{bus}	*700* V_{DC}
Line voltage	V_{ac}	*230 V (rms)*	*Bus-side inductance*	L_{bus}	*10 µH (ESR=100 mΩ)*
Line current	I_L	*12 A (rms)*	*Line-side inductance*	L_{ac}	*1.5 mH (ESR=80 mΩ)*
Number of cells per arm	N	*4*	*Total arm inductance*	L	*1.8 mH*
Submodule capacitance	C_{SM}	*1.3 mF (ESR=100 mΩ)*	*Mutual arm inductance*	M	*neglected*
App. switching frequency	f_{SW}	*10 kHz (2x4x1250 Hz)*	*Total arm resistance*	R	*neglected (see* R_{SM}*)*

Table 2. Simulation parameters reflecting the implemented downscaled laboratory prototype.

The simulated sequence corresponds to a full power reversal operated at $t=30\,ms$ by inverting the current setvalue from $I_d=+20\,A$ to $I_d=-20\,A$. Besides, fast current control dynamics are implemented[14] such that an acceptable transient regime is achieved around $t=30\,ms$ and a relatively narrow voltage spread is maintained.

14. In turn, the only difference between the implemented scheme and the one from Fig. 63, page 79 is that it is based on a conventional *dq* current control approach instead of the decou-

Comparing the obtained results, there is unfortunately not much to see as the differences between both simulations remains invisible.[15] This is of course an expected result, since only the representation varies between the two approaches, which rely on the exact same model. That said, it must be kept in mind that the employed set of assumptions may, on the other hand, be facing some limitations. In particular, as already commented about eq. (19), the possibility to decouple the I_B and I_L currents becomes void in case the arm impedances are loosing their strict equality over time.

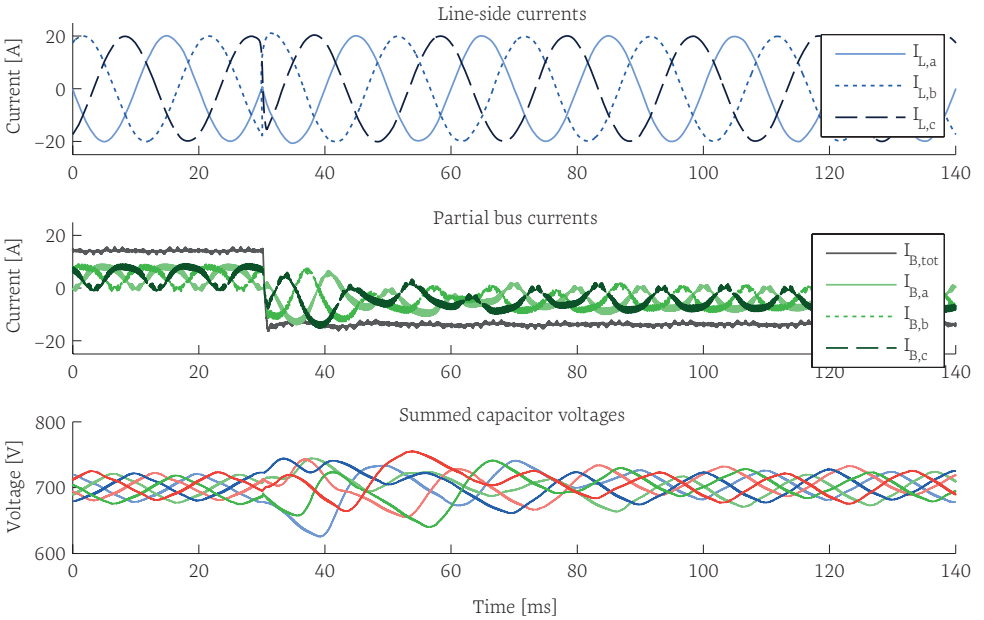


Fig. 46. Results from the structural simulation using ideal switches.

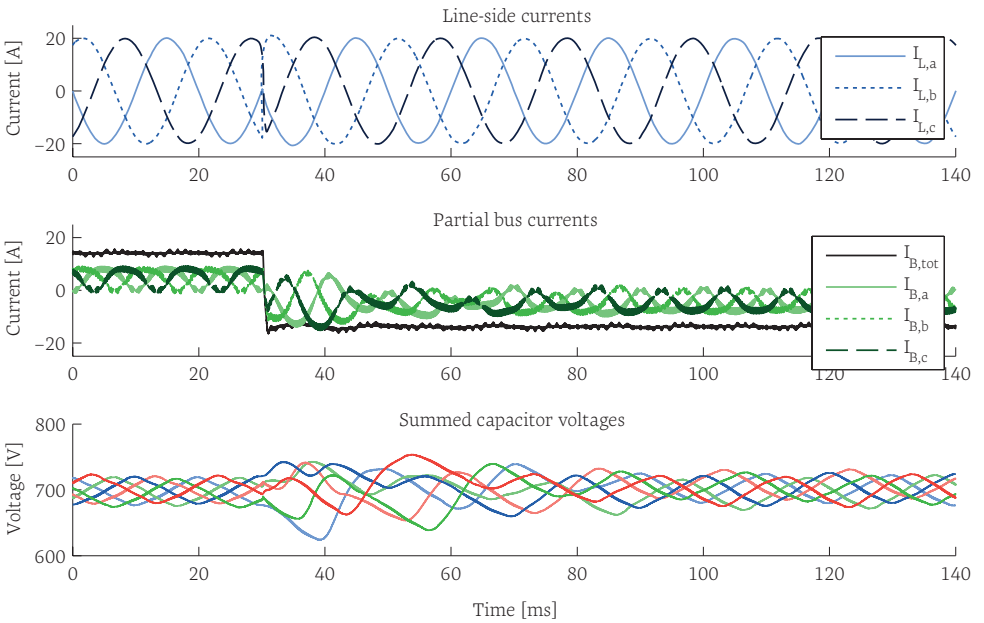


Fig. 47. Results from the functional simulation implemented as in the EMR of Fig. 37.

pled double synchronous frame current controller. This difference explains the excellent line and bus side current dynamics shown in Fig. 46 and Fig. 47.

15. In turn, there must be some slight differences between them, at least related to the accuracy of the solver, but what is anyway a freely chosen parameter.

2.5.3.2 ILLUSTRATION OF THE POWER FLOWS

Owing to the gained confidence in the developed simulation bench, the presented scenario can be further utilized to illustrate the various power flows highlighted by developed EMR-based approach.

Fig. 48 and Fig. 49 depict the four main power flows occurring in and out of the two fictive intermediate busses of each phase-leg. These results correspond to operation of the converter structure of of Fig. 26 in case of a DC/AC inverter operation and in case of a direct 16.7 Hz to 50 Hz AC/AC frequency conversion operation, respectively. The depicted power flows are:

- $I_{B,abc} \cdot E_{\Delta B,abc}$: bus-side differential-mode power (upper left).
- $I_{L,abc} \cdot E_{\Delta L,abc}$: line-side differential-mode power (upper right).
- $I_{B,abc} \cdot E_{\Sigma B,abc}$: bus-side common-mode power (lower left).
- $I_{L,abc} \cdot E_{\Sigma L,abc}$: line-side common-mode power (lower right).

Hence, for both figures, the integral of the difference between the two first rows (in blue) results *by construction* in the vertical energy imbalance. Similarly, the integral of the difference between the two last rows (in green) leads to the total phase-leg energy variation. Equations (27)-(28) materialize these two statements:

$$W_{\Delta} = \int \underbrace{I_B \cdot E_{\Delta B}}_{first\ row} - \underbrace{I_L \cdot E_{\Delta L}}_{second\ row} dt = \tfrac{1}{2}\left(2C_{arm}\right)V_{\Delta}^{\Sigma} \tag{27}$$

$$W_{\Sigma} = \int \underbrace{I_B \cdot E_{\Sigma B}}_{third\ row} - \underbrace{I_L \cdot E_{\Sigma L}}_{fourth\ row} dt = \tfrac{1}{2}\left(\tfrac{1}{2}C_{arm}\right)V_{\Sigma}^{\Sigma} \tag{28}$$

a) DC/AC inverter operation

Fig. 48 presents the results of the exact same sequence that was simulated in the previous section. It corresponds to a full power reversal operated at $t=30\,ms$ by inverting the current setvalue from $I_d=+20\,A$ to $I_d=-20\,A$.

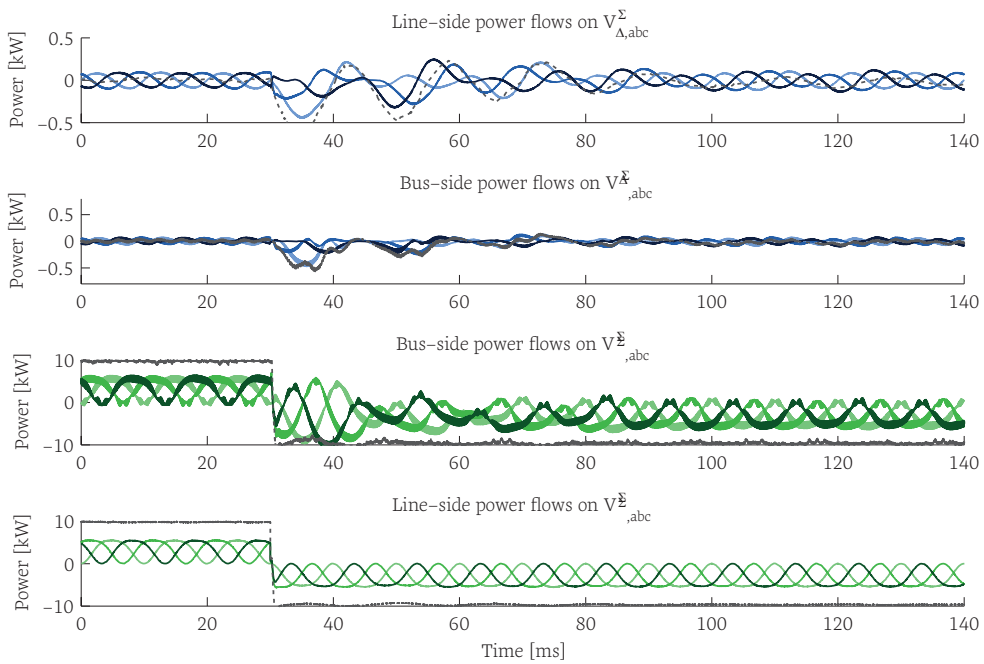


Fig. 48. Typical power flows in the phase-legs for the three-phase DC/AC scenario.

As it can be seen on Fig. 48, the differential-mode power flows (in blue), are of reduced amplitudes compared to the common-mode power flows (in green). Besides, they are essentially reactive, owing to their zero mean values, except during balancing transients. This justifies the classification introduced at the end of §2.4.3 : the differential-mode fictive bus represents undesirable input-output couplings, while the main power path is constituted by the common-mode terms.

Additionally, as shown by the last row, the 100 Hz power components related to the line-side are common-mode power components between the two arms of a phase-leg. The sum of the three instantaneous line-side powers s the total instantaneous line-side power (in gray), which is here purely constant thanks to the symmetry of the line currents and voltages. As expected, some fourth-order harmonics are also present on these individual power flows due to the products between the third harmonic zero-sequence voltage injection and the line currents.

Finally, it is important to note that, in these simulations, the bus-side instantaneous power flows are controlled such that they match very closely the line-side common-mode powers (the two last rows reveals similar waveforms). The total energy within the phase-legs are therefore pure constants, apart during balancing transients. This strategy aims to minimize the voltage ripple on the capacitors versus the sizing of the latter. This particular topic will be further discussed in §3.2.2.

b) Direct AC/AC frequency conversion

In order to simulate this second case, the same simulation bench is modified to be adapted to the operation of an AC/AC configuration. Obviously, its control is necessarily edited, as presented later in §3.4.3. Here, a full power reversal is operated at $t=130\,ms$ by inverting the bus current setvalue from $\hat{I}=+30\,A$ to $\hat{I}=-30\,A$:

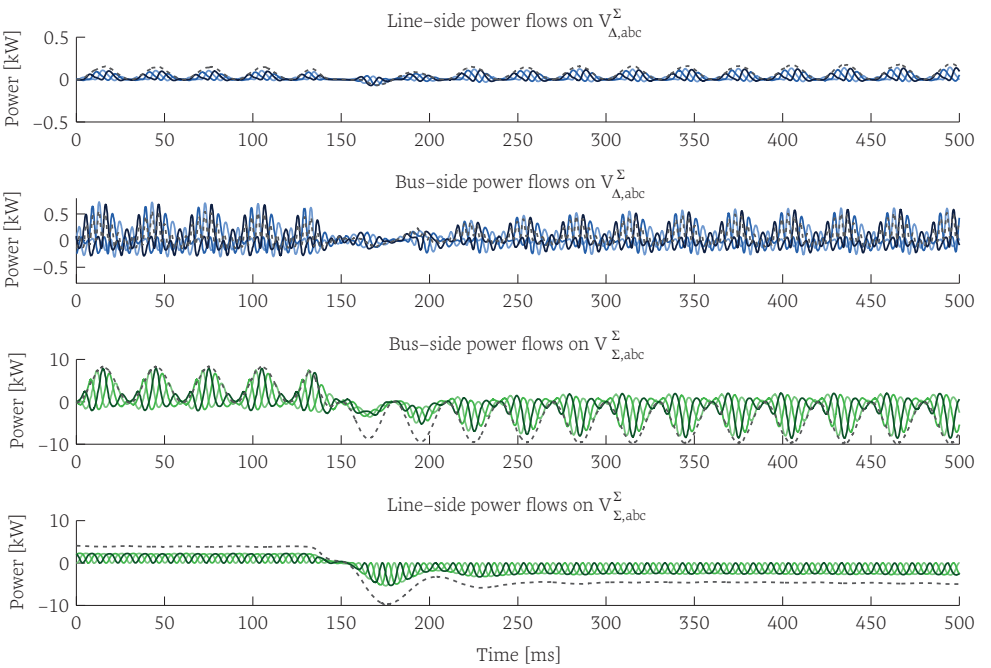


Fig. 49. Typical power flows in the phase-legs for the 1-AC/3-AC scenario.

Compared to Fig. 48, significant differences are related to the pulsating nature of the instantaneous power flow on the bus side (see the total bus-side power on the third row, in gray). Indeed, in order to exchange a constant total instantaneous power on its three-phase side (in gray on the last row), the converter is required to buffer this pulsation within its phase-legs. This strategy implies relatively large differences between the bus- and line-side common-mode power flows and therefore, necessarily induces large total energy variations as well.

Besides, as visible on the figure, the relatively slow and poorly damped inversion of the power flow (see the gray curves) allows on the other hand for a very smooth transient regime in terms of vertical imbalances (in blue) and common-mode power transfer mismatch (in green), what also corresponds to a limited transient regime in terms of capacitor voltage ripple. Section 3.6.2 will make further comments on these control issues and their relation to the corresponding sizing of the submodules capacitors.

Overall, Fig. 48 and Fig. 49 suffice to illustrate on their own the challenges related to the control of MMCs. Indeed, there are no less than four power flow paths per phase-leg, which all involve numerous frequency components related to the common-mode and differential-mode combinations of the line- and bus-side quantities. This comment thereby motivates further efforts towards the analysis of the spectral content of these various power flows, what is developed in the following section.

2.6 SPECTRAL ANALYSIS OF THE CURRENT AND VOLTAGE COMPONENTS

As illustrated in the previous sections, the operation of each phase-leg may be interpreted as involving four different power flow paths, each comprising various frequency components. This particular behavior is further detailed here, first in order to get a better understanding of the corresponding principles of operation, but also because it is key to the MMC control design. Indeed, as the control of MMC phase-legs necessitates the control of more state variables than there are *tuning variables* to impact on them,[16] some artful use of the specific spectral contents of these power flows is necessary. This is particularly true in case a cascaded control scheme must be designed, featuring voltage control loops (for the summed capacitor voltages) on the top of inner current control loops.

In the reported works of Ilves [101], Vasiladiotis [126], [199] or Li. et.al. [141], extensive mathematical developments can already be found, describing the spectral content of the MMC currents and voltages in various operating conditions and under various assumptions. In contrast, the present section aims to review this spectral analysis *in a generic manner*, only aiming to highlight how the four presented power flows can be used to impact on the arm-level voltage balancing problem. It thereby only focuses on the *average values* of these power flows.

Subsequently, and only then, specific operating conditions will be introduced as to get some insight on the operating-conditions-dependent phenomena taking place in MMCs. As it will be shown, some general conclusions can be made though, opening interesting perspectives for the control design developed later in Chapter 3.

16. Essentially four state variables for only two tuning variables per phase-leg, see §2.4.2.1.

In a general way, the converter currents and EMFs can be described by Fourier series, such as defined by equation (29). Naturally, among the corresponding terms, the amplitudes of some frequency components (or most of them) may be of negligible values and may be disregarded in the analysis:

$$(29)\qquad \begin{cases} I_L(t)=\sum_{n\in\mathbb{N}^0} i_L^n\cos\left(n\omega t+\varphi_k\right) \\ I_B(t)=\sum_{k\in\mathbb{N}^0} i_B^k\cos\left(k\Omega t+\delta_k+\gamma_k\right) \end{cases} \qquad \begin{cases} E_L(t)=\sum_{n\in\mathbb{N}^0} e_L^n\cos\left(n\omega t\right) \\ E_B(t)=\sum_{k\in\mathbb{N}^0} e_B^k\cos\left(k\Omega t+\delta_k\right) \end{cases}$$

In (29), the indices n and k refer to the harmonic orders on the line and bus side quantities, respectively. Similarly, ω and Ω are the pulsation frequencies on the line and bus sides, respectively. $E_L(t)$ is considered as the reference of phase and hence, the φ_k are the current phase angles on the line side, the δ_k are the relative phases of the bus-side voltage components (with regards to the line-side) and γ_k are the current phase angles on the bus side, all respectively to $E_L(t)$.

Making use of the coordinate transformation related to $\mathbf{T_1}$ and $\mathbf{T_2}$ in eq. (13), these equations can be combined to give rise to:

$$(30)\qquad \begin{cases} I_p(t)=I_B(t)+\frac{1}{2}I_L(t)=\sum_k i_B^k\cos\left(k\Omega t+\delta_k+\gamma_k\right)+\frac{1}{2}\sum_n i_L^n\cos\left(n\omega t+\varphi_k\right) \\ I_n(t)=I_B(t)-\frac{1}{2}I_L(t)=\sum_k i_B^k\cos\left(k\Omega t+\delta_k+\gamma_k\right)-\frac{1}{2}\sum_n i_L^n\cos\left(n\omega t+\varphi_k\right) \\ E_p(t)=\frac{1}{2}E_B(t)-E_L(t)=\frac{1}{2}\sum_k e_B^k\cos\left(k\Omega t+\delta_k\right)-\sum_n e_L^n\cos\left(n\omega t\right) \\ E_n(t)=\frac{1}{2}E_B(t)+E_L(t)=\frac{1}{2}\sum_k e_B^k\cos\left(k\Omega t+\delta_k\right)+\sum_n e_L^n\cos\left(n\omega t\right) \end{cases}$$

Recalling the elementary definition of the product of trigonometric functions:

$$(31)\qquad \cos(\alpha)\cos(\beta)=\frac{1}{2}\cos(\alpha-\beta)+\frac{1}{2}\cos(\alpha+\beta)$$

the total power flows on the positive and negative arms can be easily computed by the products of the corresponding quantities from (30). The obtained results are shown in equations (32)-(33). However, due to the fact that the resulting expressions are relatively complex and might be confusing, they are not entirely shown. Instead, only their non-zero average terms are presented, plus a remainder of zero average value.

$$(32)\qquad \begin{aligned} p_p(t)=&\frac{1}{4}\sum_{k=n} e_B^n i_B^k\cos\left(\gamma_k\right)-\frac{1}{2}\sum_{k\Omega=n\omega} e_L^n i_B^k\cos\left(\delta_k+\gamma_k\right) \\ &+\frac{1}{8}\sum_{k\Omega=n\omega} e_B^n i_L^k\cos\left(\varphi_k-\delta_k\right)-\frac{1}{4}\sum_{k=n} e_L^n i_L^k\cos\left(\varphi_k\right)+\hbar\left\{\cos(n\omega t)\right\} \end{aligned}$$

$$(33)\qquad \begin{aligned} p_n(t)=&\frac{1}{4}\sum_{k=n} e_B^n i_B^k\cos\left(\gamma_k\right)+\frac{1}{2}\sum_{k=n\frac{\omega}{\Omega}} e_L^n i_B^k\cos\left(\delta_k+\gamma_k\right) \\ &-\frac{1}{8}\sum_{k\Omega=n\omega} e_B^n i_L^k\cos\left(\varphi_k-\delta_k\right)-\frac{1}{4}\sum_{k=n} e_L^n i_L^k\cos\left(\varphi_k\right)+\hbar\left\{\cos(n\omega t)\right\} \end{aligned}$$

Of course, equations (32)-(33) are making use of the fact that only the components of identical frequencies infer a product whose average value is non-zero, what is a direct consequence of (31). For a more complete development of these power terms, the reader is advised to see the reported works of Vasiladiotis et. al. [126], Ilves et. al. [101] or Li et. al. [141].

Subsequently, by computing the sum and the difference of these expressions, the *average values* of the common-mode and differential-mode power transfers can be easily derived as in (34)-(35):

$$\left\langle p_{DM}(t)\right\rangle = \underbrace{\sum_{k\Omega=n\omega} e_L^n i_B^k \cos\left(\delta_k+\gamma_k\right)}_{\text{cross-product power}} - \underbrace{\tfrac{1}{4}\sum_{k\Omega=n\omega} e_B^n i_L^k \cos\left(\varphi_n-\delta_n\right)}_{\text{cross-product power}} \tag{34}$$

$$\left\langle p_{CM}(t)\right\rangle = \underbrace{\tfrac{1}{4}\sum_{k\in\mathbb{N}^0} e_B^k i_B^k \cos\left(\gamma_k\right)}_{\text{input power}} - \underbrace{\tfrac{1}{4}\sum_{n\in\mathbb{N}^0} e_L^n i_L^n \cos\left(\varphi_n\right)}_{\text{output power}} \tag{35}$$

Two important comments can be made out of these generic results:

- As shown by eq. (34), a *differential-mode power flow* of non-zero average value exists for all common integer multiples of ω and Ω. In other words, vertical imbalances are induced – or can be compensated – by any existing harmonic corresponding to these specific frequencies. Besides, the corresponding power terms are involving cross-products between the two converter sides, what reinforces the analysis presented at the end of §2.4.3, claiming that differential-mode power flows are belonging to a secondary and perturbation path.
- As shown by eq. (35), the expression of the average *common-mode power flow*, on the other hand, clearly resembles the general definition of the difference between two separate polychromatic power flows. Besides, as identified on the equation, the latter are entirely decoupled between the bus and line sides (no cross-product terms are present). This also reinforces the analysis presented earlier, claiming that MMCs are essentially assimilable to double-stage conversion systems, with two independent and controllable power flows for each phase-leg.

These results are also the conclusions that were originally drawn by Antonopoulos et. al. [90]. However, unlike in [90], the formulation proposed by (34)-(35) offers the important benefit to accurately mirror the proposed EMRs (typ. Fig. 34) as well as their equivalent electrical schemes (typ. Fig. 35). Hence, the three presented types of representations (equivalent schemes, EMR and mathematical expressions) are closely matching, what allows to transparently switch from one formalism to another depending on the desired perspective. Fig. 50 highlights some of these correspondences:

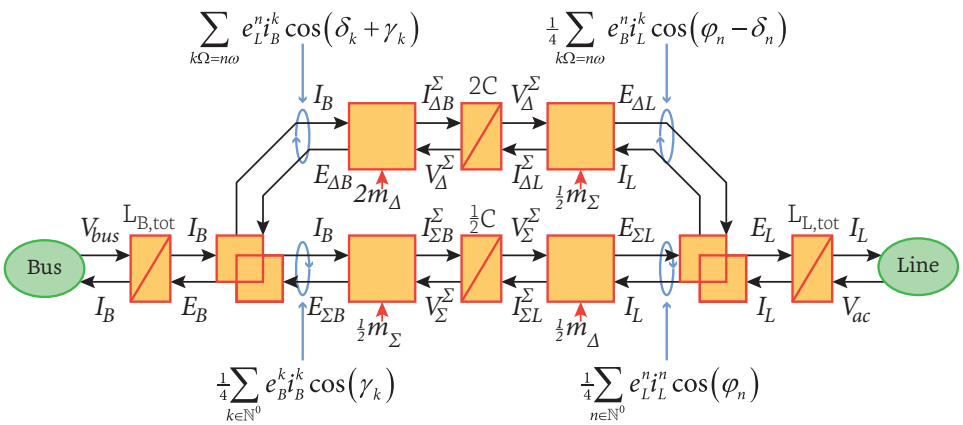


Fig. 50. Correspondences between the developed graphical representations and the typical average values of the power flows in sinusoidal operating conditions.

That said, since these equations are only generic results, few spectral components among the presented terms can be expected to be of significant amplitudes in most applications. These general results shall thus be subsequently adapted, depending on the operating conditions.

To that end, two examples are developed in §2.6.1 and §2.6.2, corresponding to DC/AC and direct AC/AC conversion, respectively. Both cases are related to topology of Fig. 26. The pursued goal is to illustrate that the spectral components that impact on these power flows differ between the two cases. Besides, as it will be shown, simple and relatively general conclusions can be made out of these developments, which will be reused in Chapter 3 to address the arm-level closed-loop voltage balancing.

2.6.1 THREE-PHASE DC/AC CONVERTER

Whether in the case of a grid-tied inverter or of a drive, the corresponding power converter is generally facing operating conditions characterized by:

- A voltage V_{bus} which is ideally constituted by a plain DC quantity only, without any oscillating terms. Hence, in the previously presented equations, the ${e_B}^k$ are opposed no counter-voltage, leading to currents angles γ^k that are directly defined by the impedance of the line-side reactors ($\sim\pi/2$). Besides, the δ^k can be imposed arbitrarily in case harmonic components are voluntarily injected through ${e_B}^k$. The only exception is the $\emptyset^{th}$ harmonic term ${e_B}^{\emptyset}$, which corresponds to the average bus-side EMF and is counteracted by the bus voltage V_{bus}.[17]
- Line-side currents that are essentially monochromatic sinusoidal functions, which corresponds to ${i_L}^n = \emptyset$ for all $n \neq 1$.
- Line-side EMFs that are constituted by a fundamental-harmonic component ${e_L}^1$, which is counteracted by the line voltage ${v_{ac}}^1$.

Besides, some additional characteristics may naturally exist or be tolerated, depending on the application:

- Small line current offsets (i.e. ${i^{\emptyset}}_L \neq \emptyset$) may exist or be tolerated during transients, as long as their long-term value remains essentially zero (for instance, in order not to influence the magnetization of the corresponding transformer).
- Generally, any harmonics are accepted in the partial bus currents as long as they remain symmetrical among the phases (i.e. ${i^n}_{B,a} + {i^n}_{B,b} + {i^n}_{B,c} = \emptyset$ for all $n > \emptyset$). However, in special cases, this requirement may not need to be enforced, for instance during transients, leading to small and short-term oscillations of the total bus current.

Consequently, the expressions of (34)-(35) can be adapted as:

$$\left\langle p_{DM}(t)\right\rangle = \underbrace{\left(E_L^0 \cdot I_B^0\right)}_{\text{p}_{\text{DM}}\text{in from 0Hz}} - \underbrace{\tfrac{1}{4}\left(E_B^0 \cdot I_L^0\right)}_{\text{p}_{\text{DM}}\text{out from 0Hz}} + \underbrace{e_L^1 i_B^1 \cos\left(\delta_1 + \tfrac{\pi}{2}\right)}_{\text{p}_{\text{DM}}\text{in from 50Hz}} - \underbrace{\tfrac{1}{4} e_B^1 i_L^1 \cos\left(\varphi_1 - \delta_1\right)}_{\text{p}_{\text{DM}}\text{out from 50Hz}} \tag{36}$$

$$\left\langle p_{CM}(t)\right\rangle = \underbrace{\tfrac{1}{4}\left(E_B^0 \cdot I_B^0\right)}_{\text{p}_{\text{CM}}\text{in from 0Hz}} + \underbrace{\tfrac{1}{4}\sum_{\substack{k\in\mathbb{N}\\ k\neq 0}} e_B^k i_B^k \cos\left(\tfrac{\pi}{2}\right)}_{\text{input harmonic power}\simeq 0} - \underbrace{\tfrac{1}{4}\left(E_L^0 \cdot I_L^0\right)}_{\text{p}_{\text{CM}}\text{out from 0Hz}} - \underbrace{\tfrac{1}{4} e_L^1 i_L^1 \cos\left(\varphi\right)}_{\text{p}_{\text{CM}}\text{out from 50Hz}} \tag{37}$$

Hence, assuming that the chosen set of harmonic components accurately describes the operation of the considered three-phase inverter, several observations can be made:

17. The reader is advised to have a look at Fig. 32, page 40 in case this is not obvious.

– As shown by the two first terms of (36), any current or voltage offset on the line side combines with the DC side quantities as to impact the vertical balance of the phase-leg. This fact is rather often omitted in the literature but is a potential cause of slight vertical imbalances that must be taken into account and/or compensated.
– As shown by the last two terms of (36), any line-frequency component on the bus side is also impacting the average differential-mode power flow. This fact is generally used to actively enforce the *vertical balancing* of each phase-leg. Two degrees of freedom are available to act on these power flows: the amplitudes of the bus-side EMFs e_B^1 and their relative phase δ_1.
– The absence of third-order terms in (36) proves that the third-order harmonic voltage injection[18] has no impact on the vertical balance unless some third-order harmonic voltages and currents are present on the bus side as well.
– As shown by the second term of (37), harmonics in the partial bus currents do not carry any active power (the γ^k are defined by the arm inductors to approx. $\pi/2$).
– As shown by the first and third terms of (37), when present, 0 Hz components are carrying non-zero common-mode powers on both sides. Generally, the third term is controlled to be zero, while the first and last terms of (37) are controlled such that they guarantee the power transfer balance for each phase-leg. Doing so allows for the *total energy control* and *horizontal balancing* of the entire converter.

Overall, the analysis of these basic equations provide means to ensure the complete balancing of the DC/3-AC converter. This can be summarized as follows:

– The *common-mode* power transfer is a matter of the difference of active powers between the input and the output of each phase-leg; the output being a product of line-frequency components, while the input is a product of DC components.
– As already mentioned, the *differential-mode* power transfer is impacted as soon as components of identical frequencies are simultaneously present on both the line and bus sides. Therefore, in case the vertical balancing must be actively enforced, line-frequency components can be purposely injected on the bus side.[19]

2.6.2 DIRECT 3-AC/1-AC FREQUENCY CONVERTER

In case it is implemented in a direct frequency conversion application, the same converter structure is facing different operating conditions characterized by:

– A bus-side external voltage which is an essentially monochromatic sinusoidal function, such that $v_{bus}{}^k = \emptyset$ for all $k \neq 1$. Consequently, i_B^1 and γ^1 can be adjusted freely, while all the other $i_B{}^k$ are desirably negligible.
– As in §2.6.1, any harmonics may generally be accepted in the partial bus currents as long as they remain symmetrical (i.e. $i^n_{B,a} + i^n_{B,b} + i^n_{B,c} = \emptyset$ for all $n > \emptyset$). When necessary, this requirement can be relaxed during transients, leading to short-term oscillations of the total bus current. In any case, the $e_B{}^k$, δ^k and $i_B{}^k$ can be chosen arbitrarily, but remain constrained by the line-side inductance for all $k \neq 1$.
– The line-side behavior is generally similar to the case described in §2.6.1.

18. Typically added in order to increase the maximum modulation depth to 1.16. In this case, equation (36) contains the cross-products from the corresponding harmonic components.
19. As first proposed by Antonopoulos et.al. [90] and further developed by Münch [120] as well as Kolb and Kammerer [74],[80]. See also §3.2.2.

Hence, assuming that the bus frequency is defined by $\Omega = 2\pi \cdot 16.7\,\text{Hz}$, while the line frequency is $\omega = 2\pi \cdot 50\,\text{Hz}$, the expressions of (34)-(35) can be adapted as:

$$\left\langle p_{DM}(t)\right\rangle = \underbrace{\left(E_L^0 \cdot I_B^0\right)}_{\text{P}_{\text{DM}}\text{in from 0Hz}} - \underbrace{\tfrac{1}{4}\left(E_B^0 \cdot I_L^0\right)}_{\text{P}_{\text{DM}}\text{out from 0Hz}} + \underbrace{e_L^1 i_B^3 \cos\left(\delta_3 + \tfrac{\pi}{2}\right)}_{\text{P}_{\text{DM}}\text{in from 50Hz}} - \underbrace{\tfrac{1}{4} e_B^3 i_L^1 \cos\left(\varphi_1 - \delta_3\right)}_{\text{P}_{\text{DM}}\text{out from 50Hz}} \tag{38}$$

$$\left\langle p_{CM}(t)\right\rangle = \underbrace{\tfrac{1}{4}\left(E_B^1 \cdot I_B^1\right)}_{\text{P}_{\text{CM}}\text{in from 16.7Hz}} + \underbrace{\tfrac{1}{4}\sum_{\substack{k\in\mathbb{N}\\ k\neq 1}} e_B^k i_B^k \cos\left(\tfrac{\pi}{2}\right)}_{\text{input harmonic power}\simeq 0} - \underbrace{\tfrac{1}{4} e_L^1 i_L^1 \cos\left(\varphi\right)}_{\text{P}_{\text{CM}}\text{out from 50Hz}} \tag{39}$$

Few conclusions are worth mentioning here:

- The *common-mode* average power transfer is a matter of the difference of active powers between the input and the output of each phase-leg; the output being here a product of 50 Hz components and the input a product of 16.7 Hz components.
- Here again, the *differential-mode* power transfer is impacted as soon as components of identical frequencies are simultaneously present on both the line and bus sides; which are here the third-order harmonics of the bus frequency combining with the fundamental of the line frequency.

Overall, by generalizing the two sets of conclusions, it can be easily deduced that:

- As shown by eq. (37) and (39), the *common-mode* power transfer (horizontal balancing/total energy control) can be easily controlled through partial-bus currents of the same frequency as on the *bus-side voltage source*.
- As shown by eq. (36) and (38), the *differential-mode* power flows (and hence, the vertical balancing) can be impacted by partial-bus currents of the same frequency as on the *line-side voltage source*.

These two fundamental observations constitute the basis of the energy control of MMCs as they show that *i)* some separation between the control of the common-mode and differential-mode power flows is possible, that *ii)* these two distinct objectives can be achieved using a *unique and common quantity*: the partial bus current, but requires that *iii)* appropriate spectral components are injected in the partial bus currents.

Moreover, these results also illustrate that, by combining the developed functional representations with a simple spectral analysis, it is possible to highlight the balancing mechanisms MMCs with a few lines of calculation only. Furthermore, these results can be easily extended by accounting for all the relevant line- and/or bus-frequency harmonics, which introduces further degrees of freedom and/or constraints. Exemplarily, such developments can allow for the mathematical description of second-order harmonic injection in the partial bus currents,[20] or the description of all the corresponding power flows in case of active filtering applications.

That said, even though the balancing of these power flows is relatively easy to achieve *in average values*, it must be recalled that the corresponding power terms are also related to pulsating power components, typically at 33 Hz, respectively 100 Hz, depending on the external sources.[21] Hence, additional efforts may be advantageously devoted

20. This is a commonly used technique in order to reduce the phase-leg energy pulsation and hence, lower the capacitance requirements for the submodules. Section 3.2.1.2 will details and illustrate this approach.

21. This is the obvious result of eq. (31) applied to the corresponding current and voltage components. In turn, power terms of 16.7±16.7 Hz, 50±16.7 Hz and 50±50 Hz are unavoidably

to improve the balancing of the *pulsating* powers, as it can lead for some cases to the minimization of the capacitive energy requirements (see §3.2.1.2). In some other cases however, such as in frequency conversion applications or variable-speed drives, some pulsating power terms cannot be compensated, leading to unavoidable and potentially troublesome oscillations of the arm energies for specific operating conditions, which thus deserve a careful analysis.

In any case, such developments are going beyond the scope of this work. Besides, they have already received a significant attention from the existing literature. However, the complexity of the issues raised by these few comments underlines how important it is that such mathematical developments remain closely linked to physical phenomena, such that they can be interpreted in a simple manner. In this sense, the fact that the developed mathematical and graphical representations maintain a close matching is certainly highly valuable.

2.7 SYNTHESIS

Through this chapter, the development of functional representations of Modular Multilevel Converters, partly based on principles of the Energetic Macroscopic Representation, has allowed to make different conclusions with respect to the fundamental operating principles of this converter technology. However, before coming to these findings, a few important comments can be made with respect to the methodology itself.

2.7.1 BENEFITS AND LIMITATIONS OF EMR

A key element of the strong formalism imposed by the use of EMR was mentioned in §2.4.1.1, related to the notion of *conflict of association*, which reveals the non-independence of some state variables. In the said case, the occurrence of this conflict is very instructive in the sense that it forces the interpretation of the currents in a common mode/differential mode frame, as it is the only option that allows the consideration of a minimum number of state variables and that allows the decoupling of these quantities.

Another important insight brought by EMR is related to the function of the arm inductors, which has appeared to go beyond a simple «protective device» against imperfections in the switching and/or the balancing of the cells, but turned out to be an indispensable element to the independent control of both sides of the phase-legs, as well as to guarantee the respect of basic rules of association when connecting two power sources (presence of an inductive element between two voltage sources).

Of course, by the end of 2014, these comments are not entirely new facts, but these few remarks show that the developed approach is able to provide some critical elements of interpretation in a methodical manner. Indeed, it is mainly the necessary respect of the EMR formalism that forced to «draw» each phase as a dual-stage conversion system. This interpretation being somewhat counter-intuitive, its establishment is to be directly credited to the functional formalism imposed by EMR.

present in such operating conditions (to which other terms are added in case second-order harmonic injection is used).

2.7.2 CONCLUSIONS

Relying on a conventional model, this chapter has introduced different representations of MMCs derived from that of the elementary phase-leg. The focus was set on the double-star chopper- (or bridge-) cells types of converter topologies, leading to various types of representations including EMR-based as well as schematic-type and mathematical approaches. An excellent compatibility has been shown between these representations. Among the proposed representations, some have also recently appeared in [105] and [108]. Otherwise, they constitute an original contribution of the present work, which has only been partially published in [104].

The relevance of these results has been demonstrated through comparative simulations conducted along with conventional structural-type representations. As it was shown, these representations are not limited to switching-averaged approaches but can account for the multilevel nature of the corresponding waveforms as well. Hence, even though their primary purpose is not to serve as simulation tools, such representations can be very useful in macroscopic /system-level types of studies. Chapters 3 and 4 will further confirm the validity of these representations by providing additional simulation and experimental results obtained through control schemes that are directly based on these developments as well.

Apart from its possible use in simulations – and before all – the EMR formalisms have proven to be an excellent *tool of analysis*, forcing an abstraction effort that is very useful to the study of MMCs. In particular, the essentially functional (as opposed to structural) nature of the obtained representations allows to take some distance on the basic principles of operation of these converters, which is of high importance in the context of an explanatory approach.

Overall, the most significant contribution of this chapter is certainly related to the proposed *interpretation* of the basic operating principles of MMCs. Indeed, by reusing a known decomposition of the summed capacitor voltages into a sum term Σ and a difference term Δ, it was proposed to interpret the fictive arm Σ as the main arm, while the fictive arm Δ can be considered as a perturbation, involving coupling terms between the bus- and line- sides of the phase-legs.

Furthermore, as illustrated by Fig. 37 or Fig. 40, the phase-legs of MMCs have been shown to be very similar to *double-stage power conversion systems*. Hence, the so constituted multi-phase MMCs have been shown to be essentially similar to multiple double-stage single-phase converters. As an example, the typical DC/3-AC structure of Fig. 26 is, from a functional point of view, identical to three DC/DC converters followed by three single-phase inverters. The mathematical analysis and the illustration through simulations of the four corresponding power flow have confirmed the relevance of these conclusions.

As a matter of fact, the concept of dual-stage is crucial because it is what allows fast dynamics to be obtained on the DC power control through the corresponding current control. It also explains that MMCs simultaneously combine the benefits of both VSCs and CSCs. Furthermore, it enables MMCs to function as a buffer between two power flows that are controllable independently, what is very useful when it comes to interfacing sources whose total instantaneous powers are not constant (single-phase or unbalanced systems, etc.).

Besides, the notion of independence between the phase-legs is also essential because it is what gives MMCs their excellent tolerance to the operation under unbalanced grid conditions, but is also what complicates their operation at low and variable frequencies (such as in drives) and makes their design relatively complex.

Together, these two properties explain several exclusive features of MMCs. In the end, although describing known mechanisms, this novel way of interpreting the operation of MMCs is therefore most interesting for its ability to explain many of the specificities of this converter family and to describe intuitively their natural behavior. Moreover, it should be noted that these comments represent partial conclusions only, since all the benefits related to control design have not been addressed yet. The latter will be the subject of Chapter 3.

2.7.3 FUTURE WORK

As a matter of fact, several features of the MMCs' operation remain incompletely described in the proposed EMR, an example of which is given by the relation between the zero-sequence line-side EMF and the vertical and horizontal balancing, which remains entirely hidden. Indeed, the presented three-phase EMRs already attempted to make a step towards a better illustration of these mechanisms, showing that the corresponding EMF is related to some degree of freedom, since the corresponding power source is conditioned by $I_{L,\emptyset}=\emptyset$ (for instance, see Fig. 42). However, despite these efforts, no solution was found to truly illustrate how these quantities are interacting with the arm-level balancing nor how they can be used during control design.

To this end, a possible approach would be to exploit the elegant mathematical formulations presented by Kolb and Kammerer in [125]. Eventually, this could open a door to a better interpretation of the special modes of operation such as those that are used in drives.

3 INVERSION-BASED CONTROL DESIGN

Abstract – Based upon the functional representations of Chapter 2, this chapter uses the inversion-based control design methodology that goes along with EMR in order to construct the control schemes of several MMC topologies. Setting a particular focus on the systematic nature of the design methodology, the presented schemes offer an improved transparency and genericity over existing results, while offering state-of-the-art capabilities and performance.

3.1 BACKGROUND

Closed-loop automation systems have long been designed and tuned using frequency response techniques or empirical rules-of-thumb. In contrast, with model-based control design techniques, the control scheme and parameters are essentially derived through the inversion of a *model of the system*. Hence, the necessary commands are directly determined using the mathematical inverse of the system, as illustrated in Fig. 51:

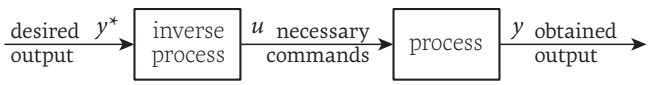


Fig. 51. Basic principle of the model-based (or inversion-based) control design.

Being given that such an open-loop control scheme cannot achieve an ideal result in practice, various closed-loop approaches can be defined in order to reach a close-to-ideal behavior.[1] Additionally, apart from their potentially excellent performance, model-based control schemes provide further benefits:

- *Reproducibility:* Suitable control schemes and controller parameters can be deduced in a straightforward and systematic manner. Besides, thanks to a functional orientation, they can be easily reused and adapted to similar systems.
- *Transparency:* The control objectives (namely the definition of the desired outputs, related to strategical choices) are clearly separated from the implementation issues (i.e. how to guarantee that the control objectives are reached). Indirectly, this also enforces the sanity of the derived control scheme.

Practically, model based design can be applied to mono- or multi-variable systems. The state-space formalism can typically be used to induce model-based multivariable control schemes. Alternatively, EMR is typically meant to construct decoupled cascaded control schemes, provided that the inner loop interactions can be appropriately separated, but to which objective EMR can also help. The latter objective remaining a challenge in to the control of the summed capacitor voltages, it also constitutes an important motivation for the use of EMR in the present work.

1. Practically mainly limited by the performance of the measurement and control hardware.

3.2 CONVENTIONAL CONTROL METHODS FOR MMCS

A direct and interesting consequence of the possible decoupling of the bus- and line-side magnitudes described earlier is that the overall MMC control problem can be split into two distinct subtopics:

- The control of the *line currents*, which poses essentially topology-independent concerns. Indeed, their reference shapes and setpoints are generally set by external constraints (as for any VSC topology) and offer no MMC-specific degree of freedom. This control sub-problem is therefore not part of the present work as conventional techniques and existing knowledge inherently apply.
- The control of the *bus-side currents,* which possesses additional degrees of freedom compared to conventional topologies. This second sub-problem is thus particularly important and is the main topic of this chapter.

The difficulties in the study of this second problem are mainly coming from the fact that the mentioned degrees of freedom are combining different issues an key benefits:

- First of all, a possible minimization of the required capacitive energy embedded in the submodules, owing to the possible shaping of the submodule capacitor voltages through the relevant instantaneous power flows (see §3.2.2). However, the corresponding shapes of the partial bus current are also related to variable RMS and peak current values, what implies variable silicon area requirements and losses. A simple example of this is provided by the comparison of Fig. 53 and Fig. 54 in the next pages, which depict two different and rather opposed voltage control strategies. One immediately notices that the corresponding currents are not the same, neither are the shapes of the summed capacitors voltages, nor the associated capacitive energy storage requirements (Fig. 54 features a significantly lower total peak-to-peak voltage ripple).
- Secondly, attractive and unique capabilities in special modes of operation, such as under unbalanced grid conditions or with very low output frequencies. However, the practical control implementation is made relatively complex due to the numerous spectral components present on all converter quantities (see §2.6). Besides, the arm-level balancing problem is far from being trivial since – as §3.3.2 will demonstrate – the vertical and horizontal balancing cannot be entirely decoupled.

Consequently, an intense research and development activity can be observed on the MMC control design in general, which the following paragraphs attempt to briefly overview.

3.2.1 CONTROL OF THE BUS-SIDE CURRENTS

3.2.1.1 CURRENT CONTROL IMPLEMENTATION TECHNIQUES

In the very first publications [34]-[38], no arm inductor was present and thereby no means were available to control the circulating currents either. Nevertheless, since the introduction of these elements [44], [54], various control schemes have been proposed:

a) No active control

In case no attempt is made to actively control the shape of the circulating currents, the latter are solely defined by the values of the passives (arm, bus and line inductors, submodules capacitors, etc.). In particular, large inductors values can be chosen

towards such a purpose [117], [111].[2] Exemplarily, Fig. 52 illustrates the shape of the arm currents for different values of arm inductances, using a purely open-loop modulation (direct modulation) approach in a passive R-L AC load:

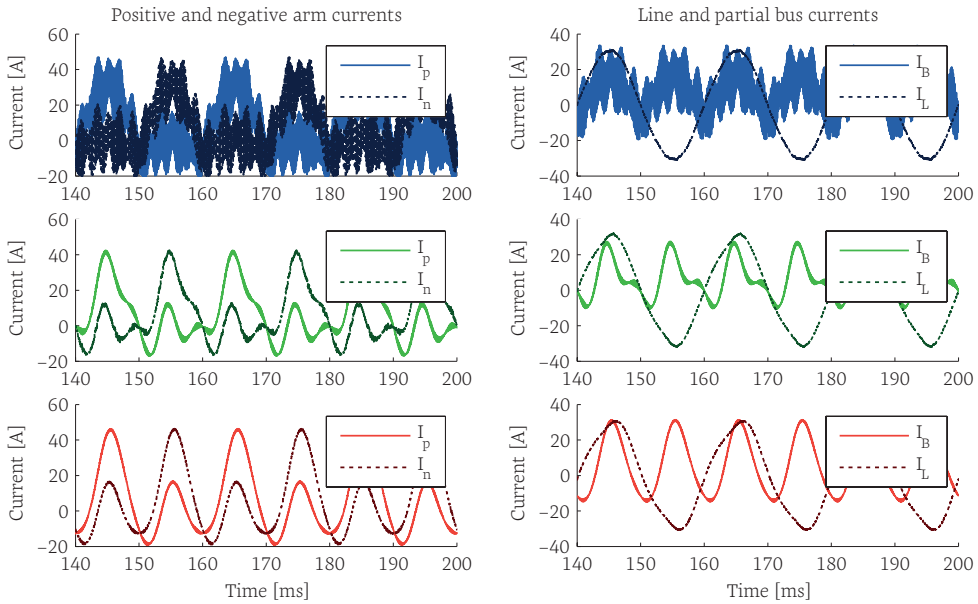


Fig. 52. Typical shapes of the arm and partial bus currents with different values of arm inductances. blue: L_{arm}=*0.1 mH* (0.3% p.u.), green: L_{arm}=*0.1 mH* (3.8% p.u.), red: L_{arm}=*2.5 mH* (7.9% p.u.).

b) Open-loop control

Using a concept introduced in [90], engineers from KTH proposed in [121] an approach that achieves a satisfying control of the partial bus currents in a feedforward manner. In fact, with respect to equation (22), page 42, while E^*_L is generated by a conventional current controller, E^*_B is produced in a open-loop fashion by the utilized energy estimator. As proposed, this approach can be combined with a trick that elegantly circumvents the voltage/energy control problem using the same estimators (see §3.2.2.1).

As extensively reported by its authors, this approach offers satisfying performance and stability [93], [122] in most cases, although it was also recently reported in [123] that the addition of a feedback terms significantly improves the overall control dynamics.

c) Closed-loop control

The closed-loop current control was first shown by Hagiwara [42]-[46], using a similar approach to what existed previously with CHB topologies. This approach directly controls the arm currents (in a *p/n* reference frame), rather than the equivalent decoupled quantities (*B/L* quantities). The proposed implementation also offers simple means towards the implementation of superposed voltage control loops and directly integrates the cell-level balancing mechanisms [41]-[42]. That said, surprisingly, the corresponding mechanims seem to have been only applied to Akagi-type modulation methods.

Relatively to Marquardt-type modulation approaches (see §1.3.5 *a)*)., Oates [45] and Winkelnkemper [72], [73] first suggested that the circulating currents should be explic-

2. Alternatively, references [56],[118] make use of an LC filter placed around the mid-point of each phase-leg in order to passively damp the second-order harmonics present in the partial bus currents. However, no information has been disclosed about the impact of this additional element on the overall performance, stability, efficiency, etc.

itly controlled in a closed-loop manner.[3] Since then, numerous authors have published on the implementation of various types of current controllers. Among them, major contributions have been provided by Münch [94] using a multivariable control approach (hence also including the line-side current control) or by Kolb and Kammerer [74],[125] using simple PI controllers in the $\alpha\beta\emptyset$ reference frame.

Alternatively, the use of a single negative-sequence reference frame rotating at the double of the line frequency has been reported by Tu and Xu [119].[4] Unfortunately, this approach is relatively inconvenient when associated with a superposed closed-loop voltage control, especially with respect to the vertical balancing. This observation was even the main motivation for Bergna to improve it in [127] using double reference frame techniques [149]-[151] in order to separate the -2ω components related to V^{Σ}_{Σ} (horizontal balancing and total energy control) from the $+1\omega$ components involved in the vertical balancing (V^{Σ}_{Δ}).

Unfortunately, as recently commented in [128], [137], both techniques remain unable to reject the zero-sequence component appearing under unbalanced grid conditions.[5] References [135], [136] therefore suggested to add an additional proportional integral resonant (PIR) controller for that specific purpose. Alternatively, the substitution of the entire CCSC with four PIRs has been proposed in [137]. However, in these three last cases – which nevertheless feature the most comprehensive control implementations so far – the current control is not, strictly speaking, inversion-based, as the number of controllers exceeds the number of controlled state variables.

3.2.1.2 SHAPING OF THE CIRCULATING CURRENTS

Beyond the choice of the control implementation techniques, the choice of the appropriate current reference is also a major issue. Existing research has suggested various usage of the free shaping of the partial bus currents:

a) Plain DC "flat" current

This control objective is often referred to as *circulating current suppression*. It aims to achieve an exchanged power with the bus that is a pure constant within each phase leg (Tu and Xu [119], Dorn et. al. [54]). By doing so, for the DC/3-AC converter under balanced grid conditions, the partial bus currents are typically defined such that:

$$I^{*}_{B,x}(t) = \frac{1}{3} I_{B,tot}(t) \tag{40}$$

This strategy is illustrated in Fig. 53. It allows for simple control implementations such as [119] and can be very convenient in single-phase systems, as shown by Vasiladiotis et. al. [75]. Moreover, it is the control objective that offers the lowest RMS arm current value for a given line current. It is therefore the most attractive strategy from both silicon area and conducting losses perspectives. On the other hand, and more importantly, it is also the worst case in terms of capacitor voltage ripple (and hence required amount of embedded energy), which is maximum. Indeed, in such a case, each phase is responsible for buffering the entire pulsation of its instantaneous power.

3. That said, seeing the waveforms of [54], one can guess that engineers from Siemens had already implemented such a current control for a long time.
4. This approach is commonly referred to as the *Circulating Current Suppressing Controller*.
5. Indeed, rotating reference frame systems are becoming very inconvenient under unbalanced grid conditions, due to the presence of numerous sequences in the partial bus currents, namely -2ω, -1ω, $\emptyset$, $+1\omega$ and $+2\omega$ frequency components [141],[199].

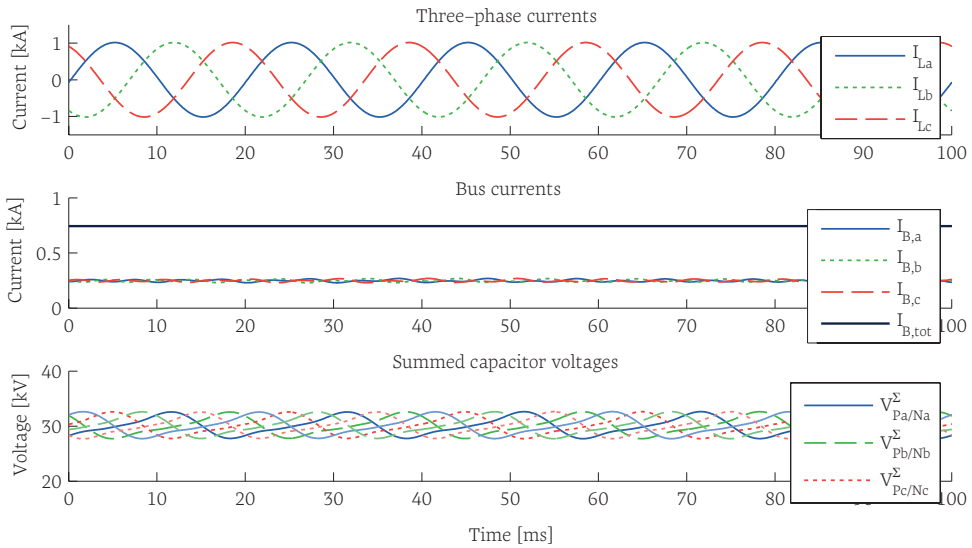


Fig. 53. Typical waveforms when a closed-loop circulating current suppression strategy is employed.[6]

b) DC current with second-order harmonic injection

As first shown by Winkelnkemper [72], the required amount of embedded capacitive energy can be drastically reduced by imposing partial bus currents that contain second-order harmonics that compensates for the double-frequency power pulsation of each phase. Hence, for the DC/3-AC inverter operating under balanced grid conditions, the partial bus currents are defined such that:

$$I^{*}_{B,x}(t) = \frac{1}{3} I_{B,tot}(t) + \frac{v_{L,x}(t) \cdot i_{L,x}(t)}{V_{DC}} \tag{41}$$

where $v_{L,x}(t)$ and $i_{L,x}(t)$ are the line voltages and currents, respectively. Hence, their products yield the instantaneous line-side powers of the corresponding phase-legs. This strategy is illustrated in Fig. 54:

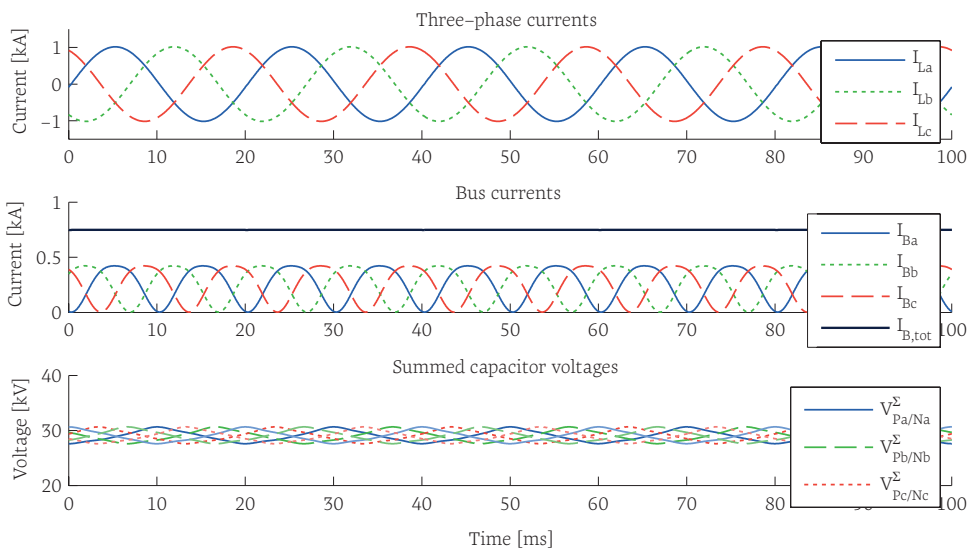


Fig. 54. Typical waveforms when a closed-loop strategy enforces the minimization of the phase-leg energy pulsation. All parameters and operating conditions are identical to those of Fig. 53.

6. More information about the implemented control strategy will be given in §3.4.

Going further, Engel et. al. have shown in [110] that the necessary amount of embedded capacitive energy can be divided by almost three when the partial bus currents are shaped with a combination of second- and fourth-order harmonics, at the cost of an increase of only 5% of the arm current RMS value compared to the "flat" I_B shaping approach of *a)*.[7] Aiming to the same objective, Bergna proposed in [128] a technique based on mathematical optimization that is suitable for online implementation. The approach was later extended in [136] in order to comply with a purely constant DC power objective, what allows for an attractive operation under unbalanced grid conditions (see also §3.2.2.2).

Finally, it is worth noting that in all the above cases, the computation of the spectral content injected in the current reference signals remains essentially parameter-based and open-loop in the sense that no feedback path is present so as to ensure that the desired minimization of the voltage oscillations is actually reached. In turn, computing the current references such that such objectives are enforced is one of the potential roles of the closed-loop voltage control. This however depends on the way the latter is implemented, what is the subject of the next section.

3.2.2 VOLTAGE / ENERGY CONTROL AND BALANCING

The closed-loop control of the summed capacitors voltages was first addressed in the context of MMCs by Akagi et. al. using techniques that already existed for CHB converters and which also encompasses the cell-level balancing [41]-[42]. Alternatively, respectively to Marquardt-type modulation and balancing techniques, the basic principles of the arm-level balancing were first suggested by Antonopoulos et. al. in [90] and alternatively detailed by Münch [94] or Kolb et. al. [125].

Nowadays, various implementations of these original proposals have been developed, but generally converge to the same objectives : *i)* the horizontal and vertical balancing of the summed capacitor voltages as well as *ii)* the mastering of the total energy amount present in the converter (see §2.4.2.1, page 41). Besides, the voltage control algorithms can also made responsible for *iii)* guaranteeing the minimization of the required amount of embedded energy, through the appropriate shaping of the summed capacitor voltages.

Concretely, as shown in §2.6, these objectives are related to the independent control (and shaping) of the common-mode and differential-mode power flows of each phase-leg, what can be achieved by various techniques.

3.2.2.1 VOLTAGE CONTROL IMPLEMENTATION TECHNIQUES

Among the existing control implementation approaches, one can distinguish :

a) The Open-loop control approach

Using a concept first introduced in [90], Angquist et. al. proposed in [121] a simple control approach that is making of estimated values instead of actual measurements as the normalization factors during the computation of the modulation indices. As shown by [93], [122], this forces the summed capacitor voltages to converge to the estimated values, hence also simultaneously serving as reference values.

7. Norrga et.al. [105] reached equivalent results showing that, for a given design, the converter operating area can be significantly extended by using such harmonic injection techniques.

Concretely, equation (42) is simply substituted by eq. (43) during the computation of the modulation indices, such as:

$$m_p = E^*_p \big/ V^\Sigma_p \quad m_n = E^*_n \big/ V^\Sigma_n \tag{42}$$

$$m_p = E^*_p \big/ \hat{V}^\Sigma_p \quad m_n = E^*_n \big/ \hat{V}^\Sigma_n \tag{43}$$

where E^*_p and E^*_n denote the reference EMFs which combine the line-side reference E^*_L and the bus-side reference E^*_B (independently of the fact that E^*_B is generated in a closed-loop manner or not). Overall, the elegance of this approach lies in its simplicity, while guaranteeing controllable – and hence balanced – summed capacitor voltages.

a) Multivariable control approaches

Alternatively, multivariable control approaches have been proposed, such as by Münch et. al. [120], that can simultaneously achieve both the voltage and current control, including the line-side quantities as well. Alternatively, model-predictive control (MPC) approaches have been initiated as well by [129]-[131], but are still facing issues related to the high computational burden implied by the control of a realistic number of cells with attractive prediction horizons.

Furthermore, an original concept introduced by Korn [124] offers a flexible design approach applicable to numerous topologies in order to achieve the arm-level voltage balancing. The proposed methodology can take advantage of all the degrees of freedom present in MMCs. However, the simultaneous alteration of both arm currents and voltages remains relatively unintuitive. Besides, no practical evidence of the performance of this approach has been provided yet.

b) Cascaded control approaches

One of the first and most straightforward cascaded control approaches for MMCs has been presented by Hagiwara et. al. in [42]. This control strategy ideally superposes over the inner current control proposed by the same research team and is well suited for distributed control implementations. As proposed, each arm current reference is directly formed with a component common to both arms (horizontal voltage balancing), a component of differential-mode (vertical voltage balancing) and a contribution from the cell-level voltage balancing. This results in a comprehensive control implementation, but whose control hierarchy remains somehow vaguely layerized, exemplarily due to the way the *current minor loop* is implemented. Besides, as there are no filters or estimators in the corresponding voltage control loops, it is generally not attempted to manipulate the instantaneous power flows and the means to implement ripple shaping strategies remain difficult to identify.

Respectively to Marquardt-type modulation mechanisms, the existing control implementations can be classified into two distinct paradigms:

b).1. Filter-based voltage control with open-loop harmonic currents injection

This first class of approaches essentially disregards the ripple present on the summed capacitor voltages using either filters or estimators. The subordinated current controllers are therefore essentially fed with constant values (in steady-state), to which the appropriate spectral components must be added (see §3.2.1.2). Consequently, the management of the spectral content of the currents and voltages is mainly associated with the current control in a feedforward/open-loop manner.

The developments reported by Kolb and Kammerer [74], [125] or Vasiladiotis [126] are essentially belonging to this category. Alternatively, but using the same philosophy, Münch [120] and Bergna in [128] rely on mathematical optimization techniques in order to directly compute the ideal current shapes as a function of the arm-level balancing problem as well as ripple reduction objectives.

Overall, these approaches can be very effective – including under unbalanced grid conditions – provided that both the utilized filters or estimators and the underlying current control are accurately accounting for all the appearing sequences / spectral components. On the other hand, this type of approach is also inevitably more or less sensitive to model parameters and may result in limited voltage dynamics when used with filters.

b). 2. Full closed-loop voltage control

The second class of approaches was first initiated by Bergna in [127]. As proposed the latter, provided that the V^{Σ}_{Σ} controller is made responsible for guaranteeing a flat voltage (that is a perfectly constant phase-leg energy), this controller will naturally inject the necessary spectral components in the partial bus currents (such as 2nd and 4th order harmonics), enforcing the minimization of the phase-leg energy variation.[8] In the end, thanks to its closed-loop nature, this second class of approach proves to perform better than the first one in terms of the minimization of the capacitive energy requirements [127].

Practically, in its original form [127], this concept is an extension of the decoupled double synchronous frame decomposition of [149]-[151] into $+1\omega$ and -2ω sequences. However, in this specific work, the $dq\emptyset$-based vertical balancing is only actively enforced on the $\emptyset$-axis, the d and q axes being left to natural balancing mechanisms. Consequently, the proposed $dq\emptyset$ voltage control scheme is inoperative under asymmetrical regimes due to the incomplete consideration of the negative- and zero- sequence components.[9]

That said and more generally, both V^{Σ}_{Σ} and V^{Σ}_{Δ} control loops could be fed with any type of references (not necessarily constant values), achieving the necessary energy management with a strictly cascaded control hierarchy. By doing so, it is hence guaranteed that the pursued objectives (typically, the shaping of the voltages / energy variations, related to some optimizations) are actually reached, regardless of parameter variations or imperfections in the implemented estimators, etc. Naturally, this principle can be applied with other control implementations than the DDSRF originally proposed in [127]. However, this also anyway implies that, if optimization objectives exist in terms of current shaping, these objectives must be translated into constraints on the shapes of the summed capacitor voltages. This is indeed one of the main limitations of this second type of approaches, particularly when the operation under asymmetric operating conditions must be considered.

In order to establish a properly constructed cascade in the sense of the inversion-based control design philosophy, this second type of approach appears as the most attractive option and will be privileged along the present chapter. Additionally, combinations of filter-based (as in *b). 1.*) and fast closed loop control (as in *b). 2.*) may of course be imagined and provide satisfying performance with a simplified control implementation.

8. In turn, this control strategy is the one that has been used to produce the results in Fig. 54.
9. See also footnote 5, page 66.

3.2.2.2 CAPACITOR VOLTAGE SHAPING / ENERGY MANAGEMENT

The shaping of the summed capacitor voltages is essentially a strategical concern that involves some possible optimizations. Hence, depending on the operating conditions, various objectives may be pursued:

a) Operation at nominal frequency and under balanced grid conditions

In symmetrical conditions, it is generally possible to freely manipulate any active or reactive power flow on the bus side as long as the corresponding alternating current components are summed so as to disappear on the bus. Given the importance of the potential benefit of such manipulations in terms of capacitor sizing, there is no reason not to minimize the amount of embedded energy, as described in §3.2.1.2 *b)*.

b) Operation under unbalanced grid conditions

Under unbalanced grid conditions, the key issue is that, if the converter is controlled as proposed above in *a)*, the asymmetrical components in the I_{Bj} produce undesirable oscillations on the bus side. In such as case, the MMC is operating as any other VSC and the pulsation of the total AC power is directly transferred to the bus side.

Being given that the controllability of the partial bus currents allows to enforce a purely constant total bus-side power flow, there is no reason not to exploit this benefit. The most recent control techniques for the bus currents have been developed to that specific end (see §3.2.1.1). On the other hand, it also implies that the total instantaneous power difference between both converter sides must be absorbed by the converter itself, desirably in a equally shared manner among the phase-legs.

With these objectives in mind, the optimization-based approach proposed by Bergna in [138] offers attractive results, but remains limited to the shaping of the bus-side instantaneous power flow. On the other hand, whenever possible, the shaping of the line-side power shall probably be used as well, as this can result in reduced total input-to-output power flow differences (and hence minimized energy requirements). On that matter, the very recent works reported by Bergna in [139] and Vasiladiotis et. al. [140], [199] show that various strategies related to instantaneous power theories can provide variable results in terms of capacitors voltage ripple.

c) Operation with very low output frequencies

With low output frequencies, such as during the startup of variable-speed drives, the variation of the arm energy being inversely proportional to the line frequency, excessive capacitor values are required unless the partial bus currents are controlled in a very specific manner.

This particular challenge was first solved by Korn [73] (and later extensively documented by Kolb et. al. [74]) by introducing an AC medium-frequency common-mode voltage between the line terminals. In such a case, the AC power pulsation is modulated (in the signal processing sense of the word) and, its spectral content is therefore shifted to higher frequencies, leading to lower capacitive energy requirements. On the other hand, the downside of this approach is that *i)* it must be possible to freely adjust the zero-sequence AC voltage (what is not always the case) and *ii)* the required blocking voltage on the arms is significantly increased [74]. Besides, some remaining limitations, such as limited torque at low speed, are also motivating constant research in this field [76]-[77].

d) Alternative voltage shaping approaches

Provided that the partial bus currents can carry any *symmetrical* components without impacting the total bus current, Ilves suggested in [129] to control them such that the submodule voltage ripple coincides with its corresponding line voltage. By doing so, the modulation depth can be maximized, leading to theoretical energy requirements as low as 21 kJ/MVA [116]. However, this particular result is related to steady-state considerations only and has not been yet extrapolated to more comprehensive operating conditions.

3.2.3 SUMMARY

Overall, as of today, the closed-loop control of all currents and voltages seems to be widely recognized as beneficial and necessary. However, as the previous sections have illustrated, its implementation is far from being trivial. Indeed, when compared to conventional topologies, MMCs happen to possess more state variables and are capable of supporting unprecedented modes of operation (low frequency mode, constant DC power under severely unbalanced grid conditions, etc.). Both these facts are inevitably inducing a comparatively more complex control implementation. Additionally, strategic considerations related to possible optimizations are also mixing with implementation concerns, what is making the control design even more challenging.

In this context, it can generally be observed that numerous contributions are available on specific topics and with specific objectives but that relatively few holistic approaches are available, leading to only few truly comprehensive control designs approaches :

- The *multivariable approaches* such as used by Münch [94], [120] offer both excellent performances and a systematic control design, although their "blackbox" nature may raise some comments about their somehow perfectible intuitiveness.
- The *open-loop approach* of [121]-[122] reveal to be very effective. On the other hand, it is inevitably bound to the usual benefits and drawbacks of its open-loop nature (less measurements, but some sensitivity to modeling imperfections). Besides, the implementation of the corresponding estimators must be specifically tailored to the operating conditions, what might be uneasy, especially if the latter are evolving over time). More generally, similar limitations also hold for all the techniques in which the shaping of the power flows is achieved in an open-loop manner, based on the current control (typically, such as in [128] as well).
- The *cascaded control implementation* used by Kolb and Kammerer [74], [125] performs well with filters, but hasn't been truly documented with the use of estimators instead. In any case, the operation under asymmetric grid conditions has not been considered yet. Alternatively, Bergna proposed a fast- and fully-closed-loop concept in [127], but using DDSRF-based techniques, which reveal to be rather inconvenient for the control of the bus-side quantities under asymmetric grid conditions, unless non model-based adaptations are made (see §3.2.2.1 *b). 2*).

Thus, all the necessary elements to control design are virtually present. That said, although some room may for potential spot improvements may be perceived, what seems more essential is a way to assess *globally* all these relatively subtle control variants. This is the main motivation for the use of a strict inversion-based control design formalism, first to provide a valuable insight on the existing techniques, but also to offer a systematic approach for the design of cascaded control schemes that

are simultaneously as comprehensive and as properly hierarchized as possible. As a matter of fact, this last objective seems of utmost importance in the perspective to *i)* add a superposed energy management layer on the top of these control algorithms or *ii)* in order to extend the existing knowledge to more exotic topologies (such as the M3C, hexverter, CMMC, resonant DC/DC topologies, etc.).

3.3 CONTROL DESIGN OF INDEPENDENT PHASE-LEGS

In this section, the phase-legs are first analyzed as independent elements in order to introduce the general principles of the inversion-based control design using EMR. The obtained results will be then extended to complete converter systems in §3.4.

3.3.1 CONTROL DESIGN METHOD

The principles of the inversion-based control design using EMR are described in [156]-[157], with additional examples given in [159]-[165]. Their application in the context of MMCs is presented hereafter in a step-by-step manner, using a basic example that focuses on the current control problem only. In subsequent steps, the same method will be applied to the complete control problem (hence including the summed capacitor voltages as well), first on the individual phase-legs in §3.3.2 and second on complete systems in §3.4. Practically, five steps can generally be considered:

a) Defining the tuning path and constraints

The first step consist in selecting and defining the control objectives. In this example, based on the developments of Chapter 2, the control objectives are chosen to be limited to the control of *i)* the partial bus current and *ii)* the line current. Then, choosing which sequence should be used to impact these magnitudes from a given *tuning variable* defines the *tuning path* [160]. In MMC applications, the tuning variables are in any case the modulation indices m_p and m_n or, in transformed coordinates, m_Δ and m_Σ. These tuning paths are shown in Fig. 55, highlighted in light blue and green colors:

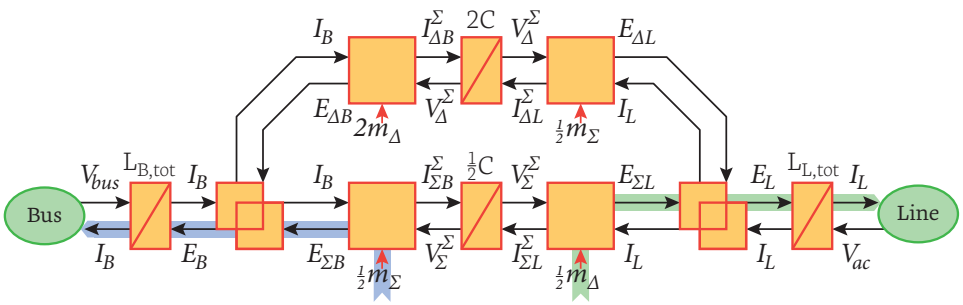


Fig. 55. Tuning paths corresponding to the decoupled control of the line and partial bus currents.

Several constraints must be identified as well, aiming to describe the operating limits of the system. For MMCs, these limits are defined by the capabilities of the arm EMFs. With half-bridge submodules, the arms can only produce positive voltages, i.e:

$$m_p, m_n \in [0;1] \quad \Leftrightarrow \quad m_\Sigma \in [0;2], \quad m_\Delta \in [-1;1] \tag{44}$$

while with full-bridge modules, the absolute limits are:

$$m_p, m_n \in [-1;1] \quad \Leftrightarrow \quad m_\Sigma \in [-2;2], \quad m_\Delta \in [-2;2] \tag{45}$$

b) Deducing the Maximum Control Structure

Based on the inversion rules defined by EMR, all subsystems are inverted along the tuning paths, first considering all variables as measurable. Hence, each quantity that is not involved along the tuning path can be directly compensated or rejected. Following this approach, the *Maximum Control Structure* of Fig. 56 is derived:

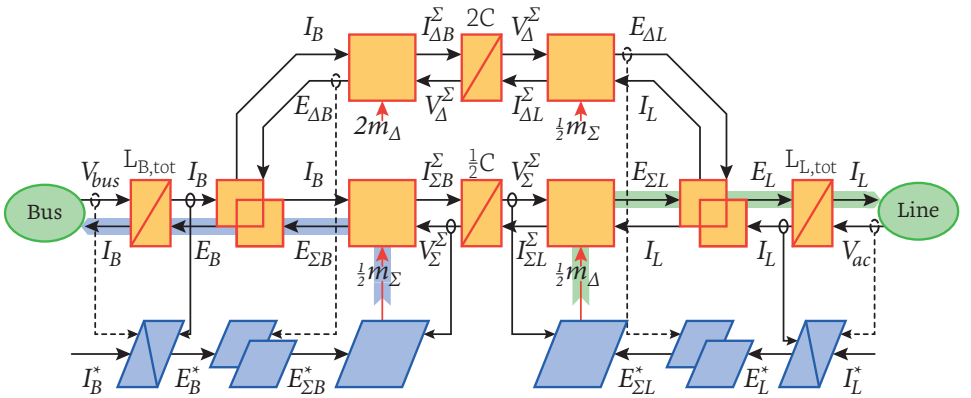


Fig. 56. Maximal Control Structure corresponding to the decoupled current control of a phase-leg.

As shown, each subsystem of the EMR (in orange) has its counterpart on the control side (in blue), which corresponds to a direct inversion of its behavior. Accumulation elements are associated with controllers and the constitutive equations are directly inverted for all other elements. Interestingly, since the two chosen tuning paths are not crossing each other, the corresponding control loops are entirely decoupled.

c) Deducing a Practical Control Structure

Subsequently, hardly- or non-measurable variables can be substituted with estimated values or simply left uncompensated. In the present case, this applies to the perturbation voltages $E_{\Delta L}$ and $E_{\Delta B}$, which can be estimated by inverting the elements of the differential-mode branch. This results in the *Practical Control Structure* of Fig. 57:

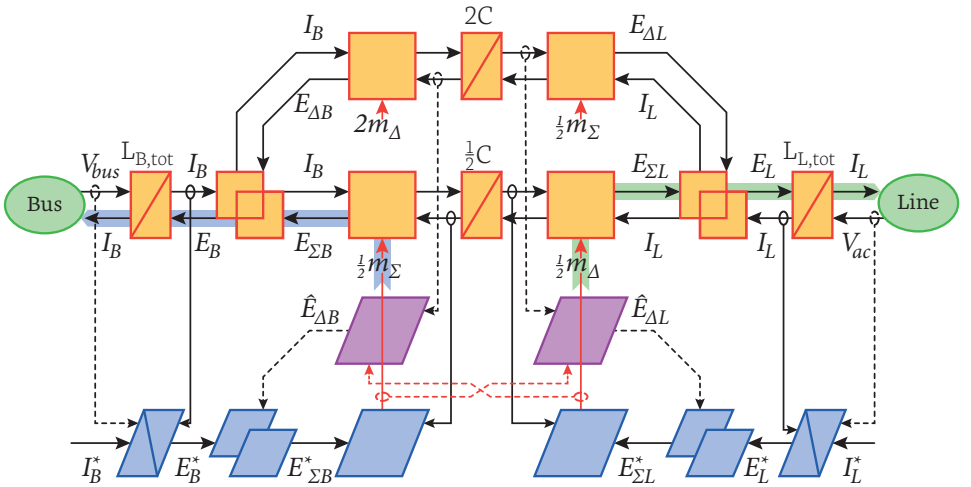


Fig. 57. Practical Control Structure derived from the MCS of Fig. 56. Non-measurable variables have been substituted with estimated quantities.

Of course, with respect to the implementation of the estimator blocks (in purple), further developments could be made to develop estimators that can only rely on easily measurable external quantities. The developments reported by [121], [126] in the con-

text of the *Open-loop voltage control scheme* (see §3.2.2.1) could for instance be used for that particular purpose as well.

d) Choosing the appropriate controller implementation

Once the control loops are defined, appropriate controllers can be chosen, based on the desired dynamics and the expected spectral content of the set values. Naturally, this choice is also related to the selection of an appropriate reference frame. Besides, anticipating on what will be developed in §3.4, several comment can already be made:

- Regarding the *line current* I_L, its alternating nature makes conventional rotating-frame controllers or proportional integral resonant controller [148] very appropriate. In case operation in asymmetric conditions is desired, double synchronous frame (DDSRF) controllers can be used as well [149]-[151]. In case of single-phase implementation, the control in rotating reference frame with fictive-axis emulation [145] is advisable for it excellent active and reactive power controllability.
- Regarding the *partial bus current(s)*, their nature being application-dependent, so is the choice of their controllers:
  - » In case the setvalues are chosen to be purely constant DC quantities, P or PI controllers offer a satisfying performance and a straightforward implementation. Implementations using rotating reference-frame(s) such as the circulating current suppressing controller of [119] or the $+\omega/-2w$ DDSRF implementation of [127] are however generally not advisable unless asymmetric grid conditions can be excluded (see §3.2.1.1 *c*)).
  - » When alternating terms are voluntarily introduced in I_B or multiple sequences are mixing, stationary-frame-based approaches, typically using proportional integral resonant controllers [148], constitute a recommendable approach as they can be relatively robust while offering excellent performances.

e) Establishing the supervisory control and setvalues

Finally, the set values I_L^* and I_B^* must be computed by an additional supervisory block, as shown by Fig. 58:

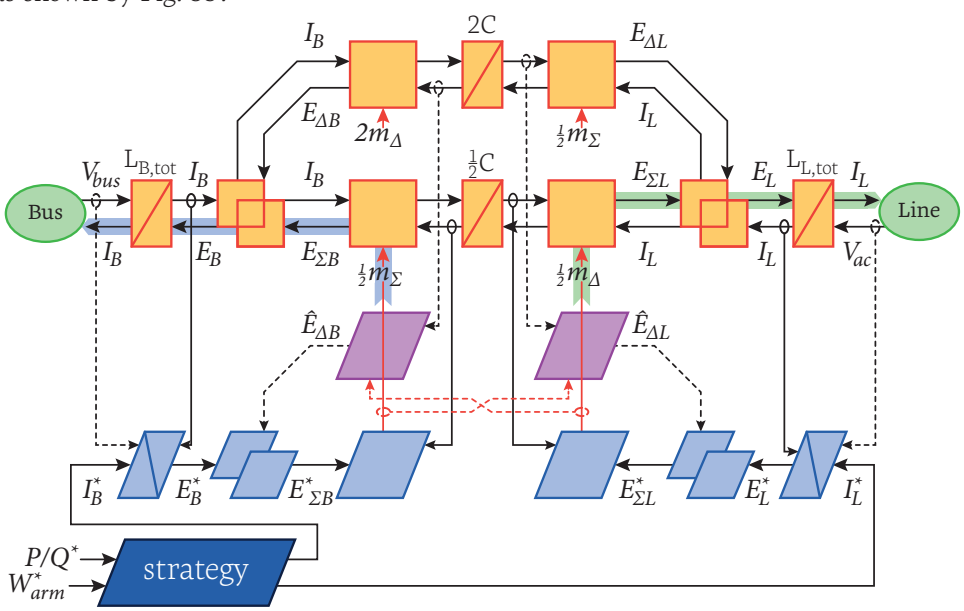


Fig. 58. Practical Control Structure with an additional strategy block (dark blue) managing the capacitor voltages/arm energy levels by appropriately shaping the partial bus currents I_{Bj}.

Importantly, similarly to the selection of the tuning paths, the definition of the set-values is not set by inversion rules but constitutes a deliberate choice that belongs to the designer. This justifies the fact that the corresponding block is considered to be related to supervisory-level or *strategical concerns*.

That said, by stopping there, only the current control is considered and the control of the power flows is rejected to strategical concerns, which must also indirectly account for the control of the summed capacitor voltages. This is the choice that was made here as an introduction, motivated by the fact that the still lacking implementation of the closed voltage control will be developed afterwards.

On the other hand, such an approach may also be considered as a sufficient control design strategy on its own. Indeed, the control of the summed capacitor voltages may be deliberately not included in the model-based part of the control design, but rejected at the strategic level, whose implementation is not necessarily formalized and systematic. In turn, this can already lead to satisfying control schemes, but it is also putting the entire responsibility of both the power flow control and the ripple shaping problems into the definition of the current setvalues (see §3.2.2.1*b*).

This is the general intent of the approaches described by Vasiladiotis [126] and Bergna [128]. Besides, although more indirectly, it is also the philosophy that is implemented through the *Open-loop voltage control* scheme. Indeed, the control design approach of [121] is in turn very similar to Fig. 58, except that *i)* no current controller is present on I_B and that *ii)* the summed capacitor voltages are not measured and rejected, but substituted with estimated values that are directly computed by the strategy block.[10] Hence, in its most basic form, the general philosophy of the open-loop approach corresponds to that depicted in Fig. 59 :

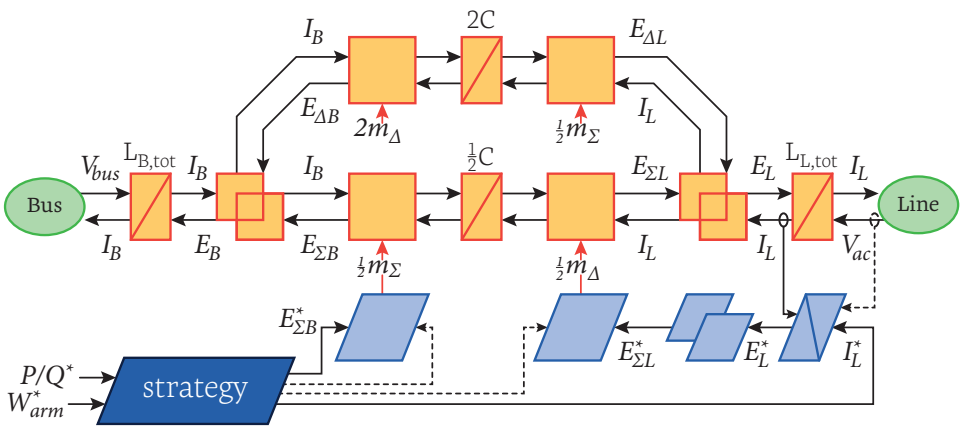


Fig. 59. General principle of the *Open-loop approach* in the light or EMR.[11]

This being said, overall and regardless of the performance of the corresponding control schemes, such approaches may nevertheless not be considered as entirely complete from an inversion-based point of view. This is one of the motivations towards the design of a fully model-based control scheme that accounts for the control of the summed capacitors voltages as well. This is the topic of the following section.

10. Which also simultaneously serve as reference values to which the actual values are deemed to converge [122], [123].

11. The scheme is here represented in Σ/Δ coordinates in order to improve the comparability with the previous schemes. It should be noted however, that the direct use of p/n coordinates is more conventional and probably more convenient as well.

3.3.2 FULL INVERSION-BASED CONTROL DESIGN

In order to achieve the full closed-loop control of the phase-legs, since only two tuning variables are available for each phase-leg, at most two tuning paths must be defined so as to encompass all four state variables. Being given the typical time constants of the latter, such tuning paths are reasonably defined with internal current loops and external voltage loops.

Concretely, several choices can be identified to control each of the state variables corresponding to the summed capacitor voltages:

a) Main branch: common-mode voltage, i.e. total phase-leg energy

In order to control $V^{\Sigma}{}_{\Sigma}$, two types of approaches are possible, namely:

– The global power transfer is controlled using the total bus current, while the intermediary bus voltage is controlled using the line current on the front-end side:

front-end: $m_{\Delta} \rightarrow E_{\Sigma L} \rightarrow E_L \rightarrow I_L \rightarrow I^{\Sigma}{}_{\Sigma L} \rightarrow V^{\Sigma}{}_{\Sigma}$

back-end: $m_{\Sigma} \rightarrow E_{\Sigma B} \rightarrow E_B \rightarrow I_B$

– The global power transfer is controlled from the front-end using the line current, while the back-end converter is responsible for controlling the cascade made of bus current and the fictive intermediate bus voltage:

front-end: $m_{\Delta} \rightarrow E_{\Sigma L} \rightarrow E_L \rightarrow I_L$

back-end: $m_{\Sigma} \rightarrow E_{\Sigma B} \rightarrow E_B \rightarrow I_B \rightarrow I^{\Sigma}{}_{\Sigma B} \rightarrow V^{\Sigma}{}_{\Sigma}$

In turn, these two choices of tuning paths are the same as for any other single-phase double-stage conversion system. Fig. 60 illustrates the second option:

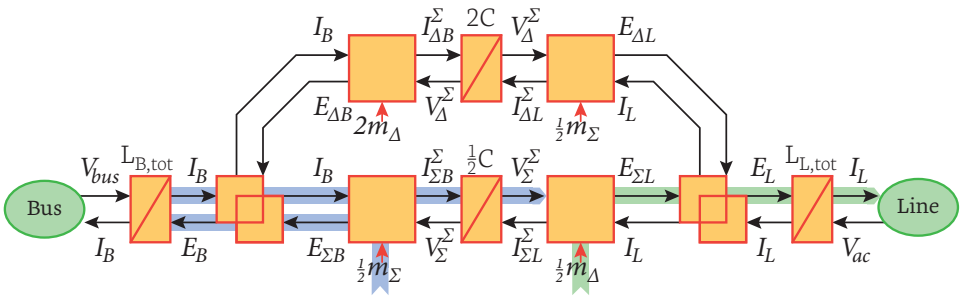


Fig. 60. Possible choice of tuning paths enclosing the control of the total arm energy (i.e. sum of the summed capacitor voltages) as a conventional double-stage conversion system.

As shown by Fig. 60 and in anticipation to the next paragraphs, it is important to note here that both tuning variables have already been used, although the secondary branch containing $V^{\Sigma}{}_{\Delta}$ is still left uncontrolled.

b) Secondary branch: differential-mode voltage, i.e. vertical energy imbalance

Being given that the vertical balancing is indispensable, it is necessary, one way or another, to implement means so as to actively control $V^{\Sigma}{}_{\Delta}$. Concretely, this requires to exploit either the power flows constituted by $I_L \cdot E_{\Delta L}$ on the line side, or $I_B \cdot E_{\Delta B}$ on the bus side. The same options are also revealed by equation (34) in section 2.6.

That said, assuming that the line current is already set by the control of the global active and reactive power transfer, $V^{\Sigma}{}_{\Delta}$ must be necessarily controlled from the bus side, establishing a tuning path such as:

back-end: $m_{\Sigma} \rightarrow E_{\Sigma B} \rightarrow E_B \rightarrow I_B \rightarrow I^{\Sigma}{}_{\Delta B} : f(m_{\Delta}) \rightarrow V^{\Sigma}{}_{\Delta}$

Such a choice of tuning paths is illustrated in Fig. 61:

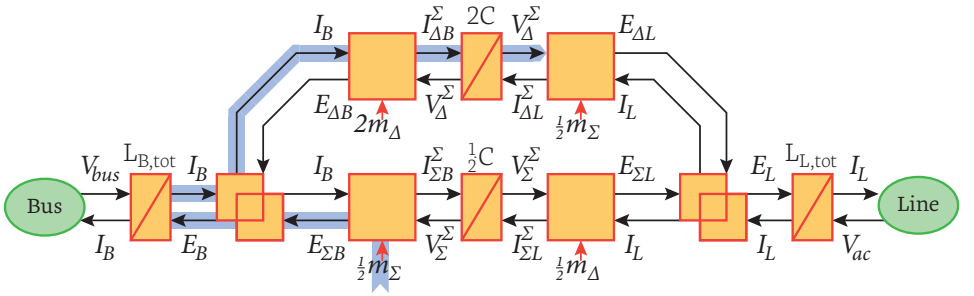


Fig. 61. Alternative choice of tuning paths enclosing the control of the differential arm energy (i.e. difference of the summed capacitor voltages) as a conventional double-stage conversion system.

In the end, both V^Σ_Δ and V^Σ_Σ must be controlled in addition to the line current, forcing to consider all the tuning paths of Fig. 60 and Fig. 61 simultaneously. Hence, three independent control objectives must be achieved with only two tuning variables and, since the two voltage control loops are relying on the same action quantity (the current I_B), the two corresponding controllers are deemed to cohabit.

In practice, one may be tempted to directly superimpose the two implicated tuning paths, hoping that they would not interfere and lead to contradictory behaviors on the current I_B. This approach is depicted in Fig. 62:

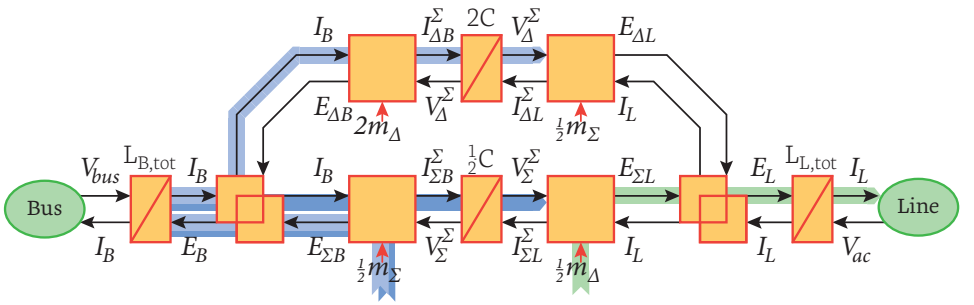


Fig. 62. Possible choice of a complete set of control objectives and tuning paths. A illustrated, the two voltage state variables are simultaneously impacting on the partial bus current I_B.

Fortunately, as previously shown in §2.6, provided that m_Σ and m_Δ possess no common frequencies, the two power flows constituted by $E_B \cdot E_{\Delta B}$ and $I_B \cdot E_{\Sigma B}$ are spectrally separated, and thereby independent *in average values*. Hence, even though the two corresponding tuning paths are relying on a common action variable, the related power flows can be decoupled *in average values*, thanks to distinct spectral contents.

That said, §2.6 also demonstrated that these power flows are directly depending on the application and its operating conditions. In other words, the means to achieve the desired separation of the power flows are not solely depending on the converter structure itself, but rather on the frequency content of the various quantities at stake.

In consequence, the complete closed-loop control design of MMCs *cannot be* uniquely model-based or inversion-based, but must comprise some application-dependent considerations, thereby justifying the various specific studies presented in the sequel.

3.4 CONTROL DESIGN OF MULTI-PHASE CONVERTERS

In the following sections, the control of the three-phase converter structure of Fig. 26 is designed. Depending whether a fixed voltage source is available on the bus side or not, two slightly different choices of tuning paths will be presented: In §3.4.1, a fixed DC voltage is assumed to be guaranteed externally (as in a typical inverter operation) while in §3.4.2, this task must be guaranteed by the converter itself, corresponding to a conventional rectifier-type of operation.

3.4.1 DC/3-AC STIFF BUS VOLTAGE

3.4.1.1 INVERSION-BASED CONTROL STRUCTURE

Assuming that a fixed DC bus voltage is guaranteed, the control objectives chosen and presented in §3.3.2 can be directly extended to the three-phase configuration. Fig. 63 depicts a possible inversion-based control structure derived from the results of §3.3:

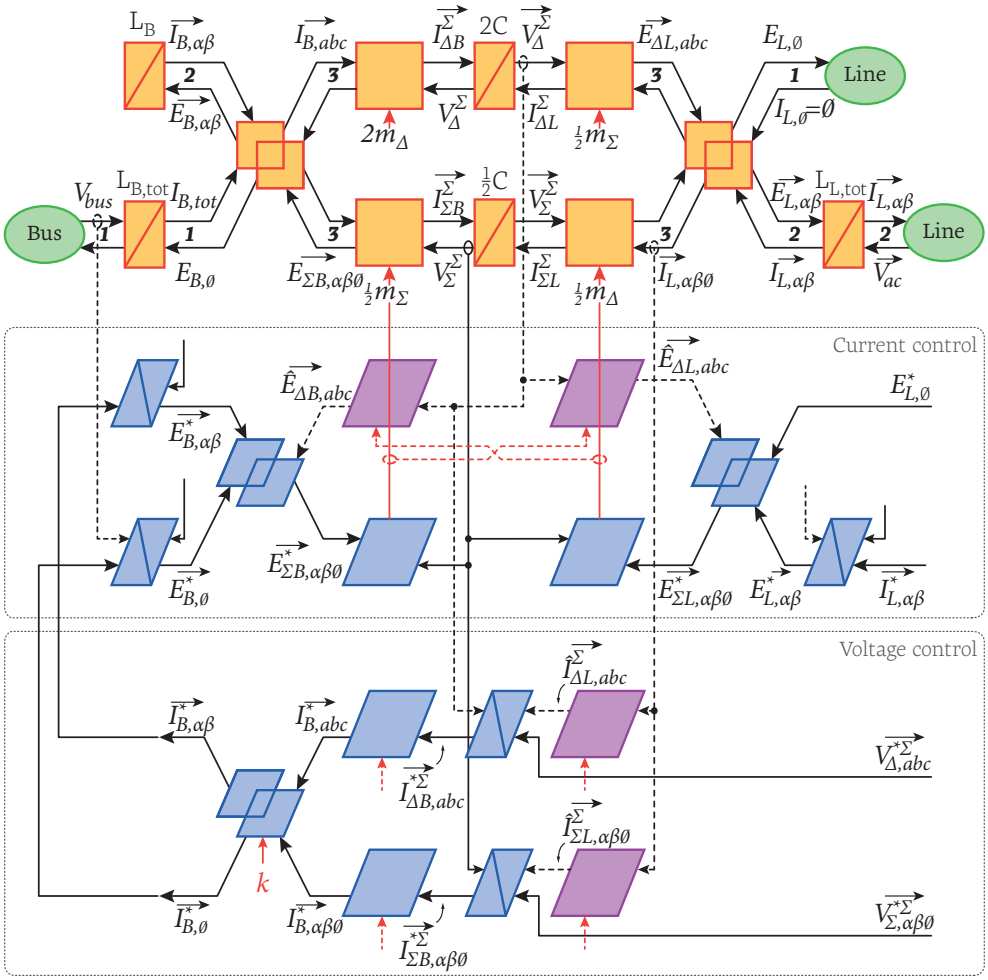


Fig. 63. Complete inversion-based *Practical Control Structure* of the DC/3-AC MMC converter structure according to the tuning paths developed in §3.3.2.

As illustrated, with such an approach, the line currents are controlled in a conventional manner. Besides, both the common-mode and differential-mode phase-leg energies are controlled from the bus side, relying on the subordinated current control.

Several important comments can be made about this control scheme:

- A weighting factor has been introduced during the inversion of the bus-side coupling block. This is imposed by the convergence of the two tuning paths related to the summed capacitor voltages V^{Σ}_{Δ} and V^{Σ}_{Σ}. As such, the rules of inversion clearly indicate that the vertical and horizontal balancing are not and cannot be fully decoupled, and that some trade-off is necessary between the two objectives.[12]
- The inversion of the two bus-side conversion blocks normally involves the division of the current references by $2m_{\Delta}(t)$ and $½m_{\Sigma}(t)$, respectively. However, such an option is not an appropriate choice here, as it prevents the spectral separation of the vertical and horizontal balancing to take place. The rules of inversion must hence be somehow bent here, what will be further discussed in the next subsection.
- As shown here, the design of a purely inversion-based control structure encourages the use of feedforward terms in the V^{Σ}_{Δ} and V^{Σ}_{Σ} voltage controllers.[13] That said, thinking in terms of spectral content, the passage through the corresponding estimation blocks produces the following results *in the present application*:
  - » $I^{\Sigma}_{\Sigma L}(t)$ being the product of $I_L(t) \cdot ½m_{\Delta}(t)$, which are typically two line-frequency terms, its spectral content is mainly constituted by a constant and a double line-frequency component. It yields the common-mode of the instantaneous line-side power when multiplied with V^{Σ}_{Σ}.
  - » $I^{\Sigma\Delta}{}_{L}(t)$ being the product of $I_L(t) \cdot ½m_{\Sigma}(t)$, its spectral content is typically made of the product of a $+\omega$ pulsation with combinations of constant, $+\omega$ and -2ω terms, that is to say numerous harmonics. It yields the differential-mode of the instantaneous line-side power when multiplied with V^{Σ}_{Δ}.

  Consequently, the feedforwarding of these terms in the "rectified" bus-side currents potentially implies significant manipulations of the four fundamental power flows per phase-leg, which may or not be desired depending on the objectives in terms of voltage ripple shaping/energy management. This will be further detailed in the next subsection as well.

3.4.1.2 PRACTICAL CONTROL IMPLEMENTATION

Once the control structure has been established as described in §3.3.1 *d)* and *e)*, it must be completed with a suitable choice of controllers as well as with a supervisory control block responsible for generating the setvalues of $V^{\Sigma}_{\Delta,abc}$, $V^{\Sigma}_{\Sigma,abc}$, $I_{L,\alpha\beta}$ and $E_{L,\emptyset}$.

As a first step, a preliminary control implementation is proposed which aims to provide easy comparison means against existing control techniques. To that end, the design of the supervisory/energy management block is left for future work and filters are used within the voltage control blocks. Besides, the following choices are made for the practical control implementation:

- The line currents are controlled in DDSRF [149]-[151] with conventional *dq*-based current controllers, because it is a very convenient way to handle asymmetric grid conditions. Third-order harmonic voltage injection may be used in $E^{*}_{L,\emptyset}$ in order to increase the possible modulation depth.

12. This weighting factor is generally disregarded in the literature but is instead indirectly revealed through the implemented controller gains and parameters.
13. To the best of the author's knowledge, the use of such blocs has not been reported in the literature, although their attractiveness is made relatively obvious here.

– The partial bus currents are controlled in $\alpha\beta\emptyset$ reference-frame using PIR controllers [148] tuned at 2ω on the $\alpha\beta$ axes and a PI controller on the $\emptyset$-axis. This type of implementation is directly linked to the main spectral components that are expected in these currents (-2ω components on the α and β axes, plain DC value on the $\emptyset$-axis, corresponding to $I_{B,tot}$). Besides, this choice also corresponds to the strict inversion of the chosen set of state variables (see Fig. 63).
– The V^{Σ}_{Δ} voltages are controlled in abc reference-frame, owing to the fact that each phase-leg is inherently independent on that regard. This choice is also motivated by the fact that the DDSRF decomposition used by Bergna [127] is inoperative under asymmetric grid conditions. Additionally, notch filters are used on each axis in order to reject the appearing line-frequency oscillations.[14]
– The V^{Σ}_{Σ} voltages are controlled in $\alpha\beta\emptyset$ reference-frame, because such a choice allows to separate the horizontal balancing problem (the $\alpha\beta$ axes) from the total energy control problem (the $\emptyset$-axis). Additionally, a double-frequency notch filter is used on the $\emptyset$-axis in order not to transmit the total AC power pulsation to the DC side in case of unbalanced grid conditions (see §3.2.2.2). Here again, from an inversion-based control design perspective, the use of filters shall be considered here as a temporary trick to be substituted later with a more appropriate scheme.

Finally, this entire structure is practically implemented as illustrated in Fig. 64:

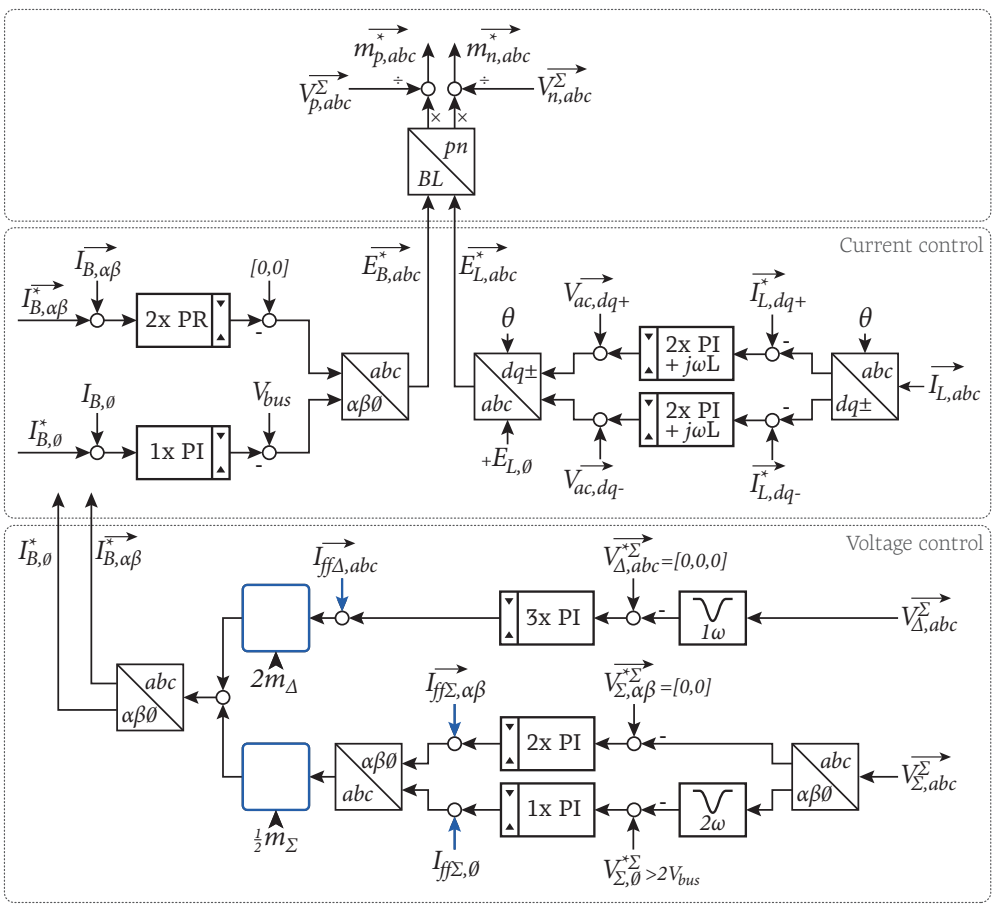


Fig. 64. Practical implementation of the control structure of Fig. 63 without a strategy-level block.

14. Again, this choice bypasses the implementation of a top-level strategy block that would generate the more appropriate voltage references containing the corresponding harmonics.

In turn, the crucial elements in this control scheme are not the controller blocks themselves but rather *i)* the way the conversion blocs are inverted and *ii)* the way the feedforward components are implemented. Both these elements *are marked in blue* on Fig. 64. Indeed, the direct inversion of the two conversion blocks on the bus side would naturally lead to:

$$I_{B,abc} = I^{\Sigma}_{\Delta B,abc} \Big/ 2m_{\Delta,abc} \tag{46}$$

$$I_{B,abc} = I^{\Sigma}_{\Sigma B,abc} \Big/ \tfrac{1}{2} m_{\Sigma,abc} \tag{47}$$

what corresponds to satisfying the exact instantaneous power balance between both sides on the conversion blocks, namely:

$$I_{B,abc} \cdot E_{\Delta B,abc} = I^{\Sigma}_{\Delta B,abc} \cdot V^{\Sigma}_{\Delta} \tag{48}$$

$$I_{B,abc} \cdot E_{\Sigma B,abc} = I^{\Sigma}_{\Sigma B,abc} \cdot V^{\Sigma}_{\Sigma} \tag{49}$$

However, respecting these direct inversions would make both control loops operate up to their full control bandwidth (as fast as possible), leading to conflicting setvalues for $I_{B,abc}$. Additionally, in the light of §2.6, such reference values would not generate the appropriate power flows for the balancing purposes. Consequently, the principles of model inversion are preferably not followed here. Alternatively, the two implicated blocks are rather implemented as follows:

a) Differential-mode branch: vertical balancing

For each phase-leg, equation (46) is substituted with a block that generates current references such that an active power flow is induced by the product $I_B \cdot E_{\Delta B}$. This corresponds to the most natural implementation of the information contained in (36), which showed that the vertical balancing can be achieved through the injection of line-frequency components in the partial bus currents. In practice, as best documented by Münch [120], the current references can be simply computed as in (50):

$$\begin{pmatrix} I_{B,a} \\ I_{B,b} \\ I_{B,c} \end{pmatrix} = \begin{bmatrix} \cos(\theta) & \frac{-1}{\sqrt{3}}\sin(\theta) & \frac{+1}{\sqrt{3}}\sin(\theta) \\ \frac{+1}{\sqrt{3}}\sin(\theta-\frac{2\pi}{3}) & \cos(\theta-\frac{2\pi}{3}) & \frac{-1}{\sqrt{3}}\sin(\theta-\frac{2\pi}{3}) \\ \frac{-1}{\sqrt{3}}\sin(\theta+\frac{2\pi}{3}) & \frac{+1}{\sqrt{3}}\sin(\theta+\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \end{bmatrix} \begin{pmatrix} I^{\Sigma}_{\Delta B,a} \\ I^{\Sigma}_{\Delta B,b} \\ I^{\Sigma}_{\Delta B,c} \end{pmatrix} \tag{50}$$

Using this approach, the diagonal terms of this matrix are responsible for producing the necessary active power flows, while the non-diagonal terms are injecting quadrature currents (i.e. reactive power flows) such that the partial bus currents are guaranteed to vanish when forming the total bus current.[15,16]

b) Common-mode branch: horizontal balancing and total energy control

Following the same principle, the product $I_B \cdot E_{\Sigma B}$ must be defined such that is generates an active power flow, what is the direct consequence of the information contained in (37). However, unlike for the differential-mode power flow, this block be kept close to the strict inversion, owing to the fact that it involves essentially DC quantities (the instantaneous power flow is identically equal to the active power flow). Nevertheless, in order to avoid any potential algebraic loops in the control algorithm, $m_{\Sigma,abc}$ can be estimated using measurements only, such as in (51):

15. That is, that the balancing currents are not inducing any oscillations on the total bus current.
16. It is worth noting here as an aside that this liberty taken with the strict inversion is in turn very similar to what is commonly implemented in any conventional rectifier when the DC bus current reference is transformed into a *d*-axis current as to induce an active power flow on its AC side. Section 3.5.2 will further comment this observation.

$$\begin{pmatrix} I_{B,a} \\ I_{B,b} \\ I_{B,c} \end{pmatrix} = \frac{1}{V_{bus}} \begin{bmatrix} V^{\Sigma}_{\Sigma,a} & 0 & 0 \\ 0 & V^{\Sigma}_{\Sigma,b} & 0 \\ 0 & 0 & V^{\Sigma}_{\Sigma,c} \end{bmatrix} \begin{pmatrix} I^{\Sigma}_{\Sigma B,a} \\ I^{\Sigma}_{\Sigma B,b} \\ I^{\Sigma}_{\Sigma B,c} \end{pmatrix} \tag{51}$$

Finally, the feedforward terms must also be edited accordingly. Indeed, as widely acknowledged in the literature and well illustrated by Fig. 48 and Fig. 49, the spectral content of the bus- and line-side power flows can obviously not be identical in *instantaneous values*.

Therefore, as the matching of the instantaneous power flows is not a desirable objective, the choice of the feedforward quantities is also subject to some necessary distance from the purely inversion-based control structure. Concretely, the "rectified" line-side currents estimated by $\hat{I}^{\Sigma}_{\Delta L,abc}$ and $\hat{I}^{\Sigma}_{\Sigma L,abc}$ on Fig. 63 may advantageously not be directly feedforwarded to the bus side, as it depends on the chosen energy management strategy, i.e. on the desired shaping of the summed capacitor voltages.

Hence, the following choices are proposed for the present application :

a) Differential-mode branch : vertical balancing

Since the oscillation of the differential-mode power transfer is a desirable phenomenon, the terms $\hat{I}^{\Sigma}_{\Delta L,abc}$ affecting the differential-mode energy flows are completely disregarded. This results in a modified feedforward term, defined by :

$$\vec{I}_{ff\Delta,abc} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix} \tag{52}$$

b) Common-mode branch : horizontal balancing and total energy control

In order to achieve a purely constant leg-energy (i.e. flat V^{Σ}_{Σ} voltage) on the α and β axes (see Fig. 54, §3.2.1.2), the double-frequency power pulsation are entirely reported to the bus side through the complete forwarding of $\hat{I}^{\Sigma}_{\Sigma L,\alpha\beta}$. On the other hand, in order not the transfer to the bus side the total power pulsation appearing under unbalanced grid conditions (see §3.2.1.2), the oscillating terms present on the $\emptyset$-axis are filtered out using a notch filter. This gives :

$$\vec{I}_{ff\Sigma,\alpha\beta} = \underset{abc\mapsto\alpha\beta}{\mathbf{T}} \vec{m}_{\Delta,abc} \circ \vec{I}_{L,abc} \qquad \vec{I}_{ff\Sigma,0} = \frac{s^2+\omega_0^2}{s^2+2\zeta\omega_0 s+\omega_0^2} \underset{abc\mapsto 0}{\mathbf{T}} \vec{m}_{\Delta,abc} \circ \vec{I}_{L,abc} \tag{53}$$

where $\circ$ is the entry-wise or "element-by-element" product.

Overall, these choices imply a mix between the fast closed-loop control originally proposed by Bergna [127] and filter-based voltage control techniques. Indeed :

- The summed capacitor voltages are controlled with a fast closed-loop control on the α and β axes, using the same concept as in [127], but enhanced by the introduction of the feedforward terms and avoiding the unsatisfying DDSRF-based control implementation. This can be fast and enforces some minimization of the embedded energy as the generated current components are guaranteed to vanish when forming the total bus current (owing to the use of (50)).
- In contrast, the $\emptyset$-axis of the summed capacitor voltages (the total energy) is implemented in order to produce a smooth total bus current and hence, buffer the total power flow oscillations internally, when necessary. This justifies here the use of the double-frequency notch filter.

In consequence to these choices, the following comments can be made:

– The general structure of the control scheme obtained here using model inversion techniques is in turn very similar to what already existed in the most comprehensive cascaded control implementations. Two additional informations have nevertheless been brought by the employed formalism:
  » There is necessarily a trade-off between the vertical and horizontal balancing objectives, what is here illustrated by the presence of a weighting factor.
  » Model inversion suggests that the line-side instantaneous power flows should be used as a feedforward contribution to the bus side, unless the pursued energy management objectives require otherwise.
– The key of the MMC control design is most certainly related to the way the bus-side conversion elements are implemented (the two blue blocks on Fig. 64), which are preferably not implemented by following strict inversion rules, but rather such that spectrally separated power flows are generated. Here again, this is similar to existing results, except that eq. (51) is generally disregarded in the literature.

3.4.1.3 SIMULATION RESULTS

In order to validate the effectiveness of the presented control scheme, simulations are run using identical assumptions as in §2.5.3, but applied to a full-scale converter model. The employed system parameters are given in Table 3:

Nominal power	P	*20 MVA*	*Bus voltage*	V_{bus}	$28\,kV_{DC}$
Line voltage	V_{ac}	*20 kV (rms)*	*Bus-side inductance*	L_{bus}	*0.1 mH (ESR= 50 mΩ)*
Line current	I_L	*600 A (rms)*	*Line-side inductance*	L_{ac}	*1.0 mH (ESR=20 mΩ)*
Number of cells per arm	N	*13*	*Total arm inductance*	L	*1.5 mH*
Submodule capacitance	C_{SM}	*2.8 mF (ESR=10 mΩ)*	*Mutual arm inductance*	M	*neglected*
App. switching frequency	f_{SW}	*10 kHz*	*Total arm resistance*	R	*neglected (see R_{SM})*

Table 3. Simulation parameters corresponding to a 20 kV / 20MVA grid-tied converter.

Several results are subsequently depicted and commented:

a) Closed-loop voltage control performance

The effectiveness of the implemented control scheme is first demonstrated in Fig. 65, which illustrates the typical performance achieved with the control of Fig. 63 when two different types of step transients are imposed to V^{Σ}_{Δ} and V^{Σ}_{Σ}:

– Between approximately $t = 50\,ms$ and $t = 180\,ms$, a global increase of the phase-leg energies is required through a step of V^{Σ}_{Σ} on its $\emptyset$-axis. As it can be seen, the implemented choice of tuning paths implies that the total bus current bears the corresponding transient, while the line-side quantities remain unaffected. Importantly, as this step impacts on the vertical balance as well, some couplings are visibly present between the V^{Σ}_{Σ} and the V^{Σ}_{Δ} voltages, but which remain satisfactorily damped.
– Between approximately $t = 320\,ms$ and $t = 500\,ms$, vertical imbalances are voluntarily imposed through the corresponding steps on $V^{\Sigma}_{\Delta,a}$ and $V^{\Sigma}_{\Delta,c}$. Here as well, some couplings are visible with the V^{Σ}_{Σ} voltages, but which remain largely acceptable. Besides, both the line currents and the total bus current remain unaffected, owing to the use of purely circulating current components enforced by the quadrature currents injection presented in eq. (50).

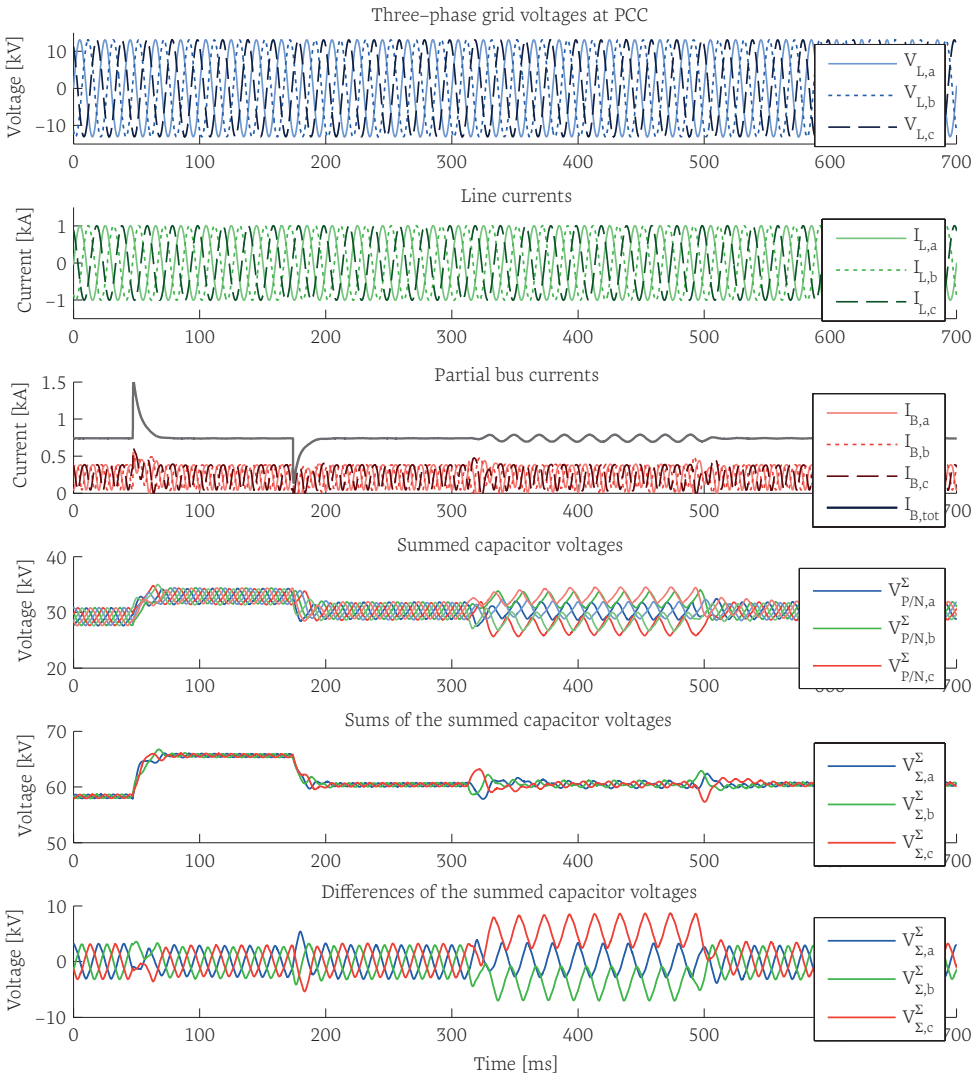


Fig. 65. Typical tracking performance of the closed-loop control as implemented in Fig. 64 and detailed in the previous paragraphs.

b) Operation under unbalanced grid conditions

Owing to its comprehensive design, the presented control scheme is also directly usable under strongly degraded grid conditions. Fig. 66 illustrates the typical perturbation rejection performance of the presented control scheme under a phase-to-neutral fault.[17] The achieved fault ride-through capability is giving rise to several comments:

– The DDSRF-based line current control succeeds to maintain symmetric currents under unbalanced grid conditions, which is the considered objective here.[18]

– As expected, the filtering of the double line-frequency oscillations on the Ø-axis of V^{Σ}_{Σ} and the sole feedforwarding of the average of the total AC power forces the converter to buffer the instantaneous power pulsation internally, what can be clearly seen on the V^{Σ}_{Σ} voltages waveforms.

17. This correspond to the harshest possible asymmetry, equivalent to a line-to-line fault on the primary transformer side (in case the latter is present).

18. Of course, other alternatives, such as active or reactive power oscillations compensation could be considered as well.

– Respectively to the differential-mode power flows (vertical balancing), the faulty phase-leg suffers from increased oscillations compared to the other phases. This is consequent to the choice of the symmetric currents imposition on the line side. As shown by Vasiladiotis et. al. in [140], instantaneous reactive power compensation through negative-sequence currents injection would perform better on that regard.

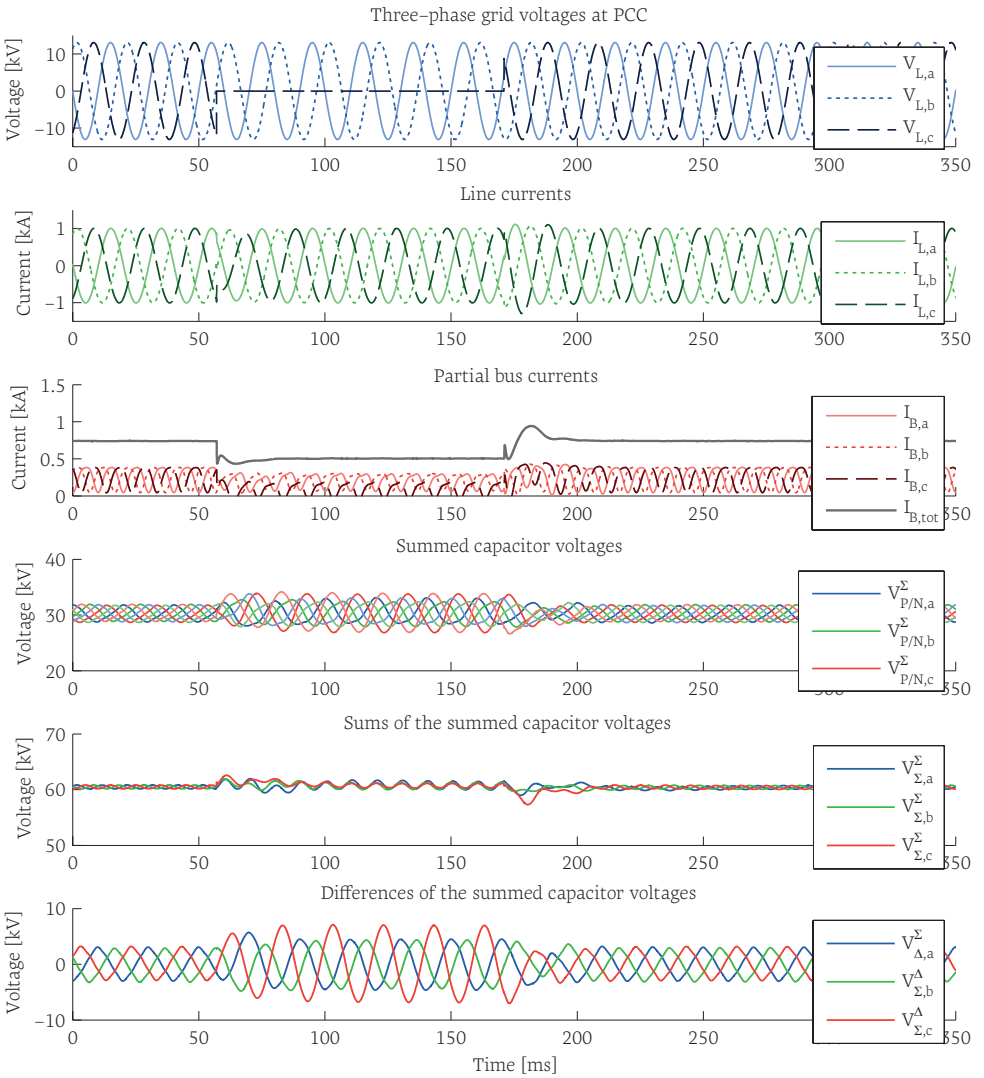


Fig. 66. Typical performance of the closed-loop control of Fig. 64 under a single phase-to-neutral fault.

These results shall be compared to those of Fig. 67 and Fig. 68, which correspond to the same control structure, but in which the implemented filters and feedforwarded currents have been modified as follows:

– Fig. 67 shows the results obtained without any filtering on the $\emptyset$-axis of $V^{\Sigma}{}_{\Sigma}$ (measurement of $V^{\Sigma}{}_{\Sigma,\emptyset}$ and feedforwarded current $I_{ff\Sigma,\emptyset}$).
– Fig. 68 depicts the particular results obtained when both the common-mode and differential-mode power flows are directly fed from the line side to the bus side using the complete feedforward terms $I_{ff\Delta} = \hat{I}^{\Sigma}{}_{\Delta L}$ and $I_{ff\Sigma} = \hat{I}^{\Sigma}{}_{\Sigma L}$.

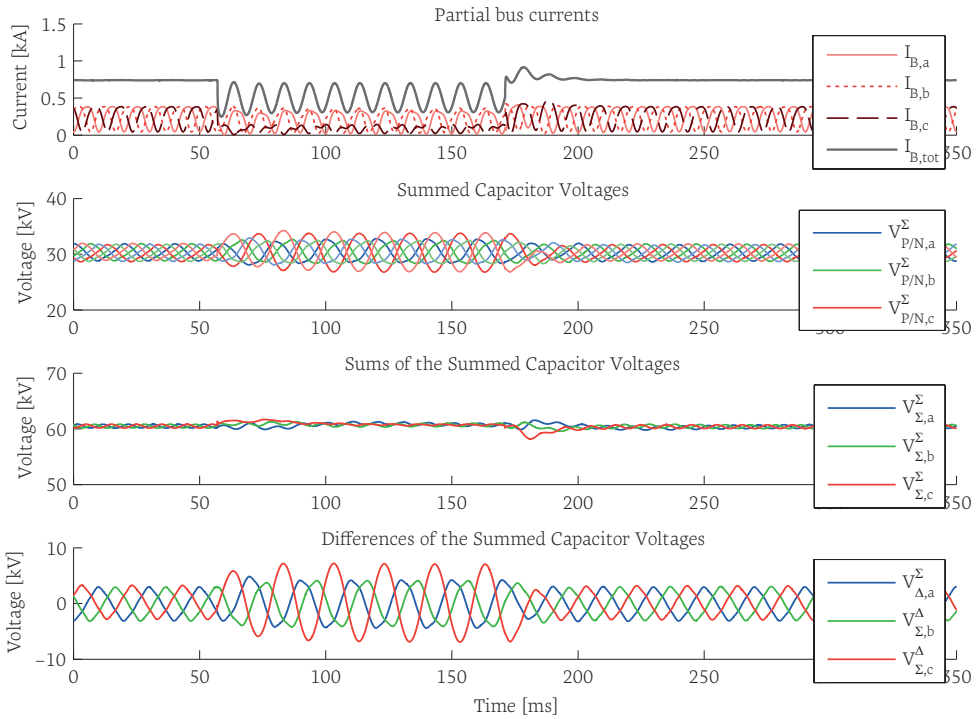


Fig. 67. Typical results in case the total instantaneous AC power is not buffered by the converter but directly transmitted to the DC side.[19]

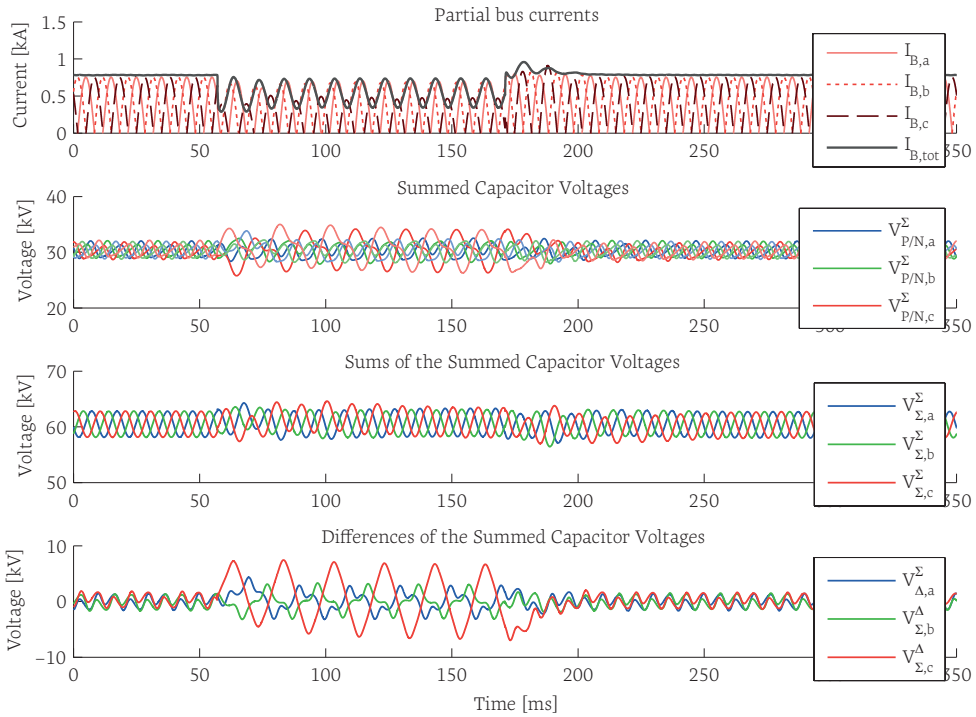


Fig. 68. Typical results when the line-side power flows are totally feedforwarded to the bus side.[56]

19. The line-side voltages and currents are not shown here as they remain strictly identical to those of Fig. 66.

Interestingly, when compared to Fig. 66, these last two simulations illustrate that significant differences can be induced by simply modifying the non model-based part of the design, namely the management of the spectral content:

- In Fig. 67, without filtering on measurement of $V^{\Sigma}_{\Sigma,\emptyset}$ and the complete feedforwarding of $I_{ff\Sigma,\emptyset}$, almost perfectly constant phase-leg energies are obtained (see third row), even in case of asymmetric grid conditions, what is completely rejecting the oscillations of the total AC power to the DC side. This behavior is absolutely normal for a conventional VSC but is a clearly unattractive control strategy for MMCs as it does not exploit their unique capability to absorb these oscillations.
- In Fig. 68, including the complete feedforwarding of the differential-mode terms, lower differential-mode power oscillations are obtained (at least in balanced conditions), but which are folding back to the common-mode due to the use of (47). Globally, this leads to a less attractive strategy in terms of embedded energy requirements (the total ripple is globally larger than in Fig. 66).

Overall, despite the use of filters as a shortcut to the implementation of a comprehensive strategy-level block, these results show that such a relatively simple control implementation can provide satisfying performance with various strategical objectives, owing to a sane control structure and implementation.

3.4.2 DC/3-AC WITH UNCONTROLLED BUS VOLTAGE

3.4.2.1 CHOICE OF THE CONTROL OBJECTIVES

In case the DC bus voltage is not defined externally as in §3.4.1, but must be controlled by the converter itself (e.g. if the bus-side source is not a stiff voltage source), the control objectives presented in §3.3.2 must be adapted. Compared to Fig. 64, this results in a globally swapped choice of control objectives and tuning paths, illustrated in Fig. 69:

- The $\emptyset$-axis of the V^{Σ}_{Σ} voltages (i.e. the total converter energy) is controlled using an active power flow from the line side (in green), as for a conventional rectifier:

  front-end: $m_{\Delta,abc} \rightarrow E_{\Sigma L,abc} \rightarrow E_{L,abc} \rightarrow I_{L,\alpha\beta\emptyset} \rightarrow I^{\Sigma}_{\Sigma L,\emptyset} \rightarrow V^{\Sigma}_{\Sigma,\emptyset}$
- The horizontal and vertical balancing are achieved using the α and β axes of the partial bus currents, i.e. the circulating currents (in blue):

  back-end: $m_{\Sigma,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow E_{\Sigma B,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow E_{B,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow I_{B,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow I^{\Sigma}_{\Sigma L,\alpha\beta} \rightarrow V^{\Sigma}_{\Sigma,\alpha\beta}$

  back-end: $m_{\Sigma,abc}{}^{(5\emptyset Hz)} \rightarrow E_{\Sigma B,abc}{}^{(5\emptyset Hz)} \rightarrow E_{B,abc}{}^{(5\emptyset Hz)} \rightarrow I_{B,abc}{}^{(5\emptyset Hz)} \rightarrow I^{\Sigma}_{\Delta L,abc} \rightarrow V^{\Sigma}_{\Delta,abc}$
- A conventional cascade is implemented on the bus side, regulating the bus voltage V_{bus} using $I_{B,tot}$ which is equivalent to $I_{B,\emptyset}$ (in blue):

  back-end: $m_{\Sigma,\emptyset} \rightarrow E_{\Sigma B,\emptyset} \rightarrow E_{B,\emptyset} \rightarrow I_{B,\emptyset}$ ($\rightarrow V_{bus}$ if necessary)

It is worth noting here that, in case the bus voltage must be controlled with good perturbation rejection performance, it is generally advisable to implement a closed control loop on that quantity as well.

In fact, this augmentation of the corresponding control scheme is naturally induced by the fact that the underlying model is changed. Indeed, since the external bus source is no longer considered as a stiff voltage source, the corresponding state-variable must be added, what obviously corresponds to some DC bus capacitance, as represented by the partial EMR of Fig. 69:

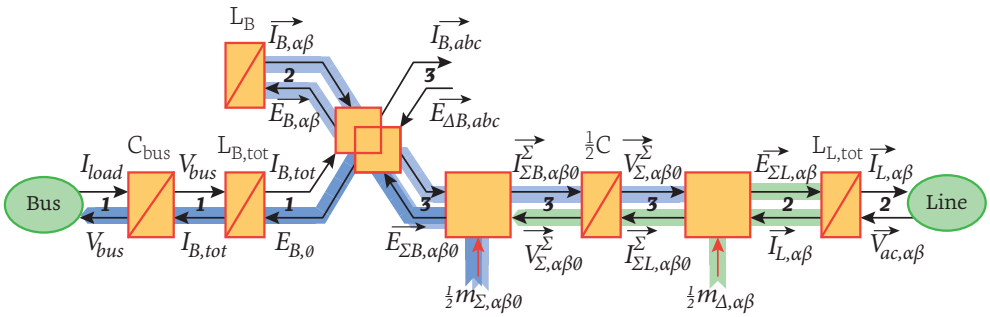


Fig. 69. Partial EMR neglecting the vertical unbalances of the summed capacitor voltages.

Obviously, other tuning paths could be defined as well, such as directly controlling V_{bus} from the line-side active power flow (i.e. $I_{L,d}$) and controlling the intermediary fictive busses from the DC side. However, in the light of Fig. 69, such a choice would be hardly justifiable in the sense of a functional inversion of the system's model.

3.4.2.2 CONTROL IMPLEMENTATION AND SYNTHESIS OF THE SETVALUES

Without re-developing the entire inversion-based control structure out of Fig. 63, a few updates can be made to Fig. 64 in order to account for the modified tuning paths:

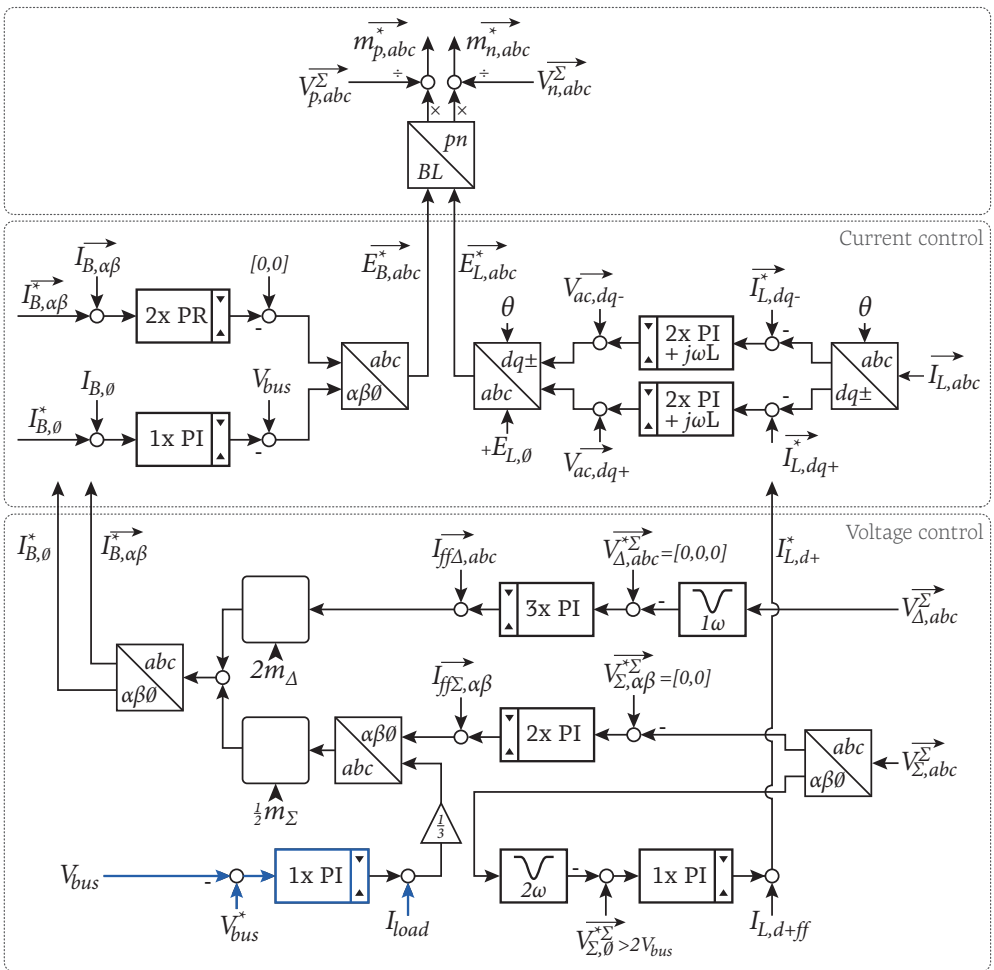


Fig. 70. Possible control implementation with alternative tuning paths, resembling a conventional standalone rectifier operation (without supervisory block).

Compared to the control scheme of Fig. 64, the reversal of the side from which $V^{\Sigma}_{\Sigma,\emptyset}$ is controlled imposes to update the way the feedforward quantities are computed:

– The total AC power is no longer feedforwarded to the back-end through $I_{ff\Sigma,\emptyset}$ but, conversely, I_{Ld+ff} can be computed so as to account for the instantaneous bus-side power in the computation of the positive-sequence AC power.
– In case it is necessary, the bus voltage control loop (in blue) accounts for the load current in the computation of the $I^{\star}_{B,\emptyset}$ reference value.

Fig. 71 illustrates the proper operation of this control scheme using the same parameters as in §3.4.1 and similar reference steps for the summed capacitor voltages. The bus voltage control loop is not implemented.

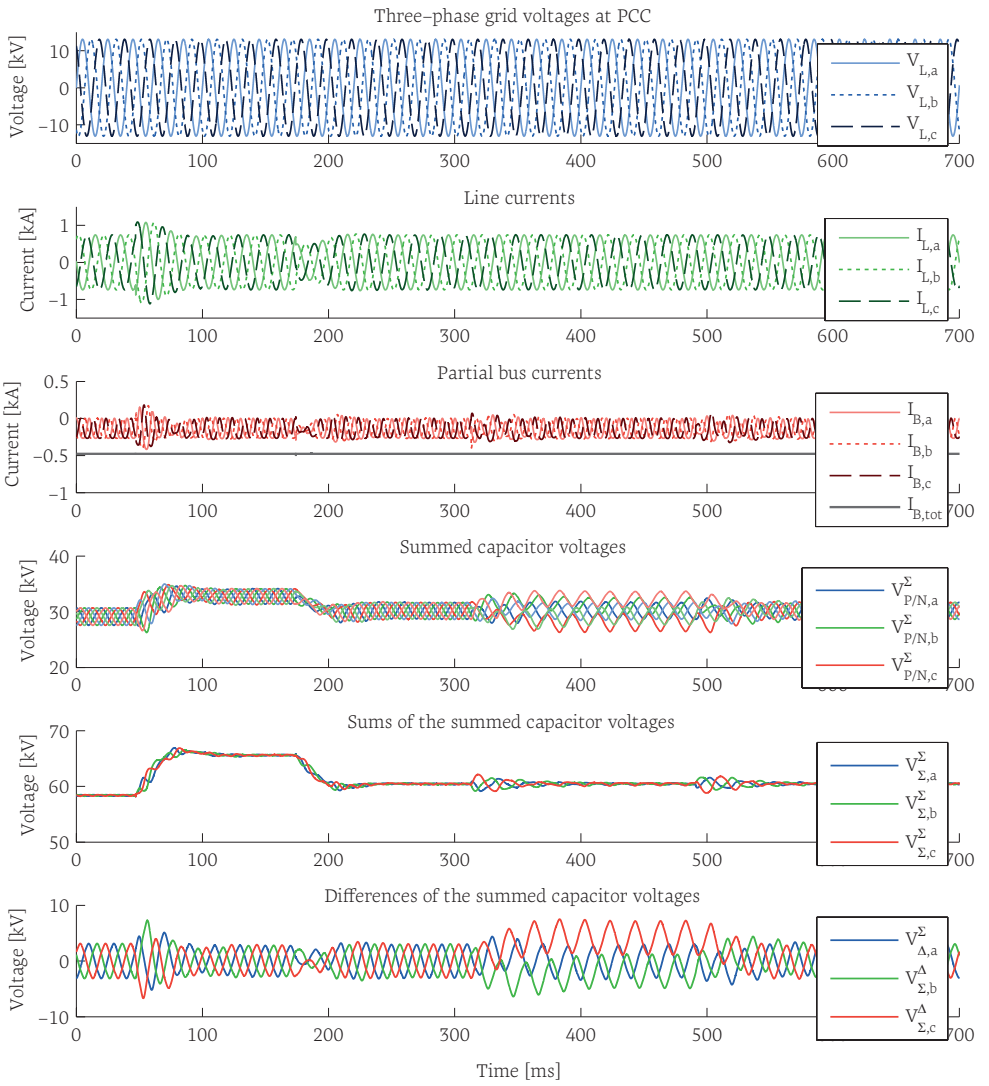


Fig. 71. Typical closed-loop control performance in rectifier mode of operation.

As expected, these results show a perfectly constant bus current, regardless of the imposed reference step. On the other hand, the line-side currents necessarily bear the corresponding transients with satisfying dynamics. Here again, despite the absence of an appropriate power/energy management control layer, satisfying overall performance is achieved as well.

3.4.3 DIRECT 3-AC/1-AC FREQUENCY CONVERTER

The 3-phase to 1-phase direct AC/AC converter possesses the exact same topology as the DC/-3AC inverter (see Fig. 26). It is thus accurately defined by the same model and functional representations. In fact, the only difference lies in the operating conditions, that correspond to an alternating voltage and current on the bus side (see §2.6.2).

3.4.3.1 CHOICE OF THE CONTROL OBJECTIVES

Assuming that both external sources are constituted by voltage sources, the use of inversion rules naturally lead to the same control structure as in Fig. 63. Indeed, since the same converter model applies, so does the inversion-based control structure!

Besides, as for the rectifier operation, it is probably wise to control the total converter energy ($V^{\Sigma}_{\Sigma,\emptyset}$) from the three-phase side owing to its constant instantaneous power. Thus, the exact same choice of tuning paths as in Fig. 69 can be used here, namely:

front-end: $m_{\Delta,abc} \rightarrow E_{\Sigma L,abc} \rightarrow E_{L,abc} \rightarrow I_{L,\alpha\beta\emptyset} \rightarrow I^{\Sigma}_{\Sigma L,\emptyset} \rightarrow V^{\Sigma}_{\Sigma,\emptyset}$

back-end: $m_{\Sigma,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow E_{\Sigma B,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow E_{B,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow I_{B,\alpha\beta}{}^{(\emptyset Hz)} \rightarrow I^{\Sigma}_{\Sigma L,\alpha\beta} \rightarrow V^{\Sigma}_{\Sigma,\alpha\beta}$

back-end: $m_{\Sigma,abc}{}^{(50Hz)} \rightarrow E_{\Sigma B,abc}{}^{(50Hz)} \rightarrow E_{B,abc}{}^{(50Hz)} \rightarrow I_{B,abc}{}^{(50Hz)} \rightarrow I^{\Sigma}_{\Delta L,abc} \rightarrow V^{\Sigma}_{\Delta,abc}$

back-end: $m_{\Sigma,\emptyset} \rightarrow E_{\Sigma B,\emptyset} \rightarrow E_{B,\emptyset} \rightarrow I_{B,\emptyset}$ (i.e. the single-phase current)

3.4.3.2 CONTROL IMPLEMENTATION AND SYNTHESIS OF THE SETVALUES

Practically, although the control structure is kept the same as in Fig. 70, the non model-based part of the design must be updated according to the modified operating conditions. Therefore, the generation of the $I_{B,abc}$ current references must be adapted. In particular, the inversion of the bus-side conversion blocks must contain edited versions of eq. (50)-(51) in order to generate the spectral components suggested by the analysis conducted in §2.6.2. More specifically:

– Equation (50) can be kept as the necessary frequency components for the vertical balancing (i.e. 50 Hz) are defined by the line-side, which remain unchanged:

$$\begin{pmatrix} I_{B,a} \\ I_{B,b} \\ I_{B,c} \end{pmatrix} = \begin{bmatrix} \cos(\theta) & \frac{-1}{\sqrt{3}}\sin(\theta) & \frac{+1}{\sqrt{3}}\sin(\theta) \\ \frac{+1}{\sqrt{3}}\sin(\theta-\frac{2\pi}{3}) & \cos(\theta-\frac{2\pi}{3}) & \frac{-1}{\sqrt{3}}\sin(\theta-\frac{2\pi}{3}) \\ \frac{-1}{\sqrt{3}}\sin(\theta+\frac{2\pi}{3}) & \frac{+1}{\sqrt{3}}\sin(\theta+\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \end{bmatrix} \begin{pmatrix} I^{\Sigma}_{\Delta B,a} \\ I^{\Sigma}_{\Delta B,b} \\ I^{\Sigma}_{\Delta B,c} \end{pmatrix} \tag{54}$$

– Equation (51) must be adapted in order to generate 16.7 Hz currents as to produce active power flows with the bus side. That is:

$$\vec{I}_{B,abc} = \frac{1}{2}\cos(\Theta)\vec{I}^{\Sigma}_{\Sigma B,abc} \tag{55}$$

Besides, the feedforward term I_{Ld+ff} can be adapted so as to represent the active power transfer on the 16.7 Hz bus side.

Overall, it can thereby be observed that the structure of the inversion-based control scheme is left unchanged when switching from DC/AC to AC/AC conversion. This is of course an expected result since the converter model is the same. On the other hand, the non model-based part of the design related to the horizontal and vertical balancing must be adapted since it depends on the operating conditions, which are changed. That said, the followed design method allows to locate and limit the corresponding changes to two equations only, with the assurance that these changes are sufficient.

Several results are depicted and commented here between Fig. 72 and Fig. 74. The corresponding simulation parameters (see Table 4) aim to describe a prospective railway intertie facility. Compared to Table 3, the main difference is related the larger capacitance installed in the submodules:

Nominal power	P	*20 MVA*	*Bus voltage*	V_{bus}	*15 kV$_{RMS}$*
Line voltage	V_{ac}	*16 kV (rms)*	*Bus-side inductance*	L_{bus}	*0.5 mH (ESR=50 mΩ)*
Line current	I_L	*600 A (rms)*	*Line-side inductance*	L_{ac}	*1.5 mH (ESR=20 mΩ)*
Number of cells per arm	N	*13*	*Total arm inductance*	L	*1.5 mH*
Submodule capacitance	C_{SM}	*4.1 mF (ESR=10 mΩ)*	*Mutual arm inductance*	M	*neglected*
App. switching frequency	f_{SW}	*10 kHz*	*Total arm resistance*	R	*neglected (see R_{SM})*

Table 4. Simulation parameters corresponding to 15 kV, 16.7 Hz medium-voltage network intertie.

The steady-sate performance of this control implementation is shown in Fig. 72:

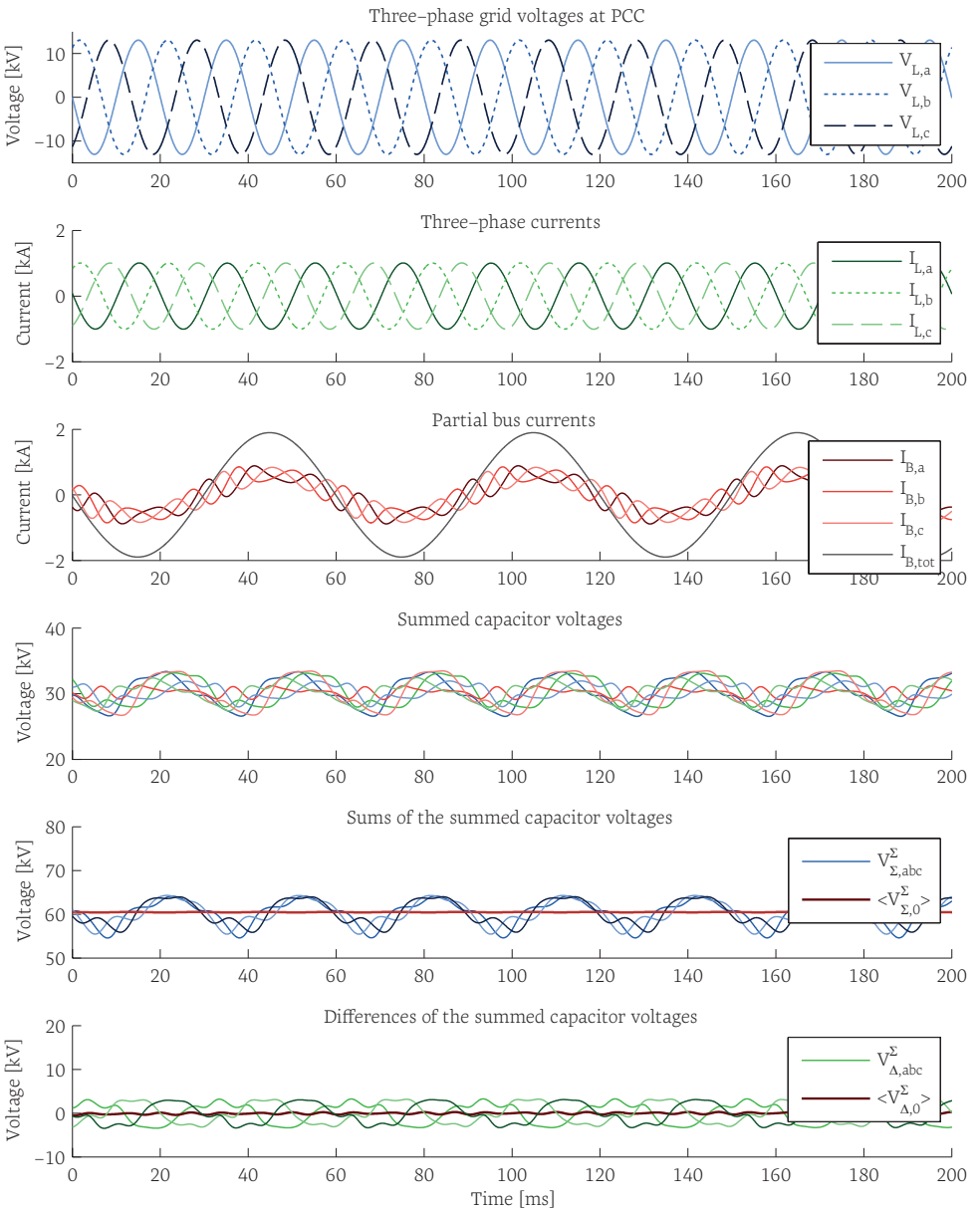


Fig. 72. Typical steady-state operation waveforms of the direct 3-AC/1-AC frequency converter.

Of course, due to the 33.3 Hz pulsation of the total bus power, constant phase-leg energy is not desirable here. The instantaneous power difference with the three-phase side must therefore be buffered by the converter. This is why significant oscillations can observed on the $V^{\Sigma}_{\Sigma,abc}$ voltages. Furthermore, as it can be see in Fig. 72 as well, relatively complex combinations of bus- and line-frequency components (here 16.7 Hz and 50 Hz) are present on the partial bus currents as well as on the summed capacitor voltages. Finally, unlike for DC/3-AC operation, the power flows are not similar among all phase-legs, owing to the relative phase of the single-phase side (versus the three-phase side). This can be easily observed on the $V^{\Sigma}_{\Delta,abc}$ voltages.

Moreover, in order to illustrate the effectiveness of the modified control scheme, Fig. 73 depicts the typical performance of the closed-loop voltage control similarly to what was shown in Fig. 65 and Fig. 71:

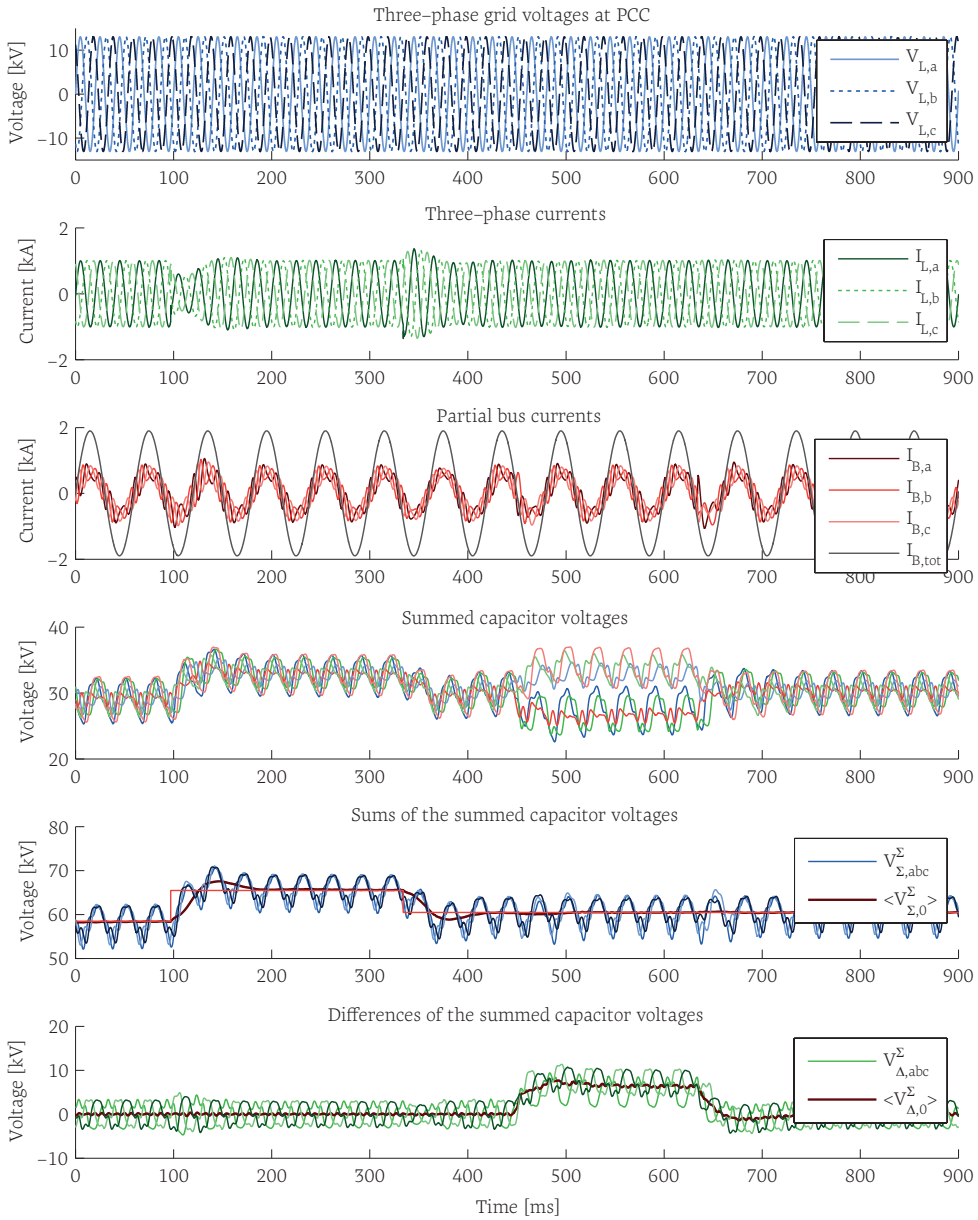


Fig. 73. Typical closed-loop control performance of the complete inner converter control.

As shown by Fig. 73, owing to the choice of tuning paths, the step operated on $V^{\Sigma}_{\Sigma,\emptyset}$ at $t = 92\,ms$ influences mainly the active power flow generated by the line currents, while only slight differences are induced on the partial bus currents for balancing purposes. In any case, the total bus current remains unaffected. Similar comments hold for the vertical unbalance reference step, except that the line side remains unaffected.

Additionally, unlike for the DC/3-AC case, the limitations of the filter-based approach are here clearly visible on the total energy control, due to limited dynamics. On the other hand, such performance is nevertheless largely acceptable and entirely state-of-the-art in the sense that no such results seems to have been reported yet.

Finally, Fig. 74 illustrates the operation of the direct AC/AC converter under unbalanced grid conditions:

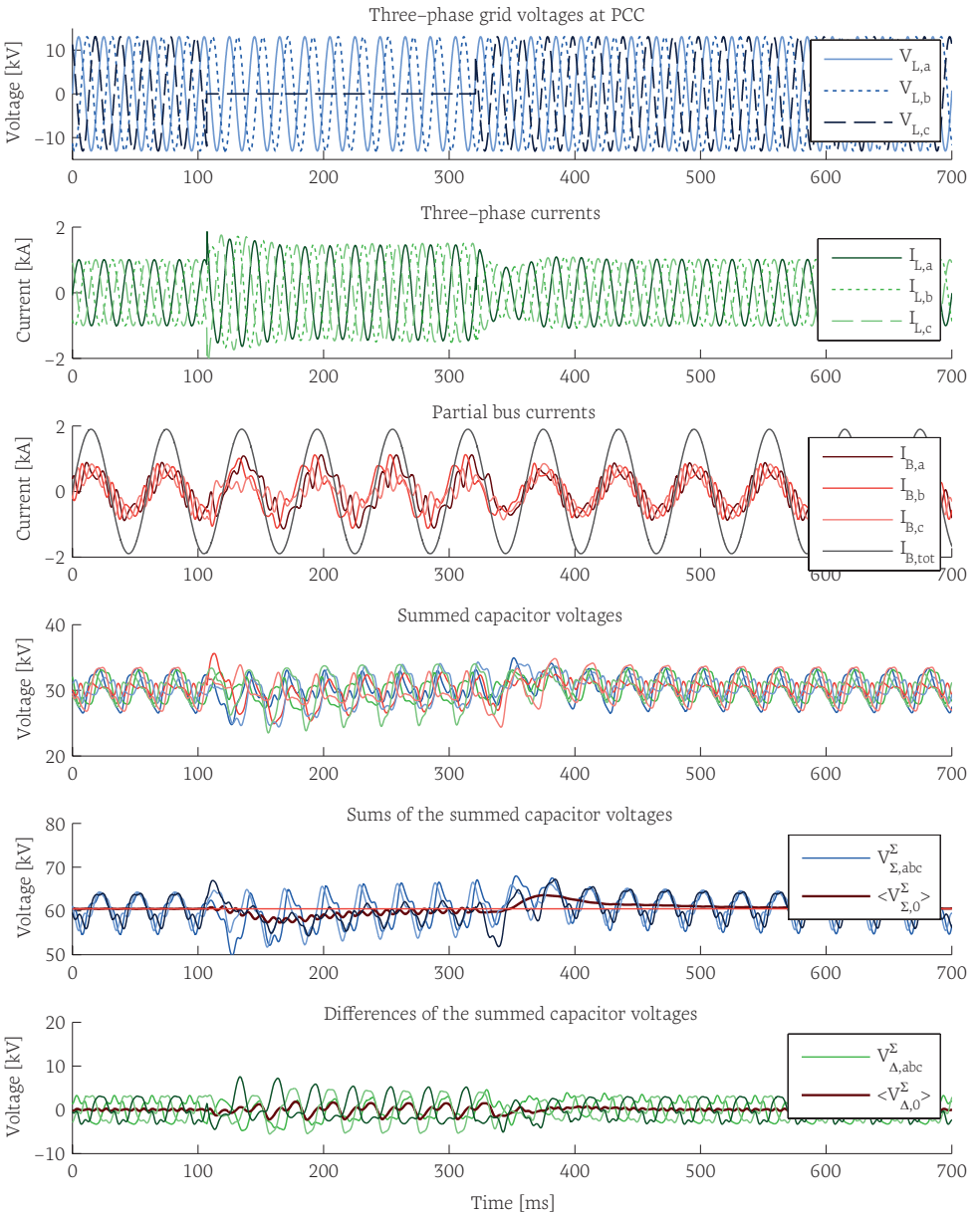


Fig. 74. Operation of the complete inner control under unbalanced three-phase grid conditions.

In Fig. 74, unlike in Fig. 66, the main power transfer reference is defined on the bus side. Therefore, the loss of one phase induces increased current amplitudes during the fault in order to maintain the same total active power transfer (assuming symmetric currents injection).

That said, this result well illustrates the proper operation of the presented scheme even under such complex operating conditions. Indeed, as it can be seen on the figure, a satisfying fault-ride-through behavior is achieved, still relying on the same control scheme as in the previous examples. To the best of the author's knowledge, this is also the first time it is reported about the operation of the direct 3-AC/1-AC converter under unbalanced grid conditions.

3.4.4 SINGLE-PHASE DC/2-AC CONVERTER

3.4.4.1 CHOICE OF THE CONTROL OBJECTIVES

As for three-phase systems, attractive representations of two-phase systems can be obtained using a coordinate transformation that highlights the relevant magnitudes. Practically, instead of using the $\alpha\beta\emptyset$ reference-frame, a useful manipulation of the phase-leg quantities is given by the common-mode / differential-mode decomposition, which is here referred to as $\alpha\emptyset$ decomposition in order not to confuse with the vertical decomposition of the summed capacitor voltages. This corresponds to the following projections, which are illustrated in Fig. 75 :

- $I_{B,\alpha}$ is the differential-mode of the partial bus currents, i.e. the only circulating current existing in the structure.
- $I_{B,\emptyset}$ is the common-mode of the partial bus currents, i.e. half the total bus current.
- $V^{\Sigma}_{\Sigma,\alpha}$ is the differential-mode between $V^{\Sigma}_{\Sigma,d}$ and $V^{\Sigma}_{\Sigma,e}$, i.e. the image of the horizontal unbalance between the total phase-leg energies.
- $V^{\Sigma}_{\Sigma,\emptyset}$ is the common-mode between $V^{\Sigma}_{\Sigma,d}$ and $V^{\Sigma}_{\Sigma,e}$, i.e. the image of the total energy stored inside the converter.

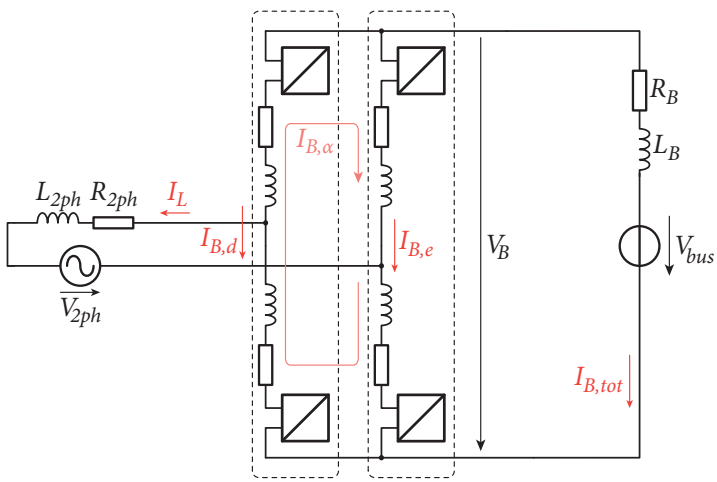


Fig. 75. Structure of the two-phase DC/AC converter (with arm-equivalent modeling, see §2.3).

Obviously, the functional representations of such a system are essentially similar to those presented in section 2.5.2 ; the only necessary change being the choice of the coordinate transformations described above. Fig. 76 depicts the corresponding EMR :

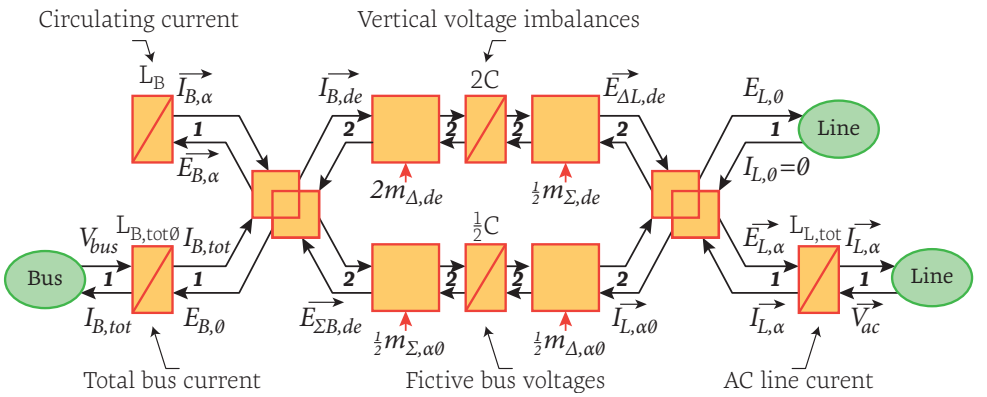


Fig. 76. EMR of a two-phase converter structure.

3.4.4.2 CONTROL IMPLEMENTATION AND SYNTHESIS OF THE SETVALUES

In terms of control implementation, significant differences must be expected though, owing to the way the partial bus currents are combining in order to form the total bus current. Indeed, due to the fact that the pulsation of the line-side instantaneous power is *in phase* between the two phase-legs (rather than shifted by 120°), second-order harmonic injection in the partial bus currents is generally not advisable, as these terms are not self-compensating on the bus. Besides, as there is no possible way to enforce that the oscillating terms generated by the vertical balancing are exactly compensating (Münch's trick of eq. (50) is not applicable), the latter may be reported to the total bus current as well.

Consequently, a practical control implementation corresponding to the system of Fig. 75 can be derived from Fig. 76 similarly to what is presented in §3.4.1, but taking into account the above comments. A possible control scheme is depicted in Fig. 77:

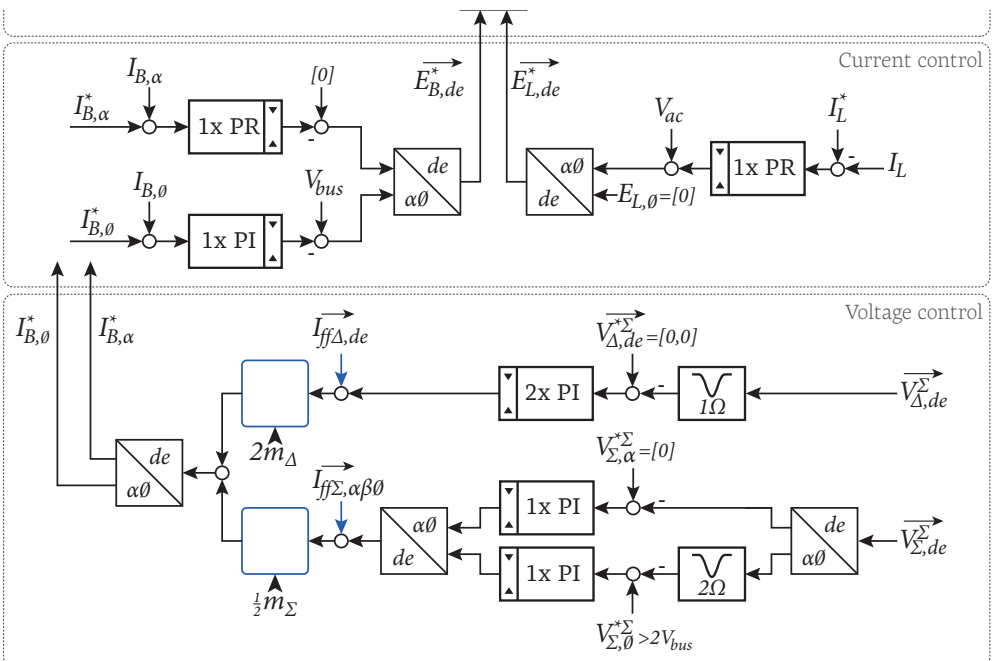


Fig. 77. Possible control implementation of a two-phase DC/AC converter without a supervisory-level strategy block, but using filters on the relevant summed capacitor voltages.

As expected, this control scheme is very similar to the previous ones, except that it features modified custom blocks (in blue), which are adapted to the two-phase inverter operation. Indeed, these block are edited in order to generate currents of the bus frequency in the common-mode branch and of line-frequency in the differential mode branch. Concretely, this corresponds to equations (56) and (57) respectively:

$$\begin{pmatrix} I_{B,d} \\ I_{B,e} \end{pmatrix} = \frac{1}{V_{bus}} \begin{bmatrix} V^{\Sigma}_{\Sigma,d} & 0 \\ 0 & V^{\Sigma}_{\Sigma,e} \end{bmatrix} \begin{pmatrix} I^{\Sigma}_{\Sigma B,d} \\ I^{\Sigma}_{\Sigma B,e} \end{pmatrix} \tag{56}$$

$$\begin{pmatrix} I_{B,d} \\ I_{B,e} \end{pmatrix} = \begin{bmatrix} \cos(\theta) & 0 \\ 0 & \cos(\theta+\pi) \end{bmatrix} \begin{pmatrix} I^{\Sigma}_{\Delta B,d} \\ I^{\Sigma}_{\Delta B,e} \end{pmatrix} \tag{57}$$

Besides, the current feedforward terms defined by equations (52)-(53) can be advantageously reused here as well.

Finally, the typical performance of this control scheme is illustrated in Fig. 78 using the parameters from Table 3.

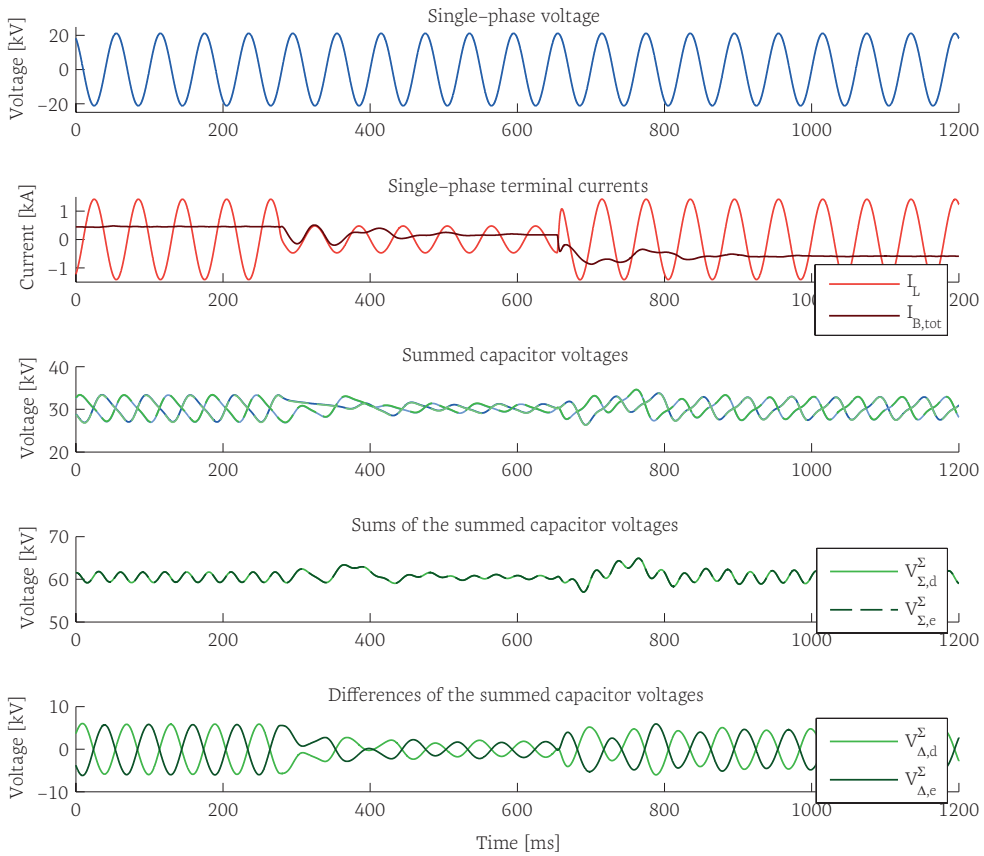


Fig. 78. Typical closed-loop control performance of the complete inner converter control.

As depicted on the figure, satisfying dynamics can be achieved in this case as well. Besides, apart during transients, where the vertical balancing induces some oscillations of the total bus current, the latter can be controlled to be a plain DC quantity, as expected.

3.4.5 INDIRECT 3-AC/DC/1-AC CONVERTER

3.4.5.1 CHOICE OF THE CONTROL OBJECTIVES

In the sequel, a possible control scheme for a 3-phase to 2-phase network intertie is derived, corresponding to the back-to-back configuration depicted in Fig. 79. As suggested in §1.4.1, such a 3-AC/DC/1-AC converter configuration may be considered for various applications at the distribution level of 16.7 Hz railway networks or at the catenary level wherever symmetric feeders are used.

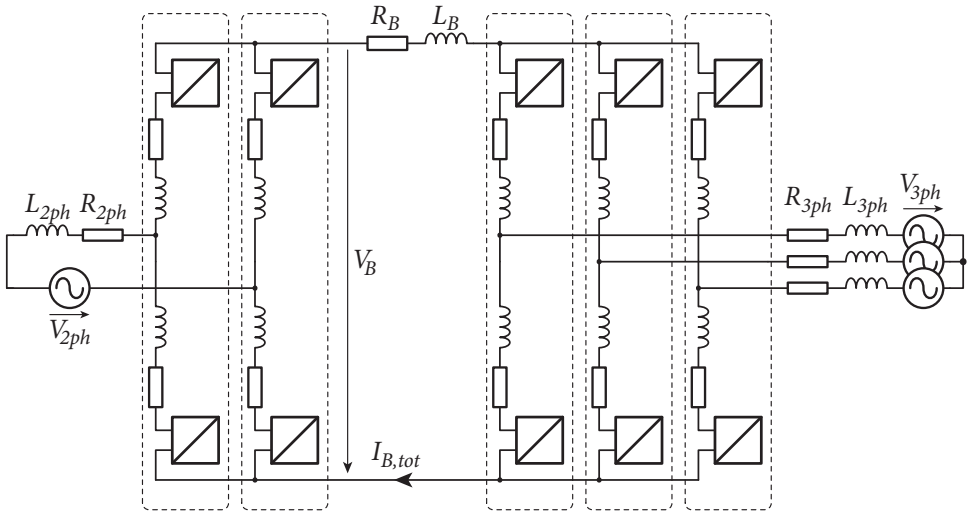


Fig. 79. Structural representation of a DC/3-AC or a direct 1-AC/3-AC converter.

In the light of the preceding developments, such a system can be represented by the EMR of Fig. 81, page 100. Obviously, in the figure, the two bus-side inductances have been merged as they constitute a unique state variable.

Importantly, this last remark is also pointing out that one of the key design choices consists in defining the roles of the two converters respectively to the intermediary DC bus. Indeed, as no capacitance is physically present on this bus, the control structure presented in §3.4.2 (see Fig. 69) is not directly applicable. A simple solution could consist in operating the three-phase side as a "blind" voltage source (in open-loop) in which the single-phase inverter is injecting or withdrawing a controlled current. The other way around is naturally possible as well.[20]

In any case, a major energy management concern arises, related to the possible free shaping of the three intermediate bus voltages (the physical one, present between both converters and the two fictive ones, present "inside" each converter). Different strategies can be outlined :

– The 2-phase converter exchanges a *purely constant power* with the physical DC bus. It is thereby forced to compensate for the 33 Hz power pulsation of the railway side, while the three-phase converter faces only 100 Hz power pulsation.[21] Consequently, two different types of submodules must be implemented inside the converters, due to different silicon area requirements and different required capacitances.

20. Droop-type control approaches could also be considered, especially when it comes to multi-terminal DC networks. This goes however far beyond the scope of the present work.

21. Whose impact on the capacitor sizing is not only much lower, but can also be alleviated with second-order harmonic injection.

– Some of *the power pulsation is fed* from the railway side to the physical DC bus, what induces a non-constant DC current, but also allows to spread the absorption of the power pulsation equally among the five phase-legs. Ideally, identical submodules could be used in the entire system, provided that such a bus current can be tolerated. This second approach has apparently never been studied in the existing literature.

Owing to its potential attractiveness, the second strategy is adopted here. The chosen tuning paths are presented along with the corresponding EMR on Fig. 81.

3.4.5.2 CONTROL IMPLEMENTATION AND SYNTHESIS OF THE SETVALUES

The control of both converters can be developed similarly to the previous sections:

– For the *three-phase AC/DC converter*, the same kind of approach as in §3.4.2 can be adopted here, i.e. a control structure that resembles the one of a conventional rectifier. The control implementation of Fig. 70 is directly applicable, except with respect to the bus current, which must be left uncontrolled as it is imposed by the single-phase inverter. Besides, the physical bus voltage is imposed in an open-loop manner.
– With regards to the *two-phase DC/AC converter*, the control implementation of Fig. 77 can be used here as well, without changes.

The derived control scheme is shown in Fig. 82 and include all the above-mentioned considerations. Importantly, the definition of no less than 13 reference values (in blue on Fig. 82) is left to be defined by a superposed strategy block. Additionally, most feedforward quantities are also dependent on the chosen energy management strategy.

These two observations suggest that this control scheme is still incomplete and that the development of an additional supervisory control layer is mandatory. On the other hand, neglecting the horizontal and vertical balancing phenomena, this entire converter structure is functionally equivalent to the partial EMR of Fig. 80, which recalls a conventional double back-to-back system. It is the belief of the author that this simplified perspective is sufficient to support the development of a sane control cascade with respect to the definition of the feedforward terms. Meanwhile, the filter-based control implementation has proved to be satisfactory[22] and can be directly reused from §3.4.2 and §3.4.4.

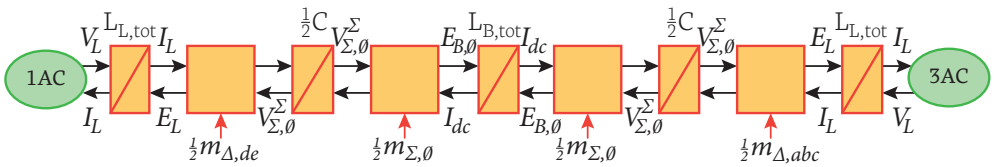


Fig. 80. Partial EMR corresponding to Fig. 81, but neglecting the vertical and horizontal balancing issues. The obtained representation is identical to a double back-to-back conversion system.

In any case, these comments are indirectly revealing here that the limits of a systematic and rigorous control design methodology are somehow reached. Exemplarily, the drawing of the *Maximal Control Structure* out of Fig. 81 would simply be unreadable. However, the fact remains that a simplified functional perspective –even simplified as in Fig. 80– greatly helps in understanding such topologies and developing the corresponding control schemes, even though they may be incompletely inversion-based.

22. In the previous sections but also more widely in the literature, see §3.2)

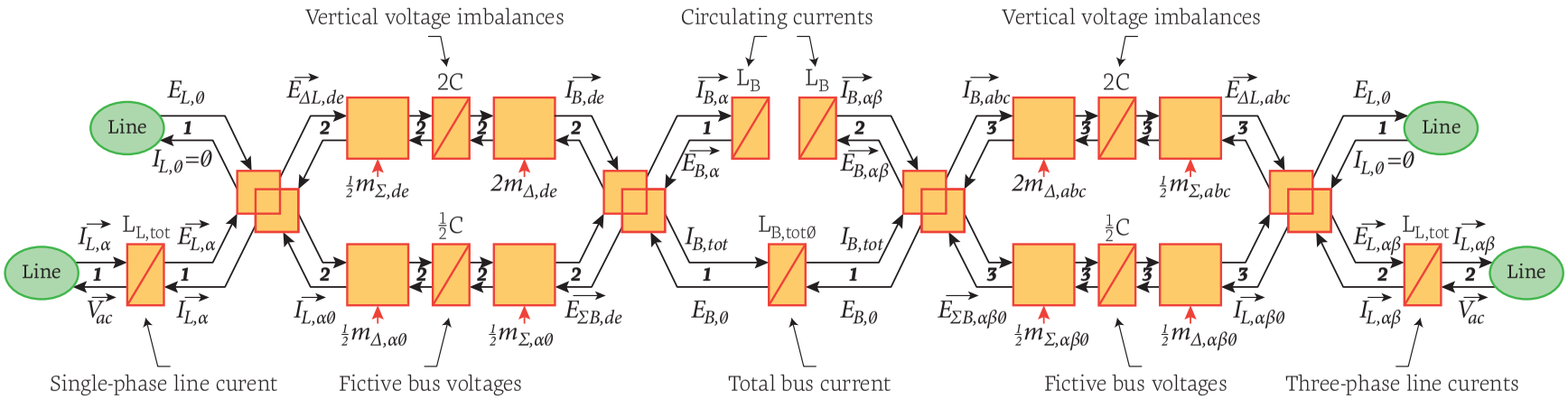


Fig. 81. EMR of the complete back-to-back 1-AC/DC/3-AC conversion system.

The chosen tuning paths are as follows:

– 3-phase front-end:	$m_{\Delta,abc}$	$\rightarrow E_{\Sigma L,abc}$	$\rightarrow E_{L,abc}$	$\rightarrow I_{L,\alpha\beta\emptyset}$	$\rightarrow I^{\Sigma}_{\Sigma L,\emptyset}$	$\rightarrow V^{\Sigma}_{\Sigma,\emptyset}$	= total converter energy
– 3-phase back-end:	$m_{\Sigma,\alpha\beta}{}^{(\emptyset Hz)}$	$\rightarrow E_{\Sigma B,\alpha\beta}{}^{(\emptyset Hz)}$	$\rightarrow E_{B,\alpha\beta}{}^{(\emptyset Hz)}$	$\rightarrow I_{B,\alpha\beta}{}^{(\emptyset Hz)}$	$\rightarrow I^{\Sigma}_{\Sigma L,\alpha\beta}$	$\rightarrow V^{\Sigma}_{\Sigma,\alpha\beta}$	= horizontal balance
– 3-phase back-end:	$m_{\Sigma,abc}{}^{(50Hz)}$	$\rightarrow E_{\Sigma B,abc}{}^{(50Hz)}$	$\rightarrow E_{B,abc}{}^{(50Hz)}$	$\rightarrow I_{B,abc}{}^{(50Hz)}$	$\rightarrow I^{\Sigma}_{\Delta L,abc}$	$\rightarrow V^{\Sigma}_{\Delta,abc}$	= vertical balance
– 3-phase back-end:	$m_{\Sigma,\emptyset}$	$\rightarrow E_{\Sigma B,\emptyset}$	$\rightarrow E_{B,\emptyset}$	$\rightarrow I_{B,\emptyset}$			= DC bus current
– 2-phase front-end:	$m_{\Delta,de}$	$\rightarrow E_{\Sigma L,de}$	$\rightarrow E_{L,de}$	$\rightarrow I_{L}$			= single-phase line current
– 2-phase back-end:	$m_{\Sigma,\alpha\emptyset}{}^{(\emptyset Hz)}$	$\rightarrow E_{\Sigma B,\alpha\emptyset}{}^{(\emptyset Hz)}$	$\rightarrow E_{B,\alpha\emptyset}{}^{(\emptyset Hz)}$	$\rightarrow I_{B,\alpha\emptyset}{}^{(\emptyset Hz)}$	$\rightarrow I^{\Sigma}_{\Sigma L,\alpha\emptyset}$	$\rightarrow V^{\Sigma}_{\Sigma,\alpha\emptyset}$	= horiz. balance + total converter energy
– 2-phase back-end:	$m_{\Sigma,de}{}^{(16.7Hz)}$	$\rightarrow E_{\Sigma B,de}{}^{(16.7Hz)}$	$\rightarrow E_{B,de}{}^{(16.7Hz)}$	$\rightarrow I_{B,de}{}^{(16.7Hz)}$	$\rightarrow I^{\Sigma}_{\Delta L,de}$	$\rightarrow V^{\Sigma}_{\Delta,de}$	= vertical balance

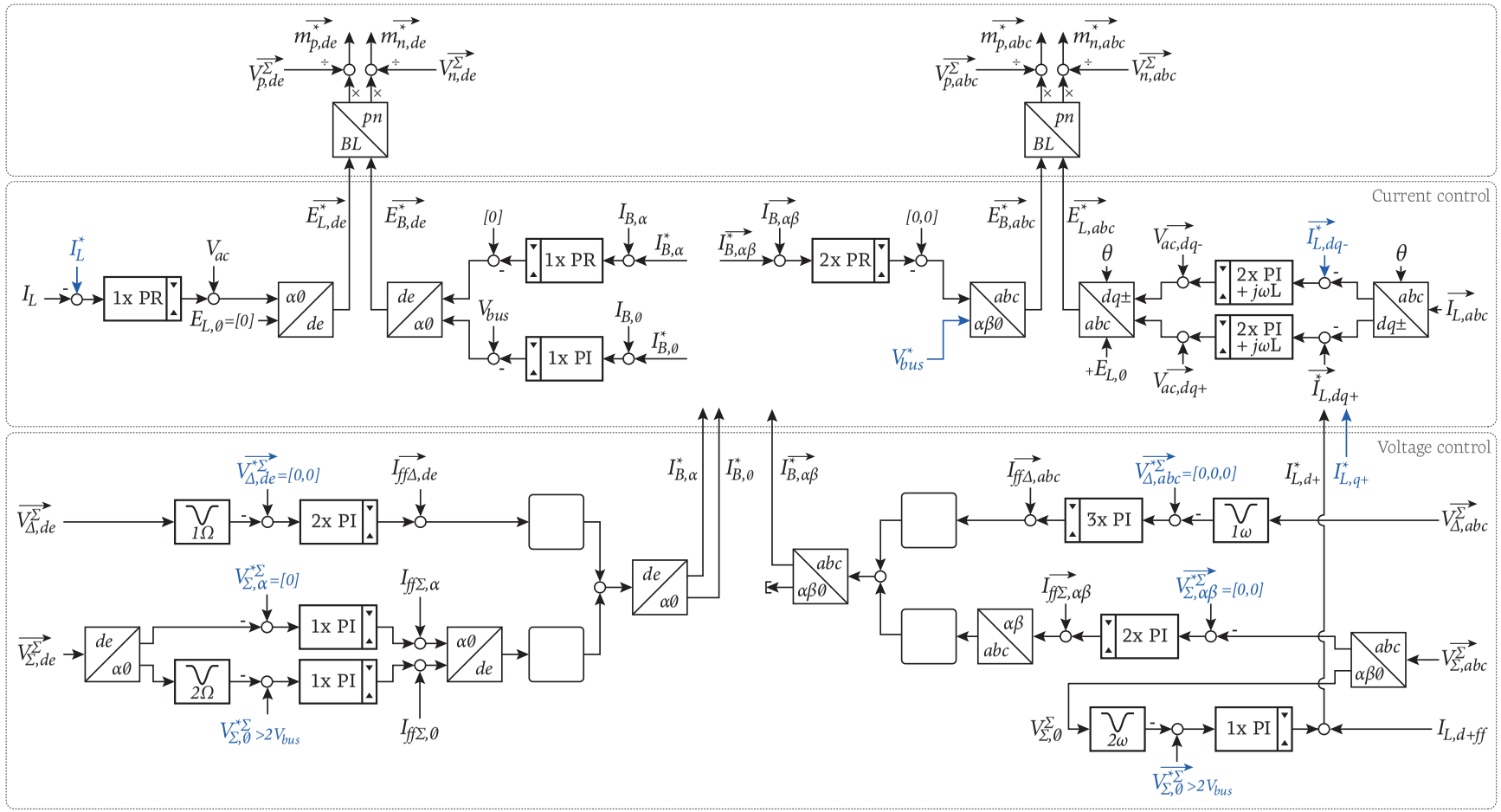


Fig. 82. Complete control scheme of the back-to-back 3-AC/DC/2-AC frequency conversion system.

Illustrative simulation results are provided in Fig. 83, using the parameters from Table 4, but with $C_{SM} = 2.8\,mF$ for all cells (the same value as for a conventional three-phase 50 Hz three-phase converter) and $V_{bus} = 28\,kV$. Two steps are operated:

- At $t = 285\,ms$, the single-phase current reference is changed from $1.5\,kA$ to $0.5\,kA$.
- At $t = 705\,ms$, the same current reference is changed to $-1.5\,kA$.

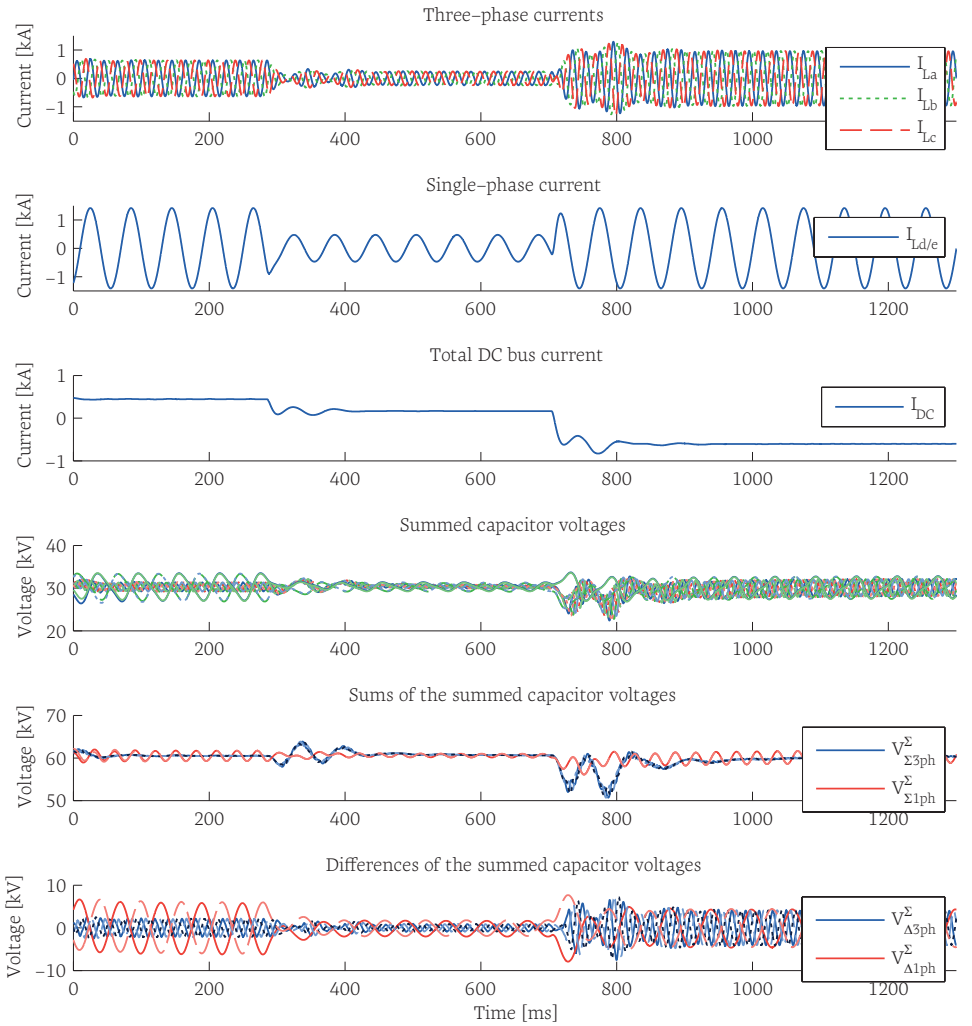


Fig. 83. Typical closed-loop control performance of the complete inner converter control.

In the figure, the impact of the vertical balancing of the single-phase side on the total bus current is clearly visible. It is here complicating the power flow management as the corresponding power pulsation must be either reported to the three-phase side (hence resulting in some oscillations of the current envelope), or absorbed internally (hence requiring the appropriate amount of embedded energy). As mentioned earlier, this is a unique and unavoidable property of single-phase systems.

Furthermore, it can also be seen that the imperfect tuning of the various control loops here results in limited control dynamics. On the other hand, with four equivalent stages of conversion, reaching exemplary dynamics is not a trivial task. Overall, these two comments illustrate that the indirect frequency conversion structure is finally functionally more complex and less convenient than the direct 3-AC/1-AC topology.

3.5 GENERAL COMMENTS

3.5.1 ABOUT MODEL-BASED CONTROL DESIGN

As seen in this chapter, the main challenges set by the control design of MMCs is not so much related to the definition of the appropriate control structures (in the sense of the hierarchy of blocks), but is rather related to the actual implementation of these blocks, in other words of their content. These two distinct stages also clearly define the boundary between the part of the control design that can be strictly obtained by the inversion of the model, and the part that cannot, or not entirely.

Indeed, the inversion rules can only help to define the causal chains of the control, while the details of the implementation (choice of controllers, choice of generated spectral components, etc.) are directly depending not on the model but on the operating conditions. As an example, this difference can be clearly seen by comparing the control implementations of the DC/AC converter and direct AC/AC converter, as both correspond to the same converter topology and the same control structure, but the content of some blocks differs (the blue blocks on Fig. 64).

In the context of MMCs, these limitations of the model-based control design also highlight those of the decoupling of the balancing mechanisms. Indeed, the presented approach has shown in §3.3 that a perfect decoupling of the vertical and horizontal balancing is impossible. This is because there is no choice of control cascades that includes all state variables without exploiting several times the same quantity for distinct purposes (typically I_B). On the other hand, the operating conditions can be exploited such that a certain separation can be provided through the spectral separation of suitable quantities. This is what is achieved here.

Finally, with respect to methodological issues, it is interesting to observe that the elements that are not solely defined by model inversion here are the same as in the case of a more conventional topology, such as that illustrated by Fig. 84:

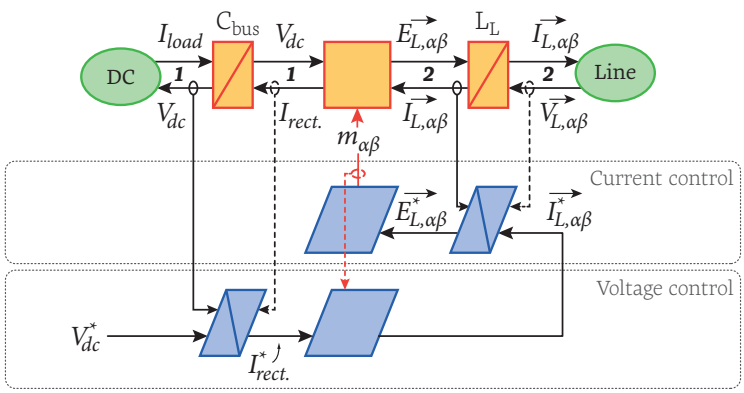


Fig. 84. EMR and *Maximal Control Structure* of a conventional DC/AC converter with a cascaded voltage control scheme controlling the DC bus voltage from the line active power flow.

Indeed, when the control of the DC bus of a conventional active rectifier is derived (see above), the passage from I^{*}_{rect} to $I^{*}_{L,\alpha\beta}$ is not a strict inversion (division by $m_{\alpha\beta}$) but requires the generation of sinusoidal current components such as an active power flow is generated on the line side. In fact, in this particular case as with MMCs, the spectral content of the line current is defined such that the desired instantaneous bus-side power flow is "translated" to an active power flow (thus an average quantity) on

the line-side. In other words, this conversion relies on the fact that 50 Hz · 50 Hz = DC (+100 Hz which compensate between phases). In fact, this is the same approach as described through the spectral analysis conducted in §2.6.

In the end, this simple comparison with a basic topology shows that there is nothing fundamentally unconventional or inappropriate in the control schemes established through this chapter, which also corresponds to what is commonly done in similar existing control structures.

3.5.2 OPERATION-RELATED ASSUMPTIONS

Still with respect to the definition of the partial bus currents, a special subtlety related to the vertical voltage balancing deserves a particular attention. Indeed, this chapter has made a wide use of the trick introduced by Münch in [120] and expressed by equation (50) in order to ensure that the vertical balancing does not impact the total current bus. This trick is remarkable because it is both fundamental (it leads to a very desirable behavior), and can apparently not be inferred by a systematic approach.

Besides, provided that (50) is used and that the corresponding current references are also perfectly tracked by their controllers, the $\emptyset$-axis components related to the horizontal and vertical balancing mechanisms are guaranteed to be null, what allows to separate these problems from the total power transfer and energy control. Practically, this corresponds to introducing an additional assumption in the model which, if sufficiently well guaranteed, allows to modify the EMR of Fig. 42 as in Fig. 85:

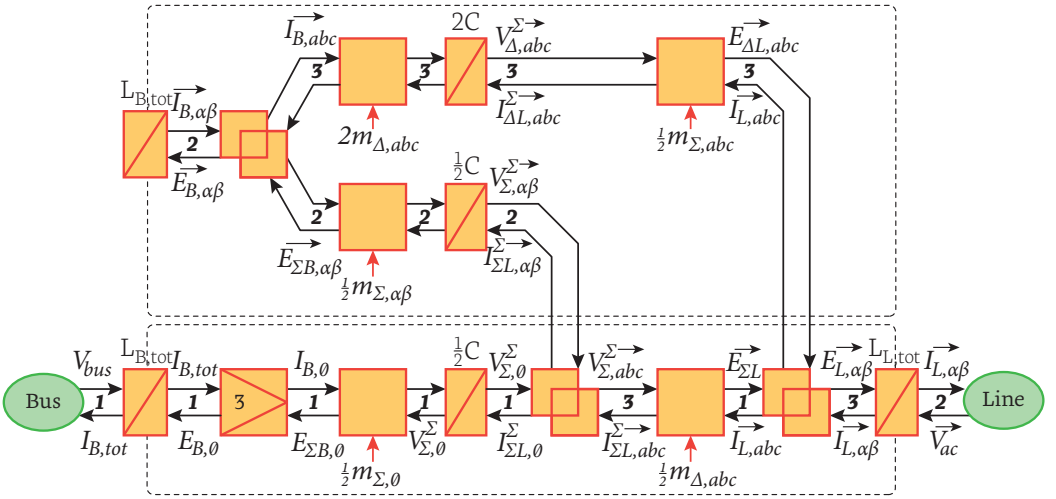


Fig. 85. EMR of the converter structure of Fig. 26 in case the use of Münch's trick guarantees the validity of the additional assumption represented by equation (50).

This new representation is interesting in the sense that it corresponds to the representation objective originally pursued and presented in Fig. 36, page 44. Indeed, Fig. 85 is exactly meeting this objective of separating the inner balancing problem from that of a conventional three-phase (double-stage) power conversion system. On the other hand, it is key to note here that although possible, this representation and interpretation of the MMCs' behavior is only allowed by the validity of the purposely introduced assumption. In other words, the representation objective of Fig. 36 can finally be reached, but is preconditioned by the implementation of suitable control techniques.

3.5.3 TOPOLOGIES FOR RAILWAY APPLICATIONS

Through this chapter, various topologies of MMCs were presented that are directly applicable to railway applications:

- For the implementation the frequency conversion *network interties* suggested in Fig. 15, page 17 (with or without the supply of advanced ancillary services), both the direct 3-AC/1-AC topology of §3.4.3 and the indirect 3-AC/DC/1-AC topology of §3.4.5 are eligible solutions. Regarding the choice between these two topologies, the former seems preferable.[23] Indeed, it was already reported by Winkelnkemper in [72] that direct AC/AC conversion is superior to indirect conversion in terms of *i)* total embedded energy, *ii)* total silicon area and *iii)* distribution of the losses. Furthermore, this chapter has shown a significant difference in control complexity, since the direct AC/AC converter structure is functionally equivalent to a back-to-back system while the indirect AC/DC/AC topology is functionally equivalent to a double back-to-back system.
- With respect to *HVDC upgrade applications* (see Fig. 16), the indirect 3-AC/DC/1-AC topology may be attractive as there is not much alternatives for this particular scenario. Besides, this topology could also be well suited in case the *four functional* stages of conversion can be advantageously exploited. An example will be given in Chapter 5.
- Finally, for the *standalone applications* suggested by Fig. 17, the single-phase STATCOM-type topology corresponding to one arm only is the most evident choice (not shown here).[24] Besides, the converter structure of §3.4.4 is theoretically usable as well, especially if the so implemented bus has some purpose. In such cases, the corresponding operation is focused on the supply of ancillary services only, such as *i)* voltage support, *ii)* active filtering/damping or *iii)* UPS-type applications.

Overall, even though the detailed comparative assessment of these topologies remains to be done for each of the mentioned applications, it can be thus seen that MMC topologies constitute an interesting catalogue of solutions capable of covering a broad range of applications. As a matter of fact, this ability to cover several variants of similar applications with variants of the same topology certainly reinforces the attractiveness of a flexible and systematic control design methodology.

3.6 SYNTHESIS

3.6.1 CONCLUSIONS

This chapter has shown how the control design of MMCs can be achieved in a systematic manner by following an approach based on the functional inversion of their subsystems. Furthermore, by closely respecting a number of control design rules, the deduced control schemes are guaranteed to be well structured and hierarchized, typically using an organization in three layers: *i)* current control, *ii)* voltage control and *iii)* strategical concerns.

In the context of MMCs, the proposed control design methodology suggests to implement cascades that allow the closed-loop control of all state variables. Besides, by trac-

23. This seems to be the choice made by most manufacturers for this particular application.
24. This also corresponds to the front-end of the PETT topology presented in [13]-[14].

ing a clear line between closed-loop control implementation and optimization-related or energy management concerns, the proposed approach suggests to implement the control of the summed capacitor voltages without filtering. Instead, it proposes to leave this responsibility to the strategy layer, which is then tasked to generate the appropriate voltage setvalues that contain the necessary spectral content. Furthermore, the inversion-based design principles also suggest to make an extensive use of feedforwarding techniques, in particular with respect to the images of the instantaneous power flows between the two functionally-equivalent conversion stages, what is a generally absent feature in most existing control schemes.

Moreover, the resulting control schemes have shown that such a control design methodology naturally reaches the same mechanisms as those individually found in some of the most comprehensive existing control implementations so far (such as in the works reported by Bergna, Kolb and Kammerer or Münch, see §3.2). Compared to these works, the conducted simulations have shown that the results obtained through a strict model inversion – even without a proper energy management layer, but using a wise filtering of some quantities – allow to reach excellent performances with relatively simple control techniques. Besides, since the phase-leg energy fluctuations are minimized through a fast closed-loop voltage control – rather than by feedforwarding the necessary spectral components in the currents and controlling only the average voltages – the summed capacitor voltages are guaranteed to be truly well controlled during transient regimes. This is probably an underestimated issue in order to really optimize the size of the submodule capacitors.

Beyond their performance, the presented control schemes also distinguish by their deliberate genericity. Indeed, as long as the corresponding blocks are implemented properly, such schemes apply without modification to a wide range of operating conditions. As a matter of fact, they correspond to what is necessary in order to take fully advantage from the specificities of MMCs (exploitation of the MMC-specific degrees of freedom, operation under unbalanced grid conditions, etc.). For some particular cases such as the operation of the direct AC/AC frequency converter under unbalanced grid conditions, it seems that the present results are unprecedented, even in simulation.

Finally, owing to their strong layerization, the proposed control implementations are naturally modular and are hence easily portable from one application or one topology to another. Besides, in case the control implementation must be adapted to different operating conditions (typically from a spectral point of view), it was shown that the modification of only a few blocks is necessary, corresponding to the inner balancing mechanisms and the operating-conditions-dependent part of the control design (the blue blocks on Fig. 64).

Overall, the presented control design methodology has demonstrated that it can lead to effective and comprehensive control schemes, whose validity has been established through simulations (and will be confirmed in Chapter 4 with experimental results). Owing to the rigourous and systematic nature of the design approach, the obtained schemes therefore constitute a sound basis towards the development of energy management mechanisms, whose implementation is the logical next step to the present work. A more transparent design of the energy management is expected, what seems indispensable towards the integration of energy storage into MMCs, especially if the latter involve several distinct technologies.

3.6.2 FUTURE WORK

As can be seen in many simulation results in this chapter, the capacitor voltage ripples bear significant variations during transients. For instance, in the presented simulation results, the summed capacitor voltages regularly exceed 150-200% of the steady-state ripple, despite control performances specifically focused on that matter. Therefore, the minimization of the peak-to-peak voltage ripple in steady-state – related to the dimensioning of the submodules capacitors – matters very little if the corresponding boundaries are substantially exceeded during transient conditions or asymmetric regimes of operation. This is why the performance of the voltage control is crucial and is certainly a generally overlooked concern in this respect.

This simple comment suggests to pay an increased attention to the relation between the performance of the closed-loop voltage control and the capacitors' sizing. Indeed, the dimensioning of the controller parameters has been deliberately disregarded throughout this work. That said, it is nevertheless an important part of the control design, set in the continuation of this work. Moreover, as the absolute decoupling of the vertical and horizontal balancing is impossible, some trade-offs are necessary during the design of the voltage controllers, what also calls for further investigations.

4 LABORATORY-SCALE PRACTICAL VALIDATION

Abstract – This chapter presents the implementation of some of the previously-presented and simulated control schemes on a downscaled converter prototype. The obtained results thereby aim to serve as a further validation of the concepts developed throughout this work. Besides, they also intend to contribute to illustrate some of the challenges related to the implementation of the necessary control hardware.

4.1 HARDWARE IMPLEMENTATION

At the time the MMC-related research activities were started at LEI-EPFL (first hardware in Fall 2009, [201]-[203]), no commercially-available control platform was truly capable to handle such systems, mainly because of the uncommonly high number of required I/O (hundreds of gating signals and measurements). Besides, no suitable commercial product was either existing in order to implement low-cost and low-voltage submodules as well. Hence, given that only few practical implementations of MMCs had been reported at that time [38], [42], [54],[1] an interesting research potential was perceived, giving rise to a strong will to develop *in-house* an extensive knowledge about practical implementation issues.[2]

Owing to these motivations, a significant part of the present work has been dedicated to the development of a laboratory test platform aimed to support the experimental validation of the present work, but also that of other research activities conducted in the same laboratory [15], [199]. Hence, joint efforts were made to develop a prototyping system, that should be as flexible and as versatile as possible. Its main elements are briefly presented in the following sections.

4.1.1 POWER SECTION

The main converter ratings were chosen such as to allow the implementation of a transformerless connection to the 230V / 50Hz grid. These specifications are summarized in Table 5 and justified by several considerations :

– Few levels are sufficient for a *proof-of-concept* in a laboratory-scale prototype.
– The apparent switching frequency is selected to resemble the one of industrial systems (typ. 10-200 kHz). This implies a rather high actual switching frequency for the prototype (in average, several kHz per cell instead of a few hundreds Hz), but emphasizes the realism of the digital control at the expense of the energy efficiency.

1. Engineers from KTH, Stockholm, Sweden were also at the commissioning phase.
2. Simultaneously, a extensive re-design of the general-purpose control platform of the laboratory was starting, rising opportunities for synergies between both developments. This system has been recently presented in [142].

– The corresponding requirements in terms of galvanic insulation do not exceed what is commonly available in low voltage applications (optocouplers, power supplies, etc..) and require no special safety measures in terms of operation, handling, etc.

Quantity	*Nominal value*	*Min./max. value*
AC line-to-line voltage [$V_{L(l\text{-}l)}$]	400 V_{RMS}	±10%
AC line current [I_L]	>14 A_{RMS}	>50 A (inst. max.)
DC bus voltage [V_C]	500 V_{DC}	800 V_{DC}
Submodule voltage	150 V	200 V
Summed capacitor voltages [V_x^{Σ}]	600 V_{DC}	800 V_{DC}
Apparent switching frequency [F_S]	10 kHz	0 Hz - 20 kHz
Total number of cells per arm [N]	4	–
Isolation voltage between cells [V_{iorm}]	>560 V permanent	>3kV peak
Grid frequency [f_0]	16,7 Hz and 50 Hz	–

Table 5. Key specifications of the developed laboratory prototype.

4.1.1.1 CONVERTER ELEMENTS

As to guarantee a maximal flexibility, the various arm elements have been designed using separate modules that are assembled using 19" rack-mount material:

a) Converter cells (submodules)

The developed submodules (see Fig. 87) support both half- and full-bridge operation through a simple terminal selection. Their electrical scheme is given in Fig. 86.[3] The design aim for a low-cost implementation and reflects a few key choices:

– The maximum DC voltage of V_{SM} = 200 V allows for a direct connection of the converter to the 230/400 V domestic network with N = 4 cells per arm.
– IGBT or MOSFET devices can easily switch more than 40 A at the desired frequencies with a thermal power losses budget of 10 W per half-bridge (typ. IRFB4332).
– The embedded A/D converter provides the measurement of the capacitor voltage through the dedicated SPI interface (up to 5 ksps).

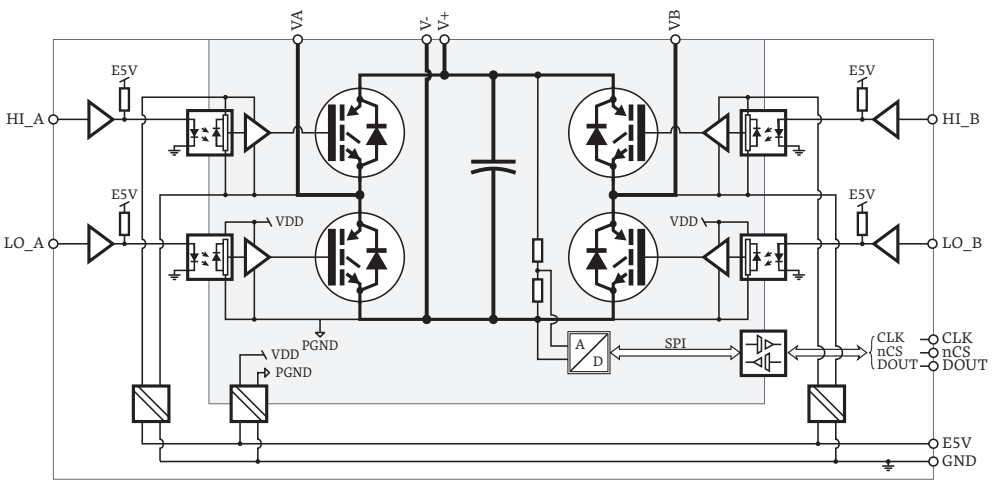


Fig. 86. Schematic of the implemented MMC submodules.

3. Studying the schematic, the reader may identify some design flaws that are dating back from the first production batch of 40 submodules in Fall 2009.

b) Arm currents measurement cells

This board can measure up to two arm currents and is meant to be typically placed in the middle of a phase-leg. Besides, for each current, two data channels are available :

– The onboard transducers and A/D converters provide ***digital outputs*** through the dedicated SPI interface (up to 5 ksps). These values is used by the FPGA-based local controllers (see §4.1.2.3 *b.*) in order to achieve the cell-level balancing.
– Improved measurement bandwidth is available via the routing of the ***analog signals*** to the ExtIO measurement boards (up to 100 ksps, see §4.1.2.3 *c.*). Along this second data path, the values are used for the global converter control.

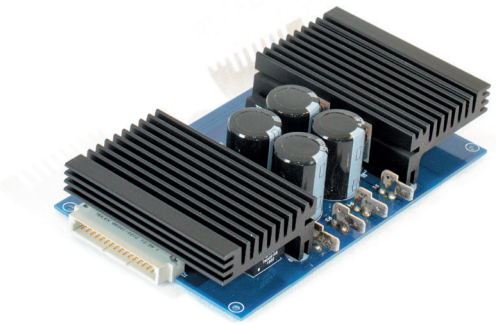


Fig. 87. Photograph of the configurable half- or full-bridge submodules.

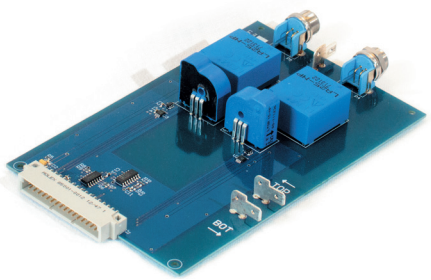


Fig. 88. Photograph of the arm currents measurement cells.

c) Phase-legs

Up to eight submodules and one current measurement cell can be assembled within a 3U 19" rack mountable chassis. Using such a configuration, one 3U chassis can be implemented with either two arms of N=4 cells or with one arm of N=8 cells. Fig. 89 illustrates the corresponding mechanical design. In both cases, the chassis backplane is responsible for carrying all the necessary gating signals (5 V logic) and power supplies as well as some additional status and error signals back to the dedicated FPGA-based local controllers (§4.1.2.3 *c.*) through a shielded 50 pins connector.

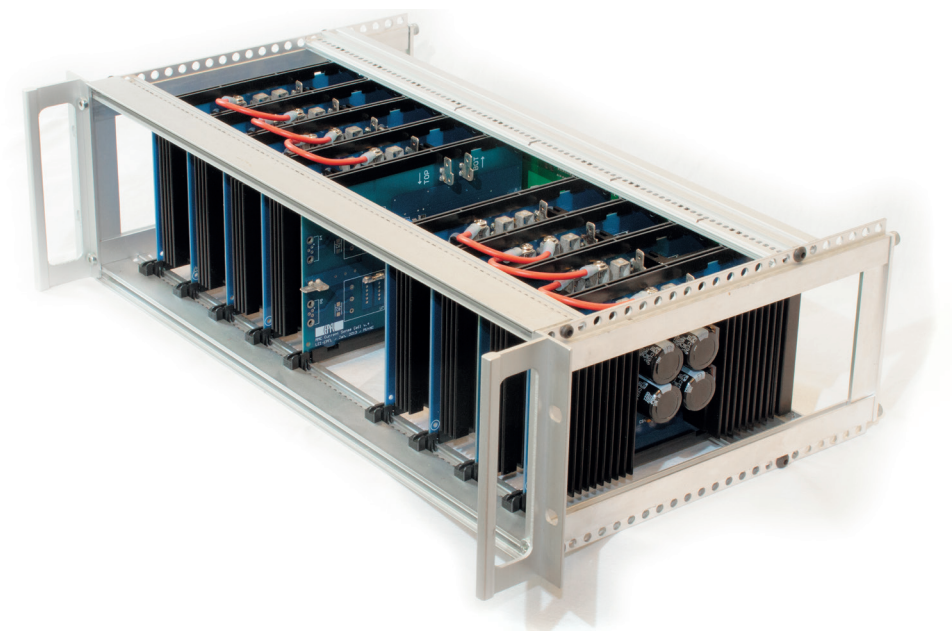


Fig. 89. Photograph of the 19" phase-leg racks with 1x N=8 or 2x N=4 submodules per arm.

The backplanes of the rack units are also responsible for multiplexing the SPI data channels between the different modules and the corresponding local controllers. Hence, the submodule voltages and arm currents values are retrieved *sequentially*, what minimizes the aggregated bandwidth requirements. The global communication structure depicted in Fig. 91.

d) Inductors

The inductances required by the control of the bus and line-side currents have been implemented using non-coupled arm inductors, combined with line-side inductors. The arm inductors have been designed and wound in-house using a powder core material and standard stranded copper wire. The arm inductors are directly mounted inside the phase-leg racks, while the line inductors are conventional laminated steel-based inductors installed at the bottom of the cabinet (see Fig. 90).

e) Cabinet-level construction

Owing to this approach, a very versatile platform is available in order to build various converter configurations with a high flexibility. Fig. 90 shows some photographs of the complete system in its maximal configuration, corresponding to 3-phase to a 2-phase AC/AC indirect conversion application. As illustrated, some additional hardware is also present:

– The external quantities such as grid- and bus-related quantities are measured using a dedicated custom-designed board providing the necessary 12 voltage and current measurements for the grid-related quantities.
– A current limiting circuit is available for precharge, and can be bypassed during normal operation. The corresponding relays and circuit breakers are also implemented in the central part of the cabinet, along with the power supplies.

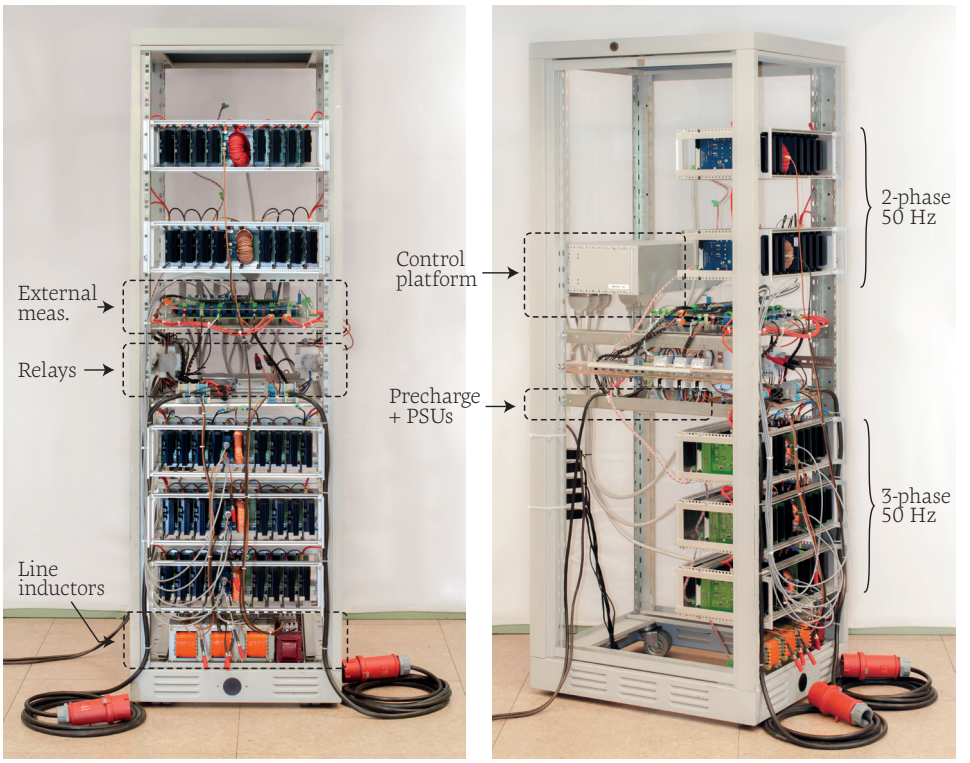


Fig. 90. Implemented prototyping platform in indirect 1-AC/DC/3-AC configuration.

4.1.2 CONTROL SECTION

As presented by §4.1.1, with such an approach, the design of the power section can be relatively straightforward. On the other hand, since no "intelligence" is embedded in the corresponding circuits, both the control and the protection of the entire system remain of the sole responsibility of the control platform. Hence, beyond the converter control software –in the algorithmic sense of the word– the corresponding hardware implementation is not an easy task.

4.1.2.1 MAIN CHALLENGES AND MOTIVATIONS

Most generally, the high scalability of MMCs as well as cost considerations generally encourage the design of converters constituted by a high number of cells. This results in a high number of gating signals and a high number of state variables that must be controlled. Exemplarily, the implemented prototype features up to 96 power switches (planned up to 160 switches with split energy storage) and more than 40 independent state variables (more than 120 with split storage). This being said, even though most of these subsystems are –taken separately– very basic, their addition is generally recognized as to pose real control challenges, especially in terms of:

- *Data communication bandwidth.* Typically, 10 - 100 kbps per cell and kHz of apparent switching frequency.[4] In total, this results in several tens to hundreds of Mbps of raw data transfer for a few hundreds of cells per arm. Moreover, even higher physical throughputs are required provided that the time window dedicated to communication shall be only a fraction of the sampling period.
- *Processing power.* Considering that the above-mentioned quantity of data shall be processed in due time, a significant computational burden is also observed.[5] Besides, the high apparent switching frequencies that result from the use of numerous cells give rise to high control bandwidths that are very beneficial to closed loop control algorithms, but that can only be fully exploited with short interrupt periods.

Facing these constraints, one essential conclusion emerges: the control section must be strongly layered and hierarchized as well as highly specialized in order to:

- Reduce the throughput requirements (communication and processing power) by dividing/disaggregating the various data paths and maintaining at the local level all the informations that may not necessarily require to be brought back to the highest control level(s).
- Allow to best select the processing units depending on the specificities of the tasks that must be performed, typically: devices optimized such as digital signal processors (DSPs) for sequential arithmetical operations and logic-type devices (FPGAs) for mostly concurrent computing tasks.
- Offer similar levels of both flexibility and reliability as the power section inherently provides. Modularization is also here a key benefit on that matter, as well as towards the implementation of redundant mechanisms.

Owing to these observations, the implemented control platform is a fully custom-made system, which is further described in the sequel.

4. This is a rough approximation assuming a Marquardt-type top-down modulation and balancing approach. See §1.3.5, page 15.
5. In turn, the aggregated data bandwidth that must be processed is relatively similar to the ones involved in real-time video processing applications.

4.1.2.2 CONTROL HARDWARE ARCHITECTURE AND HIERARCHIZATION

Owing to the above considerations, the choice of the control hierarchy is crucial. This is particularly true with respect to the communication scheme between the various computing elements. A possible solution is given by the hardware architecture depicted in Fig. 91, which is the one actually implemented on the prototype:

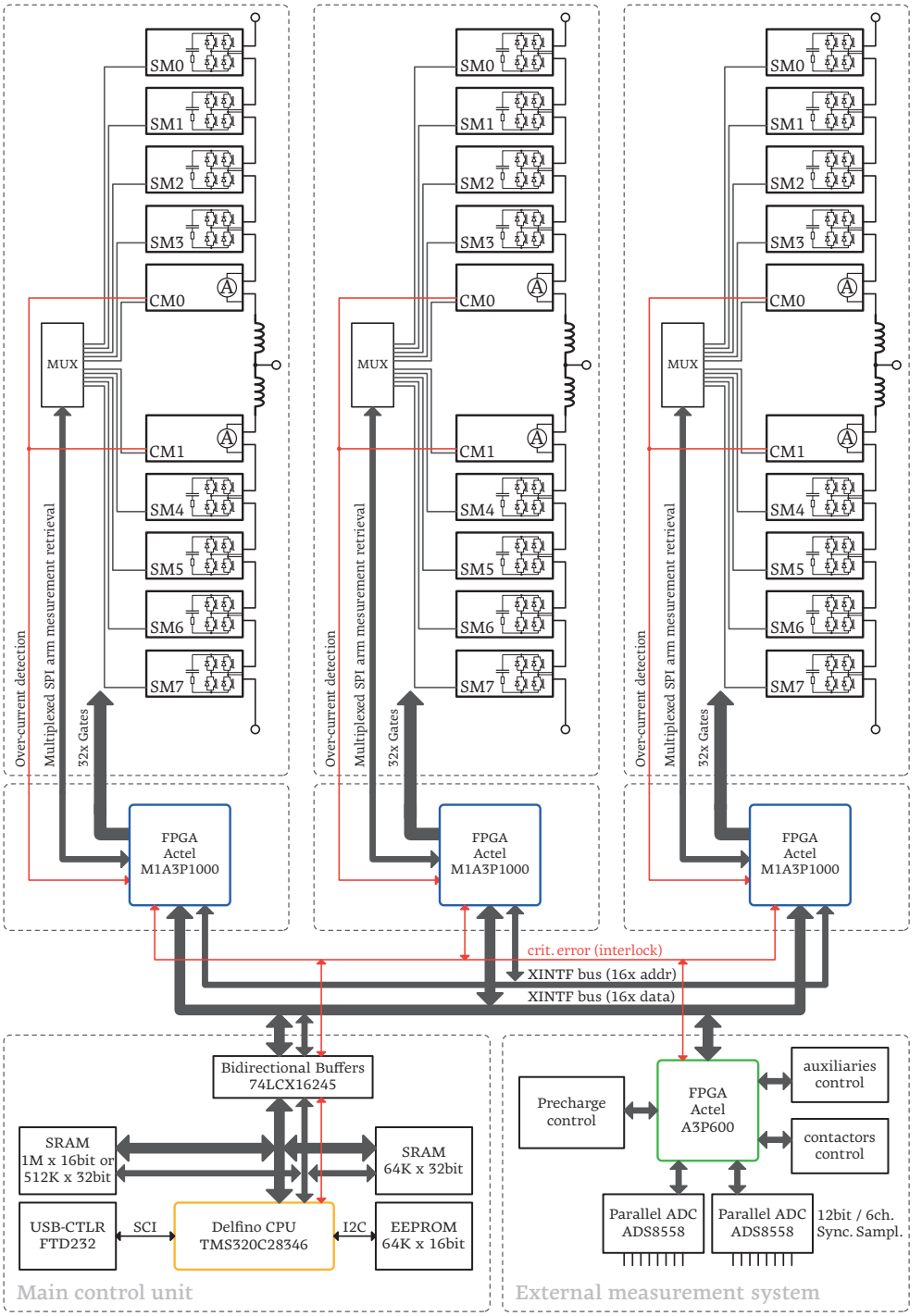


Fig. 91. Global communication structure of the implemented prototype. One central controller based on a floating-point DSP is communicating with several FPGA-based slaves through its external memory bus. The employed colors correspond to those in the dataflow diagram of Fig. 92.

Several reasons are motivating the choice of such a control structure:

1) The general software control tasks (in the sense of Chapter 3) are achieved by a master control unit based on a floating-point DSP that is programmed in C and C++ language (in yellow, see also §4.1.2.3 *a.*).

2) The cell-level balancing as well as all modulation-related concerns are kept at the arm/phase-leg level through the use of a dedicated control units (in blue, see also §4.1.2.3 *b.*). The latter are chosen to be based on FPGAs due to *i)* the high number of necessary digital outputs, *ii)* the full-custom implementation required by the modified SPI busses, *iii)* the time-deterministic nature of its operation (essential to the modulation) and *iv)* the potentially highly parallelized implementation of some control loops. By doing so, each arm, along with its associated controller, is turned into a self-balanced subsystem that can be transparently controlled via a single modulation index only.

3) The measurement of non MMC-specific quantities (such as bus and line currents and voltages) requires an increased bandwidth compared to *1)* and correspond to varying needs, as a function of the application. Therefore, these measurements are chosen to be done externally, using an additional reconfigurable board designed to that end.[6] Besides, a dedicated signal conditioning and A/D conversion interface has also been designed as to make these informations available to the to master controller (in green, see also §4.1.2.3 *c.*).

Importantly, the choice of the DSP's memory bus as the communication backbone between these various devices is not only offering a high-bandwidth bidirectional communication path, but is also and more importantly offering a low-latency direct access for the DSP from and to its FPGA-based subsystems.[7]

In the end, a relatively distributed control implementation is made possible, involving three different types of control units and various dataflows. Fig. 92 shows the different functional blocs as well as their distribution among the units, which are related to the data exchanged summarized in Table 6 on the next page. The master controller is represented in yellow, the local arm controllers in blue and the external IO interface(s) in green:

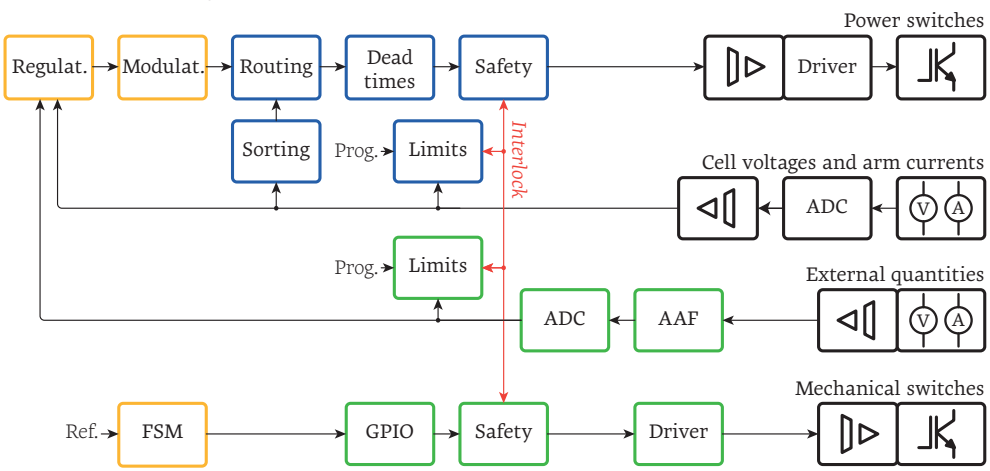


Fig. 92. Functional dataflow diagram of the MMC prototyping platform.

6. The latter also embeds the interface necessary to the control of the relays. See Fig. 90.
7. On the other hand, this element also remains the main bottleneck of such a highly hierarchized control design. Section 4.4.3 provides further comments on that matter.

	Motherboard (DSP)	Arm Controller (FPGA)	IO Board (FPGA)
Input data	• Pre-processed data from other boards (measurements, status flags, etc.) • User inputs and commands	• Raw measurements (cells voltages and arm currents) • Modulation data	• Raw measurements (external quantities) • FSM status flags
Output data	• Modulation data (number of active cells and duty-cycles) • Operation mode and various status flags	• Summed capacitor voltages • Status flags	• Pre-filtered measurements • Status flags
Tasks	• Supervisory controls (operation mode, strategies, etc.) • Low-level controls (regulation, tracking, etc) • Modulation (part of)	• Modulation (part of) • Cell-level balancing • Safety	• High-bandwidth measurement pre-processing • Control of the auxiliaries • Safety

Table 6. Control tasks distribution of the implemented control platform.

Practically, the use of this dedicated memory bus allows for a relatively simple implementation, thanks to the fact that the corresponding FPGA-implanted dual-port memories and registers can be directly mapped into the DSP's address space. On the other hand, the use of such a general-purpose and protocol-free communication system also possesses several drawbacks that turned out to be the heart of the main implementation issues of the whole prototype :

– No data integrity check is available (CRC, 8b-10b encoding, etc.)
– The use of a parallel bus poses severe constraints in terms of maximal length and EMC performance.[8]
– Clock dissemination is difficult to implement (especially with respect to syntonization) what is nevertheless key in such distributed modulation architectures.

Finally, as shown by Fig. 91 and Fig. 92, a protection scheme similar to the one of [142] has been implemented. It relies on safety thresholds that are pre-programmed for each measured quantity, and which trigger global error flags (interlock lines) according to various severity levels.

4.1.2.3 HARDWARE IMPLEMENTATION OF THE CONTROL UNITS

In practice, the control platform is implemented using several boards communicating through a common backplane. Fig. 93 depicts the complete control platform. Its constitutive boards are presented in the following paragraphs.

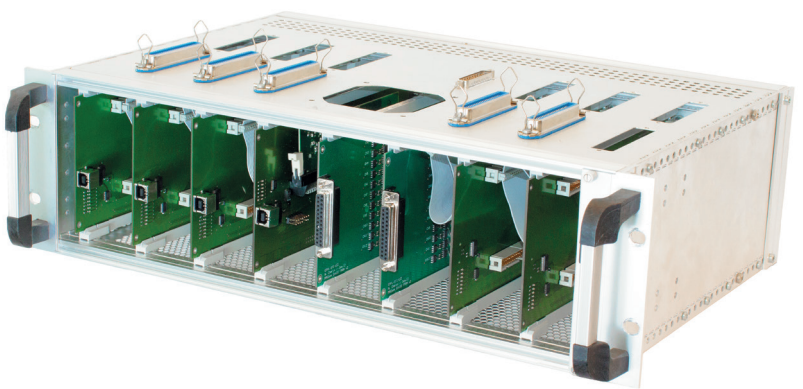


Fig. 93. Complete MMCbox with 1 master controller, 5 local controllers and 2 external IO boards.

8. Practically, the various control boards must be close to each other, what seriously limits the possible "geographical" distribution of the overall control system.

a) DSP-based motherboard

This board embeds a TI TMS320C28346 controller card which hosts the DSP and its related memory and power supplies. It also carries logic drivers for the backplane signals and a basic communication interface to the computer host (UART over USB and debugger). As a matter of fact, this board is a lightened version of the motherboard of [142], which was developed simultaneously.

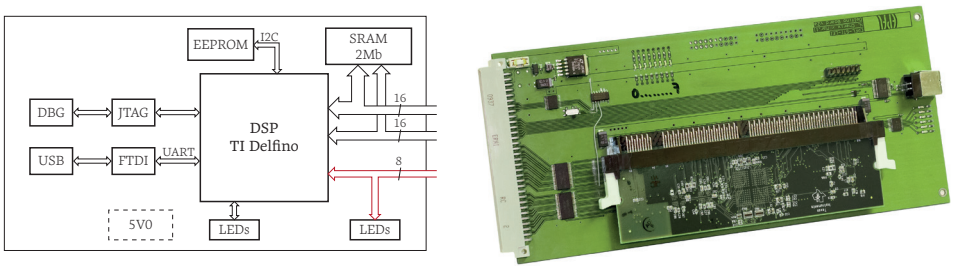


Fig. 94. DSP-based master controller board.

b) FPGA-based local controllers

The phase-leg controllers are based on Actel's AP31000 flash-based FPGAs, featuring one million logic gates. This choice leads to a relatively straightforward board design, as most of its functions are embedded inside the FPGA. Besides, as high pin-count and direct connectivity is provided to the power section through two multi-pin connectors, shielded at the enclosure level.

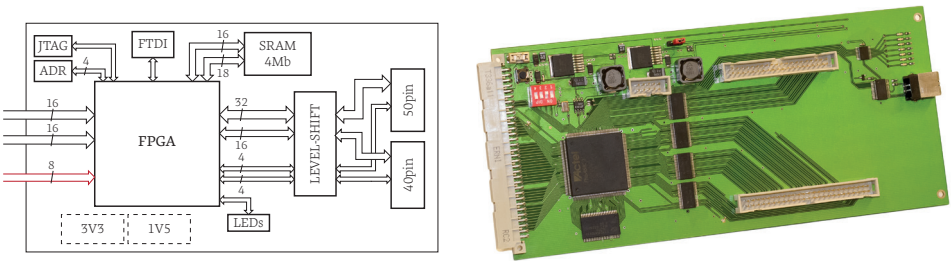


Fig. 95. FPGA-based local arm controller board.

c) FPGA-based acquisition interface boards

The external IO boards embed a basic analog front end with twelve simultaneously-sampled 16 bits analog-to-digital conversion channels. Additionally, 16 general-purpose digital outputs are also provided in order to command the auxiliaries.

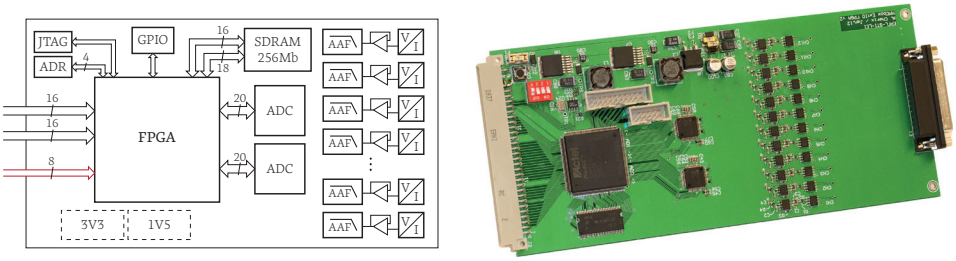


Fig. 96. FPGA-based external IO board.

Overall, configured as in Fig. 93, the MMCbox can handle up to 240 power switches, 160 low-bandwidth measurements, 24 high-bandwidth measurements and 32 general-purpose IO signals (relays, etc.).

4.2 SOFTWARE IMPLEMENTATION

The implementation of the corresponding software is split between the programming of the DSP (in C/C++) and the synthesis of the logic circuits for the two FPGA-based peripherals, which are described in VHDL.

In practice, the logic circuits of the two FPGAs can developed such that their various functional units appear as fictive peripherals to the master controller (the DSP). Hence, an very transparent architecture can be built, which features a similar behavior as a unique and highly specialized "macro"controller.

Owing to this approach, the lower software layers can be set up relatively easily, provided that the corresponding drivers are developed on the DSP side as well. Besides, the upper layers can be written such as to possess some portability. In turn, the overall software architecture very much resembles the one of [142], with which it shares many features. Concretely, both systems are organized into three main layers :

- A *driver layer* that provides reusable routines allowing a transparent access to all the FPGA-based peripherals as well as the communication with the computer.
- A *core layer* responsible for controlling the execution of the DSP and the overall application. All the safety-related feature are in turn implemented within this layer.
- A *user layer* that contains all the routines that are specific to the application. In other words, this is the "top of the iceberg" that corresponds to the control software in the sense of Chapter 3.

4.2.1 LOW-LEVEL ALGORITHMS

Owing to the chosen control hierarchy, most of the low-level and fast control tasks are maintained and processed at the local level by the corresponding FPGA-based peripherals. Based on the necessary set of functions (see Fig. 92), various peripherals have been synthesized :

- *CLK* units are responsible for managing the various processing rates (acquisition, modulation, communication, etc.) through the generation of the shared and/or local clock resources.
- *SUP* units are supervising the overall execution of the controller boards (operation modes, fault detection and reporting, status signals, initialization, etc.)
- *ACQ* units are in different types of peripherals managing the communication with their respective ADCs (3 types). Besides, they provide the same kind of threshold-based fault detection as developed in [142], but here implemented in the digital domain. The corresponding overvalue flags are obviously shared with SUP units.
- *PWM* units are configurable sets of conventional two-level modulators whose VHDL description is shared with [142]. They are meant to be used with additional power electronics interfaces in particular in each submodule (see §5.1.2 and [199]).
- *GPO* units are general-purpose digital outputs, here used to control the auxiliaries .
- *ARM* units are multilevel modulators tailored for MMC arms that also include the necessary balancing mechanisms. As such, they have a direct "spy" access to the arm-level voltage and current measurements.
- *SDR* units shall be responsible for managing the embedded SDRAM memories for datalogging purposes. This functionality has however not been implemented yet.

Fig. 97 and Fig. 98 show the corresponding logical structure with its main peripherals :

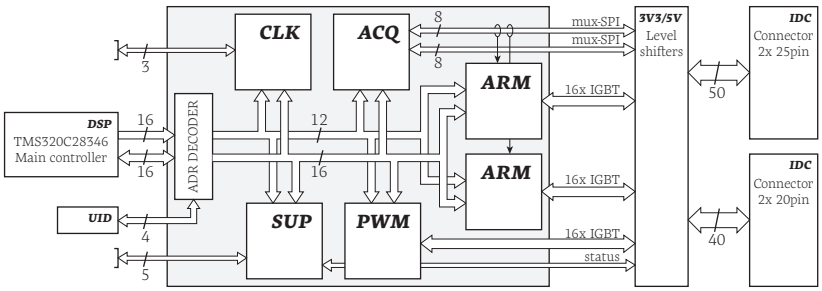


Fig. 97. Toplevel structure of the FPGA-based I/O interface boards.

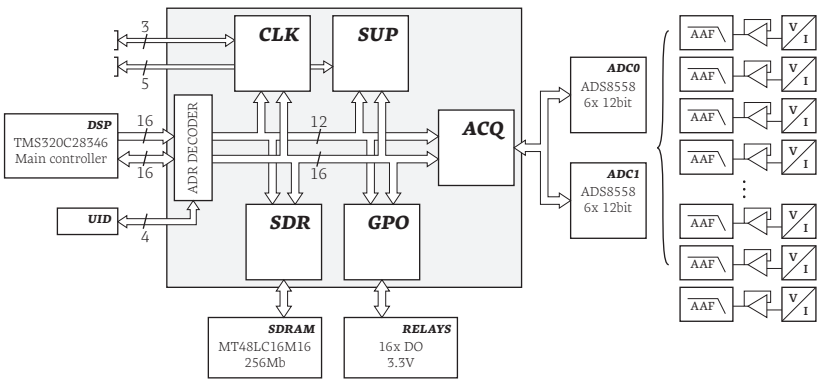


Fig. 98. Toplevel structure of the FPGA-based local controller boards.

On the DSP side, the access to these peripherals from the higher-level control function is authorized through the *driver layer*, which provides the necessary pre-compiled and optimized routines and make them directly appear as fictive peripherals to the DSP.

Overall, most of these peripherals correspond to relatively conventional signal processing and conditioning tasks that are not specific to the control of MMCs. To the contrary, one type of unit, the ARM peripheral block, is worth a particular attention, as the latter constitutes one of the key elements of the infrastructure and is the heart of several challenges. It is briefly presented afterwards.

4.2.1.1 IMPLEMENTATION OF THE **ARM** MODULATOR UNITS

For the present prototyping system, a Marquardt-type approach has been chosen for its more transparent top-down implementation (see §1.3.5). The general structure and principle of operation of this unit is illustrated in Fig. 99. It contains essentially three sub-systems : *i)* a waveform generator / modulator, *ii)* a sorting engine and *iii)* a state decoder with integrated dead-times.

As it can be understood from the schematic, such an implementation technique guarantees that only one cell is switched at a given time for both types of transitions (rising or falling between levels). This inherently ensures an optimal ratio between balancing performance and quality of the produced waveforms (see §1.3.5). On the other hand, unlike for Akagi-type balancing approaches, the implementation of such a balancing scheme inevitably relies on processes operating at different sampling rates, whose difficult selection is related to several considerations, presented in the sequel.

More specifically, with such an approach, the main issues consist in *i)* selecting the appropriate type of sorting method and *ii)* choosing at which frequency this sorting must be achieved respectively to the apparent switching frequency and the capacitor voltages sampling frequency. By way of example, the present case is shown in Table 7:

	Freq.	Domain	Triggered processes	Impact on...	Issues...
ACLK	40 Mhz	Local	• Sorting timebase • Main state machine	• PWM resolution • Maximum *dV/dt* on EMF	• Synthesis
BCLK	2 Mhz	Local	• Measurement retrieval (SPI)		• EMI sensitivity
CCLK	80 kHz	Local	• Sequential data retrieval (SPI) • Sorting (triggering event)		• Sync. sampling • Data bandwidth
SCLK	4 kHz	Global...	• Sampling interval	• Sorting performance	• Sync. sampling
DCLK	10 kHz	Global...	• Apparent switching frequency	• THD vs. switching losses	• Clock resync.

Table 7. Processing rates in the arm modulator/balanced as implemented on the prototype.

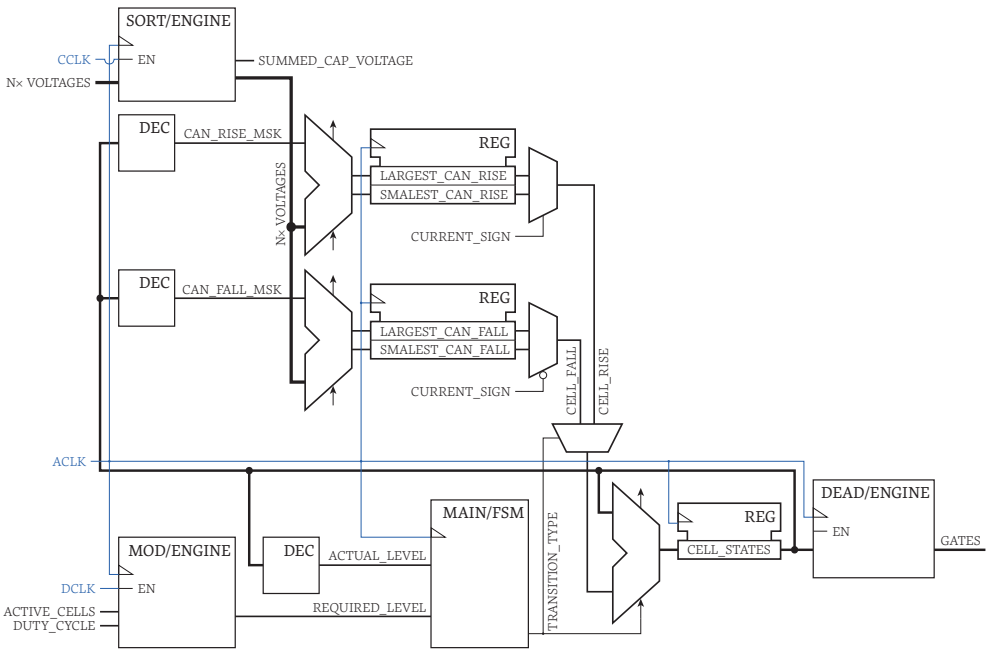


Fig. 99. Top-level schematic of the modulation/balancing peripheral implemented in the FPGA-based arm controllers.

In the present example, the adopted sequential measurement retrieval technique reveals to be simple and well suited for the subsequent sorting as it allows enough time between consecutive data "arrivals" for the sorting to take place.[9] On the other hand, this also results in the non-simultaneity of the sampling of the capacitor voltages, what is an impediment with respect to their control in closed-loop.

That said, more generally, as the state of only one cell is changed at every switching instant, the overall result of the voltages sorting changes relatively *slowly* and does not need to be refreshed very often. The sorting can hence be executed much slower than the apparent switching frequency (and even slower than it is implemented here). On the other hand, as the selection of the cells must proceed anyway, the necessity to be able to select the second, third, fourth etc. most charged/discharged cells requires that

9. This is one possibility among others to reduce the necessary total data bandwidth, what is a driving design factor with a high number of submodules (typ. N > 100).

the corresponding information is available, or is other words that more than one cell is ranked. This encourages the use of a *slowly run full sorting algorithm* rather than a min-max sorting approach that runs close to the apparent switching frequency.[10, 11] This is the approach that has been chosen here. Overall, the main benefit is that the capacitor voltages can be sampled significantly slower than the apparent switching frequency, what it essential to reduce the corresponding communication bandwidth requirements.

Among the numerous full-sort algorithms that can be considered,[12] the *bubble-sort family* of algorithms offers various time vs. area trade-offs and operates fast with data sets that are almost sorted (what is the case of the capacitor voltages when the algorithm is applied recursively). In the present case, the implemented algorithm is derived from [143], owing to *i)* its excellent scalability, *ii)* good applicability to real-time applications and *iii)* affordable total time × area cost.[13]

Overall, it is important to note however that the use of a full sorting algorithm shall not be confused with non-minimal switching effort, as the latter is only defined by eq. (1), page 16. Besides, one can reasonably argue that there is no point in introducing switching events that are not "visible" on the output EMF as they only imply a sub-optimal ratio of actual vs. apparent switching frequency.

Furthermore, Table 7 is also reminding that numerous clock domains are inevitably at stake with such distributed control implementations, what poses significant synchronization challenges. For instance, in the present case, the ACTIVE_CELL and DUTY_CYCLE registers used to control the modulator (see Fig. 99) are clocked on the memory bus (i.e. the DSP basis), while the modulator itself is based on the FPGA's own clocking resources. This requires at least some sort of clock re-synchronization but, as the different phase-legs here belong to separate clock domains, some imperfections are inevitable in the generated PWM patterns. This is in turn one of the existing sources of imperfections in the switching patterns generated on the converter prototype. More generally, this encourages the use of not only synchronization, but also syntonization techniques among the various controller boards, what has regrettably not been implemented on the present prototype.

Finally, among the numerous possible improvements of the Marquardt-type balancing that are left for future work, it could be particularly interesting to address the issue of the *balancing of the switching duty*. Indeed, the minimization of the voltages unbalances may not always be an ideal objective in the very short term, as balancing "too well" may in turn result in unequal switching duties and hence unequal thermal constraints and ageing, for instance in case of parameter mismatch (e.g. capacitance

10. Typically a min-max algorithm only attempts to extract the largest, resp. the smallest value of a given set, without ranking the intermediate values. In contrast, a full sorting algorithm classifies all the elements of the set in a ascending of descending order.
11. Besides, in case a fast transient is required on the desired arm-level EMF, the successive selection of the switching cells must be achieved within a couple of ACLK anyway, requiring that the entire list of ranks is available at all times. This alone excludes the use of min-max algorithm, unless it is largely paralleled and can be run extremely fast (typically as fast as ACLK), at the cost of a large chip area.
12. An extensive comparison of these algorithms is provided by http://en.wikipedia.org/wiki/sorting_algorithm.
13. Assuming that 20 sorting units are used, the *worst-case* sorting time for N = 200 values is 8'040 clock cycles, that is to say approximately 200 us based on similar FPGA performance as on the prototype.

variations). To the best of the author's knowledge, there has been no studies regarding "how well" should the balancing perform, but it is indeed one of the potential drawback of the Marquardt-type balancing with respect to the Akagi-type balancing that the "balancing performance" is more complex to quantify and that other balancing objectives may be difficult to take into consideration.

4.2.2 EXECUTION CONTROL

On top of these low-level mechanisms, the execution of the main control tasks is controlled by a similar *core layer* as in [142], which handles:

- The configuration and the initialization of all peripherals (default parameters, calibration values, etc.).
- The proper synchronization of the sampling and the modulation.
- The supervision of the hard real-time execution of the upper layer.
- The management of the various fault sources[14] through various severity levels.

In the present case, a unique interrupt-based routine is used for the digital control of all state variables, whose level of priority is only superseded by fault management procedures. More information about these mechanisms can be found in [142].

4.2.3 APPLICATION-LEVEL ROUTINES

Superposed to the two previous levels, the highest software level contains the application-specific part of the control software, which is edited depending on the implemented converter configuration. This so-called *user layer* is where the control schemes presented in Chapter 3 are implemented.

The execution of this part of the software is organized using a finite state machine that manages the different modes of operation (pre-charge, current control, voltage+current control, which grid is connected, emergency shut down, etc.). In each of them, various control routines are responsible for the closed-loop control implementation of the relevant state variables. In all cases, relatively widespread digital control techniques have been used, such as:

- Multivariable PI current controllers [144] in positive-sequence rotating reference frame in case of three-phase symmetric grid conditions.
- Fictive-axis emulation-based dq current control [145] for single-phase applications, although proportional-integral resonant controllers [148] could be also used for the same purpose.
- Decoupled double synchronous frame reference (DDSRF)-based current control techniques [150]-[151] in case of three-phase asymmetric grid conditions.

Besides, grid synchronization is ensured through various types of software phase-locked loop (PLL) techniques[15] depending on the grid configuration:

- Conventional *dq*-type PLL for symmetric three-phase grid configurations.
- Second-order generalized integrator (SOGI)-based PLL for 1-phase cases [146]-[147].
- DDSRF-based PLL [149] in case of three-phase asymmetric grid conditions.

14. Typically, in case a phase-leg has been blocked due to an overvalue, in case the hard real-time has been violated, or in case of software error (overflow, division by zero, etc.).
15. The implementation details of these grid synchronization techniques can be found in their respective references.

4.3 EXPERIMENTAL RESULTS

In order to validate the basic principles of operation, this section first presents some results obtained in open-loop or partially closed-loop control operation. Subsequently, the full closed-loop control scheme presented in section 3.4.1 is exploited as to further validate the results presented in Chapter 3.

In the following results, the converter parameters correspond to the specifications provided in Table 5, page 110 and the parameters given below:

Submodule capacitance	C_{SM}	*1.3 mF*	*Line-side inductance*	L_{ac}	*4.0 mH (ESR=80 mΩ)*
Submodule ESR	R_{SM}	*100 mΩ (typ.)*	*Total arm inductance*	L	*1.5 mH*
Interrupt frequency	f_{CTRL}	*16 kHz*	*Mutual arm inductance*	M	*negligible*
Switching frequency	f_{ARM}	*16 kHz (4x 4 kHz)*	*Total arm resistance*	R	*>1Ω*

Table 8. Simulation parameters reflecting the implemented downscaled laboratory prototype.

Besides, all measurable quantities have been acquired using four GW INSTEK GDS-2204 oscilloscopes that are synchronously triggered by a dedicated signal generated by the DSP. By doing so, these measurements are also synchronous to the internal variables, which are retrieved directly from the DSP's memory.

4.3.1 OPEN-LOOP OPERATION

4.3.1.1 THREE-PHASE INVERTER

First, Fig. 100 shows the steady-state operation obtained with a three-phase inverter made of chopper cells, connected to a stiff and constant DC voltage source and operated in open-loop in a passive R-L load:

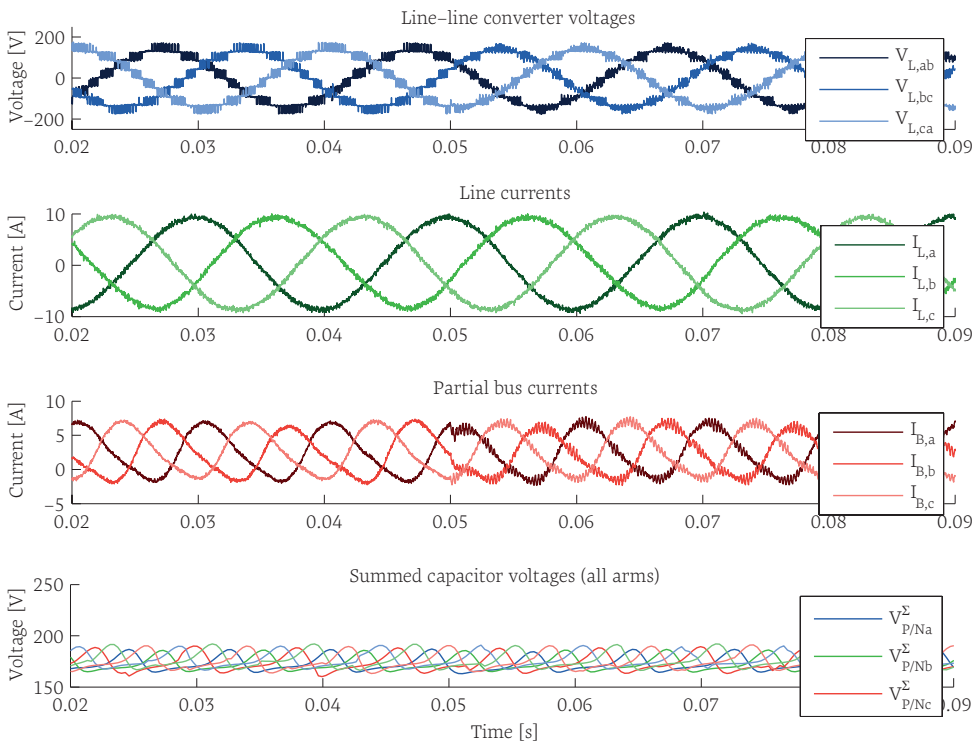


Fig. 100. Steady-state open-loop operation of the Dc/3-AC converter in a passive R-L load.

In the executed sequence, a fully open-loop modulation approach is used, which generates the modulation indices such as in (58). Besides, the modulation pattern is changed at $t = 0.05\,s$ from a N+1 level type of modulation to a 2N+1 level type of modulation (phase-to-neutral) by inverting the appropriate carrier signals.

$$m_p(t) = 0.5 \cdot \left(1 - \hat{m} \cdot \sin(\omega t + \varphi)\right) \quad m_n(t) = 0.5 \cdot \left(1 + \hat{m} \cdot \sin(\omega t + \varphi)\right) \tag{58}$$

The obtained results are typical of the open-loop operation of a MMC converter in such conditions, what can be recognized to the shapes of the summed capacitor voltages and the partial bus currents. Additionally, the change in the modulation pattern produces the expected change in the produced voltages, corresponding to 9 line-to-line levels when a N+1 level type of modulation is used (before $t = 0.05\,s$), and 17 levels when the carrier of the positive arm is flipped, corresponding to a 2N+1 levels modulation approach. As shown by these results, the impact of this change is clearly visible on the ripple of the partial bus currents. On the other hand, the opposed evolution of the line current ripple remains hidden in the measurement noise, due to the significantly larger value of the corresponding equivalent inductance.

4.3.1.2 DIRECT AC/AC CONVERTER

Second, a similar open-loop operation is executed on the three-phase 1-AC/3-AC direct frequency converter constituted of full-bridge cells. The converter is hence supplied with a 16.7 Hz stiff AC voltage source and is feeding a three-phase passive R-L load. The corresponding modulation indices are produced as in (59):

$$m_p(t) = \left(\frac{V_{bus}}{V^{\Sigma}_{\Sigma,0,ref}} - 0.5 \cdot \hat{m} \cdot \sin(\omega t + \varphi)\right) \quad m_n(t) = \left(\frac{V_{bus}}{V^{\Sigma}_{\Sigma,0,ref}} + 0.5 \cdot \hat{m} \cdot \sin(\omega t + \varphi)\right) \tag{59}$$

The obtained results are depicted in Fig. 101:

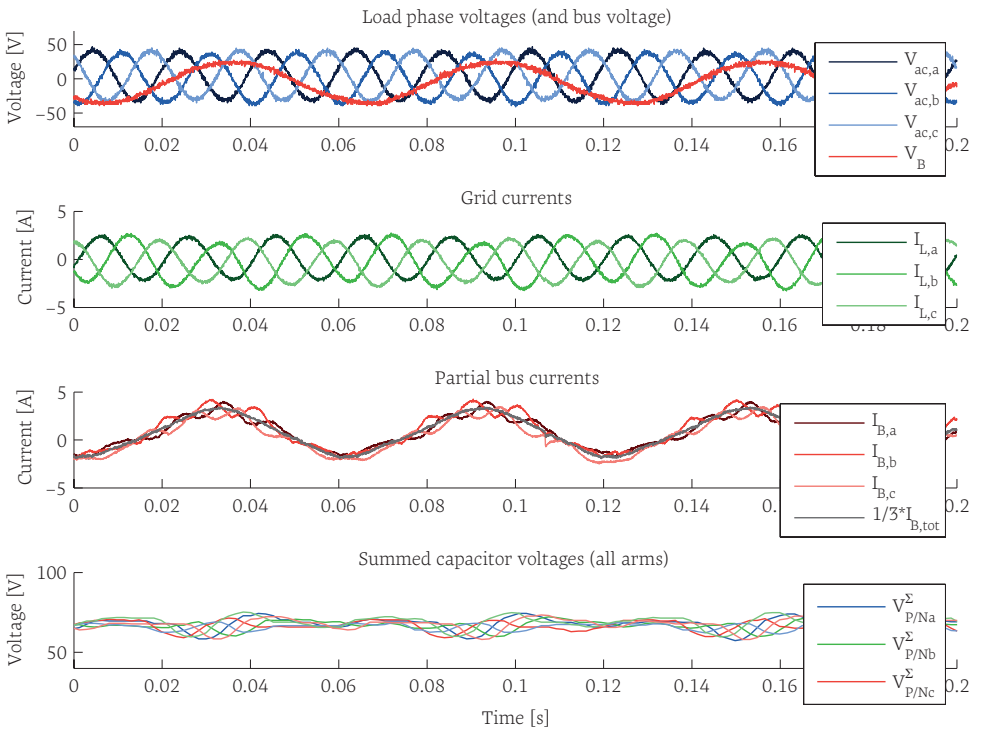


Fig. 101. Steady-state open-loop operation of the 1-AC/3-AC converter in a passive R-L load.

In the presented results, significant differences can be observed compared to Fig. 72, notably with respect to the shapes of the summed capacitor voltages and the partial bus currents. This is of course an expected result since the absence of any kind of closed-loop control prevents to act here on the shaping of these quantities. Besides, this results as well in imperfect waveforms (see the remaining 16.7 Hz component on $I_{L,b}$, for instance, or the obvious presence of a DC offset on the partial bus currents).

4.3.1.3 INDIRECT AC/DC/AC CONVERTER

Third, a last preliminary example is shown, featuring the operation of the five-phase indirect AC/DC/AC converter structure of Fig. 79. In this case, the converter is tied on both sides to the 50 Hz grid, using step-down transformers. Besides, only a conventional *dq*-type current control is used on both sides (with fictive axis emulation on the single-phase side), as well as a basic voltage controller for the intermediate DC bus, impacting I_d on the three-phase side. Hence, no control of any partial bus currents is achieved on any of the two AC/DC converters, nor any kind of explicit control of the summed capacitor voltages. The results to a complete power reversal are shown in Fig. 102, corresponding to the change of $I_{d,1ph}$ from $+5A$ to $-5A$ at $t = 167\,ms$:

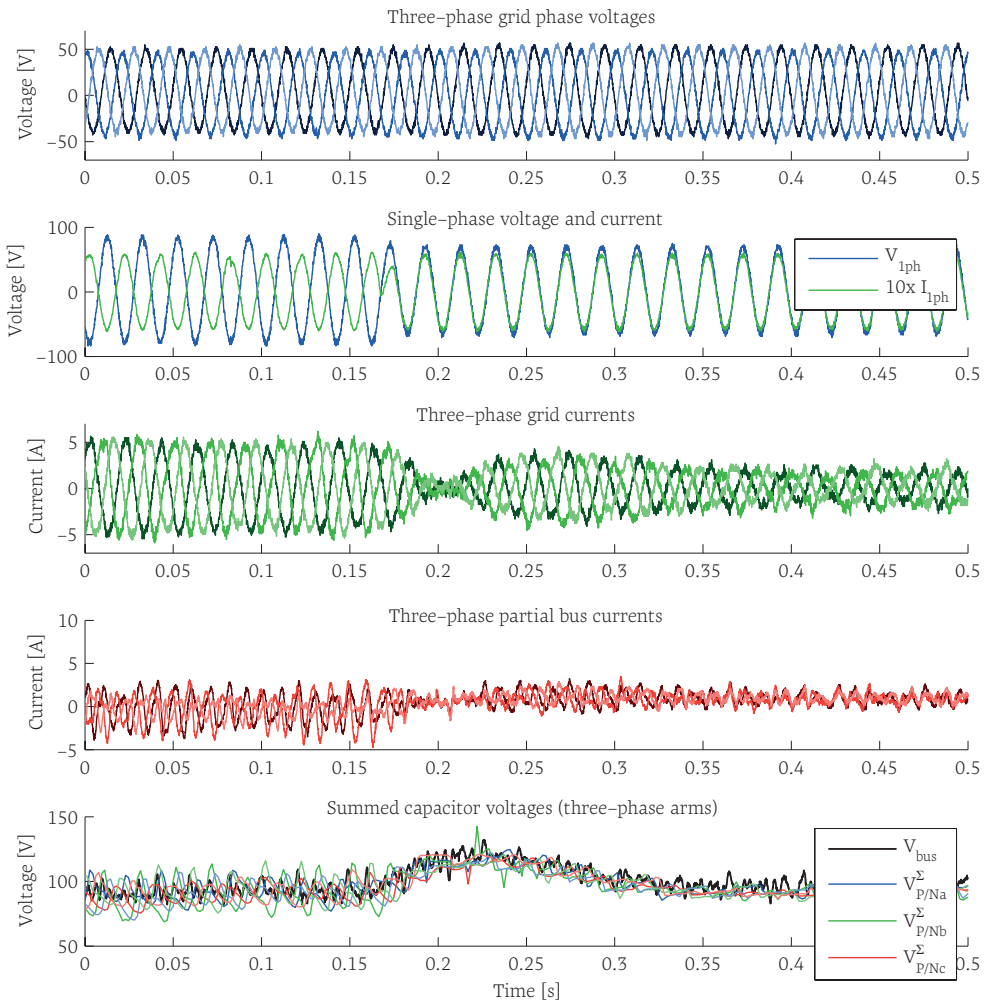


Fig. 102. Typical operation of the indirect AC/DC/AC converter, without circulating current control, nor any kind of control of the summed capacitor voltages.

Obviously, compared to Fig. 83, the executed transient results here in relatively slow dynamics. Besides, the absence of explicit control on numerous state variables leads to a difficult – and unformal – tuning of the bus voltage controller. Furthermore, due to the various uncontrolled (or poorly controlled) dynamics, rather distorted waveforms can be observed on the summed capacitor voltages and circulating currents.

In the end, provided that the closed-loop control of all state variables can be properly implemented – let's recall that this corresponds to a system combining four successive stages of power conversion – similar results as in the simulations shown in Chapter 3 could be achieved. This reinforces the motivations towards the development of closed-loop control techniques, which will be introduced in the next section.

4.3.2 COMPLETE CLOSED-LOOP OPERATION

4.3.2.1 THREE-PHASE INVERTER

Second, the effectiveness of the closed-loop control schemes developed in Chapter 3 is evaluated in several operating regimes on the converter structure of Fig. 26 using chopper cells.

In all these cases, the implemented control scheme is strictly identical to that of Fig. 63-Fig. 64, i.e. that simulated in Fig. 65-Fig. 66, except that the control parameters have been adapted to the actual prototype. The converter is thus current-controlled on both its sides and features the appropriate voltage control loops for the summed capacitor voltages superposed to its bus-side current control. In all these cases as well, the converter is supplied by a constant DC voltage source on its bus side and is tied to the 50 Hz grid on its line side through a variable auto-transformer.

The corresponding steady-state operation is shown in Fig. 103, while several other regimes will be presented in the subsequent figures.

In these results, it can be observed that the fast closed-loop control of the summed capacitor voltages along with the feedforwarding of (the image of) the instantaneous line-side power (see §3.4.1.2, page 80) allows to guarantee an almost perfectly constant total phase-leg energy. This thereby confirms the validity of this control design philosophy, which was first suggested by Bergna in [127] but apparently never confirmed experimentally. Furthermore, the remaining spectral components are as expected of even-order on the common-mode of the summed capacitor voltages V^{Σ}_{Σ} and of odd-order on the differential-mode voltages V^{Σ}_{Δ}. The corresponding current waveforms can be easily recognized on the partial bus currents as well.

Besides, these first results also constitute the opportunity to highlight some of the limitations of the achieved control performances. Indeed, the total bus current is obviously not as constant and smooth as in the corresponding simulations (typically, in the steady-state parts of Fig. 65), probably mostly due to remaining asymmetries in the converter structure, which are also visible in the partial bus currents. Additionally, some glitches are also visible on the voltages seen by the DSP,[16] which are most likely caused by a combination of factors involving data integrity issues in the employed voltage measurement retrieval and imperfections in the switching patterns.

16. As displayed in all these results, these summed capacitor voltages are largely down-sampled by the employed datalogging mechanisms (by a ratio of 25).

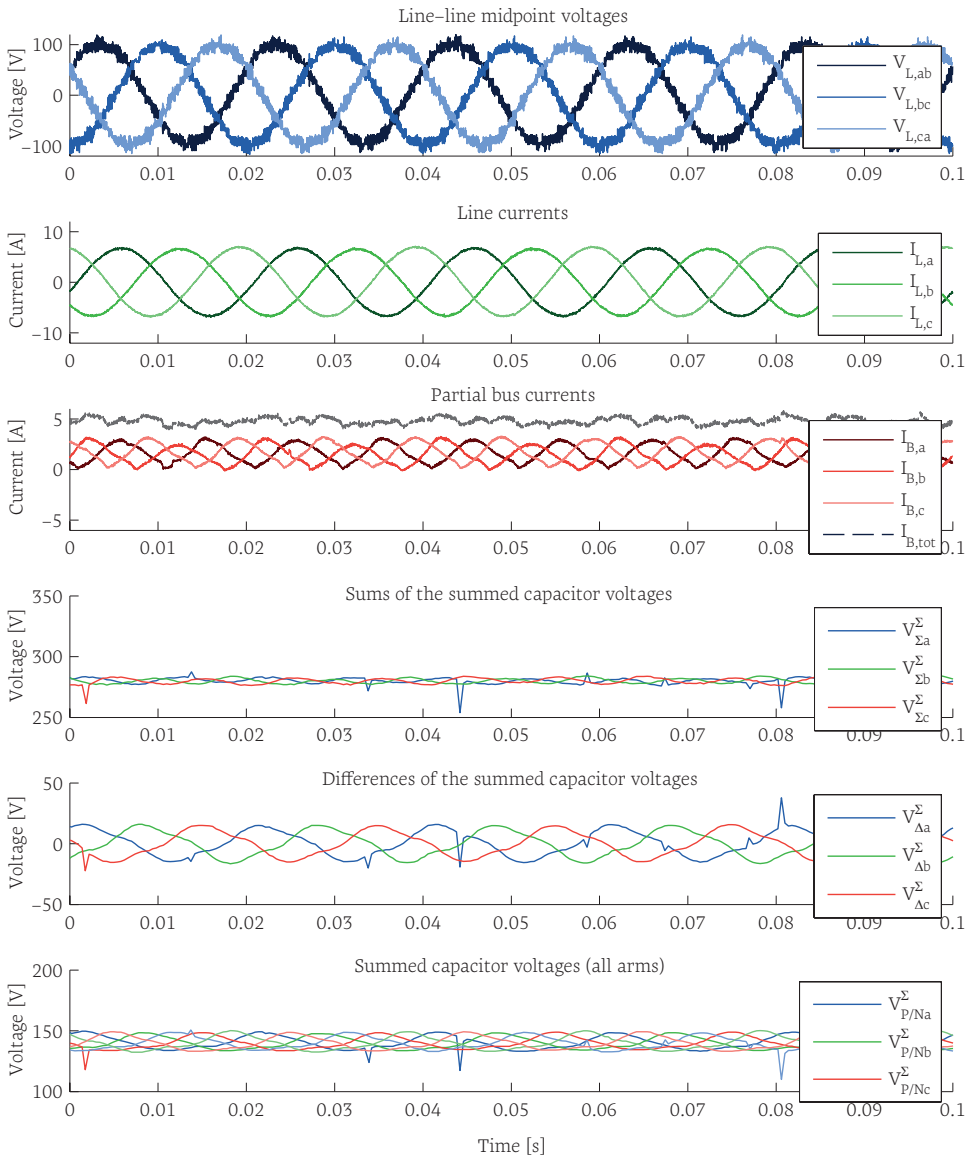


Fig. 103. a) Closed-loop operation in balanced grid conditions with $I_{d+} = 7\,A$.

Subsequently, in order to validate the effectiveness of this control scheme in a more comprehensive set of operating conditions, four different sequences are executed, corresponding to various transient regimes:

a) Active and reactive power flows reference steps

Fig. 104 shows the tracking performance corresponding to various active and reactive power setpoints using the control scheme of Fig. 64. In this sequence, two transitions are imposed to the line current values:

– At $t = 83\,ms$, the purely active power flow is reversed by changing I_{d+} from -5 A to 5 A.
– At $t = 266\,ms$, the current setvalues are changed to $I_{d+} = 5\,A$, $I_{d-} = -5\,A$ and $I_{q\pm} = 0$.

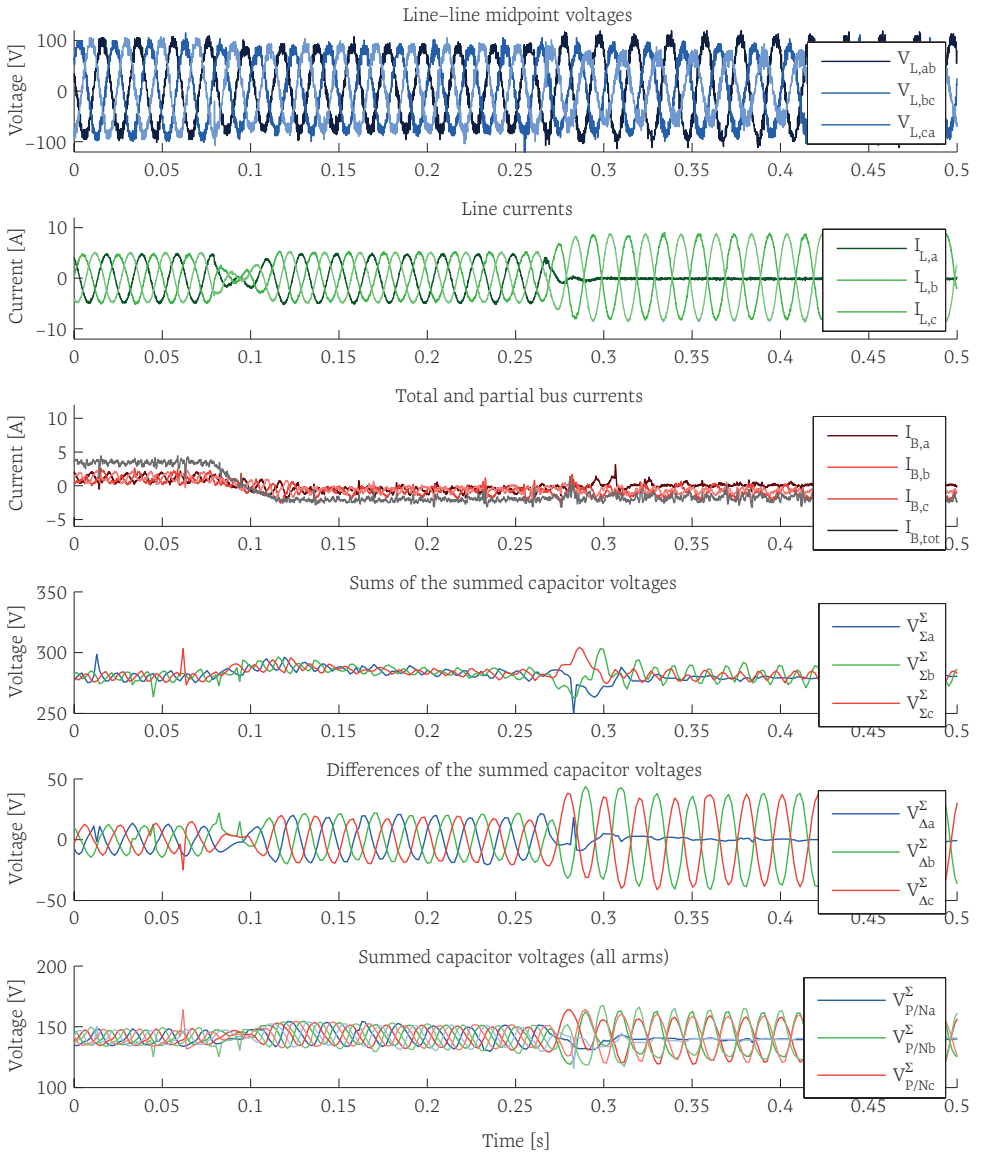


Fig. 104. Typical performance of the proposed control scheme under balanced grid conditions.[17]

As it can be seen, these results show stable dynamics and well controlled capacitor voltage ripples in all kinds of regimes. This concerns *i)* the amplitude of the ripple which is satisfyingly minimized through the constant reference values for the $V^{\Sigma}{}_{\Sigma,\alpha\beta}$ and *ii)* well managed transients thanks to the fast closed-loop control. Furthermore, when asymmetric currents are injected into the grid, the partial bus currents bear the necessary values and shapes as to maintain the total bus current to be an essentially plain DC value, despite the pulsating nature of the total line-side instantaneous power.

It remains to be demonstrated of course that the underlying energy management/ripple shaping strategy employed here corresponds to an actual minimization of the corresponding requirements in terms of embedded energy. On the other hand, this is not

17. As as side remark, it should be noted though that the significant imbalances in the converter voltages (particularly visible during the last part of Fig. 104) should not be interpreted as a malfunction, but rather as the evidence of the high grid impedance with such an important step-down ratio on the employed auto-transformer.

the intent of these results, which show however that once the appropriate reference values for the V^{Σ}_{Σ} can be computed by a suitable strategy-level block, such a closed-loop control scheme efficiently guarantees that the pursued objectives are actually reached.

Finally, it is worth reminding here that the relatively slow current dynamics shown on Fig. 104 are intrinsically limited by the decoupling of the sequences related to the DDSRF-based current control. Indeed, some filtering is unavoidably present in such a control implementation, what implies that the achievable current dynamics cannot be as fast as in a conventional *dq*-based current control. On the other hand, it must be noted that these limited dynamics are in turn very favorable to the "smooth" control of the capacitor voltage dynamics, which are here very well damped.

b) Operation with a conventional dq-based current control

In order to provide means of comparison to support these last comments, Fig. 105 shows another sequence based on a conventional *dq*-based line current control only:

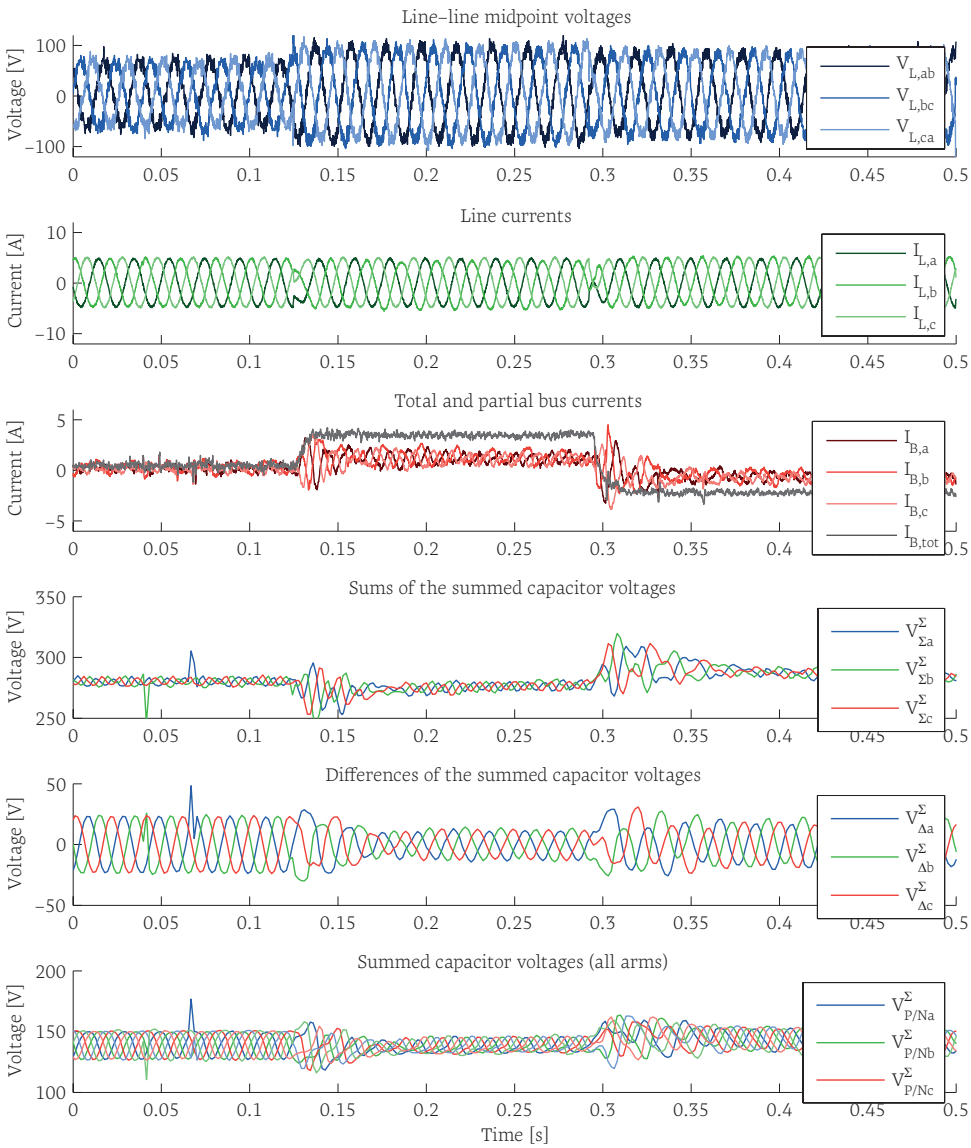


Fig. 105. Performance of conventional PI-based current control under balanced grid conditions.

In terms of control implementation, the only difference between Fig. 105 and Fig. 104 is therefore that of the line current control implementation. The presented sequence shows different regimes, defined as follows:

- Before $t = 125\,ms$, the transferred power is purely reactive, with $I_q = 5A$.
- Between $t = 125\,ms$ and $t = 292\,ms$, positive active power is transferred with $I_d = 5A$.
- After $t = 292\,ms$, negative active power is transferred with $I_d = -5A$.

Compared to Fig. 104, this sequence shows significantly faster current control dynamics, owing to the employed single rotating reference frame. On the other hand, the summed capacitor voltages naturally bear more important transient regimes, especially during the active power reversal. Nevertheless, here again, the fast closed loop control of these quantities allows to maintain the total peak-to-peak ripple within a narrow voltage band, which results in minimized capacitive energy requirements.

Interestingly, the three regimes of operation presented in Fig. 105 also well illustrate the known fact that the capacitor voltage ripple strongly depends on the current angle. Indeed the purely active power and purely reactive cases clearly feature different ripple amplitudes, confirming the results shown in [140]. More surprisingly however, the capacitor voltage ripples also differ as a function of the direction of the active power flow. This behavior is a non-ideal result, which is certainly due to the corresponding resistive voltage drops that differ between the two functional conversion stages and hence lead to different "intermediate" voltages as a function of the power flow direction.[18]

c) Voltage reference steps on the sum of the summed capacitor voltages

Finally, the effectiveness of the complete closed-loop voltage control is illustrated, non only with regard to perturbation rejection but also with regard to reference tracking, To that end, Fig. 106 and Fig. 107 show two sequences related to steps applied to the common-mode and differential mode of the summed capacitor voltages, respectively. Besides, being given that a satisfying operation under unbalanced grid conditions is sufficient to prove the applicability of the presented control scheme to balanced grid conditions as well, these transients are executed under asymmetrical grid conditions.[19] In Fig. 106, two reference steps are applied:

- At $t = 117\,ms$, the reference value $V^{\Sigma^*}_{\Sigma,\emptyset}$ is changed from $280\,V$ to $330\,V$ and then brought back at $t = 283\,ms$ to $300\,V$.
- Meanwhile, the line currents references are set to $I_{d+} = 2\,A$ and $I_{q+} = 4\,A$, corresponding to the injection of symmetrical currents[20] that are desired to be enforced despite the loss of the entire phase b due to a phase-to-neutral short circuit fault, i.e. $V_{L,b} = \emptyset$.

The presented sequence shows the satisfying operation of the considered converter structure under asymmetric grid conditions. Besides, the required voltage steps are appropriately followed, as expected, with fast dynamics and limited couplings with the differential-mode of the summed capacitor voltages. To the best of the author's knowledge, this is the first appearance of such results under asymmetric grid conditions.

18. Besides, the limited efficiency at this power level is made clearly visible by the total bus current, which shows different absolute values as a function of the power flow direction.
19. In order words, the most complex case is chosen so as to illustrate the comprehensiveness of the proposed control scheme.
20. Alternatively, active power oscillation elimination or reactive power elimination strategies could be used as well, leading to comparatively reduced ripples on the summed capacitor voltages. More detailed informations about these concerns can be found in [140].

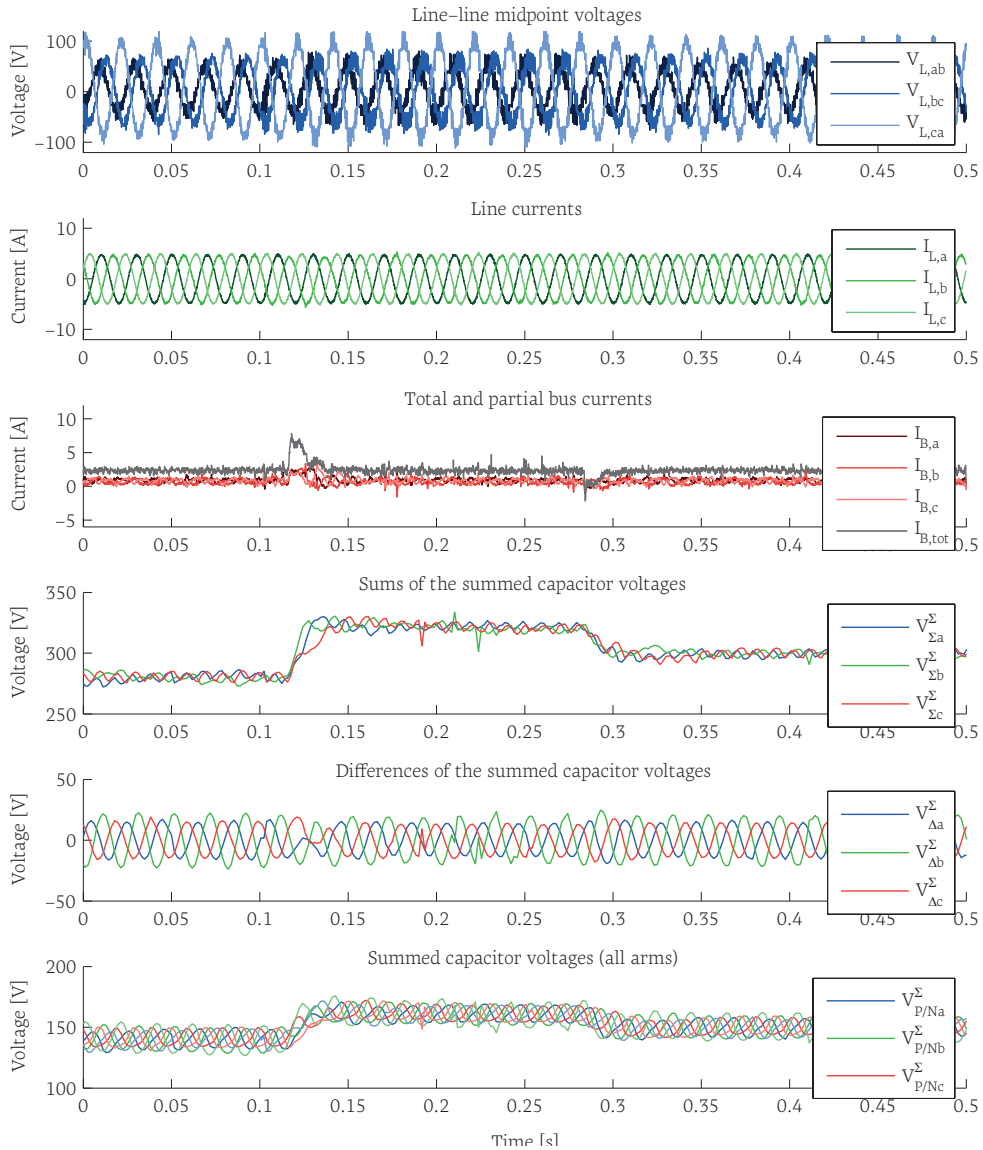


Fig. 106. Tracking performance of the control scheme of Fig. 63 under unbalanced grid conditions.

Apart from the tracking-related performance, the presented results also show that the total bus current is enforced to be a plain DC quantity despite the pulsation of the total line-side power (due to the grid asymmetry). This desirable behavior is also responsible for the 100 Hz ripple that is visible on the $V^{\Sigma}{}_{\Sigma}$ voltages, corresponding to the buffering of the total instantaneous power difference between the bus and line sides. Moreover, owing to the fast closed loops on the α and β axes, the corresponding voltage ripple is equally shared among the phase-legs, as desired. Finally, owing to the implemented control mechanisms, the impact of the grid asymmetry is confined to the differential-mode voltages $V^{\Sigma}{}_{\Delta}$, among which the faulty phase-leg can be easily identified by its larger voltage ripple.

Overall, although more optimal power management strategies may exist, these results nevertheless clearly demonstrate that based on the proposed control scheme, the operation of the MMC can be guaranteed to be satisfying in a wide range of conditions, what is the purpose of the corresponding control implementation.

d) Voltage reference steps on the difference of the summed capacitor voltages

A similar test sequence can also be executed in order to validate the performance of the differential-mode voltage control / vertical balancing. To that end, several transients are imposed in Fig. 107 :

– Between $66\,ms < t < 233\,ms$, a vertical imbalance of $+25\,V$ is required on $V^{\Sigma}_{\Delta,a}$.
– Between $183\,ms < t < 350\,ms$, a vertical imbalance of $-25\,V$ is required on $V^{\Sigma}_{\Delta,b}$.

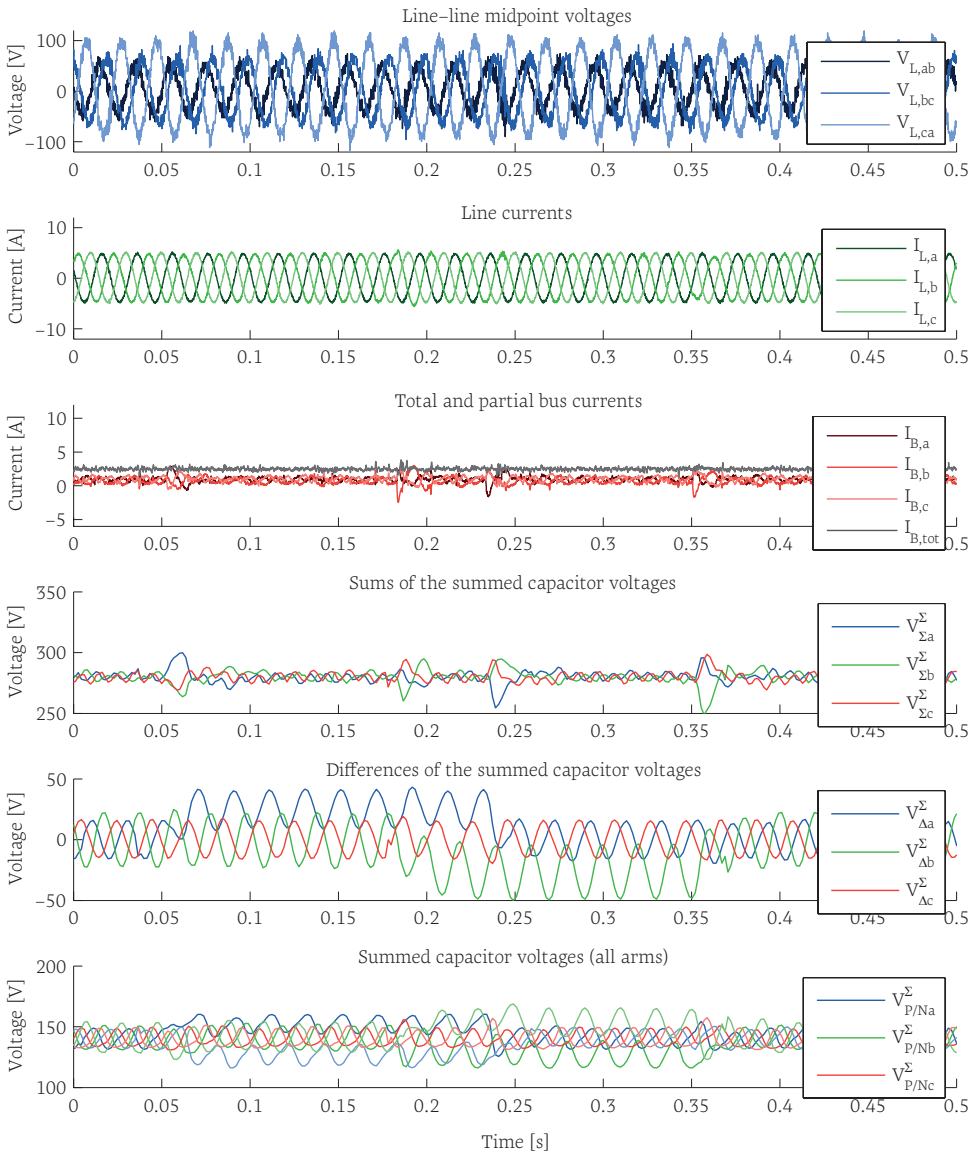


Fig. 107. Tracking performance of the control scheme of Fig. 63 under asymmetrical grid conditions.

These results depict satisfying performances as well in the sense that fast dynamics can be achieved with limited couplings to the common-mode voltage control. Furthermore, owing to the use of eq. (50), page 82 (Münch's trick), the vertical balancing of the phase-legs can be achieved without impacting the total bus current at all. This particular behavior is well illustrated here by fact that the bus and line side currents remain completely unaffected during the executed transients.

4.4 SYNTHESIS

4.4.1 EXPERIENCES LEARNT FROM THE LABORATORY

At the laboratory scale and as long as low voltage is concerned, several major hardware design challenges can be avoided. With respect to the power stage, a satisfying design can therefore be relatively easily obtained using thick copper PCB-based modules, which offer low parasitic inductance and resistance and a simple mechanical design. Besides, thanks to the MMC structure, the inductive nature of the overall construction, wiring and EMC are not causing significant issues since the arm currents are smooth and not chopped.

On the control side, for the considered prototype and number of modules, it is a matter of fact that the use of a centralized control implementation would have been possible. On the other hand, the efforts devoted to reflect realistic needs lead to the development of a dedicated control platform, what also gave rise to the opportunity to draw interesting conclusions out of some issues that were incompletely considered:

- The most severe design flaw in the developed control platform is certainly related to the way the modulation is achieved across the multiple FPGA-based *ARM* units (see §4.2.1.1). Indeed, the intrinsically *distinct clock domains* are making the synchronization among the different arms difficult, which leads to some imperfections in the generated modulation patterns. In practice, these issues are causing sporadic glitches that are negatively impacting the control of the partial bus currents.
- Besides, although the sequential retrieval of the capacitor voltages and the non-synchronous sampling of the latter is well suited to the implemented sorting approach and reduces the data bandwidth requirements, this also induces long and non-constant measurement delays. In the end, this is a limiting factor with respect to the closed-loop control of the summed capacitor voltages.[21]
- The choice of the DSP's external memory interface as the main communication backbone between the various devices revealed to be falsely influenced by the apparent simplicity of this approach as it finally corresponds to the main bottleneck in terms of data bandwidth. More generally, such a choice also strongly restrains the level of distribution of the control platform (the boards are practically forced to be inside the same enclosure) and can thus not be recommended for future work.

Overall, the main design flaws are therefore mainly related to the communication between the various control subsystems and are rather linked to industrial computing issues rather than conventional power electronic challenges.

4.4.2 CONCLUSIONS

Overall, the experimental results shown in this chapter illustrate a good agreement with those of Chapter 3 and confirm that, even by staying close to existing techniques (that is without an energy management layer), the association of fast closed-loop voltage control and of wise filtering allows to reach excellent performances with simple cascaded control techniques. Besides, the employed design approach results in very generic control schemes that are suited for a broad range of operating conditions. The latter characteristic is here highlighted by the fact that the presented experimental

21. Besides, the incomplete shielding of the corresponding signals across the power section is also the probable cause of data integrity errors.

results are apparently the first that are related to the operation of MMCs in asymmetrical grid conditions.

Furthermore, one of the essential objectives of the experimentation has been reached, which is to provide validation for the underlying model. Indeed, the mechanisms that directly depend on the validity of the model demonstrate a satisfying operation. This concerns for instance the decoupling of the bus and line currents, the separation between the vertical and horizontal balancing or the separation of these two mechanisms from the total energy control using Münch's trick.

On an entirely different perspective, the efforts placed in the hardware implementation have also recalled that all the conducted developments related to the control design are relying on a strong assumption, which is the existence of a cell-level balancing mechanism. Indeed, the arm-equivalent model is –by way of principle– entirely disregarding the cell-level balancing and completely hides the complexity related to the multilevel nature of the MMCs. As a matter of fact, this is why this approach is convenient for the control design (see Chapters 2-3), but is also why the high-level control is only one part of the challenges related to the practical implementation of MMCs.

Concretely, the implementation of these mechanisms has only been overviewed here. However, with respect to Marquardt-type (sort-and-select) balancing mechanisms, the considerations developed in this chapter have lead to recommend the implementation of full-sorting techniques but updated "slowly," as well as the use of algorithms that guarantee that only one submodule is switched at once. Furthermore, the cell-level balancing brings also back the question of the comparison between the Akagi- and Marquardt-type balancing and modulation approaches, which are bound to different modeling choices, but for which formal means of comparison are still missing.

More generally, these remarks and the various challenges related to industrial computing (including performance-related issues) reveal that the implementation of the low-level control functions is rather complex and involves highly specific mechanisms. This is why, for systems involving more than a few tens of submodules, the implementation of an entirely dedicated and tailored hardware control infrastructure seems generally indispensable.

In the end, this chapter and the previous one have illustrated that the MMC is an extremely flexible technology and that various types of converters can be implemented with few changes in the corresponding control techniques. However, this requires that the elements constituting the control software and hardware offer a similar level of modularity as that intrinsically provided by the power elements (the submodules). This postulates a strict layerization of the control structure, regardless of the control design choices in the broad sense of the term.

4.4.3 FUTURE WORK

Owing to the experiences made during the laboratory-scale hardware implementation, provided that *appropriate clock dissemination mechanisms* are established and *higher communication bandwidths* are available, nothing prevents from increasing even further the level of distribution of the control hardware. To that end, the use of carrier-based (Akagi-type) modulation and balancing techniques is probably more attractive than that of Marquard-type, as it enables to distribute the corresponding

tasks directly into the submodules. In practice, with such a level of distribution, the local phase-leg controllers can even be avoided, thereby avoiding a critical element in terms of I/O capability, processing performance and reliability. In turn, the introduction of intelligence in the submodules as well as the implementation of strict synchronization techniques constitute the two main things that would probably be worth changing if such a prototype had to be re-developed today.

More generally and from an almost philosophical point of view, if the invention of MMC has brought a real breakthrough, it may be primarily in relation to the know-how related to the operation of series-connected cells, which is completing the existing know-how related to their parallel connection (inherited from interleaved converters). Indeed, these elements constitute together the key to the complete modularization of power electronic systems using standardized building blocks connected in series or in parallel.

In this context, it could be imagined to go even further than above by completely distributing the control among the submodules, such that the central controller is made entirely dispensable. This would corresponds to operate the control infrastructure as a multi-agent system, in which only the submodules possess the required intelligence. Such an approach would certainly be beneficial in terms of reliability since everything that can be integrated in the submodules can be easily made redundant. Moreover, such an approach would allow the control infrastructure to offer the exact same degree of flexibility as the power parts, thereby enabling a total modularity and scalability by building converters through the simple association of modules.

5 TOWARDS SPLIT ENERGY STORAGE EMBEDDING

Abstract – This chapter aims to show that in the context of very demanding applications, the hybridization of several energy storage technologies and their integration in a distributed manner inside MMCs can be considered as an attractive approach to supply a broad range of ancillary services at the utility scale. However, such perspectives are also rising several system engineering aspects that remain incompletely explored, as well as control design and energy management issues. Hence, without solving all these numerous challenges, this chapter intends to illustrate how a functional a macroscopic approach –especially EMR– can be efficiently used in order to address these numerous aspects in a systematic manner.

5.1 STATE OF THE ART

5.1.1 GENERAL PRINCIPLES OF SPLIT STORAGE

As discussed in the first chapter, owing to the numerous challenges expected to take place in medium-voltage and railway networks, utility-scale energy storage is likely to play a major role in the integration of non-dispatchable energy resources in these networks, whose evolutivity is inherently limited. Besides, increasingly harsh load conditions also call for a further development of ancillary services, particularly with respect to power quality concerns, which also require some energy storage capability.

However, irrespectively of the utilized technology, the implementation of large monolithic electrical energy storage (EES) systems remains challenging. Typically, among other issues, the stacking of battery packs up to several kilovolts poses balancing concerns. In practice, this is illustrated by the fact that only few utility-scale electric energy storage systems have been demonstrated beyond the pilot stage yet.

In this context, modular multilevel systems could be very attractive in order to facilitate the implementation of highly scalable EES systems for utility-scale applications.[1] Practically, instead of using a common DC bus to which a unique and large storage unit is connected, the storage elements are split and distributed inside the converter itself. By doing so, the reduced submodule voltages as well as the inherent redundancies and balancing mechanisms of the converter can be advantageously used to help managing the storage units and allow for a transformerless integration at the medium voltage and high voltage levels. Reciprocally, the integration of energy storage largely extends the set of services that can be provided by the converter alone, with variable performances depending on the utilized storage technology.

1. Not to mention all the vehicular applications of energy storage, which can also significantly benefit from its integration into the power conversion system. The concepts presented by [85] or [89] are interesting examples of such a combined implementation.

The general principle of split storage integration in modular multilevel converters is depicted in Fig. 108, here exemplified with the double-star MMC topology (although other topologies are applicable as well). The benefits of this approach are therefore:

- On the one hand, the power conversion system offers several benefits to the operation of the energy storage itself:
  - » Allow the division of the whole energy storage system into smaller blocks down to standardized packs or modules.
  - » Take advantage of its own redundancies in order to improve the reliability of the energy storage as well.
  - » Put its balancing mechanisms at the service of the State-of-Charge (SoC) equalization, which must be implemented separately otherwise.
  - » Merge part of its monitoring functions (such as voltage and current measurements) with the energy management system.
- On the other hand, and reciprocally, the integration of energy storage inside the power conversion system comes with several benefits for the latter, such as:
  - » Augment the set of ancillary services that the converter can offer.
  - » Provide alternative means to ensure the cell- and arm-level balancing. In particular, since the short-term power balance do not need to be of zero average anymore, slower balancing mechanisms can be used.

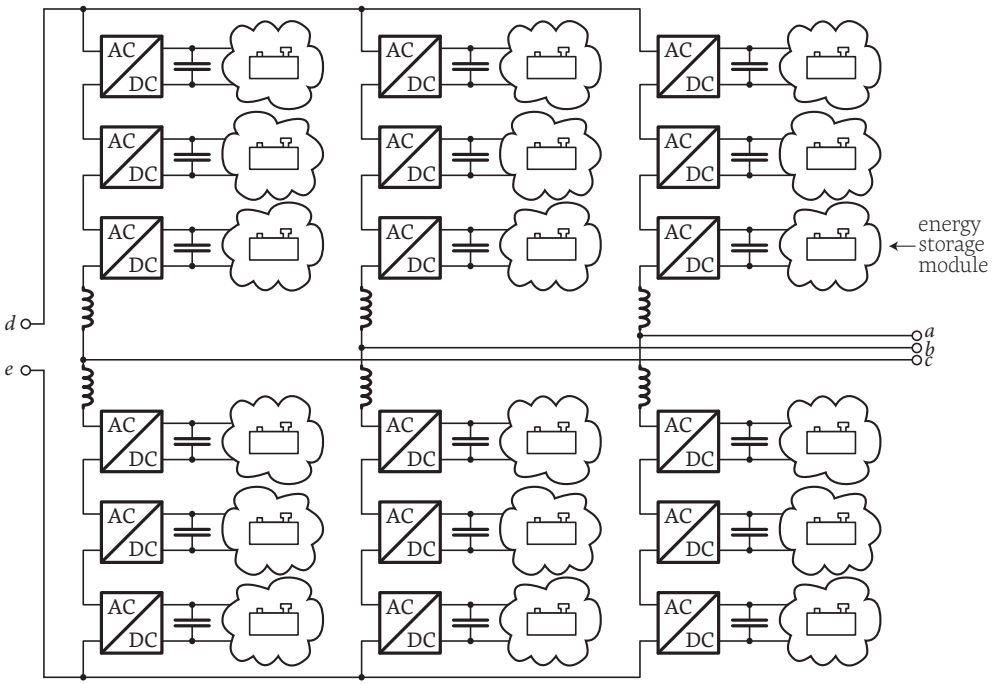


Fig. 108. General principle of split storage integration in modular multilevel converters. Alternatively, all the topologies of Fig. 8 and following are suitable as well.

In principle, a split storage system can be based on any EES technology. Typically, electrochemical technologies such as batteries or (super)capacitors are evident candidates. However, some choices are unavoidably more appropriate than others, what implies that the feasibility and attractiveness of the combined system is highly dependent on the final application. This is why a precise case scenario will be presented in §5.2.1 as a support to the present developments.

One of the first mentions of the use of energy storage in multilevel converters dates back to Tolbert et. al. in 1999 [188], suggesting the use of batteries as the separate DC sources of CHB converters in large electric drives. However, the detailed study of such systems was only initiated in the late 2000s by Maharjan and Akagi, who were first to report about the practical integration of energy storage, using supercapacitors in [189] and NiMH batteries in [190]. The authors were focusing on medium-voltage grid-tied applications with respect to renewables integration, motivating their approach by the necessity to avoid the low-frequency transformer. More recently, the same authors commissioned a prototype of 500 kW that demonstrates the effectiveness of the proposed control techniques [200].

The use of double star-type topologies was first presented by Vasiladiotis and Rufer in [87] in the context of a medium-voltage ultra-fast charging station for electric vehicles, in which the energy storage is used to provide some load leveling capability to the stations. However, in this case as in the reported works of Hillers et. al. [191] or Schröder et. al. [192], the global medium-voltage DC bus remains essentially unused. In other words, the choice of the double-star topology over the single-star or -delta ones remains unclearly motivated. A possible answer was recently brought by Trintis et. al. [194], who positioned this second family of topologies for the enhancement of HVDC converter stations, aiming for renewables integration as well.

Practically, the implementation of split energy storage into MMCs poses various types of challenges, outlined in the following sections:

5.1.2 DESIGN OF THE INTERFACES FOR THE SUBMODULES

In principle, any kind of electrical source could be connected to a MMC submodule. However, various practical considerations are limiting these possibilities and are calling for several design choices and trade-offs depending on the utilized energy storage technology. In particular, the insertion of an additional interface between the energy storage devices and the submodules (as in Fig. 109) can be suggested by various concerns presented hereafter.

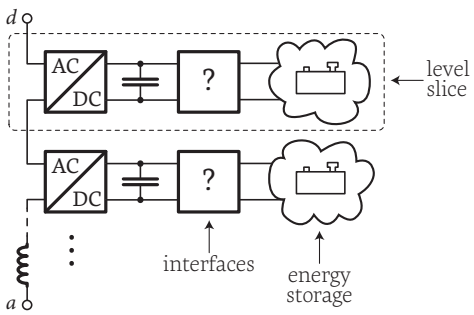


Fig. 109. General principle of EES integration into Modular Multilevel Converters.

a) Relation between submodule voltage and state-of-charge

The proper operation of MMCs requires that the summed capacitor voltages remain larger than the desired arm-level EMFs at all times.[2] In particular, this must be guaranteed regardless of the state of charge (SoC) of the energy storage elements.

2. This is an obvious consequence of the structure of the submodules (half-bridge, full-bridge) and particularly the presence of the reverse diodes, which start conducting as soon as this condition is not satisfied anymore.

While this can be easily guaranteed using the direct connection of batteries to the submodules, this is impossible using the direct connection of capacitive elements, unless only part of their capacity is effectively exploited. Indeed, supercapacitors possess an essentially quadratic relation between their voltage and their state of charge (see eq. (60)) while batteries feature an essentially flat voltage between typically 20% and 80% of their SoC.

$$SoC(V) \cong W = \tfrac{1}{2}CV^2 \tag{60}$$

Consequently, these simple observations are the first motivation for the use of additional interfaces between the submodules and the energy storage elements in order to allow the voltage of the energy storage element to fluctuate independently from the capacitor voltage, and thereby maximise the achievable depth of discharge (DoD) of the utilized energy storage.

b) Presence of low-frequency current components

In case the energy storage devices are directly tied to the submodule capacitors, they must also bear part of the rectified current that flows through the submodule capacitors. Hence, these two elements are unavoidably sharing some current harmonics (typ. first-, second- and third-order line frequency harmonics) with variable amplitudes depending on their internal impedances. These current components are obviously an unavoidable part of the $I^{\Sigma}_{p/n}$, as they are the ones which, once integrated, result in the capacitor voltage ripple. Besides, they are necessarily of significant importance (compared to the rms value of the line currents) as they directly relate to the singe-phase nature of each MMC phase-leg.

As a matter of fact, the presence of these alternating components is raising numerous remarks in the literature, especially when batteries are used. Indeed, numerous authors[3] are justifying the use of power electronic interfaces (as in Fig. 109) by the fact that these current components would induce an unacceptable reduction of the battery lifetime, unless they are filtered out. More specifically, the invoked mechanisms are related to *i)* the possible influence of these currents on the internal chemical reactions and *ii)* the increase of the batteries temperature due to the additional Joule losses ($R{\cdot}I^2$) related to these additional harmonic terms.

This analysis was the motivation for Trintis et. al. [194]-[195] and Vasiladiotis et. al. [87], [198] to add a chopper cell structure between the submodules and the batteries in order to *actively filter out these low-frequency components*. Alternatively, the use of isolated DC / DC converters has been suggested by Hillers et. al. [191].

Although still a subject of controversy, it seems that electrochemists nowadays tend to conclude that temperature rise is the main and only true consequence of these large alternating currents, at least with respect to the newest technologies such as lithium-ion. For instance, in [184], it is concluded that above approximately 10 Hz, the presence of such currents has no other effect on lifetime than temperature rise, as these phenomena are too fast for ion exchanges to actually take place. Furthermore, authors of [185] concluded that the presence of a 120 Hz current ripple of twice the average current value increases the total heat generation by only about 15%. That said, as shown by [186]-[187], temperature rise has anyway a strong impact on lifetime when the batteries are operated over 45°C and is therefore no a phenomenon to be neglected.

3. In particular Trintis et.al. [194]-[195], Vasiladiotis [198]-[199], Hillers et.al. [191] and Barushka [193].

Overall, despite its major impact on the choice of interfaces, it is evidently difficult to decide on this issue, which still calls for further investigations. Indeed, these current components could even be tolerated, provided that the overall battery cooling system is designed accordingly. Besides, from an efficiency point of view, no evidence has been brought that the corresponding losses are more, respectively less, important than the ones caused by the introduction of a filtering interface.

c) Mechanical considerations

Finally, a number of mechanical issues are also called to tip the balance with respect to strategic implementation choices. Among other examples, disconnection and protection mechanisms must be considered as well. Besides, galvanic isolation concerns at the converter level are also a major issue.

Indeed, a multilevel system naturally implies to distribute the galvanic isolation requirements among the submodules, which requires that all elements, including the built-in storage devices, must be referenced to floating potentials. While this is not necessarily an issue with (super)capacitors or batteries, this may be challenging with flywheels or more exotic sources (PV, wind turbines, etc.). In particular, if galvanically isolated interfaces should be placed between the sub-modules and storage elements, the corresponding increment of complexity may start questioning the entire design approach.

In the end, this simple example highlights the need for *a more systemic view* of all the system engineering aspects related to the integration of energy into MMCs, which are mixing numerous types of concerns and remain incompletely explored.

5.1.2.1 SELECTION OF THE INTERFACE TYPE

Independently of the above-mentioned system engineering considerations, provided that the use of some kind of interface is required, several implementation techniques may be considered. In order to systematize the study of the possible options, a possible classification of these variants is shown in Table 9 :

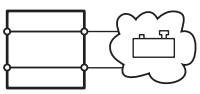
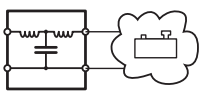
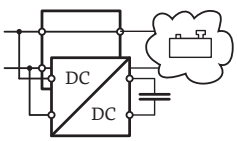
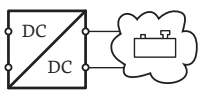
Direct connection	**Passive series filtering**	**Active shunt filtering**	**Active series filtering**
			
• Fixed output voltage	• Fixed output voltage	• Fixed output voltage	• Controllable step-up/ step-down ratio
• N.A.	• N.A.	• N.A.	• Controllable power flow
• Precharge/coldstart circuit required	• Precharge/coldstart circuit required	• Precharge/coldstart circuit required	• No additional circuit required
• No filtering	• Passive filtering	• Active filtering	• Active filtering
• Straightforward	• Difficult trade-off between size, complexity and efficiency • May instroduce additional stability concerns • High reliability and robustness • Most likely bulky and heavy	• Possibility high efficiency • Simple autonomous implementation	• Limited efficiency • Increase by 50–100% of the number of switches • Attractive for energy management purposes

Table 9. Possible implementations of the energy storage interfaces.

Obviously, as it highlighted in Table 9, not all these interfaces are solving all of the three previously-mentioned types of issues. In particular, the review of the existing literature as well as several students projects conducted on this topic allow to form the following preliminary comments:

- The direct connection is mostly interesting for its simplicity, but must be at least adapted with some kind of cold start/precharge mechanisms. As mentioned earlier, this is the choice made by Akagi et. al.
- The passive filtering may be of low-pass or band-notch type and tuned to one or several of the targeted frequencies (typ. 50, 100, 150 Hz, etc.). In any case, complex trade-offs are most likely involved between filter order, efficiency, volume, etc. [204]. Besides, as additional resonances are introduced, stability concerns may also occur with respect to the voltage control loops of the summed capacitor voltages V^{Σ}_{abc}. Overall, it seems that this approach has never been studied in details.
- The active shunt interface is interesting for its good filtering performances and its attractive volume and efficiency [205], [206]. On the other hand, as for the two first variants, the power flow between the two interfaced elements cannot be controlled actively (both elements are "tied" together). A few elements are presented by Vasiladiotis in [199].
- The series active filtering is likely to be – generally speaking – the least attractive solution from an efficiency point of view, but is also the only one which offers the possibility to step-up/-down the voltage [204] and hence offers the possibility to act on these local energy flows in order to decouple the SoC/energy management from the capacitor voltages. This is the choice made by Vasiladiotis and Trintis along with batteries. It is also the only possible choice of interface type in case a galvanic isolation is required [207], [208].

5.1.2.2 ELIGIBLE CONVERTER TOPOLOGIES

In case an interface is required, whether serial type or shunt type, many choices of topologies are available to the designer. It will not be attempted to review here the state of the art of DC/DC converters. That said, regardless of the adopted classification, a certain selection process can be highlighted. An example is given in Fig. 110, which leads to the common choice of the buck topology for the active series interface:

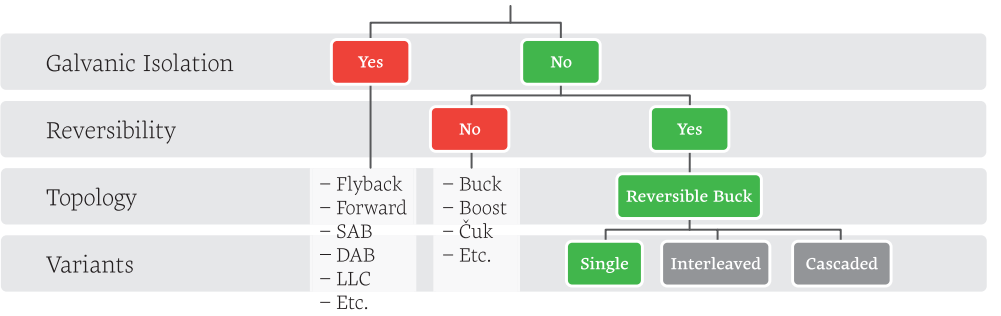


Fig. 110. Possible classification and selection of the most appropriate DC/DC topology.

Several reasons can be identified to explain this common choice:

- Isolated topologies are usually immediately rejected since the primary focus of the split integration is placed on storage technologies that are well adapted to floating voltages conditions (battery, capacitors, supercapacitors, etc.).

– Among these solutions, the necessity of the power reversibility is obvious.
– In the end, the reversible buck structure is an evident choice offering one of the simplest possible implementations.

More generally, among the possible choices of topology (and their variants), many criteria can be evaluated in order to make a choice of topology that is optimal in the sense of some objective (performance, reliability, complexity, operation, etc.). In particular, the buck topology is widely known for its limited performances with large step-down ratios, i.e. when the associated storage element is largely discharged or when its nominal voltage is significantly lower than the submodule voltage. There is therefore room for improvement when a large range of operating voltage shall be provided.

Overall, such an analysis goes naturally beyond the scope of this work. Nevertheless, these comments highlight here again that a more *systemic analysis* of the possible design choices would be of high interest with respect to split storage integration in general. A few additional interrogations will be mentioned in §5.4.3 as well.

5.1.3 CONTROL DESIGN AND IMPLEMENTATION

5.1.3.1 POWER FLOW CONTROL

For all the mentioned interface types but the active series one, the submodule voltages are essentially set and maintained by the storage elements. In other words, by controlling the states of charge, the cell voltages are controlled as well. This comment is at the origin of the balancing techniques first reported by Maharjan et. al. [189], [190], which are essentially substituting the submodule voltages with the battery-related states of charge in the employed converter modulation and balancing mechanisms.

Alternatively, in case the chosen interfaces are of the *active series type*, additional means are available to control the power flows between the cells and the storage elements. In particular, the management of the cell voltages can be decoupled from the SoC management. For instance, Trintis et. al. introduced in [194]-[195] independent current control loops for each of these additional converters. Alternatively, Vasiladiotis very recently presented in [198]-[199] the first complete control implementation that applies when active interfaces are used. Concretely, the author proposed to balance the SoCs using similar techniques as in Maharjan's work [189]-[190], on top of which the control of the submodule voltages is achieved with additional voltage + current cascaded control loops (see §5.3.1.2). Interestingly, the presented control techniques have been applied to single-star-, single-delta- and double-star-type topologies, including their operation under unbalanced grid conditions.

That said, these are two possibilities among possibly many others. More generally, it can be hence observed that this research field is still very young and remains largely unexplored (a quick look on the dates on which these contributions have been published confirms this ascertainment).

5.1.3.2 POWER AND ENERGY MANAGEMENT

Most generally, the term *energy management* refers to the mechanisms that allow to plan and define the appropriate energy exchanges between various energy storage systems, relatively to strategical concerns. Energy management thereby strives to some sort of optimization of the way energy is stored and manipulated, similarly

to industrial stock management. With respect to MMCs, this relates to the way the energy exchanges are controlled between all the storage elements (external sources, submodules capacitors, when applicable batteries, supercapacitors, etc.) as well as how the "stock" of energy is managed in each of these elements.

Chapter 3 presented elementary aspects of the *energy management* of MMCs when only capacitors are present in the submodules. In that context, the main issue is related to the optimization of the embedded energy, which in turn is rather a matter of *power management* than of energy management, strictly speaking. However, with integrated split storage, energy management is becoming a subject on its own, in the stock management sense of the word. This is especially true if additional degrees of freedom are added through active interfaces. Indeed, a MMC converter then becomes similar to a system that manages power flows between three controllable power ports (the DC bus, the AC network and storage elements), of which one is characterized by a finite amount of energy capacity.

Trintis et. al. [195] recently described the corresponding power flow paths and operating modes, but did not comment on the management of the stored energy. Maharjan discussed the need to manage different active power flows among the cells in [197] (with respect to aging issues), but did not pursue further either. The same comment also hold true in the case of the fast-charging station proposed by Vasiladiotis [199], that well describes the operating modes, but do not specifically address the energy management as such.

Overall, these aspects are located at the boundary between what is specific to MMCs and what is independent from the topology. That said, the development of relevant energy management strategies most certainly relies on a thorough understanding of the power flows and the power management concerns specific to MMCs first. As mentioned in the introduction, these perspectives combining energy management concerns and basic understanding concerns are indeed the main motivations for this work to chose EMR as a description and control design tool, for both of which it is known to be well suited.

5.1.4 PERSPECTIVES OF THE CHAPTER

In the light of the previous sections, it is clear that a certain know-how already exists on the integration of EES into MMCs, particularly with respect to batteries. On the other hand, it was also shown that this integration is setting implementation and control design challenges that remain incompletely explored and that differ among the utilized storage technologies.

Hence, the feasibility and attractiveness of the combined system is highly dependent on the final application. This is why the first issue tackled by this chapter is the question of the adequacy between prospective applications and the possibilities offered by existing storage technologies. In particular, one of the objectives is to highlight the limits of feasibility / attractiveness of such facilities for the provision of ancillary services to railway energy grids. As it will be shown, it quickly appears that the hybridization of several energy storage technologies is an approach that may be of significant interest for such demanding applications. With split storage integration, this perspective is all the more attractive that mixing storage technologies can be achieved in a relatively straightforward manner.

On the other hand, the hybridization of several technologies also induce an additional complexity for everything related to power and energy management, which is the price to pay to take advantage of this flexibility. This is why, in a second stage, this chapter introduce some of the bases of the model-based control design of MMCs *with split storage.* As it will be shown, the analysis and control design tools introduced earlier in Chapter 3 are becoming particularly important and allow a systematic approach that becomes absolutely essential with systems as complex as that of MMCs with integrated *hybrid* storage.

5.2 TECHNOLOGIES FOR SPLIT ENERGY STORAGE

As mentioned earlier, the growing interest for ancillary services can be expected to be particularly exacerbated in railway grids, which are therefore very interested by the possible applications of energy storage, especially if the latter can be incorporated in the future network interties.

This interest requires to assess what kind of ancillary services may be provided in addition to the transfer of active and reactive power. This section thereby attempts to analyze the particular case of the Swiss electric railways, starting from the evaluation of the needs in §5.2.1 and evaluating the possible technical answers in §5.2.2–5.2.3.

As an interesting side-effect, these developments also provide a clear context and a relatively general system engineering approach that can be easily applied to other applications of MMCs with split storage.

5.2.1 CASE STUDY: RAILWAY APPLICATIONS

In order to outline prospective applications of energy storage in railway grids, the Swiss case is analyzed hereafter using a few load profiles derived from measurements made between February 7th and 13th 2011 at various geographical levels of the SBB supply network:

- *National:* The whole Switzerland (sum of all substations).
- *Regional:* A fraction of the North-west part of Switzerland (sum of the substations of Yverdon, Neuchâtel, Bienne, Romont and Berne).
- *Local:* Measurements from the substation of Neuchâtel only.

It is worth noting here that being given the well established SBB-operated and conventional 50 Hz hydropower-based electricity generation infrastructure in Switzerland, as well as the ongoing development of large pumped hydro-storage facilities,[4] the flexibility of the production is well and easily guaranteed for the railway-related needs at the regional level and above. This is particularly true with respect to variations of several minutes and longer, which can be accounted for by the load scheduling mechanisms. Consequently, these requirements need to be assessed in the perspective not only to determine realistic applications as such, but especially those which constitute attractive alternatives to flexible hydropower-based generation and pumped hydro storage.

4. Such as the Nant-de-Drance project, involving 900 MW of variable-speed pump turbines, in which SBB is involved up to approximately one third. See http://www.nant-de-drance.ch/.

5.2.1.1 TYPICAL LOAD PROFILES

The load profile of the whole Switzerland during this period of time is illustrated in Fig. 111. Its analysis reveals various features:

- Daily variations of about ±50% are related to the traffic intensity, with two peaks around 8 a.m. and 6 p.m. due to the traffic of commuting passengers.
- Half-hour variations of several percents, related to the regular timetable which is used in Switzerland.[5]
- Variations of a few percents within minutes, due to the stochastic nature of the load (moving trains).

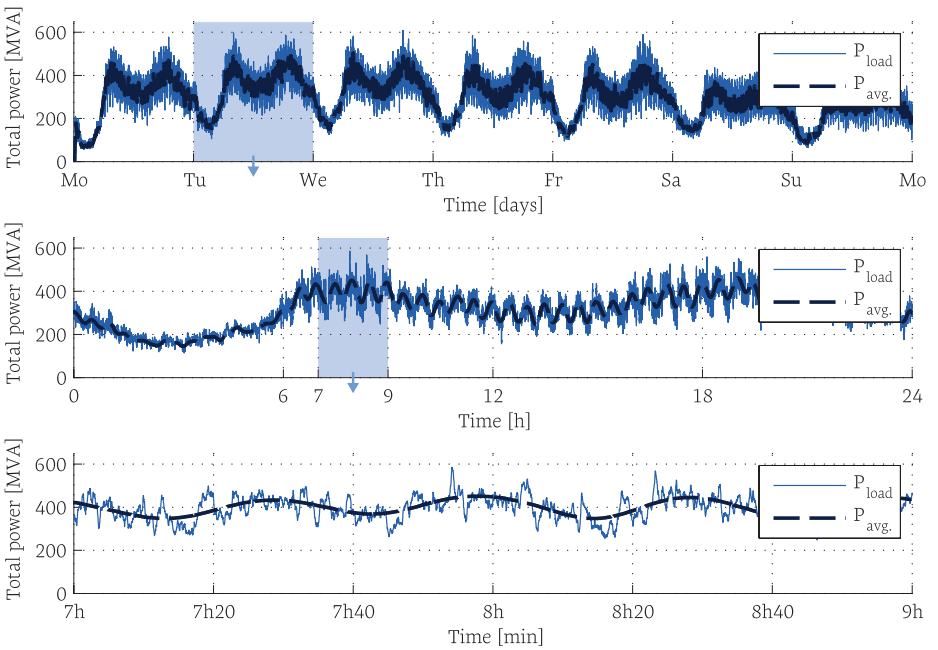


Fig. 111. National load profile for a typical week in winter (Switzerland).

The regional load profile of the North-West part of Switzerland is given in Fig. 112. When compared to the national profile, it can be observed that the time evolution is essentially similar, but with more stringent variations around the average values. Half-hour variations are still clearly noticeable as well.

5. In the largest train stations, all trains arrive and leave simultaneously at a clocked interval, usually around the full hour of the half hour, what explains the observable load profiles.

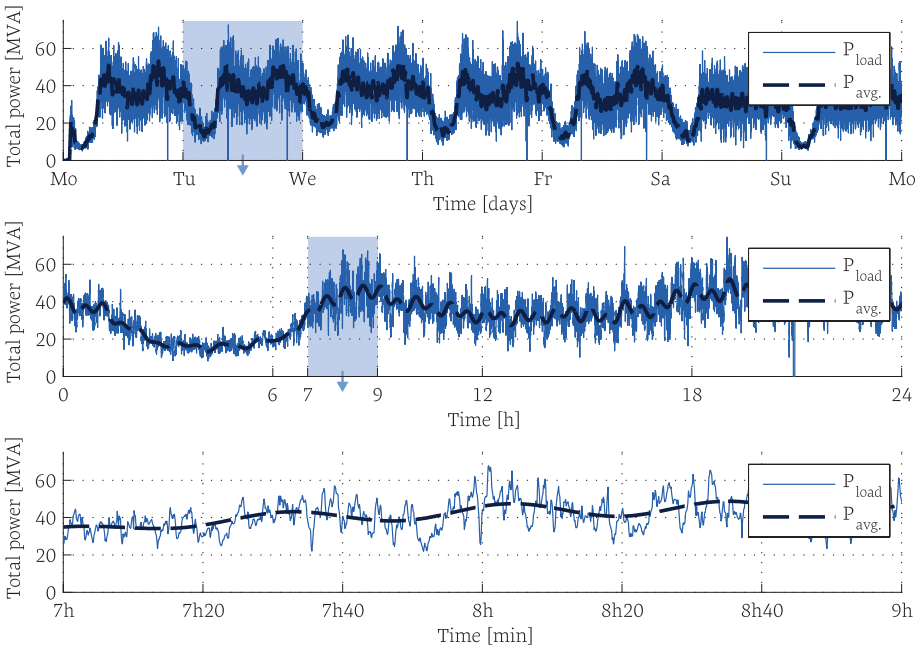


Fig. 112. Regional load profile for a typical week in winter (NW part of Switzerland).

Finally, the analysis of the load profile in Neuchâtel is given in Fig. 113. Daily variations and the impact of the commuting traffic are still noticeable, but are of less importance compared to shorter-term variations. Indeed, short-term variations of more than 100% can be observed within few minutes, typically around 7h50 in the following figure. These are due to the combined loads of the various trains (including regenerative braking) and are highly unpredictable. Obviously, at a given time, the total consumed power may even be negative.

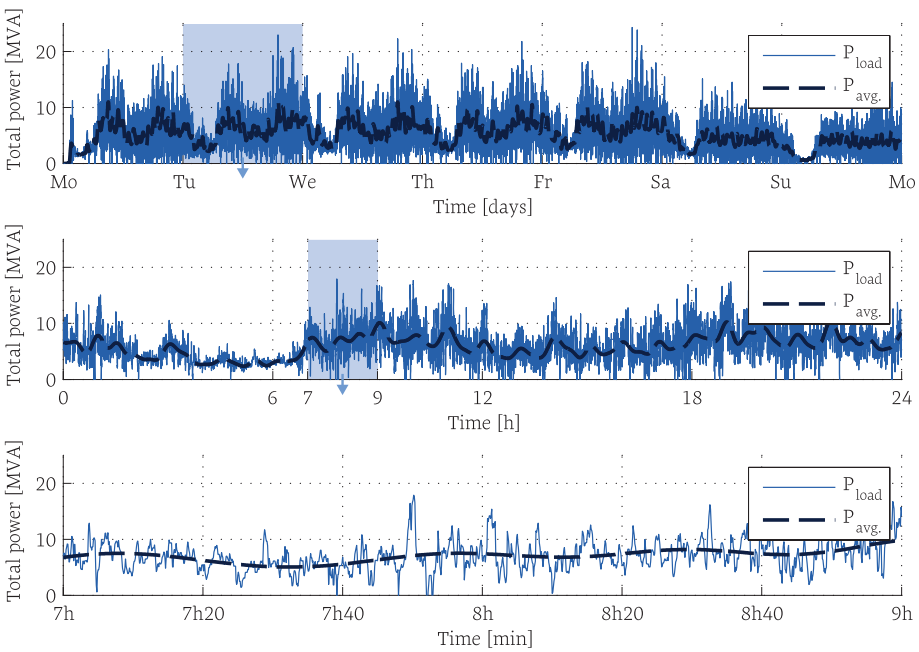


Fig. 113. Local load profile for a typical week in winter (Neuchâtel).

Overall, although these three load profiles correspond to very specific instants in time and geographical places, they well illustrate the particular needs that are likely to be shared by most railway energy grids:

- Important load variations can be noticed, especially at the local level but also (to a smaller extent) at the regional level. These profiles are indeed strongly impacted by only a few trains which represent heavy and varying loads. Consequently, the substations are generally sized generously, what results in a relatively low average network usage compared to the installed supply capacity.
- Due to the stochastic nature of the combination of the produced/consumed instantaneous powers (instants of acceleration or braking), the load profiles are rather unpredictable at the local, respectively regional levels. These load variations are less significant at the national level, where the stochastic nature of the load profile is naturally smoothed by the higher number of trains involved.
- Finally, the wider the considered area, the more significant the effect of the operational time schedule. In Switzerland, the half-hour regular basis is clearly noticeable at the regional and national levels. This behavior of the load profiles can be easily forecasted and accounted for on the production side. However, it cannot be either changed nor influenced since the operational schedule has anyway priority over any demand-side load management wishes.

5.2.1.2 POTENTIAL APPLICATIONS OF ENERGY STORAGE

Assuming that a prospective facility may be responsible for providing ancillary services related to such load profiles, this facility would need to manipulate significant amounts of energy, first approximations of which can be extracted from the analysis of these profiles in order to outline some potential applications.

To that end, Fig. 114 and Fig. 115 depict the energy exchanges of a hypothetical split EES integrated in a network intertie for two different scenarios, corresponding to *load-leveling* and *peak-shaving* applications, respectively. In both cases, the amounts of energy involved have been obtained by integrating the power differences between the actual load profile and the desired smoothed profile, respectively the shaving threshold. These figures are here shown for the case of Neuchâtel only, while the statistics of all the corresponding 18 cases are summarized in Table 10 and Table 11.

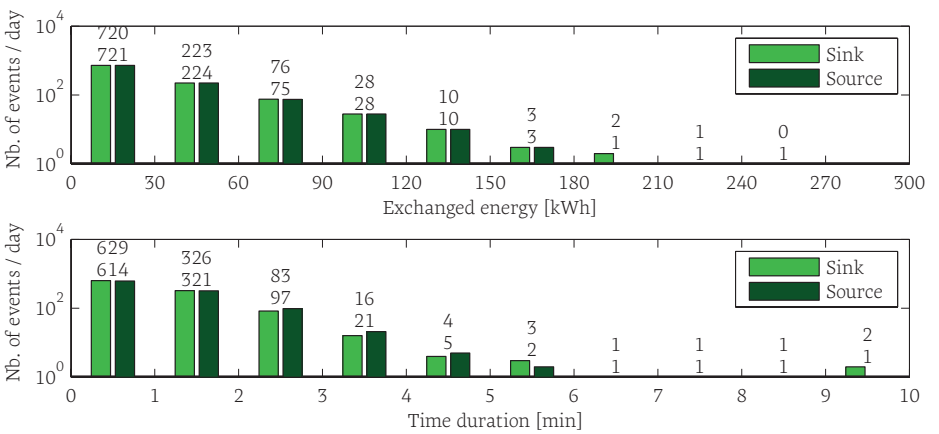


Fig. 114. Number of energy exchange events for a *30' load-leveling* scenario in Neuchâtel as a function of the amount of exchanged energy and as a function of time.

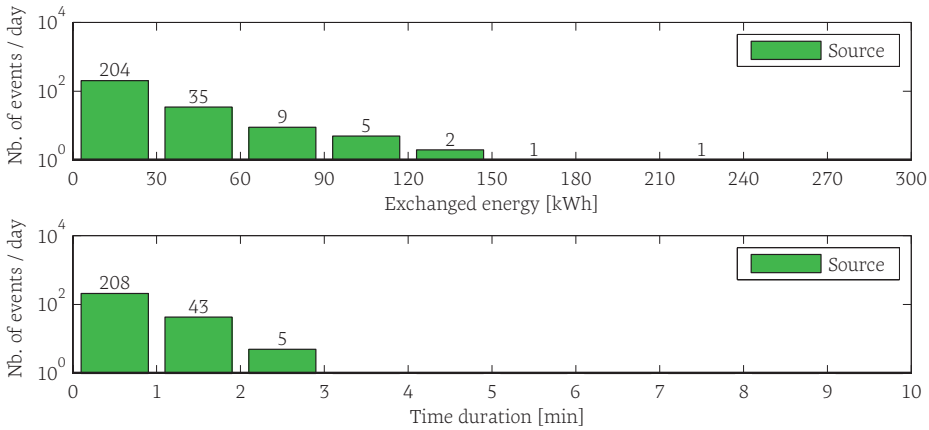


Fig. 115. Number of energy exchange events for a *peak shaving* scenario in Neuchâtel as a function of the amount of exchanged energy and as a function of time.

	Capacity	Time horizon	Max. energy	Median energy	Daily exchange	Daily full cycles
Local	*25 MVA*	*30 min*	*250 kWh*	*6,1 kWh*	*123 MWh*	*410 x 300 kWh*
Regional	*75 MVA*	*30 min*	*1,5 MWh*	*14 kWh*	*345 MWh*	*230 x 1,5 MWh*
Global	*1 GVA*	*20 min*	*4,8 MWh*	*20 kWh*	*1.8 GWh*	*280 x 6.5 MWh*

Table 10. Approximate energy requirements for *load-leveling* scenarios.

	Capacity	Threshold	Max. energy	Median energy	Daily exchange	Daily full cycles
Local	*25 MVA*	*10 MW*	*290 kWh*	*6,3 kWh*	*93 MWh*	*310 x 300 kWh*
Regional	*75 MVA*	*45 MW*	*1,2 MWh*	*16 kWh*	*255 MWh*	*170 x 1,5 MWh*
Global	*650 MVA*	*500 MW*	*6,4 MWh*	*61 kWh*	*208 MWh*	*32 x 6.5 MWh*

Table 11. Approximate energy requirements for *peak shaving* scenarios.

In the case of ***load-leveling***, Fig. 114 reveals that, in Neuchâtel, more than a thousand cycles of less than three minutes must be served every day. Being given the stochastic nature of these energy exchanges, the latter are also most likely the ones that involve the smallest amounts of energy. In turn, only a few daily events are involving more than a hundred of kWh in Neuchâtel, bust also remain most likely completely unpredictable. The summary shown in Table 10 confirms the important total amount of manipulated energy (daily exchange).

Moving to larger scales, the profiles are benefiting from natural averaging effects and fewer short events must served. However, the amounts of energy at stake are becoming extremely important (typically 20 kWh / MVA on the regional scale). In any case, these results are highly dependent on the time basis chosen for the load leveling, here 30 or 20 min. Obviously, longer time constants require even larger amounts of energy.

Considering the ***peak shaving*** approach, Table 11 applies. In such as case, involving similar amounts of energy as in the load leveling case, a reduced number of daily cycles is expected by this analysis. On the other hand, when considered on the local or regional scales, peak shaving mostly aims to avoid overloads on the T&D supply network, what may not necessarily be the most critical issue, especially for such short events (< 3 min).

In the end, the choice to focus here on the applications that constitute alternatives to hydropower-based generation and storage is favoring the “short” and “local” appli-

cations, as it is where the low system voltage and power quality issues are expected to be the most acute, especially in the remote / weak sections of the grid. Thus, the scenarios presented above are undeniably closer to applications such as *frequency regulation* than conventional *load leveling* and *peak shaving* applications.[6] This can be easily seen in the number and the length of the proposed cycles, which represent tens or even hundreds of cycles of a few minutes per day.

Of course, other applications could also be shown, particularly in the context of other railway networks, which may not have a mountain environment as favorable to the exploitation of water resources as in Switzerland. In such cases, it is clear that the compensation of the hourly, daily and seasonal variations of the load is one of the areas where attractive applications are likely to be found.

More generally, this rough analysis clearly illustrates the highly specific nature of traction-related requirements, which are several order of magnitude higher than in automotive applications, and what inevitably puts severe constraints to the realization of such plants and especially to the choice of the appropriate energy storage technology.

5.2.2 TECHNOLOGY OVERVIEW

Numerous studies have attempted to summarize the state of the art of EES technologies and identify the most promising ones. In particular, the US Department of Energy (DoE) has repeatedly appeared as a very active source on that matter [171]-[175]. Table 12 attempts to summarize the results of such studies, showing the characteristics of some of the most attractive EES technologies for split-storage systems:[7]

Name	*Energy density*	*Power density*	*Roundtrip efficiency*	*Bulk storage cost*	*Cycle life (>80% DOD)*	*Lifetime*	*Maturity (utility scale)*
	[Wh/kg]	*[W/kg]*	*[%]*	*[$/kWh]*	*[cycles]*	*[years]*	
Supercapacitors (EDLC)	*3 - 10*	*1k - 8k*	*> 95 %*	*15k - 80k*	*10k - 1M*	*30*	*?*
Mid- & high-speed Flywheels	*5 - 30*	*< 300*	*> 90 %*	*1000 - 2k*	*10k - 100k*	*15*	*Pilot*
Advanced Lead-Acid	*30 - 50*	*200*	*75 - 90 %*	*150 - 350*	*200 - 1500*	*5 - 15*	*Commercial*
Nickel-Metal Hydride (NiMH)	*40 - 100*	*250 - 1000*	*60 - 70 %*	*250 - 500*	*600 - 1500*	*?*	*Pilot*
Lithium-Ion (various types)	*60 - 200*	*1000-2.5k*	*80 - 90 %*	*350 - 2000*	*300 - 8k*	*< 10*	*Pilot*
Sodium-Sulfur (NaS)	*100 - 250*	*150*	*70 - 90 %*	*150 - 250*	*2500 - 5k*	*15*	*Commercial*
Pumped-hydro (PHS)	*NA*	*NA*	*70 - 85 %*	*10 - 15*	*> 10k*	*40 - 70*	*Mature*

Table 12. Performance comparison of eligible EES technologies for split-storage applications (PHS is provided as a comparison). Sources [172]-[173] and [175]-[176].

Obviously, as there is no technology which simultaneously combines high power density, high energy density and high cycle life, the choice of a technology is clearly a matter of trade-offs. In turn, the latter especially depend on the *time frame* in which the storage element is likely to be cycled. Short- and very short-term applications[8] are conventionally associated with high power density technologies while longer-term

6. It has been chosen here not to refer to them as frequency regulation scenarios as the latter is in turn not the heart of the issue, but rather the low system voltage and power quality related to harsh loading conditions.
7. This list is limited to the technologies that have already demonstrated their eligibility for the implementation of utility-scale systems. Besides, some Nickel-type battery technologies have been omitted due to a lack of comparable information.
8. Between few milliseconds and few minutes.

applications[9] are often associated with high energy density technologies. However, there is most generally no direct relation between cycle lifetime and the power or energy density performance of a given technology.

In order to better highlight the performance of the eligible EES technologies with respect to time, two additional metrics can be proposed :

– The *energy-to-power ratio* is the ratio between energy density and power density. It aims to highlight the inherent propensity of a given technology to be cycled within a given time frame. The idea is that, when comparing technologies for shorter, respectively longer cycling times, a technology possessing a higher power density, respectively a higher energy density is naturally preferable.
– The *typical lifetime-based cycle length* is calculated through the ratio between the estimated calendar lifetime and the cycle lifetime. It describes the cycle length that leads to reaching the maximum number of cycles within the calendar lifetime. It is a very approximate metric but which is related to a reasonable context of use for a given technology. Cycling more intensively than the produced metric results in the cycle lifetime to be reached earlier than usual, while longer cycle lengths lead to a reduced utilization of the cycling capability compared to existing usage.

Hence, the energy-to-power ratio is a relatively theoretical metric, while the typical lifetime-based cycle length is a more empirical value corresponding to conventional usage. Table 13 presents these values for the technologies of Table 12 :

Name	*Energy-to-power ratio*	*Typical lifetime-based cycle length*
Double-Layer Capacitors (EDLC)	*1.5 - 10 s*	*15 min - 2.5 h*
Mid- & High-speed Flywheels	*1 - 5 min*	*1 - 15 h*
Advanced Lead-Acid	*10 - 15 min*	*30 - 650 h*
Nickel-Metal Hydride (NiMH)	*3 - 30 min*	*?*
Lithium-ion (various)	*2 - 15 min*	*10 - 300 h*
Sodium-Sulfur (NaS)	*0.5 - 2 h*	*50 - 100 h*
Pumped-hydro (PHS)	*0.5 - 4 h*	*3.5 - 6 h*

Table 13. Time-related performance of the energy storage technologies listed in Table 12.

Studying Table 13, it can be observed that the typical *lifetime-based cycle lengths* are significantly longer that what the *energy-to-power ratios* may suggest. Indeed, most applications are setting their focus on energy supply rather than power, thus intentionally setting their dimensioning towards longer cycle durations. Besides, for most battery-type storage technologies, the cycle lifetime is an inverse exponential function of the depth of discharge. Therefore, it is generally advantageous to "oversize in energy" in order to reduce the average depth of discharge and significantly increase the lifetime expectancy.

Fig. 116 attempts to synthesize these informations showing the appropriateness of a given technology as a function of the time interval in which it is operated, i.e. the equivalent cycle time. It is of course a purely qualitative assessment of their adequacy, which is subject to numerous technical and cost considerations that are going beyond the scope of this work. Nevertheless, this figure clearly illustrates the *presence of a "gap"* between high power density technologies and high energy density technologies, in the range of several seconds to several minutes :

9. Ranging from tens of minutes to few hours, day, or even seasons.

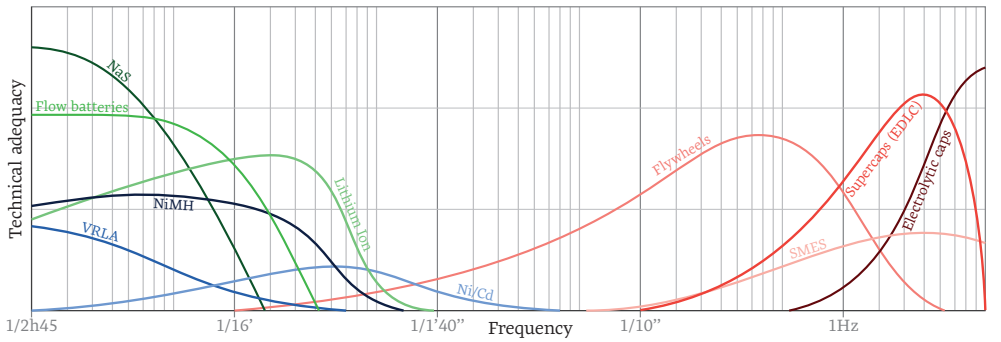


Fig. 116. **Qualitative** attractiveness of energy storage technologies as a function of the cycling time.

5.2.3 ELIGIBLE ENERGY STORAGE TECHNOLOGIES

Considering the EES technologies presented in Fig. 116, all of them are obviously not benefitting from the splitting of the whole storage system into smaller elements.[10] Practically, only few of them are truly well suited for split storage applications :

a) All types of batteries

Because of their low operating voltage (few tens to hundreds of volts), battery packs conventionally need to be stacked in order to reach usable voltages in utility-scale applications. Besides, parallel-connected stacks are also commonly implemented in order to meet energy-related dimensioning criteria. By doing so, up to several hundreds of battery packs are typically assembled to constitute a complete system. Hence, the splitting of these elements into the MMC submodules is a relatively natural solution that mirrors pretty well the conventional structure employed to build a large storage system anyway.

Among battery technologies, lead-acid remains a good technological choice for utility-scale applications, owing to its excellent maturity and low price. Alternatively, Lithium-ion batteries are receiving an increasing interest because of their comparatively high power density. In particular Lithium-Iron-Phosphate (LFP) [179]-[180] and the recent Lithium-Titanate (LTO) technology [181]-[182] are excellent candidates, although their performance – especially their cycle life expectancies – remain to be demonstrated in the field. Finally, the recent concept known under the commercial name UltraBattery™ is also promising attractive performances [183], although the latter require to be truly demonstrated as well.

More generally, an intense development activity can be observed concerning fast charge (i.e. high power) applications, partly thanks to the emergence of electric mobility. On the other hand, in applications such as the ones stated in §5.2.1, *cycle life* remains the heart of the problem as it can be reached within a few months only! Hence, in any case, a drastic over-sizing of the installed capacity can be expected to be necessary in order to reduce the average depth of discharge. This being said, if there is no other choice than to drastically oversize the installed capacity, new opportunities and applications can also emerge. In other words, different applications can be targeted as well. Further comments on that matter will be given in §5.2.4.

10. Typically those for which the presence of complex auxiliaries is likely to favor the implementation of few large elements over numerous small ones (flow batteries, compressed air-based, thermal energy storage, etc.).

Examples of existing systems using a high number of shallow cycles of high power are given by *i)* the 3MW/2.1MWh frequency regulation facility in Lyon Station (USA) implemented using UltraBattery™ or *ii)* the 32MW/8MWh frequency regulation facility in Laurel Mountain based on Lithium-Ion (shown in Fig. 117).

Fig. 117. 32 MW/8 MWh frequency regulation facility in Laurel Mountain (WV/USA) by AES Energy Storage and A123 Systems. The facility is co-operated with a 98 MW wind farm.

b) Capacitors and supercapacitors (EDLC)

Due to their very low intrinsic operating voltage (a few volts), super-capacitors are sharing the same concerns as batteries, but with an even higher number of elementary components: cells must be assembled in packs, that are stacked and paralleled in order to build up complete systems. They are thereby also very much benefitting from split-type implementations.

The attractiveness of this technology is mainly related to its maturity and excellent cycle life (see Table 12), what is of utmost importance in the considered applications. Since supercapacitors are best suited for power-oriented applications, the higher the application's *energy-to-power ratio*, the more likely they are to be an appropriate choice of technology (see Table 13 and Fig. 116).

When compared to conventional electrolytic capacitors, supercapacitors feature a better energy density [176]-[177], what can be a significant advantage in terms of volume and weight, but only provided that their lower operating voltage is not an issue. Indeed, for some applications, by considering not only the storage itself, but also the necessary interfaces, the resulting power/energy density may finally be similar to that of standard electrolytic capacitors. An example of such system is given by the power supply of one of the particle accelerators in CERN, Geneva, using about 18 MJ of conventional electrolytic capacitors operated in cycles of 2.4 seconds at a power level of 60 MW 7.5-[170]. An example using supercapacitors is presented in [178].

c) Flywheels, especially medium- and high-speed systems

With typical power ratings from a few tens to hundreds of kilowatts, fast flywheels also require to be assembled in order to form utility-scale energy storage systems. However, due to the presence of variable-speed drive converters along with each rotating mass, stacking is not trivial, which could then benefit from a split design approach.

In terms of performance, high-speed flywheels are an interesting technology as it is the only candidate that is somehow naturally "located" in the middle of the gap between high power density and high energy density technologies (see Fig. 116). They have been successfully implemented in a 20MW/4MWh pilot plant in Stephentown for

a frequency regulation application. This project uses 200 flywheels of 100kW/25kWh, grouped in 1MW units. The overall facility is illustrated in Fig. 118:

Fig. 118. 20 MW / 4 MWh frequency regulation facility in Stephentown (NY/USA) by Beacon Power.

Additionally, more exotic systems can be imagined, in which the MMC is used as an energy collection system. Indeed, MMCs could also be suggested to assemble strings of photovoltaic panels, wind turbines, etc. However, the attractiveness of the split integration technique most certainly depends on the feasibility of generating separate floating voltages with a high voltage separation from ground (see §5.1.2 *c.*).

Coming back to the present case study, the estimated requirements extracted from the load profiles correspond to the following approximations when applied to the converter parameters of Table 4, page 92:

- *Using capacitors:* Aiming to serve approximately 90% of the events suggested by the 30' load leveling scenario for the SBB substation in Neuchâtel, about 200 kWh (i.e. 720 MJ) must be embedded in the entire facility. This corresponds to approximately 2.6 kWh, what represents about 10 m^3 of conventional capacitors per submodule.[11] Hence, the total unpackaged volume of capacitors for the entire facility can be estimated to be about 700 m^3. This is about fourty times the volume of capacitors integrated in the power supply of the PS accelerator at CERN 7.5-[170].
- *Using supercapacitors:* Substituting the capacitors with supercapacitors allows to multiply the volumetric energy density by almost a factor of ten. Therefore, the same scenario could be covered with a typical total volume of "only" 100 m^3 of supercapacitors, but still assumes that the energy capacity can be fully exploited and that there are no integration concerns of any kind (typically, see §5.1.2).
- *Using lithium-titanate batteries:* Over-sizing the facility by a factor of thirty, that is embedding 6 MWh of energy, corresponds to a raw total volume of about 60 m^3 of batteries (assuming a volumetric energy density of 100 Wh/l[12]) what s about 0.75 m^3 per submodule. According to Altairnano [181]-[182], this corresponds to a feasible scenario, since the promised cycle life can be as high as 3'000'000 cycles with at a 5% depth of discharge (i.e. 410 daily cycles of 5% DoD over 20 years).
- *Using high-speed flywheels:* Unfortunately, the flywheel case is uneasy to assess without the appropriate expertise. However, Stephenstown's pilot plant is giving a realistic image of a facility which is probably addressing similar power, energy and cycle life requirements as in the presented scenarios.

11. Assuming 1 J / cc. Packaging, interfacing, monitoring etc. are entirely disregarded.
12. Source: datasheet of Altairnano's 24 V 60 Ah module. (http://www.altairnano.com/wp-content/uploads/2011/10/60Ah-DataSheet.pdf)

5.2.4 SUMMARY

The two previous sections showed a very quick overview of potential applications related to the Swiss railway network and a rough evaluation of the eligible energy storage technologies adapted to grid-scale split-storage implementation.

In general, the question of the adequacy between the needs and their solutions is most certainly involving an indispensable notion of economic relevance, which goes far beyond the scope of this work. It will therefore not be drawn here any conclusions with respect to this issue. Nevertheless, retaining only the orders of magnitudes sketched above, it can be generally observed that such aspirations are flirting with the limits of feasibility. This being said, on the other hand, it is also clear that the presented scenarios are located within the range of possible, even with respect to a relatively short term horizon.

Hence, postulating that the necessary technical evolution is on its way, some applications are anyway likely to reach a true technical and economic attractiveness sooner than others. Table 12 summarizes some of the likely trends, combining the results of the above *case studies* with some elements of the current context of the railway energy supply (see §1.1.3):

	Short-term (t < 30 s)	**Mid-term (30 s < t < 30 min)**	**Long-term (t > 30 min)**
Local	• Could be interesting for power quality enhancement, peak shaving, etc. • Maybe worth investigating	• Could support weak sections and provide emergency backup supply. • Maybe worth investigating	• Could support weak sections, provide extended UPS and assist renewables integration. • Possibly an attractive case
Regional	• Typical P.Q. applications / frequency regulation scenario. • Need are feasibility are questionable	• High amounts of energy + cycles required. • Hardly feasible and profitability is questionable	• Typical load leveling / renewables integration scenario. • Hardly feasible and profitability is questionable
Global	• Typical frequency regulation scenario. • Unrealistic and useless	• Tremendous amounts of energy required. • Unrealistic and useless	• Already covered by pumped hydro facilities. • Unrealistic and useless

Table 14. Rough evaluation of the technical relevance of the considered scenarios.

As already mentioned, the *value* of such applications fundamentally depends on the available alternatives. In the case of Switzerland, hydropower-based generation and storage is probably unbeatable anyway. Therefore, if applications of energy storage exist, they must be sought where hydro is not to its advantage. This is the main reason why the proposal made in this work is focusing on the weak points of the network and on power quality-related services. Besides, simple feasibility considerations make it difficult to conceive facilities aiming to wider geographical or temporal scales, simply because of the orders of magnitude involved.

Overall, regardless of the technical and economical relevance of such applications, the above-presented developments have shown that the considered scenarios are posing in any case two major constraints:

– They are setting requirements that are located right in the middle between *very short-term* storage and *medium-term* storage.
– They are demonstrating extremely demanding needs. Typically, as illustrated by Table 10 and Table 11, the proposed applications represent between 1.6 and 3 millions cycles of several tens to hundreds of kWh over twenty years!

Regarding the eligible EES technologies for this kind of applications, it has also been confirmed that :

– The amount of energy at stake is the main factor limiting the use of capacitors or supercapacitors due to a relatively low energy density.
– The number of cycles is the major problem preventing the use of the vast majority of the existing battery technologies.
– The issues are related to the interfacing with the submodules for other technologies.

Consequently, for such scenarios, it is a matter of fact that no existing ESS technology is truly well suited to handle as much energy in as short time intervals and with as many cycles. The same kind of observation also applies to other fast and ultra-fast energy storage systems such as in [85]-[87].

In all these cases, the use of hybridization techniques combining multiple storage technologies could be very beneficial as it would allow to cycle each technology in its most appropriate time frame. Typically, this can be achieved with energy management mechanisms that exploit a fast and high cycling-capable technology to support fast phenomena, whereas a slower but more energy-attractive technology is employed to the pursue the operation during longer intervention cycles.

This kind of approach seems all the more natural for split-storage systems that the latter are structurally well suited to support the use of various technologies. Indeed, the separation of such power flows is *"only"* a control issue, since the corresponding means of action (the tuning variables) are already made available by the converter itself. On the other hand, as mentioned in §5.1, the use of different storage technologies is raising various implementation issues, not to mention the design of the corresponding control architecture and mechanisms.

Overall, these perspectives are thereby opening a relatively wide area of potential research, of which some preliminary control considerations are developed in the following sections.

5.3 PERSPECTIVES OF CONTROL IMPLEMENTATION

5.3.1 POWER FLOW CONTROL

It was shown in section 5.1 that the presence of controllable interfaces between the submodules and the energy storage elements can completely change the way the states of charge are managed. Indeed, the presence of an active serial interface provides an additional tuning variable, which makes it possible to directly influence the power flow into or out of the storage elements, irrespectively of the voltage on the submodules. In terms of controllability, two very distinct cases can thus be distinguished :

5.3.1.1 DIRECT CONNECTION

As shown in §5.1.2.1, the direct connection is an attractive technique to integrate storage elements whose voltage characteristic is essentially flat. This approach corresponds to Fig. 120, which reuses the arm-equivalent model presented in §2.2.3 and where *Eq. bat.* represents the combination of the storage elements and the capacitors. As illustrated, from a functional point of view, this arm-equivalent system is very

similar to the one studied in the previous chapters, except that the state variable corresponding to the summed capacitor voltages is substituted with an *external source*:

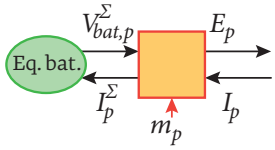


Fig. 119. Arm-equivalent EMR of an MMC arm in case of direct connection.

Interestingly, by doing so, the underlying model pushes these voltages out of the state-space control problem (they no longer need to be controlled) and transfers the definition of the corresponding power flows to energy management concerns. This modeling approach typically corresponds to what has been reported by Maharjan et. al. [189]-[190] using a control implementation that is essentially identical to the case without embedded energy storage:

– The *cell-level* balancing is achieved with a conventional Akagi-type modulation and balancing approach (see §1.3.5, page 15 *b.*), except that the capacitor voltages are substituted with the overall SoCs.

– The *arm-level* balancing is achieved using either the zero-sequence line voltage in case of star configuration or the circulating current in case of delta configuration.

Moreover, by extending these considerations to other topologies, the work of Maharjan et. al. could be easily generalized, to Marquardt-type modulation approaches and/or to double-star-type topologies (what has not been reported so far). The EMR of Fig. 120 shows that this is trivial since the control design approach presented in section 3.3 and 3.4 directly applies. This ascertainment is also illustrated by Fig. 121, which shows that the behavior of such a system can be assimilated to the known equivalent system possessing an additional power source on the fictive intermediate busses.

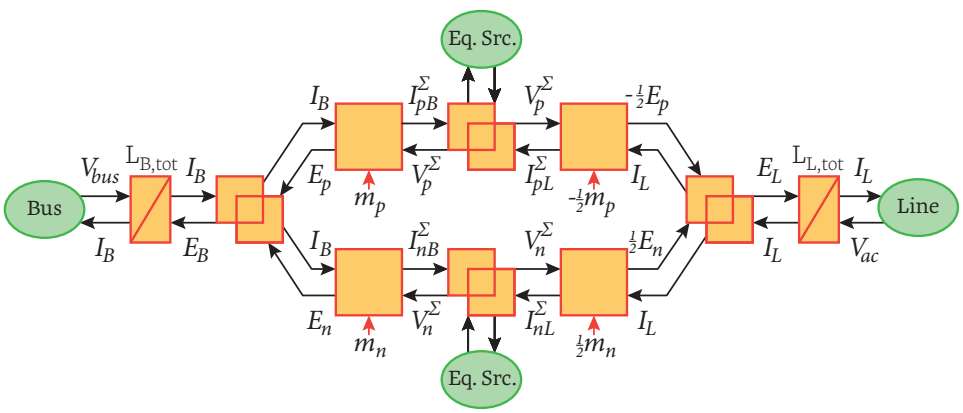


Fig. 120. EMR of a phase-leg in case an energy storage element is directly tied to the submodules.

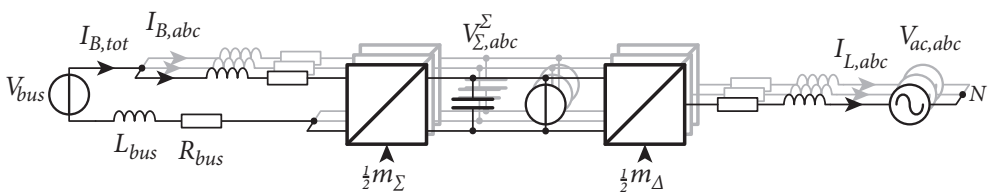


Fig. 121. Simplified equivalent schematic (neglecting the vertical balancing) when voltage-source-type energy storage elements are directly tied to the submodules.

In order to control such a converter system, the same approach as in §3.3.1 can be used, leading to the following conventional choice of tuning paths:

$$\textit{back-end}: \; m_{\Sigma,\alpha\beta\emptyset}{}^{(\emptyset Hz)} \rightarrow E_{\Sigma B,\alpha\beta\emptyset}{}^{(\emptyset Hz)} \rightarrow E_{B,\alpha\beta\emptyset}{}^{(\emptyset Hz)} \rightarrow I_{B,\alpha\beta\emptyset}{}^{(\emptyset Hz)} \rightarrow I^{\Sigma}{}_{\Sigma B,\alpha\beta\emptyset}$$
$$\textit{back-end}: \; m_{\Sigma,abc}{}^{(50Hz)} \rightarrow E_{\Sigma B,abc}{}^{(50Hz)} \rightarrow E_{B,abc}{}^{(50Hz)} \rightarrow I_{B,abc}{}^{(50Hz)} \rightarrow I^{\Sigma}{}_{\Delta B,abc}$$
$$\textit{front-end}: \; m_{\Delta,abc} \rightarrow E_{\Sigma B,abc} \rightarrow E_{L,abc} \rightarrow I_{L,\alpha\beta}$$

Naturally, such a choice of tuning paths would require to be associated with an appropriate supervisory layer responsible for managing the states of charge, such as:

- $I^{\Sigma}{}_{\Sigma B,\alpha\beta} \rightarrow SoC_{\Sigma,\alpha\beta}$ corresponding to the *horizontal balancing* of the arm-level SoCs.
- $I^{\Sigma}{}_{\Delta B,abc} \rightarrow SoC_{\Delta,abc}$ corresponding to the *vertical balancing* of the arm-level SoCs.
- $I^{\Sigma}{}_{\Sigma L,\emptyset} \rightarrow SoC_{\Sigma,\emptyset}$ corresponding to the *total energy control*.

This simple example shows that the integration of direct-attached storage fundamentally changes very little to the MMC control design. To some extent, this even facilitates the latter in the sense that *i)* the control of the summed capacitor voltages is no more required and that *ii)* the much higher amount of embedded energy is significantly relaxing the corresponding time constants and hence facilitating general power flows control problem. Consequently, a control design philosophy such as the one described in §3.3.1 comprising a strategy layer directly generating current references (see Fig. 58, page 75) is sufficient, and is in turn the appropriate choice in the light of the inversion-based control design principles.

Finally, the use here of the arm-equivalent model (see §2.2.3) is also an opportunity to recall that it postulates the existence of an underlying balancing mechanism, which is here assumed to by of Marquardt type. That said, the works of Maharjan and Vasiladiotis both rely on Akagi-type balancing mechanisms, whose equivalence to the Marquardt-type balancing approach remains to be demonstrated. The formal comparison of the Marquardt- and Akagi-type modulation and balancing approaches is therefore a relatively sensitive but unexplored topic, especially when the voltages are substituted with states of charge. As a matter of fact, such an investigation could be elegantly supported by a functional analysis such as using the EMR formalism.

5.3.1.2 USE OF DC/DC SERIES INTERFACES

In case an active series interface is implemented, each arm may desirably be assimilable to the EMR – and its underlying model – represented in Fig. 122:

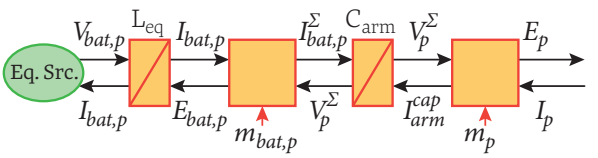


Fig. 122. Obtainable EMR in case the interfaces and the energy storage elements can be also modeled with a unique arm-equivalent approach.

Here again, such a representation relies on the validity of the assumption of arm equivalence (see §2.2.3), which allows to disregard the cell-level balancing issues inside the model. This implies that the control of the reversible buck converters must be assimilable to a unique and fictive arm-level converter which guarantees the SoC balancing internally, as for the submodule voltages. Concretely, this postulates that the same principle as in equations (3)-(4) can be applied to the energy storage elements. Equations (61)-(62) illustrate the suggested approach:

$$E_{bat,p/n}(t) = \sum_{k=1}^{N} m_{bat,k}(t) \cdot V_{SM,k}(t) = \underbrace{\frac{1}{N}\sum_{k=1}^{N} m_{bat,k}(t)}_{s_{bat,p/n}(t)} \cdot \underbrace{\sum_{k=1}^{N} V_{SM,k}(t)}_{V^{\Sigma}_{p/n}(t)} \tag{61}$$

$$E_{bat,p/n}(t) = m_{bat,p/n}(t) \cdot V^{\Sigma}_{p/n}(t) \tag{62}$$

Hence, provided that the available SoC balancing mechanisms allow the use of such a model, the operation of the whole MMC phase-leg can be described by the EMR of Fig. 123, which can be compared to the one of Fig. 120:

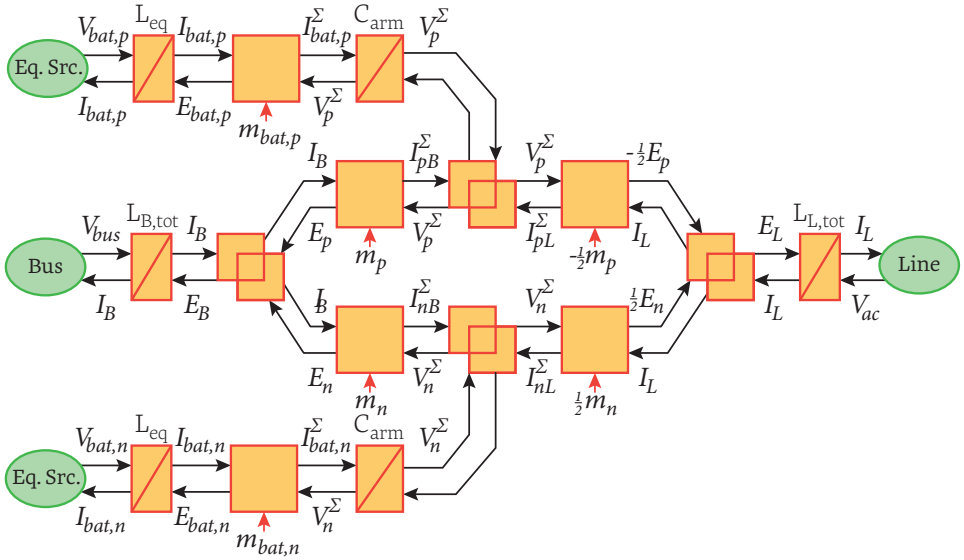


Fig. 123. EMR of a complete phase-leg with integrated energy storage using active series interfaces.

This representation is interesting as it clearly shows that, from a functional point of view, the embedded energy storage is simply inserted on the fictive intermediate busses by means of the corresponding equivalent converters. In other words, the three conversion chains are functionally joining on these busses, as illustrated in Fig. 121 (neglecting the vertical balancing):

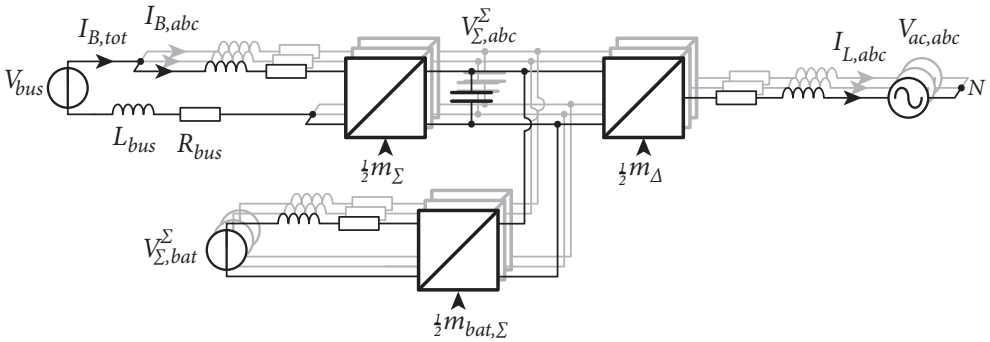


Fig. 124. Simplified equivalent schematic (neglecting the vertical balancing) when additional buck-type interfaces are added in the submodules.

This kind of perspective is similar to what can be understood through the various operating modes described by Trintis et.al. in [195], except that in the latter the MMC control implementation is preventing this fundamental notion of intermediate bus to be truly perceived. This is all the more regrettable that with means of interpretation

as simple as Fig. 124, it is relatively easy to reduce the overall complexity of all *power* and *energy management* considerations to simpler and known problems and to drawn the corresponding parallels in order to reuse existing techniques.

Overall, it can be thus seen that means to tackle the control design (including the development of energy management mechanisms) are readily available, thanks to the functional perspective brought by such representations. This is in turn the whole purpose of the developments made in this section.

However, it must be noted that one of the keys challenges probably lies here again not in the high-level control design, but in the enforcement of the validity of the underlying model, particularly with respect to the arm-level equivalence of the active series interfaces. Indeed, the simplification related to eq. (61)-(62) suggests the presence of a Marquardt-type balancing mechanisms on the interfaces as well, whose implementation has apparently never been addressed yet. On the other hand, existing techniques such as those used by Trintis [194]-[195] and Vasiladiotis [199] are achieving the same result, but using an Akagi-type approach.

Once again,[13] this disparity between these paradigms calls for a more formal way to unify them under the same model and to determine the exact equivalences. Nevertheless, despite the absence of such results, the validity of eq. (61)-(62) may yet be guaranteed by Akagi-type techniques, of which two variants are described hereafter:

a) The folded cascade

This approach, presented in [198]-[199] defines tuning paths that are directly regulating the battery SoC from the main converter drawing active power from the line side. This is in turn the same principle as developed earlier by Maharjan [189]-[190], to which a current + voltage closed-loop control cascade is added in order to regulate the voltage of each submodule independently, using energy from the corresponding battery. These tuning paths are hence forming partly folding loops that are first reaching the SoC of the batteries and then coming back to the capacitor voltages. Fig. 125 illustrates the corresponding principle:

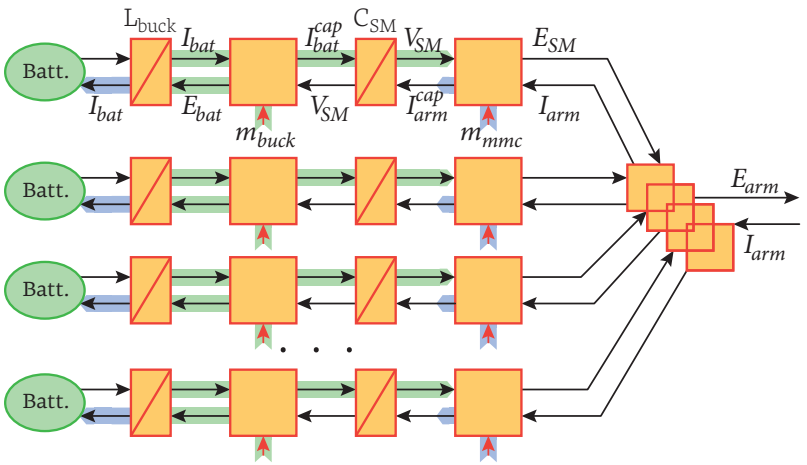


Fig. 125. EMR of one converter arm constituted by N submodules with split EES and active series interfaces. The depicted selection of tuning paths[14] correspond to those suggested in [198]-[199].

13. See also page 158.

14. Strictly speaking, these are not really tuning paths, since the tuning variables here called m_{mmc} are directly exploited to manage the SoCs, without implementing the corresponding cascade of causal relationships (the intermediate variables are *not* controlled).

In turn, even though the effectiveness of this approach has been clearly demonstrated in [198], it implies tuning paths that are crossing each other, hence leading to superposed power flows that may be of opposed signs, if not contradicting. Besides, and more importantly, this approach is inoperative unless a battery is present. Consequently, a significant part of the MMC control structure differs between the cases with and without energy storage, what can be a significant impediment when split storage is desired to be implemented inside an already existing converter (typically in order to extent the set of ancillary services that the converter can provide).

b) The straight cascade

Alternatively, tuning paths can be defined such that the faster control loops are maintained inside the slower ones, and such that the tuning paths are not crossing. It can for instance be imagined that the regulation and the balancing of the submodule voltages is achieved as in a conventional MMC and that additional and independent tuning paths are implemented in order to control the SoCs of the batteries, drawing energy from the submodules. In turn, this is the approach that is indirectly suggested by Trintis in [195]. The corresponding choice of tuning paths is shown in Fig. 126 :

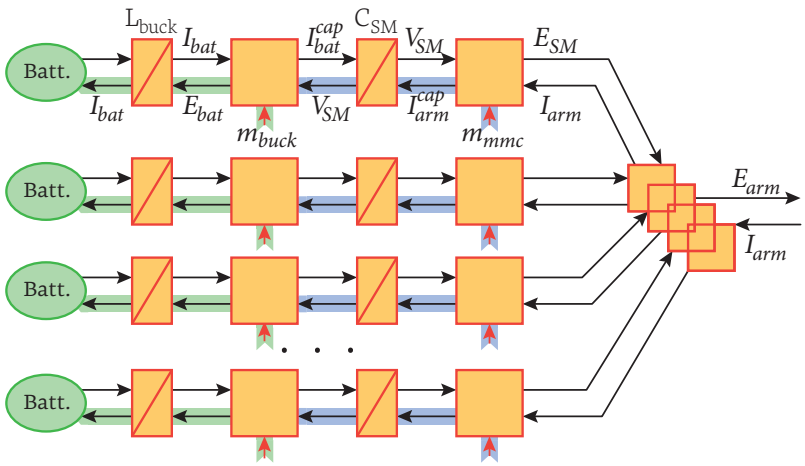


Fig. 126. EMR of Fig. 125, but with an alternative choice of tuning paths that correspond to a more conventional cascaded control hierarchy.

This second approach allows to keep the main converter control unchanged in comparison with the case without storage, to which the additional control problem is added, corresponding to the control problem posed by the energy storage itself. Besides, in the light of Fig. 126, the corresponding tuning paths may even be the most natural choice of the approaches, but has apparently not been implemented yet and still required to be validated. Furthermore, this approach is also certainly well suited to address the SoC balancing problem in a similar way to the submodule balancing problem, that is by modeling the corresponding behavior with an equivalent fictive and self-balanced multilevel DC/DC converter. In turn, this would open the door to Marquardt-type balancing approaches as well (see above).

Overall, it can be seen that the use of interfaces is completely changing the game in terms of power flow management and control design, compared to the case without them. Indeed, when an active series interface is used, an additional tuning variable is available, what allows to practically separate the conventional MMC control problem from the energy storage-related control design and energy management. The com-

parison of Fig. 121 and Fig. 124 clearly highlights this contrast. In terms of system engineering, it can hence be expected that this fundamental difference in controllability is eventually a crucial element to the choice between an active serial interface and all other types.

5.3.2 INTEGRATION OF HYBRID ENERGY STORAGE

The previous sections have discussed *i)* how can energy technologies be integrated into MMCs and *ii)* how the principles of model inversion can be used for the control design of the corresponding systems. In parallel, for fast and demanding load levelling applications, section 5.2.4 has suggested the integration of multiple energy storage technologies inside MMCs.

In this context, the aim of this section is to outline how can multiple technologies be simultaneously integrated into these converters, using two examples of topologies taken from Chapter 3. In both cases, the goal is not to make here the complete control design of these structures, but essentially to show how the inversion-based control design methodology applies to these specific cases.

5.3.2.1 INDIRECT AC/DC/AC WITH HYBRID ENERGY STORAGE

In the case of indirect 3-AC/DC/1-AC frequency conversion structure, the most natural approach to integrate hybrid split energy storage is probably that of Fig. 127 :

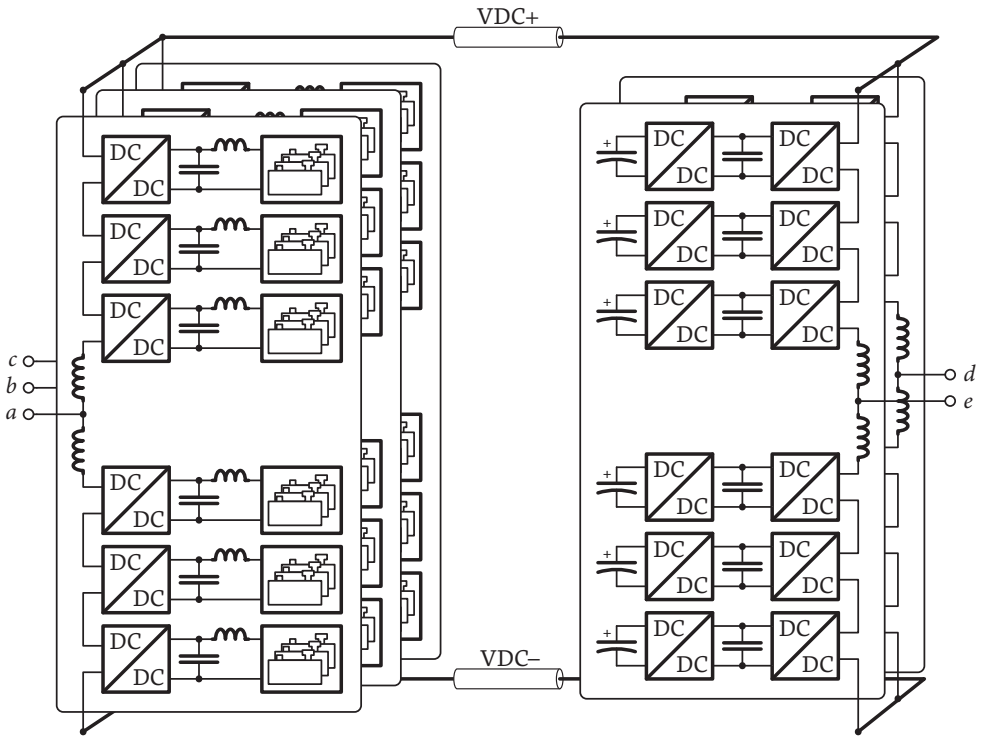


Fig. 127. Indirect 3-AC/DC/1-AC with hybrid storage.

Indeed, in order to keep things simple and given the storage technologies suggested in §5.2.3, it is reasonable to propose to split the technologies between the two half-converters, placing supercapacitors the railway side, which is subject to the most intense load variations, and have batteries placed on the 50 Hz side.

Based on Chapter 2 and §5.3.1, a possible EMR corresponding to the converter structure of Fig. 127 can be easily derived. The result is shown in Fig. 132 on the next page, while an equivalent scheme is also depicted in Fig. 133.[15] In these representations, the converter arms along with the corresponding energy storage elements are both modeled using an arm-equivalent approach, whose validity is discussed in §5.3.1. Besides, the previously-introduced choices of interfaces can be easily identified : direct connection for the batteries and controllable interfaces for the supercapacitors. In the end, the resulting EMR is relatively complex, involving no less than 14 power sources, 15 state variables and numerous power flows paths. On the contrary, thanks to the fact that the elements related to the vertical balancing are neglected, the equivalent scheme presented in Fig. 133 shows a relatively simple way of describing the functional nature of this converter system, what also reveals that this complete converter topology may also be interpreted easily, provided that some basic simplifications are made.

Based on these representations, it is possible to easily design the control of such an installation. A possible approach may be envisaged using tuning paths similar to those of §3.4.5, what leads to control these converters independently of the presence of energy storage. More specifically, the tuning paths associated with Fig. 81 are directly applicable, except those related to the control of the summed capacitor voltages on the three-phase side. Indeed, according to §5.3.1.1, since the batteries are directly tied to the submodules and considered as sources, there is no need to implement a closed-loop voltage control.

On top of that, a supervisory layer can logically be tasked to produce the necessary setvalues for the remaining manipulable inputs. This thereby represents essentially three main power flows for which the references must be defined. Among the most basic energy management mechanisms that can be imagined, the following proposal can be made :

– The *railway-side line current* can be typically computed as a function of the desired active-reactive power exchanges or more advanced objective such as active filtering or resonance damping. With the presented choice of tuning paths, the corresponding active power is directly drawn from the batteries across the DC link. Apart from that, from the perspective of the energy management of the converter, there is no strategical aspect here, as the corresponding current value and shape are assumed to be constraints.
– The reference values for the *summed capacitor voltages on the railway side* can be typically computed such that the 33 Hz power pulsation is partially or totally absorbed by the two corresponding phase-legs. The strategic aspect here involves distributing intelligently this power pulsation. In the present case, since batteries are present on the three-phase side, the most natural choice is probably that corresponding to enforce a perfectly smooth current on the DC bus.
– The current references related to the *power injected from the supercapacitors* must be computed such that the supercapacitors are kept balanced. Moreover, the simplest strategy is to define the power injection from supercapacitors as a high-pass filtered version of the active power reference on the railway side. In this way, the power flow crossing the DC bus and charging or discharging the batteries is an already smoothed version of the power fluctuations of the railway side.

15. As throughout this work, for the sake of clarity, this equivalent scheme disregards the vertical imbalances. However, the latter could of course be represented as well, as in Fig. 35.

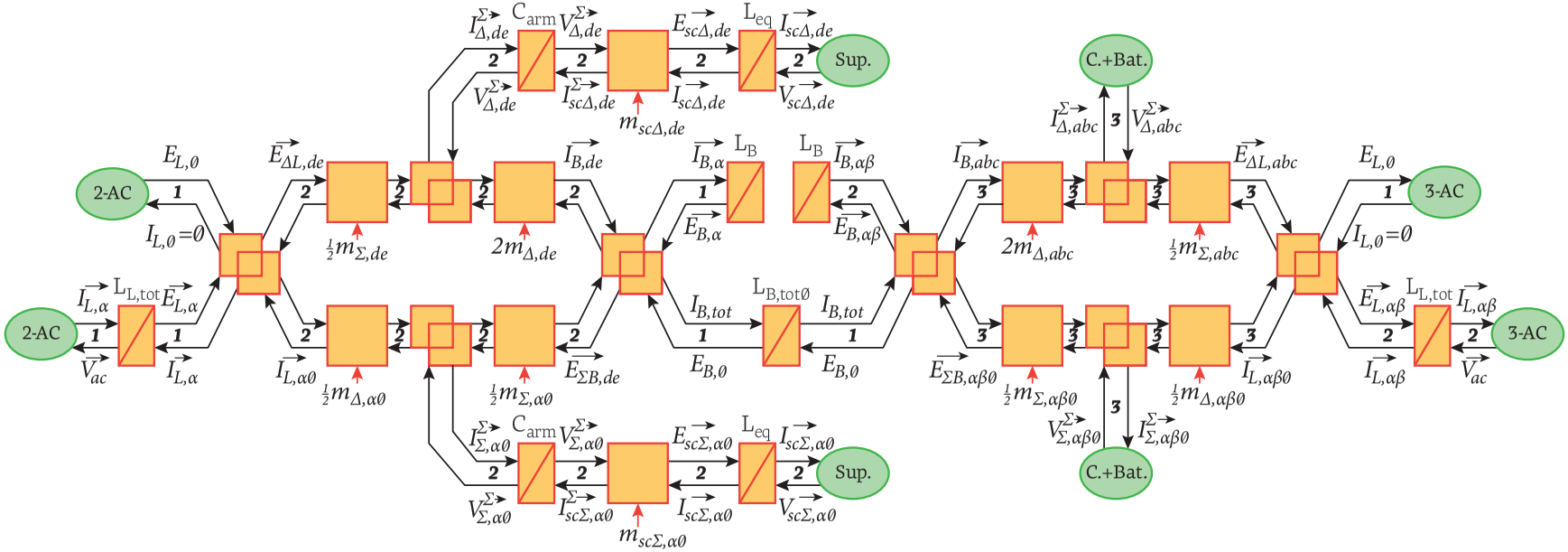


Fig. 132. EMR of the complete back-to-back 1-AC/DC/3-AC conversion system with integrated hybrid storage.

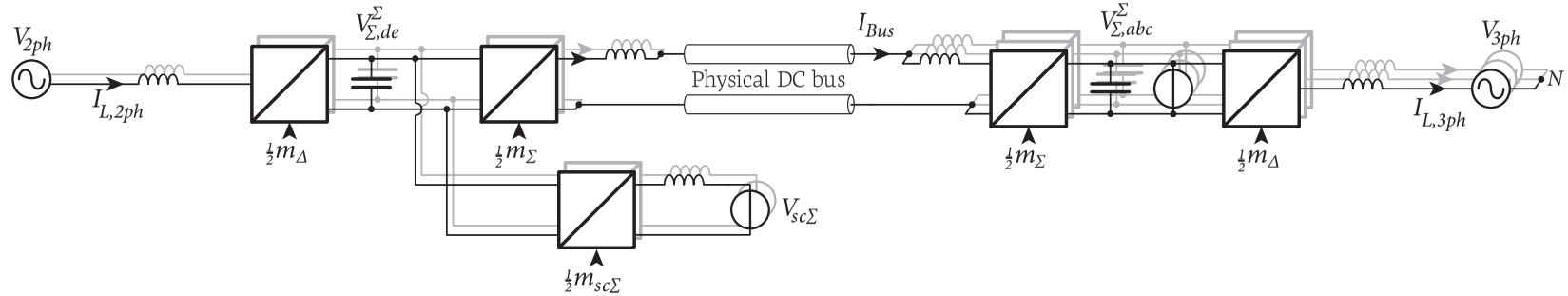


Fig. 133. Equivalent functional schematic of the EMR of Fig. 132 neglecting the vertical imbalances.

– With this choice of tuning paths, the *current references on the three-phase side* correspond to the active and reactive power exchanges between the batteries and the 50 Hz grid. This allows to manage the three-phase side entirely independently of the railway side, the batteries serving as a buffer between the two. The most basic strategy is thus to maintain the references on the three-phase side to the values defined in the corresponding commercial bid.

In the end, this is of course only an example of a possible choice of implementation among others. This nevertheless shows that with such a choice of topology, the control design choices are still relatively easy to make and their implementation should not rise any particular concerns.

5.3.2.2 DIRECT AC/AC WITH HYBRID ENERGY STORAGE

In the case of the direct 3-AC/1-AC conversion structure, the same kind of separation of the technologies is not possible. Therefore, provided that several technologies must be used, they must be mixed inside the converter arms, as shown by Fig. 128:

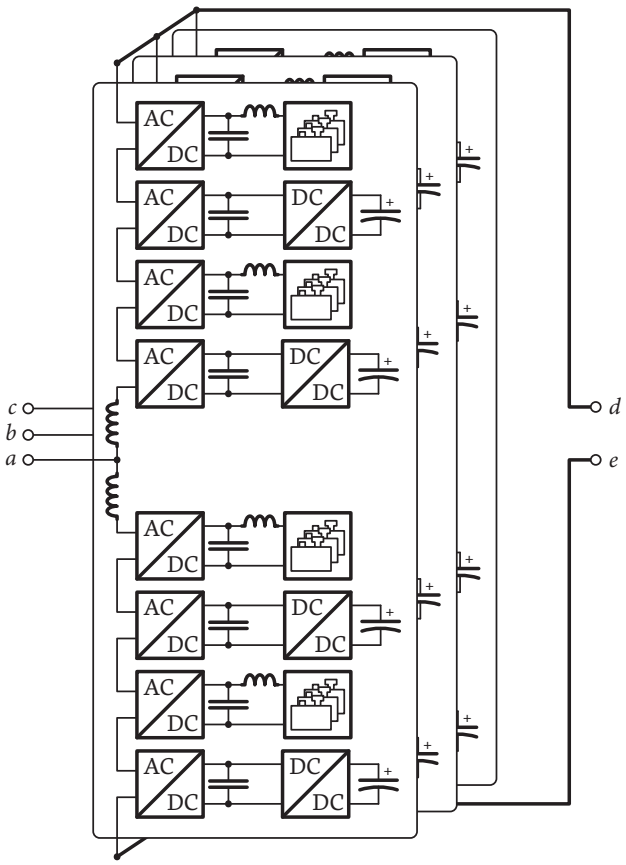


Fig. 128. Direct 3-AC/1-AC with hybrid storage.

In terms of modeling, the same kind of approach as in §2.2.3 and equations (3)-(4) can be applied here. The result is illustrated in Fig. 129, which is essentially grouping the cells associated to the same storage technology to a corresponding sub-arm. By doing so, several (here two) sub-arms can be considered to be connected in series in each arm, what is functionally equivalent to having two large fictive submodules per arm. Fig. 130 shows how the EMR of Fig. 29 can be adapted to account for this new model.

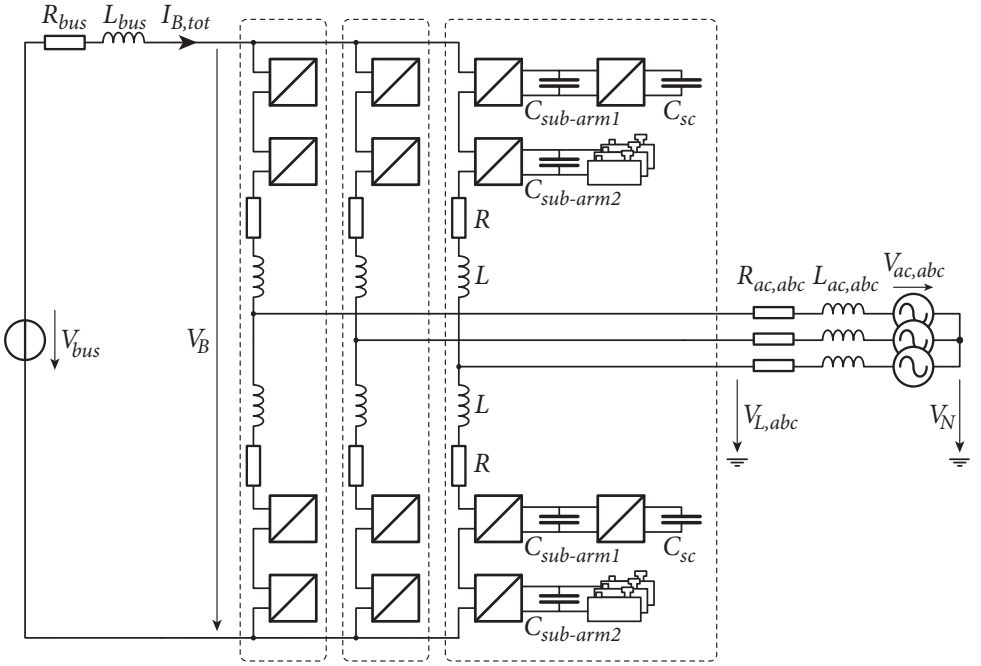


Fig. 129. Arm-equivalent modeling approach extended to the integration of hybrid energy storage.

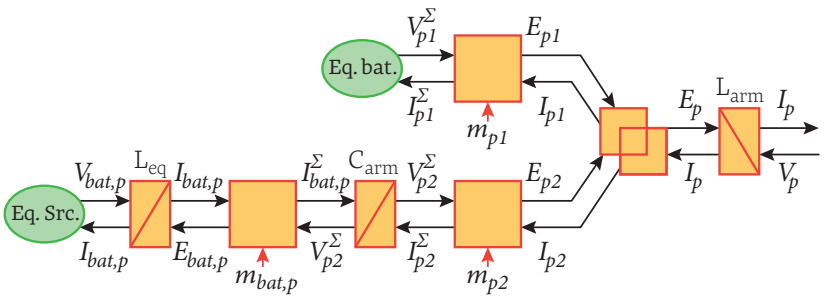


Fig. 130. EMR of a MMC arm with integrated energy storage of mixed technologies.

By observing this EMR, it can be immediately observed that the integration of energy storage in the direct 3-AC/1-AC frequency conversion topology is rising more complex concerns than in the indirect conversion structure. In particular, due to the mixing of technologies and interface types inside the same arms, the corresponding sub-arms must be balanced between each other, what can be expected to lead to a more complex control design.

Therefore, a significant amount of future investigations seem necessary in order to establish and validate possible control techniques for this particular scenario. To that end, the simple perspective offered by Fig. 130 probably constitutes a good starting point. Besides, it also shows that such an objective may intuitively be considered as feasible. Indeed, in the absence of a better option, it can for instance be imagined that the overall balancing concerned are managed by a combination of existing techniques such as:

– Within the sub-arms, the balancing could typically be implemented using a Marquardt-type balancing technique, hence guaranteeing the validity of the modeling approach shown in Fig. 129.

– Between the sub-arms and at the converter-level, an Akagi-type approach should be capable of guaranteeing a proper balancing, although the different time constants may complicate the control design on that matter.

At the converter level, the simple summation of the two partial EMFs can be directly exploited to equation (15) such as in (63):

$$\begin{pmatrix} E_L \\ E_B \end{pmatrix} = \mathbf{T}_1 \begin{pmatrix} E_p \\ E_n \end{pmatrix} = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2} \\ 1 & 1 \end{bmatrix} \begin{pmatrix} E_{p1} + E_{p2} \\ E_{n1} + E_{n2} \end{pmatrix} \tag{63}$$

This naturally results in the EMR of Fig. 131, corresponding to one converter phase-leg, here represented without a common-mode/differential-mode decomposition.[16]

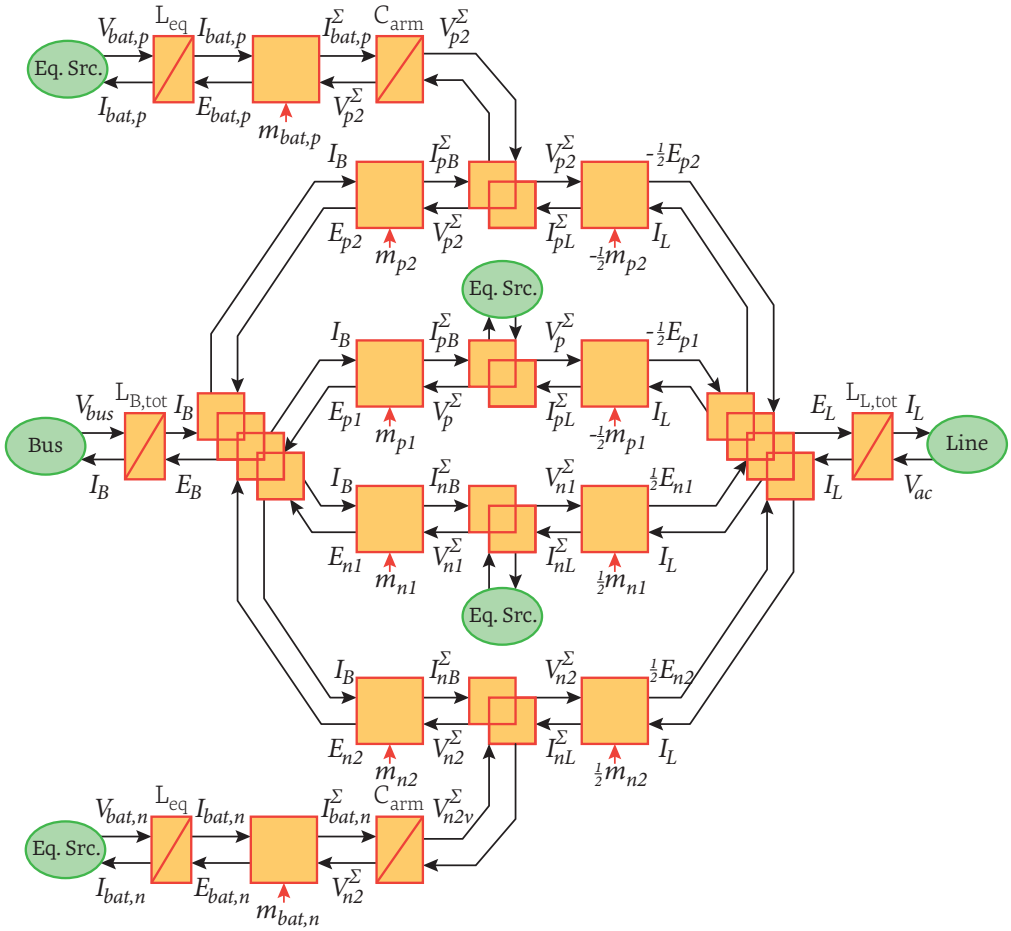


Fig. 131. EMR of a phase-leg in case two different types of energy storage are directly integrated in the converter arms.

Overall, such a representation shows that the integration of hybrid storage poses truly new challenges and that the corresponding power flows become really difficult to interpret intuitively. This naturally calls for additional efforts in order to further highlight the functional nature of such a system as well as to develop the corresponding control mechanisms, which can be expected to be far from trivial.

Furthermore, this also shows that, at some point, the control complexity becomes such that the introduction of additional elements (additional tuning variables) may be ben-

16. Of course, the latter could be developed as well by adapting the developments of §2.4.3.

eficial, even if only for the sake of simplifying the control implementation. Indeed, a possible alternative to the above approach would be to implement active series interfaces for all submodules, what would allow to keep the control unchanged compared to the case without energy storage and hence to manage the storage units through their dedicated interfaces only (typically, as suggested by Fig. 126).

In the end, apart from the considerations already mentioned in §5.1.2, these remarks suggest that the presence, respectively the absence, of a controllable input is probably the most important decision criteria when selecting the type of interface to interconnect the energy storage elements to the submodules. Indeed, for such complex systems, the control complexity is most likely related to a design cost that must be weighted against other system engineering aspects.

Hence, if only one thing had to be retained from the two above examples of hybrid split storage, it is that the integration of storage cannot be done without questioning the overall converter topology, nor considering in depth the needs in terms of degrees of freedom, that is in terms of tuning variables. In this sense, the analysis of the various challenges affecting the system design under a macroscopic and energetic angle is probably an approach worth pursuing.

5.4 SYNTHESIS

5.4.1 ENERGY STORAGE IN RAILWAY GRIDS

Chapter 1 showed that modern static converters are particularly attractive when combined with energy storage as this enables to provide a broad range of ancillary services. In this context, this chapter has shown that MMCs are an excellent technical solution on that matter as their implementation truly involve a mutual exchange of benefits between the converter and the energy storage system.

The first part of this chapter attempted to illustrate concretely how MMCs with split energy storage can be put to use in railway grid applications. In turn, the main question was to determine whether there is a possible match between existing needs and technical possibilities, both of which are issues that are still relatively unclear. It was chosen here to start from the needs and to focus on applications that do not compete with pumped hydro storage. This has lead to "fast" and demanding scenarios, which are flirting with the limits of feasibility. That said, by having the opposite though and thinking in terms of what can be done with a given technology (it's the solution looking for a problem to solve !), such thoughts would have probably resulted in other remarks. For instance, with 2-3 relatively deep cycles per day (what corresponds to something feasible for a recent battery technology with a high cycle life), interesting applications can already be considered with respect to renewables integration. However, it remains to be seen whether this is a need that cannot be better met by another solution, such as pumped hydro storage.

In any case, since the detailed assessment of these applications and prospective technical solutions directly calls for an evaluation of their economic profitability, no further comments will be made here on this respect. On the other hand, it is worth noting that it seems particularly interesting to consider these applications primarily as a complement to other ancillary services (voltage support, active filtering/damping),

what corresponds to more immediate needs. In turn, the establishment of such facilities could even be done in two phases, what encourages to adapt the control design in such a perspective.

Anyway, if there is a need for fast applications that require high amounts of energy exchanges and a high cycling capability, it is then possible that no energy storage technology is really well suited, what indirectly suggests hybridization as a possible alternative to significant over-sizings. This comment of course extends beyond the sole applications in railway grids, but is particularly evident here, as the orders of magnitude involved prevent to divert a storage technology too far out of its target applications.

5.4.2 CONCLUSIONS

As shown by this chapter, the integration of energy storage in MMCs poses various constraints, typically related to *i)* the voltage profiles of the employed storage elements or *ii)* the filtering of the current components flowing into them. Besides, *iii)* the integration of storage also rises questions with respect to the controllability of the corresponding power flows. This results in a broad combination of *system engineering issues*, most of which are related to unsolved questions.

In this context, this chapter has provided some insight on these issues, which has allowed to review the state of the art and present it in a way that suggests a systematic and macroscopic approach of these issues. Its main conclusions are as follows:

a) Selection of the technologies

In general terms, the most attractive energy storage technologies for split storage applications are those that *i)* store the energy directly in the electrical form and *ii)* are adapted to an operation at a floating potential. Among them, the selection of a particular technology should ideally be achieved based on the needs of the application. However, as presented earlier, particular cases can lead to choices that account for a large over-sizing or the hybridization of several technologies.

b) Selection of the interfaces

This chapter has first suggested to select the type of interface as a function of the constraints set by the chosen storage technology. In such a case, even though certain decision criteria remain subject of controversy, the following conclusions can be drawn, which slightly differ from those that can be found in the literature:

- When the energy capacity of the storage elements cannot be fully exploited without stepping-up/stepping-down the voltage from the submodule, the *active series interface* is almost indispensable and is an evident choice. This is for instance the case with capacitors or supercapacitors.
- When the storage elements can be fully exploited without an interface, but when some filtering is still required, the two *active interfaces* are likely to be the most attractive solutions. Among them, the final choice certainly depends whether the controllability of the local power flows is required or not.
- Finally, if the voltage characteristic of the storage elements is directly usable as such – i.e. is sufficiently flat regardless of the SoC – the simpler is probably the better choice, what calls for a *direct, or almost direct connection*. This is for instance

the case with batteries, provided that the presence of strong alternating current components is not causing any other issue than increased Joule losses.

With respect to the choice of the interfaces, this chapter has also illustrated that in the most complex cases such as those related to the integration of hybrid split storage, the controllability of the corresponding power flows is of utmost importance, what can lead to favoring the choice of the active series type of interface for that particular objective only.

c) Control design

As in the previous chapters, it was shown here that the use of a functional approach results in several possible interpretations that are very useful to the control design and provides all the necessary tools for its systematic implementation.

In case active series interfaces are used, it has been shown that alternatives to the existing approaches may be worth investigation, especially with respect to the choices of the tuning paths. This would allow a potentially more rigorous layerization and improved portability of the control between the cases with and without storage. Moreover, in the case where the storage elements are directly tied to the submodules, it has been shown that the integration of storage is rather facilitating the control design in the sense that the closed-loop voltage control of the summed capacitor voltages becomes irrelevant and the performance requirements with respect to the power flow control are alleviated. Finally, it was shown that when several energy storage technologies are integrated inside the same arms, the corresponding control design is highly complex and remains a subject of future research.

In the end, owing to these remarks and even though the development of energy management mechanisms remains here a future perspective, the presented control design methodology has proved that all the necessary means are available pour bien faire. This comment regards mainly the control design, but also holds with respect to all the benefits derived from a functional and macroscopic vision of the system engineering, such as the selection of the interface type. Furthermore, as the last part of this chapter has shown, such tools of analysis and design are becoming almost indispensable with complex systems such as MMCs with hybrid split storage, since they are key to divide / modularize the whole control problem into known and already well mastered functional sub-problems. This is also why, although significant work is still ahead with respect to the control design of MMCs with split storage, there is a good chance that a significant part of the challenges can be simply solved by enabling a better fragmentation and hierarchization of the corresponding issues.

5.4.3 FUTURE WORK

As the first part of this chapter has repeatedly mentioned, several design issues would be worth investigating in a global or systemic perspective. In particular, the following questions seem especially interesting:

– Provided that the impact of the large low-frequency current components flowing in the batteries in case of direct connection is "only" a matter of Joule losses and hence of temperature (see §5.1.2 *b.*), is it more appropriate to tolerate the corresponding losses, or to add typically reversible buck converters (with an imperfect efficiency), at the risk of ending up with the same amount of losses to evacuate?

- A important part of the attractiveness of the split integration of energy storage in MMCs is related to the possibility to use the converter's own balancing mechanisms in order to balance the SoCs and usage of the storage elements. However, being given the usual voltage levels in high power applications, these elements must probably be balanced inside each submodule level as well. This naturally leads to the question of defining the most appropriate degree of modularization / voltage level for a given technology / application ?
- The two examples of network interties with hybrid split storage have shown that the global choice of topology can be affected by the integration of energy storage. In that particular case, the indirect frequency conversion structure may even be more advantageous than the direct one. Is it really a reasonable conclusion from a systemic point of view, or is it more attractive to make use of the direct structure, even putting interfaces in all cells for the sake of simplifying the control design ? This last question also rises the larger issue of the evaluation of the "cost of complexity," what is likely to be a important issue with such systems, especially as it could be possibly counter-balanced by sacrifices in terms of efficiency, volume, etc.

6 GENERAL CONCLUSIONS AND PERSPECTIVES

6.1 SUMMARY OF THE CONTRIBUTIONS

Based upon the context of the railway energy grids, this work has shown that thanks to a good controllability and unique capabilities, MMCs are flexible enough to adapt easily to a variety of needs and are thus very well suited to the supply of ancillary services.[1] The needs for such service are currently growing in the railway grids, and may become important as well in tomorrow's 50 Hz medium-voltage networks, with which they share numerous common points. Among them, some are calling for energy storage, whose integration into MMCs can be achieved in a split manner, allowing a mutual exchange of services between the converter and the energy storage system. Furthermore, provided that the design of the control hardware and control has been anticipated accordingly, the energy storage can be seen as an additional plug-in feature that can augment the set of functions / services of an existing facility.

With respect to split-storage, Chapter 5 has presented a picture of the existing knowledge on this subject and found that many system engineering issues are still pending. Moreover, for the most demanding applications, this chapter has suggested the hybridization of several energy storage technologies within a single converter and has shown how this concept can be implemented in two types of frequency conversion facilities. These examples have shown that such systems are complex to control, which is why the controllability of the local power flows inside each storage element is probably an underestimated aspect in the choice of interfaces that connect these elements to the submodules. In addition, towards the control of such complex systems, it is important to first make sure of the sanity of all the existing control mechanisms. This motivates to take a step back on the control design techniques, which is the central objective of this thesis.

Chapter 2 has applied a functional analysis approach to MMCs, based on several types of representations, including EMRs. Consistent results have been derived from the study of single phase-legs and have been extended to several variants of multiphase topologies as well as different operating conditions. In the end, these representations primarily constitute a set of analysis tools, which have resulted in one of the original contributions of this work, namely a new interpretation of the basic operating principles of this family of converters. Indeed, it has been shown that, from a functional point of view, MMCs can be assimilated to associations of single-phase and two-stage conversion systems. Consequently, MMCs are thus neither truly VSCs nor CSCs, but

1. In railways, the supply of ancillary services is primarily possible from the network interties, as it combines several uses, but is also conceivable independently (at the weak points of the grid) with services such as voltage support, active filtering / damping or UPS-type capabilities.

rather both simultaneously. These findings are important because they *i)* can explain most of the unique properties of MMCs and *ii)* allow to address the control design with a new perspective.

On this last topic, Chapter 3 has shown that the control design of MMCs can be based on a strict methodology and has shown how to do so. In addition, several important nuances have been highlighted:

- First, a clear line has been drawn between the part of the control design that is strictly model-based and that which is not. Therefore, even though a significant amount of work is still needed to compare in detail the existing techniques, it has been shown which ones of them are close to the strict inversion of the model and which ones are not. Furthermore, by making a parallel with the control design of a conventional three-phase inverter, it has been shown that the non-strictly model-based elements remain also fully justifiable. This has finally allowed to clearly define the limits between what is feasible and what is not. One especially thinks here of the aspects of the decoupling of the currents or that of the summed capacitor voltages.
- Second, another clear line has been drawn between the state-space control design and that of the strategical issues such as related to the power flow/energy management and/or to the exploitation of the MMC-specific degrees of freedom. In the light of the principles of the inversion-based control design, it has been suggested that the shaping of the summed capacitor voltages should be handled by a specific control layer, the voltage and current control then implemented by fast and unfiltered subordinated closed control loops. This type of hierarchized control seems *i)* important in order to ensure that the strategic control objectives are actually achieved (such as the minimization of the capacitor voltage ripple), but also *ii)* essential for the proper structuring of the control as to allow the future implementation of a true energy management layer, particularly in the context of the integration of energy storage in MMCs.

In the end, the most important issues are not found within the definition of the control structure as such (which is strictly model-based), but rather in the definition of the exact content of each of the blocks constituting this structure (which is not strictly model-based, but depends on the operating conditions). Besides, it has been shown that by staying close to the inverse model, the presented approach easily results in control schemes that are:

- Relatively simple, owing to cascaded structures, but nonetheless guaranteeing *excellent performances* thanks to the extensive use of feedforwarding techniques, whenever possible.
- *Generic and comprehensive* as they can be easily designed such that they account for a broad range of operating conditions. The operation under asymmetric grid conditions is one example, but one also thinks of the seemless passage between three-phase inverter to the 3-AC/1-AC frequency converter, the low-frequency operation as in drives, or even to a possible operation as active filters.

  Moreover, these schemes correspond to what is necessary in order to fully exploit the possibilities of MMCs such as the decoupling of the bus- and line-side currents or the exploitation of the degree of freedom constituted by the circulating currents, the shaping of the summed capacitor voltages, etc.

– *Strictly layerized*, hence modular and therefore portable from one application to another, or from some operating conditions to some others, with a minimal adaptation effort limited to a few functional blocks only.

Chapters 3 and 4 have largely demonstrated these three characteristics trough numerous simulation results, which have also been validated experimentally for the most representatives ones. It should also be noted that although the focus was mostly set on the approach itself, the obtained results are entirely state-of-the-art, since they are the first comprehensive experimental results under asymmetric grid conditions.

Chapter 5 has shown that with built-in storage, especially with active series interfaces, alternatives to existing control techniques could be beneficial. In this sense, with the systematic approach and interpretations proposed by this work, all the necessary tools to support the control design are available, allowing to compare the possible strategies and implement the most relevant option. In addition, this chapter has also shown that the use of such tools for analysis and design becomes virtually indispensable when it comes to dealing with problems as complex as those of MMCs with hybrid split storage.

In parallel to these considerations, as recalled in Chapter 4, it is important to bear in mind that all these developments are based on an arm-equivalent model, which postulates the existence of independent mechanisms balancing the submodules. This assumption is very ambivalent in the sense that it allows to disregard a large part of the control design issues, but also requires a complex implementation for the modulation. As part of this work, the coding in VHDL language of the modulation/balancing mechanisms for the submodules has notably been the source of many difficulties.

More generally, it is clear that this work remains fundamentally limited to the Marquardt-type (or sort-and-select) balancing procedures. Indeed, the keys of equivalences to make the link with the Akagi-type approaches are still missing. It seems therefore important that ways are found in order to break the split between these two paradigms and hence allow to get a real overview of the MMC control design.

In the end, the control design of MMCs appears to be a relatively uneasy task despite an apparently simple topology. This is the price to pay for a mechanical structure and performances that are typical of a single-stage topology, while the control capabilities are those of a dual-stage conversion system. On the other hand, once the double-stage nature of the MMCs and their arm-level balancing mechanisms have been assimilated, the control design reveals to be significantly more intuitive. This ascertainment also holds with respect to the control design elements that are not strictly model-based, for which the presented methodological developments also most certainly help.

At the application level, either in railway applications or 50 Hz medium-voltage applications, where MMCs probably have a nice card to play, especially in combination with energy storage. That said, it is likely that the overall attractiveness of MMCs compared to other technologies decreases at the same time with the power level, unless their reliability, flexibility and global scalability justify on their own the use of such a technology. It therefore seems important that the control (or at least its design) is not a handicap; in other words, that the flexibility provided by the structure of the MMC is not undermined by a complex control design. This also justifies the objectives of hierarchization and layerization present throughout this work, providing some clarity and ease of approach to the proposed control schemes.

6.2 FUTURE RESEARCH PERSPECTIVES

The most direct extension of this work is to develop the strategic layer that has been often mentioned, but never implemented. For this purpose, the first step would be to express the existing control strategies as references for the summed capacitor voltages. Existing developments related to the estimation of the ripple could be easily adapted for this purpose. Subsequently, the implementation of the actual energy management mechanisms can be considered in function of specific applications and energy storage technologies, probably giving rise to different optimization approaches.

On an entirely different aspect, a strong conviction drawn from this thesis is that a similar level of modularity should be made available within all parts of the overall converter design, that is not only in mechanical terms in the power section, but also in terms of control. This would require to evolve towards techniques that further enhance the segmentation/modularization of the control software and hardware, which could be key to provide total flexibility and scalability for all the elements constituting the MMCs. Multiple perspectives in this direction have been mentioned throughout this work. Among them, Chapter 4 presented some possible leads, especially concerning the integration of intelligence in submodules as well as the further distribution of the control. In this sense, it is likely that the use of distributed modulation techniques such as derived from Akagi-type approaches are an attractive approach to integrate a maximum – if not all – of the control functionality directly inside the submodules.

In more theoretical terms, it would finally be interesting to see if the entire control design could be systematized, that is not only in terms of control algorithms, but also in terms of physical placement of the corresponding functions. In other words, this would correspond to determining an "inversion-based control segmentation" approach able to place the control blocks among the suitable hardware processing units (DSP, FPGA, etc.). In such a case, the control design could become fully systematic, thereby also opening the door to automated control synthesis techniques.

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7.5 STUDENT PROJECTS

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INFORMATIONS PERSONNELLES

- Date de naissance : 25 septembre 1986
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EXPÉRIENCE ENTREPRENARIALE

depuis 2013 **Co-fondateur et directeur de la technologie** *imperix*

- Développement d'un système de contrôle commande dédié à l'électronique de puissance (Bbox) commercialisé depuis Q4 2014.
- Réalisation de solutions de conversion statique « clé en main » pour le micro-réseau expérimental du DESL (laboratoire de l'EPFL).

FORMATION

2011-2014 (att.) **Doctor Philisophiae en Energie** *Ecole Polytechnique Fédérale de Lausanne*

- Travail de recherche ayant trait au développement des convertisseurs modulaires multiniveaux (MMC) dans le cadre de l'alimentation du réseau électrique ferroviaire.
- Contribution aux techniques de modélisation et de contrôle des convertisseurs MMC avec stockage d'énergie intégré.
- Développement de dispositifs de contrôle-commande avancées dédiées aux applications d'électronique de puissance.

2008-2010 **Master of Science en Génie Electrique** *Ecole Polytechnique Fédérale de Lausanne*

- Spécialisation en « Electronique et Microélectronique »
- Travail pratique de Master sur le thème « Conception et réalisation d'un convertisseur modulaire multiniveaux triphasé»
- Projet de 8^{e} semestre sur le thème « Contrôle semi-actif du bruit par synthèse d'impédance »

Moyenne générale 5.7/6
Prix LEM récompensant un excellent travail pratique de Master

2005-2008 **Bachelor of Science en Génie Electrique** *Ecole Polytechnique Fédérale de Lausanne*

- Travail de Bachelor réalisé sur le thème « Réalisation d'un processeur de dynamique audio au moyen d'une puce PSoC »

Moyenne générale 5.5/6

2002-2005 **Maturité fédérale, option math-physique** *Gymnase de Burier, Vevey*

- Travail de maturité réalisé sur le thème « Réalisation d'un amplificateur audio de classe AB »

Moyenne générale 5.4/6
Prix de mathématique, physique et excellents résultats généraux

LANGUES

Français : Langue maternelle
Anglais : Courant à l'oral et à l'écrit, usage quotidien (niveau C1)
Allemand : Niveau scolaire post-obligatoire (niveau A2/B1)

INFORMATIQUE

Ingénierie : MatLab/Simulink, PLECS, Altium, PSpice, Simplorer, Solidworks, Inventor, Libero, ModelSim, Vivado, EMTP-RV, Tiphoon HIL
Langages : C, C++, VHDL, VHDL-AMS, HTML
Bureautique : MS Office, Photoshop, Illustrator, Indesign

VOLONTARIAT

depuis 2003 Membre de la station de sauvetage 7/08 du Secours Alpin Suisse, responsable d'intervention.
2009-2014 Entraîneur J+S et responsable juniors du Badminton Club de Château-d'Oex.
2005-2010 Délégué de classe, membre de la commission d'enseignement, membre actif de l'association des étudiants électriciens.

PUBLICATIONS

2014 M. Vasiladiotis, N. Cherix and A. Rufer, *"Impact of Grid Asymmetries on the Operation and Design of Modular Multilevel Converters,"* in IEEE Trans. on Ind. Electron., Acceptance Pending.

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2012 N. Cherix, M. Vasiladiotis and A. Rufer, *"Functional Modeling and Energetic Macroscopic Representation of Modular Multilevel Converters,"* in Proc. EPE-PEMC Conference, Novi Sad, Serbie, Sept. 2012.

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2011 M. Vasiladiotis, S. Kenzelmann, N. Cherix and Alfred Rufer, "*Power and DC link voltage control considerations for indirect AC/AC Modular Multilevel Converters,"* in Proc. EPE Conference, Birmingham, Sept. 2011.