Charge-transport properties of monolayer MoS_2 at the interface with dielectric materials

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Through the creatures Thou hast made
Show the brightness of Thy glory...
Massy rock and tender blade
Tell the same unending story:
"We are Truth in form arrayed."

James Clerk Maxwell

To my family.

To all my good friends in Italy, Canada, Switzerland...

Abstract

Two-dimensional (2D) semiconductors, consisting of single-sheets of layered transition-metal dichalcogenides (TMD), are attracting enormous interest from both fundamental science and technology. Monolayer molybdenum disulfide (MoS_2), a typical example from this class of materials, is currently under intense research investigation because its direct band gap, atomic-scale thickness and mechanical flexibility could enable a wide range of novel technological applications, such as low-power flexible/transparent electronics, displays and wearable sensors. Critical to all these applications are the material mechanical strength, the mobility of charge carriers in the 2D semiconductor and its interaction with the surrounding environment. This thesis describes experimental research conducted on these critical aspects and shows a proof-of-concept device application based on heterostructures of MoS_2 and graphene. The main goal of the research was to assess experimentally the potential of monolayer MoS_2 for application in flexible electronics.

The thesis is based on three papers. The first paper [1] describes the measurements of the in-plane stiffness and breaking strength of free-standing membranes of monolayer MoS_2. Nanoindentation experiments were performed with the tip of an atomic force microscope (AFM) to extract the material's Young's modulus ($E \sim 270\,\text{GPa}$) and breaking strength ($\sigma_{\max} \sim 23$ GPa). Breaking occurred at maximum internal strain $\varepsilon_{\text{int}} \sim 11\,\%$, which indicates that monolayer MoS_2 is suitable for integration on flexible plastic substrates.

The second paper [2] represents the core work of this thesis. It explores the charge-transport properties of monolayer MoS_2 supported by different dielectric substrates, such as thin polymer films of parylene, atomically flat sapphire and 2D sheets of hexagonal boron nitride (h-BN). It was found that substrate surface corrugations do not represent a major limit to charge-carrier mobility in monolayer MoS_2, which seems at this stage dominated by impurities and material's defects. Field-effect transistors with mobility $\mu \sim 100$ cm^2/Vs and on/off current ratio $I_{\text{on}}/I_{\text{off}} > 10^5$ were successfully integrated on parylene substrates, whose root-mean-square roughness Rq can be more than two times larger than the thickness of the transistor channel itself. Because parylene is also a flexible material, this work showed a viable method for the realization of high-mobility and high-performance flexible devices based on 2D semiconductors.

Finally, the third paper [3] describes a flash-memory cell fabricated using monolayer

MoS_2/graphene heterostructures and dielectric layers of HfO_2 grown by atomic layer deposition (ALD). The architecture of the device resembles that of a floating-gate transistor. Monolayer MoS_2 acts as the transistor channel, graphene electrodes are used to collect and inject the charge carriers, and a piece of multilayer graphene serves as ultrathin charge-trapping layer. In this paper, it was shown that graphene contacts to monolayer MoS_2 result in ohmic-like current-voltage characteristics at room temperature. Moreover, the use of graphene and 2D semiconductors in flash memory technology was indicated as a potential strategy for further scaling of memory cells and for their integration in flexible electronic devices.

Keywords: Two-dimensional (2D) materials, transition metal dichalcogenides, molybdenum disulfide (MoS_2), field-effect transistors, mechanical properties, dielectrics, flash memory.

Papers in this thesis

[1] Simone Bertolazzi, Jacopo Brivio and Andras Kis, *"Stretching and breaking of ultrathin MoS_2"*, ACS Nano **2011** 5 (12), 9703-9709
DOI:10.1021/nn203879f

[2] Simone Bertolazzi, Adrien Allain, Dumitru Dumcenco, Kenji Watanabe, Takashi Taniguchi, Philippe Gillet and Andras Kis, *"High-performance monolayer MoS_2 transistors on thin polymer films"*, submitted, **2015**

[3] Simone Bertolazzi, Daria Krasnozhon and Andras Kis, *"Nonvolatile memory cells based on MoS_2/graphene heterostructures"*, ACS Nano **2013** 7 (4), 3246-3252
DOI:10.1021/nn3059136

Résumé

Les semi-conducteurs bidimensionnels (2D), constitués d'une seule couche de métaux de transition dichalcogène, attirent actuellement un grand intérêt dans la science fondamentale et la technologie. La monocouche de disulfure de molybdène (MoS_2), un exemple typique de cette classe de matériaux, fait actuellement l'objet de recherches intensives, parce que son gap d'energie direct, son épaisseur atomique et sa flexibilité mécanique pourraient permettre une large éventail de nouvelles applications technologiques, comme de l'électronique à basse puissance flexible et transparente, des écrans et des capteurs portables. La résistance mécanique du matériaux, la mobilité des porteurs de charge dans le semiconducteur 2D et son interaction avec le milieu environnant sont des characteristiques importantes pour toutes ces applications. Ce travail de thèse décrit la recherche expérimentale menée sur ces aspects critiques ainsi qu'un dispositif de preuve-de-concept basé sur des hétérostructures de MoS_2 et de graphène. Le principal objectif de la recherche était d'évaluer de manière expérimentale le potentiel de monocouches de MoS_2 afin de les appliquer à l'électronique flexible.

La thèse est basée sur trois articles. Le premier article [1] décrit les mesures de rigidité dans le plan et de résistance à la rupture des membranes à base de monocouche de MoS_2 suspendues. Des expériences de nanoindentation ont été réalisées avec la pointe d'un microscope à force atomique (AFM) pour extraire le module d'Young du matériau ($E \sim 270\,\text{GPa}$) et sa résistance à la rupture ($\sigma_{\text{max}} \sim 23\,\text{GPa}$). La rupture se produit avec une déformation interne maximale $\varepsilon_{\text{int}} \sim 11\,\%$, ce qui indique que le monocouche de MoS_2 est approprié pour l'intégration sur des substrats flexibles en plastique.

Le deuxième article [2] présente le travail central de cette thèse. Il explore les propriétés de transport electronique de monocouches de MoS_2 sur différents substrats diélectriques, tels que le parylène, le saphir (atomiquement plat) et le nitrure de bore hexagonal (h-BN). On a constaté que la rugosité du substrat ne représente pas une limite majeure pour la mobilité des porteurs de charge dans le monocouche de MoS_2. Cette dernière est, semble-t-il, encore dominée par les défauts du matériaux et par les impuretés. Des transistors à effet de champ avec une mobilité $\mu \sim 100\,\text{cm}^2/\text{Vs}$ et un rapport de courants on/off $I_{\text{on}}/I_{\text{off}} > 10^5$ ont été intégrés avec succès sur des substrats de parylène, dont la rugosité quadratique moyenne Rq peut être plus de deux fois plus grand que l'épaisseur du canal du transistor

lui même. En raison du fait que le parylène est également un matériau flexible, ce travail a démontré une méthode viable pour la réalisation de dispositifs flexibles à haute mobilité et haute performance à base de semiconducteurs 2D.
Enfin, le troisième article [3] décrit une cellule de mémoire flash fabriquée en utilisant des hétérostructures à base de monocouches de MoS_2 et de graphène en combinaison avec des couches diélectriques de HfO_2 déposées par atomic layer deposition (ALD). L'architecture du dispositif ressemble à celle d'un transistor à grille flottante. Le monocouche de MoS_2 agit en tant que canal du transistor, des électrodes en graphène sont utilisées pour recueillir et injecter les porteurs de charge, et un morceau de graphène multicouche sert comment electrode flottante ultra-mince pour stocker les charges. Dans cet article, nous avons montré que le graphène peut être utilisé comme matériau de contact pour les monocouches de MoS_2, et il produit des caractéristiques courant-tension de type ohmique à température ambiante. En outre, l'utilisation de graphène et de semi-conducteurs 2D est une stratégie envisageable pour réduire les dimensions des cellules de mémoire et pour les intégrer dans des dispositifs électroniques flexibles.

Mots-clés : Matériaux bidimensionnels (2D), métaux de transition dichalcogène, disulfure de molybdène (MoS_2), transistor à effet de champ, propriétés mécaniques, dielectriques, mémoire flash.

Articles dans cette thèse

[1] Simone Bertolazzi, Jacopo Brivio and Andras Kis, *"Stretching and breaking of ultrathin MoS_2"*, ACS Nano **2011** 5 (12), 9703-9709
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[2] Simone Bertolazzi, Adrien Allain, Dumitru Dumcenco, Kenji Watanabe, Takashi Taniguchi, Philippe Gillet and Andras Kis, *"High-performance monolayer MoS_2 transistors on thin polymer films"*, submitted, **2015**

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1 Introduction

The discovery of graphene [1, 2], a single atomic layer of graphite, is being regarded as a veritable breakthrough in material science, with the potential to revolutionize several existing technologies and enable the creation of new ones. Being only one atom thick, graphene can be considered as a truly two-dimensional (2D) system, where the confinement of electrons in the vertical dimension gives rise to novel extraordinary properties. For instance, graphene not only holds the record for the highest thermal and electrical conductivity, but it is also the strongest material ever measured [3, 4]. The profound novelty of its physical properties was acknowledged with the 2010 Nobel Prize in Physics, jointly awarded to Andre Geim and Konstantin Novoselov.
However, graphene is only one example among a large number of 2D crystals available in nature, and nowadays several researchers worldwide are turning their attention towards a newly emerging class of 2D materials, i.e. the so-called "2D crystals beyond graphene". Among these, monolayers of transition metal dichalcogenides (TMD) – such as MoS_2, WS_2 or WSe_2 – are attracting tremendous interest, as they provide a broad spectrum of electronic and optical properties alternative to those of graphene. For instance, while the latter is a zero-gap semimetal, monolayer MoS_2 is a semiconductor with a direct bandgap of $\sim$ 1.8 eV and therefore is suitable for applications in digital electronic switches and optoelectronic devices.

In the last four years, particular attention has been given to monolayer MoS_2, mainly due to the large availability of molybdenite ores. Several studies have revealed that monolayer MoS_2 is a promising semiconductor for pursuing the miniaturization of field-effect transistors (FET) beyond the limit of silicon technology. In 2011, FETs with optimal switching characteristics – namely high ON/OFF current ratio ($I_{on}/I_{off} \sim 10^8$) and almost ideal subthreshold swing ($SS \sim 74$ meV/dec) – have been demonstrated by Radisavljevic *et al.* [5], who revealed for the first time the strong technological potential of this 2D semiconductor. Due to its atomic-scale thickness (~ 0.6 nm) and sizeable bandgap, monolayer MoS_2 offers ideal electrostatic control in the FET geometry, minimal short-channel effects and low

standby power dissipation [6, 7]. All these interesting characteristics are combined with a high degree of mechanical flexibility [8] and transparency, so that monolayer MoS_2 is also presently being regarded as an ideal candidate for application in flexible electronic devices for wearable and transparent systems.
However, serious challenges remain to be solved before the first consumer products based on 2D MoS_2 can enter the market. One critical aspect consists in the fact that the experimental charge carrier mobility ($40-50\ cm^2/Vs$ at room temperature [9, 10]) is much lower compared to the calculated theoretical limit ($\sim 410\ cm^2/Vs$) set by intrinsic phonon scattering. This indicates that extrinsic sources of disorder are at this stage the major causes of mobility degradation. Among these, one can include defects and impurities in the material, atmospheric adsorbates, and other forms of disorder related to the substrate, such as charge traps, remote polar phonons and surface corrugations. In this complex scenario, new investigations are necessary to shed light on the mechanisms that affect the charge transport in monolayer MoS_2, in the effort to reduce the discrepancy between the theoretical limit and the experimental mobility values.

1.1 Objectives

The first step to be undertaken before considering a specific application for a new material consists in the characterization of its physical properties, which in turn allows evaluating the effective technological potential of the material. For application of MoS_2 in flexible electronics, it is necessary to acquire data about its mechanical and charge-transport properties, and compare them with existing requirements and performance metrics.

i) Mechanical properties. One of the objectives of this doctoral research consists in evaluating experimentally the mechanical properties of monolayer MoS_2, such as the in-plane stiffness and breaking strength, to see if the material fulfills the technological requirements for incorporation into flexible electronic devices. For instance, common plastic substrates, such as polyimide, typically breaks at a strain level of the order of $\sim 7\%$. Hence, the question arises whether 2D MoS_2 can withstand such a level of strain. This research work aims to answer this question by means of nanoindentation experiments performed with the tip of an atomic force microscope (AFM) on free-standing membranes of monolayer MoS_2.

ii) Charge-transport properties. The thesis is especially devoted to the investigation of the charge transport properties of monolayer MoS_2 sheets deposited on different dielectric surfaces. Nowadays, the most common substrate in use for the fabrication of FETs based on 2D materials is SiO_2. However, the oxide surface is known to contain a large amount of charge traps and impurities that degrade the mobility of the overlying 2D sheets. This research work aims at reducing the amount of substrate-related disorder by replacing

the conventional SiO_2 with alternative substrates, among which thin films of parylene, a material that is also suitable for flexible electronic applications.
The overall goal of the work is to optimize the mobility of the charge carriers within the 2D semiconductor and boost the performance of MoS_2-based electronic devices. To achieve this objective, it is necessary to complete two sequential tasks. The first consists in the identification of the most detrimental sources of charge carrier scattering. The second task deals with the development of suitable strategies to minimize the influence of the identified sources. This research is expected to provide useful information on the mechanisms that influence the charge transport properties of monolayer MoS_2 in real device applications.

iii) Proof-of-concept device. After characterizing the physical properties of 2D MoS_2, it is also of high interest to explore how this ultrathin semiconductor could be employed in various technological applications. The final objective of this thesis consists in providing an example of a proof-of-concept device that exploits to advantage the unique characteristics of 2D materials. More specifically, the thesis aims to show that 2D crystals with complementary properties, such as MoS_2 and graphene, can be combined together to build all-2D electronic devices with advanced functionalities.

1.2 Outline of the thesis

This thesis is based on three papers, which are correlated with the three sets of objectives indicated in the previous part of this introduction. The overall organization of the manuscript is reported in the following.

► Chapter 2 provides the reader with a literature review on the physical properties of monolayer MoS_2 and refers to the latest theoretical and experimental investigations conducted in the research field. Moreover, the chapter describes the state-of-the-art techniques for the production of MoS_2 and other 2D TMDs. Finally, it presents the latest advancements in the development of electronic and optoelectronic devices based on these unique materials.

► The measurement of the mechanical properties of free-standing monolayer MoS_2 membranes is included in chapter 3, which contains the original report of the work:

• Simone Bertolazzi, Jacopo Brivio and Andras Kis, *"Stretching and breaking of ultrathin MoS_2"*, ACS Nano **2011** 5 (12), 9703-9709
DOI:10.1021/nn203879f

► A review on the charge transport properties of monolayer MoS_2 is given in chapter 4. The intrinsic and extrinsic limits to the charge carrier mobility are introduced by presenting the results of different computational and experimental studies, which have been reported in the literature of the last four years. Furthermore, the chapter provides a comprehensive

list of extrinsic sources of disorder – both internal and external to the 2D semiconductor – and discusses their influence on the charge transport properties of monolayer MoS_2.

► Chapter 5 represents the main work of this thesis. It deals with the fabrication and characterization of monolayer MoS_2 FETs on a set of dielectric substrates alternative to the common SiO_2, among which hexagonal boron nitride (h-BN), atomically flat sapphire and thin films of parylene. A strong focus has been given to the polymer substrates, mainly due to the envisioned application of monolayer MoS_2 in flexible electronics.
Tuning the properties of the supporting dielectric material is an example of interface engineering for enhancing the performance of MoS_2 FETs. Another possibility for device optimization consists in the minimization of internal defects. The chapter presents as well a defect-engineering approach to reduce the amount of sulfur vacancies, which are the most common type of defects present in MoS_2. The methods and the results of the experimental investigation are reported in the paper:

• Simone Bertolazzi, Adrien Allain, Dumitru Dumcenco, Kenji Watanabe, Takashi Taniguchi, Philippe Gillet and Andras Kis, *"High-performance monolayer MoS_2 transistors on thin polymer films"*, submitted, **2015**

► Chapter 6 presents a proof-of-concept memory device based on heterostructures of MoS_2 and graphene. It shows that the two materials can be advantageously combined together within the floating-gate FET architecture, offering great potential for the vertical and lateral scaling of flash memory devices [11]. The concept, fabrication procedure and advantages of the 2D memory cell are described in the following paper:

• Simone Bertolazzi, Daria Krasnozhon and Andras Kis, *"Non-volatile memory cells based on MoS_2/graphene heterostructures"*, ACS Nano **2013** 7 (4), 3246-3252
DOI:10.1021/nn3059136

► Finally, chapter 7 summarizes the main results of this doctoral research. Moreover, it discusses the challenges that need to be faced in the next years to enable the first consumer products based on monolayer MoS_2 and other 2D materials.

2 Monolayer MoS_2 – physical properties and device applications

2.1 Introduction

Nature offers a large number of layered materials, from which several two-dimensional (2D) crystals can be extracted. The discovery of graphene, a single atomic layer of graphite, stimulated renewed interest in layered compounds, such as transistion metal dichalcogenides (TMDs). Similarly to graphite, also these materials retain their stability when thinned down to monolayers, and give rise to a set of physical properties remarkably different from those of the bulk.

TMDs have the common chemical formula MX_2, where M is a transition metal (e.g. Mo, W, Nb, Ta, Re) and X is a chalcogen element (S, Se and Te). In nature, more than 40 different MX_2 compounds exist, most of which have a layered structure [12, 13]. Layered TMDs present a wide spectrum of electronic properties (table 2.1). For example, monolayer MoS_2 is a semiconductor with a direct bandgap of $\sim 1.8\,eV$, while $NbSe_2$ is a metal and exhibits superconductivity and charge denisity wave (CDW) at low temperature [13].

The large variety of compounds and properties available in the family of layered TMDs stimulated the beginning and the fast development of a new research field, known as "2D crystals beyond graphene". One can think to this class of materials as a complete material library where to find *ad hoc* properties to engineer devices with specific functionalities. Entering this field is made even attractive by the undergoing development of techniques for assembling heterostructures of different 2D crystals [15].

Among all the TMDs, the best known is certainly MoS_2, which is commonly used as dry lubricant in racing car engines and ultrahigh-vacuum technology [16]. In its aspect, bulk molybdenite (figure 2.1c) is similar to graphite (figure 2.1d). In this regard, it is interesting to notice that the ancient Greeks could not distinguish between the two minerals and employed the same word, $\mu o\lambda \upsilon \beta \delta o\varsigma$ (*molybdos*), to refer to all those substances that loose color, among which lead, graphite and MoS_2 [17]. In the mid 18^{th} century molybdenite was still thought to contain lead and to be identical to graphite. The proof of the difference

MX_2	-S_2	-Se_2	-Te_2
Mo	SEMICONDUCTING 1L: 1.8 eV Bulk: 1.2 eV	SEMICONDUCTING 1L: 1.5 eV Bulk: 1.1 eV	SEMICONDUCTING 1L: 1.1 eV Bulk: 1.0 eV
W	SEMICONDUCTING 1L: 1.9 eV Bulk: 1.4 eV	SEMICONDUCTING 1L: 1.7 eV Bulk: 1.2 eV	SEMICONDUCTING 1L: 1.1 eV
Nb	METAL SUPERCONDUCTING CDW	METAL SUPERCONDUCTING CDW	METAL

Table 2.1: Properties of layered TMDs. Electronic characteristics of different layered TMDs, classified as semiconducting, metallic, superconducting or charge density wave (CDW). The values of the energy bandgaps E_g of the semiconducting compounds are reported for the bulk and monolayer (1L) forms. Adapted with permission from ref. [14], © 2012 Nature Publishing Group.

among these substances dates back only to the second half of the 18th century, when the Swedish chemist Carl Wilhelm Scheele discovered the oxide of molybdenum, which was till that time an unknown metal [18].

There are various similarities between MoS_2 and graphite. Both materials are classified as van der Waals solids. These are formed by stacks of atomic planes that weakly interact among each other, whereas the atoms in each plane are held together by strong covalent bonds. The weak van der Waals interaction among the planes is at the origin of the excellent tribological properties of both solids. Figure 2.1a and b show the structure of single-layer sheets of MoS_2 and graphene, respectively. The latter is the thinnest possible material and is made of a single plane of carbon atoms arranged in a hexagonal honeycomb lattice. A monolayer of MoS_2 consists instead of three atomic planes, i.e. a Mo plane sandwiched between two S planes (S-Mo-S) stacked in trigonal prismatic coordination (section 2.2.1). Optical microscopy images of monolayer flakes of MoS_2 and graphene deposited on the surface of oxidized silicon substrates are shown in figure 2.1c and d respectively. It can be seen that in the two-dimensional limit, the similarity in appearance between the two materials is preserved, with few-layers thick graphene flakes being barely distinguishable from monolayer MoS_2.

Despite these common features, the different nature of the C and Mo-S chemistry give rise to dramatic differences in the electronic, optical, mechanical and thermal properties of the two materials. For example, while graphene is a semimetal and lacks a bandgap in its pristine form, monolayer MoS_2 comes naturally with a large semiconducting energy

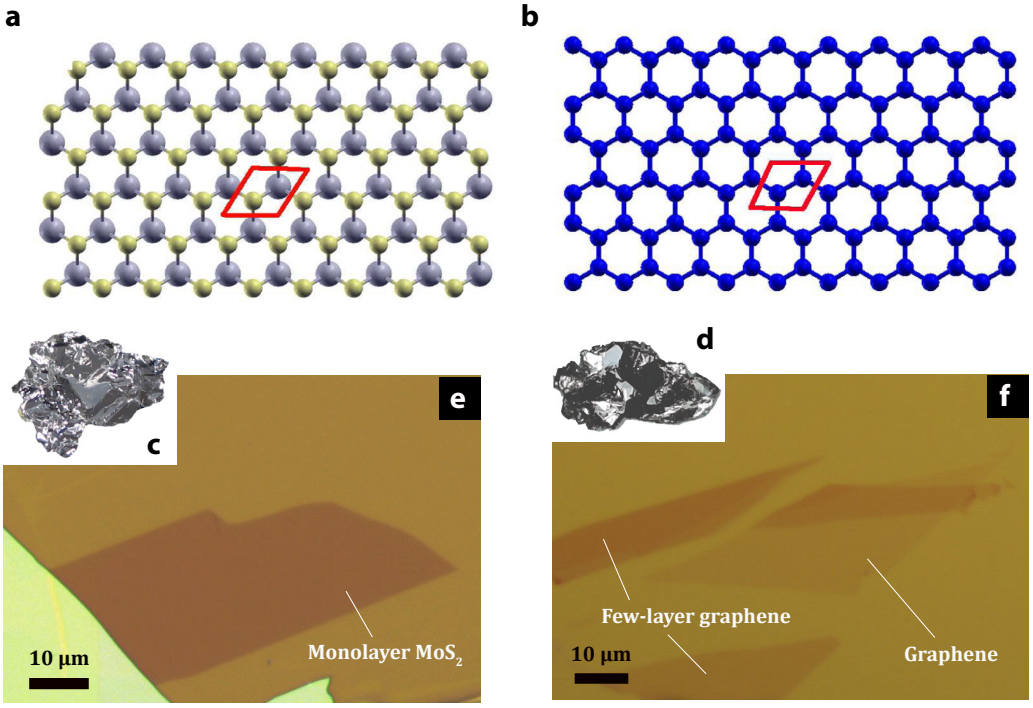

Figure 2.1: Comparison between MoS_2 and graphene's structure and appearance. Ball-and-stick model of the in-plane structure of monolayer MoS_2 (**a**) and graphene (**b**). Red rhombus enclose the unit cells, made by: **a**, 1 Mo (gray) and 2 overlapped S (yellow) atoms; **b**, 2 carbon atoms (blue). Adapted from [20]. **c,d,** Photograph of a piece of bulk molybdenite (**c**) and graphite (**d**) approximately 1 cm long. **e,f,** Optical micrographs of monolayer MoS_2 (**e**) and mono- and few-layer graphene flakes (**f**) mechanically exfoliated on oxidized silicon substrates (270 nm thick SiO_2).

bandgap (1.8 eV [19]) and therefore is suitable for use in digital electronic switches.
The chapter is organized as follows. In section 2.2 the physical properties of monolayer MoS_2 will be reviewed; section 2.3 will describe the methods available today to produce 2D sheets of MoS_2; and finally, section 2.4 will give an overview of the emerging device applications based on the unique properties of this novel 2D semiconductor.

2.2 Physical properties of MoS_2

TMDs have been studied for more than 50 years, mainly because of their excellent lubrication properties that found broad application in the automobile and aerospace industry [16]. Pioneering investigations of the electronic and optical properties of bulk MoS_2 and other TMDs were conducted in the 1960's (e.g.[21, 22]). In the same decade, Frindt *et al.* [23, 24] reported on the exfoliation and characterization of MoS_2 thin flakes with thickness smaller than 10 nm. The first report on single-layer MoS_2 produced by lithium intercalation and

characterized by X-ray diffraction was published in 1986 by Joensen, Frindt and Morrison [25]. The interest in the properties of ultrathin flakes of MoS_2 exploded in 2011, when Radisavljevic *et al.* [5] reported the realization of high-performance single-layer MoS_2 transistors with remarkably high on/off current ratio ($I_{on}/I_{off} \sim 10^8$) and almost ideal sub-threshold swing ($SS \sim 74$ mV/dec), showing the potential of this 2D semiconductor for the fabrication of electronic devices with low stand-by power dissipation [26, 27]. These results, enabled by the unique combination of atomic-scale thickness and energy bandgap, sparked renewed interest in all the physical properties of MoS_2 and stimulated the development of new device concepts aimed to exploit its potential [12, 28].

2.2.1 Crystal structure of MoS_2

The crystal structure of MoS_2 (figure 2.2) was reported in 1923 by Dickinson and Pauling [29], who conducted pioneering X-ray diffraction experiments that revealed the hexagonal lattice and the structural parameters of MoS_2.
Bulk MoS_2 has three different polymorphs, namely 2H, 3R and 1T (figure 2.2a). 2H and 3R consist of stacks of S-Mo-S layers, where each Mo atom is covalently bonded to 6 S atoms with trigonal prismatic coordination (D_{3h}). These polymorphs differ from each other in the stacking of the layers. 2H has two layers per unit cell stacked in hexagonal symmetry, whereas 3R has three layers per unit cell stacked in rhomboedral symmetry. On the other hand, the 1T polymorph is characterized by Mo and S atoms arranged in octahedral coordination (O_h) with only one layer per unit cell (tetragonal symmetry). In the single-layer limit only two different structures exist, with either D_{3h} or O_h coordination. These phases, referred to as 2H (sometimes also 1H [30]) and 1T, are shown in 2.2b and c respectively. It is worth noting that, differently from its bulk counterpart and from graphene, monolayer 2H-MoS_2 has no inversion symmetry. This fact has important implications in the valley physics of the material [31], as we shall see in section 2.2.2.
The most stable polymorph is 2H, which is an intrinsic semiconductor [34]; 3R is rare and tends to transform into 2H upon heating [35], whereas 1T is metastable and has metallic conductivity. The observation of the 1T polymorph was first reported in 1991 by Yang *et al.* [36] for the case of single-layers of MoS_2 produced by lithium intercalation. In the following year, Wypych and Schöllhorn [37] described an electrochemical process to obtain crystals of MoS_2 with 1T structure and metallic conductivity. It was found that the stabilization of the 1T phase is due to an electron donation process that involves the organolithium compound used for intercalation [33].
Transmission electron microscopy (TEM) is a powerful tool for studying the structural properties of ultrathin materials. Brivio *et al.* [38] performed TEM studies of mono- and few-layer thick MoS_2 membranes produced by mechanical exfoliation. They confirmed the existence of a stable 2H configuration also in the 2D limit and observed ripples up to

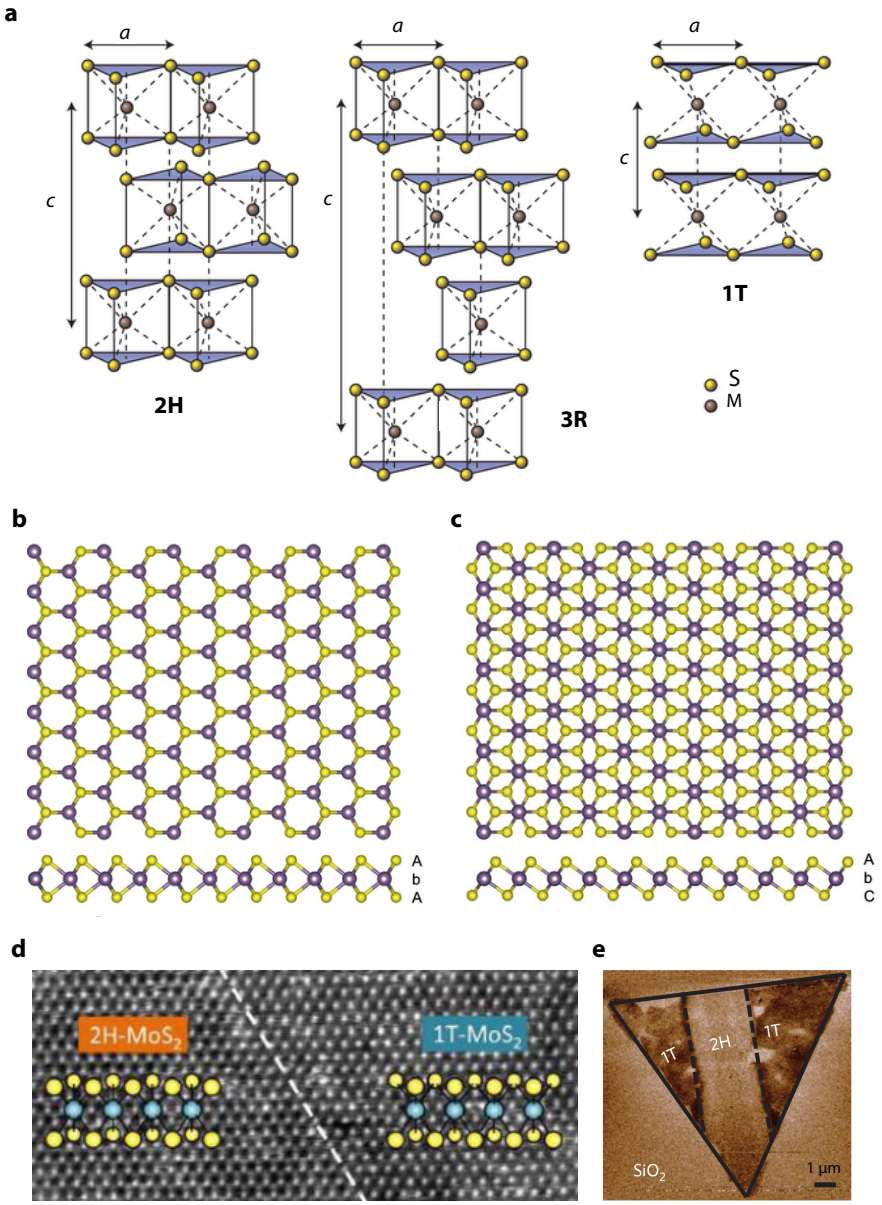

Figure 2.2: Crystal structure and polymorphs of MoS_2. a, Schematic representation of different MoS_2 polymorphs: 2H (two layers per repeat unit, hexagonal symmetry), 3R (three layers per repeat unit, rhombohedral symmetry) and 1T (one layer per repeat unit, tetragonal symmetry). The 2H and 3R polymorphs share the same trigonal prismatic coordination (D_{3h}); the 1T polymorph has octahedral (O_h) coordination. The lattice constant is $a = 3.16\,\text{Å}$ and the vertical separation between the molybdenum layers is $\sim 6.15\,\text{Å}$. Adapted with permission from ref. [14], © 2012 Nature Publishing Group. **b,c,** Section-view along the c-axis of monolayer MoS_2 with trigonal prismatic (**b**) and octahedral (**c**) coordination. Adapted with permission from ref. [13], © 2013 Nature Publishing Group. **d,** Scanning TEM image of monolayer MoS_2 with both 2H and 1T phases; the boundary between them is marked with a white dashed line. Adapted with permission from ref. [32], © 2012 American Chemical Society. **e,** Triangular sheet of monolayer MoS_2 imaged with electrostatic force microscopy, showing locally patterned 1T and 2H regions. Adapted with permission from ref. [33], © 2013 Nature Publishing Group.

1 nm in height, which are responsible for the thermodynamic stability of free-standing atomic sheets. Moreover, in the case of monolayers, they observed distinctive features in the diffraction pattern due to inversion symmetry breaking. TEM investigations (figure 2.2d) conducted by Eda *et al.* [32] revealed that the 2H and 1T phases can coexist in monolayers obtained through chemical exfoliation (see section 2.3). Recent reports have also shown the intriguing possibility to locally control the structure of the material by inducing phase transformations, e.g. by means of n-butyllithium exposure [33] or electron beam irradiation [39]. Figure 2.2e gives an example of phase patterning performed by Kappera *et al.* [33] on a monolayer MoS_2 flake deposited on a SiO_2 substrate. The 1T metallic regions were found to be characterized by a much higher charge-carrier density ($\sim 10^{13}$ cm^{-2}) compared to the 2H semiconducting regions. The ability to control the structure and thus the conductivity of the material on the nanoscale, could enable the realization of electronic devices with 1T contacts and 2H semiconducting channel.
In the next of this chapter we will focus on the 2H polymorph, which is the most common polytype and has made the object of the whole experimental investigation conducted during this doctoral work.

2.2.2 Electronic properties

Pioneering first-principles calculations of the electronic band structure of MoS_2 were carried out in the early 1970's by Bromley [40], Edmonson [41] and Mattheiss [34, 42]. These calculations could explain the main features of the optical spectra [23, 43, 44] and the results of the photoemission experiments reported by Williams and McEvoy (1971 [45]) and by Mecmenamin and Spicer (1972 [46]).
MoS_2 was found to be an indirect bandgap semiconductor ($E_g \sim 1.2$ eV [47]), where the valence band (VB) maximum lies at the high-symmetry point Γ and the conduction band (CB) minimum at a low-symmetry point between K and Γ. As a reference, figure 2.3a shows the first Brillouin zone of 2H-MoS_2, where the high-symmetry points (full circles) and the directions (green lines) used for plotting the band structures are indicated. Recent calculations [48, 49] revealed that the electronic band structure of ultrathin MoS_2 sheets depends dramatically on the number of layers, due to the onset of quantum confinement effects [50]. As the thickness is reduced from bulk to monolayer (figure 2.3b), the indirect gap increases monotonically, but the direct gap at the K point remains almost unaffected. In the single-layer limit, the indirect gap becomes larger than the direct gap and both the CB minimum and VB maximum shift to the K point. This implies that monolayer MoS_2 is at all effects a direct bandgap semiconductor. Photoluminescence studies conducted first by Splendiani *et al.* [49] and subsequently by Mak *et al.* [19] proved the occurrence of an indirect-to-direct bandgap transition, which manifests itself in a much stronger photoemission in monolayers than in thicker layers.

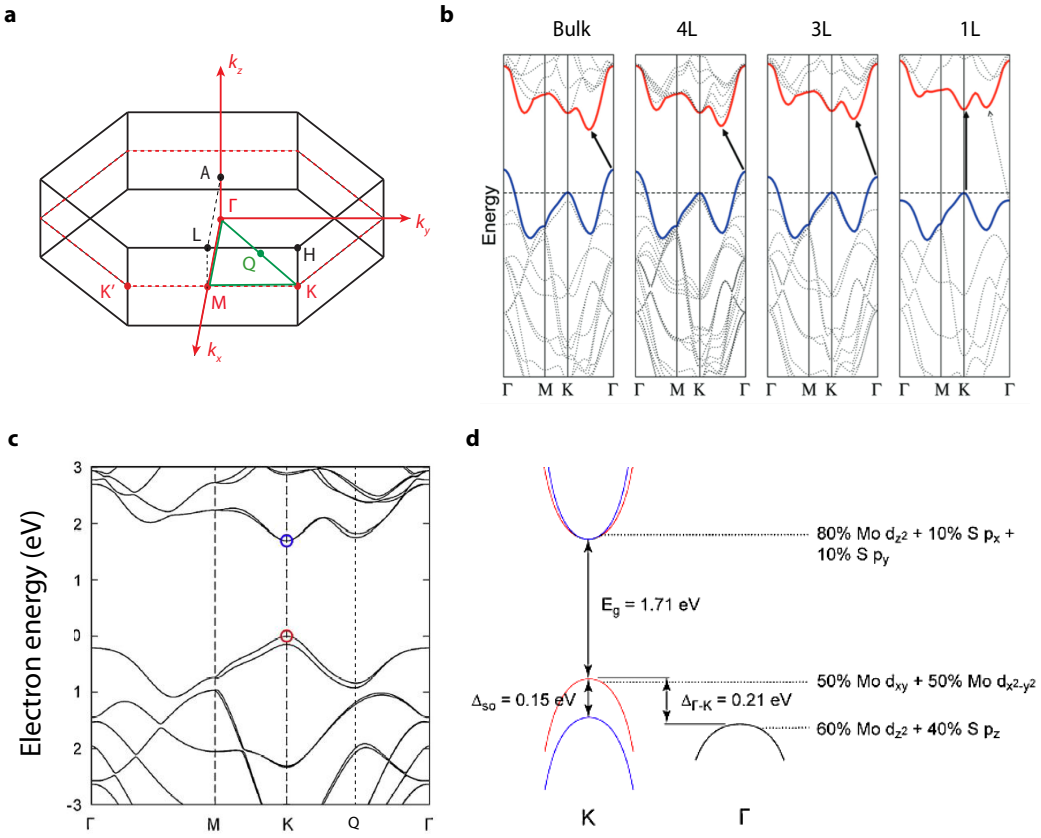

Figure 2.3: Electronic band structure of MoS_2. a, Brillouin zone of MoS_2 with indication of the high-symmetry points. Q represents the midpoint of the $\overline{\Gamma K}$ line. **b,** Evolution of the band structure of MoS_2 with decreasing thickness. From left to right: bulk crystal, four-layer (4L), bilayer (2L) and monolayer (1L). Blue: highest VB; red: lowest CB. **c,** Calculated electronic band-structure of monolayer MoS_2 along the directions marked by the green lines in **a**. The CB minimum and the VB maximum (set to 0 eV) are indicated by a blue and red circle respectively. **d,** Schematic drawing of the VB and CB near their respective maxima and minima. The spin-orbit splitting Δ_{so}, the $\Gamma - K$ valley band offset $\Delta_{\Gamma-K}$ and the orbital compositions are indicated in the graph. **b** is adapted with permission from ref. [49], © 2010 American Chemical Society. **c** and **d** are reproduced from ref. [51], © 2015 Elsevier.

Reasons for these changes in the electronic structure upon reducing the number of layers can be ascribed to the varying orbital compositions of the electronic states [51]. A simple ligand field model of the electronic structure of MoS_2 is presented in the review by Enyashin and Seifert [52]. Each Mo atom has 6 valence electrons ($5s4d$ shells) and is covalently bonded to 6 S atoms. The chemical bonds are made through Mo$4d$-S$3p$ hybridized orbitals. The electronic states corresponding to the highest VB and lowest CB consist prevalently of Mo$4d$ orbitals. This simple model is not able to predict the evolution of the band structure with changing number of layer, as it assumes that the $3p$ shells of the S atoms are "saturated" and that the Mo$4d$ orbitals do not range out the S-Mo-S layer. More detailed

analysis [53] showed that the electronic states of the highest VB and lowest CB at the K point are composed nearly exclusively by localized d orbitals (e.g. d_{xy} and $d_{x^2-y^2}$) confined within the S-Mo-S layer. These orbitals are insensitive to the number of layers, which explains why the direct gap at the K point does not depend on the thickness of the material. On the other hand, the electronic states of the highest-VB at the Γ point have anti-bonding nature and consist of combinations of Mo d_z^2 and S p_z orbitals. The energy of these states diminishes with decreasing interlayer interaction, which gives reason for the increase in the indirect bandgap upon reduction of the number of layers [52]. A detailed study of the thickness-dependent orbital composition of the band-edge states was recently conducted by Padilha *et al.* [54] through first-principles calculations.
The outlined evolution of the electronic band-structure with thickness has been confirmed experimentally by Jin *et al.* [55] *via* angle-resolved photoemission spectroscopy (ARPES) measurements. They could observe and quantify another striking feature, i.e. the strong increase in the hole effective mass m^* at the Γ point going from bulk ($m^* \sim 0.67m_0$) to monolayers ($m^* \sim 2.4m_0$). Since the hole mass at the K point barely changes with thickness, the overall hole effective mass turns to be dramatically larger in monolayer compared to bulk, leading to the expectation of a much lower hole mobility.

Band structure calculations. The band structure of monolayer MoS_2, as obtained by density functional theory (DFT) calculations, is shown in figure 2.3c and d. The resulting orbital mixing for the CB and VB electronic states close to the K and Γ points is reported in figure 2.3c. The calculated energy gap is ($E_g = 1.71$ eV) and the VB maximum at the K point is shifted with respect to the maximum at Γ by $\Delta_{\Gamma-K} = 0.21$ eV. While the CB maintains its spin degeneracy at the K point, spin-orbit interaction is responsible for splitting the VB into two sub-bands [56] separated in energy by $\Delta_{so} = 0.15$ eV. The values of the energy gap and spin splitting obtained from experiments are $E_g = 1.9$ eV [19, 49] and $\Delta_{so} = 154$ meV [57] respectively. It should be mentioned that all the theoretical values reported above can be subjected to significant deviations depending on the specific methods and approximations used for calculations. In particular, DFT calculations are known to underestimate the value of the energy gap, due to unreliable exited states. The interested reader is referred to [58] or [59] for a summary of the different techniques with their corresponding results. One further remarkable feature of the band structure in figure 2.3c is the proximity in energy between the CB valleys at the K and Q points of the Brillouin zone. Calculations by Li *et al.* [60] indicate that the energy difference between these two valleys can be as low as $\Delta_{K-Q} = 70$ meV, in which case intervalley scattering processes can significantly influence the transport properties of the material (see section 4.3). Furthermore, the effective mass of electrons in the Q valleys ($m^*_{Q,l} = 0.62m_0$ and $m^*_{Q,t} = 1.0m_0$ in the longitudinal ($\Gamma - K$) and transverse direction, respectively) was found to be larger than in the K valleys ($m^*_{K,l} = m^*_{K,t} = 0.5m_0$).

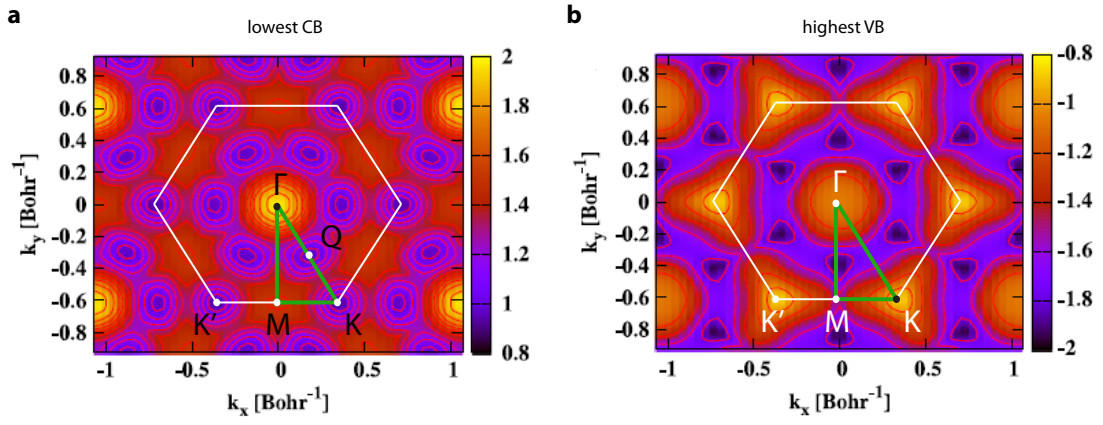

Figure 2.4: Topology of VB and CB in monolayer MoS_2. **a**,**b**, Energy maps showing the topology of the lowest CB (**a**) and highest VB (**b**) as obtained from first-principles calculations. As a reference, the high-simmetry points and directions indicated in figure 2.3a are reported. Colorbar unit: eV. Adapted with permission from ref. [61], © 2012 Elsevier.

Topology of VB and CB. In order to provide the reader with a complete picture the lowest CB and highest VB of monolayer MoS_2, the topology of the two bands is illustrated in figure 2.4 that shows the reciprocal-space energy maps calculated by Kadantsev and Hawrylak [61]. The global CB minima and VB maxima are located at each of the six corners (K and K' points) of the first Brillouin zone. The VB has an additional local maximum at the Γ point, while its global minima are attained along the line connecting the Γ and M points. On the other hand, the conduction band has additional minima at the Q point, whereas its global maximum lies at the Γ point.

Valley and spin polarization. Low-energy carriers lying at each CB/VB valley possess an additional degree of freedom, i.e. the valley index, which stems from the nonequivalence of the valleys located at the K and K' points of the hexagonal Brillouin zone. The capability to control the valley index of the carriers, or equivalently their valley polarization, can lead to the emergence of a novel technology platform, referred to as valleytronics, where the information is stored in the crystal momentum of the carriers rather than in their electrical charge. In both graphene and monolayer MoS_2, the large distance in reciprocal space among the valleys promotes the realization of stable valley-polarization states [62]. However, two additional features can be found in monolayer MoS_2 but not in graphene, namely: (i) the lack of inversion symmetry (section 2.2.1) and (ii) the large spin-orbit-induced spin-splitting [65]. The first feature leads to the valley Hall effect (figure 2.5a), where carriers in different valleys move towards opposite edges of a sample in response to an in-plane electric field; moreover, it sets valley-dependent selection rules for interband transitions (figure 2.5b), so that valley polarization can be easily achieved through optical pumping by circularly polarized light and detected using circularly-polarized PL spectroscopy [64, 66].

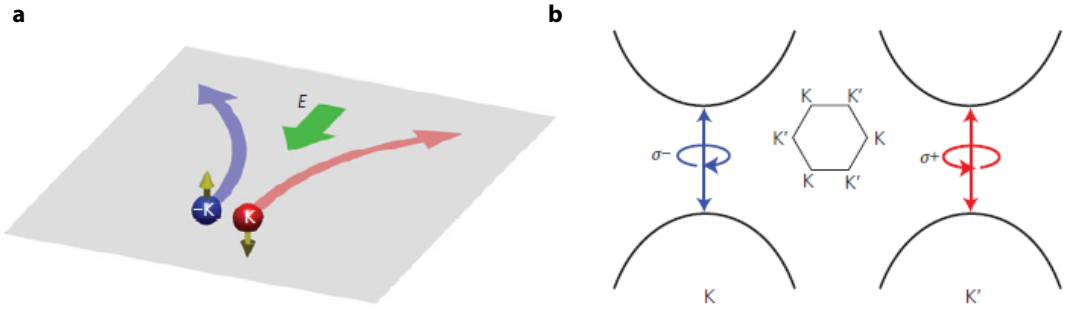

Figure 2.5: Valley physics in monolayer MoS_2. **a,** Schematic representation of the valley Hall effect, where carriers in inequivalent valleys accumulate at opposite edges of the sample, moving perpendicularly to an externally applied electric field E. **b,** Selection rules for interband transitions in monolayer MoS_2: carriers at the K (K') points of the highest VB are photoexcited to the lowest CB only by circularly polarized σ^- (σ^+) light. **a** is reproduced with permission from ref. [63], © 2014 Nature Publishing Group. **b** is reproduced with permission from ref. [64], © 2012 Nature Publishing Group.

On the other hand, the large VB spin splitting at the K and K' points, enables the possibility to generate spin-polarized carriers, as shown in figure 2.6b, thus paving the way towards novel studies and applications in the field of spintronics.
One of the most interesting aspects of the physics of monolayer MoS_2 is the fact that valley and spin degrees of freedom are intrinsically coupled to each other. Xiao et *al.* [62] discuss three major implications of the valley-spin coupling. First of all, the coexistence of spin and valley Hall effects, which is schematically represented in figure 2.6a for the case of a moderately hole-doped system. Since the two split VBs have contrasting spin moments at the inequivalent K and K' points, holes with different combinations of valley and spin indexes can accumulate at the two opposite edges of a sample. Second, due to the requirement of total momentum conservation, the flipping of each spin and valley index alone is forbidden, so that both spin- and valley-polarized carriers can be generated with relatively long relaxation times [59]. Finally, the third implication consists in the possibility to excite carriers with different combinations of spin and valley indexes, by means of polarized light with varying frequencies and circular polarizations, as illustrated in figure 2.6b.

All these aspects are sparking a growing interest in monolayer MoS_2 as an excellent platform to explore new phenomena related to the internal degrees of freedom of carriers [67]. At the origin of the rich and fascinating physics outlined above there is a unique electronic band-structure, whose most peculiar characteristics originate from the non-centrosymmetric lattice of monolayer MoS_2 combined with the special character of its d-electrons. We refer the reader to section 4.3 for a description of the intrinsic charge transport properties, which are a direct consequence of the electronic band-structure presented in this section and of the lattice dynamics (section 2.8).

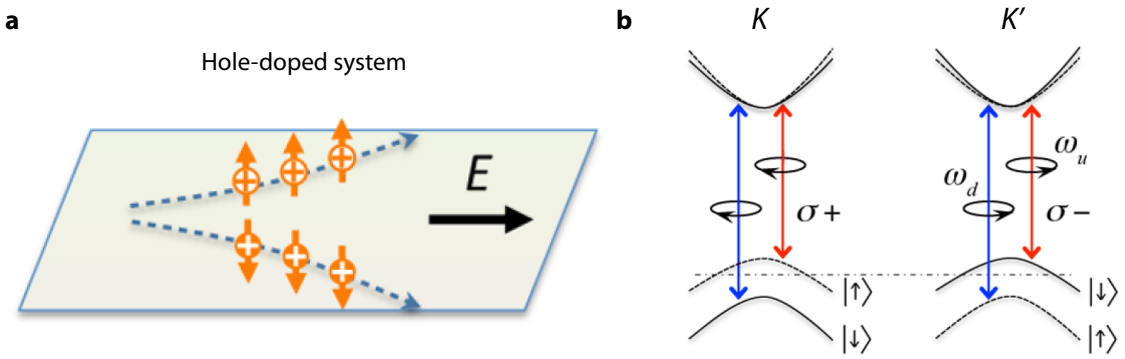

Figure 2.6: Coupled spin and valley physics in monolayer MoS_2. a, Schematic representation of the valley and spin Hall effects for a hole-doped system. Holes (+) in the K (K') valley are denoted by full (empty) circles. The Fermi level (dashed line in **b**) lies between the two split VBs. **b,** Optical selection rules involving both valley and spin degrees of freedom. The transition frequencies from the tops of the two split VBs to the bottom of the CB are denoted as ω_d and ω_u. The symbols $|\uparrow\rangle$ and $|\downarrow\rangle$ are used to indicate the spin-up or spin-down in the two split VBs; σ^+ and σ^- denote the polarization of the incident light. **a** and **b** are adapted with permission from ref. [62], © 2012 American Physical Society.

2.2.3 Optical properties

The optical properties of bulk MoS_2 have been investigated experimentally back in the 1960's [22, 23, 43, 68] using different optical measurement techniques, such as photoemission, reflectivity, photoconductivity (PC) and absorption spectroscopy. First-principles calculations performed by Coehoorn *et al.* [69, 70] in the 1980's provided a coherent explanation for the presence of two distinctive peaks in the absorption spectra, namely the A (1.88 eV) and B (2.06 eV) peaks. Their origin was related to direct interband transitions occurring at the K point of the first Brillouin zone, between the two split VBs and the two-times degenerate CB. These transitions are indicated in the simplified band structure of figure 2.7a. In the last decade, after the discovery of graphene and 2D materials, the interest of researchers shifted from bulk structures to atomically thin layers. The evolution of the optical properties of MoS_2 with decreasing thickness from bulk to monolayer was reported for the first time in 2010 by Splendiani *et al.* [49] and by Mak *et al.* [19]. Figure 2.7b shows the thickness-dependent photoluminescence (PL) spectra of MoS_2, which reflect the evolution of the electronic band structure discussed in section 2.2.2. For bulk MoS_2, the PL signal is negligible, whereas thinner MoS_2 nanocrystals have relatively higher PL emission. The strongest PL emission is attained in the mononolayer limit, since the material changes from an indirect- to a direct-bandgap semiconductor. In fact, the direct electronic transitions allowed in monolayer MoS_2 are characterized by a much higher radiative recombination rate compared to indirect transitions occurring in bulk and few-layer MoS_2. The two peaks visible in the PL spectra correspond to the direct exciton transitions

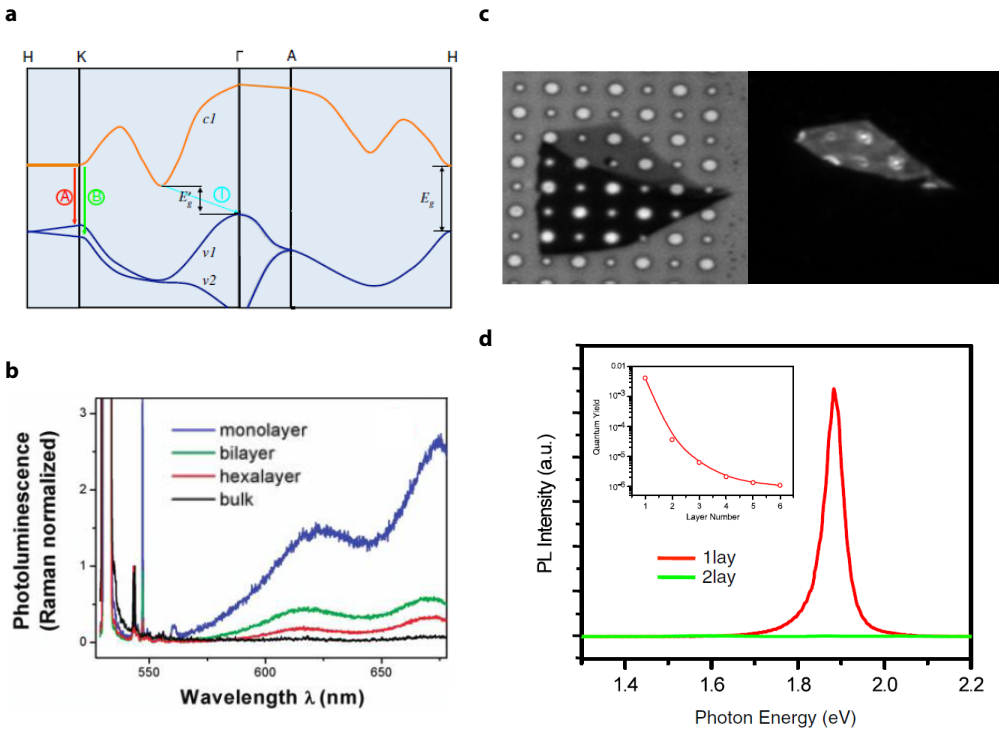

Figure 2.7: Optical properties of MoS_2. **a,** Simplified band structure of bulk MoS_2, showing the lowest CB $c1$ and the highest split VBs $v1$ and $v2$. A and B are the direct-gap transitions, and I is the indirect-gap transition. $E_g^{'}$ is the indirect gap for the bulk, and E_g is the direct gap for the monolayer. **b,** Layer dependence of PL in MoS_2 for monolayer, bilayer, hexalayer and bulk samples. **c,** Left: optical image of a mono- and few-layer MoS_2 crystals on a silicon substrate with etched holes of 1 and 1.5 μm. Right: PL image of the same samples. **d,** PL spectra for mono- and bilayer MoS_2 samples in the photon energy range from 1.3 to 2.2 eV. Inset: PL QY of thin layers for $N = 1$–6. **a**, **c** and **d** are adapted with permission from ref. [19], © 2010 American Physical Society. **b** is adapted with permission from ref. [49], © 2010 American Chemical Society.

A (~ 670 nm) and B (~ 627 nm), whose energy shift ΔE_{AB} (~ 127 meV) can be correlated with the spin-orbit-induced splitting Δ_{so} of the VB at the K point.

Mak *et al.* [19] measured the optical properties of ultrathin free-standing membranes of MoS_2 in order to avoid possible quenching effects induced by the supporting substrate. Figure 2.7c shows the optical micrograph (left) and the corresponding PL image (right) of a mono- and few-layer thick MoS_2 specimen deposited on a silicon substrate with etched holes. The PL emission is much stronger from the suspended regions, whereas it is negligible from the few-layer thick areas of the sample. It is worth to mention at this point that PL emission from ultrathin TMDs can be severely influenced by a number of factors, among which the underlying substrate [71], the adsorption of molecular species from the environment (e.g. O_2 and H_2O) [72], the bonding of oxygen to intrinsic material's defects (e.g. sulfur vacancies) [73], the crystalline phase [74] and also by the doping in

the material [75]. Therefore, for a correct interpretation and comparison of PL data it is essential to evaluate and control the experimental conditions in which the measurements are performed.
The intensity and quantum yield (QY) of the PL signal emitted from the free-standing MoS_2 membranes is reported in figure 2.7d. It can be seen that the photoemission in monolayer is dramatically higher than in bilayer, as a result of the indirect-to-direct bandgap crossover. The inset shows the measured PL QY as a function of number of layers: with increasing thickness from mono- to bilayer, the QY decreases approximately by two orders of magnitude, i.e. from $\sim 4 \times 10^{-3}$ to $\sim 3 \times 10^{-5}$. In the case of a six-layer thick nanosheet the QY further diminishes to $\sim 1 \times 10^{-6}$.
The energies of the direct exciton transitions A and B of bulk MoS_2 could be extracted from absorption measurements. They were found to be only slightly red-shifted compared to those of mono- and few-layer MoS_2, since the direct gap at the *K* point of the Brillouin zone does not depend significantly on thickness (section 2.2.2). In the case of monolayer MoS_2, both PL and adsorption spectra showed a characteristic A peak with the same energy-width and position. This peak was ascribed to the semiconductor direct bandgap with energy value of $\sim$ 1.9 eV [71].
Recent quasiparticle band-structure calculations by Cheiwchanchamnangij *et al.* [58, 76] revealed that the experimental optical bandgap could be much lower than the quasiparticle bandgap relevant for charge transport. This is due to the large exciton binding energy of monolayer MoS_2, which can be as high as $\sim$ 0.9 eV [76]. The quasiparticle bandgap is estimated to be between 2.7 and 2.9 eV, that is significantly larger than the energies of the direct optical transitions.

The presence of valleys and VB spin-splitting in the electronic structure of monolayer MoS_2 and other 2D TMDs, gives rise to a series of novel opportunities in optoelectronics. For instance, as a consequence of valley polarizations, these materials can emit light with selective dichroism[66] and could therefore serve as switchable chiral-light sources [77]. Finally, the rich physics of 2D materials beyond graphene opens up new routes for fundamental studies in different areas, such as exitonics [78, 79] and many-body interactions, whose most prominent example is the discovery of trions [80].

2.2.4 Lattice dynamics

The first experimental investigations of lattice dynamics in MoS_2 date back to 1971, when Wieting and Verble [81] reported infrared and Raman measurements of long-wavelength optical phonons in bulk molybdenite crystals. Few years later, Wakabayashi *et al.* [82] measured the acoustic- and optical-phonon dispersion relationships by means of inelastic neutron scattering (INS). Figure 2.8a shows the calculated phononic band-structure of

bulk MoS_2 [83] as well as the results (circles) of the INS experiments. Having six atoms per unit cell, the 2H polymorph of bulk MoS_2 presents a total of 18 phonon branches, 3 of which are acoustic and 15 are optical [84]. The longitudinal and transverse acoustic phonon branches depend linearly on wavenumber q near the Γ point of the Brillouin zone, whereas the zone-edge acoustic (ZA) branch shows a quadratic $\sim q^2$ behavior. Three distinct optical branches are found in the low-frequency range $35-60\,\mathrm{cm}^{-1}$ that merge with the acoustic branches for large values of q. The remaining 12 optical phonons are separated from the low-frequency modes by a gap of $\sim 220\,\mathrm{cm}^{-1}$. Raman spectroscopy studies [81, 85] identified a total of four Raman-active modes. Among these, the most investigated are E^1_{2g} and A_{1g} that correspond to in-plane and out-of-plane polar vibrations, respectively.

Monolayer MoS_2 has only 3 atoms per unit cell, thus the number of phonon modes reduces to 9, where 3 branches are acoustic and 6 are optical. The frequency-wavenumber dispersion of these modes, as obtained from DFT calculations, is shown in figure 2.8b. All the phonon modes of the monolayer have their corresponding modes in the bulk, where they are split into two branches due interlayer interactions. The most remarkable difference between monolayer and bulk is the absence of low-frequency optical phonons in the former case. It is worth to mention that the broken inversion symmetry in 1H-MoS_2 requires the use of a different notation, so that the Raman-active modes in the monolayer are usually referred to as E' and A'_1 [86].

Figure 2.8c illustrates the motion (eigenvectors) of the 9 normal modes of vibration of monolayer MoS_2 close to the Γ point of the first Brillouin zone. The zone-edge acoustic (ZA) is an out-of-plane flexural mode characterized by a quadratic frequency-wavenumber dispersion, as its analogous in the bulk. The transverse acoustic (TA) and longitudinal acoustic (LA) branches are instead in-plane translational modes with group velocities along the $\Gamma - M$ direction equal to $\sim 690\,\mathrm{m/s}$ and $\sim 1110\,\mathrm{m/s}$ respectively (ref. [88]). These values are significantly smaller than the corresponding ones in graphene, i.e. $\sim 3740\,\mathrm{m/s}$ (TA) and $\sim 5950\,\mathrm{m/s}$ (LA). The first two pairs of optical phonon branches correspond to intralayer shearing modes. In the first pair, the two S planes move whereas the Mo plane is stationary, giving rise to a non-polar lattice vibration (E''). In the second pair, both S and Mo planes move in counterphase resulting in a polar vibration (E'). The almost dispersionless branch at $\sim 396\,\mathrm{cm}^{-1}$ is a homopolar intralayer breathing mode (A'_1) where the S planes vibrate in counterphase along the direction perpendicular to the layer, whereas the Mo plane is fixed. This is equivalent to a change of the thickness of the S-Mo-S layer and it is known to give rise to a large deformation potential detrimental for charge transport [89]. Finally, the optical phonon branch at the highest frequency (A''_2) is another intralayer breathing mode, where both Mo and S planes participate in the vibration.

The bulk modes E^1_{2g} and A_{1g} are expected to have higher frequencies than the corresponding modes in mono- or few-layer thick specimens of MoS_2 owing to the presence of a

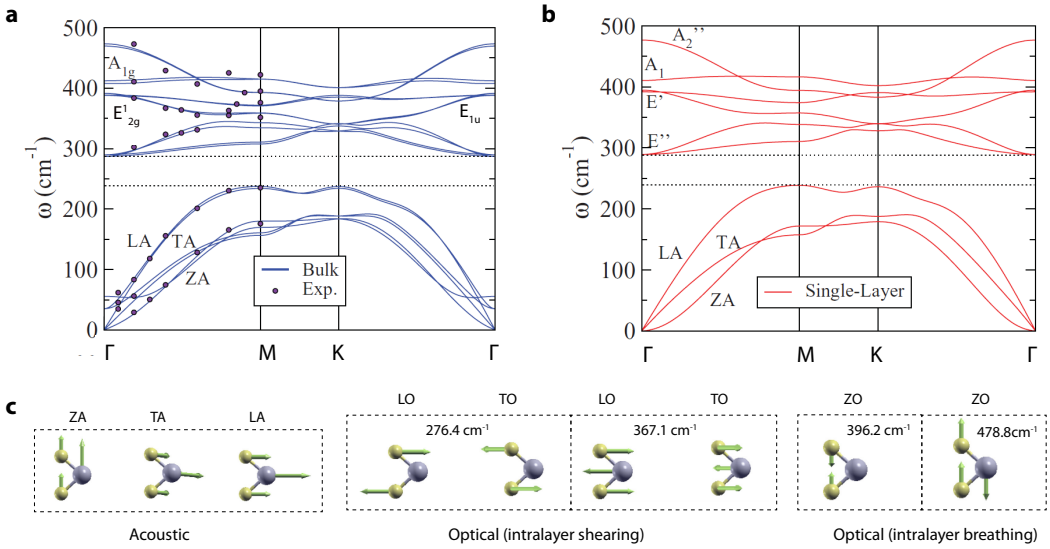

Figure 2.8: Lattice dynamics and phonon dispersion in MoS_2. **a,b,** Phononic band-structure of bulk (**a**) and monolayer (**b**) MoS_2 obtained from DFT calculations. The experimental points in **a** (circles) are extracted from ref. [82]. **a** and **b** are adapted with permission from ref. [**?**], © 2011 American Physical Society. The main Raman-active modes in the monolayer (bulk) are E' (E^1_{2g}) and A'_1 (A_{1g}). **c,** Schematic representation of the 9 phonon modes of monolayer MoS_2. Three of them are acoustic (A) and six are optical (O). In-plane vibrations can be either longitudinal (L) or transverse (T). Out-of-plane modes are denoted with Z. Adapted with permission from ref. [87], © 2013 AIP Publishing LLC.

higher interlayer interactions. However, while the frequency of A_{1g} is coherently higher than that of A'_1, an unexpected behavior is observed in the case of the E^1_{2g} and E' modes. This anomalous phenomenon was first reported by Lee *et al.* [90], who investigated the evolution of the Raman spectra of MoS_2 upon reduction of the number of layers (figure 2.9). They found that, as expected, the A_{1g} undergoes a red shift as the thickness is reduced from bulk to monolayer, whereas the E^1_{2g} mode blue shifts. Therefore, other factors beyond the interlayer van der Waals interaction need to be considered in order to explain the experimental observation. Lee *et al.* [90] proposed long-range Coulomb interactions as possible explanation. *Ab initio* calculations performed by Molina-Sánchez and Wirtz [83] revealed that upon thickness scaling, the dielectric screening of the material changes, together with the intensity of the long-range Coulomb interactions. The effective constant forces of each individual mode are therefore determined by a more complex interplay between interlayer van der Waals interactions and screened Coulomb interactions.

The most important result emerging from Raman studies is the finding that the difference $\Delta\omega$ between the frequencies of the E^1_{2g} and A_{1g} modes can be used as a reliable feature to determine the number of layers in a thin MoS_2 nanosheet. Instead, the intensity and the width of the peaks do not depend monotonically on the number of layers [91]. It is worth to mention that several factors have been reported in the literature to affect these features,

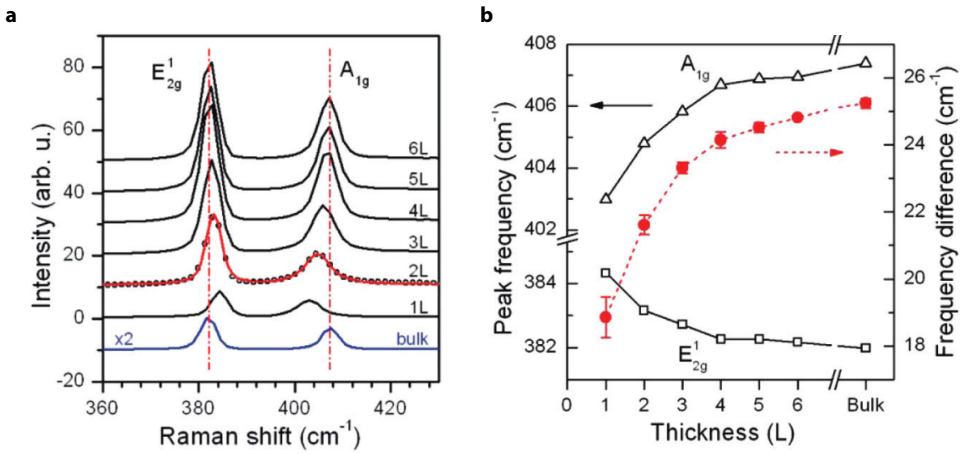

Figure 2.9: Thickness-dependent Raman spectra of MoS_2. a, Raman spectra of thin (nL) and bulk MoS_2 films. **b,** Frequencies of E^1_{2g} and A_{1g} Raman modes (left vertical axis) and their difference (right vertical axis) as a function of layer thickness. Adapted with permission from ref. [90], © 2010 American Chemical Society.

among which thermal [92] and doping [93] influences, as well as strain [94] and the dielectric environment [95]. Figure 2.9b shows the dependence on thickness of the frequencies of the two Raman modes, as well as their difference $\Delta\omega$. In the case of monolayer, $\Delta\omega$ is usually smaller than 20 cm^{-1} with a slight sample-to-sample variation due to the effects mentioned above; more importantly, the shift recorded from mono- to bilayer is as large as 3 cm^{-1}. Hence, Raman spectroscopy can be used as a reliable, fast and non destructive approach to discriminate among monolayers and few-layer thick nanosheets of MoS_2.

2.2.5 Thermal conductivity

The phenomenon of electrical transport through a resistive material can be described by the well-known Ohm's law

$$\vec{j} = -\sigma \cdot \nabla V \tag{2.1}$$

where $\vec{j}$ is the local current density, σ is the electrical conductivity and ∇V is the gradient of the electric potential. At the same way, the transport of heat through a thermally-resistive material can be described by Fourier's law

$$\vec{j}_q = -\kappa \cdot \nabla T \tag{2.2}$$

that relates the heat flux density $\vec{j}_q$ to the temperature gradient ∇T. The link is made *via* the physical quantity κ, i.e the thermal conductivity, which will be discussed throughout this section.

The thermal conductivity (TC) is a crucial material's property that can influence in large extent the efficiency of electronic devices. A high TC is necessary for a fast dissipation of the heat produced in nanoscale devices, where undesired overheating effects should be necessarily avoided.
The discovery of graphene in 2004 boosted the amount of research efforts undertaken in the field of 2D materials for application in electronics. Nevertheless, a relatively low number of papers was published concerning the TC of these materials. In 2008, Balandin *et al.* [96] reported the first experimental measurement of graphene's TC *via* temperature-dependent Raman spectroscopy. They found that suspended graphene sheets hold the record for the highest TC, ranging between 4840 and 5300 W/mK, which proves that graphene is indeed superb material and largely satisfies the needs for several envisioned applications.
The first reports on the TC of MoS_2 appeared only in the last two years. Different thermal properties, such as heat capacity (1956 [97]) and thermal expansion coefficients (1979 [98]), had already been thoroughly investigated in bulk crystals of MoS_2. However, until recently, the experimental TC data were still missing. Sahoo *et al.* [99] were the first to report on the TC of few-layer thick MoS_2 sheets, providing an in-plane value of $\sim$ 52 W/mK at room temperature (RT). Muratore *et al.* [100] evaluated the TC-anisotropy by measuring the TC along the c-axis of a bulk crystal ($\sim$ 3 W/mK). Moreover, in thin films (50 – 150 nm) of MoS_2, they observed a TC increase from 0.25 to 1.5 W/mK for directions perpendicular and parallel to the basal plane, respectively. Jo *et al.* [101] measured the temperature dependence of the in-plane TC of exfoliated MoS_2 samples (4-7 layers thick) using suspended micro-devices with integrated resistance thermometers. The highest TC ($\sim$ 70 W/mK) was observed at a temperature T = 120 K, above which the TC was found to decrease monotonically down to 44−52 W/mK at RT, likely due to intrinsic phonon-phonon scattering and surface disorder. It is worth noting that in the case of a semiconductor with sizeable bandgap, such as MoS_2, the contribution of electrons to the intrinsic TC is very limited compared to that of phonons; thus, the experimental investigations are focused on the phonon-related thermal properties.

Thermal conductivity measurements by Raman spectroscopy. The first Raman measurement of the TC of monolayer MoS_2 was reported by Yan *et al.* [102] and will be described in the following. The experiment was carried out on suspended MoS_2 membranes that were fabricated in the context of this thesis using the transfer technique described in appendix B. Figure 2.10a and b show the schematic depiction of the experiment (a) and the optical image (b) of a typical MoS_2 nanosheet suspended across a series of circular holes etched in thin Si_3N_4 membranes ($\sim$ 20 nm thick). The technique consists in measuring the evolution of the frequencies of the Raman modes E^1_{2g} and A_{1g} (section 2.2.4) upon changing the power P of the excitation laser and the temperature T of the sample. The laser is focused at the center of the hole and the beam spot-size (0.36/0.6 μm) is chosen in such a way to be smaller than the membrane diameter (1.2 μm).

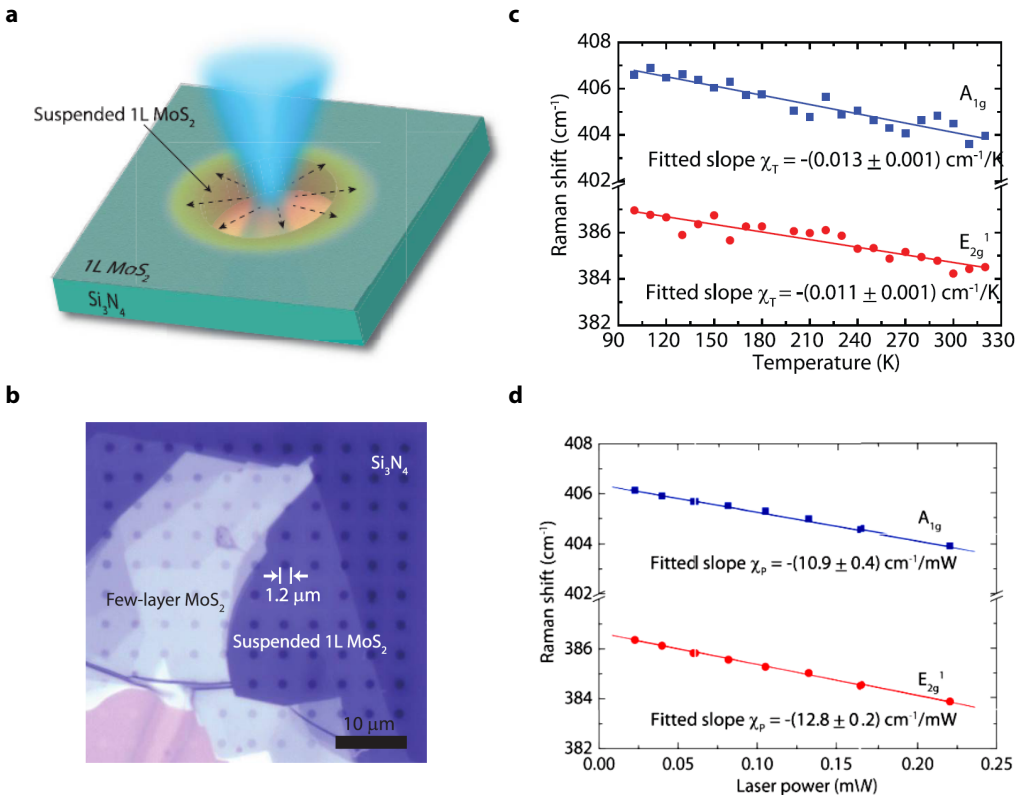

Figure 2.10: Thermal conductivity of monolayer MoS_2 from temperature-dependent Raman spectroscopy. a, Schematic depiction of the Raman measurements performed on monolayer MoS_2 sheets suspended across microfabricated circular holes. The laser beam is focused at the center of the hole and the heat propagates towards its edges. **b,** Optical micrograph of exfoliated MoS_2 flakes placed on a Si_3N_4 perforated grid. **c,d,** Raman peak frequencies of both A_{1g} (blue squares) and E^1_{2g} (red circles) modes as a function of temperature (**c**) and laser power (**d**). Fit lines and resulting linear temperature coefficients χ_T and power coefficients χ_P are shown in **c** and **d** respectively. Reprinted with permission from ref. [102], © 2014 American Chemical Society.

Under low-power excitations (< 0.14 mW), the thermal conduction through the suspended material is high enough for avoiding local heating so that constant temperature measurements can be performed. It is possible to observe in figure 2.10c that the frequencies of both E^1_{2g} and A_{1g} peaks decrease linearly with increasing temperature in the whole range 90 – 330 K. The negative linear dependence of the Raman modes in a given temperature range is encountered in several materials; it stems from the anharmonic nature of the interatomic potential that is also at the origin of lattice thermal expansion. The knowledge of the temperature coefficients χ_T of the Raman modes opens the way to a novel and non-invasive Raman method to monitor local T changes in MoS_2 devices, due for instance to Joule heating or light exposure.

With increasing P, the thermal conductance of the MoS_2 membrane is not sufficiently

large to avoid local increase of T and therefore the Raman-active modes undergo a red shift. Figure 2.10d displays the linear dependence of the E^1_{2g} and A_{1g} frequencies on P, as extracted from a series of Raman spectra acquired at RT upon changing the excitation laser power. The linear P coefficients (χ_P) of each mode are indicated in the same figure. Hence, a linear relationship could be attained between the P input and T at the center of the hole. Theoretical models describing the dynamics of heat transport through the 2D sheet and the surrounding Si_3N_4 were used to fit the T *vs.* P data and thus to obtain the material's TC. A final value of 34.5 ± 4 W/mK was extracted, in fair agreement with the results of first-principles lattice dynamics simulations (35.5 W/mK at RT) [102]. Additional calculations based on density functional perturbation theory (DFPT) have been performed also by Cai *et al.* [88], who reported the phonon dispersion relationships of monolayer MoS_2, as well as its intrinsic thermal conductivity. The latter was obtained using a non equilibrium Green's function (NEGF) approach and was found to be equal to ~ 23 W/mK. Other theoretical and computational works have been published (e.g [87], [104], [105]) whose results (1 – 30 W/mK) are lower compared to the experimental values.
In table 2.2, the TC of monolayer MoS_2 is compared to that of other materials commonly used or envisioned to be used in electronics. The most striking aspect is the large difference – more than two orders of magnitude – between the TC of graphene and that of monolayer MoS_2. This can be attributed to a number of factors, among which the very high group

Material	TC (W/mK)
Si	150 [a]
SiO_2	1.4 [a]
Ge	60 [a]
Carbon Nanotubes (single-wall)	3500 [b]
Graphene	4840-5300 [b]
h-BN (few layers)	250-360 [c]
Monolayer MoS_2	**34.5**

Table 2.2: Comparison among the TCs of different materials. TC of common materials used in microelectronics (a, ref. [18]), carbon-based materials (b, ref. [96]) and hexagonal boron nitride (c, ref. [103]).

velocities of acoustic phonons in graphene (sound velocity up to ~ 20 km/s [106]) and the different behavior of thermal expansion and anharmonic vibrations [105] of the respective lattices.
The low thermal conductivity of monolayer MoS_2 is convenient for application in thermoelectric devices, where a low TC in combination with a high Seebeck coefficient results in high thermoelectric efficiency (i.e. large figure of merit ZT [104, 107]). Recently, a large and tunable value of the Seebeck coefficient between -4×10^2 and -1×10^5 μV/K has been reported by Buscema *et al.* [108]. They showed that monolayer MoS_2 is a promising thermoelectric material [107] and could be advantageously employed in nanoscale applications such as thermal energy harvesting and thermopower generators.

2.2.6 Mechanical properties

The relationship between strain ε and stress σ in a material subjected to a loading force is described by the well-known Hooke's law. Its most simple formulation in one dimension takes the form

$$\sigma_x = E_x \cdot \varepsilon_x \tag{2.3}$$

where E_x is the Young's modulus that quantifies the stiffness of the material along a direction x parallel to a uniaxial load σ_x. This formula is the mechanical equivalent to Ohm's law (equation 2.1) and describes the behavior of a material for relatively small loads, i.e. in the elastic regime. However, for higher load values, the material can be irreversibly modified till the point of rupture. The maximum load $\sigma_{\max}$ that a material can withstand prior to its mechanical failure is referred to as breaking strength. In the case of a defect-free crystal, the breaking strength is ultimately determined by the intrinsic strength of the crystal's interatomic bonds [109]. This aspect was investigated in the 1920's by Griffith, who predicted the ultimate strength of a solid to be $\sigma_{\max} \approx \frac{E}{9}$. In 2008, Lee *et al.* [110] measured the mechanical properties of exfoliated sheets of graphene and obtained a $\frac{E}{\sigma_{\max}}$ ratio close to the ideal value indicated by Griffith. Thanks to its high-crystallinity and to the superlative strength of its sp^2 hybridized C–C bonds, graphene holds the record for the strongest material ever measured, with a breaking strength of ~ 130 GPa and a Young's modulus of ~ 1 TPa [110].
The discovery of the outstanding mechanical properties of graphene stimulated intense experimental and theoretical research to quantify the unexplored mechanical properties of 2D materials beyond graphene, such as monolayers of TMDs. These materials are nowadays of high technological interest because they hold great potential for use in high-end bendable and transparent electronics. For example, monolayer MoS_2, combined with conducting graphene and insulating h-BN, could be advantageously employed as semi-

conducting channel in all-2D field-effect transistors (FET) integrated on flexible substrates [111]. However, before implementing bendable technologies based on these materials, it is necessary to attain detailed information on their mechanical properties and characterize the influences of strain/deformation on the electronic and optical characteristics of the 2D crystals. In this thesis, an experimental study was conducted to extract the in-plane stiffness E and breaking strength $\sigma_{\max}$ of mono- and bilayer sheets of MoS_2. The measurements were carried out through nanoindentation experiments performed with the tip of an atomic force microscope (AFM) on free-standing 2D membranes. These were fabricated by transferring ultrathin flakes of MoS_2 on oxidized silicon substrates prepatterned with an array of microfabricated circular holes. The transfer procedure is reported in appendix B, whereas the results of the investigation and its methods are described in chapter 3, which contains to the original report of the work (ref. [8]). The latter was published in late 2011 and since then a number of experimental and theoretical studies have been conducted on the same subject by different research groups, who reported results in agreement with those indicated in ref. [8]. This section will briefly review the work done in the last four years to characterize the mechanical properties of 2D sheets MoS_2.

The nanoindentation method adopted in this thesis was previously employed for single-layer [110] and multilayer [112, 113] graphene sheets. Its main advantage consists in the possibility to access, within a single experiment, to different material's properties, among which the Young's modulus of the 2D membrane E^{2D}, its pretension σ_0^{2D} and breaking strength $\sigma_{\max}$. A schematic illustration of the technique is presented in figure 2.11. During the indentation process, the tip is pushed against the center of the membrane using the vertical displacement Δz_p of the piezotube of the AFM. The cantilever deflection Δz_c is measured *via* the optical beam deflection method [114] and recorded at the same time as the membrane is being deformed under the force F exerted by the tip. Under equilibrium conditions, the tension forces responsible for the stretching of the membrane balance the force F, which is calculated from Hooke's law

$$F = k \cdot \Delta z_c \tag{2.4}$$

where k is the spring constant of the cantilever and can be measured with multiple techniques, such as the thermal noise method (Hutter-Bechoefer) described in ref. [115]. From the diagram of the z-displacements reported in figure 2.11a and b, the following expression can be deduced to calculate the membrane deflection δ

$$\delta = \Delta z_p - \Delta z_c \tag{2.5}$$

Hence, F *vs.* δ curves can be readily obtained, as the ones reported in figure 2.11c for the case of mono- and bilayer MoS_2 sheets. It is from these curves, in combination with

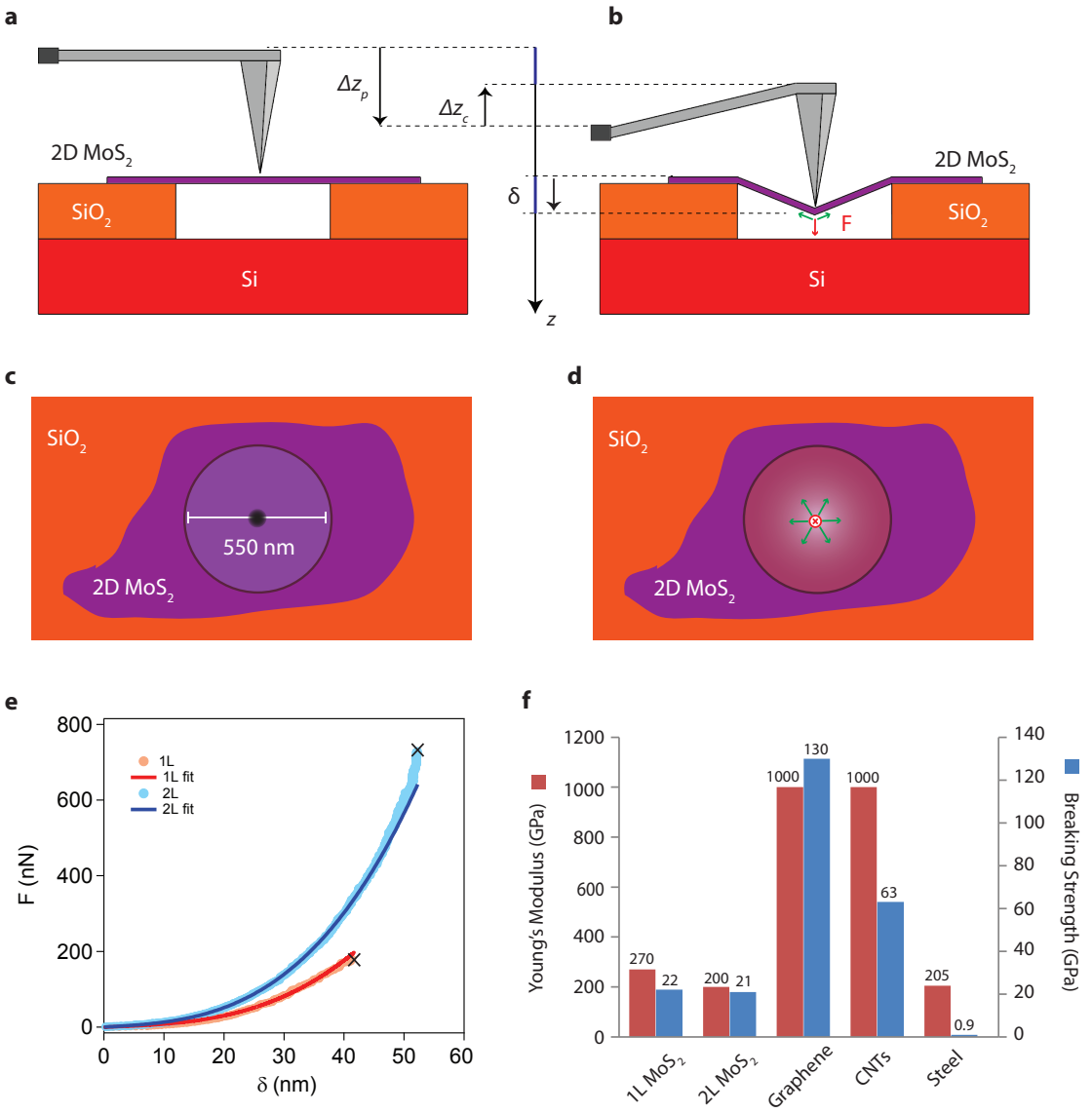

Figure 2.11: Nanoindentation of 2D MoS_2 membranes. Schematic illustration of the nanoindentation measurements performed with the tip of an AFM. **a**, The tip lies close to the center of the membrane without exerting any force. **b**, The vertical motion of the AFM piezotube towards the sample, Δz_p, results in the positive deflection δ of the membrane and in the negative deflection Δz_c of the cantilever. The force F exerted by the AFM tip (red arrow) is balanced by the tension forces (green arrows) responsible for the stretching of the membrane. **c,d,** Top-views of the drawings shown in **a** and **b** respectively. The black circle in **c** represents the AFM tip, whose radius is $\sim 12\,\mathrm{nm}$. **e,** Example of loading curves F vs. δ for mono- (1L) and bilayer (2L) MoS_2 fitted with equation 2.6 (see main text). The black crosses denote the occurrence of breaking events. **f,** Young's modulus (red) and breaking strength (blue) of 2D MoS_2 are compared to those of graphene, carbon nanotubes (CNT) and stainless steel. The data are extracted from table 1 of ref. [8].

suitable physical models, that the desired information about the material's mechanical properties can be extracted.
The 2D MoS_2 membranes are assumed to behave as clamped circular membranes, made of a linear isotropic elastic material. Moreover, as the AFM tip curvature radius is considerably smaller than the radius of the circular membrane (figure 3c and d), the point-load force approximation can be reasonably applied. Under these assumptions, the F *vs.* δ curves are described by the semiempirical formula

$$F = \sigma_0^{2D}\pi\delta + E^{2D}\frac{q^3}{r^2}\delta^3 \tag{2.6}$$

where $q = q(\nu)$ is a dimensionless function of the Poisson ratio ν of the material (~ 0.3). The Young's modulus of the 2D sheet E^{2D} and the membrane pretension σ_0^{2D} are extracted by fitting the aforementioned analytic expression to the experimental data, leading to $\sigma_0^{2D} = 0.02 - 0.2$ N/m and $E^{2D} = 180 \pm 60$ N/m for the case of monolayer MoS_2. The corresponding effective bulk modulus (270 ± 100 GPa) is given by $E = \frac{E^{2D}}{t}$, where the thickness t of monolayer MoS_2 is assumed to be 0.65 nm. The breaking strength of the material is evaluated by further indenting the membranes up to the occurrence of their mechanical failure (black crosses in figure 2.11e). The maximum load before rupture is estimated to be $\sigma_{max} = 22 \pm 4$ GPa. Over a total of 9 monolayer membranes investigated, the highest recorded breaking strength is ~ 30 GPa, which corresponds to approximately 11% of the Young's modulus (i.e. $\frac{E}{9}$). This represents, in agreement with Griffith [109], the upper theoretical limit of a material's breaking strength and reflects the intrinsic strength of the interatomic bonds. The results obtained for both mono- and bilayer MoS_2 are summarized in the histogram of figure 2.11, which also provides a comparison with the mechanical characteristics of carbon-based materials and stainless steel. Due to the intrinsic properties of its sp^2 C-C bonds, graphene shows superior Young's modulus and breaking strength, being 4-5 times stiffer and ~ 6 times stronger than 2D MoS_2. However, the latter is ~ 24 times stronger than steel, suggesting that nanosheets of MoS_2 could be conveniently employed as reinforcing elements in composites.
Other nanoindentation experiments were performed by Castellanos-Gomez *et al.*, who [116] studied the in-plane stiffness of thicker MoS_2 membranes (5 to 25 layers) and reported an average Young's modulus of 330 ± 70 GPa comparable to that of graphene oxide nanosheets. Follow-up computational works are also in fair agreement with the results of experiments. For instance, Li [117] evaluated the biaxial in-plane elastic modulus of 2D MoS_2 sheets from first-principles calculations and obtained excellent agreement with experiments (250.2 ± 5.8 GPa). Jiang *et al.* [87] developed a Stillinger-Weber parametrization of the interatomic potential of a single layer of MoS_2 and predicted its stiffness to be 229 GPa. More recently, Lorenz *et al.* [118] carried out an atomistic simulation of the AFM nanoindentation process using DFT based tight-binding methods, and found the Young's

modulus of a single MoS_2 layer to be ~ 262 GPa. The non-linear elastic behavior of the 2D membranes was investigated by Cooper *et al.* [119], who conducted a combination of experimental and theoretical studies. The authors performed AFM nanoindentation measurements on 2D membranes fabricated without the use of a transfer procedure, in an effort to avoid transfer-induced defects and contamination; moreover, they carried out first-principles DFT calculations to obtain the non-linear elastic properties of the material, which were further used in a finite element analysis (FEA) model to predict the behavior of the MoS_2 membrane during the indentation process. Their work resulted in a breaking strength of ~ 27 GPa and Young's modulus ~ 210 GPa related to each other as $\frac{E}{\sigma_{\max}} \approx 8$, similar to the case of graphene [110].

All the reports mentioned above are in agreement with the value obtained with nanoindentation measurements [8] within its experimental error. It was also found that monolayer MoS_2 can be deformed up to 11% of internal strain prior to mechanical failure, whereas polyimide, a typical plastic substrate used in flexible electronics, can withstand a maximum strain of ~ 7%. This indicates that the mechanical properties of MoS_2 do not represent a limit to the implementation of flexible devices.

Variations of electrical conductivity upon strain have to be carefully evaluated for use of 2D materials in flexible applications. Lee *et al.* [111] demonstrated MoS_2 FETs on flexible polymer substrates that can be stretched up to 1.5% and show unaffected electron mobility. The coupling between mechanical deformations and electronic properties of monolayer MoS_2 has been investigated by different groups (e.g. [120–122]). Calculations by Ghorbani-Asl *et al.* [122] revealed that the bandgap and the transport properties of 2D MoS_2 can be effectively tuned by means of mechanical deformations. Upon application of isotropic strain, the bandgap changes from direct to indirect, and a semiconductor-metal transition was predicted to occur at a strain level of ~ 11%, i.e. close to the maximum strain recorded in AFM experiments. This suggests the intriguing possibility to engineer novel nanomechanical devices where the electronic/optical response of the active material can be controlled by strain.

The results presented throughout this section are stimulating further research to be conducted on the mechanical and (opto-)electronic properties of other 2D semiconductors, beyond MoS_2. The objective is to translate the new and rich physics of these materials into real device applications.

2.3 Production methods

Graphene, the world's first 2D material, was originally produced using the mechanical exfoliation technique, commonly known as scotch tape method [1]. This consists in thinning down a macroscopic specimen of graphite by peeling off its layers with a piece of sticky tape. It is actually the same approach that surface scientists have used for several years to produce fresh surfaces of highly-oriented pyrolytic graphite (HOPG), a reference sample employed for the calibration of scanning tunneling microscopes (STM). Noble prize winners Andre Geim and Konstantin Novoselov had the intuition that what was left on the tape could be extremely thin. Instead of throwing away the tape with the thin graphite fragments, as microscopists used to do, they transfered them onto oxidized silicon substrates with the intention to explore their electronic properties. Unexpectedly, under the optical microscope, the colors generated by light interference allowed the observation of some atomically thin flakes [123]. Since then, the same method has been adopted by several research groups worldwide to investigate the exceptional properties and the extraordinary physics of graphene and other layered materials, among which hexagonal boron nitride (h-BN) and TMDs. As far as MoS_2, it is interesting to notice that a similar "peeling" technique was employed back in the 1960's by Frindt *et al.* [24] to produce $\sim$ 10 nm thick flakes on insulating mica substrates.
The main approach adopted throughout this thesis was scotch tape exfoliation. This allowed depositing high-quality 2D layers of MoS_2 with a high-degree of cleanliness on different substrates (e.g. sapphire), as shown in figure 2.12. The scotch tape method can be classified as a top-down production technique, where highly-crystalline 2D materials are obtained from the exfoliation of their bulk counterparts. However, this approach can

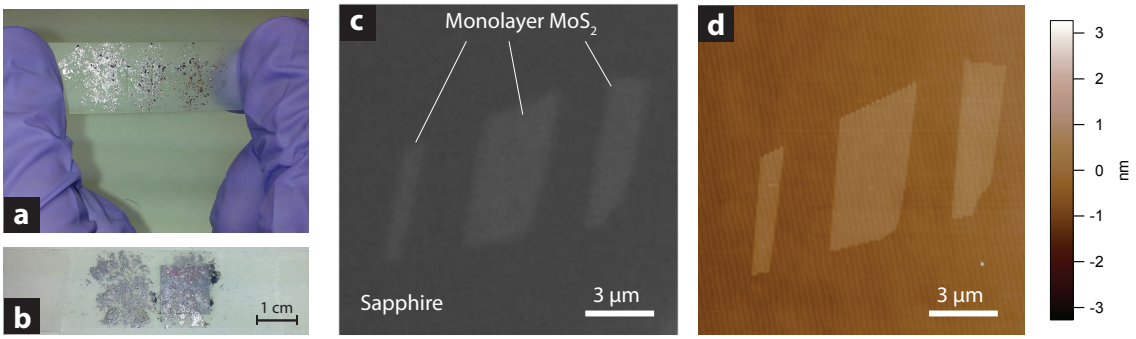

Figure 2.12: Monolayer MoS_2 flakes produced by mechanical exfoliation. **a,** Photograph of a piece of scotch tape with molybdenite fragments. **b,** The tape is applied on a 12 mm × 12 mm substrate. After tape removal, careful analysis of the sample surface under an optical microscope allows finding ultrathin MoS_2 flakes. **c,** Optical micrograph of three monolayer MoS_2 flakes identified on the surface of sapphire. The original image was converted into grayscale and the contrast was enhanced. **d,** AFM image of the flakes shown in **c**.

be used exclusively in the context of exploratory research, since it is characterized by a low yield of monolayers, slow production times and overall, the typical lateral size of 2D flakes rarely exceeds the dimensions of ~ 50 μm. Hence, mechanical exfoliation is not suitable for practical applications, which require high yield of 2D materials with uniform properties over centimeter-scale large areas. In the last few years, fast-moving research has been carried out by several academic and industrial laboratories to develop novel techniques for the large-scale production of 2D crystals. Two different strategies have been followed, namely large-scale liquid exfoliation and bottom-up growth methods. The aim of this section is to provide the reader with a description of the rapid progress done in this field, with a special focus on the novel methods for the production of monolayer MoS_2.

2.3.1 Liquid phase exfoliation

Among the family of top-down methods, liquid phase exfoliation represents a fast and low-cost approach to obtain large quantities of 2D materials, which are necessary in applications such as catalysis, electrochemical devices and sensors [13]. The use of liquids for exfoliation of MoS_2 has been reported back in 1986, when Joensen, Frindt and Morrison [25] succeeded to exfoliate MoS_2 down to a "one-molecule-thick layer" using ion intercalation. This approach consists in inserting ions between the MoS_2 atomic planes to increase the distance between adjacent layers and favor their separation. N-butyllithium in hexane can be used as the intercalation agent [124], whereas the exfoliation process is usually conducted *via* ultrasonication in water. The strong reaction of lithium with water produces gaseous H_2 that promotes the separation of the layers. A major drawback is represented by the lack of control over the degree of intercalation, so that material decomposition or low monolayer yield can occur as a consequence of an excessive or incomplete ion insertion. Zeng *et al.* [125] developed a controllable electrochemical lithiation process (figure 2.13a) that enabled high-yield production of different 2D crystals. The method consists in using bulk pieces of layered materials as the cathode electrode and lithium foils as the anode of a simple electrochemical cell. In this set up, the control over the degree of ion intercalation is easily attained by monitoring the current flow in the cell; in addition, the process can be conducted at room temperature and it requires only ~ 6 h [127]. Figure 2.13b shows an AFM image of a set of monolayer MoS_2 flakes obtained by spin-coating a solution of MoS_2 in methanol onto an oxidized silicon substrate. It can be seen that the film is not continuous but is composed by several flakes with submicrometer-scale lateral dimension. The monolayer yield is excellent, as almost 100% of the flakes are single layers [13]; however, the small size of the flakes makes them not suitable for fabrication of electronic devices and circuits. Another problem related to lithium intercalation was anticipated in section 2.2.1, when it was mentioned that exposure to n-butyllithium can transform the original semiconducting 2H phase into the 1T metallic polytype. This represents a serious obstacle

for technological applications, since local variations of the crystal structure correspond to detrimental non-uniformities in the material's electronic and optical properties. A possible solution was proposed by Eda *et al.* [74], who reported the use of thermal annealing at 300 °C to restore the 2H phase and recover the direct bandgap photoluminescence.
In 2011, Coleman *et al.* [126] published a comprehensive study on liquid phase exfoliation of layered compounds, where they showed that these materials can be exfoliated through ultrasonication in common organic solvents without the use of highly reactive ions. For example, MoS_2 and WS_2 were successfully dispersed in n-methyl-pyrrolidone (NMP) and boron nitride (BN) in isopropanol (IPA), as shown in figure 2.13c. They tested a large number of material-solvent combinations and observed that the enthalpy of exfoliation could be minimized by choosing the surface energy of the solvent to be equal to that of the layered compound. NMP was found to be the optimal solvent for MoS_2 with a surface energy of ~ 70 mJ/m^2 [126, 128]. The use of solvents overcomes the problem of undesired polytype transitions occurring during lithium intercalation, but results in a lower yield of monolayer flakes with irregular size distribution. Coleman and coworkers have also demonstrated that layered TMDs can be mixed with different types of materials in hybrid dispersions and composites. As an example, they showed that MoS_2 effectively reinforces polymers and can be combined with graphene in multifunctional hybrid films.
Different technologies are envisioned thanks to the ready availability of gram-scale quan-

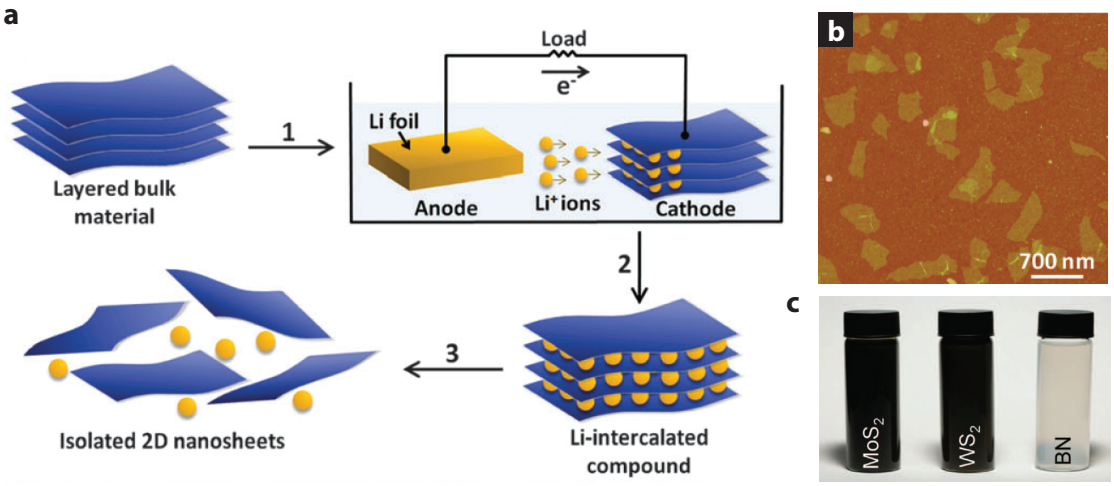

Figure 2.13: Liquid phase exfoliation of 2D MoS_2. **a,** Schematic illustration of the electrochemical lithiation process used for the fabrication of 2D nanosheets from layered bulk materials. **b,** AFM image of MoS_2 nanosheets on Si/SiO_2 substrates obtained as illustrated in **a** and deposited by spin-coating. The sheet thickness is ~ 1 nm. **a** and **b** are adapted with permission from ref. [125], © 2011 John Wiley and Sons. **c,** Photographs of dispersions of layered materials in different solvents: MoS_2 and WS_2 are in NMP and BN is in IPA. Adapted with permission from ref. [126], © 2011 American Association for the Advancement of Science.

tities of 2D materials in solutions. Further progress in this research area is expected to enable advanced composite materials and to pave the way towards electronic devices manufactured with inexpensive solution-based techniques. In this context, TMDs may represent a potential high-mobility alternative to organic materials for use in low-cost flexible electronics.

2.3.2 Large-area growth

For the fabrication of highly-integrated (opto-)electronic devices based on 2D materials, it is necessary to develop robust techniques to synthesize continuous films with uniform properties over centimeter-scale large areas. To this purpose, the most promising method is chemical vapor deposition (CVD), a technique that has been extensively utilized in the microelectronic industry for the deposition of a broad range of materials [129]. It is based on the use of volatile precursors that react/decompose on the surface of a sample to produce an amorphous or crystalline film of the desired material.
In 2009, Li and coworkers [130] demonstrated the CVD growth of graphene on copper foils, a key achievement that enabled the progress of several technologies envisioned for this extraordinary 2D material. Since early 2012, intensive research has been performed also on the large-scale production of 2D TMDs. Most investigations have been focused on MoS_2, the prototypical and best studied TMD to date, and a variety of bottom-up methods have been proposed to attain its scalable synthesis. Some of these methods will be described in the following of this section.

In 2012, Lin *et al.* [131] reported on the direct sulfurization of MoO_3 thin films thermally-evaporated on sapphire substrates. The process is schematically presented in figure 2.14a. Sapphire samples are coated with thin films of MoO_3 ($3-4$ nm thick), which are then reduced to MoO_2 through thermal annealing at 500 °C in Ar/H_2 atmosphere. Afterwards, the samples are exposed to sulfur vapor and a second annealing step at 1000 °C is performed to convert MoO_2 into a thin layer ($\sim$ 2 nm thick) of MoS_2. This method allows for the wafer-scale deposition of a continuous MoS_2 film, as shown in figure 2.14b. However, the as-grown material is highly polycrystalline, it is thicker than a monolayer and its electrical properties show low electron mobility ($\mu \sim 0.8\,cm^2/Vs$) and uncontrolled n-type doping.
Zhan *et al.* [132] reported a similar procedure based on the direct sulfurization of thermally-evaporated Mo thin films [133]. In this way, they could produce p-doped MoS_2 nanosheets on SiO_2 substrates, though with low mobility ($\mu \sim 0.04\,cm^2/Vs$).
Liu *et al.* [134] adopted an alternative approach, based on the thermal decomposition of ammonium-thiomolybdate ($(NH_4)_2MoS_4$) on the surface of different materials. Figure 2.14c illustrates the growth procedure: different insulating substrates, such as sapphire and SiO_2, are dip-coated with the liquid $(NH_4)_2MoS_4$ precursor; the molecular films are

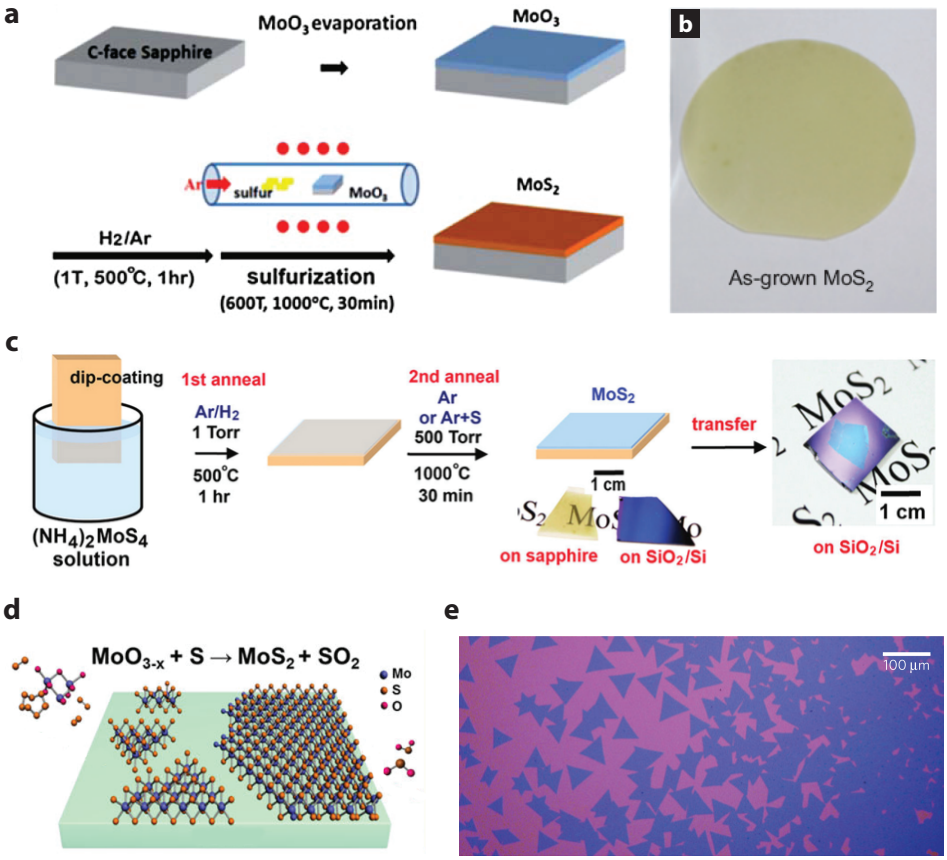

Figure 2.14: Growth of large-area monolayer MoS_2 films. **a,** Schematic illustration of the MoO_3 sulfurization process. **b,** Photograph of a 2D MoS_2 film deposited on a 2 inch sapphire wafer. **c,** Schematic depiction of the growth process based on $(NH_4)_2MoS_4$. The as-grown material can be transferred onto arbitrary substrates. **d,** Schematic representation of the synthesis of 2D MoS_2 films on insulating substrates: MoO_3 and S precursors react in the vapor phase and form a monolayer of MoS_2 on the substrate surface. **e,** Optical micrograph of monolayer MoS_2 triangular sheets grown by CVD using MoO_3 and S precursors.
a and **b** are adapted with permission from ref. [131], © 2012 Royal Society of Chemistry. **c** is adapted with permission from ref. [134], © 2012 American Chemical Society. **d** is adapted with permission from ref. [135], © 2015 American Chemical Society. **e** is adapted with permission from ref. [136], © 2013 Nature Publishing Group.

then transformed into MoS_2 by a two-step thermolysis process, consisting of (i) annealing at 500 °C in Ar atmosphere and (ii) annealing at 1000 °C in a sulfur-rich environment. The final MoS_2 sheet is on overage three-layers thick and its electrical properties resemble that of the high-quality exfoliated material with electron mobility $\mu \sim 4.6\,\mathrm{cm}^2/\mathrm{Vs}$.
Lee *et al.* [137] were the first to report on the growth and characterization of MoS_2 films with single-layer regions. Their approach relied on the gas-phase reaction of MoO_3 and S powders both vaporized inside a CVD furnace. The involved chemical reaction and the growth of MoS_2 on the sample surface are shown in figure 2.14d. It was found that

treating the substrate surface with aromatic molecules, such as graphene oxide, promoted the uniform growth of the 2D material thanks to the seeding effect of the molecules. The first report on this technique [137] described 2D MoS_2 sheets grown on SiO_2 with n-type semiconducting behavior and low electron mobility ($\mu \sim 0.02$ cm^2/Vs); moreover, the films displayed remarkable thickness variations over their surface area. A following report [138] showed the growth of monolayer MoS_2 on different surfaces (e.g sapphire, quartz, SiO_2) with uniform thickness on centimeter-scale areas and with electrical properties comparable to that of the exfoliated flakes. Key to this achievement was judged to be the use of perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) molecules, serving as seed layer to promote nucleation. However, similar results were obtained with the same CVD method by van der Zande *et al.* [136] also on bare SiO_2 substrates, presumably due to a limited exposure to air of the solid precursors. Figure 2.14e presents an optical image of a typical monolayer MoS_2 film grown on SiO_2. The triangular domains on the left correspond to the monocrystalline grains that are typically observed in the early stages of the growth. As new material is adsorbed on the substrate surface, the triangles keep growing and finally merge forming a continuous polycrystalline film (on the right). The size of largest individual islands before merging was observed to be ~ 120 μm [136]. It is worth to noting that the coalescence of islands with different shapes and orientations can give rise to severe grain boundaries that destroy the electrical and mechanical properties of the material. The experimental characterization of the grain boundaries was reported by both Hone's [136] and Lou's groups [139]. It was found that the major limiting factor to the growth of monocrystalline monolayer MoS_2 lies in its rare and complex nucleation process, which is modulated by the substrate surface [139].

If the objective of producing a high-quality monolayers with uniform thickness over large areas has been satisfactorily achieved by the end of 2013, the new challenges facing the field are now related to the enlargement of the crystal domains and to the suppression of the detrimental effects of the grain boundaries. In this context, further studies are needed in order to achieve control over the density, shape and orientation of the islands in the early stages of the growth, as well as to shed light on the effects of the underlying substrate. Dumcenco *et al.* [140] made important steps in this direction by proving that the lattice orientation during growth can be controlled *via* a careful choice and engineering of the substrate surface. An epitaxial-like growth was observed on the c-plane surface of sapphire, which was thermally annealed at 1000 °C in air to produce atomically smooth terraces. The van-der-Waals interaction between the substrate and MoS_2 was found to be strong enough to template the growth of islands with a limited number of lattice orientations, so that upon coalescence a large monocrystalline domain can be formed with a very low concentration of grain boundaries.

Along with thickness uniformity and large single-crystal domains, an additional requirement consists in the synthesis of 2D films with very low density of defects (e.g. sulfur

vacancies) and impurities. In fact, the latter can strongly alter the electronic properties of the material [141], thus hampering the manufacturing of electronic devices. At this stage, the lack of wafer-scale monocrystalline 2D semiconductors with very low defect and impurity densities still represents the bottleneck to the realization of the first commercial (opto-)electronic products. However, the fast progress made in only few years can be seen as an optimistic indicator that new strategies will be soon available to overcome the remaining obstacles.

2.4 Device applications based on monolayer MoS_2

The growing technological interest in 2D MoS_2 and related TMDs was initiated in 2011 by Radisavljevic *et al.* [5], who demonstrated the first single-layer MoS_2 transistor with optimal switching characteristics. Their work highlighted the potential of 2D semiconductors for use as channel materials in field-effect transistors (FET), where they can bring considerable advantages. Their atomic-scale thickness and high semiconducting energy bandgap allow for ideal electrostatic control and low standby power dissipation [26, 27]. Moreover, due to the presence of a direct bandgap, these materials can be further harnessed in optoelectronic devices, such as photodetectors and solar cells [142, 143].
Since 2011, several research groups worldwide focused their attention on the emerging class of 2D semiconductors. Experimentalists and theoreticians joined their forces to provide new insights in their physical properties and to evaluate their potential for different types of applications, ranging from (opto-)electronics to sensing and energy harvesting. In only few-years a large number of proof-of-concept devices were reported, which showed that 2D TMDs could lead significant improvements in existing technologies, as well as enable novel device concepts.
The goal of this section is to show how the properties of 2D semiconductors can be advantageous in electronics and optoelectronics. This will be done by presenting a series of emerging devices based on MoS_2 and other 2D materials.

2.4.1 Field-effect transistors

The FET (figure 2.15a) is a three-terminal device where the electric current flowing between a pair of electrodes – source and drain – is modulated by the voltage applied to a third electrode – the gate. The drain-source current I_{DS} flows through a semiconducting channel (red), which is separated from the gate electrode by a thin insulating layer – the gate dielectric (gray). In an ideal n-type FET, for gate voltages V_G smaller than the threshold voltage V_{th}, the channel should behave as an open circuit, with negligible off-current I_{off}. On the contrary, for $V_G > V_{th}$ the channel should become highly conducting and sustain a

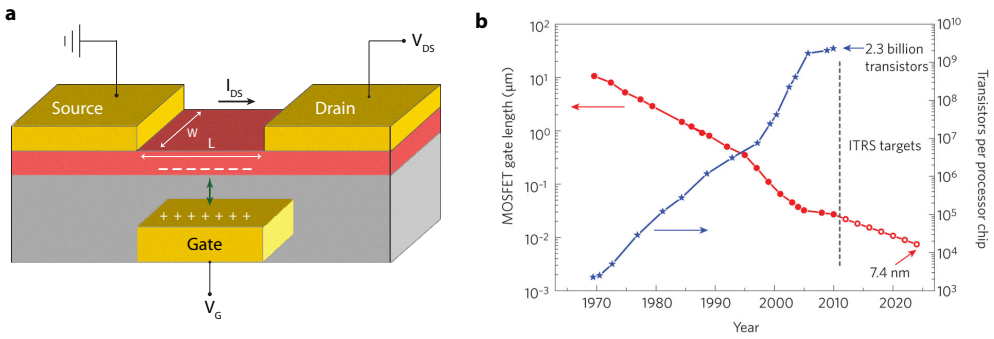

Figure 2.15: Structure and scaling of FETs. **a,** Schematic structure and electrical connections of a back-gated FET. L is the length and W the width of the transistor channel. **b,** Evolution of gate length L in production-stage integrated circuits (filled red circles) and ITRS targets (open red circles). As gate lengths have decreased, the number of transistors per processor chip has increased (blue stars). Adapted with permission from ref. [145], © 2010 Nature Publishing Group.

high current I_{on}. In practice, a large ratio ($10^4 - 10^7$ [59]) between the on- and off-current is required for the use of FETs as switches in digital electronic circuits.

The performance of transistors is in large extent determined by the length L of the channel. This is an important device parameter because it corresponds to the distance that charge carriers have to travel to carry information. The most common strategy to improve the speed of FETs consists in reducing their dimensions, which enables the integration of a larger number of devices on the same chip area. Since the 1970's, the microelectronic industry has intensively pursued the shrinking of FETs in order to boost the speed of operation and the computing power per unit area of chip processors. This led also to the strong decrease in the cost of electronic devices [144]. Figure 2.15b shows the evolution during the last four decades of the size of metal-oxide-semiconductor (MOS) devices and the corresponding change in the number of transistors per chip processor. The exponential increase of the transistor count follows the trend described in 1965 by Gordon Moore, who predicted that the density of transistors would have doubled approximately every 18 months. Unfortunately, the predicted miniaturization trend cannot last for many more years. Scaling theories affirm that Moore's law is approaching its limit, due to the onset of quantum effects as the transistor dimensions approaches the interatomic distance. Moreover, if the channel length L is reduced to be comparable with the thickness of the semiconducting channel, a number of detrimental phenomena occur, known as short channel effects (SCE), which hamper the correct functioning of the devices [145].

The International Technology Roadmap for Semiconductors (ITRS, www.itrs.net), which defines the technology requisites for future electronic devices, predicts that further scaling of transistors can be achieved by the use of novel device architectures, such as non-planar multiple-gate structures, or novel materials alternative to silicon. In this context, 2D semiconductors such as MoS_2 gained considerable attention and have been included in

the list of emerging research materials already in the 2011 version of the ITRS.
An electrostatic model based on Poisson equation can be used to evaluate the intensity of SCEs, which are induced by the undesired penetration of the drain-electrode field into the transistor channel [146]. This phenomenon is quantified by the natural length λ, which gives the position of the maximum of the electrostatic potential inside the channel, and is expressed as

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{N \cdot \varepsilon_i} \cdot t_{ch} \cdot t_i} \tag{2.7}$$

where t_{ch} (t_i) and ε_{ch} (ε_i) are the thickness and the dielectric constant of the channel material (dielectric insulator) respectively. N is the effective gate number and depends on the architecture of the device; it corresponds to 1 in the case of a single-gate (figure 2.15a), 2 for a double-gate (i.e. one top and one bottom gate) and 3 for a tri-gate device (i.e. one top and two side gates) [144]. FETs can be considered immune from SCEs when $L \gtrsim 6 \cdot \lambda$. The model allows understanding the effects of both device architecture and material properties. A transistor can be made robust against SCEs by three different strategies: (i) increasing its effective gate number, (ii) improving the gate capacitance through high dielectric permittivity and small thickness of the dielectric layer, and by (iii) vertical scaling of the channel material. However, increasing N demands for high fabrication complexity/costs, while reducing t_i augments the risk of leakage currents. Scaling of the channel thickness represents therefore a more convenient option. In the case of silicon devices, this has been achieved through the use of silicon-on-insulator (SOI) substrates, where a thin crystalline Si layer lies on a SiO_2 film. However, decreasing the Si thickness leads to uncontrolled bandgap variations – due to quantum confinement – and to mobility degradation due to broken bonds and surface roughness. Similar phenomena are encountered in other electronic materials such as Ge and III-Vs, and in heterostructure quantum wells, such as GaAs/AlAs, where the roughness-limited charge carrier mobility scales as $\mu_R \propto t_{ch}^6$ [147]. In this context, 2D semiconductors can bring significant advantages thanks to their ultimate thinness, absence of broken bonds and uniform single-layer thickness.

Short channel effects in 2D MoS_2 FETs. Common indicators of SCEs are the threshold voltage roll-off and the degradation of the subthreshold characteristics upon reducing the channel length. In the first case, V_{th} can significantly shift from the long-channel value to the point that a non-negligible current may flow in the device also when no voltage is applied to the gate electrode. In the second case, the subthreshold swing (SS) – which indicates how sharply the subthreshold current changes with incremental gate voltage – can significantly increase over the lowest ideal value of 60 mV/dec degrading the switching behavior of the FET. Therefore, controlling both phenomena is crucial for the correct and efficient functioning of transistors.
To prove the benefits associated with the use of 2D materials, Cao *et al.* [11] carried out

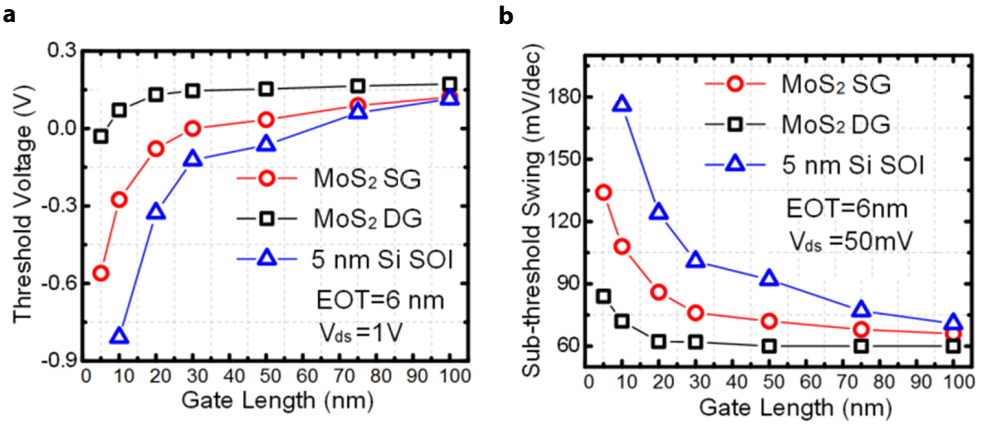

Figure 2.16: SCEs in FETs based on ultrathin MoS_2 and Si (SOI) channels. Comparison among SCEs in three different types of devices: thin Si layer with single gate (5nm Si SOI); monolayer MoS_2 with single (MoS_2 SG) and double gate (MoS_2 DG). The dielectric layer has an equivalent oxide thickness (EOT) of 6 nm. **a,** Calculated dependence of the threshold voltage on the gate length L. **b,** Calculated SS degradation with gate-length scaling. Adapted from ref. [11], © 2014 IEEE.

simulations based on the non-equilibrium Green's function (NEGF) formalism. They obtained the L-dependence of V_{th} (figure 2.16a) and SS (figure 2.16b) for monolayer MoS_2 FETs with single and double gate architecture. The results are compared to those obtained from a 5 nm thick Si (SOI) transistor. It can be seen that the characteristics of the Si FET deviate severely with respect to the long channel case when L is reduced below 40 nm. On the other hand, MoS_2 FETs show much better immunity against SCEs. As expected from the analysis of equation 2.7, the combined use of 2D MoS_2 and double-gate structure produces the best results: for $L = 10$ nm the threshold voltage has still a positive sign and SS is preserved as low as $\sim$ 70 mV/dec. This shows that 2D semiconductors such as MoS_2 are ideal transistor channel materials and hold great potential for further miniaturization of electronic devices. The latter is probably the major driving force behind the intensive research performed nowadays in this field that started growing tremendously after the realization of the first single-layer MoS_2 transistors [5], which will be described in the rest of this section.

Dual-gated single-layer MoS_2 FETs. The structure of the dual-gated FETs originally designed by Radisavljevic *et al.* is shown in figure 2.17a. The devices were fabricated on monolayer MoS_2 sheets exfoliated with the scotch tape method (section 2.3) and deposited on oxidized silicon chips. A heavily doped silicon substrate was employed as back-gate electrode and a layer of SiO_2 (270 nm thick) functioned as back-gate dielectric. A 30 nm thick film of HfO_2 ($\varepsilon_r \sim 19$) was deposited by atomic layer deposition (ALD) on the surface of monolayer MoS_2 and served as top-gate dielectric. The HfO_2 film was further capped with a metal layer (Cr/Au) that functioned as top-gate electrode. Figure 2.17b presents a

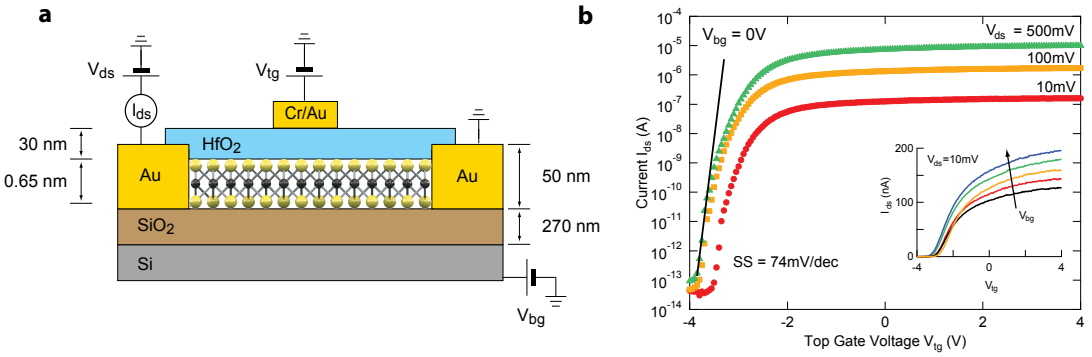

Figure 2.17: Single-layer MoS_2 transistors with optimal switching characteristics. a, Schematic cross-sectional view of a dual-gated transistor based on single-layer MoS_2. The heavily doped Si substrate serves as the back-gate, while a Cr/Au electrode serves as the top gate. The back- and top-gate dielectric consist of 270 nm of SiO_2 and 30 nm of HfO_2, respectively (not in scale). **b,** Drain-source current I_{ds} as a function of top-gate voltage V_{tg} for different drain-source bias voltages V_{ds}. Inset: I_{ds} *vs.* V_{tg} for different values of back-gate voltage V_{bg}. Top gate width, 4 mm; top gate length, 500 nm. Adapted with permission from ref. [5], © 2011 Nature Publishing Group.

set of current-voltage transfer characteristics acquired from one such device for different drain-source voltage biases V_{ds}. The back-gate electrode V_{bg} was connected to the ground, whereas a voltage V_{tg} was applied to the top gate and swept in the range $\pm$ 4 V, resulting in I_{ds} *vs.* V_{tg} transfer curves with remarkably high I_{on}/I_{off} ratio and significantly low subthreshold swing SS. From the curve acquired at V_{ds} = 500 mV it was possible to extract $I_{on}/I_{off} \approx 10^8$, with $I_{off} \approx 100$ fA (25 fA/μm) and $I_{on} \approx 10$ μA (2.5 μA/μm). The highest measured transconductance, defined as $g_m = \frac{\partial I_{ds}}{\partial V_{tg}}$, was $\sim$ 4 μS (1 μS/μm) and the subthreshold swing was found to be as low as SS = 74 mV/dec. It should be noted that the first transistors suffered from high access resistance and limited gate control due to the partial overlapping of the top-gate electrode with the underlying channel area, as schematically illustrated in figure 2.17a. In 2012, Lembke and Kis [6] succeeded in fabricating high-performance single-layer MoS_2 transistors with full gate-channel overlap (figure 2.18a) and reported a two-orders of magnitude increase in I_{on}, as well as a 30× improvement in g_m. For the first time, they showed the appearance of current saturation at large $V_{ds} > 1$ V and the achievement of a drain-source conductance $g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}}$ smaller than 2 μS/μm. In this way, they proved that an individual single-layer MoS_2 FET can offer a gain $G = \frac{g_m}{g_{ds}}$ larger than 10, revealing the possibility of employing this ultrathin semiconductor in analog electronic circuits (section 2.20). Finally, it was found that monolayer MoS_2 can sustain a current density as large as 4.9×10^7 A/cm^2 before breaking down. This value is about two orders of magnitude smaller than in graphene, but more 50 times larger than in copper, whose breakdown current density j_{BD} lies close to the limit set in metals by electromigration. The higher j_{BD} of monolayer MoS_2 is likely to be due to the covalent nature of the Mo-S bonds that are intrinsically stronger than the ionic bonds in metals.

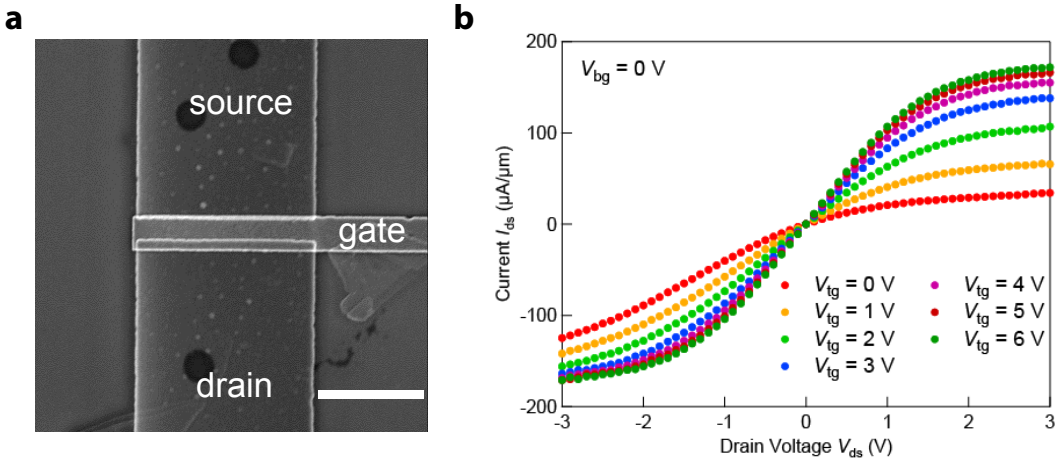

Figure 2.18: Single-layer MoS_2 transistor with optimized gate-channel overlap. **a,** Scanning electron microscopy (SEM) image of a single-layer MoS_2 FET with top-gate electrode overlapping the whole channel area and the edge-regions of the contacts. Scale bar is 2 μm. **b,** I_{ds} *vs.* V_{ds} output characteristics showing current saturation at large V_{ds}. Adapted from ref. [6], © 2012 American Chemical Society.

All these promising results brought to light the potential of MoS_2 and 2D semiconductors for use in next-generation electronic devices and stimulated novel theoretical/computational works for further assessment of the material's functional properties.

Theoretical works on MoS_2 transistors. Soon after the experimental demonstration of switchable devices (ref. [5]), Yoon *et al.* [7] carried out a computational study to evaluate the ultimate performance limits of single-layer MoS_2 transistors by means of quantum transport simulations based on the NEGF formalism. They fixed the channel length to 15 nm and assumed the charge transport to be ballistic, after estimating an electron mean-free-path of the order of 15-20 nm. The simulated device presented I_{on}/I_{off} ratio in excess of 10^{10} and $SS \approx 60$ mV/dec, approaching the lowest possible value for thermionic devices [148]. At $V_{ds} = 500$ mV and $V_{tg} = 600$ mV, the maximum drive current was predicted to be $I_{on} = 1.6$ mA/μm and the transconductance $g_m = 4$ mS/μm. The authors concluded that monolayer MoS_2 is an ideal material for use in low-power electronics, as a result of its sizeable bandgap and optimal electrostatic integrity. However, as the charge transport enters the diffusive regime ($L > 15$ nm), the relatively low mobility (section 4.2) and high effective mass (section 2.2.2) could hinder its application in high-performance digital electronics, where other currently explored materials, such as state-of-the-art III-V heterostructures [7], present higher performance metrics.
In subsequent works, Alam and Lake [26] and Liu *et al.* [27] performed simulations on aggressively scaled devices ($L \leq 10$ nm), where the charge transport is purely ballistic and the low mobility value does not represent a real problem [149]. They pointed out that, under this condition, the high effective mass of charge carriers in monolayer MoS_2 is actually a

benefit, as it allows reducing the direct drain-to-source tunneling and consequently the leakage current in the off-state. Moreover, due to the fact that the large effective mass is associated with a large density of states, a higher drive current I_{on} and transconductance g_m can be achieved in these ultra-scaled FETs.
More specifically, in 2012 Alam and Lake investigated the performance of a monolayer MoS_2 FET with channel length of 5 nm and compared it with the case of an identical transistor with 3 nm thick Si (SOI) channel. They found that the MoS_2 transistor is significantly more robust against SCEs than the Si counterpart. In addition, its figures of merit were found to fulfill the ITRS requirements for low operating power technology of 2026. The following year, Liu *et al.* studied the scaling limit of dual-gated monolayer MoS_2 FETs in comparison with equivalent 3 nm thick Si transistors: the first can be scaled down to 8 nm, whereas SCEs hampers the scaling of Si transistors below 10 nm. At the scaling limit, it was found that the MoS_2 FETs, in the double-gate architecture, satisfy the ITRS targets for high-performance logic devices of 2023.

Challenges and opportunities. The computational studies presented above highlighted the potential of monolayer MoS_2 for replacing traditional semiconductors, such as silicon, in low-power electronic applications. They also showed that, in the context of high-performance electronics, monolayer MoS_2 will bring significant advantages only if a purely ballistic transport is achieved. This requires fabricating FETs with small channel lengths ($L < 15$ nm), which in turn demands for the realization of ohmic contacts with resistance much lower than that of the short channel. This is presently one of the main challenges facing the field, together with the manufacturing of large-area defect-free single-crystals of 2D semiconductors – as outlined in section 2.3.2 – and the achievement of systematic control over doping, necessary for the production of complementary logic circuits with both *p*- and *n*- channel transistors. Several research efforts will have to be undertaken in the next years to overcome the aforementioned challenges. In the short term, it is expected that FETs based on 2D TMDs will find application in flexible electronics, where they can already bring substantial advantages over currently used materials, i.e. organic semiconductors, thanks to a high degree of mechanical flexibility, relatively higher mobility and transparency. [149, 150].
If the FETs are not aggressively scaled, diffusive transport dominates and the low charge carrier mobility sets an upper limit to the maximum operating speed of the devices. In their recent review papers, Fiori *et al.* [149] and Akinwande *et al.* [150] discuss the relationship between mobility and different performance metrics, such as current density, switching delay, frequency capability and energy efficiency. Nowadays, several reports in the literature presenting new electronic materials or novel device architectures, put a strong focus on the measurement or calculation of the mobility μ, since it provides important information on charge transport and quantify the material's potential for different types of applications.

Charge carrier mobility. In this thesis work, a great deal of attention has been given to the charge transport properties of monolayer MoS_2, which have been investigated by measuring μ under different conditions, in particular upon changing the properties of the surrounding dielectric environment. A detailed discussion on charge transport and mobility in 2D MoS_2, as well as on its limiting factors, will be given in chapter 4. Some of the most important results on the subject will be briefly reported in the next paragraphs.
The first studies of the charge carrier mobility in MoS_2 date back to the 1960's, when Fivaz and Moser [21] investigated the transport properties of different bulk layered compounds by means of temperature-dependent Hall effect measurements. For MoS_2, $MoSe_2$ and WSe_2, they observed a predominant n-type semiconducting behavior and extracted a Hall mobility $\mu_H \sim 100\ cm^2/Vs$ at room temperature (RT). In 2005, Novoselov *et al.* [2] reported on the fabrication and characterization of back-gated n-type FETs based on monolayer MoS_2 sheets. Thinning the semiconducting material down to a single layer resulted in strongly reduced mobility values, in the range $0.5-3\ cm^2/Vs$. The dual-gated FETS fabricated by Radisavljevic *et al.* showed significant improvement, with μ at RT of the order of $40-50\ cm^2/Vs$, as extracted from Hall and field-effect measurements [5, 9, 10]. It was proposed that the use of HfO_2 gate dielectrics – with high permittivity κ – resulted in a significantly higher mobility due to an enhanced screening of the Coulomb potential of ionized impurities located within the MoS_2 channel or at the MoS_2-dielectric interface (see Chapter 4). Measurements by Schmidt *et al.* [151], performed on FETs fabricated on CVD grown monolayer MoS_2 sheets (section 2.3.2), have also revealed typical RT mobility values of $\sim 45\ cm^2/Vs$ [151], proving that the electronic properties of the synthetic MoS_2 are equivalent to those of the mechanically exfoliated material.
Kaasbjerg *et al.* [89] carried out DFT calculations to estimate the highest achievable mobility in monolayer MoS_2, considering exclusively intrinsic factors, such as crystal lattice vibrations (section 2.2.4). Theoretically, μ can be as high as $410\ cm^2/Vs$ at RT, which corresponds to the upper limit set by optical phonon scattering. The remarkable difference between the theoretical and experimental values indicates the presence of large amount of extrinsic scattering centers, such as impurities or other types of defects (e.g. sulfur vacancies). Therefore, further work will be necessary in the next years to eliminate these detrimental sources of scattering and raise the mobility up to the highest predicted theoretical value. In this way, single-layer MoS_2 FETs can become competitive with Si (SOI) transistors with channel thickness $t_{Si} \sim 4$ nm. It is worth to mention that the highest mobility achievable in Si FETs with 4.3 nm thick channel is $\mu = 450\ cm^2/Vs$, which is close to the highest prediction for monolayer MoS_2. However, if t_{Si} is decreased below 3 nm, the mobility dramatically drops and becomes smaller than $10\ cm^2/Vs$ for $t_{Si} = 0.9$ nm [152].

Graphene versus MoS_2. Before concluding this section, it seems worth to mention the case of FETs based on graphene. The latter, in its pristine form, is a semimetal with zero bandgap. If the charge carrier mobility is taken as the only term of comparison, the po-

tential of MoS_2 or other ultrathin semiconductors for electronic applications is drastically inferior. In fact, graphene FETs with record mobility – reaching 150,000 cm^2/Vs at RT – have been already experimentally demonstrated using h-BN/graphene heterostructures [153]. However, the absence of an intrinsic energy bandgap in graphene results in extremely low I_{on}/I_{off} ratio (few tens), which hampers it use in digital electronics. Radiofrequency (RF) flexible electronics is perhaps the most promising domain of application for graphene, where thanks to its extremely high mobility and saturation velocity ($\sim 4.3 \times 10^7$ cm/s), it can compete with state-of-the-art RF devices based on III-V semiconductors [154].

2.4.2 Digital and analog electronics

Following the successful demonstration of individual top- and back-gated single-layer MoS_2 FETs, Radisavljevic *et al.* extended their work by implementing more complex digital and analog electronic devices – comprising of a set of FETs integrated on the same chip – that were able to perform the basic logic operations, as well as of amplifying electronic signals [155, 156]. In 2011, they reported the first digital logic inverter built on a monolayer MoS_2 flake obtained with the micromechanical cleavage method [155]. The device is shown in figure 2.19. It consists of two FETs connected in series, with the common electrode serving as the output and the top-gate of the "lower" FET as the input, as illustrated in the circuit diagram in figure 2.19d (left inset). The drain terminal of the "upper" FET is connected to a voltage supply $V_{DD} = 2$ V, whereas the source terminal of

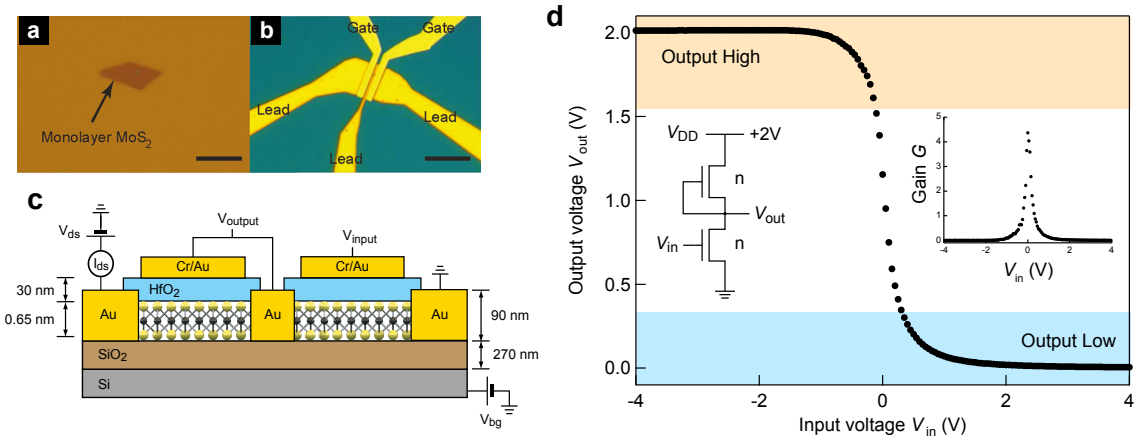

Figure 2.19: Logic inverter fabricated on mechanically exfoliated monolayer MoS_2. **a**,**b**, Optical micrographs of the monolayer MoS_2 flake (**a**) and of the logic inverter (**b**) fabricated on it. **c**, Schematic structure and electrical connections of the logic inverter, composed of two dual-gated FETs connected in series. **d**, V_{out} *vs.* V_{in} characteristic of the fabricated inverter. Insets: circuit diagram (left) and gain G as a function of V_{in} (right). Adapted with permission from ref. [155], © 2011 American Chemical Society.

the "lower" FET is connected to the ground. The dependence of the output voltage V_{out} on the input voltage V_{in} (figure 2.19d) is characterized by a pronounced high-to-low voltage transition in proximity of $V_{in} = 0$ V. It can be seen that the logical 0 (1), corresponding to low (high) input voltage is converted into the logical 1 (0), corresponding to high (low) output voltage. Due to the significant n-doping of MoS_2, the presented proof-of-concept device showed different input and output voltage levels. However, this problem could be solved by tuning the position of the threshold voltage, for instance by means of material surface functionalization [155].

The gain G of the inverter is calculated as $G = -\frac{dV_{out}}{dV_{in}}$ and is reported in figure 2.19d (right inset). It can be seen that a gain larger than 4 could be achieved, which means that monolayer MoS_2 can be effectively used for the fabrication of more complex digital circuits, consisting for example of cascaded inverters, where a gain greater than one is required.

In ref. [155], a device with two digital inputs was also presented, which consisted of two top-gated FETs connected in parallel and an external load resistor connected in series to them. The device functioned as NOR logic gate, which is a fundamental building block of digital electronics. In fact, through the assembling of multiple NOR gates, all logic operations can be implemented.

In a subsequent work, Radisavljevic *et al.* proved that a device like the logic inverter of figure 2.19, could be operated as well as analog small-signal amplifier [156]. An AC voltage

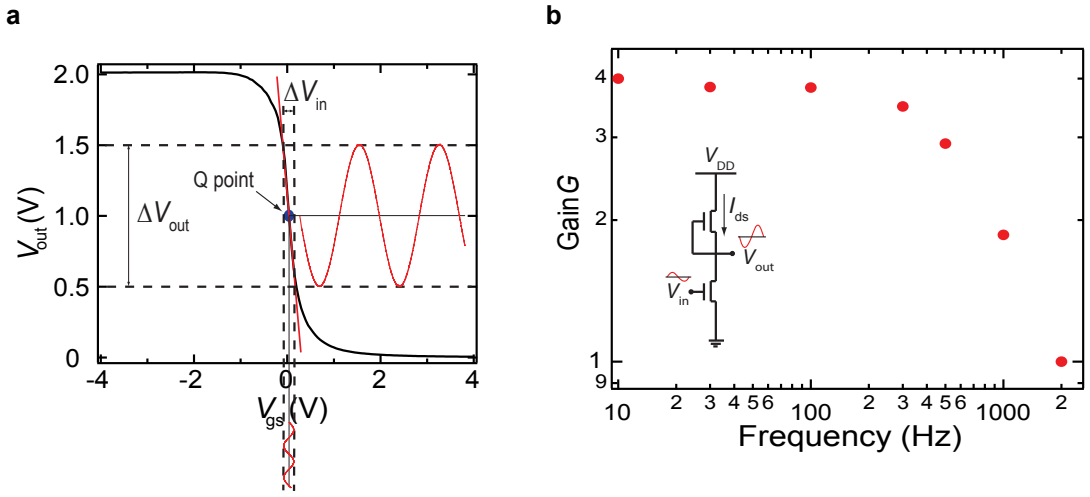

Figure 2.20: Analog small-signal amplifier fabricated on mechanically exfoliated monolayer MoS_2. a, Output voltage (V_{out}) as a function of input voltage (V_{gs}). A DC bias voltage is applied to the gate of the "lower" FET (input) to set the working point of the amplifier at Q (quiescent point). An AC signal, with amplitude $\frac{\Delta V_{in}}{2}$, is superimposed to the DC voltage, which causes the output voltage to oscillate with phase delay π and amplitude $\frac{\Delta V_{out}}{2}$. **b,** Gain G of the amplifier as a function of the AC signal frequency. G was calculated as $|\frac{\Delta V_{out}}{\Delta V_{in}}|$. Inset: equivalent circuit of the small-signal amplifier. Adapted with permission from ref. [156], © 2012 AIP Publishing LLC.

with amplitude of 100 mV and frequency f ranging from 10 Hz to 2 kHz was applied to the input terminal of the amplifier to produce a synchronous output voltage with amplified amplitude, as illustrated in 2.20a. The gain G of the amplifier, defined as the ratio between the amplitudes of the output and input signals, was found to be ~ 4 at low frequency ($f < 200$ Hz) and greater than one for $f < 2$ kHz. The cut-off frequency of this proof-of-concept device is limited by the high parasitic capacitance (e.g. due to bonding pads) and contact resistance of the FETs. Further device engineering is necessary to eliminate the parasitic components and to increase the transconductance g_m, in such a way that MoS_2 FETs can be advantageously employed in analog electronic applications.

2.4.3 High-frequency electronics

Experimental investigations on the high-frequency operation of MoS_2 FETs have been recently reported by Krasnozhon *et al.* [157], who fabricated and characterized a set of top-gated devices based on mono- and few-layer thick MoS_2 sheets, as reported in figure 2.21. Their results proved that MoS_2 FETs can operate in the technologically relevant GHz range of frequencies.

Two important figures of merit are used to evaluate the speed limits of transistors. These are the cut-off frequency f_T and the maximum oscillation frequency f_{max}. The first is defined as the frequency at which the absolute value of the small-signal current gain h_{21} becomes equal to unity, as indicated in figure 2.21c; it is related to the transit time of the charge carrier through the transistor channel and it scales with the transconductance g_m. In addition, the cut-off frequency is influenced by the parasitic impedances that are unavoidably present in any real device [154].

Similarly, the second figure of merit, f_{max}, is defined as the frequency at which the power-gain becomes equal to one. It depends on f_T, on the source and gate series resistances – R_s and R_g, respectively – and on the gate-to-drain parasitic capacitance C_{gd}. The maximum frequency of oscillation can be expressed as

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}\,(R_g + R_s) + 2\pi\, f_T\, C_{gd}\, R_g}} \tag{2.8}$$

For applications in high-speed analog electronics it is necessary to pursue both high f_T and f_{max}. To this purpose, the most common strategy consists in increasing g_m by choosing a material with high mobility μ and by reducing the channel length [154]. Another critical aspect is related to the aforementioned parasitic impedances, which need to be carefully minimized. From equation 2.8 it can be deduced that, in order to increase f_{max}, the drain-source conductance g_{ds} needs to be as low as possible, which is normally obtained by making the device operate at high V_{ds}, in the current saturation regime. At present,

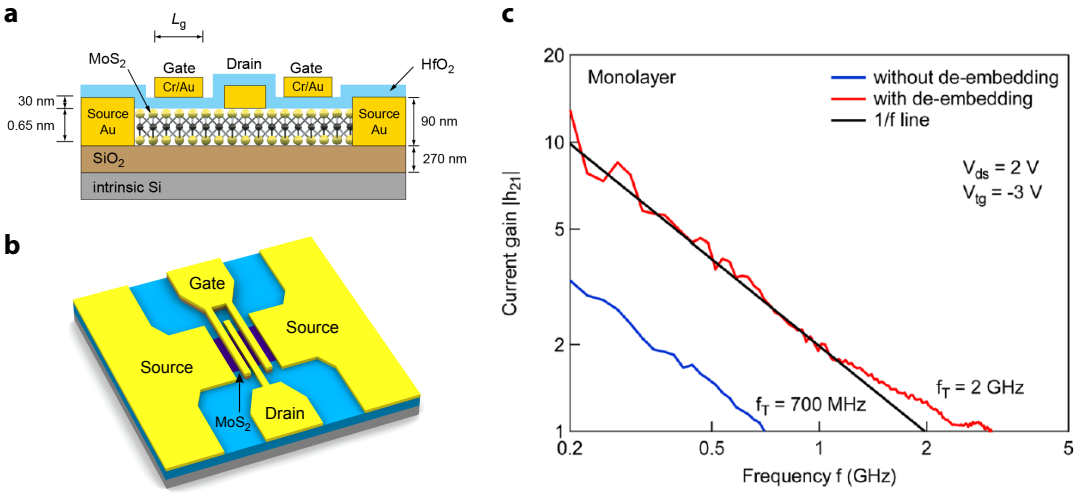

Figure 2.21: MoS_2 FETs operating in the GHz frequency range. **a,** Schematic cross sectional view of the high-frequency devices built on mechanically exfoliated flakes of MoS_2. Each device consists of two FETs connected in parallel, with common drain electrode and grounded source electrodes (ground-signal-ground configuration). The channel length L is ~ 340 nm; the gate electrode does not fully overlap with the channel and its length L_g is 240 nm. The channel width W varies in the range $9-21.5\,\mu$m. **b,** Three-dimensional schematics of the device. **c,** Small-signal current gain $|h_{21}|$ versus frequency f in log-log scale. A cut-off frequency $f_T = 2$ GHz is extracted for the case of monolayer MoS_2. De-embedding is used to take into account the effects of the parasitic impedances. Adapted with permission from ref. [157], © 2014 American Chemical Society.

the absence of I_{ds} saturation in graphene is the major limitation to its application in RF electronics. The largest reported f_{max} to date for graphene is lower than the corresponding f_T and does not exceed 100 GHz [158].

Monolayer MoS_2 could also be an interesting material for high-frequency electronics, as it presents high intrinsic transconductance, drain-source current saturation [6], as well as high mechanical flexibility, which makes it suitable for integration on flexible plastic substrates. It is worth to mention that the results of the simulations by Yoon *et al.* [7], described in section 2.4.1, allows estimating a cut-off frequency above 100 GHz for monolayer MoS_2 devices operating in ballistic regime, having $L_g = 15$ nm.

In their recent work, Krasnozhon *et al.* succeeded to fabricate MoS_2 FETs with high g_m (up to 54 μS/μm) and pronounced current saturation; they also applied the de-embedding procedure [154] to evaluate the intrinsic speed-limit of their devices characterized by a gate length of ~ 240 nm. In the case of monolayer MoS_2 FETs, they extracted $f_T \approx 2$ GHz and $f_{max} \approx 2.2$ GHz. However, the best values, namely $f_T \approx 6$ GHz and $f_{max} \approx 8.2$ GHz, were recorded in the case of FETs built on three-layer thick MoS_2 sheets, presumably due to lower contact resistance and better current saturation. The authors argue that additional improvements could be obtained by further scaling the gate length and by reducing the parasitic capacitances.

The results outlined throughout this section showed that MoS_2 can be used for realizing high-speed amplifiers and logic circuits. At this stage, it cannot compete with the materials currently employed in state-of-the-art digital and analog electronics. However, it could enable the intriguing possibility to transfer these technologies on flexible substrates, while offering interesting levels of performance.

2.4.4 Optoelectronic devices

The presence of a direct bandgap in single layers of MoS_2 and other TMDs is one of the most interesting aspects of these materials. It could enable novel opportunities in optoelectronics, such as flexible light-emitting devices [143] or transparent ultrasensitive photodetectors [142]. Moreover, the bandgap of these ultrathin semiconductors can be tuned by changing the thickness (section 2.2.2 and 2.2.3), which offers the additional intriguing possibility to adapt the material's optical response to a desired wavelength range. In the last three years, a series of MoS_2-based optoelectronic devices have been successfully demonstrated. The first phototransistor – built on exfoliated flakes of monolayer MoS_2 – was reported in 2012 by Yin *et al.* [159] and showed a photoresponsivity of 7.5 mA/W. This value is comparable to that obtained with graphene devices, but is significantly lower than in the case of Si-based photodetectors (few 100s mA/W). Soon after, Lee *et al.* exploited

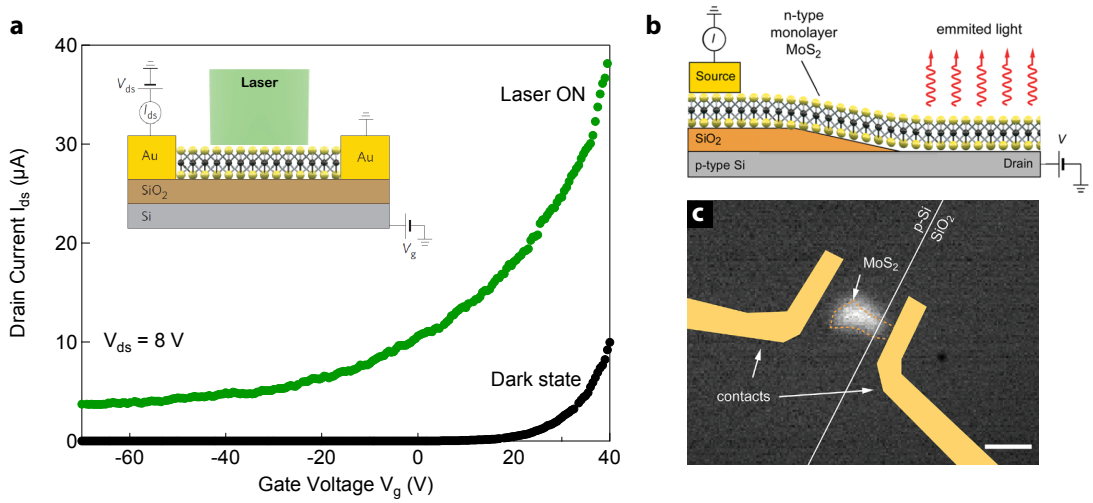

Figure 2.22: Optoelectronic devices based on exfoliated monolayer MoS_2. **a,** I_{ds} *vs.* V_g transfer characteristics of a back-gated monolayer MoS_2 FET, whose schematic structure is shown in the inset. The curves were acquired with (green) and without (black) laser-light illumination. **b,** Schematic cross-sectional view and electrical connections of the *pn* junction based on a vertical heterostructures of MoS_2 and *p*-doped Si. **c,** Map of the electroluminescence intensity with superimposed outline of the most important device components. **a,** is adapted with permission from ref. [142], © 2013 Nature Publishing Group. **b** and **c** are adapted from ref. [143], © 2014 American Chemical Society.

the aforementioned bandgap tunability to produce a set of MoS_2 photodetectors with maximum responsivity located at various wavelengths. For instance, mono- and bilayers ($E_g \sim 1.8$ eV and 1.65 eV, respectively) were found to be efficient detectors of green light, whereas three-layer thick Mo_2 ($E_g \sim 1.35$ eV) was suitable to detect red light.
In 2013, Lopez-Sanchez *et al.* reported a record photoresponsivity of 880 A/W. The measurement was performed on a back-gated monolayer MoS_2 FET, whose channel area was illuminated by means of a laser beam ($\lambda = 561$ nm) with spot size of ~ 2.8 μm, as illustrated in figure 2.22a. It can be seen that illuminating MoS_2 with the laser light produces a significant increase in drain-source current I_{ds} over the entire investigated gate-voltage range. This indicates that the photoexcited carriers provide a strong contribution to I_{ds} in both the off- (large negative V_g) and on-state (large positive V_g). It was also shown that, in the off-state, the dark current I_{off} can be extremely small, thanks to the sizeable energy gap and high electrostatic integrity of 2D MoS_2. As a consequence, the level of noise in the 2D limit can be dramatically reduced with respect to the bulk case. The noise equivalent power (NEP) is an important figure of merit that quantifies the sensitivity limit of a detector system. In monolayer MoS_2 phototransistors, NEP can be as low as 1.5×10^{-15} W/$\sqrt{\text{Hz}}$ that is more than one order of magnitude better than in commercial Si avalanche photodiodes.
In the same year, Sundaram *et al.* [160] built back-gated FETs on transparent substrates and observed electrically excited luminescence from a small region of the MoS_2 channel close to the drain electrode. Reasons for the observed electroluminescence were attributed to hot carrier processes occurring at high electric field in proximity of the contacts. More recently, Lopez-Sanchez *et al.* [143] implemented pn junctions based on vertical heterostructures of p-doped Si and n-type MoS_2 (figure 2.7b). These devices were capable to emit light from the entire heterostructure surface (figure 2.7c), through a radiative recombination process involving electrons injected into monolayer MoS_2 and holes in p-type Si. It was further proved that the Si/MoS_2 heterostructures could function as well as solar cells with external quantum efficiency (ratio between charge carriers generated and incident photons) exceeding 4 %.
In early 2014, Baugher *et al.* [161] and Ross *et al.* [162] reported the observation of light emission from lateral pn junctions based on monolayer WSe_2, where the p and n regions were formed by a simple electrostatic gating of the ambipolar 2D sheet. Different from MoS_2, which is naturally n-doped, WSe_2 occurs in nature with low levels of doping and both electrons and holes can be injected and transported.
In the next years, it is expected that the wealth of materials and properties available in the family of TMDs will promote further development of 2D optoelectronics. Moreover, the presence of spin and valley degrees of freedom (section 2.2.2) could enable new generations of optoelectronic devices. One example was recently given by Zhang *et al.* who implemented a novel chiral light source that exploits to advantage the valley degrees of freedom in ambipolar WSe_2 (ref. [77]).

2.4.5 Heterostructures of MoS_2 and other 2D materials

Nowadays, the research community is giving a great deal of attention to van-der-Waals heterostructures, i.e. vertical stacks of different 2D materials. Researchers argue that the growing ability to assemble 2D crystals in the form of 3D heterostructures will soon offer the unique opportunity to engineer materials with novel functional properties, which can be tailored *ad hoc* by choosing the appropriate 2D building blocks.
The first multilayer heterostructures, beyond the use of h-BN as substrate for graphene [166], were reported in 2011 by Ponomarenko *et al.* and consisted of a layer of graphene sandwiched between two thin layers of h-BN, which led to the observation of new physical phenomena in graphene (ref. [167]). Afterwards, several research groups worldwide have made serious efforts to fabricate high-quality heterostructures of various 2D materials. It was soon realized that hydrocarbon contaminants and/or water trapped between two artificially stacked layers (ref. [168]) represented a major obstacle to the practical implementation of van-der-Waals hybrid crystals [15]. Also in the context of this doctoral thesis, a significant fraction of work has been focused on the optimization of the transfer method (appendix B), which enabled the assembling of heterostructures based on monolayer MoS_2, graphene or h-BN.

Field-effect tunneling transistors. In the last three years, many researchers in the field faced the heterostructure fabrication challenge and built a number of (opto-)electronic devices based on 2D materials stacked on top of each other. For instance, vertical graphene heterostructures were fabricated by Britnell *et al.* [169] and by Georgiou *et al.* [163] to demonstrate graphene field-effect tunneling transistors (FETT) with improved switching ratio and low subthreshold swing. The FETT is a new type of device that exploits the tunneling of charge carriers through a barrier rather than thermionic emission, so that *SS* is not fundamentally limited to 60 mV/dec. The structure and working principle of the device are schematically illustrated in figure 2.23a. An insulating nanosheet of h-BN or TMDs (MoS_2, WS_2) is sandwiched between two graphene electrodes and serves as vertical transport barrier. The height of the energy barrier and the density of tunneling states are modulated by the voltage applied to a Si gate electrode. The proof-of-concept tunneling devices showed improved I_{on}/I_{off} compared to standard graphene FETs, namely 50, 10^4 and 10^6 in the case of h-BN, MoS_2 and WS_2, respectively. The much higher values obtained with TMDs were ascribed to the onset of thermionic transport (red arrow in figure 2.23a) – in addition to tunneling (blue arrow) – as a consequence of a lower energy barrier of semiconducting TMDs compared to insulating h-BN [163]. Note also that the observed *SS* is smaller than 60 mV/dec only in the gate voltage range where the tunneling current dominates over the thermionic current.

Solar cells. The same structure as in figure 2.23a – with WS_2 nanosheets sandwiched

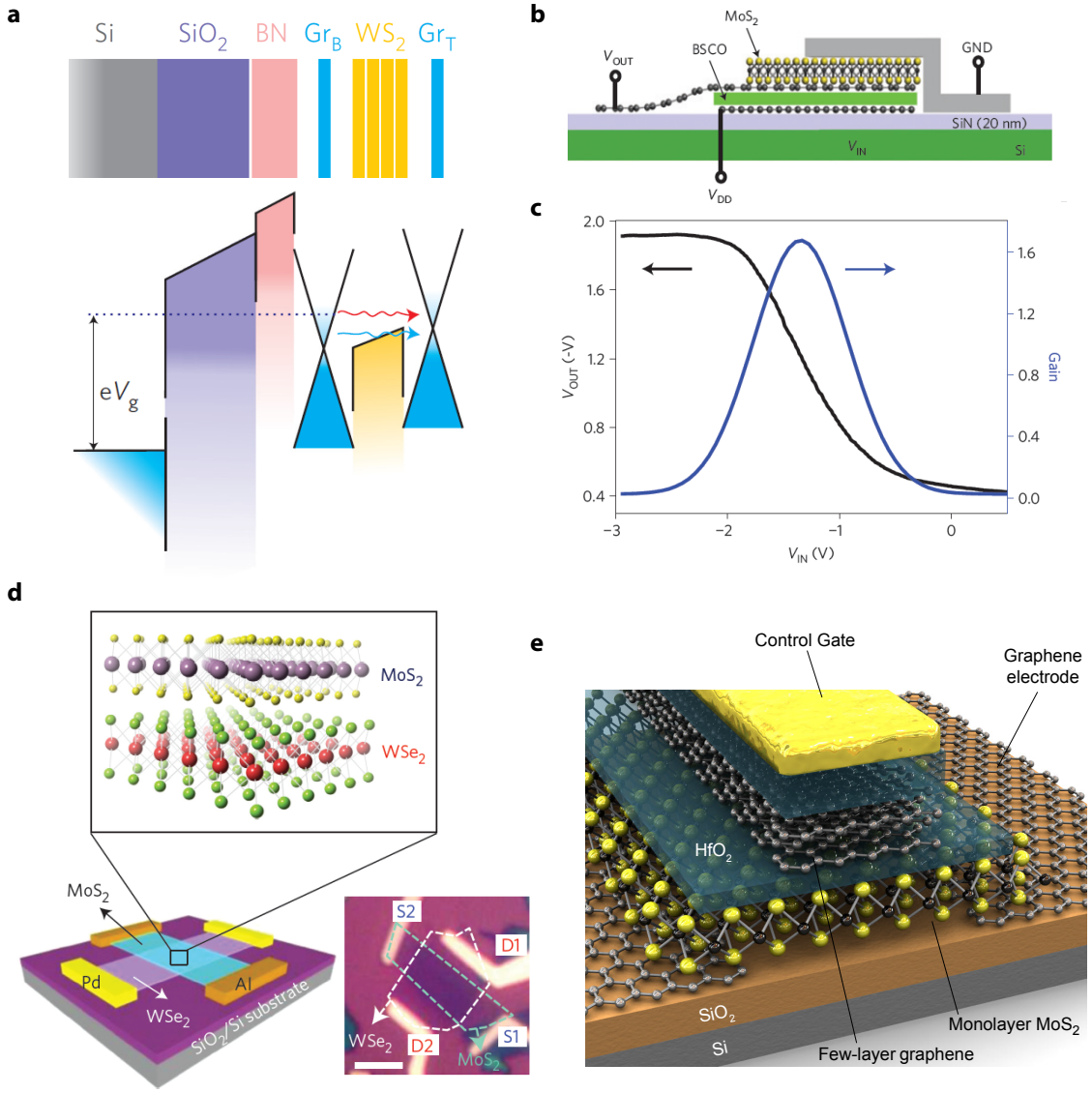

Figure 2.23: Devices based on heterostructures of monolayer MoS_2 and other 2D materials. a, Top: schematics of the architecture of the FETT based on vertical graphene heterostructures. As barrier layer, not only WS_2, but also MoS_2 and h-BN have been used. Bottom: band diagram of the heterostructure upon application of a positive voltage V_g to the Si gate. For sufficiently high V_g both thermionic (red arrow) and tunneling (blue arrow) currents flow through the barrier. **b,** Schematic cross-sectional view of the complementary logic inverter that incorporates a stack of n and p–type vertical FETs (see text). The input voltage V_{in} is applied to the Si gate and the supply voltage, $V_{DD} = -2$ V, to the bottom graphene layer. **c,** Output voltage V_{out} (black) and gain G (blue) as a function of V_{in}. **d,** Three-dimensional schematics (bottom left) and optical micrograph (bottom right) of the WSe_2/MoS_2 pn junction. The crystal structure of the hybrid bilayer is shown in the zoomed image (top). **f** Illustration of the memory device built using graphene/MoS_2 heterostructures as well as high-κ films of HfO_2. **a** is adapted with permission from ref. [163], © 2012 Nature Publishing Group. **b** and **c** are adapted with permission from ref. [164], © 2012 Nature Publishing Group. **d** is adapted with permission from ref. [165], © 2014 Nature Publishing Group. Image credit for **e**: Prof. Andras Kis.

between transparent graphene electrodes – was used to produce efficient photovoltaic devices (ref. [170]). Upon illumination, electrons and holes generated in the photoactive WS_2 layer, were separated by the built-in potential established by differently doped graphene electrodes. The solar cells were further integrated on flexible plastic substrates and showed an external quantum efficiency as high as 30%.

Complementary logic inverters. Another interesting example of device applications based on van-der-Waals heterostructures was reported by Yu *et al.* [164], who implemented n-type and p-type vertical FETs using graphene/MoS_2 and graphene/$Bi_2Sr_2Co_2O_8$ (BSCO) bilayer stacks, respectively. They assembled the two types of transistors in a multiheterostructure (figure 2.23b), which functioned as complementary logic inverter. The transfer characteristic (V_{out} *vs.* V_{in}) of the device and its gain G as a function of V_{in} are reported in figure 2.23c. It can be seen that G was greater than one (~ 1.7), proving that the developed technology is suitable for use in digital electronic circuits.

Atomically thin *pn* junctions. By assembling monolayers of MoS_2 (n-type) and WSe_2 (p-type), Lee *et al.* [165] recently demonstrated atomically thin pn junctions (figure 2.23d). The rectification of the current flowing between a pair of source (S) and drain (D) electrodes could be modulated by the voltage applied to the Si substrate, which served as gate electrode. The same devices showed as well gate-tunable photovoltaic response. These heterostructures represent the ultimate limit of pn junction scaling and, differently from common semiconductor rectifiers, they have no regions depleted from majority carriers. It was shown that, in the 2D limit, the current flowing through the device at forward bias was due to tunneling-mediated recombination of majority carriers across the van-der-Waals interface. The demonstration of a 2D pn junction added a new fundamental element to the list of components necessary for the realization of flexible (opto-)electronic devices based on the newly emerging class of 2D materials.

Memory cells. The development of an additional element of the list, i.e. a memory device, was carried out as a part of this doctoral research and is described in chapter 6, which includes the original report of the work (ref. [171]). It deals with a new type of nonvolatile memory cell that combines to advantage the high conductivity of graphene with the semiconducting properties of monolayer of MoS_2. It is based on vertical heterostructures of graphene and MoS_2, as well as thin films of high-κ HfO_2 grown by atomic layer deposition (ALD) on the surface of the 2D materials. The architecture of the device resembles that of a floating gate (FG) FET, where monolayer MoS_2 acts as ultrathin channel and a piece of multilayer graphene as FG, serving for the storage of information in the form of electrical charge. A three dimensional illustration of the memory cell is given in figure 2.23. On its side edges, monolayer MoS_2 overlaps two graphene sheets that serve for the injection/extraction of charge carriers. The MoS_2 channel and the graphene/MoS_2

heterostructures are covered with a thin "tunnel oxide" layer (HfO_2, 6 nm thick), on top of which lies the multilayer graphene FG. The latter is further capped by a thicker "control oxide" layer (HfO_2, 30 mn thick) and by a control gate electrode. The reader is referred to chapter 6 for a description of the various fabrication steps and of the working principle of the FG-FET. Hereafter, the reasons behind the conception of such device are presented, together with the advantages brought by 2D materials in the context of memory devices.
First, as in the case of conventional FETs, the use of a semiconducting material with sizeable energy gap and ultrathin form factor, helps limit the intensity of SCEs – more severe in FG-FETs – and enables further scaling of memory cells. Second, thanks to its small thickness, the few-layer graphene FG reduces parasitic capacitive couplings with neighboring cells. Third, the possibility to tune the bandgap of the semiconductor by a suitable choice of the TMD compound could offer the interesting possibility to engineer the tunneling barrier to improve the time-retention of the memory device (ref. [11]). Finally, the use of graphene as an electrode material represents a step forward towards the realization of all-2D memory devices to be integrated in flexible transparent electronics.
Indeed, 2D materials offer a complete new range of opportunities, which stimulates the creativity of researchers to conceive and demonstrate new types of devices. The memory cell built in this thesis is only one example of proof-of-concept device – among a large number reported in the literature – that aims to indicate a possible way to exploit the unique characteristics of 2D materials in real technological applications.

2.5 Contributions from this thesis

After providing the reader with a review of the physical properties of monolayer MoS_2 and its production methods, the latest advancements in the field of (opto-)electronic devices based on MoS_2 and related 2D materials were described. The goal of the chapter was to present the general context in which the research reported in this thesis has been developed.
It is worth mentioning that this doctoral work started in early 2011, i.e. soon after the demonstration of dual-gated single-layer MoS_2 transistors by Radisavljevic *et al.* [5]. Since then, several research groups worldwide started to work actively in the field of TMDs and in only few years, the knowledge of their properties expanded dramatically, together with the awareness of their strong technological potential.
In this rapidly evolving context, the contributions from this thesis regarded both the physical properties of monolayer MoS_2, as well as its device applications. On one side, they consisted in the measurement of the mechanical properties of ultrathin MoS_2 membranes (section 2.2.6); a collaboration with the group of Prof. Huili Xing (University of Notre Dame) led also to the first experimental evaluation of the material's thermal conductivity (section 2.2.5). On the other side, a contribution was given to the development 2D technologies by

showing that MoS_2 and graphene can be advantageously combined to build a nonvolatile memory cell (section 2.4.5).
Finally, the core work of this thesis lies in the middle between fundamental properties and applications, and concerns the study of charge transport in monolayer MoS_2 FETs that employ different gate dielectric materials (chapter 4). The objective of the research was to provide further knowledge on the mechanisms that affect the transport properties in actual devices, which is an essential step towards real technological products based on MoS_2 and 2D semiconductors.

3 Mechanical properties of ultrathin MoS_2

3.1 Stretching and breaking of ultrathin MoS_2

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Stretching and Breaking of Ultrathin MoS_2

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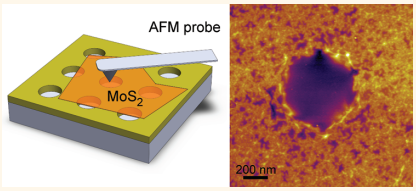
ABSTRACT



We report on measurements of the stiffness and breaking strength of monolayer MoS_2, a new semiconducting analogue of graphene. Single and bilayer MoS_2 is exfoliated from bulk and transferred to a substrate containing an array of microfabricated circular holes. The resulting suspended, free-standing membranes are deformed and eventually broken using an atomic force microscope. We find that the in-plane stiffness of monolayer MoS_2 is 180 ± 60 Nm^{-1}, corresponding to an effective Young's modulus of 270 ± 100 GPa, which is comparable to that of steel. Breaking occurs at an effective strain between 6 and 11% with the average breaking strength of 15 ± 3 Nm^{-1} (23 GPa). The strength of strongest monolayer membranes is 11% of its Young's modulus, corresponding to the upper theoretical limit which indicates that the material can be highly crystalline and almost defect-free. Our results show that monolayer MoS_2 could be suitable for a variety of applications such as reinforcing elements in composites and for fabrication of flexible electronic devices.

KEYWORDS: two-dimensional materials · dichalcogenides · MoS_2 · AFM · mechanical properties

Two-dimensional crystals, consisting of single or few atomic layers extracted from layered materials such as graphite or MoS_2,[1−3] are attracting a great deal of interest due to their promising potential for applications in nanotechnology. Graphene is the best known 2D material because of its high mobility, presence of massless Dirac fermions,[4,5] and a wealth of interesting physical phenomena such as the fractional quantum Hall effect.[6] Other 2D materials such as transition metal dichalcogenides or BN could have practical applications and fundamental properties complementary to those of graphene, although they are at this point much less explored.

Single-layer MoS_2 is a typical two-dimensional semiconductor from the class of layered transition metal dichalcogenides (TMD). Individual layers, 6.5 Å thick, can be extracted from bulk crystals using the micromechanical cleavage technique commonly associated with the production of graphene,[2,3] lithium-based intercalation,[7,8] or liquid phase exfoliation[9] and used as ready-made blocks for electronic device fabrication.[10] Bulk MoS_2 is an indirect gap semiconductor with a band gap of 1.2 eV (ref 11). Reducing the number of layers modifies the band structure and, as a consequence, monolayer MoS_2 becomes a direct gap semiconductor[12−15] with a band gap of 1.8 eV (ref 14) due to quantum confinement.[15] The presence of a band gap in monolayer MoS_2 makes it interesting for applications in nanoelectronics where it allows the fabrication of transistors with low power dissipation and current on/off ratios exceeding 10^8 at room temperature. Together with the possibility of large-scale liquid-based processing of MoS_2 and related 2D materials,[9] MoS_2 could also be very interesting for applications in flexible electronics where it would combine high performance with low cost. It is however not clear at this point if monolayer MoS_2 would be characterized by mechanical properties necessary for integration with stretchable polymer substrates in order to produce high-end bendable electronics.

Previous measurements on MoS_2 and WS_2 nanotubes,[16,17] which can be thought of as monolayers of MoS_2 and WS_2 wrapped up in the form of a cylinder, show superior mechanical properties with Young's modulus reaching 255 GPa and strength reaching 11% of its Young's modulus.[18,19] Subnanometer MoS_2 nanowires on the other hand have lower Young's modulus, 120 GPa.[20]

Here, we report on the measurement of the in-plane elastic modulus and breaking strength of single and bilayer MoS_2. MoS_2 consists of a stack of covalently bonded S−Mo−S layers weakly interacting with each other *via* van der Waals forces. The in-plane

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crystal structure is determined by polar covalent bonds resulting from the overlap between the 4d and 3p electron orbitals of molybdenum and sulfur. The in-plane stiffness (E^{2D}) of an ideal defect-free single-layer MoS_2 is related to the effective spring constant of these molecular bonds. A defect-free material would have the upper theoretical limit of the breaking strength ($\sigma_{max}^{2D} \approx 10\%$ of the Young's modulus).[21] We use nanoindentation in an atomic force microscope in order to perform nanomechanical measurements on ultrathin MoS_2 suspended over circular holes in patterned substrates, using a technique previously used for measurements on multilayer[22,23] and single-layer graphene.[24] Mechanical properties of graphene have also been probed by performing uniaxial measurements.[25,26]

RESULTS AND DISCUSSION

Single- and few-layer MoS_2 was extracted from bulk crystals of naturally occurring MoS_2 using the micromechanical cleavage technique commonly employed for the production of graphene.[1] We found that direct exfoliation on patterned substrates yielded a relatively small number of samples, presumably because of reduced adhesion between the substrate and MoS_2. We therefore employed a transfer technique[27] to first exfoliate MoS_2 on polymer films and then transfer the resulting material onto prepatterned surfaces. MoS_2 is first deposited on Si substrates covered with 270 nm SiO_2 on top of which polyvinyl alcohol (PVA) and polymethyl methacrylate (PMMA) films have previously been spin-coated. We have reported elsewhere[28] that this SiO_2 thickness results in optimal visibility of monolayer MoS_2. Once an interesting flake with an optical contrast corresponding to a monolayer is located using an optical microscope, AFM is used to verify the thickness. The sample is then immersed in water to dissolve the PVA film and release the PMMA layer which ends up floating on the water surface. The film is moved onto a pierced glass slide and aligned to the new substrate with the help of a micromanipulator. The new substrate consisted of a 270 nm thick SiO_2 (ref 28) patterned with 550 nm diameter holes defined by e-beam lithography followed by dry etching. Finally, the sample is kept in vacuum at 400 °C for 4 h in order to release the polymer film without the use of solvents that could break MoS_2 during drying. In this way, we obtain a relatively high yield of intact MoS_2 membranes suspended over circular holes. Figure 1a shows a monolayer flake after the transfer on the new substrate, while Figure 1b shows a corresponding AFM image of the sample topography. Resulting suspended ultrathin layers of MoS_2 are tightly clamped to the edges of the holes, without visible wrinkles or discontinuities.

Mechanical properties of the membranes were probed with indentation experiments[29] using an AFM (Asylum Research Cypher) with a standard silicon

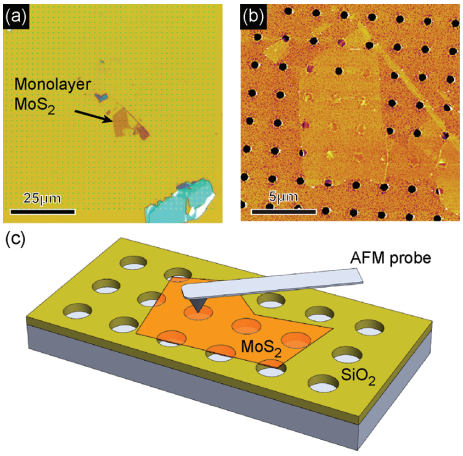

Figure 1. Sample preparation and the measurement method. (a) Optical image of a monolayer MoS_2 flake transferred onto the prepatterned SiO_2 substrate containing an array of circular holes 550 nm in diameter. (b) AFM image of the same single-layer MoS_2 as in part (a) shows that the monolayer is clean, free of wrinkles, and forms locally suspended membranes over multiple holes in the substrate. (c) Schematic depiction of the indentation experiment. During measurements, the AFM tip is placed above the center and slowly lowered while monitoring its deflection.

cantilever (Olympus AC240). Figure 1c shows the schematic depiction of the experiment. For each hole, an AFM topographical image of the suspended membrane was acquired in amplitude modulation mode and used to position the tip in the middle of the membrane; see Figure 2a.

Cantilever deflection is measured while the probe is moved in the vertical direction with a speed of 2 μm s^{-1}, resulting in controlled loading and unloading of the suspended MoS_2 membrane. Typical force *versus* piezo extension curves are shown on Figure 2d. Mechanical drift is minimized by means of a temperature controller integrated with the AFM system. Multiple curves with increasing indentation depths were acquired for each hole until mechanical failure was observed, as illustrated in Figure 2b. Mechanical failure typically occurs for vertical deflections <50 nm, well below the hole depth. No evidence of MoS_2 sheets sliding over the substrate was observed. The height profile in Figure 2c shows that the membrane adheres to the sidewalls of the hole over a distance on the order of 5 nm. This adhesion is due to van der Waals interaction and is presumably at the origin of the membrane pretensioning. Similar sidewall adhesion and pretension was reported in suspended graphene membranes.[24,30] SEM imaging was used to check tip quality, confirming that no damage occurred to the Si AFM tips during measurements. This observation is also supported by the fact that AFM image quality and measured results did not show any observable change during the experiment.

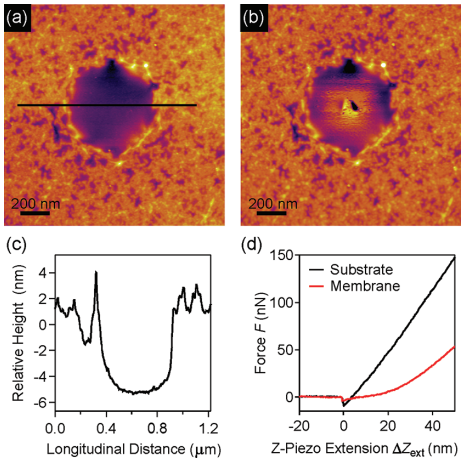

Figure 2. Suspended MoS_2 membranes and their mechanical failure. (a) AFM image of a monolayer MoS_2 flake suspended over a hole before the indentation experiment and (b) after it. A hole can be clearly seen in the center of the membrane at the location where the AFM tip punctured it. (c) Height profile of the section highlighted in (a) shows that the membrane adheres to the sidewalls over a vertical distance on the order of 5 nm, resulting in pretension between 0.02 and 0.1 Nm^{-1}. (d) Acquired force *versus* z-piezo extension curves for the suspended membrane and the substrate.

We performed experiments on a total of 9 monolayer (1 L) and 6 double-layer (2 L) MoS_2 membranes. A representative force *F versus* z-piezo extension (ΔZ_{ext}) curve for a monolayer membrane and the substrate is shown on Figure 2d. Loading and unloading curves in general overlap, indicating that no plastic deformation or membrane detachment occurs during the measurements and that the material can be considered as elastic.

The schematic diagram of the measurement geometry is given in Figure 3a. Because the measurement geometry (both tip and the sample) has circular symmetry and MoS_2 has six equivalent crystalline directions in terms of the stress-strain response, we model MoS_2 as an isotropic film characterized by Young's modulus E_Y, Poisson ratio ν and thickness h. Simulations on MoS_2 and measurements on WS_2 nanotubes[18,19] show that these materials related to monolayer MoS_2 are brittle and deform as materials with linear stress−strain relationship up to their failure. This is in stark contrast to carbon nanotubes or graphene where carbon atom chain formation and Stone-Wales transformations can lead to ductile behavior.[31] Such mechanisms are absent in MoS_2.[19] Because MoS_2 monolayers and nanotubes share the same type of chemical bonds, we also model MoS_2 as a linear elastic material.

The membrane is suspended over a circular hole with diameter $a = 2r = 550 \pm 10$ nm and deformed in the middle by an AFM tip with a radius $r_{tip} = 12 \pm 2$ nm. We suppose that the film is prestretched due to van der Waals adhesion between the film and the substrate leading to internal strain ε_0. Mechanical response of

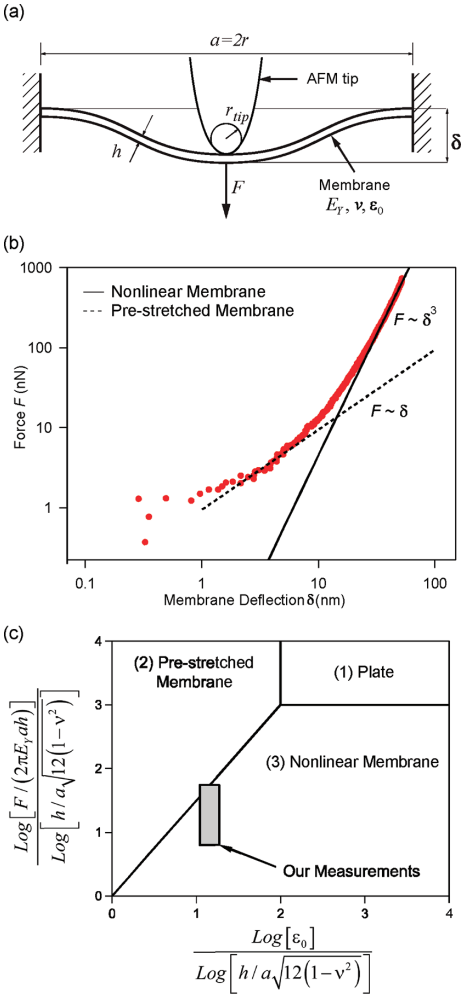

Figure 3. (a) Schematic diagram of the indentation test. A circular suspended membrane with Young's modulus E_Y, Poisson ratio ν, and prestrain ε_0 is elastically deformed in the middle by an AFM tip. The membrane is clamped at the edges and is loaded in the middle, resulting in membrane deflection δ. (b) Typical loading curve for a monolayer MoS_2 membrane. Small loads are characterized by a linear relationship between load *F* and deflection δ. For high loads, a cubic $F \sim \delta^3$ behavior dominates. (c) Parameter space according to Komaragiri *et al.*[32] delineating between different regimes of mechanical behavior for suspended circular membranes. The region in which our measurements are performed is shaded in gray.

such free-standing films can then fall into three distinct regimes, depending on the geometric factor h/a, applied load, and internal prestrain ε_0.[32] Linear plate bending and prestrained membrane deflection are characterized by linear force *versus* deflection behavior and are valid for small loads. Which one of these two governs the mechanical behavior depends on whether stiffness generated by prestrain is greater than the bending stiffness. The nonlinear membrane behavior

characterized by a cubic $F \sim \delta^3$ relationship dominates at large loads. In order to elucidate between these different deformation regimes, we plot a typical force–deflection curve in a logarithmic scale on Figure 3b. We can see that for small deflection and loading forces, limited by the resolution of our setup to ~1 nN, the curve follows a linear behavior (dashed line). For forces >10 nN, the curve starts to follow cubic behavior, typical of deformed membranes. We therefore fit the force–deflection data using a formula that captures both the linear behavior for small deformations and the cubic term for larger deformations:[32]

$$F = \sigma_0^{2D}\pi\delta + E^{2D}\frac{q^3\delta^3}{r^2} \quad (1)$$

where the cubic term containing the elastic modulus E^{2D} represents the modified form of the classical Schwerin solution for point loading of a circular membrane[33] valid for all values of the Poisson's ratio.[32] The term linear with deflection δ, where σ_0^{2D} is the prestress in the membrane, corresponds to the linear, prestretched membrane regime with an internal strain of ε_0.

Finite element simulations by Lee *et al.*[24] showed that this model can be applied to small and finite sized indenters as long as $r_{tip} \ll r$. We extract the tip radius r_{tip} ~ 12 nm from SEM images, resulting in $r_{tip}/r = 0.05$ in our case. The dimensionless constant q is related to the Poisson ratio ν as $q = 1/(1.05 - 0.15\nu - 0.16\nu^2) = 0.95$, where $\nu = 0.27$ is the Poisson ratio of bulk MoS_2.[34] The map of possible regimes of film response according to Komaragiri *et al.*[32] is presented on Figure 3c, together with the range of range of tests covered in this paper, confirming that most of the mechanical response that we record is expected to be in the region described by the cubic $F \sim \delta^3$ behavior.

Figure 4 shows representative experimental force–deflection curves acquired for mono- and bilayer MoS_2. From a least-squares fit of the experimental curves with the eq 1, we can extract the pretension σ_0^{2D} and the membrane elastic modulus E^{2D}. The fit agrees well with experimental data, validating our assumptions that led to the choice of eq 1 as the model. For a total of 9 monolayers (1 L), we obtain the average value for the elastic modulus E^{2D} of 180 ± 60 Nm^{-1} (Figure 5, left) and prestress σ_0^{2D} in the 0.02 to 0.1 Nm^{-1} range. Throughout the paper, the experimental uncertainty for the measured values of the elastic modulus and the breaking strength corresponds to the standard deviation of experimental values. Assuming an effective monolayer thickness of 0.65 nm, we obtain for the Young's modulus E_{Young} = 270 ± 100 GPa, close to the Young's modulus of MoS_2 nanotubes (230 GPa, ref 18), bulk MoS_2 (238 GPa, ref 34), or steel (210 GPa, ref 35). The elastic modulus of bilayer MoS_2 is 260 ± 70 Nm^{-1}, which corresponds to a lower Young's modulus of 200 ± 60 GPa, possibly due to defects or interlayer sliding.

During nanomechanical measurements, suspended membranes are deformed up to their mechanical failure, denoted by the symbol × in Figure 4, typically occurring for fracture forces of $F_{max} \approx$ 200 nN and

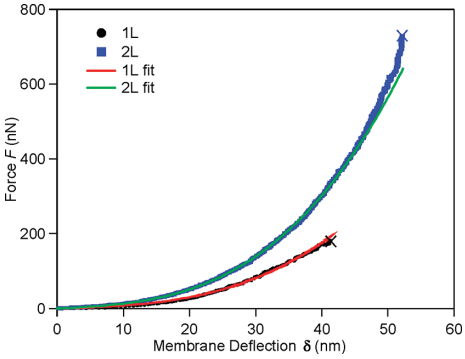

Figure 4. Examples of loading curves for single and bilayer MoS_2 and the least-squares fit of the experimental indentation curves to the eq 1. The fitting allows us to extract the pretension of the membrane σ_0^{2D} and its Young modulus E^{2D}. Experimental and fitted curves show good agreement. Membranes are fractured at the point marked by the symbol ×.

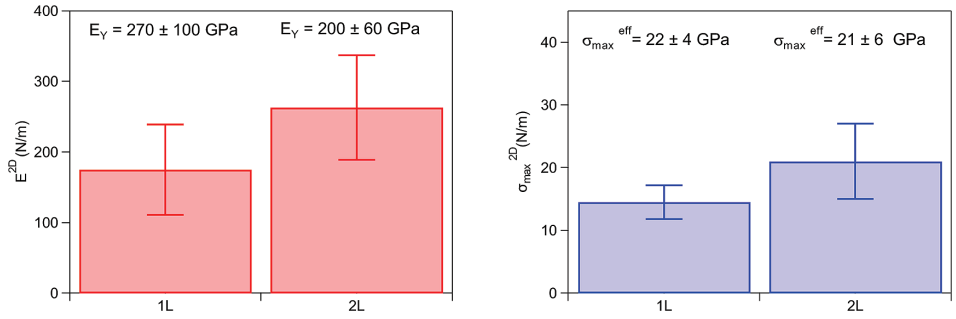

Figure 5. (Left) Young's modulus E^{2D} and (right) maximum breaking stress σ_{max}^{2D} at the central point of the film for 1 L and 2 L MoS_2 flakes extracted from the experimental data. The corresponding effective bulk modulus assuming a monolayer flake thickness of 6.5 Å is also shown for comparison with the bulk material.

TABLE 1. Comparison of Young's Moduli and Breaking Strengths for Several Engineering Materials, Including Monolayer MoS_2[19,24,34,35,39–43]

material	Young's modulus E_{Young} (GPa)	breaking strength σ_{max}^{eff} (GPa)	breaking strength/Young's modulus (%)
stainless steel ASTM-A514	205	0.9	0.4
molybdenum	329	0.5–1.2	0.15–0.36
polyimide	2.5	0.231	9
PDMS	0.3–0.87	2.24	2.5
Kevlar 49	112	3	2.6
monolayer MoS_2	270	16–30	6–11
bulk MoS_2	238		
WS_2 nanotubes	152	3.7–16.3	2.4–10
carbon nanotubes	1000	11–63	1.1–6.3
graphene	1000	130	13

deflections ≈50 nm. For such extreme deformation, in addition to large-scale deformation, the membrane is locally indented within a typical area extending $\sim 2r_{tip}$ distance from the center.[32] Here, the local curvature of the membrane is constrained by the tip diameter of the AFM probe, as long as the membrane is allowed to deform smoothly onto the indenter. Our experiment falls in the limit of small indenters characterized by $r_{tip}/r \ll 1$ ($r_{tip}/r = 0.05$ in our case) and large loads with respect to pretension, characterized by a factor $\kappa \ll 1$ defined as[36]

$$\kappa = \left(\frac{\sigma_0}{E_Y}\right)^{1/3}\left(\frac{2r_{tip}}{r}\right)^{2/3} \quad (2)$$

In our case, $\kappa < 0.02$. Here, we can extract the maximum stress at the central, protruding part of the film σ_{max}^{2D} using the expression for the indentation of a linearly elastic membrane by a spherical indenter in the limit of large load:[36]

$$\sigma_{max}^{2D} = \sqrt{\frac{F_{max}E^{2D}}{4\pi r_{tip}}} \quad (3)$$

The averages of maximum stress values for 1 L and 2 L-MoS_2 membranes are 15 ± 3 and 28 ± 8 Nm^{-1}, respectively (corresponding to 22 ± 4 GPa for a monolayer and 21 ± 6 GPa for a bilayer), as reported in Figure 4. On the average, these correspond to 8 and 10% of the Young's modulus for monolayer and bilayer MoS_2. The strength of individual MoS_2 monolayers is between 6 and 11% of their Young's modulus. These values are at the theoretical upper limit of a material's breaking strength and thus represent the intrinsic strength of interatomic bonds in MoS_2. This exceptionally high strength indicates that MoS_2 membranes are mostly defect-free. To put these high values of breaking strength and Young's modulus in perspective, we can compare them to several common engineering materials in Table 1. The strength of monolayer MoS_2 is exceeded only by carbon nanotubes and graphene. Even though MoS_2 has a smaller Young's modulus and strength than graphene, the absolute 2D elastic modulus E^{2D} and strength σ_{max}^{2D} of monolayer MoS_2 are smaller than those of graphene only by a factor of ~2.

In order to investigate if MoS_2 could be suitable for integration with flexible materials, for example, in flexible electronic circuits, it is necessary to quantify the membrane strain at the breaking point, ε_{int}, and compare it to the breaking strain of standard flexible substrates. Assuming a linear relationship between stress and strain $\sigma = E\varepsilon$ leads to an internal stress at failure $\varepsilon_{int} \sim 0.06–0.11$.

In comparison, thin polymer films such as polyimide (PI) or polydimethylsiloxane (PDMS), commonly used as substrates for flexible electronics, break at a strain of ~7% (ref 37), which is smaller than the aforementioned value extracted for single-layer MoS_2. This suggests that 2D MoS_2 can be readily integrated with PI or PDMS substrates for use in flexible electronics.

CONCLUSIONS

Our results show that monolayer MoS_2 is a flexible and strong material with a high Young's modulus, comparable to stainless steel. The measured strength of monolayer MoS_2 is close to the theoretical intrinsic strength of the Mo–S chemical bond, indicating that the monolayer is mostly free of defects and dislocations capable of reducing mechanical strength. As MoS_2 can be readily dispersed in a wide variety of solvents,[9] our finding indicates that MoS_2 could be interesting as a reinforcing element in composites. The presence of sulfur in MoS_2 could furthermore allow easy functionalization and efficient load transfer between MoS_2 and the composite matrix.

We also find that the exceptional mechanical properties of monolayer MoS_2 make it suitable for incorporation into flexible electronic devices where commonly used substrates such a PI would undergo mechanical failure at a smaller deformation than MoS_2.

MATERIALS AND METHODS

Single layers of MoS_2 are exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide) using the scotch-tape micromechanical cleavage technique pioneered for the production of graphene.[1] Monolayer and few-layer MoS_2 was first deposited on a silicon substrate with 270 nm thick SiO_2 that has previously been coated with polyvinyl alcohol (Sigma-Aldrich) and polymethyl methacrylate (PMMA, Microchem Corp). The PMMA film is released by dissolving PVA in water and transferred on top of a prepatterned SiO_2 substrate. After transfer, PMMA is removed by heating the

sample in a vacuum furnace at 400 °C for 4 h. AFM imaging and indentation experiment was performed using the Asylum Research Cypher AFM equipped with the air temperature controller for minimizing drift and using Olympus AC240 silicon cantilevers. AFM probe spring constants were calibrated using the thermal method.[38]

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Supporting Information Available: SEM images of atomic force microscope probes. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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3.2 Comments on ACS Nano 5 (12), p. 9703, 2011

The paper presents the first experimental investigation of the in-plane stiffness and breaking strength of mono- and bilayer sheets of MoS_2. To the best of our knowledge, this is also the first measurement of the mechanical properties of a truly 2D system beyond graphene. The latter was investigated in 2008 by Lee *et al.* (ref. [110]), who performed AFM nanoindentation experiments on 2D membranes prepared by direct exfoliation (scotch tape method) of graphene sheets on perforated Si substrates. The fabrication of similar membranes using 2D TMDs is made challenging by the relatively small lateral size and low yield of monolayer flakes, which hamper the production of free-standing membranes by direct exfoliation. The paper describes an alternative approach based on the use of transfer techniques (appendix B). Monolayer MoS_2 sheets are first exfoliated on a conventional SiO_2/Si substrate and then transferred with a polymer-based method onto a new substrate prepatterned with circular holes. The polymer can then be removed by thermal annealing (400 °C) in a vacuum furnace, resulting in a high yield of suspended MoS_2 membranes. The use of this method enabled performing nanoindentation measurements on a total of 9 mono- and 6 bilayer MoS_2 membranes. It is worth mentioning that the experiments were carried out in 2011, when the techniques for the large-area growth of MoS_2 just started being developed and no publications were available yet. Nowadays, similar measurements could be easily performed on CVD grown monolayer MoS_2 (section 2.3.2). In this context, such experiments could also provide an insight into the influence of defects (e.g. grain boundaries and dislocations) on the mechanical properties of the CVD material. Recently, Liu *et al.* [172] reported nanoindentation measurements on CVD monolayer MoS_2. They extracted a 2D Young's modulus of ~ 170 N/m, which is close to the value reported in this thesis for the exfoliated material (~ 180 N/m). However, to the best of our knowledge, experimental data on the breaking strength of monolayer CVD MoS_2 have not yet been reported.

The paper provides a clear answer to the question introduced in section 1.1, i.e. whether monolayer MoS_2 is suitable for incorporation into flexible electronic devices. The experiments showed evidence that atomically thin sheets of MoS_2 are strong and stiff, and are highly suitable for the envisioned flexible applications. In fact, the Young's modulus of monolayer MoS_2 is ~ 270 GPa, which is even larger than that of stainless steel (E ~ 205 GPa). The breaking strength of the strongest MoS_2 membrane (σ_{max} ~ 30 GPa) corresponds to 11% of the Young's modulus, which is the ideal value predicted by Griffith [109] for a defect-free material (section 2.2.6). Finally, the maximum internal strain at rupture is ~ 11%. This value is higher than the breaking strength of the common substrate materials used in flexible electronics, such as polyimide. The latter typically breaks at an internal strain of the order of 7%. This proves that monolayer MoS_2 does not introduce additional mechanical constraints and can be easily integrated on flexible plastic substrates.

The results reported in the paper have been subsequently confirmed by different experimental and theoretical works. The reader is referred to section 2.2.6 for a review on the nanoindentation method and on follow-up studies on the mechanical properties of monolayer MoS_2.

4 Charge transport properties of monolayer MoS_2

4.1 Introduction

The charge transport properties of monolayer MoS_2 and other 2D TMDs have attracted significant research interest after the demonstration, in 2011, of the first switchable single-layer MoS_2 FET (section 2.4.1). Since then, a number of experimental and theoretical works have been carried out to investigate the transport phenomena occurring in these atomically thin semiconductors. A strong focus has been given to the charge carrier mobility, since it represents a critical material property that determines in large extent the performance of semiconductor devices.
Research on charge transport is essential to understand the causes of mobility degradation and helps identify strategies for the improvement of mobility up to the intrinsic theoretical limit. In case of monolayer MoS_2, all the mobility values obtained so far from experiments are remarkably lower than the intrinsic limit. This observation suggests that several sources of charge scattering, internal to MoS_2 or in the external surrounding environment, are present in all the investigated samples and dominate the overall transport properties. In this scenario, it is necessary to identify the detrimental sources of scattering, as well as to develop techniques to remove or limit their influences. In particular, in FETs (section 2.4.1) it is crucial to choose a gate dielectric material that does not degrade the intrinsic charge carrier mobility, due to impurities, roughness or remote phonons. The identification of ideal dielectrics for use in monolayer MoS_2 FETs was one of the main objectives of this doctoral research, which explored the charge transport properties of monolayer MoS_2 at the interface with various dielectric materials.

The chapter is organized as follows. The first section introduces the fundamental concepts related to charge transport in MoS_2; it will provide the reader with the list of intrinsic and extrinsic scattering mechanisms that limit the charge carrier mobility of this 2D semiconductor. Section 4.3 will focus more specifically on the intrinsic transport properties

of monolayer MoS_2 – as evaluated from first-principles calculations – whereas section 4.4 will describe its extrinsic transport properties – as obtained from experiments on field-effect devices. The different extrinsic sources of scattering, both internal and external to MoS_2, will be reviewed in section 4.4.

4.2 Charge scattering and mobility in MoS_2

For harnessing the potential of 2D semiconductors in electronic devices, a detailed knowledge is required of the scattering mechanisms that limit the charge carrier mobility. The latter is a crucial parameter for applications, as it indicates how quickly electrons or holes can move in the presence of an electric field. By the definition, the charge carrier mobility μ is given by

$$\mu = \frac{v_d}{E} \tag{4.1}$$

where v_d is the average drift velocity acquired by the carriers under the driving force of an electric field E. The mobility is related to the frequency of the scattering events through which carriers lose momentum and can be expressed as

$$\mu = e \cdot \frac{\tau}{m^*} \tag{4.2}$$

where e is the electron charge, τ is the average time between consecutive scattering events (relaxation time) and m^* is the effective mass of electrons or holes. Inside a material, the charge carriers interact with a number of scatterers, among which intrinsic lattice phonons, impurities, defects, and several others. The intensity of the different scattering mechanisms vary significantly with temperature T, so that measuring μ as a function of T is often carried out to identify the contributions from the different types of scatterers.
In the 1960's, Fivaz and Moser [21] investigated the transport properties of several bulk samples of MoS_2 and measured the T-dependence of μ in the range from 100 to 700 K (figure 4.1a). All the crystals of MoS_2 showed n-type unipolar transport along the direction perpendicular to the c-axis, so that only the in-plane electron mobility could be evaluated. Above 200 K, the latter could be described by the following equation

$$\mu = \mu_0 \cdot (\frac{T}{T_0})^{-\gamma} \tag{4.3}$$

where $\mu_0 = 100$ cm^2/Vs, $T_0 = 300$ K and $\gamma = 2.6$. The average RT electron mobility was therefore ~ 100 cm^2/Vs, i.e. about one order of magnitude smaller than in moderately doped bulk Si (ref. [148]). Theoretical models allowed understanding that, at sufficiently high T, the mobility of electrons within the planes was dominated by scattering from the

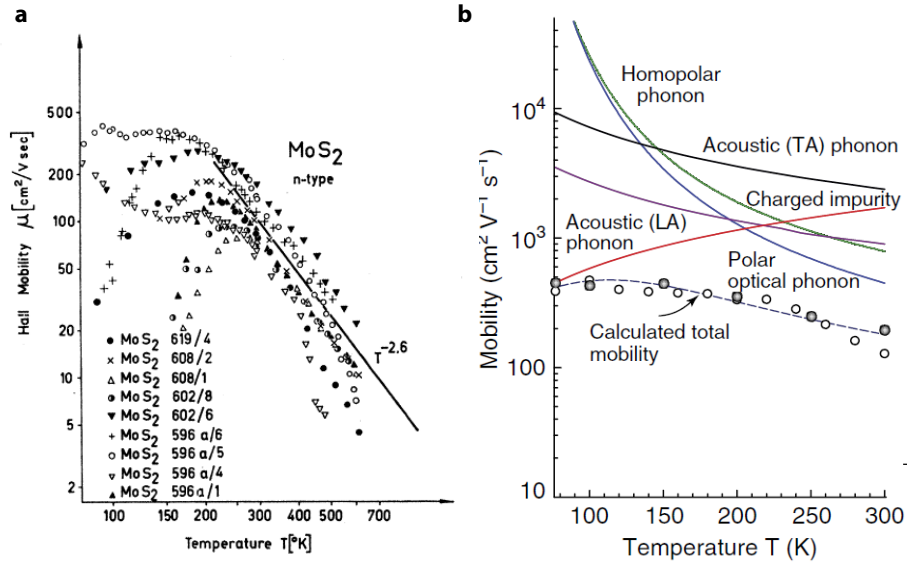

Figure 4.1: Temperature-dependent mobility in bulk and multilayer MoS_2. **a,** Temperature dependence of the electron mobility in several bulk MoS_2 samples, as obtained from Hall effect measurements by Fivaz and Moser. **b,** Temperature-dependent mobility as measured by Kim *et al.* [173] (white circles) and by Fivaz and Moser [21] (gray circles). The blue dashed line represents the total mobility calculated from a theoretical model. The solid lines are computed assuming exclusively one type of scattering mechanism. **a** is adapted with permission from ref. [21], © 1967 American Physical Society. **b** is adapted with permission from ref. [173], © 2012 Nature Publishing Group.

lattice optical phonons. The measured temperature damping parameter, γ, could be used in combination with models to identify the most relevant phonon modes involved in the scattering. It was found that the most detrimental phonon mode was the out-of-plane homopolar A_{1g} (section 2.2.4) mode, resulting in a significant deformation potential. At low temperature ($T < 200$ K), the electron mobility was instead dominated by other scatterers, such as acoustic phonons and charged impurities.

In 2012, Kim *et al.* [173] measured the T-dependent mobility of multilayer MoS_2 sheets (20-80 nm thick), in the range from 80 to 300 K, and obtained results very similar to those by Fivaz and Moser, as shown in figure 4.3b. Calculations based on theoretical models were also performed to evaluate the total electron mobility (dashed line) limited by different scattering mechanisms. This could be calculated using Matthiessen's rule

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{hom}}} + \frac{1}{\mu_{\text{pol}}} + \frac{1}{\mu_{\text{a-l}}} + \frac{1}{\mu_{\text{a-t}}} + \frac{1}{\mu_{\text{imp}}} \tag{4.4}$$

where μ_{hom} is the mobility in the presence of homopolar optical phonons; equivalently, μ_{pol} is related to polar optical phonons, $\mu_{\text{a-l/t}}$ to acoustic phonons (longitudinal or transversal) and μ_{imp} to impurities. The "partial mobilities" are plotted as solid lines in figure 4.3b. It can be seen that at high T, optical phonons dominate, whereas at low T, charged impu-

rities set the upper mobility limit. A fair agreement was obtained between experimental and theoretical mobility values, which supported the validity of the model.
As the thickness of MoS_2 is decreased, the surface-to-volume ratio of the material increases, together with its sensitivity to external perturbations. 2D crystals, such as monolayer MoS_2, offer the ultimate limit of surface sensitivity, which is a real advantage for the realization of sensors (e.g. ref. [174]), but requires critical attention during design and fabrication of electronic devices. In fact, these ultrathin materials can be also highly sensitive to detrimental sources of scattering present in their surrounding environment. In FETs, the latter coincides with the substrate and gate dielectric material, which need to be properly chosen and optimized in order not to degrade the electron mobility.
Figure 4.2 shows the list of scattering mechanisms that influence the mobility of monolayer MoS_2 and includes also those sources of scattering that are commonly present in practical

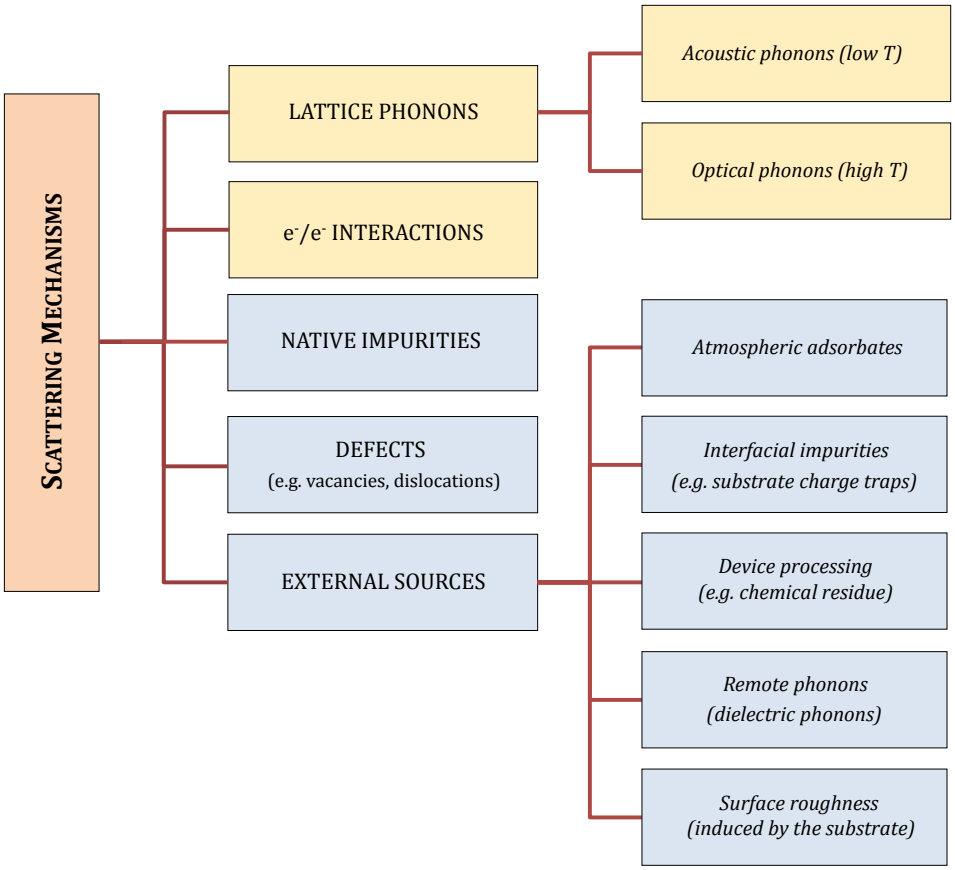

Figure 4.2: Charge scattering in monolayer MoS_2 at the interface with dielectric materials. Diagram of the scattering mechanisms that affect the electron mobility in monolayer MoS_2. The list includes intrinsic (yellow) and extrinsic (blue) sources of scattering. The first are present even in a perfect and isolated material. The second can in principle be eliminated; they include also external influences due the substrate, gate dielectric material, device processing and gaseous adsorbates.

devices, where MoS_2 typically lies on the surface of a dielectric substrate. Intrinsic scatterers (yellow), such as optical and acoustic lattice phonons, will be described in section 4.3, which deals with the intrinsic transport properties of monolayer MoS_2. For reasons of completeness, electron-electron (e^-/e^-) interactions are included in the list, but they do not represent a major influence to charge transport in the range of carrier density at which FETs typically operate ($10^{11} - 10^{13}$ cm^{-2}). Electron-electron scattering is expected to play an important role for carrier densities larger than 10^{13} cm^{-2} [89, 175]. The other scattering mechanisms (blue) are considered as extrinsic, in the sense that they could in principle be eliminated from the system, for example through an optimized growth process or through a careful design/fabrication of the device. Among them, there are defects (e.g. sulfur vacancies and grain boundaries) and impurities internal to monolayer MoS_2, as well as a number of external influences due the substrate, gate dielectric material, device processing and gaseous adsorbates. The experimental transport properties and the influence of these extrinsic sources will be discussed in sections 4.4 and 4.5, respectively.

4.3 Intrinsic transport properties of monolayer MoS_2

The intrinsic transport properties of monolayer MoS_2 are determined by the scattering of charge carriers with lattice phonons. The intrinsic mobility limits can be calculated from the knowledge of the electronic and phononic band structures, whose characteristics have been outlined in section 2.2. Kaasbjerg *et al.* performed first-principles calculations of the electron-phonon couplings and evaluated the phonon-limited electron mobility at high temperature ($T > 100$ K) [89]. It was found that the upper theoretical limit was set by optical phonon scattering, similarly to the case of bulk MoS_2 [21]. However, not only the homopolar A_1' mode, but also the longitudinal polar E' mode plays a significant role *via* the Frölich interaction. For monolayer MoS_2, the intrinsic mobility can be expressed again with equation 4.3, but the temperature damping parameter assumes a value of 1.69, which is smaller than in the bulk ($\gamma \sim 2.6$). It is interesting to notice that the model by Fivaz and Moser predicted

$$\gamma_{\text{pol}} \simeq \gamma_{\text{hom}} - 1 \tag{4.5}$$

where γ_{pol} and γ_{hom} are the temperature damping factors if the mobility is dominated by polar and homopolar phonons, respectively. The lower value of γ in the monolayer compared to the bulk is likely due to the different dominating phonon scattering, which includes significant contributions from polar phonons in the case of the monolayer. The observed change in electron-phonon coupling could be a consequence of the indirect-to-direct bandgap transition, which shifts the conduction band minima from the Γ point (bulk) to the K point (monolayer) of the Brillouin zone (section 2.2.2).

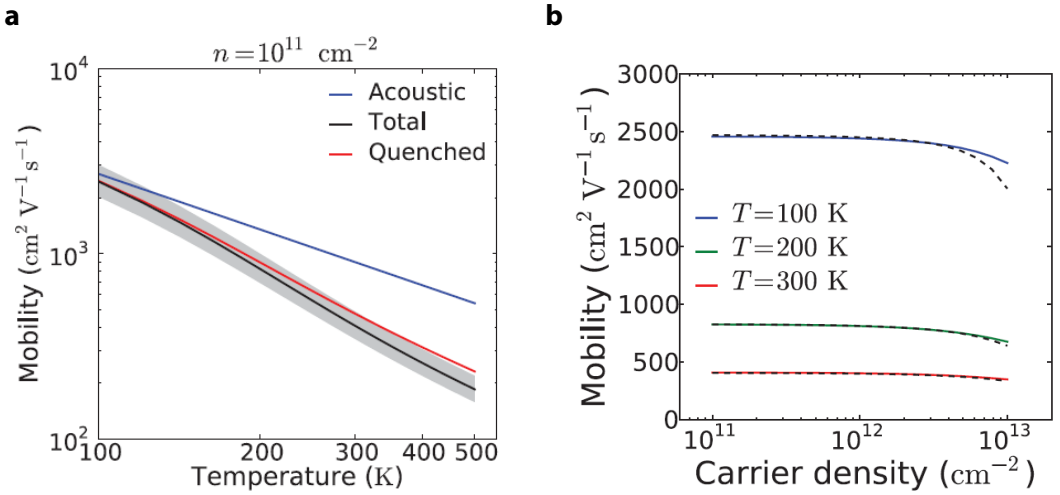

Figure 4.3: Intrinsic phonon-limited mobility of monolayer MoS_2 for $T > 100$ K. a, Mobility *vs.* temperature curves in the case of only acoustic phonon (blue), acoustic and optical phonons (black), quenched homopolar mode (red), as discussed in the main text. The shaded area (gray) shows the variation in the mobility associated with 10% uncertainty in the calculated deformation potentials. **b,** Mobility as a function of charge carrier density at different temperatures. Dashed lines represent calculations carried out using Boltzmann distribution (non-degenerate electrons) and relaxation time approximation. **a** and **b** are adapted with permission from ref. [89], © 2012 American Physical Society.

The theoretical T-dependence of the electron mobility is reported in figure 4.3a for three different cases. The total mobility (black) is calculated by taking into account all scattering mechanisms, including the optical phonons. When the latter are removed, the resulting curve (blue) corresponds to the acoustic phonon limited mobility, characterized by $\gamma = 1$. Finally, the red μ *vs.* T curve is computed by assuming that the homopolar mode is quenched, which is expected to be the case when the surface of monolayer MoS_2 is encapsulated in dielectric materials. The choice was motivated by the contemporary demonstration of dual-gated FETs (section 2.4.1), which showed a remarkable improvement in mobility after encapsulation with a high$-\kappa$ oxide. It was found that the quenching mechanism reduced the temperature damping parameter compared to that of the total mobility (1.52 *vs.* 1.69) and increased the RT mobility of about ~ 70 cm^2/Vs.

Figure 4.3b shows the electron mobility as a function of charge carrier density n, at three different temperatures (100, 200 and 300 K). It can be seen that μ is weakly dependent on n and due to phonon scattering it decreases from ~ 2450 cm^2/Vs to ~ 400 cm^2/Vs as T is increased from 100 to 300 K. The theoretical intrinsic limit at RT for $n = 10^{11}$ cm^{-2} was calculated to be 410 cm^2/Vs, which is often cited in the literature as a reference value for the highest achievable mobility in monolayer MoS_2. This relatively low limit, which is comparable to the mobility of holes in bulk Si [148], corresponds to an intrinsic mean free path $\lambda \sim 14$ nm [89].

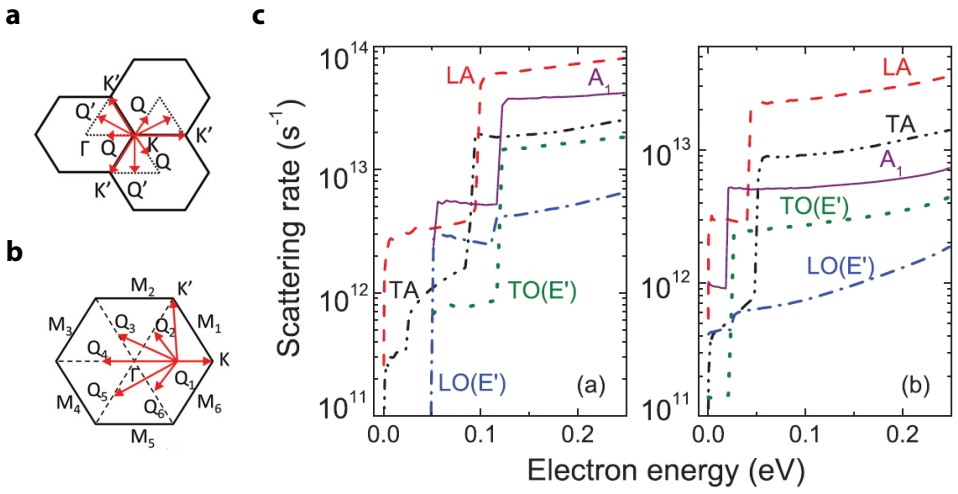

Figure 4.4: Phonon scattering in monolayer MoS_2 with *Q*-*K* intervalley transitions. **a**,**b**, Schematics of the intervalley transitions for electrons in K and Q valleys, respectively. **c**, Phonon scattering rates calculated at RT for electrons in the K valleys *via* emission (left) and adsorption (right) of phonons. The wave vector $\vec{k}$ of the initial electron state is assumed to be oriented along the $\Gamma - K$ direction. **a**, **b** and **c** are adapted with permission from ref. [60], © 2013 American Physical Society.

More recently, Li *et al.* [60] showed that the RT intrinsic limit of the electron mobility can be even lower, namely ~ 130 cm^2/Vs. They calculated the electronic band structure within the DFT formalism and found that the distance in energy between the K and Q valley Δ_{Q-K} (section 2.2.2) was as low as 70 meV, in contrast with the calculations by Kaasbjerg *et al.*, who found $\Delta_{Q-K} = 200$ meV and therefore did not take into account the Q states. On the other hand, Li *et al.* included these states in their calculations and obtained significantly higher scattering rates. In fact, the proximity in energy between the K and Q valleys opens additional channels for the intervalley electron-phonon scattering. For example, electrons in the K valleys can be scattered not only to the K', but also to the Q and Q' valleys, as indicated by the red arrows in figure 4.4a. Similarly, electrons in Q can be scattered to the surrounding Q and K valleys (figure 4.4b). To show the effects of the extra $Q - K$ intervalley transitions, the RT electron-phonon scattering rates are reported as a function of electron energy in figure 4.4c, for the case of K-electrons interacting with the most relevant acoustic and optical phonons. Some of the step-like changes observable in these curves can be ascribed to the onset of intervalley transitions at precise energies. It can be seen that the acoustic phonons are dominant scatterers, with the longitudinal acoustic mode (LA) mode providing the highest scattering rate. A Monte Carlo simulation based on Boltzmann equation was carried out using the calculated scattering rates, in order to extract the dependence of the carrier drift velocity on the applied electric field and extract the electron mobility. The latter was evaluated to be 1900 cm^2/Vs at 100 K and 130 cm^2/Vs at 300 K. Furthermore, it was found that at high electric fields, the carrier

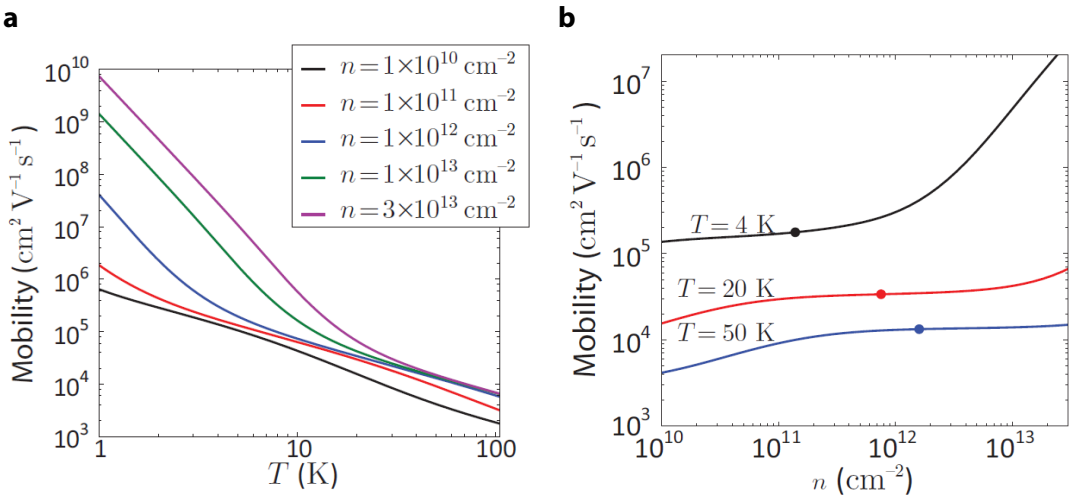

Figure 4.5: Acoustic phonon limited mobility of monolayer MoS_2 for $T < 100$ K. a, Acoustic phonon limited mobility as a function of temperature for different carrier densities. **b,** Mobility as a function of carrier density at different temperatures. The dots mark the quantum-classical crossover from a non-degenerate to a degenerate carrier distribution. **a** and **b** are adapted with permission from ref. [177], © 2013 American Physical Society.

velocity saturated at $\sim 3.4\times10^6$ cm/s at RT, which is approximately one order of magnitude smaller than the RT saturation velocity in graphene [176].

It is worth noting that these results are sensitive to the energy difference Δ_{Q-K} between the Q and K valleys, whose value has been reported to vary between 50 meV and 200 meV, due to different techniques and approximations used in calculations [61, 89]. If a large value of Δ_{Q-K} is assumed (e.g. 200 meV), then the effect of the Q valleys can be neglected. Under this condition, the simulations by Li *et al.* provide a higher RT intrinsic mobility of $\sim$ 320 cm^2/Vs. It was also pointed out that at high carrier density ($n \gtrsim 10^{13}$ cm^{-2}), the screening from degenerate electrons could significantly lower the scattering rates in 2D MoS_2. This would lead to a much more optimistic estimate of the intrinsic mobility, with values exceeding 1000 cm^2/Vs at RT [147].

In a subsequent work, Kaasbjerg *et al.* [177] investigated the intrinsic transport properties of monolayer MoS_2 at low temperature ($T < 100$ K), where the optical phonons are suppressed and only the acoustic phonon modes are excited. In particular, they studied the scattering of electrons by longitudinal (LA) and transverse (TA) acoustic phonons through deformation potential as well as piezoelectric interaction, which occurs in monolayer MoS_2 as a consequence of its non-centrosymmetric crystal structure (section 2.2.1). Calculations were performed to evaluate the acoustic phonon limited mobility (figure 4.5) taking into account the screening by free electrons, which is expected to be relevant at low T, where the transition from non-degenerate to degenerate electrons (marked by dots in figure 4.5b) occurs at lower carrier densities, of the order of 10^{11} cm^{-2} at $T = 4$ K.

A set of calculated μ *vs.* T curves is reported in figure 4.5a. The acoustic phonon limited

mobility follows a power law, $\mu \propto T^{-\gamma}$, where the temperature damping parameter assumes different values ($\gamma = 1-4$) depending on temperature range, carrier density and dominant scattering mechanism. For $T \lesssim 10$ K the mobility exceeds 10^5 cm^2/Vs, whereas at $T = 100$ K it lies within the range $10^3 - 10^4$ cm^2/Vs. The dependence of μ on carrier density n is displayed in figure 4.5b for three different temperatures, namely 4, 20 and 50 K. The mobility increases monotonically with n and its rate of increase becomes larger at high n and low T due to the onset free-carrier screening. It was fount that, above the non-degenerate to degenerate transition (marked by dots), μ is dominated primarily by the deformation potential of the TA phonons, which is not screened as efficiently as the LA deformation potential and the LA/TA piezoelectric interaction.
The goal of this section was to present the intrinsic limits to the high- and low-temperature electron mobility of monolayer MoS_2. It was seen that the mobility of non-degenerate electrons is expected to be lower than $130-410$ cm^2/Vs at RT, whereas it can exceed 10^5 cm^2/Vs for $T < 10$ K. These values represent a valuable reference to be used for the analysis of experimental results. They should serve as well for evaluating the influence of the extrinsic sources of scattering.

4.4 Extrinsic transport properties of monolayer MoS_2

In 2004-2005, Novselov *et al.* [2] carried out an experimental investigation of the transport properties of a number of 2D crystals, which were mechanically exfoliated from the bulk and deposited on oxidized Si substrates. Among these materials, they investigated also monolayer MoS_2, which was found to be a heavily doped n-type semiconductor with RT mobility ranging between 0.5 and 3 cm^2/Vs. The remarkable discrepancy between these experimental results and the aforementioned theoretical limits is a sign for the presence of a large amount of extrinsic sources of scattering. The observed high level of doping further suggests the existence of a high density of defects/impurities that could act as electron donors. The intrinsic mean free path calculated by Kaasbjerg *et al.* [89], i.e. $\lambda \sim 14$ nm, allowed estimating the minimum density of impurities necessary for decreasing the RT mobility below the limit set by intrinsic phonons. This was found to be $\sim 5 \times 10^{11}$ cm^{-2}, consistent with heavy doping [14].
A strategy to limit the influence of charged impurities was proposed by Jena and Konar [20]. It consists in surrounding the 2D semiconductor with a high-κ dielectric material, which allows for damping the scattering potential originated by ionized impurities. Figure 4.6 shows the Coulomb potential contour of an impurity located inside a semiconductor membrane of thickness a. If the permittivity ε_e of the environment is chosen to be larger than that of the semiconductor, ε_s, then a substantial damping of the scattering potential occurs. The opposite conditions, $\varepsilon_e < \varepsilon_s$, results in the detrimental amplification of the scattering potential.

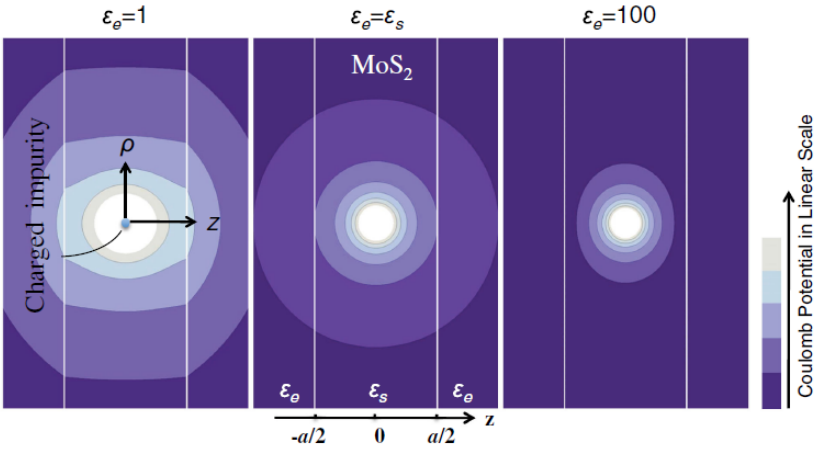

Figure 4.6: Dielectric screening of the Coulomb potential of ionized impurities. Effects of the dielectric environment on the Coulomb potential of ionized impurities located inside a 2D semiconductor membrane of thickness a. The dielectric constant of the semiconductor (MoS_2) is assumed to be $\varepsilon_s = 7.6$. Adapted from ref. [147].

Radisavljevic *et al.* implemented the dielectric-mismatch strategy by encapsulating monolayer MoS_2 with a high-κ HfO_2 dielectric layer within a dual gate FET architecture. The first report [5] showed RT mobilities of ~ 200 cm^2/Vs, but were affected by parasitic capacitive interferences between the back- and top-gate. However, subsequent Hall effect measurements enabled a correct estimate of the gate-to-channel capacitance [9, 10] and revealed RT mobilities of $\sim 40-50$ cm^2/Vs, which represents a remarkable improvement over the first pioneering investigations [2]. Reasons for the strong mobility increase were ascribed to the dielectric screening of charged impurities as well as to the presumable quenching of the homopolar phonon mode after encapsulation (section 4.3).
Variable-temperature electrical transport measurements were performed [9] to acquire information on the mechanisms that limit the experimental charge carrier mobility. Two different types of device architecture were studied, namely the single-gate FET with SiO_2/Si back-gate stack (figure 4.7a) and the dual-gate FET with HfO_2 gate dielectric and top metal gate (figure 4.7b). The devices had internal voltage probes (inset of figure 4.7c) and the measurements were performed in the four-probe scheme in order to remove the contribution of the contact resistance and access the MoS_2 sheet conductivity σ. Figure 4.7a shows a set of transfer curves (conductance G versus back-gate voltage V_{bg}) acquired at different T in a single-gate device. It can be seen that the conductance of monolayer MoS_2 increases with increasing T, indicating that the 2D semiconductor behaves as an insulator in the range of carrier density explored, i.e. up to $\sim 3.6 \times 10^{12}$ cm^{-2} at $V_{bg} = 40$V. For 80 K $\leq T \leq$ 280 K and $V_{bg} > 0$ V , it was found the conductance could be fairly described by an Arrhenius-type activated behavior

$$G = G_0 \cdot e^{-\frac{E_a}{k_B T}} \tag{4.6}$$

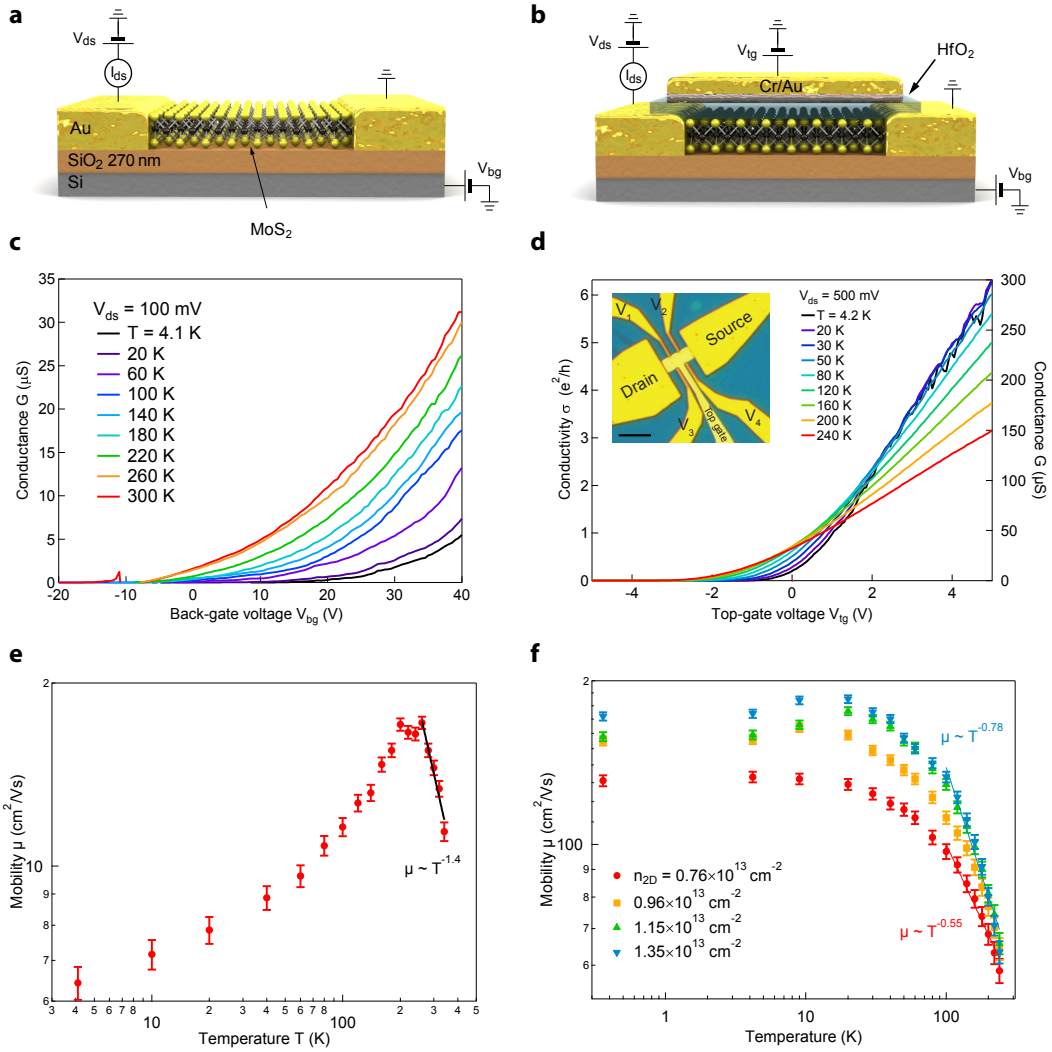

Figure 4.7: Temperature-dependent electrical transport measurements in monolayer MoS_2 FETs. **a,b,** Schematic cross-sectional view of back-gated and dual-gated FETs, respectively. The SiO_2 layer has a thickness of $\sim 270\,\mathrm{nm}$ and the HfO_2 layer of $\sim 30\,\mathrm{nm}$. **c,** Conductance G as a function of back-gate voltage V_{bg} for the structure shown in **a**. G was measured at various T in the four-probe geometry and was calculated as $G = \frac{I_{\mathrm{ds}}}{V_{1,2}}$, where $V_{1,2}$ is the voltage difference between the inner probes. **d,** Sheet conductivity σ versus top-gate voltage V_{tg} for the structure in **b** with the back gate connected to the ground. Inset: optical micrograph of a dual-gated multiterminal device (scale bar, $5\,\mu\mathrm{m}$). **e,f,** Field-effect mobility as a function of T for back-gated and dual-gated FETs, respectively. Adapted with permission from ref. [9], © 2013 Nature Publishing Group.

where E_{a} is the activation energy, k_{B} is Boltzmann constant and G_0 is a fitting parameter. For $T < 80\,\mathrm{K}$, the system entered a strongly localized regime, and the conductance showed a weaker T-dependence. A transport model based on hopping through localized states, – e.g. variable range hopping (VRH) [56, 178] – seemed to provide a fair description of the

conductance at low T. The observation of both thermally-activated and hopping transport pointed out the existence of a high degree of disorder inside or in the proximity of the 2D material. Thermally-activated transport usually occurs in the presence of shallow localized states, whereas VRH is induced by deep localized states [56].
The field-effect mobility as function of T is reported in figure 4.7e. It was calculated using the formula

$$\mu_{FE} = \frac{1}{C_i} \cdot \frac{\partial \sigma}{\partial V_g} \tag{4.7}$$

where C_i is the gate-to-channel insulator capacitance and V_g the gate voltage. σ is given by $G \cdot \frac{L_{1,2}}{W}$, where W and L_{12} correspond the width and the length, respectively, of the portion of the channel included between a pair of voltage probes. It is worth noting that μ_{FE} is related to the drift mobility $\mu = \frac{\sigma}{e \cdot n}$ by the following expression

$$\mu_{FE} = \frac{e}{C_i} \cdot \frac{\partial n}{\partial V_g} \cdot (\mu + \frac{\partial \mu}{\partial n} \cdot n) \tag{4.8}$$

so that the two mobilities are equivalent only if the capacitor model applies (i.e. $\frac{\partial n}{\partial V_g} \cdot e = C_i$) and if μ does not depend on n [179]. Therefore, critical attention has to be paid when comparing experimental data based on FE mobilities with theoretical models that estimate the drift mobility.
The μ_{FE} *vs.* T curve shown in figure 4.7e presents a peak at $\sim$ 200 K. For $T > 200$ K, μ_{FE} follows a power law (equation 4.1) with temperature damping parameter $\gamma = 1.4$, suggesting the occurrence of an intrinsic phonon scattering mechanism, due to the close agreement with the prediction by Kaasbjerg *et al.* [89]. For $T < 200$ K the mobility drops with decreasing T due to the effect of disorder.
A remarkably different scenario is observed in the case of dual-gated FETs, where the high dielectric constant ($\varepsilon_r \sim 18$) and lower thickness (30 nm) of the HfO_2 gate dielectric allows accessing carrier densities up to $\sim 3.6 \times 10^{13}$ cm^{-2}, i.e. one order of magnitude higher than in back-gated devices. Figure 4.7d displays a series of transfer curves (σ *vs.* V_{tg}) acquired at different T with a crossover occurring at $V_{tg} \sim 2.2$ V, which corresponds to a carrier density of $\sim 10^{13}$ cm^{-2}. Below this value, referred to as metal-insulator transition (MIT) point, σ depends on T as in the case of single-gate devices, i.e. with thermally-activated behavior. On the other hand, over the MIT point, σ increases with decreasing T, which is a sign of band-like metallic transport.
The conductivity at the MIT point was found to be of the order of the quantum of conductance $\frac{e^2}{h}$, with h being Planck constant. Reasons for the occurrence of the transition were originally attributed to the onset at high n of electron-electron interactions, such as in strongly correlated 2D electron gases [9]. Further studies revealed that the transition is likely to be related to the presence of a high density of trap states (presumably due to

defects, section 4.5) below the bottom of the conduction band, which form a band-tail of localized states [56, 175]. Under this condition, thermal-activation stems from the fact that carriers in the band-tail can be thermally activated into the conduction band. Instead, at high carrier density ($n \gtrsim 10^{13}$ cm^{-2}), the localized states are filled and a significant amount of electrons starts populating the conduction band, so that band-like metallic transport occurs. Hence, the use of the high-κ was useful, not only to screen the Coulomb potential of charged impurities, but also to access the band-transport at high carrier density, which is not easily obtained with standard back-gated structures. In fact, the latter are characterized by a gate-to-channel capacitance much smaller than in top-gated devices, by approximately a factor of 40.

The field-effect mobility as a function of T is shown in figure 4.7f for various carrier densities, in the range from 7.6×10^{12} cm^{-2} to 1.35×10^{13} cm^{-2}. Between 4 K and 100 K, all the μ_{FE} *vs.* T curves form a plateau; the highest mobility is obtained for $n = 1.35\times10^{13}$ cm^{-2} and is equal to ~ 174 cm^2/Vs. For $T > 100$ K, the curves follow a power law, where the damping parameter γ increases from 0.55 to 0.78 with increasing n . These γ-values are significantly lower than those predicted in the case of intrinsic phonon scattering, suggesting that other mechanisms may play a dominant role. One possible source of deviation from theoretical models lies the discrepancy between the FE and the drift mobility, as highlighted by equation 4.8. However, both Ma and Jena [147] and Ong and Fischetti [180] showed that the damping of mobility at high T can be explained using an impurity-scattering model,

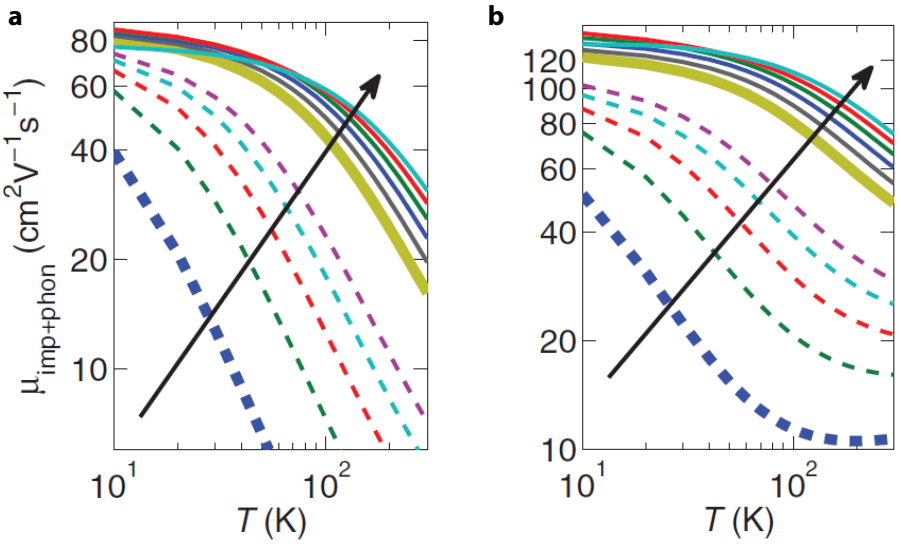

Figure 4.8: Mobility limited by charged impurities and intrinsic phonons in monolayer MoS_2. **a,** Calculated μ *vs.* T curves for back-gated FETs without HfO_2 capping layer. Dashed lines: n from 10^{12} to 5×10^{12} cm^{-2}. Solid lines: n from 10^{13} to 2×10^{13} cm^{-2}. **b,** Same curves as in **a** for the case of dual-gated FETs incorporating an HfO_2 dielectric. Adapted with permission from ref. [180], © 2013 American Physical Society.

by taking into account the T-dependence of the polarizability. The latter is related to the screening of the Coulomb potential by free electrons and is therefore strongly dependent on n. Figure 4.8 displays the T-dependent mobility calculated by Fischetti *et al.* in the case of FETs without (a) and with (b) HfO_2 gate dielectric. The density of impurities was assumed to be $n_{imp} = 4 \times 10^{12}$ cm^{-2}, whereas the carrier density was tuned in the range from 10^{12} to 2×10^{13} cm^{-2}. It can be seen that the use of high-κ dielectrics results in an effective mobility enhancement. The damping of μ at high T was found to be set by impurity scattering rather than by phonons and showed a strong dependence on both carrier density and dielectric environment. For $n = 10^{13}$ cm^{-2}, the temperature damping parameter was calculated to be ~ 0.5 and ~ 1 in dual-gated and back-gated FETs, respectively. This model provided a good interpretation of the results by Radisavljevic *et al.* and pointed out the strong dependence of μ and γ on carrier density, suggesting that charged impurities are likely to be the dominant scattering mechanism at all temperatures.
In this context, a question arises concerning the origin of charged impurities, i.e. whether they are internal to MoS_2 or induced by the supporting substrate or surrounding environment. Moreover, it is expected that other forms of disorder (e.g. defects) may contribute to decrease the mobility. In the last four years, variable-temperature transport measurements have been performed by several groups on both exfoliated [175, 178, 179, 181] and CVD-grown [56, 151] monolayer MoS_2. The goal of these measurements was to shed light on the influence of different extrinsic sources of disorder, in order to develop suitable strategies for improving the performance of electronic devices based on 2D MoS_2.

4.5 Extrinsic sources of charge scattering

In this section, the influence of the extrinsic sources of scattering – listed in figure 4.2 – will be presented and discussed. The first two sources, namely native impurities and defects, are internal to MoS_2 and can be reduced primarily through the optimization of the material growth process. The remaining sources are due to external factors, such as atmospheric gases, substrate and gate-dielectric material. Their influence can be limited *via* a careful design/fabrication of the devices.

4.5.1 Native impurities and defects

High-level of n-doping observed in monolayer MoS_2 suggests the existence of donor impurities within the material. Naturally occurring MoS_2 crystals contain different impurity elements, such as for instance rhenium [182]. The latter is known to be present in molybdenite ores, where it substitutes Mo and acts as n-dopant [183]. Figure 4.9a displays the concentration of Re measured in a total of 422 MoS_2 specimens collected in 135 localities

around the world and belonging to different geological eras. It can be seen that typical Re concentrations are of the order of few hundreds parts per million, sometimes up to 1 % (table in the inset). These high values indicate that dopants such as Re could be responsible not only for *n*-doping, but also for the strong degradation of the carrier mobility that is commonly ascribed to ionized impurities.

Internal defects – such as sulfur vacancies, dislocations, structural phase changes, grain boundaries, etc. – represent another detrimental source of disorder that can dominate the overall transport properties. A detailed experimental characterization of these intrinsic defects was recently provided by Zhou *et al.* [185], who conducted high-resolution TEM investigations on CVD grown monolayer MoS_2 and identified several types of defects, among which grain boundaries and point vacancies. DFT calculations by Ghorbani-Asl *et al.* [186] showed that these defects induce strongly localized gap states that act as scattering centers and can significantly reduced the conductance.
The effects of point defects (e.g. sulfur vacancies) on charge transport were studied both experimentally and theoretically by Qiu *et al.* [184]. They performed variable-temperature transport measurements on exfoliated few-layer MoS_2 sheets, which were employed as channel material in conventional back-gated FETs. At low carrier density ($n \lesssim 3 \times 10^{12}$ cm^{-2}), they observed VRH and nearest-neighbor hopping, at low and high

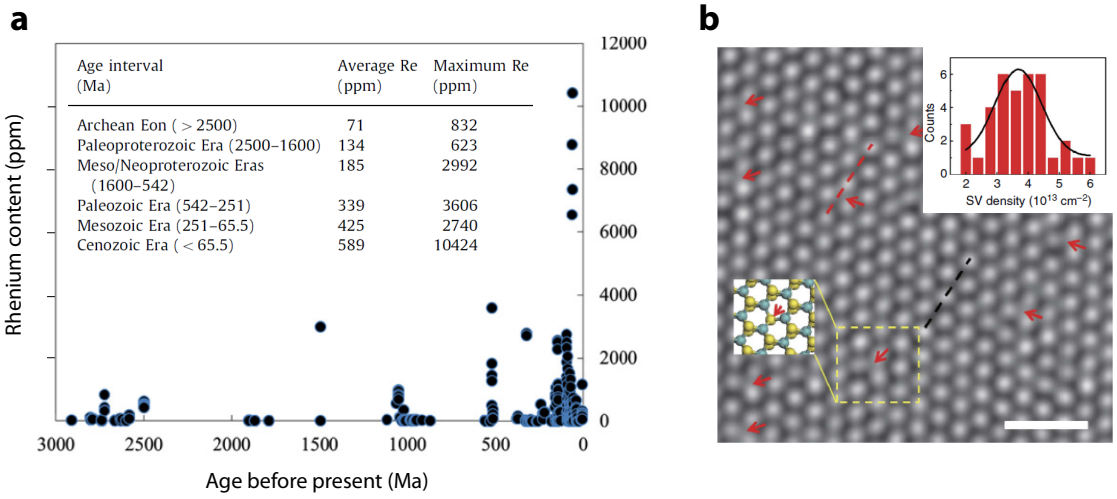

Figure 4.9: Impurities and defects internal to MoS_2. **a,** Content of Re impurities as a function of geological age (1 Ma = 10^6 years) obtained from 422 samples from 135 different localities. The table in the inset displays the average and maximum Re concentrations for specimens of six different eras. Adapted with permission from ref. [182], © 2013 Elsevier. **b,** Aberration-corrected TEM image of monolayer MoS_2 with sulfur vacancies (marked by red arrows). Scale bar: 1 nm. Lower inset: schematics of the highlighted region. Upper inset: histogram of SV density. The image was acquired with a 80 keV electron beam and the estimated density of beam-induced vacancies was $\sim 10^{12}$ cm^{-2}. Adapted with permission from ref. [184], © 2013 Nature Publishing Group.

T, respectively. In combination, they carried out TEM investigations and observed a very high density of sulfur vacancies ($\sim 10^{13}$ cm^{-2}), as reported in figure 4.9b, indicating a high degree of short range disorder. First-principles calculations were also performed to evaluate the influence of sulfur vacancies on the electron transport. It was found that strongly localized donor states were induced by the vacancies inside the bandgap of 2D MoS_2; moreover, due to the high surface density of the sulfur vacancies, the transport could occur *via* hopping mechanisms through defect-induced localized states.

The landscape of disorder internal to monolayer MoS_2 can be complex and requires careful attention. It has been shown that, in the low carrier-density range, internal defects can dominate the overall transport. On the other hand, at high carrier densities, the defect-induced localized states are filled and the conduction band starts being populated, so that band-like transport occurs. However, delocalized electrons in the band will still experience short-range scattering from vacancies and other types of defects [151].
At this stage, there is agreement in the research community about the need for reducing the amount of internal defects and impurities to enable further progress in the field of MoS_2 electronics. To this purpose, the main strategy consists necessarily in the optimization of the growth/synthesis process (section 2.3.2) as well as in the thorough purification of the material sources. Other approaches have been reported (e.g. ref. [175]), where specific chemical treatments are used to repair defects (sulfur vacancies) and have been explored as well in the context of this thesis [187]. The methods consists in exposing the surface of monolayer MoS_2 to a solution of thiol molecules that react with the unsaturated Mo atoms, decompose and "repair" the defects by leaving a S atom on the vacancy site. This process was first experimentally investigated by Makarova *et al.* [188] by means of scanning tunneling microscopy (STM) and then employed by Yu *et al.* [175] as a defect-engineering approach to improve the performance of monolayer MoS_2 FETs (section 5.3).

4.5.2 Atmospheric adsorbates

Band-like metallic transport was observed by Jariwala *et al.* [181] in back-gated single-layer MoS_2 FETs fabricated on oxidized Si samples. Electrical transport measurements were performed on unencapsulated devices (inset of figure 4.10b) located inside a high-vacuum chamber (pressure $< 2 \times 10^{-6}$ mbar) in order to remove atmospheric adsorbates from the surface of monolayer MoS_2. Figure 4.10a compares the transfer characteristics (I_d *vs.* V_g) of one such device in ambient air (red) and high-vacuum (blue). In both cases the turn-on voltage V_{on} (i.e. the gate voltage at which the drain-source current starts increasing exponentially) lies at negative voltages, indicating that the 2D material is n-doped. As the environment is changed from ambient air to high-vacuum, V_{on} shifts from ~ -20 V to ~ -65 V, which suggests that atmospheric adsorbates, such as molecular oxygen and

water, act as electron acceptors. The strong negative shift of V_{on} allows for higher carrier density to be achieved in conventional back-gated devices. This fact, combined with the high-quality of the MoS_2 surface under vacuum, enabled the observation of a transition from VRH (at low n) to band-like transport (at high n). In the metallic regime, the μ_{FE} *vs.* T curves (figure 4.10b) displayed a trend very similar to that reported by Radisavljevic *et al.* [9] (figure 4.7f) with field-effect mobility of $\sim 60\,cm^2/Vs$ at RT and up to $\sim 120\,cm^2/Vs$ for $T < 100\,K$.

Recently, Yue *et al.* [189] carried out first-principles calculations to investigate the adsorption of different gas molecules on the surface of monolayer MoS_2 and to evaluate the charge transfer between the molecules and the 2D semiconductor. It was found that O_2 and H_2O,

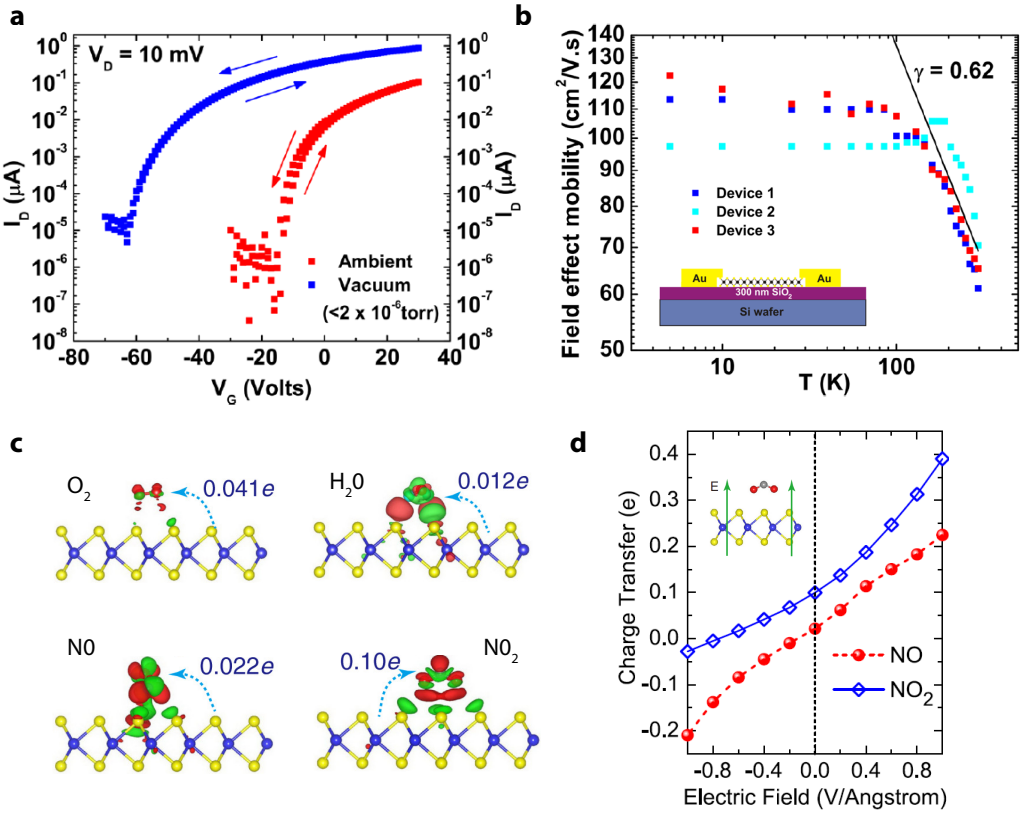

Figure 4.10: Effects of the environment on the transport properties of monolayer MoS_2. **a,** Semi-log plot of drain-source current I_d as a function of gate voltage V_g for a device in ambient air (red) and high-vacuum (blue) at a pressure lower than 2×10^{-6} mbar. **b,** μ_{FE} *vs.* T curves acquired in vacuum from three different samples. Inset: schematics of the back-gated unencapsulated single-layer MoS_2 FET. **c,** Charge density difference plots for different molecules interacting with monolayer MoS_2. The magnitude and direction (light-blue arrow) of the charge transfer are also indicated. **d,** Charge transfer as a function of electric field applied perpendicularly to a monolayer MoS_2 sheet (schematics in the inset). **a** and **b** are adapted with permission from ref. [181], © 2013 AIP Publishing LLC. **c** and **d** are adapted from ref. [189].

as well a number of other molecules (e.g. NO and NO_2), are only weakly adsorbed on the MoS_2 surface and behave as electron acceptors (figure 4.10c). Therefore, in high-vacuum conditions, these molecules can be easily desorbed, resulting in the full recovery of the material's *n*-doping. It was also found that the magnitude and direction of the charge transfer are modulated by an external electric field, as shown in figure 4.10c, which explains the hysteresis commonly observed in the transfer characteristics of unencapsulated FETs exposed to ambient air [190]. It is worth noting that the calculations by Yue *et al.* [189] assume the MoS_2 surface to be ideal. However, in real samples, the presence of defects could significantly alter both the strength of the adsorption and the charge transfer. For instance, oxygen can be chemisorbed on sulfur vacancies and the resulting charge transfer (0.997 electrons [73]) is much larger than in the case of weak adsorption (0.041 electrons [189]).
These results showed the importance of vacuum conditions for limiting the occurrence of charge transfer processes, which are known to be highly detrimental for the performance of electronic devices. Adsorbed molecules, if ionized, can also act as long-range Coulomb scatterers [191] and therefore have to be removed. To this purpose, a common practice consists in performing a thermal annealing ($80-140^{\circ}C$) in high-vacuum [192, 193], which results in an efficient removal of adsorbates and increases remarkably the density of free carriers in monolayer MoS_2. In this way, Baugher *et al.* [179] were able to observe the occurrence of MIT in conventional back-gated devices. Hall effect measurements were conducted to accurately measure the carrier density, which was found to exceed 10^{13} cm^{-2} in the metallic regime.

4.5.3 Interfacial impurities

When used as channel material in FETs, monolayer MoS_2 has to be sandwiched between a substrate and a gate dielectric material. The quality of the bottom and top interfaces is critical for the performance and reliability of electronic devices and demands careful attention during design and fabrication. In fact, charge traps, adsorbates and dangling bonds on the substrate surface or at the interface with the overgrown dielectric can induce severe performance degradation.
The typical substrate employed for testing the properties of 2D materials is SiO_2/Si (see section 5.1). In the case of graphene, it was soon understood that charged impurities on the SiO_2 surface were responsible for carrier mobility degradation [194]. The replacement of the conventional SiO_2 substrate with the trap-free h-BN enabled extremely high quality graphene devices exhibiting high mobility ($\sim 60,000$ cm^2/Vs) and micrometer scale ballistic transport [166]. On the other hand, in the case of monolayer MoS_2, it is not yet clear if charged impurities from the substrate represent a major cause of mobility degradation or if defects/impurities located inside MoS_2 play a more important role.

Ghatak *et al.* [178] performed variable-temperature transport measurements on back-gated devices fabricated on 2D MoS_2 sheets deposited on SiO_2/Si substrates. They observed carrier localization up to RT and VRH transport. From the correlation energy T_0 of the VRH model, they deduced that charged impurities located in the SiO_2 substrate were responsible for the observed carrier localization. However, in a recent work [195] based on the measurement of low-frequency noise in MoS_2 FETs, they extracted a density of trap-states one to two order of magnitude higher than the typical values of interfacial trap states at the SiO_2 surface, suggesting a possible internal origin of the traps.
Hence, further investigation is required to shed light on the relative influence of the substrate charged impurities compared to internal defect/impurities. In this direction, studies of different dielectric substrates and trap characterization via capacitance-voltage measurements can provide valuable information [187].
Finally, it should be mentioned that the growth of high-quality dielectric layers on the surface of 2D semiconductors, with very low densities of defects, charged impurities and dangling bonds, represents a major challenge, which needs to be solved for the production of electronic devices based on these materials [196].

4.5.4 Device processing

To explore the charge transport properties of a 2D crystal, it is essential to adopt a device fabrication technique that does not introduce further impurities and defects. Contact fabrication is usually performed *via* lithographic processes, where the surface of the semiconductor layer is covered with an organic resist. The latter is then removed by the use of solvents, but residual contamination usually remains on the surface. Due to the ultimate surface sensitivity of 2D materials, the presence of extrinsic chemicals can affect their electronic, optical and vibrational properties. Strategies to limit contamination have been found in the use of highly soluble acrylic resists [197], as well as in thermal annealing processes with forming gases (e.g. Ar and H_2). It is worth noting that during annealing at high T ($300-400°C$), one should be careful to avoid mechanical stresses and material cracks induced by a difference in the thermal expansion coefficients of the 2D material and its substrate. Recently, a new strategy has been developed where the 2D material is encapsulated between h-BN sheets prior to lithography and does not enter in contact with any organic resist (ref. [198]).
In the last four years, a great deal of attention has been given to the fabrication of high-quality heterostructures, where multiple polymer-based transfer steps (appendix B.3) are required for stacking different 2D crystals one on top of the other. In this context, the problem of contamination is critical, since at each step, new chemical residue is added. Furthermore, within the assembled heterostructure, the 2D materials do not perfectly adhere to each other, but may form ripples, bubbles and corrugations that act as

a detrimental source of charge inhomogeneity [15]. These problems were faced as well in this thesis (appendix A) for the realization of monolayer Mo_2/h-BN heterostructures.

4.5.5 Remote optical phonons

In section 4.4, it was mentioned that the use of high-κ dielectric materials is advantageous for screening the potential of Coulomb impurities. However, high-κ dielectrics are typically characterized by low-energy polar optical phonons that can severely limit the RT charge carrier mobility [199]. Electrons in the conducting channel can remotely excite polar optical phonons in the dielectric *via* long-range Coulomb interactions. The coupling between the electrons and these "remote optical phonons" represents an additional source of charge carrier scattering, which becomes more relevant as the number of "active" phonons in the dielectric increases. It is worth noting that the effect of remote optical phonons is expected to be critical in 2D materials, since the charge transport occurs in the atomic-scale proximity of the dielectric surface.
Table 4.1 reports the energies of the polar phonon modes for a set of insulating materials having different dielectric constants. It can be seen that high-κ oxides, such as ZrO_2 and HfO_2 are characterized by optical phonon modes with relatively low energies, smaller than 25 meV. This means that even at RT the optical phonons of these materials are active and can induce remote phonon scattering (RPS). On the other hand, low-κ dielectrics, such as BN and SiO_2 present higher optical phonon energies, so that the influence of RPS becomes relevant only at higher temperature.
Zeng *et al.* [200] performed Monte Carlo simulations based on the results of first-principles

Dielectric	ε_r	E_{op}^{1st} [meV]
SiO_2	3.9	55.6
AlN	9.14	81.4
BN	5.09	93.07
Al_2O_3	12.53	48.18
HfO_2	23	12.4
ZrO_2	24	16.67

Table 4.1: Polar optical phonons in common inorganic dielectrics. Energy of the 1st optical polar phonon mode E_{op}^{1st} and relative dielectric constant ε_r of different dielectric materials. Adapted from ref. [147].

calculations (ref. [89]) and evaluated the influence of remote optical phonons on the RT electron mobility of monolayer MoS_2. It was found that RPS from the SiO_2 substrate decreased the mobility from ~ 420 cm^2/Vs (intrinsic value) to ~ 230 cm^2/Vs. If a top-gate dielectric material was added, μ further decreased to ~ 116 cm^2/Vs and ~ 28 cm^2/Vs in the case of Al_2O_3 and HfO_2 dielectrics, respectively. These results show that RPS from high-κ materials is highly detrimental and can be even more severe than scattering from charged impurities. Therefore, a trade-off should has to be chosen between low κ – for limiting RPS – and high κ for screening the potential of Coulomb impurities.
The combined effect of RPS and dielectric screening in monolayer MoS_2 was investigated theoretically by Ma and Jena [147], whose calculations offered useful guidelines for the choice of the substrate and gate dielectric materials. In their work, they considered the scattering from charged impurities, intrinsic phonons and RPS and they took into account the free-carrier screening effect, which is modulated by both temperature and dielectric environment. Figure 4.11a shows the electron mobility of monolayer MoS_2 surrounded by materials with different dielectric constants, assuming $n_{imp} = 10^{13}$ cm^{-2}. At low temperature (T = 100 K), the remote optical phonons are not active and the mobility increases with the dielectric constant ε_e of the environment, due to the higher dielectric screening of

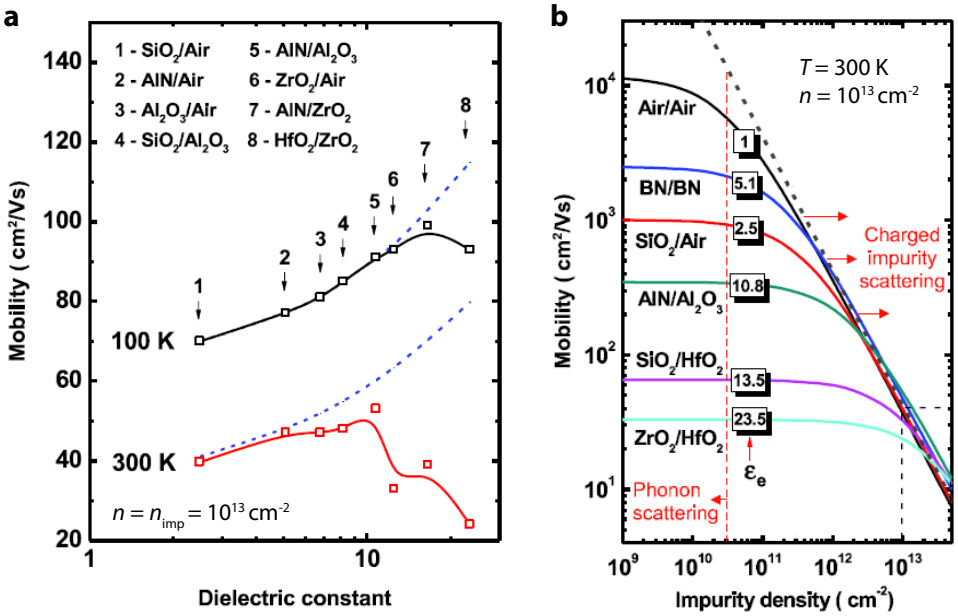

Figure 4.11: Effects of the dielectric environment on the electron mobility of monolayer MoS_2. **a,** Calculated μ as a function of effective dielectric constant ε_e of the surrounding environment. Dashed lines represent the mobility without the effect of RPS. The data for phonon energies are reported in table 4.1. The density of impurities n_{imp} and the carrier density n are both equal to 10^{13} cm^{-2}. **b,** Calculated RT mobility as a function of impurity density for different dielectric environments. Intrinsic phonons, charged impurities and RPS are included in the calculations. Adapted from ref. [147].

the impurity potential. A different trend is observed at RT, where the onset of RPS cancels the benefit associated with dielectric screening and severely degrades the mobility, which starts decreasing already from $\varepsilon_e \sim 6-7$.
Figure 4.11b displays the RT mobility as a function of n_{imp}. For low impurity densities, i.e. $n_{imp} \lesssim 3\times10^{10}$ cm^{-2}, the limit to the electron mobility is set uniquely by RPS. Under this condition, the best results are obtained in the case of a suspended sheet ($\mu \sim 10^4$ cm^2/Vs) or through encapsulation in BN ($\mu \sim 2\times10^3$ cm^2/Vs). It is worth mentioning that such high theoretical values stem from the inclusion of the free-carrier screening effect, which represents a relevant influence at high carrier densities ($n \gtrsim 10^3$ cm^{-2}). For higher impurity densities, the limit to the electron mobility is set by both RPS and charged impurity scattering; it can be seen that μ starts to become weakly dependent on dielectric environment for $n_{imp} \gtrsim 10^{13}$ cm^{-2}. It is within this range that the use of high-κ dielectrics could be advantageous.
The work by Ma and Jena [147] showed that low-κ dielectrics are necessary to obtain high RT mobility, once the density of impurities is made of the order of 10^{12} cm^{-2}, which is a target to be achieved to enable further progress in MoS_2-based electronics.

4.5.6 Surface roughness

Surface roughness is a detrimental source of carrier scattering that severely degrades the performance of FETs based on ultrathin channel materials, such as Si (SOI) or heterostruc-

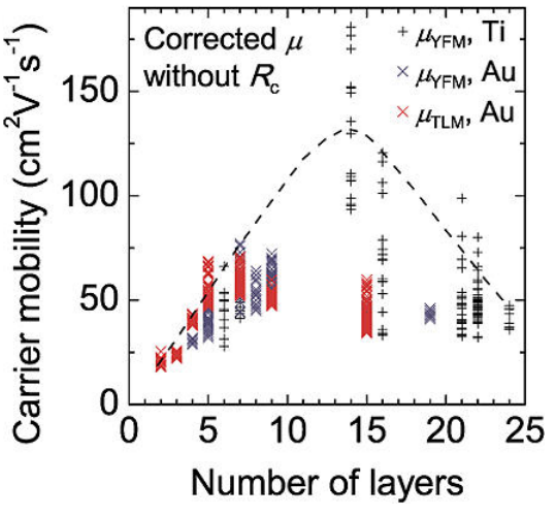

Figure 4.12: Dependence of the FE mobility on the thickness of the MoS_2 channel. Plot of the FE mobility as a function of channel thickness, as obtained from several back-gated MoS_2 devices. The devices had Au (×) and Ti (+) contacts and the effect of contact resistance R_C was removed by using the Y-function method (YFM) and transfer length method (TLM). Adapted with permission from ref. [191], © 2013 American Chemical Society.

ture quantum wells (e.g. GaAs/AlAs) [147]. Surface roughness scattering (SRS) is due to changes in the channel thickness t, resulting in local perturbation of the potential experienced by the charge carriers. The roughness-limited mobility μ_{SR} scales as a sharp power law, namely $\mu_{SR} \propto t^6$. Li *et al.* [191] measured the dependence of the carrier mobility on thickness in the case of MoS_2 nanosheets (figure 4.12) and found that the μ *vs.* t curves could not be fitted with such a sharp power law, indicating a different dominant scattering mechanism.
2D materials are expected to be immune from SRS [147, 191] because they have uniform atomic-scale thickness and ideally, have no dangling bonds. However, both free-standing and substrate-supported 2D sheets present out-of-plane corrugations, which can introduce disorder and scattering. Brivio *et al.* carried out TEM investigations of free-standing monolayer MoS_2 membranes and found that the 2D sheets were characterized by out-of-plane waviness, with ripples having typical lateral size of 6 – 10 nm and height in the range of 6 – 10 Å, which represents short-range disorder. On the other hand, AFM investigations of substrate-supported MoS_2 nanosheets, revealed that the 2D sheets assume a roughness similar to that of the underlying substrate [187]. For instance, monolayer MoS_2 deposited onto a smooth sapphire surface presented a root-mean-square roughness Rq $\lesssim$ 1 Å over a μm-scale large area. If deposited onto a rough polymer film, monolayer MoS_2 showed Rq up to $\sim$ 1 nm. In this thesis, the effect of substrate roughness was investigated by performing transport measurement on FETs fabricated on such remarkably different substrates. It was found that surface corrugations did not represent a major cause of mobility degradation [187].

4.6 Conclusion

A remarkable aspect of the charge transport properties of monolayer MoS_2 is the strong discrepancy between the theoretical and experimental mobility. The latter is strongly limited by different extrinsic sources of disorder. It was shown that, in the metallic regime (high n), the measured μ *vs.* T curves can be fairly modeled through an impurity-limited mobility. Instead, in the insulating regime (low n), the occurrence of hopping transport can be ascribed to the presence of defect-induced localized states below the bottom of the conduction band. The strong influence of sources of scattering external to MoS_2, such as atmospheric adsorbates, remote optical phonons and interfacial impurities, has also been highlighted in the last section of the chapter.
In this complex scenario, minimizing the discrepancy between intrinsic and extrinsic mobility has to be pursued by the use of multiple strategies, which aim both to optimize the quality of the interfaces and to reduce internal disorder. We shall see in chapter 5 that a combined interface- and defect-engineering approach resulted in an interesting improvement of the charge transport properties of monolayer MoS_2.

5 Monolayer MoS_2 FETs and alternatives to SiO_2 substrates

5.1 Introduction

Field-effect transistors (FET) based on 2D materials are commonly fabricated on oxidized silicon substrates due to some immediate advantages. Besides being widely commercially available, SiO_2/Si substrates offer a high optical contrast for the visualization of 2D crystals, which greatly facilitates the device fabrication process. Moreover, the heavily doped Si support can be readily employed as gate electrode, providing a straightforward method to implement a back-gated FET. However, it is known that the SiO_2 surface is rich with dangling bonds, adsorbates and impurities that can severely degrade the transport properties of the overlying materials. In the case of graphene, Bolotin *et al.* [201] showed that removing the substrate by suspending the 2D sheet *via* chemical etching of SiO_2 enabled a tenfold improvement in mobility after current annealing, reaching values as high as 200,000 cm^2/Vs at 5 K. Subsequently, Dean *et al.* [166] proved that replacing the conventional SiO_2 substrate with a trap-free alternative, namely h-BN, resulted in almost one order of magnitude reduction of the charge density inhomogeneity and in a threefold decrease in the scattering rate due to charged impurities. These results proved the detrimental influence of the SiO_2 substrate on the transport properties of graphene and stimulated similar experimental investigations also in the case of 2D TMDs. There is presently a strong need to identify suitable dielectric substrates to be used in combination with these atomically thin semiconductors. Research in this direction has been carried out in this thesis, which explored the transport properties of monolayer MoS_2 lying at the interface with three different dielectric materials, namely trap-free h-BN, sapphire and thin films of parylene.

The chapter is organized as follows. The first part will describe the properties of the three dielectric substrates, illustrating the reasons that supported their choice. Some additional features that emerged during the development of this doctoral research will be

also reported. The second part will present a combined interface- and defect-engineering approach (ref. [175]), which has been adopted in this thesis to reduce the influence of both internal and external sources of charge carrier scattering. The results of the work are reported in the form of a paper (Bertolazzi *et al.*, submitted, 2015 [187]), whose main conclusions are summarized at the end of the chapter.

5.2 Interface engineering

Tuning the properties of the dielectric/semiconductor interface with the objective to improve the charge carrier mobility in the semiconductor can be referred to as an interface-engineering approach. This type of approach has been implemented by choosing dielectric substrates with different advantageous properties. The goal was to minimize the interfacial disorder related to impurities, remote phonons and surface corrugations. In chronological order of investigation, the most relevant aspects of h-BN, sapphire and parylene will be presented in the following of this section.

5.2.1 Hexagonal boron nitride

The interest in h-BN as a substrate for 2D electronic devices exploded in 2010, when Dean *et al.* [166] reported a tenfold improvement in graphene's charge carrier mobility by replacing the SiO_2 substrate with a thin crystalline sheet of h-BN. Potential fluctuations induced by charged impurities on the SiO_2 surface were found to be responsible for detrimental charge density inhomogeneities in graphene, resulting in a remarkable mobility degradation. Kelvin probe force microscopy (KPFM) investigations carried out by Burson *et al.* [202] revealed that the fluctuations were about one-to-two orders of magnitude lower in the case of h-BN (figure 5.1), which can therefore be referred to as an impurity- and trap-free substrate.
The energy of the polar optical phonons in h-BN is relatively large, namely ~ 93 meV (table 4.1), so that remote phonon scattering (RPS) is expected to be low at RT. Moreover, the thermal conductivity of h-BN is ~ 200 times larger than that of SiO_2 (table 2.2), indicating that a highly efficient heat dissipation can be achieved by employing h-BN as a substrate and gate dielectric material in FETs. The roughness Rq of h-BN nanosheets can be as low as 1 Å, i.e. approximately 3 times smaller than in SiO_2 [187]. Therefore, h-BN can reduce to a minimum level also the influence of surface corrugations.
From a structural point of view, boron nitride is an isomorph of graphene, where B and N atoms occupy inequivalent sublattices of the honeycomb hexagonal structure. The alternating B-N chemistry is at the origin of the material's electrical insulating properties, characterized by a large energy bandgap $E_g \sim 6$ eV and high breakdown field $E_{bd} \sim 0.7$ V/nm

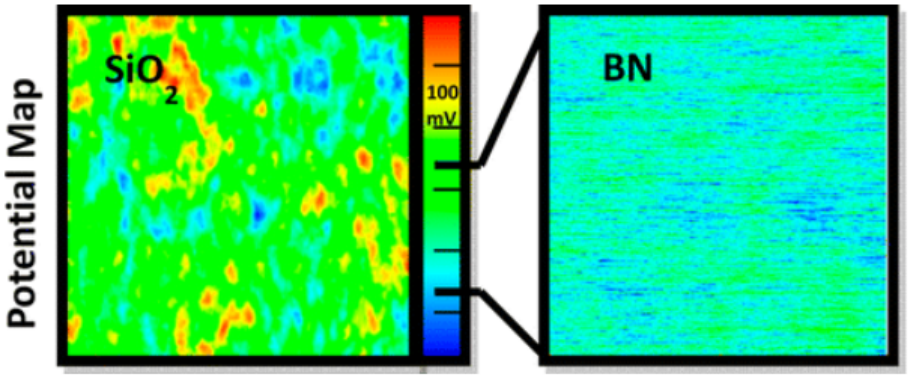

Figure 5.1: Direct imaging of charged impurity density in SiO_2 and h-BN. Local electrostatic potential fluctuations on the surface of SiO_2 (left) and h-BN (right), as measured by KPFM in ultrahigh vacuum. On SiO_2, the impurity density extracted from modeling is $\sim 2.5 \times 10^{11}$ cm^{-2}, whereas on h-BN is more than one order of magnitude lower. Adapted with permission from ref. [202], © 2013 American Chemical Society.

[166]. H-BN is considered to be a low-κ insulator, since its static dielectric constant ε_r is similar to that of SiO_2 [166]. Thus, its only drawback lies in the fact that it can not provide an efficient screening of the Coulomb potential of charged impurities (section 4.4).
Similarly to MoS_2 and graphene, h-BN thin sheets can be obtained by mechanical exfoliation of bulk crystals. With the scotch-tape method (section 2.3) it is possible to produce thin flakes with thickness in the nanometer scale and with a typical lateral size in the range of $10 - 100$ μm. Therefore, in order to use these nanosheets as substrates for monolayer MoS_2, it is necessary to employ a flake-transfer technique (appendix B) for assembling h-BN/MoS_2 heterostructures. During the assembly, it is critical that monolayer MoS_2 is not damaged or contaminated, otherwise all the benefits associated with the use of h-BN can be lost due to the introduction of additional extrinsic disorder (section 4.5, device processing). At the early stages of this doctoral research it was understood that damages, contamination and sheet-rippling generated during the transfer process represented the most critical issues to be solved. For this reason, a large part of the experimental work was devoted the optimization of the heterostructure fabrication procedure, whose details are reported in appendixes A.3 and B.

5.2.2 Atomically smooth sapphire

Sapphire is a crystalline form of aluminum oxide, namely corundum or α-Al_2O_3, which is characterized by hexagonal crystal structure. Substrates of sapphire can be prepared with various crystalline orientations, providing lattice-matching conditions for the epitaxial growth of important (opto-)electronic materials, among which GaN and Si. Figure 5.2a shows the atomic structure of the C-plane surface of sapphire, which shares with MoS_2 the

same hexagonal lattice symmetry. Recently, Dumcenco *et al.* [140] showed that this surface can be exploited for the van der Waals epitaxial growth of large-area monolayer MoS_2 (section 2.3.2). Given the growing importance of sapphire in the field of 2D materials, it is presently of high interest to explore the influence of this substrate on the charge transport properties of atomically thin semiconductors. This has been done during this doctoral research through the fabrication and characterization of FETs based on monolayer MoS_2 flakes mechanically exfoliated from the bulk and deposited on sapphire.
The most remarkable feature of the sapphire substrates is their ultralow roughness. AFM investigations revealed that Rq can be smaller than 1 Å over a micrometer-scale large area. Moreover, upon thermal annealing at 1000 °C in air, the sapphire surface undergoes a reconstruction and forms a series of atomically smooth terraces [203]. Figure 5.2b shows the morphology of a C-plane sapphire surface after annealing, as measured by AFM. From the height profile, the average width of the terraces is deduced to be ~ 70 nm, whereas the height of the steps is ~ 0.2 nm, which is even lower than the overall Rq of SiO_2 (~ 0.3 nm). Wider terraces could be obtained by the use of sapphire substrates with different orientations. For example, thermal annealing of R-plane substrates resulted in terraces as large as ~ 200 nm (appendix A.4). It is worth noting that this type of morphology offers also the intriguing possibility to investigate the effect of surface roughness on charge transport, by measuring the dependence of the electron mobility on the angle between the current flow and the step-edges. We report here that no significant dependence could be measured, indicating that step-induced roughness did not represent a major limit to charge transport.

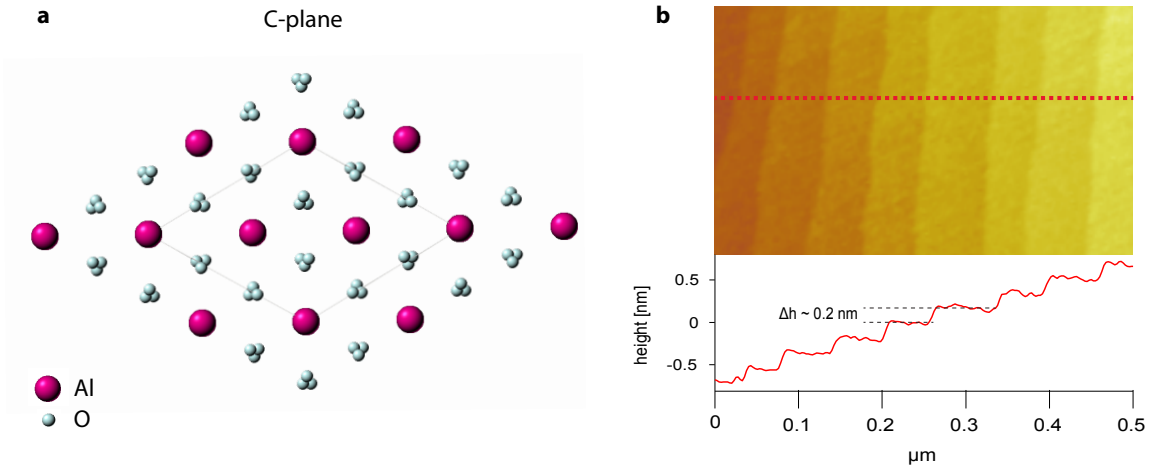

Figure 5.2: Structure and morphology of the sapphire surface. a, Atomic structure of the C-plane surface of sapphire, i.e. oriented perpendicular to the *c*-axis of the hexagonal crystal structure. Made online at http://webmineral.com. **b,** Top: intermittent-contact AFM scan of the C-plane surface of sapphire, acquired after annealing at 1000 °C in air. Bottom: height profile along the red dashed line, showing atomic terraces with average width of ~ 70 nm and height of ~ 0.2 nm.

Differently from h-BN and SiO_2, sapphire is a high-κ material with dielectric constant ranging between 9 and 12, depending on crystal orientation [18]. The energy of its polar optical phonons ($\sim$ 48 meV) is not much lower than that of SiO_2 ($\sim$ 55 meV). This might represent a good compromise to obtain significant screening of the charged impurity potential without introducing too detrimental RPS.
The highly hydrophilic nature of the sapphire substrates was found to represent a critical feature. In ambient air, the surface of sapphire can be highly hydroxylated [204] so that a large amount of charge traps and impurities, in the form of hydroxyl groups or molecular adsorbates, can be accumulated at the substrate/MoS_2 interface (appendix A.4). In addition, the insulating sapphire substrate can easily become electrostatically charged during device processing, further promoting the absorption of ionic species. Finally, if a top-gated FET architecture is used, then the removal of the adsorbates by vacuum annealing can be hindered by the presence of the gate dielectric. All these aspects became clear during the development of the research and brought to light the strong influence of adsorbed impurities and interfacial traps on the transport properties of monolayer MoS_2.

5.2.3 Parylene thin films

The term "parylene" denotes a class of poly(p-xylylene) polymers that are deposited from the vapor phase – by means of chemical vapor deposition polimerization (CVDP) [205] – and form highly conformal and chemically inert coatings on various surfaces. Parylene films are commonly used for packaging of microelectronic devices, because of their excellent performance as moisture barriers. They are also thermally stable and insoluble in common organic solvents, which makes them compatible with different microfabrication techniques, such as e-beam lithography. Moreover, parylene is an interesting flexible and biocompatible material and can be conveniently employed as a substrate for flexible (bio-)electronic applications [206].
There are more than 20 types of parylene, associated with variations in the chemical structure of the monomer, but only few of them are commercially available. Among these, parylene C (figure 5.3a) is one of the most popular, as it offers a useful combination of electrical and physical properties [205]. It has been used in the context of this doctoral research to prepare thin polymer films (5 – 90 nm thick) serving as substrates for the fabrication of monolayer MoS_2 FETs. Figure 5.3b shows a topographic AFM image of a thin film of parylene C ($\sim$ 33 nm thick) deposited on a SiO_2/Si substrate. The height profile reveals nanometer-scale corrugations with peak-to-peak excursions exceeding 4 nm; however, deep pinholes were not found, indicating a complete coverage of the substrate surface.
The histogram of the height distributions is reported in figure 5.3c. It could be fitted to a Gaussian function with standard deviation Rq of $\sim$ 1.3 nm, i.e. two times larger than the thickness of monolayer MoS_2. AFM images acquired on MoS_2 flakes lying on such a rough

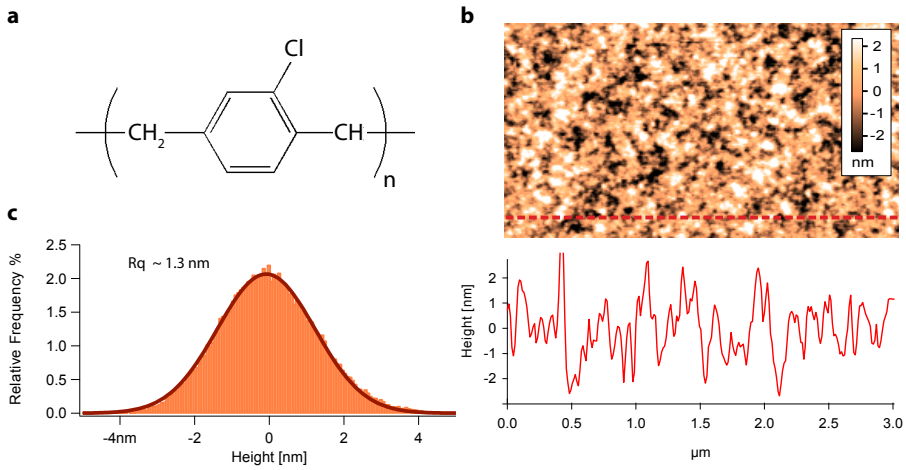

Figure 5.3: Surface morphology of parylene thin films. **a,** Chemical structure of the monomer of parylene C. **b,** Top: intermittent-contact AFM scan of a thin film of parylene C (~ 33 nm thick) deposited on a SiO_2/Si substrate. Bottom: height profile along the red dashed line, showing pronounced surface corrugations with peak-to-peak excursion exceeding 4 nm. **c,** Histogram of the height distributions. The fitting is done with a Gaussian function with standard deviation equal to Rq = 1.31 nm.

surface (appendix A.1) revealed that the substrate corrugations were not fully transferred to the overlying 2D material. This could be deduced from the fact that the roughness Rq of monolayer MoS_2 was on average 70-80 % smaller than that of the substrate, suggesting the presence of voids between the 2D semiconductor and the polymer film.

Other relevant characteristics of parylene are its low dielectric constant ($\varepsilon_r = 3.15$) and its high-energy polar optical phonons (~ 150 meV), which lead to the expectation of minimal RPS at room temperature [187]. Moreover, parylene is a hydrophobic and oxygen-free polymer. This helps limit the adsorption of water and allows suppressing the trapping from hydroxyl groups that are normally present on oxide surfaces.

The use of parylene as a substrate material alternative to SiO_2 was proven to be advantageous in the context of carbon nanotube (CNT) FETs [207], where it allowed restoring the intrinsic ambipolar transport of CNTs through a critical reduction of interfacial charge traps. Parylene was also employed in combination with graphene, where it enabled the realization of FETs with minimal hysteresis [208]. Furthermore, Hulea *et al.* [209] revealed that parylene is a convenient dielectric material for use in organic single-crystal transistors, thanks to its low polarizability that results in a weak coupling between charge carriers in the organic channel and polar vibrations in the polymer dielectric.

These several reasons have stimulated the investigation of parylene thin films as substrates for monolayer MoS_2. It will be shown in section 5.4 that FETs fabricated on the polymer films showed the highest RT mobility, up to 100 cm^2/Vs, proving that parylene allows reducing the level of extrinsic disorder and that surface roughness does not exert a major influence on charge transport.

5.3 Combining interface and defect engineering

Replacing the SiO_2 substrate with alternative dielectrics aims to reduce the level of extrinsic disorder associated with interfacial impurities, remote phonons and surface corrugations. Recent experimental studies have brought to light the presence of a considerable amount of defects internal to the MoS_2 sheets, both exfoliated [184] and CVD grown [185]. There is consensus in the research community that further progress in MoS_2 electronics will be enabled not only by improvements in the quality of the interfaces, but also by reducing the density of internal defects. This can be achieved mainly through the optimization of the growth/synthesis processes; however, researchers are developing as well defect-engineering strategies to decrease the level of disorder within the as-grown or as-exfoliated material. One example was recently provided by Yu *et al.* [175], who developed a thiol-chemistry based technique [188] to "repair" the most common type of defects in MoS_2, namely sulfur vacancies (SV). The method is relatively simple and consists in exposing the surface of the 2D material to a solution of thiol molecules, such as 3-mercaptopropyl trimethoxysilane (MPS, figure 5.4a). The latter has chemical formula $HS(CH_2)_3Si(OCH_3)_3$ and can react with sulfur vacancies according to following "vacancy healing" reaction

$$HS(CH_2)_3Si(OCH_3)_3 + SV = CH_3(CH_2)_2Si(OCH_3)_3$$

where the sulfur vacancy is repaired through the removal of the S atom from the MPS molecule. The reaction is favored by the weak S-C bond of the MPS molecule and by the

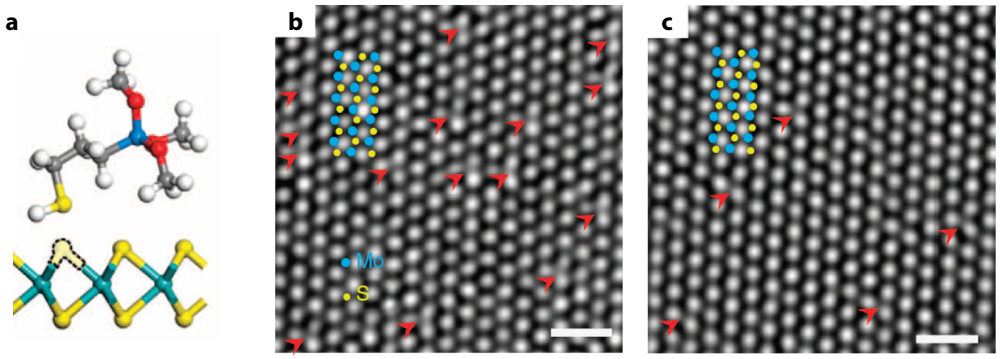

Figure 5.4: Defect engineering *via* thiol chemistry. a, Top: ball-and-stick model of MPS. C is gray, H white, Si blue, O red, and S yellow. Bottom: Schematic drawing of monolayer MoS_2 with a sulfur vacancy (SV). **b,c** Aberration-corrected high-resolution TEM images of mechanically-exfoliated monolayer MoS_2 before (**b**) and after (**c**) treating the top-surface with MPS. The red arrows highlight the SVs and the blue and yellow symbols mark the position of Mo and S atoms, respectively. Scale bar, 1 nm. The SV generation rate due to electron beam irradiation was $\sim 5.6 \times 10^{10}\,cm^{-2}s^{-1}$. Adapted with permission from ref. [175], © 2014 Nature Publishing Group.

high chemical reactivity of the SV sites [175]. The effective healing of the sulfur vacancies has been confirmed by aberration-corrected TEM investigations. Figure 5.4b and c show high-resolution TEM images taken before (b) and after (c) the thiol-chemistry treatment and prove the occurrence of a significant reduction in the density of sulfur vacancies, namely from $\sim 6\times10^{13}$ cm^{-2} to $\sim 1.6\times10^{13}$ cm^{-2}.

After reducing the density of sulfur vacancies in the MoS_2 samples, Yu *et al.* [175] adopted as well an interface-engineering approach. They used MPS for depositing a molecular self-assembled monolayer (SAM) on the surface of SiO_2, in order to minimize the influence of substrate-related sources of scattering. The combination of these approaches led the authors to the observation of an experimental RT charge carrier mobility as high as ~ 80 cm^2/Vs. Variable-temperature electrical transport measurements were performed on MPS-treated monolayer MoS_2 sheets lying on both SAM/SiO_2 and bare SiO_2. In addition, theoretical modeling was carried out to interpret the transport data and to shed light on the factors limiting the mobility. Due to their relevance with the work presented in this thesis, the main results of the investigation by Yu *et al.* are briefly summarized in the following.
It was found that electron mobility was limited by (i) localized trap states, (ii) ionized impurities and (iii) short range scatterers.
i) The trap states, which lie below the bottom of the conduction band, were ascribed primarily to sulfur vacancies. However, adsorbed species trapped between MoS_2 and the substrate were suggested as another possible source of trapping. These traps are known to be highly detrimental for the performance of devices, because they strongly limit the density of free carriers in the conduction band n_b compared to the total density of carriers n in the 2D material. It is worth noting that under this condition the field-effect mobility does not necessarily correspond to the mobility of free-carriers in the band [56] .
ii) The density of ionized impurities was found to decrease with both defect- and interface-treatment, suggesting that charged impurity scattering can be induced by both sulfur vacancies and impurities located on the SiO_2 substrate.
iii) Short range scatterers were straightforwardly related to sulfur vacancies. After traps and ionized impurities, they were found to be the most detrimental source of scattering, setting a mobility limit – not dependent on temperature – of the order of few 100s cm^2/Vs.

These results brought to light the critical importance of improving both interface and sample quality. To this purpose, the thiol-chemistry treatment was combined with the interface-engineering method based on dielectric substrates alternative to SiO_2. This combination has been investigated in the case of the dielectric material that offered the most promising results, namely parylene. Moreover, capacitance-voltage (C-V) measurements were carried out to explore the effect of the substrate on the density and distribution of the trap states. The methods and the outcome of the research are reported in the paper (Bertolazzi *et al.*, submitted, 2015 [187]) included in the next section.

5.4 High-performance monolayer MoS_2 transistors on thin polymer films

Manuscript submitted for publication.
Supporting information for the paper is available in appendix A

High-performance Monolayer MoS_2 Transistors on Thin Polymer Films

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ABSTRACT

Two-dimensional semiconductors are attracting a considerable interest because of the combination of a direct band gap and high degree of mechanical flexibility that could enable a host of new device applications. Critical for many of these applications are the charge carrier mobility and subthreshold behavior in transistors that can be degraded by the presence of band-tail states. We report here on the fabrication of monolayer MoS_2 transistors deposited on parylene that serves as the substrate and the gate dielectric. We achieve a room-temperature mobility of $\sim 100\,cm^2/Vs$. Capacitance-voltage measurements show a much narrower distribution of band-tail states in parylene than in devices based on oxide substrates while the subthreshold behavior can be further improved by sulphur vacancy healing. Because parylene can be easily integrated with flexible substrates, our results provide a way for achieving high room-temperature mobility in flexible devices based on MoS_2 and 2D semiconductors.

INTRODUCTION

Due to their excellent mechanical properties, low weight and optical transparency, two-dimensional (2D) materials are ideal candidates for applications in flexible transparent electronics such as displays, touch screens and wearable sensors [1–4]. In particular, monolayer molybdenum disulfide (MoS_2) is gaining increasing attention [5], as it offers a unique combination of high charge carrier mobility (theoretically up to $410\,cm^2/Vs$ at room temperature [6], high mechanical strength [7],

ultimate electrostatic control resulting in a high current ON/OFF ratio in a field effect geometry [8], and atomic-scale thickness, making it suitable for integration in highly flexible systems. Monolayer MoS_2 is also a direct band gap semiconductor [9–12] making it interesting for fabrication of optoelectronic devices such as photodetectors [13, 14].

Recent advances in large-area growth of MoS_2 [15–17] and the possibility of transferring them to arbitrary substrates [18], have stimulated intense research efforts towards the integration of MoS_2 electronic devices on bendable substrates. However, serious challenges remain to be solved. Among these is the fact that the experimental charge carrier mobility ($40-50\ cm^2/Vs$ at room temperature [19]) is still far away from the theoretical limit of $\sim 410\ cm^2/Vs$ set by intrinsic phonon scattering [6].

In field-effect transistors (FET), the charge transport can be affected by a number of factors, whose origin can be internal to MoS_2 (e.g. sulfur vacancies, dislocations and native impurities [20–22] that can give rise to trap states) or induced by the surrounding environment through external adsorbates [23] or through the supporting substrate. The latter can influence the electron transport *via* multiple scattering mechanisms, such as substrate-surface corrugations, remote interfacial phonons and substrate charge traps [24, 25]. There is presently an urgent need to shed light on the complex interplay among all these extrinsic factors in order to establish a roadmap for the improvement of MoS_2 electronic devices. In this context, the two approaches that have been followed to reduce the amount of disorder and boost the performance of MoS_2 devices are defect and interface engineering. The first approach aims to minimize the formation of defects during synthesis/growth, or to repair them by means of post-growth treatments. One such example is given by Yu et *al.* [26] who employed the thiol-chemistry treatment [27] to repair the sulfur vacancies in monolayer MoS_2, resulting in an improvement of the field-effect mobility of exfoliated flakes up to $\sim 80\ cm^2/Vs$. The second approach consists in tailoring the properties of the dielectric/MoS_2 interface through a careful choice of the supporting dielectric material. Ideally, the dielectric substrate should be flat, trap-free and characterized by high-energy optical phonons for minimal perturbation of the charge transport. Electronic devices based on monolayer MoS_2 are commonly fabricated on SiO_2/Si substrates and only few experimental investigations have been reported to date concerning the performance of monolayer MoS_2 transistors fabricated on substrates alternative to SiO_2 (e.g. ref. [28]). In the case of graphene, replacing SiO_2 with h-BN substrates [29] enabled extremely high quality graphene devices. In the case of monolayer MoS_2, it is still not clear to which extent it would be possible to improve the performance of FETs uniquely by removing the effects of the substrate. At present, the reported mobilities for suspended monolayer MoS_2 [30], MoS_2 on h-BN [28, 31] or MoS_2 in flexible devices[32] are not higher than those

for best devices on SiO_2 [33, 34].

Here, we show that record high room-temperature mobilities ($\sim 100\,cm^2/Vs$) in monolayer MoS_2 can be obtained using parylene, a typical substrate for applications in flexible electronics. Two particular properties prompted us to investigate parylene in this context. First is its hydrophobic nature that can limit the adsorption of water from the environment and help suppress charge trapping at the substrate/channel interface. This was successfully demonstrated in the case of carbon nanotubes [35] and graphene FETs [36, 37]. Moreover, the polar optical phonons at the parylene surface have been reported to be weakly interacting with the charge carriers in the channel of organic single-crystal transistors [38] and their energy is higher than in SiO_2 (150 meV *vs.* 60 meV in SiO_2) [38–41].

After reaching record-high room temperature mobilities using parylene substrates, we implement the sulfur-vacancy healing treatment recently proposed by Yu et *al.* [26]. In our case however, this did not result in an observable change in charge carrier mobility but we observed improved subthreshold characteristics of our FETs and were able to access intrinsic band transport at lower values of carrier density.

The effects of the substrate and of the sulfur-vacancy healing treatment were further explored by capacitance-voltage (C-V) measurements. Band-tail states similar to those reported in ref. [42] were also present in monolayer MoS_2 flakes deposited on parylene. However, their penetration length into the gap was found to be ~ 2.1 times smaller for parylene than for oxide-supported devices. The thiol-chemistry treatment had the additional effect of suppressing the hysteresis in the C-V curves due to a reduction in the number of slow traps related to sulfur vacancies.

RESULTS

Figure 1a shows the structure of a back-gated monolayer MoS_2 transistor with parylene gate dielectric. Thin films of parylene C were deposited by chemical vapor deposition polymerization [43] on top of 270 nm SiO_2 deposited on heavily n-doped silicon substrates. The thickness of the polymer films (typically between 20 and 70 nm) was measured by atomic force microscopy (AFM) after each deposition run. The surface morphology was characterized by AFM to ensure the uniform surface coverage, as well as to determine the roughness Rq of the polymer film, which was found to be in the 0.9 - 1.6 nm range. Thin flakes of MoS_2 were mechanically exfoliated directly on the parylene-coated substrates (Figure 1b) and identified through a combination of optical microscopy [44] and Raman spectroscopy (Supplementary Section 1). Multiterminal devices with Au (90 nm) or a Ti/Au (2/50 nm) contacts were defined through standard e-beam lithography as shown on Figure

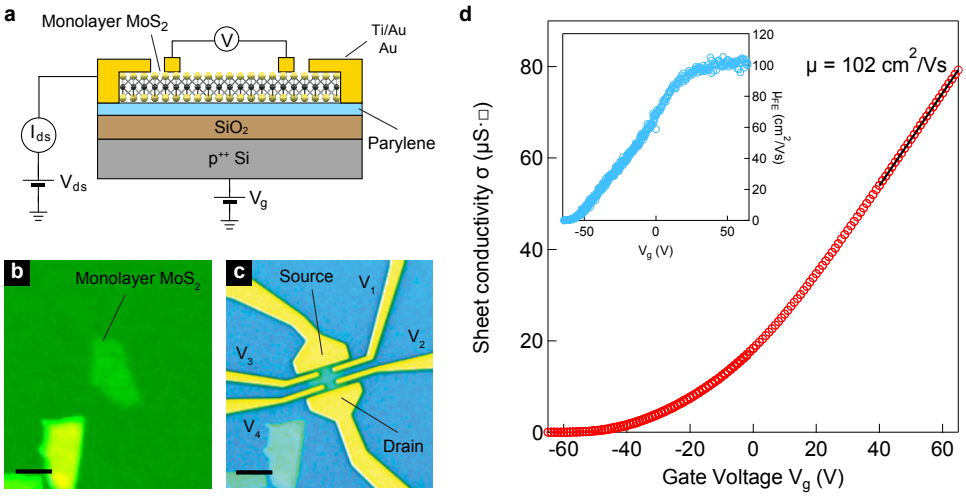

Figure 1: Monolayer MoS_2 on parylene thin films. **a,** Schematics of monolayer MoS_2 FETs fabricated on SiO_2/Si substrates coated with a thin polymer film of parylene C. The heavily doped silicon substrate is used as the back-gate electrode. **b,** Optical micrograph of a monolayer MoS_2 flake on 70 nm thick parylene-C film. **c,** Multiterminal device fabricated on the MoS_2 flake. Scale bars: 2 μm. **d,** Transfer characteristic (sheet conductivity σ *vs.* gate voltage V_g) obtained in the 4-probe measurement scheme ($V_{ds} = 50$mV). The curve was acquired immediately after vacuum annealing and cooling down to room temperature. Inset: field-effect μ as a function of V_g.

1c. Electrical characterization is performed in vacuum with a base pressure of $\sim 1 \times 10^{-6}$ mbar after annealing at 140 °C for 12 hours to remove gaseous adsorbates [45] and to reduce the contact resistance. The intrinsic sheet conductivity of monolayer MoS_2 was measured in the four-probe measurement scheme to remove the non-negligible contribution of the contact resistance. In this geometry, the sheet conductivity is given by $\sigma = (\frac{L_{12}}{W})(\frac{I_{ds}}{V_{12}})$, where L_{12} is the longitudinal spacing between the voltage probes, W the width of the channel, I_{ds} the drain-source current and V_{12} the potential drop between the voltage-probes. In Figure 1d we report the measurement of σ as a function of gate voltage V_g, performed immediately after annealing and cooling down to room temperature. The field-effect mobility was calculated from the slope of the σ *vs.* V_g curve, according to the equation $\mu_{FE} = (1/C_i)(\frac{d\sigma}{dV_g})$, where $C_i \sim 9.7\,\mathrm{nF/cm^2}$ is the capacitance per unit area of the gate stack with consists of 270 nm SiO_2 ($\varepsilon_r = 3.9$) in series with 70 nm thick parylene film ($\varepsilon_r = 3.15$). The inset shows the dependence of the mobility on gate voltage, where μ_{FE} saturates at $\sim 100\,\mathrm{cm^2/Vs}$ for $V_g > 40$ V. To the best of our knowledge, this value is the highest mobility for monolayer MoS_2 at room temperature reported so far in the literature. After electrical characterization, the devices are treated with (3-mercaptopropyl)trimethoxysilane (MPS) using the procedure described in ref. [26] and in the methods section.

In Figure 2a we report the room-temperature transfer characteristics of a monolayer

MoS_2 transistor on a 70 nm thick parylene film, before (red circles) and after (blue circles) the MPS treatment. After annealing, the threshold voltage V_{th} undergoes a strong negative shift [34], the current ON/OFF ratio is dramatically reduced [33] ($\frac{I_{on}}{I_{off}} = 22$ for V_g in the ± 60 V range) and the device can no longer be turned off. Treating the sample with MPS results in a positive shift of the threshold voltage; the device can now enter the OFF state at $V_g \sim -60$V and shows an ON/OFF current ratio of $\frac{I_{on}}{I_{off}} \sim 10^5$. Due to the non-negligible contact resistance R_c, the field-effect mobility extracted in the two-probe configuration ($\sim 50\ cm^2/Vs$) was found to be ~ 55 % of the four-probe mobility ($\sim 90\ cm^2/Vs$ for this particular device). At a gate voltage $V_g = 60$ V we found $R_c \sim 38\ k\Omega \cdot \mu m$. The corresponding σ *vs.* V_g curves are shown in Figure 2b. After the treatment (blue symbols) the conductivity is significantly lower than before the treatment (red symbols), a fact that can be ascribed to the aforementioned shift of V_{th}. However, at $V_g \sim 20$ V, both curves approach a linear behavior with identical slopes. This observation implies that (i) the mobility is not modified by the MPS treatment and that (ii) the carrier density required to access the intrinsic band transport is lowered by the MPS treatment. This can be understood considering that the carrier density can be evaluated using the expression $n = (\frac{1}{e}) \cdot C_i \cdot (V_g - V_{th})$. The gate voltage at which both curves start following a linear behavior is $V_g \sim 20$ V, while V_{th} lies at larger negative voltages before the treatment. Measurements of carrier density *via* Hall Effect (Supplementary Section 6) provide a value for insulator capacitance C_i of $9.5 \pm 1.9\ nF/cm^2$, in agreement with calculations. The effects of the thiol-chemistry treatment were further investigated by performing variable temperature electrical measurements on the MPS-treated devices on parylene. Figure 2c shows a series of σ *vs.* V_g curves acquired at different temperatures, ranging from 4 K to 300 K. As expected, the metal-insulator transition (MIT) occurs at conductivity values of $\sim 30 - 40\ \mu S \cdot \square$ ($\sim \frac{e^2}{h}$) , consistent with other reports in the literature [19, 33, 34]. However the carrier density n_{MIT} at which the transition occurs is relatively low and is estimated to be $\sim 6 \times 10^{12}\ cm^{-2}$ (compared to e.g. $n_{MIT} \sim 10^{13}\ cm^{-2}$ in ref. [19]). Devices fabricated on parylene that did not undergo the MPS treatment typically show $n_{MIT} \sim 8 \times 10^{12}\ cm^{-2}$ (Supplementary Section 7). It has been shown that n_{MIT} is related to the density of traps n_{tr} [26]. For $n << n_{tr}$, the localized trap states are not yet filled and the density of carriers in the conduction band n_b decreases exponentially with decreasing temperature [42]; under such condition (insulating regime), the overall temperature dependence of the conductivity is dominated by n_b. On the other hand, for $n >> n_{tr}$, all the trap states are filled; the Fermi level lies above the conduction band edge and n_b does not depend on temperature. Under such condition (metallic regime) the σ *vs.* T behavior is dominated by the temperature dependence of the band mobility. From this discussion, it is possible to see that $n_{MIT} \approx n_{tr}$. Therefore, the

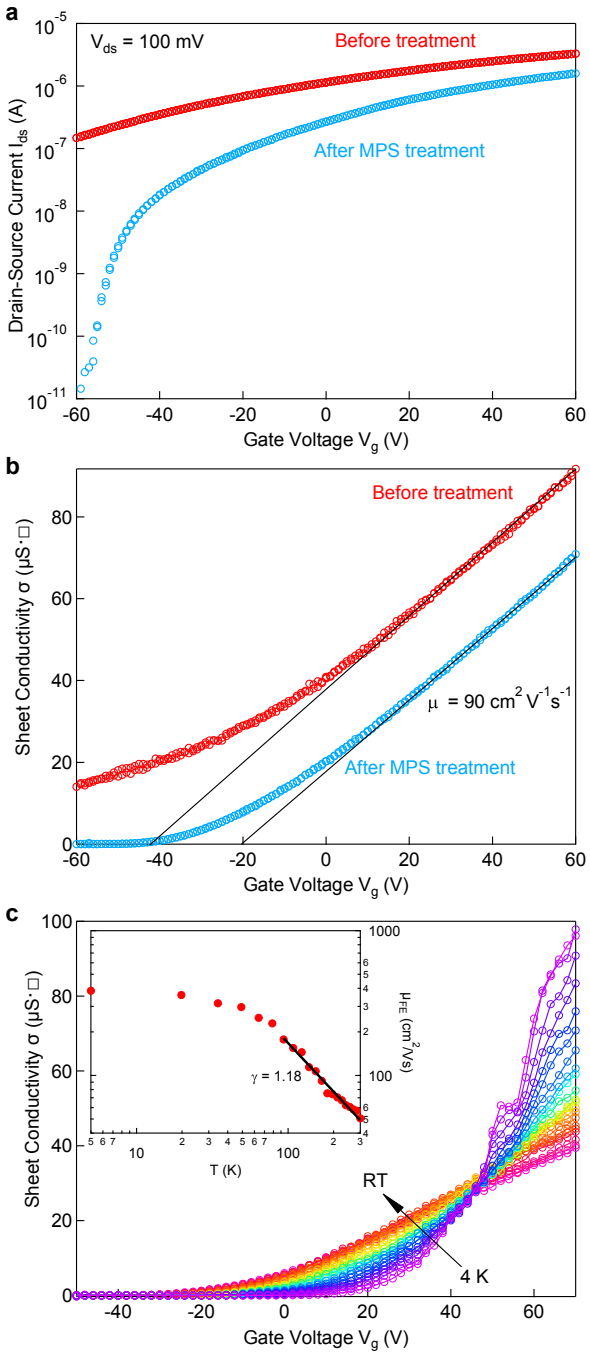

Figure 2: Effects of the MPS treatment on the electrical characteristics of MoS_2 FETs. a, Transfer curves (drain-source current I_{ds} *vs.* gate voltage V_g) for a monolayer MoS_2 FET on parylene. The curves were acquired on the same device before (red symbols) and after (blue symbols) the MPS treatment. **b,** Sheet conductivity σ *vs.* gate voltage V_g curves obtained with the 4-probe method before and after the MPS treatment. **c,** Transfer curves were acquired at different temperatures (from 4 K to 300 K) for the MPS-treated device. The curves intersect at the metal-insulator-transition point ($n_{MIT} \sim 6 \times 10^{12}\,cm^{-2}$ and $\sigma_{MIT} \sim 35\,\mu S \cdot \square$) . The inset shows the extracted field-effect mobility μ_{FE} as a function of temperature. The black line represents the fitting of mobility with the expression $\mu \propto T^{-\gamma}$ where $\gamma = 1.18$ is the temperature damping factor. Device dimensions: $L = 5.05\,\mu m$; $L_{12} = 2.3\,\mu m$ and $W = 4.3\,\mu m$.

observed reduction of n_{MIT} after MPS treatment indicates a reduced trap density in monolayer MoS_2. The inset of Figure 2c shows the temperature dependence of the field-effect mobility extracted at large positive V_g, i.e. in the metallic regime, with low-temperature values up to $\sim 400\,\mathrm{cm}^2/\mathrm{Vs}$. Such a large value of low-temperature mobility is another signature of the reduced disorder. To furher explore the effects of parylene and MPS treatment on the trap density, we perform C-V measurements on metal-insulator-semiconductor (MIS) capacitors. The MIS devices (Figure 3a and Supplementary Section 2) were integrated on sapphire substrates in order to minimize fringing capacitive contributions. They consist of a local bottom gate (Au),

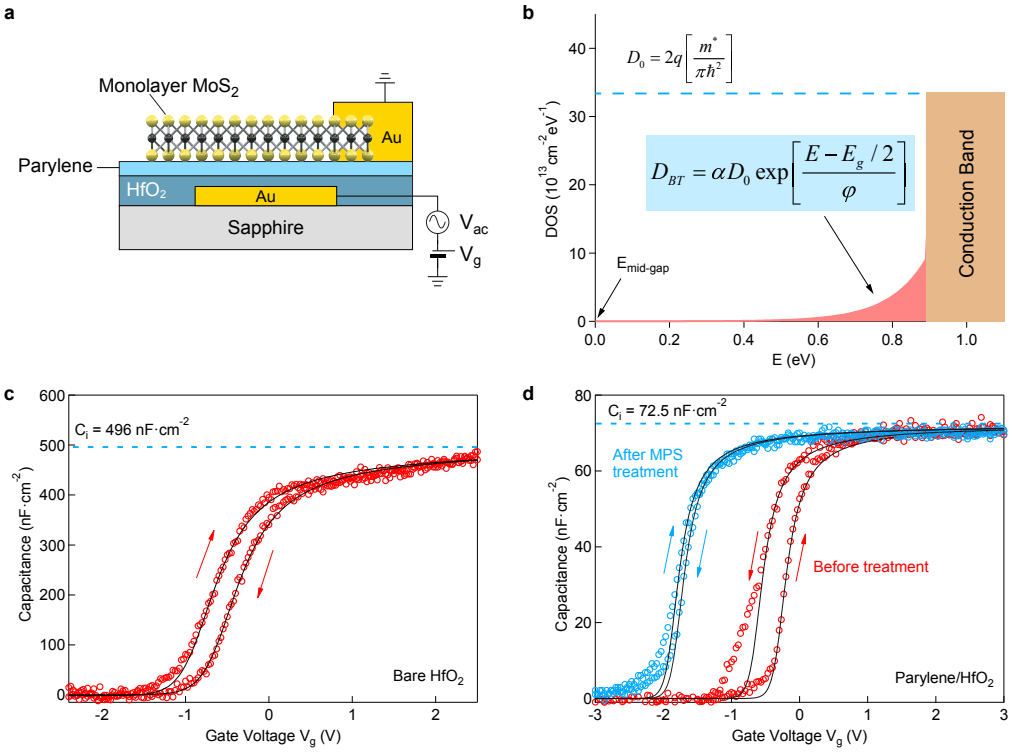

Figure 3: Capacitance-voltage measurements and the band-tail model. a, Schematics of the vertical heterostructure used for capacitance-voltage measurements, consisting of an Au back-gate electrode, HfO_2 insulating layer (30 nm) coated with 30 nm of parylene C and CVD-grown monolayer MoS_2. **b,** Band-tail model with the density of states of monolayer MoS_2. The origin of the energy scale corresponds to the center of the energy gap, where $E_g = 1.8\,\mathrm{eV}$. The parameter α determines the height of the band-tail (red) relative to the conduction-band density D_0; the extension of the tail inside the gap is set by ϕ. **c,** C-V characteristic of a vertical heterostructure without the parylene coating layer. The measurement was performed after vacuum annealing using an AC signal with frequency $f = 5\,\mathrm{kHz}$ and amplitude $V_{\mathrm{ac}} = 40\,\mathrm{mV}$. **d,** The same measurements as in (**c**) were performed on a device with a parylene coating layer, before (red) and after (blue) the MPS treatment. The dashed curves in (**c**) and (**d**) show the results of calculations based on the band-tail model. The arrows in both graphs indicate the direction of the gate-voltage sweep.

an insulating layer of HfO_2 (30 nm) coated with a thin film of parylene (~33 nm), and a triangular single-crystal of monolayer MoS_2 (edge size 5 to 20 μm) grown by chemical vapor deposition (CVD) on sapphire [46]. The use of CVD-grown MoS_2 allows us to fabricate devices with a larger surface area, resulting in a larger capacitance and higher signal/noise ratio for C-V measurements. The electrical contact to monolayer MoS_2 was realized with a top electrode (Au) contacting the MoS_2 triangle on a small edge area. All our devices were measured in vacuum ($\sim 1 \times 10^{-6}$ mbar) and underwent the same vacuum-annealing step for removal of adsorbates, which otherwise represent an additional uncontrolled source of trapping [23].

The capacitance between the bottom gate and the semiconducting MoS_2 channel was measured with the low-terminal (ground) connected to the top electrode and the high-terminal (small AC voltage superimposed to a DC voltage) connected to the bottom gate. We noticed that for AC excitation frequencies larger than $\sim$ 10 kHz, the C-V curves (Supplementary Figure S4d) are characterized by a pronounced frequency dispersion, which can be explained by the large resistance of monolayer MoS_2 near the band edge [47] with the full charging/discharging of the flake in response to the fast AC signal being hindered by the slow movement of electrons through the localized trap states. However, for low excitation frequencies ($\lesssim$ 10 kHz), the curves perfectly overlap. Therefore, in the following, we focus on the low-frequency C-V characteristics. Figure 3b shows the simplified model of the density of states (DoS) of monolayer MoS_2, which includes the band-tail states discussed in detail by Zhu et *al.* 42. These states can be described by the exponential distribution displayed in Figure 3b, where the height of the tail and its extension inside the bandgap can be tuned by the parameters α and ϕ, respectively. Using the band-tail model for the density of states and the values of the gate insulator capacitance C_i measured with the MIM structures (Supplementary Sections 2 and 5), we can calculate the C-V curves for different values of the two parameters and compare them with the experimental results. In Figure 3c, we show the measurement of the C-V characteristic of a MIS device where monolayer MoS_2 lies in contact with the bare HfO_2 surface. It can be seen that the calculated C-V curve for $\alpha = 0.3$ and $\phi = 150$ meV fits the experimental experimental data wery well. This is comparable with results obtained by Zhu et *al.* [42] ($\alpha = 0.33$ and $\phi = 100$ meV) for devices covered by Al_2O_3. In addition, we also observe a large hysteresis in C-V measurements, whose origin could be related to slow traps [48]. Additional C-V measurements were performed on MIS structures with a parylene coating layer (Figure 3d) before (red circles) and after (blue circles) the MPS treatment. The C-V curves before the treatment could be partially modeled using $\alpha = 0.3$ and $\phi = 70$ meV. However, a relatively large hysteretic loop can still be observed. Following the MPS treatment, the hysteresis is drastically diminished, as a consequence of the reduction of the

amount of sulfur vacancies. The experimental curves after treatment can be modeled by setting $\alpha = 0.3$ and $\phi = 70$ meV. This confirms that the total density of traps in the MPS-treated monolayer MoS_2 on parylene is about a factor of ~ 2.1 smaller than in the case of the bare HfO_2 surface.

At this point, substrate-surface corrugations do not represent a major performance limiting factor for monolayer MoS_2 devices. An AFM investigation (Supplementary Figures S1 and S2) conducted on exfoliated flakes on parylene revealed that the Rq of monolayer MoS_2 is on the average 70-80% smaller than the Rq of the bare polymer film, suggesting that MoS_2 is partially suspended, with the high in-plane stiffness of MoS_2 [7] being the likely reason. To shed more light on the role of the substrate roughness, we have fabricated a set of devices on ultraflat dielectrics, such as h-BN and sapphire, whose Rq values are reported in Table 1. The devices were fabricated following the methods described in detail in the Supplementary Sections 3 and 4.

Dielectric Environment	**Substrate roughness (nm)**	**Energy of the 1st optical phonon (meV)**
SiO_2	~0.3	~60
Sapphire/HfO_2	0.06-0.09	~48 /~12
h-BN	~0.1	~101
Parylene C	0.9-1.6	~150

Table 1: Properties of different dielectric substrates used in this study. Data for surface optical phonons are taken from the literature [38–41]. SiO_2 is included as a reference substrate. The substrate surface roughness was estimated from $2\,\mu$m $\times$ $2\,\mu$m AFM scans.

Figure 4a shows the room-temperature transfer characteristic σ *vs.* V_g of a monolayer MoS_2 transistor fabricated on a thin flake of h-BN (inset). The gate insulator stack ($C_i \sim 11.3$ nF/cm^2) consists of 270 nm of SiO_2 ($\varepsilon_r = 3.9$) in series with 36 nm of h-BN ($\varepsilon_r \sim 3.9$) [49]. From the linear fitting of the four-probe transfer curve, we extract a field-effect mobility $\mu_{FE} \sim 30$ cm^2/Vs. To our best knowledge this is the highest field-effect mobility reported so far for monolayer MoS_2/h-BN heterostructures [28, 50, 51]. We believe that this was made possible *via* a careful optimization of the heterostructure fabrication procedure, where the active area of the device

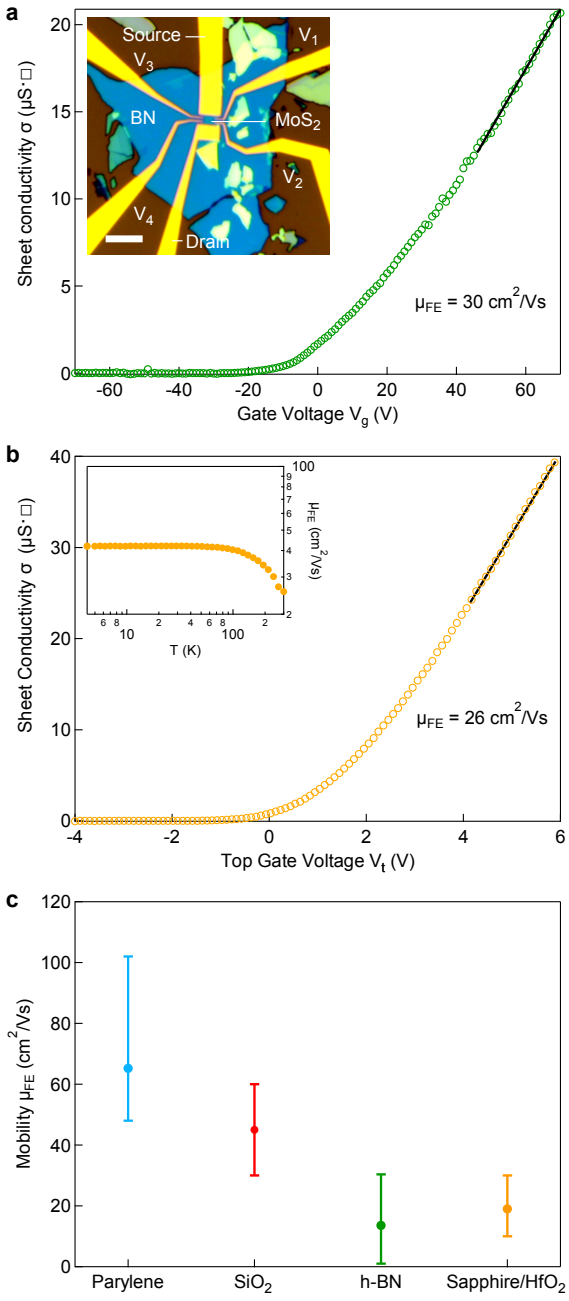

Figure 4: Monolayer MoS_2 FETs on ultraflat dielectric substrates. a, Transfer characteristic (sheet conductivity σ *vs.* gate voltage V_g) of the MoS_2-on-BN multiterminal device shown in the figure inset (scale bar of the optical micrograph: $5\,\mu m$). The device was annealed in vacuum prior to the measurement. **b,** Transfer curve of a top-gated multiterminal FET fabricated on sapphire (gate dielectric: 30 nm HfO_2). The inset shows the temperature dependence of the field-effect mobility obtained with the 4-probe method. **c,** Comparison between the room-temperature mobilities on different substrates (SiO_2 is included as a reference). For each substrate, the average values (full circles) and those of best/worst performing devices (error bars) are indicated. All the devices were measured after the vacuum-annealing step.

was selected in such a way as to be clean and free of transfer-induced ripples and bubbles (Supplementary Section 3). It is worth noting that the maximum sheet conductivity ($\sim 20\,\mu S\cdot\square$) at the highest gate voltage did not exceed the typical conductivity values at which the MIT transition occurs ($\sim 30-40\,\mu S\cdot\square$). Improvement of the gating efficiency, for example through fabrication of local gates with higher gate-insulator capacitance (compared to the SiO_2/h-BN stack), could allow further increase of the conductivity and enable the observation of the intrinsic band transport in monolayer MoS_2 on h-BN. We report on Figure 4b an equivalent transfer curve acquired on a top-gated device fabricated on atomically smooth [52] sapphire. As a top gate dielectric material we used 30 nm thick films of high-κ HfO_2. The room temperature field-effect mobility, evaluated from the transfer characteristics of several measured devices, span from 10 to 30 cm^2/Vs. At low temperatures, the mobility increases only up to $\sim 40\,cm^2$/Vs (Figure 4b, inset). Similarly to what has been recently reported for the case of graphene transferred on flat oxides [53], the electronic quality of monolayer MoS_2 transistors on sapphire is surprisingly low. This occurs despite monolayer MoS_2 being encapsulated in the sapphire/HfO_2 high-κ environment, which is expected to weaken the scattering potential of charged impurities [22, 25, 54]. We conclude that a much higher degree of extrinsic disorder exists in the case of MoS_2 devices fabricated on sapphire substrates. Even though we do not use a transfer procedure that could result in surface contamination, it is plausible that a larger number of adsorbates, e.g. water and molecular oxygen, are trapped between the MoS_2 monolayer and the hydrophilic sapphire surface (Supplementary Figure S10). Moreover, high-κ dielectric materials, such as HfO_2 and sapphire, are characterized by optical phonon modes with relatively low energies (12 meV and 48 meV, Table 1). Therefore, remote phonon scattering is expected to be more severe for these high-κ dielectrics than for standard SiO_2 or parylene. As discussed by Ma et *al.* [25], the benefit from using high-κ materials for screening the potential of Coulomb impurities can be entirely lost due to the detrimental effect of the polar optical phonons in the dielectric. Surprisingly, the relatively high surface roughness of parylene does not seem to negatively affect monolayer MoS_2 transistors, in comparison to other substrates shown on Figure 4c, and parylene substrates actually turn out to be superior to ultraflat sapphire or trap-free h-BN substrates.

CONCLUSION

In conclusion, we successfully integrated monolayer MoS_2 transistors on polymer substrates, where Rq can be more than two times larger than the thickness of the transistor channel itself. Our best performing device on parylene showed a

room-temperature field-effect mobility of ~ 100 cm^2/Vs . This is the highest value reported so far for conventional back-gated monolayer MoS_2 transistors. We showed that FETs fabricated on parylene thin films can outperform equivalent devices on conventional SiO_2 or on flat substrates, such as h-BN and sapphire. This allows us to conclusively rule out substrate surface corrugation as a major cause of mobility degradation in monolayer MoS_2 at this stage. C-V measurements performed on unencapsulated vacuum-annealed MIS devices revealed that exponentially distributed band-tail states are present regardless of the dielectric substrate used. However, the extension of the band-tail on parylene samples (ϕ = 70 meV) was found to lower than for bare HfO_2 (ϕ = 150 meV). By treating CVD MoS_2 monolayers with MPS molecules, we observed the suppression of hysteresis in C-V curves, which indicates a reduction of slow trap concentration. The same treatment performed on exfoliated monolayer MoS_2 allowed improving the subthreshold characteristics of the FETs and enabled reaching the intrinsic band transport at lower values of carrier density. All these results show that both interface and defect engineering are promising approaches for the realization of high-performance monolayer MoS_2 electronic devices.

METHODS

Device fabrication. Single layers of MoS_2 are exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide) using the scotch-tape micromechanical cleavage technique [55]. Monolayer MoS_2 has been grown by chemical vapor deposition (CVD) on C-plane sapphire with the procedure described in ref. [46]. Parylene films were deposited using a Comelec C-30-S parylene deposition system. AFM imaging was performed using the Asylum Research Cypher AFM. The root-mean-square Rq surface roughness of the different dielectric substrates was evaluated from 2 μm × 2 μm AFM scans. Thin flakes of MoS_2 were mechanically exfoliated from the bulk using the scotch tape method originally developed for graphene [56] and deposited directly on the parylene-coated substrates. Monolayer flakes were identified through a combination of optical microscopy [44] and Raman spectroscopy (Supplementary Section 1). Once an interesting monolayer flake had been identified and characterized, multiterminal devices were defined through standard e-beam lithography and lift-off procedure. As the contact material to MoS_2 we employed either Au (90 nm) or a Ti/Au (2/50 nm) metal stack. The devices were inserted into a vacuum chamber with a base pressure of ~ 1×10^{-6} mbar and annealed at 140 °C for 12 hours to remove gaseous adsorbates [45] and to reduce the contact resistance.

Electrical characterization of the devices was carried out using National Instru-

ments DAQ cards, SR570 current preamplifiers, SR560 low noise voltage preamplifiers, and an Oxford Instruments cryo magnetic system. C-V measurements were performed using Agilent E4980A Precision LCR Meter.

MPS treatment. Samples previously annealed in vacuum at 140 °C were transferred into an Ar-filled glovebox and annealed for several hours on a hot-plate at 120°C to desorb oxygen and water. Following annealing, they were immersed and left for 24h in a 1:15 solution of (3-mercaptopropyl)trimethoxysilane (MPS) (Sigma Aldrich) in dichloromethane. After treatment, the samples were moved back into the probe-station vacuum chamber where they were further annealed (140 °C for 12h) to remove the extra MPS molecules physisorbed on the MoS_2 surface.

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Author contributions. SB worked on device fabrication. SB and AA performed electrical characterization while DD performed CVD growth of MoS_2. SB performed AFM characterization while DD carried out Raman characterization. KW and TT performed h-BN synthesis. PG supervised Raman characterization. AK coordinated and initiated the work. All authors performed work on manuscript preparation.

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5.5 Summary and conclusion

The paper presented a method to implement high-performance monolayer MoS_2 FETs on polymer thin films. It was shown that the optimization of the substrate/MoS_2 interface by means of parylene enabled RT electron mobility up to $\sim 100\ cm^2/Vs$ for carrier density of $\sim 8 \times 10^{12}\ cm^{-2}$. This is at present the best value reported so far in the literature for conventional back-gated structures. The MPS treatment did not result in any further increase of mobility, but it allowed improving the subthreshold characteristics of the devices, consistent with a reduction of localized gap states. Comparison with devices fabricated on h-BN and sapphire allowed ruling out surface corrugation as a major cause of mobility degradation.

Charge traps. Capacitance-voltage (C-V) measurements – performed on vacuum-annealed MoS_2 samples deposited on parylene and on oxide surfaces – turned out to be a powerful technique to investigate the effect of the substrate on the density and distribution of the trap states. Three observations were reported in the paper. The first was the presence of a high-density of band-tail states [56] in all the specimens, regardless of the dielectric substrate used, suggesting a predominant internal origin of the traps (e.g. sulfur vacancies). This is in agreement with the conclusion drawn by Yu *et al.* [175], who also pointed out the possibility of contributions from other interfacial sources (e.g. adsorbates). In fact, the second observation was related to the narrower energy distribution of trap states in parylene as compared to the oxide surface, indicating that interfacial traps play as well a dominant role. In the case of the oxide substrate, additional trap states might be induced by hydroxyl groups or adsorbed molecular species (e.g. water) lying between MoS_2 and the substrate, and not efficiently removed during the vacuum annealing procedure. It is likely that the use of parylene limits the accumulation of these types of traps thanks to the oxygen-free chemistry and hydrophobic character of the polymer. Finally, the third observation was about the hysteresis in the C-V curves, which could be strongly reduced upon MPS treatment, pointing to the existence of slow traps corresponding to sulfur vacancies.

Surface roughness. The paper provided as well information on the role of surface roughness. Unexpectedly, FETs fabricated on the roughest substrate – parylene – provided the highest electron mobility at both high and low temperature, whereas devices fabricated on ultraflat sapphire and h-BN resulted in significantly lower performance. This clearly indicates that surface corrugations do not represent a major limit to the electron mobility, which is a this stage dominated by other extrinsic sources of scattering. In the following, the most important results for each dielectric substrate are reported.

Boron nitride. It was mentioned that the fabrication of monolayer MoS_2 FETs on h-BN

required a careful optimization of the flake-transfer procedure, which is necessary for assembling the MoS_2/h-BN heterostructure. In fact, flake-damages and hydrocarbon contamination induced during fabrication were found to severely degrade the charge carrier mobility, making the benefits from the trap-free h-BN substrate not easily observable. The paper reported a method for fabricating high-quality monolayer MoS_2/h-BN heterostructure devices, which enabled the achievement of a RT electron mobility of ~ 30 cm^2/Vs for carrier densities of $\sim 7 \times 10^{12}$ cm^{-2}. This is the highest value reported for this type of devices [195, 210], but it is still lower than the best results obtained using SiO_2 substrates ($\mu \sim 60$ cm^2/Vs). This fact highlights the critical role of the extrinsic disorder introduced during device processing, such as organic residue or transfer-induced bubbles/ripples (appendix A.3). It is worth mentioning that in the range of carrier density accessed in these experiments, namely $n \lesssim 7 \times 10^{12}$ cm^{-2}, it was not possible to enter the metallic regime, and the highest mobility at low temperature ($T = 10$ K) was of the order of ~ 15 cm^2/Vs. Further improvement is expected to be possible through the development of polymer-free fabrication techniques, based for instance on the full encapsulation of MoS_2 in h-BN sheets, in order to avoid exposure to acrylic resists. Increasing the gate-to-channel capacitance, e.g. by fabricating local back gates, was also suggested as a strategy to extend the carrier density range and access the band-like metallic transport in monolayer MoS_2/h-BN heterostructures.

Sapphire. The fabrication of FETs on sapphire substrates was carried out without making use of any transfer procedure, in an effort to avoid contamination and damages. Monolayer flakes of MoS_2 were mechanically exfoliated from the bulk and deposited directly on the transparent substrates by means of the scotch tape method. Thorough inspection of the sapphire surface by optical microscopy enabled the identification of 2D MoS_2 sheets, whose thickness was confirmed by both Raman spectroscopy and AFM. This allowed studying for the first time clean monolayer MoS_2 flakes with extremely low surface roughness, corresponding to that of the underlying substrate (Rq $\lesssim 1$ Å). The devices have been fabricated in the top-gate architecture, using HfO_2 as a gate dielectric material, and with direction of the current-flow oriented at different angles with respect to the terrace-edges (section 5.2.2). All the investigated FETs showed RT electron mobility included in the range $10-30$ cm^2/Vs and no dependence was found on the angle between the current flow and the sapphire steps, confirming the minimal influence of surface roughness. The high-κ HfO_2/sapphire dielectric environment, characterized by low-energy optical phonons, is expected to be a possible reason for the relatively low RT mobility. Lowering temperature down to 4 K resulted in mobilities as low as 40 cm^2/Vs in the metallic regime, indicating the presence of a high-density of traps or charged impurities, which could also play a significant role at RT [147, 180]. These are likely to be related to ionized impurities or electrical charges in the insulating substrate and to adsorbed molecular species trapped between the hydrophilic sapphire surface and the MoS_2 sheet, as brought to light by AFM

investigations (appendix A.4).

Parylene. Also in the case of parylene substrates, monolayer MoS_2 flakes were deposited directly on the polymer films using the scotch tape technique, resulting in clean 2D sheets. FETs fabricated on parylene showed the best RT electron mobility among all the investigated dielectric materials, indicating that the use of hydrophobic polymers allowed for an effective minimization of sources of disorder external to MoS_2, such as interfacial charge traps and impurities. Indeed, C-V measurements revealed that fewer traps were present on parylene compared to the oxide surface and low-temperature transport measurements showed a relatively higher electron mobility ($\sim 400\ cm^2/Vs$) consistent with a lower density of charged impurities.
Parylene has the additional benefit of high-energy polar optical phonons, suggesting that the RT carrier mobility is not limited by remote phonon scattering. The highest value obtained in this research work ($\sim 100\ cm^2/Vs$) represents a step forward towards the suppression of the discrepancy between experimental results and theoretical intrinsic limits ($130-410\ cm^2/Vs$, section 4.3). This progress was achieved uniquely through an interface-engineering approach, which highlights the need to continuously improve the quality of the interfaces.

Thiol-chemistry treatment. The charge carrier mobility extracted in the metallic state, above the MIT point, was not improved by the healing of sulfur vacancies (SV) with MPS molecules. This suggests that SVs are not the most detrimental source of scattering. However, they give rise to localized gap states that have to be filled by charge carriers prior to achieving band-like transport, resulting in poor subthreshold behavior and poor mobility at low carrier density. In this context, the MPS treatment revealed to be an effective method to improve the subthreshold characteristics of monolayer MoS_2 devices.

In conclusion, the paper illustrated a combined interface- and defect-engineering strategy to increase the charge carrier mobility and reduce the amount of traps internal and external to the 2D material. Following both directions was found to be essential for improving the overall performance of monolayer MoS_2 FETs.
Finally, the successful integration MoS_2 electronic devices on rough polymer films showed that 2D semiconductors are suitable for integration on common plastic substrates for flexible electronic applications.

6 Proof-of-concept device based on monolayer MoS_2 and graphene

6.1 Nonvolatile memory cells based on MoS_2/graphene heterostructures

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Nonvolatile Memory Cells Based on MoS_2/Graphene Heterostructures

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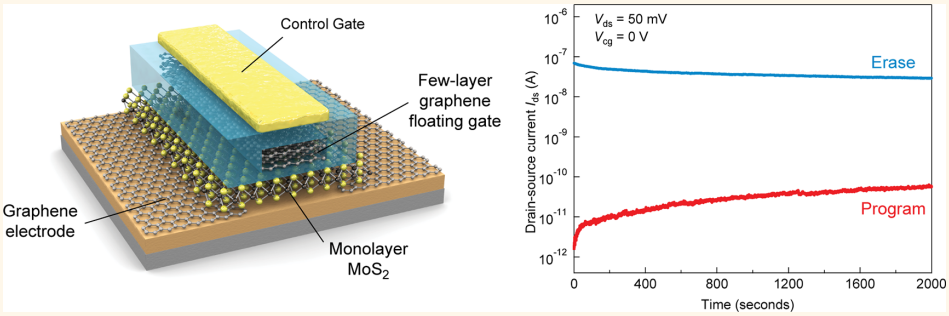
ABSTRACT



Memory cells are an important building block of digital electronics. We combine here the unique electronic properties of semiconducting monolayer MoS_2 with the high conductivity of graphene to build a 2D heterostructure capable of information storage. MoS_2 acts as a channel in an intimate contact with graphene electrodes in a field-effect transistor geometry. Our prototypical all-2D transistor is further integrated with a multilayer graphene charge trapping layer into a device that can be operated as a nonvolatile memory cell. Because of its band gap and 2D nature, monolayer MoS_2 is highly sensitive to the presence of charges in the charge trapping layer, resulting in a factor of 10^4 difference between memory program and erase states. The two-dimensional nature of both the contact and the channel can be harnessed for the fabrication of flexible nanoelectronic devices with large-scale integration.

KEYWORDS: two-dimensional materials · dichalcogenides · MoS_2 · graphene · nanoelectronics · memory · heterostructures

Two-dimensional materials, such as graphene and single layers of boron nitride (BN) or molybdenum disulfide (MoS_2), are the thinnest known materials with electronic properties that can be advantageous for a wide range of applications in nanotechnology.[1−6] Being only one layer thick, they represent the ultimate limit of scaling in the vertical direction and could offer reduced power dissipation because of smaller short channel effects.[7] They can also be regarded as a complete material library containing all the components necessary for building electronic circuits in which insulating BN could act as the substrate and gate dielectric barrier,[6] graphene as an interconnect while MoS_2 or another 2D semiconductor could play the role of a semiconducting channel.[4] Because graphene is semimetallic, it could form the ideal contact to 2D semiconductors, capable of supporting large current densities,[8] exceeding 10^9 A/cm^2 (ref 9). Furthermore, the lack of dangling bonds at the interface between graphene and 2D semiconductors would suppress the appearance of interface states and charge traps. As the graphene's work function can be electrostatically or chemically tuned,[10] it could also be adapted to a wide variety of 2D semiconductors with different work functions and band gaps. In this work, we demonstrate the integration of a 2D semiconductor in the form of monolayer MoS_2 with graphene electrodes. The basic device functions as a field-effect transistor, with ohmic contacts and performance comparable to similar devices with metal contacts.[4] Furthermore, this device can serve as a prototype for more advanced devices based on a 2D architecture. We demonstrate this by adding a charge trapping layer in the form of a multilayer graphene floating gate, resulting in a new heterostructure capable of operating as a nonvolatile memory cell.

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The use of 2D materials could offer immediate practical advantages for the realization of memory devices based on the floating gate transistor structure.[11] In current flash memory technology, serious hurdles need to be overcome to advance device miniaturization, both in the lateral and vertical directions. Vertical scaling leads to reduction of the program/erase voltages but is limited by the requirement of charge retention on the floating gate, which sets the limit for a minimum tunneling oxide thickness (~5 nm). On the other hand, lateral scaling, driven by the quest for higher data storage capability, is seriously limited by the capacitive coupling between the drain electrode and the floating gate, which results in a longer penetration of the drain field in the transistor channel[12] as the device is scaled. Furthermore, interference between neighboring cells leads to an undesirable spread in the threshold voltages of the devices.[13] The effect of capacitive interference can be significantly diminished through the reduction of the floating gate thickness,[14] while the reduction of electrode thickness can diminish the coupling between the electrodes and the floating gate. Because of this, it is extremely interesting to investigate the suitability of 2D materials for use in memory devices where they could replace traditional choices for semiconducting channels, interconnects, and charge trapping layers.

RESULTS AND DISCUSSION

Figure 1 shows the structure of our memory device, composed of two transistors fabricated on the same monolayer MoS_2 flake placed over graphene stripes acting as source and drain electrodes. A piece of multilayer graphene (MLG), 4−5 layers thick, separated by a 6 nm thick tunneling oxide layer (HfO_2) from the monolayer MoS_2 channel acts as the floating gate. We chose multilayer graphene as the floating gate because of its work function (4.6 eV) which is not sensitive to the number of layers and results in a deep potential well for charge trapping and improved charge retention. Furthermore, the low conductivity along the vertical *c*-axis suppresses detrimental ballistic currents across the floating gate,[15] while a higher density of states (>4.4 × 10^{13} cm^{-2} eV^{-1}) with respect to its single-layer counterpart (8 × 10^{12} cm^{-2} eV^{-1})[16] would allow more charge to be stored on it resulting in a larger memory window. The floating gate is further capped by a 30 nm thick blocking oxide layer at the top. The conductivity of the MoS_2 channel depends on the amount of charge stored in the floating gate (FG) and is modulated by the voltage V_{cg} applied to the control gate electrode (CG), which can also be used to vary the amount of charge stored on the floating gate.

The fabrication process includes three transfer steps.[17] Figure 1C shows the appearance of the device at several stages of the fabrication procedure. We start by growing graphene using chemical vapor deposition (CVD)[18] and transferring it onto a silicon substrate with

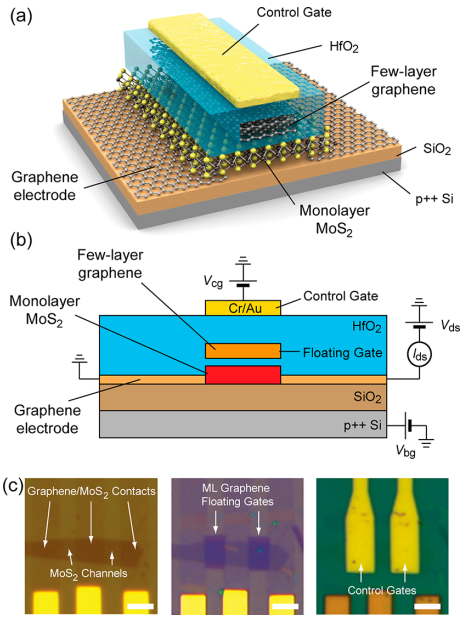

Figure 1. MoS_2/graphene heterostructure memory layout. (a) Three-dimensional schematic view of the memory device based on single-layer MoS_2. (b) Schematics of a heterostructure memory cell with a single-layer MoS_2 semiconducting channel, graphene contacts and multilayer graphene (MLG) floating gate. The MLG floating gate is separated from the channel by a thin tunneling oxide (*ca.* 1 nm Al_2O_3 + 6 nm HfO_2) and from the control gate by a thicker blocking oxide (1 nm Al_2O_3 + 30 nm HfO_2). (c) Optical micrographs of two graphene/MoS_2 heterostructure transistors fabricated on the same MoS_2 monolayer flake at various stages of fabrication. Left: single-layer MoS_2 transferred over an array of graphene stripes patterned on oxidized silicon chips and contacted with metal leads (Cr/Au: 10/50 nm); middle: the same device after deposition of the tunneling oxide and transfer/patterning of MLG floating gates; right: final device after the deposition of the blocking oxide and definition of the control gate electrodes (Cr/Au: 10/50 nm). Scale bars: 3 μm.

a 270 nm thick thermally grown silicon-dioxide (SiO_2) layer. Graphene is patterned into stripes and contacted with metal leads. MoS_2 is then exfoliated on another SiO_2/Si substrate covered with a sacrificial polymer layer. Individual layers are detected using optical microscopy[19] and transferred[20] on top of the graphene stripes that form the source and drain electrodes in direct contact with monolayer MoS_2. Fabrication continues with the deposition of the tunneling oxide layer on top of the MoS_2/graphene heterostructure, in the form of a 6 nm thick HfO_2 film grown using atomic layer deposition (ALD). We use a thermally oxidized Al seed layer[21] to facilitate the ALD deposition over graphene and MoS_2. Multilayer graphene flakes 1.5 nm thick are transferred onto the tunneling oxide and positioned above the MoS_2 flakes. Finally, the floating gate is capped by a 30 nm thick HfO_2 layer followed by the deposition of the control gate.

Figure 2a shows the small-bias current *versus* bias voltage (I_{ds} − V_{ds}) characteristic of one of our floating

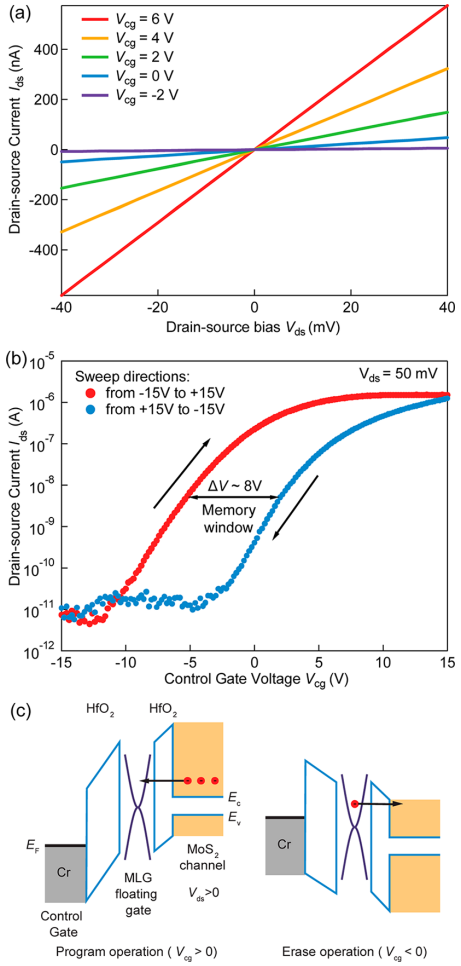

Figure 2. Device characteristics and charge trapping in the device. (a) Output characteristics (drain-source current I_{ds} *vs* drain-source voltage V_{ds}) of the floating gate transistor in the ON state, for different control gate biases V_{cg}. The curve linearity at small V_{ds} indicates that graphene acts as a ohmic contact to monolayer MoS_2. (b) Transfer characteristic (drain-source current I_{ds} *vs* control-gate voltage V_{cg}) of the floating gate transistor, acquired along two different control-gate voltage sweep directions. The large hysteresis of ~8 V is related to accumulation of charge in the MLG floating gate. The voltage sweep rate was 1.4 V/s. (c) Simplified band diagram of the memory device in program and erase states. Application of a positive control gate voltage V_{cg} programs the device. Electrons tunnel from the MoS_2 channel through the 6 nm thick HfO_2 and accumulate on the multilayer graphene floating gate. Application of a negative control gate voltage V_{cg} depletes the floating gate and resets the device.

gate transistors acquired for different values of the control gate voltage V_{cg}. The symmetry of the curves with respect to the origin and their linear behavior indicates the formation of ohmic contacts between graphene and monolayer MoS_2. This is due to a tunable and favorable graphene work function.[10] The relatively large current, on the order of 500 nA for a 40 mV bias, corresponding to a total series resistance of 125 kOhm shows that efficient charge injection from graphene to MoS_2 is possible even though the distance between the two is close to the interlayer distance in graphite (3.4 Å). This is in agreement with density functional theory-based calculations of the electronic structure of graphene/MoS_2 hybrids showing that charge transfer between graphene and MoS_2 is possible in spite of a lack of interaction and the relatively large interlayer separation.[22]

As this device is in two-contact configuration, we can only estimate the upper limit for the contact resistance from the highest recorded channel current during the gate voltage sweep shown on Figure 2a. From $I_{ds} = 1.5\ \mu$A, a bias voltage $V_{ds} = 50$ mV, and channel width of 3 μm, we estimate the upper limit for the contact resistance of 50 k$\Omega\cdot\mu$m. Future four-contact and transfer-length measurements will result in a more accurate measurement of contact resistance in this material combination. This value could be further reduced by chemical doping, local electrostatic control or the use of flat substrates. The use of graphene as a contact material for 2D semiconductors in place of thicker metallic films is expected to be advantageous as it allows fabricating devices and circuits[23] in a truly 2D architecture, using for example roll-to-roll printing and with reduced parasitic interference between neighboring devices and increased resistance to short-channel effects.[7] Work-function tunability[10] of graphene will allow it to be adapted to a wide variety of 2D materials. Furthermore, because it is chemically inert and mechanically flexible, graphene is the ideal noninvasive contact to other 2D materials.

The information storage capability of our device can be deduced from the transfer characteristics (drain current I_{ds} *versus* control-gate voltage V_{cg}), shown in Figure 2b, acquired in two sweeping directions, from negative to positive voltages (blue) and in the opposite sweep direction (red). The large hysteresis, characterized by a maximum voltage shift ΔV of approximately 8 V, is related to the charging/discharging of the floating gate in response to the control gate voltage. As the control gate voltage is swept toward high positive values (red curve), Fowler-Nordheim electron tunneling occurs from the channel into the floating gate through the HfO_2 oxide barrier, Figure 2c.[24] At this stage, electrons are accumulated in the floating gate and the device is in the program state. Accumulation of electrons in the floating gate results in a positive shift of the threshold voltage. This is observable from the blue curve, where the control gate voltage is swept in the opposite direction. As the control gate voltage V_{cg} reaches negative values, electrons are transferred back from the floating gate to the channel. For sufficiently high fields the floating gate is fully discharged, resulting in the erase state. For the purpose of reading the

memory state, zero voltage should be applied to the control gate (V_{cg} = 0). This would result in high drain current in the erase state and low drain current current in the program state.

Other hysteresis mechanisms[25] could be present in the device, but they can be ruled out as potential sources of such a high memory effect. Trapping states related to charge impurities present at the semiconductor/dielectric interface cannot generate a permanent threshold voltage shift. As shown in Figure 3a, we can generate permanent current/threshold voltage states characterized by varying memory windows ΔV by modulating the amount of charge stored in the floating gate. To calculate the threshold voltage shift, we define a reference erase state by assuming that the floating gate is not likely to accumulate positive charge (see Supporting Information). The floating gate can be depleted of all residual charge by sweeping the control gate voltage from 0 V to a low negative voltage, denoted as $V_{cg,min}$ (<−5 V). This places the device in the erase state. Immediately after floating gate depletion, we sweep the control gate voltage in the negative-to-positive direction, starting from $V_{cg,min}$ = −18 V, resulting in the black dashed line in Figure 3a, characterized by a threshold voltage $V_{th} \approx 0$ V. Repeating this voltage sweep results in a set of curves with no observable dependence of the V_{th} on the different values tested for $V_{cg,min}$.[17] This indicates that the multilayer graphene floating gate is not likely to accumulate positive charge (holes) in response to a negative voltage applied to the control gate. Hence, a reference *E* state with $V_{th} \approx 0$ V could be defined, corresponding to approximately zero charge stored in the FG. We can now reach different program (*P*) states by performing successive V_{cg} sweeps, stopping at gradually increasing maximum values of $V_{cg,max}$. Figure 3a shows a family of curves acquired in this way, corresponding to different program states characterized by their own memory windows. The threshold voltage shift ΔV (memory window), measured from the reference *E* state, is strongly dependent on the maximum control gate voltage, as can be inferred from the inset graph in Figure 3a. A maximum control gate voltage of +18 V results in a memory window exceeding 8 V. Gate leakage during these measurements is less than 10 pA and is within the noise limits of our instrument (see Supporting Information).

We estimate the amount of charge stored on the floating gate from the expression $n = (\Delta V \times C_{FG-CG})/q$, based on the charge balance equation,[26] where q is the electron charge, ΔV is the difference in the threshold voltage for read and erase states, while the C_{FG-CG} is the capacitance between the floating gate and the control gate, modeled as $C_{FG-CG} = \varepsilon_0\varepsilon_{bl}/d_{bl}$, with ε_0 the vacuum permittivity, ε_{bl} the relative dielectric constant of the HfO_2 blocking layer (~19), and d_{bl} its thickness (~30 nm). This results in a density of stored electrons

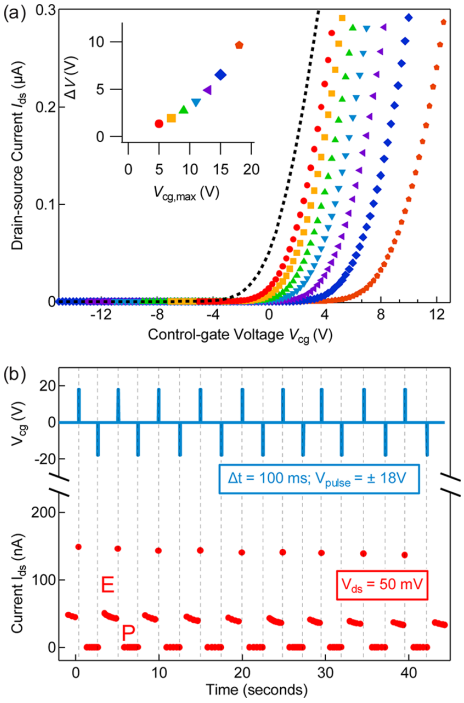

Figure 3. Memory states. (a) Dependence of the memory window on the control-gate voltage. Symbols: transfer characteristics (drain-source current I_{ds} *vs* control-gate voltage V_{cg}) of the floating gate transistor acquired from positive to negative control gate voltages V_{cg}, for different $V_{cg,max}$ (plotted in the inset). The drain-source voltage V_{ds} is fixed to 50 mV. Dashed line: transfer curve of the device in the erase state, corresponding to no charge stored on the floating gate. The inset graph shows the dependence of the memory window, related to charging of the floating gate, on the maximum voltage applied to the control gate. (b) Switching between erase (*E*, high current, device ON) and program (*P*, low current, device OFF) states induced by the application of alternating V_{cg} pulses (±18 V for 100 ms) with a time interval of 2.3 s. The application of a positive V_{cg} pulse (*E* → *P*) induces a drain-source current I_{ds} peak (130−150 nA) due to the increase of the charge density in the MoS_2 channel during the pulse.

on the order of ~2.8 × 10^{13} cm^{-2}. In agreement with Mishra *et al.*[14] and Hong *et al.*[27] we conclude that MLG, due to its higher density of states than in graphene, allows a larger memory window with strong potential for multilevel data storage.

We now test the dynamic behavior of our device, reported in Figure 3b. Switching between program and erase states is achieved through the application of voltage pulses to the control gate electrode, with the source grounded and the drain biased at 50 mV. The device is initially in the *E* state, corresponding to the ON current level. A positive voltage pulse (+18 V) with the duration of 100 ms leads to both accumulation of charge in the transistor channel, indicated by the ~150 nA current spike and to tunneling of electrons into the floating gate. When the control gate voltage is

reset to 0 V, the device remains in its program state, holding a stable OFF current. The application of a symmetric negative pulse (−18 V, 100 ms duration) 2.3 s later restores the initial erase state. We performed an endurance test measurement for our memory device, observing a well-defined and reproducible *P*/*E* switching for over 120 cycles. The slow decay of the ON current is presumably due to trapping mechanisms related to charge impurities present at the semiconductor/dielectric interface, as observed elsewhere.[25]

The stability of *E* and *P* states, crucial for nonvolatile information storage, was further investigated by monitoring their time-resolved behavior at a constant drain-source bias of 50 mV, reported in Figure 4. During the entire observation time, the corresponding erase state current was measured to be in the range 10^{-8}–10^{-7} A, with an exponential decay saturating to about 20 nA. After this measurement, the memory was programmed to the program state through a voltage pulse (V_{cg} = +18 V, duration 3 s), resulting in the OFF state of the drain current I_{ds}. Although slowly increasing with time, the I_{ds} current remained in the 10^{-12}–10^{-10} A range during at least 2000 s. Room for improvement can be identified in both lowering the density of charge impurities in and around the channel in order to stabilize the erase-state current and in improved engineering of the tunneling oxide layer to increase the retention performance.

For the program and erase states we measured a maximal program/erase (*P*/*E*) current ratio exceeding 10^4. Such a remarkable *P*/*E* current ratio not only allows easy readout of the device state, but also allows multilevel storage, where more than one bit of information could be stored in the memory cell in the form of several distinct floating-gate charge levels.

As the final step of our device characterization procedure, we studied the memory charge retention characteristics (Figure 4b), which are related to both the nature of the tunneling barrier and to the work function of the MLG. The latter determines the depth of the potential well for the electrons stored in the floating gate. After programming the memory through a positive pulse (V_{cg} = +18 V during 3 s), we measured the threshold voltage at different time intervals, determined using a linear fit of the transfer characteristics, as shown in the inset of Figure 4b. These curves were acquired in a narrow range of control voltage V_{cg}, from 0 to +12 V, in order to prevent undesired electron depletion/injection occurring at the floating gate. Successive voltage sweeps carried out immediately one after the other resulted in similar V_{th} values, confirming the fact that the measurement itself was not perturbing the system. We observe a threshold voltage variation from 7.5 to 5 V during a time period of 10^4 seconds. Assuming that the reference erase state is characterized by $V_{th} \approx 0$ V, we estimate that, after 10 years, 30% of the initial charge would still be stored on the floating gate. This result proves that the charge leakage from

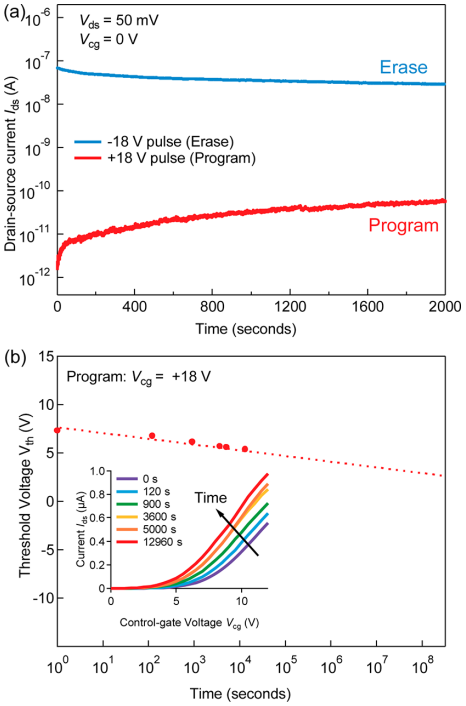

Figure 4. Device dynamics and charge retention. (a) Temporal evolution of drain-source currents (I_{ds}) in the erase (ON) and program (OFF) states. The curves are acquired independently for the program (10^{-8}–10^{-7} A) and erase (10^{-12}–10^{-10} A) current states and plotted on a common time scale. The drain-source bias voltage is 50 mV and the duration of the control-gate voltage (V_{cg}) pulse is 3 s. (b) Time-resolved behavior of the device threshold voltage after application of the programming voltage pulse (+18 V for 3 s). Threshold voltage was determined from linear fits to transfer curves (inset) in the linear regime. We estimate that after 10 years the device retains 30% of the charge stored on the floating gate.

the floating gate is slow on the time-scale of years and that the combination MoS_2/MLG indeed has a potential for application in nonvolatile memory technology. The value extracted for charge retention appears encouraging, considering that this is the first prototype of its kind. Further improvement can be achieved by means of a thorough engineering of the blocking oxide layer, using for instance novel insulating 2D crystals, such as BN or 2D oxides.[28]

CONCLUSION

We have demonstrated a new type of heterostructures based on 2D materials in which we use graphene as an ohmic contact to monolayer MoS_2 in a field-effect transistor geometry, paving the way toward the realization of truly 2D device architectures. The final device includes a multilayer graphene floating gate and operates as a nonvolatile memory cell. This demonstrates that it is possible to design memory devices using 2D building blocks, including contacts, floating gate, and

the semiconducting channel. Moreover, the excellent mechanical properties of 2D semiconductors such as MoS_2 (ref 29) can be exploited for fabrication of transistor circuits and memory devices on flexible substrates, with a naturally emerging range of related applications. Such devices could be produced massively and inexpensively using liquid-scale processing[30] or roll-to-roll printing[31] of CVD-grown material.[32,33]

METHODS

Single layers of MoS_2 are exfoliated from commercially available crystals of molybdenite (SPI Supplies Brand Moly Disulfide) using the scotch-tape micromechanical cleavage technique method pioneered for the production of graphene.[1] AFM imaging was performed using the Asylum Research Cypher AFM. Electrical characterization of the memory device was performed in ambient conditions at room temperature using an Agilent E5270B parameter analyzer.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Detailed description of the device fabrication procedure and additional characterization of the device. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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6.2 Comments on ACS Nano 7 (4), p. 3246, 2013

The unique physical properties of monolayer MoS_2 and other 2D crystals can be exploited to create novel technologies or to improve existing ones (section 2.4). This paper aims at providing a practical example of how the technological potential of 2D materials can be harnessed in flash memory devices. To this purpose, a proof-of-concept memory cell based on heterostructures of graphene and monolayer MoS_2 is presented. The advantages introduced by the 2D building blocks are highlighted throughout the paper.

The ultrathin form factor of monolayer MoS_2 and its sizeable bandgap offer high sensitivity to electrical charges stored in the floating gate (FG), enabling a remarkably large current ratio between the "program" and "erase" states of the memory cell, namely $\frac{I_{er}}{I_{pr}} \sim 10^4$. It is worth noting that such a high value cannot be obtained if graphene is used as the channel material, due to the lack of a bandgap, which represents the major obstacle to the realization of graphene-based flash memories. At the end of March 2013, soon after the publication of the paper, Sup Choi *et al.* [211] published a report on the fabrication and characterization of back-gated memory devices based on three-layer heterostructures of 2D materials. Graphene and MoS_2 (bottom ad top) were alternatively employed as channel and FG, while h-BN (middle) served as tunneling barrier. In agreement with the results reported in this thesis, it was found that the use of monolayer MoS_2 as channel material enabled $\frac{I_{er}}{I_{pr}} \sim 10^4$, whereas transistor channels made with graphene resulted in a much lower ratio, $\frac{I_{er}}{I_{pr}} \sim 2$, which is not suitable for application in flash memory devices.

Misra *et al.* [212] showed that multilayer graphene (MLG) can be conveniently employed as FG material. Thanks to its small thickness – of the order of few nm – and metallic conductivity, MLG has the potential to solve one the most serious problems that hamper the scaling of flash memory devices based on Si. Figure 6.1 shows a three-dimensional schematic view of two adjacent FG-FETs connected in series, as in the case of a Si NAND flash. The FG of one cell can interfere capacitively with the drain/source electrodes, as well as with the FGs of the neighboring cells. In particular, cell-to-cell interferences represent a highly detrimental influence, since they give rise to uncontrolled variations of threshold voltage among different cells. The best strategy to limit the effects of capacitive interferences consists in scaling the thickness of the FG. However, in conventional Si technology, reducing the thickness of the FG down to ~ 7 nm results in a ballistic leakage current through the FG, which severely degrades the reliability of the memory device [213]. In this context, MLG offers various advantages. It has the desired small thickness for minimal cell-to-cell interference together with a relatively high density of states ($\sim 4.4 \times 10^{13}\,\mathrm{cm^{-2}eV^{-1}}$ [212]) suitable for charge storage. Moreover, it is characterized by a low conductivity along the c-axis that helps suppress the ballistic leakage current.

A follow-up computational work by Cao *et al.* [11] showed that further reduction of cell-to-cell interference can be obtained by etching the MLG FG in the form of discrete nanorib-

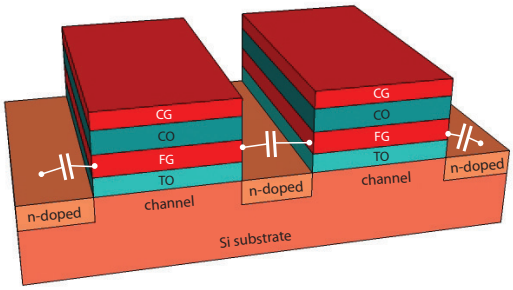

Figure 6.1: Parasitic capacitive interferences in flash memory devices. Three-dimensional schematic view of two adjacent FG-FETs built on a Si substrate. The vertical gate stack consists of tunneling oxide (TO), floating gate (FG), control oxide (CO) and control gate (CG). In conventional Si technology, the FG is made in poly Si. The capacitance symbols highlight the parasitic capacitive coupling between the FGs of two neighboring cells and between the FGs and the source/drain electrodes.

bons. In this geometry, only the ribbons laterally placed are severely affected by capacitive interferences, whereas those at the center of the FG are less affected, resulting in much lower cell-to-cell variations of threshold voltage. The same authors investigated the benefits associated with the use of 2D TMDs as channel materials. They showed that, besides providing great potential for scaling of FG-FETs, 2D TMDs in combination with MLG offer a new way to improve the charge retention in flash memory devices. The strategy consists in tuning the band offsets in the heterostructure by a careful choice of the 2D semiconductor. The latter should have an electron affinity significantly smaller than the work function of MLG (4.6 eV [212]) in order to reduce the probability of direct tunneling. Among the class of TMDs, the most suitable appeared to be WSe_2, which has a low electron affinity of 3.6 eV [214].

It seems clear at this stage that the combined use of MLG and 2D semiconductors can bring several advantages to flash memory technology. The paper aimed to spark renewed interest on this subject by demonstrating the first memory cell based on such combination of materials. It is worth to mention that there is still significant room for improving the electrical characteristics of the presented proof-of-concept device. For instance, a different choice of the tunneling and control oxide layers could lead to better retention characteristics and faster program/erase operations. Moreover, the deposition of dielectrics on 2D materials requires to be throughly optimized for reducing the amount of charge traps in the tunneling layer. These traps can severely degrade the performance of the memory due to trap-assisted tunneling mechanisms [11].

The paper also showed for the first time that graphene can be used as a contact material to monolayer MoS_2. This represents a step forward towards the realization of electronic device entirely based on 2D materials. The use of all-2D components could greatly facilitate the integration of memory cells in novel flexible and transparent electronic devices.

7 General conclusion and outlook

7.1 Summary

This thesis described experimental research focused on monolayer MoS_2, an emerging 2D semiconductor with newly recognized technological potential. Among the several applications envisioned for this material, one of the most appealing is certainly flexible and transparent electronics, where the ultimate thinness and the intrinsic semiconducting bandgap of monolayer MoS_2 could be exploited to great advantage. As it happens with all newly discovered materials, before considering a particular application, it is mandatory to perform a quantitative characterization of the relevant material's properties. To this purpose, a large part of this doctoral work has been dedicated to investigate the mechanical and charge-transport properties of this novel 2D material.

Mechanical properties. The AFM nanoindentation experiments reported in this thesis (Bertolazzi, Brivio and Kis, *ACS Nano*, 2011 [8]) represent the first measurement of the mechanical properties of 2D MoS_2. The physical quantities that have been accessed experimentally are the Young's modulus E and the breaking strength $\sigma_{\max}$ of free-standing monolayer sheets, corresponding to 270 ± 100 GPa and 23 ± 5 GPa, respectively. These values revealed that 2D MoS_2 is even stiffer that stainless steel ($E \sim 205$ GPa) and about 30 times stronger, suggesting that nanosheets of MoS_2 could be conveniently employed as reinforcement elements in composites. The experiments proved that monolayer MoS_2 is suitable for incorporation into flexible electronic devices. In fact, the maximum 2D isotropic strain that this material can withstand prior to breaking is $\sim$ 11%, whereas common substrate for flexible electronic applications, such as polyimide, typically breaks at lower strain levels ($\sim$ 7%). These experimental results have been subsequently confirmed by several theoretical and experimental studies (section 2.2.6).
Further research work is expected to be performed in the next years to characterize the mechanical properties of other 2D TMDs beyond MoS_2, which could offer similar mechanical

characteristics in combination with different electronic properties.

Charge transport properties. After the demonstration in 2011 of high-performance single-layer MoS_2 transistors (ref. [5]), the charge transport properties of MoS_2 and other 2D TMDs have made the object of intense research work. Several efforts have been stimulated by the promising combination of atomic-scale thickness and sizeable bandgap offered by these materials, which holds great potential for advancing the miniaturization of FETs beyond the limit of silicon technology (section 2.4.1). The most investigated property has been the charge carrier mobility, a critical parameter that determines in large extent the performance of electronic devices, such as FETs. In the case of monolayer MoS_2, a number of experimental and theoretical investigations have brought to light that a remarkable discrepancy exists between the predicted intrinsic phonon-limited mobility (~ 410 cm^2/Vs, section 4.3) and the experimental field-effect mobility ($\mu \sim 40-50$ cm^2/Vs, section 7) indicating that extrinsic scattering mechanisms dominate the overall transport properties. In this context, it is essential to identify the most detrimental sources of scattering, which could be internal to MoS_2 (e.g. sulfur vacancies) or located in the external surrounding environment. The latter is usually represented by a substrate and gate dielectric material that need to be carefully selected in order not to degrade the transport properties (section 4.5). The experimental investigations carried out in this thesis, consisting in the fabrication and characterization of FETs on different dielectric substrates (Bertolazzi *et al.*, submitted, 2015 [187]), provided new insights into the influence of external sources of disorder. Optimizing the semiconductor/dielectric interface, by minimizing the amount of interfacial charge traps and impurities, was found to be essential for reducing the gap between theoretical and experimental mobilities. The use of parylene substrates turned out to be the most convenient strategy to implement the aforementioned optimization, resulting in the highest mobility, namely ~ 100 cm^2/Vs at RT. This result was obtained despite the large surface roughness Rq of the polymer films – as high as two times the thickness of the monolayer – so that surface corrugations can be ruled out as a major cause of mobility degradation in 2D MoS_2. The use of the thiol-chemistry treatment developed by Yu *et al.* [175] to "repair" the sulfur vacancies did not result in any further improvement of the electron mobility, as extracted in the metallic transport regime ($n \gtrsim n_{MIT}$, section 4.4), pointing to the dominant influence of charged impurity scattering in this regime. However, the treatment allowed improving the subthreshold behavior of the devices, consistent with a reduction of localized trap states.
In conclusion, it was proved that high-performance monolayer MoS_2 FETs could be advantageously integrated on parylene films, which are as well convenient substrates for flexible electronics [206]. This further supports the suitability of 2D semiconductors for the envisioned flexible/transparent electronic applications.

Proof-of-concept device. The investigation of the charge transport properties of mono-

layer MoS_2 was conducted through the fabrication of FETs and its practical goal was to improve the performance of 2D transistors. This type of research can be viewed as lying in the middle between property characterization and device applications. On the other hand, the last part of the thesis focused entirely on device applications, providing an example of a proof-of-concept floating-gate transistor that exploits to advantage the properties of graphene and monolayer MoS_2. The nonvolatile memory cell developed in this doctoral research (Bertolazzi, Krasnozhon and Kis, *ACS Nano*, 2013 [171]) showed that the newly emerging class of 2D materials hold great potential for scaling of memory devices and for their integration on flexible substrates. The MoS_2 channel revealed to be highly sensitive to the presence of electrical charges in the floating gate, due to its ultrathin form factor and sizeable bandgap, and enabled a ratio between the currents in the "program" and "erase" states as high as $\sim 10^4$. Moreover, the use of few-layer graphene as charge trapping layer was shown to be advantageous for various reasons (ref. [11]). The most important is related to its small thickness ($1-4$ nm) that would allow reducing the parasitic capacitive coupling between neighboring cells, thus promoting further lateral scaling of memory devices. In the context of this research, it was demonstrated that graphene is a good contact material to monolayer MoS_2, resulting in ohmic-like current-voltage characteristics at RT. This represents a step forward towards the realization of all-2D electronic devices, where one could envision 2D TMDs employed as semiconducting transistor channels, graphene as contact and interconnect material, and h-BN – for instance – as gate dielectric insulator. Due to the ultimate thinness of each component, these devices would provide unique functional properties, among which a high degree of mechanical flexibility and transparency.

7.2 Challenges and prospects

Since 2011, tremendous progress has been made in the understanding of the physical properties of MoS_2 and other 2D TMDs. New interesting physics has emerged, such as the coupling between the spin and valley degrees of freedom, which is attracting growing attention due to the possibility to design combined spin- and valleytronic technologies. At the same time, a number of proof-of-concept devices have been demonstrated showing the effective benefits brought by 2D semiconductors in several technological applications, among which flexible (opto-)electronics, sensors, displays and solar cells, to mention a few examples. However, continuous advancement towards the manufacturing of real consumer products will require facing some serious challenges. Figure 7.1 displays a list of problems that are considered to be relevant hurdles and need to be addressed in the next years to enable further progress in the field of MoS_2 electronics. There is consensus in the research community that one of the major obstacle consists in the lack of large-area monocrystalline single layers with a minimal density of grain boundaries. The fast progress achieved in only a few years by means of CVD techniques offers the optimistic perspective

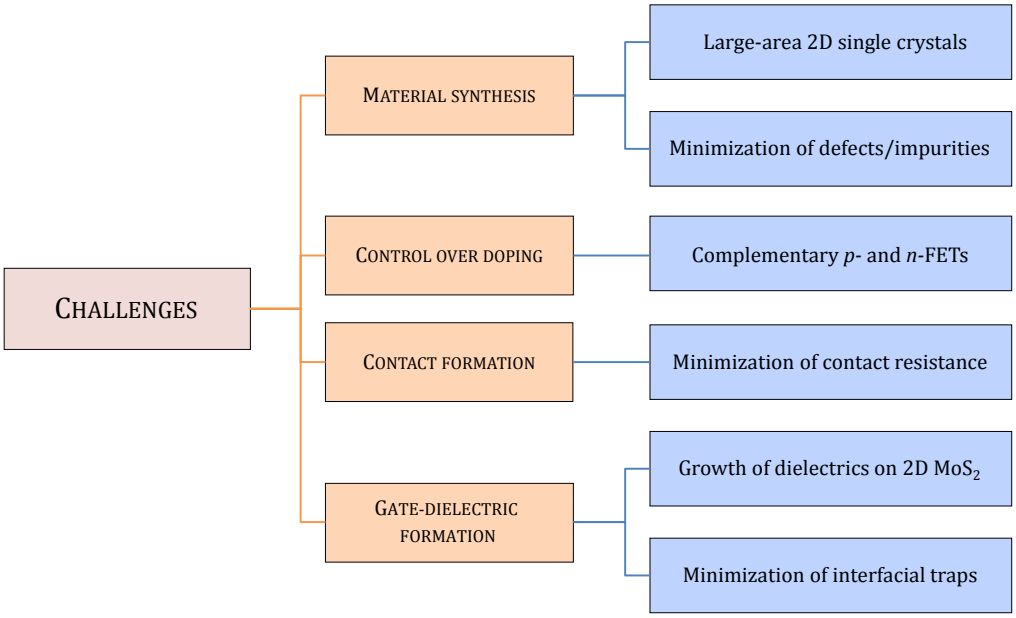

Figure 7.1: Major challenges to be faced in the next years. List of issues that need to be addressed to enable the large-scale manufacture of electronic devices based on MoS_2 and 2D semiconductors.

that this critical hinder might be soon overcome (section 2.3.2). During the synthesis process, it is also mandatory to reduce native impurities and internal defects (e.g. sulfur vacancies), which were shown to be highly detrimental to the charge transport properties of the 2D semiconductor.

At this stage, there is also no control over doping, a fundamental requirement for the development of digital electronic circuits based on complementary p- and n-FETs. Moreover, p-type transport in monolayer MoS_2 has not been observed yet, despite the use of high work-function contacts or liquid gating [215]. It is therefore necessary to develop robust strategies to acquire control over the doping levels in the material. Possible methods include the substitution of Mo atoms with other metal atoms – e.g. Re (donor) and Nb (acceptor) [183] – as well as the deposition of donor and acceptor molecules on the surface of the 2D material [189].

A large part of this doctoral work has been devoted to the investigation of the dielectric/MoS_2 interface in FETs. However, the same level of importance should be attributed to the metal/MoS_2 interface, where the presence of Schottky barriers can strongly limit the injection/extraction of charge carriers [193] resulting in a prohibitively large contact resistance R_c. According to the ITRS (section 2.4.1), the total source-drain parasitic resistance should be lower than $\sim 130\,\Omega\cdot\mu$m, whereas current MoS_2 FETs show R_c of the order of few 10s k$\Omega\cdot\mu$m. The limit becomes even more strict as the channel length L is decreased, since R_c should be much smaller than the ON channel resistance. Serious research efforts

have therefore to be made, especially in the perspective to reduce L below the electron mean free path ($\lambda \sim 15$ nm), which aims to overcome the performance limits imposed by the relatively low mobility of monolayer MoS_2 (section 2.4.1). A promising step forward has been recently reported by Kappera *et al.* [33], who developed a contact-engineering approach based on the local conversion of the 2H semiconducting phase into the metallic 1T phase (section 2.2.1) that enabled a significant reduction of contact resistance ($R_c \sim 200-300\,\Omega\cdot\mu$m).

For the large-scale manufacturing of FETs based on 2D TMDs, it is also necessary to develop suitable methods for the formation of the gate dielectric. For instance, due to the lack of dangling bonds on the pristine surface of monolayer MoS_2, the growth of oxide layers by ALD is not straightforward [196]. This requires performing a step of surface functionalization, e.g. the deposition of a "seed layer", to promote the uniform nucleation and growth of the dielectric material. The process has to be carefully optimized in order to avoid introducing interfacial charge traps and impurities. Such optimization is essential for preserving the mobility of charge carriers as close as possible to the intrinsic theoretical limit, as it was discussed extensively throughout this thesis.

The list of challenges outlined above might appear not so encouraging. However, the literature of the research field is reporting, almost on a daily basis, the occurrence of significant

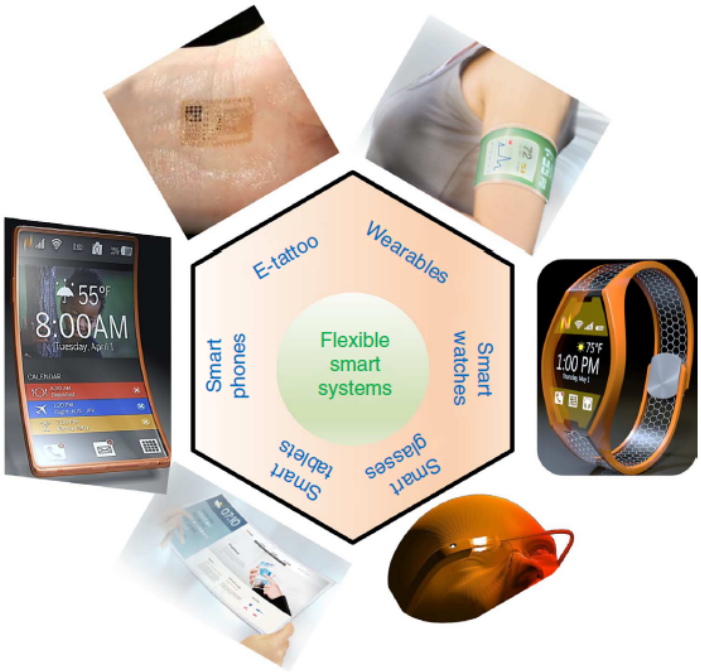

Figure 7.2: Flexible electronics on wearable and transparent systems. TMDs, graphene and other 2D materials can fulfill many of the optical, electronic and mechanical requirements for flexible smart systems. Adapted with permission from ref. [150], © 2014 Nature Publishing Group.

advancements, which stimulate researchers to undertake new efforts. It is worth noting that similar challenges have been faced as well in the case Si or III-V semiconductors. The broad experience matured in these fields could strongly facilitate the solution of the aforementioned problems and accelerate the path towards the first commercial products based on monolayer MoS_2 and other 2D crystals.

Among all the applications envisioned for these materials, low-cost flexible electronic devices are expected to be the most probable in the short term, because of their lower technological requirements [149, 150]. Figure 7.2 shows a few examples of flexible systems having the potential to create completely new markets in the next years. All these interesting and innovative products will be made possible only by the unique combination of mechanical, electronic and optical properties that are available in the newly emerging class of 2D materials.

A Supplementary information

Supporting Information for High-performance Monolayer MoS_2 Transistors on Thin Polymer Films

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1. Characterization of monolayer MoS_2 on parylene films

Thin films of parylene C were characterized by atomic force microscopy (AFM) to ensure the presence of uniform substrate coverage and to extract the values of the root-mean-square surface roughness Rq of the polymer films. The AFM scans shown in Figure S1a and b correspond to the topography of parylene and SiO_2, respectively. The values of Rq were obtained from AFM scans ($2\,\mu m \times 2\,\mu m$) acquired in the intermittent-contact mode.

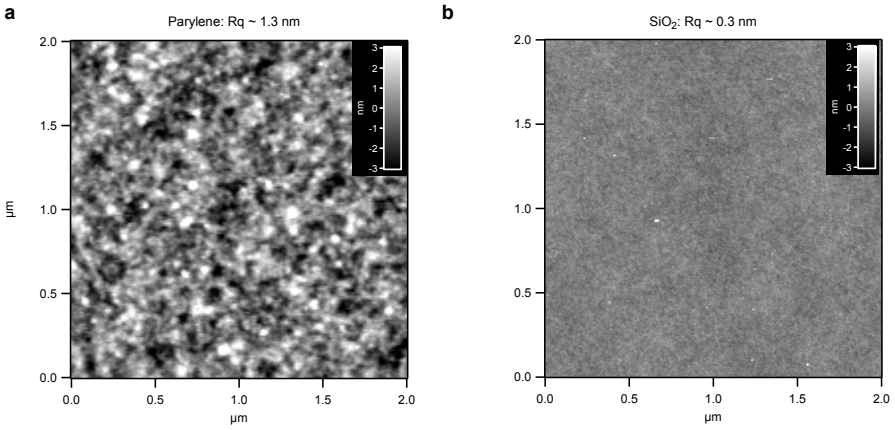

Figure S1: Roughness of parylene and SiO_2. AFM topographic image of the surface of **a,** ~ 33 nm thick parylene film; **b,** thermal SiO_2 with a thickness of 270 nm. The two AFM images share the same color height scale.

The hydrophobicity of parylene films was evaluated by measuring the static water contact angle θ. We obtained $\theta = 73° \pm 3°$ that is significantly higher than for SiO_2 ($\theta \sim 20°$) and sapphire (total wettability). Figure S2 presents an AFM scan taken at the edge of the monolayer MoS_2 flake shown in Figure 1 (main text).
It can be seen that it is difficult to determine the thickness of monolayer MoS_2 (~ 0.6 nm) from the AFM topographic image, since the thickness itself is more than two times smaller than the Rq of the underlying substrate. Therefore, ultrathin flakes were first identified with optical microscopy and successively investigated with Raman spectroscopy (Figure S3). The occurrence of a monolayer was confirmed by a difference $\Delta\omega$ between the E' and A_1' modes smaller than $20\,\mathrm{cm}^{-1}$ [1]. The unique

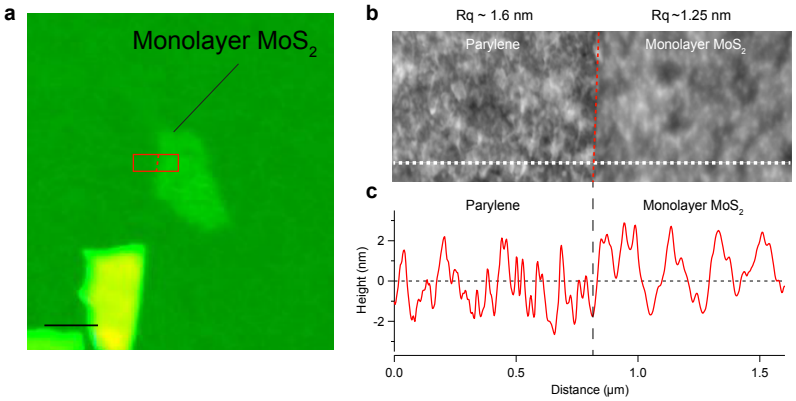

Figure S2: AFM characterization of monolayer MoS_2 on 70 nm thick parylene films. a, Optical micrograph of the monolayer MoS_2 flake presented in Figure 1 of the main text (scale bar, $2\,\mu$m); the red rectangle indicates the area of the AFM scan shown in **b**. **b,** Intermittent-contact AFM image of theMoS_2/parylene edge region. **c,** Height profile along the white dashed line shown in **b**.

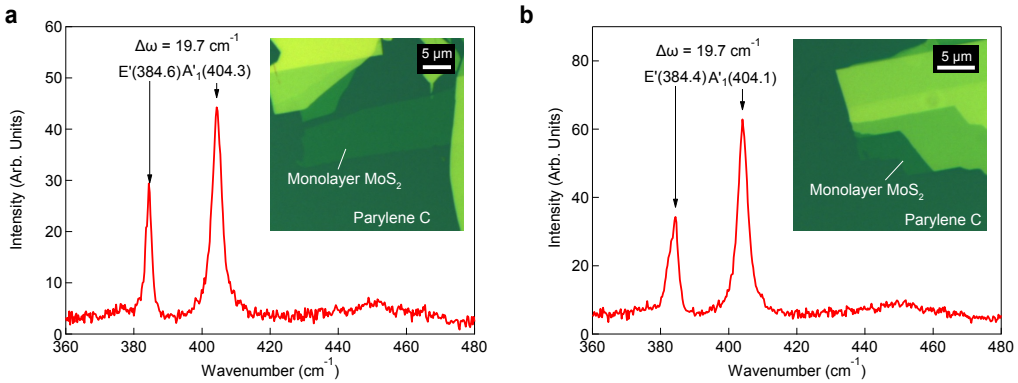

Figure S3: Raman spectra of monolayer MoS_2 on parylene. Raman spectra and optical micrographs of two monolayer MoS_2 flakes mechanically exfoliated using the scotch tape method and deposited on 70 nm thick parylene films. The difference $\Delta\omega$ between the E' and A_1' is smaller than $20\,\mathrm{cm}^{-1}$, indicating that the flakes have monolayer thickness.

optical contrast [2] of the identified monolayers compared to thicker flakes could then be used as a reference in the search of other monolayer MoS_2 flakes using optical microscopy.

2. Capacitance-voltage measurements

In this section we describe the fabrication of the MIS capacitors and the measurement of their C-V characteristics. Figure S4a shows the structure of a vertical MIS heterostructure integrated on an insulating sapphire chip. First, we pattern the back-gates using e-beam lithography, e-beam evaporation of Cr (2 nm) and Au (30 nm), and lift-off procedure. Then, we deposit a 30 nm thick film of HfO_2 by

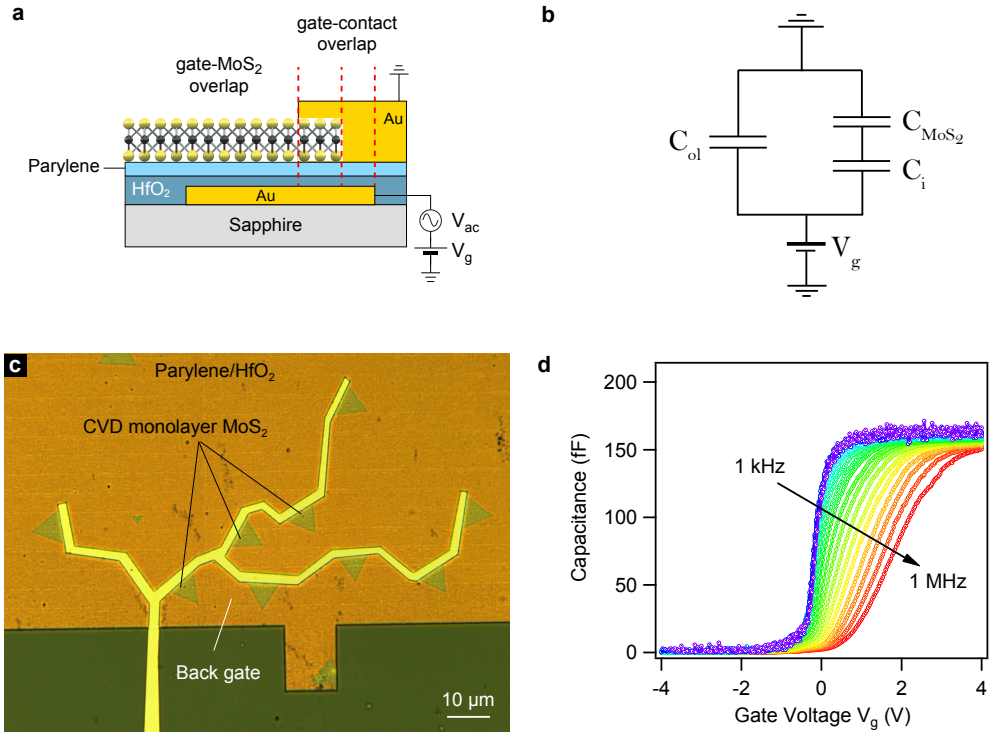

Figure S4: Devices for C-V measurements. a, Schematic structure of MIS devices used for C-V measurements. The top Au electrode touches MoS_2 triangular islands on a small edge area. The top and bottom metal electrodes overlap each other giving rise to a background capacitance C_{ol} that does not depend on gate voltage. **b,** Simplified electrical network of the device, including the capacitive contributions from (i) the overlap capacitance C_{ol}, (ii) the quantum capacitance of monolayer MoS_2 C_{MoS_2} and (iii) the gate insulator capacitance C_i. **c,** Optical micrograph of a MIS device with a parylene/HfO_2 insulating layer. Multiple triangles where connected in parallel in order to increase the capacitance signal. **d,** C-V curves of the device shown in **c**, acquired at different frequencies using an excitation signal with amplitude $V_{osc} = 40\,\mathrm{mV}$. For each curve, the V_g-independent background capacitance (C_{ol}) was subtracted.

atomic layer deposition (ALD) inside a reaction chamber held at 200 °C [3]. At this point, some of the samples were coated with a ~ 33 nm thick film of parylene C. Monolayer MoS_2 triangular sheets were grown on sapphire by CVD (ref.[4]) and then transferred onto the back-gate/insulator stack using a PMMA-based transfer method [5]. Finally, we pattern the top Au edge-contact (90 nm) to MoS_2 by e-beam lithography. Before each e-beam exposure step we deposit a thin layer of Cr (20 nm) on top of the resist in order to avoid pattern distortion due to electrical charging of the insulating sapphire substrate. On the same samples we have also fabricated a set of MIM capacitors (w/ and w/o parylene coating layer) by depositing a top metal electrode (Au) with a variable overlapping area. The capacitance of these structures was measured at a frequency of 5 kHz using a high-precision LCR meter. From the linear fitting of the capacitance $vs.$ area curves we extracted the gate insulator capacitance C_i equal to 72.5 nF $\cdot$ cm^{-2} (with parylene) and 496 nF $\cdot$ cm^{-2}. Knowing the thickness of parylene and HfO_2 films we could estimate the dielectric constant of HfO_2 ($\varepsilon_r = 16.8$) and of parylene ($\varepsilon_r \sim 3.15$). The latter was found to be in excellent agreement with the material specifications.

Figure S4b shows the electrical network of the MIS capacitor, which includes the quantum capacitance of monolayer MoS_2 connected in series with the geometric gate-insulator capacitance C_i. In the model, the device under test is connected in parallel with the overlap capacitance C_{ol}, which is due to the overlap between the top metal electrode and the back-gate. This capacitance gives a constant contribution that does not depend on the gate voltage.

In order to increase the capacitance signal, particularly in the case of samples with a parylene coating layer, we connected multiple CVD MoS_2 triangles in parallel (e.g. figure S4c) to augment the MoS_2 film area and to obtain a variation of capacitance from the OFF to the ON state ΔC significantly larger than the noise level in our set-up. One such example is shown in Figure S4c, where the background capacitance due to C_{ol} (i.e. the capacitance value measured in the OFF state) was subtracted from the acquired C-V curves. The plotted variation of capacitance ΔC is therefore referred to the OFF state value (Y axis origin). We performed C-V measurements at different frequencies, ranging from 1 kHz to 1 MHz. We found that the curves from 1 kHz (purple) to 10 kHz (dark blue) fully overlap each other, while strong frequency dispersion is observed for frequencies larger than 10 kHz.

3. Fabrication of monolayer MoS_2/h-BN heterostructures

Figure S5 shows a typical multiterminal field-effect transistor that comprises a heterostructure of monolayer MoS_2 and h-BN. The MoS_2/h-BN heterostructures were fabricated according to the procedure described in ref. [6], which involves the use

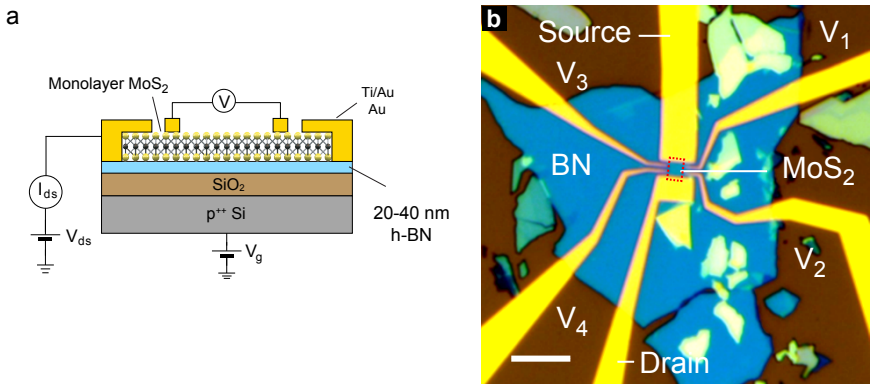

Figure S5: Monolayer MoS_2 transistors on h-BN. a, Schematics of a monolayer MoS_2 transistor on h-BN with inner voltage probes for measuring the intrinsic sheet conductance. b, Optical micrograph of a MoS_2/h-BN device fabricated on a 36 nm thick h-BN flake using Ti/Au metal contacts. The monolayer MoS_2 flake is indicated by a red dashed line.

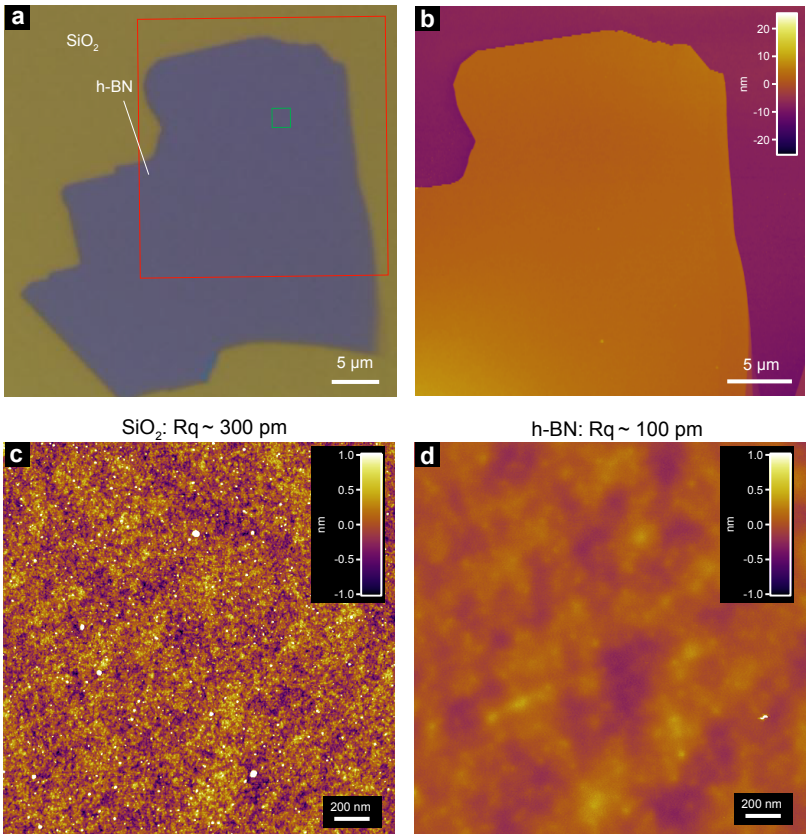

Figure S6: AFM Characterization of h-BN flakes. a, Optical micrograph of a thin flake of h-BN mechanically exfoliated and deposited on an SiO_2/Si chip. **b,** AFM topographic image of the area indicated by the large red square in **a** showing a clean surface with uniform thickness. **c,** AFM image taken on the SiO_2 region. **d,** AFM image of the h-BN region corresponding to the green square in **a**.

of a “dry-transfer” technique. First, thin flakes of h-BN are mechanically exfoliated from bulk crystals using the scotch-tape method and deposited on oxidized silicon chips (270 nm SiO_2). Large h-BN flakes (Figure S5), with thickness ranging from 10 to 40 nm, were identified by optical microscopy and characterized by AFM. High-quality h-BN flakes with uniform thickness and Rq between 0.1 and 0.15 nm were selected as substrates for our MoS_2/h-BN devices (Figure S6).

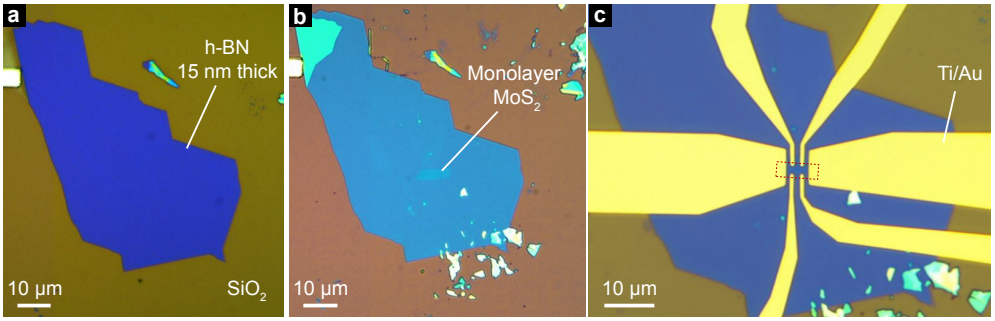

Figure S7: Fabrication of monolayer MoS_2/h-BN FETs. a, Optical micrograph of a thin flake of h-BN used as substrate and gate-dielectric material. **b,** Optical image of a monolayer MoS_2 sheet transferred on top of the h-BN flake. **c,** Optical image of the final devices with electrodes and voltage probes (Ti/Au, 2/55 nm). The red dashed line indicates the area of the monolayer MoS_2 flake.

Similarly, monolayer MoS_2 flakes were mechanically exfoliated from bulk molybdenite (SPI Supplies) and deposited onto SiO_2/Si chips coated with a polymer layer stack consisting of a sacrificial layer of polyvinyl alcohol (PVA) and a ~ 200 nm thick polymethyl methacrylate (PMMA) film. Monolayer flakes of MoS_2 are identified via a combination of optical microscopy and AFM. The sacrificial polymer layers supporting the MoS_2 flakes were subsequently dry-peeled off the SiO_2/Si chips and deposited onto a polydimethylsiloxane (PDMS) elastomer stamp. The latter was aligned with the target substrate in such a way that the MoS_2 flakes could be transferred on top of the selected h-BN flakes, as shown in figure S6. A thorough cleaning of the transferred flakes was performed through annealing in Ar atmosphere at 350 °C followed by AFM contact-mode mechanical cleaning [7]. Afterwards, Ti/Au (2/50 nm) source/drain electrodes and voltage probes were defined through standard e-beam lithography, metalization and lift-off. Bubbles and ripples induced during transfer represent a detrimental source of charge inhomogeneity. We used a combined AFM and optical microscopy approach to align/design our devices in such a way that only uniform regions of the MoS_2 flake are used as the transistor channel area. The result of this approach is shown in Figure S8.

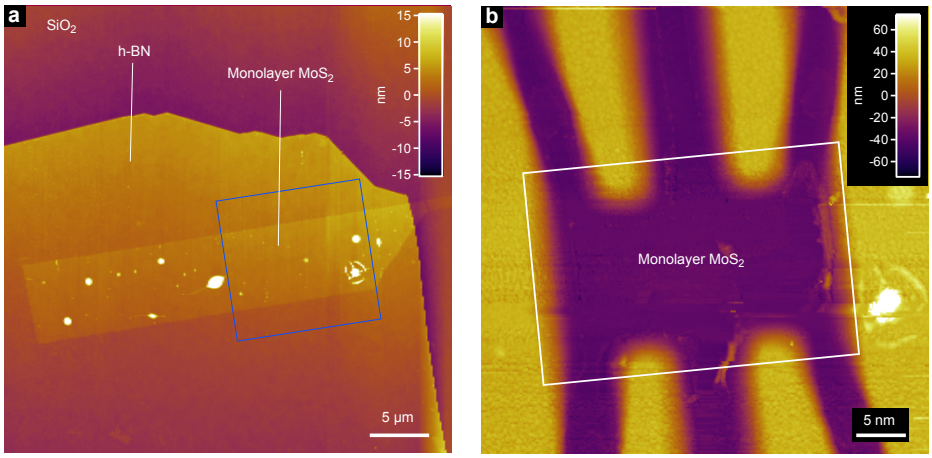

Figure S8: Selecting the active area of the devices. **a,** Example of an AFM image used to precisely align the electrodes with respect to bubbles and ripples. **b,** AFM scan of the fabricated device in the area indicated by the blue square in **a**.

4. Fabrication of monolayer MoS_2 transistors on sapphire

We describe here the fabrication of top-gated devices based on mechanically exfoliated monolayers of MoS_2 (Figures S9 and S10a). To preserve the quality of the exfoliated MoS_2 flakes we did not use any transfer procedure, in an effort to avoid additional defects and contaminants. Thus, we deposited the ultrathin MoS_2 flakes directly onto the sapphire surface and we conducted the monolayer detection on the transparent chips. Prior to deposition, we anneal the sapphire in air at $1000\,^{\circ}C$, resulting in atomically smooth sapphire surfaces [8] with $\sim 50-70$ nm (C-plane) and ~ 200 nm (R-plane) wide terraces due to a small miscut angle. We fabricate all the devices in such a way that current transport occurs along the terraces. We noticed that the monolayer MoS_2 flakes can be visualized with conventional

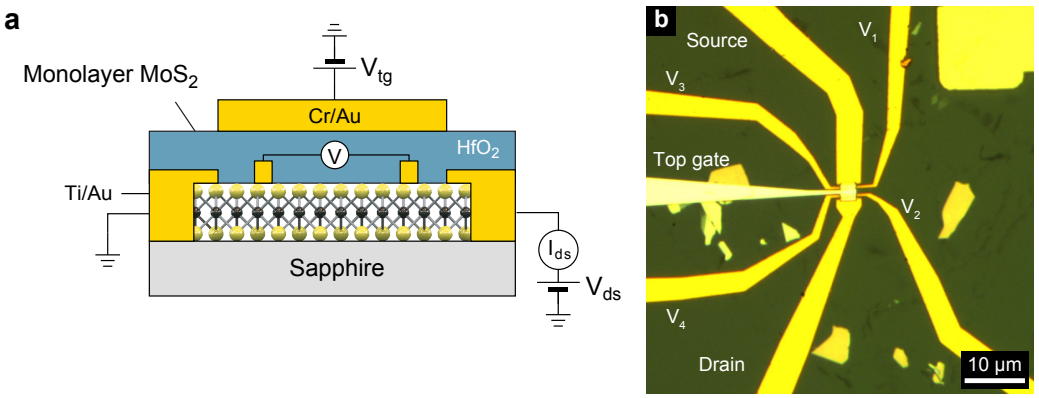

Figure S9: Monolayer MoS_2 transistors on sapphire. **a,** Schematics of a multi-terminal top-gated FET on sapphire with HfO_2 gate dielectric. **b,** Optical micrograph of a typical FET on sapphire.

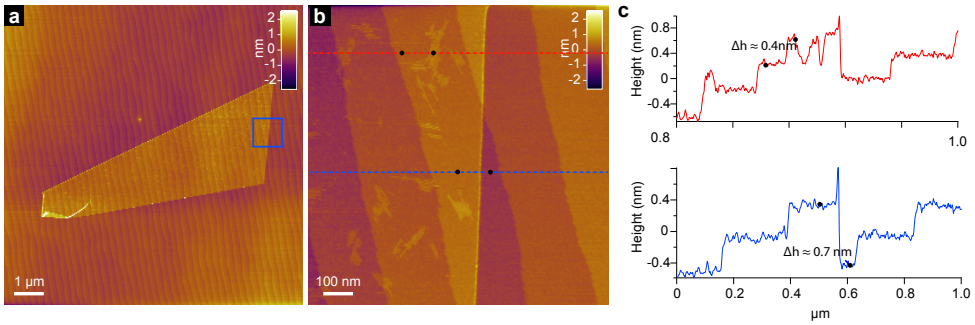

Figure S10: AFM characterization of monolayer MoS_2 on sapphire. **a,** AFM scan of a monolayer MoS_2 flake mechanically exfoliated and deposited on the R-plane surface of sapphire. **b,** Higher magnification AFM scan of the area indicated by the blue square in **a**. **c,** Height-profiles along the red line (passing through molecular adsorbates) and blue line (with no adsorbates) in part **b**.

reflection-mode optical microscopy under intense illumination conditions.

The thickness of the flakes was measured by AFM (Figure S10b) and confirmed by Raman spectroscopy. The electrical contacts (Ti/Au) and the top-gate electrode (Cr/Au) (figure 2B, main text), were defined with e-beam lithography. As a top-gate dielectric material we used 30 nm thick films of HfO_2 grown by ALD. The charge carrier mobility of the devices fabricated on sapphire was limited to $10-30\ cm^2/Vs$ at room temperature and $\sim 40\ cm^2/Vs$ at low temperature (4 K). This suggests the presence of a high density of impurities. It is plausible that a large amount of adsorbates, e.g. water and molecular oxygen, are trapped between the MoS_2 monolayer and the hydrophilic sapphire surface, which is known to be hydroxylated under ambient conditions [9]. This is supported by the AFM images of several monolayer MoS_2 flakes on sapphire (figure S10), where characteristic topographic features suggest the existence of a trapped molecular film of water (~ 0.4 nm thick), similar to previous reports of graphene on atomically flat mica substrates [10]. Moreover, the unintentional electrostatic charging of the insulating substrate – deduced from the frequent uncontrolled deflection of the AFM tip during scan – can also promote the absorption of ionic species from the environment or during the different steps of fabrication. It is also worth to note that capping the monolayer MoS_2 flake with HfO_2 is expected to hamper the removal of adsorbed species during the vacuum annealing step.

5. Calculation of capacitance-voltage characteristics

Figure S11 shows the band diagram of the MIS capacitor along the direction perpendicular to the heterostructure plane. V_g is the potential applied to the metal electrode and V_{ch} (red) is the channel potential referred to the center of the gap

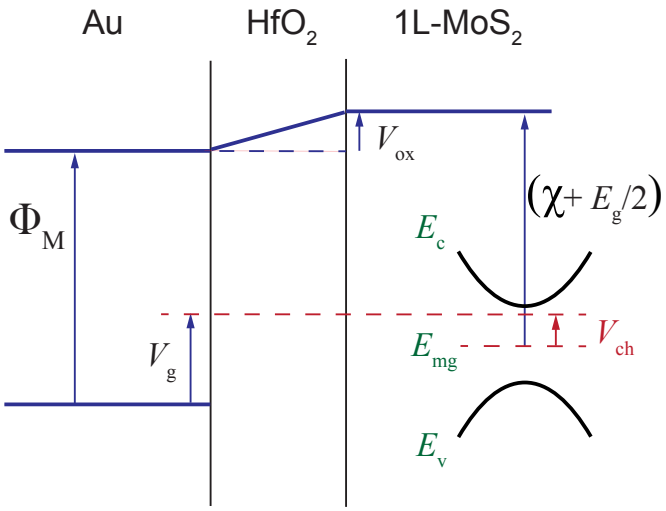

Figure S11: Band diagram of the MIS structure. Schematic representation of the band diagram of the MIS capacitor along the direction perpendicular to the plane containing the heterostructure.

E_{mg}, which is assumed to be located 0.9 eV (i.e. $E_g/2$) below the bottom of the conduction band E_c(green). Φ_m is the work function of the metal back-gate (Au) and χ is the electron affinity of single-layer MoS_2. The voltage drop V_{ox} across the insulating layer is given by:

$$V_{ox}(V_{ch}) = \frac{Q_{ch}(V_{ch})}{C_i} \tag{1}$$

C_i is the geometric insulator capacitance and Q_{ch} is the density of charge in the single-layer MoS_2 channel, which is described by the following function of V_{ch}:

$$Q_{ch}(V_{ch}) = e \int_{-\infty}^{+\infty} f_T(E - eV_{ch})\, D(E)\, \mathrm{d}E \tag{2}$$

where $f_T(E)$ is the Fermi function at a given temperature T and $D(E)$ is the density of states that includes the exponentially distributed band-tail states. The latter can be expressed as

$$D(E) = \begin{cases} D_0 = 2\,\frac{m^*}{\pi\hbar^2} & \text{if } E \geq Ec \\ \alpha\, D_0\, e^{\frac{E-Ec}{\varphi}} & \text{if } E < Ec \end{cases} \tag{3}$$

where m^* is the effective electron mass in single-layer MoS_2 and it is assumed to be 0.4 m_0. Therefore, the conduction band density $D_0 \approx 3.33 \cdot 10^{14}\ eV^{-1}\, cm^{-2}$. From the band diagram in figure S11 we obtain the equation that describes the

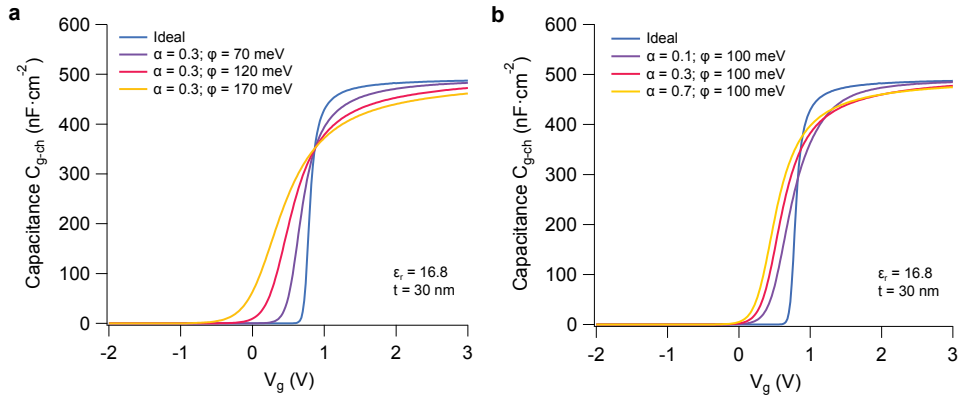

Figure S12: Calculation of capacitance-voltage curves. a, Calculated C-V curves for MIS structures with 30 nm thick HfO_2 insulating layer for different values of the parameter φ. **b,** Calculated C-V curves for the same MIS structures for different values of the parameter α. All the curves are calculated at $T = 300\,K$.

electrostatic problem, that is

$$\Phi_M + V_{\text{ox}} = V_{\text{g}} - V_{\text{ch}} + \chi + \frac{E_{\text{g}}}{2} \tag{4}$$

This includes the expressions (1), (2) and (3) and was solved with an iterative-loop numerical method that allows relating Q_{ch} and V_{ch} to the gate voltage V_{g}. Finally, the gate-channel capacitance $C_{\text{g-ch}}$ used for comparison with the experimental results is calculated as

$$C_{\text{g-ch}} = \frac{\partial Q_{\text{ch}}}{\partial V_{\text{g}}} \tag{5}$$

In figure S12 we present the results of our calculations for different values of the parameters α and φ, under the assumptions $\Phi_M = \chi + \frac{E_{\text{g}}}{2}$ and $T = 300\,K$. We show the effect of tuning the band-tail extension φ (figure S12a) and the band-tail height with α (figure S12b)

6. Hall effect measurements

In Figure S13a we report the measurement of the transversal resistance $R_{\text{xy}} = \frac{(V_4 - V_2)}{I_{\text{ds}}}$ as a function of the perpendicular magnetic field B. The measurement was performed at $T = 5$ K and $V_{\text{g}} = 65$ V. The offset resistance, due to the geometric mismatch between the voltage probes, has been removed using the transformation: $R_{\text{xy}} = \frac{R_{\text{xy,0}}(B) - R_{\text{xy,0}}(-B)}{2}$, where $R_{\text{xy,0}}(B)$ is the measured resistance. From the linear fitting of the R_{xy} *vs.* B curve we obtained a carrier density $n \approx 7.5 \times 10^{12}$ cm^{-2}. The values of carrier density extracted at different V_{g} are reported in Figure S13b.

From the linear fitting of the n *vs.* V_g plot we estimated the capacitance C_i of the parylene/SiO_2 stack and the residual carrier density n_0 at $V_g = 0$ V (indicated in the graph). The intersection with the x-axis occurs at $V_g \sim -60$ V, which corresponds to the room-temperature turn-on voltage V_{on} of the transistor, defined as the gate voltage at which a measurable current (≥ 1 pA) starts flowing in the device [11]. We observed this correspondence in several devices, suggesting that the carrier density measured via Hall effect can be correctly approximated by the relationship $n = (\frac{1}{e}) \times C_i \times (V_g - V_{on})$.

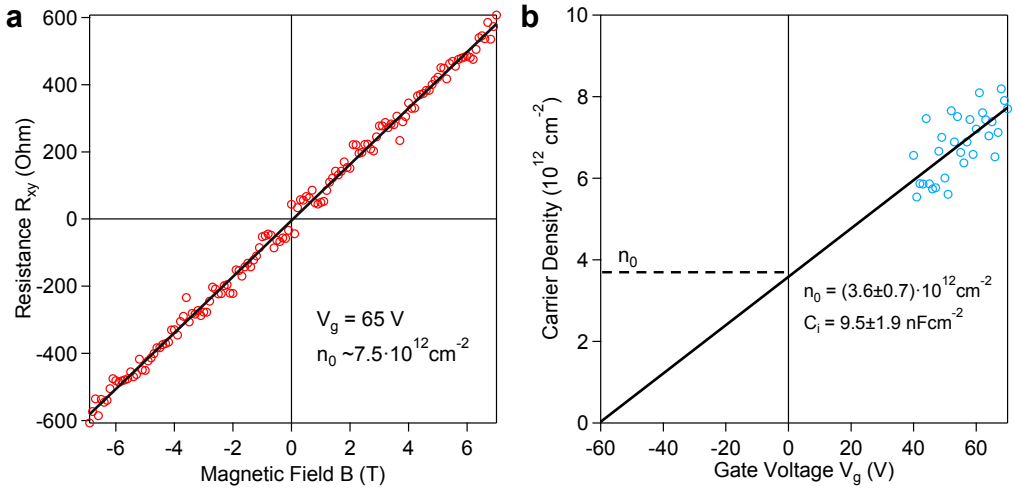

Figure S13: Hall Effect measurements. a, Measured transversal resistance R_{xy} as a function of perpendicular magnetic field B. **b,** Plot of the carrier density extracted from Hall effect measurements performed at different values of V_g. The linear fitting provides the value of the gate insulator capacitance C_i and residual carrier density n_0.

7. Metal-insulator transition in untreated FETs on parylene

The carrier density at the metal-insulator transition was estimated also for devices that did not undergo the MPS treatment. Figure S14 shows the variable-temperature transfer characteristics of a device fabricated on a 20 nm thick parylene film. The metal-insulator transition occurs at a gate voltage $\sim$ 60 V ($V_{on} \sim -55$ V), which corresponds to a carrier density $n_{MIT} \sim 8 \times 10^{12}$ cm^{-2}.

8. Output characteristics of high-performance monolayer MoS_2 FETs on parylene

In figure S15 we show typical output curves (I_{ds} *vs.* V_{ds}) acquired at room temperature in a monolayer MoS_2 transistor fabricated on a 70 nm thick parylene film.

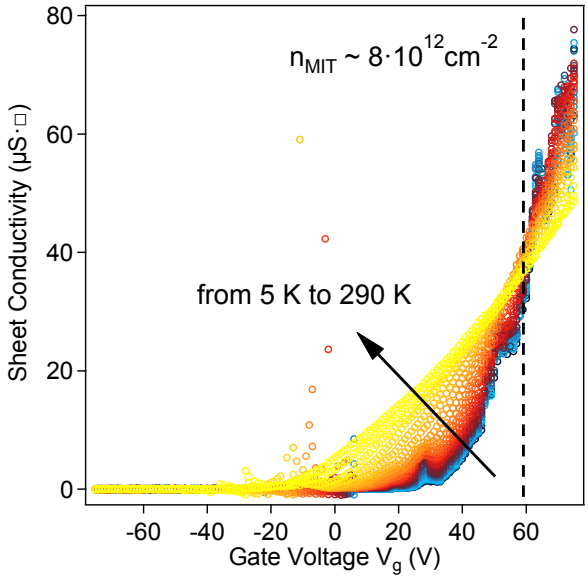

Figure S14: Metal-insulator transition in untreated FETs on parylene. **a,** Transfer characteristics (sheet conductivity σ *vs.* gate voltage V_g) obtained in the 4-probe measurement scheme at different temperatures. The device is fabricated on 20 nm thick parylene film deposited on 270 nm thick SiO_2 ($C_i \sim 11.7\,\mathrm{nF} \times \mathrm{cm}^{-2}$).

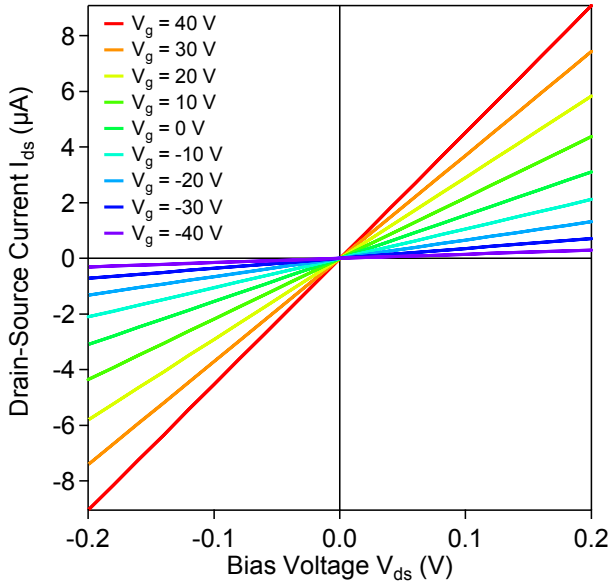

Figure S15: Output characteristics of FETs on parylene. I_{ds} as a function of V_{ds} curves acquired at different values of gate voltage V_g. The dimensions of the device are: $L = 2.4\,\mu\mathrm{m}$ and $W = 6.8\,\mu\mathrm{m}$.

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B Transfer and alignment of 2D materials

This appendix describes the techniques used for transferring ultrathin flakes of MoS_2 and other 2D materials on different substrates. Such techniques have enabled the realization of the most important structures and devices investigated in this thesis. For instance, the free-standing membranes employed for nanoindentation experiments (chapter 3) were prepared by transferring mono- and bilayer flakes of MoS_2 onto arrays of microfabricated circular holes. The measurement of the thermal conductivity by Raman spectroscopy (section 2.2.5) was performed on monolayer MoS_2 sheets transferred on perforated Si_3N_4 grids. Moreover, the assembly of MoS_2/h-BN heterostructures (chapter 5), as well as the fabrication of nonvolatile memory cells (chapter 6), required an intensive use of the transfer techniques.
Two different approaches were adopted, namely "wet" and "dry" transfer. The first involves exposing the 2D materials to a solution of potassium hydroxide (KOH). This can result in the adsorption of a large amount of ions (OH^- and K^+) and water, which is highly detrimental to the charge transport properties of the 2D materials (section 4.5). Hence, a second approach was developed to perform the transfer in a completely dry fashion. In this way, the ultrathin flakes enter into contact only with the supporting polymer film and are never exposed to liquids.
The two techniques are based on previous work by Brivio and Kis, who designed and implemented the experimental setup shown in figure B.1. This "transfer station" allows controlling the temperature of the "target" samples as well as their angle with respect to the flakes to be transferred. The x, y position of the substrate and the x, y, z motion of the glass slide holding the polymer film are controlled by a set of micromanipulators. A microscope objective with a long focal length enables an excellent visualization of both the substrate and the 2D sheets, which greatly facilitates the overall alignment procedure.

Wet transfer. The process flow for the "wet" transfer technique is illustrated in figure B.2. First, ultrathin flakes of MoS_2 or other 2D materials are exfoliated with the scotch tape method and deposited on the surface of an oxidized silicon chip (figure B.2a). On

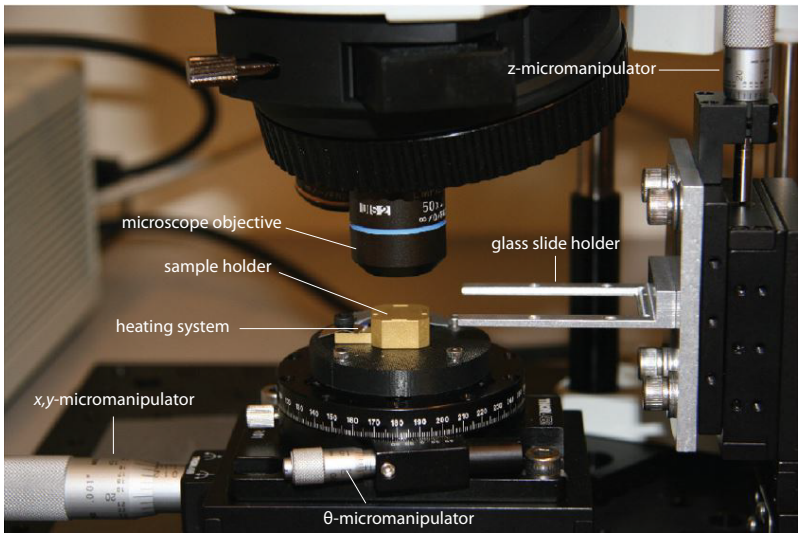

Figure B.1: Photograph of the "transfer station". Experimental setup for the transfer and alignment of 2D materials built by Dr. Jacopo Brivio and Prof. Andras Kis. The stage at bottom of the setup can rotate and move in the x, y directions. The sample holder is provided with a heater and a thermocouple for controlling the temperature of the "target" substrate. A vacuum line is available to hold the sample in position. The glass slides that carry the polymer films with the 2D sheets are mounted on *ad hoc* supports, which can move in the x, y, z directions.

common SiO_2/Si substrates, the monolayers can be easily identified by optical microscopy, as described by Benameur *et al.* (ref. [216]). Once a suitable monolayer is found, the chip carrying the flake is spin-coated at 2500 rpm with a 8% solution of PMMA (495k) in anisole (figure B.2b). Subsequently, the substrate is baked at 180 °C for 5 minutes and then immersed in a 30 wt.% solution of KOH in DI water, which is heated at 60 °C (figure B.2c). Intercalation of KOH between the PMMA layer and the substrate promotes the detachment of the polymer film holding the flakes, which typically starts floating after a time variable between 10 and 40 minutes (figure B.2d). The film is then scooped, brought into several baths of DI water for thorough rinsing, and flipped with the flakes facing up. A pierced glass slide is used to fish the polymer film (figure B.2e), paying attention that the desired monolayer lies within the hole. The slide and the film are then dried on a hot plate for 10 minutes at 90 °C. Afterwards, an annealing step at 180 °C for 5 minutes is performed to stretch the PMMA film suspended across the hole. The slide is then mounted on the transfer station (figure B.2f) and the film is approached to the "target" sample, which is kept at a temperature of 90 °C. After performing the alignment, the polymer is brought into contact with the substrate, whose temperature is increased up to 120 °C to promote the adhesion of the PMMA. After 5 minutes of annealing, the glass slide is lifted up and the polymer film with the flakes remains on the sample. The latter is immersed in acetone to strip the PMMA and it is finally annealed for 4 hours inside a furnace (temperature:

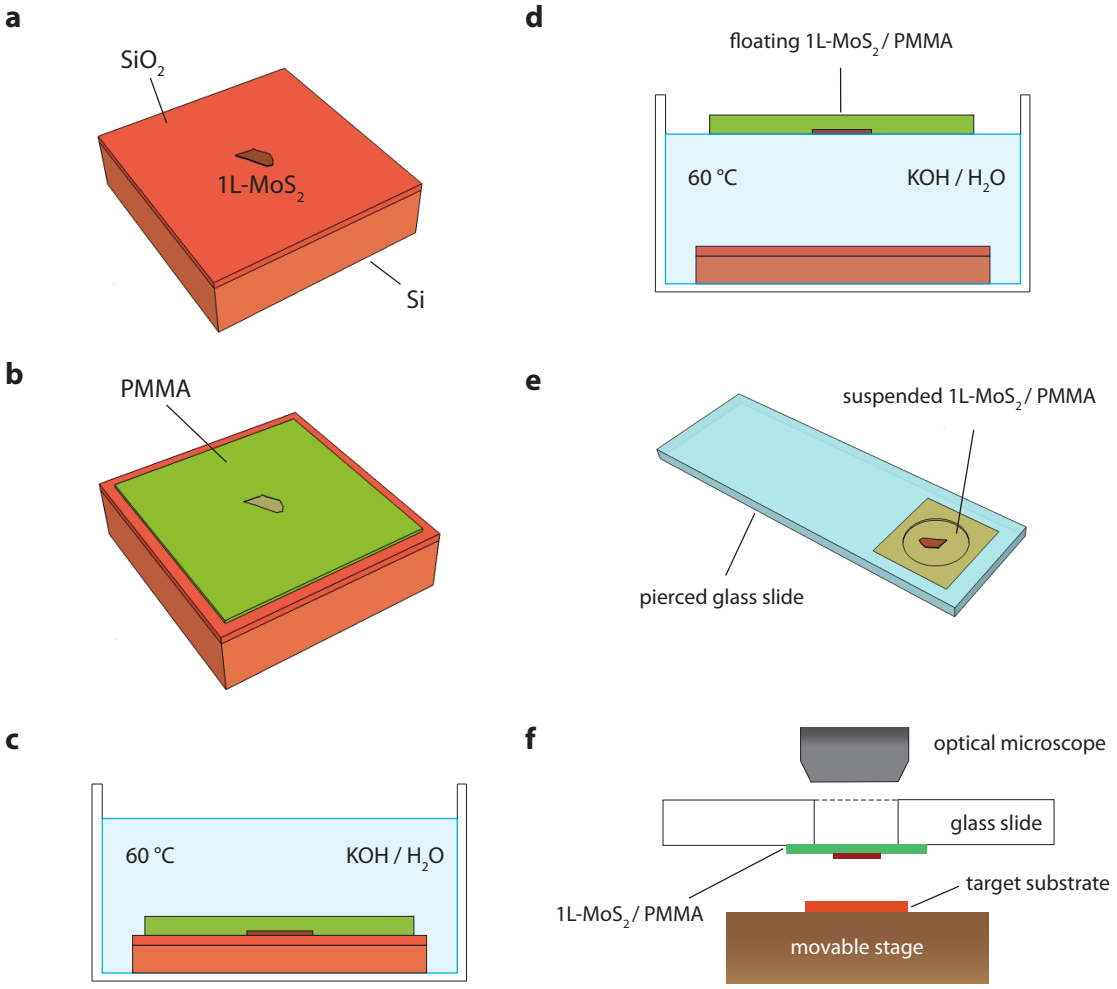

Figure B.2: Process flow for "wet" transfer of 2D materials. **a,** Schematic view of a SiO_2/Si chip employed in this work ($12\,\mathrm{mm} \times 12\,\mathrm{mm}$, $270\,\mathrm{nm}$ thick SiO_2). Monolayer (1L) flakes of MoS_2 or other 2D materials are deposited on the SiO_2 surface with the scotch tape method. **b,** The chip carrying the flakes is spin-coated with a thin layer of PMMA. **c,** Subsequently, the sample is immersed into a 30 wt.% solution of KOH in DI water. **d,** Intercalation of KOH between PMMA and SiO_2 promotes the detachment of the polymer film holding the flakes. **e,** The film can be scooped from the KOH solution to pure DI water and flipped with flakes facing up. A glass slide with a hole ($5\,\mathrm{mm}$ in diameter) is then used to fish the PMMA layer. The part of the polymer film with the flake to be transferred is suspended across the hole. **f,** The glass slide is brought to the transfer station, where the desired flake can be aligned and transferred onto the "target" substrate.

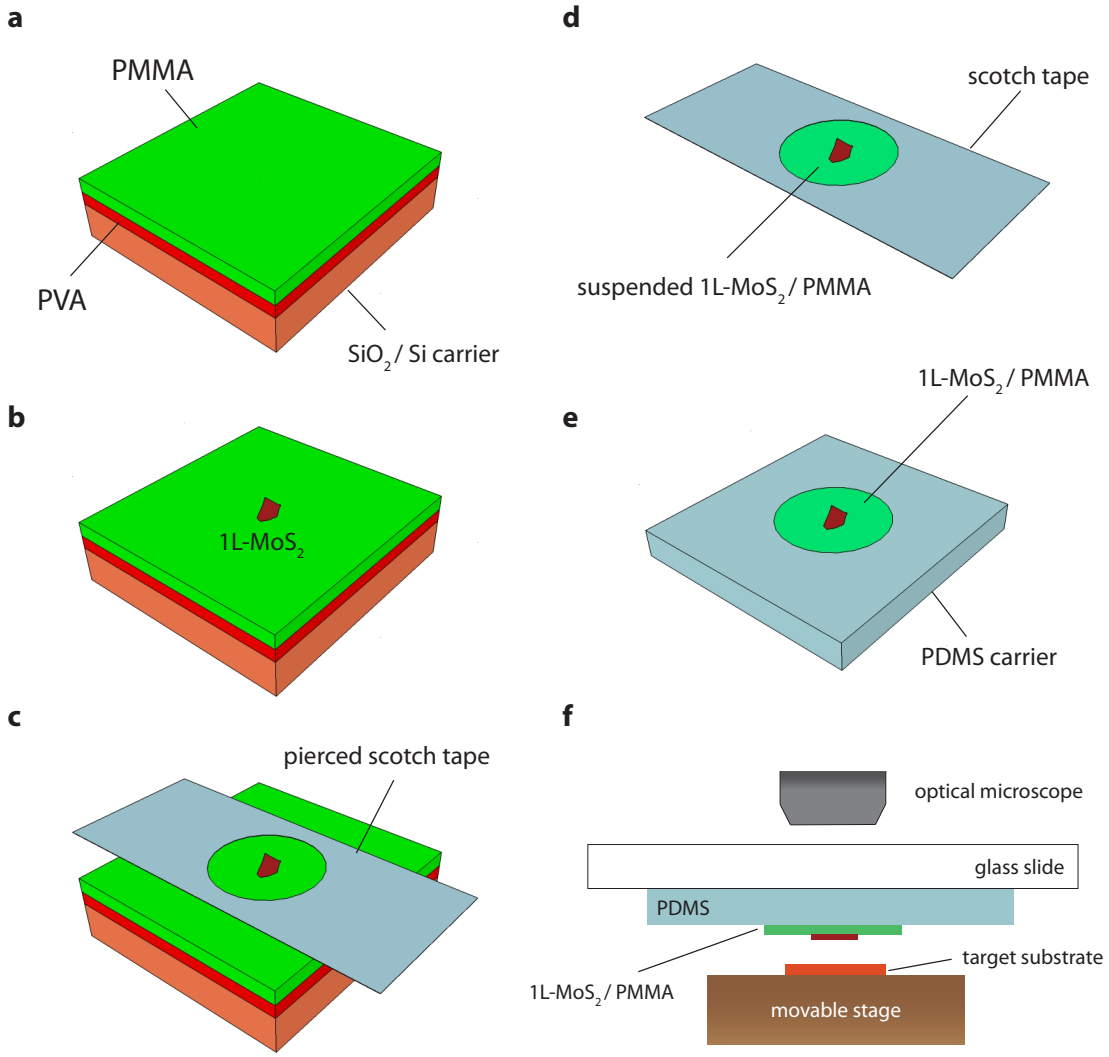

Figure B.3: Process flow for "dry" transfer of 2D materials. **a,** A SiO_2/Si chip is coated with a double polymer layer of PVA and PMMA. **b,** Atomically thin flakes of MoS_2 (1L-MoS_2) or other 2D materials are deposited on the PMMA surface with the scotch tape method. **c,** A new piece of tape with a hole ($5\,\mathrm{mm}$ in diameter) is applied onto the chip, in such a way that the desired flake lies within the hole. **d,** A few droplets of DI water are deposited at the edges of the substrate. As the water starts dissolving the PVA layer, the tape is slowly lifted up resulting in a PMMA film suspended across the hole. **e,** The PMMA layer is then laid on a PDMS stamp ($\sim 2\,\mathrm{mm}$ thick) with flakes facing up and the tape is removed. **f,** The stamp is mounted on a glass slide, which is then brought to the transfer station, where the desired flake can be aligned and transferred onto the "target" substrate.

350 °C, argon flow: 200 sccm) to remove the organic residue. For best removal of polymer contamination it was found to be useful to "brush" the surface of the 2D flakes with the tip of an AFM operated in contact mode, as described in reference [217].

Dry transfer. The procedure for "dry" transfer is schematically illustrated in figure B.3. It is based on the use of a sacrificial layer of polyvinyl alcohol (PVA), which is a water-soluble polymer. The sample is prepared as follows. A 1 wt.% solution of PVA (89k–98k, hydrolyzed 99%) in DI water is spin-coated at 4000 rpm on a SiO_2/Si substrate, resulting in a uniform film with a thickness of ~ 50 nm. The chip is then baked at 90 °C for 10 minutes. Afterwards, a 4% solution of PMMA (950k) in anisole is spin coated at 1500 rpm on the PVA surface (figure B.3a), followed by baking at 90 °C for 10 minutes. These temperatures and times where found to be critical for the detachment of the polymer film in a dry fashion. Ultrathin flakes of MoS_2 or other layered materials are mechanically exfoliated on the PMMA layer (figure B.3b) and detected through a combination of optical microscopy and AFM. Once a suitable 2D sheet is identified, a piece of scotch tape with a hole (figure B.3c) is applied on the substrate, in such a way that the desired flake lies within the hole. Subsequently, a few droplets of DI water are deposited on the edges of the chip. The water slowly penetrates below the PMMA layer and starts dissolving the PVA. At the same time, the scotch tape can be gently lifted up to induce the detachment of the PMMA film. In this way, it is possible to obtain a suspended PMMA membrane, which supports the flake to be transferred, as illustrated in figure B.3d. At this stage, it was found to be convenient to use a polydimethylsiloxane (PDMS) stamp as a carrier for the PMMA film. The latter is deposited on the PDMS surface with flakes facing up, followed by fast removal of the scotch tape (figure B.3e). Afterwards, the PDMS stamp is applied onto the glass slide, which is then mounted on the transfer station (figure B.3f). At this point the procedure continues as described in the case of "wet" transfer. It is worth mentioning that the high transparency of PDMS is suitable for conducting the alignment, which is made easier by the better flatness of the polymer film supported by the rigid silicone stamp. The key factor enabling the "dry" transfer is the preferential adhesion of the PMMA layer to the substrate rather than to the hydrophobic PDMS. This greatly facilitates the release of the polymer film with the flakes from the stamp to the "target" sample.

Example: multilayer heterostructures. Hereafter, an example is provided of how the "wet" and "dry" transfer techniques can be combined together for the fabrication of a multilayer heterostructure consisting of h-BN (bottom), graphene (middle) and monolayer MoS_2 (top). The goal is to obtain a FET where h-BN acts as the gate dielectric, graphene as the electrode material and monolayer MoS_2 as the transistor channel (figure B.4), towards the realization of electronic devices entirely based on 2D materials.
Few-layer (FL) sheets of graphene are deposited on SiO_2/Si substrates and then patterned in the form of stripes (B.4a). Afterwards, the "wet" method is employed to transfer these

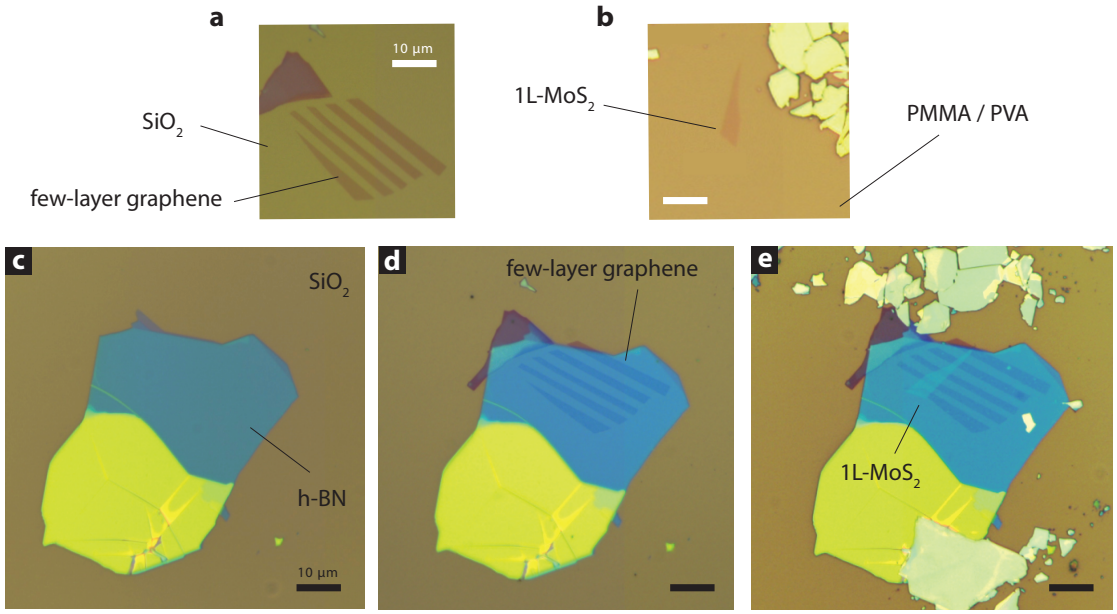

Figure B.4: Heterostructures of h-BN, graphene and monolayer MoS_2. Optical micrographs of the multilayer heterostructure and of its building blocks at different stages of the fabrication process. **a,** FL graphene stripes lying on an oxidized Si chip ($\sim 270\,\mathrm{nm}$ thick SiO_2). The stripes were obtained by etching of graphite thin sheets deposited with the scotch tape method. **b,** Monolayer (1L) MoS_2 flake lying on the PMMA/PVA polymer stack prior to "dry" transfer. **c,** Thin flake of h-BN produced by mechanical exfoliation of bulk crystals. The blue region has a uniform thickness of $\sim 24\,\mathrm{nm}$. **d,** The "wet" transfer method is used to pick up the FL graphene stripes (**a**) from the SiO_2/Si substrate and transfer them onto the h-BN sheet (**c**). **e,** Finally, the 1L-MoS_2 flake shown in **b** is transferred onto the h-BN/FL-graphene heterostructure. The flake in **e** appears mirrored compared to **b** as consequence of the flipping of the PMMA film occurring during the "dry" transfer procedure. The scale bar in all images is $10\,\mu\mathrm{m}$.

stripes from the SiO_2 surface onto an h-BN sheet (figure B.4c and d). The "wet" transfer technique is suitable for this process as the only requirement consists in producing FL graphene electrodes with a conductivity much higher than that of the semiconducting channel. On the other hand, the "dry" technique is employed to transfer a monolayer MoS_2 sheet (figure B.4b) on top of the h-BN/FL-graphene heterostructure. The experimental setup (figure B.1) enables orienting the longitudinal axis of the monolayer MoS_2 flake perpendicular to the FL graphene stripes. The final result of the fabrication process is shown in figure B.4e. The FL graphene electrodes can be further contacted with metal leads to provide electrical connections to the device.

Abbreviations

AFM Atomic Force Microscopy
ALD Atomic Layer Deposition
CVD Chemical Vapor Deposition
CB Conduction Band
DFT Density Functional Theory
DI Deionized
DOS Density of States
EBL Electron Beam Lithography
EOT Equivalent Oxide Thickness
FEA Finite Element Analysis
FET Field Effect Transistor
FETT Field Effect Tunneling Transistor
FG Floating Gate
FL Few Layer
HOPG Highly Oriented Pyrolytic Graphite
HRTEM High Resolution Transmission Electron Microscopy
HV High Vacuum
IC Integrated Circuit
INS Inelastic Neutron Scattering
IPA Isopropanol
ITRS International Technology Roadmap for Semiconductors
KPFM Kelvin Probe Force Microscopy
MBE Molecular Beam Epitaxy
MIT Metal Insulator Transition
MLG Multi-Layer Graphene
MMA Methyl methacrylate
MPS 3-mercaptopropyl trimethoxysilane
NEGF Non Equilibrium Green Function
NEP Noise Equivalent Power
PC Photoconductivity

PDMS Polydimethylsiloxane
PL Photoluminescence
PMMA Polymethyl methacrylate
PTAS Perylene-3,4,9,10-Tetracarboxylic Acid tetrapotassium Salt
PVA Polyvinyl alcohol
QY Quantum Yield
RPS Remote Phonon Scattering
RT Room Temperature
SAM Self Assembled Monolayer
SEM Scanning Electron Microscopy
SRS Surface Roughness Scattering
STM Scanning Tunneling Microscopy
SV Sulfur Vacancy
TC Thermal Conductivity
TEM Transmission Electron Microscopy
TMD Transition Metal Dichalcogenide
VRH Variable Range Hopping
VB Valence Band

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Lausanne, 4 February 2015 S.B.

Curriculum Vitae

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Education

03/2011 - 04/2015	PhD in Physics (Docteur ès sciences) **École Polytechnique Fédérale de Lausanne**, Switzerland Laboratory of Nanoscale Electronics and Structures Advisor: Prof. Andras Kis Subjects: nanoelectronics, 2D materials, microfabrication
08/2008 - 12/2010	Master of Applied Science (Maîtrise ès sciences appliquées) **École Polytechnique de Montréal**, Québec, Canada Laboratory of Advanced Electroactive Materials Advisor: Prof. Clara Santato. Coadvisor: Prof. Federico Rosei Subjects: organic electronics, semiconductor device physics
09/2007 - 12/2010	Master of Science in Engineering Physics (Laurea Specialistica) **Politecnico di Milano**, Italy Grading: 110/110 with honors
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09/2004 - 09/2007	Bachelor of Science in Engineering Physics (Laurea Triennale) **Politecnico di Milano**, Italy Grading: 110/110 with honors
09/1999 - 07/2004	High School Diploma (Maturità Scientifica) **Istituto all Stimate**, Verona, Italy Grading: 100/100

Research interests

Nanoscience and nanotechnology – Two-dimensional materials – Organic electronics

Technical skills

Microfabrication: photolithography, e-beam lithography, thermal evaporation, atomic layer deposition, physical and chemical etching, solution processing, design of (opto-) electronic devices, transfer and alignment of mesoscopic objects.

Characterization techniques: atomic force microscopy, cryogenics, electrical and magnetic measurements, spectroscopic ellipsometry, scanning electron microscopy.

Computer skills: Microsoft Windows and Office, Origin, Igor, DesignCAD, Adobe Illustrator. Basic knowledge of C/C++, LaTeX, MATLAB and LabVIEW.

Publications

- Dominik Lembke, **Simone Bertolazzi**, and Andras Kis. Single-layer MoS_2 electronics. *Accounts of Chemical Research*, 2015.
- Dumitru Dumcenco, Dmitry Ovchinnikov, Kolyo Marinov, Predrag Lazic, Marco Gibertini, Nicola Marzari, Oriol Lopez Sanchez, Yen-Cheng Kung, Daria Krasnozhon, Ming-Wei Chen, **Simone Bertolazzi**, Philippe Gillet, Anna Fontcuberta i Morral, Aleksandra Radenovic, and Andras Kis. Large-area epitaxial monolayer MoS_2. *ACS Nano*, 2015.
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- Rusen Yan, Jeffrey R Simpson, **Simone Bertolazzi**, Jacopo Brivio, Michael Watson, Xufei Wu, Andras Kis, Tengfei Luo, Angela R. Hight Walker, and Huili Grace Xing. Thermal conductivity of monolayer molybdenum disulfide obtained from temperature-dependent raman spectroscopy. *ACS Nano*, 8(1):986–993, 2014.
- **Simone Bertolazzi**, Daria Krasnozhon, and Andras Kis. Nonvolatile memory cells based on MoS_2/graphene heterostructures. *ACS Nano*, 7(4):3246–3252, 2013.
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- Hongyan Shi, Rusen Yan, **Simone Bertolazzi**, Jacopo Brivio, Bo Gao, Andras Kis, Debdeep Jena, Huili Grace Xing, and Libai Huang. Exciton dynamics in suspended monolayer and few-layer MoS_2 2D crystals. *ACS Nano*, 7(2):1072–1080, 2013.
- Julia Wünsche, Giuseppe Tarabella, **Simone Bertolazzi**, Maimouna Bocoum, Nicola Coppedè, Luisa Barba, Gianmichele Arrighetti, Luca Lutterotti, Salvatore Iannotta, and Fabio Cicoira. The correlation between gate dielectric, film growth, and charge transport in organic thin film transistors: the case of vacuum-sublimed tetracene thin films. *Journal of Materials Chemistry C*, 1(5):967–976, 2013.
- Rusen Yan, **Simone Bertolazzi**, Jacopo Brivio, Tian Fang, Aniruddha Konar, A Glen Birdwell, Nhan V. Nguyen, Andras Kis, Debdeep Jena, and Huili Grace Xing. Raman and photoluminescence study of dielectric and thermal effects on atomically thin MoS_2. *arXiv:1211.4136*, 2012.
- **Simone Bertolazzi**, Jacopo Brivio, and Andras Kis. Stretching and breaking of ultrathin MoS_2. *ACS Nano*, 5(12):9703–9709, 2011.
- **Simone Bertolazzi**, Julia Wünsche, Fabio Cicoira, and Clara Santato. Tetracene thin film transistors with polymer gate dielectrics. *Applied Physics Letters*, 99:013301, 2011.
- Clara Santato, Laura Favaretto, Manuela Melucci, Alberto Zanelli, Massimo Gazzano, Magda Monari, Dilek Isik, David Banville, **Simone Bertolazzi**, and Sébastien Loranger. Influence of the oxidation level on the electronic, morphological and charge transport properties of novel dithienothiophene S-oxide and S, S-dioxide inner core oligomers. *Journal of Materials Chemistry*, 20(4):669–676, 2010.
- **Simone Bertolazzi**. Organic gate dielectrics for tetracene field effect transistors. Master's thesis, École Polytechnique de Montréal, 2010.

Participation in conferences and meetings

06/2014 – Cork, Ireland	Workshop on Dielectrics in Microelectronics at Tyndall. *Winner of best presentation award.*
03/2014 – Denver, USA	APS March Meeting, American Physical Society.
06/2013 – Basel, Switzerland	Poster presentation at Swiss Nanoconvention.
06/2012 – Mainz, Germany	Transition Metal Chalcogenide and Halide Nanostructures.
05/2010 – Atlanta, USA	F-Pi-9, Symposium of Functional Pi-Electron Systems.
11/2009 – Boston, USA	MRS Fall Meeting, Materials Research Society. *Nominated for best poster award.*

Teaching

Teaching assistant for the courses:

2012–2015	"Measuring systems"
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Languages

English: Fluent French: Fluent Italian: Mother tongue

Interests and Activities

Literature and arts. Music: bass guitar. Sports: running, swimming, canoeing, skiing.