Modeling nanoscale quasi-ballistic MOS transistors: a circuit design perspective

THÈSE N^{O} 6385 (2014)

PRÉSENTÉE LE 12 NOVEMBRE 2014

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DE CIRCUITS INTÉGRÉS
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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ÉCOLE POLYTECHNIQUE
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Suisse
2014

Abstract

The scaling of device technologies poses new challenges, not only in circuit design, but also in device modeling, especially because of the short-channel effects and the emergence of novel phenomena like ballistic transport. Nonetheless, it enables the design of ultra low-power analog and Radio Frequency (RF) circuits by allowing to push the operating points into moderate and eventually weak inversion regions, which are increasingly becoming the preferred regions of operation for such applications. Even though modern compact models have evolved to adequately model the short-channel effects in all regions of operation, there is a lack of simpler models that (a) reliably predict the physics of downscaled devices while (b) remaining continuous through moderate inversion and (c) aid the designer's intuition through simple design methodologies.

In this work, we extend the EKV charge based model to include the velocity saturation effect for weak inversion operation. Using the simple analytical model hence developed, we propose a design methodology for low-power analog circuit design.

Then, we focus our attention on ballistic transport in MOSFETs, that is expected to dominate in the deeply scaled devices. Again, despite the extensive body of work available in the literature, most models remain deeply rooted in physics, consisting of fairly complicated equations, that are of little use for an intuitive understanding and design. In addition, the quasi-ballistic devices, which lie on the continuum between the ballistic and the diffusive devices, pose their own modeling challenges: a model for the quasi-ballistic devices would have to remain continuous between the ballistic and diffusive regimes. Most of the published works, based on the carrier flux transport over the source-channel potential barrier approach, seem to ignore the electrostatics in the rest of the channel. The shape of the electrostatic potential in the channel is approximated through polynomial functions, which is adequate for the very short-channel devices but not scalable to long channel quasi-ballistic devices.

In this work, we study the role of the gate and the electrostatics in a ballistic channel by drawing on the insights gained from Monte-Carlo simulations on quasi-ballistic and ballistic double-gate MOSFETs. We propose a simple semi-empirical model of the channel charge, using which we develop an analytical model for the channel potential, both of which could be used as precursors to a scalable compact model that would encompass the ballistic, quasi-ballistic and drift-diffusion regimes.

Keywords: Nanoscale devices, Semiconductor device modeling, Compact model, Ballistic transport, Quasi-ballistic MOSFETs, Short-channel effects, Design methodology

Résumé

La réduction de la taille des transistors dans les technologies avancées pose de nouveaux défis pour la conception des circuits intégrés, mais également pour la modélisation, ceci tout particulièrement à cause des effets dits 'canaux courts' ainsi que par l'apparition de nouveaux phénomènes comme le transport balistique. Malgré tout, cette miniaturisation permet de concevoir des circuits analogiques et Radio Fréquence (RF) à très faible consommation si l'on prend soin de décaler le point de polarisation vers l'inversion modérée, voire la faible inversion, qui sont les domaines optimaux pour ces genres d'applications. Bien que les modèles compacts aient évolué pour tenir compte de ces effets canaux courts dans tout les régimes de polarisation, il manque encore un modèle simple, d'une part pour (a) prédire de manière fiable le comportement des transistors de très petite taille tout en (b) conservant une analyse continue en passant par l'inversion modérée, et d'autre part pour (c) guider les designers en leur fournissant une méthodologie plus simple et plus intuitive.

Dans ce travail, nous étendons le modèle EKV basé sur les charges afin d'y inclure le saturation de la vitesse des porteurs, *«velocity saturation»*, en inversion faible. A l'aide de ce modèle analytique, nous élaborons une méthodologie de conception de circuits analogiques pour la basse consommation.

Par la suite, nous nous sommes concentrés sur le transport balistique de charges au sein du MOSFET, qui est susecptible d'être le mécanisme dominant dans les transistors nanométriques. Bien que de nombreux modèles soient décrits dans la littérature, la plupart sont basés exclusivement sur la physique et consistent en un ensemble d'équations peu utiles et peu intuitives pour la conception de circuits, car très complexes. De plus, les transistors quasi-balistiques posent de nouveaux défis : un modèle pour les transistors quasi-balistiques se doit d'être continu entre le régime balistique et le régime de diffusion. La plupart des travaux publiés, basés sur un concept de flux de porteurs traversant une barrière de potentiel entre la source et le canal, semblent ignorer les effets électrostatiques le long du canal. En fait, il s'avère que l'approximation par des fonctions polynomiales du potentiel dans un canal très court n'est pas appropriée pour les transistors quasi-balistiques à canal long.

Dans ce travail, nous étudions le rôle de la grille au travers de l'électrostatique qu'elle impose au sein d'un canal balistique, ceci en s'appuyant sur des simulations Monte-Carlo de transistors à double grille, à la fois ballistiques et quasi-balistiques. Nous proposons un modèle semi-empirique de la charge dans le canal, ainsi qu'un modèle analytique du potentiel qui lui est associé, qui pourront servir de point de départ à un modèle compact englobant les différents régimes, à savoir balistique, quasi-balistique et de conduction-diffusion.

A note on the page layout of this thesis

The rather unconventional page layout of this document is inspired by the layouts of the books *The Feynman Lectures on Physics*[1] and *Visual Explanations*,[2] both of which use a block of main text that is narrower than the page width, and make extensive use of the margins to present information. In this thesis I have chosen to do this, not simply to imitate great works in scientific literature, or just to be unconventional, but to optimize the experience for the reader of this thesis. You might be reading this thesis on an iPad™ or Kindle™, on a computer screen, or on paper. Through this particular layout I have tried to ensure that you can read this document without tiring your eyes and hands too much, irrespective of your reading media.

1. R. P. Feynman, R. B. Leighton and M.L. Sands, *The Feynman Lectures on Physics.* Addison Wesley, 1963.

2. E.R.Tufte, *Visual explanations: images and quantities, evidence and narrative.* Graphics Press, 1997.

It is well known in the field of typography that for the ease of reading, the ideal length of a single column text is 60 to 70 characters. This prevents the eye from making too many back-and-forth jumps, which is the case if the lines are shorter. On the other hand, longer lines cause the eyes to lose their anchor point in the text, and they have to jump too far back to the beginning of the next line. When using a given font, the appropriate line length can be calculated mathematically.[3] This document uses *Utopia* and *Source Sans* fonts and the line length (size of the main text block) is 26 picas. It is typeset in LaTeX 2_ε, borrowing the elements of the *UiO Thesis class*,[4] which itself is based on the *Memoir class*.

3. P. Wilson, The Memoir Class. http://www.ctan.org/pkg/memoir

4. https://github.com/jrk/uggedal-thesis/blob/master/src/uiothesis.cls

One of the major problems that I experience myself while reading on electronic devices, is that of excessive scrolling. To refer to an equation or diagram that was in the previous chapter, the reader has to scroll all the way to its location, and at the same time, remember the current location to continue reading from there. In this document, I have deliberately tried to keep all the figures within one page distance of the place where they are referred to— so that you don't have to scroll or flip more than one page to see it. Any equation that is more than a page away from the point where it is referred, is repeated as a margin-note at that point. The bibliographic entries (at the end of the document) have a list of pages where they are cited on, so that you can click on it to return to the original location.[5]

5. If supported, **please turn on *link highlighting*** in your pdf reader, to clearly see all the hyperlinks: all the citation and references are hyperlinked.

Acknowledgements

MY LIFE, and consequently my work, has been touched in numerous ways by so many people that it would take more than a couple of pages to do the slightest of justice in thanking them all. At the risk of being ungrateful to *many*, I highlight *the few* who deserve more than just words of thanks.

I must thank Prof. Christian Enz and Dr Jean-Michel Sallese, my thesis advisors, in the same breath. I have had the honor and pleasure of learning from these two great teachers since my days as a MS student at EPFL. Obviously, they taught me about MOSFETs and how to model them, and about microelectronic circuits and how to analyze them; but they taught me more. While Prof. Enz taught me to be methodical in my research work, Dr Sallese taught me to be rigorous about it. I am grateful for their humility while they taught, their patience when I took my time to learn, and the constant motivation and encouragement. Thanks to Prof. Enz for initiating me to Latex, Mathcad, Mathematica; to Jean-Michel for being my constant *Obi-Wan Kenobi* like friend-philosopher-guide.

Most of the work in this thesis is built around Monte-Carlo simulation data that Prof. Francisco Gamiz and Prof. Carlos Sampedro of University of Granada provided to me without any reservations. They deserve a big thanks not only for the data, but also for being so kind to critically review and help improve the papers I wrote. Prof. Sampedro deserves a special mention for his prompt, yet painstakingly detailed, replies to all my questions. I take this opportunity to thank them, and José-Luis, also for their hospitality during my two-week stay in Granada.

Thanks are due also to Profs. Ionescu, Iniguez, Gamiz and Dr. Boero for very kindly accepting to be the members of my thesis jury.

On countless occasions in the last four years, I have asked Marie Halm, Isabelle Buzzi, Karin Jaymes, Chrisitina Govoni, Nicky Taveira and Catherine Falik for their help in dealing with administrative matters; all

of them have obliged with big smiles on their faces. I thank you all for your smiles and for making my life as easy as sending an email.

I have been very lucky to have another mentor in Dr. Wladek Grabinski. He is ever-ready to go out of his way to connect you to the right people, to find the right resources, and advise you. I really admire his broad range of interests and passion for technology, some of which he might have rubbed on to me during our discussions over coffee. It was a real pleasure to have worked with him in establishing the IEEE student branch of EPFL.

No words of gratitude are enough to thank the *Aumôniers* Maria Zufferey and Chrisitan Vez who have the magical powers to turn a sad, unhappy face into a beaming happy one, in an instant. Thank you for being my *guardian angels*.

I have had great colleagues and friends-at-work in Aravind, Viswa, Antonios, Maria-Anna, Lucian, Farzan, Omid, Raghav, Jeremy, Vincent, Vladimir and the two visitors from Bordeaux: Francois and Gabrielle. Despite the pressures of work, the time spent in the office and outside of it has been delight because of these lovely people. Thanks to Moritz for the time spent hiking in the Swiss mountains, to Elsa for helping me develop my social skills, to Anna for the random philosophical discussions and to Rammohan for the discussions about India and Switzerland, to Hauke, Christelle and Carole for being the ideal flatmates. But for the lovely companionship of Elisa, I might have never found my work-life balance; I thank her for all the fantastic moments.

A special thanks to Prof. Neeta Pandey (who introduced the world of semiconductors to me) and to Prof. Anuradha Basu, both of whom kept me motivated through their regular emails.

I had been reserving this last paragraph to thank my sister and parents, who have been very understanding and patient with all my whims and fancies all these years, so that I can follow my dreams. I dedicate this thesis to my parents, from whom I learnt my first alphabet and a lot more.

Anurag Mangla
July 17, 2014

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Introduction 1

1.1 Device modeling for circuit design

ANALOG circuit design is a complex exercise involving multiple trade-offs, e.g. between power consumption and speed, and several degrees of freedom like the drain current and transistor dimensions [1]. The importance of accurate device models, which stems from the fact that analog design has special modeling needs, has long been recognized [2]. It is all the more emphasized with the aggressive scaling of the CMOS technology which, although driven by the needs of digital circuits, is important also from the perspective of low-power analog and RF circuit design.

Technology scaling offers a part of the solution to the increasingly stringent requirements on the energy consumption of electronic devices, demanded by the emergence of applications like the Internet of Things (IOT), wireless body area networks (WBAN) etc., by allowing to pushing the operating points of the devices towards moderate and weak inversion while maintaining performance [3, 4]. Nonetheless, shifting the operating point towards weak inversion might not be straightforward in nanoscale technologies – design with advanced deep-submicron technology nodes is complicated because of the short-channel effects [5] – and might be further complicated due to the emergence of novel phenomena like ballistic transport.

Evidently, the scaling of device technologies poses new challenges, not only in circuit design, but also in device modeling. Models that would support the design of low-power analog and RF circuits would need to accurately and reliably predict the complex physics of downscaled devices, being efficient at the same time, to be used for circuit simulations [6].

1.2 Need for simple models

Device models can be broadly classified into the following distinct categories:

- *Physical* As the name implies, these models are based on the physics of the device. Such models would often consist of coupled nonlinear partial differential equations [2] to accurately describe the physical phenomena in the device. Even though the physical models are imperative for device design, computationally they are too demanding to be used for circuit analysis and design.

- *Empirical* This is the other end of the spectrum where the models consist of curve fitting with no physical significance attached to the equations and the parameters.

In the ideal world, a device model would be physical while remaining computationally efficient – consisting of only simple equations with a few parameters. In the real world however, the requirement that a model be accurate as well as fast, and that it is able to describe all the physical phenomena of advanced devices, makes the advanced compact models quite complex.[1]

1. About 90 % of the code in the bulk BSIM models is devoted to the modeling of “real device effects” like velocity saturation, mobility degradation, DIBL, tunneling current, parasitic effects etc., while only about 10 % models the “core device”. [7]

Notwithstanding that modern circuit simulators coupled with sophisticated compact models are powerful tools for design and analysis of circuits with advanced technology nodes, most experienced analog designers still rely on their design intuition and do “hand calculations” before performing any simulation. Evidently, for such purposes the designer would need a “stripped-down” version of the full compact model, one that is simple enough for initial design guidance, yet accurate enough to minimize trial-and-error simulations.[2] Such a model would provide a good understanding of the device with clarity (which can be enhanced using graphical representations) taking precedence over accuracy [8]. From this perspective, another category of device models can be added to the above list:

2. “[The model] should ‘speak to the mind’, using no complicated or chained equations.”[8]

- *Semi-empirical* Such models are physics based, with suitable assumptions and approximations to keep the model equations reasonably simple.

1.3 The goal of this work

Most of the work on modeling dealing with incorporating ballistic transport in nanoscale channel length devices has done so without considerations about ensuring continuity with transport in non-minimum (long) channel lengths. From a designer's perspective, there is thus a need for a scalable compact model which would capture the ballistic, the quasi-ballistic and the drift-diffusion regimes in a unified formalism ensuring continuous transitions between them. Moreover, in the literature, most of the analytical treatment of the new transport phenomena comprises of sets of complicated equations. Even though this ensures physical accuracy of the models, the non-intuitive nature of these models do not make them attractive to the circuit designer.

As the goal of this work, we attempt to model the ballistic and quasi-ballistic double-gate MOSFETs in a semi-empirical manner that is more approachable to a designer.

1.4 Structure of the thesis

- *Chapter 2* presents the inversion coefficient based design methodology and its application for low-power analog and RF design. Impact of velocity saturation on transconductance efficiency is analyzed and the EKV model is extended to include the velocity saturation effect in a continuous manner between weak inversion and strong inversion. A figure-of-merit for RF design that allows optimization of the tradeoff between gain, transit frequency and noise is presented.

- *Chapter 3* introduces the concept of ballistic transport that starts to appear in MOSFETs when their dimensions are scaled to nanometer lengths. The concept of local equilibrium is discussed at length, since it no longer holds in the presence of ballistic transport and necessitates the development of new models for the ballistic regime. An overview and critique of the state of the research in modeling nanoscale ballistic MOSFETs is also presented.

- *Chapter 4* presents a first attempt in developing a compact model that includes ballistic transport and is continuously scalable between the nanometer scale ballistic and the long channel diffusive regimes. The I-V characteristics of this model as well as its limitation in terms of electrostatics are also presented.

- *Chapter 5* In this chapter, we study the electrostatics in a ballistic channel, especially the role of the gate through Monte-Carlo simulations on devices with a partial gate geometry.

- *Chapter 6* In this chapter, we develop an analytical model of the profile of the channel charge and potential in quasi-ballistic double-gate MOSFETs, that is continuous between the ballistic and long channel devices.

- *Chapter 7* summarizes the results and accomplishments of this thesis along with a retrospective discussion about the work. Finally, the scope for continuation and extension of this work is presented.

Design methodology for ultra low-power analog circuits 2

In this chapter, we present the inversion coefficient based design methodology that is especially suitable for circuit level optimization in low-power analog and RF design, and demonstrate its application through a couple of examples. We then analyze the impact of short-channel effects, concentrating especially on velocity saturation, and extend the EKV model equations to include the velocity saturation effect in a continuous manner between weak inversion and strong inversion. Finally, we analyze a figure-of-merit for RF design and demonstrate that it is possible to find an operating point to optimize the tradeoff between power consumption, transit frequency and noise.

2.1 The need for design methodologies

As mentioned in Chapter 1, analog CMOS design is a difficult, time consuming process: increasingly complex functions need to be implemented under increasingly constrained power and area budgets while circumventing the challenges posed by newer device technologies. In addition to choosing the appropriate circuit architecture, a designer would need to make optimum choices in the degrees of freedom available to him, typically, the drain current (or the bias voltages) and dimensions (length and width) of the individual devices, to do well in the performance metrics like gain, current efficiency, bandwidth and noise. Evidently, some design guidance would be invaluable for the designer to navigate this multi-dimensional design space, and indeed, there is considerable interest in design methodologies for analog design [9].

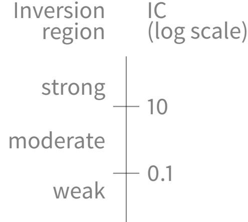
2.2 Inversion coefficient based design methodology

The inversion coefficient *IC* is the measure of the level of channel inversion and is equal to the normalized drain current in forward saturation

[8]:

$$IC \triangleq \frac{I_\mathrm{D}|_\mathrm{saturation}}{I_\mathrm{spec}} \tag{2.1}$$

using which the different regions of operation of a MOSFET in saturation can be classified as



$$\begin{aligned} IC &\leq 0.1 \quad \text{weak inversion} \\ 0.1 < IC &\leq 10 \quad \text{moderate inversion} \\ 10 < IC & \quad \text{strong inversion.} \end{aligned}$$

In (2.1), the normalizing factor I_spec is called the *specific current*, and is defined as

$$I_\mathrm{spec} = I_{\mathrm{spec}\square} \frac{W}{L} \qquad \text{with} \tag{2.2a}$$

$$I_{\mathrm{spec}\square} \triangleq 2n\mu_0 C_\mathrm{ox} U_\mathrm{T}^2, \tag{2.2b}$$

where μ_0 is the constant low-field mobility. $I_{\mathrm{spec}\square}$ is generally called the *technology current* since it is dependent only on a given technology and the operating temperature, but is independent of the device dimensions. Hence, the inversion coefficient *IC* is stripped off of any size and technology dependence.

As opposed to the conventional degrees of freedom, viz., drain current, channel width and channel length, the inversion coefficient provides a direct numerical measure of the region and level of inversion of a MOSFET, therefore permitting to design freely in any of the three inversion regions [1]. The inversion coefficient based design methodology is especially suitable for design in moderate inversion, the preferred operating region for low-power analog and RF circuits, and has been used extensively for such purposes [10, 11, 12, 13]. In the following sections we present a couple of simple design problems to illustrate the design methodology.

2.3 Simple example of *IC* based design methodology

Figure 2.1 shows a capacitively loaded common-source stage. To optimize this circuit, we need to minimize its current consumption for a desired gain A_v at a given frequency of operation ω, which is assumed to be higher than the cut-off frequency ω_c, i.e., $\omega > \omega_\mathrm{c}$ [14].

The small-signal voltage gain of the circuit (loaded by an external load

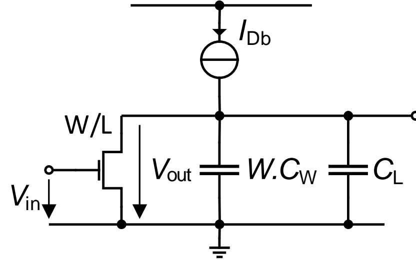


Figure 2.1: A capacitively loaded common-source gain stage

capacitance C_L) can then be approximated as

$$A_v \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{G_m}{\omega C_{tot}} \tag{2.3}$$

where

$$C_{tot} = C_w W + C_L. \tag{2.4}$$

Here C_w is the self-loading load capacitance per unit width of the gain transistor and W its width. From (2.3),

$$C_{tot} = \frac{G_m}{\omega A_v} = \frac{g_{ms} G_{spec}}{n\omega A_v} = \frac{g_{ms} I_{spec\square}(W/L)}{nU_T \omega A_v}. \tag{2.5}$$

Let us define a constant

$$\omega_0 = \frac{I_{spec\square}}{nU_T C_w L_0}, \tag{2.6}$$

with L_0 being the minimum channel length provided by the chosen technology, that is then a parameter dependent entirely on the technology and temperature, and independent of the operating point and frequency. Solving (2.4) and (2.5) for W and substituting using (2.6), we get

$$W = \frac{C_L}{C_w}\left(\frac{A_v(\omega/\omega_0)(L/L_0)}{g_{ms} - A_v(\omega/\omega_0)(L/L_0)}\right) \tag{2.7}$$

Now, we define

$$W_0 = \frac{C_L}{C_w}, \tag{2.8a}$$

$$\Omega_v = \frac{\omega}{\omega_0} A_v \quad \text{and} \tag{2.8b}$$

$$\ell = \frac{L}{L_0}, \tag{2.8c}$$

to rewrite (2.7) in a normalized form:

$$w = \frac{W}{W_0} = \frac{\Omega_v \ell}{g_{ms} - \Omega_v \ell}. \tag{2.9}$$

Using (2.1), (2.2a) and (2.9), we can obtain the bias current as

$$\begin{aligned} I_{Db} &= I_{spec\square} \frac{W}{L} IC \\ &= I_{spec\square} \frac{W_0}{L_0} \frac{\Omega_v}{g_{ms} - \Omega_v \ell} IC, \end{aligned} \tag{2.10}$$

which we normalize by defining

$$IC_0 = IC_{spec\square} \frac{W_0}{L_0}, \tag{2.11}$$

to obtain

$$i_{db} = \frac{I_{Db}}{IC_0} = \frac{\Omega_v}{g_{ms} - \Omega_v \ell} IC. \tag{2.12}$$

Here, $g_{ms} = G_{ms}/G_{spec}$ is the normalized source transconductance, which is a function of the inversion coefficient [8]:

$$g_{ms} = \frac{2IC}{\sqrt{4IC + 1} + 1}. \tag{2.13}$$

Eq. (2.12) allows us to pursue our initial design goal – minimizing the bias current for a desired gain at a given operating frequency – independent of the technology. In Fig. 2.2, i_{db} is plotted as a function of IC for three different values of Ω_v. We see that for any value of Ω_v, i_{db} has a minimum. Evidently, the bias current I_{D_b} of the common-source stage can be minimized for a given gain and operating frequency; the target gain and frequency set the value of Ω_v through (2.8a), and the channel length, which is an independent degree of freedom, determines ℓ. An optimum inversion coefficient IC_{opt}, for achieving the minimum bias current, can then be obtained by minimizing (2.12) with respect to IC. The optimum IC is given by

$$IC_{opt} = 2\Omega_v \ell (1 + \Omega_v \ell) + \sqrt{1 + 5\Omega_v \ell (1 + \Omega_v \ell)}, \tag{2.14}$$

which is plotted in Fig. 2.2.[1] Having obtained IC_{opt}, we can calculate the remaining parameter, width W_{opt} of the channel, by plugging-in IC_{opt} in (2.13) and using in (2.9). Finally, the required optimum bias current

1. Interestingly, this optimum lies in the moderate or the weak inversion region.

can be calculated as

$$I_{D_{bopt}} = I_{spec\square} \frac{W_{opt}}{L} IC_{opt}. \tag{2.15}$$

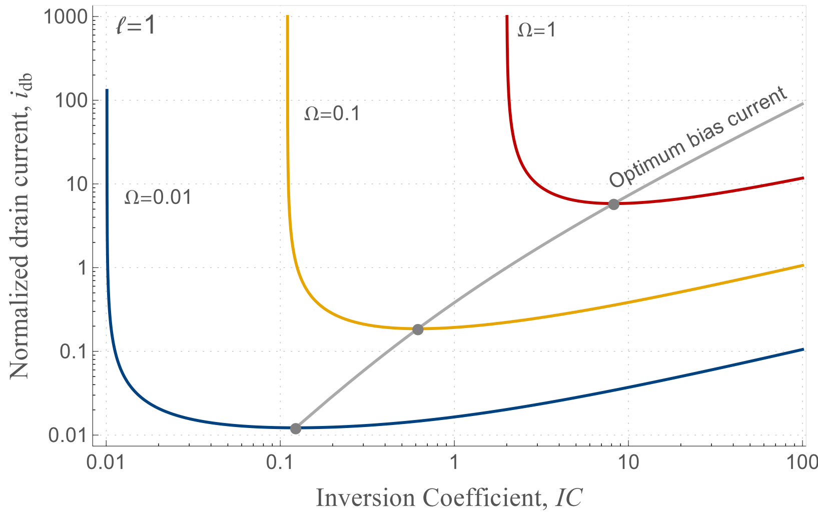


Figure 2.2: Normalized bias current for the capacitively loaded common-source stage vs. inversion coefficient

2.4 A figure-of-merit for low-power RF design

A more practical requirement for low-power RF design would be to not only minimize the consumption to obtain a given gain, but also to minimize the noise. Maximizing the gain, minimizing the noise and minimizing the consumption involves a mutual tradeoff. Rather than dealing with the gain, noise and current individually, we can quantify this tradeoff by introducing a figure-of-merit (FoM) and then optimize this FoM.

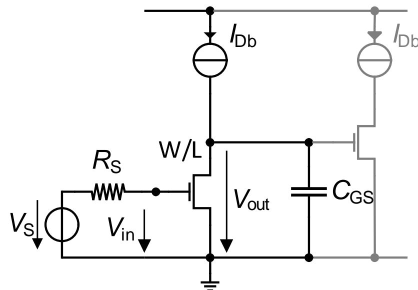


Figure 2.3: A common-source gain stage loaded with an identical load stage

Consider a common-source stage loaded with an identical transistor such that it presents a load C_{GS} to the first stage, as shown in Fig. 2.3. The small signal voltage gain is given by

$$A_v = \frac{G_m}{\omega C_{GS}} = \frac{\omega_t}{\omega}, \tag{2.16}$$

where

$$\omega_t \cong \frac{G_m}{C_{GS}} \tag{2.17}$$

is approximately equal to the transit frequency. The noise factor is given by

$$F \cong 1 + \frac{\gamma_{nD}}{G_m R_S}, \tag{2.18}$$

with γ_{nD} being the noise excess factor of the gain transistor, and R_S being the source resistance [8]. In order to maximize the gain A_v and minimize the noise factor F, at a given bias current I_D, we can define a figure-of-merit as

$$FoM_{GainNoise} \triangleq \frac{A_v}{(F-1)I_D} = \frac{R_S}{\omega \gamma_{nD}} \frac{G_m \omega_t}{I_D}. \tag{2.19}$$

$FoM_{GainNoise}$ is proportional to an important FoM for low-power RF design –

$$FoM_{RF} \triangleq \frac{G_m \omega_t}{I_D} \tag{2.20}$$

– that can be written in the normalized form as following

$$fom_{rf} \triangleq \frac{g_{ms} \bar{\omega}_t}{i_d}, \tag{2.21}$$

with $\bar{\omega}_t$ being the normalized angular transit frequency, normalized to

$$\begin{aligned} \omega_{spec} &= \frac{G_{spec}}{n C_{ox} W L} \\ &= \frac{I_{spec\square}}{n U_T C_{ox} L^2} \\ &= \frac{2 \mu_0 U_T}{L^2}. \end{aligned}$$

In (2.20), both G_m / I_D [9, 15] and ω_t [3, 9] are important metrics in their own standing. Since G_m / I_D is maximum in weak inversion, it is advan-

tageous to bias the device towards this region from the point of view of dc gain and power consumption. However, the linearity and noise of the device degrade in this region. The transit frequency ω_t is defined as the frequency at which the extrapolated small-signal current gain of the transistor in common-source configuration falls to unity. Devices are biased in strong inversion to obtain significant gain at RF, better noise and linearity, albeit at the cost of a higher current consumption. FoM_{RF} combines these tradeoffs into a single metric. This figure-of-merit was introduced in [16] and discussed further in [17]. Since it combines the two quantities which have their maxima in opposite directions of the IC axis, it is particularly suited for low-power RF design, serving as a tool to locate the optimum operating point (IC) of the device. This optimum can be rapidly located by plotting the normalized fom_{rf} as a function of IC using (2.13) and (2.17). It should be noted that the gate capacitance C_{GS} in (2.17) is a bias dependent parameter [8], but can be approximated by a constant value, accounting not only for overlap and other extrinsic capacitances (such as fringing capacitances, which are becoming increasingly important in deep-submicron devices), but also for bias dependent intrinsic capacitances. Although this simplification obviously comes at the expense of accuracy (especially in strong inversion), it is acceptable for simple hand calculations.

To be able to use the equations developed in this and the previous sections reliably with the advanced technology nodes, we would need to account for the short-channel effects that become prominent at sub-micron channel lengths. To maintain sufficient accuracy, these effects should be accounted for even in the simplistic model for hand calculations. We will return to the discussion of fom_{rf} in Section 2.6 with the short-channel effects included, which we discuss next.

2.5 Short channel effects

Two of the especially important short-channel effects are drain induced barrier lowering (DIBL) and velocity saturation (VS). In addition, there is mobility reduction due to the vertical field (VFMR). Both velocity saturation and mobility reduction due to vertical field are related to the mobility of the carriers and affect not only the magnitude but also the slopes of I_D vs. V_G and G_m/I_D vs. IC curves [8].

2.5.1 Velocity saturation and its effect on drain current and transconductance

Conventionally, velocity saturation is believed to happen due to the saturation of drift velocity v_{drift} of the charge carriers, to a particular value

v_{sat}, when the longitudinal electrical field E_{x} in the MOSFET channel exceeds a certain critical value E_{c}. A mobility term μ_{eff}, called *effective mobility*, that relates the drift velocity to the combined effect of longitudinal and vertical electric field, can be defined as

$$\mu_{\text{eff}} \triangleq \frac{v_{\text{drift}}(E_{\text{x}})}{|E_{\text{x}}|}. \tag{2.22}$$

Normalizing the velocity and electric field terms to v_{sat} and E_{c} respectively, so (2.22) can be written as

$$u_{\text{eff}} \triangleq \frac{\mu_{\text{eff}}}{\mu_{\text{z}}} = \frac{\nu(e)}{e}, \tag{2.23}$$

where $\nu(e)$ is the normalized velocity, e is the normalized electric field and

$$\mu_{\text{z}} \triangleq \frac{v_{\text{sat}}}{E_{\text{c}}}. \tag{2.24}$$

μ_{z} includes the effect of the vertical electrical field, since the value of the critical field E_{c} is dependent on the value of the low-field mobility μ_0, which in turn depends on the vertical electrical field. In the presence of mobility reduction due to vertical field, μ_{z} is not equal to μ_0. We will return to this when we discuss mobility reduction due to vertical field.

Different velocity-field models can be used to account for the velocity saturation effect [8]:

- *Model 1* Piecewise linear

$$u_{\text{eff}} = \begin{cases} 1 & \text{for } e < 1 \\ 1/e & \text{for } e \geq 1 \end{cases} \tag{2.25}$$

- *Model 2* Continuous

$$u_{\text{eff}} = \frac{1}{1+e} \tag{2.26}$$

- *Model 3*

$$u_{\text{eff}} = \begin{cases} \dfrac{1}{1+e/2} & \text{for } e < 2 \\ 1/e & \text{for} e \geq 2 \end{cases} \tag{2.27}$$

The drain current in a MOSFET is conventionally given by the drift-

diffusion equation,

$$I_D = \mu_{eff} Q_i E_x + \mu_{eff} U_T \frac{\partial Q_i}{\partial x}. \tag{2.28}$$

Eq. (2.28) can be written in the normalized form as

$$i_d = 2q_i \frac{u\, e}{\lambda_c} - u \frac{\partial q_i}{\partial \xi}, \tag{2.29}$$

where u is the effective mobility normalized to the low-field mobility μ_0 (and not μ_z), i.e.,

$$u \triangleq \frac{\mu_{eff}}{\mu_0} = \frac{\mu_{eff}}{\mu_z} \frac{\mu_z}{\mu_0}, \tag{2.30}$$

and λ_c, called the *velocity saturation parameter*, is defined as

$$\lambda_c \triangleq \frac{2U_T}{E_c L} = \frac{2\mu_0 U_T}{v_{sat} L}. \tag{2.31}$$

The normalized inversion charge density q_i in (2.29) ($q_i = Q_i/Q_{spec}$), normalized using specific charge $Q_{spec} = 2nU_T C_{ox}$ is given by the basic charge equation of the MOSFET [18]:

$$2q_i + \ln q_i = v_p - v. \tag{2.32}$$

where v_p and v are the pinch-off and channel voltages respectively, normalized to the thermal voltage U_T.

Traditionally, velocity saturation is considered to occur only in strong inversion and therefore only the drift term in (2.29) is considered for the analyses. In the nanoscale devices however, owing to their very short channel lengths it is possible that the longitudinal electrical field reach the critical value even in weak inversion. In the following analyses, we will consider the effect of velocity saturation on the drain current while including both the drift and diffusion terms so as to derive expressions that are continuous from weak to strong inversion.

According to the concept of charge potential linearization [18], the normalized surface and pinch-off potentials in a MOSFET can be related to the normalized inversion charge density by

$$\psi_s = \psi_p + 2q_i. \tag{2.33}$$

Since the derivative of the surface potential is nothing but the negative of the longitudinal electric field, taking the derivative with respect to

the normalized distance along the channel $\xi (= x/L)$ on both sides of (2.33) we obtain

$$-e\left(\frac{E_{\mathrm{c}}L}{U_{\mathrm{T}}}\right) = \frac{\partial \psi_{\mathrm{s}}}{\partial \xi} = 2\frac{\partial q_{\mathrm{i}}}{\partial \xi} \quad \text{i.e.} \tag{2.34}$$

$$e = -\lambda_{\mathrm{c}}\frac{\partial q_{\mathrm{i}}}{\partial \xi}. \tag{2.35}$$

Substituting (2.35) in (2.29) gives

$$i_{\mathrm{d}} = -u\left(2q_{\mathrm{i}} + 1\right)\frac{\partial q_{\mathrm{i}}}{\partial \xi}. \tag{2.36}$$

In a velocity saturated device, the inversion charge density at the drain, q_{d}, approaches a particular saturated value $q_{\mathrm{d_{sat}}}$, unlike a long channel transistor in which it approaches 0. The drain current is saturated at the drain to a value $i_{\mathrm{d_{sat}}}$ which limits the current in the entire channel to $i_{\mathrm{d_{sat}}}$ because of current continuity. So, ignoring the effect of mobility reduction due to vertical field for the moment, such that $\mu_{\mathrm{z}} = \mu_0$, implying $u = u_{\mathrm{eff}}$, under velocity saturation, at the drain we can write

$$q_{\mathrm{i}} = q_{\mathrm{d_{sat}}}, \tag{2.37a}$$

$$v = u\,e = 1, \tag{2.37b}$$

$$\frac{\partial q_{\mathrm{i}}}{\partial \xi} = 0, \tag{2.37c}$$

and hence, from (2.29),

$$i_{\mathrm{d_{sat}}} = \frac{2\,q_{\mathrm{d_{sat}}}}{\lambda_{\mathrm{c}}}. \tag{2.38}$$

The normalized source transconductance is calculated as

$$g_{\mathrm{ms}} \triangleq -\frac{\partial i_{\mathrm{d}}}{\partial q_{\mathrm{s}}}\frac{\partial q_{\mathrm{s}}}{\partial v_{\mathrm{s}}}. \tag{2.39}$$

Let us now consider the effect of each of the mobility models (2.25) to (2.27) on (2.36) separately.

- *Model 1*
  Assuming that the lateral electric field remains less than the critical field at each point along the channel so that the carrier velocity saturates right at the drain and hence $u = 1$ throughout the channel upto the

drain, integrating (2.36) from source to drain results in

$$i_{\mathrm{d}} = q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d}} - q_{\mathrm{d}}^2. \tag{2.40}$$

In velocity saturation, as mentioned earlier, $q_{\mathrm{d}} = q_{\mathrm{d_{sat}}}$ and $i_{\mathrm{d}} = i_{\mathrm{d_{sat}}}$, therefore the drain current can be rewritten as

$$i_{\mathrm{d_{sat}}} = q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d_{sat}}} - q_{\mathrm{d_{sat}}}^2. \tag{2.41}$$

Solving (2.41) and (2.38) together, we obtain

$$q_{\mathrm{d_{sat}}} = \frac{2\,\lambda_{\mathrm{c}}\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}} + \sqrt{4\left(1+\lambda_{\mathrm{c}}\right) + \lambda_{\mathrm{c}}^2\left(1 + 2\,q_{\mathrm{s}}\right)^2}}, \tag{2.42a}$$

$$i_{\mathrm{d_{sat}}} = \frac{4\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}} + \sqrt{4\left(1+\lambda_{\mathrm{c}}\right) + \lambda_{\mathrm{c}}^2\left(1 + 2\,q_{\mathrm{s}}\right)^2}}. \tag{2.42b}$$

From (2.42b) we can write the following two asymptotes of $i_{\mathrm{d_{sat}}}$:

$$\text{weak inversion } \left(q_{\mathrm{s}} \ll 1\right): \quad i_{\mathrm{d_{sat}}} \approx \frac{q_{\mathrm{s}}}{1 + \lambda_{\mathrm{c}}/2}, \tag{2.43a}$$

$$\text{strong inversion } \left(q_{\mathrm{s}}\,\lambda_{\mathrm{c}} \gg 1\right): \quad i_{\mathrm{d_{sat}}} \approx \frac{2\,q_{\mathrm{s}}}{\lambda_{\mathrm{c}}}. \tag{2.43b}$$

Eq. (2.42b) can be inverted to obtain

$$q_{\mathrm{s}} = \frac{\sqrt{\lambda_{\mathrm{c}}^2\, i_{\mathrm{d_{sat}}}^2 + 2\,\lambda_{\mathrm{c}}\, i_{\mathrm{d_{sat}}} + 4\, i_{\mathrm{d_{sat}}} + 1}}{2} - \frac{1}{2}. \tag{2.44}$$

In strong inversion $\lambda_{\mathrm{c}}\, i_{\mathrm{d}} \gg 1$, so that (2.44) becomes

$$q_{\mathrm{s}} \approx \sqrt{i_{\mathrm{d_{sat}}}\left(1 + \frac{\lambda_{\mathrm{c}}^2\, i_{\mathrm{d_{sat}}}}{4}\right)}. \tag{2.45}$$

Comparing this with (2.40) for strong inversion saturation ($q_{\mathrm{d}} = 0$ and $q_{\mathrm{s}} \gg 1$) such that

$$q_{\mathrm{s}} \approx \sqrt{i_{\mathrm{d}}},$$

we can define an effective inversion coefficient that includes the effect of velocity saturation:

$$IC_{\mathrm{vs}} \triangleq i_{\mathrm{d}}\Big|_{\substack{\text{strong inversion}\\ \text{velocity saturation}}} = i_{\mathrm{d_{sat}}}\left(1 + \frac{\lambda_{\mathrm{c}}^2\, i_{\mathrm{d_{sat}}}}{4}\right). \tag{2.46}$$

Interestingly, the RHS of (2.46) has the same form as an empirical inversion coefficient introduced by Binkley to account for velocity saturation

[1, 9] –

$$IC_{\text{Binkley}} = IC\left(1 + \frac{IC}{4\,IC_{\text{crit}}}\right)$$

– from which we see that

$$IC_{\text{crit}} = \frac{1}{\lambda_c^2}.$$

The importance of $1/\lambda_c^2$ as a critical value of inversion coefficient that demarcates the onset of velocity saturation becomes clear when we consider the transconductance efficiency.

Using (2.32) and (2.42b) in (2.39), the transconductance is obtained as

$$g_{ms} = \frac{2\,q_s}{\sqrt{4(1+\lambda_c) + \lambda_c^2(1+2\,q_s)^2}}. \tag{2.47}$$

The weak inversion asymptote of g_{ms} is obtained for $q_s \ll 1$

$$g_{ms} = \frac{q_s}{1+\lambda_c/2} \tag{2.48}$$

which is equal to $i_{d_{sat}}$ in weak inversion (2.43a), hence,

$$\frac{g_{ms}}{i_{d_{sat}}} = 1. \tag{2.49}$$

In strong inversion $q_s \gg 1$, $q_s^2 \gg q_s$ and $q_s\,\lambda_c \gg 1$. The denominator of (2.47) can thus be reduced as

$$\begin{aligned}
&2+\lambda_c+\sqrt{4(1+\lambda_c)+\lambda_c^2(1+2\,q_s)^2}\\
=&2+\lambda_c+\sqrt{4\,\lambda_c(1+q_s\lambda_c)+(4+4\,q_s^2\lambda_c^2)+\lambda_c^2}\\
\approx&2+\lambda_c+\sqrt{4\,q_s\lambda_c^2+4\,q_s^2\lambda_c^2+\lambda_c^2}\\
=&2+\lambda_c+\sqrt{4\,\lambda_c^2(q_s^2+q_s)+\lambda_c^2}\\
\approx&2+\lambda_c+\sqrt{4\,q_s^2\lambda_c^2+\lambda_c^2}\\
\approx&2+\lambda_c+2\,q_s\lambda_c\\
\approx&2\,q_s\lambda_c.
\end{aligned}$$

Hence, in strong inversion

$$g_{ms} \approx \frac{1}{\lambda_c}, \tag{2.50}$$

and therefore,

$$\frac{g_{\rm ms}}{i_{\rm d_{sat}}} \approx \frac{1}{\lambda_{\rm c}\, i_{\rm d_{sat}}}. \tag{2.51}$$

Remarkably, even though both the drain current $i_{\rm d}$ and transconductance $g_{\rm ms}$ are affected by velocity saturation in both strong inversion and weak inversion regions, the transconductance efficiency $g_{\rm ms}/i_{\rm d_{sat}}$ remains invariant in weak inversion. It has the same value in weak inversion ($g_{\rm ms}/i_{\rm d_{sat}} = 1$) as for case without velocity saturation. On the other hand, in strong inversion, $g_{\rm ms}/i_{\rm d_{sat}}$ takes on a $1/i_{\rm d_{sat}}$ dependence as opposed to the $1/\sqrt{i_{\rm d_{sat}}}$ that it has without velocity saturation.

Eq. (2.47) can be equivalently expressed in terms of $i_{\rm d_{sat}}$ as

$$g_{\rm ms} = \frac{\sqrt{\lambda_{\rm c}^2\, i_{\rm d_{sat}}^2 + 2\,\lambda_{\rm c}\, i_{\rm d_{sat}} + 4\, i_{\rm d_{sat}} + 1} - 1}{\lambda_{\rm c}^2\, i_{\rm d_{sat}} + \lambda_{\rm c} + 2}, \tag{2.52}$$

eventually resulting in the following expression for transconductance efficiency:

$$\frac{g_{\rm ms}}{i_{\rm d_{sat}}} = \frac{\sqrt{\lambda_{\rm c}^2\, i_{\rm d_{sat}}^2 + 2\,\lambda_{\rm c}\, i_{\rm d_{sat}} + 4\, i_{\rm d_{sat}} + 1} - 1}{\lambda_{\rm c}^2\, i_{\rm d_{sat}}^2 + \lambda_{\rm c}\, i_{\rm d_{sat}} + 2 i_{\rm d_{sat}}}. \tag{2.53}$$

Eq. (2.53) is continuous from weak inversion to strong inversion with the term $i_{\rm d_{sat}}$ in the RHS being the same as inversion coefficient *IC* according to (2.1). The same strong inversion velocity saturation asymptote as given by (2.51) can be obtained by using $\lambda_{\rm c} i_{\rm d_{sat}} \gg 1$ in (2.53). The strong inversion asymptote without velocity saturation can be obtained by putting $\lambda_{\rm c} = 0$ and using $i_{\rm d_{sat}} \gg 1$:

$$\frac{g_{\rm ms}}{i_{\rm d_{sat}}} = \frac{1}{\sqrt{i_{\rm d_{sat}}}}. \tag{2.54}$$

Solving (2.51) and (2.54) together, i.e., finding the intersection point of the velocity saturation and non-velocity saturation strong inversion asymptotes, we obtain

$$i_{\rm d_{sat}} = \frac{1}{\lambda_{\rm c}^2},$$

where $i_{\rm d_{sat}}$ is the same as *IC*. This means that $IC = 1/\lambda_{\rm c}^2$ is that value of inversion coefficient at which the velocity saturation effect starts to manifest. It is for this reason that, as mentioned earlier, $1/\lambda_{\rm c}^2$ acts as a *critical inversion coefficient* for velocity saturation. However, more importantly, the role of $IC = 1$, that serves as the demarcation between the

weak inversion and strong inversion regions in a long channel MOSFET, is superceded by $IC = 1/\lambda_c$, which is the intersection of the strong inversion (velocity saturation) asymptote with the weak inversion asymptote in a short channel MOSFET. Thus, the value of the *velocity saturation factor* λ_c can be readily extracted from the g_{ms}/i_d characteristics of a device by simply locating the intersection of the curve's asymptotes. Eq. (2.53) as well as the asymptotes are plotted in Fig. 2.4.

- *Model 2*
Using (2.35) in (2.26) we can write the continuous mobility model as

$$u_{\text{eff}} = \frac{1}{1 - \lambda_c \frac{\partial q_i}{\partial \xi}}, \tag{2.55}$$

which, on substitution in (2.36), results in the normalized drain current

$$i_d = \frac{-\left(2q_i + 1\right)}{1 - \lambda_c \frac{\partial q_i}{\partial \xi}} \frac{\partial q_i}{\partial \xi} \quad \text{or}$$

$$i_d = -\left(2q_i + 1 - \lambda_c i_d\right) \frac{\partial q_i}{\partial \xi}. \tag{2.56}$$

Integrating from source to drain

$$\int_0^1 i_d \,\partial\xi = -\int_{q_s}^{q_d} \left(2q_i + 1 - \lambda_c i_d\right) \partial q_i$$

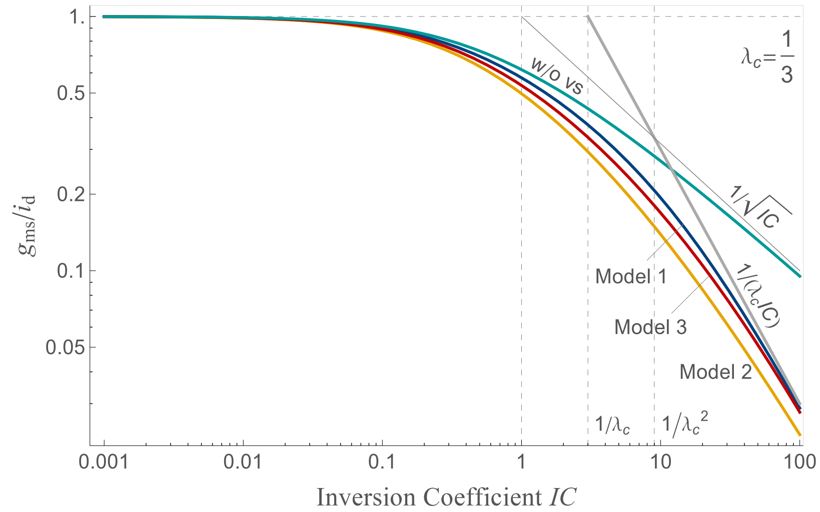


Figure 2.4: Transconductance efficiency g_{ms}/i_d as function of inversion coefficient IC for three different velocity-field models

leads to

$$i_{\mathrm{d}} = q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d}} - q_{\mathrm{d}}^2 - \lambda_{\mathrm{c}} i_{\mathrm{d}} \left(q_{\mathrm{s}} - q_{\mathrm{d}}\right),$$

i.e.,

$$i_{\mathrm{d}} = \frac{q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d}} - q_{\mathrm{d}}^2}{1 + \lambda_{\mathrm{c}} \left(q_{\mathrm{s}} - q_{\mathrm{d}}\right)}. \tag{2.57}$$

Since, in velocity saturation $q_{\mathrm{d}} = q_{\mathrm{d_{sat}}}$ and $i_{\mathrm{d}} = i_{\mathrm{d_{sat}}}$, the drain current can be rewritten as

$$i_{\mathrm{d_{sat}}} = \frac{q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d_{sat}}} - q_{\mathrm{d_{sat}}}^2}{1 + \lambda_{\mathrm{c}} \left(q_{\mathrm{s}} - q_{\mathrm{d_{sat}}}\right)}. \tag{2.58}$$

Solving (2.57) and (2.58) together, we obtain

$$q_{\mathrm{d_{sat}}} = \frac{2\,\lambda_{\mathrm{c}}\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}}\left(1 + 2\,q_{\mathrm{s}}\right) + \sqrt{4 + \lambda_{\mathrm{c}}^2 + 4\,\lambda_{\mathrm{c}}\left(1 + 2 q_{\mathrm{s}}\right)}}, \tag{2.59a}$$

$$i_{\mathrm{d_{sat}}} = \frac{4\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}}\left(1 + 2\,q_{\mathrm{s}}\right) + \sqrt{4 + \lambda_{\mathrm{c}}^2 + 4\,\lambda_{\mathrm{c}}\left(1 + 2 q_{\mathrm{s}}\right)}}, \tag{2.59b}$$

and on inverting (2.59b),

$$q_{\mathrm{s}} = \frac{\sqrt{4 i_{\mathrm{d_{sat}}} + 1} + \lambda_{\mathrm{c}}\, i_{\mathrm{d_{sat}}}}{2} - \frac{1}{2}. \tag{2.59c}$$

Using (2.37), the source transconductance is obtained to be

$$g_{\mathrm{ms}} = \frac{2 q_{\mathrm{s}}\Big(\lambda_{\mathrm{c}} + 4\left(1 + 2\,q_{\mathrm{s}}\right)\Big)}{\left(1 + 2\,q_{\mathrm{s}}\right)\left(4 + \lambda_{\mathrm{c}}^2 + 4\,\lambda_{\mathrm{c}}\left(1 + 2 q_{\mathrm{s}}\right) + 2\sqrt{4 + \lambda_{\mathrm{c}}^2 + 4\,\lambda_{\mathrm{c}}\left(1 + 2 q_{\mathrm{s}}\right)}\right)}. \tag{2.60}$$

Eqs. (2.60) and (2.59b) together would eventually give the transconductance efficiency $g_{\mathrm{ms}}/i_{\mathrm{d}}$. Alternatively, (2.59c) q_{s}, as a function of $i_{\mathrm{d_{sat}}}$ (*IC*), can be used directly in (2.60). The $g_{\mathrm{ms}}/i_{\mathrm{d}}$ as a function of *IC* is plotted in Fig. 2.4, in which we observe that the transconductance efficiency predicted by this model (Model 2) is lower than that predicted by Model 1.

- *Model 3*
  Following the same analyses as for Model 2, but using

$$u_{\mathrm{eff}} = \frac{1}{1 - \frac{\lambda_{\mathrm{c}}}{2} \frac{\partial q_{\mathrm{i}}}{\partial \xi}}$$

for effective mobility, we obtain

$$q_{\mathrm{d_{sat}}} = \frac{\lambda_{\mathrm{c}}\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}}\left(1 + q_{\mathrm{s}}\right)}, \tag{2.61a}$$

$$i_{\mathrm{d_{sat}}} = \frac{2\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2\right)}{2 + \lambda_{\mathrm{c}}\left(1 + q_{\mathrm{s}}\right)}, \tag{2.61b}$$

$$q_{\mathrm{s}} = \frac{\sqrt{\lambda_{\mathrm{c}}^2\, i_{\mathrm{d_{sat}}}^2 + 4\,\lambda_{\mathrm{c}}\, i_{\mathrm{d_{sat}}} + 16\, i_{\mathrm{d_{sat}}} + 4} + \lambda_{\mathrm{c}}\, i_{\mathrm{d_{sat}}}}{4} - \frac{1}{2}, \tag{2.61c}$$

and

$$g_{\mathrm{ms}} = \frac{2q_{\mathrm{s}}\left(2 + 4\,q_{\mathrm{s}} + \lambda_{\mathrm{c}}\left(1 + q_{\mathrm{s}}\right)^2\right)}{\left(1 + 2\,q_{\mathrm{s}}\right)\left(2 + \lambda_{\mathrm{c}}\left(1 + q_{\mathrm{s}}\right)\right)^2} \tag{2.62}$$

The $g_{\mathrm{ms}}/i_{\mathrm{d}}$ as a function of *IC* is plotted in Fig. 2.4. Model 3 lies between the Model 1 and Model 2 and is closer to the curve of Model 1; the difference between the two being the largest in the moderate inversion region.

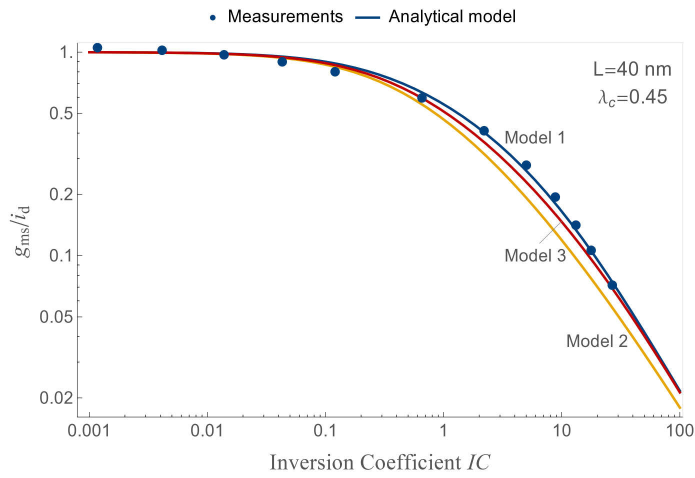
For all the three models discussed above, the conventional long-channel (sans velocity saturation) charge, current and transconductance equations can be obtained by using $\lambda_{\mathrm{c}} = 0$, which results in

$$q_{\mathrm{d_{sat}}} = 0, \tag{2.63a}$$

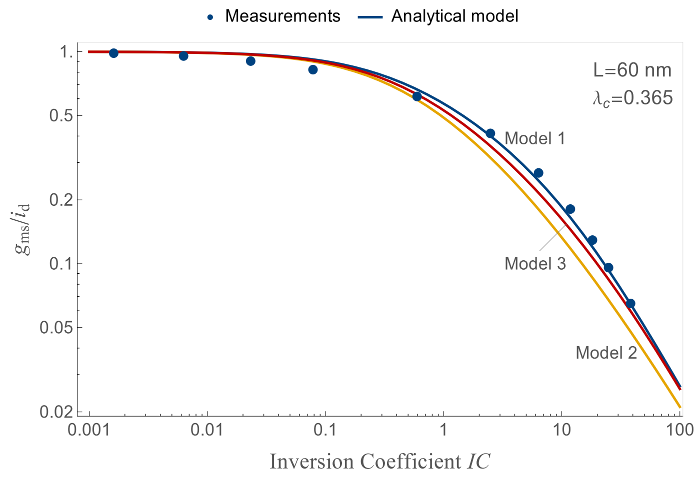
$$i_{\mathrm{d_{sat}}} = q_{\mathrm{s}} + q_{\mathrm{s}}^2, \tag{2.63b}$$

$$g_{\mathrm{ms}} = q_{\mathrm{s}}. \tag{2.63c}$$

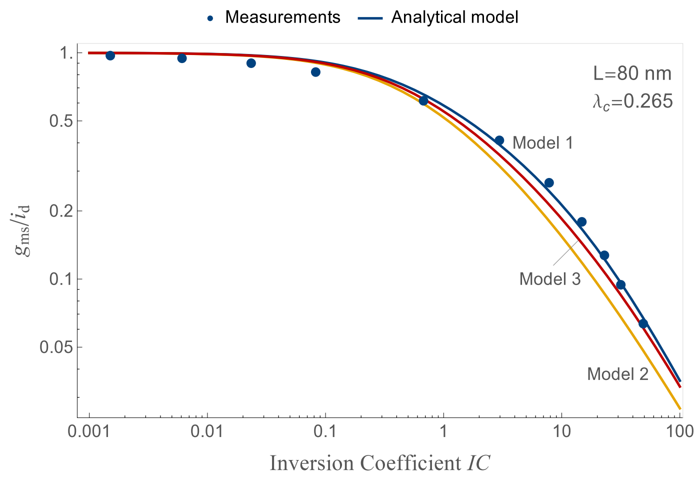
In Fig. 2.5 we show a comparison of the three analytical models of the transconductance efficiency $g_{\mathrm{ms}}/i_{\mathrm{d}}$ with measurement data from a 40 nm standard CMOS process. The comparison with three different channel lengths – 40 nm, 60 nm and 80 nm – using the appropriate value of the parameter λ_{c} for each one, reveals Model 1 to be the best match for the measurement data. Consequently, we will use Model 1 for further analytical developments, especially in Section 2.6.



(a)



(b)



(c)

Figure 2.5: Transconductance efficiency g_{ms}/i_d as function of inversion coefficient IC for three different velocity-field models: comparison with measurements from a 40 nm standard CMOS process for 40 nm, 60 nm and 80 nm channel lenghts

2.5.2 Drain Induced Barrier Lowering (DIBL)

DIBL is modeled as a shift in the threshold voltage [8] which can simply be accounted for in (2.32) as a shift in v_p.

2.5.3 Mobility reduction due to vertical field

Strictly speaking, mobility reduction due to vertical field is not a short-channel effects, but an effect related to the vertical dimension of the MOSFET. The effective mobility μ_eff defined in (2.22) or its normalized form u_eff defined in (2.23) are affected by both the longitudinal and vertical electrical fields. The normalizing factor μ_z includes the effect of the vertical electrical field, since the value of the critical field E_c is dependent on the value of the low-field mobility μ_0, which in turn depends on the vertical electrical field. In the presence of mobility reduction due to vertical field μ_z is not equal to μ_0.

Our previous analyses of velocity saturation effect was done while assuming the absence of mobility reduction due to vertical field, and therefore, assuming $\mu_\mathrm{z} = \mu_0$. In fact, in the presence of mobility reduction due to vertical field, μ_z is related to the low field mobility μ_0 [8] by

$$\frac{\mu_\mathrm{z}}{\mu_0} = \frac{1}{1+\theta\left(q_\mathrm{b}+q_\mathrm{i}/2\right)} = \frac{1}{k_1 q_\mathrm{i} + k_2}, \tag{2.64}$$

where

$$\theta = \frac{Q_\mathrm{spec}}{\epsilon_\mathrm{Si} E_0}, \tag{2.65a}$$

$$k_1 = \theta\left(\frac{1}{2} - \frac{1}{1+\frac{2}{\gamma_\mathrm{b}}\sqrt{\psi_\mathrm{p}}}\right), \tag{2.65b}$$

$$k_2 = 1 + \frac{\theta\psi_\mathrm{p}}{1+\frac{2}{\gamma_\mathrm{b}}\sqrt{\psi_\mathrm{p}}}. \tag{2.65c}$$

In (2.65), E_0 is the electric field intensity at which the mobility starts to decrease significantly, γ_b is the normalized body factor and ψ_p is the normalized pinch-off surface potential (corresponding to $q_\mathrm{i} = 0$). In (2.29), u is the effective mobility normalized to low-field surface mobility, i.e.,

$$u = \frac{\mu_\mathrm{eff}}{\mu_0} = \frac{\mu_\mathrm{eff}}{\mu_\mathrm{z}}\frac{\mu_\mathrm{z}}{\mu_0}.$$

Therefore, to account for the effect of mobility reduction due to vertical

field in the analyses carried out earlier, it is sufficient to multiply the u term by the RHS of (2.64), such that the drain current relation (2.36) becomes

$$i_{\mathrm{d}} = -u \frac{(2q_{\mathrm{i}}+1)}{k_1 q_{\mathrm{i}} + k_2} \frac{\partial q_{\mathrm{i}}}{\partial \xi}. \tag{2.66}$$

Assuming that velocity saturation right at the drain such that $u = 1$ throughout the channel and integrating from the source to drain

$$\int_0^1 i_{\mathrm{d}} \, \partial \xi = -\int_{\mathrm{q_s}}^{\mathrm{q_{d_{sat}}}} \frac{(2q_{\mathrm{i}}+1)}{k_1 q_{\mathrm{i}} + k_2} \partial q_{\mathrm{i}},$$

results in

$$\begin{aligned} i_{\mathrm{d_{sat}}} = &\frac{1}{k_1}\left[2q_{\mathrm{s}} + \left(1 - 2\frac{k_2}{k_1}\right)\ln\left(1 + \frac{k_1}{k_2} q_{\mathrm{s}}\right)\right] \\ &-\frac{1}{k_1}\left[2q_{\mathrm{d_{sat}}} + \left(1 - 2\frac{k_2}{k_1}\right)\ln\left(1 + \frac{k_1}{k_2} q_{\mathrm{d_{sat}}}\right)\right]. \end{aligned} \tag{2.67}$$

Eq. (2.67) can be approximated by its series expansion upto third order

$$\begin{aligned} i_{\mathrm{d_{sat}}} \approx &\frac{1}{k_2}\left[q_{\mathrm{s}} + \left(1 - \frac{k_1}{2k_2}\right) q_{\mathrm{s}}^2 - \frac{2k_1}{3k_2} q_{\mathrm{s}}^3\right] \\ &-\frac{1}{k_2}\left[q_{\mathrm{d}} + \left(1 - \frac{k_1}{2k_2}\right) q_{\mathrm{d_{sat}}}^2 - \frac{2k_1}{3k_2} q_{\mathrm{d_{sat}}}^3\right], \end{aligned} \tag{2.68}$$

which can be further simplified to the following, by assuming $\frac{k_1}{2k_2} \ll 1$,

$$i_{\mathrm{d_{sat}}} = \frac{1}{k_2}\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d_{sat}}} - q_{\mathrm{d_{sat}}}^2\right). \tag{2.69}$$

Now, just as (2.41)[2] and (2.38)[3] are equivalent, we define a similar equivalence for (2.69):

2. $i_{\mathrm{d_{sat}}} = q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d_{sat}}} - q_{\mathrm{d_{sat}}}^2$

3. $i_{\mathrm{d_{sat}}} = \frac{2 q_{\mathrm{d_{sat}}}}{\lambda_{\mathrm{c}}}$

$$\frac{1}{k_2}\left(q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d_{sat}}} - q_{\mathrm{d_{sat}}}^2\right) \equiv \frac{2\, q_{\mathrm{d_{sat}}}}{\lambda_{\mathrm{c}}} \quad \text{or} \tag{2.70a}$$

$$q_{\mathrm{s}} + q_{\mathrm{s}}^2 - q_{\mathrm{d_{sat}}} - q_{\mathrm{d_{sat}}}^2 \equiv \frac{2k_2\, q_{\mathrm{d_{sat}}}}{\lambda_{\mathrm{c}}} \tag{2.70b}$$

so that,

$$i_{\mathrm{d_{sat}}} = \frac{2\, q_{\mathrm{d_{sat}}}}{\lambda_{\mathrm{ck}}}, \tag{2.71}$$

with

$$\lambda_{\mathrm{ck}} = \frac{\lambda_{\mathrm{c}}}{k_2}. \tag{2.72}$$

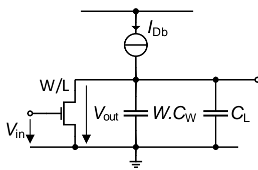
In effect, this means that we can continue to use all the analytical relations developed for velocity saturation and incorporate mobility reduction due to vertical field simply by replacing the velocity saturation factor λ_{c} with a modified factor λ_{ck}, which is slightly bias dependent due to the bias dependence of k_2.

Figure 2.6 shows the comparison of the analytical model of transconductance efficiency $g_{\mathrm{ms}}/i_{\mathrm{d}}$, as developed under with the full BSIM6 compact model for 40 nm, 60 nm and 80 nm channel lengths; measurements data is superimposed for convenience of comparison. It is evident that the simple analytical model accounting for short-channel effects developed in this section does a reasonably good job at fitting the measurement data. Thus, the model developed here can be used as the simple "stripped-down" version of the full BSIM6 compact model that serves the designer for the initial design guidance.

2.6 *IC* based design methodologies: short-channel effects

Let us now revisit the design methodologies for the design of simple analog and RF building blocks, discussed in Sections 2.3 and 2.4, and see how the short-channel effects, especially velocity saturation impacts them.

2.6.1 Bias current optimization for the gain stage

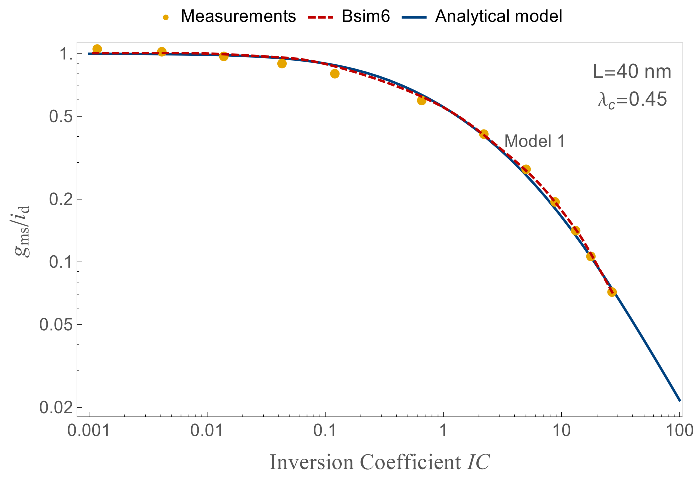


In Fig. 2.2, we plotted the normalized bias current for the capacitively loaded common-source stage , which is nothing but a plot of (2.12):

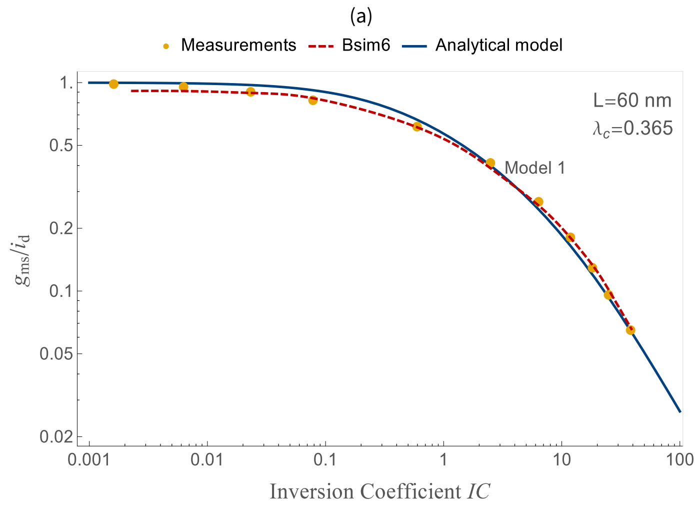
$$i_{\mathrm{db}} = \frac{\Omega_{\mathrm{v}}}{g_{\mathrm{ms}} - \Omega_{\mathrm{v}}\,\ell} IC.$$

Following our discussion of the previous section, it is easy to see that the short-channel effects affects the g_{ms} term in this equation. Using the Model 1 equation for g_{ms}[4] (2.52), and using $\lambda_{\mathrm{c}} = 1/3$, we again plot the normalized bias current as a function of IC as shown in Fig. 2.7. Here, we see that for a required gain, a higher bias current is required at the same IC than when velocity saturation is absent. This is especially noticable at high ICs and higher gains. Despite this increase in the required current, the optimum IC, i.e., the inversion coefficient for

4. $g_{\mathrm{ms}} = \frac{\sqrt{\lambda_{\mathrm{c}}^2 i_{\mathrm{dsat}}^2 + 2\lambda_{\mathrm{c}} i_{\mathrm{dsat}} + 4 i_{\mathrm{dsat}} + 1} - 1}{\lambda_{\mathrm{c}}^2 i_{\mathrm{dsat}} + \lambda_{\mathrm{c}} + 2}$



(a)



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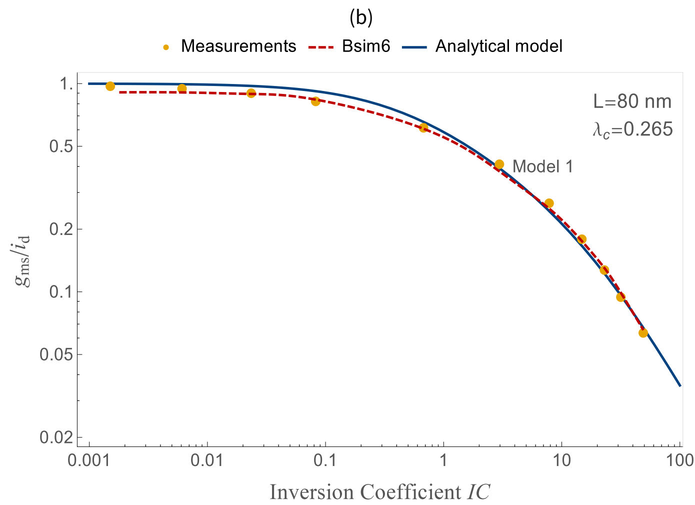


(c)

Figure 2.6: Transconductance efficiency g_{ms}/i_d as function of inversion coefficient IC: comparison with BSIM6 and measurements from a 40 nm standard CMOS process for 40 nm, 60 nm and 80 nm channel lengths

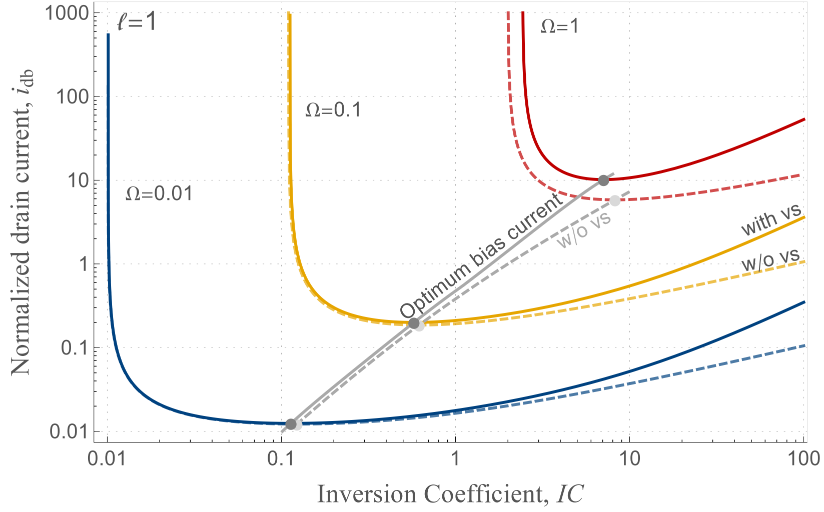


Figure 2.7: Effect of velocity saturation on normalized bias current for the capacitively loaded common-source stage (Fig. 2.1) vs. inversion coefficient

obtaining the minimum current at a given gain, shifts to the left towards weak inversion.

To verify the design methodology outlined above, we attempt the design of a common-source stage loaded with another common-source transistor of width 100 µm (implying a load capacitance $C_L = 18.5$ fF). We target a gain $A_v = 15$ dB and a working frequency $f = 24$ GHz, giving $\Omega_v = 0.83$. Choosing the minimum channel length, 40 nm ($\ell = 1$), provided by the 40 nm standard CMOS technology, we obtain the optimum value of IC, $IC_{opt} = 6.3$, that is in moderate inversion. The normalized optimum width $w_{opt} = 1.41$ is calculated using (2.9)[5] and the normalized bias current $i_{d_{bopt}} = 8.78$ is calculated using (2.12),[6] with the Model 1 equation for g_{ms}. Knowing the values of technology parameters we can calculate the optimum bias current $I_{D_{bopt}}$ and width W_{opt}. Eventually, plugging the values of W_{opt} and $I_{D_{bopt}}$ for simulating with the BSIM6 model, we obtain a gain of 14 dB at 24 GHz, which is close to the target gain of 15 dB[19].

5. $w = \frac{\Omega_v \ell}{g_{ms} - \Omega_v \ell}$

6. $i_{db} = \frac{\Omega_v}{g_{ms} - \Omega_v \ell} IC$

2.6.2 Optimum IC for RF design

Let us now consider the influence of short-channel effects on the FoM for RF design, defined in (2.21).[7] The FoM is proportional to two factors: g_{ms}/i_d and $\bar{\omega}_t$. While the former is equal to 1, the latter is proportional to IC at low values of the inversion coefficient IC; the FoM (fom_{rf}) will hence be proportional to IC at such low values of the inversion coefficient. At higher values of IC, however, owing to velocity satura-

7. $fom_{rf} \triangleq \frac{g_{ms}\bar{\omega}_t}{i_d}$

tion, g_{ms}/i_d becomes inversely proportional to IC (2.51)[8] and the $\bar{\omega}_t$ is practically constant (being equal to $g_{ms} = 1/\lambda_c$). Hence, the high-IC asymptote of fom_{rf} varies as $1/\lambda_c^2 IC$. Evidently, fom_{rf} that has an increasing low-IC asymptote while a decreasing high-IC asymptote will have a **maximum**. We must contrast this with the long channel case,

8. $\frac{g_{ms}}{i_{d_{sat}}} \approx \frac{1}{\lambda_c i_{d_{sat}}}$

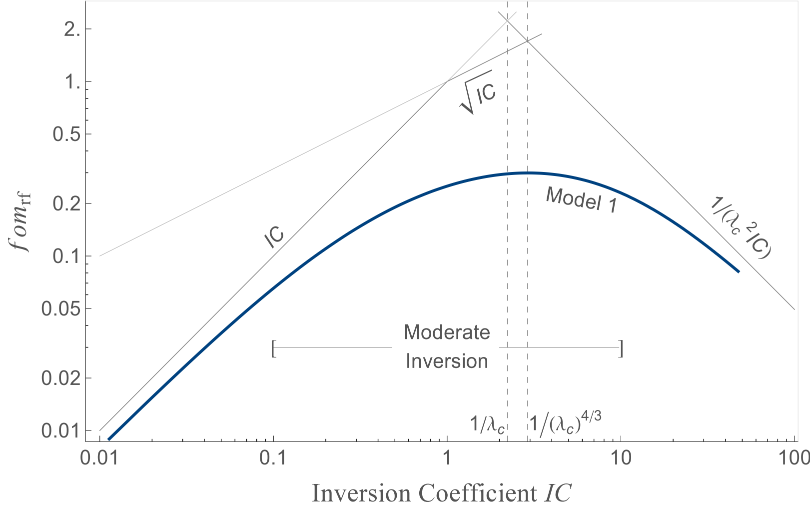
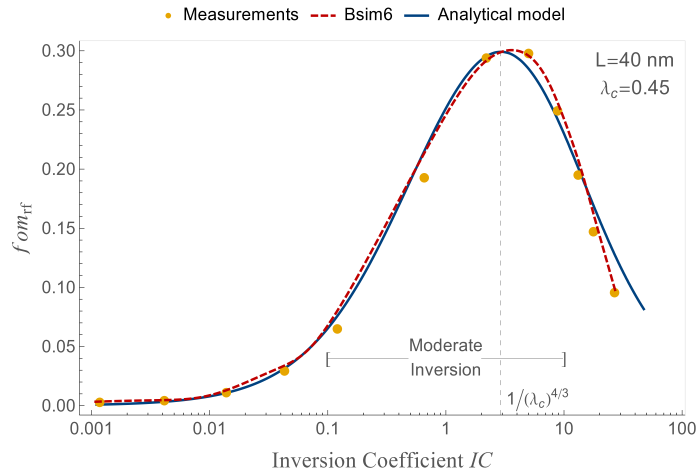


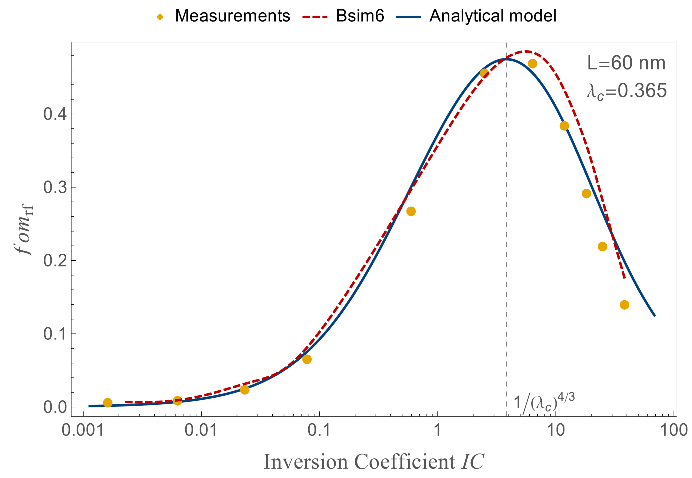
Figure 2.8: Normalized figure-of-merit fom_{rf} (on a log scale) as a function of inversion coefficient IC, along with the weak inversion and strong inversion asymptotes. The peak of the FOM lies at the intersection of $\sqrt{IC}$ and $1/(\lambda_c^2 IC)$ asymptotes

where g_{ms}/i_d would be proportional to $1/\sqrt{IC}$ and $\bar{\omega}_t$ to $\sqrt{IC}$, rendering fom_{rf} (nearly) constant. It is the prospect of the existence of a maximum in fom_{rf} vs. IC, because of which it was proposed as a FOM for low-power RF design using dwonscaled devices. As discussed in Section 2.4, the inversion coefficient at which fom_{rf} is maximum can be used as the optimum IC that would allow to maximize the dc gain and minimize the noise at a given bias current. Figure 2.9 shows a comparison of the analytical function of fom_{rf}, derived from the g_{ms}/i_d and g_{ms} for the Model 1 velocity-field model, with BSIM6 and measurements from a 40 nm standard CMOS process for 40 nm, 60 nm and 80 nm channel lengths. The presence of the peak and hence of the optimum inversion coefficient can be readily noticed.

From Fig. 2.8, it can be noticed that the peak of fom_{rf} lies at the intersection of its strong inversion asymptote $1/\lambda_c^2 IC$ with an $\sqrt{IC}$ asymptote, instead of being located at the former's intersection with the IC asymptote. The same is confirmed in Fig. 2.9 at two other channel lengths. The $\sqrt{IC}$ can be attributed to g_{ms}/i_d that starts to tend to $1/\sqrt{IC}$ before tending to $1/\lambda_c IC$ due to velocity saturation (see Fig. 2.4), while $\bar{\omega}_t$ is still tending slightly to IC, thereby lending a $\sqrt{IC}$ dependence to fom_{rf}.



(a)



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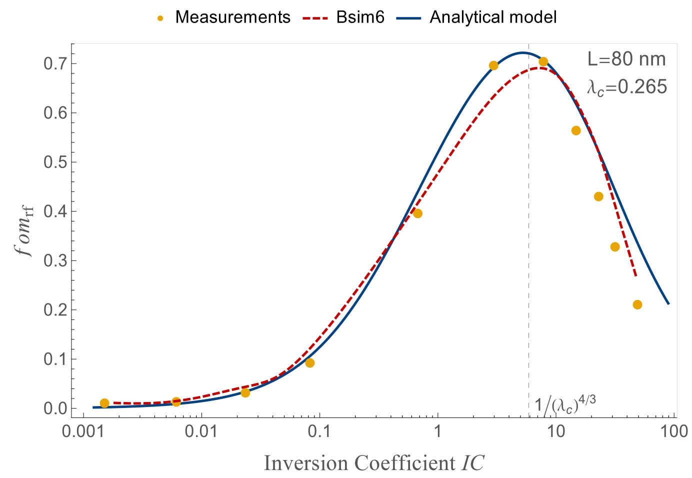


(c)

Figure 2.9: fom_{rf} as a function of inversion coefficient IC: comparison with BSIM6 and measurements from a 40 nm standard CMOS process for 40 nm, 60 nm and 80 nm channel lengths

Consequently, the intersection point that corresponds to the peak value of fom_{rf} lies at $IC = 1/\left(\lambda_{\mathrm{c}}^{4/3}\right)$, which is the optimum inversion coefficient. This optimum IC lies in the **moderate inversion** region as can be seen from Figs. 2.8 and 2.9. Since the velocity saturation parameter λ_{c} increases with decreasing channel length,[9] the optimum IC is bound to be pushed further left into the moderate inversion region towards weak inversion. This trend has been confirmed by other researchers through TCAD simulations [20] and measurements [21] over a wide variety of device geometries.

9. $\lambda_{\mathrm{c}} \triangleq \frac{2U_{\mathrm{T}}}{E_{\mathrm{c}} L}$

2.7 Summary

In this chapter we presented a simple, inversion coefficient IC based design methodology for the design of low-power analog and RF circuits. This methodology, which is intended to be used for initial design guidance, relies on a FOM (fom_{rf}) that allows to maximize the gain of a MOSFET operating at a given frequency, while minimizing its noise figure for a given current. It was shown that this FOM has a peak at a certain IC that can be treated as an optimum value for the MOSFET design. It was shown that this optimum IC lies in the moderate inversion region reinforcing the importance of this region for low-power design using downscaled devices from the state-of-the-art processes. The peaking behavior of the FOM, whose two constituents are the transconductance efficiency $g_{\mathrm{ms}}/i_{\mathrm{d}}$ and the cutoff frequency ω_{t}, is largely due to the short-channel effects, especially velocity saturation. In this context, the effect of velocity saturation on the drain current and transconductance efficiency was discussed and analytical expressions were derived using three different velocity-field models.

The importance of velocity saturation for short devices cannot be overemphasized. It has been well understood that velocity saturation is a consequence of scattering of charge carriers inside the MOSFET channel. On scaling the devices into nanometer regime (channel lengths below 30 nm), where the transport is expected to become quasi-ballistic and eventually ballistic, velocity saturation effects should be expected to diminish and eventually disappear for ultra-short devices. To the contrary, it has been shown in the literature that the carrier velocities still saturate in such devices, albeit near the source, due to the thermal limits.

In the rest of this thesis we will discuss the behavior of the ballistic and quasi-ballistic devices.

3 Ballistic transport: concepts and modeling approaches

In this chapter, we introduce the concept of ballistic transport in MOSFETs. Following a discussion on local equilibrium, a concept that no longer holds in the presence of ballisticity, we outline why new models are required for the ballistic regime. Subsequently, we give an overview and critique of the state of the research in modeling nanoscale ballistic MOSFETs.

3.1 Ballistic transport in semiconductor devices

BALLISTIC transport in semiconductor devices was postulated as a solution for low-power, high-speed applications by Shur [22, 23] in 1979. In 1985, IBM demonstrated experimental evidence of ballistic transport in GaAs devices [24]. In 1988, another team from IBM presented the I-V characteristics of sub-100 nm MOSFET at 77 K that provided further evidence of ballistic transport in semiconductor devices [25]. Since 2003, ballistic transport has also been included in the ITRS roadmap [26] as a possible technology booster.

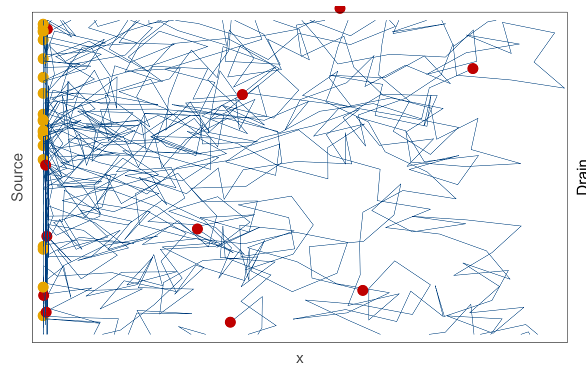
Ballistic transport in a semiconductor device implies that the charge carriers (electrons) travel across the device under the influence of a driving force, without experiencing any collisions and scattering that impede their motion, resulting in high currents. Such a transport of electrons would happen in a device with channel length L smaller than the mean free path of the carriers λ (in a given semiconductor and at a given temperature). Conventional long channel devices have channel lengths much greater than λ such that the electrons experience a lot of scattering events while traveling across. In such a channel, the velocity of the electrons is limited due to the scattering[1] and the transport is diffusive.[2] A device with a channel length comparable to λ lies on the continuum between the purely ballistic and purely diffusive regime. In such a device, high energy electrons travel ballistically, while the ones

$L < \lambda$	ballistic
$L \sim \lambda$	quasi-ballistic
$L \gg \lambda$	diffusive

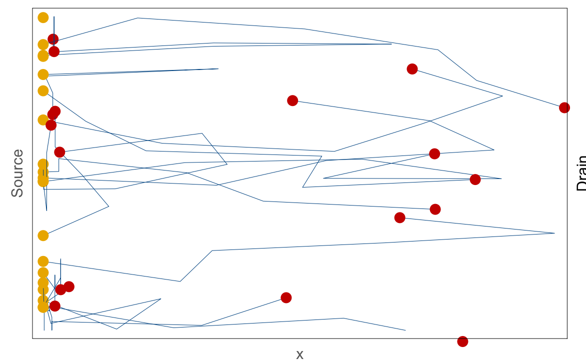
1. Velocity overshoot can occur in regions with very high longitudinal electric field.

2. In this context, the term *diffusive* includes the *drift* transport which is scatter dominated as well.

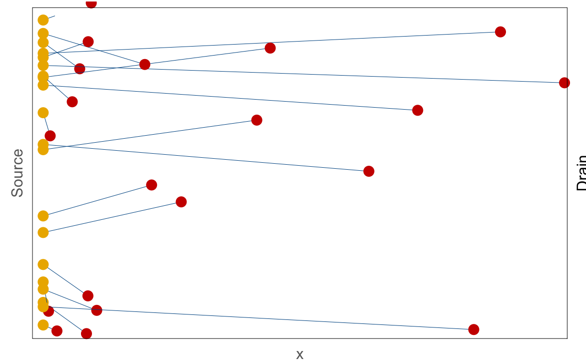
with lower energies travel through the drift-diffusion mechanism. Such a device is referred to as quasi-ballistic. This is shown graphically in Fig. 3.1.



(a) Diffusive $L \gg \lambda$



(b) Quasi-ballistic $L \sim \lambda$



(c) Ballistic $L < \lambda$

Figure 3.1: Schematic representation of the trajectories of electrons in semiconductor devices with different channel lengths

One may wonder whether the so-called ballistic transport in semiconductors is truly ballistic. Unlike in vacuum, or even in a gas, the electrons in a semiconductor travel inside the crystal and exchange energy with

it; consequently, the transport is not scatter-free. The answer to this conundrum lies in the *effective mass theory*, according to which, the motion of an electron in the periodic potential in a semiconductor crystal can be considered analogous to that of a free particle, albeit with an effective mass m^* instead of its free mass. So, indeed, once the electrons "adapts to the ideal crystal environment" [27], within the effective mass approximation, their motion in the crystal can be ballistic. Crystal impurities as well as electron-electron interactions introduce various scattering events that tend to bring the electron population in equilibrium. Observed over a time range greater than the *relaxation time* of electrons in the crystal (the time it takes for the electrons to come in equilibrium), the energy distribution function of electrons shows a Maxwellian equilibrium shape. On the contrary, the ballistic electrons occupy high energy regions of the energy distribution function [27] and show distinct high energy peaks [28]. This is shown schematically in Fig. 3.2. Up until the emergence of ballistic transport, most of the theory

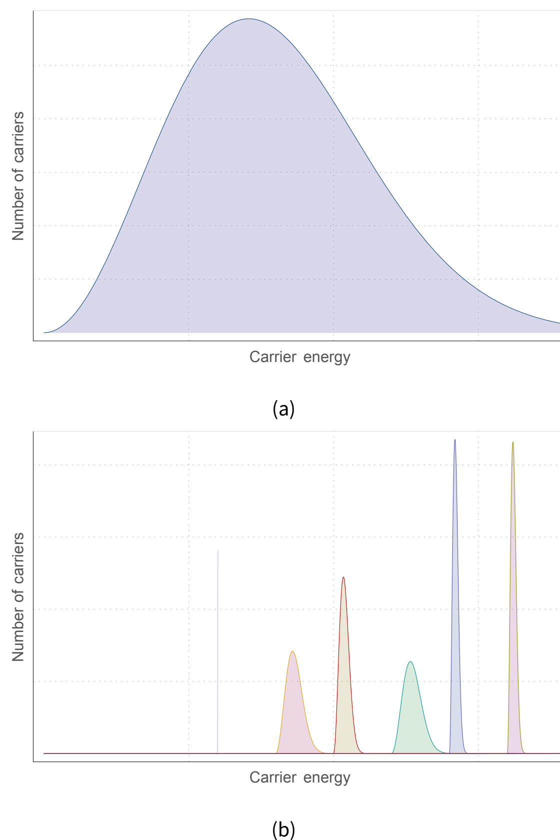


Figure 3.2: Schematic representation of the energy distributions of diffusive and ballistic electrons

of semiconductor devices has been built upon the assumption of *local equilibrium* that allows us to define a quasi Fermi level throughout the

device. To understand why the existing theory cannot be used as it is to model the ballistic and quasi-ballistic device, it is instructive to revisit the concept of equilibrium.

3.2 Concept of local equilibrium and Fermi level

To understand the concept of equilibrium, let us delve into thermodynamics. A given system can be characterized by a number of variables like temperature, pressure, volume etc., related to its physical and chemical properties. The system is in **equilibrium** if all these variables are independent of time though they may vary with position inside the system [29]. A *phase* is defined as a region of this system within which the variables is constant both in time and position, so that the whole system is nothing but an aggregate of mutually interacting phases.

- *Static equilibrium* A system will be in static equilibrium if it is completely isolated from its surroundings so that no energy exchange can take place. This implies that all the parameters would remain constant throughout the system. Obviously, such a system cannot carry any currents.

- *Nonuniform equilibrium* On the other hand, a system that can exchange energy with the surroundings through externally applied potentials, e.g., a homogeneous semiconductor bar with voltages V_{S} and V_{D} ($V_{\mathrm{S}} \neq V_{\mathrm{D}}$) applied to its left and right sides respectively, will not be in static equilibrium since the potential (electrostatic potential) inside the system would vary spatially. If this system does not exchange heat and matter with the surroundings, the system is in nonuniform equilibrium.

To define a condition for nonuniform equilibrium, we can divide it into different phases approximating the potential in each phase to be a constant. Then, the internal energy of a phase located at a position x would be given by

$$U(x) = T(x)S(x) - P(x)V(x) + \mu_{\mathrm{c}}N(x) + \Phi(x)N(x) \tag{3.1}$$

where, T, S, P and V are the temperature, entropy, pressure and volume respectively, and N is the number of particles. Φ is the potential energy associated with the system, i.e., the work done due to the externally applied forces. The chemical potential of the particles, formally defined

as

$$\mu_c = \frac{\partial U}{\partial N}\bigg|_{S,V,...}, \tag{3.2}$$

is the change in energy particle in adding ∂N particles to the system. More intuitively, the chemical potential μ_c quantifies (as a physical quantity) the tendency of a system to change [30], in the absence of external potentials. For example, a chemical reaction or a diffusion of a gas takes place because the μ_c is higher in the initial state than in the final state. In addition to the difference of the chemical potentials, the flow of the particles can also be driven by an external potential ϕ, e.g. gravitational, thermal or electric potential. In this case, the total driving potential becomes

$$\mu = \mu_c + \alpha\,\phi, \tag{3.3}$$

where α is the appropriate intrinsic quantity like mass, charge or entropy corresponding to the type of external potential. In our case dealing with electrons in a semiconductor device, the electric charge q is the relevant quantity. Then, the total driving potential becomes the **electrochemical potential** given by

$$\mu = \mu_c + q\,\phi, \tag{3.4}$$

so that the total driving force on the electrons is

$$\nabla\mu = \nabla\mu_c - q\,\nabla\phi. \tag{3.5}$$

It must be noted here that while $q\,\nabla\phi$ is a real physical force on the electrons, $\nabla\mu_c$ is only a *statistical* force; yet both cause a flow of electrons. The electrochemical potential μ is known as **Fermi level** in solid-state physics.

Now, in equilibrium, the change in entropy of a system is 0. Therefore, from (3.1), it follows that

$$\Delta S = \frac{\mu(x1) - \mu(x2)}{T}\Delta N = 0, \tag{3.6}$$

implying

$$\mu(x1) = \mu(x2), \tag{3.7}$$

that is, a dynamic system can be in nonuniform equilibrium if the electrochemical potential (Fermi level) is constant throughout the system.

Obviously, if a voltage is applied to the system, a gradient of the electrochemical potential is developed and the system is no longer in equilibrium. A **local equilibrium** can be said to exist in this system if we can still divide it into small regions that are close to equilibrium can be selected in the system. In this case the quantities like temperature and electrochemical potential can be locally defined if their variation in time and position is slow. In a semiconductor device, as we mentioned in the preceding section, such an equilibrium is established through the interaction amongst electrons and other scattering mechanisms. It should be noted, however, that in such a semiconductor the electron populations in the conduction and valence bands is displaced from their thermal equilibrium values. Hence, the charge carrier populations (holes and electrons) cannot be described using a single Fermi level for the semiconductor, but using separate Fermi levels for each band called the **quasi Fermi levels**. For a semiconductor device in local equilibrium, a quasi Fermi level can be defined locally at each point, and hence carrier distribution can be calculated at each point using Fermi-Dirac statistics.

As mentioned in Section 3.1, most of the semiconductor device theory has been built on the assumption of local equilibrium. Due to the absence of scattering and collisions, the mechanism that brings about the equilibrium is lost and the assumption of local equilibrium is no longer valid in devices with ballistic transport. This is the main reason that makes the modeling of ballistic semiconductor devices difficult, as we discuss in the next section.

3.3 Challenges in modeling ballistic devices with classical models

Even though, owing to the effective mass theory, the motion of each electron in a semiconductor crystal can be regarded as that of a classical particle, obviously, it would be practically impossible to formulate the physics of a device in terms of the aggregate motion of each electron. The transport of electrons in a semiconductor has to be treated statistically: as that of a distribution of particles. The Boltzmann transport equation (BTE) [31, 32] captures the physics of carrier transport from a semi-classical point of view by describing the change of the carrier distribution function in position-velocity space due to internal and

external forces, collisions and generation-recombination of particles. The distribution function, which is a solution of the BTE, can then be used to calculate the charge, current and kinetic-energy densities. Accurate solutions of the BTE are possible numerically. Monte-Carlo (MC) simulations which solve the BTE numerically are highly effective in understanding the behavior of a device but are not suitable for design of circuits because of their computationally intensive nature. However, by making several simplifying assumptions (e.g. relaxation time approximation for scattering), the BTE can be solved analytically.

The drift-diffusion (DD) equation is the simplest transport model that can be derived from the BTE. It is derived by taking the first two moments of the BTE and describes the current as a sum of two components- drift, governed by the electric field gradient and diffusion, governed by the electron density gradient. Effects like velocity saturation and mobility reduction due to vertical field are introduced as second order effects in short channel devices through the field dependent velocity and mobility expressions as discussed in detail in Chapter 2. The DD equation has been the workhorse of the modeling and simulation activities down to the sub-micrometer technologies but it starts to show its limitations in the nanometer regime. Even though the drift-diffusion equation can be used to model nanometer MOSFETs (e.g. 30 nm [33]), unphysical values of parameters like saturation velocity need to be used. In general, the DD equation underestimates the current in a nanometer MOSFET [34].

The inaccuracy of the DD equation in the nanometer regime can be attributed to the underlying assumptions, most notably the assumption of local equilibrium [35, 36]. In the presence of ballistic electrons, ballistic peaks develop in the overall electron distribution function and it is no longer in equilibrium [28]. In such a case, no local Fermi level can be defined and transport becomes non-local in nature, limiting the applicability of the drift-diffusion based models.

Higher order transport equations like hydrodynamic or energy-transport models have been derived from the BTE under various assumptions and using different methods [35, 37, 38, 39]. These models account for effects like hot-electron transport and velocity overshoot but none is formulated explicitly for ballistic transport. It has been shown that the moment based equations are not able to describe quasi-ballistic transport accurately [28, 34].

3.4 Modeling approaches for ballistic & quasi-ballistic MOSFETS

3.4.1 Transport over a barrier: Natori model

Owing to the challenges and complications involved in modeling ballistic and the quasi-ballistic nanoscale MOSFETs through classical methods, an alternative physical picture of the MOSFET has been proposed. Initially proposed by Natori for the ballistic MOSFET [25, 40], in this model, the source and drain ends are considered to be electron reservoirs in thermal equilibrium. The shape of the potential in the channel of a nanoscale MOSFET is such that a potential barrier exists from the source to the channel and then the potential gradually decreases towards the drain (assuming $V_{DS} > 0$), as shown in Fig. 3.3. The height of

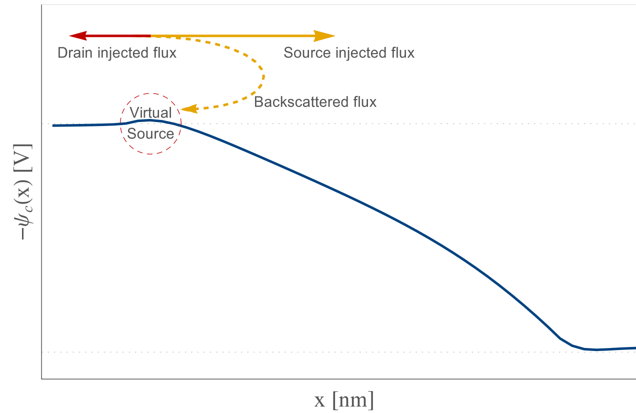


Figure 3.3: Potential profile and fluxes in a nanoscale MOSFET

the potential barrier, known as the **virtual source** [41], is controlled by the gate voltage, that ultimately controls the number of carriers injected over this barrier into the channel.

The Natori model is in fact based on the flux theory of McKelvey et al. [42] who presented an alternative flux based approach to model the carrier transport in semiconductors. A flux is defined as the number of carriers crossing an unit area per unit time and can be represented as the product of the volume density of the carriers and the velocity, i.e.,

$$f(x) = n(x)\,v(x). \tag{3.8}$$

The transport is treated in terms of fluxes injected from the source and

the drain [43], such that the drain current density can be written as

$$I_{\mathrm{D}} = q\left(f_{\mathrm{s}}^{+} - f_{\mathrm{d}}^{-}\right), \tag{3.9}$$

where the subscripts s and d stand for source and drain and the superscripts refer to the direction of flux flow, + being from source to drain.

As discussed in the preceding section, in the presence of ballistic transport there is no local equilibrium. Because of this, the flux or the drain current cannot be defined at each point in the channel. However, the virtual source is in a special kind of equilibrium such that carriers injected from the source are in equilibrium with the source and those coming from the drain are in equilibrium with the drain. Therefore, the overall drain current density in ballistic or quasi-ballistic MOSFET is expressed as the current density (drain current normalized to the channel width) evaluated at the virtual source

$$I_{\mathrm{D}} = qn(0)\,v(0), \tag{3.10}$$

where $n(0)$ is the carrier density at the virtual source and $v(0)$ is the average carrier velocity, in the longitudinal direction, at the virtual source. Eq. (3.10) is, in fact, universally valid, irrespective of the mode of transport.

3.4.2 Flux scattering theory: Lundstrom Model

Using the flux theory Lundstrom extended the Natori model to account for scattering in the channel. In Lundstrom's model of quasi-ballistic devices (transport with scattering) a backscattered flux is also accounted for, and the MOSFET I-V characteristics are presented in terms of scattering parameters (reflection/transmission coefficients) [44, 45, 46]. The claimed advantage of the scattering model over the conventional model is its success in modeling the quasi-ballistic and ballistic current in the nanoscale MOSFET.

The basic postulates of the flux scattering theory of the MOSFET are:

1. The current through the device can be decomposed into positively (from source to drain) and negatively (from drain to source) directed fluxes.

2. The positive flux over the source to channel barrier is injected from the source.

3 The height of the barrier is controlled by the gate to source voltage V_G.

4 The negative flux is composed of two components:
- Backscattered fraction of the flux injected from the source.
- Fraction of the drain injected flux reaching the source.

5 Combining the three components to obtain the net flux on top of the source-channel barrier (virtual source), the drain current density at this point can be evaluated as [46]:

$$I_D = q\, n_i(0) \left(\frac{1-r}{1+r}\right) \upsilon_T \left(\frac{1 - e^{-V_{DS}/U_T}}{1 + \left(\frac{1-r}{1+r}\right) e^{-V_{DS}/U_T}}\right) \tag{3.11}$$

where, $q\, n_i(0)$ is the inversion charge density at the virtual source, υ_T is the thermal injection velocity and V_{DS} is the drain-source bias. This result is applicable for non-degenerate statistics but can be modified to account for degenerate statistics by replacing the exponentials with appropriate Fermi functions [46]. r, called the *backscattering coefficient*, is an important parameter about which we discuss further in detail a bit later.

6 The flux injected from the drain is suppressed at high drain bias.

7 The left and right directed reflection/transmission coefficients are assumed to be equal at low drain bias.

8 In the special case when $r \to 0$, i.e., the transport becomes purely ballistic and (3.11) then becomes:

$$I_D = q\, n_i(0)\, \upsilon_T \left(\frac{1 - e^{-V_{DS}/U_T}}{1 + e^{-V_{DS}/U_T}}\right), \tag{3.12}$$

which is Natori's formulation of ballistic transport [40].

9 For high drain bias, $V_{DS} \gg U_T$, (3.11) can be rewritten as

$$I_D = C_{ox}\big(V_{GS} - V_T\big) \left(\frac{1-r}{1+r}\right) \upsilon_T \tag{3.13}$$

wherein, $q\, n_i(0) = C_{ox}\big(V_{GS} - V_T\big)$ has been substituted. (3.13) is the current in saturation.[3]

3. It is interesting to note that in a quasi-ballistic MOSFET, the drain current saturates at V_{DS} greater than a few U_T, similar to what happens in weak inversion.

10 For the case $V_{DS} < U_T$ we can rewrite (3.11) as

$$I_D = q\,n_i(0)\big(1-r\big)v_T\frac{V_{DS}}{2U_T}, \tag{3.14}$$

which is similar to the long channel non-saturation in that it is linearly dependent on V_{DS}.

The **backscattering coefficient** r in (3.11) is one of the most important parameters in the virtual source based formulation of nanoscale MOSFETs, the reason why it has merited a lot of research [45, 47, 48, 49, 50, 51]. As the name implies, the parameter r $(0 < r < 1)$ is the fraction of the flux, injected from the source, that backscatters in the channel and reenters the source. Evidently, its value depends on the physics of scattering in the channel and ultimately on the applied source, drain and gate voltages. Invoking the Bethe condition for thermionic emission[4] [52], r is estimated to be

4. Bethe condition: thermionic emission over a junction occurs when the first U_T potential drop at the junction occurs over a length less than the mean free path.

$$r = \frac{\ell}{\ell+\lambda}, \tag{3.15}$$

where λ is the mean free path for backscattering and ℓ is the critical distance over which the potential drops by 1 U_T. In fact, the average velocity of the carriers at the virtual source is related to the thermal velocity through r:

$$v(0) = \left(\frac{1-r}{1+r}\right)v_T. \tag{3.16}$$

While (3.11) is a very simple model for nanoscale MOSFETs, its limitation is evident in (3.15), the definition of backscattering coefficient r. Even though it is possible to estimate the value of r through MC simulations, it cannot be extracted through physical measurement. In addition, there is a lack of agreement on its definition and alternative definitions and models have been proposed [47, 53]. It has also been shown that it is not only the scattering in the critical length ℓ but also the scattering as far as the drain that affects the drain current in a quasi-ballistic MOSFET [54]. Finally, even though a compact model based on the scattering theory has been developed [46, 55], it is apparent that this model does not scale seamlessly to the well established drift-diffusion for long channel devices.

3.4.3 Semiempirical model: Khakifirooz/Antoniadis model

Khakifirooz et al. have described a semiempirical model based on transport over the source channel barrier approach in [56]. The model employs 10 parameters out of which 6 are measured and 4 are fitted. The model is based on the same premise that current density through the MOSFET can be expressed as the product of charge density and the carrier velocity at the virtual source (3.10). The virtual source charge density is given by [56]

$$Q_i(0) = C_{inv}\, n\, U_T \ln\left(1 + \exp\frac{V_{GS} - \left(V_T - \alpha U_T F_f\right)}{n U_T}\right) \tag{3.17}$$

where C_{inv} is the effective gate capacitance per unit area in strong inversion, n is the subthreshold coefficient, V_T is the strong inversion threshold voltage corrected for DIBL, α is a fitting parameter and F_f is an empirical *inversion transition function* given by

$$F_f = \frac{1}{1 + \exp\left(\frac{V_{GS} - \left(V_T - \alpha U_T F_f/2\right)}{\alpha U_T}\right)}. \tag{3.18}$$

The nonsaturation region is modeled by modifying the velocity term with an empirical *saturation function*

$$F_s = \frac{V_{DS}/V_{DS_{sat}}}{\left(1 + \left(V_{DS}/V_{DS_{sat}}\right)^{\beta}\right)^{1/\beta}}. \tag{3.19}$$

Eventually, the drain current density can be expressed as

$$I_D = Q_i(0) v(0) F_s. \tag{3.20}$$

The function F_f given by (3.18) tends to zero in strong inversion while in weak inversion it tends to unity. This function is thus also used to account for saturation in weak inversion such that $V_{DS_{sat}}$ is equal to U_T in weak inversion and a particular value $V^s_{DS_{sat}}$ in strong inversion:

$$V_{DS_{sat}} = V^s_{DS_{sat}}\left(1 - F_f\right) + U_T F_f. \tag{3.21}$$

The function F_s given by (3.19) is similar to the velocity saturation function used in [8] but has been used empirically in this model to define the nonsaturation behavior. F_s is zero for $V_{DS} = 0$ and unity for $V_{DS} \gg V_{DS_{sat}}$. Evidently, in the strong inversion saturation case, the current will be

saturated because of the velocity term which will attain its full value and will be related to the thermal injection velocity. In weak inversion, the current has an exponential dependence on the overdrive voltage $V_{GS} - V_T$ and would again be saturated for $V_{DS} \gg U_T$, to a value dictated by the thermal injection velocity.

This model has been extended to be continuous between ballistic and drift-diffusion regimes [57] and has been validated with 45 nm devices, yet there is no denying the fact that the model is built upon purely empirical functions. In addition, the charge partitioning model of this extended model is founded on the claim that the gradual channel approximation cannot hold in ballistic MOSFETs. We doubt the universal validity of this claim and discuss it further in Section 5.5.

3.4.4 A unified model including drift-diffusion, velocity saturation and quasi-ballistic transport

In silicon the values of the saturation velocity and thermal injection velocity at room-temperature are very close but their temperature dependence is opposite. Whereas saturation velocity decreases with increasing temperature due to increased scattering, the thermal injection velocity increases. In [58], by performing thermal measurements on a strained-Si MOSFET and extracting the limiting velocity, the authors have shown that even at lengths down to 22 nm, strong scattering mechanisms are present within the channel. According to the authors, the mechanism limiting the velocity and hence the current is still the scatter dominated saturation velocity as opposed to the claim of the flux theory that limiting velocity is the thermal one. They propose an alternative current formulation to unify the drift-diffusion, velocity saturation and ballistic currents:

$$\frac{1}{I_D} = \frac{1}{I_{DD}} + \frac{1}{\min(I_B, I_{sat})} \tag{3.22}$$

where I_{DD} is the current due to carriers under drift and diffusion, I_B is the current due to the carriers which become ballistic and I_{sat} is the current due the velocity saturated carriers.

3.4.5 Chain of ballistic MOSFETs: Mugnaini model

Mugnaini et al. [59, 60] have demonstrated that a diffusive device can be modeled as a series combination of N ballistic devices and one drift-diffusion device. On the premise that the carrier population at the virtual source can be calculated as a sum of two separate carrier populations, one that is in equilibrium with the source and the other

that is in equilibrium with the drain, they develop the charge model for the ballistic MOSFET. The mobile charge density is given by

$$q_{\mathrm{m}} = q_{\mathrm{i}} \mathscr{W}\left(\frac{1}{2} e^{\frac{V_{G}-V_{S}-V_{T}}{U_{T}}} + \frac{1}{2} e^{\frac{V_{G}-V_{D}-V_{T}}{U_{T}}}\right), \tag{3.23}$$

with $q_{\mathrm{i}} = 2C_{\mathrm{eff}} U_{\mathrm{T}}$. $\mathscr{W}(\cdots)$ is the Lambert-ω function [61] and C_{eff}, V_{T} and U_{T} are the effective gate capacitance, threshold voltage and thermal equivalent voltage (kT/q), respectively. Based on the ideas of Buttiker [62], they postulate that in a diffusive, each scattering event can be treated as a thermalizing *Buttiker probe*. In other words, they propose that between each successive scattering event the electrons travel ballistically and are fully thermalized when they scatter, as they would in the source/drain contact of a ballistic device. Schematically, this is equivalent to representing a device with multiple scattering events as a chain of n ballistic devices, with

$$n = \frac{L}{\lambda},$$

where L is the channel length and λ the mean free path. The drain current density of the diffusive device is then shown to be given by

$$I_{\mathrm{D}} = \frac{\mu\, q_{\mathrm{i}}\, U_{\mathrm{T}}}{L}\left(\frac{q_{\mathrm{ms}}^2 - q_{\mathrm{md}}^2}{2q_{\mathrm{i}}^2} + \frac{q_{\mathrm{ms}} - q_{\mathrm{md}}}{q_{\mathrm{i}}}\right), \tag{3.24}$$

which is very similar to the EKV equation of the MOSFET [8, 63]. Here, μ_{n} is the low field mobility. The authors further demonstrate that a quasi-ballistic MOSFET can be modeled as a chain of $n+1$ ballistic devices, with the first n devices (with $n = 9$) on the source side aggregated into a single drift-diffusion device. The last ballistic device serves to provide the velocity saturation that is characteristic of nanoscale MOSFETs.

3.5 Impact of ballistic transport on RF performance of MOSFETS

As mentioned at the beginning of this chapter, ballistic transport was proposed as a solution for low-power and high-speed applications. In principle, a transit frequency in the range of terahertz can be achieved with nanoscale ballistic devices. Referring to the Lundstrom model, from (3.13),[5] for the ballistic case ($r = 0$) we can write the transconductance as

$$G_{\mathrm{m}} = W C_{\mathrm{ox}}\, \upsilon_{\mathrm{T}}. \tag{3.25}$$

5. $I_{\mathrm{D}} = C_{\mathrm{ox}}(V_{\mathrm{GS}} - V_{\mathrm{T}})\left(\frac{1-r}{1+r}\right)\upsilon_{\mathrm{T}}$

The transit frequency f_T is then given by

$$f_T \triangleq \frac{G_m}{2\pi C_{ox} W L} = \frac{v_T}{2\pi L}, \tag{3.26}$$

which results in a numerical value of 1.9 THz for $L = 10\,\text{nm}$ at $v_T = 1.2 \times 10^5\,\text{cm}\,\text{s}^{-1}$. This has been validated using NEGF simulations [64].

The question of noise in ballistic devices has not yet received much attention in the literature. It appears that due to the absence of diffusion the thermal noise would be completely absent and the noise in the ballistic deivces will be dominated by shot noise. Nonetheless, this is not a trivial question to answer and requires further research.

3.6 Summary & discussion

At the first encounter, the concept of ballistic transport seems very simple: just a bunch of electrons traveling under the influence of an electric field. Thus, developing a model for ballistic devices seems no more complicated than solving a high-school physics problem. However, a survey of the state-of-the-research very rapidly makes it clear that this apparent simplicity is deceptive. As we have discussed in this chapter, to model ballistic transport in semiconductor devices many fundamental concepts need to be revisited, and the model development has to start from the first-principles.

No doubt, the model of the ballistic MOSFET proposed by Natori [40], extended by Lundstrom [44] to include scattering, also manage to model the essential device physics in an elegant manner through simple mathematical formulations. However, these and the derivative works [47, 65, 66, 67] fail in providing a consistent set of charge, potential and drain current equations, that are **seamlessly scalable** from the ballistic to the long channel diffusive regime. Apart from the initial works, most of the subsequent models cannot even be classified as *compact models* because they rely on numerical solutions of integrals. In addition to the modeling approaches discussed in this chapter, and of course Monte-Carlo simulations, there are approaches to modeling nanoscale devices, notably the scattering matrix based approach [68], which is neither intuitive nor compact. In our opinion, the model developed by Mugnaini [59], discussed in Section 3.4.5, does a remarkably good job at being simple, compact and scalable, even though, unfortunately, it has not managed to gain a good traction.

Not surprisingly, from the circuit design perspective, the barrier to entry into ballistic transport regime is too high. The circuit design ecosystem including the CAD tools have been built around the drift-diffusion formulation that elegantly captures the complex physics of carrier transport, scattering, short-channel effects etc. into relatively simple equations that scale nicely with device dimensions. It is not hard to imagine the impracticality of a circuit design environment where the designers have to plug in a different model simply when they decide to change the channel length of a device.

In the subsequent chapters, we will discuss our attempts in understanding the ballistic phenomena and eventually modeling the nanoscale MOSFETs in a compact yet scalable manner.

A design oriented nanoscale MOSFET model 4

Despite the fact that several approaches and models exist for modeling ballistic MOSFETs, as summarized in the previous chapter, a compact model that includes ballistic, quasi-ballistic and drift-diffusion in a continuous manner is still missing currently. Barring the Mugnanini model, discussed in Section 3.4.5, the other approaches are either too mathematical or too empirical to fill in this gap. In this chapter, we outline the behavior that a MOSFET model that is scalable between ballistic and diffusive regimes needs to follow. We propose one such model and its I-V characteristics.

4.1 A scalable model

ACCORDING to the flux based model of MOSFETs, the drain current in saturation consists of the electrons injected over the virtual-source barrier [45, 69]. Depending on whether the channel length L is much longer than, comparable to, or shorter than the mean free-path λ of the electrons in the channel material, the transport in the device is diffusive, quasi-ballistic and ballistic, respectively [25]. Inspired by this modeling approach, let us perform a thought experiment in which we attribute the mean free-path as the scattering distance of each individual electron, i.e., we assume that each electron injected from the virtual-source encounters a scattering event after traveling a distance exactly equal to the mean free-path. It follows then, that just after the injection from the virtual-source, electrons would travel a distance λ without any scattering, i.e., ballistically. This would be true even in a device with a very long channel length such that electrons scatter throughout the rest of the channel.

This thought experiment leads us naturally to a macro-model of the MOSFET, like that shown in Fig. 4.1, in which we can split the channel into two sections – the first section of length λ at the source end (labeled

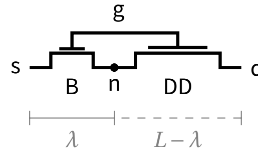


Figure 4.1: Macro-model schematic of a MOSFET with its channel split into two sections, a ballistic section of fixed length λ and a diffusive section of variable length $L-\lambda$, connected in series

B), and the remaining section of length $L-\lambda$ (labeled DD) – connected in series. This model is expected to be continuously scalable, as a function of channel length, between ballistic and diffusive regimes. To this end, the following conditions must be met:

1 *Current continuity* If the ballistic and diffusive MOSFETs are considered separately, for the same applied voltages, we would normally expect

$$I_{\mathrm{B}} > I_{\mathrm{DD}}.$$

The series connection of the ballistic and diffusive devices in Fig. 4.1 forces current continuity.

2 $V_{\mathrm{S}} \le V_{\mathrm{n}} \le V_{\mathrm{D}}$ Naturally, to ensure current continuity, the voltage V_{n} at the intermediate node (labeled n in Fig. 4.1) will have to take on values such that for this macro-model,

$$I_{\mathrm{B}} = I_{\mathrm{DD}}.$$

The expected behavior of this macro-model in two asymptotic cases can be readily defined:

- $L \gg \lambda$ With its channel length much larger than the mean free-path, a MOSFET is nothing but a long channel diffusive device. The transport in the DD part of the channel, which is scattering dominated, should dictate the overall behavior. Consequently, the device characteristics obtained with this model should resemble those obtained from a conventional drift-diffusion model.

- $L < \lambda$ A MOSFET with its channel length smaller than the mean free-path would be ballistic by definition. Likewise, for this case, the overall behavior of the model should resemble the behavior of a model for ballistic MOSFETs.

4.2 Model equations

Taking a cue from the above discussion, we implemented the macromodel of Fig. 4.1 using I–V equations from Natori's ballistic model [40, 46] for the B section and from the EKV model for long-channel bulk MOSFETs [8] for the DD section, such that

$$I_B(V_G, V_S, V_n) = I_{DD}(V_G, V_n, V_D). \tag{4.1}$$

In (4.1), assuming non-degenerate statistics, the current density I_B is given by [46]

$$I_B = Q_S \upsilon_T \left(\frac{1 - e^{-(V_n - V_S)/U_T}}{1 + e^{-(V_n - V_S)/U_T}} \right), \tag{4.2}$$

where Q_S is the inversion charge density at the source[1] and υ_T is the thermal velocity. The current density I_{DD} is given by the following set of equations [8] (already discussed in Chapter 2)

1. In fact, Q_S is the inversion charge density at the virtual source. However, since the exact position of the virtual source in the channel cannot be determined, we will treat its position as that of the source.

$$I_{DD} = \frac{2n\mu_0 C_{ox} U_T^2}{L - \lambda} (i_f - i_r) \tag{4.3a}$$

$$i_f = q_n + q_n^2 \tag{4.3b}$$

$$i_r = q_d + q_d^2 \tag{4.3c}$$

$$2q_{n,d} + \ln q_{n,d} = \frac{V_P - V_{n,D}}{U_T}. \tag{4.3d}$$

To maintain consistency in the manner the inversion charge is calculated for a given gate voltage, Q_S in (4.2) is also calculated by evaluating (4.3d) at source and using

$$Q_S = 2nC_{ox} U_T q_s. \tag{4.4}$$

Also, λ is related to υ_T, μ_0 terms in (4.2) and (4.3) through the Einstein relation

$$\lambda = 2\frac{\mu_0 U_T}{\upsilon_T}. \tag{4.5}$$

4.3 A modified model

A second look at (4.3a) reveals a couple of problems with this formulation:

- For a MOSFET with $L = \lambda$, $I_{DD} \to \infty$, i.e., the current takes an unphysical value.

- Similarly, when $L < \lambda$, I_{DD} becomes negative. This too is not physical since the drain cannot reverse its direction simply due to a device being short.

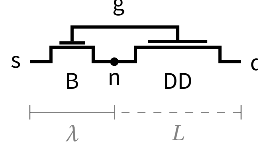


Figure 4.2: Macro-model schematic of a MOSFET with a ballistic section of fixed length λ added at the source side of a conventional diffusive section of variable length L

To overcome the problem pointed out above, we propose an alternative macro-model as shown in Fig. 4.2. This model is a slight modification of the model of Fig. 4.1: instead of splitting off a ballistic section of length λ from the total channel length L, in this model we simply append the ballistic section to the diffusive channel of length L, so that the total channel of the device is now $L+\lambda$. Eq. (4.3a) for current density through the DD section of the MOSFET now becomes

$$I_{\mathrm{DD}} = \frac{2n\mu_0 C_{\mathrm{ox}} U_{\mathrm{T}}^2}{L} (i_{\mathrm{f}} - i_{\mathrm{r}}), \tag{4.6}$$

with i_{f} and i_{r} being the same as in (4.3). Eq. (4.2) for current density I_{B} remains unchanged.

It is worth noting that the drain current equations given by (4.2) and (4.3) are saturating functions – I_{B} saturates when V_{n} is greater than 3 to 4 U_{T}, while $\mathrm{I_{DD}}$ saturates for $V_{\mathrm{D}} \geq V_{\mathrm{P}}$ – though the magnitude of the saturated currents would be different. Since the voltage at node n cannot go beyond the V_{S} and V_{D} limits, i.e., $V_{\mathrm{S}} \leq V_{\mathrm{n}} \leq V_{\mathrm{D}}$, the total drain current through the MOSFET cannot be more than I_{B} or I_{DD}, whichever is minimum:

$$I_{\mathrm{MOSFET}} \leq \min(I_{\mathrm{B}}, I_{\mathrm{DD}}). \tag{4.7}$$

Evidently, this modified model is faithful to the asymptotic cases discussed in Section 4.1:

1. $L \gg \lambda$ In the long channel case, $I_{\mathrm{DD}} < I_{\mathrm{B}}$, and therefore, according to (4.7), the drain current through the MOSFET will follow the behavior of the current through the diffusive device (I_{DD}).

2. $L < \lambda$ According to (4.6), when L becomes too small, I_{DD} becomes very large. Hence, following (4.7), the drain current through the MOSFET will

be dictated by I_B.

We can nonetheless wonder why, the B section in case 1 above, and likewise the DD section in case 2, would not have any impact (or, would have very little impact) on the overall behavior of MOSFET. To understand this we must study the behavior of the intermediate node n.

4.4 The intermediate node n

Assuming that the MOSFET in Fig. 4.2 is operating in saturation ($V_D \geq V_G$), for the long channel case ($L \gg \lambda$),

$$I_{\text{MOSFET}} \approx I_{DD},$$

therefore, I_B ($= I_{\text{MOSFET}}$) will have to be less than its saturation value $Q_S\, v_T$. From (4.2), this implies that V_n, the voltage at the node n, will have to be no larger than a few fractions of U_T above V_S, i.e, the ballistic part B, with its drain voltage as V_n, will operate in linear mode. In this case, the B section can be considered as a series resistor with a very small voltage drop across it, connected at the source end of the drift-diffusion MOSFET. On the other hand, for the ultra-short channel case ($L < \lambda$),

$$I_{\text{MOSFET}} \approx I_B,$$

with $I_B = Q_S\, v_T$, its saturation value. I_{DD} given by (4.6) would tend to take very high values for such small L, unless the $(i_f - i_r)$ term in the numerator compensates for it; that will indeed be the case, because I_{DD} ($= I_{\text{MOSFET}}$) cannot be any larger than I_B. Since the MOSFET is in saturation, i.e, $V_D \geq V_P$, from (4.3) $i_r \to 0$ and hence,

$$I_{DD} = \frac{2n\mu_0 C_{ox} U_T^2}{L - \lambda}\, i_f. \tag{4.8}$$

Given that the B section is in saturation, we can reasonably assume that the voltage V_n at its drain n would be at least as large as 3 to 4 U_T more than V_S, yet it would not be close to V_D so as to maintain the rather large drain current density I_B. Consequently, in this case, the DD section will act as a resistor at the drain end of the ballistic MOSFET across which a large fraction of V_{DS} will drop.

As a result of the above discussion, we can modify the condition with respect to the voltage at node n that we had stated in Section 4.3 as $V_S \leq V_n \leq V_D$. It is apparent that the upper limit of V_n will be always

below V_D, i.e.,

$$V_S \le V_n < V_D. \tag{4.9}$$

The above discussion is validated in Figs. 4.3 and 4.4, which were obtained by equating (4.2) and (4.3) and numerically solving for V_n. For the diffusive limit ($L \gg \lambda$), we observe in Fig. 4.3 that even in saturation for all $V_D \ge V_p$, the voltage drop V_n across the B part is only about 0.1 U_T, and therefore all the applied drain voltage is dropped only across the DD section (see Fig. 4.4). On the contrary, for the ballistic limit ($L < \lambda$), V_n saturates to a much higher value of approximately 12 U_T, yet it remains less than V_D. Rest of the V_D is dropped across the DD section, as can be seen in Fig. 4.4.

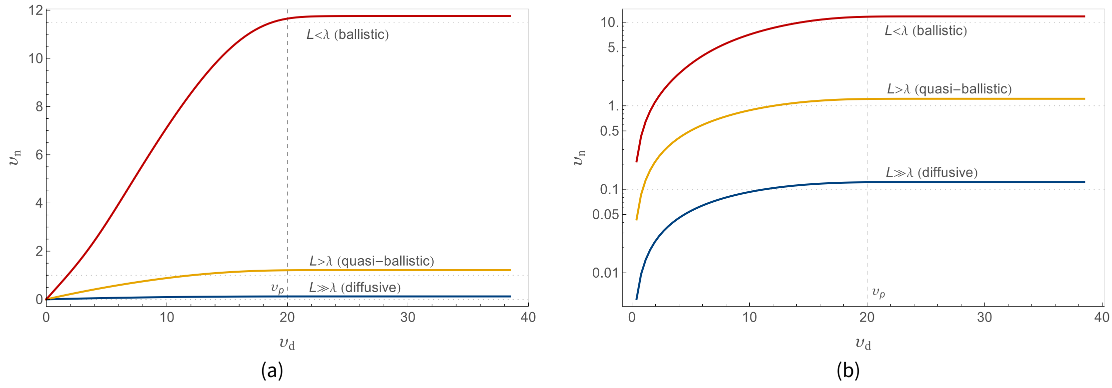


Figure 4.3: Variation of the voltage at intermediate node n (in linear and log scales) as a function of drain voltage for the ballistic, quasi-ballistic and diffusive cases. All voltages are normalized to U_T

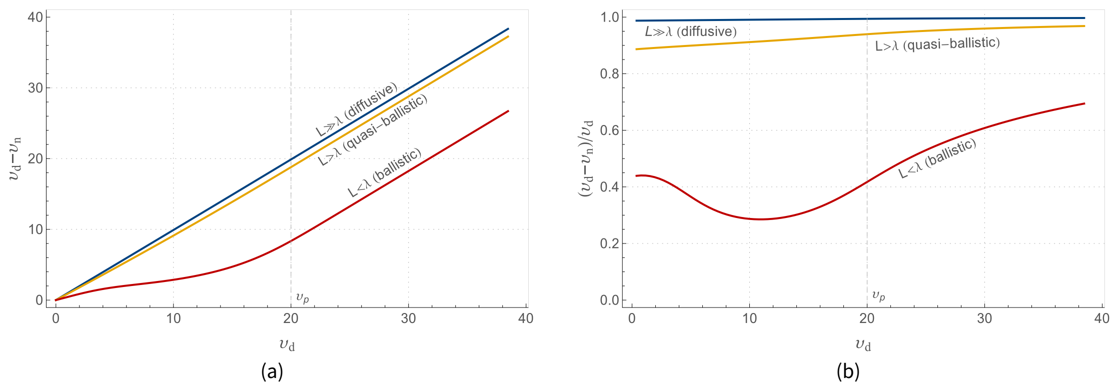


Figure 4.4: Voltage drop and the fraction of drain voltage drop across the DD section of Fig. 4.2 as function of drain voltage

4.5 *I–V* characteristics

In Fig. 4.5, we plot the I_D-V_G and I_D-V_D characteristics of the proposed model for three different channel lengths, namely 2 nm, 20 nm and 200 nm, which correspond respectively to the ballistic ($L < \lambda$), quasi-ballistic ($L > \lambda$) and diffusive ($L \gg \lambda$) cases. Recalling the discussion of Section 4.1 where we outlined the expected asymptotic behavior of a model scalable between ballistic and diffusive regimes, we see in this figure that for $L < \lambda$, the model practically follows the Lundstrom's ballistic model; using the EKV drift-diffusion model would overestimate the drain current by several orders of magnitude. Likewise, for $L \gg \lambda$, the model characteristics follow the drift-diffusion model, whereas the ballistic model overestimates the drain current.

The $L > \lambda$ case, which corresponds to a quasi-ballistic device, is quite interesting. In this case, the I_D-V_G curve follows the drift-diffusion curve except at very high V_G where it converges to the ballistic model. In a similar manner, the I_D-V_D starts off close to the drift-diffusion model, then starts deviating before converging to the ballistic model at high V_D. Since the ballistic current sets the limit of the drain current attainable in any device, that I_D tends to the ballistic curve at higher voltages, is not surprising. However, at low voltages, whether I_D should be close to drift-diffusion current or ballistic current is not immediately apparent. This behavior merits further verification using device level simulation, e.g., Monte-Carlo simulations.

4.6 Summary & discussion

In this chapter we have proposed a macro-model approach to model the MOSFET in a continuous manner between the purely ballistic and the drift-diffusion regimes. This macro-model can use existing ballistic and diffusive device models while filling in the gap between the two. We outlined the behavior expected from a model that can be used to model a MOSFET at all possible channel lengths, ranging from several micrometers to a few nanometers. Finally, we showed that the proposed model behaves well in the asymptotic cases. Nonetheless, this model would need to be validated against physics based device simulations.

Admittedly, the model proposed in this chapter is inspired by the work of Mugnaini et al. [59] who proposed to model the diffusive and quasi-ballistic MOSFETs as a drift-diffusion device connected in series with a ballistic one. One major difference between the model proposed in

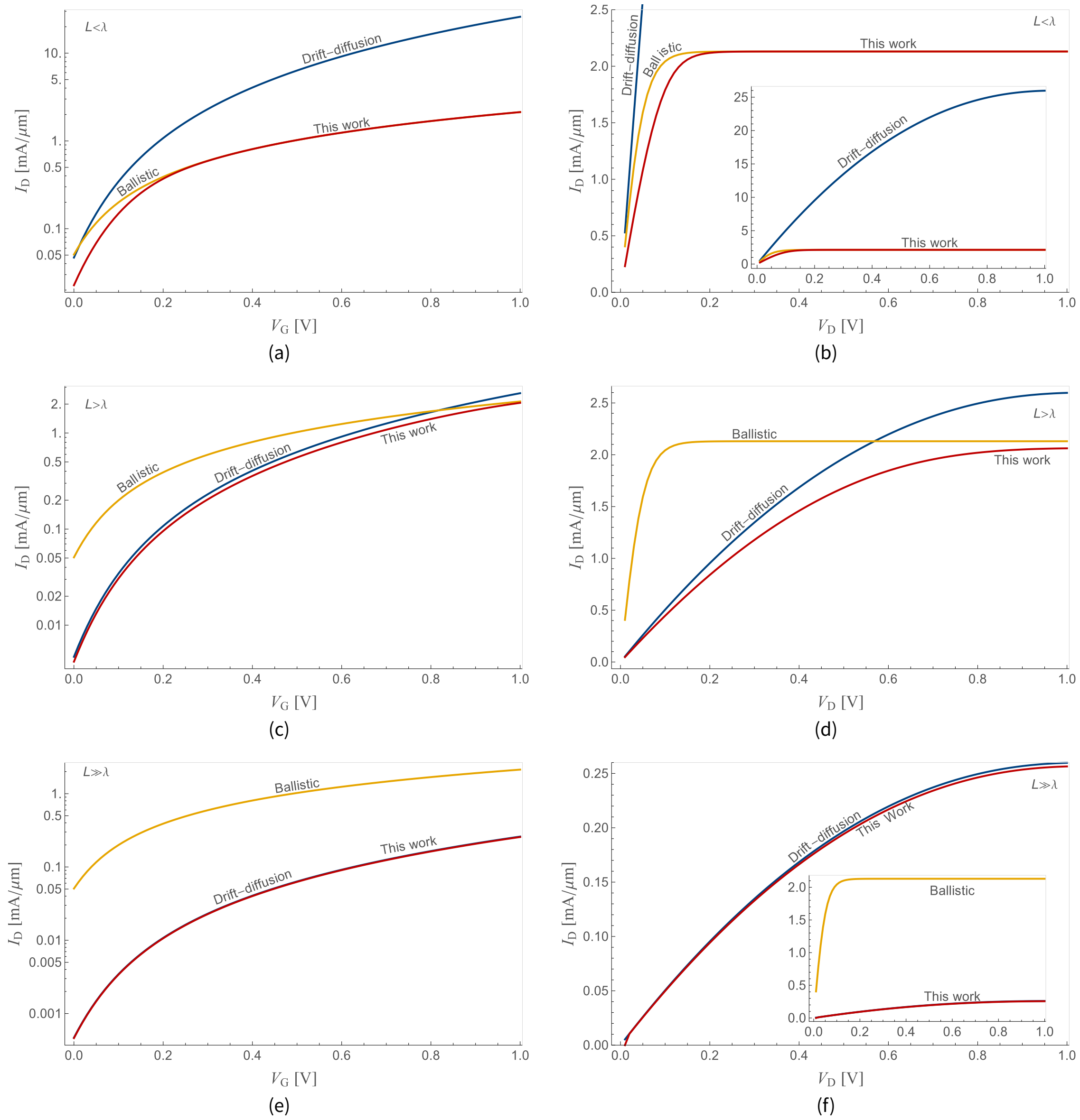


Figure 4.5: I_D-V_G (in log scale) and I_D-V_D characteristics for three different channel lengths obtained using the proposed model. Characteristics for the same device, obtained using EKV drift-diffusion model (without short-channel effects) and Lundstrom's ballistic model, are shown for comparison

this chapter and theirs is that the ballistic device is connected at the source of the drift-diffusion device in the former model, but at the drain in the latter. We believe that our approach is closer to reality since, as discussed in Section 4.1, in any given device, the electrons would always be ballistic before they encounter the first scattering event, whether it is in the channel or in the drain. The ballistic device at the source end in our model serves to capture this part of the channel, whereas, in Mugnaini's approach, the ballistic device at the drain end

serves to capture the velocity saturation effect. With our approach, any existing robust drift-diffusion compact model can be used with the simple Natori model thus avoiding any rejig/reprogramming of the existing CAD framework. At the same time we need to consider the impact of introducing an additional node (discussed in Section 4.4) in the model.

It must be remarked that in developing this model, we assumed that ballistic and diffusive would be governed by the same electrostatic behavior. This was done implicitly by using (4.5) (that gives the inversion charge density in the drift-diffusion model) as expression for inversion charge density in the ballistic model (4.2). Since, electrostatics and transport are coupled in a MOSFET, there is no a-priori reason to believe that the same electrostatics applies in both ballistic and diffusive devices, even though the transport mechanisms are very different. Moreover, while the dc behavior of the model appears correct, the same cannot be said about its dynamic behavior which might be affected by the intermediate node. This provides us with another motivation to seek a model for quasi-ballistic devices that takes into account the electrostatics of the channel, encompassing all the regimes of operation, in such a manner that introduction of additional nodes can be avoided. We will discuss this in the following chapters.

Understanding the electrostatics in ballistic MOSFETS 5

In this chapter, we start by questioning the role that the gate plays in a ballistic MOSFET. We report the results of Monte-Carlo simulations performed on double-gate ballistic MOSFETs with a geometry such that the gates overlap only a fraction of the channel. We present a qualitative analysis of the simulation results highlighting the similarities and differences between ballistic devices of 10 nm and 100 nm channel length, in an attempt to understand the electrostatics in a ballistic channel, especially the influence of the gate, source and drain terminals on the channel.

5.1 Ballistic MOSFET vis-a-vis vacuum tube

BALLISTIC transport in semiconductor devices occurs when the charge carriers emitted from one end (source) are collected at the other end (drain), without being scattered in the channel [40]. This is indeed similar to electron transport in vacuum tubes. In fact, ballistic n^+-n-n^+ semiconductors have even been shown to demonstrate the same I-V characteristics as the Langmuir-Child law [22] for vacuum tubes.

In addition to the scatter-free transport in their respective channels, according to the well-accepted virtual-source model of ballistic transport in MOSFETs, even the current control mechanisms in the vacuum tubes and ballistic MOSFETs is identical. Similar to the description of transport in vacuum tubes [70, 71], the virtual-source model considers the top of the potential barrier that appears in the channel as an effective source of charge carriers (electrons) [45]. This virtual-source appears near the source end of the MOSFET and its height modulates the drain current. According to the model, in a scatter-free channel, the carriers injected from the source with energies higher than the virtual-source barrier pass through to the drain; the rest are reflected back. The carriers collected by the drain constitute the drain-current. While the source and

1. The carriers injected from the drain are suppressed at a drain-source voltage much higher than the thermal voltage.

drain voltages control the number of carriers injected into the channel,[1] the gate voltage controls how many of them pass through the channel by controlling the barrier height.

The model does a good job at explaining the transport and the current control mechanism, but it does not provide a clear explanation of the role that the gate plays throughout the channel. From the above description it appears that the gate plays its role only locally at the virtual-source, like the grid in a vacuum tube.

5.2 The role of the gate

Unlike the grid, the gate physically covers the entire channel of the MOSFET, and should affect the electrostatic potential at every point in the channel. In fact, the electrostatic control exerted by the gate at each point of the channel is imperative in a conventional diffusive MOSFET, where the transport is affected by the local quasi-Fermi potential. On the other hand, it can be argued that since transport in a ballistic device is non-local and the carrier populations are governed by the source and drain Fermi potentials [46] and not the local quasi-Fermi level in the channel, the gate needs not play the same role as in the diffusive device. The carriers which manage to surpass the barrier at the virtual-source would continue their flight unimpeded, exclusively under the influence of the drain-source electric field, and therefore, the influence of the gate should be limited only around the virtual-source. Consequently, we can wonder whether, in a ballistic MOSFET, a gate electrode that physically covers the channel only partially near the source would be sufficient to modulate the conduction in the device. Assuming that this is indeed the case, we do the following 1D analysis in the channel of the MOSFET.

The current continuity equation

$$I_{\mathrm{D}} = qn(x)v(x) \tag{5.1}$$

can be used to obtain the velocity in terms of the current and carrier density,

$$v(x) = \frac{I_{\mathrm{D}}}{qn(x)}, \tag{5.2}$$

where the subscript x is used to imply the value of the corresponding quantity at position x in the channel. In a ballistic device, since there is no scattering, the carriers gain kinetic energy as they travel from the

virtual source ($x = 0$) towards the drain. Therefore, we can write

$$\frac{\partial\left(\frac{1}{2}mv(x)^2\right)}{\partial x} = q\frac{\partial\psi(x)}{\partial x}, \tag{5.3}$$

from which we can obtain the carrier velocity at any point x

$$v(x) = \sqrt{\frac{2q}{m}\left(\psi(x) - \psi(0)\right) + v(0)^2}, \tag{5.4}$$

where we can replace $v(0)$ using current continuity to obtain:

$$v(x) = \sqrt{\frac{2q}{m}\left(\psi(x) - \psi(0)\right) + \left(\frac{I_\mathrm{D}}{qn(0)}\right)^2}. \tag{5.5}$$

Now, using (5.1) and (5.5), the Poisson's equation for the undoped channel

$$\frac{\partial^2\psi(x)}{\partial x^2} = \frac{qn(x)}{\varepsilon_\mathrm{si}} \tag{5.6}$$

can be rewritten as

$$\frac{\partial^2\psi(x)}{\partial x^2} = \frac{qn(0)}{\varepsilon_\mathrm{si}}\left(1 + \frac{2q^3n(0)^2}{mI_\mathrm{D}^2}\left(\psi(x) - \psi(0)\right)\right)^{-1/2}. \tag{5.7}$$

Making the following substitution

$$\phi(x) = 1 + \frac{2q^3n(0)^2}{mI_\mathrm{D}^2}\left(\psi(x) - \psi(0)\right) \tag{5.8}$$

and normalizing x

$$\xi = x\bigg/\sqrt{\frac{\varepsilon_\mathrm{si}\,m\,I_\mathrm{D}^2}{2q^4n(0)^3}}, \tag{5.9}$$

we can rewrite (5.7) as

$$\frac{\partial^2\phi(\xi)}{\partial\xi^2} = \frac{1}{\sqrt{\phi(\xi)}} \tag{5.10}$$

or

$$\frac{\partial\left(\frac{\partial\phi(\xi)}{\partial\xi}\right)^2}{\partial\xi} = \frac{2}{\sqrt{\phi(\xi)}}\frac{\partial\phi(\xi)}{\partial\xi}, \tag{5.11}$$

from which we obtain

$$\frac{\partial\phi(\xi)}{\partial\xi} = \sqrt{4\left(\sqrt{\phi(\xi)} - \sqrt{\phi(0)}\right) + \phi'(0)^2}. \tag{5.12}$$

As we know from the theory of ballistic MOSFETs that the potential peaks at the virtual source, hence at $x = 0$, $\psi'(0) = 0$. Therefore, from (5.8)

$$\phi'(0) = 0, \tag{5.13a}$$

$$\phi(0) = 1, \tag{5.13b}$$

simplifying (5.12) to

$$\frac{\partial\phi(\xi)}{\partial\xi} = 2\sqrt{\sqrt{\phi(\xi)} - 1}. \tag{5.14}$$

On integrating (5.14) between the limits 0 and ξ and using (5.13a), we obtain the following implicit equation:

$$\frac{2}{3}\left(\sqrt{\phi(\xi)} + 2\right)\sqrt{\phi(\xi) - 1} = \xi \tag{5.15}$$

or, equivalently,

$$\frac{2}{3}\sqrt{\phi(\xi)^{3/2} + 3\phi(\xi) - 4} = \xi \tag{5.16}$$

which is plotted in Fig. 5.1.

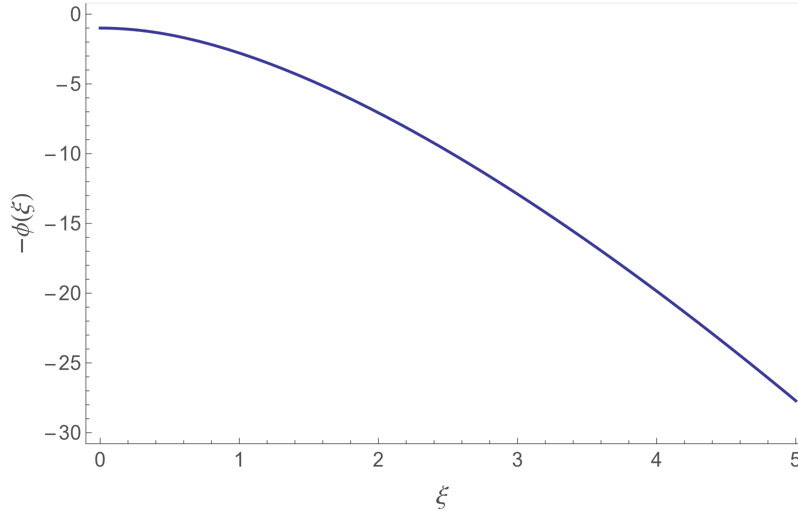


Figure 5.1: Normalized electron potential profile in a ballistic device plotted as a function of normalized distance along the channel calculated using (5.16)

While deriving (5.16) we started off with the 1D Poisson's equation,

thereby completely neglecting the effect of vertical electrical field of the gate. This approach would be immediately called into question, had we been analyzing nanoscale diffusive MOSFETs but, as discussed earlier, it remains unclear whether this is valid for ballistic MOSFETs or not. To understand whether the gate in a ballistic MOSFET behaves like the grid in a vacuum tube, or like the gate of a conventional diffusive MOSFET, we propose a MOSFET geometry such that the metal gate overlaps the channel partially. By exploring the possibility and consequences of using a partial gate that does not affect the electrostatics along the entire channel, we aim to better understand the role of the gate in the ballistic MOSFETs.

5.3 Device templates and monte-carlo simulation

We ran Monte-Carlo simulations on idealized partially gated symmetric double-gate MOSFET whose geometry is shown in Fig. 5.2. This is a DG-MOSFET with a 5 nm thick Si body and 1 nm thick SiO_2 gate oxide. A metal gate with work-function 4.61 eV is used. The source and drain extensions are each 10 nm long and are n-type doped to 1.2×10^{20} cm^{-3}. The channel is considered undoped with a residual doping of 1.2×10^{15} cm^{-3}. Two different channel lengths (L_c =10 nm, 100 nm, and six different gate lengths (L_G/L_c =0.1, 0.3, 0.5, 0.8, 0.9 and 1) were simulated.

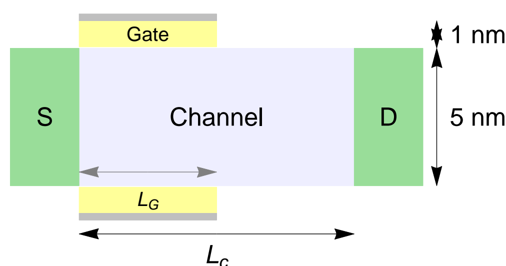


Figure 5.2: Geometry of the partially gated symmetric DG-MOSFET used for the Monte-Carlo simulations. The channel length L_c is the length of the semiconductor between the source and drain junctions. The gate length L_G is the length of the channel covered by the metal gate. This structure was simulated for L_G/L_c =0.1, 0.3, 0.5, 0.8, 0.9 and 1

Multi-Subband Ensemble Monte-Carlo (MSB-EMC) simulations contributed by the Nanoelectronics Research Group at University of Granada, Spain, were used to study the electrostatics and transport.[2] The devices were made artificially ballistic by turning off all the scattering mechanisms in the channel region. The electrons are completely thermalized in the source and drain regions, i.e., they scatter in these regions while

2. The Monte-Carlo simulator is described briefly in Appendix A.

they travel ballistically through the channel. In the semiclassical picture, depending on the respective bias voltages, the electrons can be visualized as being injected from the source and drain terminals. Under the influence of the applied electric field these injected electrons drift scatter-free but can be reflected at any potential barriers that they encounter. The reflected electrons are collected by the injecting terminal whereas the rest of the electrons are collected at the opposite terminal. Several quantities of interest like the electrostatic potential, electron density, average electron velocity etc. can be obtained as a result of these simulations.

5.4 Simulation results

In the following discussion we refer to the channel length L_c as the length of the semiconductor between the source and drain junctions while the gate length L_G is the length of the channel covered by the metal gate and is not necessarily equal to L_c. The x coordinate refers to the direction along the channel from the source to drain; the y coordinate refers to the direction between the gates.

5.4.1 Comparison between different gate lengths

Fig. 5.3 shows the potential and charge profiles at the center of the channel $(y = 0)$ in the 100 nm and 10 nm channels for different partial gate lengths. The potential and charge profiles in the two devices with different channel lengths seem to be markedly different from each other. Even for a given channel length, L_c, devices with different gate length fraction, L_G/L_c, show different profiles; the differences amongst the 100 nm devices being more pronounced than between the 10 nm ones.

To understand the observed behavior let us consider the gated and the non-gated parts of the channel separately. Because of the presence of the gate, the potential in the gated part of the channel is governed by the 2-D Poisson's equation

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = \frac{qn(x,y)}{\varepsilon_{si}}, \tag{5.17}$$

while in the non-gated part only the 1-D Poisson's equation

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} = \frac{qn(x,y)}{\varepsilon_{si}} \tag{5.18}$$

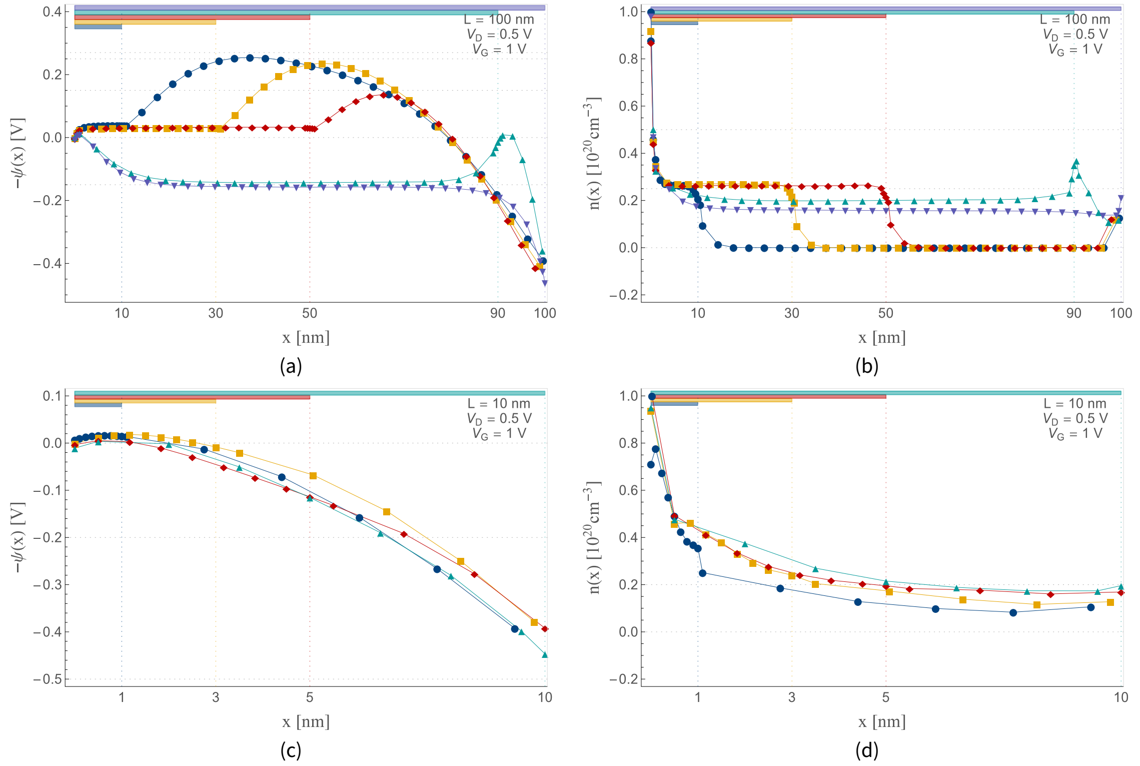


Figure 5.3: The potential and carrier density profile at the center of the channel ($y = 0$) obtained through Monte-Carlo simulations of 100 nm and 10 nm partially gated devices. The bars on the top show the gate length corresponding to the plot of the same color

applies. The term $n(x, y)$ primarily includes charge contributions from the mobile charge which is injected from the source because the channel is practically undoped.

Similar to the vacuum tubes, where the space-charge results in the potential profiles observed in the tube (especially the potential barrier near the cathode) [70], the potential profiles observed in the MOSFETs considered here are caused by the space-charge that is injected from the source.[3]

3. It must be borne in mind that the potential, $\psi(x, y)$, and the charge density, $n(x, y)$, at any point in the channel, result from a self-consistent solution of electrostatic (Poisson-Schrödinger) equations and the transport equations. We use cause-effect arguments to aid explanation.

Now, in Fig. 5.3 we observe that the carrier density $n(x, y)$ is uniform along the non-gated region i.e., $n(x, y) = n$, so, the solution to (5.18) is of the form

$$\psi(x) = \frac{qn}{2\varepsilon_{\text{si}}} x^2 + c_1 x + c_2, \tag{5.19}$$

where c_1 and c_2 are constants determined by the boundary conditions. Evidently, the electrostatic potential in the non-gated part takes a parabolic shape. The height of the peak of the potential is proportional

to the length of this region. Therefore, a longer non-gated region (small L_G) implies a larger parabolic potential barrier for the electrons, as can be confirmed in Fig. 5.3(a).

In Fig. 5.3(a) we also observe that, for the *long-gate* device with gate length 90 nm, the magnitude of the potential maximum in the non-gated region is small, yet slightly larger than the potential peak at the virtual-source in the gated part. This means that the electrons injected from the source with energies much higher than the top of the virtual-source peak (the first potential barrier) would be able to cross this second barrier, but a small fraction of electrons with energy just near the top of the first barrier would be reflected back at this second one. In contrast, when the gate length is 30 nm (*short-gate*), the second barrier is much higher than the first one. Thus, a significant portion of the electrons would be reflected here with only a small fraction of the electrons (with energies much higher than the top of the second barrier) that would be able to cross over to the drain. Because of these reflected electrons, the electron density in the gated region of the *short-gate* device is higher than in the *long-gate* one, while the density of the injected electrons would be the same in both the cases. This explains the difference in electron densities between the *short-gate* and *long-gate* cases seen in Fig. 5.3(b).

In Figs. 5.3(c) and 5.3(d) we observe that the potential and carrier density profiles at various gate lengths in the 10 nm channel are different as well, though the differences are much less pronounced than for the 100 nm device. Because of the very short length of the non-gated region, the magnitude of the parabolic potential (5.19) does not reach a high value, and it always remains lower than the potential barrier in the gated region, i.e., unlike the 100 nm device there is no second potential barrier in the 10 nm device.

5.4.2 Comparison at different gate voltages

Since we are interested in understanding the role of the gate, naturally, our next curiosity is to observe the effect of the gate voltage at the different partial gate lengths. Fig. 5.4 shows the comparison of potential and carrier density values (at the center of the channel) at two different gate voltages, $V_G = 0.6\,\text{V}$ —●— and $V_G = 1\,\text{V}$ —■—, for the *long-gate* 100 nm and 10 nm. As we would normally expect,[4] at $V_G = 0.6\,\text{V}$ the first potential barrier near the source is significantly higher than that at $V_G = 1\,\text{V}$, resulting in much lower carrier density in the channel in the 100 nm

4. A higher applied voltage on the gate is expected to push the virtual-source potential barrier lower.

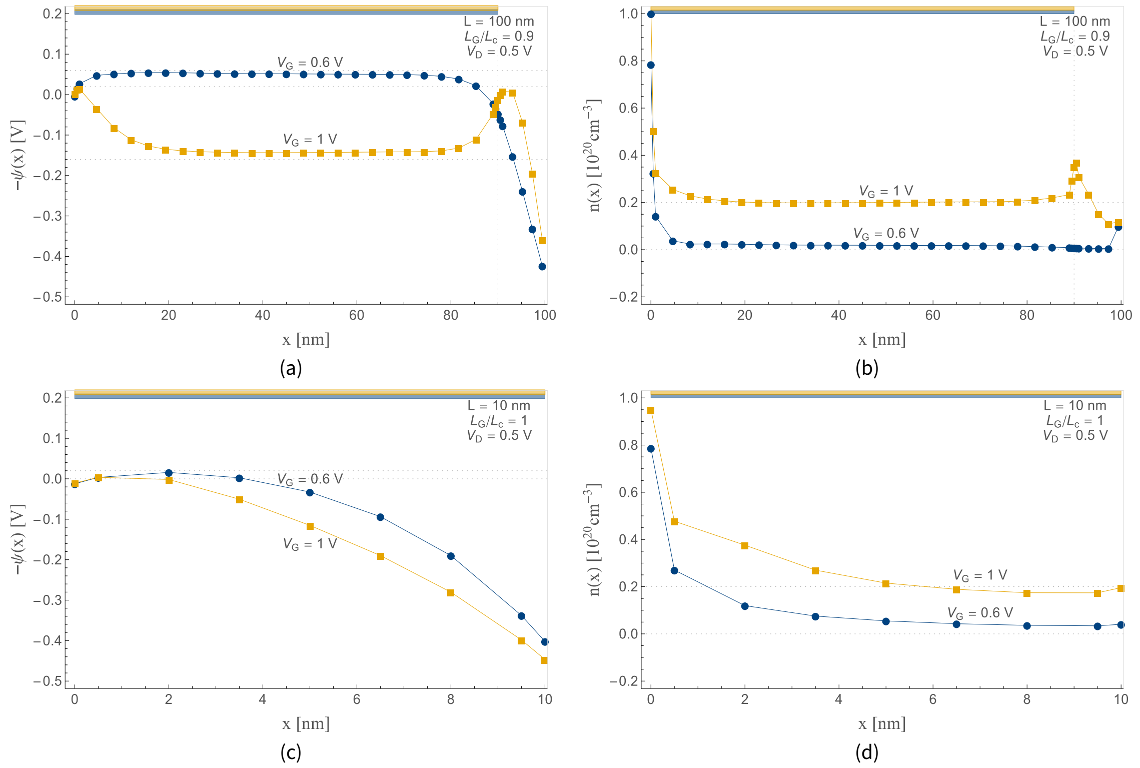


Figure 5.4: Comparison of the (a), (c) potential profiles and (b), (d) carrier density profiles, at the center of the channel, at two different gate voltages in the *long-gate* 100 nm and 10 nm devices

device (Fig. 5.4(a)). A notable difference is the absence of the second potential peak in the *long-gate* device at $V_G = 0.6$V, which can be attributed to the self-consistent solution of the potential and the charge in the gated region which results in a potential value which is higher than that of the peak that would have appeared in the non-gated region. Similarly, for the 10 nm device too, a higher gate voltage causes a lower channel potential and higher carrier density as seen in Fig. 5.4(c).

For the *short-gate* case, shown in Fig. 5.5, we observe something quite interesting. Contrary to expectation, in *short-gate* 10 nm device, $V_G =$ 1V does not manage to push the potential at the virtual-source below its value at $V_G = 0.6$V (see Fig. 5.5(c)). In addition, throughout the rest of the channel the $V_G = 1$V curve —■— is higher than the $V_G = 0.6$V curve —●—. The fact that such a behavior is not observed for the 100 nm device in Fig. 5.5(a) indicates that due to the short channel and the short gate length, the drain exerts a strong influence on the channel electrostatics in the 10 nm device, and that control of the gate is diminished. This can be confirmed by looking again at the potential profile in Fig. 5.5(c), where we remark that the potential profiles in the ungated part of the

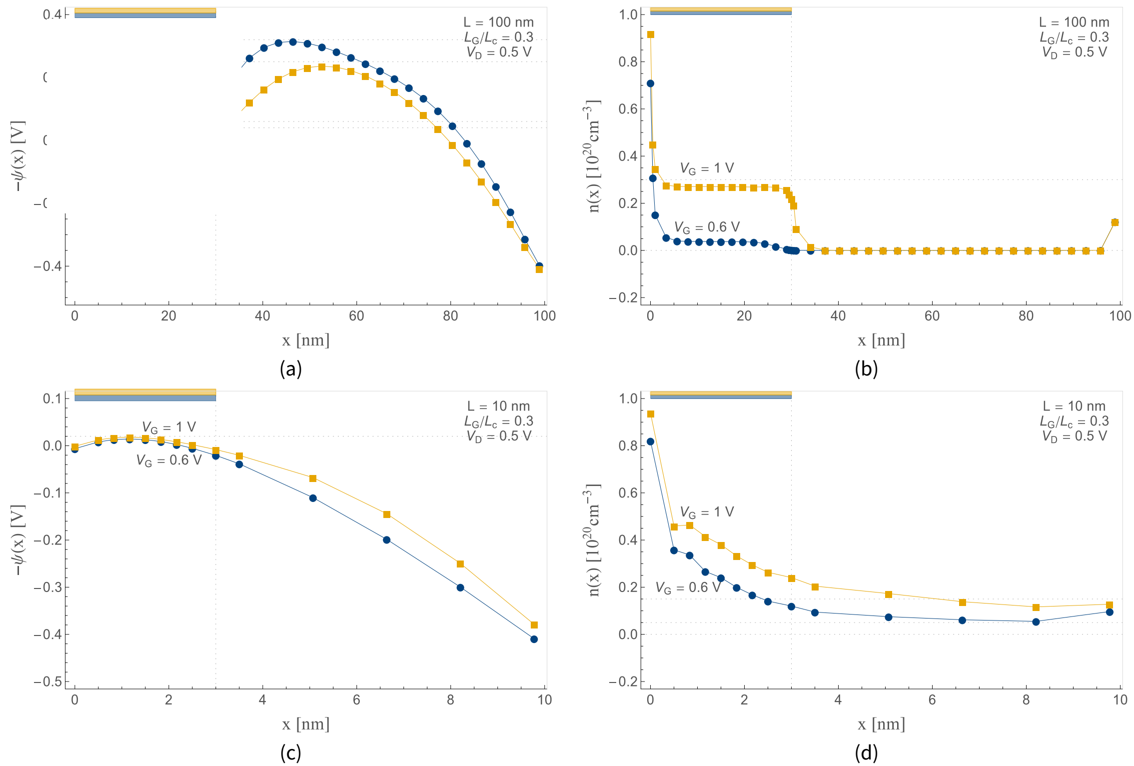
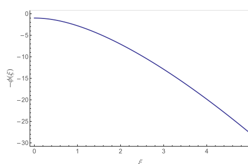


Figure 5.5: Comparison of the (a), (c) potential profiles and (b), (d) carrier density profiles, at the center of the channel, at two different gate voltages in the *short-gate* 100 nm and 10 nm devices

5. $\psi(x) = \frac{qn}{2\varepsilon_{si}}x^2 + c_1 x + c_2$

channel are more linear than parabolic. This implies that in (5.19)[5] the term $c_1 x$ is dominant over the $\frac{qn}{2\varepsilon_{si}}x^2$ term (where the constant c_1 depends on the the drain and source voltages), indicating a stronger influence of the drain on the electrostatics in the 10 nm channel. This influence of the drain is more pronounced when the gate voltage is low (e.g. $V_G = 0.6$V) and cannot compete with the drain voltage. On the other hand, in the 100 nm channel, the potential profile in the ungated part is predominantly parabolic even at a low gate voltage implying that the electrostatics is dependent on the channel charge which in-turn, is determined the electrostatics in the gated region controlled by the gate terminal.



At this point, we must recall the discussion from Section 5.2, especially Fig. 5.1 that shows the channel variation of the potential in a ballistic device, calculated analytically assuming the device behaves as a gateless vacuum tube. Comparing Fig. 5.1 with the potential profiles of 100 nm and 10 nm devices shown in this section, we see that the former curve resembles the profiles of the 10 nm device but there is no similarity with the profiles of the 100 nm one. We can then reasonably conclude that

whether a ballistic MOSFET behaves as a vacuum tube or not depends on its channel length (which determines whether the gate or the drain controls the channel), but definitely not simply on the fact that the transport in it is ballistic.

5.4.3 Comparison of drain currents

In Fig. 5.6, we show the I_D-V_G characteristics of the 100 nm and 10 nm devices, each with two different lengths of the partial gate. Given that

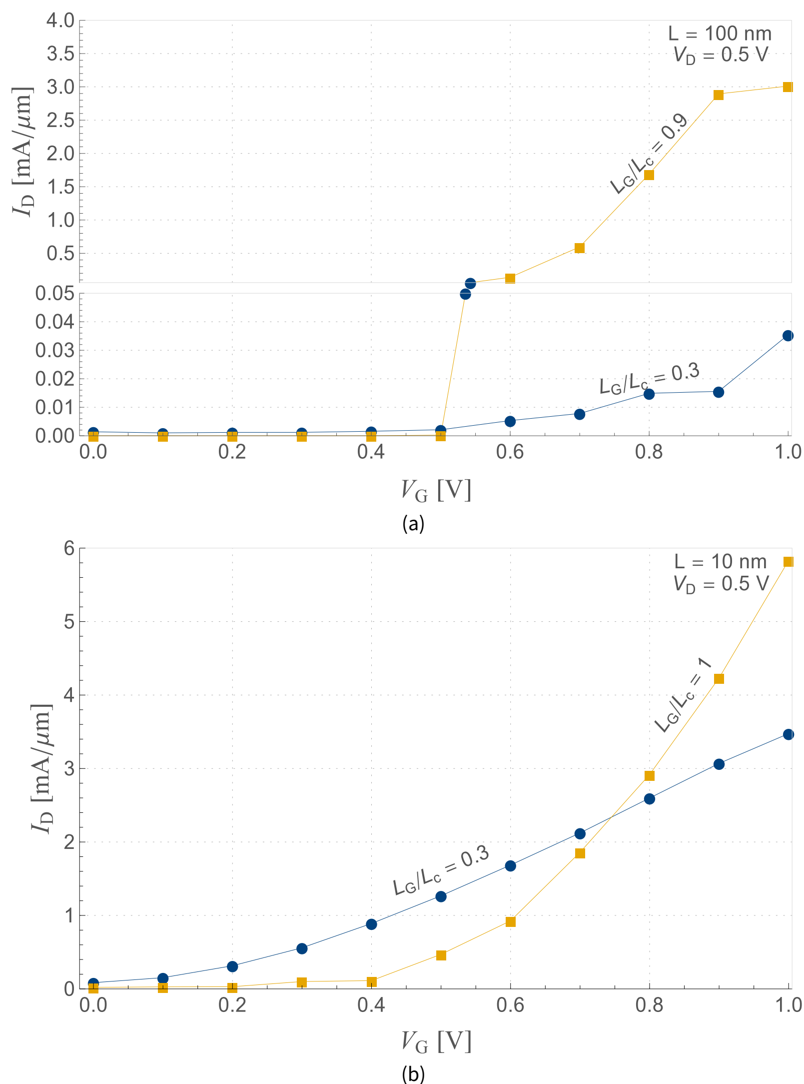


Figure 5.6: $I_D - V_G$ characteristic for two different gate lengths of 100 nm and 10 nm devices. Two different linear scales are used on the I_D axis in (b)

the drain current density, given by (5.1),[6] is directly proportional to the carrier density, and that the carrier density in the 100 nm *long-gate* device is much higher than that in 100 nm *short-gate* (compare

6. $I_D = qn(x)v(x)$

Figs. 5.4(b) and 5.5(b)), the I_D-V_G behavior of the 100 nm in Fig. 5.6(a) is expected: the drain current density for the *long-gate* case is two orders of magnitude higher than that of the *short-gate* case.

The behavior of the 10 nm is very different: firstly, the drain current densities of *long-gate* and *short-gate* cases are similar in magnitude and secondly, the *short-gate* device has a higher current than the *long-gate* one for all gate voltages up to 0.75 V. Although, the similar magnitudes of drain current in the two cases can be explained by comparing the carrier densities in the channel (which are also of similar order of magnitude), the carrier densities do not serve to explain the behavior at low gate voltages. To search for an explanation, we must look at the second term, $v(x)$, in (5.1).

The velocity $v(x)$ of ballistic electrons at a point x ($x > 0$) in the channel is given by

$$v(x) = \sqrt{-\frac{2q}{m}\left(\psi(x) - \psi(0)\right) + v(0)^2}, \tag{5.20}$$

where $x = 0$ is the location of the top of the virtual-source. It is evident that the carrier velocity at any point x depends on the difference of the channel potential at that point to the potential at the virtual source. So, if we compare the channel potentials for the *long-gate* and *short-gate* cases at V_G =0.6 V and 1 V, which we show in Figs. 5.7(a) and 5.7(b) respectively, we can deduce the behavior of the average velocity in the respective cases. In Fig. 5.7(a) we clearly observe that, for $V_G = 0.6$V, the gradient of $-\psi(x)$ for the *short-gate* case is higher than that of the *long-gate* case implying that a higher average carrier velocity for the former. This is indeed what we observe in Fig. 5.7(c). For $V_G = 1$V however, the situation inverses and the gradient of the potential is higher in the *long-gate* device, implying a higher velocity in this case, as can be seen in Fig. 5.7(d). Evidently, this behavior of the $v(x)$ term in (5.1) is the reason that drain current density is higher for the *short-gate* device at low gate voltages, and for the *long-gate* one at high gate voltages.

From the discussion above it might seem that a *short-gate* short-channel device can be advantageously used at low gate voltages since it affords a higher drain current than its *long-gate* counterpart, however, we must note that this device, even though offering a higher current has a much lower gate transconductance (the slope of I_D-V_G curve is less than that of the *long-gate* one).

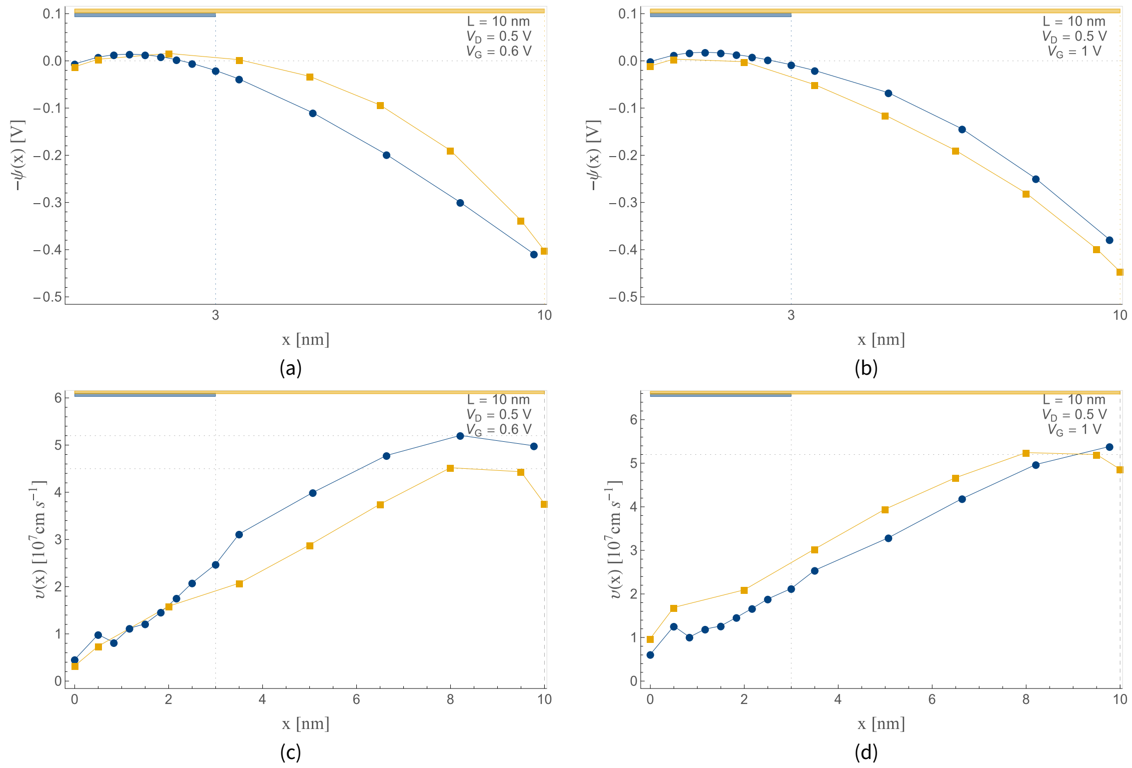


Figure 5.7: Comparison of the channel potential and average electron velocity in the channel of the 10 nm device for the *long-gate* and *short-gate* cases at V_G =0.6 V and 1 V

5.5 Gradual channel approximation in ballistic MOSFETS

A fundamental assumption in most analyses of conventional long channel MOSFETs is the gradual channel approximation (GCA). According to GCA, the vertical electrical field in the channel (exerted by the gate) is much higher than the longitudinal field, implying that the gate exclusively controls the electrostatics in the channel.

By the means of an analytical derivation it has been shown in literature [57] that GCA fails in a ballistic MOSFET. Looking back at our discussion in the preceding sections, we understand that this claim cannot be broadly applied to all ballistic MOSFETs. The potential profiles in the channels of long channel ballistic devices (100 nm) are completely flat throughout most of the channel implying the longitudinal field is much lower (practically 0) than the vertical field and hence GCA is not invalid. In our opinion, the incorrect result that GCA is invalid in ballistic devices [57] originates from a wrong mathematical analysis.

As the first step in their analysis, the authors write the carrier velocity in

the channel (not specifically ballistic) as

$$v(x) = \sqrt{v(0)^2 + b(x)\frac{2q}{m}\big(-\psi(x)\big)} \tag{5.21}$$

with $b(x)\ \big(0 \leq b(x) \leq 1\big)$ being a coefficient that quantifies the fraction of potential energy converted to kinetic energy (i.e., not lost due to scattering). In fact, the energy conservation equation in a more fundamental form would be written as

$$m\,v(x)\frac{\partial v(x)}{\partial x} = b(x)\left(-q\frac{\partial \psi(x)}{\partial x}\right). \tag{5.22}$$

Integrating both sides, we obtain

$$m\int_0^x v(x)\,\partial v(x) = -q\int_0^x b(x)\,\partial\psi(x) \tag{5.23}$$

$$\frac{1}{2}m\big(v(x)^2 - v(0)^2\big) = q\big(b(0)\,\psi(0) - b(x)\,\psi(x)\big) + q\int_0^x \psi(x)\,\partial b(x). \tag{5.24}$$

Comparing (5.21) and (5.24) we see that (5.21) corresponds to the latter if we take $\psi(0) = 0$ and

$$q\int_0^x \psi(x)\,\partial b(x) = 0 \tag{5.25}$$

which holds if

$$\partial b(x) = 0 \tag{5.26}$$

implying

$$b(x) = \text{constant.}$$

The authors claim that with the assumption of GCA, for (5.21) to be physically valid $b(x)$ needs to be a monotonic increasing function of x and since, for a ballistic device $b(x) = 1$, i.e., a constant, GCA does not hold. On the other hand, we have just shown that beginning from a more fundamental starting point (5.22), to obtain (5.21), $b(x)$ needs to be a constant irrespective of GCA.

The error in the authors' analysis lies in writing the energy conservation equation directly as (5.21). In this form, the parameter $b(x)$ quantifies some fraction of the *potential* $\psi(x)$, and not the fraction of *potential energy*, converted to kinetic energy as intended by the authors. To

illustrate this, instead of (5.22) we now write

$$m v(x) \frac{\partial v(x)}{\partial x} = -q \frac{\partial \big(b(x)\, \psi(x)\big)}{\partial x}, \tag{5.27}$$

$$m \int_0^x v(x)\, \partial v(x) = -q \int_0^x \partial \big(b(x)\, \psi(x)\big), \tag{5.28}$$

and obtain

$$\frac{1}{2} m \big(v(x)^2 - v(0)^2\big) = q \big(b(0)\, \psi(0) - b(x)\, \psi(x)\big) \tag{5.29}$$

which is the same as (5.21) (assuming $\psi(0) = 0$).

Therefore, we believe that the claim that GCA is not valid in ballistic MOSFET [57] has been made on the basis of a flawed analytical derivation. The analytical result closer to physics, given by (5.24), does not substantiate this claim. Moreover, the flat potential profiles in the longer channel ballistic devices negate this claim. We believe that the failure of GCA is not a consequence of ballistic transport, rather a consequence of the short channel lengths, irrespective of diffusive or ballistic transport.

5.6 Conclusion

To gain a better understanding of the mutual influence of the electrostatics and transport in ballistic MOSFETs we studied the results of Multi-Subband Monte-Carlo simulations performed on partially gated ballistic double-gate MOSFETs. By the use of partial gate geometries we were able to construct both 1-D and 2-D electrostatic structures in the same device. This enabled us to see the effects of gate and drain terminals on the channel electrostatics in isolation of each other.

We had started by inquiring about the role that the gate plays in influencing the electrostatics, the transport and eventually the drain current in a ballistic MOSFET. From the results of the simulations and the discussion above, we infer that in the ballistic MOSFETs, like in the conventional diffusive MOSFETs, which of the terminals– the gate or the drain– has the dominating control on the channel electrostatics is determined by the channel length. In the 100 nm device, the gate almost exclusively controls the channel electrostatics, whereas in the 10 nm device, the gate gives up the control of the channel electrostatics to the drain, retaining control only near the source (around the *virtual-source*). Although, this seems like a textbook description of short-channel effects, there is no a-priori reason to expect the same in ballistic MOSFETs. As discussed

in Section 5.2, unlike diffusive transport, ballistic transport does not depend on the local quasi-Fermi potential in the channel. Hence, the short-channel effects affecting the local potential could not be expected to influence the transport. As such, the drain current in a ballistic MOSFET is expected to be independent of the channel length [40]. However, through this work, we have shown that it is indeed not the case; the channel length directly affects the electrostatics in the channel which in-turn affects the magnitude of the drain current.

We observed that the gate is indispensable in the long-channel (100 nm) device to suppress the potential barrier created by the channel space-charge, whereas in the short-channel (10 nm) device, a gate long enough to suppress the barrier near the source was adequate because the drain controlled the potential in the rest of the channel. In this respect, the 10 nm device with a partial gate can be considered akin to a vacuum tube with the gate serving as the charge-control, but not the 100 nm one. Therefore, we can conclude that the gate-control only at the virtual-source, and its apparent lack through the rest of the ballistic channel, is not due to the ballistic nature of transport but only due to the short channel length.

6 A simple, scalable model for channel charge and potential in quasi-ballistic nanoscale MOSFETs

In this chapter, we present an analytical semi-empirical model of the profile of the channel charge and potential in quasi-ballistic double-gate MOSFETs. The charge model is based on the premise of separating the charge density in the quasi-ballistic channel into two hypothetical components – one that is exclusively ballistic (collision-free), and the other, a collision-dominated component – but which are governed by the same electrostatics. Using the proposed charge model, and the double-gate MOSFET electrostatics, an analytical expression for the channel potential is derived which, like the charge model, is continuous between the diffusive and ballistic regimes.

6.1 Quasi-ballistic devices

EVEN though it remains unclear whether 100 % ballisticity can be achieved at room temperature in nanoscale silicon devices [58, 72], there is no doubt that such devices are quasi-ballistic, e.g., it has been demonstrated through simulations that even in a 200 nm device, a significant population of charge carriers injected from the source reaches the drain ballistically [73]. Of course, the exact definition of a quasi-ballistic device would imply such a device whose channel length is comparable to the carrier mean free path [25], however, as is common in the literature, we use the term to denote any device in which non negligible ballisticity can be detected, irrespective of the channel length.

The quasi-ballistic devices lie on the continuum between the ballistic and the diffusive devices, and pose their own challenges to compact modeling: neither the ballistic models (which do not account for scattering [40]), nor the conventional drift-diffusion models (which do not take the non-local off-equilibrium nature of ballistic transport into account),

are directly applicable. Evidently, a model for the quasi-ballistic devices would have to account for both collision-free and collision dominated transport thus remaining continuous between the ballistic and diffusive regimes. As discussed in Chapter 3, several models for quasi-ballistic MOSFETs based on different approaches have been proposed in the literature: backscattering coefficient based [46, 67], scattering matrix based [68], chain of ballistic MOSFETs [59, 60] and virtual-source based [56, 57]. These and other models are based on the carrier flux transport over a barrier picture [44, 45], where the source-channel potential barrier plays an important role. However, the shape of the potential in the rest of the channel is generally approximated through parabolic [57, 74] or higher-power polynomial [46] functions. Though these polynomial functions approximate the channel potential profiles in the short-channel quasi-ballistic devices fairly well, they would not be able to model the potential profiles that are rather flat (constant potential) [40, 54], in the longer channel yet predominantly ballistic devices.

In this chapter, we propose a semi-empirical analytical model of the channel charge using which an analytical model for the channel potential is derived.

6.2 Device templates and monte-carlo simulation

As in Chapter 5, the symmetric double-gate (DG) MOSFET structure is used for the analyses and discussion in this chapter. The geometry of an idealized device, shown in Fig. 6.1, consists of 5 nm thick silicon body and 1 nm thick SiO_2 gate oxide. A metal gate with work-function 4.61 eV is used. The source and drain extensions are each 10 nm long and are n-type doped to 1.2×10^{20} cm^{-3}. The channel is considered undoped with a residual doping of 1.2×10^{15} cm^{-3}. Two different channel lengths, 10 nm and 100 nm, are studied to evaluate the effect of channel length on the electrostatic potential profile.

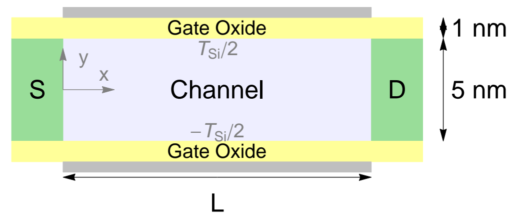


Figure 6.1: Geometry of the symmetric DG-MOSFET used for the Monte-Carlo simulations

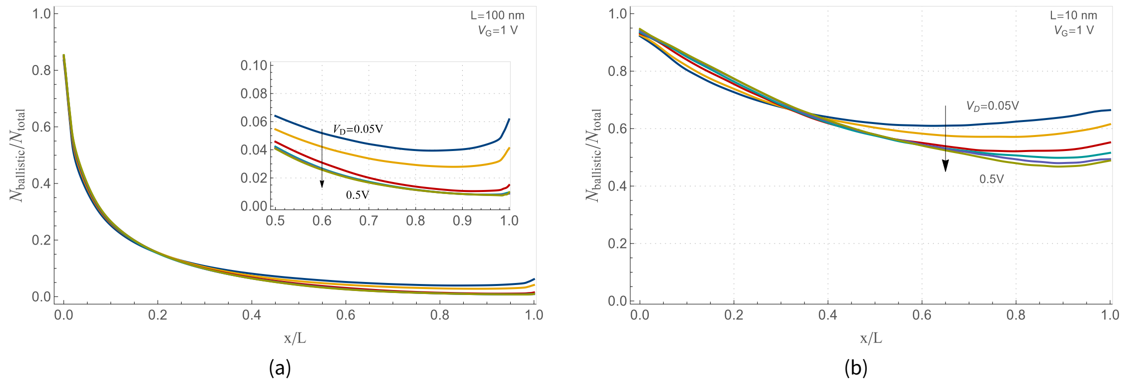


Figure 6.2: Ratio of ballistic carriers to the total number of carriers along the channel in 100 nm and 10 nm devices

The same Multi-Subband Ensemble Monte-Carlo (MSB-EMC) simulation approach as described in Chapter 5 is used here. To compare the effects between diffusive and ballistic scenarios, the 10 nm and 100 nm devices are rendered artificially ballistic by turning off all the scattering mechanisms in the channel but letting the charge carriers (electrons) thermalize completely in the source and drain regions. On application of suitable bias voltages on the source, drain and gate terminals, the electrons are injected from the source into the channel where they undergo consecutive scatter-free random walks before being collected at the drain. The electrons do not scatter with each other or phonons but they can backscatter at a potential barrier.

6.3 The channel charge

The model of the channel charge that we will develop in this section is based on the premise that while traversing the channel in a quasi-ballistic device, a fraction of the carrier population injected from the source would remain ballistic, i.e., it would reach the drain while having encountered exactly zero scattering events. This has been demonstrated for 200 nm devices [73] and for 25 nm devices [47]. Through our own simulations on 10 nm and 100 nm devices, as shown in Fig. 6.2, we observe that the ratio of ballistic carriers to the total number of carriers decreases monotonically from the source to the drain,[1] but it has a non-zero value at the drain end. This implies that even though the number of carriers scattered in the channel increases progressively from the source to the drain, a certain minimum number of carriers travel scatter-free from the source to the drain. This minimum number of ballistic carriers has to be a constant through the channel, being equal to number of ballistic carriers collected at the drain, because any carrier that has encountered even one scattering event cannot be considered ballistic.

1. The slight increase in the number of ballistic carriers at the drain end, seen especially at low values of V_D, is due to the carriers injected from the drain.

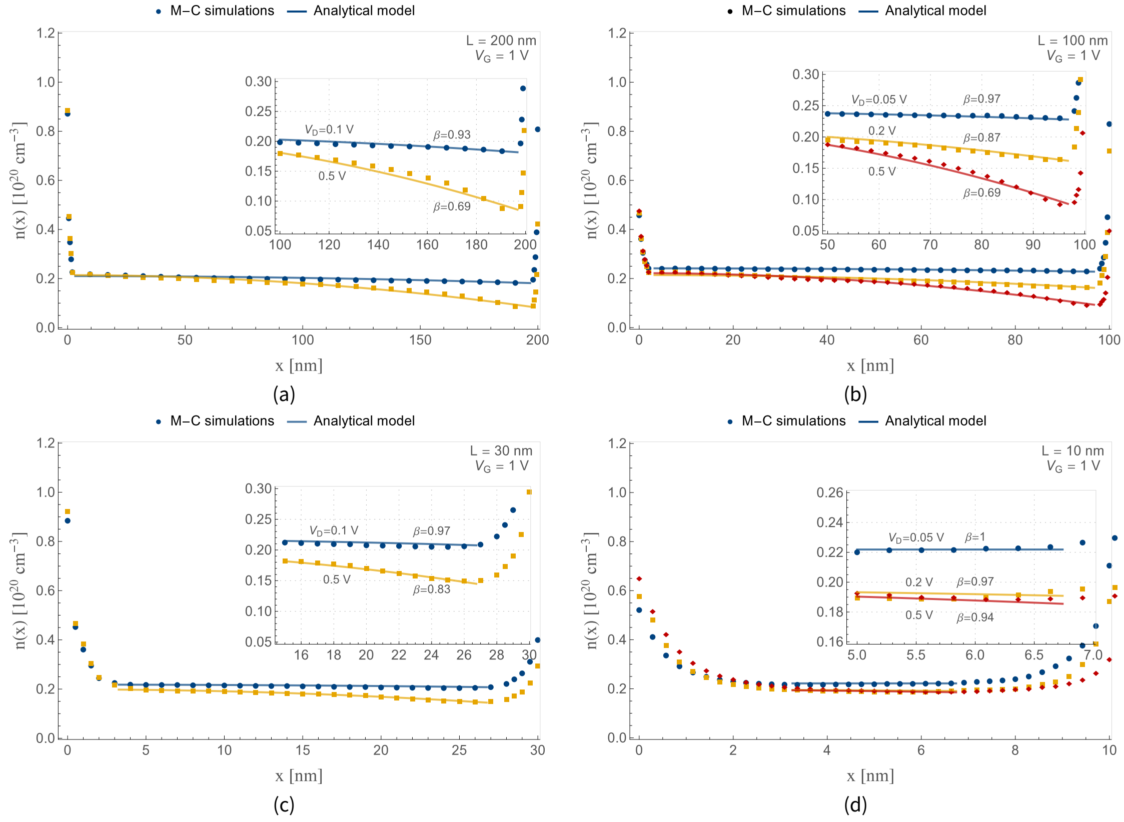


Figure 6.3: Carrier density profile along the center of the channel for 200 nm, 100 nm, 30 nm and 10 nm quasi-ballistic devices

We propose to model the carrier density in the channel $n(x)$ in a similar way, as a sum of two components – an intrinsically ballistic[2] component n_b whose magnitude remains constant throughout the channel and a diffusive component n_d (which includes the carriers which are ballistic at the beginning but scatter later) whose magnitude is position dependent – such that

2. The percentage of carriers which are ballistic at the drain end is called intrinsic ballisticity [75].

$$n(x) = n_\mathrm{b} + n_\mathrm{d}(x). \tag{6.1}$$

In a diffusive device the x dependence of n can be described through the quasi-Fermi potential defined locally at each point in the channel. On the other hand, in the presence of ballistic transport (which is non-local and off-equilibrium [28]), the definition of a local quasi-Fermi level has no meaning[59]. Therefore, we account for the x dependence of $n_\mathrm{d}(x)$ semi-empirically as following:

$$n(x) = n_\mathrm{b} + n_{\mathrm{d}_0}\left(1 - \frac{2\,x^2}{L^2}\right). \tag{6.2}$$

Here, n_{d_0} is the magnitude of the carrier density at the source excluding the density of the carriers which remain ballistic and L is the channel length. We note upfront that (6.2) would not be valid in close proximity of the source and drain extensions where, as can be seen in Fig. 6.3 (especially evident in Figs. 6.3(c) and 6.3(d)), the carrier density varies rapidly between the doping density in the source/drain extensions and the carrier density in the channel. In the vicinity of source/drain, this gradient of carrier density can be modeled using decaying exponential functions, with a decay factor characterized by the Debye length of electrons in the channel, and an expression for carrier density that is continuous from the source/drain into the channel can be obtained. We discuss this further in Section 6.6.

Now, we define a parameter β as

$$\beta = \frac{n_b}{n_b + n_{d_0}}, \tag{6.3}$$

using which, we can rewrite (6.2) as

$$n(x) = \frac{n_b}{\beta}\left(1 - (1-\beta)\frac{2x^2}{L^2}\right) \qquad (0 < \beta \leq 1). \tag{6.4}$$

In a fully ballistic device, $\beta = 1$, therefore, the charge density is

$$n(x) = n_b \qquad \text{(ballistic)}, \tag{6.5}$$

whereas for a diffusive device, $\beta \to 0$ and $n_b \to 0$, therefore from (6.2),

$$n(x) = n_{d_0}\left(1 - \frac{2x^2}{L^2}\right) \quad \text{(diffusive)}. \tag{6.6}$$

Eq. (6.4) can thus describe the carrier density from that in a fully ballistic device to that in a diffusive (quasi-ballistic) device, in a scalable manner, using the parameter β. The validity of (6.5) that predicts the constant carrier density for the ballistic devices can be questioned; like in the diffusive devices, the carriers achieve high velocities very close to the drain and hence, to maintain current continuity, the carrier density should drop. That is why, it is necessary to emphasize that the separation of carrier densities into two components, as done in (6.1), is simply a conceptual formulation and we do not attempt to physically associate the two components to real ballistic and diffusive populations in the device. The degree of accuracy would be a priori expected to be low near the source and drain ends.

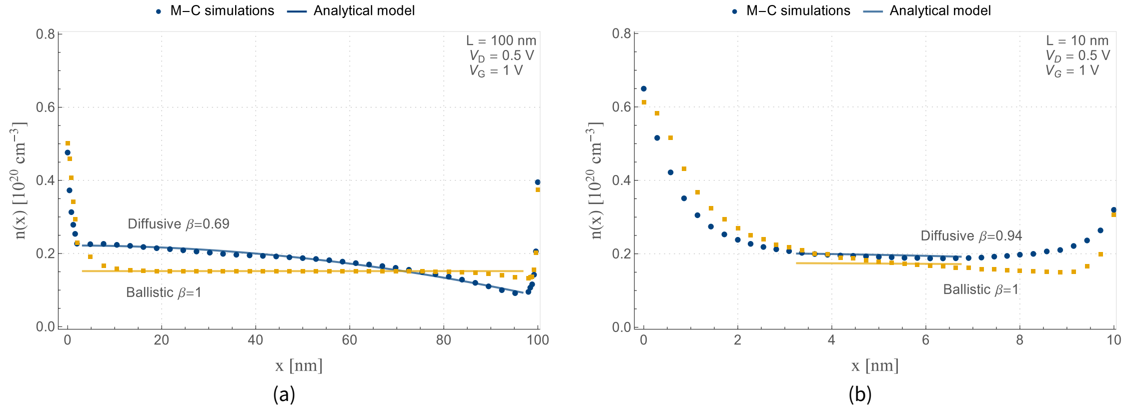


Figure 6.4: Comparison of the carrier density profile along the center of the channel between the ballistic and quasi-ballistic cases in 100 nm and 10 nm devices

To determine n_b, we recall from (6.3) and (6.4) that the carrier density at the source is

$$n(0) = \frac{n_\mathrm{b}}{\beta} = n_\mathrm{b} + n_{\mathrm{d}_0}, \tag{6.7}$$

which constitutes the carriers which remain ballistic throughout the channel (n_b) and the carriers which are ballistic initially but scatter later (n_d). This carrier density at the source can be calculated as a sum of two separate carrier populations, one that is in equilibrium with the source and the other that is in equilibrium with the drain [59]:

$$n^*(0) = 2C_\mathrm{eff}\,U_\mathrm{T}\,\mathscr{W}\left(\frac{1}{2}e^{\frac{\mathrm{V_G-V_S-V_T}}{\mathrm{U_T}}} + \frac{1}{2}e^{\frac{\mathrm{V_G-V_D-V_T}}{\mathrm{U_T}}}\right), \tag{6.8}$$

$n^*(0)$ being the carrier density per unit area at the source. In (6.8) $\mathscr{W}(\cdots)$ is the Lambert-ω function and C_eff, V_T and U_T are the effective gate capacitance, threshold voltage and thermal equivalent voltage (kT/q), respectively. Assuming a uniform carrier distribution between the gates, we can determine n_b for the double-gate ballistic MOSFET as:

$$n_\mathrm{b} = \beta\,n(0) = \beta\,\frac{n^*(0)}{T_\mathrm{si}}. \tag{6.9}$$

In Fig. 6.3, we show the comparison of the analytical model of the carrier density, given by (6.4), with the carrier density obtained from Monte-Carlo simulations (in the center of the channel, i.e., $y = 0$), for four different devices with channel lengths 200 nm, 100 nm, 30 nm and 10 nm. Using β as a parameter we obtain a good match between the model and the simulations at different values of V_D. The curves of

the analytical model do not extend right upto the source and drain boundaries because (6.4) does not take into account the *charge spillover* from the source and drain which extends several nanometers into the channel. While this spillover region is quite negligible in longer devices, we remark that in the 10 nm one it consumes about two-thirds of the channel. It must be pointed out that in addition to β, a slight adjustment of C_{eff} in (6.8) was required to obtain the fit of model with the simulations at different values of V_{D}, while a constant value of threshold voltage $V_{\text{T}} = 0.65\,\text{V}$ was used. Fig. 6.4 shows the comparison of the carrier density profile along the center of the channel between the ballistic (all scattering mechanisms turned off in the simulations) and quasi-ballistic cases in 100 nm and 10 nm devices. By varying the value of the parameter β, both the quasi-ballistic and ballistic cases can be captured.

6.4 The parameter β

To understand the meaning of β better, we evaluate (6.4) at $x = 0$, resulting in

$$n_{\text{QB}}(0) = \frac{n_{\text{b}}}{\beta} \tag{6.10}$$

for a quasi-ballistic device, and in

$$n_{\text{B}}(0) = n_{\text{b}} \tag{6.11}$$

for a fully ballistic device for which $\beta = 1$. From (6.10) and (6.11) we can interpret β to be a measure of the excess charge at the source end of a quasi-ballistic device, as compared to the amount of charge this same device would have had, had it been fully ballistic. In other words, a quasi-ballistic device would have $1/\beta$ ($0 < \beta \leq 1$) times more charge at the source end than an identical ballistic device, at the same bias conditions.

At a given bias, we would expect a shorter device to be more ballistic than a longer one: β for the shorter device would be greater than that for the longer one.

In addition, ballisticity is dependent on the applied biases [48] as can be seen in Figs. 6.2 and 6.3. It is interesting to note that in Fig. 6.3, we need a higher value of β to fit the carrier density curves at lower V_{ds}, implying higher ballisticity at such bias. This might seem surprising at first, especially considering the results of various studies (e.g., [47, 49])

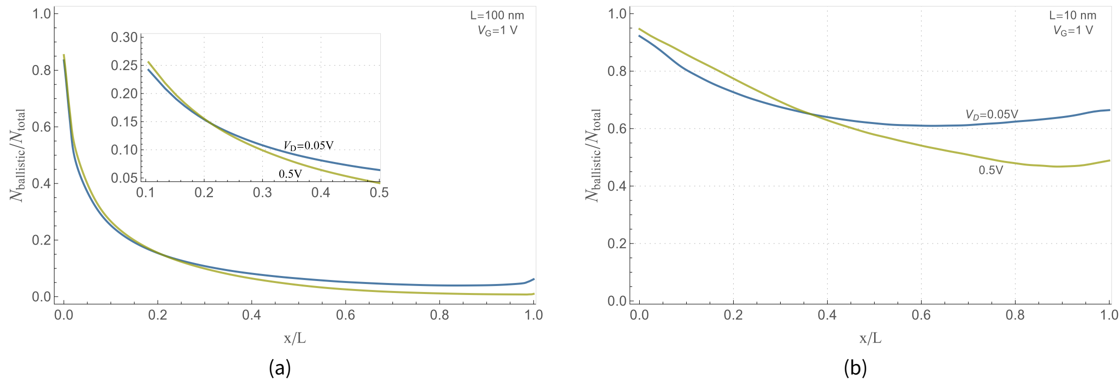


Figure 6.5: Ratio of ballistic carriers to the total number of carriers along the channel in 100 nm and 10 nm devices

which demonstrate that the backscattering probability is higher at lower values of V_{DS}. It is true that at low V_{DS}, the potential barrier for the carriers traveling backwards towards the source is low, and hence, the probability of backscattered carriers returning to the source is high, as is evident in the studies that evaluate the backscattering coefficient at the virtual source. But, beyond the virtual source, deeper into the channel, the scattering probability decreases, precisely because at low V_{DS}, the carriers cannot gain enough energy to emit an optical phonon, optical phonon scattering is suppressed and acoustic phonon scattering is dominant [40]. As discussed by Sano [76], the overall scattering rate is diminished at low electron energies when acoustic phonon scattering is the dominant scattering mechanism.[3] Evidence for this can be seen in Fig. 6.5, (which is a reproduction of Fig. 6.2 and shows the ratio of carriers that have encountered no scattering to the total number of carriers) we make the comparison of the ballisticity at low and high V_{DS}. We observe that near the source, the number of ballistic carriers is higher at high V_{DS}, as we would expect based on the analyses of backscattering coefficient at the virtual source. However, we also observe that the two curves cross over at about $x/L = 0.3$, and the number of ballistic carriers remains higher for low V_{DS}, right upto the drain. Moreover, as shown by other researchers [50], and as seen through our own simulations in Fig. 6.6, at low V_{DS}, the carrier density profile for the diffusive case is very close to the one in which all the scattering is turned off, therefore leading us to believe that carrier density profiles at low V_{DS} appear highly ballistic. Thus, for a given quasi-ballistic device, we would expect higher values of β at low V_{DS} and vice-versa.

3. "if elastic acoustic phonon scattering is the only dominant scattering, the scattering rate approaches to zero as electron energy diminishes."

We have not been able to develop an analytical model to account for the length and bias dependence of β, so, for our purposes we use it as a fitting parameter.

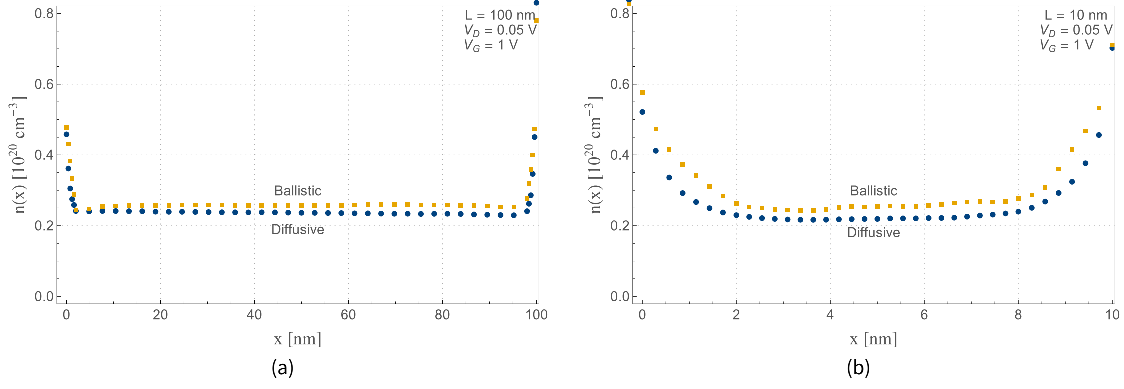


Figure 6.6: Comparison of the carrier density profile along the center of the channel between the ballistic and quasi-ballistic cases in 100 nm and 10 nm devices for small V_{D}

6.5 The channel potential

We start with the Poisson's equation that needs to be solved with appropriate boundary conditions to obtain the potential $\psi(x,y)$:

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{q\,n(x,y)}{\varepsilon_{\mathrm{si}}}, \tag{6.12}$$

where, q and $n(x,y)$ are the electronic charge and the carrier (electron) density, respectively. We assume a general parabolic shape in the y direction (perpendicular to the gates) to eventually simplify the 2-D Poisson's equation to a quasi 1-D equation [77, 78]. Using the boundary conditions –

$$\frac{\partial\psi(y)}{\partial y}=0 \quad \text{at } y=0 \text{ (channel center)}, \tag{6.13a}$$

$$\psi=\psi_{\mathrm{s}}(x) \quad \text{at } y=\pm\frac{T_{\mathrm{si}}}{2} \text{ and} \tag{6.13b}$$

$$\varepsilon_{\mathrm{ox}}\frac{V_{\mathrm{G}}-V_{\mathrm{fb}}-\psi_{\mathrm{s}}(x)}{T_{\mathrm{ox}}}=\varepsilon_{\mathrm{si}}\frac{\partial\psi(y)}{\partial y}\Big|_{\mathrm{y=\pm T_{si}/2}} \tag{6.13c}$$

where $\varepsilon_{\mathrm{si}}$ and $\varepsilon_{\mathrm{ox}}$ are the dielectric constants of silicon and silicon dioxide respectively, V_{G} is the applied gate voltage, V_{fb} is the flat-band voltage, T_{ox} and T_{si} are the respective thicknesses of the oxide and silicon layers, and $\psi_{\mathrm{s}}(x)$ is the surface potential which varies along the channel

depending on the applied voltages – we obtain:

$$\psi(x,y) = -\frac{\varepsilon_{ox}\left(T_{si}^2 - 4y^2\right)\left(V_G^{'} - \psi_s(x)\right)}{4\varepsilon_{si}T_{ox}T_{si}} + \psi_s(x), \tag{6.14}$$

where $V_G^{'} = V_G - V_{fb}$. Evaluating $\psi(x,y)$ at $y = 0$ we obtain the center potential $\psi_c(x)$, using which we can rewrite (6.14) as

$$\psi(x,y) = -\frac{\left(T_{si}^2 - 4y^2\right)\left(V_G^{'} - \psi_c(x)\right)}{8\lambda^2} + \frac{\left(\kappa^2 - 1\right)V_G^{'} + \psi_c(x)}{\kappa^2}, \tag{6.15}$$

where

$$\kappa^2 = 1 + \frac{\varepsilon_{ox}T_{si}}{4\,\varepsilon_{si}T_{ox}} \text{ and} \tag{6.16a}$$

$$\lambda^2 = \frac{\varepsilon_{si}T_{si}T_{ox}}{2\,\varepsilon_{ox}}\kappa^2. \tag{6.16b}$$

Using (6.15) in (6.12) and evaluating at the center of the channel, the Poisson's equation becomes

$$\frac{\partial^2\psi_c(x)}{\partial x^2} + \frac{V_G^{'} - \psi_c(x)}{\lambda^2} = \frac{q\,n(x)}{\varepsilon_{si}}, \tag{6.17}$$

which can be solved with the boundary conditions

$$\psi_c(0) = V_S \tag{6.18a}$$

$$\psi_c(L) = V_D, \tag{6.18b}$$

to obtain the center potential:

$$\begin{aligned}\psi_c(x) = &V_D\,\xi_x + V_S\,\xi_{L-x} + V_G^{'}\left(1 - \xi_x - \xi_{L-x}\right) \\ &- \frac{q\lambda^2}{\varepsilon_{si}}\left(n(x) - n(L)\,\xi_x - n(0)\,\xi_{L-x}\right) \\ &+ \frac{q\lambda^4}{\varepsilon_{si}}\frac{4\,n_b(1-\beta)}{\beta L^2}\left(1 - \xi_x - \xi_{L-x}\right).\end{aligned} \tag{6.19}$$

Here, $n(x)$ is the carrier density as defined by (6.4), and $n(0)$ and $n(L)$ are the values of $n(x)$ evaluated at the source and the drain, respectively,

$$n(0) = \frac{n_\mathrm{b}}{\beta} \tag{6.20a}$$

$$n(L) = \frac{n_\mathrm{b}}{\beta}\left(2\beta - 1\right), \tag{6.20b}$$

and the terms ξ_x and $\xi_\mathrm{L-x}$ are defined as following:

$$\xi_\mathrm{x} = \frac{e^{x/\lambda} - e^{-x/\lambda}}{e^{L/\lambda} - e^{-L/\lambda}} \tag{6.21a}$$

$$\xi_\mathrm{L-x} = \frac{e^{(L-x)/\lambda} - e^{-(L-x)/\lambda}}{e^{L/\lambda} - e^{-L/\lambda}}. \tag{6.21b}$$

In (6.19), the factor λ, called the natural length of the double-gate SOI MOSFET [78] (defined in (6.16)), characterizes the distance over which the source and drain terminals influence the channel. The terms ξ_x and $\xi_\mathrm{L-x}$, and consequently $V_\mathrm{D}\,\xi_\mathrm{x}$ and $V_\mathrm{S}\,\xi_\mathrm{L-x}$ in (6.19), decay rapidly (with the decay factor λ) on moving away from the drain and source respectively. For the device dimensions under consideration in this chapter $\lambda = 3.26\,\mathrm{nm}$, which is negligible in the long channel devices but not in the very short channel (e.g., 10 nm) devices, implying that the channel potential in the short devices would be significantly affected by the drain and source voltages even towards the middle of the channel.

The compact form of (6.19) permits us to see the individual contributions of the applied voltages, V_D, V_S and V_G, to ψ_c more easily. The first, second and third terms are the contributions of the applied drain, source and gate voltages, respectively, weighted by the exponential factors defined in (6.21). The term $n(x)$ depicts a parabolic variation of $\psi_\mathrm{c}(x)$ through (6.4), which could serve as a basis for the parabolic approximations of the channel potential profile generally assumed for the analyses of nanoscale transistors, as discussed in the Introduction. It should be kept in mind that the carrier density terms in (6.7) are themselves dependent on the applied drain, source and gate voltages through (6.8). In Fig. 6.7 we see that the model of (6.19) corresponds well with the simulations on 100 nm and 10 nm devices. Note that (6.19) is expected to be least accurate in the proximity of source/drain extensions because, as mentioned in Section 6.3, the expression for $n(x)$ in (6.4), which is in turn used in deriving (6.19), does not account for the carrier density profile near the source/drain extensions.

In the same way as (6.4) models the carrier density between the quasi-

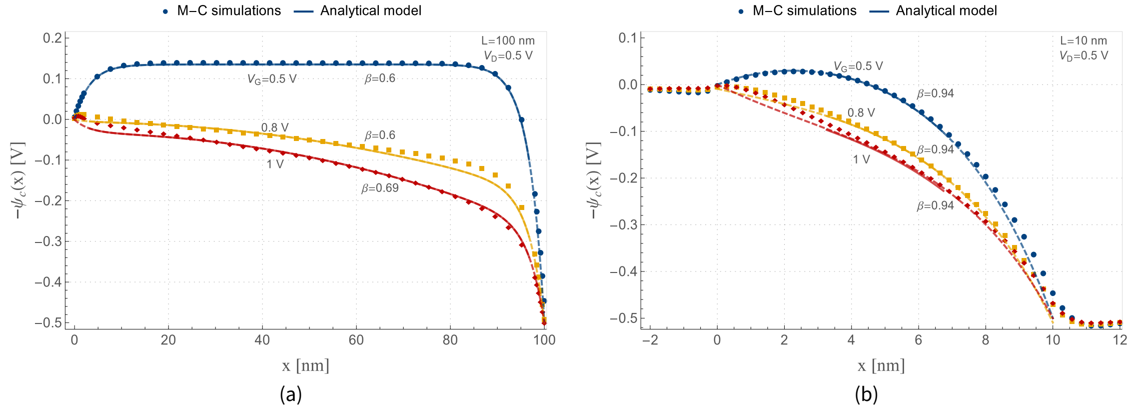


Figure 6.7: Potential profile along the center of the channel in 100 nm and 10 nm quasi-ballistic devices, for different values of applied gate voltage V_G. The dashed lines extend the analytical model beyond the expected range of validity of (6.19)

ballistic and ballistic devices in a continuous manner, (6.19) models the channel potential between the two. It predicts the flat potential profile in the longer channel ballistic devices. In the fully ballistic case for which $\beta = 1$ in (6.19), the last term disappears. Also, the x^2 dependence in $n(x)$ vanishes (according to (6.4)). As discussed above, the ξ_x and ξ_{L-x} terms decay in the channel away from the source and drain proximity. Consequently, $V_D\,\xi_x$ and $V_S\,\xi_{L-x}$ terms are negligible, and $(1-\xi_x-\xi_{L-x}) \approx 1$, a few nanometers away from the drain and source. This leaves only the term $V_G^{'} + (q/\varepsilon_{si})\lambda^2 n_b$, a constant, to shape $\psi_c(x)$ in the middle regions of the channel. On the other hand, the ξ_x and ξ_{L-x} terms are non-negligible even in the middle of the channel of the very short ballistic devices, thereby influencing the shape of $\psi(x)$ which is not flat anymore. The potential profile of the 10 nm fully ballistic device is markedly different from that of the 100 nm device, as can be seen in Fig. 6.8. In Figs. 6.7 and 6.8, the potentials profiles are quite insensitive to the value of β at $V_G = 0.5$V, because for $V_G < V_T$, the potential shape is largely determined by the first three terms in (6.19) that are independent of β.

6.6 The source and drain junctions

The analyses in the previous sections did not consider the source-channel and the drain-channel interfaces. As mentioned in Section 6.3, the carrier density has a gradient from the n^+ source and drain extensions into the undoped channel. We could not find much literature on the analyses of such junctions. The carrier density gradient at the junctions, which spans a length of the order of a 1 nm to 3 nm, is normally neglected in device analyses, probably due to its very short length.

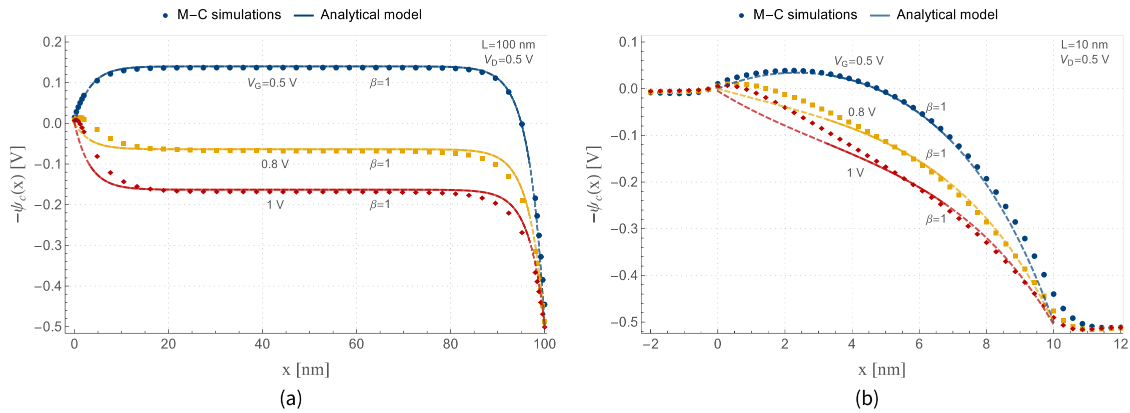


Figure 6.8: Potential profile along the center of the channel in 100 nm and 10 nm fully ballistic devices, for different values of applied gate voltage. The dashed lines extend the analytical model beyond the expected range of validity

As shown in Figs. 6.3 and 6.4, the charge gradient from the source and drain edges can consume as much as two-thirds of the channel, and obviously, this will not be negligible in short-channel devices like the 10 nm one. It should be mentioned here that modeling such a junction in a MOSFET is not trivial due to the following reasons:

1 To obtain a solutions for the carrier density and potential, Poisson's equation will need to be solved self-consistently with the current continuity equation and Boltzmann or Fermi-Dirac statistics and, in the general case, an analytical solution cannot be found.

2 While only 1-D Poisson's equation would apply in the extension regions, the 2-D equation would have to be used in the channel region, further complicating the problem.

3 The gate would exert its influence through a fringing field that would not be negligible because of the small device dimensions.

To circumvent the complications listed above, here we attempt to model the junctions semi-empirically.

In a homo-junction of an undoped semiconductor with a heavily doped contact, the contact region spills electrons into the undoped region [79]. Even in a ballistic device, where the electrons in the channel are not in local equilibrium, due to the scattering dominated source/drain junctions, there will be local equilibrium in the respective *spillover* regions. Using Fick's law, we can define a diffusive current density J that will cause the flux of the electrons from the n^+ region to the undoped

one:

$$J = -D\frac{\partial n(x,t)}{\partial x}, \tag{6.22}$$

so that,

$$\frac{\partial J}{\partial x} = -D\frac{\partial^2 n(x,t)}{\partial x^2}, \tag{6.23}$$

where D is the diffusion constant.

Now, similar to the *relaxation time approximation*, used in the Boltzmann transport equation for the scattering dominated semiconductors, we can approximate that electrons travel at a rate

$$\big(n(x,t) - n_\mathrm{c}\big)/\tau.$$

The implication of this is that at a given position x and given time t, the electrons are traveling at a constant rate $1/\tau$ to try to establish an equilibrated concentration between the highly doped source/drain and the undoped channel. Then, because of carrier conservation and current continuity, we can write

$$\frac{\partial n(x,t)}{\partial t} = -\frac{\partial J}{\partial x} - \frac{n(x,t) - n_\mathrm{c}}{\tau}, \tag{6.24}$$

where n_c is the carrier density inside the channel.[4] In steady state, from (6.23) and (6.24), we have

4. n_c is nothing but the carrier density given by (6.4) at the point where the *charge spillover region* ends.

$$\frac{\partial^2 n(x)}{\partial x^2} = \frac{n(x) - n_\mathrm{c}}{\lambda_\mathrm{d}^2}, \tag{6.25}$$

where

$$\lambda_\mathrm{d} = \sqrt{D\tau} \tag{6.26}$$

is called the diffusion length [80]. Using the boundary conditions,

$$n(0) = n_\mathrm{j}, \tag{6.27a}$$

$$n(\ell) = n_\mathrm{c}, \tag{6.27b}$$

we obtain the solution of (6.25) as

$$n(x) = n_\mathrm{c} + \big(n_\mathrm{j} - n_\mathrm{c}\big)\left(\cosh\left(\frac{x}{\lambda_\mathrm{d}}\right) - \tanh\left(\frac{\ell}{\lambda_\mathrm{d}}\right)\sinh\left(\frac{x}{\lambda_\mathrm{d}}\right)\right), \tag{6.28}$$

where $x = 0$ is at the junction and $x = \ell$ ($\ell > \lambda_d$) is a point deeper into the channel. Since $\tanh(\xi) \to 1$ for $\xi > 2$, (6.28) can be simplified as

$$n(x) \approx n_c + (n_j - n_c)e^{-x/\lambda_d}, \tag{6.29}$$

where n_c is determined using (6.4).[5]

5. Similar exponential form, as in (6.29) has been used to describe the carrier gradients in solar cells [81], thin layer semiconductor junctions semiconductors [80], and metal-semiconductor junctions [82] but, to our knowledge, this has not been done for the nanoscale MOSFETS.

From the carrier density profiles shown in Fig. 6.3, it is clear that the density at the junction is not exactly equal to the doping density N_D. There is a depletion region at the inside edge (in the source/drain extension) of the junction. Assuming that the length of this depletion region is ℓ_{ext}, we can relate n_j to N_D as

$$n_j = N_D e^{-\ell_{ext}/\lambda_d}. \tag{6.30}$$

Alternatively, n_j can be related to N_D using Boltzmann statistics

$$n_j = N_D e^{-\Delta\phi/U_T}, \tag{6.31}$$

where $\Delta\phi$ is the potential drop between the boundary of the source/drain extension (where the density is exactly N_D) and the channel junction. We use (6.31) for plotting the results shown in Fig. 6.9. In addition, we treat the diffusion length λ_d as a fitting parameter for our purposes, while being aware that its value should not be more than the natural length λ discussed earlier. The carrier density at the drain end is also obtained using (6.29) but replacing x by $L - x$ and evaluating n_c near the drain end. In fact, now we can write the complete model for the carrier density that is valid from the source to the drain as

$$n(x) = (n_{j_S} - n_{c_S})e^{-x/\lambda_{dS}} + \frac{n_b}{\beta}\left(1 - (1-\beta)\frac{2x^2}{L^2}\right) + (n_{j_D} - n_{c_D})e^{-(L-x)/\lambda_{dD}} \tag{6.32}$$

which is plotted in Fig. 6.10 for 100 nm and 10 nm devices.

On comparison with MC simulations, we observe that at the source end, $\Delta\phi$ and λ_d in (6.29) need to be changed with the applied gate voltage V_G but not with the applied drain voltage V_D, affirming our initial notion that this carrier density gradient is due to the diffusion at the junction and is independent of the transport in the channel.

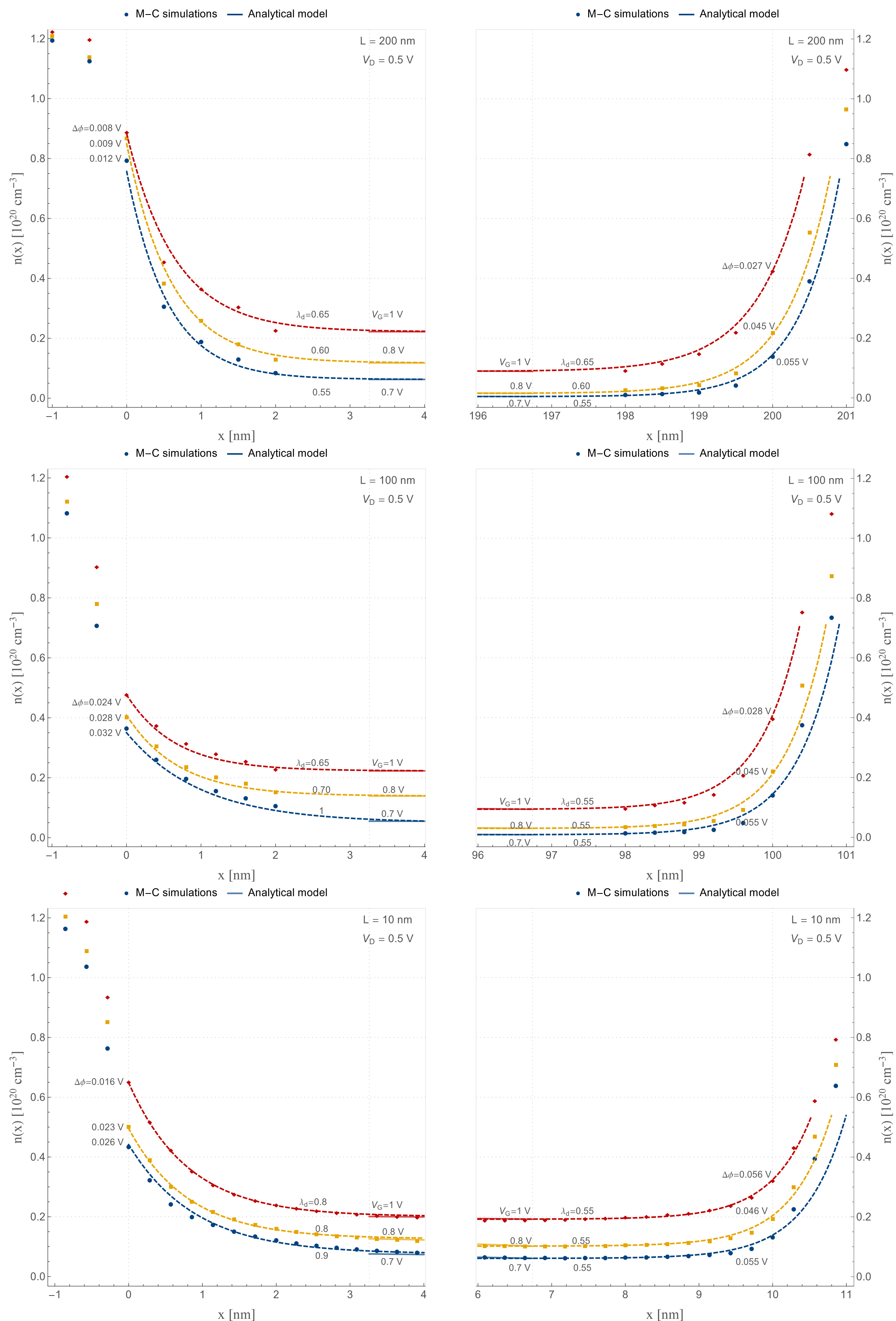


Figure 6.9: Carrier density profiles at the source and drain ends of the 200 nm, 100 nm and 10 nm quasi-ballistic devices. The model of Fig. 6.3 (solid line) is shown for comparison

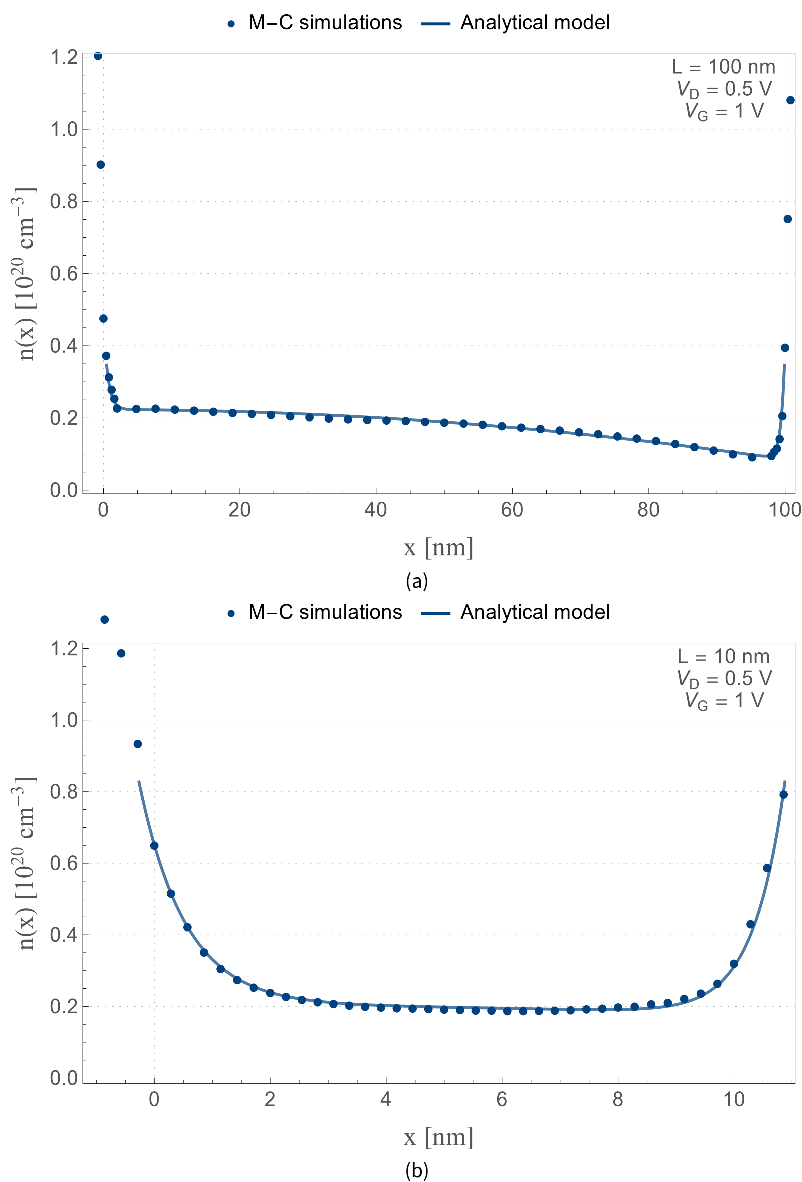


Figure 6.10: Carrier density profiles continuous from the source to the drain in 100 nm and 20 nm quasi-ballistic devices

6.7 Conclusion

In this chapter we presented an analytical description of the channel profile of the carrier density (6.4) and the center potential (6.19) in nanoscale DG MOSFETs. The equations so developed can be scaled between the quasi-ballistic and ballistic cases simply by varying the value of a single parameter (β) between 0 and 1. Admittedly, the carrier density equation is semi-empirical in nature. However, it corresponds well with the results of the Monte-Carlo simulations. We have

been able to model the charge and potential profiles of the ballistic and quasi-ballistic MOSFETs, which are evidently different from each other, in a continuous yet compact manner, while retaining the device physics, which was indeed our goal at the onset. We believe that the conceptual separation of the channel charge into ballistic and diffusive components, represented by (6.1), can be used as the starting point for a complete I-V model for circuit simulation.

† A part of the work in this chapter (Section 6.1 to Section 6.5) appears as a paper in IEEE TED [83].

Conclusion: retrospective & perspective 7

Lundstrom and Antoniadis argue that from a compact-modeling perspective, the development of fully physical models that are seamlessly scalable between the long-channel and nanoscale FETs is an interesting intellectual exercise, but not an essential one [84]. In the same spirit, the main goal of this work was to be able to model the phenomena in the deeply scaled, nanometer size MOS transistors, through simple analytical equations that lend themselves easily to an intuitive understanding of the device behavior.

For an accurate description of the device, a model would need to account for the plethora of physical effects that occur in a nanoscale MOSFET. In this thesis, we have focused our attention on two of the effects: (1) velocity saturation, which is perceivable even in relatively long channel devices and (2) ballistic transport that starts to appear in silicon devices scaled below 30 nm.

It must be remarked that despite the availability of a large body of scientific work, sometimes it is difficult to find direct answers to questions that seem to challenge our understanding. One of our goals during this work has been to ask questions, often fundamental questions, and then try to find answers to those through thought experiments, simulations and mathematical analyses. In the following sections we summarize the major results, unfinished attempts and some possibilities of extending this work.

7.1 Summary of results

7.1.1 Velocity saturation model valid from weak to strong inversion

We extended the EKV model equations to include the velocity saturation effect in a continuous manner between weak inversion and strong inversion. Using this analyses we showed that velocity saturation has a

very small impact on drain current and no impact on the transconductance efficiency $g_{\mathrm{ms}}/i_{\mathrm{d}}$ in weak inversion, whereas in strong inversion, it strongly impacts both. The simple analytical equations thus developed were showed a very good agreement with measurement data of short channel devices fabricated in 40 nm standard CMOS process of ST Microelectronics, as well as with the simulations using the full BSIM6 model. The application of the equations developed for velocity saturation was demonstrated through the design methodology that was eventually applied to design simple analog building-block circuits.

7.1.2 Design methodology for low-power analog & RF circuits

We presented the inversion coefficient *IC* based design methodology, intended to be used for initial design guidance, and highlighted its application for the design of low-power analog and RF circuits. We analyzed a figure-of-merit for RF design and demonstrated that this FoM has a peak at a certain *IC* that can be treated as an optimum value for the MOSFET design since it allows to maximize the gain of a MOSFET operating at a given frequency, while minimizing its noise figure for a given current. It was shown that this optimum *IC* lies in the moderate inversion region, reinforcing the importance of this region for low-power design using downscaled devices from the state-of-the-art processes.

7.1.3 Partial gate ballistic MOSFET to understand the role of the gate

We proposed a geometry of the double-gate ballistic MOSFET in which the gates overlap only a fraction of the channel near the source side. Using such we were able to construct both 1D and 2D electrostatic structures in the same device. Through Monte-Carlo simulations on such devices, we were able to understand the effects of gate and drain terminals on the channel electrostatics in isolation of each other.

The motivation behind this study was to understand the role that the gate plays in influencing the electrostatics, the transport and eventually the drain current in a ballistic MOSFET, an issue that the well established virtual source model does not adequately address. By comparing and contrasting the channel potential and charge profiles in 100 nm and 10 nm ballistic devices, we demonstrated that the gate-control only at the virtual-source, and its apparent lack through the rest of the ballistic channel, is not due to the ballistic nature of transport but only due to the short channel length. We also demonstrated that the parabolic potential profiles similar to those in vacuum tubes, and very often assumed in the

case of ballistic devices, are also a consequence of the drain influence, rather than that of ballistic transport. We also demonstrated that the claim that the gradual channel approximation (GCA) is invalid in ballistic MOSFET is not universally valid. The GCA loses its validity due to small dimensions of the device but not as a consequence of ballistic transport.

7.1.4 Charge & potential model scalable between ballistic and diffusive regimes

To address the inadequacy of the existing models in scaling between the ballistic and diffusive regimes, and especially in assuming parabolic potential profiles, we developed an analytical model of the profile of the channel charge and potential in quasi-ballistic double-gate MOSFETs. The semi-empirical charge model is based on the premise of separating the charge density in the quasi-ballistic channel into two hypothetical components, one that is exclusively ballistic (collision-free), and the other, a collision-dominated component. Using this charge model, we derived an analytical expression for the channel potential, which, like the charge model, is continuous between the diffusive and ballistic regimes. Both the charge and potential equations were shown to have a very good match with Monte-Carlo simulations on ballistic and quasi-ballistic devices of various channel lengths and at different gate and drain voltages.

The profile of the space charge spilled over from the highly doped source and drain extensions into the undoped/lightly doped channel is generally neglected in MOSFET modeling. Realizing that the extant of the space charge in the nanoscale devices is a significant fraction of the channel length, and thus cannot be neglected, we developed an analytical expression to model the profile of the charge near the source and drain ends, as well.

7.1.5 Macro-model approach for I-V model scalable between ballistic and diffusive regimes

We proposed a macro-model approach to model the MOSFET in a continuous manner between the purely ballistic and the drift-diffusion regimes. This model – based on our hypothesis that just after entering into the channel, electrons travel ballistically till they encounter the first scattering event – consists of a ballistic device with channel length equal to the mean free path connected at the source end of a diffusive device. This macro-model can use the existing ballistic and diffusive

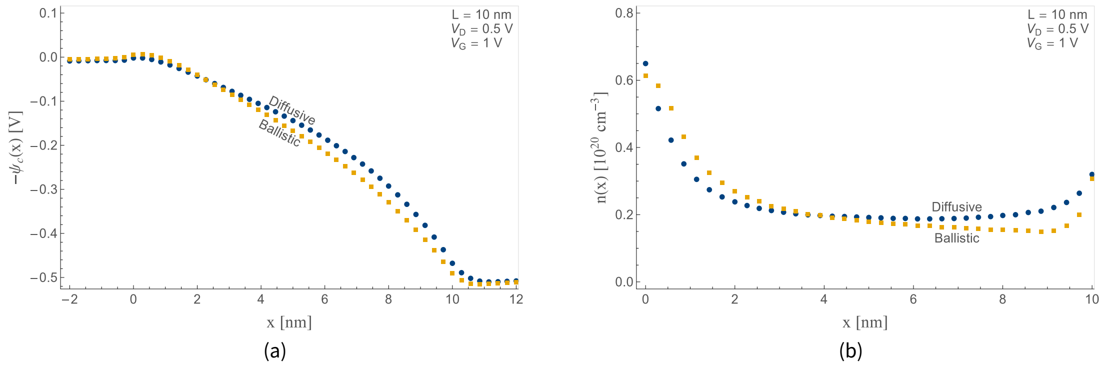


Figure 7.1: Comparison of potential and carrier density profiles in 10 nm double gate MOSFET obtained using Monte-Carlo simulations with scattering on (diffusive) and scattering off (ballistic)

device models while filling in the gap between the two. We showed that the proposed model behaves well in the asymptotic cases.

7.2 Long channel ballistic devices

The wisdom of studying and modeling ballistic transport in long channel double gate MOSFETs, e.g. the 100 nm device studied in this work, can very well be questioned, because such long channel devices cannot ever be expected to be ballistic. We believe that such a study is interesting for the following reasons:

7.2.1 To separate the effect of ballistic transport from short-channel effects

Like in most of the existing literature, we started off by studying the short channel devices. We were surprised by the results of the Monte-Carlo simulations for the 10 nm device, shown in Fig. 7.1, in which we observed very similar potential profiles irrespective of whether there is scattering in the channel or not. Suspecting the short-channel effects to be influencing the behavior, we ran the same simulations but increased the channel length to 100 nm. Since ballistic transport is independent of length while diffusive transport is scatter dominated and hence highly dependent of the length, we expected the potential profile in the 100 nm ballistic device to resemble that of the ballistic 10 nm one and that in the diffusive cases to be quite different. To our surprise, the results, shown in Fig. 7.2 we obtained were contrary to our expectations. The explanation of such profiles in the long channel ballistic has been given in Chapters 5 and 6.

Even though not completely absent, the analysis of long channel bal-

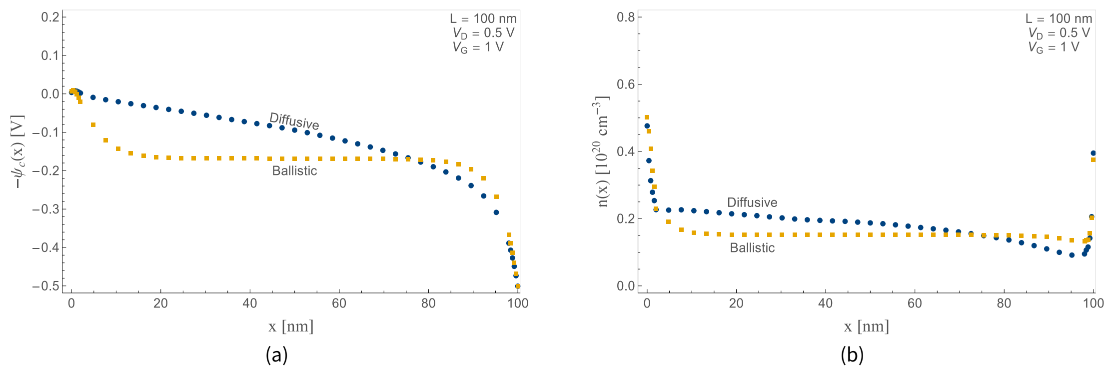


Figure 7.2: Comparison of potential and carrier density profiles in 100 nm double gate MOSFET obtained using Monte-Carlo simulations with scattering on (diffusive) and scattering off (ballistic)

listic MOSFETs is largely neglected in the literature[1] where parabolic potential profiles are assumed as a norm. Through the qualitative discussion of the equation for the center potential (6.19) that we developed in Chapter 6, we showed that in the short channel ballistic devices, the potential profiles are rather strongly influenced by the source and drain voltages. Therefore, in our opinion, Fig. 7.2(b) provides a truer understanding of the nature of a ballistic channel since the picture is not corrupted by short-channel effects. Based on this observation of pretty uniform potential and carrier density profiles in ballistic devices, there seems to be a resemblance with weak inversion in conventional diffusive MOSFETs where the surface potential is uniform as well. This conclusion remains unsubstantiated at the moment and merits further work.

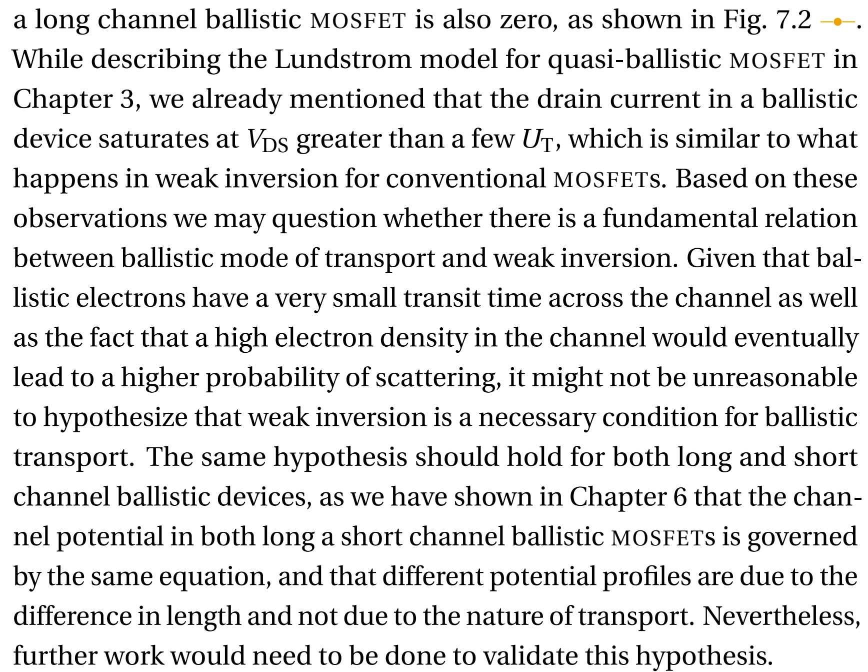
1. Natori mentions briefly about uniform charge and potential profile in long ballistic MOSFETs [40], Svizhenko et al. show a comparison of potential profiles with scattering on and off [54].

7.2.2 Newer materials and devices

There is no doubt that silicon devices with channels as long as 100 nm cannot be expected to be ballistic at room temperatures. Yet, the concepts, ideas and models developed in this work could still be applicable for devices operating at low temperature, devices made with III-V materials [24, 85], graphene [86], carbon nanotubes etc., all of which are expected to be ballistic even at relatively long dimensions.

7.3 Commonalities between conduction in weak inversion, ballistic transport and velocity saturation

The conduction in a conventional long channel MOSFET operating at sub-threshold (weak inversion) is dominated by diffusion, since the gradient of the surface potential in weak inversion is zero [8]. Similarly, the gradient of the center potential (hence surface potential) in



a long channel ballistic MOSFET is also zero, as shown in Fig. 7.2 -•-. While describing the Lundstrom model for quasi-ballistic MOSFET in Chapter 3, we already mentioned that the drain current in a ballistic device saturates at V_{DS} greater than a few U_T, which is similar to what happens in weak inversion for conventional MOSFETs. Based on these observations we may question whether there is a fundamental relation between ballistic mode of transport and weak inversion. Given that ballistic electrons have a very small transit time across the channel as well as the fact that a high electron density in the channel would eventually lead to a higher probability of scattering, it might not be unreasonable to hypothesize that weak inversion is a necessary condition for ballistic transport. The same hypothesis should hold for both long and short channel ballistic devices, as we have shown in Chapter 6 that the channel potential in both long a short channel ballistic MOSFETs is governed by the same equation, and that different potential profiles are due to the difference in length and not due to the nature of transport. Nevertheless, further work would need to be done to validate this hypothesis.

Parallels between velocity saturation and ballistic transport have already been drawn by Mugnaini et al. [59] by showing that modeling a diffusive MOSFET as a chain of ballistic ones, automatically leads to the characteristics similar to velocity saturation operation. The last ballistic device in this chain (towards the drain end) is the one which serves as an equivalent of the velocity saturation region in a diffusive device. This is not entirely surprising as it has been shown by Lundstrom [45] that the electron velocity saturates even in a ballistic MOSFET, albeit near the source end as opposed to the drain end in conventional diffusive ones. We may draw another parallel based on the carrier density profiles for ballistic MOSFETs shown in Figs. 7.1 and 7.2. In these figures, we observe that the carrier density profiles are uniform through the channel, which is also the case in a short channel diffusive MOSFET under velocity saturation [8]. Again, it would be interesting to explore this resemblance in further detail since this may lead to a simpler compact model continuous between diffusive and ballistic regimes.

7.4 A difficult exercise

Electronic conduction in solids is a result of various physical phenomena. The interaction of the carriers with the medium (semiconductor crystal in our case), with impurities and irregularities in the material and with each other, as well as carrier generation and recombination, quantum mechanical effects make the understanding and analyses un-

wieldy. Most of the large body of quantitative and qualitative analyses relies on reasonable assumptions and approximations to simplify the results, at least enough to be of practical use. However, such assumptions and approximations are stretched to their limits with the semiconductor device technology diving deeper and deeper into the nanometer scales, and thus need to be revisited in their context.

A flavor of the difficulty of the exercise of modeling nanoscale MOS devices, which are neither fully ballistic nor fully diffusive, was presented in this thesis. In the quasi-ballistic context, the fundamental assumptions like gradual channel approximation, relaxation time approximation, easily applicable to long channel diffusive devices, cannot be directly applied. Similarly, any simplification brought by absence of scattering is annulled due to the non-equilibrium nature of the transport. Irrespective of the type of transport, the analyses of nanoscale devices is rendered more difficult because of the electrostatics. The Poisson equation must now be solved in 2D and it must be solved self-consistently with the Boltzmann transport equation (which itself is nonlinear integro-differential equation). Not surprisingly, this a difficult exercise [73] and solutions are sought through numerical methods, conformal mapping, Green's function, Monte-Carlo simulations etc. [87].

In addition to analytical formulation presented in this thesis, we also attempted a hybrid numerical solution which we outline here. For the double-gate MOSFET, we start by assuming a parabolic potential profile between the gates such that the 2D Poisson equation (6.12)

$$\frac{\partial^2\psi\left(x,y\right)}{\partial x^2}+\frac{\partial^2\psi\left(x,y\right)}{\partial y^2}=\frac{q\,n(x,y)}{\varepsilon_{\mathrm{si}}}$$

simplifies to a second order 1D equation (6.17):[2]

2. See Chapter 6 for an explanation of the symbols.

$$\frac{\partial^2\psi_{\mathrm{c}}(x)}{\partial x^2}+\frac{V_{\mathrm{G}}^{'}-\psi_{\mathrm{c}}(x)}{\lambda^2}=\frac{q\,n(x)}{\varepsilon_{\mathrm{si}}}. \tag{7.1}$$

Since, in the presence of ballistic transport equilibrium statistics cannot be applied, no functional form for $n(x)$ can be defined a priori. As a workaround, we decided to use the available Monte-Carlo simulation data. Therefore, to discretize (7.1), our step size is now limited by the number of data points available for $n(x)$. We define the step as:

$$\Delta=\frac{L}{N+1}, \tag{7.2}$$

where L is the length of the channel and N is the number of simulation data points for $n(x)$. Using the three point approximation of the second derivative, we can write (7.1) in the finite difference form as

$$\left(2+\frac{\Delta^2}{\lambda^2}\right)\psi_c[i] = \psi_c[i-1] + \psi_c[i+1] + \Delta^2\left(\frac{V_G'}{\lambda^2} - \frac{q\,n[i]}{\varepsilon_{si}}\right), \tag{7.3}$$

with the Drichilet boundary conditions

$$\psi_c[0] = V_S \tag{7.4a}$$

$$\psi_c[1] = V_S. \tag{7.4b}$$

The solution for ψ_c thus obtained was seen to diverge exponentially from source to drain and did not correspond at all to that obtained through Monte-Carlo simulations. We could not explore further the reasons for this behavior and alternative methods, and more work remains to be done here.

7.5 Perspectives

Following up on the research and the work done for this thesis, we would like to address the following areas:

7.5.1 *I-V model of quasi-ballistic devices: parallel & serial approaches*

In this thesis, conspicuous by its absence is the full I-V model that is continuously scalable between the ballistic and diffusive regimes. Our first attempt at such a model was presented in Chapter 4. This approach involves modeling a quasi-ballistic device as a series connection of a ballistic and a drift-diffusion device (shown again Fig. 7.3). The ballistic device has a fixed channel length equal to the mean free path λ while the drift-diffusion device is of variable length L. Depending on whether L is smaller, of the same order, or larger than λ, the model characteristics emulate those of ballistic, quasi-ballistic and drift-diffusion devices, respectively.

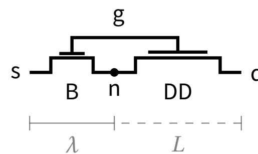


Figure 7.3: Macro-model schematic of a MOSFET with a ballistic section of fixed length λ added at the source side of a conventional diffusive section of variable length L

Another model can be proposed based on the hypothetical separation of the channel charge into ballistic and diffusive components as proposed in Chapter 6 (6.2).[3] Schematically, this is equivalent to splitting the MOSFET channel as a parallel combination of two channels: one that carries only ballistic charge and one that carries the rest of the charge (that scatters). This is shown in Fig. 7.4. By developing appropriate

3. $n(x) = n_\mathrm{b} + n_{\mathrm{d}_0}\left(1 - \frac{2x^2}{L^2}\right)$

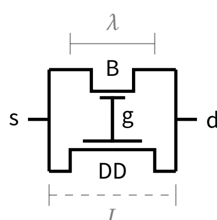


Figure 7.4: Macro-model schematic of a MOSFET with its channel visualized as a parallel combination of a ballistic section of fixed length λ and a conventional diffusive section of variable length L

velocity models for the ballistic and diffusive channels, we would be able to write the drain current as

$$I_\mathrm{D} = q\, n_\mathrm{b} v_\mathrm{b} + q\, n_\mathrm{d} v_\mathrm{d}, \tag{7.5}$$

where v_b and v_d are the average carrier velocities of the ballistic and scattered carriers, respectively.

One of the advantages of the parallel model over the serial one is that it does not introduce any additional intermediate node, which might be a limitation for the dynamic behavior of the latter. Nonetheless, the relative merits of the parallel and serial approaches would be worth analyzing in detail.

7.5.2 *I-V model of quasi-ballistic devices: moments of BTE method*

The drain current equation (7.5) leads to another idea: deriving the current by taking the moments of the Boltzmann transport equation (BTE). The BTE is basically a conservation equation which determines how the distribution of carriers evolve under various internal and external forces, currents and generation-recombination [88]. Consequently, the solution of the BTE is the distribution function of the carriers. The method of moments involves multiplying the distribution function with successive powers of the carrier momentum and integrating over the momentum space [89]. The successive moments equations correspond to particle conservation, energy conservation, momentum conservation etc.[4] The

4. In fact, the drift-diffusion equations are nothing but the first two moments of the BTE under relaxation time approximation.

moments equations constitute a system of infinite equations. Therefore, for practical purposes, to truncate the system after at a finite number, a closure condition is determined using reasonable approximations. This was first proposed by Blotekjaer [37]. Hansch et al. [38] used the same method for hot-electrons by starting with an Ansatz for the distribution function such that the distribution function consists of a sum of two functions: one symmetric term representing diffusive electrons and the other, a term weighted in the direction of the electric field, representing the hot electrons. Chen [90] proposed a similar splitting of the distribution function into ballistic and diffusive components to derive ballistic-diffusive heat conduction equations. In a similar vein, we had attempted to derive ballistic-diffusive equations for charge conduction. Notwithstanding the involved mathematics, we faced a roadblock while determining the appropriate closure condition.

It is interesting to note that the approach we proposed in Chapter 6 is very similar to the approaches of Hansch and Chen, although our approach involves splitting the carrier density and not the distribution function. The drain current equation (7.5) then corresponds to taking the first moments. We believe that this approach merits further work and may lead to an intuitive, simple, yet analytical I-V model.

7.5.3 The vacuum MOSFET

A new semiconductor MOSFET like device with a channel composed of air (and not of a semiconductor) has been proposed recently [91]. The device brings the ballistic transport of the vacuum tubes to the monolithic MOSFET like devices thus promising THz speeds and small sizes. We believe that discussion on partial gate devices in Chapter 5 and especially the analytical development of Section 5.2 would be applicable to this device. Modeling this device could be an interesting work for the future.

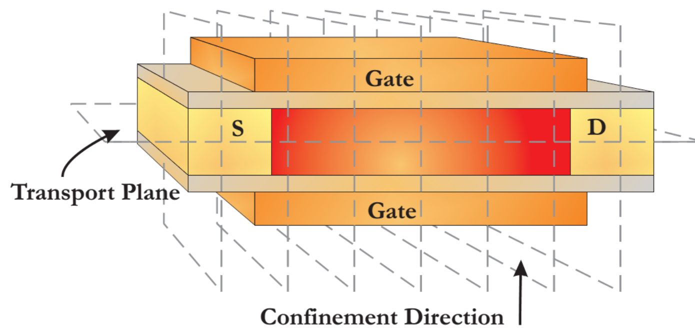
The monte-carlo simulator

A

The Monte-Carlo simulations used in this thesis have been furnished by the Nanoelectronics Research Group of the University of Granada.[1]

1. The text and figure for this appendix has been contributed by Prof. Carlos Sampedro of University of Granada, Spain.

Their Multi-Subband Ensemble Monte Carlo code (MSB-EMC) has been successfully applied for the study of different nanodevices including bulk [92], DGSOI [93] and FDSOI [94]. It is based on the space-mode approach of quantum transport [95], which provides one of the most detailed descriptions of carrier transport including in a natural way the ballistic behavior of ultra-short devices. This approach treats the transport as semiclassical and solves 1D Schrödinger equation for different slabs in the confinement direction. The electrostatics of the



system is obtained from the coupled solution of 2D Poisson and 1D Schrödinger system. In this way, the evolution of the eigen-energies and wavefunctions for the *i-th* valley and the v-*th* subband is obtained along the transport direction. To evaluate the transport properties, the Boltzmann Transport equation (BTE) is solved by the Ensemble Monte Carlo method (EMC) considering a non-parabolic conduction band approximation in both confinement and transport directions [96]. According to the space-mode approach, the driving field undergone by a simulated particle is calculated from subband's gradient corresponding to a different driving force for each the subbands. The subband population needed to obtain the electron density is then obtained from a

re-sampling of the particles weighted by the corresponding distribution function $\left|\xi_{i,v}(x, y)\right|^2$ using the cloud-in-cell method. Finally, the electrostatic potential is updated by solving the 2D Poisson equation using the previous $n(x, y)$ as input. This approach is especially appropriate for the study of 1D confinement in nanoscale devices since the computational impact of the inclusion of quantum effects is partially overcome thanks to the efficient parallel implementation of the code [97]. Concerning scattering models, the simulator includes acoustic and intervalley phonons [96], surface roughness scattering [98] and Coulomb interaction. All the scattering models include non parabolic and ellipsoidal bands and a different scattering rate table is calculated for each slice in order to catch the local particularities of the wavefunctions.

Bibliography

[1] D. M. Binkley, "Tradeoffs and Optimization in Analog CMOS Design," in *Mixed Design of Integrated Circuits and Systems, 2007. MIXDES '07. 14th International Conference on*, Jun. 2007, pp. 47–60. (Cited on pp. 1, 6, and 16)

[2] Y. Tsividis and K. Suyama, "MOSFET modeling for analog circuit CAD: problems and prospects," *Solid-State Circuits, IEEE Journal of*, vol. 29, no. 3, pp. 210–216, Mar. 1994. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=278342 (Cited on pp. 1 and 2)

[3] C. Enz, "An MOS transistor model for RF IC design valid in all regions of operation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 342–359, 2002. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=981286 (Cited on pp. 1 and 10)

[4] E. Vittoz, "Origins of weak inversion (or sub-threshold) circuit design," in *Sub-threshold Design for Ultra Low-Power Systems*, 2006, pp. 1–3. [Online]. Available: http://link.springer.com/content/pdf/10.1007/978-0-387-34501-7_2.pdf (Cited on p. 1)

[5] P. Dautriche, "Analog design trends and challenges in 28 and 20nm CMOS technology," *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, pp. 1–4, 2011. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6044906 (Cited on p. 1)

[6] Y. Tsividis, *Operation and modeling of the MOS transistor*. McGraw-Hill, 1999. (Cited on p. 1)

[7] C. Hu and C. Enz, "Free Standard SPICE Model Supported by University Partners." [Online]. Available: http://www.gsaglobal.org/forum/2012/1/articles_uc_berkeley_epfl.asp (Cited on p. 2)

[8] C. C. Enz and E. A. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV model for low-power and RF IC design.* John Wiley &

Sons, Ltd, 2006. (Cited on pp. 2, 6, 8, 10, 11, 12, 22, 42, 44, 49, 95, and 96)

[9] D. M. Binkley, *Tradeoffs and Optimization in Analog CMOS Design.* Chichester, UK: John Wiley & Sons, Ltd, Jun. 2008. [Online]. Available: http://doi.wiley.com/10.1002/9780470033715 (Cited on pp. 5, 10, and 16)

[10] A.-S. Porret, T. Melly, C. Enz, and E. Vittoz, “A low-power low-voltage transceiver architecture suitable for wireless distributed sensors network,” in *2000 IEEE International Symposium on Circuits and Systems. Emerging Technologies for the 21st Century. Proceedings (IEEE Cat No.00CH36353)*, vol. 1, no. 1. Presses Polytech. Univ. Romandes, 2000, pp. 56–59. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=857025 (Cited on p. 6)

[11] T. Hollis, D. Comer, and D. Comer, “Optimization of MOS amplifier performance through channel length and inversion level selection,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 9, pp. 545–549, 2005. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1510874 (Cited on p. 6)

[12] J. H. Nielsen and E. Bruun, “A CMOS Low-Noise Instrumentation Amplifier Using Chopper Modulation,” *Analog Integrated Circuits and Signal Processing*, vol. 42, no. 1, pp. 65–76, Jan. 2005. [Online]. Available: http://link.springer.com/10.1023/B:ALOG.0000042329.18883.8a (Cited on p. 6)

[13] R. Harrison and C. Charles, “A low-power low-noise CMOS amplifier for neural recording applications,” *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 6, pp. 958–965, 2003. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1201998 (Cited on p. 6)

[14] T. Melly, “Conception d’un émetteur-récepteur à faible consommation intégré en technologie CMOS,” Ph.D. dissertation, EPFL, 2000. (Cited on p. 6)

[15] P. Jespers, *The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches*, ser. Analog Circuits and Signal Processing. Springer, 2009. [Online]. Available: http://books.google.ch/books?id=jdyr_ZYzunAC (Cited on p. 10)

[16] A. Shameli and P. Heydari, “A novel power optimization technique for ultra-low power RFICs,” *International Symposium on Low Power Electronics and Design 2006- ISLPED ’06, Proceedings of the*, vol. 01, no. 2, p. 274, 2006. (Cited on p. 11)

[17] T. Taris, J. Begueret, and Y. Deval, “A 60μW LNA for 2 . 4 GHz Wireless Sensors Network Applications,” in *Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE*, no. V, 2011, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5940633 (Cited on p. 11)

[18] J.-M. Sallese, M. Bucher, F. Krummenacher, and P. Fazan, “Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model,” *Solid-State Electronics*, vol. 47, no. 4, pp. 677–683, 2003. [Online]. Available: http://www.sciencedirect.com/science/article/B6TY5-47DM3S0-B/2/c43a25f26b99264b1de60326247c7d07 (Cited on p. 13)

[19] A. Mangla, M.-A. Chalkiadaki, F. Fadhuile, T. Taris, Y. Deval, and C. Enz, “Design methodology for ultra low-power analog circuits using next generation BSIM6 MOSFET compact model,” *Microelectronics Journal*, vol. 44, no. 7, pp. 570–575, Jul. 2013. [Online]. Available: http://dx.doi.org/10.1016/j.mejo.2013.02.022http://linkinghub.elsevier.com/retrieve/pii/S0026269213000621 (Cited on p. 26)

[20] A. Antonopoulos, M. Bucher, K. Papathanasiou, N. Mavredakis, N. Makris, R. K. Sharma, P. Sakalas, and M. Schroter, “CMOS Small-Signal and Thermal Noise Modeling at High Frequencies,” pp. 3726–3733, 2013. (Cited on p. 29)

[21] A. Antonopoulos, M. Bucher, K. Papathanasiou, N. Makris, N. Mavredakis, R. K. Sharma, P. Sakalas, and M. Schroter, “Modeling of high-frequency noise of silicon CMOS transistors for RFIC design,” *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, pp. n/a–n/a, 2014. [Online]. Available: http://dx.doi.org/10.1002/jnm.1959 (Cited on p. 29)

[22] M. S. Shur and L. F. Eastman, “Ballistic transport in semiconductor at low temperatures for low-power high-speed logic,” *IEEE Transactions on Electron Devices*, vol. 26, no. 11, pp. 1677–1683, Nov. 1979. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1480249http:

//ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1480249 (Cited on pp. 31 and 57)

[23] M. Shur, "Ballistic transport in a semiconductor with collisions," *Electron Devices, IEEE Transactions on*, no. 10, 1981. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1481651 (Cited on p. 31)

[24] M. Heiblum, M. Nathan, D. Thomas, and C. Knoedler, "Direct observation of ballistic transport in GaAs," *Physical review letters*, vol. 55, no. 20, pp. 2200–2203, 1985. [Online]. Available: http://journals.aps.org/prl/abstract/10.1103/PhysRevLett.55.2200 (Cited on pp. 31 and 95)

[25] K. Natori, "Ballistic/quasi-ballistic transport in nanoscale transistor," *Applied Surface Science*, vol. 254, no. 19, pp. 6194–6198, Jul. 2008. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0169433208004698 (Cited on pp. 31, 38, 47, and 73)

[26] R. Clerc and G. Ghibaudo, "Analytical models and electrical characterisation of advanced MOSFETs in the quasi ballistic regime," *International Journal of High Speed Electronics and Systems*, vol. 22, no. 01, Nov. 2013. [Online]. Available: http://www.worldscientific.com/doi/abs/10.1142/S012915641350002X (Cited on p. 31)

[27] K. Hess and G. J. Iafrate, "Theory and applications of near ballistic transport in semiconductors," *Proceedings of the IEEE*, vol. 76, no. 5, pp. 519–532, 1988. (Cited on p. 33)

[28] J.-H. Rhew, Z. Ren, and M. S. Lundstrom, "A numerical study of ballistic transport in a nanoscale MOSFET," *Solid-State Electronics*, vol. 46, no. 11, pp. 1899–1906, Nov. 2002. [Online]. Available: http://www.sciencedirect.com/science/article/B6TY5-45H08GY-2/2/a96dfe5a67a30a2d177991f452914039 (Cited on pp. 33, 37, and 76)

[29] A. C. Smith, J. F. Janak, and R. B. Adler, *Electronic conduction in solids*, ser. McGraw-Hill physical and quantum electronics series. McGraw-Hill, 1967. [Online]. Available: http://books.google.ch/books?id=BRFRAAAAMAAJ (Cited on p. 34)

[30] G. Job and F. Herrmann, "Chemical potential—a quantity in search of recognition," *European Journal of Physics*, vol. 27, no. 2, pp. 353–371, Mar. 2006. [Online]. Available: http://stacks.iop.org/0143-0807/27/i=2/a=018?key=crossref.9bbe444516c72d361f66b3a2b73fd812 (Cited on p. 35)

[31] M. Lundstrom, "6 - The Boltzmann transport equation," in *Fundamentals of Carrier Transport*. Cambridge: Cambridge University Press, 2000, pp. 119–157. [Online]. Available: http://ebooks.cambridge.org/ref/id/CBO9780511618611 (Cited on p. 36)

[32] K. Hess, *Advanced theory of semiconductor devices*. IEEE press, 2000. (Cited on p. 36)

[33] J. Bude, "MOSFET modeling into the ballistic regime," *International Conference on Simulation Semiconductor Processes and Devices*, pp. 23–26, 2000. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=871197 (Cited on p. 37)

[34] M. Vasicek, J. Cervenka, D. Esseni, P. Palestri, and T. Grasser, "Applicability of Macroscopic Transport Models to Decananometer MOSFETs," *IEEE Transactions on Electron Devices*, vol. 59, no. 3, pp. 639–646, Mar. 2012. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6140555 (Cited on p. 37)

[35] T. Grasser and T. Tang, "A review of hydrodynamic and energy-transport models for semiconductor device simulation," *Proceedings of the IEEE*, vol. 91, no. 2, 2003. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1182061 (Cited on p. 37)

[36] B. Meinerzhagen and W. Engl, "The influence of the thermal equilibrium approximation on the accuracy of classical two-dimensional numerical modeling of silicon submicrometer MOS transistors," *Electron Devices, IEEE ...*, vol. 35, no. 5, 1988. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=2514 (Cited on p. 37)

[37] K. Blotekjaer, "Transport equations for electrons in two-valley semiconductors," *IEEE Transactions on Electron Devices*, vol. 17, no. 1, pp. 38–47, Jan. 1970. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=1476105http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1476105 (Cited on pp. 37 and 100)

[38] W. Hänsch and M. Miura-Mattausch, "The hot-electron problem in small semiconductor devices," *Journal of Applied Physics*, vol. 60, no. 2, p. 650, 1986. [Online]. Available: http://link.aip.org/link/JAPIAU/v60/i2/p650/s1&Agg=doi (Cited on pp. 37 and 100)

[39] R. Thoma and A. Emunds, "A generalized hydrodynamic model capable of incorporating Monte Carlo results," *IEDM*, vol. 00, no. 1, pp. 139–142, 1989. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=74246 (Cited on p. 37)

[40] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *Journal of Applied Physics*, vol. 76, no. 8, p. 4879, 1994. [Online]. Available: http://link.aip.org/link/JAPIAU/v76/i8/p4879/s1&Agg=doi (Cited on pp. 38, 40, 45, 49, 57, 72, 73, 74, 80, and 95)

[41] A. Khakifirooz and D. A. Antoniadis, "Transistor Performance Scaling: The Role of Virtual Source Velocity and Its Mobility Dependence," in *2006 International Electron Devices Meeting*. IEEE, Dec. 2006, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4154292 (Cited on p. 38)

[42] J. McKelvey, R. Longini, and T. Brody, "Alternative Approach to the Solution of Added Carrier Transport Problems in Semiconductors," *Physical Review*, vol. 123, no. 1, pp. 51–57, Jul. 1961. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRev.123.51 (Cited on p. 38)

[43] S. Datta, F. Assad, and M. S. Lundstrom, "The silicon MOSFET from a transmission viewpoint," *Superlattices and Microstructures*, vol. 23, no. 3-4, pp. 771–780, Mar. 1998. [Online]. Available: http://www.sciencedirect.com/science/article/B6WXB-45KV8CH-1B/2/38e3156c061273d994fae8e848ba54ad (Cited on p. 39)

[44] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Letters*, vol. 18, no. 7, pp. 361–363, Jul. 1997. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=596937 (Cited on pp. 39, 45, and 74)

[45] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 133–141, 2002. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=974760 (Cited on pp. 39, 41, 47, 57, 74, and 96)

[46] A. Rahman and M. Lundstrom, "A compact scattering model for the nanoscale double-gate MOSFET," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 481–489, Mar. 2002.

[Online]. Available: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=987120http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=987120 (Cited on pp. 39, 40, 41, 49, 58, and 74)

[47] E. Fuchs, P. Dollfus, G. LeCarval, S. Barraud, D. Villanueva, F. Salvetti, H. Jaouen, and T. Skotnicki, "A New Backscattering Model Giving a Description of the Quasi-Ballistic Transport in Nano-MOSFET," *IEEE Transactions on Electron Devices*, vol. 52, no. 10, pp. 2280–2289, Oct. 2005. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1510920 (Cited on pp. 41, 45, 75, and 79)

[48] C. Sampedro, F. Gamiz, A. Godoy, and S. Cristoloveanu, "Ballisticity at very low drain bias in DG SOI Nano-MOSFETs," in *2007 International Semiconductor Device Research Symposium*. IEEE, Dec. 2007, pp. 1–2. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4422322 (Cited on pp. 41 and 79)

[49] R. Kim and M. S. Lundstrom, "Physics of Carrier Backscattering in One- and Two-Dimensional Nanotransistors," *IEEE Transactions on Electron Devices*, vol. 56, no. 1, pp. 132–139, Jan. 2009. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4717241 (Cited on pp. 41 and 79)

[50] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Ballistic ratio and backscattering coefficient in short-channel NW-FETs," in *2009 Proceedings of the European Solid State Device Research Conference*, no. 2. IEEE, Sep. 2009, pp. 476–479. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5331475 (Cited on pp. 41 and 80)

[51] J. J. D. Lee, J. Jeon, J. Kim, B. G. Park, and H. Shin, "Experimental Investigation of Quasi-Ballistic Carrier Transport Characteristics in 10 nm scale MOSFETs," *IEEE Transactions on Nanotechnology*, no. 99, 2010. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5624636 (Cited on p. 41)

[52] F. Berz, "The Bethe condition for thermionic emission near an absorbing boundary," *Solid-State Electronics*, vol. 28, no. 10, pp. 1007–1013, Oct. 1985. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/0038110185900310 (Cited on p. 41)

[53] G. Giusi, G. Iannaccone, and F. Crupi, “A Microscopically Accurate Model of Partially Ballistic NanoMOSFETs in Saturation Based on Channel Backscattering,” *IEEE Transactions on Electron Devices*, vol. 58, no. 3, pp. 691–697, Mar. 2011. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5709977 (Cited on p. 41)

[54] A. Svizhenko and M. Anantram, “Role of scattering in nanotransistors,” *IEEE Transactions on Electron Devices*, vol. 50, no. 6, pp. 1459–1466, Jun. 2003. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1213817 (Cited on pp. 41, 74, and 95)

[55] A. Rahman, Z. Ren, J.-H. Rhew, and M. Lundstrom, “Towards a compact scattering model for nanoscale MOSFETs,” in *2001 International Conference on Modeling and Simulation of Microsystems - MSM 2001*, 2001, pp. 554–557. [Online]. Available: http://www.scopus.com/inward/record.url?eid=2-s2.0-6344257156&partnerID=40&md5=9186e4997ea48ca382773fbbd9d76b10 (Cited on p. 41)

[56] A. Khakifirooz, O. M. Nayfeh, and D. A. Antoniadis, “A Simple Semiempirical Short-Channel MOSFET Current–Voltage Model Continuous Across All Regions of Operation and Employing Only Physical Parameters,” *IEEE Transactions on Electron Devices*, vol. 56, no. 8, pp. 1674–1680, Aug. 2009. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5161294 (Cited on pp. 42 and 74)

[57] L. Wei, O. Mysore, and D. Antoniadis, “Virtual-Source-Based Self-Consistent Current and Charge FET Models: From Ballistic to Drift-Diffusion Velocity-Saturation Operation,” *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1263–1271, May 2012. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6163383 (Cited on pp. 43, 69, 71, and 74)

[58] D. Fleury, G. Bidal, A. Cros, F. Boeuf, T. Skotnicki, and G. Ghibaudo, “New Experimental Insight into Ballisticity of Transport in Strained Bulk MOSFETs,” in *VLSI Technology, 2009 Symposium on*, 2009, pp. 16–17. (Cited on pp. 43 and 73)

[59] G. Mugnaini and G. Iannaccone, “Physics-Based Compact Model of Nanoscale MOSFETs—Part I: Transition From Drift-Diffusion to Ballistic Transport,” *IEEE Transactions on Electron Devices*, vol. 52, no. 8, pp. 1795–1801, Aug. 2005. [Online].

Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1468370 (Cited on pp. 43, 45, 53, 74, 76, 78, and 96)

[60] ——, "Physics-Based Compact Model of Nanoscale MOSFETs—Part II: Effects of Degeneracy on Transport," *IEEE Transactions on Electron Devices*, vol. 52, no. 8, pp. 1802–1806, Aug. 2005. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1468371 (Cited on pp. 43 and 74)

[61] R. M. Corless, G. H. Gonnet, D. E. G. Hare, D. J. Jeffrey, and D. E. Knuth, "On the LambertW function," *Advances in Computational Mathematics*, vol. 5, no. 1, pp. 329–359, Dec. 1996. [Online]. Available: http://link.springer.com/10.1007/BF02124750 (Cited on p. 44)

[62] M. Buttiker, "Role of quantum coherence in series resistors," *Physical Review B*, vol. 33, no. 5, pp. 3020 LP – 3026, Mar. 1986. (Cited on p. 44)

[63] J. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid-State Electronics*, vol. 49, no. 3, pp. 485–489, Mar. 2005. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0038110104003491http://dx.doi.org/10.1016/j.sse.2004.11.013 (Cited on p. 44)

[64] A. Pan and C. O. Chui, "RF performance limits of ballistic Si field-effect transistors," *2014 IEEE 14th Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems*, pp. 68–70, Jan. 2014. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6828529 (Cited on p. 45)

[65] D. Jimenez, J. J. Saenz, B. Iniguez, J. Sune, L. F. Marsal, and J. Pallares, "Unified compact model for the ballistic quantum wire and quantum well metal-oxide-semiconductor field-effect-transistor," *Journal of Applied Physics*, vol. 94, no. 2, p. 1061, 2003. [Online]. Available: http://link.aip.org/link/JAPIAU/v94/i2/p1061/s1&Agg=doi (Cited on p. 45)

[66] G. Curatola, G. Fiori, and G. Iannaccone, "Modelling and simulation challenges for nanoscale MOSFETs in the ballistic limit," *Solid-State Electronics*, vol. 48, no. 4, pp. 581–587, Apr. 2004. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0038110103004052 (Cited on p. 45)

[67] S. Martinie, D. Munteanu, G. Le Carval, and J.-L. Autran, "Physics-Based Analytical Modeling of Quasi-Ballistic Transport in Double-Gate MOSFETs: From Device to Circuit Operation," *IEEE Transactions on Electron Devices*, vol. 56, no. 11, pp. 2692–2702, Nov. 2009. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5280316 (Cited on pp. 45 and 74)

[68] H. Wang and G. Gildenblat, "Scattering matrix based compact MOSFET model," in *International electron devices meeting*, IEEE Elect Devices Soc. 345 E 47TH ST, NEW YORK, NY 10017 USA: IEEE, 2002, Proceedings Paper, pp. 125–128. [Online]. Available: http://pspmodel.asu.edu/downloads/iedm02.pdf (Cited on pp. 45 and 74)

[69] C. Crowell and M. Hafizi, "Current transport over parabolic potential barriers in semiconductor devices," *IEEE Transactions on Electron Devices*, vol. 35, no. 7, pp. 1087–1095, Jul. 1988. [Online]. Available: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=3368 (Cited on p. 47)

[70] I. Langmuir and K. Compton, "Electrical discharges in gases part II. Fundamental phenomena in electrical discharges," *Reviews of modern physics*, 1931. [Online]. Available: http://rmp.aps.org/abstract/RMP/v3/i2/p191_1 (Cited on pp. 57 and 63)

[71] W. H. Aldous and E. V. Appleton, *Thermionic Vacuum Tubes and Their Applications*, ser. Methuen's monographs on physical subjects. London, John Wiley & Sons: New York, 1952. [Online]. Available: http://books.google.ch/books?id=fIPpMgEACAAJ (Cited on p. 57)

[72] M. V. Fischetti, S. Jin, T.-W. Tang, P. Asbeck, Y. Taur, S. E. Laux, M. Rodwell, and N. Sano, "Scaling MOSFETs to 10 nm: Coulomb effects, source starvation, and virtual source model," *Journal of Computational Electronics*, vol. 8, no. 2, pp. 60–77, Jul. 2009. [Online]. Available: http://www.springerlink.com/index/10.1007/s10825-009-0277-z (Cited on p. 73)

[73] D. Csontos and S. E. Ulloa, "Crossover from diffusive to quasi-ballistic transport," *Journal of Applied Physics*, vol. 101, no. 3, p. 033711, 2007. [Online]. Available: http://link.aip.org/link/JAPIAU/v101/i3/p033711/s1&Agg=doi (Cited on pp. 73, 75, and 97)

[74] M.-J. Chen and L.-F. Lu, "A Parabolic Potential Barrier-Oriented Compact Model for the $k_B T$ Layer's Width in Nano-MOSFETs,"

IEEE Transactions on Electron Devices, vol. 55, no. 5, pp. 1265–1268, May 2008. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4475503 (Cited on p. 74)

[75] J. S. Martin, A. Bournel, and P. Dollfus, "On the ballistic transport in nanometer-scaled DG MOSFETs," *IEEE Transactions on Electron Devices*, vol. 51, pp. 1148–1155, 2004. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1308640 (Cited on p. 76)

[76] N. Sano, "Kinetics of Quasiballistic Transport in Nanoscale Semiconductor Structures: Is the Ballistic Limit Attainable at Room Temperature?" *Physical Review Letters*, vol. 93, no. 24, p. 246803, Dec. 2004. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.93.246803 (Cited on p. 80)

[77] R.-H. Yan, A. Ourmazd, and K. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *IEEE Transactions on Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=141237&navigation=1 (Cited on p. 81)

[78] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFET's," *IEEE Transactions on Electron Devices*, vol. 40, no. 12, pp. 2326–2329, 1993. [Online]. Available: http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=249482http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=249482 (Cited on pp. 81 and 83)

[79] K. Hess, "Self-consistent potentials and dielectric properties of semiconductors," in *Advanced Theory of Semiconductor Devices*, pp. 81–88. (Cited on p. 85)

[80] J. Bisquert, "Theory of the impedance of electron diffusion and recombination in a thin layer," *The Journal of Physical Chemistry B*, pp. 325–333, 2002. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/jp011941g (Cited on pp. 86 and 87)

[81] J. P. Gonzalez-Vazquez, J. a. Anta, and J. Bisquert, "Determination of the Electron Diffusion Length in Dye-Sensitized Solar Cells by Random Walk Simulation: Compensation Effects and Voltage Dependence," *The Journal of Physical Chemistry C*, vol. 114, no. 18, pp. 8552–8558, May 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/jp100874e (Cited on p. 87)

[82] C. Black and J. Welser, "Electric-field penetration into metals: consequences for high-dielectric-constant capacitors," *IEEE Transactions on Electron Devices*, vol. 46, no. 4, pp. 776–780, Apr. 1999. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=753713 (Cited on p. 87)

[83] A. Mangla, J. Sallese, C. Sampedro, F. Gamiz, and C. Enz, "Modeling the Channel Charge and Potential in Quasi-Ballistic Nanoscale Double-Gate MOSFETs," *IEEE Transactions on Electron Devices*, no. 99, pp. 1–1, 2014. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6832484 (Cited on p. 90)

[84] M. S. Lundstrom and D. A. Antoniadis, "Compact Models and the Physics of Nanoscale FETs," *IEEE Transactions on Electron Devices*, vol. 1, pp. 1–9, 2013. (Cited on p. 91)

[85] J. a. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors." *Nature*, vol. 479, no. 7373, pp. 317–23, Nov. 2011. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/22094691 (Cited on p. 95)

[86] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene." *Nature nanotechnology*, vol. 3, no. 8, pp. 491–5, Aug. 2008. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/18685637 (Cited on p. 95)

[87] D. Vasileska and S. M. Goodnick, *Computational Electronics*, Jan. 2006, vol. 1, no. 1. [Online]. Available: http://www.morganclaypool.com/doi/abs/10.2200/S00026ED1V01Y200605CEM006 (Cited on p. 97)

[88] M. Lundstrom, "5 - Balance equations," in *Fundamentals of Carrier Transport*. Cambridge: Cambridge University Press, 2000, pp. 212–246. [Online]. Available: http://ebooks.cambridge.org/ref/id/CBO9780511618611 (Cited on p. 99)

[89] K. Hess, "The heterojunction barrier and related transport problems," in *Advanced Theory of Semiconductor Devices*. Wiley-IEEE Press, ch. 10, pp. 147–166. [Online]. Available: http://ieeexplore.ieee.org/servlet/opac?bknumber=5265897 (Cited on p. 99)

[90] G. Chen, "Ballistic-Diffusive Heat-Conduction Equations," *Physical Review Letters*, vol. 86, no. 11, pp. 2297–2300, Mar. 2001.

[Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.86.2297 (Cited on p. 100)

[91] J.-W. Han, J. Sub Oh, and M. Meyyappan, "Vacuum nanoelectronics: Back to the future?—Gate insulated nanoscale vacuum channel transistor," *Applied Physics Letters*, vol. 100, no. 21, p. 213505, 2012. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/100/21/10.1063/1.4717751 (Cited on p. 100)

[92] C. Sampedro, F. Gamiz, A. Godoy, R. Valin, A. Garcia-Loureiro, N. Rodriguez, I. M. Tienda-Luna, F. Martinez-Carricondo, and B. Biel, "Multi-Subband Ensemble Monte Carlo simulation of bulk MOSFETs for the 32 nm-node and beyond," *Solid-State Electronics*, vol. 65-66, pp. 88–93, 2011. (Cited on p. 101)

[93] C. Sampedro, F. Gámiz, A. Godoy, R. Valín, A. García-Loureiro, and F. Ruiz, "Multi-Subband Monte Carlo study of device orientation effects in ultra-short channel DGSOI," *Solid-State Electronics*, vol. 54, no. 2, pp. 131–136, Feb. 2010. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0038110109003505 (Cited on p. 101)

[94] C. Sampedro, F. Gámiz, L. Donetti, and A. Godoy, "Reaching sub-32nm nodes: ET-FDSOI and BOX optimization," *Solid-State Electronics*, vol. 70, pp. 101–105, Apr. 2012. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S0038110111004060 (Cited on p. 101)

[95] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom, and D. Jovanovic, "Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches," *Journal of Applied Physics*, vol. 92, no. 7, p. 3730, Oct. 2002. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/92/7/10.1063/1.1503165 (Cited on p. 101)

[96] M. V. Fischetti and S. E. Laux, "Monte Carlo Study of Electron Transport in Silicon Inversion Layers," *Physical Rev. B*, vol. 48, no. 4, pp. 2244–2274, 1993. (Cited on pp. 101 and 102)

[97] R. Valin, C. Sampedro, N. Seoane, M. Aldegunde, A. Garcia-Loureiro, A. Godoy, and F. Gamiz, "Optimisation and parallelisation of a 2D MOSFET multi-subband ensemble Monte Carlo simulator," *International Journal of High Performance Computing Applications*, vol. 27, no. 4, pp. 483–492, Nov. 2012. [Online]. Available: http://hpc.sagepub.com/cgi/doi/10.1177/1094342012464799 (Cited on p. 102)

[98] F. Gámiz, P. Cartujo-Cassinello, J. B. Roldán, and F. Jiménez-Molinos, “Electron transport in strained Si inversion layers grown on SiGe-on-insulator substrates,” *Journal of Applied Physics*, vol. 92, no. 1, p. 288, 2002. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/92/1/10.1063/1.1481962 (Cited on p. 102)

Anurag Mangla

Education

EPFL PhD in Microsystems & Microelectronics 2014 (expected)

EPFL MS in Microelectronics 2010

GGSIPU BTech in Electronics & Communication 2006

Work History

EPFL Research Assistant 2010–2014

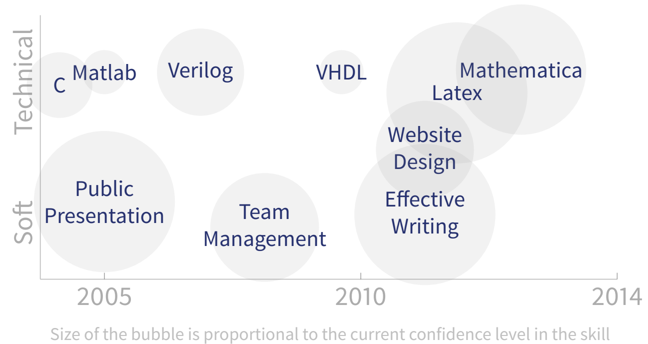
nSys Design Systems Design Engineer 2006–2008

Volunteering

IEEE (Re)founder Chair at EPFL Student Branch 2011–2012

IEEE Founder Chair at BVP Delhi Student Branch 2005–2006

Skills



Size of the bubble is proportional to the current confidence level in the skill

Areas of Interest

Semiconductors Devices | Physics | Modeling | Applications

Circuits Methodologies | Architectures | Models

Digital science Tools & softwares | Data analyses | Document engineering | Presentation of information

New technologies IoT | DIY engineering (Arduino, MSP430)

Accomplishments

EPFL

Starting from scratch, learned about and developed a new model for quasi-ballistic double-gate MOSFETs, including proposing a new partial-gate device structure.

Conducted tutorials and supervised student projects.

nSYS

Worked up my way, within one year, from a being a trainee to leading the company's flagship product (Verification IP solutions for PCIe and PCIe 2.0).

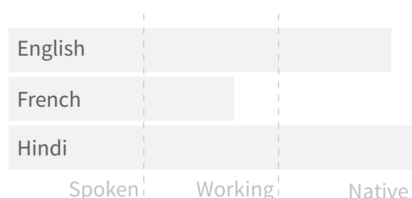
Led the engineering team to win a quarter-million USD project with a prestigious client.

IEEE

BVP Delhi: Identified the absence of, and hence established, an organization to help students advance their engineering careers.

EPFL: Relaunched the dormant student branch, taking a coffee-time idea to execution; won the 'most active IEEE SB in Switzerland.'

Languages



Publications

Modeling the channel charge and potential in quasi-ballistic nanoscale double-gate MOSFETs
IEEE Transactions on Electron Devices, June 2014

Role of the gate in ballistic nanowire SOI MOSFETS
EUROSOI, January 2014

Design methodology for ultra low-power analog circuits using next generation BSIM6 MOSFET compact model
Microelectronics Journal, July 2013

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The future isn’t in solving the problems to which we already know the answers. It’s in learning how to work through the problems you’ll experience in life, in any subject.

Amar Bose, *acoustic technology pioneer*