Graphene Field Effect Devices Operating in Differential Configuration

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After decades of miniaturization and performance tuning, Silicon electronics is approaching its technological limits[1]. In the search for alternative transistor channel materials, Graphene has been given much attention since its discovery in 2004 [2], mainly because it offers compelling values of carrier mobility and a consequent potential for high frequency operation, possibly reaching into the THz range [3]. Certain drawbacks however, such as the weak or absent current saturation or the high "off' current, limit the use of Graphene for traditional CMOS-like circuitry [4]. Here we investigate the possibility of employing an alternative approach based on differential signaling, where saturation and off-current are not expected to preponderate.

We used samples of commercially available, CVD-grown single layer Graphene, transferred onto a Silicon substrate covered by 285nm of SiO_2. Channel regions were defined by removing Graphene in the surrounding areas by an ion-beam etch. Cr/Au Source and Drain (S/D) contacts were evaporated and patterned by EBL and lift-off, followed by Atomic Layer Deposition of a 15nm thick Al_2O_3 gate dielectric. Finally, the gate electrode is patterned and deposited similarly to the S/D electrodes. The gate dielectric, which also covers the S/D metal prevents a short circuit with the gate electrode and allows for tight alignment, reducing the length of un-gated channel regions to a minimum. An example of fabricated device is shown in Fig. 2.

Measurements were taken to assess the transistor's DC characteristic (Fig. 3.). The resulting drain current vs gate voltage (I_D/V_G) curves were analyzed in terms of several key parameters, using the following expressions for fitting: $G_{ds} = \sqrt{g'^2_m (V_G - V_0) + g_0^2}$, where G_{ds} is the transistor's overall conductance between source and drain, $g'_m$is the transconductance per unit of drain-source bias ($g'_m = g_m/V_{ds}$), $V_0$is the Dirac voltage, and g_0 is the conductance minimum ($G_{ds}(V_G = V_0) = g_0$). This intrinsic conductance translates into an extrinsic output current, $I_{extr} = V_{DS} \cdot G_{ds}/(1 + R_S G_{ds})$, when taking the contact resistances into account ($R_S = 2R_C$).

With the same model and the coefficients obtained from a surface fit of a series of I_D/V_G as well as I_D/V_D curves (inset Fig. 3), we programmed a compact model in Verilog-AMS for use with a circuit simulator, in this case CADENCE/Spectre. The circuit of interest is shown in the inset of Figure 4, forming a differential pair of two Graphene field-effect transistors (FETs), connected together at the source with a constant current source, and to one pull-up resistor each at the drain terminal. A differential input signal is applied to the gates around a common offset voltage $V_{G1,2} = V_{com} \pm V_{in}$, whereas the output is taken at the drain terminals as $V_{out} = V_{D1} - V_{D2}$.

The results depicted in Figure 4 show a fairly linear transfer curve in the input voltage range roughly between -1V and +1V, depending on the bias current. No saturation occurs beyond the output peak, instead the differential output drops back down to zero, owing to the ambipolar nature of the transistors. The tradeoff is between input swing and voltage gain (steepness of the transfer curve), which reaches a slightly amplifying value of 1.4.

In conclusion, we obtained a useful circuit model based on measured current-voltage characteristics of actual Graphene devices. This allowed us to estimate the behavior of a circuit comprised of two GFETs and other circuit elements. Such circuit elements could be used as building blocks in future RF and differential logic electronics applications.

[1] ITRS 2013, Process integration, devices, and structures summary
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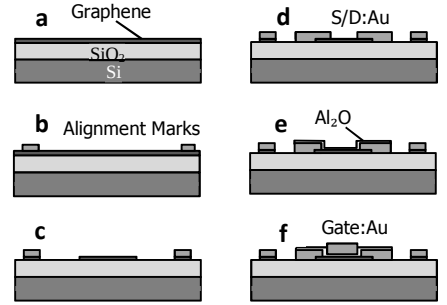

Figure 1. Process flow. (a) Substrate Si, 512um + SiO_2, 285nm + Graphene; (b) Alignment Marks, Cr/Au (c) Graphene etch (d) S/D contacts, Cr/Au (e) gate dielectric, Al_2O_3; (f) gate metal

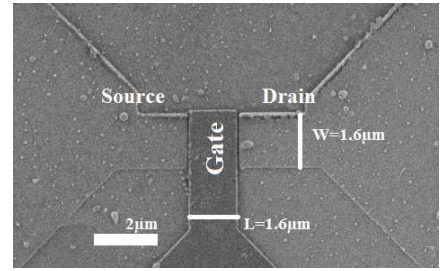

Figure 2. SEM image of a single Graphene FET, with L=1.6µm and W=1.6µm. (In order to protect the Graphene from electron irradiation device was imaged after electrical characterization – hence the contamination)

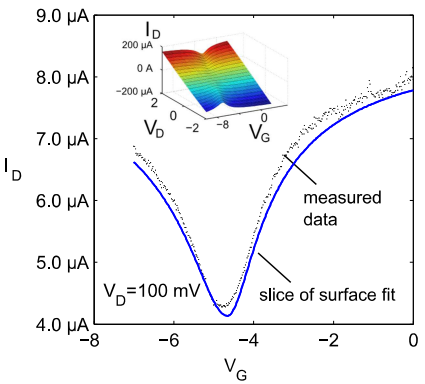

Figure 3. Typical I_D/V_D curve. The fit is obtained from multiple I_D/V_D measurements on the same device with varying V_D. Inset: extrapolation of complete current-voltage characteristic.

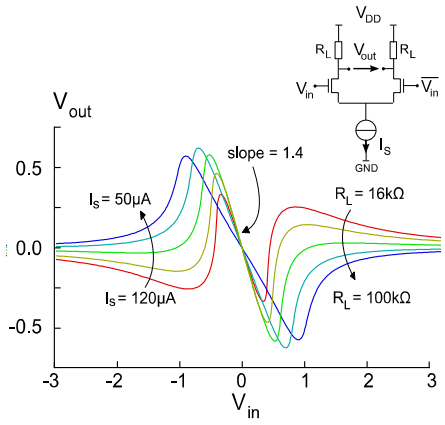

Figure 4. Sample of a differential input-output voltage transfer curve; $V_{DD} = 5\text{V}, g_m = 100\mu\text{S}$, $g_0 = 30\mu\text{S}$. Inset: schematic of the simulated circuit.