Characterization and analysis of InAs/p–Si heterojunction nanowire-based solar cell

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Abstract

The growth of compound semiconductor nanowires on the silicon platform has opened many new perspectives in the area of electronics, optoelectronics and photovoltaics. We have grown a 1×1 mm^2 array of InAs nanowires on p-type silicon for the fabrication of a solar cell. Even though the nanowires are spaced by a distance of 800 nm with a 3.3% filling volume, they absorb most of the incoming light resulting in an efficiency of 1.4%. Due to the unfavourable band alignment, carrier separation at the junction is poor. Photocurrent increases sharply at the surrounding edge with the silicon, where the nanowires do not absorb anymore. This is further proof of the enhanced absorption of semiconductors in nanowire form. This work brings further elements in the design of nanowire-based solar cells.

Keywords: InAs, molecular beam epitaxy, solar cell, light absorption

(Some figures may appear in colour only in the online journal)

1. Introduction

Compound semiconductors (III–V) are of special interest for electronic and optoelectronic devices thanks to their high electron mobility and direct band gap [1–3]. A key issue to make them attractive for industrial applications is their integration on the widely developed Si platform. There are numerous challenges for a successful integration of III–Vs on silicon, such as lattice mismatch, differences in thermal expansion coefficients and polarity [4]. It has been shown that III–V nanowires can overcome these challenges thanks to their small footprint [5–7]. In the case of nanowires the strain can be relaxed laterally thanks to their small diameter and dislocations are present only at the interface, with little impact on the device performance [8, 9]. Alternative high potential devices consider the heterojunction between Si and a monolayer semiconductor such as graphene [10, 11] or MoS$_2$ [12, 13].

In numerous applications a control on the position and orientation of the nanowires is required. Vertical orientation of nanowires can be achieved on Si (1 1 1) substrates in very high yields [14–16]. In the case of catalyst-free growth, ordered arrays of nanowires can in principle be attained by employing a patterned SiO$_2$ mask [15, 17–19].

Among the applications of III–V arrays on silicon are tunnel diodes [23], photoelectrochemical water splitting [24, 25] and solar cells [26, 27]. By combining a GaAs nanowire array on a silicon cell, a dual junction with a theoretical efficiency higher than 30% could, in theory, be achieved [28]. Another consequence of the nanowire small diameter is that light absorption can only be understood from a wave optics perspective. This results in the appearance of interesting phenomena such as the presence of guided and leaky modes [29, 30]. Recently, it has been shown that standing semiconductor nanowires are extremely efficient in absorbing light [31–33]. Their absorption cross-section is much larger than their physical bounds. Thanks to this property, the optimal design of nanowire-based solar cells includes arrays with a relatively large pitch, leading to very large void fractions up to 90%. This discovery has led to the achievement of InP solar cells with an efficiency up to 13.8% [34]. The achievement of such an efficiency by other groups is limited to the ability of growing these high quality arrays and by the ability of producing the devices with high yield. The challenges linked to the growth of GaAs arrays on silicon have hampered so far the achievement of a GaAs nanowire array solar cell on silicon
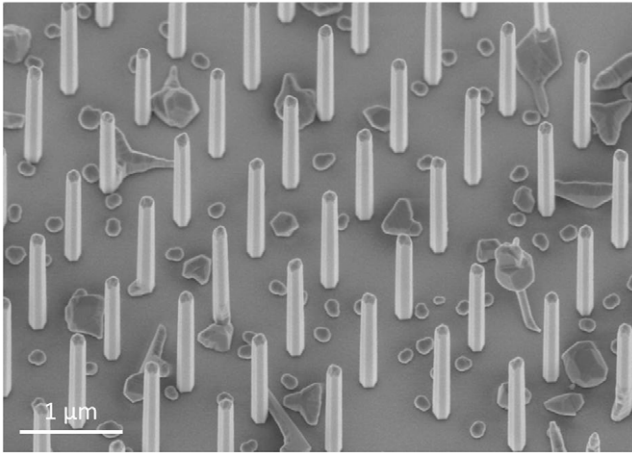
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Figure 1. SEM image tilted 25° of a position-controlled InAs nanowire array on a Si (1 1 1) substrate. More detailed characterization on the length and diameter distribution is given in the appendix.

[20–22]. The same device is much more straight forward for InAs, though the small band gap hinders the achievement of high efficiency. InAs surfaces are known to be n-type due to the Fermi level pinning at the surface [35], which results in a n-InAs/i-InAs/p-Si heterostructure. An efficiency of 0.76% has been previously obtained for non-ordered arrays of n-InAs on p-Si substrate [26]. A dramatic decrease of the generated photocurrent for wavelengths above the silicon absorption edge was observed. In this work, we analyse the contribution of both InAs nanowires and silicon substrate to the overall photocurrent considering the fundamental physical properties of the heterojunction.

2. Experimental

InAs nanowire arrays were grown by molecular beam epitaxy in a DCA P600 system, following recent works [15, 36]. They were grown on 275 μm thick Czochralski $\langle 1\,1\,1 \rangle$ p-doped Si wafers with a resistivity of 10–20 Ω cm. In view of making a solar cell device, the patterned area was 1×1 mm^2. The diameter and pitch of the holes was respectively 100 nm and 800 nm, which should lead to a light self-concentration effect in the nanowires [36]. The InAs nanowires were grown at 500 °C, with an arsenic partial pressure of 6×10^{-6} Torr and a rotation of 7 rpm for 1 h. We used a nominal In growth rate of 0.2 Å s^{-1}. A typical scanning electron microscope (SEM) image of the nanowires can be shown in figure 1. 1.8 ± 0.1 μm long wires were obtained with diameters of 165 ± 6 nm. After the growth, the device was fabricated. As shown in figure 2(*a*), the core of the InAs nanowire is in electrical contact with the p-type silicon through the opening in the SiO$_2$ mask. In order to electrically insulate the p-doped Si substrate from a subsequent front contact, the nanowires and the substrate were covered by a 17 nm thick conformal layer of sputtered SiO$_2$ (figure 2(*b*)). Then, the nanowires were embedded in a polymer matrix which would act as an etch barrier for the oxide located on the substrate. For this purpose, photoresist AZ1512HS was spin-coated at 1700 rpm for 1 min and baked at 120 °C for

5 min, obtaining a homogeneous film of 2050 nm (figure 2(*c*)). Afterwards, the resist layer was etched down for 2 min using an O$_2$ induced coupled plasma (ICP). A controlled etch was achieved by using an electrostatic chuck power of 100 W and an ICP source power of 600 W. The remaining photoresist thickness was around 275 nm. The sputtered oxide covering the polymer-free part of the wires was removed by dipping the samples in a buffered HF 7 : 1 solution for 45 s (figure 2(*d*)). Before depositing the front contact, a last O$_2$ plasma removal was carried out, in order to ensure the sample would be clean from any organic residue. Finally, 200 nm of aluminum was sputtered on the backside of the device and 500 nm of ITO on the front side (figure 2(*e*)). On top of the ITO, a ring around the arrays consisting of 10 nm of Ti and 200 nm of Au was evaporated through a metallic mask. This last step has shown to be critical for a low resistance contact with the probe tip [37].

The current–voltage characteristics were measured by a sourcemeter (Keithley 2611) in the dark and under illumination conditions of AM1.5G by using a standard solar simulator (Sol2A Oriel 150 W Xenon lamp). The spectral response measurements were performed with a 250 W tungsten–halogen lamp coupled to a grating monochromator (Acton SpectraPro SP2155) and the photocurrent measured with a Keithley 2100 multimeter.

3. Results

The current–voltage measurements in the dark and under illumination are shown in figure 3(*a*). In the dark, the device presents a typical curve of a diode. Under illumination, the current–voltage characteristics are down-shifted due to the photogeneration of carriers. The short-circuit current density obtained was 14 mA cm^{-2}, taking into account the total illuminated area, which was 1.5×1.5 mm^2 (2.25 mm^2). This includes both the InAs array and the surrounding Si substrate. The open-circuit voltage and fill factor are respectively 310 mV and 0.32, resulting in a conversion efficiency of 1.4%. The Shockley–Queisser limit for an InAs single junction is around 6% [38]. In the following, we analyse the characteristics of the device and explain the reasons why our efficiency is four times lower than the theoretical prediction. We will start by presenting the external quantum efficiency (EQE) measurement and follow by an analysis of the band alignment and light absorption.

The EQE of the device is shown in figure 3(*b*). Even though the infrared part of the spectrum is not shown, we can already see that the photoresponse at the Si absorption edge decreases close to zero. Moreover, the overall photoresponse is below 15% with maximum values between 700 and 800 nm. This means that overall, each impinging photon has a chance of 15% to result into a collected electron–hole pair. These values are dramatically low for a solid-state photoconversion device. To give an example, we have reported values of EQE between 70% and 80% in Si microwire solar cells before [37]. In order to shed some light on the reasons for these low values, we have performed finite difference time-domain (FDTD) simulations of light propagation and absorption by using the MEEP package [39]. The goal was to understand
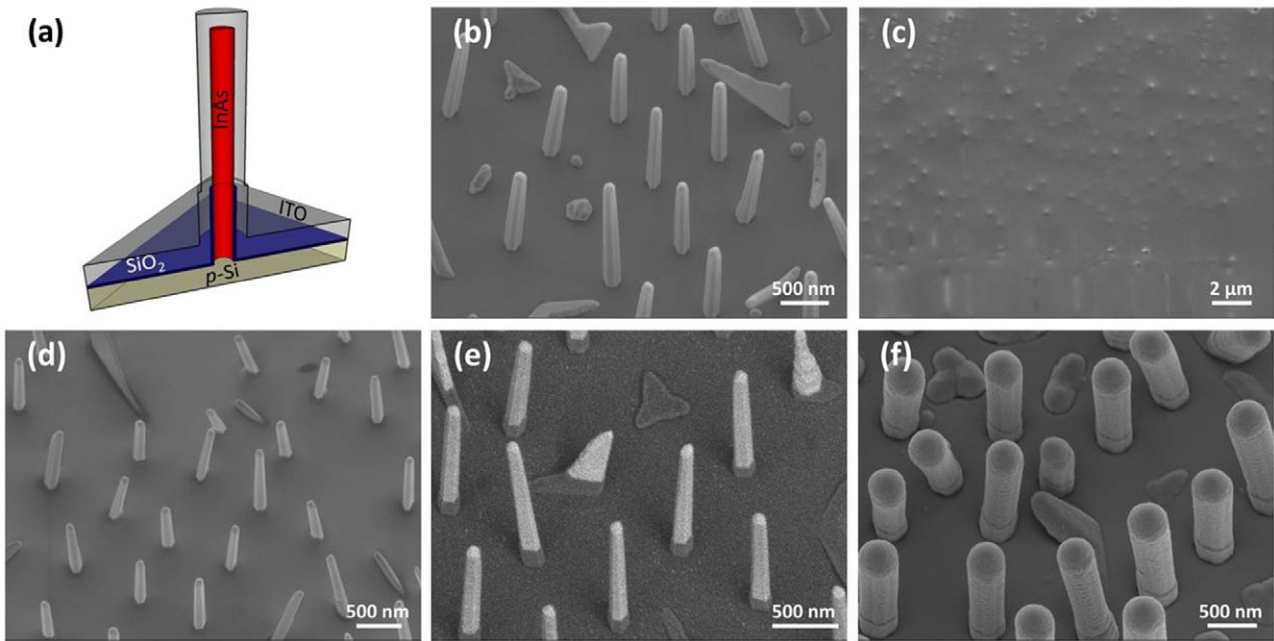
Figure 2. 20° tilted SEM images of the fabrication process. (*a*) Schematic of the final device composed by a Si–InAs p–n heterojunction. (*b*) As-grown InAs nanowires array on a p-doped Si substrate with a 17 nm layer of sputtered SiO_2. (*c*) Spin-coating of a 2 μm thick AZ1512HS photoresist. (*d*) Partially etched photoresist and removal of the unprotected oxide. (*e*) Removal of the remaining photoresist. (*f*) Sputtering of ITO front contact.
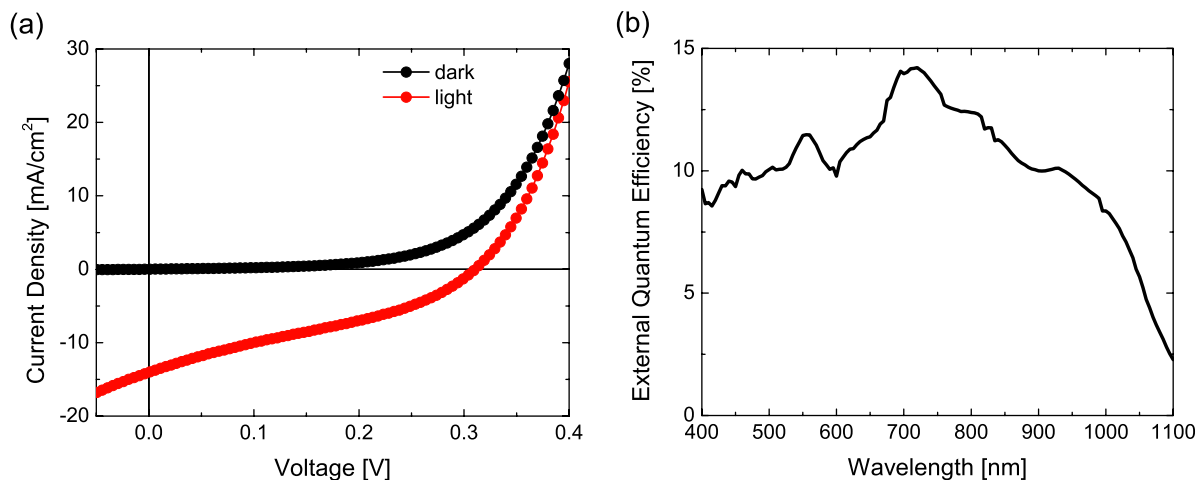

Figure 3. (*a*) *I*−*V* characteristic curve in the dark and under AM 1.5G illumination and (*b*) EQE spectrum of the device formed by InAs nanowires on a p-doped Si substrate.

what part of the spectrum and where light was absorbed in the device. The simulations were performed for an array of InAs nanowires with similar dimensions as our device standing on a 1 μm thick Si substrate. The nanowires had a diameter of 160 nm, a length of 2 μm and 800 nm of pitch. We included a layer of 17 nm of silicon dioxide covering the substrate and a layer of 150 nm of ITO as the front electrode. An incoming linearly polarized plane wave, approaching the structure at normal incidence was modelled. We simulated the electric field energy distribution for the following wavelengths: 450, 550, 600, 700, 800 and 1000 nm. The cross-section mappings are plotted in figure 4. We show the results for cross-sections taken in and perpendicular to the plane of light polarization. According to the simulations, for most of the wavelengths

light is absorbed mainly at the upper part of the nanowire. As a consequence, even though light is efficiently absorbed, the low EQE values indicate that the photogenerated electron–holes are not collected efficiently. Interestingly, in the case of wavelengths between 700 and 800 nm, light is absorbed more homogeneously along the wire and also close to the InAs/Si junction. This allows a higher electron–hole pair separation and carrier collection, which could explain the slight photocurrent increase within this range of wavelengths.

Now, in order to link light absorption to carrier collection, we refer to the band structure of our device, typical of type-I abrupt heterojunctions. Figure 5 shows the band diagram of the heterostructure in the dark and under illumination calculated with the software package next**nano**[3] [40]. The junction is
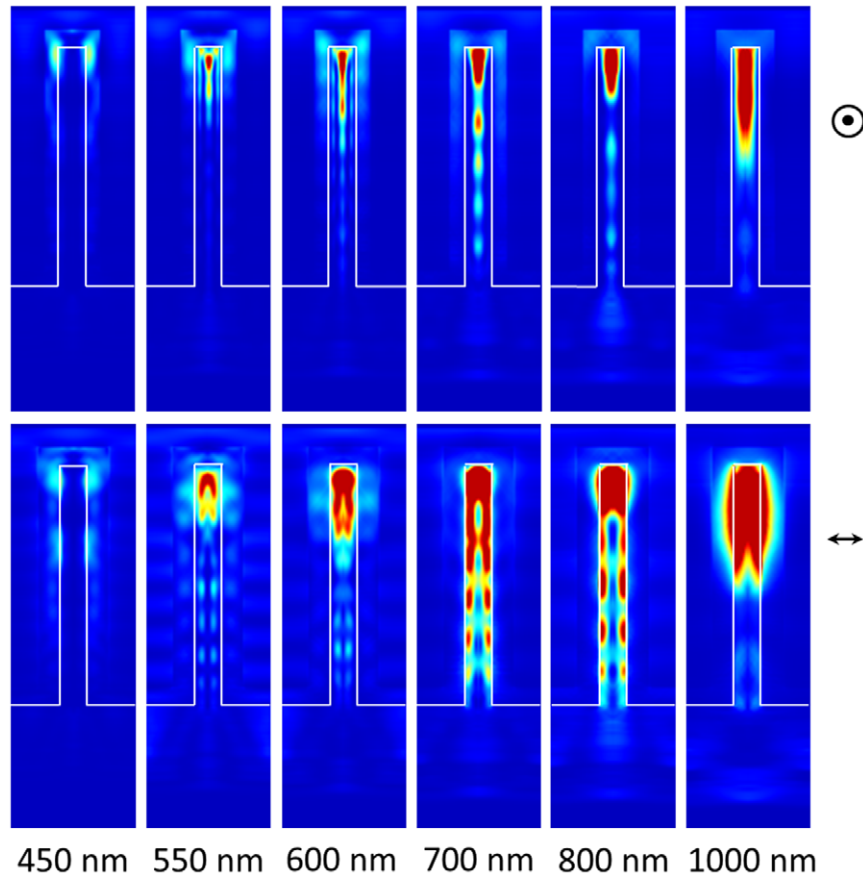
Figure 4. FDTD simulated cross-sections of the electric field energy density (top: cross-section at $x = 0$; bottom: cross-section at $y = 0$) at 450, 550, 600, 700, 800 and 1000 nm.
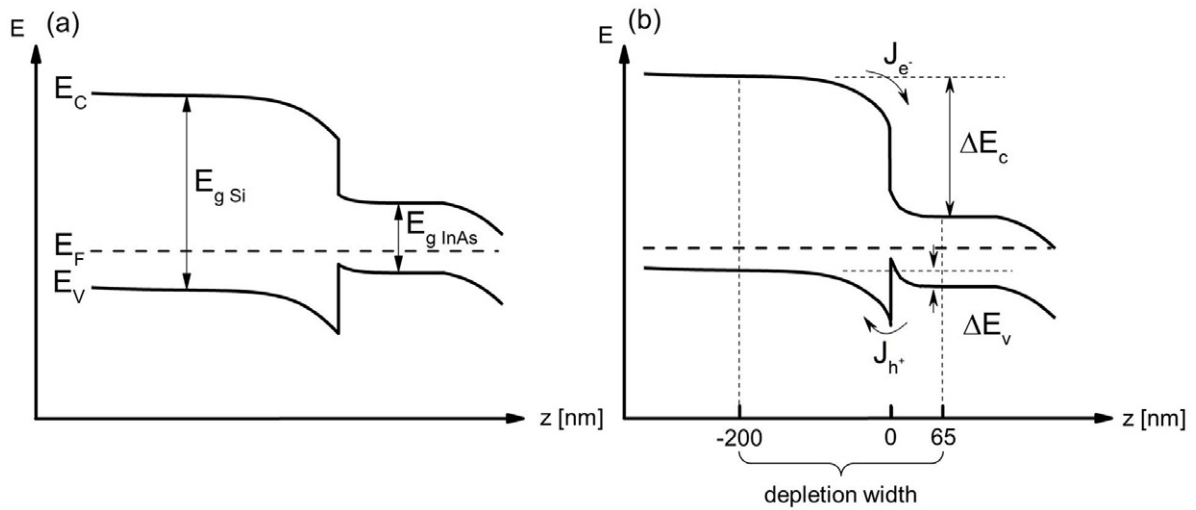

Figure 5. Band diagram of the Si/InAs heterojunction at thermal equilibrium (*a*) in the dark and (*b*) under illumination. J_{h^+} denotes the hole tunnelling current and J_{e^-}, current due to electron drift.

characterized by conduction and valence band offsets due to different electron affinities and band gaps of Si and InAs. We can see that due to the band alignment, the injection of holes from the InAs side to the Si side is blocked, while the injection of electrons from the Si side to the InAs side is favoured. Figure 6 shows the calculated electric field at the junction. It can be observed from the plot that the depletion region at the

Si side is about three times larger (around 200 nm) than at the InAs side (around 65 nm), helping preferentially the collection of carriers from the substrate. It is well known that self-catalysed InAs nanowires present a high density of stacking faults and polytypism, which results in a small diffusion length of carriers, typically around a few tens of nanometres [41]. This means that most of the carriers generated at the nanowire
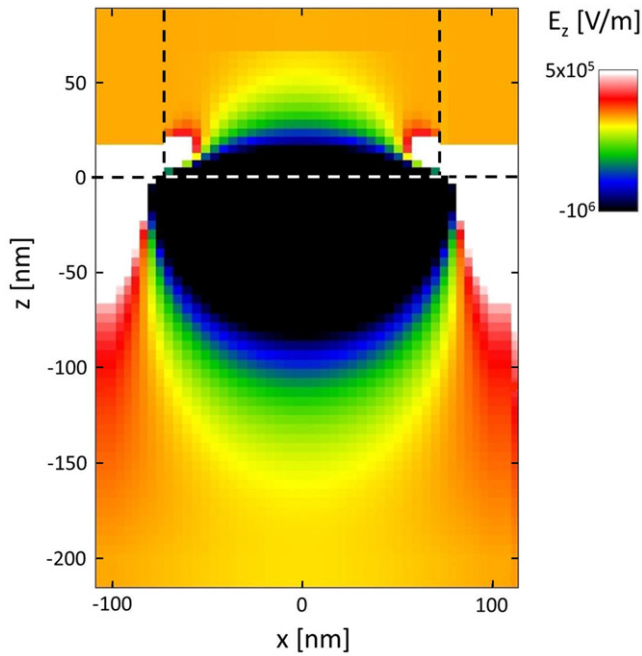
Figure 6. Axial component of the calculated built-in electric field at the InAs/Si junction.

will recombine before diffusing to the junction. These results justify the low values of the quantum efficiency.

Finally, in order to further confirm the origin of the low carrier collection of the device, we performed spatially resolved photocurrent measurements on the device. The nanowire array was mounted on an $x-y$ piezostage and illuminated with a wavelength of 600 nm, 800 nm and 950 nm and a spot diameter of 976 nm, 1301 nm and 1545 nm, respectively. As the solar cell device was 1.5 mm long, we could not scan the entire device, but performed line scans across the device and to the surrounding silicon substrate. The line scans were 80 μm long, from the InAs nanowire array to the silicon substrate, away from the junction. Figure 7 shows the photocurrent generated under zero bias by the Si/InAs heterojunction and the exponential decay dependence on the distance from the junction for each wavelength. The response is quite homogeneous when the light spot is placed on the nanowires but increases significantly when the uncovered silicon substrate next to the junction is illuminated. Then the photoresponse decreases exponentially when moving away from the array. It is interesting and a bit counterintuitive to note that electron–hole collection is higher when light impinges at the edge of the InAs array and Si. Even though light impinging on the array is highly absorbed, electron–hole pairs are not collected because of the unfavourable band alignment and bad diffusion of carriers in the InAs nanowire. On the contrary, provided the carrier diffusion length is high enough, electrons photogenerated in the silicon substrate close to the InAs array are attracted to the junction by the built-in electric field of the conduction band offset and collected. These results confirm what is stated above: in the InAs array region even though the void fraction is extremely high, the light is mainly absorbed within the nanowires. Then, due to the band alignment, discontinuities occur in the valence band

with band cusps that hamper hole injection efficiency from InAs to Si and limit the device current. Nevertheless, when light is absorbed within the silicon, the conduction band offset assists the drift of electrons to the junction. The photoresponse profile at the InAs-to-Si transition becomes less sharp with the wavelength because the spot of the light increases linearly with it. These results also explain the disagreement between the EQE spectrum and the short-circuit current density: the spectral response was taken from the nanowire array while $I-V$ measurements were done on a surface larger than the array. Thus, the Si substrate surrounding the array also contributed to the generated photocurrent. As shown here below this leads to an overestimation of the conversion efficiency.

On the other hand, the diffusion length of minority carriers in silicon can be extracted from the exponential decay of the photoresponse versus the distance from the junction by the following expression:

$$I_{ph} \propto \exp\left(-\frac{d}{L_{diff}}\right), \qquad (1)$$

where I_{ph} is the photocurrent, d is the distance from the junction and L_{diff} is the diffusion length. The diffusion lengths obtained were 17.8 μm, 39.8 μm and 123.3 μm for a wavelength of 600 nm, 800 nm and 950 nm, respectively. This increase is due to the surface effect: photons with longer wavelengths are absorbed deeper inside the silicon, where there is lower density of traps and, hence, lower recombination rate. However, these values are still lower than bulk lifetimes. All values should increase when illuminating with higher intensities. When the density of carriers is lower than the density of traps, the recombination rate presents a constant maximum dominated by the concentration of traps. Then, for higher densities of photocarriers the recombination rate decreases, leading to an enhancement of lifetime over one order of magnitude [42], which would be in agreement with values reported in literature for bulk lifetimes.

We conclude that the potential of InAs nanowire arrays on Si as a solar cell could be further improved by increasing the spacing between wires and thus, reducing the total InAs volume. In this way, more light could be absorbed in the silicon substrate by keeping the antireflective function of nanowires.

4. Conclusions

Ordered arrays of vertical InAs nanowires on a patterned Si substrate were grown by means of molecular beam epitaxy. The potential and pitfalls of the InAs/Si heterojunction for photovoltaic applications was evaluated. An efficiency of 1.4% and a J_{sc} of 14 mA cm^{-2} was obtained. It is demonstrated that for a nanowire spacing of 800 nm the light is mostly absorbed within the nanowires. However, due to the band alignment of the heterostructure the contribution of InAs to the overall photocurrent is dramatically low. Thus, InAs nanowires have the function of antireflection coating and carrier collector. As a consequence, a better performance could be achieved by reducing the density and length of nanowires and thus, increasing the light absorption in the silicon substrate.
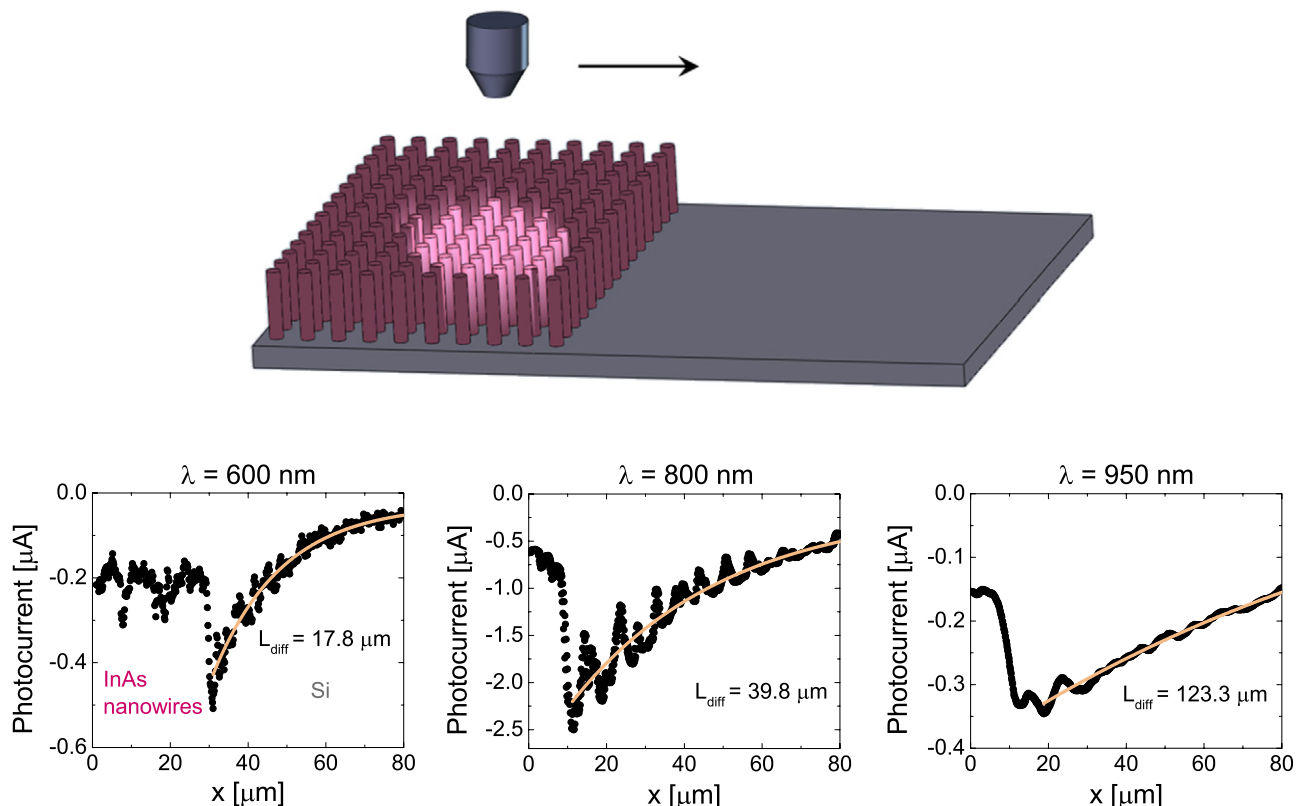
Figure 7. Schematic of the photocurrent line-scan measurement and photocurrent profiles at 600, 800 and 950 nm. The red line shows the fitted photoresponse exponential decay versus distance from the heterojunction. Note that the measured photocurrent is depicted with a negative sign.
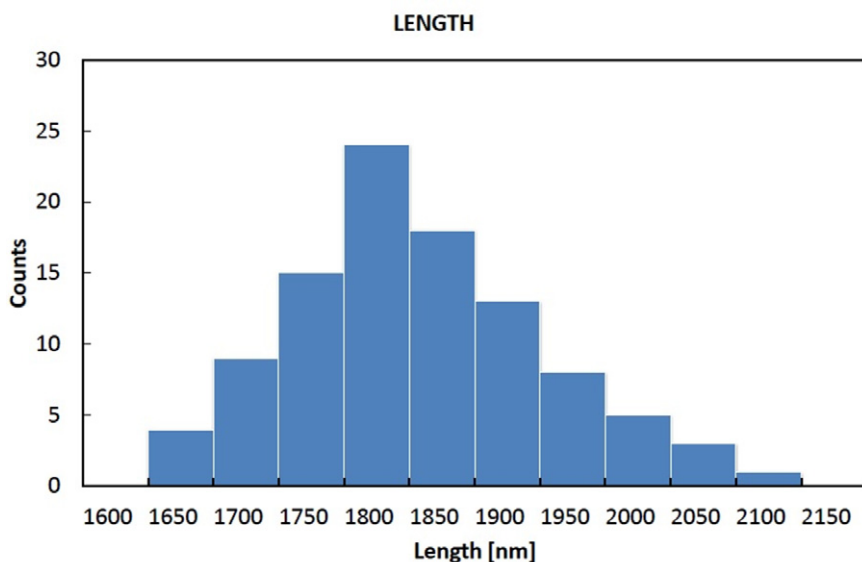

Figure A1. Length of InAs nanowires.

Finally, the diffusion length of minority carriers in the silicon substrate was shown to be strongly affected by the surface recombination.

Appendix

Histograms of the length and diameter of InAs nanowires generated from 100 random nanowires are presented in figures A1 and A2.

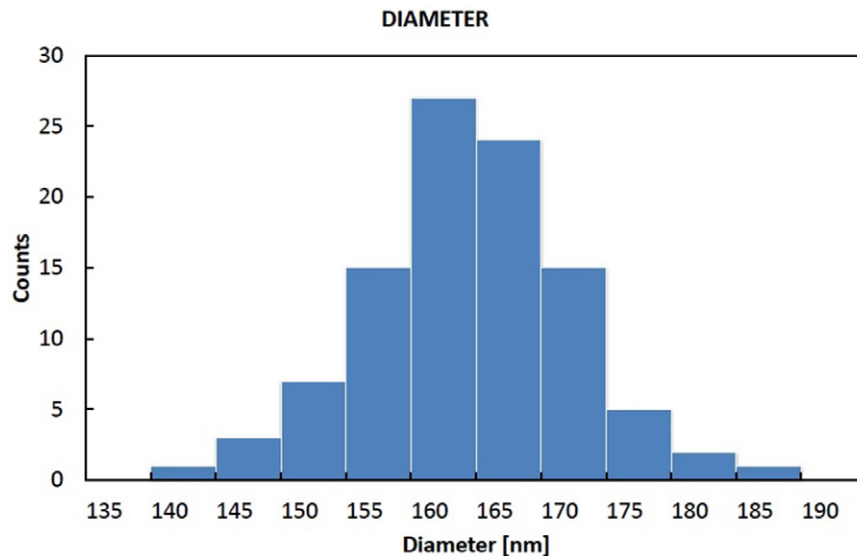J. Phys. D: Appl. Phys. **47** (2014) 394017

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Figure A2. Diameter of InAs nanowires.

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