Passivating contacts for homojunction solar cells using a-Si:H/c-Si hetero-interfaces

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Abstract

Crystalline silicon (c-Si) homojunction solar cells account for over 90% of the current photovoltaic market. However, further progress of this technology is limited by recombinative losses occurring at their metal-semiconductor contacts. The goal of this thesis is to develop passivating contacts to resolve this issue. The novel idea presented in this work is to insert an ultra-thin wide bandgap semiconductor—hydrogenated amorphous silicon (a-Si:H)—film underneath the metal to passivate the doped c-Si surface and suppress the recombination of minority charge carriers. Simultaneously, this layer should provide a contact to the metal allowing majority charge carrier transport. A transparent conductive oxide is additionally inserted between the a-Si:H layer and the metal to ensure efficient carrier collection. This concept is inspired by the silicon heterojunction solar cells, a technology characterized by extremely high open-circuit voltages.

The development of these new passivating contacts requires two features: a homojunction, for charge separation, and a silicon heterojunction contact for improved passivation. In this thesis, we explicitly focus on large-area thin-film deposition technology for fabrication of our devices, guaranteeing the scalability of our findings. The main results of this thesis are then threefold. First, we show that, using low-temperature plasma enhanced chemical vapor deposition, a doped homo-epitaxial layer can be deposited to form the homojunction. Second, we develop passivating contacts and optimize them in silicon heterojunction solar cells. An in-depth analysis of the contact formation is provided, including a detailed investigation of the relevant interfaces in our proposed structure. Finally, combining these two technologies, we demonstrate a proof-of-concept for these passivating contacts. Highly doped phosphorus- and boron-doped c-Si surfaces are shown to be efficiently passivated by a-Si:H layers and a lower contact resistivity is obtained for our optimized passivating contacts on such doped surfaces compared to a heterojunction contact on lightly doped surfaces. We show that homojunction solar cells on diffused and ion-implanted wafers featuring such passivating contacts (called homo-hetero cells hereinafter) yield improved open-circuit voltages compared to conventional homojunction solar cells, due to reduction of recombination losses. Additionally, the temperature coefficient of such homo-hetero solar cells is lower. With these advantages, the homo-hetero cells outperform homojunction solar cells when operating at a cell temperature above 60 °C.

This work contributes to the research and development of high-efficiency silicon solar cells by providing new insights on the properties of contact formation and a novel contact-type.

Keywords: passivating contact, silicon solar cells, silicon heterojunction solar cells, passivation, amorphous silicon, epitaxial growth, PECVD, fill factor analysis, sputter damage, atomic layer deposition, contact resistivity, homo-hetero structures, diffused junctions, ion-implantation, temperature coefficient.

Résumé

Les cellules solaires à homojonction en silicium cristallin (c-Si) représentent de nos jours plus de 90% du marché du photovoltaïque. Actuellement, le rendement énergétique de cette technologie est limité par les pertes de recombinaison se produisant au contact métal/semi-conducteur. L'objectif de cette thèse est de développer des contacts passivants pour s'affranchir de ces pertes. L'idée originale est d'insérer en dessous du métal une couche ultra-mince de silicium amorphe hydrogéné (a-Si:H) pour passiver la surface du c-Si dopé et réduire ainsi la recombinaison des porteurs de charge minoritaires. Simultanément, cette couche doit servir de contact permettant le transport des porteurs de charge majoritaires. Pour favoriser ce dernier, un oxyde conducteur transparent est inséré entre le a-Si :H et le métal. Ce concept de contact est inspiré des cellules solaires à hétérojonction en silicium, une technologie caractérisée par de tensions records en circuit ouvert. Le développement de ces nouveaux contacts passivants nécessite la combinaison de deux technologies différentes sur une même cellule solaire: d'une part la fabrication d'une homojonction, et d'autre part la formation d'un contact à hétérojonction en silicium. Dans cette thèse, nous nous concentrons sur la fabrication de ces deux éléments par la technique de dépôt de couches minces

Les principaux résultats de cette thèse se présentent en trois volets. Tout d'abord, nous montrons que, en utilisant un dépôt chimique en phase vapeur assisté par plasma, une couche homo-épitaxiale dopée peut être déposée pour former l'homojonction. Deuxièmement, les contacts passivants sont développés et optimisés dans les cellules solaires à hétérojonction en silicium. Une analyse en profondeur de la formation de ces contacts est présentée. Finalement, en combinant ces deux technologies, nous démontrons une preuve de concept pour ces contacts passivants. Les surfaces de plaquettes de c-Si fortement dopées peuvent être efficacement passivées par des couches d'a-Si:H et une résistivité de contact inférieure est obtenue par rapport à des surfaces plus légèrement dopées. Des cellules solaires à homojonction comportant de tels contacts passivants montrent une augmentation de la tension en circuit ouvert par rapport à une cellule à homojonction conventionnelle, indiquant que les pertes de recombinaison sont effectivement réduites. De plus, les cellules avec ces contacts passivants bénéficient d'un coefficient de température bas. Combinant ces avantages, les cellules à contacts passivants sont alors plus performantes que les cellules à homojonction, quand opérées à une température de cellule supérieure à 60 °C.

Ce travail contribue au développement de cellules solaires en silicium à haut rendement en fournissant une nouvelle approche sur la formation des contacts et de leur passivation.

Mot-clé: Contact passivant, cellules photovoltaïques à homojonction en silicium cristallin, cellules photovoltaïques à hétérojonction en silicium cristallin, passivation de surface, silicium amorphe, croissance homo-epitaxiale, PECVD, analyse du facteur de forme de courbe courant-tension, dommage induit par le sputtering, atomic layer deposition, résistivité de contact, structures à homo- et hétéro-jonction.

Acronyms and abbreviations

a-Si:H	amorphous silicon
BSG	borosilicate glass
c-Si	crystalline silicon
E_F	Fermi level energy
FF	fill factor
J	current density
J_{sc}	short circuit current density
JV	current-voltage
J_0	recombination current density prefactor
LBIC	light beam induced current
i*FF,* i*J,* iV_{oc}	implied-fill factor, implied-current density, implied open-circuit voltage
µc-Si:H	microcrystalline silicon
MS	metal-semiconductor
MIS	metal-insulator-semiconductor
MPP	maximum power point
PECVD	plasma enhanced chemical vapor deposition
p*FF,* p*J,* pV_{oc}	pseudo-fill factor, pseudo-current density, pseudo-open-circuit voltage
PSG	phosphosilicate glass
R_s	series resistance
ρ_c	contact resistivity
SE	spectroscopic ellipsometry
SHJ	silicon heterojunction
SRH	Shockley-Read-Hall
TCO	transparent conductive oxide
TLM	transfer length measurement
τ_{eff}	effective minority carrier lifetime
V	voltage
V_{oc}	open-circuit voltage

Chapter 1 Introduction

Here, we provide a general overview of the development of the photovoltaic market. Within this context, we explain the relevance and goals of the work presented in this thesis. After a description of the structure of this thesis, the main contributions to the research field resulting from this work are summarized.

1.1 General context

1.1.1 Electricity production and environment: the advantages of solar energy

In 2011, the world energy consumption amounted to more than 150'000 TWh [IEA 2013b]. With the exception of nuclear energy, this energy is all, in some form, retrieved from the sun: Fossil fuel is biomass that has been concentrated by pressure and heat within the earth's crust, hydroelectricity uses the potential energy of sun-evaporated water and, photovoltaics (PV) and photothermal energy are direct conversions of sunlight into electricity and heat, respectively. An important difference between these energy sources is the timescale of renewal. While it takes thousands of years to convert biomass into fossil fuels, only a few decades are needed to grow a forest and a few days suffice to fill a hydroelectric dam. Wind and solar energies may be renewable instantaneously depending on the weather. To have a sustainable energy source, the timescale of renewal must be equal or shorter to the timescale of consumption. Fossil fuels are, in this regard, not a sustainable source of energy in the long term. Most importantly, burning fossil fuels releases carbon dioxide (CO_2) into the atmosphere, and the emitted quantities are so large that it has amplified the native atmosphere greenhouse effect, leading to a global rise of temperature on land and in the ocean [IPCC 2013]. As seen in Figure 1.1, to generate 1 GWh of electricity, energy production with solar PV mitigates the CO_2 released into the atmosphere by more than one order of magnitude compared to fossil fuel [WNA 2011]. Furthermore, contrary to nuclear energy which is a non-renewable source (uranium-235 was formed in supernovas about 6.6 billion years ago), there is no dangerous waste to dispose of. Therefore, PV presents a solution to produce energy in a sustainable way, by drastically reducing the CO_2 emissions compared to fossil fuels and by not generating radio-active wastes. Remarkably, solar energy is available around the world: almost all countries can use it as a significant source of their energy mix and therefore secure their supply, without relying on potentially fickle geopolitical relations.

In addition, in 90 minutes, enough sunlight reaches the earth to provide the entire planet's energy needs for one year [IEA 2011]. To summarize, solar energy combines simultaneously the advantages of being renewable, having a low environmental and social impact and being a potentially large energy source.

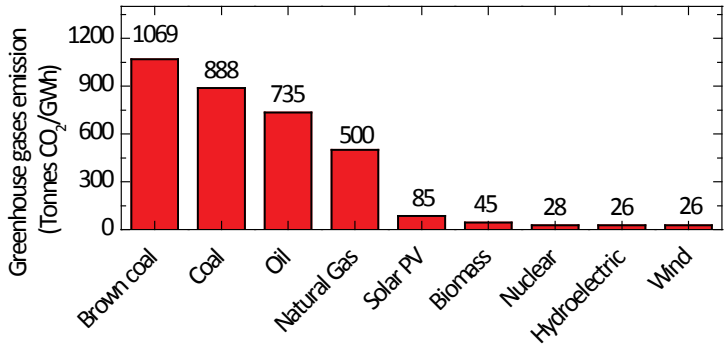


Figure 1.1: Comparison of CO_2 equivalent emissions of the main sources of electricity generation. [WNA 2011]

Despite the clear attractiveness of photovoltaics, persistent myths surround this technology. As an example, sometimes, solar energy is denounced as having a too low energy conversion efficiency and a too long energy payback time. First, nowadays, the energy-conversion efficiency for a state-of-the-art commercial PV module reaches 20%. This means that 20% of the sun's energy that reaches the panel is converted into electricity. When compared to the 30 to 40% efficiency of systems that are used to convert biomass or fossil fuels into electricity this could seem limited, but this is not taking into account that biomass is retrieving energy from the sun via photosynthesis, the efficiency of which is limited to 1%. In the same manner, the alternator used to transform the potential energy of water into electricity has an efficiency close to 95%, but it uses only a small fraction of the potential energy of the water evaporated by the sun. Second, on average as little as 0.5 to 3 years is needed for a PV system to give back the energy that has been used to fabricate it, depending on the technology used and the annual irradiance level of the area where the panel is installed [Fthenakis 2012]. Most solar panels are guaranteed by the manufacturer for at least 20 years, which will likely increase in the coming years to values as high as 50 years.

1.1.2 Cost decrease and competitiveness: the economics of photovoltaics

The performance of a photovoltaic system is often expressed in watt-peaks (Wp). This unit expresses the cumulated power of the modules of a system measured by the manufacturer under standard test conditions (STC, 25 °C, 1000 W/m^2, AM 1.5 spectrum). It basically represents the maximum power that can be expected from the module under ideal atmospheric and geographical conditions. The energy that can be extracted from a system will depend on the

precise geographic location. As an example, in Switzerland, for a mean irradiance of 1000 W/m^2, a solar panel will produce 1 kWh/Wp. This means, that if a household consumes 5'500 kWh/year (CH average for a 4 people household [Nipkow 2013]), using a 20% (10%) module, 25 m^2 (50 m^2) of modules would be needed to provide this energy.

The price of an installed photovoltaic system is given in currency (e.g. CHF) per Wp. This price includes the costs of the solar modules and balance-of-system (inverters, mounting structures, land, engineering/design, installation). The price of electricity produced from a PV system is given in currency per kilowatt-hours (kWh). The ratio between the system's lifetime cost (including capital cost) and cumulated system lifetime energy production is called the levelized cost of energy (LCOE). For a given PV system price, the LCOE will depend mainly on the annual irradiance level of the area where the PV system is installed. Figure 1.2 illustrates PV installations in Switzerland.

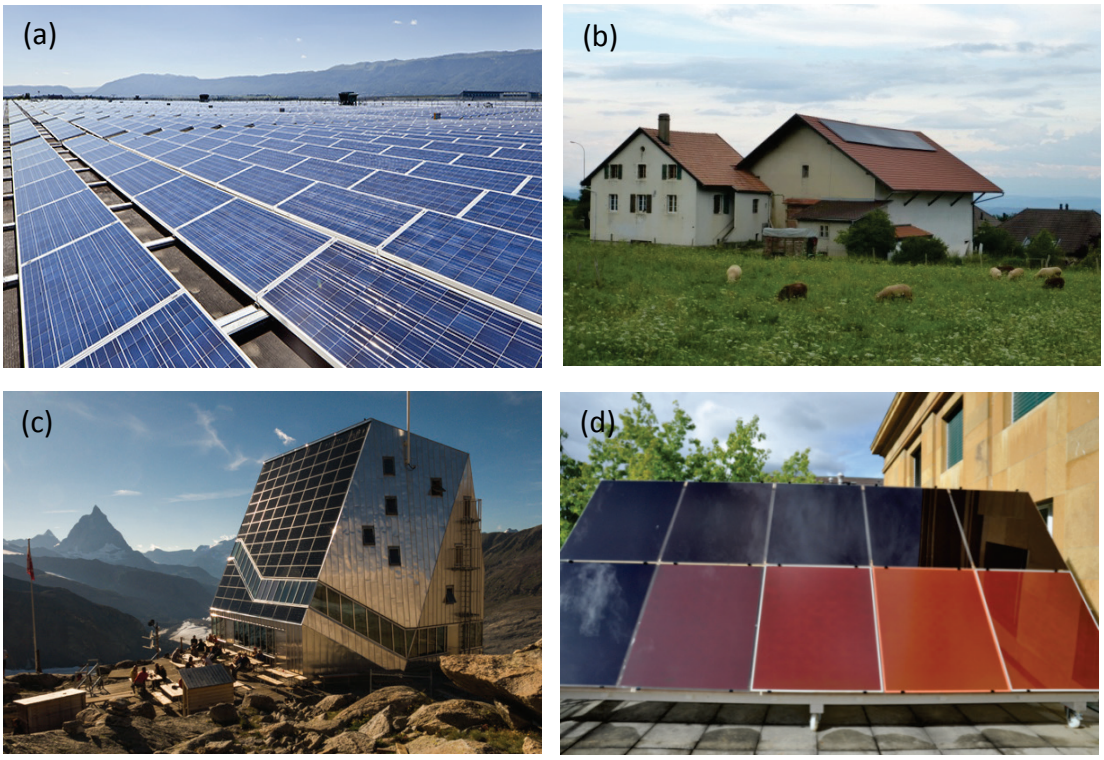


Figure 1.2: (a) Palexpo PV power plant (Geneva, Switzerland, 4'200 MWh, crystalline silicon modules) [SIG 2012]. (b) PV system connected to the grid in a house in Montmollin, Switzerland (Sunpower crystalline silicon modules). (c) The south face of the Monte Rosa Hut near Zermatt, Switzerland, is covered with PV to cover its electricity needs with a storage system (off-grid) [Blog 2013]. (d) PV-Lab's demonstration of the color tunability of silicon thin-film modules for integration on terracotta rooftops.

For the last 30 years, PV module prices have been steadily decreasing at a rate of about 20% per year, reaching less than 1 CHF/Wp in 2012 [Jäger-Waldau 2013]. However, the price per Wp of a complete system strongly depends on its size and the country of the installation. In 2012, in Switzerland, installed prices ranged from 2.3 to 5.5 CHF/Wp for on-grid systems and the

lowest LCOE is around 0.2 CHF/kWh [IEA 2013c]. On average, off-grid systems are about twice as expensive as on-grid systems, due to the requirements of storage batteries and associated equipment [IEA 2013c]. As a comparison point, the retail (grid) electricity price is between 0.08-0.25 CHF/kWh [Hüsser 2013].

Grid parity occurs when the LCOE from a PV system is at a similar or lower level than the LCOE of conventional energy sources in a given area. In the residential market, this means that the cost of electricity production from the rooftop system of a private consumer is lower than the grid operator's retail price. Grid parity is reached first in countries where conventional energy is expensive or with a high annual irradiance level. Switzerland is forecasted to reach grid parity within a few years [Breyer 2013].

Reaching grid parity was expected to unlock PV market development without the further need of public incentives. However, now that that grid parity is achieved for on-grid systems in several countries (Italy, Denmark and more recently Spain [Breyer 2010]) and that PV electricity is reaching a significant share of electricity production (for example 7% in Italy), grid operators do not accept self-consumption combined with grid connection based on the standard retail price. Indeed, the grid operators need to maintain the grid. Self-consumption decreases their revenue while keeping constant the maintenance cost. Therefore, even if self-consumed electricity can be fully cost effective, solutions should be found to alternatively finance access to the grid. To conclude, grid parity does not necessarily lead to the full competitiveness of PV with traditional electricity sources yet, but it certainly indicates that it is getting close.

1.1.3 Current global installed capacity and outlook

In 2012, PV electricity accounted for 0.6% of the world's electricity production. Fossil and nuclear accounted for 78.2%, hydropower for 16.5% and other renewables for 5% [IEA 2013a]. In 2014, PV is forecasted to reach 1% [Nowak 2014]. Indeed, the market growth for renewables is much higher than that for conventional sources of energy. From 2000 to 2013, the cumulative PV installation has been multiplied by more than 100 (Figure 1.3). In the early 2000's this increase was driven mostly by the European market, especially thanks to Germany and its stimulating feed-in tariff program, which promotes the investment in and production of PV systems with financial incentives.

Since 2010, however, the growth is due mainly to emerging market countries and the USA. Interestingly, according to the International Energy Agency, in 2012, almost 50% of China's new energy installation was based on renewables, from which 10% was PV [IEA 2013a]. Worldwide, PV is forecasted to provide 10% of the world's electricity consumption by 2035 [IEA 2013a]. In Europe, PV already has 3% of the share and is planned to be 8% in 2020 and 15% in 2030 according to the European Photovoltaic Industry Association [EPIA 2013].

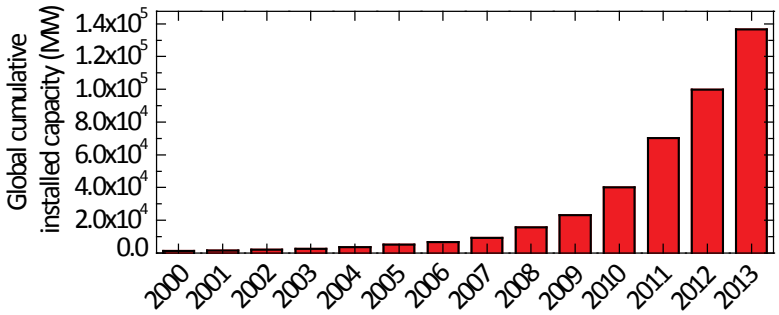


Figure 1.3: Evolution of the global cumulative installed capacity. Adapted from [EPIA 2014].

1.1.4 The different PV technologies: an efficiency race

The core of a PV system is an array of solar cells, which converts sun light into electricity. A solar cell is typically made of two parts:

- A semiconductor material in which sunlight is absorbed and generates electron and hole pairs through the photovoltaic effect (the absorber).
- Contacts to selectively collect electrons or holes in order generate an electrical current (the electron and hole collector).

The efficiency of a solar cell is the ratio of the electrical output power to the input power of the striking sunlight. The output power can also be expressed as the product of the open-circuit voltage (V_{oc}), the short-circuit current density (J_{sc}) and the fill factor (*FF*) of the device. These parameters are more precisely defined in Chapter 2.

Solar cells can be made out of different semiconductor materials, which classify PV modules in different technologies. There are two main classes available commercially: wafer-based solar cells and thin-film solar cells. The former is based on the use of crystalline silicon (c-Si) ingots that are cut into 100–300 µm wafers. The latter refers to vacuum-deposited semiconductors such as cadmium telluride (CdTe), copper indium sellenide (CIS) and thin-film silicon. Moreover, currently organic and so-called hybrid solar cells using organic and inorganic materials are being developed. The fabrication of such cells avoid vacuum or high-temperature processes making them potentially very cheap and reducing their energy payback time. All these technologies are in competition to become the most cost-effective way to produce electricity.

An important factor for the cost-effectiveness of a technology is the energy conversion efficiency of a device: the more efficient it is, the higher the power output per surface unit. The efficiency of a solar module is critical when considering applications with restricted available surface like rooftops. Moreover, the module price represents only a small share of the total PV system cost (typically 20% in the case of a c-Si–based PV system [Jäger-Waldau 2013]), and most of the remaining costs depend on the surface occupied by the panels and not the rated power

(encapsulation, mounting, land). Therefore, on the module level, the investment necessary for an improvement of efficiency is distributed over a bigger part of the system cost, resulting in higher revenue.

The efficiency of a solar cell is intrinsically limited by the photovoltaic effect itself. First, to generate an electron-hole pair in the semiconductor material from an impinging photon, an energy threshold exists. This implies that, for each material, the photon must have a minimum energy, called the material bandgap energy, before generating carriers in the material. Conversely, if the photons have a higher energy, this extra energy is lost by thermalization. Second, the solar spectrum is composed of photons of various energies following a black body radiation formula with a maximum around 2.5 eV. Therefore, for single-junction devices, there is a theoretical limit for solar cell efficiency depending on the absorbing material, called the Shockley-Queisser limit [Shockley 1961]. The efficiency limit for various absorbing materials is shown in Figure 1.4. This limit can be overcome using cells with different absorbing materials and stacking them on top on each other (multi-junction solar cells).

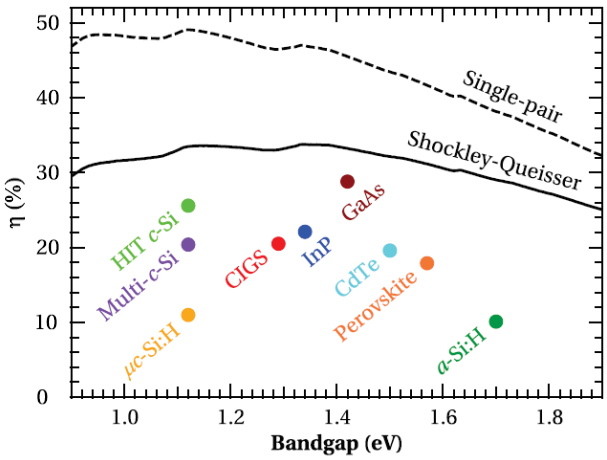


Figure 1.4: Efficiency as function of the bandgap for theoretical limits and record-devices. Reproduced from [Stückelberger 2014].

In Table 1:1 the current record efficiencies for single-junction solar cells are shown (exception made for thin-film silicon) for different technologies. They are measured in certified institutes under standard test conditions, which enables international comparison.

Conversely, these values do not provide information on the power the device will produce in a given location. This will depend on how the PV technology will react to a given climate (high/low temperature and irradiance level). For example, the STC temperature is 25 °C but a solar panel operates generally at around 60 °C. The efficiency variation with the temperature depends on the technology used and is characterized by the temperature coefficient of the device. The ratio between the rated and field efficiency is called the performance ratio.

Table 1:1 Record efficiency of single-junction devices (except thin-film Si) for different technologies. [Green 2014a, Green 2014b, Panasonic 2014].

Technology	Company / Institution	**Country**	**Efficiency [%]**	**Year**
Gallium Arsenide	Alta Devices	United States	28.8	2011
Heterojunction c-Si	Panasonic	Japan	25.6	2014
Mono c-Si	UNSW	Australia	25.0	1998
Multi c-Si	FhG-ISE	Germany	20.4	2004
Copper indium gallium selenide	NREL	United States	19.8	2008
CdTe	GE Global Research	United States	19.6	2012
Perovskites	KRICT Institute	South Korea	17.9	2014
Thin-Film Si	LG Electronics	South Korea	13.4	2012

GaAs solar cells are very costly and are thus used mainly for space applications. Therefore, c-Si based solar cells dominate the terrestrial PV market, as shown in Figure 1.5. This can be explained by the stability, non-toxicity and abundance of this material and by its well-known properties from its use in the microelectronics industry. We now focus on this technology.

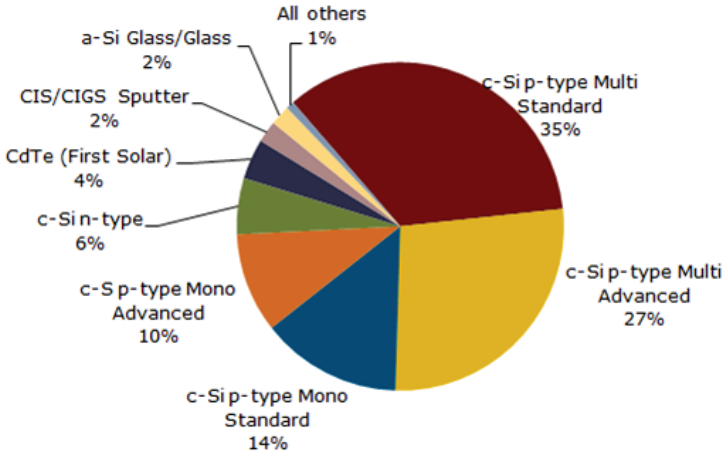


Figure 1.5 Prediction for 2014 for solar PV module production by technology [SolarBuzz 2013].

1.2 Motivation

Crystalline silicon homojunction solar cells currently account for over 90% of the module production in the PV market. A sketch of such a device is presented in Figure 1.6.

In 1954, the first solar cells based on a c-Si wafer with a pn-junction yielded an efficiency of 6% [Chapin 1954]. Since then, the efficiency has been increasing by improving the c-Si material quality, a better control of the junction formation, and development of passivating layers to prevent surface recombination of carriers (silicon oxide and silicon nitride stacks, SiO_x/SiN_x stacks) and of metal contacts with low contact resistivity. The design of the solar cell was also

optimized. However, further progress of this standard technology with regard to efficiency is limited by electron and hole recombining via defect states present at the contact between the absorber and the metal [Glunz 2007b, Swanson 2005]. Such recombination losses decrease the efficiency of the device by affecting the *FF* and particularly the V_{oc} of the devices. To address this problematic loss, two approaches have been developed: reducing the contact area fraction or passivating the contact.

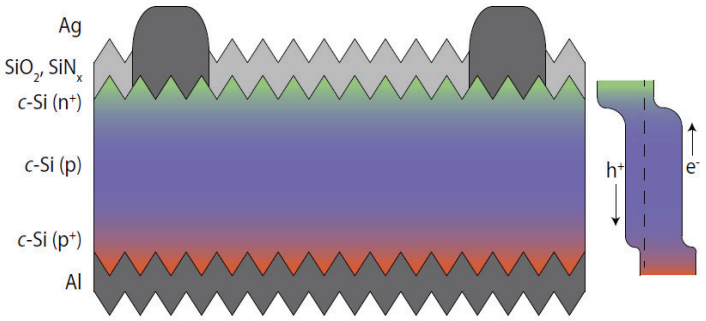


Figure 1.6: Schematic view of a homojunction solar cell. The green graded region indicates the presence of diffused phophorus atoms which form the pn-junction which separates the electron and holes and forms the electron collector. Conversely, the graded red region indicates the presence of boron atoms and forms the hole collector. The sketch on the right illustrates the energy band diagram of the structures and the current flow of electrons and holes. The front silicon dioxide (SiO_2) and silicon nitride (SiN_x) stack prevent recombination losses at the c-Si surface and enhance the light coupling in the c-Si absorber. We observe a direct contact between the absorber and the metal in this structure. Adapted from [De Wolf 2012c].

In the first approach, starting from a diffused-junction c-Si wafer, microelectronic techniques have led to efficiencies as high as 25% using a passivated emitter and rear locally diffused (PERL) structure [Green 2009, Zhao 1999]. A schematic view of this cell is shown in Figure 1.7 (a). This high efficiency was enabled mainly by engineering small local metal contacts with heavy doping underneath to minimize the contact resistance and the recombination losses by reducing one type of carrier at the defective semiconductor/metal interface. Outside the contacted region, first, a dielectric film passivates the c-Si surface by chemically reducing the number of interface states at the c-Si surface and also by introducing an internal electrical field, reducing the density of one type of carrier at the recombinative surface. Second, a lowly diffused c-Si region is used to prevent recombination losses induced by heavy doping at passivated surfaces. For such dielectric films, typically thermal SiO_2 is used for the highest-efficiency cells, while lower-temperature alternatives such as silicon nitride were developed for more industrial types of cells. These materials have low absorption coefficients in the visible range and thus low parasitic absorption. The approach for this structure relies on spatially decoupling the passivation and the contacting. The best geometrical trade-off must then be found [Cuevas 1996, Sterk 1994, Tous 2014]. Importantly, this structure results from 32 processing steps and cannot be scaled up to production lines. Industrial compatible structures then have lower efficiencies.

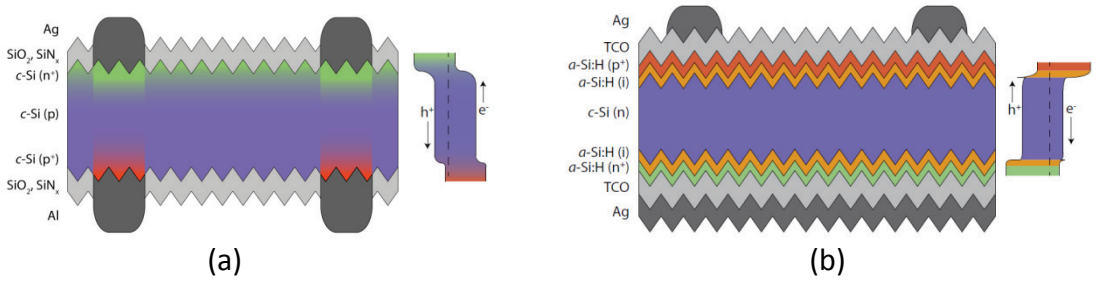


Figure 1.7: Schematic view of (a) a PERL homojunction and (b) an amorphous / crystalline silicon heterojunction solar cell with their respective band diagrams. Adapted from [De Wolf 2012c].

The second approach answered the contact-recombination issue by using an amorphous/crystalline silicon heterojunction (SHJ) which displaces the recombinative contact from the photo-electrically active c-Si wafer by the insertion of a wider bandgap hydrogenated amorphous silicon (a-Si:H) thin film [Taguchi 1990, Tanaka 1992]. In these cells, the emitter and back-surface field are formed by thin doped a-Si:H films sandwiching the c-Si wafer. As the electronic passivation properties of intrinsic a-Si:H are superior to those of doped films due to lower defect densities [De Wolf 2009], an intrinsic buffer layer a few nanometers thick is typically inserted between the c-Si surface and the doped a-Si:H films to improve the passivation even further. Physically, the passivation stems from hydrogenation of the c-Si surface states. A transparent conductive oxide (TCO) is sputtered on both sides for lateral transport of the charges and optical requirements, while metallization at the front and rear finishes the SHJ cell. A schematic view of this device is shown in Figure 1.7 (b). The full c-Si area is passivated with the a-Si:H and thus there is no direct contact between the c-Si absorber and the metal. This approach does not decouple passivation and contacting and, therefore, enables very high V_{oc} to build up. However, this structure has two main drawbacks. First, that the a-Si:H and TCO layers parasitically absorb light in the short (< 400 nm) and in the long wavelengths (> 1000 nm), respectively which decreases the J_{sc} [Holman 2012, Holman 2013a, Holman 2013b, Holman 2014]. To prevent these losses, back-contacted SHJs are being developed, which provide an interesting solution if low-cost patterning may be achieved. Second, the carrier transport through these contacts is not yet well understood, resulting in many low *FF* devices. Additionally, the process for SHJ solar cells is simple but requires both high-quality c-Si wafers and a stringent wafer cleaning procedure to achieve high-quality passivation.

The record efficiency of these two technologies is given in Table 1:2. As the engineering of the 25% homojunction cell requires non-industrial processes, we also add the record efficiency using industrial processes for a PERL cell as well as for a passivated emitter and rear totally diffused (PERT) cell on an n-type wafer, both of which give a benchmark for the homojunction industry. A difference of over 3% absolute in efficiency is observed between the record homojunction and the industrial-type homojunction, resulting from process differences. In the case of

silicon heterojunction solar cell, an industry, Panasonic, developed this technology and is leading the efficiency 'race'.

Table 1:2 Silicon homojunction [Green 2009, Zhao 1999] and heterojunction solar cells.

	V_{oc} (mV)	J_{SC} (mA/cm2)	FF (%)	Efficiency (%)	References
Record silicon homojunction (PERL)	706	42.7	82.3	25	[Green 2009]
Industrial compatible silicon homojunction (PERL)	676	40.6	79.4	21.8	[Benick 2009]
Industrial compatible silicon homojunction (PERT)	677	39.1	81.3	21.5	[imec 2014]
Record silicon heterojunction	750	39.5	83.2	24.7	[Taguchi 2014]
Record back-contacted silicon heterojunction	740	41.8	82.7	25.6	[Panasonic 2014]
Production line silicon heterojunction	740	39.5	80	23.4	[Panasonic 2013]

Table 1:3 summarizes the advantages and drawbacks of these two technologies. Combining the advantages of the structures, i.e. the low parasitic absorption of the homojunction cell and the passivating contacts of the SHJ cell, could enable higher efficiency solar cells to be achieved, as summarized in Table 1:3. Moreover, field-effect passivation induced by the dopant gradient in the c-Si wafer could reduce the sensitivity of the passivation on the surface impurities allowing for less stringent cleaning requirements and thus a more robust process compared to SHJ solar cell. The diffusion process also enables the use of less pure c-Si substrates due to gettering [Siffert 2004].

Table 1:3 Summary of the advantages and drawbacks of silicon homojunction, heterojunction and homo-hetero solar cells.

	V_{oc} (mV)	J_{SC} (mA/cm2)	FF (%)
Silicon homojunction	—	+	+
Silicon heterojunction	+	—	+
Homo-hetero solar cell	+	+	+

From a more scientific perspective, ideal passivating contacts should have the following properties:

(1) low recombination losses—characterized by the minority carrier recombination—,

(2) low contact resistance losses—unimpeded majority carrier transport—,

(3) optically low parasitic absorption in the none metalized regions.

These three contact properties are illustrated in Figure 1.8 and the relative position of the homojunction, heterojunction and ideal contacts indicated. Furthermore, we note that the ideal contact should also be easily implemented at industrial scale.

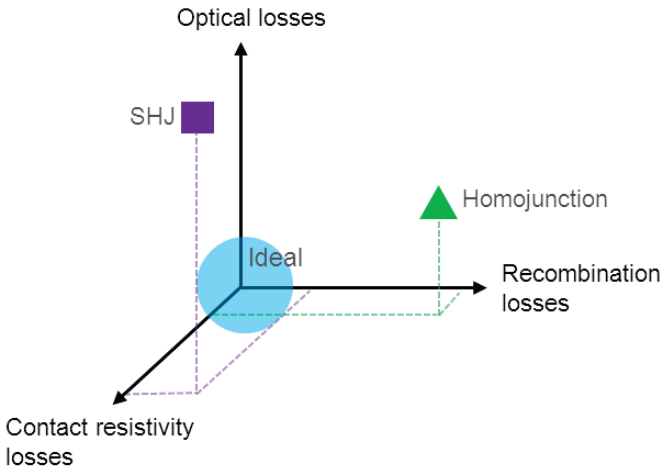


Figure 1.8: Schematic view of the three parameters determinant for contacts: recombination, optical and contact resistivity losses. The silicon heterojunction (SHJ) and homojunction contacts are approximatively positioned in this three-parameter space as well as the ideal contact.

1.3 Goal and structure

The goal of this thesis is to obtain the electronically ideal structure with optically ideal contacts by using the amorphous/crystalline silicon contacts on a homojunction structure and the homojunction passivation schemes between the contacts as sketched in Figure 1.9. For this reason, these novel devices are called homo-hetero solar cells.

The objective of this thesis is twofold. First, the scientific target is to develop and investigate the detailed properties of contacts used in SHJs solar cells and, based on this contact, to develop a novel type of contact on doped c-Si wafers. Second, the technological goal is to obtain passivating contacts for diffused-junction solar cells, enabling higher voltage devices, yielding higher V_{oc} values.

After this introduction, this thesis is composed of four main chapters.

Chapter 2 reviews the main theory needed for passivating contacts, namely contacting and passivation. This chapter then discusses the requirements for an ideal contact and presents the state-of-the-art for silicon-based passivating contacts.

Chapter 3 focuses on the experimental fabrication of homojunction solar cells. Three methods to induce a doping gradient in c-Si are presented. One of these methods consists of depositing doped homo-epitaxial film by low temperature plasma-enhanced chemical vapor deposition. An in-depth study discusses the growth conditions, the microstructure and electronic properties of such epitaxial films.

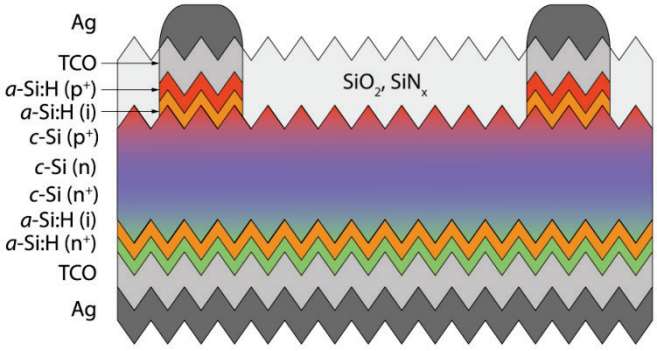


Figure 1.9: Schematic view of a passivating contact for homojunction solar cells using a-Si:H/c-Si hetero-interfaces.

Chapter 4 focuses on the properties of silicon heterojunction solar cells. After briefly reviewing the basic properties and fabrication of silicon heterojunction solar cells, we focus on the formation and characterization of their contacts. In particular, we report on damage of the amorphous silicon layers induced by sputtering the overlaying TCO. A damage-free process is developed which evidences recombination losses induced by the TCO work function.

Chapter 5 combines the developments of chapter 3 and 4. It investigates homo-hetero passivation and contacting properties. Using a specifically developed design, homo-hetero devices are demonstrated and optimized. The advantages and drawbacks are then examined. The homo-hetero solar cells show increased V_{oc} but lower *FF* compared to homojunction solar cells.

Chapter 6 summarizes and concludes this thesis.

1.4 Contribution to the research field

This thesis contributes to the research field of c-Si solar cells by presenting a novel passivating contact for homojunction solar cells. The main scientific outputs of this thesis are summarized hereafter.

In the study of homojunction formation, we developed epitaxial layers by low-temperature (≤ 180 °C) plasma-enhanced chemical vapor deposition (PECVD). Epitaxial growth enables precise thickness, doping and thermal-budget control, and hence advanced-design semiconductor devices. Moreover, homo-epitaxy simplifies the deposition of multi-layer passivating contacts, i.e. the doped c-Si layer forming the homojunction and the a-Si:H passivating layers, within a single deposition tool and without the need for high-temperature processes. For homo-epitaxial growth, we provide a model that depends only on the silane concentration in the plasma and the mean free path of surface adatoms to determine the growth mode. We then determine the precise conditions necessary to grow homo-epitaxial layers. We show that the presence of a persistent defective interface layer between the crystalline silicon substrate and the epitaxial layer stems not only from the growth conditions but also from unintentional contamination of

the reactor. Based on our findings, we determine the plasma conditions to grow high-quality bulk epitaxial films and propose a two-step growth process to obtain device-grade material [Demaurex 2014a].

Studying the amorphous/crystalline silicon contacts, we report on damage of the hydrogenated amorphous/crystalline silicon interface passivation during transparent conductive oxide sputtering. This occurs in the fabrication process of SHJ solar cells. We observe that this damage is at least partially caused by luminescence of the sputter plasma. Following low-temperature annealing, the electronic interface properties are recovered. However, the silicon-hydrogen configuration of the a-Si:H film is permanently changed, as observed from infrared absorbance spectra [Demaurex 2012]. This raises the question whether a sputter-free process could increase the efficiency of SHJ solar cells.

Consequently, we then present damage-free transparent-electrode deposition to fabricate high-efficiency amorphous silicon/crystalline SHJ solar cells. Using atomic layer deposition (ALD), we insert thin protective films between the amorphous silicon layers and sputtered contacts and investigate their effect on device operation. We find that a 20-nm-thick protective layer suffices to preserve, unchanged, the amorphous silicon layers beneath. We first confirm that the carrier lifetime decrease at low injection, often observed following TCO deposition, is linked solely to the deposited material and is process independent. Insertion of such protective atomic layer deposited layers yields slightly higher internal voltages at low carrier injection levels. However, we identify the presence of a silicon oxide layer, formed during processing, between the amorphous silicon and the atomic layer deposited transparent electrode that acts as a barrier, impeding hole and electron collection [Demaurex 2014b]. We eventually point out in which device structure ALD TCO layers would be necessary. This work also contributes to provide a method to analyse and understand the *FF* losses in SHJ solar cells: This method can be easily generalized to other passivating contacts.

Combining the homojunction and heterojunction technologies, we demonstrate the high quality passivation properties of a-Si:H on highly doped surfaces obtained by diffusion. We show that a-Si:H(i/n) stacks provide state-of-the-art surface passivation of phosphorus-doped surfaces. The optimal thickness of the amorphous layers is determined and, depending on the underlying dopant surface concentration, it may be reduced compared to a SHJ solar cell. To characterize the contact, we show that the contact resistivity may be determined using the transfer length measurement method. We find that, in most cases, the underlying diffusion provides a lower contact resistivity than an undoped wafer. Implementing these contacts in a test device, the optimized design yields a V_{oc} gain of 10 to 20 mV for dopant profile for homojunction solar cells. Even though a *FF* loss due to increased series resistance and non-ideal diode recombination losses overcomes the V_{oc} gain, these promising results open new perspectives for homojunction solar cells.

During this thesis, several internal and external collaborations contributed to the understanding of light-induced degradation of a-Si:H layers [De Wolf 2011, El Mhamdi 2014], to enhancing the efficiency of SHJ solar cells [Descoeudres 2011, Geissbühler 2013], to the development of passivating contacts with Bullock *et al.* from ANU [Bullock 2014a, Bullock 2014b, Bullock 2014c], to the doping of sputtered amorphous silicon layers with Zhang *et al.* from ANU [Zhang 2014] and to the passivation of nanowires using different materials [Dalmau Mallorqui 2014]. These results will not be discussed in this report, however.

Chapter 2 Contacts and passivation in solar cells

This chapter presents the key theoretical elements necessary for this thesis: contacts and passivation. First, it reviews the fundamental contact types: metal-semiconductor (ohmic and Schottky) and metal-insulator-semiconductor. Second, it reports recombination processes in semiconductors and passivation schemes at their interfaces. Third, the direct impact of contacts and passivation on the properties of solar cells is discussed. Finally, a literature review of passivating contacts is presented.

2.1 Introduction

Fundamentally, a solar cell consists of a light-absorbing semiconductor with two selective contacts that extract only holes on one side of the device and only electrons on the other. Ideally, under illumination, neither limitation in current nor recombination would occur at these contacts, implying: (1) the contact resistivity of these contacts should be low and (2) recombination of photogenerated carriers at the contacts should be prevented by passivation of the interface defects. These contacts would be called *passivating contacts*.

In this chapter, we will first discuss how contacts with the lowest contact resistivity can be engineered and what are the difficulties encountered. Second, after a short review of recombination paths in bulk semiconductors and at their surfaces, the schemes to prevent recombination will be discussed. The methods to characterize passivation quality will then be described. In a third part, the impact of contacts and passivation on solar cell performance will be discussed. The trade-off between passivation and contact resistance for homojunction contacts will be discussed and compared to heterojunction contacts. Finally, an overview of the state-of-the-art contacts in silicon solar cells is presented.

The goal of the theoretical part of this chapter is not to provide an exhaustive list of the processes involved in contact formation and passivation but rather to highlight a few properties that are essential for the concept and devices presented in this thesis. For a comprehensive review of semiconductor properties, the reader is referred to [Kittel 2005, Sze 2002, Sze 2006, Würfel 2008].

2.2 Contacts

In this section, metal-semiconductor and metal-insulator-semiconductor contacts are discussed. Here, we review the necessary points for the understanding of this thesis.

2.2.1 Metal – Semiconductor contacts

The formation of a metal-semiconductor (MS) contact is crucial for most electronic devices. In Figure 2.1, the energy band diagrams of a metal and an n-type semiconductor without any interaction are drawn.

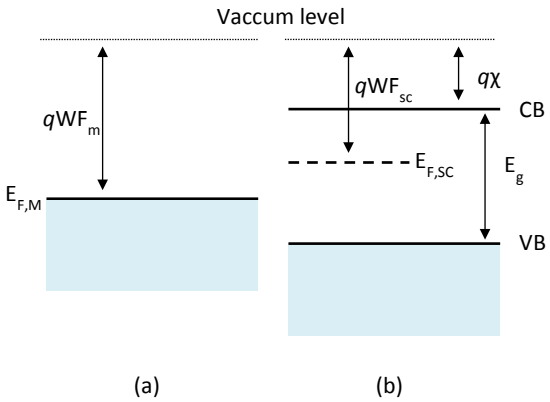


Figure 2.1: Band diagrams of (a) a metal and (b) a semiconductor without any interaction.

In a metal, the delocalized electronic states responsible for conduction are around its Fermi level ($E_{F,M}$) and the energy difference between the vacuum level and $E_{F,M}$ is the metal work function (WF_M). Conversely, in a semiconductor of bandgap E_g between the conduction band (CB) and valence band (VB), these states are located near the CB minimum, at an energy equal to the difference between the semiconductor work function (WF_{SC}) and the semiconductor electron affinity (χ) from the semiconductor Fermi level ($E_{F,SC}$). If no interaction between the two materials occurs, the energy offset between WF_M and WF_{SC} becomes the Schottky barrier height Φ_{Bn} (Φ_{Bp}), according to the Schottky-Mott rule [Schottky 1942]. The Schottky barrier height is crucial: it acts as a potential barrier and determines the electrical characteristic of the MS interface [Sze 2002]. However, the Schottky-Mott rule is rarely confirmed by measurements: at this interface, new electronic interface states may form, and the charge distribution will likely differ from the superposition of the charge distribution at the metal and semiconductor original surface [Tung 2014]. These rearrangements may lead to barrier heights that are mostly independent of WF_M. This effect is known as Fermi level pinning [Tung 2014]. Typical energy band diagrams of a metal in contact with an n-type and a p-type semiconductor are drawn in Figure 2.2.

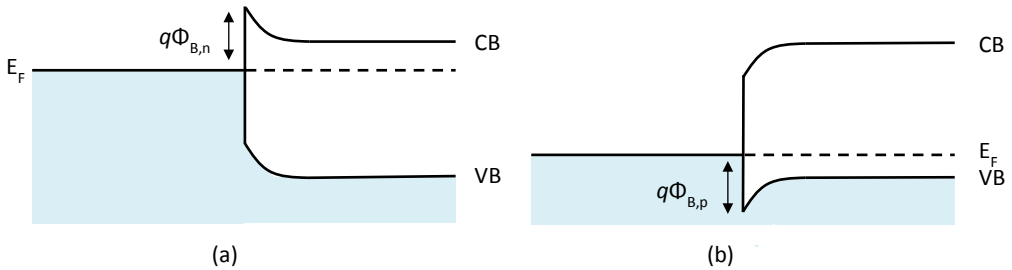


Figure 2.2: Energy band diagrams of the interface between a metal and a semiconductor (a) n-type and (b) p-type.

In a metal, the screening length is assumed to be small, whereas in a semiconductor the depletion-layer width *w* is given by

$$w = \sqrt{\frac{2\epsilon_s\,(V_{bi}-V)}{qN_D}} \qquad (1)$$

where ϵ_s is the dielectric permittivity, V_{bi} the difference between the semiconductor and metal work function, V the applied voltage and N_D the donor concentration [Sze 2002].

2.2.1.1 Schottky contacts

Schottky contacts are the most common contacts. In such a contact, the flow of electrons between the semiconductor and the metal is easier in one direction than in the other. This is known as a rectifying behavior. The current is dominated by the majority carriers and this contact is then unipolar. The main transport mechanism is thermionic emission of majority carriers over the potential barrier into the metal. Thus, the current flowing in a Schottky contact is given by [Schubert 2006]:

$$J_{thermionic\ emission} = A^* T^2 e^{\frac{-q\Phi_B}{kT}} \left(e^{\frac{qV}{kT}} - 1\right) \qquad (2)$$

where A^* is the effective Richardson constant, *q* the elementary charge, *k* the Boltzmann constant and *T* the temperature. This non-linear current is determined, for a given material, by the barrier height and the temperature.

2.2.1.2 Ohmic contacts

Ohmic contacts are defined as contacts in which carriers can flow over the junction in the two directions with negligible contact resistance compared to the bulk or series resistance of the semiconductor [Sze 2002, Yu 1970]. Consequently, they have a linear *JV* dependence and a voltage-independent resistance. Such contacts can be achieved by: (1) a low Schottky barrier height—thermionic emission is then efficient to overcome the small barrier height (Figure 2.3(a))—or (2) decreasing the depletion region width *W* in such a way that carriers can tunnel by thermionic-field emission or field emission through the thin barrier at the interface (Figure

2.3 (b)) [Schroder 1984]. The tunneling probability in a square barrier potential of width *L* is reduced exponentially with *L* and the square root of the barrier height [Cohen-Tannoudji 2005, Sze 2002]:

$$J_{(thermionic-)field\ emission} \sim e^{-2L\sqrt{\frac{2m_n(q\Phi_B - qV)}{\hbar^2}}} \sim e^{-\frac{(\Phi_B - V)}{\sqrt{N_D}}} \qquad (3)$$

where m_n is the effective mass, N_D is the donor concentration and $\hbar$ reduced Planck constant.

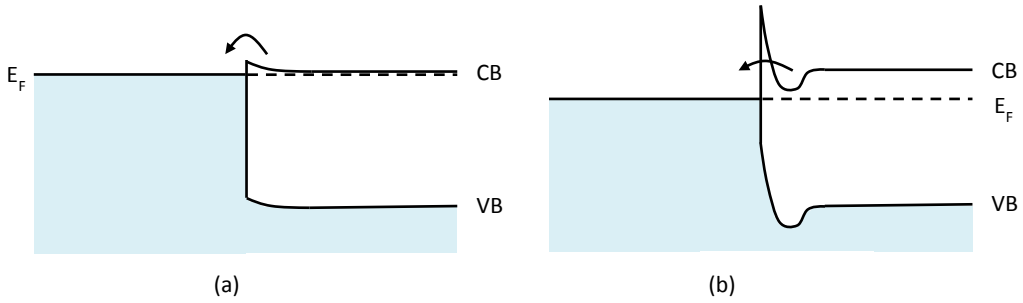


Figure 2.3: Energy band diagrams of the two types of ohmic contact: (a) reduced barrier height and (b) reduced barrier width.

2.2.2 Metal – Insulator – Semiconductor contacts

The insertion of a thin insulator between the metal and the semiconductor modifies the interface structure of the MS junction. Metal-insulator-semiconductor (MIS) contacts are typically used to reduce the contact resistivity of pinned MS interfaces by several mechanisms as discussed by Roy [Roy 2012]: First the E_F is depinned by reduction or passivation of the interface defects, then the Schottky barrier can be reduced by interface dipoles and fixed charge in the insulator or at its interfaces. In such contacts, the main charge transport through the insulator under standard operating conditions is by tunneling [Sze 2006]. As the tunneling probability depends mainly on the barrier width, the barrier thickness should be well controlled and narrow (in the nanometer range) [Green 1974]. For this contact, the best trade-off must be found between the added resistance induced by charge tunneling through the insulator and the reduced resistance resulting from the lowered Schottky barrier height [Roy 2012].

The insulator is often a dielectric but may also be a semiconductor such as amorphous silicon (a-Si:H) as in the case of silicon heterojunction devices. Then, depending on the semiconductor film's characteristics, the transport mechanisms may change. As an example, in a-Si:H layers, transport may occur by conduction in the extended states around the band edges, activated or variable range hopping [Le Comber 1972, Le Comber 1970, Mott 1968, Mott 1969]. The a-Si:H film may, thus, be much thicker than an insulating film in MIS contacts [Bullock 2013, Bullock 2014c].

Under zero bias, depending on the metal-to-insulator barrier height, two different situations may occur, as drawn in Figure 2.4: (a) The metal-to-insulator barrier height is low, and the

semiconductor's surface is in accumulation. The *JV* characteristics differ from those of an ideal diode under reverse bias and the majority-carrier current dominates the structure [Green 1974]. (b) The metal-to-insulator barrier height is high, and the semiconductor's surface is inverted. Its *JV* curve is similar to that of an ideal diode and the minority-carrier current dominates the structure. The latter case is used to form solar cells and will be discussed in section 2.5.2 [Green 1974, Shewchun 1974].

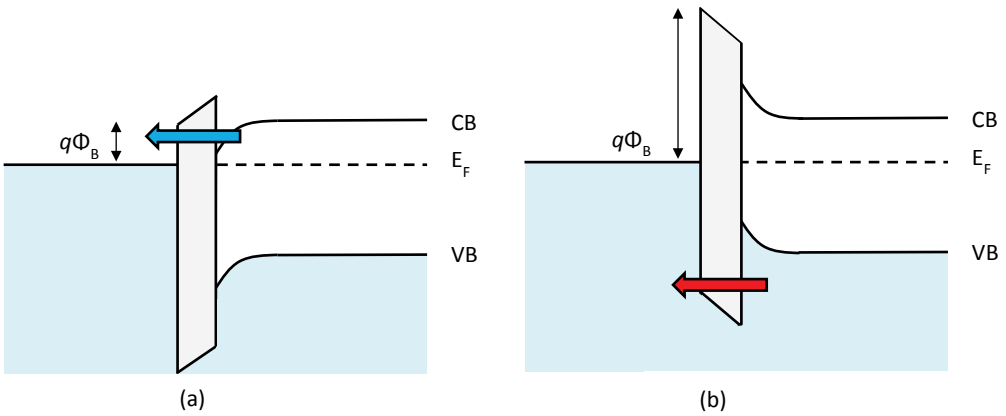


Figure 2.4: Energy band diagrams of ideal MIS diodes in (a) accumulation condition in which the majority-carrier current dominates and (b) inversion condition in which the minority-carrier current dominates.

2.2.3 Characterizing the contact and dependence on doping

Generally, for a MS and MIS contact, the current transport is characterized by its specific contact resistivity, ρ_c, which is defined as [Yu 1970]

$$\rho_c = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \quad \Omega cm^2. \qquad (4)$$

The contact resistivity must be minimized throughout the full current range of interest. Figure 2.5 illustrates the contact resistivity dependence on the crystalline silicon (c-Si) wafer doping concentration for a c-Si(n)/platinum contact. We observe that to obtain low resistivity values (thermionic-) field emission must be efficient, implying that a thin barrier and thus a high doping concentration of the underlying c-Si are required.

2.3 Recombination losses and passivation

In solar cells, as well as in other devices such as bipolar transistors, the minority-carrier lifetime is crucial: generated (or injected) electrons and hole recombining in the semiconductor bulk and at its surfaces result in a direct loss of carriers which affects the device properties. As nowadays high-quality wafers are available, the dominant paths of carrier recombination are often in regions of high carrier concentration (either by doping or carrier injection) and at the c-

Si surface states. To avoid severe losses at the surfaces or interfaces, the active surface states need to be "passivated." Two passivation schemes exist: reducing chemically the number of defect states or reducing the number of one type of carriers available for recombination processes.

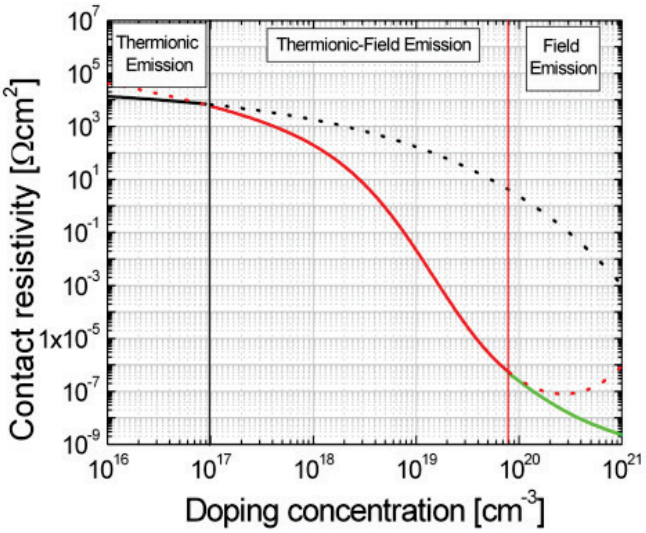


Figure 2.5: Contact resistivity versus doping concentration for an n-type crystalline silicon wafer in contact with platinum. The Schottky barrier height is Φ_B = 0.78 eV. Graph reproduced from [Schubert 2006].

In this section, the basics of recombination processes and passivation schemes relevant for this thesis will be discussed. The measurement technique used in this thesis to characterize the carrier lifetime is described, as well.

2.3.1 Recombination processes

The recombination processes are separated between bulk recombination and surface recombination.

In semiconductor physics, the carrier lifetime, τ, is the average time between generation and recombination. Several recombination paths exist and will be described in this section. They are characterized by a recombination rate, *U*, per unit volume and per second ($cm^{-3}s^{-1}$). If charge trapping and electric fields are negligible, the excess concentration of holes (Δp) and electrons (Δn) are equal. The lifetime and the recombination rate are then related by

$$\tau = \frac{\Delta n}{U}. \qquad (5)$$

Bulk recombination

In bulk semiconductors, there are three recombination processes: radiative recombination, Auger recombination and recombination via defect states. The two first processes are intrinsic to the semiconductor and occur also in defect-free semiconductors. Conversely, the third re-

combination process is extrinsic and depends on the presence of contaminants and defects in the lattice. These processes are illustrated in Figure 2.6.

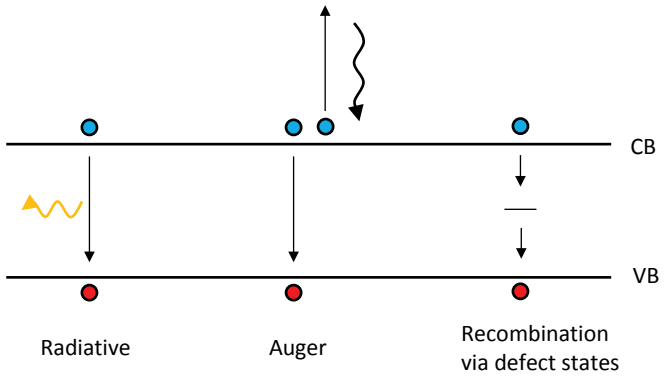


Figure 2.6: Recombination processes occurring in bulk semiconductors.

Radiative recombination involves an electron recombining with a hole. The excess energy is emitted as a photon, which has the energy of the material bandgap. The radiative recombination rate is given in [Trupke 2003]. As c-Si has an indirect bandgap, radiative recombination is several orders of magnitude lower than for a direct semiconductor, as a phonon needs to be involved to conserve momentum [Varshni 1967]. This recombination mechanism is not the dominating recombination process in silicon solar cells. Interestingly, as the photon emitted in radiative recombination has a narrow energy range close to the c-Si bandgap, it may be used in photoluminescence imaging to monitor the c-Si wafer quality and handling issues [Trupke 2006]: high luminescence intensity indicates the absence of other recombination mechanisms. This technique is part of the routine check for all c-Si based samples.

Band-to-band Auger recombination is a three-particle process: the excess energy and momentum resulting from a recombination of an electron with a hole, is transferred to a third free charge carrier (hole or electron), which then thermalizes by emitting phonons. An empirical formula is generally used in the silicon photovoltaics community, as the theoretical formula only approximately describes the reality due to Coulomb-correlation-enhanced recombination rates [Beattie 1959, Dziewior 1977]. A recent derivation of this empirical expression is given in [Richter 2012], which is an update to earlier work [Altermatt 1997, Dziewior 1977, Kerr 2003, Sinton 1987]. Auger recombination is effective in the presence of high carrier concentration, such as in highly doped silicon. Importantly, the carrier lifetime can also be Auger limited in lowly doped silicon. This will be the case under high-injection conditions, which is a relevant problem for many high-efficiency solar cells.

A recombination event via a defect state is a two-step process with successive capture of free charge carriers into the defect state. The excess energy can be emitted as a photon or phonons. It is commonly described by the statistical Shockley-Read-Hall (SRH) formalism [Hall 1952, Shockley 1952]. The SRH recombination rates depends on the density of traps, on the capture

cross section of the traps for electrons and holes, on the occupation probability of the trap state and on the trap energy [Aberle 1999, Schulze 2011a]. For the latter point, the recombination rate, for similar values of capture cross sections, is the highest if the trap states lie close to mid-gap, as illustrated in Figure 2.7. Typically, for c-Si materials, a detrimental recombination center results from iron contamination.[1] Typical concentrations of iron are in the 10^{11} cm^{-3} range [Macdonald 2008]. For the float-zone (FZ) n-type material from Topsil[2] used in this thesis, the exact density is not known, however, it is less than 10^{12} cm^{-3} (0.1 particle per billion atoms), which is the detection limit of neutron activation analysis measurements used by Topsil.

The total bulk lifetime is then given by

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{Radiative}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}}. \qquad (6)$$

In Figure 2.7, the excess carrier density dependence of the separate and total bulk recombination processes is plotted for two trap energy levels. We observe the Auger recombination restricts the lifetime at high injection whereas SRH recombination limits the low injection region.

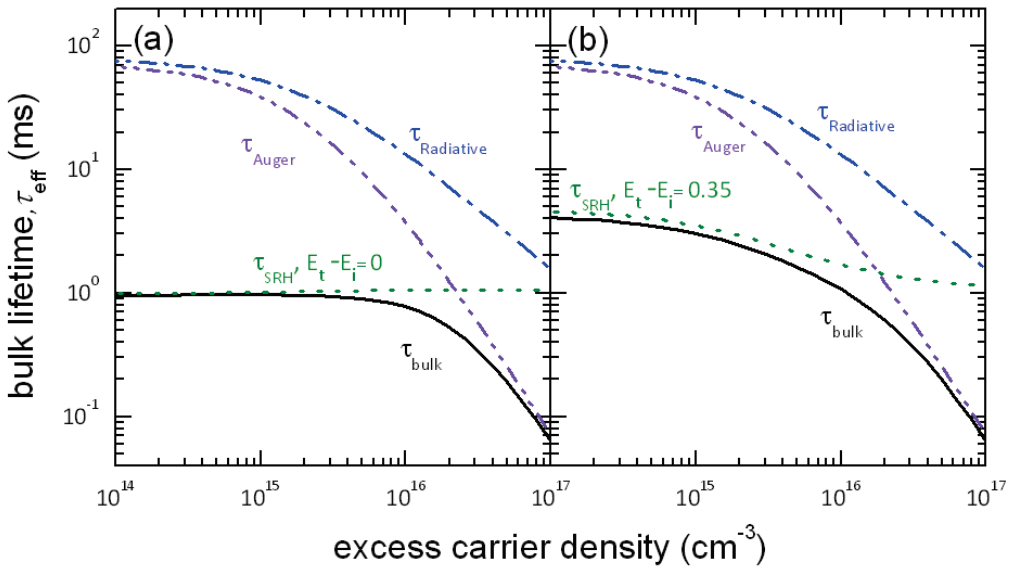


Figure 2.7: Injection dependence of the bulk lifetime in a 2.4 Ωcm n-type c-Si wafer resulting from the three bulk recombination mechanisms: radiative, Auger and SRH recombination. The SRH curve was calculated for a capture cross section of electrons (holes) of 1.5 10^{-15} cm^2 (1.5 10^{-16} cm^2) for a (a) deep (the trap energy, E_t, equal to the intrinsic Fermi level, E_i) and (b) shallow defect (E_t is above the E_i by +0.35 eV) with a trap density of 4 10^{11} cm^{-3}.

[1] For Czochralski-grown (CZ) p-type wafers, the boron-oxygen complex is also a major SRH recombination center.
[2] www.topsil.com

Surface recombination

At a semiconductor surface, the discontinuity in the covalent bond network is a source of defect states, known as dangling bonds (DB). For silicon, these states are around the middle of the bandgap and are thus efficient recombination centers. A surface recombination rate per unit area and time ($cm^{-2}s^{-1}$), U_S, is used and the surface recombination velocity S (cms^{-1}) is then defined as

$$U_S = S\,\Delta n_S \qquad (7)$$

where Δn_S is the excess minority-carrier concentration at the surface itself [Schroder 2006]. However, as a result of electrical charges at the silicon surface, in an overlaying film or due to band alignment requirements with an overlaying film, a surface potential may be present, yielding the energy bands to be bent (i.e. not flat) at the wafer's surface. A space charge region of width *d* then exists. In this case, an effective surface recombination, S_{eff} , may be defined according to

$$S_{eff} = \frac{U_{x=d}}{\Delta n_{x=d}} \qquad (8)$$

where U_d and Δn_d are taking at the edge of the space charge region (at a distance *d* from the surface), i.e. in the field-free wafer [Aberle 1999].

Recombination through surface states is calculated similarly to the SRH formalism but the states are integrated over the bandgap [Sproul 1994]. Moreover, in the case of amphoteric defects which can accommodate three charge states as in a-Si:H and as assumed at the a-Si:H/c-Si hetero-interface, this formalism is modified: two different energy levels are relevant for the treatment of the recombination statistics [Olibet 2008, Schulze 2011a].

2.3.2 Characterizing the recombination losses

There are two major quantities that are used to characterize the recombination losses.

1. The effective lifetime

The effective lifetime, τ_{eff} , of a symmetric sample includes all the recombination in a sample and is defined by [Schroder 2006]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + D\beta^2 \qquad (9)$$

where *D* is the minority carrier diffusion constant and β is found from the relationship

$$\tan\left(\frac{\beta W}{2}\right) = \frac{S_{eff}}{\beta D} \qquad (10)$$

with *W* the wafer thickness. This equation then simplifies to

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \qquad (11)$$

when S_{eff} is sufficiently small so that the tangent function may be linearly approximated, i.e. *tan(x) = x* [Schroder 2006]. If the S_{eff} is too large, the diffusion of the carriers to the surface will limit the effective lifetime.

Throughout this thesis, we will be using τ_{eff} as a parameter to monitor the active defects in our samples with no doping gradients in the c-Si wafer.

2. The recombination current density prefactor, J_0

In the case of dopant profiles below the wafer surface, the recombination current density prefactor, J_0 (Acm^{-2}), also known as the saturation current density, is typically used to characterize the electronic quality of this doped region, based on the standard diode equation [Aberle 1999, Cuevas 2014]. Combining this diode equation with continuity equations and assumptions described in Ref. [Jain 1981], a relation linking the effective surface recombination velocity and the recombination current density prefactor can be derived [Aberle 1999].

$$S_{eff} = \frac{J_0 N_{Dopant}}{q n_i^2} \qquad (12)$$

where q is the elementary charge, n_i the intrinsic carrier concentration and N_{Dopant} the dopant concentration. Kane and Swanson generalized this equation using the injection-level dependence of lifetime to [Kane 1985]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2J_0(n_0 + \Delta n)}{q n_i^2 W}. \qquad (13)$$

This J_0 parameter takes into account Auger, bulk SRH and surface recombination in the highly doped region [Cuevas 2014]. It will be used to characterize the recombination losses in wafers with a dopant profile.

The next section will report how to experimentally access these quantities.

2.3.2.1 Quantifying the passivation quality

Before reviewing the concrete impact of passivation in devices, we present a simple and fast method to experimentally evaluate τ_{eff} and J_0 using an instrument developed by Sinton and Cuevas based on a photoconductance decay measurement [Sinton 2013, Sinton 1996a, Sinton 2000, Sinton 1996b]. The basic operating principle of this instrument is as follows: the photoconductance induced during and after a light pulse is monitored by a calibrated eddy-current conductivity sensor. Assuming $\Delta n = \Delta p$, it can then be converted into a carrier density:

$$\Delta n = \frac{\Delta \sigma}{q W \mu} \qquad (14)$$

where $\Delta\sigma$ is the variation in the conductivity, μ is the sum of the electron and hole mobilities in silicon and W the wafer thickness.

The generalized formula, derived by Nagel *et al.* [Nagel 1999], then properly performs the data analysis under transient, in which the generation is negligible ($G = 0$), and quasi-steady-state (QSS, $\frac{d\Delta n(t)}{dt} = 0$) conditions:

$$\tau_{eff} = \frac{\Delta n}{G - \frac{d\Delta n(t)}{dt}}. \qquad (15)$$

In the QSS measurement mode, the coupling of light into the sample is important and must be taken into account by using the optical constant. It can, for example, be adjusted by comparing the transient and QSS measurements.

The same measurement can also be used to access the recombination current prefactor J_0, according to the method described by Kane and Swanson [Kane 1985]. Even though J_0 is commonly used to evaluate the passivation quality of homojunction emitters, recent publications still focus on this parameter [Cuevas 2014, Mäckel 2013, McIntosh 2014]. To enable comparison with the literature, in this thesis we will use its most common determination method [Sinton 1996b].

The measurement of photoconductance decay cannot be performed on metallized samples if the metal layer is thicker than a few nm (up to 20 nm in case of silver) because the eddy current generated in the metal parts of the samples cancels the magnetic field. However, by suns-V_{oc} measurements, which under illumination directly measure the external voltage changes generated in the sample by the excess carrier concentration, similar quantities as discussed above can be obtained [Sinton 2000].

This powerful technique will be further discussed in section 2.4.2.

2.3.3 Passivation of interface defects

2.3.3.1 Chemical and field-effect passivation

Recombination through defects at the surface is often a major limitation in solar cells, as the surface state density of non-passivated silicon is measured on the order of 10^{13} cm^{-2} [Aberle 1999]. Two schemes can reduce this loss:

1. Chemical passivation of the dangling bonds, by which the number of defects is reduced, for instance by terminating the dangling bonds with a hydrogen atom [Higashi 1990, Yablonovitch 1986].
2. Field-effect passivation, in which the number of defects stays constant but the probability of recombination via the defect state is reduced by decreasing the minority-carrier density. This effect is introduced, when two materials are in contact, either by band alignments induced by different materials' work functions or by fixed charges near the interface.

These two schemes are illustrated in Figure 2.8. In practice, the two schemes are often combined.

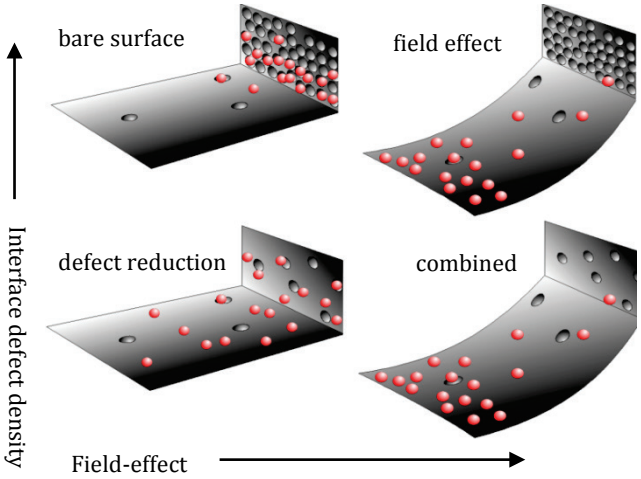


Figure 2.8: Illustration of chemical and field-effect passivation. Reproduced from [Hofmann 2008].

The lifetime data as a function of excess carrier density can be fitted using a model developed by Girisch *et al.* [Girisch 1988] and adapted for a-Si:H by Olibet *et al.* [Olibet 2007]. The two major model parameters are the surface dangling-bond density and the fixed-charge density. Lifetime measurements provide a means to determine whether the passivation of tested samples relies on chemical passivation or field-effect passivation. The limitations of this model, principally based on simplifications by Hubin *et al.* [Hubin 1992], have been established in [Li 2008]. Other models have also been developed [Leendertz 2010, Steingrube 2010]. Unfortunately, for diffused-junction c-Si substrates, the model developed by Olibet *et al.* is not valid (it does not include Auger recombination) [Olibet 2007].

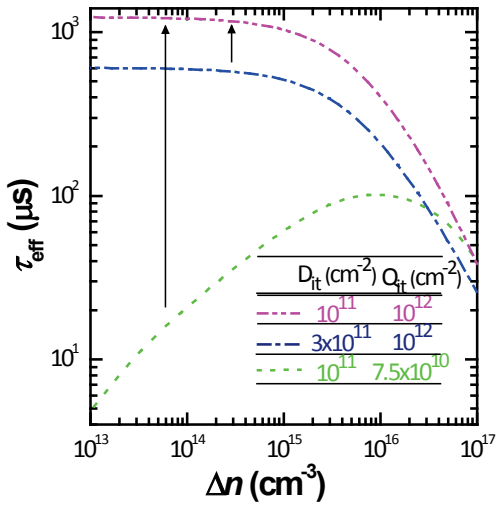


Figure 2.9: Effect on the minority-carrier lifetime (τ_{eff}) as a function of the carrier concentration (Δn). The effect of the reduction of the number of interface states D_{it} (green to pink curve) and of the increase of the effective charge at the interface (Q_{it}) leading to a field-effect passivation is illutrated [De Wolf 2012a].

In Figure 2.9, an illustration of the effect of chemical passivation and field-effect passivation for a-Si:H is plotted using this model [Olibet 2007]. We point out that the lifetime decrease in low carrier injection may also indicate sample edge effects [Kessler 2012, Veith 2014].

2.3.3.2 Dependence of the passivation on doping

Empirically, the surface recombination velocity S depends on the surface dopant density, N_S, according to [Cuevas 1996]:

$$S = N_S \, 10^{-16} cm^4 s^{-1} \qquad (16)$$

However, as the surface dopant density requires sophisticated methods to be determined, the sheet resistance which can be easily determined by four-point measurements is usually plotted instead. The relation between the surface doping concentration and the sheet resistance is, in the case of a uniform doping profile of thickness t and resistivity ρ simply given by $R_{SH} = \rho/t \approx 1/qN_s\mu t$, where μ is the mobility of the majority carriers. Figure 2.10 is a typical graph showing J_0 as function of the sheet resistance.

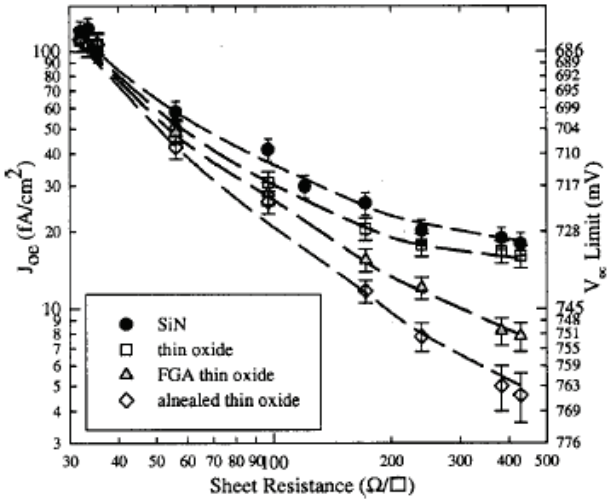


Figure 2.10: Comparison of the emitter J_0 (J_{0e}) of phosphorus-diffused, planar emitters passivated with plasma-enhanced chemical vapor deposition silicon nitride (SiN_x) and thin thermal silicon oxides (SiO_2) with forming gas anneal (FGA) and an alneal treatment, where an aluminum layer is evaporated onto the thermal oxide prior to annealing. Reprinted with permission from [Kerr 2001]. © 2001 American Institute of Physics.

2.3.3.3 State-of-the-art passivation

The best-known passivating layers in the silicon photovoltaics community are composed of dielectric layers such as SiO_2, SiN_x, stacks of SiO_2 and SiN_x, aluminum oxide (Al_2O_3) and of a-Si:H. In all these materials, chemical passivation is achieved by hydrogen termination. The properties of these layers and the associated references are shown in Table 2:1.

2.4 Contacts, passivation and solar cells

In this section, we investigate the impact of the contact resistance and of the passivation quality on the cell characteristics.

Table 2:1: The main passivating materials and their characteristics. The a-Si:H density of interface states and the equivalent charge are extracted from fits using the model described in [Olibet 2007], based on the highest lifetime obtained: τ_{eff} = 22 ms, corresponding to S_{eff} = 0.7 cms^{-1}.

Material	Chemical passivation: density of interface states	Field-effect passivation: Equivalent charge	Characteristics	References
HF	negligible	-	Passivation not necessarily stable	[Yablonovitch 1986]
SiO_2	$<10^9$ cm^{-2}	Positive charge $5\cdot10^{10}$–$2\cdot10^{11}$ cm^{-2}	Dielectric, high-temperature (<1000 °C)	[Aberle 1999, Deal 1965, Zhao 1998]
SiN_x	10^{11}–$5\cdot10^{12}$ $cm^{-2}eV^{-1}$ at mid gap	Positive charge 10^{11}–$5\cdot10^{12}$ cm^{-2}	Dielectric, efficient anti-reflective coating	[Aberle 1999, Lanford 1978, Lauinger 1996]
SiO_2/SiN_x			a-SiN_x:H hydrogenates and stabilizes the Si/SiO_2 interface	[Aberle 1997, Chen 1993]
Al_2O_3	$<10^{11}$ $cm^{-2}eV^{-1}$	Negative charge -10^{11}–-10^{13} cm^{-2}	Dielectric, SiO_2-like interface (1–2 nm), a-SiN_x capping layers may also be used	[Agostinelli 2006, Dingemans 2012, Hoex 2006]
a-Si:H	$<10^7$ cm^{-2}	10^7–10^{12} cm^{-2}	Semiconductor, extended states conductivity at 25 °C	This thesis

2.4.1 Basic properties of solar cells

As plotted in Figure 2.11(a), solar cells are characterized by

- Open-circuit voltage (V_{oc}), which indicates the ability of the device to maintain the carrier density when no current is flowing. The V_{oc} is determined by recombination losses.
- Current under short-circuit condition (J_{sc}), limited by optical losses.
- Fill factor (*FF*), evidencing the losses due to recombination, series resistance (R_s) and shunt resistance (R_{sh}).

Combined, these parameters yield the efficiency η,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{oc}J_{sc}FF}{P_{in}} \qquad (17)$$

where P_{out} and P_{in} are, respectively, the output and input power.

The equivalent circuit of a solar cell is shown in Figure 2.11(b). The diode equation under illumination with parasitic resistance is then given by

$$J = J_L - J_0\left(e^{\frac{q(V+JR_S)}{nkT}} - 1\right) - \frac{V+JR_S}{R_{sh}} \qquad (18)$$

where J_L is the photogenerated current. This model provides a simplified view of a solar cell, as the ideality factor *n* is assumed to be independent of voltage. This is generally not observed in solar cells, and a two-diode model is typically used instead.

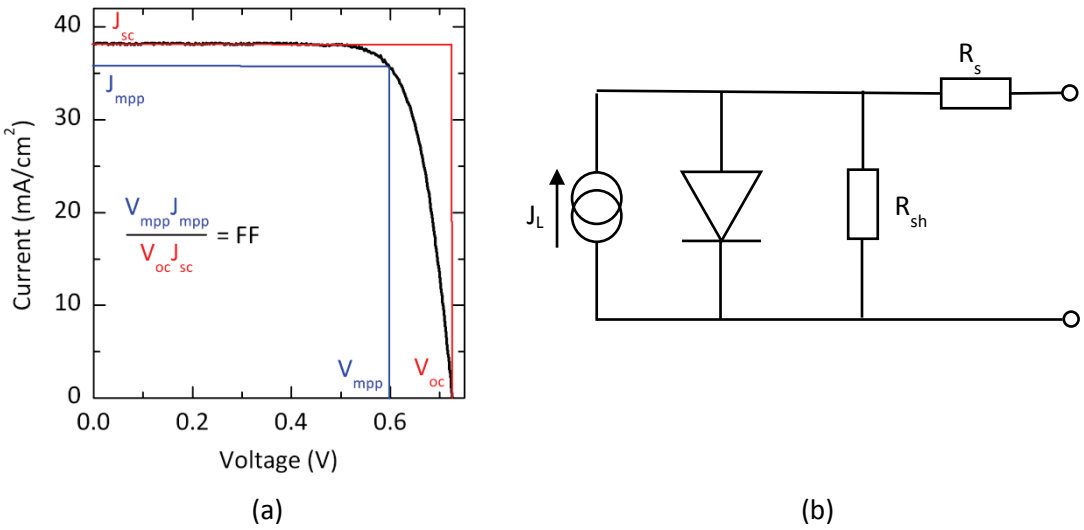


Figure 2.11: (a) Illuminated current-voltage characteristic of a solar cell and (b) equivalent circuit of a solar cell.

2.4.2 Influence of recombination and contacts on cell characteristics

We now focus on the effect of τ_{eff} and contact resistance on cell characteristics.

- **τ_{eff} impacts V_{oc} and *FF*.**

The internal voltage of a solar cell is directly linked to the splitting of the quasi-Fermi levels (E_{F_n} and E_{F_p}) in the devices, which describe the population of carriers in the conduction and valence bands (n and p, respectively). Assuming $\Delta n = \Delta p$, the difference in population between the conduction band and the valence band will diminish with recombination and consequently the internal voltage, V_{int}, will decrease according to

$$qV_{\mathrm{int}} = E_{F_n} - E_{F_p} = kT \ln\left(\frac{np}{n_i^2}\right) = kT \ln\left(\frac{(n_0+\Delta n)\Delta n}{n_i^2}\right) \qquad (19)$$

where $n = n_0 + \Delta n$ (analogous for p), n_0 and p_0 are the carrier densities at equilibrium (in dark condition) and we assume that $n_0 \gg p_0$ for an n-type wafer.

Furthermore, the excess carrier density is related to the effective minority-carrier lifetime τ_{eff} by

$$\Delta n = \frac{\tau_{\mathrm{eff}} U_{\mathrm{bulk}}}{1 - \tau_{\mathrm{eff}} \frac{(S_{\mathrm{front}} + S_{\mathrm{back}})}{W}} \qquad (20)$$

where U_{bulk} is the bulk recombination rate. Combining these two relations, τ_{eff} is shown to dictate the internal voltage of the solar cell. A lifetime limited by bulk recombination mechanisms must then be aimed for at all injection levels.

Using photoconductance measurements (see section 2.3.2), the excess carrier density may be accessed by equation 14. Then, using equation 19, the internal voltage of the cell may be obtained at various carrier injection level. As the sample is measured in open-circuit condition, this voltage is generally referred to as the implied-V_{oc}. Moreover, using a calibrated photodiode next to the measured sample and exposed to the same light pulse, each illumination intensity may be related to an effective sun and to a carrier injection level. Assuming a short-circuit for the sample and applying the superposition principle , an implied-*J* can be determined for each voltage, according to implied-*J* = J_{sc}*(1-*effective suns*). Thus, we now have an implied-V_{oc} and implied-*J* for various injection level. Therefore, an implied-*JV* curve may be plotted, as illustrated in Figure 2.13, and a maximum power point (MPP) determined [Sinton 1999]. This implied-*JV* curve is limited by recombination losses and resistance-free as no carrier transport occurs during this measurement. Importantly, the implied-V_{oc} provides at an injection level corresponding to one sun illumination, an upper limit to the device V_{oc}. Conversely, at an injection level corresponding to the MPP, an implied-*FF* can be computed, which, as it is series resistance-free, highlights the *FF* limitations due to recombination. Figure 2.12 illustrates, on a lifetime curve, the injection-level corresponding the implied-V_{oc} at one sun and to the implied-V_{oc} at MPP.

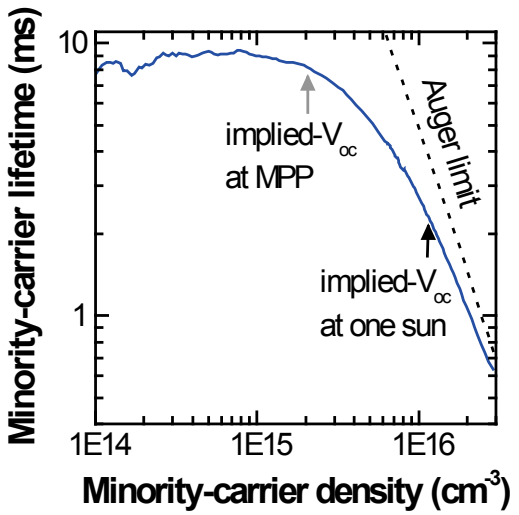


Figure 2.12: Lifetime of a silicon heterojunction solar cell precursor after deposition of the a-Si:H layers with the lifetimes corresponding implied-V_{mpp} and implied-V_{oc}.

An analytical expression can be derived linking the *FF* to the V_{oc}, which gives an upper limit to the *FF* [Khanna 2013]. However, an empirical formula is commonly used instead as it is more simple to calculate [Green 1983a] :

$$FF_{J0} = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \qquad (21)$$

where $v_{oc} = {}^{qV_{oc}}/_{nkT}$.

- **Contact resistivity impacts *FF*.**

The contact resistivity (section 2.2.3) directly contributes to the series resistance of the cell. The *FF* losses linked to the series resistance are estimated according to [Khanna 2013]:

$$\Delta FF_{Rs} = \frac{J_{mpp}^2 R_s}{V_{oc} J_{sc}} \qquad (22)$$

Typical series resistance in homojunction cells are 0.2–1 Ωcm^2 [Tous 2014] while in a silicon heterojunction they are 0.8–1.5 Ωcm^2. The series resistance can be determined by five different methods described in [Pysch 2007]. One of these methods is based on suns-V_{oc} measurements. In this measurement, the external voltage of a sample in open-circuit condition is probed under a light pulse. In a similar way than for the implied-*JV* curve, a *JV* curve, called the pseudo-*JV* curve, can be determined. As no carriers flow in the device (open-circuit measurement), no resistance losses occur. Interestingly, comparing such a measurement with a *JV* measurement, a series resistance can then be extracted [Pysch 2007].

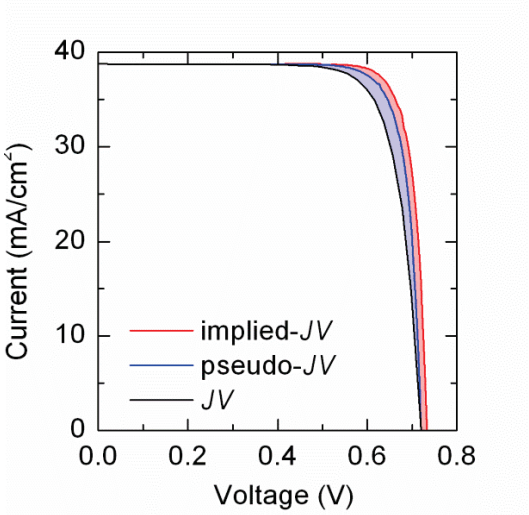


Figure 2.13: Implied-*JV* (red line) of a silicon heterojunction solar cell precursor after deposition of the a-Si:H layers, pseudo-*JV* of a silicon heterojunction solar cell precursor after deposition of the transparent current oxide and annealing (blue line), and *JV* (black line) of the finished device.

As highlighted previously, the device performances can be monitored by an implied-*JV*, pseudo-*JV* and *JV* curve, depending on the processing step, which enables an analysis of the losses in the solar cell [Sinton 1996a]. These curves are shown for a silicon heterojunction solar

cell in Figure 2.13. We observe that the implied-*JV* curve (red curve), giving an internal voltage of the cell, provides an upper limit due to recombination losses. Then, the external voltage with no resistance losses is given by the pseudo-*JV* curve, after the contacting step (TCO and metallization). In Figure 2.13, the pseudo-V_{oc} and pseudo-*FF* are observed to be lower than the implied-V_{oc} and implied-*FF*. This loss is due either to increased recombination losses induced by contacting or to a difference in the quasi-Fermi level splitting of the sample by measuring an internal or an external voltage (see Chapter 4.5)). Eventually, the *JV*-curve (black line) is shown. We observe the effect of the series resistance from the slope in the vicinity of the V_{oc}. This device will be discussed in Chapter 4.

2.4.3 Passivation and contacts: a trade-off?

Standard homojunction solar cells, as introduced and sketched in Chapter 1, account for over 90% of the photovoltaic market. These devices have part of their surfaces in direct contact with the metal contact and the remaining area passivated by dielectrics. Each region is then characterized by a J_0 and the total recombination current prefactor is a combination of these two regions as described in Ref. [Fischer 2003] and [De Wolf 2005].

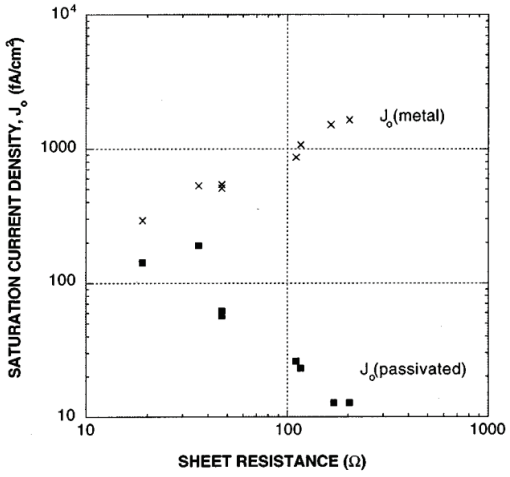


Figure 2.14: "*Comparison of the J_{0e} of phosphorus-diffused, planar emitters passivated with PECVD SiN and thin thermal oxides*". Reprinted with permission from[Cuevas 1996]. © 1996 American Institute of Physics.

As the lowest J_0 value achieved for a metallized surface approaches 350 fAcm^{-2} [Woehl 2011] and the J_0 value for passivated samples are typically one or two orders of magnitude lower, homojunction cells are typically limited by recombination losses at their contacts. At these contacts, the contact resistivity and the passivation quality are not decoupled: On one hand, to achieve an ohmic contact with a low contact resistivity, the underlying c-Si region must be highly doped, as shown in Figure 2.5 [Schubert 2006]. On the other hand, the lowest J_0 values are obtained for passivated surface on a lightly doped c-Si region (Figure 2.10). Moreover, reducing the

metallization area to point contact increases efficiently the V_{oc}. However, as the carrier must travel longer distances in silicon, higher R_s are observed, reducing the *FF* [Wijekoon 2013]. Thus, the optimal device design is limited by geometrical constraint and the best trade-off between ohmic and recombination losses must be found [Wolf 2010]. Figure 2.14 summarizes the constraints arising from the antagonism between passivating material and metallization.

Recombination losses can be characterized by the recombination current pre-factor J_0 (Acm^{-2}) and the contact resistance losses by the contact resistivity ρ_c (Ωcm^2). To illustrate this trade-off between these two quantities, Bullock et al. simulated an idealized solar cell structure based on a quasi-analytical model [Bullock 2014b, Cuevas 2012, Cuevas 2013, Cuevas 2008]. The results are shown in Figure 2.15. The PERL and SHJ cells are indicated in the graph. Although for both types of devices similar efficiencies can be achieved, we observe that they are situated on opposite sides in the graph: SHJ have a low J_0 value but relatively high ρ_c, conversely, PERL solar cells have a low ρ_c and a relatively high J_0.

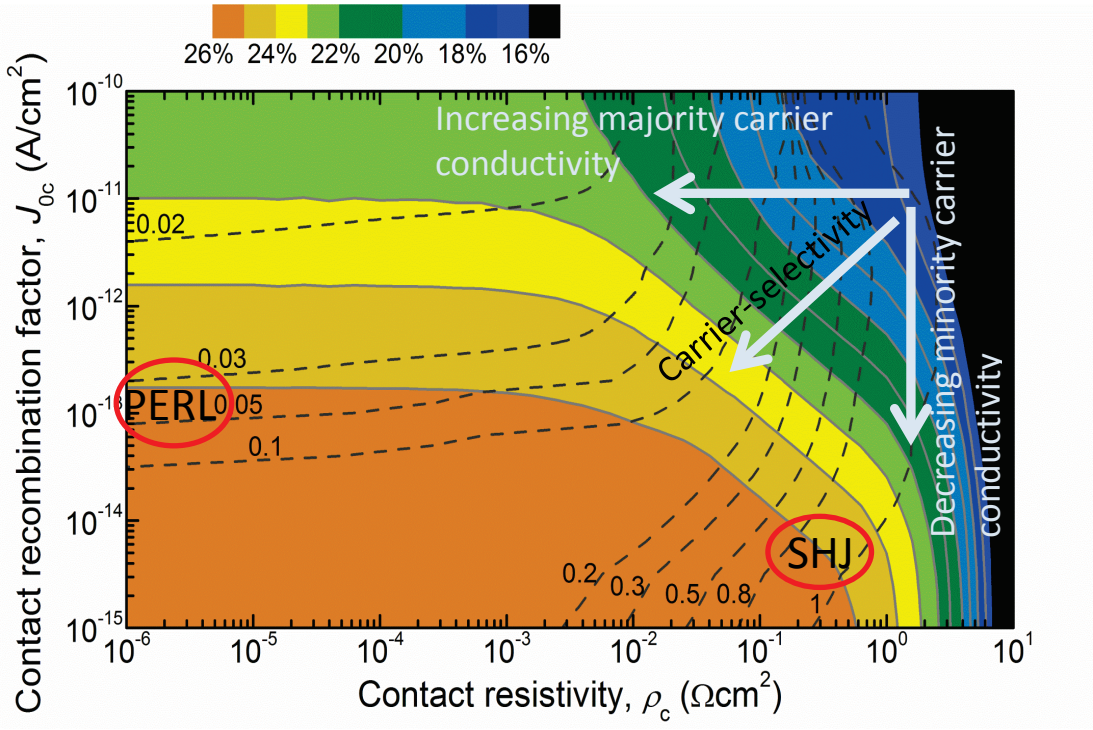


Figure 2.15: "Simulated optimum contact fraction (dotted lines) and resultant efficiency (contour plot) as a function of rear contact ρ_c and J_0." The 26 % limit in this simulation is due to a current limit at 40 mA/cm^2. Reproduced from [Bullock 2014b].

2.5 Passivating contacts

The previous sections have discussed the importance of contacts and passivation for solar cells. Further progress of homojunction solar cell is limited by losses due to a direct contact between the semiconductor material and the metal. In the past few years, designing alternative contacts for silicon-wafer-based solar cells has become a hot and attractive field. Several groups worldwide have proposed new structures to form a passivated electron or hole collector. In this section, we review the published work on passivating contacts, after a brief nomenclature classification.

2.5.1 Nomenclature and general principles of passivating contacts

In general, all contact designs mentioned here involve a carrier-selective junction with a full-area passivated wafer surface and a metallization scheme for current extraction. We propose a classification of the structures according to their physical working principles: First, passivating contact structures in which the carrier selectivity arises from the overlayers solely will be referred to as “selective passivating contacts”. No heavily doped region is needed in the wafer and this case is typically illustrated by the a-Si:H/c-Si heterojunction contact. The carrier selective junction is at the position of the buffer layer on the wafer surface. Conversely, we identify a second class of passivating contacts that comprises a highly doped region in the Si wafer (diffused or implanted) that provides charge-carrier selectivity and a passivating layer to suppress charge-carrier recombination. In this case, the carrier selective junction is defined by the highly doped region and is thus inside the wafer, and the charge carriers are separated before they are extracted to the metal. We refer to these contacts as “non-selective passivating contacts.”

A common feature of the passivating contacts presented in the next section is the presence of a buffer layer. This layer has three key properties [von Roedern 1993]: the chemical (and optionally also field-effect) passivation abilities of the wafer surface, a low bulk defect density, and a reduced minority-carrier mobility.

2.5.2 Literature review of passivating contacts

2.5.2.1 Selective passivating contacts

Semiconductor/transparent conductive oxide or metal contacts

The best-known passivating contact is the one used for silicon heterojunction solar cells, which is composed of c-Si/a-Si:H(i)/a-Si:H(doped)/transparent conductive oxide (TCO)/metal. In this contact, the selectivity of the carriers depends on the doping type of the a-Si:H(doped) layer: n-doping will form an electron collector and p-doping a hole collector [Tanaka 1992]. This contact enables extremely high V_{oc}, as demonstrated by Panasonic: 750 mV on a 98-µm-thick

wafer which is close to the theoretical limit [Taguchi 2014, Tiedje 1984]. However, the *FF* of such devices was believed to be limited by these contacts, as lower *FF* values than those of homojunction solar cells were usually achieved with this technology (Figure 2.16). In a recent record, Panasonic demonstrated a cell efficiency of 25.6% with a *FF* of 82.7%, proving that this structure does not have a fundamental *FF* limitation compared to homojunction devices [De Wolf 2012c, Panasonic 2014]. This contact will be further discussed in Chapter 4.

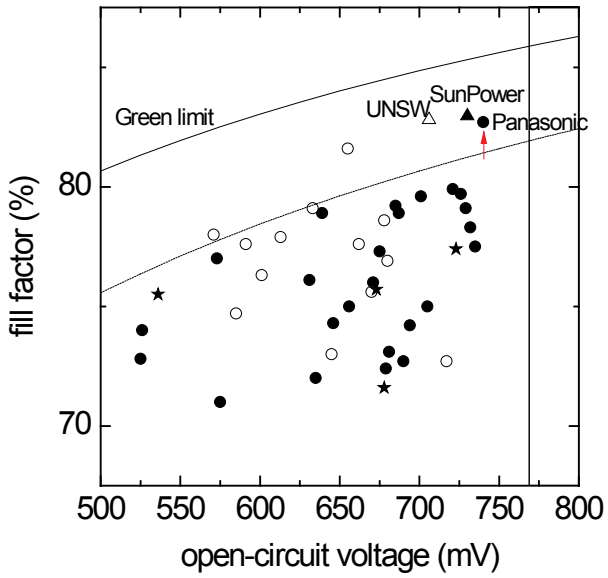


Figure 2.16: V_{oc} vs. *FF* for published devices. Discs: SHJ solar cells, stars: IBC-SHJ devices, triangles: homojunction devices. Open symbols: p-type wafers, closed symbols: n-type wafers.
Adapted from [De Wolf 2012c].

The a-Si:H/c-Si heterojunction contact is sensitive to temperature: the a-Si:H passivation quality deteriorates when exposed to temperatures above 250–300 °C due to hydrogen effusion. This limits the use of a-Si:H/c-Si contacts to processes below 250 °C, which might constrain its use for specific applications.

A similar contact structure as the SHJ contact, i.e. a c-Si wafer with a semiconductor buffer layer and metallic top contact, was developed by Avasthi *et al.* [Avasthi 2013]. They used a 3-nm-thick titanium oxide as a buffer layer on a c-Si wafer and obtained an efficient hole-blocking heterojunction contact.

Semiconductor/insulator/metal solar cells

In the 1970's, solar cell research focused on MIS structures (section 2.2.2). In these solar cells, the insulator forms the buffer layer and the selectivity of this contact is induced by the difference between the WF_M and WF_{SC} forming an inversion layer. In these structures, the depletion induced by this work function mismatch is less pronounced, however, as part of the potential drop occurs in the insulator as well, as also drawn in Figure 2.4. Nonetheless, this disad-

vantage is partly compensated for by using e.g. silicon dioxide as an insulator, which has a high fixed positive charge density [Würfel 2008]. Experimentally, starting from a p-type wafer, the electron-selective contact is typically formed by a thin SiO_2 layer with an Al overlayer (minority-carrier MIS structure) and the hole collector by an ohmic Al contact. In 1979, the best efficiencies reached with such devices were 17.6%, approaching the best efficiency at that time of diffused junction solar cells, which was 18.6% [Godfrey 1979]. However, MIS solar cells had the drawback of requiring at their front either a full-area thin metal layer (<20 nm) or a grid-like structure to enable incident light to generate carriers in the semiconductor wafer while maintaining the inversion layer stable for device operation [Shewchun 1974]. The inversion layer of such formed cells is sensitive and depends on electrostatic effects. As rear-emitter cells necessitate high-quality wafers which were not available at that time, this structure was then mostly abandoned.

In 1984, Kwark *et al.* investigated the use of semi-insulating polycrystalline silicon (SIPOS, a disordered material composed of polysilicon and silicon oxide) as a buffer material [Kwark 1984, Takeshi 1976, Yablonovitch 1985]. Its use in solar cells drastically lowered the J_0 value. Adding a SiO_2 buffer layer between the c-Si wafer and the SIPOS or polysilicon layer reduced the J_0 value even further [Kwark 1987]. The advantage of SIPOS or polysilicon over amorphous silicon is, first, to have a reduced parasitic absorption and, second, to withstand higher temperature processes for device integration.

We note that, in 1985, Swanson, a co-author of Kwark's and Yablonovitch's, founded Sunpower Corporation which produces high-efficiency solar cells using passivating contacts [Cousins 2010, Smith 2012]. Sunpower recently presented a 24.97%-efficient cell of 121 cm^2 [Smith 2014]. Although not yet published, similar passivating contacts than described in the previous paragraph might be used in their solar cells.

Recently, Feldmann *et al.* reported a passivated electron collector (TOPCon) composed of 1.5 nm of SiO_2 and of 20 nm of phosphorus-doped "deposited silicon" followed by a TCO and silver layers [Feldmann 2014a]. The precise nature of the deposited silicon layer is not revealed, however. A cell with such a passivating back contact and a selective front emitter yielded an efficiency of 24.4% [Feldmann 2014b], and a device with selective passivated hole and electron collectors provided a V_{oc} of 694 mV [Feldmann 2014c]. Römer *et al.* and Young *et al.* are also developing similar contacts [Römer 2014, Young 2014]. The current transport through these contacts could be dominated either by tunneling through the oxide layer or by the current flow through the pinholes in the oxide [Wolstenholme 1987]. This contact is stable up to 900 °C [Moldovan 2014].

Dielectric/transparent conductive oxide based contacts

Garcia-Alonso *et al.* modified the MIS structure, directly replacing the metal with a TCO [Garcia-Alonso 2013]. They prepared a thin passivating Al_2O_3 layer on a c-Si(p) wafer, and capped it with aluminum-doped zinc oxide. They showed that the contact is selective to holes,

with a hole accumulation at the c-Si(p)/Al_2O_3 interface due to the negative built-in charge of the Al_2O_3 layer. Enhanced passivation can be obtained by a thin a-Si:H layer under the Al_2O_3 layer [Smit 2014]. In a similar approach, Young *et al.* have also been developing passivating contacts based on TCOs [Young 2014].

For a dielectric-based contact, Battaglia *et al.* used molybdenum oxide (MoO_x) to form a hole contact directly on a c-Si wafer [Battaglia 2014b] or on an a-Si:H(i) layer to reduce J_0 [Battaglia 2014a]. Replacing the a-Si:H(p) layer with a wide-bandgap material greatly increased the short-circuit current density (+2.4 mA/cm^2). However, the authors reported a reduced *FF* which they attributed to a band misalignment between the MoO_x and a-Si:H/c-Si.

Organic-silicon hybrid contacts

In an organic-silicon hybrid solar cell, PEDOT:PSS was used as a hole-conducting emitter [Schmidt 2013]. However, to obtain good passivation, a thin SiO_x layer is required between the c-Si wafer and the PEDOT:PSS. With such a hole collector at the front and a diffused junction at the back to form the electron collector, efficiencies as high as 17.4% were obtained [Zielke 2014].

We note that the main technological improvement between the first MIS structures and these new generations of contacts is the use of TCOs to replace the metal's role, even though the first TCO, cadmium oxide, was discovered in 1907.

2.5.2.2 Non-selective passivating contacts

We now focus on contact structures that rely on a selection of carriers prior to tunneling, induced by a diffused or ion implanted region.

Metal-insulator-semiconductor with an underlying diffused/implanted junction

As discussed in the previous section, the first MIS solar cells were limited by their unstable inversion layer [Shewchun 1974]. To avoid this, a new structure was proposed in 1981 using an underlying pn-junction formed by diffusion or ion implantation with a MIS top contact, named the MINP cell [Green 1983c, Green 1981]. Hezel *et al.* reached efficiencies of up to 21.1% in 2002 with the MINP structure using SiO_x as a buffer layer [Hezel 2002], while most of the PV community focused on increasing the selectivity of diffused junctions by process optimization and local metal-Si contacts [Green 1995]. Recently, the MINP approach regained interest and several groups are now working on this structure. Zielke *et al.* have innovated in a new dielectric layer for MINP structures using a thin Al_2O_3 layer deposited by atomic layer deposition (ALD) [Zielke 2011]. With such layers, a diffused n-type emitter formed the electron collector and the passivation properties of the 24-Å-thick Al_2O_3 film yielded a V_{oc} increase of 12 mV. Loozen *et al.* have investigated similar passivating contacts as well [Loozen 2012]. Bullock *et al.* have compared J_0 and the contact resistivity of structures consisting of a diffused c-Si wafer passivated with thermally grown SiO_2 or Al_2O_3 films deposited by ALD capped with Al and predicted a theo-

retical V_{oc} gain of 15 mV for the optimized film without any increase in resistance losses [Bullock 2013].

MSS structures

In a slightly different approach, the insulator film of MIS contacts can be replaced with a semiconductor film such as a-Si:H, which is known to achieve extremely good passivation quality (section 2.3.3). Bullock *et al.* implemented c-Si(n)/a-Si:H(i)/Al structures and showed that, even though several-nanometer-thick a-Si:H layers were needed to achieve good passivation, the contact resistivity remained reasonable, due to carrier tunneling and Al spiking through the a-Si:H(i) layer [Bullock 2014c]. With such structures, a gain of up to 50 mV in V_{oc} could be obtained. However, due to Al spiking, these contacts are affected by temperature steps above 110 °C. Bullock *et al.* improved the thermal stability of MSS structures using a-Si:H layers by inserting a dielectric layer between the semiconductor diffused layer and the a-Si:H layer. These structures benefit from a higher passivation quality than a pure MIS contact due to the hydrogen-rich a-Si:H overlayer acting as a hydrogen reservoir for the dielectric layer and to a low contact resistivity due to the Al diffusion in the a-Si:H layer [Bullock 2014b].

2.6 Contacts investigated in this thesis

The passivating contacts investigated during this thesis are described in Chapter 1 and aim to find an efficient trade-off between J_0 and ρ_c. Technologically, they can be viewed as a-Si:H/c-Si local contacts on a diffused wafer.[3] No work on such contacts has been published so far. Sihua *et al.* simulated such contacts using AFORS-HET, a simulation program developed by Helmholtz-Zentrum Berlin [Froitzheim 2003, Sihua 2013]. They pointed out that such contacts would indeed lead to high V_{oc} and *FF*. However, no experimental proof supports their work. The results of such structures will be presented in Chapter 5.

Compared to a standard diffused-junction c-Si solar cell contact, this new contact has the advantage of being passivated, implying less recombination and the possibility of higher V_{OC}s. Compared to a standard SHJ solar cell contact, the fill factor (*FF*) might be improved due to a lower contact resistance. Moreover, the optical requirements can be decoupled from the contacts by patterning local contacts. Then, using a transparent passivating layer in between the contacts should enable high J_{sc} .

[3] A similar structure was patented by Nils-Peter Harder in 2011. Patent US 20110174374 A1

Chapter 3 Homojunction formation

Silicon homojunctions are the building blocks of many microelectronics devices and standard crystalline silicon (c-Si) solar cells, as discussed in Chapter 1. The main role of such junctions is the efficient charge separation in a semiconductor device. This chapter investigates and discusses the advantages and challenges of three approaches to form such junctions for homo-hetero devices. First, thermal diffusion, the most common process in the photovoltaics community, is investigated. As this approach usually yields junctions at both wafer sides simultaneously, we evaluate several methods to obtain single-side doping profiles (needed for homo-hetero solar cells fabrication) and show that a dry back-etching process is the most efficient way. Second, ion implantation, commonly used in microelectronics and receiving an increasing interest for photovoltaics applications, is convenient as it directly provides single-side dopant profiles, even though it may be costly. Eventually, we investigate low-temperature (≤ 180 °C) plasma-enhanced chemical vapor deposition (PECVD) epitaxial growth to from the homojunction. This method exploits thin-film deposition technology, similar to that used in silicon heterojunction devices fabrication, and avoids a high-temperature process step to form the homo-hetero contact. For this reason, particular emphasis is laid on this approach. To begin with, we determine the conditions leading to epitaxial growth in light of a model that depends only on the silane concentration in the plasma and the mean free path length of surface adatoms. For such growth, we show that the presence of a persistent defective interface layer between the c-Si substrate and the epitaxial layer stems not only from the growth conditions but also from unintentional contamination of the reactor. Based on our findings, we determine the plasma conditions to grow high-quality bulk epitaxial films and propose a two-step growth process to obtain device-grade material. We then discuss the phosphorus doping of epitaxial layers and characterize them.

3.1 Introduction

All solar cells rely on the generation of electron-hole pairs, their separation and their collection at the device terminals. Each of these processes should occur as efficiently as possible, incurring minimal losses. Focusing on efficient carrier collection, ideally, two contacts acting as semi-permeable membranes are needed: one to collect holes and block electrons, and the other to collect electrons and block holes. In a classic homojunction c-Si solar cell, a p-doped region

serves as a hole collector and an n-doped region as an electron collector, as illustrated in Figure 3.1. These regions are characterized by their dopant profile, defined by their dopant concentration at the surface (N_s), depth and shape. In such homojunction c-Si solar cells, the ideal dopant profile results from an important tradeoff: on one hand, a high doping concentration is required to ensure good contact properties, on the other hand, for passivated surfaces, a low doping concentration lowers the recombination current pre-factor (J_0), especially suppressing undesired Auger recombination, as discussed in Chapter 2. Moreover, with high doping concentration, bandgap narrowing and reduction in the mobility of the carriers may as well occur. More information about the physics of these junctions can be found in [De Wolf 2005, Sze 2002, Würfel 2008].

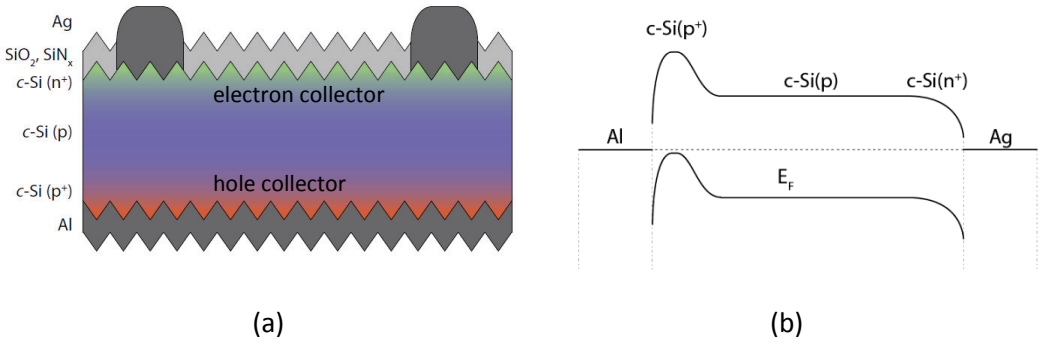


Figure 3.1: (a) Sketch and (b) band diagram of a silicon homojunction solar cell on p-type c-Si wafer (c-Si(p)) with a full front (c-Si(n^+)) and rear (c-Si(p^+)) diffused surfaces. These regions act as, respectively, the electron and hole collector. The silicon oxide (SiO_2)/silicon nitride (SiN_x) stack passivates the c-Si wafer and acts as an anti-reflecting coating. At the rear, an alloy is typically formed between the c-Si and aluminium (Al).

This chapter evaluates three methods to obtain homojunctions:

1) Thermal diffusion of dopants
2) Ion implantation of dopants
3) homo-epitaxial growth by low-temperature (<180 °C) PECVD

The first two methods are well established and widely used in the PV community. Therefore, rather than explaining the basics of these methods, which can be found in literature [Rohatgi 2012, Sze 2002, Szlufcik 2002], we focus on discussing the practical challenges that may arise when fabricating hybrid solar cells, combing both low- and high-temperature technology. Indeed, in all-high temperature technology, the parasitic rear junction is usually dissolved completely during aluminum rear-contact firing. In our envisioned process, this is not the case. Hence, we discuss here practical solutions to remove such parasitic rear junctions, engineered by diffusion (section 3.2). Conversely, ion implantation (section 3.3) has the advantage of being a single-side process and simplifies the processing of homo-hetero devices. The third method,

homo-epitaxial growth by low-temperature PECVD, is specially developed for the purpose of this thesis: forming passivating contacts for silicon homojunction solar cells using a-Si:H deposited by PECVD (see Chapter 4). Being capable of forming the homojunction using the same deposition technique as to deposit the a-Si:H layers might therefore be a decisive advantage for these contacts. Although silicon homo-epitaxial growth has already been studied for several decades at high temperature [Theuerer 1960] and more recently also at low temperature by PECVD [Damon-Lacoste 2010a, Nagamine 1987], no in-depth study has yet established the necessary conditions for epitaxial growth at low temperature. In this context, in section 3.4, we identify first the parameters dictating the growth mode on a c-Si wafer and then determine the requirements for epitaxial growth. The homo-epitaxial films are then doped and their conductivity determined.

3.2 Diffusion

The most common way of forming a homojunction consists of the thermal diffusion of dopants in a c-Si wafer. In a first step, a phosphosilicate glass (PSG) or a borosilicate glass (BSG) is grown on the wafer using either a vapor or a liquid source of dopants. A high-temperature step (750—1100 °C) then drives the dopants further into the c-Si wafer, with or without further growth of the dopant glass, depending on the profile desired. For a constant total-dopant diffusion, where during the drive-in step no diffusion-glass is grown, this leads to a Gaussian-like profile. For a constant surface concentration, where during the drive-in step diffusion-glass is grown, the profile will have a complementary-error-function-like profile [Sze 2002]. The dopant profile is further optimized by changing the dopant gas fluxes, the deposition time, the temperature ramp, the drive-in temperature ramp and the duration of each individual step. Simulation programs, such as Athena (Silvaco), can be used to narrow the optimization region.

The advantage of this method is its wide use and the relatively soft dopant introduction. Often, it may also lead to electronic improvement of the bulk of (solar grade) wafers, especially for the case of phosphorus diffusion, a process usually referred to as gettering. As in this work we use exclusively high-grade wafers, this phenomenon is of little relevance and will not be further discussed. The main disadvantage of diffusion consists of the high temperature needed to activate the dopants, which may simultaneously diffuse impurities or dissolve clusters of impurities already present, so-called wafer poisoning. Moreover, it is a two-side process, requiring extra steps to achieve a single-side diffusion as needed in a solar cell.

3.2.1 CSEM and CMi diffusion tubes

First diffusion tests were performed at the Centre Suisse d'Electronique et de Microtechnique (CSEM) using a CVD-grown silicon oxide with a high dopant concentration as the dopant source. However, the grown oxide was not sufficiently pure and, during the drive-in step, do-

pants and impurities were simultaneously diffused in the wafer, the latter creating recombination centers detrimental for the solar cells performance. The diffusion of impurities was evidenced by testing the passivation quality by depositing on both sides of the wafer a PECVD-grown a-Si:H layer, which is known to provide excellent surface passivation, and extracting the effective minority-carrier lifetime (τ_{eff}) of such samples using a a photoconductance measurement. A wafer with an undoped silicon oxide layer that had been exposed to a high-temperature step (800 °C) in the CSEM furnace had $\tau_{eff} \leq 200$ µs, whereas a sample which had no undoped silicon oxide layer and no high-temperature step had $\tau_{eff} \geq 4$ ms. This indicates that the bulk c-Si had been contaminated by the high-temperature process, likely from impurities in the silicon oxide layer.

At EPFL-Centre de Microtechnique (CMi), a Centrotherm phosphoryl chloride ($POCl_3$) diffusion tube is available. Several diffusion processes were tested at temperatures ranging from 750 to 850 °C, resulting in various sheet resistances, as shown in Figure 3.2.

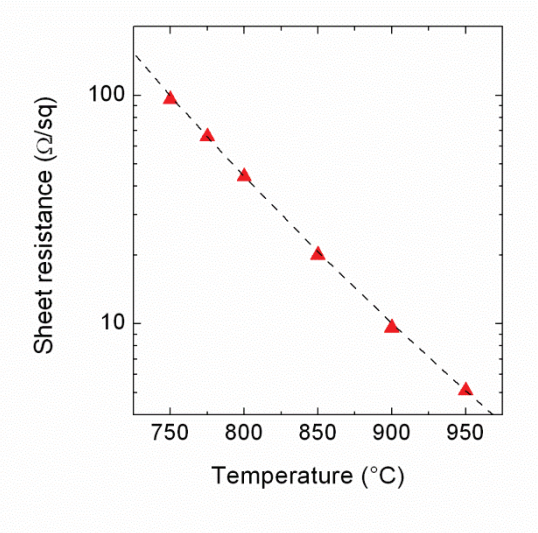


Figure 3.2: Sheet resistance as a function of the diffusion temperature. The dashed line is a fit using an exponential function.

To study the obtained profiles, a comparison between a secondary ion mass spectroscopy (SIMS) profile, which takes into account all dopant atoms present in the film, and a spreading resistance profile, which measures only the active dopants, was made and is shown in Figure 3.3. We observe a relatively high concentration of inactive dopants, likely due to the low diffusion temperatures used [Solmi 1996].

Very high concentration of dopant atoms will typically form a highly resistive layer at the wafer surface, called a dead-layer, in which carriers have extremely low lifetimes (<100 ps) [Lindmayer 1990]. Such layers can be removed either by a high-temperature step, which will diffuse the dopants deeper and activate them, or by chemically etching them. As no clean high-temperature furnace was available, the second solution was investigated. The dead-layer could

be at least partially removed by several oxidation and oxide etching steps in nitric acid (HNO_3) at 80 °C and 5% diluted hydrofluoric acid (HF).

Finally, a collaboration was set with the Australian National University (ANU) to acquire diffused wafers with optimized profiles for solar devices.

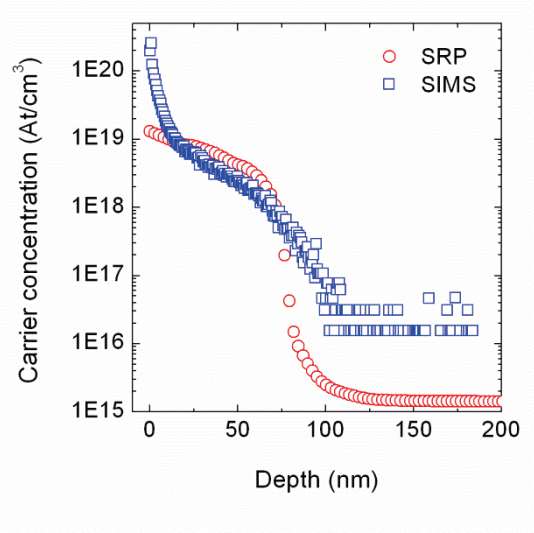


Figure 3.3: Doping profile of a $POCl_3$ with 5 minutes of oxide growth, 15 minutes exposed to a $POCl_3$ gas and 15 minutes of drive-in at 750 °C. The profile corresponds to an error function. A spreading resistance profile (SRP) considers only active dopants in contrast to a SIMS profile, which takes into account all dopant atoms present in the film.

3.2.2 Single-side diffusion

In a solar cell, a selective contact for both types of carrier (electrons and holes) is needed. In the process flow of an industrial homojunction solar cell (Figure 3.1), a $POCl_3$ diffusion is performed on a p-type wafer. The resulting c-Si(n+) at the front is used as the electron collector. Conversely, the c-Si(n+) region at the rear is then overcompensated by an Al-Si alloy, forming the hole collector. However, in the homo-hetero structures investigated in this thesis, no Al-Si alloy is desired and thus a single-side diffusion is needed. Single-side diffusion may be obtained by additional processing steps either before or after the diffusion process. In the former case, a single-side oxide or a similar protective layer of high purity is usually grown. The PSG is then deposited on top of this layer and dopant diffusion occurs within this sacrificial layer without diffusing into the c-Si wafer. This layer is then generally chemically etched. Conversely, if both sides of the wafer are exposed to the diffusion, a back-etching of the doped region on one side of the wafer must be performed. This can be achieved either by wet chemistry or by a dry plasma process. In this section, we present several methods to back-etch one side of a wafer and determine the best suited method.

3.2.2.1 Wet chemistry

First, we investigate chemical back-etching by an alkaline potassium hydroxide (KOH) bath with one side of the c-Si wafer protected. The alkaline solution etches c-Si anistropically revealing {111} faceted pyramids. First, a KOH bath with an additive to obtain random pyramids was used. Using a polished wafer, 20 minutes were necessary to etch the first micrometers of the c-Si surface in all places as evidenced in scanning electron microscope (SEM) micrographs of Figure 3.4.

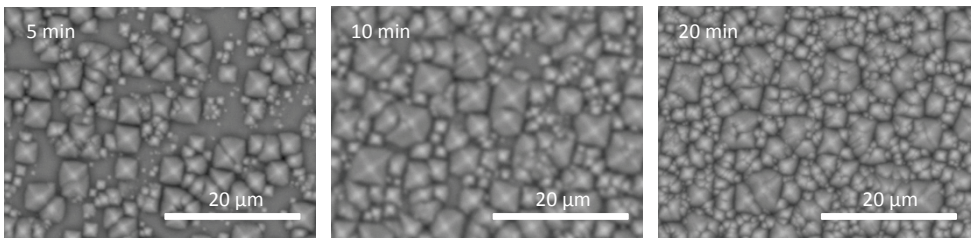


Figure 3.4: Scanning electron microscope micrographs of a polished wafer exposed to a KOH solution for (a) 5 minutes (b) 10 minutes and (c) 20 minutes. After 20 minutes, no flat areas remain.

Therefore, on a diffused wafer, the unprotected side was etched for 20 minutes in a KOH bath to remove a few micrometers of c-Si on all the exposed surfaces, including the diffused region. Three techniques were investigated to protect the other side from the alkaline etching:

1. A mechanical system was designed and machined for this purpose (Figure 3.5 (a)). It is composed of a Teflon chuck. Joints in a fluoroelastomer (Viton) are moreover needed to ensure impermeability. However, with such protection, the chemical fluxes flowing on the wafer are not homogenous, leading to a non-uniform texturing (Figure 3.5 (b)).

2. Protective layers, such as silicon oxide (SiO_x) and silicon nitride (SiN_x),, were deposited by low-temperature (< 200 °C) PECVD. However, as shown in Figure 3.5 (c) and (d), the deposited SiO_x and SiN_x layers are porous (pinhole density as high as 9 10^2 mm^{-2}) . Despite a thick or multilayer stack, during KOH etching, the pinholes reached the c-Si surface and the c-Si was etched as well. Stacks of SiN_x/SiO_x provided better protection but dust particles in the CVD system caused the protective layer to be locally inefficient.

3. A Protek B3 resist was spin-coated, which offered sufficient protection on textured wafers if a double spin-coating was used.[4] The resist was then removed in a sulfuric (H_2SO_4) and hydrogen peroxyde (H_2O_2) bath in a (3:1) ratio. This solution is known as a piranha solution. The wafers were cleaned with a subsequent HNO_3 bath at 80 °C. This process gave good results: not only was a single-side diffused wafer obtained but also the c-Si surface was preserved and yielded good passivation quality ($\tau_{eff} \geq 4$ ms). In a solar cell,

[4] http://www.brewerscience.com/protek-b3

no difference in the characteristic parameters could be observed. However, this process is time consuming as it consists of eight steps, as sketched in Figure 3.6.

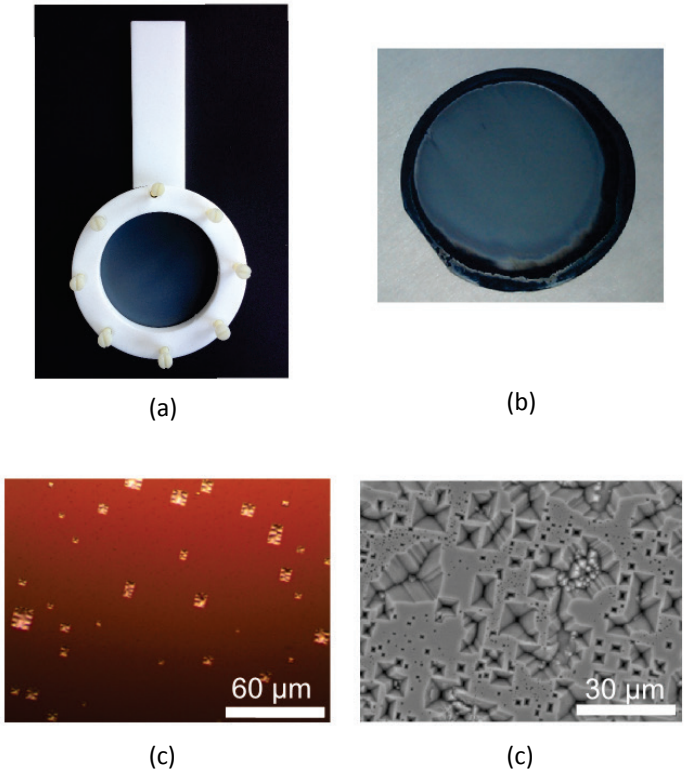


Figure 3.5: (a) Photograph of a mechanical protection system. (b) Photograph of the wafer after mechanical protection. (c) Microscope image of pinholes in the SiN_x protection layer. (d) SEM image of the c-Si wafer etched underneath the protective layer due to pinholes observed in (c).

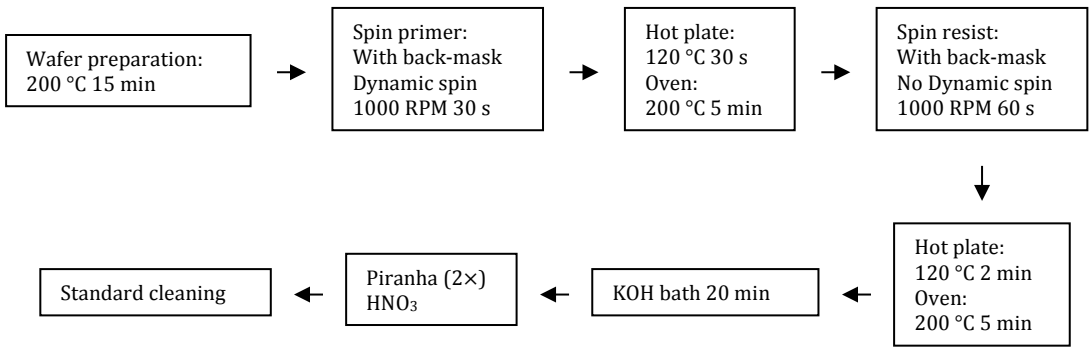
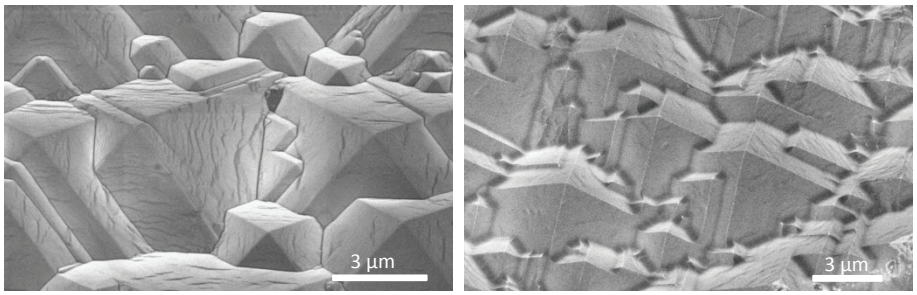


Figure 3.6: Process flow for one-side texturing using Protek B3 resist.

3.2.2.2 Dry plasma etching

Finally, a simplified process was established by using a dry plasma etching with sulfur hexafluoride (SF_6) and molecular oxygen (O_2) gases. The flux, power and pressure of the gases were optimized for homogeneity. Passivation of a wafer directly after etching yields lifetimes below 100 µs; however, after a piranha clean, lifetimes as high as on a pristine wafer were obtained ($\tau_{eff} \geq 5$ ms). Such a plasma etching smoothens the valley and peaks of the pyramids as shown in Figure 3.7.



(a) (b)

Figure 3.7: SEM images of (a) a standard texture and (b) a texture after dry etching of 800 nm of c-Si.

3.2.3 Conclusion

In a homojunction solar cell with passivating contacts, single-side diffusion processes are needed. In this thesis, we evaluated several methods to achieve such structures by removing the diffused region on one side on the wafer while maintaining the other side with a pristine diffused region. The methods investigated involved mechanical, chemical and dry etching processes. The latter yielded the best results in terms of homogeneity, passivation quality after processing and process time.

3.3 Ion implantation

Ion implantation consists of accelerating dopants in an electrical field, focusing them into a beam, and then bombarding a target substrate —a c-Si wafer in this case—with them. The doping profile is controlled by the energy and the flux of the ionized dopant as well as by the implantation duration. The time-integrated ion flux is called the ion dose, expressed in ions per cm^2. Defects are created during this process and are removed by subsequent annealing typically at 800 °C, which simultaneously grows a SiO_x layer. This technique is widely used nowadays in integrated-circuit processing because of its precise control of doping depth and concentration, uniformity and reproducibility. Moreover, as it is highly directional, patterning can be simplified by focusing the beam on specific regions. However, for a long time, it was considered too expensive for solar cell mass production [Nastasi 1995]. In the past decade, it has regained interest

for its potential to simplify processes, and thus lower the cost, of high-efficiency solar cells [Rohatgi 2012]: It is indeed a single-side process, provides simultaneous SiO_x passivation and requires no process to remove a PSG or BSG [Jeon 2011].

For this work, Georgia Institute of Technology kindly provided implanted wafers. The dopant profiles obtained by the electrochemical capacitance voltage (ECV) technique are shown in Figure 3.8. As the ion-implanted wafers (n-type, 5 Ωcm) have an alkaline textured surface and the determination of the doping level depends on the square of the surface, a coefficient of 1.73 was applied to the surface, corresponding to an angle of 54.7° for the pyramids. This approximation typically leads to an error range increase of 10% compared to an ECV profile on a flat surface. The sheet resistance was calculated from the ECV profiles and compared to four-point probe measurements. The integrated ECV profile for phosphorus overestimated the sheet resistance by 5 to 16%. However, the integrated boron profile overestimated the sheet resistance by nearly a factor of 2. This difference could arise from the different junction type formed by the phosphorus or boron implantation. As an n-type wafer is used in this experiment, for a boron implantation, a pn-junction forms. Due to the depletion region, no current can flow through in the base wafer. Conversely, for a phosphorus implantation, a high-low junction forms instead and the current may flow through the wafer. However, further investigations are needed to fully understand this discrepancy.

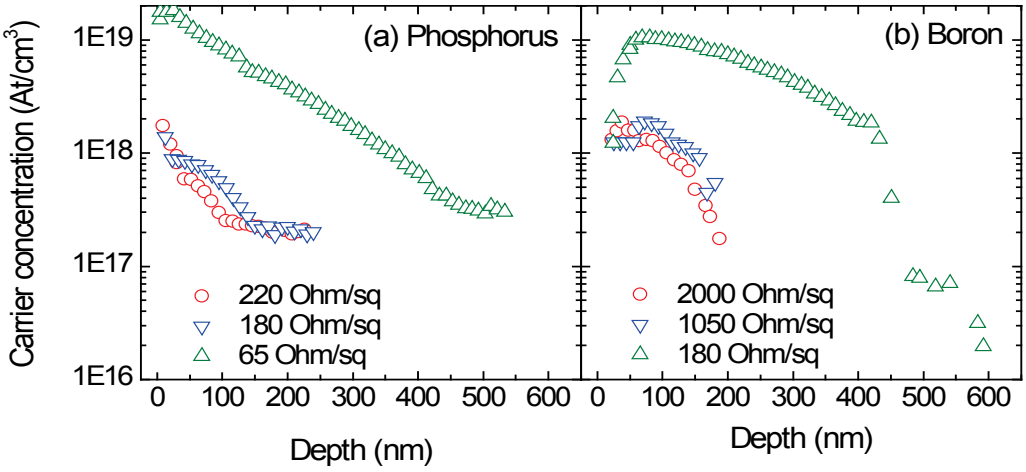
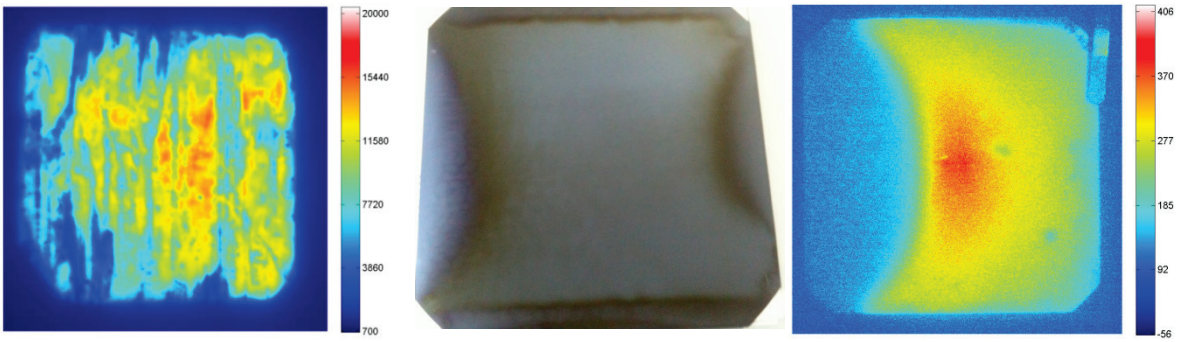


Figure 3.8: Electrochemical capacitance voltage (ECV) profile of (a) phosphorus- and (b) boron-implanted n-type wafers.

A first set of ion-implanted wafers was processed to form homo-hetero devices and the results are presented in Chapter 5. The c-Si bulk quality was observed to limit the devices. Therefore, a new set of ion-implanted wafers was agreed on. For this set, after testing the passivation quality of 6-inch wafers from various providers, high-quality wafers from Norsun were send to Georgia Institute of Technology for ion implantation. The CZ wafers were diamond wire cut and necessitated a 40% longer time in the saw damage removal bath (KOH concentration > 30%)

than our standard wafers. In Figure 3.9 (a), a photoluminescence image shows lines with lower passivation quality, evidencing the need for a longer time in the saw damage removal bath. Unfortunately, after ion implantation, the chemical treatment after annealing to reduce the inactive boron concentration was not uniform, as pictured in Figure 3.9 (b) and (c). Despite selecting the best-quality regions for cell processing, this ion-implanted batch systematically revealed a negative V_{oc} difference of 30-50 mV compared to the co-processed wafers l from the first batch. Due to these low performances, no further experiments were performed using these wafers.



(a) (b) (c)

Figure 3.9: (a) Photoluminescence image of a wafer with insufficient saw damage removal after passivation with a-Si:H by PECVD. (b) Picture of an ion-implanted wafer with a processing issue. (c) PL image of a similar wafer with a passivating SiO_2 layer.

3.4 Low-temperature plasma-deposited silicon epitaxial films

3.4.1 Motivation and prior art

The passivating contacts developed in this thesis combine c-Si technology to form the homojunction and thin-film technology to deposit the a-Si:H-based passivating contacts by PECVD. For photovoltaic applications, low-temperature (≤ 200 °C) PECVD is a well-established technique to grow a-Si:H and microcrystalline (µc-Si:H) silicon thin films, with important applications in thin-film silicon and high-efficiency silicon heterojunction solar cell fabrication. Using PECVD to form the homojunction by growing a homo-epitaxial layer would greatly simplify the processing of the homo-hetero devices. Moreover, at the high temperatures typically used to form a homojunction, unintentional dopant and impurity diffusion may also occur, detrimentally affecting the bulk electronic properties of the substrate (e.g. the charge-carrier lifetime) or impairing the properties gained by earlier processing steps. PECVD promotes the chemical reaction in a radio-frequency (or higher frequencies) discharge instead of thermally. It thus dissociates process gasses at significantly lower temperatures compared to thermal CVD [Sterling 1965]. Finally, PECVD is a single-side deposition technique, making the use of procedures described in section 3.2.2 unnecessary.

Homo-epitaxy enables the growth of high-quality semiconductor films with a well-defined doping-concentration profile and accurate layer-thickness control. For c-Si films, the first suc-

cessful implementation was found in bipolar transistor fabrication [Theuerer 1960], which rapidly extended to advanced microelectronics processing technology, including metal-oxide-semiconductor integrated circuits [Baliga 2012]. Silicon epitaxial growth has been studied since the early 1950s, using a variety of methods such as vapor-phase, liquid-phase, solid-phase and molecular beam epitaxy (MBE). Initially, high-temperature processes (> 800 °C) were preferred to guarantee epitaxial layers of sufficient quality. Elevated temperatures clean the surface by volatizing contaminants present prior to the growth and sustain defect-free crystal growth. Even though epitaxial growth by PECVD was first reported in the early 1970s, since then it has been only occasionally further investigated [Baert 1987, Reif 1984, Townsend 1973, Tsai 1989]. Recently, PECVD epitaxial layers regained increased interest, as it was recognized that such layers are ideally suited to engineer silicon solar cells, either as (relatively thick) optically active absorber layers that replace the still-costly wafer [Cariou 2011, Moreno 2010] or as thin layers for junction formation (electron or hole collectors, depending on the doping type) [Damon-Lacoste 2010b, Hekmatshoar 2014, Hekmatshoar 2012, Hekmatshoar 2011b, Labrune 2010, Plá 2002]. Despite this, the precise influence of the plasma conditions on the electronic and microstructural quality of the grown layers has been elusive. Characterization of these plasma conditions is important to gain insight into the growth of device-grade epitaxial layers, as already evidenced for a-Si:H and µc-Si:H films [Strahm 2007b]. Moreover, such knowledge is also valuable in fundamentally understanding how to avoid epitaxial growth and to which extend a-Si:H films can be deposited on c-Si wafers with atomically sharp interfaces. Sharp interfaces are critical for high-efficiency crystalline silicon / amorphous silicon heterojunction solar cells, the current world-record c-Si solar cell technology [De Wolf 2007, Panasonic 2014]. The results from this section was published in [Demaurex 2014a].

3.4.2 Plasma-deposited silicon epitaxial growth and properties

In this section, we first discuss the growth regimes arising from different substrates and surface structures. We determine the plasma conditions needed to obtain epitaxial growth on a <100> c-Si wafer and discuss the relevant parameters that determine such growth. Second, we find that an interfacial layer between the c-Si substrate and the epitaxial layer is systematically present and we discuss the origin of this layer. Thirdly, we investigate the microstructural quality of the epitaxial bulk by transmission electron microscopy (TEM) and ellipsometry, and identify the lowest defect density growth conditions. Finally, we study the electronic properties of the epitaxial films and outline the consequences for future device incorporation.

3.4.2.1 Experimental setup

Three types of substrates were used: a) Schott AF 45 glass b) thin PECVD µc-Si:H layers (~55 nm) deposited on such glass and c) float-zone 2 Ωcm phosphorus-doped mirror-polished c-Si <100> wafers. Surface cleaning of the wafers involved removal of the native oxide in a diluted

hydrofluoric acid solution (HF 5%) for 45 s. The substrates were then loaded directly into a PECVD system for intrinsic silicon film deposition using silane (SiH_4) mixed in hydrogen gas (H_2). A KAI-M PlasmaBox™ reactor (Oerlikon / Tokyo Electron) in parallel-plate configuration powered at very high frequency (VHF, 40.68 MHz) with an inter-electrode distance of 12.5 mm was used for the depositions [Bubenzer 1990, Seif 2014]. The base pressure of the reactor was typically about 4×10–7 mbar. The three substrates were always co-deposited for given conditions. The deposition pressure (1–7 mbar), power (0.098–0.42 W cm–2), and gas flux were varied at a fixed reactor temperature of 180 °C.

The deposited films were subsequently investigated by multi-angle spectroscopic ellipsometry (SE, Horiba UVISELTM) to determine their thickness, which ranged between 150 and 300 nm, and their amorphous fraction. Direct confirmation of the phase of the deposited material and Raman crystallinity fraction were obtained by Raman spectroscopy (Ar^+ laser with an excitation wavelength of 514 nm) [Droz 2004]. To characterize the microstructure of the epitaxial films and their interfaces with the wafers, high-resolution TEM (HRTEM) was performed with Philips CM300 UT and FEI Tecnai Osiris instruments; the latter was also used for energy dispersive X-ray (EDX) mapping using Super-X silicon drift detectors in scanning TEM (STEM) mode. Samples were prepared by mechanical polishing using the Allied High Tech Multiprep™ method followed by low-energy Ar ion milling. SIMS measurements were used to characterize the atomic composition of the films.

3.4.2.2 Special methods used: plasma diagnosis

To characterize the plasma during the depositions, an in-house-built plasma diagnosis was used to measure *in-situ* the SiH_4 depletion fraction [Bartlome 2009]. In this setup, a quantum cascade laser probed the rotovibrational absorption lines that are characteristic of the SiH_4 molecule [Beck 2002]. The SiH_4 depletion fraction, *D,* can then be accessed according to

$$D = 1 - \frac{A_{SiH_4}^{on}}{A_{SiH_4}^{off}} \qquad (1)$$

where $A_{SiH_4}^{on}$ and $A_{SiH_4}^{off}$ are the absorbances measured at the relevant wavenumber before and after ignition of the plasma, respectively. The silane depletion is a direct consequence of the reduction of silane partial pressure due to dissociation by the plasma. Silane dissociation into radicals (Si, SiH, SiH_2, SiH_3) is essential for film growth. Notably, SiH_3 has a low reactivity and therefore long-lived nature, and is often argued to be the dominant film growth precursor for high-quality a-Si:H and µc-Si:H films [Matsuda 2004a]. Next, the silane concentration in the plasma, c_p, is defined as

$$c_p = c\,(1 - D) \qquad (2)$$

where *c* is the input silane concentration before plasma ignition. For the gases used in this study, *c* is the silane flow rate divided by the total flux in standard cubic centimeters per minute

[Strahm 2007c]. Thus, c_p is directly linked to the flux ratio of hydrogen atoms and silane radicals arriving at the growing film surface. Low c_p values imply that a significant fraction of SiH_4 is dissociated into radicals. Conversely, high values indicate low depletion in the plasma [Matsuda 2004b]. Strahm *et al.* demonstrated that this parameter is fundamentally linked to the microstructural transition from amorphous to microcrystalline silicon [Strahm 2007c]. We will also use c_p in this study and confirm its relevance for the growth of epitaxial silicon films.

As c_p is of interest, we now briefly discuss a simple way to experimentally access this parameter.First, we estimate the maximum possible deposition rate, R_{max}. For this, we assume that all present Si atoms injected in the reactor volume contribute to the film growth, which yields [Strahm 2007c]

$$R_{max} = \frac{\Phi_{SiH_4} V m_{Si}}{A\,\rho}\,, \quad (3)$$

where Φ_{SiH_4} is the molecular flux in $particles\,m^{-3}s^{-1}$, V the reactor volume, A the area of the reactor exposed to the plasma and ρ the silicon density. Using the ideal gas equation, the molecular flux can be converted into the flow rate in standard cubic centimeters per minute (sccm):

$$R_{max} = 20.97\frac{F_{SiH_4}}{A\,\rho}, \quad (4)$$

with F_{SiH_4} being the silane flow rate. If we consider deposition on glass of a-Si:H or µc-Si:H, the hydrogen content of the film can be assumed to be around 10% (2180 kg/m^3). Second, the silane dissociation efficiency, defined as the ratio between the measured deposition rate R and ideal R_{max}, is linked to c_p in a simple plasma model as follows [Strahm 2007a]:

$$\frac{R}{R_{max}} = \frac{c - c_p}{c(1+c_p)}. \quad (5)$$

With this simple model, measuring the deposition rate gives an estimate of the c_p value in the plasma. This method is valid only if no powder, dust or polysilane molecules (Si_2H_6, Si_3H_8,…) are formed in the plasma. These species are formed by secondary reactions. To verify this simple model experimentally, in Figure 3.10 we show for various plasma conditions the linear dependence between c_p values obtained by optical measurements using the quantum cascade laser and those obtained by the growth rate method. We see a slight but systematic overvaluation of c_p by the growth rate method, which may come from the limits of the used plasma chemistry model and the non-uniform deposition in the reactor.

The three data points which are clearly off the trend line stem from dusty plasma regimes and were not taken into account for the fitting. The formation of powder occurs in regimes at high pressure, high RF power or high silane concentration.

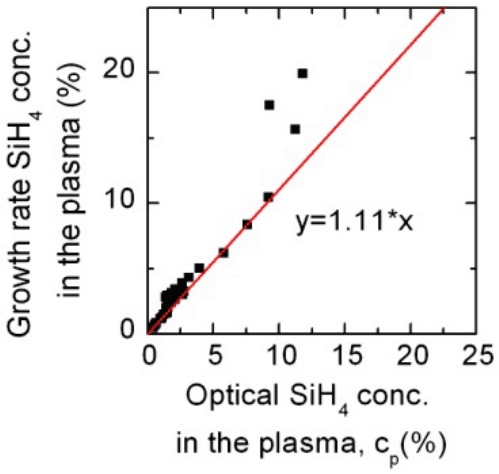


Figure 3.10: Relation between c_p obtained by optical measurements using a quantum cascade laser and obtained using the growth rate method. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

3.4.2.3 Results and discussion

3.4.2.3.1 Determining parameters for epitaxial growth

In this section, the plasma conditions triggering the a-Si:H, the µc-Si:H and the epitaxial c-Si growth modes are determined. First, for reference, we plot in Figure 3.11 (a) the Raman crystallinity fraction of films deposited on glass as a function of c_p. On this type of substrate, µc-Si:H growth occurs for low c_p (< 1%), whereas for higher c_p (> 2.7%) the deposited films are fully amorphous. These two growth modes are separated by a transition regime in which both a-Si:H and µc-Si:H growth may happen. This graph clearly demonstrates a direct correlation between the phase of the deposited films and c_p, confirming earlier findings [Strahm 2007c].

Deposition on a substrate precoated with µc-Si:H (70% Raman crystallinity fraction, without native oxide removal) provides a similar c_p dependence as on glass, as seen in Figure 3.11 (b). As the optical penetration depth of the used Raman laser (~50 nm in a-Si:H and ~150 nm in µc-Si:H) is less than the film thickness, the µc-Si:H underlayer should not contribute to the Raman signal. In this figure, we see that the transition regime is not shifted with respect to c_p when changing the substrate surface. However, in the transition regime, we observe a higher Raman crystallinity fraction of these samples compared to a deposition directly on glass. Despite the presence of a surface oxide on the µc-Si:H substrate, this increase likely stems from the promotion of additional nucleation sites due the local underlying crystalline structure.

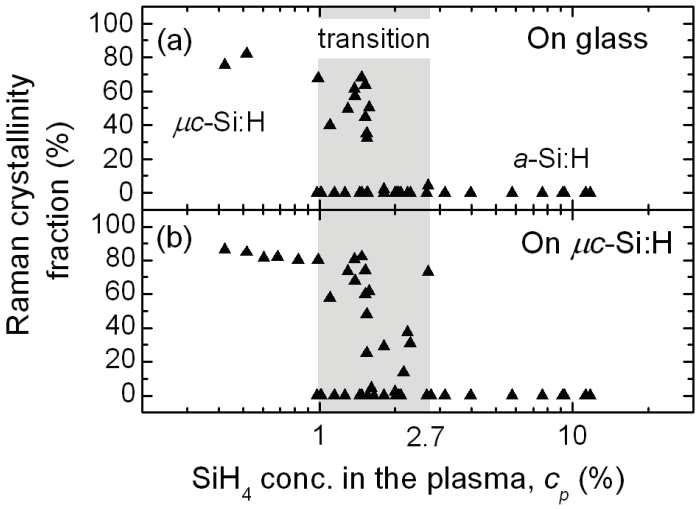


Figure 3.11: Raman crystallinity fraction as a function of c_p on (a) a glass substrate and (b) a µc-Si:H layer (70% Raman crystallinity fraction). The deposition pressure (1–7 mbar), power (0.098–0.42 W cm^{-2}), and gas flux were varied at a fixed reactor temperature to change c_p. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

Figure 3.12 shows film growth on a perfectly crystalline substrate, i.e. a mirror-polished <100> c-Si wafer after native oxide etching in HF. Again we observe three main growth modes, where now low c_p conditions result in epitaxial rather than µc-Si:H growth. The similarity in the c_p dependence confirms that c_p is a fundamental parameter for epitaxial growth as well, underlining how plasma conditions directly dictate the phase of the growing film. We observe that the transition region lies now at higher c_p values (3% ≤ c_p ≤ 9%), compared to the previously discussed cases.

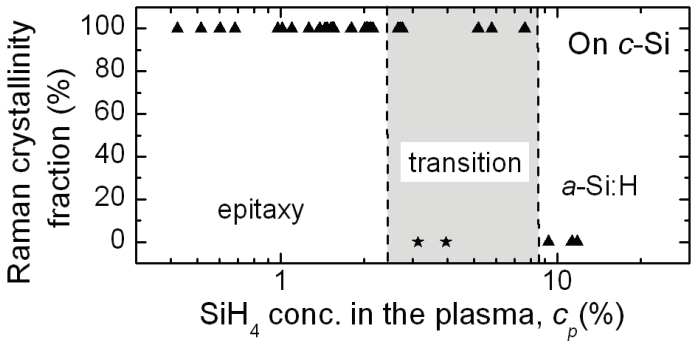


Figure 3.12: Raman crystallinity fraction as a function of c_p for <100> c-Si substrates. The stars indicate epitaxial breakdown after 2–5 nm growth, as observed by TEM (micrograph not shown here). The deposition pressure (1–7 mbar), power (0.098–0.42 W cm^{-2}), and gas flux were varied at a fixed reactor temperature to change c_p. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

For epitaxial film growth, the transition from epitaxial to amorphous growth may occur as well (stars in Figure 3.12), which is usually referred to as epitaxial breakdown [Eaglesham 1995, Karpenko 1997]. This phenomenon is not studied here and its dependence on c_p is unknown. The absence in the transition regime of data points with partial crystallinity between 1 and 99% is related to the optical penetration depth of the Raman laser: if epitaxial breakdown occurs at a depth > 50 nm measured from the top surface, Raman spectroscopy will probe only the amorphous part of the deposited layer. For c_p < 3%, sustainable epitaxial growth is observed up to the deposited thickness for these films. However, for c_p < 1%, we will show in section 3.4.2.3.3 that these films are very defective, pointing to a fourth growth regime.

Even though the data in Figure 3.12 prove that c_p plays an essential role, it cannot be the only parameter dictating the phase of the deposited film in the transition regime. Arguably, the mean free path length of the adatoms on the film growth surface must be equally important. Several factors impact this parameter, such as the surface microstructure, the deposition rate, the deposition temperature, deposition-related ion bombardment, and other deposition-specific parameters [Kalache 2003]. In the following paragraphs, we briefly discuss two of these factors, the surface microstructure and deposition rate, as the other parameters cannot be easily accessed.

First, we consider co-deposition of films on <100> and <111> wafers, of which cross-sectional TEM micrographs are shown in Figure 3.13 (a) and (b). The growth on the <100> surface is homo-epitaxial, whereas the one on the <111> substrate is purely amorphous. This dependence of the growth mode on the crystal orientation can have significant implications for fabrication of devices such as silicon heterojunction solar cells [Das 2008]. Such solar cells usually feature textured surfaces obtained by alkaline etching of <100> wafers, yielding pyramids with <111> facets. Practically, however, epitaxial needles may be initiated, when the surface orientation locally deviates from the <111> pyramidal facets (Figure 3.13 (c)), due to locally non-ideal surface texture. This difference in growth mode between <100> and <111> surfaces is in line with earlier findings using PECVD [Levi 2006, Roca i Cabarrocas 2012]. The origin of this phenomenon has been elusive. Interestingly, this crystalline-orientation-dependent growth mode shows a striking resemblance with observations made for low-temperature epitaxial growth using MBE in ultra-high vacuum conditions [Gossmann 1985]. In the latter case, the presence of strings of Si(100)-(2×1) dimers are known to play an essential role for epitaxial growth [Hamers 1990, Metiu 1992]. An ideal <111> surface contains only a single silicon dangling bond per surface atom, whereas for <100> surfaces two dangling bonds are present (insets in Figure 3.13 (a) and (b)). Such ideal <100> surfaces can easily reconstruct: between the dangling bonds of adjacent surface atoms, a σ bond—the so-called dimer bond—is formed [Appelbaum 1976, Hamers 1990]. Such dimers are unique to the Si <100> surface and strongly depend on the specific surface preparation [Gielis 2008, Neuwald 1993]. On Si(100)-(2×1) reconstructed surfaces, epitaxial growth then occurs as long dimer strings, perpendicular to the present surface strings, at remarkably low temperatures. This phenomenon is unknown for <111>

surfaces, for which significantly higher temperatures are usually needed and where epitaxial growth follows island formation [Jona 1966]. For our PECVD experiments, even though the involved surfaces are far from ideal [Beyer 1998, Kitagawa 2000, Matsuda 2004a], we speculate that the microscopic differences between <100> and <111> surfaces during deposition critically affect the phase of the deposited material.

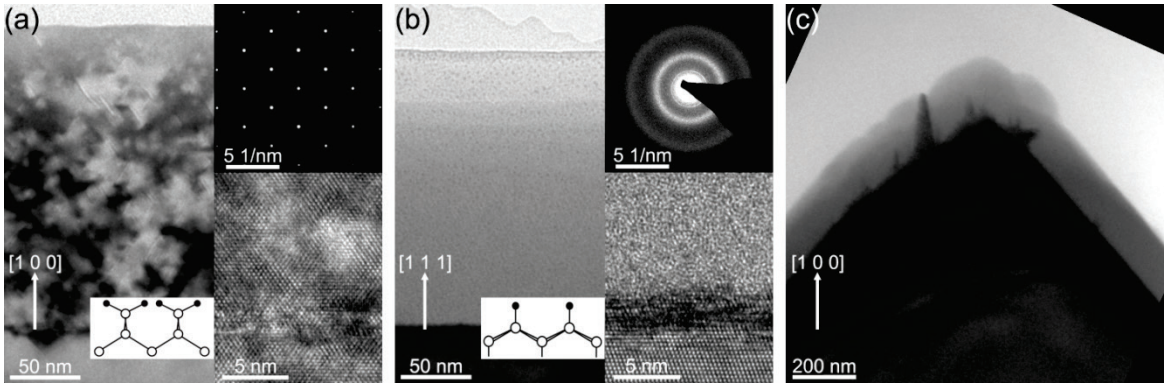


Figure 3.13: TEM micrographs of co-deposited at c_p = 1.1% on wafers with (a) a <100> orientation, (b) a <111> orientation and (c) a <100> textured surface. (a) and (b) (left) A TEM bright-field (BF) micrograph, (top right) a selected-area diffraction pattern from the film, and (bottom right) a HRTEM micrograph of the substrate-film interface. The film deposited on <100> preserves crystalline, epitaxial growth throughout its thickness, while that deposited on <111> is fully amorphous after ~3 nm of highly defective initial epitaxial growth. Insets in the BF micrographs show schematic illustrations of the unreconstructed surface termination of H atoms (filled circles) bonded to the Si atoms (open circles) for both crystalline orientations. The film in (c) grown on a textured substrate is also fully amorphous except close to the tip of the pyramid, where the surface deviates from a <111> orientation; here small crystalline needles are observed in the otherwise amorphous film. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

Second, Figure 3.10 (a) shows the Raman crystallinity fraction of different films as a function of their deposition rate. Outside the transition regime, the deposition rate can vary significantly without impacting the growth mode. Conversely, in the transition regime, the growth mode is markedly influenced by the deposition rate, since increasing deposition rates will lower the mean free path length of the adatoms, suppressing the probability of crystalline film growth.

Combining all our findings so far, we draw a simplified view of the amorphous-to-crystalline transition during PECVD using only two main parameters: the SiH_4 concentration in the plasma, c_p, and the mean free path of the adatoms on the film growth surface. This is illustrated in Figure 3.14 (b). The width of the transition regime in our model stems from additional 'hidden' parameters, including ion bombardment [Feltrin 2008] and secondary radical gas phase reactions (e.g. Si_2H_5, etc.) which could decrease the number of adatoms without altering c_p [Strahm 2007c].

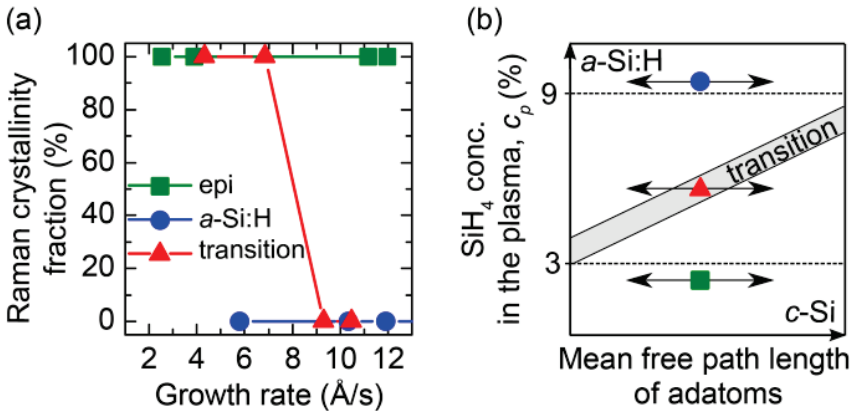


Figure 3.14: (a) Raman crystallinity fraction of films deposited on a <100> wafer as a function of the growth rate in the amorphous, epitaxial, and transition regimes (blue circles, green squares and red triangles, respectively). (b) Schematic representation of the amorphous-to-crystalline transition for plasma-deposited Si films. The symbols correspond to the approximate c_p value of the corresponding data series of (a). Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

3.4.2.3.2 Interface layer of epitaxial films

The surface structure and plasma conditions influence nucleation, as discussed in the previous sections. However, impurities in the reactor may also affect growth of the first few nanometers, which we now discuss.

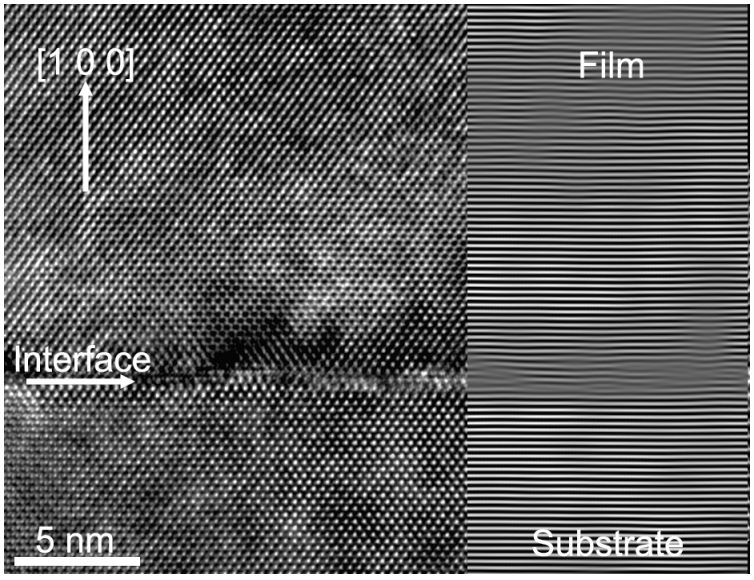


Figure 3.15: HRTEM micrograph of the interface between an epitaxial film grown on a c-Si substrate. The contrast change and discontinuity at the substrate surface represent the sub-nm interface layer discussed in the next section, as emphasized by Fourier-filtering on the (2 0 0) plane on the right-hand side. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

The presence of a thin interface layer between the c-Si substrate and PECVD epitaxial film is indicated in the HRTEM micrographs shown in Figure 3.15. Such interface layers have been reported for epitaxial layers grown by low-temperature MBE [Grunthaner 1989], hot-wire CVD [Teplin 2006] and PECVD [Moreno 2010, Rizzoli 2002].

We now address the question of why such an interface layer occurs and start by analysing its composition. SIMS measurements point to an excess of hydrogen and oxygen (Figure 3.16) at this interface. Hydrogen is abundantly present in the plasma and may thus indeed easily be incorporated in the deposited films. Conversely, oxygen could originate only from a remaining native oxide film prior to deposition, or from oxygen contamination in the reactor or gas bottles.

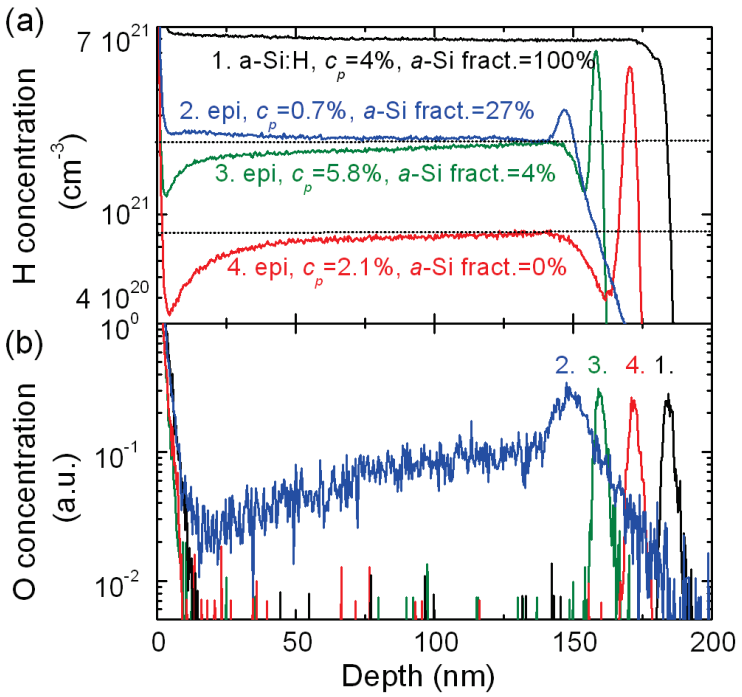


Figure 3.16: (a) Hydrogen and (b) oxygen depth profiles, obtained from SIMS, of four films deposited at different c_p values and containing various amorphous fractions (see section 3.4.2.3.3). The film surface is at zero depth and its thickness varies between 150 to 200 nm. Excess hydrogen and oxygen are observed at the interface between the grown film and the c-Si wafer. The trailing edge of the sample (c_p = 0.7%) is due to the rough surface of the sample, which blurs the interface. The dotted lines are guides for the eye. Films with 3% < c_p < 9% are in the transition regime. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

Interestingly, in spectroscopic ellipsometry (SE) measurements, this interface layer yields interference fringes that occur between photon energies from 1 to 3 eV (due to light reflected at this interface and the surface roughness layer) [Teplin 2005]. These interferences allow accurate monitoring of the interface and epitaxial layer thicknesses by SE data fitting. To model this

interface layer, an effective medium approximation (EMA) of c-Si bulk material and voids is used. If these interferences are absent (because the interface layer is either too thin or simply absent), the thickness of the epitaxial layer can be determined only by co-deposition on an amorphous test-substrate, assuming similar growth rates for both substrates. Intriguingly, we deduce from Figure 3.17 (a) that the interface layer thickness does not depend on the amount of time the wafer surfaces are exposed to air after native oxide removal and loading in the reactor. Its thickness rather depends on the number of subsequent depositions in the reactor (Figure 3.17 (b)). This strongly suggests that the interface layer thickness depends on the presence of impurities such as oxygen in the reactor, which accumulate in the reactor for each loading and unloading of the samples. The decreasing oxygen content throughout the film grown at very low c_p confirms this hypothesis. For these conditions, a high impurity concentration could further be explained by the very low growth rate of these films (< 2 Å s^{-1}), which enables more impurities to be incorporated [Torres 1996].

To avoid the presence of such undesired oxygen at the interface between the substrate and the epitaxial layer, the reactor was cleaned using a nitrogen trifluoride or a sulfur hexafluoride plasma with subsequent conditioning of the reactor following each deposition. The pumping time was kept constant between the cleaning and the deposition. Under such conditions, for the samples in Figure 3.12, we observe a direct dependence of the interface layer thickness on the tested deposition parameters (dilution, power and pressure, see Figure 3.17 (c), (d) and (e)). Each of these tested parameters influences c_p. In Figure 3.17 (f), we plot the interface layer thickness as a function of these corresponding c_p values and for the remaining data from Figure 3.12, allowing for direct comparison of each deposition parameter. Here, we observe a certain spreading in the data, indicating that the interface layer thickness does not depend solely on the plasma parameters.

3.4.2.3.3 Epitaxial bulk

Following the first nanometers of growth, further crystal propagation depends mainly on the conditions in the plasma. To determine which conditions yield high-quality epitaxial films, we discuss now the microstructural quality of the epitaxial bulk films.

For this purpose, we took SE data of the samples discussed in Figure 3.12. These data were then fitted using an EMA featuring c-Si and a-Si:H fractions [Levi 2006, Teplin 2006], from which a qualitative estimate of the amorphous fraction of the deposited films can be made, as plotted in Figure 3.18. This SE amorphous signature observed in several epitaxial films probably stems from bonds with non-ideal angles and lengths compared to c-Si bonds. We note that Raman spectroscopy did not offer sufficient sensitivity to probe such differences (Figure 3.12). We observe here the presence of a possible fourth regime for very low c_p values [Tsai 1991], in which the layers show a high amorphous fraction, which we discuss below.

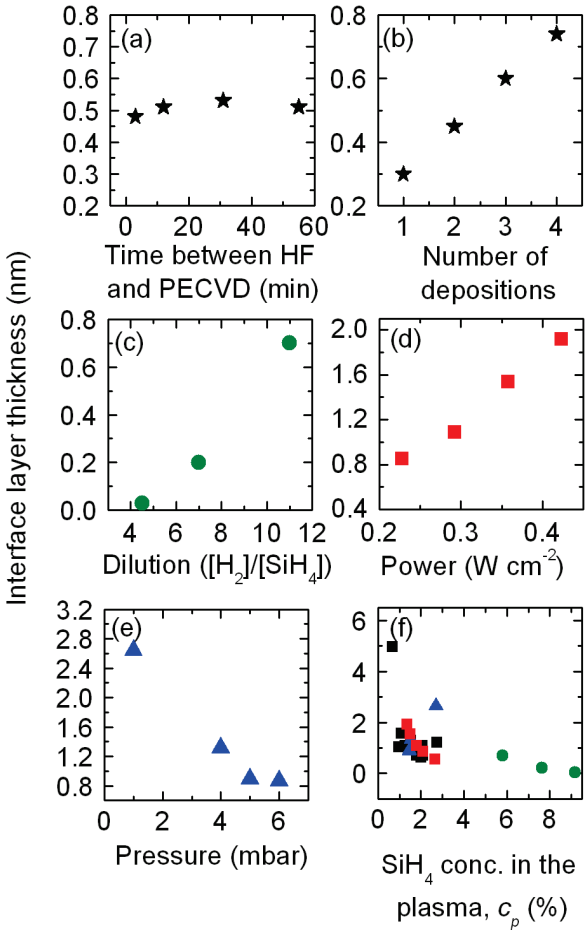


Figure 3.17: Dependence of the interface layer thickness on (a) the time elapsed since HF etching of the native oxide, (b) the number of subsequent depositions in the reactor keeping a constant pumping time after sample loading, (c) the H_2 dilution (green circles), (d) the RF power density (red squares), (e) the reactor pressure (blue triangles), and (f) c_p. The black squares are other data points from samples in Figure 3.12. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

To reveal the microscopic structure and local details of the films and to relate them to the SE data, we also performed cross-sectional analysis using HRTEM imaging. Our epitaxial layers typically contain dislocations or dislocation loops on {1 1 –1} planes, as for instance shown in Figure 3.19. This micrograph was taken from the middle (bulk) of a 90-nm-thick layer deposited at c_p = 1.6%. We see a clear correlation between the defect densities extracted by HRTEM and bright-field (BF) TEM and the amorphous fraction in deposited films extracted by SE (data not shown).

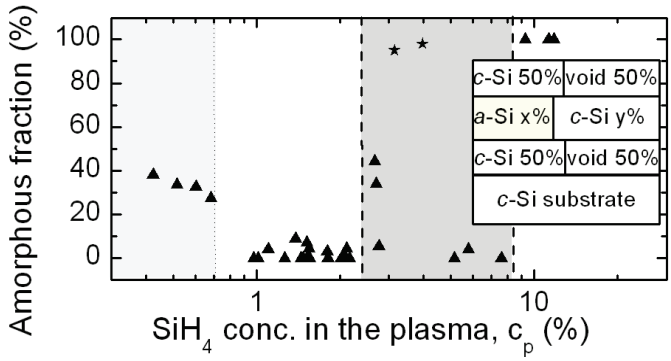


Figure 3.18: Ellipsometry data fitted using the model shown in the inset. The stars indicate epitaxial breakdown after 2–5 nm of growth, observed by TEM. The model uses an EMA of c-Si and void to simulate the interface layer between the substrate and the film (see section 3.4.2.3.2). The second and third layers from the substrate represent the epitaxial and the roughness layer (c-Si and void), respectively. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

STEM BF micrographs of layers deposited at very low c_p values reveal that such films are indeed composed of both amorphous and crystalline regions. EDX analysis of such films, shown in Figure 3.20 (b), reveals that oxygen is present within the film in the form of irregular hazy layers. Fourier filtering obtained at different positions of a HRTEM micrograph (Figure 3.20 (c)) demonstrates that the film features epitaxial as well as amorphous regions. Notably, the regions rich in oxygen correspond to the amorphous zones. Likely, the (unintentional) incorporation of oxygen provokes a disruption of crystalline growth. In addition, we observe a rotation of a few degrees in the crystalline orientation of the growing layer in this sample, possibly due to an accumulation of dislocations or cracks. On a glass substrate and in such low c_p regimes, the layer peels off as soon as it is exposed to air, indicative of high stress buildup in the deposited material. Decreasing c_p even further provokes wafer etching [Geissbühler 2013].

To further investigate the bulk quality of the epitaxial layers, we turn back to the SIMS results shown above (Figure 3.16). Expectedly, the amorphous film has the highest hydrogen content, while the epitaxial films grown at very low c_p (c_p = 0.7%) and in the transition regime (c_p = 5.8%) show a hydrogen density of about 2×10^{21} cm^{-3}. Finally the purely crystalline (a-Si:H content of 0%) epitaxial layer, deposited at c_p = 2.1%, has the lowest bulk hydrogen content. The epitaxial film grown in the transition regime (c_p = 5.8%) has a higher hydrogen content than the one grown in the nearby epitaxial regime (c_p = 2.1%). This c_p dependence of the hydrogen incorporation is similar to that observed for µc-Si:H film growth, for which the transition regime contains the highest hydrogen content [Kroll 1996]. We remark that the hydrogen content throughout the film may either decrease (films with c_p = 4% and 2.1%) or increase (films with c_p = 0.7%) with thickness.

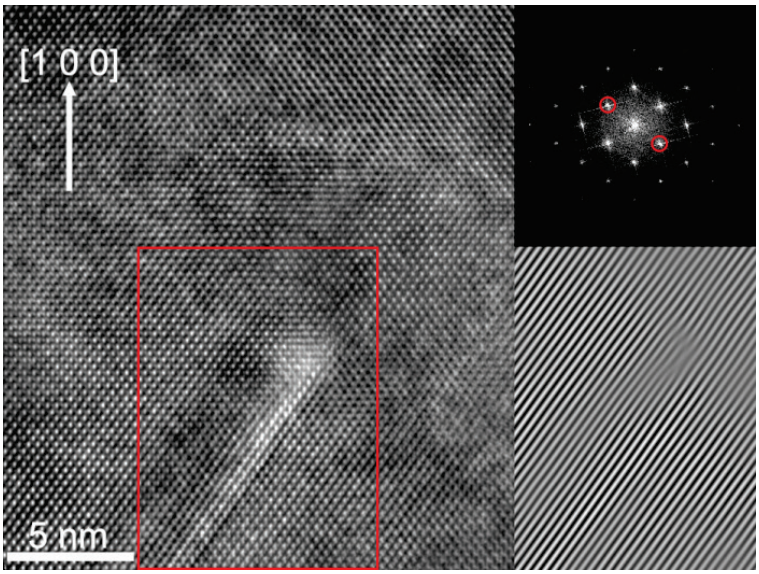


Figure 3.19: HRTEM micrograph of the bulk of an epitaxial layer with a dislocation/dislocation loop on a {11–1} plane in the region marked by the red box. The top right inset shows the diffractogram of the region marked in the red box; Fourier filtering of the region marked in red using the {11–1} planes indicated by red circles in the diffractogram highlights the plane termination at the end of the dislocation (bottom right inset). Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

Quite generally, in epitaxial as well as in microcrystalline films, compressive stress—linked to the hydrogen content of the films [Kroll 1996, Shahrjerdi 2012]—may cause defects or a distortion of the crystalline lattice. We now briefly outline how the observed differences in hydrogen content in our films may be traced back to their precise deposition details. According to the different film growth models available in the literature [Matsuda 2004b], hydrogen can (1) enhance the diffusion process of SiH_3 by full surface coverage and local heating (surface diffusion model),[5] (2) break weak Si-Si bonds (etching model) and (3) penetrate the subsurface region and cause crystallization (chemical annealing model). Therefore, we have two fundamentally opposing effects of hydrogen: hydrogen promotes epitaxial growth, and conversely when incorporated in the film, it can then distort the crystalline lattice, ultimately yielding epitaxial breakdown. These two effects compete with each other and explain why sustainable epitaxial growth only occurs for intermediate c_p values.

[5] For ultra-high vacuum epitaxy at high temperature (MBE), hydrogen hinders the diffusion of the Si species, which disrupts the layer-by-layer growth on the bare surface and builds up surface roughness which could eventually lead to a crystalline-to-amorphous transition.

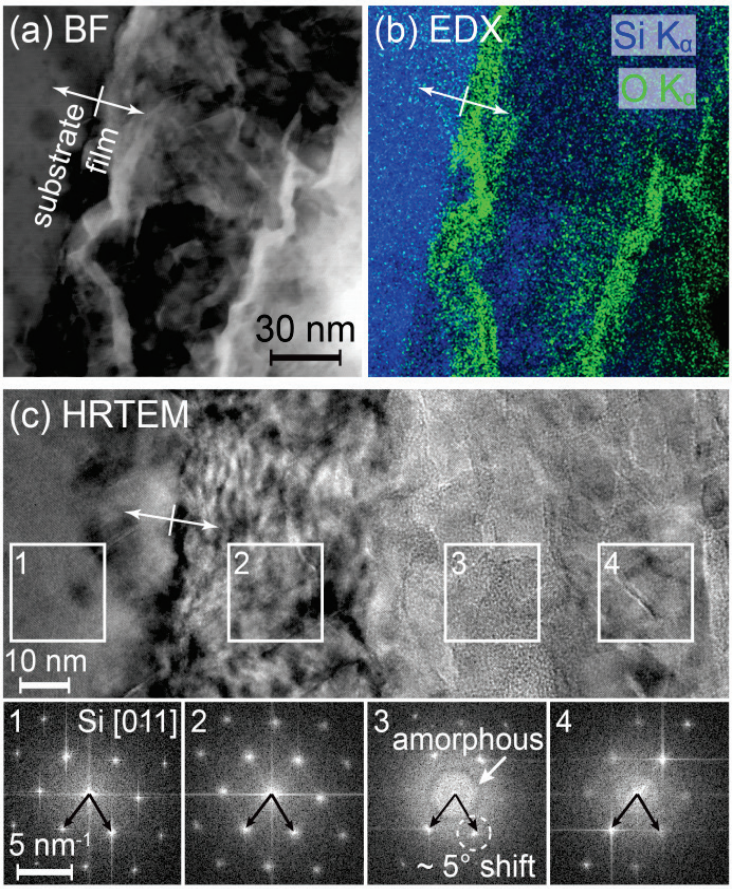


Figure 3.20: STEM micrographs of a low c_p sample (0.7%). (a) STEM BF micrograph and (b) STEM EDX map of the BF micrograph. (c) HRTEM of the first 100 nm of a film and diffractograms of the four regions marked in white boxes. Starting from the c-Si substrate (region 1), epitaxial growth (regions 2 and 4) is observed to alternate with a-Si:H growth (region 3). Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

Summarizing our findings so far, from previous studies linking plasma conditions to deposited material quality, device-grade µc-Si:H on glass should be deposited close to the amorphous-to-crystalline silicon transition, i.e. in the transition regime of Figure 3.11 (a) [Mai 2005, Vetterl 2000]. The validity of this argument was extended for thin-film a-Si:H absorber layers, as well as for layers designed for c-Si surface passivation [Descoeudres 2010]. For epitaxial films, it also appears that bulk quality deteriorates for films deposited far away from the transition region, namely under very low c_p conditions. However, in the transition regime, the epitaxial film contains more hydrogen than in the nearby epitaxial regime, and hydrogen strains the crystalline lattice and creates defects. Hence, for high-quality bulk epitaxial films, the ideal conditions appear to be close to but not necessarily within the transition regime. Conversely, in the case of µc-Si:H layers, the higher hydrogen content in the transition regime has rather a beneficial effect and likely passivates the grain boundaries, leading to higher open-circuit voltages in solar cells [Johnson 2008, Kroll 1996]. Moreover, the stress induced by this excess of hydrogen in the µc-Si:H layers can be accommodated by the flexible amorphous network around the crystalline

grains, which is not the case for an epitaxial film. These two reasons could explain why, microscopically, high-quality epitaxial films are obtained at lower c_p values than are necessary for high-quality µc-Si:H layers.

Figure 3.21 illustrates the three main regimes outlined in this section: (1) defective epitaxial layers are grown with very low c_p values, (2) the least defective layers are grown close to the transition regime, and (3) the thinnest interface layers are obtained close to the amorphous regime.

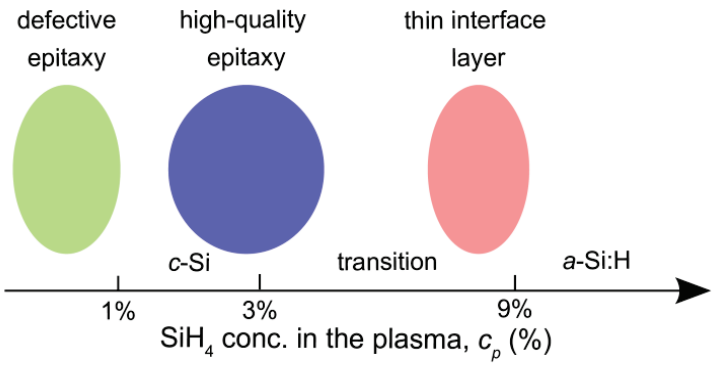


Figure 3.21: Sketch of the growth regimes as a function of c_p, leading from poor-quality epitaxial growth (green region) to high-quality epitaxial growth (blue region) and to a thin interface layer (red region).

3.4.2.3.4 Electronic properties of epitaxial layers and consequences for solar cells

Finally, to verify the electronic quality of the deposited films, photoconductance measurements were performed on symmetrical samples composed of an epitaxial layer and a passivating intrinsic a-Si:H layer. As stated earlier, we used exclusively high-quality wafers and we know that the amorphous passivating layers are excellent. Hence, carrier lifetime measurements of such samples are ideal probes to assess the electronic quality of the deposited epitaxial films. Figure 3.22 shows how the carrier lifetime of a wafer featuring such epitaxial / a-Si:H(i) layer stacks varies as a function of the thickness of the interface between the wafer and the epitaxial layer. The data presented here were obtained by growing epitaxial films using increasing hydrogen dilution in the plasma. For this series, TEM micrographs show that the number of defects in and the thickness of the interface layer between the wafer and the epitaxial film do not dictate the bulk epitaxial quality. Indeed, starting from a thick interface layer, the bulk epitaxial layer can exhibit fewer defects compared to the case with a thin interface layer (micrographs not shown here). From this, we conclude that the defects at the interface and within the interface layer limit the effective carrier lifetime of these samples.

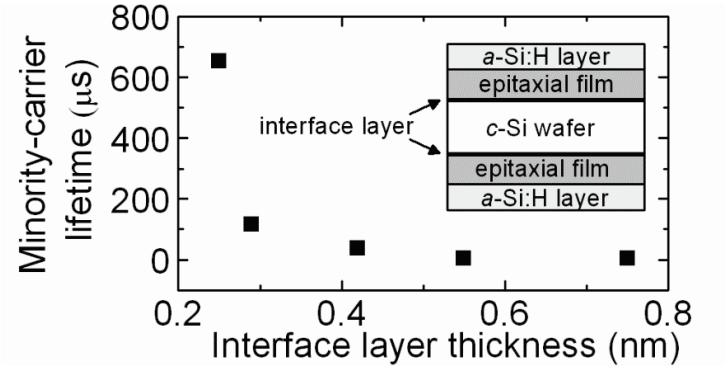


Figure 3.22: Minority-carrier lifetime as a function of the interface layer thickness for 130-nm-thick epitaxial films deposited at different c_p. Reprinted with permission from [Demaurex 2014a] © 2014 American Institute of Physics.

As a consequence, if the epitaxial layer is used to form the electron or hole collector of a device (either as the emitter or back-surface field), the defective interface layer should be as thin as possible to avoid increased recombination losses. To accomplish this, the first nanometers should be deposited in a regime as close as possible to the amorphous-to-crystalline transition. Subsequently, to sustain a device-grade epitaxial layer, the deposition conditions should be changed to lower c_p values, as discussed in section 3.4.2.3.3 [Ryuichi 2007]. Conversely, if the epitaxial layer is grown as an optically active absorber (i.e. as the replacement for a c-Si wafer), the interface layer can be maximized to act as a weak layer that can later be exploited to separate the thin film from the wafer as suggested in [Moreno 2010].

3.4.2.4 Conclusions

Low-temperature epitaxial growth by PECVD could have a wide range of applications in advanced-design semiconductor devices if the determinant parameters for such growth are understood and mastered. We have shown that the silane concentration in the plasma, c_p, is a crucial parameter for determining the growth mode of epitaxial silicon thin films on c-Si substrates. However, the mean free path of adatoms, which is influenced by substrate type and growth rate effects, also plays an important role. The bulk of the epitaxial film is found to show fewer dislocations and lower hydrogen content for films close to the amorphous-to-crystalline transition regime. Between the epitaxial layer and the c-Si substrate, an interface layer limits the minority-carrier lifetime. The thickness of this interface layer—a porous layer with an excess of hydrogen and oxygen—depends not only on the conditions in the plasma but also on impurities in the reactor. The layer thickness is effectively reduced by using c_p in the transition regime and by cleaning the reactor between each deposition. Therefore, to grow a high-quality epitaxial layer with the thinnest possible interface layer, we suggest a two-step process composed of a high c_p step to grow the first nanometers and then a lower c_p step to have stable, high-quality epitaxial growth.

3.4.3 Doped homo-epitaxial layers

We have now determined the region of interest to grow the best-quality intrinsic homo-epitaxial layers. To form the emitter, we need to dope the layer. For this purpose, a phosphine (PH_3) flux is added during the film growth. We first investigate the impact of adding a PH_3 flux to the deposited films and then quantify the active dopants in the epitaxial films.

3.4.3.1 Effect of phosphorus atoms on growth properties

To investigate the effect of phosphorus atoms in the plasma on the film quality, epitaxial layers were deposited on an n-type mirror-polished c-Si <100> wafer by changing the H_2 flux while maintaining the SiH_4 flux constant. The phosphorus-doped layers were obtained by adding a PH_3 flux. As phosphine in gas bottles is diluted in molecular hydrogen (2% phosphine), the H_2 flux was adjusted to maintain a similar H_2 flux in the reactor as in the intrinsic deposition conditions.

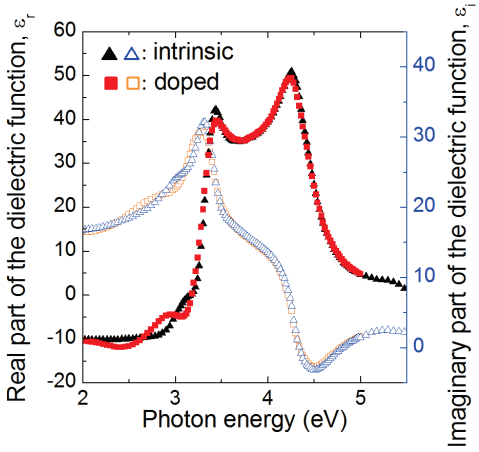


Figure 3.23: Spectroscopic ellipsometry data of an intrinsic and phosphorus-doped epitaxial film obtained using the SiH_4 and H_2 fluxes and adding a PH_3 flux for the doping.

To characterize the layers, SE is again used. However, the integration of dopants is observed to perturb the well-ordered diamond cubic crystal structure of silicon: the Si critical points at 3.4 and 4.7 eV are less pronounced (Figure 3.23) and the corresponding peaks broadens.

Using the model described in section 3.4.2.3.3, the amorphous fraction can be accessed. In the transition regime, as c_p decreases, the amorphous fraction of an intrinsic epitaxial layer decreases, as shown in Figure 3.24. Conversely, we observe that the phosphorus-doped epitaxial layer has an increasing disorder in its lattice. This could be explained by the non-linear incorporation of phosphorus in the homo-epitaxial films [Shahrjerdi 2012]. In Figure 3.24, we also observe an intrinsic homo-epitaxial film become amorphous when a phosphine flux is added. This points to a shift of the transition regime to lower c_p values.

When a trimethylboron (TMB) flux is added to the SiH_4 and H_2 fluxes to obtain a boron-doped layer, no epitaxial growth was obtained. The TMB was diluted in 2% H_2. From microcrystalline growth conditions, it is well established that boron disrupts the crystalline growth and that very small fluxes are required to achieve p-type microcrystalline growth [Cuony 2010, Flückiger 1994, Jenq-Shiuh 1992, Saleh 2003]. In the case under study, a more diluted bottle is needed. This was not further investigated.

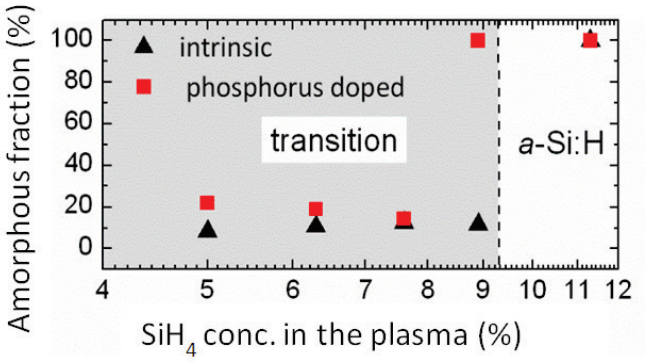


Figure 3.24: Amorphous fraction of intrinsic and phosphorus-doped homo-epitaxial films for a dilution series.

3.4.3.2 Characterization of phosphorus-doped epitaxial layers

In this section, we investigate several methods to characterize the dopant concentration in the homo-epitaxial layers.

Phosphorus-doped epitaxial samples were deposited on a mirror-polished 2 Ωcm p-type c-Si <100> wafer. The phosphine flux was modified, while maintaining a constant c_p value of 1.3%. The dopant concentration in the plasma is defined as the ratio between the phosphine flux and the silane flux.

To characterize the films conductivity, several methods were evaluated: transfer length measurement (TLM), Hall measurement and dark conductivity measurements. Hall measurements were typically found to be sensitive to how the contact between the probes and the layer is made, i.e. with simple pressure on the pins or with soldered contacts. TLM measurements as well as the dark conductivity measurements required us to cleave the sample to the size of the pads, which prevented current from flowing on the pads sides. When a sample was not cleaved, this undesired current flow typically decreased the sheet resistance by a factor of 1.5. To form the contact, aluminum (Al) and silver were both compared. Both contacts gave similar results. These two measurement techniques gave results within a 25% range. Finally, dark conductivity measurements with Al contacts were used to characterize the epitaxial layers, as it is a standard technique used in the thin-film industry.

For dark conductivity measurements, a thick (≈100 nm) layer was deposited on a p-type wafer, forming a pn-junction. Two Al contacts were then evaporated on the film at a distance of

0.5–1 mm from each other to form an ohmic contact with the layer. The lateral conductivity is then monitored as a function of temperature in the dark and in a 1 mbar nitrogen environment. By fitting the Arrhenius plot, an activation energy, $E_{a,}$ and a dark conductivity, σ, value can be extracted:

$$\sigma(T) = \sigma_0 e^{\frac{-E_a}{k_B T}}. \quad (6)$$

This conductivity dependence on temperature is valid only for extended state conduction. The most precise values for the conductivity are obtained by fitting the cooling ramp in the low-temperature range. In Table 1:2, the conductivity of different layers (amorphous and homo-epitaxial) deposited in the KAI-M reactor are given. The conductivity of the homo-epitaxial layers corresponds to a range close to a dopant concentration of 10^{19} cm^{-3}, as also evidenced by Figure 3.25. In the experimental range measured for these layers, increasing the dopant concentration increases the conductivity.

Table 3.1: Conductivity of a-Si:H layers measured by dark conductivity for various carrier concentrations measured by SIMS, of c-Si bulks calculated for different carrier concentrations, and of homo-epitaxial layers grown by PECVD for different phosphine-to-silane fluxes deposited in the KAI-M reactor.

	Carrier concentration (cm^{-3})	Dopant concentration $[PH_3]/[SiH_4]$	Conductivity, σ_{RT} ($S\ cm^{-1}$)	Activation energy, E_a (eV)
a-Si:H(n)	4E20		1E-02	0.183
a-Si:H(p)	1E21		4E-06	0.475
a-Si:H(i)	--		3E-11	0.786
c-Si(n)	1E19		184	--
c-Si(n+)	1E20		1246	--
c-Si(n-)	1E15		0.22	--
epi(n-)		0.04	129	0.0457
epi(n)		0.2	483	0.0400
epi(n+)		0.4	920	0.0029

A typical ECV profile of a phosphorus-doped epitaxial layer is shown in Figure 3.25. The active doping profile is abrupt and well defined compared to the previously discussed diffusion and ion implantation method. This underlines the unique precision of epitaxial layers. Cell results using epitaxial layers are presented in Chapter 5.

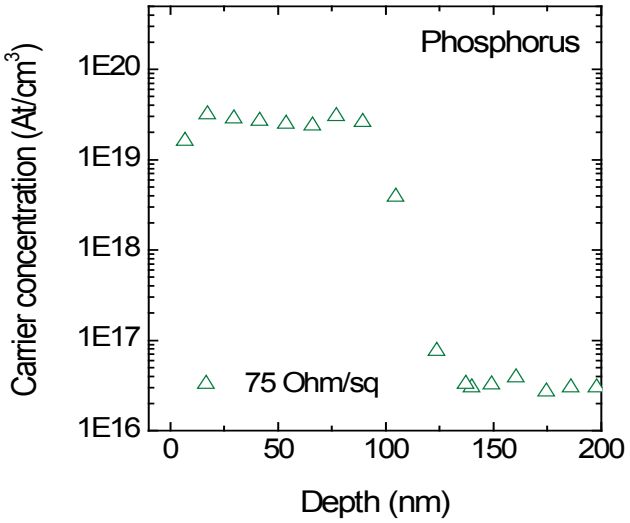


Figure 3.25: Electrochemical capacitance voltage technique (ECV) of a phosphorus-doped epitaxial layer.

3.4.4 Summary

First, adding dopants to a film having a sustainable epitaxial growth regime decreases the intensity of the critical points in a c-Si material, resulting in an increase in the amorphous fraction for these films. We show also that, when growing films with a phosphorus flux, the c_p values corresponding to the transition zone between the epitaxial and amorphous regimes are shifted to lower c_p values. These phosphorus-doped epitaxial layers may be efficiently characterized using dark conductivity measurements. A sharp and well-defined dopant profile may be obtained with an active dopant density of 3 10^{19} cm^{-3}.

3.5 Conclusion

Three methods to form a silicon homojunction were discussed. First, we presented several methods to obtain a highly doped surface on a single side of a c-Si wafer after a diffusion process. A dry etching process was shown to provide the best results in terms of passivation quality after processing and the shortest processing time. Second, ion implantation directly yielded a single-side highly doped surface, simplifying the solar cell process. Third, low-temperature (≤ 200 °C) plasma-enhanced chemical vapor deposition epitaxial growth was developed to form homojunctions. The silane concentration in the plasma, c_p, and the mean free path of adatoms, which is influenced by the substrate type and growth rate effects, play a crucial role to determine the growth mode. Between the epitaxial layer and the c-Si substrate, a defective interface layer is present. The thickness of this interface layer—composed of a porous layer with an excess of hydrogen and oxygen—depends not only on the conditions in the plasma but also on the impurities in the reactor We studied the plasma conditions and determined the conditions yielding high-quality epitaxial growth by minimizing, first, the thickness of the defective interface

layer and, second, the defects in the epitaxial bulk layer. Phosphorus doping of these layers was then achieved and active dopant concentration could be obtained up to 3 10^{19} cm^{-3} in the homo-epitaxial films.

Chapter 4 Silicon heterojunction solar cells

Passivating contacts are the key feature of silicon heterojunction solar cells. These passivating contacts consist of amorphous silicon layers which displace the highly recombinative metal contact from the optically active absorber (i.e. the silicon wafer) avoiding thus interface recombination. By doping of the amorphous silicon films, hole and electron collectors are formed. To provide lateral electrical conductivity and for improved light coupling into the device, transparent conductive oxides (TCO) are inserted in between the amorphous silicon films and metal overlayers, on the front as well as rear side. The general aim of our work is to apply such contacts to doped crystalline silicon surfaces, and to prove their merit in 'classic' homojunction cells. Specifically in this chapter, we focus on the contact fabrication steps, and their possible effects on the final contact performance.

First, we show that deposition of the TCO's using an aggressive technique such as sputtering can detrimentally affect the cell's internal voltage if no thermal post-deposition treatment is applied. Inserting a thin protective layer by a soft deposition technique such as atomic layer deposition prevents these losses. Secondly, the TCO work function is shown to play a crucial role in a-Si:H-based passivating contacts, affecting recombination and transport properties. We probe the interface TCO work function by two innovative techniques. The contact resistivity of the contact stacks is then investigated. The last section presents a method for fill factor (*FF*) analysis that points the way to improve this complex contact.

4.1 Introduction

Silicon heterojunction (SHJ) solar cells are silicon-wafer-based devices fabricated with thin-film deposition technology. The potential of this technology was recently demonstrated by implementing such contacts in an interdigitated-back-contacted solar cell, yielding a conversion efficiency of 25.6%, the highest-ever reported value for any silicon-based solar cell [Panasonic 2014]. The key features compared to conventional homojunction silicon solar cells are their passivating contacts, which enable extremely high open-circuit voltage (V_{oc}). This is underlined by reported values as high as 750 mV for 98-micron-thick wafers, approaching the theoretical V_{oc} limit for silicon-based solar cells (~770 mV for a 100-micron-thick wafer) [Taguchi 2014, Tiedje 1984]. Thanks to their high V_{oc}, SHJ solar cells have the advantage of having a low temperature coefficient and high performance ratio [Seif 2014]. The main drawback of SHJ solar cells is their somewhat modest current compared to other high-efficiency devices based on crystalline silicon (c-Si). These losses are due to parasitic absorption in the a-Si:H, TCO and metal layers [Holman 2012, Holman 2013b, Holman 2014]. To overcome these losses, three approaches are investigated: (1) reducing the parasitic absorption in the front layers by replacing the highly absorbing a-Si:H layer with other, less absorbing, materials [Battaglia 2014a, Seif 2014], (2) engineering the rear reflector [Holman 2013a], and (3) imple-

menting back-contacted SHJ solar cells, for which the front side can be optically optimized, as the contacts are at the rear of the device. A recent literature review on back-contacted SHJ solar cells may be found in [De Wolf 2014] and [Tomasi 2014]. Furthermore, a complete review of SHJ solar cells can be found in [De Wolf 2012a, De Wolf 2014, Fuhs 2006, van Sark 2011].

In this thesis, to form passivating contacts based for homojunction solar cells on a-Si:H/c-Si interfaces, the development of adapted heterojunction contacts is needed. For this reason, silicon heterojunction solar cells were developed and optimized, with a strong emphasis on contact formation and the contact's electrical properties. The sketch and band diagram of a front-emitter device are shown in Figure 3.1. The band diagram will be discussed in this chapter.

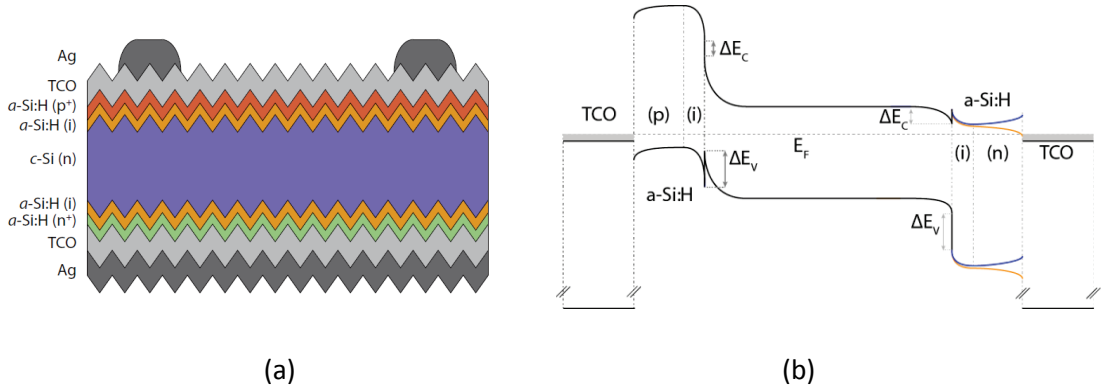


Figure 4.1: (a) Sketch and (b) band diagram of a silicon heterojunction solar cell. In (b) the yellow and blue lines indicate possible band bending depending on the work function mismatch between the a-Si:H(n) and TCO layers.

In this chapter, following a brief description of the fabrication process of SHJ solar cells in section 4.2, we focus on contact formation. In section 4.3.1, we report that the contact formation process damages the underlying amorphous / crystalline silicon interface passivation during TCO sputtering. We observe that this damage is at least partially caused by luminescence of the sputter plasma. Following low-temperature annealing, the electronic properties of the interface are mostly recovered. However, the silicon-hydrogen configuration of the a-Si:H film is permanently changed, as observed from infrared absorbance spectra. In SHJ solar cells, although the microstructure of an as-deposited film cannot be restored after sputtering, no significant losses are observed in the film's V_{oc}.

To confirm this, in section 4.3.2, we examine damage-free transparent-electrode deposition to fabricate high-efficiency amorphous silicon / crystalline silicon heterojunction solar cells. We investigate atomic layer deposited (ALD) aluminum-doped zinc oxide as a protective layer in our devices, inserted between the a-Si:H layers and sputtered contacts. We find that a 20-nm-thick protective layer suffices to preserve the pristineness of the a-Si:H layers beneath. Insertion of such protective ALD-prepared layers yields higher internal voltages. However, we identify the presence of a silicon oxide barrier layer between the a-Si:H and the ALD transparent electrode formed during processing acting as a barrier, impeding hole and electron collection.

Section 4.4 presents the characterization methods investigated and developed in this thesis to study these contacts. Eventually, a *FF* analysis method is presented.

4.2 Fabrication process of a silicon heterojunction solar cell

In this thesis, float-zone 2-4 Ωcm phosphorus-doped Topsil c-Si(100) wafers were used. Alkaline texturering was performed by Meier Burger (previously RRS) and CSEM PV-Center. The final surface cleaning consisted of removing a protective oxide in a diluted hydrofluoric acid (HF 5%) solution for 45–60 s.

The passivating contacts of SHJ consist of thin (~10 nm) layers of either boron- or phosphorus-doped hydrogenated amorphous silicon (a-Si:H(p) or a-Si:H(n)) which form hole, a-Si:H(p), and electron, a-Si:H(n), collectors. To provide improved passivation of the c-Si surface, a thin intrinsic a-Si:H(i) layer is typically deposited between the carrier-collecting layers and the absorber [Tanaka 1992]. In this thesis, two different reactors were used to deposit the a-Si:H layers: (1) a KAI-M PlasmaBox™ reactor (Tel Solar, formely Oerlikon) in the parallel-plate configuration powered at VHF 40.68 MHz with an inter-electrode distance of 12.5 mm and (2) an Octopus-I and Octopus-II plasma-enhanced chemical vapor passivation (PECVD) cluster tool (INDEOtec[6]) powered at 13.56 or 40.68 MHz with an inter-electrode distance of 15 mm. Silane (SiH_4), hydrogen (H_2), phosphine (PH_3) and trimethylboron ($B(CH_3)_3$) are used as gas precursors.

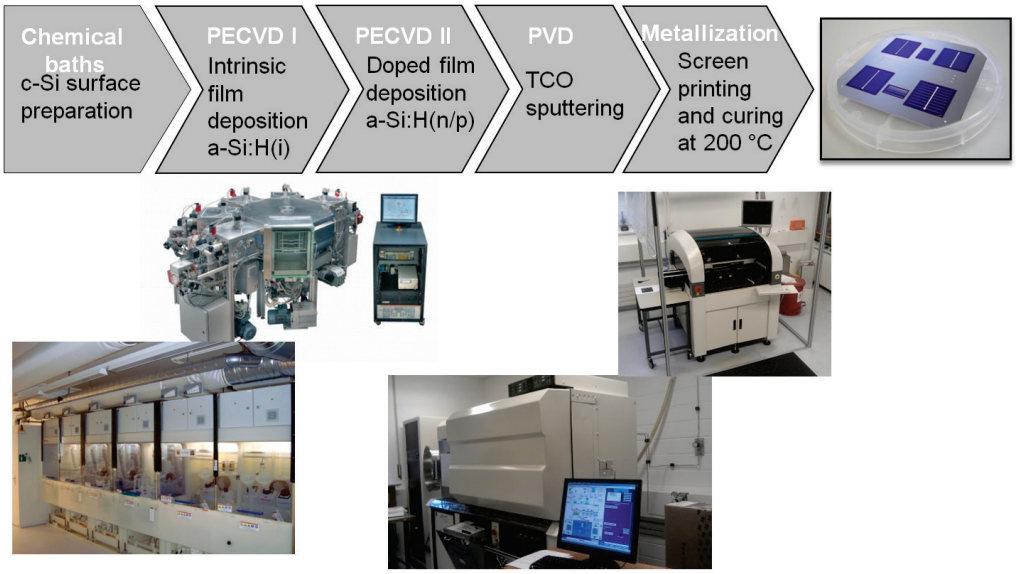


Figure 4.2: Process of a silicon heterojunction solar cell. The pictures show snapshots of our processing facilities.

Due to the poor lateral conductivity of these layers, but also for improved optical performance of the device, TCOs are usually deposited on both contact sides of the cell. For SHJ solar cells with a front and back contact, the requirements for these two layers differ slightly, depending on their location: The front TCO should ensure lateral transport to the metallic grid (especially in the case of a front-emitter design, usually in the configuration of an n-type wafer with hole collector at the front), be transparent and act as an anti-reflection coating that maximizes light in-coupling into the wafer. Conversely, for textured surfaces, the rear TCO should be optimized to minimize the absorption of the evanescent waves in the metal back-reflector, while guaranteeing a good electrical contact to the latter [Holman 2012, Holman 2013a, Holman

[6] http://www.indeotec.com/

2013b, Holman 2014]. Depending on the electronic properties of the a-Si:H and the TCO material—in particular their respective work functions—Schottky barriers are prone to form which can impede carrier transport. In our work, TCOs are deposited using a refurbished MRC 603 magnetron reactive-ion sputtering tool, operated in DC mode, with Ar as the carrier gas. An additional oxygen flow was introduced to tune the optical and electronic properties of the films. Occasionally, an Oerlikon Clusterline 200 system for physical vapor deposition was used (courtesy of CSEM PV-Center).

To form the metal contacts, silver is sputtered at the rear, while at the front the optimized grid for the cell size is screen-printed. The curing step of the metal paste was optimized to reach the highest Ag conductivity and the highest passivation quality. For this thesis, mainly 2x2 cm^2 and 6x6 cm^2 cells were fabricated. The timeline evolution on the efficiencies are shown in Figure 4.3.

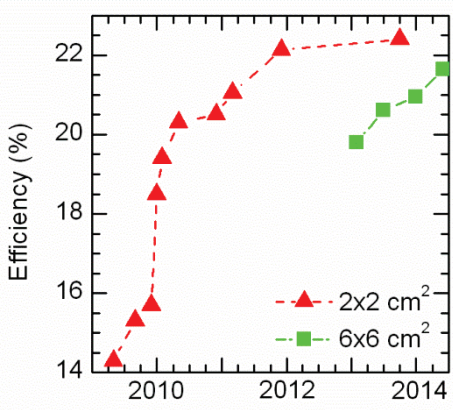


Figure 4.3: Evolution of the EPFL – PV-Lab silicon heterojunction solar cell efficiencies for 2×2 cm^2 and 6×6 cm^2.

4.3 Contact formation

In this section, we focus on the contacts in the SHJ solar cell. Two published papers compose this section. First we present results published in [Demaurex 2012] and carry on with results based on [Demaurex 2014b].

4.3.1 Damage at hydrogenated amorphous / crystalline silicon interfaces by indium tin oxide overlayer sputtering

4.3.1.1 Motivation

Damage of a-Si:H layers by sputter-induced ion bombardment has been known for decades [Street 1979] and may be of concern for high-efficiency SHJ device fabrication too. Regarding this,

Table 4:1 shows the evolution of the effective carrier lifetime (τ_{eff}) and the so-called implied-V_{oc} at one sun (iV_{oc}) during typical SHJ cell fabrication. The iV_{oc} is calculated from the excess carrier density generated under one-sun illumination in open-circuit conditions, and is indicative of the V_{oc} measured on finished devices (Chapter 2). Directly after deposition of device-relevant intrinsic/doped a-Si:H stacks, a high carrier lifetime value is obtained without the need of any post-deposition annealing. In earlier work, it was found

that high-quality passivation in the as-deposited state is a necessary condition for fabrication of high-efficiency silicon heterojunction solar cells [Descoeudres 2010, Descoeudres 2011]. Here, following indium tin oxide (ITO) sputtering, a severe drop of 76% in τ_{eff} and of nearly 30 mV in implied-V_{oc} at one sun can be observed, indicating indeed an undesired loss in wafer passivation. Subsequent curing (~190 °C for a few minutes) after screen-printing the metal grid front electrode brings the finished-device V_{oc} almost fully back up to the initial iV_{oc}. These results confirm that TCO sputtering damages the a-Si:H/c-Si interface in SHJ structures [Lu 2007, Zhang 2011] but that most of the damage is recovered by subsequent low-temperature annealing. In this section, we first discuss the origin of the sputter damage. Second, its electronic and microscopic reversibility under annealing is investigated.

Table 4:1: Passivation during SHJ cell processing. τ_{eff} was measured at an excess carrier density of 1015 cm-3. Note that τeff of a full device cannot be measured with the photo-conductance decay method because of the metallization present. Reprinted with permission from [Demaurex 2012]. © 2012 American Institute of Physics.

	τ_{eff}(ms)	(Impl.) V_{oc} (mV)
After PECVD	5.1	(730)
After sputtering	1.2	(697)
After curing	-	726

4.3.1.2 Special methods used

Float-zone 4 Ωcm phosphorus-doped mirror-polished Topsil c-Si(100) wafers were used. After deposition of intrinsic and doped a-Si:H layers as described in the previous section, ITO films were sputtered. An additional oxygen flow was introduced to tune the optical and electronic properties of the films. The passivation quality of the a-Si:H/c-Si interfaces was monitored by measuring τ_{eff} of the samples with the photo-conductance technique, either in transient or quasi-steady-state mode [Sinton 1996b]. In addition, to characterize the microstructure of thin a-Si:H films, attenuated total reflectance (ATR) Fourier transform infrared (FTIR) spectroscopy was used in transmission mode, under nitrogen atmosphere.

4.3.1.3 Origin of the sputter damage

We now turn our attention to the origin of the sputter damage, for which symmetric samples of intrinsic a-Si:H (15–20 nm) on c-Si were used, without any doped layers. This specific structure averts possible thin-film degradation due to Fermi-level-induced lowering of the Si–H bond-rupture energy during annealing [De Wolf 2009, Takashi 2008] which may otherwise obscure the phenomena under study. For our passivation samples, ITO sputtering leads to a loss in lifetime of over 90%. We observed no dependency of this damage on the experimentally tested range of sputtering parameters such as the pressure (5–16 mTorr), oxygen partial pressure (0–3.2%) or power (100–1000W). Increasing the a-Si:H layer thickness leads to a less severe electronic degradation, however. Sputtered zinc oxide (ZnO) introduces a similar degradation. By contrast, boron-doped ZnO TCO layers deposited by metal-organic chemical vapor deposi-

tion do not lead to passivation losses. Therefore, the observed degradation is likely linked to the sputtering process rather than the specific used TCO material.

Based on the loss in electronic passivation, the sputter damage must be in the form of a deep defect at the interface, most likely the Si dangling bond [De Wolf 2012b, De Wolf 2008]. The dangling bonds may be created from plasma luminescence (visible or UV) or electron or particle bombardment (neutrals and ions from the gas phase, the sputtering target and their compounds) [Plagemann 2007], as illustrated in Figure 4.4:

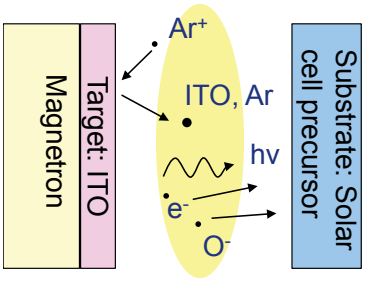


Figure 4.4: Species susceptible of damaging the passivation quality of an a-Si:H layer on a c-Si substrate.

In our experiments, the TCO deposition time strongly influences the induced damage, as shown in Figure 4.5. From this, we conclude that the deposited ITO film starts to shield the passivated wafer surface from the origin of the damage.

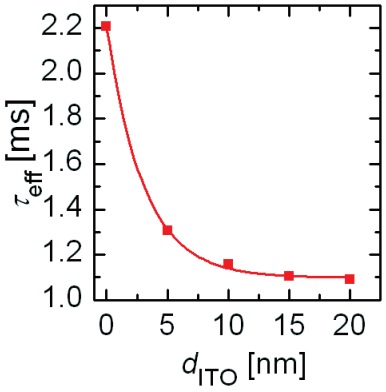


Figure 4.5: Effective carrier lifetime of an n-type wafer with 20-nm-thick intrinsic a-Si:H layers measured as a function of ITO thickness (d_{ITO}), deposited in several steps. Reprinted with permission from [Demaurex 2012]. © 2012 American Institute of Physics.

To test the role of the plasma luminescence, lifetime samples were fabricated that were shielded during TCO sputtering by standard glass (10% transparency at 4.7 eV) or quartz glass (10% transparency at 7.8 eV), or were left bare. Co-deposited lifetime samples showed a reduction in τ_{eff} during sputtering of 14% when shielded by standard glass, of 27% when shielded by quartz glass, and of 96% when left bare, as shown in Figure 4.6. During sputtering, the substrate temperature remained below 75 °C in all conditions, excluding thus *in-situ* annealing effects. Thus, the damage must be caused at least partially by plasma luminescence, agreeing with experiments focusing on sample exposure to argon plasmas, without film deposition [Illiberi 2011]. The remaining damage stems from either deeper UV (higher than 7.8 eV) irradiation,

or from particle bombardment (energies up to 150 eV) [Takagi 2006]. Historically, damage in different types of silicon structures has been reported for both mechanisms: UV light for the creation or activation of deep defects at the silicon dioxide/c-Si interface [Gruenbaum 1989, Reinwand 2010] and in amorphous hydrogenated silicon nitride [Kanicki 1991]; and electron [Schade 1981] or Ar^+ [Durny 2000, Illiberi 2011, Kessels 2002] ion bombardment for the creation of similar defects in a-Si:H. In our experiments, we observed a drop in lifetime of 92% for an unprotected sample, and of 15% with glass protection, when exposed to an Ar plasma in a PECVD system. Further investigations are needed to quantitatively assess the impact of each of these species on the passivation degradation in heterojunction solar cells.

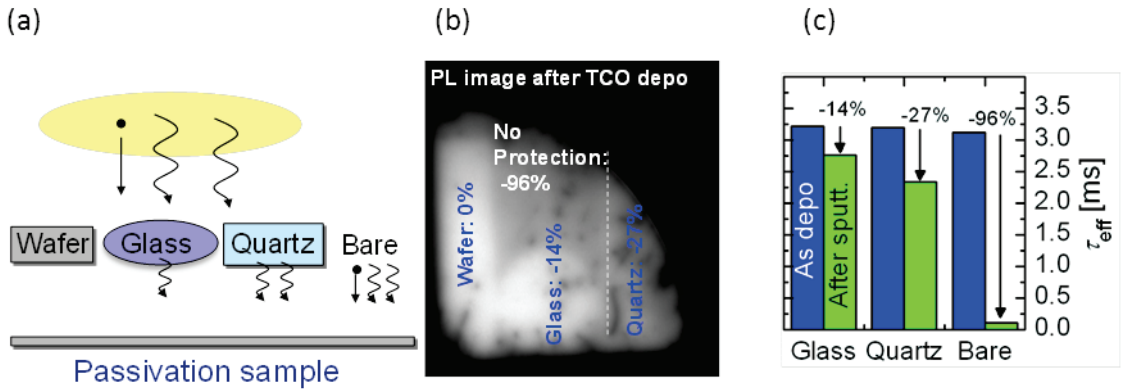


Figure 4.6: (a) Sketch of the deposition configuration for a lifetime sample protected by a wafer, glass, quartz, or left bare (b) Photoluminescence (PL) image of a typical sample after ITO sputtering with the same protective materials than in (a). The light (dark) region indicate a low (high) defect density. (c) Effective carrier lifetime at an excess carrier density of 10^{15} cm^{-3} of a wafer passivated with 15 nm of a-Si:H in the as-deposited state and after sputtering protected by glass, quartz, or left bare. The percentages indicate relative losses in lifetime. Adapted with permission from [Demaurex 2012]. © 2012 American Institute of Physics.

4.3.1.4 Reversibility of the sputter damage: electronically and microscopically

For SHJ devices, since paste curing is part of the standard process flow, the reversibility of the sputter-induced defects by annealing is of critical importance. To study the electronic reversibility, cycles of sequential ITO deposition, ITO etching and annealing were performed. The ITO was removed after sputtering but before annealing by using hydrochloric acid (HCl, 16%) or HF (5%) for two reasons. First, the difference in electronegativity between ITO and a-Si:H leads to a field effect at the interface, affecting the shape of the lifetime curve. Second, the induced Fermi-level shift at the interface may lower the (deep) defect-formation energy compared to samples without ITO overlayers, obscuring our analysis [De Wolf 2009, Takashi 2008]. With spectroscopic ellipsometry we verified that no ITO traces remained on the sample and that etching of the a-Si:H layer (less than 1 Å removed per HF dip) did not affect the film properties. Moreover, as thin films may degrade under annealing depending on their precise microstructure [Descoeudres 2010], a film that withstands prolonged annealing (monotonic improvement in passivation during the cumulated annealing time of the experiment) was selected in order to focus solely on the sputter damage behavior.

Figure 4.7 shows three ITO sputtering/ITO etching/annealing cycles. They appear to be electronically reversible, as after a few minutes of annealing (190 °C) the original carrier lifetime is recovered at a carrier

injection of 10^{15} cm^{-3}. From Figure 4.8, in the injection range > 10^{15} cm^{-3}, we observe a full recovery of the effective lifetime, indicating a full recovery of the iV_{oc}. The fact that the final V_{oc} is slightly lower than the iV_{oc} measured directly after PECVD, as shown in Table 4:1, may rather be explained by the presence of doped layers and TCO in the finished devices, as discussed previously.

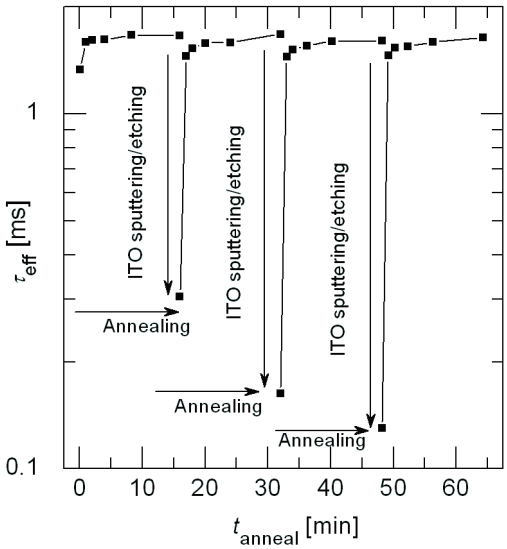


Figure 4.7: Effective carrier lifetime at a minority-carrier concentration of 10^{15} cm^{-3} of an n-type wafer with 20-nm-thick a-Si:H layers as a function of cumulated annealing time (t_{anneal}) during repeated ITO deposition/ITO etching/annealing cycles. These cycles show a reversible behavior of the passivation quality at this injection level. Reprinted with permission from [Demaurex 2012]. © 2012 American Institute of Physics.

However, the lifetime curves for the as-deposited and sputtered/annealed states do not fully superimpose at low injection, as shown in Figure 4.8. As discussed in Chapter 2, an implied voltage at the maximum power point (iV_{mpp}) can be obtained from the effective lifetime curve as function of minority-carrier density. Thus, the effective lifetime at the corresponding minority-carrier density will determine the implied fill factor (i*FF),* and consequently an upper limit for the *FF*. The TCO sputtering appears to detrimentally affect the iV_{mpp} while conserving the as-deposited iV_{oc}, pointing to a decrease of 2–3% in the i*FF.* The origin of this loss will be further discussed in section 4.3.2.2.2.

The apparent electronic reversibility at high injection raises the question of whether a corresponding microstructural reversibility of the material is present too. Indeed, carrier lifetime measurements probe several nanometers into the a-Si:H film bulk starting from the c-Si interface [De Wolf 2012b]. Therefore, most likely, the complete bulk of the films becomes damaged as well, as it sits between the plasma-exposed film surface and the (electronically probed) a-Si:H/c-Si interface. Linking microstructural and electronic phenomena may elucidate whether dangling bonds originate from the rupture of Si–H or (weak) Si–Si bonds, or both. The energy required to remove a hydrogen atom from an isolated Si–H bond in an a-Si:H network is 3.55 eV [Van de Walle 1995] and the energy required to break weak Si–Si bonds is lower (2.5 eV for a strong Si–Si bond [Wehrspohn 2000]) [Stutzmann 1986]. Thus, as many species are present during sputtering with higher energies, both bonds are susceptible to be affected.

To probe the (bulk) Si–H microstructure of the films, ATR-FTIR spectra were recorded on a c-Si prism cut from a wafer identical to our carrier lifetime samples and bifacially coated with thin intrinsic a-Si:H films, as sketched in Figure 4.9.

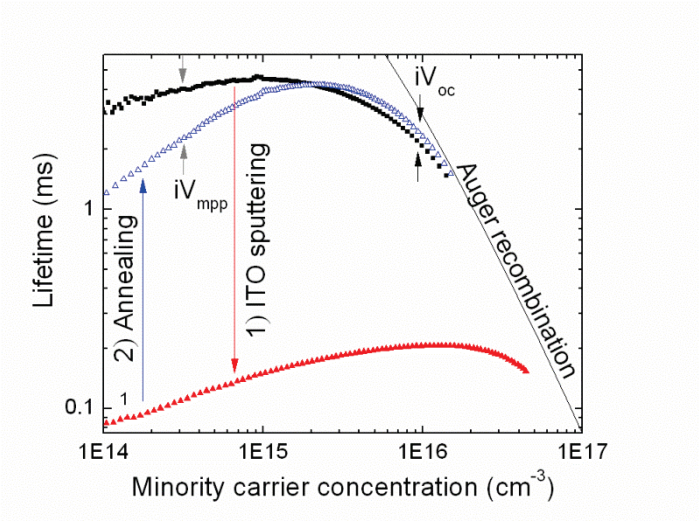


Figure 4.8: Effective carrier lifetime of an n-type wafer with 20-nm-thick a-Si:H layers as a function of the excess carriers density for a same sample at subsequent processing step: black closed squares: as-deposited state, red closed triangles: after ITO sputtering, blue open triangles: after annealing with ITO. We observe no losses in the implied-V_{oc} at one sun (iV_{oc}). However, at the implied voltage corresponding to the maximum power point (iV_{mpp}), the lifetime does not fully recover.

Typically, the hydrogen bonding environment of bulk a-Si:H is characterized by high and low stretching modes (HSM at 2070–2100 cm^{-1} and LSM at 1980–2010 cm^{-1}) [Langford 1992]. The LSM is a fingerprint for monohydrides, whereas the HSM indicates the presence of (mono- and multi-) hydrides on internal surfaces of nanosized voids in the film [Smets 2003]. Surface hydrides may exhibit additional Si–H stretching modes in the 2080–2135 cm^{-1} range [Burrows 2008].

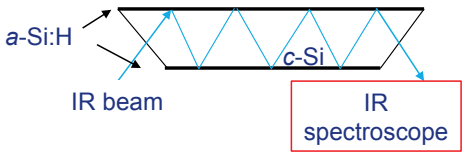


Figure 4.9: Attenuated total reflectance (ATR) Fourier transform infrared (FTIR) prism with schematic light beam path.

Figure 4.10 shows the absorbance signal of an as-deposited sample, deconvoluted into the bulk HSM and LSM responses. Figure 4.10 (b) displays the evolution of the absorbance during a series of sputtering and annealing treatments. Each spectrum represents the change in absorbance relative to the preceding spectra. Furthermore, before each measurement, the ATR prism was dipped in HF for 30 s to remove ITO (if present) or native oxide, and to ensure consistently identical surface termination. Spectrum (α) shows the absorbance change induced by an HF dip alone. The LSM absorbance is decreased by such etching. Spectrum (β) shows the absorbance difference [relative to spectrum (α)] after sputtering ITO on both faces

of a prism protected by quartz. After exposure to the plasma luminescence, the LSM absorbance slightly drops further compared to the effect of an HF etch whereas the HSM signal hardly changes. Spectrum (γ) shows that bifacial ITO sputtering with no protection induces loss similar to spectrum (β) for the LSM. By contrast, the HSM absorbance drops notably. Apparently electrons, ions, or neutrals in the plasma, or deep UV irradiation decrease the HSM absorbance. Subsequent annealing of the prism (5 minutes at 190 °C) decreases the LSM absorbance further but increases the HSM absorbance, as shown in spectrum (δ). Conversely, a pristine a-Si:H-coated ATR prism exposed to similar annealing does not yield any HSM increase. Thus, the HSM increase after annealing of the sputtered film indicates recovery of the sputter damage. Further annealing of either pristine or sputtered/etched prisms leads to a strong LSM absorbance decrease as well as a HSM absorbance decrease [spectrum (ε)]. Figure 4.10 (c) summarizes the passivation quality evolution under the same treatments as in Figure 4.10 (b).

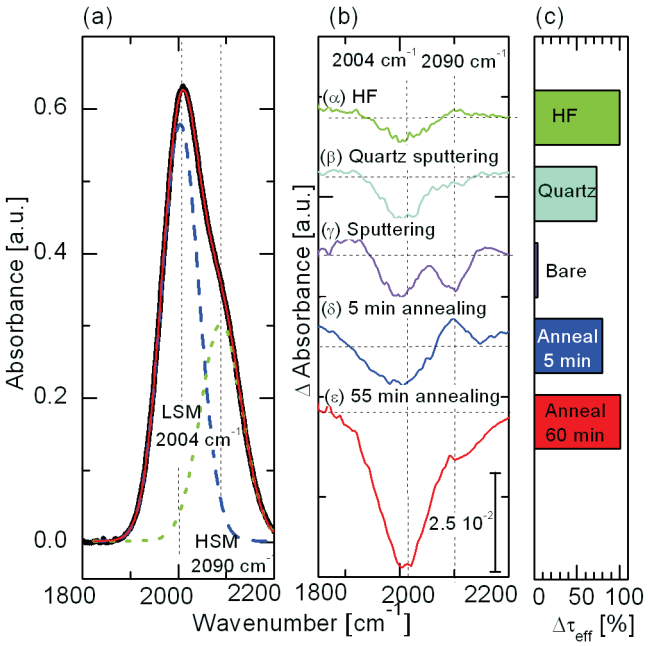


Figure 4.10: ATR spectra of 15-nm-thick intrinsic a-Si:H films on a c-Si wafer. (a) Absorbance spectrum and deconvolution of the LSM and HSM peaks at 2004 cm^{-1} and 2090 cm^{-1}. (b) Difference in absorbance spectra for each step of the experiment. The difference at each step is reported relative to the immediately preceding spectrum. Effect on absorbance of (α) a 30 s HF etch of the a-Si:H prism, (β) sputtering both sides of the prism protected by a quartz glass and a 30 s HF etch, (γ) sputtering both sides of the prism with no protection and a 30 s HF etch, (δ) annealing the prism in air for 5 min and a 30 s HF etch, and (ε) annealing the prism in air for 55 min and a 30 s HF etch. Curves are offset vertically. (c) Corresponding relative τ_{eff} changes compared to the as-deposited state. Reprinted with permission from [Demaurex 2012]. © 2012 American Institute of Physics.

Four key points ensue from our experiments: 1) Sputtering decreases the HSM intensity of an a-Si:H film, which may be (partially) recovered by short annealing. 2) Annealing of an as-deposited or sputtered a-Si:H film modifies the Si–H bonding configuration of the film (both in HSM and LSM). 3) The film does not regain its initial Si–H bonding state after sputtering and annealing. 4) The microscopic changes in the Si–H stretching modes due to sputtering and annealing do not relate unequivocally to changes in the electronic

passivation quality of the interface. Indeed, the changes in the HSM of spectra (γ) and (δ) may be related to the loss and recovery in passivation after sputtering and short annealing. However, under prolonged annealing, the HSM decreases whereas the lifetime increases further. To resolve this apparent paradox, we note that low-energy Ar^+ ions (~ 20 eV) impinging on an a-Si:H surface may break Si–H bonds close underneath the surface, rather than deep in its bulk [Kessels 2002]. Therefore, the bonding changes seen here after sputtering [spectrum (γ)] may mainly arise from the a-Si:H sub-surface region, rather than from the electronically probed a-Si:H/c-Si interface. However, this does not explain the observed electronic changes yet.

The passivation quality may depend on Si–Si bond rupture/formation as much as, or instead of, the Si–H bonding state. Changes in Si–Si bonding are often linked to electronically reversible phenomena in a-Si:H, as illustrated in Figure 4.11. Usually, a weak Si–Si bond ruptures into two dangling bonds, whereupon a nearby bonded H-atom may switch positions with one of the Si dangling bonds for stabilisation. A prime example of this reversible phenomenon is the light-induced Staebler-Wronski effect (SWE) [Staebler 1977], also observed recently at a-Si:H/c-Si interfaces [De Wolf 2011, Hekmatshoar 2011a]. Si–Si bonding is not observable with FTIR due to bond symmetry. The data in Figure 4.10 (b) show that, upon annealing, permanent changes in the Si–H vibration intensity occur. Importantly, such changes could be either due to Si–H bond rupture but also to changes in dielectric environment (such as due to bond switching) without actual deep-defect generation [Oguz 1980, Wehrspohn 2000]. However, the discrepancy between electronic reversibility and microstructural irreversibility during annealing suggests that Si–Si bond formation dictates the electronic trends at the interface in these films, rather than Si–H re-formation.

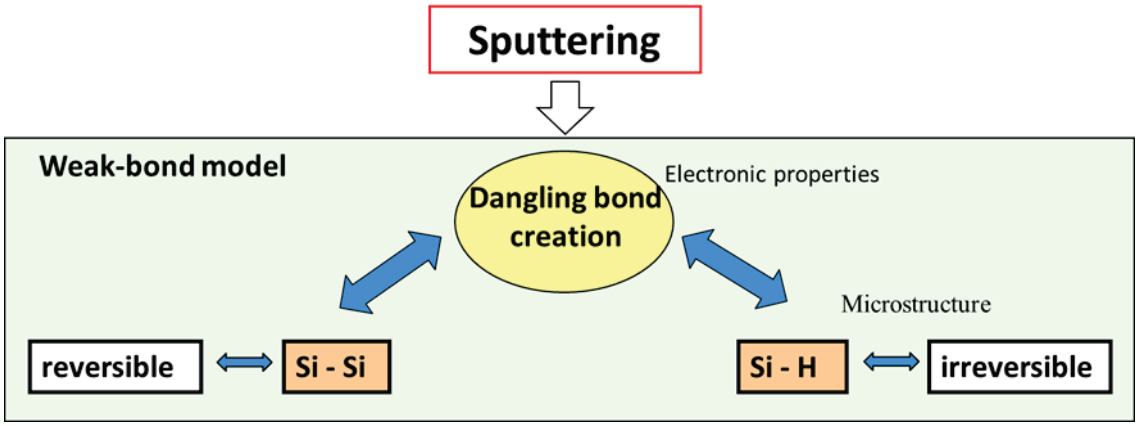


Figure 4.11: Schematic of impact of sputtering on the a-Si:H layer in the framework of the weak-bond model. Adapted from [Stutzmann 1986].

It is of particular interest that very similar findings appear to apply in the study of the reversibility of the passivation quality of amorphous / crystalline silicon interfaces under repeated cycles of low-temperature annealing and visible light soaking. Visible-light-induced defect creation in a-Si:H is often referred to as the Staebler–Wronski effect and is reported to be reversible by low-temperature annealing [Staebler 1977]. El Mhamdi *et al.* show that this is true only if no hydrogen evolution in the films can be detected under annealing [El Mhamdi 2014]. Once such evolution is no longer observed, the electronic improvement occurs much faster and is reversible [El Mhamdi 2014]. For passivating contacts, this phe-

nomenon seems to be present as well. This indicates that post-deposition annealing changes the microstructure of the film, giving new insight into the optimization of the thin a-Si:H films for SHJ and passivating contacts devices using a-Si:H / c-Si interfaces.

4.3.1.5 Reversibility of the sputter damage: the amorphous silicon thickness dependence

Thinning the a-Si:H layer, as shown in Figure 4.12, not only increases the passivation drop due to sputter damage but also prevents a complete recovery of the passivation quality. Using a different material to reduce parasitic absorption, such as microcrystalline silicon, may also prevent complete recovery from sputter damage by annealing (data not shown).

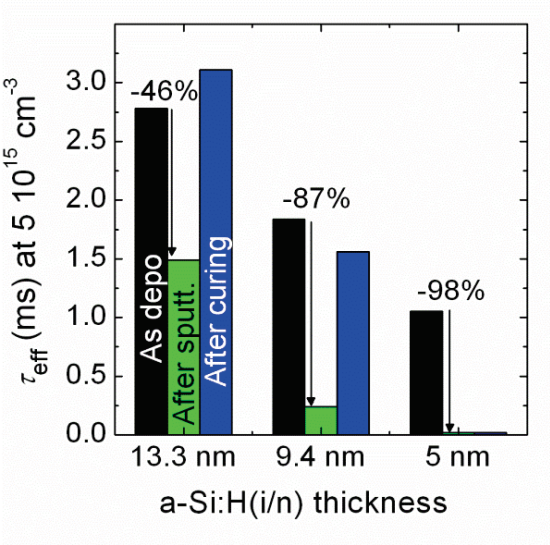


Figure 4.12: Sputter damage and recovery after curing of a-Si:H(i/n) passivating layers of different thicknesses.

4.3.1.6 Conclusion

Sputtering degrades the electronic passivation quality of the a-Si:H/c-Si interface. Dangling bonds are created at least partially by plasma luminescence. From an electronic point of view, these defects appear to be mostly reversible under low-temperature annealing. Despite this, permanent microscopic changes in the a-Si:H network, involving Si–H bonds, are observed after sputtering and subsequent annealing. The as-deposited film's microstructure cannot be fully recovered. Nevertheless, with device-grade films, we do not observe a notable loss in device V_{oc} but the *FF* might be detrimentally affected.

4.3.2 Atomic layer deposited electrodes as protection against sputter damage

In this section, thin aluminum-doped zinc oxide (ZnO:Al) layers prepared by ALD (hereafter called ALD ZnO:Al) are used as a showcase to investigate the advantages of a damage-free TCO deposition. We discuss to what extent it may be beneficial to preserve pristine a-Si:H layers during electrode fabrication and the

resulting implications on the internal voltages and thus the *FF* in SHJ solar cells. The results presented here are published in [Demaurex 2014b].

First, the effect of ALD ZnO:Al on the electronic passivation properties of the amorphous layers is studied and the minimum thickness necessary to protect these structures against subsequent sputter damage is determined. We then demonstrate sputter-damage-free devices and analyze the cell results: The benefits and losses associated with the ALD-prepared buffer layer are identified. Finally, we comment on future developments.

4.3.2.1 Experiments

The sample fabrication procedure is given in Figure 4.13. After alkaline texturing and wet-chemical cleaning of the wafers (FZ, n-type, 2–3 Ωcm, 230 µm), an industrial-sized PECVD reactor (KAI-M Plasma-Box™ reactor (Tel Solar, formely Oerlikon)), powered at 40.68 MHz, was used to deposit the intrinsic and doped a-Si:H layers. The doping and thickness of these layers were optimized at device level to yield the highest efficiency with sputtered TCO layers. Subsequent to PECVD, a water-based thermal ALD process (Oxford Instruments OpAl system) was used to deposit ZnO:Al layers of different thickness (nominal: 5, 10, 20 and 40 nm) using diethyl zinc and dimethylaluminum isopropoxide as precursors. The ZnO:Al films were deposited at 180 °C on either the front or the back side, i.e. directly on the a-Si:H(p) or a-Si:H(n) layer. ALD depositions were performed at TU Eindhoven, the Netherlands. Each ALD ZnO:Al layer was co-deposited on a c-Si wafer coated with silicon dioxide (SiO_2, thermally grown, 450 nm thick) for characterization. All samples were kept in the ALD chamber for the same total time in order to ensure identical thermal loads. A reference sample was kept inside the chamber without deposition as well. For further details about the ALD process, the reader is referred to [Wu 2013b]. To characterize the electrical properties of the ZnO:Al layers, Hall measurements were performed. Moreover, to fully characterize the thinnest layer, spectroscopic ellipsometry (SE) data of the ZnO:Al layers on SiO_2-coated c-Si were fitted using a Cody-Lorentz and an adapted Drude model, from which the carrier concentration and the optical mobility values were extracted [Ruske 2009, Wu 2013a]. As such optical measurements do not take into account the scattering of charge carriers at the grain boundaries, the obtained optical values represent an upper limit for the mobility.

For clarity, in the remainder of the present chapter, the samples with ALD ZnO:Al on the p-layer (n-layer) side are labeled as *x-ip-* (or *x-in-*) samples, where the optional prefix "*x*" indicates the ZnO:Al layer thickness. When both *ip-* and *in*-samples are considered, they are referred to as ALD samples.

Following the deposition of ZnO:Al on 4-inch wafers, the wafers were laser-scribed and cleaved into pseudo-squares (8×8 cm^2), thereby removing any shunts created by the conformal ALD. Subsequently, ITO layers were sputtered, using a magnetron reactive-ion sputtering tool with Ar as a carrier gas. Anti-reflective coating stacks at the front (with a total thickness of 65 nm, ALD ZnO:Al + ITO) and contact layers at the back (total thickness of 110 nm) were deposited on all samples. Hall measurements were performed to access the mobility and the carrier concentration of the ITO layers. Note that, unless stated differently, the thickness values reported in this paper refer to those obtained on a textured wafer, i.e. the thickness measured on a flat substrate divided by a geometrical factor of 1.7 [De Wolf 2012c]. To finalize the cells,

the back of each cell was covered with a sputtered silver layer to form the back contact and a metallic grid was screen-printed at the front using a low-temperature Ag paste that was cured at temperatures below 200 °C.

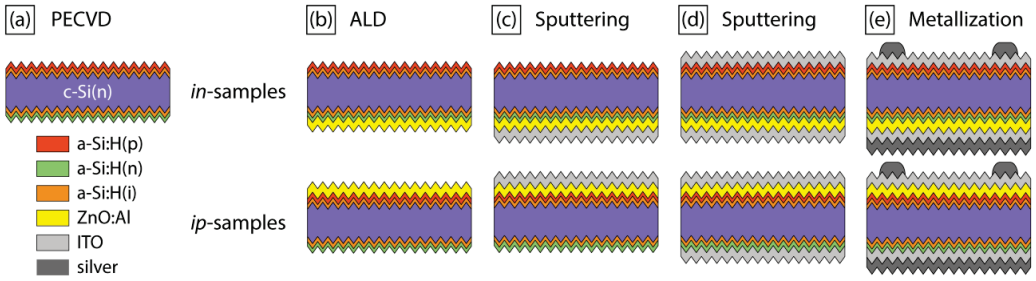


Figure 4.13: (a)–(e) Processing steps used in this work following wet-chemical cleaning and texturing. Layers are not drawn to scale. The *in*-samples have the ZnO at the majority contact (or back side); the *ip*-samples at the minority contact (or front side). Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

In order to evaluate the effect of sputter damage, photoluminescence (PL) imaging [Trupke 2006] and photoconductance measurements (Sinton Instruments, WCT-100 [Sinton 1996a]) were used throughout the entire process flow. The former technique images the radiative recombination occurring in the c-Si wafer after a uniform generation of carriers therein: areas with dominating non-radiative Shockley-Read-Hall (SRH) recombination show lower radiative signal intensity. Conversely, the latter technique converts the relative change in the wafer's photoconductivity—measured after illumination—into an injection-dependent carrier lifetime. This measurement gives access to the corresponding internal voltage V_{int} (which is basically equal to the quasi-Fermi level splitting distance), which at 1 sun corresponds to the iV_{oc}.

The finished solar cells were characterized using standard 1-sun current-voltage (*J*-*V*) measurements at 25 °C and elevated temperatures (up to ~80 °C), to determine their performance and investigate the carrier-transport behavior. The active cell area was defined using a 2×2 cm^2 mask covering the rest of the wafer. Etching the ALD ZnO:Al layer between the cells for the *ip*-samples did not lead to changes in the cell parameters. Furthermore, the cells were measured by suns-V_{oc}, to obtain the series-resistance-free pseudo *J*-*V* curves [Sinton 2000].

To investigate in greater detail the interfaces between the different layers, we used high-resolution transmission electron microscopy (HRTEM, JEM ARM200, with a beam energy of 200 kV) and energy-filtered TEM (EFTEM, Tecnai F30ST, 300 kV). The silicon and silicon oxide plasmon loss peaks were deconvoluted to image each contribution separately.

4.3.2.2 Results and discussion

4.3.2.2.1 TCO characterisitics

Table 4:2 shows the properties of the ALD ZnO:Al layers obtained from Hall measurements after annealing for 25 minutes at 190 °C. The 5-nm-thick ALD ZnO:Al layer could not be measured by this tech-

nique, likely due to the lack of coalescence of the grains. We clearly see an increase in both mobility and carrier concentration with increasing thickness of the ALD ZnO:Al films. This trend is confirmed also for the 5-nm-thick film from SE measurements (data not shown). Importantly, the increase of the carrier concentration in the ALD ZnO:Al layer is directly linked to a decrease of its work function [Klein 2009]. This thickness dependence can be tentatively explained by (1) the island-growth mode [Ohring 2001] of ZnO:Al that occurs when ZnO:Al is deposited by ALD on silicon oxide surfaces and on a-Si:H [Gu 1996], or (2) the adsorption of unintentional species at the ZnO:Al surface modifying the deposited layer properties during air exposure [Brillson 2011].

For ZnO:Al films, such initial island growth during the ALD process originates from inhibited nucleation [Baji 2012, Nilsen 2007, Thompson 2000]. For the deposition conditions used in this work, we expect that about 80 cycles (corresponding to about ~15 nm of film thickness) suffice to achieve impingement and coalescence of the grains. This is corroborated by the thickness-dependent properties of the ALD ZnO:Al film: for thin films (<20 nm), the property variations are more pronounced than for the two thicker films.

Table 4:2: Carrier concentration and mobility for the ALD ZnO:Al and standard ITO for SHJ solar cells. The ZnO:Al parameters are extracted from Hall measurements and spectroscopic ellipsometry data fitting.

	Hall Carrier concentration (cm^{-3})	**Hall Mobility ($cm^2V^{-1}s^{-1}$)**	**SE Carrier concentration (cm^{-3})**	**SE Mobility ($cm^2V^{-1}s^{-1}$)**
ZnO:Al 5 nm	—	—	$6.2\ 10^{19}$	2.9
ZnO:Al 10 nm	1.3×10^{18}	0.1	$6.7\ 10^{19}$	2.5
ZnO:Al 20 nm	6.4×10^{19}	2.8	$1.6\ 10^{20}$	16.2
ZnO:Al 40 nm	1.2×10^{20}	10.4	$2.1\ 10^{20}$	14.8
ITO front 110 nm*	3.4×10^{20}	24.7		
ITO back 210 nm*	6.7×10^{19}	27.4		

4.3.2.2.2 Injection-level dependence of underlying passivation layers

To assess the effect of the ALD process on the passivation quality of the two types of thin a-Si:H stacks (n- and p-type), we monitor τ_{eff} in the c-Si wafer as a function of the injection level. The full injection range is investigated, as the iV_{oc} of the device is determined by the lifetime at high injection (>10^{16} cm^{-3}), whereas the implied voltage at maximum power point (iV_{mpp}), and thus the implied-*FF*, are dictated by the lifetime at lower injection (<3×10^{15} cm^{-3}) [Sinton 1996a].

The deposition of a TCO on the a-Si:H(p) hole collector by reactive sputtering impacts the lifetime curve in two ways, as illustrated in Figure 4.14 (a). First, the curve shifts to lower lifetime values over the full injection range due to deep defect generation at the a-Si:H/c-Si interface induced by plasma luminescence and, likely, ion bombardment. It has been shown previously that, at high injection, this damage can be almost fully recovered by thermal annealing [Demaurex 2012] (section 4.3.1), which is also observed for the samples used in this study. Second, the minority-carrier lifetime is lower at low injection levels (<10^{15} cm^{-3}) than at higher injection levels. Such a "tailing" of the lifetime curve can be explained by a work function mismatch between the TCO, which is n-type and degenerate, and the a-Si:H(p). The Schottky contact formed between these two materials induces band bending in the thin a-Si:H(p) film and possibly also in the crystalline bulk [Bivour 2014a], from which an accumulation of minority carriers (holes) at the a-Si:H/c-

Si interface ensues. The direct consequence is an increased recombination at the TCO/a-Si:H(p) interface, within the a-Si:H(p), and at the a-Si:H/c-Si interface [Bivour 2013, Favre 2013].

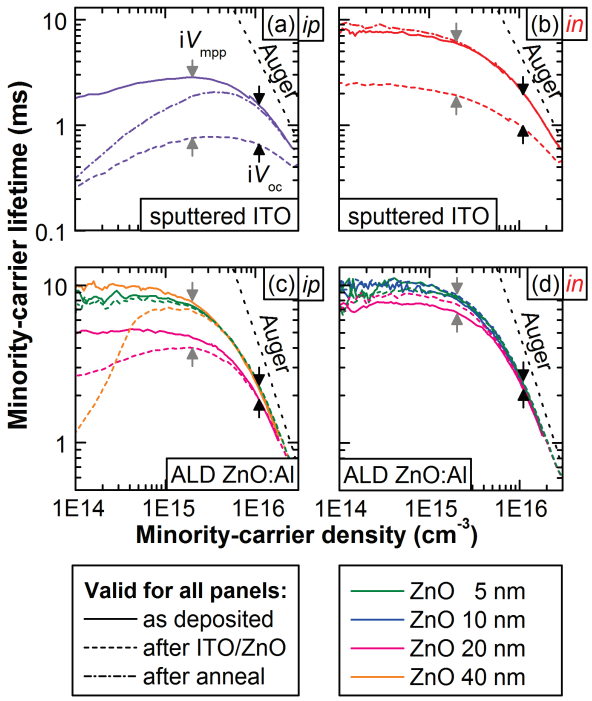


Figure 4.14: Effective lifetime vs. minority-carrier density of SHJ solar cell precursors with asymmetric stacks after PECVD, after ITO sputtering on the (a) a-Si:H(i/p) side and (b) on the a-Si:H(i/n) side, and after annealing; and after ZnO:Al ALD on the (c) a-Si:H(i/p) layer (*ip*-samples) and (d) a-Si:H(i/n) layer (*in*-samples) (no ITO overlayers). The Auger limit is plotted as an upper limit [Richter 2012]. The carrier densities at iV_{oc} (725 mV) and at the maximum power point (590 mV), labeled iV_{mpp}, are ~1.1×10^{16} cm^{-3} and ~2×10^{15} cm^{-3}, respectively, indicated by the black and grey arrows. Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

The influence of the work function is illustrated in Figure 4.15. A direct consequence of such increased recombination at low injection is a loss in internal voltage at maximum power point, and thus a loss in *FF* [Reusch 2013]. The associated *FF* losses will be discussed in section 4.4.1.2. Figure 4.14 (c) and (d) illustrate the advantage of using a soft deposition technique such as ALD: no global reduction in τ_{eff} is observed. However, we note that the decrease in carrier lifetime at low injection is present as well for the a-Si:H(i/p)/c-Si interface (Figure 4.14 (c)). This confirms that this low-injection-lifetime loss does not depend on the deposition technique but accounts for changes in the recombination statistics induced by the mere presence of the TCO [Bivour 2013]. Notably, we observe a dependence of the slope of the lifetime curves at low injection on the ALD ZnO:Al thickness. This could be explained by the thickness dependence of the ALD ZnO:Al carrier concentration (Table 4:2), which affects the work function [Klein 2009]. Changes in the inversion layer [Kleider 2008b] in the c-Si(n) close to the a-Si(i/p)/c-Si interface that cause edge effects [Kessler 2012, Veith 2014] are unlikely as photoluminescence imaging at low intensity does not support this explanation and photoconductance measurements were performed more than 3 cm away from the edges.

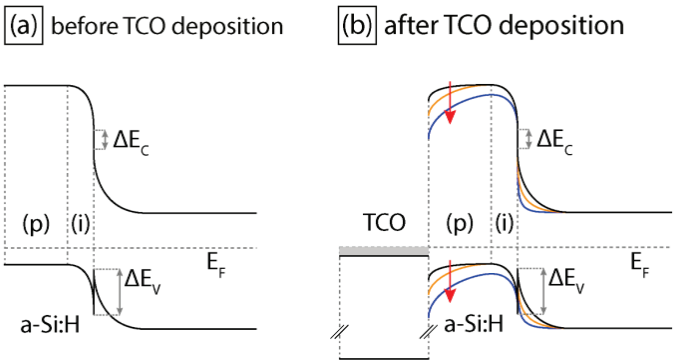


Figure 4.15: Schematic band diagram illustrating the effect of the TCO work function on the band alignment at the a-Si:H(i/p)-side. The arrows indicate the increasing work function mismatch (towards a smaller work function). Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

Sputtering on the a-Si:H(n) electron collector leads to a decrease in global lifetime as well (for all injection levels), although this effect is less pronounced compared to the p-side when similar sputtering conditions (plasma properties and deposition time) are used (Figure 4.14 (b)). This discrepancy could be related to differences in a-Si:H layer thickness (for optical reasons, the a-Si:H(p) layer is thinner than the a-Si:H(n) layer) or differences between a-Si:H(p) and a-Si:H(n) layers in proneness to defect creation. The details of defect creation strongly depend on the position of the Fermi level in the material and are discussed elsewhere [De Wolf 2009, Powell 1996]. The asymmetry in capture cross section for electrons and holes of dangling bonds at the c-Si surface could play a role in this phenomenon as well [Descoeudres 2013]. Importantly, longer deposition times, as used for the back TCO, elevate the sample temperature, leading to a complete *in-situ* annealing of the sputter damage. However, in contrast to the p-type case discussed before, for n-type stacks the carrier lifetime at low injection remains unaffected by the TCO's presence (Figure 4.14 (b) and (d)). Following similar arguments as before, this may be explained in two ways: (1) There is no work function mismatch between the TCO electrode and the a-Si:H(n) film. However, according to the literature [Klein 2009], the ITO and ZnO:Al work functions are expected to be at mid-gap of the amorphous silicon, thus probably also lead to a work function mismatch at the a-Si:H(n)/TCO interface; (2) The work function mismatch does not strongly affect the recombination statistics. This could be explained by the thicker a-Si:H(n) layer and its higher doping—we measure a difference in dark conductivity of two orders of magnitude [Martín de Nicolás 2011, Tucci 2012]—compared to the a-Si:H(p) layer, mitigating the effect of the work function on the bands [Bivour 2013].

4.3.2.2.3 Impact of sputtering on implied-V_{oc}

During capping of the ALD ZnO:Al films by sputtered ITO overlayers, the passivation quality was tracked using PL images. The results for the *ip*-samples are shown in Figure 4.16 (a)–(d) for ALD ZnO:Al thicknesses from 5 to 40 nm. The PL images were taken at an equivalent illumination level of 1.4 suns. We patterned the TCO into three 2×2 cm^2 solar cells and three extra pads for additional characterization using a shadow mask during sputtering of the front ITO (Figure 4.16 (e)). As the shadow mask fully protects the

wafer surface outside the active cell areas, these regions were not affected by sputter damage and show the highest PL signal after ITO deposition. For the regions exposed to sputtering, a clear reduction of the sputter damage is observed when increasing the ALD ZnO:Al layer thickness. To quantify this impact, the iV_{oc} of each precursor was extracted by photonductance lifetime measurements before and after sputter deposition of the ITO (Figure 4.16 (f)). The reference sample with no ALD ZnO:Al layer shows a drop of over 30 mV in iV_{oc}. With increasing ALD ZnO:Al layer thickness, the iV_{oc} drop becomes less severe until no loss is observed anymore. This clearly indicates that at least 20 nm of ALD ZnO:Al are needed to protect the a-Si:H/c-Si interface from sputter damage. This result is in agreement with the postulation of a self-screening effect of TCO films against sputter damage [Demaurex 2012].

Sputter deposition of the ITO back contact does not further decrease the iV_{oc}, independent of the presence of an ALD ZnO:Al screening layer (data not shown). This is explained partially by the longer sputter time needed for the back which heats the sample and hence reduces the sputter damage by *in-situ* annealing, but also, likely, by the higher defect-creation resilience of n-type films, compared to their p-type counterparts, as pointed out in section 4.3.2.2.2.

4.3.2.2.4 Cell results and analysis

In the following section, we present solar cell results ensuing from the previously discussed samples (Figure 4.17 (a)–(d)). First, compared to the reference, the V_{oc} values of the *ip*-samples are not significantly higher, even though an enhanced iV_{oc} was measured for these samples after sputtering (Figure 4.17 (f)). This can be explained by the recovery of the sputter damage due to thermal annealing during the curing step after screen-printing. Moreover, at high injection levels the lifetime is Auger-recombination-limited and SRH plays only a minor role. As for the *in*-samples, we observe systematically lower V_{oc}s.

Second, though the TCO stacks may have varying parasitic absorption, the resulting differences in photogenerated carrier density are low and the short-circuit current density (J_{sc}) values similar. Consequently, even though, close to 1 sun, the V_{oc} varies by 0.7 mV(mAcm^{-2})$^{-1}$ with J, the J_{sc} differences hardly affect the measured V_{oc} values. This coefficient was obtained by illumination-dependent measurements.

Third and most strikingly, the *FF* for most of the ALD samples is significantly lower compared to the fully sputtered reference cell. Indeed, for both *in*- and *ip*-samples with thin ALD-prepared layers, the *FF* is as low as 71.9% and increases with increasing ZnO:Al layer thickness.

In order to understand this behavior, we now consider the *FF* loss and its possible causes: series resistance (R_s), shunt resistance (R_{sh}) and non-ideal diode behavior linked to the recombination current $J_{0,\neq 1}$ [Khanna 2013]. These losses are depicted schematically in Figure 4.18. Assuming a V_{oc} of 730 mV and an ideality factor of 2/3 [Reusch 2013], and considering only losses due to recombination within the absorber and at its interfaces with a-Si:H, the achievable ideal *FF* would be 89.7% (FF_0) [Green 1983a]. From suns-V_{oc} measurements, we obtain the series-resistance-free *FF,* referred to as the pseudo-*FF* (p*FF*). The results are shown in Figure 4.17 (e). For thin ALD-prepared layers, the p*FF* values surpass the reference value of 83.1% by almost 2% absolute. This is owed to higher implied voltages (up to 17 mV compared to the reference) at the pseudo maximum power point (pV_{mpp}), while the measured pseudo-V_{oc} (at 1 sun) remains virtually un-

changed (Figure 4.19 (c) and (d)). This indicates that the ALD samples have the potential to reach higher *FF* than the reference, provided that no R_s losses occur.

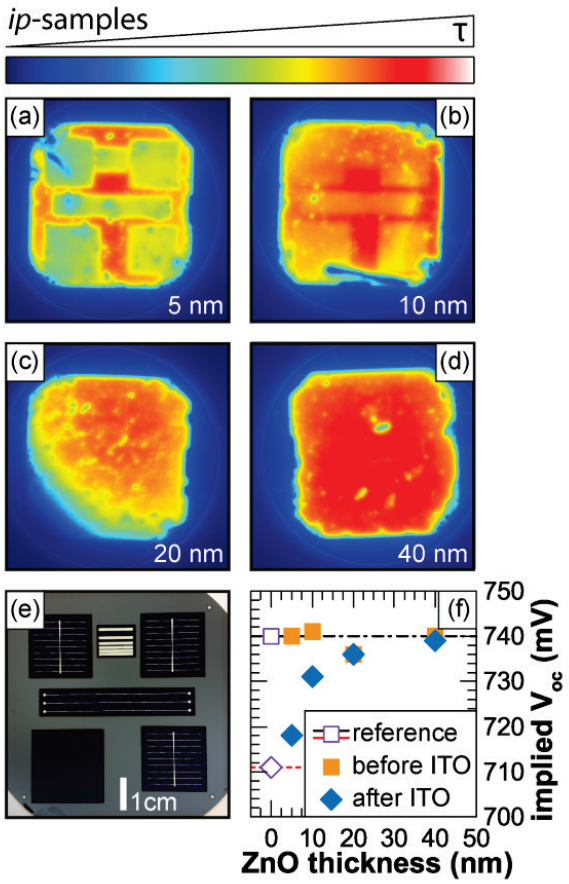


Figure 4.16: PL images after sputter deposition of ITO at the front for (a) 5, (b) 10, (c) 20 and (d) 40 nm of ALD ZnO:Al deposited on the p-side. (e) Photo of the wafer layout with three metallized cells, an ITO pad for spectral response measurement, and two structures for TCO transfer length and metal line resistance measurements. (f) iVoc before and after ITO deposition for the samples shown above, indicating the loss linked to sputter damage. The dashed and dashed-dotted lines indicate the value of the reference (violet data points). Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

The difference in the p*FF* values stems from the R_{sh} and J_0 components. The R_{sh} extracted from dark *J-V* measurements is high (10^4–10^5 Ωcm^2) for all of our cells, and thus hardly impacts the *FF*. The J_0 component must then be responsible for this gain. This parameter includes the recombination current and is a function of the minority-carrier lifetime at a carrier concentration corresponding to the maximum power point. However, for both *ip*- and *in*-samples, the *FF* gain associated with J_0 decreases with increasing ZnO:Al thickness. Hence, the increased p*FF* cannot be explained by protection of the a-Si:H layers by the ALD-prepared layer, as this protection is most efficient for films thicker than 20 nm and not for the thinnest film.

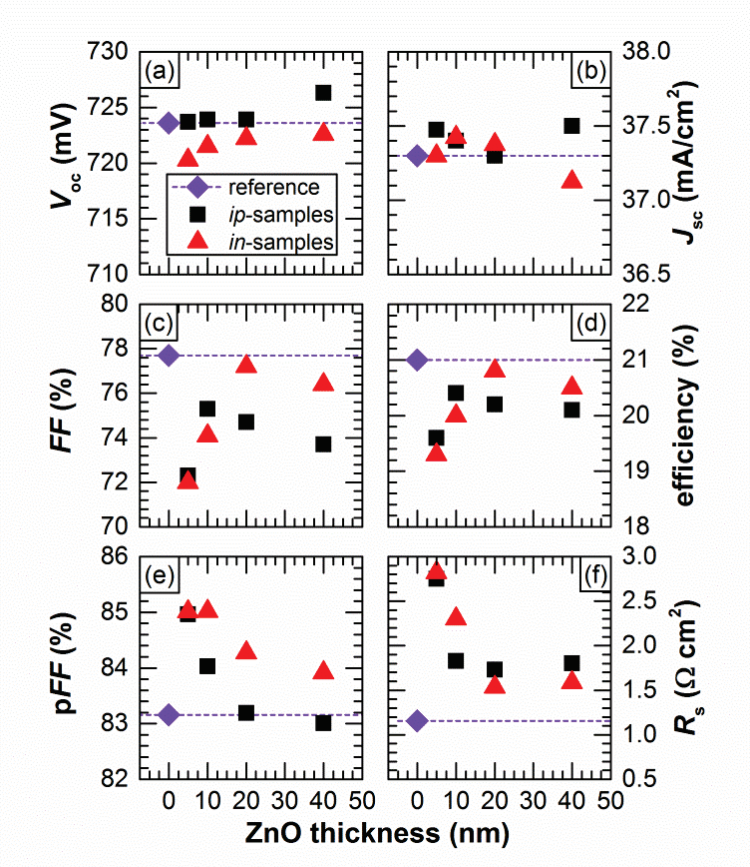


Figure 4.17: (a)–(d) Voc, Jsc, FF and cell efficiency obtained for ip- and in-samples from 1-sun J-V measurements. (e) pFF from suns-Voc and (f) Rs determined from comparing J-V and suns-Voc data for each cell. For each wafer the results of the best cell are shown. Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

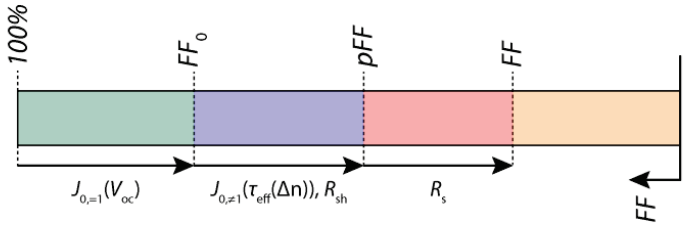


Figure 4.18: Schematic representation of the FF losses attributed to J0,=1, J0,≠1, Rsh and Rs. Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

Suns-V_{oc} measurements at high illumination, shown in Figure 4.19, characterize qualitatively the Schottky barriers formed at the doped a-Si:H/TCO interface [Bivour 2012, Bivour 2014a, Glunz 2007a, Sinton 2000]. From Figure 4.19 (a), we observe for the *ip*-samples an increasing deviation from the Auger limit when decreasing the ALD ZnO:Al layer thickness, indicating the presence of a Schottky diode. The ideality factor at 100 suns (n_{100}) is used to characterize this deviation [Bivour 2014a]. It can be calculated by fitting the suns-V_{oc} slope in the vicinity of the illumination intensity of interest using the single-diode equa-

tion. Then, if the fit is performed in a logarithmic ($\log_{10}$) scale, we have $slope * \ln(10) = {}^{q}/_{nkT}$. Looking at the n_{100} data, we observe opposite trends for *in*- and *ip*-samples. This is expected as TCO work function changes should impact antithetically the a-Si:H(i/n)/TCO contact and a-Si:H(i/p)/TCO contact. Further investigations are needed to understand suns-V_{oc} measurements at high illumination which show an n_{100} larger than the Auger limit (n = 2/3). The trend observed with n_{100} could explain the R_s trend measured in the cells, assuming that all deviations from the n_{100} = 2/3 curve affect the *FF* negatively (including the curves with n_{100} > 2/3). However, we do not have a clear correlation for the relation between n_{100} and the R_s and cannot draw conclusions at this point. The case of n_{100} > 2/3 is worth investigating further but is beyond the scope of the present study.

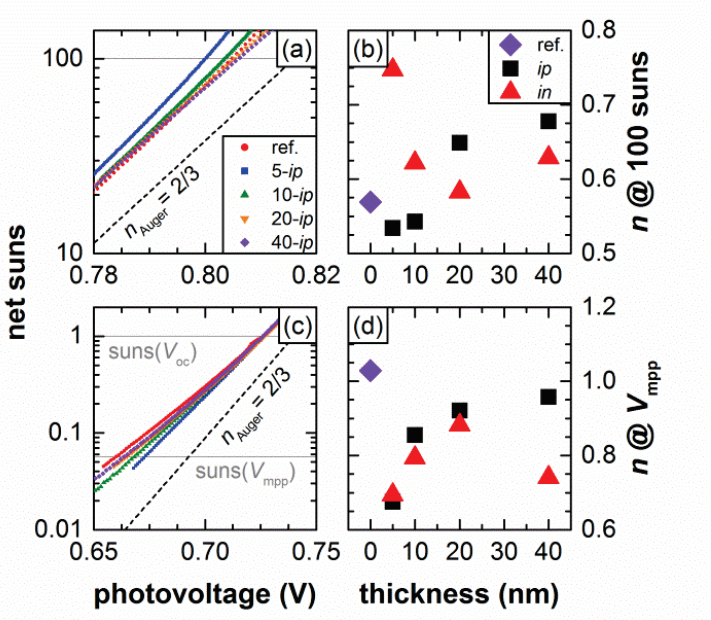


Figure 4.19: (a) High and (c) low suns-V_{oc} data with extracted ideality factor n at (b) 100 suns and (d) the maximum power point.

We continue our analysis by studying the differences between the p*FF* and the *FF*, which arise from the contribution of the R_s. From a comparison of suns-V_{oc} and 1-sun *J*-*V* measurements, an R_s value can be computed, the results of which are shown in Figure 4.17 (f) [Pysch 2007]. The cells with 5 nm of ALD ZnO:Al show the highest R_s value of 2.8 Ωcm^2, which corresponds to a *FF* loss of nearly 13% absolute with respect to p*FF* [Khanna 2013]. Devices with ALD ZnO:Al layers thicker than 5 nm show a lower R_s, which nevertheless remains above the reference value of 1.2 Ωcm^2. We therefore conclude that the *FF*s of the ALD samples are clearly limited by their R_s.

We now focus on finding the origin of the increased R_s for ALD samples, based on the analysis of its two components: (1) ohmic losses (including the contribution of each material); and (2) non-ohmic losses related to barriers to carrier transport. Investigating ohmic losses first, the main difference between the cells arises from the ZnO:Al/ITO stack characteristics, as all the other layers (PECVD and sputtered) were co-deposited for, and can be considered to be identical for the samples under study. Concerning the lateral carrier transport to the metal grid within the *ip*-samples, the thickness dependence of ZnO:Al's electrical

properties is to a large degree compensated by the presence of the sputtered ITO overlayer, which ensures lateral transport. This is based on Hall measurements of the ZnO:Al/ITO stacks. Assuming that the front ITO transports the entire generated current, its sheet resistance (90 ± 20 Ω/sq for a range between 25 and 60 nm) leads to a *FF* change of less than ±0.35% absolute due to lateral transport losses. Nevertheless, as the 5- and 10-nm-thick ALD-prepared layers exhibit much lower carrier concentrations compared to the ITO layers, an increased R_s is expected from impeded transverse transport of the carriers in the ALD-prepared layers even though it cannot be easily quantified.

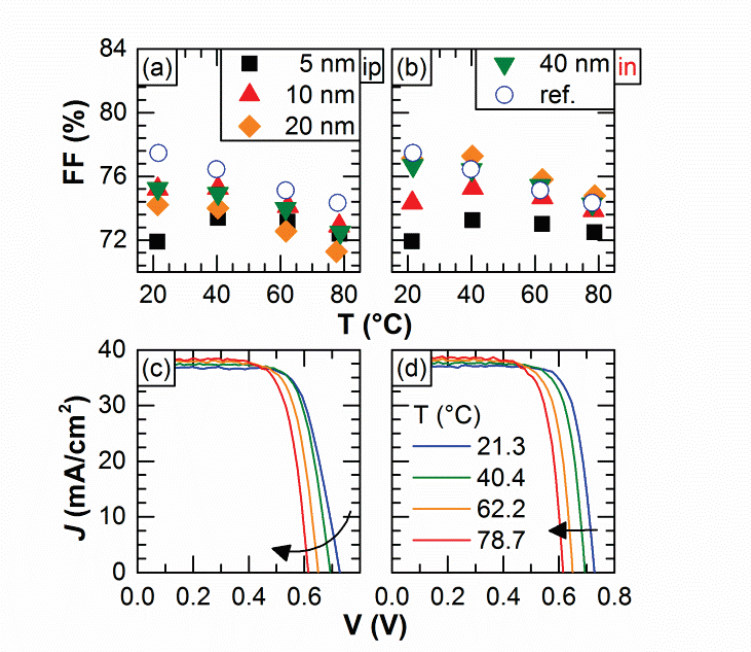


Figure 4.20: *FF* vs. temperature for the (a) *ip*- and (b) *in*-samples (with ZnO:Al layers 5–40 nm thick). *J-V* curves for (c) the 5-*ip*-sample and (d) the reference cell for different temperatures. The arrows indicate their behavior with increasing temperature. Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

We now turn to non-ohmic losses. To further investigate the losses in the ALD samples, the *J-V* characteristics were measured at temperatures between 20 and 80 °C, and are shown in Figure 4.20. Such measurements can be instructive for the detection of charge-collection barriers in finished devices [Seif 2014]: transport dominated by thermionic emission will be enhanced with increasing temperature whereas tunneling is temperature independent. These effects add to the common decrease in V_{oc} with increasing temperature [Löper 2012]. For the 5-*ip*-, 5-*in*- and 10-*in*-samples, we observe a positive temperature coefficient for the *FF* up to ~40 °C (Figure 4.20 (a) and (b)). For higher temperatures, the behavior of the samples is similar to that of the reference cell and the *FF* starts to decrease. To illustrate this effect we show the *J-V* curves measured at different temperatures for the 5-*ip*-sample (Figure 4.20 (c)) and the reference cell (Figure 4.20 (d)). In the following sentences, |Δ| refers to the absolute difference of both the V_{oc} and the V_{mpp}'s temperature coefficient. The error has been estimated from both measurement of the voltages ±2 mV and the temperature error ±1 °C. For the former, the V_{mpp} decreases at a slower rate (−1.25 mV/°C) than the V_{oc} (−1.97 mV/°C; |Δ| = (0.72±0.1) mV/°C) leading to an increase in *FF*. This contrasts with the reference cell, for which the rates for both the V_{mpp} and V_{oc} are more comparable (−2.0 mV/°C and −1.64

mV/°C; |Δ| = (0.36±0.1) mV/°C), and a linear decrease in *FF* is observed. There are two possible causes for this behavior, namely a work function mismatch between the TCO and doped films [Bivour 2014a], or the presence of an unintentional layer acting as a transport barrier [Seif 2014].

One might expect that a work function mismatch would affect the contact formed by a-Si:H(n) or a-Si:H(p) differently, as the *in*-samples and *ip*-samples were co-deposited for the ALD ZnO:Al layer. This is, however, not the case. Therefore, we investigated the samples for a possible transport barrier. For this, we employed HRTEM and EFTEM for the 5-*ip*-sample and the reference, and specifically searched for a possible silicon oxide (SiO_x) interlayer, as this material is likely to form and might act as a transport barrier. From the EFTEM micrographs of both samples (Figure 4.21 (a) and (b)), which were taken by selecting the SiO_x plasmon loss signal only, we clearly observe a SiO_x-rich layer in the ALD sample. Importantly, this contrast is absent in the micrograph of the reference cell. The presence of a SiO_x layer is corroborated by energy-dispersive X-ray spectroscopy (Figure 4.21 (c) and (d)), from which we find the onset of the oxygen signal to be located within the a-Si:H layer for the 5-*ip*-sample but not for the reference sample. Judging from the 5-*ip*-sample, we infer that this thin SiO_x barrier is also present in the other ALD samples and hinders carrier transport.

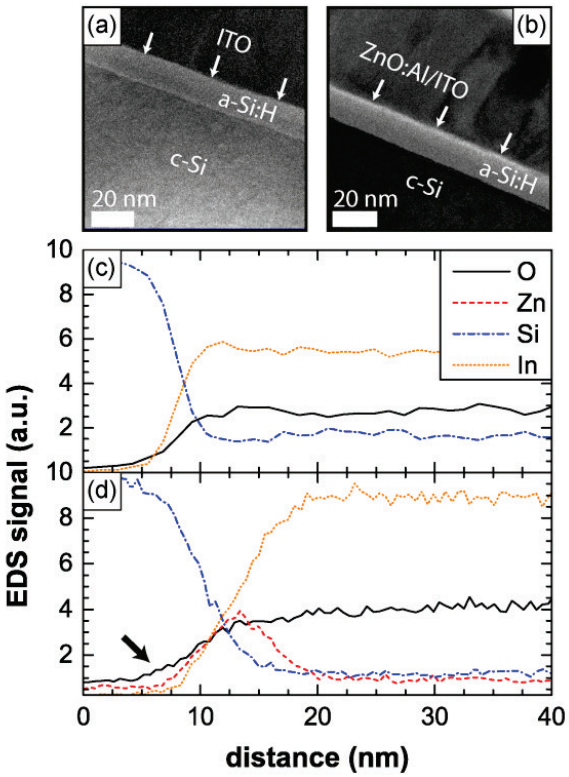


Figure 4.21: EFTEM of (a) the reference and (b) the 5-*ip*-sample showing the SiO_x plasmon loss signal, where white refers to an increased presence of SiO_x. Arrows indicate the a-Si:H/TCO interface at which a SiO_x layer is observed for the 5-*ip*-sample but not for the reference. (c) and (d) Energy-dispersive X-ray spectroscopy signals for oxygen (O), zinc (Zn), silicon (Si) and indium (In) for the sample in (a) and the sample in (b) respectively. In (d) the arrow indicates the early oxygen onset. Reprinted, with permission, from [Demaurex 2014b] © 2014 IEEE.

As observed in Figure 4.17 (f), the R_s value of the ALD samples saturates at around 1.6 Ωcm^2, which is approximately 0.4 Ωcm^2 higher than the reference value. For a full ALD ZnO:Al back electrode, we obtain a value of 1.5 Ωcm^2, which is in line with this saturation limit. For thin ALD samples, we measure much higher R_s values which are likely linked to the ZnO:Al properties as discussed above. We thus conclude that the SiO_x barrier accounts for an increase in the R_s value of 0.4 Ωcm^2 for ALD-prepared films, which, given previous experience with metal–insulator–semiconductor (MIS) contacts, is unexpected [Green 1974]. The origin of this SiO_x layer is still unclear, however. A possible explanation is the formation of a native oxide, either during the transport of the samples, or while loading the samples on a pre-heated plate, prior to ALD. This would imply that the native oxide of the reference sample—which also underwent the transport and loading into the ALD system, to ensure the same thermal load—was removed during sputtering, likely by ion bombardment. Another possible explanation involves the ALD growth process itself. Indeed, for ALD-prepared aluminum oxide layers, a thin SiO_2 layer was reported to form during the first cycles of the deposition [Dingemans 2012, Roy Chowdhuri 2002]. Further investigations are needed to clarify the origin of the SiO_x transport barrier for the ALD ZnO:Al samples.

4.3.2.2.5 Summary

In this section, we first confirmed that the carrier lifetime decrease at *low injection,* often observed following TCO deposition, is linked solely to the deposited material and is process independent. We then showed that a 20-nm-thick ALD-prepared layer effectively protects the underlying a-Si:H layers and the a-Si:H/c-Si interface against sputter damage, as evidenced by lifetime measurements.

Furthermore, on one hand, for the ALD samples, higher p*FF* values were obtained due to lower recombination losses at low injection. However, these improvements appear not to be linked to the protection against sputter damage, as the thinnest ALD-prepared layers—offering the least protection—yield the lowest recombination losses. On the other hand, an increased R_s was observed for all ALD samples. This leads to important *FF* losses which outweigh the potential gain linked to higher p*FF* values. The increased R_s is partly explained by the presence of a transport barrier for electrons and holes. EFTEM images revealed that this barrier is formed by a thin SiO_x layer at the a-Si:H/ZnO:Al interface. Therefore, further investigations are needed to find ways to avoid this increased R_s and maintain the benefits of lower recombination losses at low injection.

4.3.3 Summary and outlook

In this section, we discussed three consequences of contact formation for a front-emitter SHJ solar cell:

(1) During TCO sputtering, the a-Si:H/c-Si interface is damaged and dangling bonds are formed. For 20-nm-thick amorphous layers, this damage can be fully recovered by annealing. Thin a-Si:H layers do not fully recover from sputter damage.

(2) A soft deposition technique, such as ALD, does not damage a-Si:H layers. For thin amorphous layers, buffer layers applied by ALD or other soft deposition techniques could become useful if not crucial to achieve high internal voltages.

(3) The TCO work function mismatch with the a-Si:H(p) can reduce the i*FF* by 2 to 3%. New investigations are needed to find ways of reducing this loss and bring the carrier lifetime as close as possible to the Auger limit throughout the full carrier injection range (10^{14}–10^{16} cm^{-3}).

This brings new considerations for optimized SHJ cell architectures. As the a-Si:H(i/p)/c-Si interface is most affected by the TCO work function and as thicker layers would prevent the i*FF* losses induced by the work function mismatch [Bivour 2013], using a rear-emitter architecture would enable thicker a-Si:H(i) and a-Si:H(p) films without suffering from increased parasitic absorption in the blue. Moreover, the a-Si:H(i/n) at the front could be thinned if capped with an ALD TCO to prevent the unrecoverable sputter damage losses occurring in thin layers. This could be an interesting device architecture to reach high efficiencies.

4.4 Contact characterization

As already pointed out in Chapter 2, contacts in solar cells are critical. In the c-Si/a-Si:H/TCO/metal stacks, the TCO work function plays a crucial role [Arch 1991, Bivour 2013, Demaurex 2014b]. This complex layer stack can be split in two, the c-Si/a-Si:H/TCO and TCO/metal contact, by using TCO bilayers [Barraud 2013, Bivour 2014b]. These stacks can then be optimized separately.

The first two sections of the contact characterization will be devoted to characterizing the TCO work function by using, in a first approach, MIS-like structures and, in a second approach, lifetime samples. The contact resistivity of the c-Si/a-Si:H/TCO contact is then discussed by using transfer-length measurements. As the TCO/metal contact is usually not the limiting contact in SHJ and is easily characterized, the last section only briefly discusses this contact interface.

4.4.1 c-Si/a-Si:H/TCO contact: TCO work function

The TCO work function can be measured using capacitance-voltage-based measurements [Ginley 2010]. Such measurements were performed at CEA-INES[7] on different ITO layers prepared in our laboratory by varying the oxygen flow during sputtering. The ITO effective work function is plotted as a function of carrier density and resistivity in Figure 4.22. We observe that the work function can be tuned between 4.5 and 5 eV, in agreement with values from the literature [Klein 2009]. In this figure we see a clear direct dependence of the work function on the carrier density.

Despite this direct dependence, the TCO work function of a bulk material will not necessarily be similar to the local one at the interface with another material. This is due to the interaction between the two materials and the creation of interface states that may pin the Fermi level, as explained in Chapter 2. Simulations using AFORS-HET ([Froitzheim 2003]) do indeed suggest that such pinning occurs in SHJs: to match device results, the TCO work function must be lowered compared to values from the literature. Therefore

[7] http://www.ines-solaire.org/anglais/INDEX/index/Home.html

it is important to have a characterization technique that directly quantifies this local interfacial work function value, rather than its bulk equivalent. Two techniques were investigated for this purpose and will be discussed in the next sections.

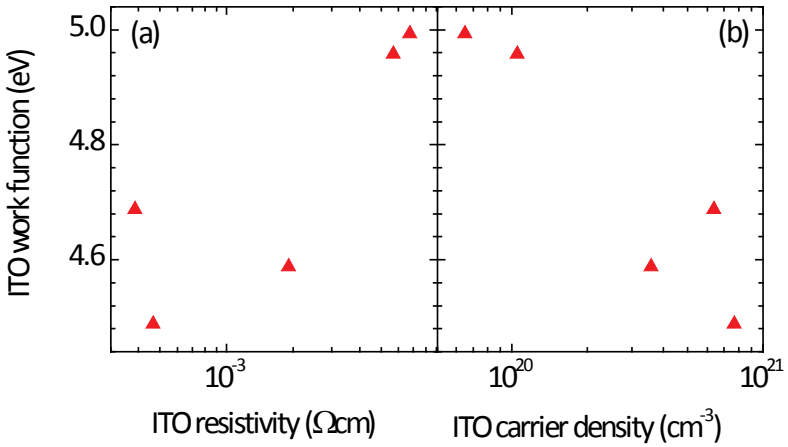


Figure 4.22: ITO work function dependence on (a) the resistivity and (b) the carrier density.

4.4.1.1 TCO work function by MIS-like structures

To gain information about the interfacial work function, we prepared MIS-like structures with a direct TCO/a-Si:H(i) contact, i.e. without the presence of a boron-doped layer as shown in Figure 4.23 and with a SHJ electron collector. In these structures, as the a-Si:H(p) layer usually forming the selectivity of the hole contact is omitted, the TCO work function is expected to dictate the junction properties. Depending on the work function mismatch between the a-Si:H(i) and TCO layer, an inversion or accumulation layer may form at the c-Si surface (see Chapter 2). The internal and external voltage of this device should then be altered. Monitoring the V_{oc} of devices described in Figure 4.23 and changing the TCO work function should evidence whether the TCO is pinned at this interface or not. Moreover, if the work function is not pinned, this experiment would give insight on the variation of TCO work functions.

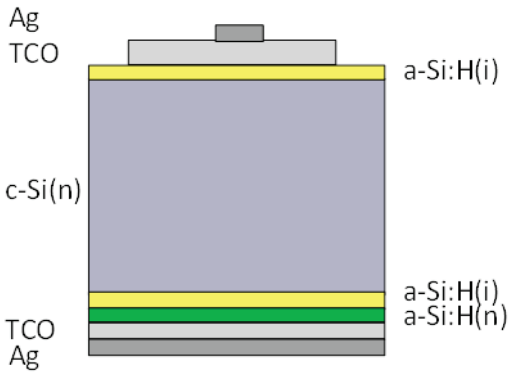


Figure 4.23: (a) Sketch of the devices prepared to study the interfacial TCO work function.

Figure 4.24 shows the V_{oc} as function of the carrier density of the ITO, which we tune by varying the oxygen flux in the sputtering tool. First, we observe that the a-S:H(i)/TCO contact acts as an emitter, collecting holes. We then observe a systematically decreasing V_{oc} when increasing the ITO carrier density. This indicates that the Fermi level is not completely pinned at the a-Si:H/TCO interface. Recently, using a similar approach, Ritzau *et al*. determined a pinning factor of 0.2–0.3 of the a-Si:H(i) layer with several materials [Ritzau 2014]. We note that, in a metal–semiconductor contact, a pinning factor, corresponding to the discrepancy between the bulk material (prior to contact) and interface work function, can be defined as:

$$WF_{interface} = S \cdot (WF_{bulk\ material} - \Phi_{CNL}) + \Phi_{CNL}\ ,$$

where Φ_{CNL} is the charge neutral level, described in [Bardeen 1947]. However, this pinning factor may differ for doped a-Si:H contacts [Kanicki 1988].

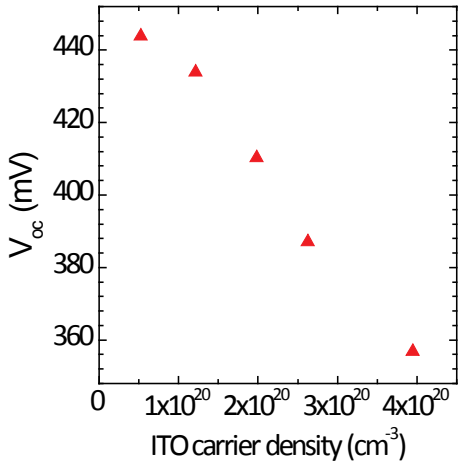


Figure 4.24: V_{oc} of structures defined in Figure 4.23 as function of the ITO carrier density.

In Figure 4.22, we noticed that the *bulk* work function decreases with increasing carrier density. Assuming the work function at the interface also decreases with increasing carrier density, this implies that an increasing interfacial TCO work function increases the V_{oc} of the MIS-like structures. The V_{oc} increase directly results from an increased internal voltage. High-work function TCOs on the a-Si:H(i/p) contact should, as a consequence, lead to higher performances. These results are confirmed by literature [Bivour 2012].

4.4.1.2 TCO work function investigations by lifetime curves

In this section we focus on the impact of the TCO material on the implied *JV* curve and, especially, the implied-*FF* (i*FF*) which is computed from the lifetime data. Based on the findings of section 4.3.2 and Figure 4.15, we use the impact of the TCO on the change in recombination statistics to rapidly probe the TCO work function at the a-Si:H/TCO interface and conclude on the TCO effect on the junction properties.

For this purpose, symmetric samples were prepared for photoconductance lifetime measurements with either *in*-stacks or *ip*-stacks on each side using an Octopus-II PECVD tool.[8] A TCO film was then co-deposited on the *in*- and *ip*-samples. ZnO and ITO were sputtered and 5-, 10-, 20- and 40-nm-thick ZnO buffer layers were deposited by ALD under the same conditions as described in section 4.3.2. Therefore, for the ALD ZnO:Al layers, the ZnO work function decreases with increasing thickness (section 4.3.2.2.1).

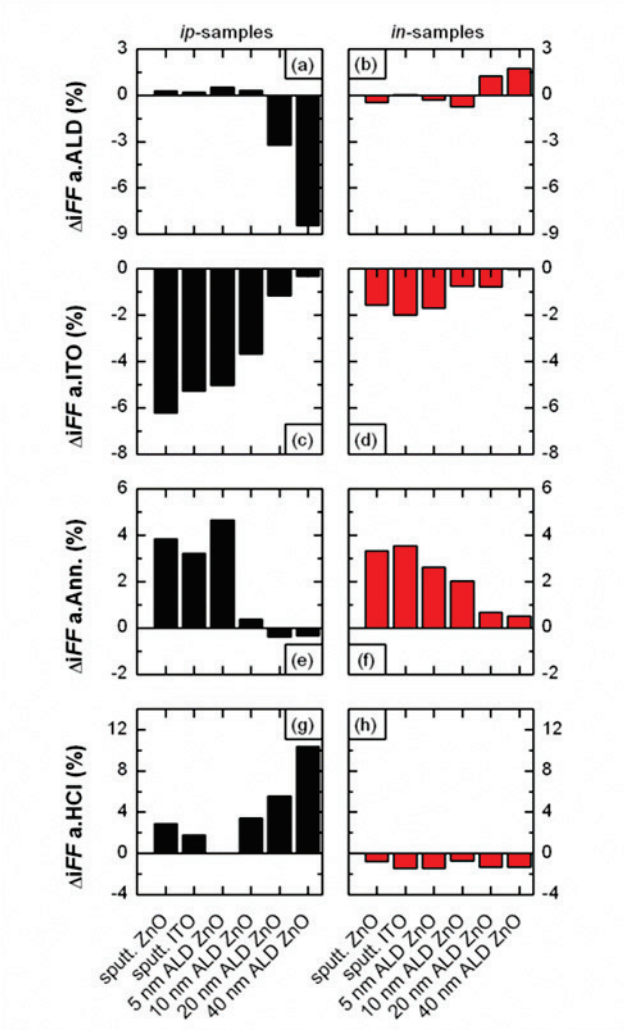


Figure 4.25: Variations in implied FF with respect to the preceding processing step, for the *ip*- and *in*-samples. (a, b) difference between as-deposited and after ALD, (c, d) after ITO, (e, f) after 25 min of annealing < 200 °C in air and (g, h) after stripping of the TCO stacks by HCl.

In Figure 4.25, the difference in i*FF* is plotted at four times during subsequent processing: (1) between the as-deposited state and ALD deposition (Figure 4.25 (a) and (b)), (2) between ALD deposition and ITO sputtering on all *in*- and *ip*-samples with 60 nm of ITO and on the sample with 60 nm of sputtered ZnO (Figure 4.25 (c) and (d)), (3) between the previous step and annealing for 25 min at 195 °C (Figure 4.25 (e) and (f)) (4) between annealing and etching of the TCO in HCl (Figure 4.25 (g) and (h)). The first three steps

[8] The amorphous layers used in this study are not the same as those in Section 4.3.2 as two different PECVD tools were used.

illustrate the discussion from section 4.3.2.2.2. The last step (Figure 4.25 (g) and (h)), removing the annealed TCO with HCl, is particularly interesting as we notice that for *ip*-samples, etching of the TCO increases the i*FF* and conversely, for the *in*-samples, it decreases the i*FF*. This indicates that the recombination statistics are changed by the TCO work function. At the a-Si:H(i/p) contact, as sketched in Figure 4.15, the TCO work function increases the recombination statistics. Conversely, on the a-Si:H(i/n) side, the TCO work function decreases the recombination statistics. Based on this observation and simulation in AFORS-HET [Froitzheim 2003], we can conclude that the TCO work function is lower than the a-Si:H(n) work function, as sketched in Figure 4.26 (c). Indeed, in the case of a higher TCO work function than the a-Si:H(n) work function, the recombination statistics would be negatively affected by the TCO's presence. From Figure 4.26 (c), we note that for decreasing TCO work function (<< a-Si:H(n) work function), the Fermi level will be pinned close to the a-Si:H conduction bands due to the charging of Urbach tail states induced by the Fermi level shift. These defect states at mid-gap will be negatively charged and counteract the effect of the TCO work function: a-Si:H cannot be degenerated [Street 2005].

From these measurements, we also confirm that the effect of the work function mismatch between the baseline sputtered ITO and the a-Si:H(p) layer induces 2–3% i*FF* losses.

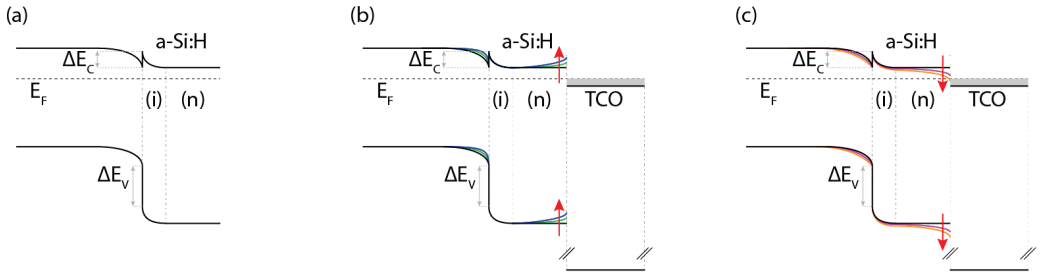


Figure 4.26 Schematic band diagram illustrating the effect of the TCO work function on the band alignment at the a-Si:H(i/n)-side. (a) Band diagram without TCO, (b) with a TCO work function higher than a-Si:H(n) and (c) with a TCO work function lower than a-Si:H(n). The arrows indicate the increasing work function mismatch. These sketches were supported by AFORS-HET simulations.

In this section, we demonstrated that comparing photoconductance lifetime measurements before and after TCO deposition is a fast way to gain valuable information on the TCO work function at the a-Si:H/TCO.

4.4.2 a-Si:H/TCO contact: contact resistivity measurements

As discussed in the previous section, the c-Si/a-Si:H/TCO stack acts as a metal–insulator–semiconductor contact, in which the TCO may affect the c-Si properties. Therefore, it is not representative to study only the c-Si/a-Si and a-Si:H/TCO contact separately. In this section, we focus on establishing a measurement method to characterize the contact resistivity of a c-Si/a-Si:H/TCO stack.

The transfer length measurement (TLM) technique is widely used to measure contact resistivity [Schroder 1984]. In this technique, the metal-semiconductor pads are separated by various distances as sketched in Figure 4.27. The pad size and the inter-pad spacing are designed to measure contact resistance

in a range accessible to the instruments used. The patterning methods of the pads depend on the feature sizes. Resistance between subsequent pads is measured with four-terminal sensing. The resistance is plotted as a function of the inter-pad distance.

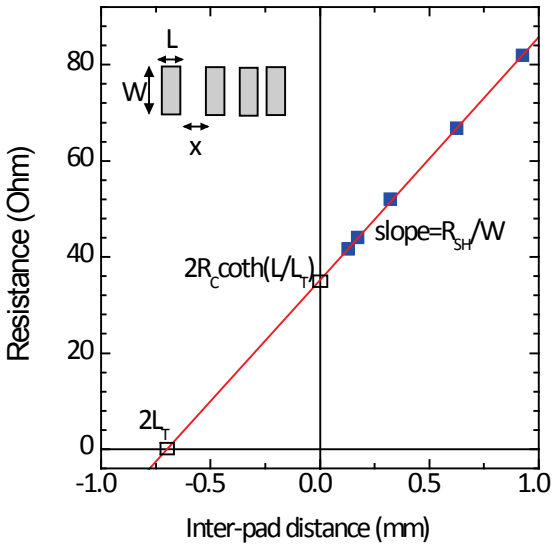


Figure 4.27: Transfer length measurement technique

The optimized solution for the contact resistance is then obtained by solving the nonlinear equation using a random starting point followed by iterations in the controlling Labview program:

$$R_{sh}{L_T}^2 \ tanh\left(\left(\left(\sqrt{\frac{R_{sh}}{\rho_c}}\right)L\right)^2\right) - \rho_c = 0$$

To investigate the c-Si/a-Si:H/TCO contact, a photolithography process using a negative tone photoresist followed by an etching of the Ag (TCO) in a diluted HNO_3 (HCl) solution was used to form micrometric inter-pad sizes (Figure 4.28).

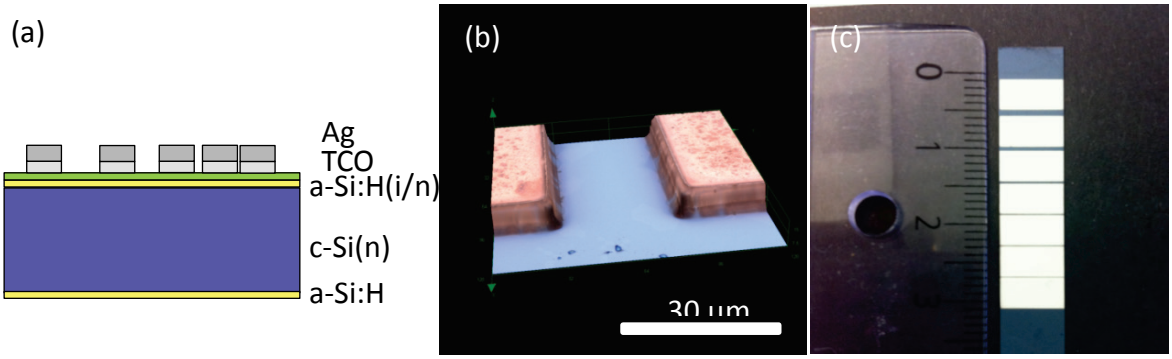


Figure 4.28: (a) Sketch of the structure of the TLM samples (b) Laser scanning microscope 3D reconstruction of a gap between two TLM pads processed by photolithography. The image has been taken after the TCO/metal etching and before stripping the resist (c) Picture of TLM structures patterned by photolithography.

Before measurement, the TLM samples were annealed for 25 minutes at 190 °C to ensure the same contact as in a SHJ solar cell (TCO crystallization). We note that if the samples are not annealed, the contact resistivity is typically an order of magnitude higher than for an annealed sample. The time between deposition of the a-Si:H layers, fabrication of the TLM structures and measurement must be kept as short as possible to prevent oxidation of the layers, which rapidly leads to increased contact resistivity values. The samples were cleaved the length of the pads (W) to prevent current flowing away from the edges of the TLM pads before being recollected. This step is usually known as mesa isolation. This undesired current flow leads to non-linear dependence between the resistance and inter-pad distances. To test the measurement coherence, different pad widths, *W*, were used. The results are plotted in Figure 4.29 and we observe a relatively good reproducibility.

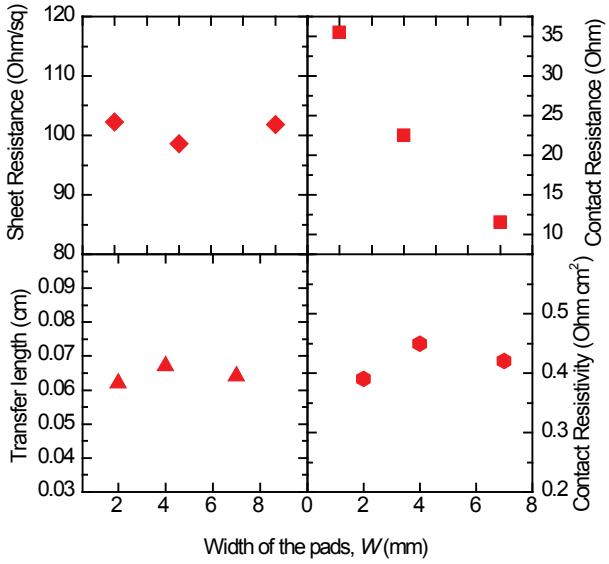


Figure 4.29: Variation of the TLM outputs as a function of pad width for a c-Si(n)/a-Si:H(i/n)/ITO/Ag structure (Figure 4.28).

The contact resistivity measured on a c-Si(n)/a-Si:H(i/n)/ITO/Ag stack is 0.4 Ωcm^2 and c-Si(n)/a-Si:H(i/n)/ZnO/Ag stack is 0.2 Ωcm^2, indicating the impact of different TCO material in the series resistance. However, more studies are needed to systematically address the effect of the TCO work function on the series resistance.

Probing the hole collector contact (c-Si(n)/a-Si:H(i/p)/TCO/Ag stack) with this technique, we expect the current flow to be well defined in the c-Si wafer as an inversion channel, arising from the band discontinuity at the c-Si/a-Si:H interface, from the a-Si:H doping and from the TCO work function, is present [Filipič 2013, Kleider 2011, Kleider 2008a, Maslova 2013]. However, in this case, a strong diode is measured which prevents current from flowing between the pads. Using a c-Si(p)/a-Si:H(i/p)/TCO/Ag stack, we observe hardly any current flowing between pads (Figure 4.30). When the TLM structure is illuminated we observe a diode-like behavior (Figure 4.30). The contact resistivity of the hole collector could not be reliably determined from these measurements.

In TLM structures, carriers have to cross the Ag/TCO/a-Si:H/c-Si(n) in two different ways:

(a) Similar to the case of a solar cell, carriers flow from the wafer to the contact.

(b) In the opposite direction.

To prevent carriers from flowing in the opposite direction, vertical structures can be used as described in Cox and Strack [Cox 1967] and Brooks [Brooks 1971]. Recently, Gogolin *et al.*, Lee *et al.* and Labie *et al.* have also used such structures [Gogolin 2014, Labie 2014, Lee 2014]. During this thesis, structures of various sizes with a front electron contact and a rear ohmic contact (c-Si(n)/Al) were processed. However, dark *JV* measurement did not show a linear dependence in the first trials. Further investigation is needed to have a coherent picture of this contact and evaluate the most relevant method of characterizing it.

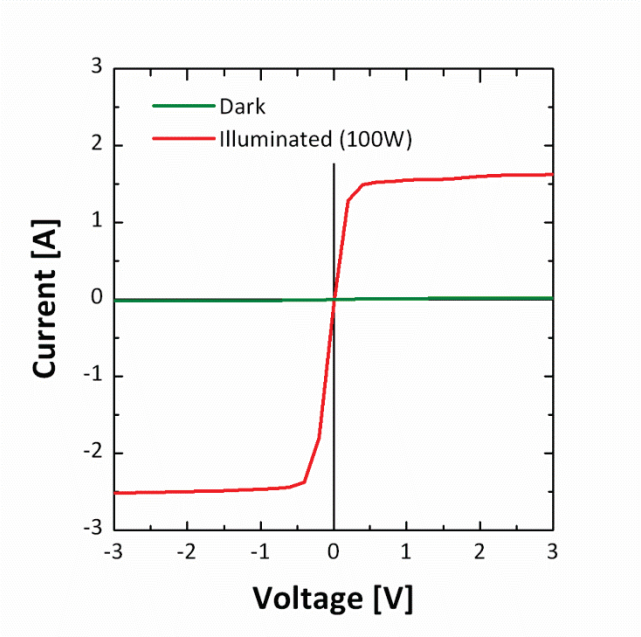


Figure 4.30: Current-voltage characteristics of a TLM structure to measure to contact resistivity of the hole collector on a c-Si(p) substrate.

4.4.3 TCO/metal contact

The TCO/metal contact resistivity can be obtained by TLM. The width and the length of the pads are 12.5 mm and 1 mm respectively and the pad spacing ranges from 0.1 to 2 mm. For patterning, a shadow mask during Ag sputtering is then used or the Ag is screen-printed. The contact resistivity is typically in the 10^{-2}–10^{-5} Ωcm^2 range [Geissbühler 2014]. As discussed previously, the contact resistance of the full contact stack is at least two orders of magnitude higher. Therefore, the TCO/metal contact is not the dominant contribution to the contact resistivity.

This contact can be decoupled from the optimization process of the TCO work function for the a-Si:H/TCO interface as TCO bilayers can be used [Barraud 2013, Gogolin 2014].

4.5 *FF* analysis in silicon heterojunction and passivating contact structures

As discussed in Chapter 2, SHJ may suffer from lower *FF* compared to homojunction solar cells. *FF*s are influenced both by recombination and transport losses. Distinguishing the origin of the *FF* losses is not straightforward. Here, a simple *FF* analysis method is presented to track to *FF* losses and their origin. This method is based on the work of many researchers [Khanna 2013, Pysch 2007, Sinton 1996a, Sinton 2000, Sinton 1996b, Swanson 1990]. To ensure clarity, Figure 4.31 summarizes this analysis method.

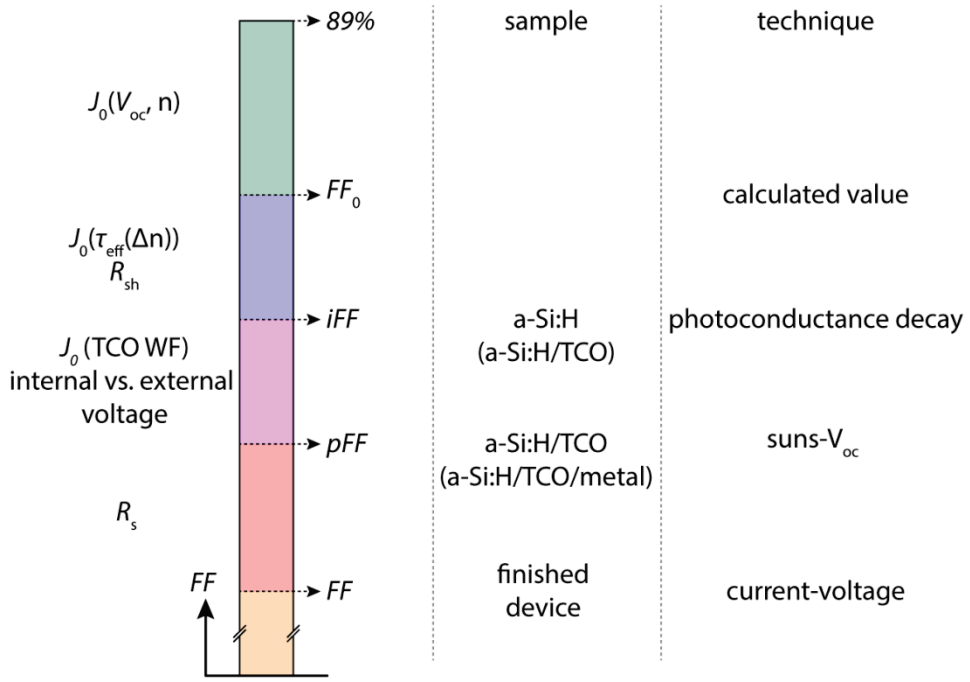


Figure 4.31: Summary of a *FF* analysis method

This figure reports on the different *FFs* often used in literature and useful to monitor during the process flow of a SHJ solar cell. The maximum theoretical value for a crystalline silicon solar cell was calculated to be 89% assuming a 100-µm-thick wafer and only radiative and Auger recombination processes [Tiedje 1984]. For a given V_{oc} and ideality factor, *n*, this value decreases to a specific *FF* limit, FF_0, which is generally computed using the equation given by Ref. [Green 1983a] (see Chapter 2). Other theoretical formulas exist as well [Khanna 2013, Swanson 1990]. The implied-*FF* (i*FF*) accounts for all the recombination losses (J_0) in the sample and corresponds to the internal voltage of the sample. It can be accessed using a photoconductance decay tool [Sinton 1996b] and can be measured after deposition of the intrinsic and doped a-Si:H layers and of the TCO overlayer. Shunt resistance are also taken into account in this measurement. Then, open-circuit decay measurements on a sample with the contacting layers (TCO or TCO/metal), knows as suns-V_{oc} measurements, give information on the recombination losses induced by the contacts (e.g. impact of TCO work function) as well as on a possible decrease in the quasi-Fermi level between the internal and external voltage [Sinton 2000]. To illustrate the difference between the internal and external voltage of a device, we plot the implied-*JV* (i*JV*), pseudo-*JV* (p*JV*) and *JV* curve of a SHJ solar with no a-Si:H(p) layer in Figure 4.32 (see section 4.4.1.1). As no current flows during this measurement, a series-resistance free *FF*

(p*FF*) is obtained [Wolf 1963]. Eventually, the real *FF* is measured using *JV*-measurements, which includes series resistance losses.

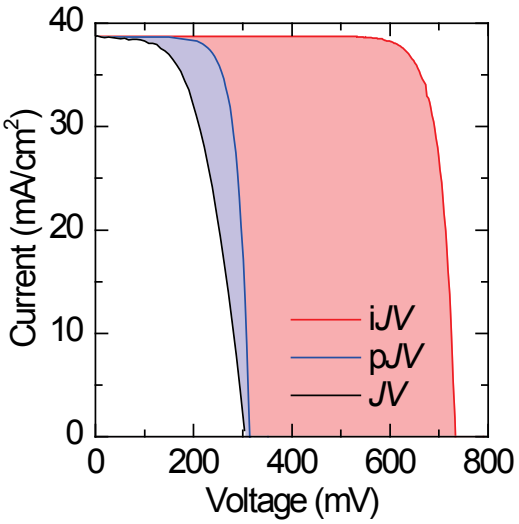


Figure 4.32: Implied-*JV* (i*JV)* of a a-Si:H(i)/c-Si(n)/a-Si:H(i/n) sample, pseudo-*JV* (p*JV*) of a TCO/a-Si:H(i)/c-Si(n)/a-Si:H(i/n)/TCO and *JV* curve of a sample with Ag/TCO/a-Si:H(i)/c-Si(n)/a-Si:H(i/n)/TCO/Ag, i.e. a SHJ solar cell with no a-Si:H(p) layer.

This analysis may be completed using temperature and illumination dependent *JV* curves to investigate the R_s losses [Pysch 2007, Seif 2014]. Future work is needed to assess to effect of the potential Schottky or V_{oc} pinning diode visible in high suns-V_{oc} measurements in this analysis (see Figure 4.19) [Bivour 2012, Bivour 2014a, Bivour 2014b, Green 1983b, Sinton 2000].

An example of a *FF* analysis for SHJ is presented in section 4.3.2. This analysis method can be generalized to silicon-based passivating contacts devices.

4.6 Summary and conclusions

In SHJ solar cells, thin a-Si:H layers passivate the surfaces of the c-Si absorber while guaranteeing charge collection through them. These passivating layers are the key feature to high-efficiency devices and hence significant attention is dedicated to their optimization. In this chapter, we report that these layers are damaged by subsequent sputtering of the transparent electrode[Demaurex 2012]. A drop of over 4% in V_{oc} was observed. We reported that this damage is at least partially caused by plasma luminescence during sputtering. Following low-temperature annealing, the passivation quality is almost fully recovered. However, the silicon–hydrogen configuration of the a-Si:H film is permanently changed, as detected from infrared absorbance spectra. This raises the question whether a damage-free deposition could enable devices with even higher V_{oc}s. To answer this, we used atomic layer deposition (ALD) to deposit a protective zinc oxide layer underneath the sputtered electrode. First, we showed that ALD does not induce any damage to the passivation at high injection. Secondly, we presented that an ALD layer efficiently protects against sputter damage if the layer thickness exceeds 20 nm. A first investigation of the consequences of this pro-

tective ALD layer at the cell level indicated that cells with thin protective ALD layers show neither direct V_{oc} nor *FF* improvement, even though higher pseudo-*FF* are measured. The latter is explained by the presence of a thin silicon oxide layer at the a-Si:H/TCO interface which impedes the collection of electrons and holes, resulting in increased series resistance and severe *FF* losses.

Using damage-free deposition for TCO, at the hole collector (a-Si:H(i/p) layers), we showed that a decrease in minority-carrier lifetime occurs in the low-injection region which is induced by the work function mismatch between the TCO and the underlying layers. The depletion of the a-Si:H(p) and, likely, of the a-Si:H(i) layer changes the recombination statistics at the c-Si/a-Si:H(i) interface by increasing the number of minority carriers at that interface. This recombination loss induces a decrease of 2-3% in the i*FF* for our devices. The TCO work function must be optimized to overcome these losses. At the electron collector (a-Si:H(i/n)), the lifetime decrease at low injection does not occur.

Affecting recombination losses and transport properties, the interfacial TCO work function is demonstrated to be efficiently probed using MIS-like structure and lifetime sample. The TCO work function may then be approached and optimized to prevent recombination losses. To characterize transport losses, contact resistivity measurements of the contact stacks were investigated using transfer length measurement. From this technique, the contact resistivity of the c-Si(n)/a-Si:H(i/n)/TCO contact could be obtained but not the one of the c-Si(n)/a-Si:H(i/p)/TCO contact. Further work is needed to assess the most relevant characterization technique, focusing on vertical structures. Eventually, we summarized a *FF* analysis method to access the *FF* losses in SHJ devices. This method can be easily extended to various c-Si–based passivating contacts.

Chapter 5 Passivating contact solar cells

In this chapter we present passivating contacts for homojunction solar cells based on silicon heterojunction contacts. First we show that amorphous silicon (a-Si:H) layers provide state-of-the-art passivation for highly doped n - and p- type surfaces. Then, the contact resistivity of this passivating contact is measured to be lower on highly phosphorus-doped crystalline silicon surfaces than on lowly doped ones. The design of the homo-hetero solar cells is studied by light-beam-induced current measurements and improved. The amorphous layer (a-Si:H(i) and a-Si:H(p)) thicknesses are then optimized for the homo-hetero contact. A detailed analysis of these cells is presented. Finally, we show that the homo-hetero structures test outperforms the conventional homojunction solar cell under in-the-field conditions thanks to the high internal voltage and low temperature coefficient induced by the passivating contacts.

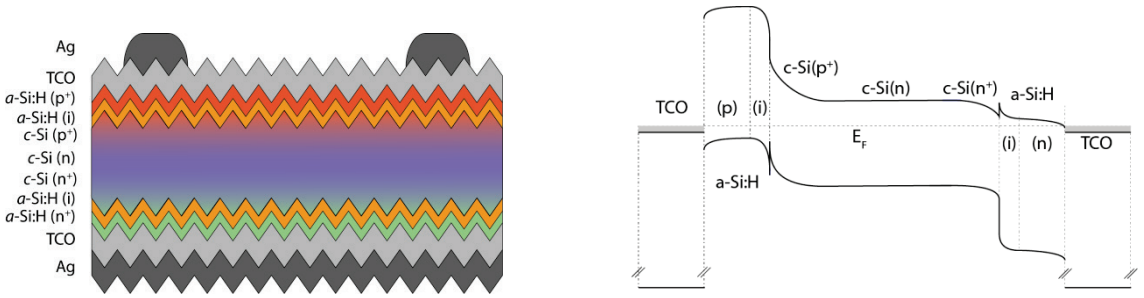
5.1 Introduction

Crystalline silicon (c-Si) homojunction solar cells currently account for over 90% of the module production on the photovolatics market, as discussed in Chapter 1. However, further progress of this technology is limited by carrier recombination losses due to direct contact between the semiconductor material and the metal. Hence, the efficiency of such solar cells is bound by a trade-off between recombination, expressed by means of the recombination current density prefactor J_0 and the contact resistivity ρ_c. So far, this trade-off has been optimized by using dielectric layers for surface passivation, combined with localized contacts. A better compromise may however be obtained by using passivating contacts, as discussed in Chapter 2.

Passivating contacts are the key feature of silicon heterojunction (SHJ) solar cells (Chapter 4), and they explain why these devices feature very high open-circuit voltages. Their implementation in homojunction solar cells may be advantageous as well. In principle, such contacts are metal-insulator-semiconductor-like and consist of (1) a thin (~10 nm) intrinsic amorphous silicon (a-Si:H) layer, providing excellent passivation of the c-Si surface; (2) an equally thin boron- or phosphorus-doped a-Si:H film, to form respectively the hole- or electron-selective transport layers; (3) a transparent conductive oxide (TCO), to provide lateral conductivity, efficiently contact the a-Si:H layers and enhance the optical performance of the solar cell; and (4) a front metal grid and rear full metal coverage to further improve lateral transport. In this chapter, to overcome the contact-recombination limitation of homojunction solar cells, we investigate the use

of amorphous layers to form a contact on c-Si wafers with diffused emitters, with the direct aim of increasing their voltage, especially under open-circuit conditions (V_{oc}).

Electrically, this approach can be viewed from two different perspectives: (1) from the homojunction perspective, where we wish to develop passivating contacts to increase their V_{oc} and (2) from the SHJ perspective, where we aim at reducing the contact resistivity of the existing contacts by increasing the surface doping of the underlying c-Si. The latter approach is briefly discussed in section 5.2 whereas the former is the focus of this chapter. In section 5.3, the J_0 and ρ_c values for phosphorus-diffused surfaces are investigated. We present, in section 5.4, test structures that have a full area a-Si:H-passivated c-Si surface, as shown in Figure 5.1. However, as discussed in Chapter 1, for ultimate device performance, patterning should be used to restrict the a-Si:H passivation to the area beneath the contacts, thereby avoiding parasitic light absorption in these layers. The remaining area would then be passivated by a transparent dielectric. In this way, the advantages of homojunction solar cells (minimal parasitic light absorption) can be fully combined with those of heterojunction technology (minimal recombination losses).



(a) (b)

Figure 5.1: (a) Sketch and (b) band diagram of a test structure for homojunction solar cells with passivating contacts.

Crystalline silicon wafers featuring emitters formed by (1) epitaxial films grown by low-temperature plasma-enhanced chemical vapor deposition (PECVD), (2) ion implantation and (3) diffusion are used as substrates. For each design, we give the J_0 values as they are key for these contacts. First, we show that homo-hetero solar cells featuring epitaxial emitters are limited by deposition time issues. The design of homo-hetero solar cells is then investigated and improved to minimize recombination losses using light-beam-induced current measurements. Then, we make a proof of concept of such homo-hetero carrier-selective contacts on ion-implanted and diffused wafers. Using various ion-implanted emitters and back-surface fields, we show that a-Si:H films passivate phosphorus- and boron-doped surfaces, which is commonly not the case for other passivating layers. The thickness of the intrinsic and doped amorphous layers, dictated by the wafer surface doping, is then optimized. A detailed analysis of the optimal structures is provided. Eventually, to benchmark our homo-hetero solar cells against homojunctions, we process

homo-hetero structures on high-efficiency emitters developed for conventional homojunction solar cells. We show that higher voltages are achieved in devices with passivating contacts. We evaluate the gain in efficiency for the passivating contacts devices to be 0.4–0.6% given all other cell parameters are kepts constant.

We draw the reader's attention to the changes in the homo-hetero cells' design throughout this chapter. The first-generation homo-hetero solar cells were 2×2 cm^2 solar cells on a 4-inch c-Si wafer with a full front emitter. This design was used for the homo-hetero devices featuring epitaxial emitters. The second generation featured 2×2 cm^2 cells with a patterned 2×2 cm^2 emitter and was used for the homo-hetero devices featuring ion-implanted emitters. The final cell design featured 6×6 cm^2 solar cells on a 6×6 cm^2 patterned emitter. The results of the homo-hetero devices on diffused wafers were obtained using the latter design.

5.2 Highly doped surfaces for silicon heterojunction solar cells

In this section, we investigate the homo-hetero solar cell proposed in this thesis from the SHJ solar cell perpective, i.e. a SHJ contact on a highly doped surface. The interst of this perspective arises from the fact that, as highlighted in Chapter 2, the contact resistivity of metal-semiconductor contacts and metal-insulator-semiconductor contacts decrease for increasing surface doping concentration [Roy 2012, Schubert 2006]. Thus, we investigate, here, whether changes in the c-Si surface doping could modify the SHJ in a similar way and thus decrease the series resistance (R_s) of SHJ contact.

This question is of particular interest as SHJ solar cells may suffer from low *FF*, despite high voltages, enabled by the excellent passivation of silicon surfaces by a-Si:H (Chapter 4). Indeed, high voltages at the maximum power point are a prerequisite for high *FF*. However, transport (ohmic or non-ohmic) losses can also severely limit the *FF*. While heterojunction solar cells rarely suffer from shunt losses, R_s may limit device performance [De Wolf 2014]. Usually, the TCO layers are sufficiently thin to not contribute transversely to any series resistance. Lateral conduction losses can easily be mitigated by tuning the TCO sheet resistance.[9] Similarly, the contact resistance between metal and TCOs is sufficiently low (Chapter 4.4.3), and will not be considered here. Therefore, we focus only on transverse resistance losses in this section.

As highlighted in Chapter 2, to achieve a low contact resistance, the c-Si(n)/a-Si:H(i/p or n)/TCO contacts must be engineered to lower the Schottky barrier height and width while maintaining a sufficiently low transport resistance through the a-Si:H layers as well as a low recombination rate at the c-Si/a-Si:H interface. Several methods to decrease the ρ_c value of SHJ devices have been investigated in literature. First, the thickness, bandgap and quality of the a-Si:H(i) are known to strongly influence the ρ_c value by changing the transport resistance through the a-Si:H

[9] To avoid undesired parasitic absorption losses, especially for long-wavelength light by free-carrier absorption, the sheet resistance should be tuned down by increasing the carrier mobility of the TCO.

layers [Rahmouni 2010, Taguchi 2008, Taguchi 2014]. Second, the a-Si:H(p) layer doping and thickness have a crucial effect on the *FF* by modifying the internal voltage in the wafer [Bivour 2012, Bivour 2014a, Bivour 2013]. Third, the TCO work function can be tuned to minimize the Schottky barrier height [Bivour 2014b] [Ritzau 2014].

In a novel approach, we address here the question whether changes in the c-Si surface doping, i.e. in the Fermi level, could provide a more efficeint energy band alignement for the SHJ contact such as to increase the majority carrier conductivity. We focus on the hole collector as this contact was reported to have a higher contact resistivity compared to the electron contact [Gogolin 2014]. For this purpose, we first need to estimate the local Fermi level position and effective free carrier concentration at the c-Si surface in a c-Si(n)/a-Si:H(i/p) structure. We then discuss whether a higher carrier concentration, induced by doping the c-Si surface, could be obtained.

At the hole collector of a SHJ solar cell, an inversion layer forms close to the c-Si(n) wafer surface as a consequence of (1) the band discontinuity at the c-Si/a-Si:H interface, (2) the a-Si:H doping and (3) the TCO work function [Kleider 2009, Kleider 2008b]. Here, we investigate the inversion layer formed at the c-Si(n)/a-Si:H(i/p) collector and deduce the resulting hole concentration in the c-Si wafer close to the a-Si:H layer. For this, we perform simulations with AFORS-HET, a software developed at Helmholtz-Zentrum Berlin [Froitzheim 2003, Stangl 2006]. The parameters used for this simulation are typical values used for our SHJ solar cells. A simulated band diagram of a silicon heterojunction is shown in Figure 5.2.

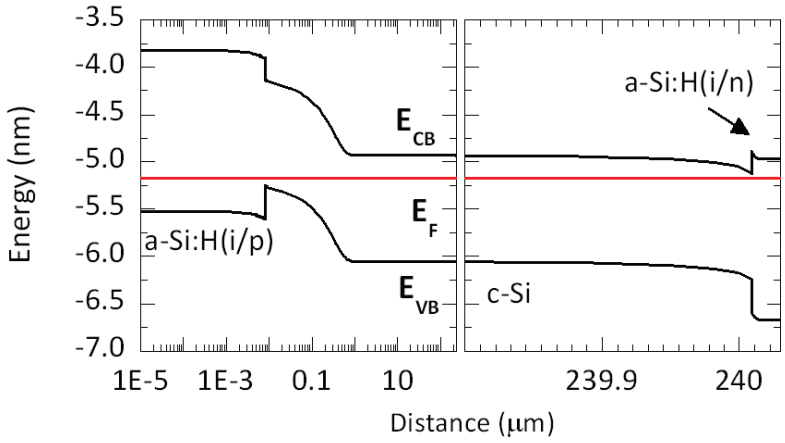


Figure 5.2: Energy band diagram of a SHJ simulated from AFORS-HET, in the dark, under thermal equilibrium in short-circuit conditions.

For such simulations, the a-Si:H(p) doping is needed. Secondary ion mass spectroscopy (SIMS) measurements cannot be used for this purpose as SIMS yields the total amount of boron present in the a-Si:H layer (typically 1 10^{21} atoms/cm^3 for our a-Si:H(p) baseline layer) rather than only the active dopants which is what is needed for the simulations. Therefore, the a-Si:H(p) doping is evaluated by dark conductivity measurements (section 3.4.3). From such

measurements, an activation energy (E_{act}) equal to 0.45 eV is deduced and the resulting Fermi level (E_F) position may be estimated. However, as the E_F does not remain fixed with varying temperature, the E_{act} does not directly equal the E_F with but must be corrected by the statistical shift: E_{act} – 150 meV = $E_F - E_{VB}$, where E_{VB} is the energy level of the valence band [Shah 2010]. From this approximated E_F value, a corresponding a-Si:H(p) doping of about $6.8 \cdot 10^{19}$ cm^{-3} is calculated. Consequently, the simulations show that the E_F of the c-Si wafer is 0.08 eV above the E_{VB} at the c-Si/a-Si:H contact.[10] This would correspond to a local inversion doping concentration of typically $1.5 \cdot 10^{18}$ cm^{-3} in the c-Si material. These values correspond to literature values of 0.4 to 0.6 eV for a valence band offset between the c-Si and a-Si:H layers [Filipič 2013, Kleider 2011, Schulze 2011b, Varache 2013]. For comparison, a higher E_{act} of 0.50 eV would only give rise to an equivalent doping concentration in the c-Si wafer of $5 \cdot 10^{17}$ cm^{-3}. As discussed in Chapter 4, the presence of the TCO may deplete the a-Si:H layers and reduce band bending in the c-Si wafer. This effect is not taken into account here and the calculated value then represents an upper limit for the carrier concentration.

In the c-Si(n)/a-Si:H(i/p) contact, we determined a carrier concentration in the inversion layer of the c-Si wafer on the order of 10^{18} cm^{-3}, in agreement with the literature [Kleider 2011]. Much higher dopant concentration may be obtained in silicon (Chapter 3). Thus, for SHJ contacts, introducing a highly doped c-Si layer might improve their ρ_c value. However, no experimental data support this hypothesis so far.[11] In the next sections, we will benchmark the ρ_c values obtained for homo-hetero structures with undiffused or ion-implanted-free structures to pursue this perspective.

5.3 Characterization of homo-hetero contacts

To evaluate the potential of these homo-hetero carrier-selective contacts, J_0 and ρ_c were measured on symmetrical test structures having a full area a-Si:H-passivated c-Si surface. The c-Si substrates were diffused using a $POCl_3$ process followed by a drive-in process at six different temperature combinations at the Australian National University (ANU). The resulting dopant profiles measured by electrochemical capacitance voltage (ECV) are plotted in Figure 5.3.

For such bifacially diffused surfaces, the most straightforward way to compare their passivation levels is by evaluating the associated J_0 value. This value will strongly depend on the doping of the surface, as well as on the passivating properties of the overlayers. The J_0 value is extracted using the Kane and Swanson method, described in Chapter 2. For this, an injection

[10] We note that, in AFORS-HET, the Maxwell-Boltzmann statistics are implemented whereas the Fermi-Dirac are not. This implies that, for the simulations to be valid, the energy difference between the valence band (VB) and the Fermi level (E_F) should be larger than 3 kT/q.

[11] A simulation study by Sihua *et al*. indicated that series resistance of such homo-hetero structures was decreased compared to a heterojunction solar cell, due at least partially to the thinner a-Si:H layers used in the homo-hetero simulated device and not to the mere presence of the c-Si doped region [Sihua 2013].

level ten times that of the base doping and an intrinsic carrier concentration at 25 °C of $8.6 \cdot 10^9$ cm^{-3} were considered [Kane 1985]. The Auger model proposed by Sinton *et al.* ($\tau_{AUG} = \frac{1}{\Delta n^2 * 1.66 * 10^{-30}}$) was used [Sinton 1987].

Regarding dielectric passivating layers, Plagwitz *et al.* demonstrated that a-Si:H/SiN_x stacks provided good passivation on diffused phosphorus and boron emitters [Plagwitz 2006]. This is a non-trivial result, as most dielectrics do not offer equally good passivation on both doping types: they prefer to passivate p-type surfaces (such as AlO_x, due to the presence of fixed negative charges), or n-type surfaces (such as SiO_x and SiN_x, due to the presence of fixed positive charges). It is of note that a-Si:H layers (without SiN_x) also offer excellent symmetric passivation, as a-Si:H passivation principle mostly relies on interface state reduction by hydrogenation, rather than a field effect.

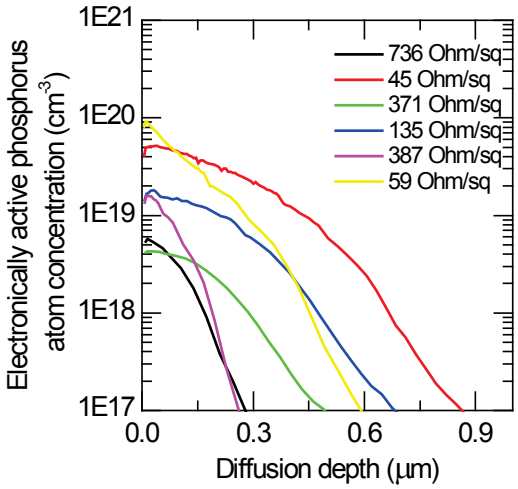


Figure 5.3: Electrically active phosphorus diffusion profile and associated sheet resistance against diffusion depth. The sheet resistance calculation utilizes the mobility model described in [Klaassen 1992].

Here, to have a-Si:H layers similar to the final electron collector structure, an 11-nm-thick a-Si:H(i/n) stack was deposited by PECVD. Figure 5.4 shows J_0 as a function of the phosphorus surface concentration (Figure 5.4(a)) and the sheet resistance (Figure 5.4(b)). Amorphous silicon layers achieve similar J_0 values compared to the state-of-the-art SiO_x layer. We observe J_0 to decrease with decreasing dopant surface concentration (and thus increasing sheet resistance), as expected from Chapter 2. Capping the a-Si:H layers with a sputtered TCO did not lead to significant changes in the J_0 values after annealing for 25 minutes at 190 °C (data not shown). This is in agreement with data discussed in section 4.3.2 for an undiffused c-Si substrate.

In Figure 5.4, we also plot literature values for the dependence of the J_0 of metallized samples (no passivation layer) on the dopant surface concentration and the sheet resistance. Contrary to passivated samples, J_0 increases as the dopant concentration decreases. This is explained by the high interface defect states density at the metal/c-Si interface. Field-effect pas-

sivation, induced by the dopant profile, then dominates the effective surface recombination velocity and thus the J_0. The opposing trend between the passivated and metallized sample underlines the key feature of the homo-hetero device: passivating contacts. The J_0 values measured here using a-Si:H layers may be the same as in the finished, fully contacted, device. Conversely, the J_0 of a homojunction device is the area-weighted sum of the J_0 of the passivated area and of the contacting area (Chapter 2).

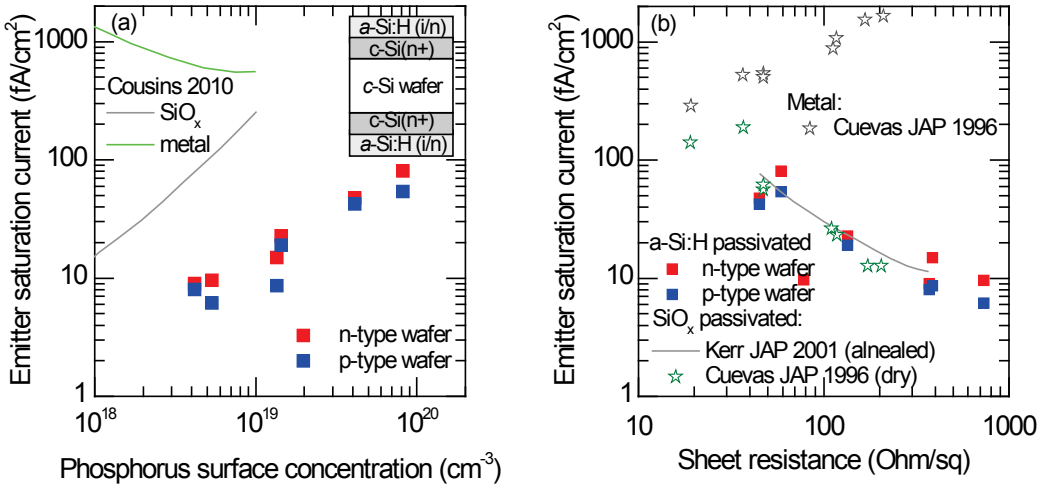


Figure 5.4: Recombination current prefactor as function of (a) surface dopant concentration and (b) sheet resistivity for $POCl_3$ diffused c-Si surfaces passivated by 11-nm-thick a-Si:H(i/n) stacks. Data taken from [Cousins 2010], [Kerr 2001] and [Cuevas 1996].

The ρ_c value of the electron collector was measured by the transfer length method (section 4.4.2). These test samples were fabricated from samples identical to the passivation samples, except with additional pads of ITO/Ag. The a-Si:H, TCO and metal layers were co-deposited for all samples. As shown in Figure 5.5, we find values in the 0.3–0.5 Ωcm^2 range. Thus, the ρ_c values of the homo-hetero structure are typically an order of magnitude higher than those of contacts in homojunction solar cells [Tous 2014].

Figure 5.5 also highlights that the underlying diffusion provides a lower contact resistivity, compared to a diffusion-free wafer. As discussed in the previous section and according to Roy *et al.*, in tunneling contacts, the substrate semiconductor doping can play an important role in the contact resistivity for thin insulator layers [Roy 2012]. Our data suggest that it also plays a role in our contact.

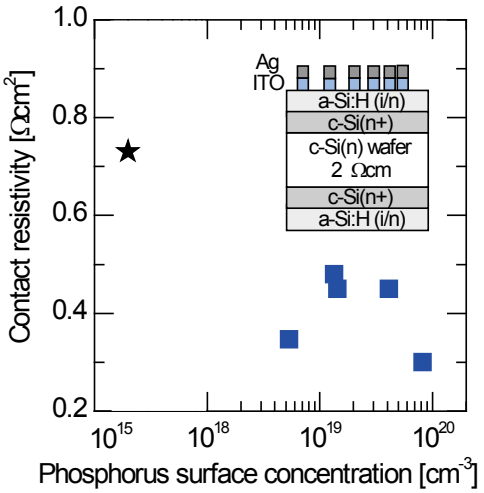


Figure 5.5: Contact resistivity as a function of surface dopant concentration for diffused c-Si surfaces passivated by 11-nm-thick a-Si:H(i/n) stacks. The star-shaped data point indicates the contact resistivity of a SHJ contact (no diffusion) co-processed with the diffused sample.

5.4 Homo-hetero solar cells

Motivated by the promising J_0 and ρ_c results, we implemented the homo-hetero contacts in devices. This section first presents results from the emitter formed by epitaxial films grown by PECVD (section 3.4). In section 5.4.2, we discuss improvements to the design of the passivating contact cells. Finally, we present the results obtained with junctions created by using ion implantation (section 5.4.3) and diffusion (section 5.4.5).

5.4.1 Homo-hetero solar cells using an epitaxially grown emitter

In section 3.4, we showed that high-quality epitaxial layers could be grown by low-temperature PECVD. However, due to the diffusion length of the adatoms for the growing film, high-quality films are obtained only on {100} oriented surfaces. Therefore, alkaline textured wafers, which surfaces consist of {111} faceted pyramids, cannot be used for devices featuring homo-epitaxial emitters.

In this section, we use a <100> p-type double side polished wafer and grow phosphorus-doped homo-epitaxial films to form a homojunction. Passivating contacts using a-Si:H layers are then used in a similar way as in a SHJ cell (Chapter 4).

Homo-hetero cells were processed with a 10-nm-thick epitaxial film for various dopant concentrations, defined as the ratio between the phosphine flux and the silane flux (Chapter 3). The current-voltage (*JV*) characteristics of these cells as function of dopant concentration in the epitaxial layer are shown in Figure 5.6 and the cell structure is shown in the inset. The SHJ baseline on a flat p-type wafer is given as a reference in red. In the film with the highest phosphine

concentration, an epitaxial-to-amorphous breakdown occurred after 2 nm of growth, likely due to defect accumulation owing to the incorporation of phosphorus atoms (Chapter 3).

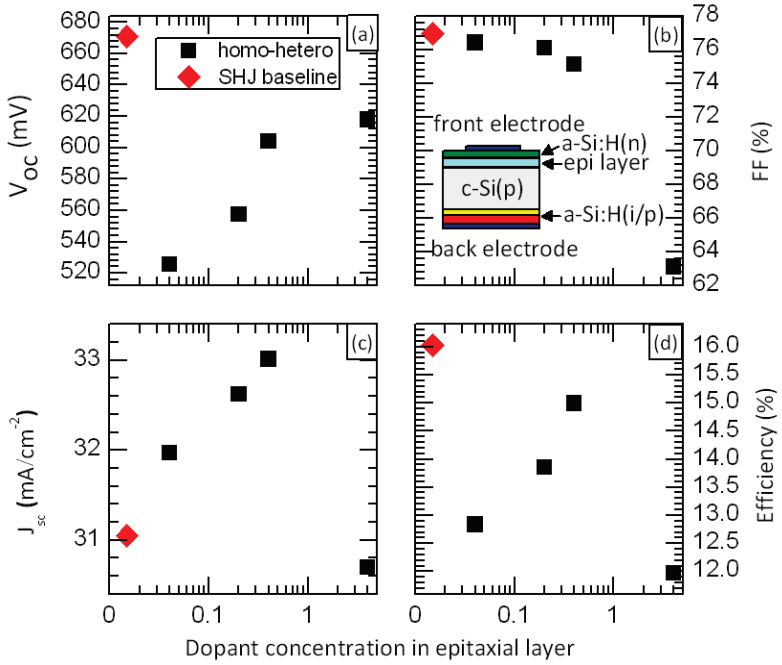


Figure 5.6: *JV* parameters of cells with a homo-epitaxial layer with a structure as sketched in the inset. The red diamond-shaped data points represent a silicon heterojunction baseline with an a-Si:H(i) layer. The back and front electrodes are formed by ITO and silver. An epitaxial breakdown occurred in the layer with the highest dopant concentration.

First, we focus on the V_{oc} of the processed cells (Figure 5.6(a)). Due to an enhanced field-effect passivation, the V_{oc} improves when increasing the dopant concentration in the epitaxial films. As evidenced in the *JV* results, the V_{oc} of the homo-hetero devices is lower than the SHJ counterpart and can be explained by the absence of the a-Si:H(i) buffer layer. We now investigate the effect of adding an a-Si:H(i) layer on the carrier transport in homo-hetero devices using temperature-dependent *JV* measurements. Figure 5.7 shows the temperature-dependent *JV* parameters of a homo-hetero cell with an a-Si:H(i) layer compared to a SHJ baseline. By adding this layer, we observe a strong increase in the V_{oc} from 618 to 661 mV for the homo-hetero solar cell due to the enhanced passivation. However, a severe decrease in the fill factor (*FF*), compared to homo-hetero cells without the a-Si:H(i) layer (Figure 5.6) is observed. Unfortunately, this results in poorer device performance for the homo-hetero cells with the a-Si:H(i) layers. The sharp decrease of the *FF* may be attributed to an increased R_s for these solar cells due to the presence of the 7-nm-thick a-Si:H(i) layer which impedes the electron flow [Seif 2014]. Unfortunately, thinner a-Si:H layers cannot be achieved due to limitations of the deposition reactor hardware: current deposition times are already as brief as a few seconds, and cannot easily be further reduced. Approaching the hardware limitations also results in thickness variations, pre-

venting fair and meaningful comparison between cells: the a-Si:H layer of the homo-hetero cell is measured to be 2 nm thicker than the one of the SHJ baseline cell. We note that this is not a limitation for textured wafers as the deposited layer is 1.7 times thinner due to the random pyramid structure. However, deposition of epitaxial emitters on such textured surfaces is not a straightforward task, as textured surfaces feature pyramids with {111} oriented facets. In Chapter 3, we discussed how the quality of epitaxial material critically depends on the wafer orientation.

Therefore, to overcome the limitation with intrinsic buffer layers on epitaxial emitters, an a-Si:H(n) was developed with improved passivation quality. This layer, without the presence of an a-Si:H(i) passivating layer, yielded implied-V_{oc} above 730 mV in a SHJ structure (as opposed to the 650 mV of the baseline a-Si:H(n) layer), which is a remarkable result. However, this layer affected the electronic properties of devices causing S-shaped *JV* curves as well, likely because of insufficient doping (data not shown).

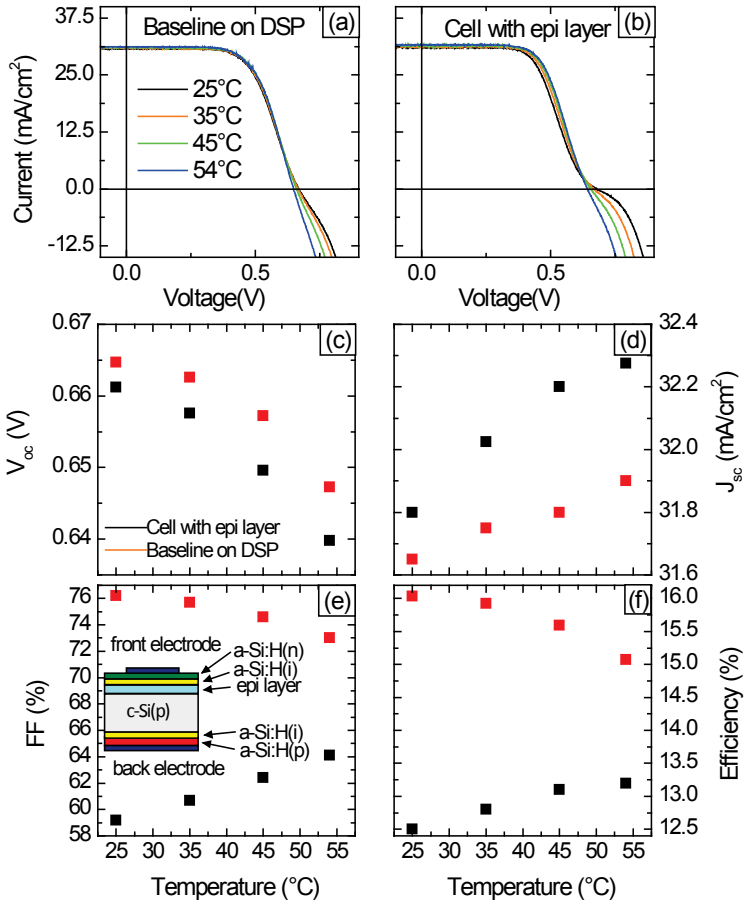


Figure 5.7: *JV* temperature dependence of a silicon heterojunction baseline on a double side polished (DSP) wafer with an a-Si:H(i) layer below the a-Si:H(n) with and without an epitaxial layer for a dopant concentration of 0.4.

Second, in Figure 5.6, we observe an increased current density (J_{sc}) for homo-hetero devices compared to the SHJ baseline device, except for the cell with the breakdown of the epitaxial-to-amorphous film (dopant ratio ~4, data point on the far right). To further investigate this behavior, the internal quantum efficiency, which is the ratio of the number of charge carriers collected to the number of photons at each wavelength absorbed in the cell, is plotted in Figure 5.8. In such measurements, the reflected or transmitted photons are not taken into account. At short wavelengths, corresponding to absorption at the front of the cell, we observe less parasitic absorption in the homo-hetero cells. Conversely, the SHJ baseline shows a higher IQE between 500 and 1000 nm. At longer wavelength, the four curves overlap as expected as all the cells have the same rear sides and similar front TCOs leading to similar free-carrier absorption. From optical studies of SHJ solar cells made in our laboratory, the front a-Si:H(i) layer parasitically absorbs over 0.1 mA/cm^2 per nm [De Wolf 2014, Holman 2012]. Moreover Jensen et *al*. showed that in a SHJ formed on a p-type wafer with an *a*-Si:H(n) layer [Jensen 2002], 85% of the photogenerated carriers the *a*-Si:H(n) recombined. Therefore, the increase in current for the homo-hetero layers cannot be solely explained by the absence of the intrinsic a-Si:H layer. This current increase could correspond to an enhanced charge collection from the photogenerated carriers in the epitaxial film at J_{sc} conditions. Further investigations are needed to assess this phenomenon.

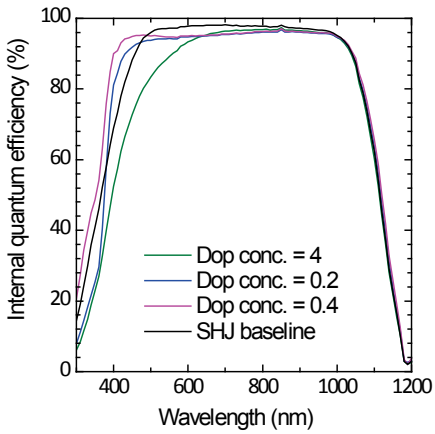


Figure 5.8: Internal quantum efficiency of cells for four cells presented in Figure 5.6.

Third, looking back at Fig. 5.6, the *FF* decreases for more conductive layers indicating that the carrier collection at the voltage at maximum-power-point (V_{mpp}) is hindered. This effect will be discussed in the next section.

To further improve our devices on double side polished wafers, several solar cell series were processed and measured. However, all cells yielded S-shaped curves due mainly to processing but also contamination issues that affected all cells in our laboratory for several months. Further investigations are needed to yield higher efficiency cells using epitaxial layers.

To conclude, we demonstrated homo-hetero structures using an emitter grown by low-temperature homo-epitaxy. We demonstrated the field-effect passivation of such layers and evidenced *FF* losses. To yield higher performances on such structures, PECVD tools yielding lower achievable deposition times are needed.

5.4.2 Homo-hetero solar cell design

The first generation of homo-hetero cells were processed using wafers featuring a diffusion over the full front and/or back surface, depositing a-Si:H layers on the full front and full back of the wafer and patterning the front TCO, as pictured in Figure 5.9. The back TCO/Ag stack is sputtered on the full back surface.

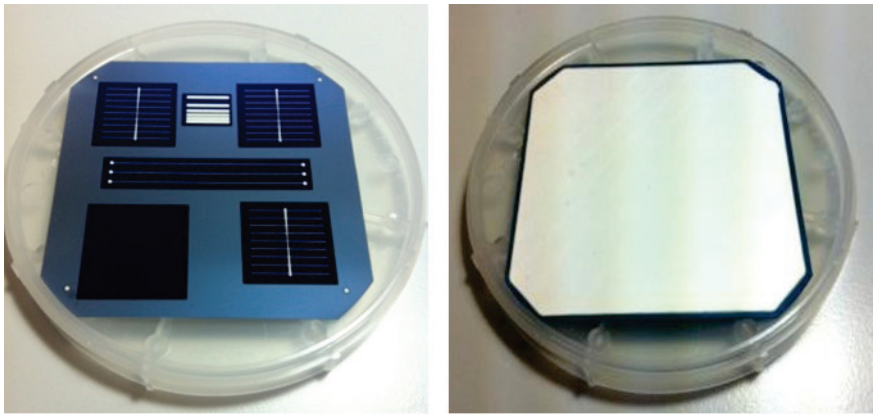


Figure 5.9: Photograph of the (a) front and (b) back of the first-generation 2×2 cm^2 homo-hetero solar cell.

By using this design, the homo-hetero cells systematically yielded *FF*s lower than 74% for highly doped c-Si surfaces, contrasting with the anticipated increase in *FF* for these devices compared to SHJ devices (see section 5.3). Moreover, the total collected current, deduced from the external quantum efficiency (EQE) measurement, was lower than the J_{sc} value from the illuminated *JV* measurements. For such measurements, the cell is in J_{sc} conditions and only part of the cell is illuminated (the EQE spot size is 0.5×0.5 cm^2). As shown in Figure 5.10, the collection of the photogenerated charges depends on the size of sample measured using a probe.

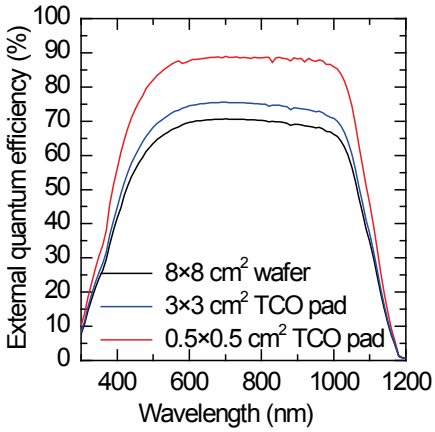


Figure 5.10: External quantum efficiency of a homojunction cell with passivating contacts with varying TCO pad size. The J_{sc} value of this cell from a *JV* measurement was 35.7 mA/cm^2.

These observations were then related to the extension of the doped region outside the cell region, which thus acts as a lateral transport channel, conducting the charges away from the collection area.

To investigate this potential design loss, light-beam-induced current (LBIC) measurements were performed using a custom system. A schematic of the experimental setup is presented in Figure 5.11. A red solid-state laser (λ=650 nm) pulsed at a 72.4 Hz frequency is used for scanning the cell parallel to the busar. To place the cell in real operating conditions, a halogen lamp with a 1-sun intensity is used as light bias. The cell was connected via a Kelvin probe to a transimpedance amplifier which fixes the voltage of the cell at a constant and transduces the current variation (δI) to a voltage signal (δV) read by a lock-in amplifier. The lock-in amplifier allows us to perfectly separate the contributions of the laser from those of the bias light. A Labview program records the intensity of the laser signal and provides the voltage setpoint to the transimpedance amplifier.

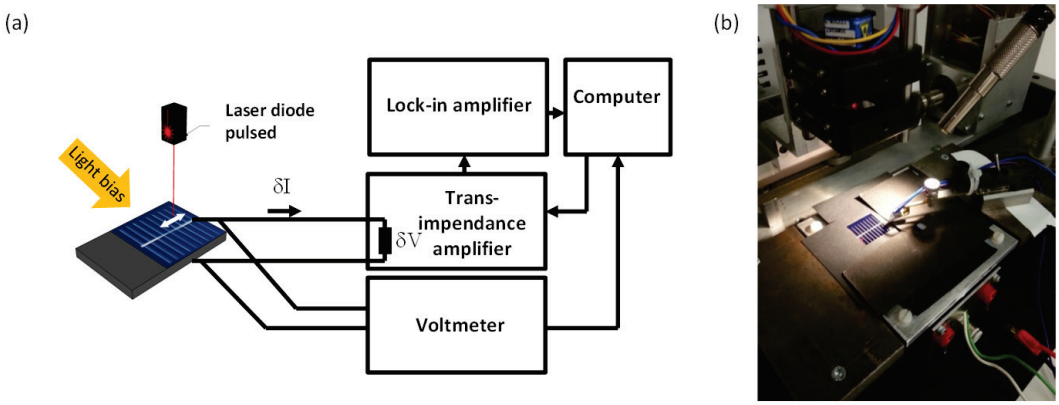


Figure 5.11: (a) Schematic of the LBIC setup. (b) Picture of a LBIC measurement.

LBIC intensity measurements displayed in Figure 5.12 provide information on the collection of the generated carriers. Figure 5.12(a) plots the LBIC signal for a SHJ reference cell in the dark and with bias light under J_{sc}, V_{mpp} and close to the V_{oc} conditions. The sharp drop in the signal intensity observed at regular intervals is caused by the silver fingers which reflect entirely the laser beam.

Several observations come out of this measurement, which can be classified according to the region in which the effects occur, in the cell or in the adjacent passivated wafer:

1. The LBIC signal intensity depends on the voltage of the cell. This effect is directly related to the *JV* curve. When approaching open-circuit, the collection probability decreases.
2. An interesting effect occurs at the cell edges, between the last finger and the TCO edge. We observe a different LBIC signal intensity depending on the applied voltage. Under maximum power point and open-circuit, we measure a decay in the LBIC signal, which is not seen at short-circuit. This decay is induced by an increased amount of current flowing through the front TCO, leading to an important voltage drop across this TCO area. In contrast, at J_{sc} conditions, the local voltage remains in the flat part of the *JV* curve and the collection probability is not affected, hence this decay is not to be seen.
3. For similar reasons, we observe at V_{oc} conditions (blue line) a decrease of the LBIC intensity in-between the fingers.
4. Focusing now on the effect of moving out of the TCO, i.e. onto the passivated wafer without any TCO electrodes, we observe an exponential decay which corresponds to the carrier diffusion process in the bulk. Fitting this slope at J_{sc} conditions in the dark, the diffusion length of the carriers can be extracted (using function $\exp(-x/L_D)$) and yields in this case of a diffusion length of 1.2 mm. Under illumination (J_{sc}, illum), we observe an increase of the diffusion length to 1.3 mm. This increase is consistent with the injection dependency of the minority-carrier lifetime: At high injection, often the carrier lifetime is higher, yielding thus longer diffusion lengths. We also observe that the intensity is reduced by ~10% in this area compared to the SHJ reference cell due to the absence of an anti-reflective coating layer, coupling then less efficiently the laser beam into the cell.

Now, looking at the LBIC signal of a homo-hetero solar cell in Figure 5.12(b), a striking difference is observed under the J_{sc} dark condition for the part without TCO coverage. Here, a constant collection is observed instead of the exponential decay. This effect is attributed to the diffused junction providing an efficient lateral conductive channel for the generated carriers similar to the front-TCO, as sketched in Figure 5.13(a). Conversely, when the cell is illuminated by a bias light but still in J_{sc} conditions, this collection effect is not observed anymore. We explain this phenomenon as follows: As more current flows through the channel, a potential drop is established in the conductive channel. Then, when moving away from the cell edges, the local potential becomes closer to the one under V_{oc} condition and, according-

ly, the collection probability decreases. To explain these observations, an equivalent electronic circuit is proposed in Figure 5.13(b).

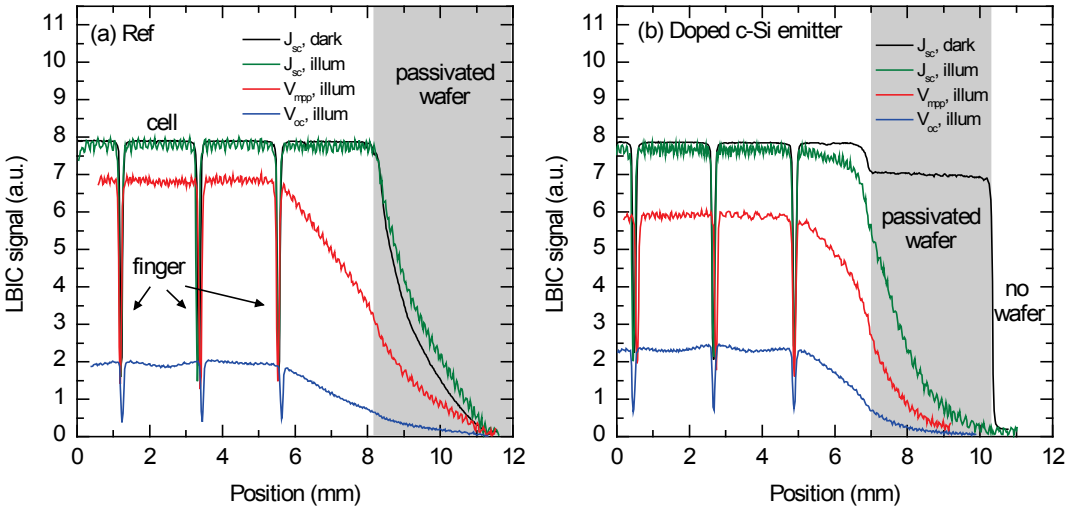


Figure 5.12: LBIC measurement of (a) a reference cell and (b) a homo-hetero cell. The shaded area corresponds to areas of the passivated wafer without TCO.

Here, we relate the LBIC observations to device performance. In *JV* measurements, a black mask defines the cell area. Thus no light is generated outside the cell area and this unilluminated area is in the same state as for LBIC measurements in the dark. In this situation, two competing phenomena then occur: (1) as carriers diffuse outside the cell area they can be nevertheless collected if re-conducted by the doped channel and (2) the emitter area contributing to the J_0 value of the measured cell is thus much larger than the illuminated cell area. This leads to a decrease in V_{oc} and *FF*.

We note that in the case of rear emitter SHJ cells, a measurement artifact with the same characteristic has been observed [Descoeudres 2013].

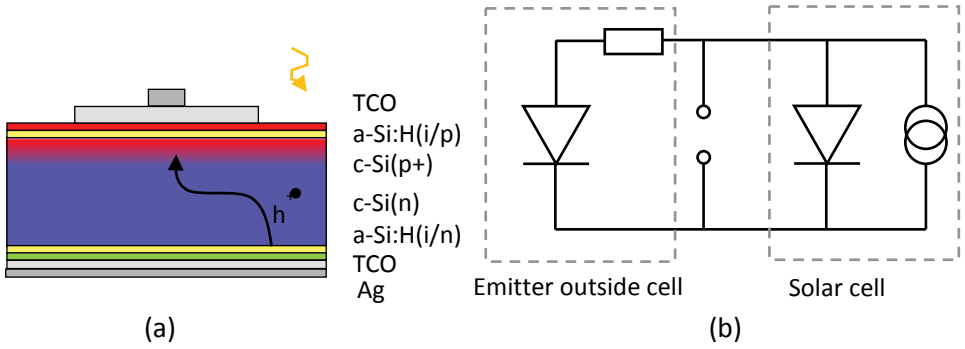


Figure 5.13: (a) Schematic and (b) electronic diagram of the first generation of the homo-hetero cell design.

To prevent such losses, the doped area is required to be the same size as the cell. As the diffused or ion-implanted wafers are received with their full front sides doped, they need to be etched back to the size of the cell. Two approaches are possible: patterning the homojunction before or after deposition of the a-Si:H layers. As seen in Chapter 3, the homojunction depth varies between a few tens of nm to a few µm. Chemically etching a selected region on the wafer can be done using a similar process to obtain a single-side diffused wafer, as explained section 3.2. However, as this involves multi-step processing, a dry etching process using SF_6 is preferred. Conveniently, as ITO is not etched by SF_6, it directly protects the underlying layers. However, silver oxidizes and is etched when exposed to such plasmas; a protective layer is needed for the present metals. For this purpose, three different layers were tested on a standard heterojunction cell: (a) a piece of glass placed on top of the cell area, (b) ink deposited by a water-soluble pen and (c) a liquid plastic solution (P70), applied with a brush, which solidifies in air (15–30 minutes drying time) and which can be removed with acetone. In Figure 5.14, the *JV* curves of the tested cells before and after etching are plotted.

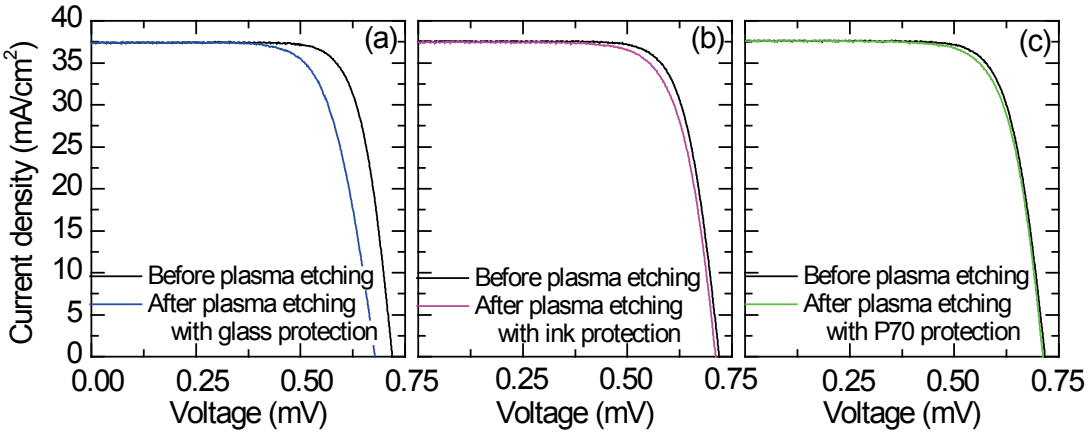


Figure 5.14: *JV* curves of cells before and after plasma etching with (a) glass, (b) ink from a water-soluble pen and (c) liquid plastic P70 protective layer.

The glass protection prevented neither the silver oxidation on the cell edges nor a passivation loss, as evidenced by its brownish color. Thus, this lack of protection induced a strong loss in V_{oc} and *FF,* as observed in Figure 5.14(a). The ink protection also damaged the passivation quality, likely during the ink dispensing (Figure 5.14(b)). Consequently, the protective layer that impacted the solar cell performance least used the liquid plastic protection (Figure 5.14(c)). It is noteworthy that this technique did not induce any losses with an ITO TCO but did with an indium oxide/ITO stack.

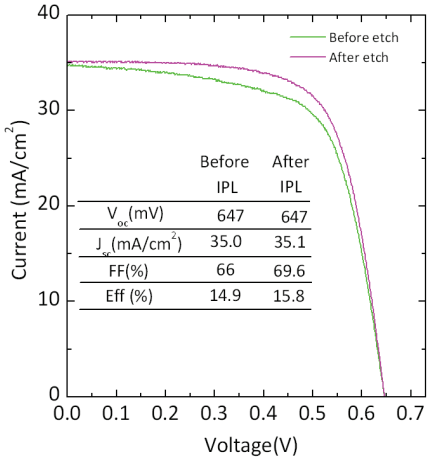


Figure 5.15: *JV* curve of a homo-hetero cell before and after back-etching of the doped region outside the cell area.

Therefore, patterning the crystalline doped region prior to PECVD would be convenient and prevent edge recombination losses. For this purpose, a process was developed based on local SF_6 etching around the future cell area protected with a liquid plastic solution. Subsequent to the acetone bath to remove the plasticized layer, a stringent cleaning was needed, typically using a piranha solution, to remove the organic residues. This cleaning step was key to obtaining high-efficiency and reliable devices. To avoid contamination of the cleaning baths used in the standard surface conditioning after texturization, the cleaning for this process was done in separate beakers. Moreover, for safety reasons, the bath volume was restricted and only a single wafer could be cleaned at a time. The reproducibility of this process was then insufficient to study the homo-hetero cell structure, as can be seen in Figure 5.16. The patterning of the cell region was then rather performed after PECVD.

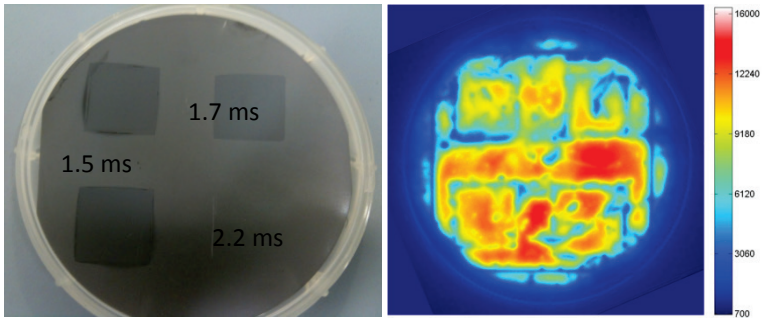


Figure 5.16: Photograph and photoluminescence image of a wafer with a dry back-etch of 800 nm outside the patterned regions passivated by a 10-nm-thick a-Si:H layer.

5.4.3 Homo-hetero solar cells with ion-implanted wafers

Homo-hetero devices were processed using ion-implanted wafers kindly supplied by the Georgia Institute of Technology (GT). The dopant profiles are shown in Chapter 3. Starting with a 10 Ωcm n-type wafer, five types of hole and electron collector profiles were implanted:

- Hole collector, 2000 Ω/sq
- Hole collector, 1050 Ω/sq
- Hole and electron collector, respectively 2000 Ω/sq and 220 Ω/sq
- Hole and electron collector, respectively 1050 Ω/sq and 180 Ω/sq
- Hole and electron collector, respectively 180 Ω/sq and 65 Ω/sq

5.4.3.1 Passivation of ion-implanted wafers

First, to investigate the passivation quality, symmetric samples were fabricated with a-Si:H(i), a-Si:H(i/n) or a-Si:H(i/p) passivating layers (inset of Figure 5.17(b)). The passivation quality is assessed from photoconductance decay measurement by monitoring the implied-*FF* and implied-V_{oc}. As presented in Chapter 2, the former gives an upper limit for the *FF* due to recombination losses but without any resistance losses (low injection level). The latter gives an upper limit for the V_{oc} (high injection level). The data are shown in Figure 5.17. Importantly, we observe that the same material yields effective passivation of p- and n-type surfaces. Interestingly, for the implied-*FF* (Figure 5.17(a)), we observe that for phosphorus-implanted surfaces, the a-Si:H(i/n) layers yield the highest passivation quality. Conversely, for boron-implanted surfaces, a-Si:H(i/p) layers do. The difference between the passivation capabilities of the a-Si:H(i/n) and a-Si:H(i/p) layers is increased for heavily doped surfaces. This points to the importance of field-effect passivation in these structures as well. The implied-V_{oc} does not show this difference in the passivation capability. At implied-V_{oc} conditions, bulk Auger recombination is the dominating recombination mechanism and, possibly, masks this low-injection effect.

5.4.3.2 Solar cell results: Ion implantation a-Si:H(i) thickness series

Surface passivation may result from two mechanisms: reduction of interface states density (chemical passivation) and asymmetry in the carrier concentration (field-effect passivation). Compared to SHJ solar cells, the homo-hetero devices have a doping gradient near their surface, resulting in enhanced field-effect passivation. For this reason, the defect density at the doped homo-hetero interface might be higher than in the SHJ, while maintaining a similar surface recombination velocity. Therefore, thinner a-Si:H layers, leading to higher surface states density, could be used in homo-hetero structures. At the front side, thinning the a-Si:H layers will decrease the losses due to parasitic absorption and thus increase the J_{sc}. The parasitic absorption in a-Si:H was determined to be about 0.1 mA/cm^2 per nm of a-Si:H [Holman 2012]. Moreover, decreasing the a-Si:H(i) layer thickness could decrease the R_s losses due to transport through the

layers according to [Sihua 2013, Taguchi 2008], resulting in increased *FF*. However, increased *FF* was not observed in [Holman 2012].

To investigate these potential gains, homo-hetero devices with various a-Si:H layer thicknesses were processed. The results are presented below.

Prior to PECVD, the wafers were cleaned in a piranha solution and etched for 45 s in a diluted HF solution. The hole collector was limited to the cell area by etching back outside the cell area after PECVD passivation and using a liquid plastic to protect the silver contacts (see previous section).

By co-processing a SHJ on 10 Ωcm GT and 2 Ωcm IMT wafers, we observe the former to yield lower efficiencies due to lower V_{oc}s (ΔV_{oc} > 20 mV) and *FF*s (ΔFF > 3%), as shown in Figure 5.18(a)–(d). This highlights the material quality limitations of the GT wafers (see also Chapter 2). We focus now on the *FF* losses. According to the Green formula [Green 1983a], a 20 mV drop would decrease the *FF* by less than 0.4%, assuming an ideality factor of 1.2. This effect is likely not the major effect explaining lower *FF* for the SHJ cells processed on GT wafers. The difference in the wafer base resistivity might at least partially explain this difference, as a 2 Ωcm wafer leads to a resistance of $4.8 \cdot 10^{-3}$ Ωcm^2 and a 10 Ωcm wafer to $2.4 \cdot 10^{-2}$ Ωcm^2, resulting in a *FF* loss of 0.2% abs, when considering only transverse transport which is a restrictive case. For the homo-hetero devices, the SHJ reference using a GT wafer should then be considered as comparison point.

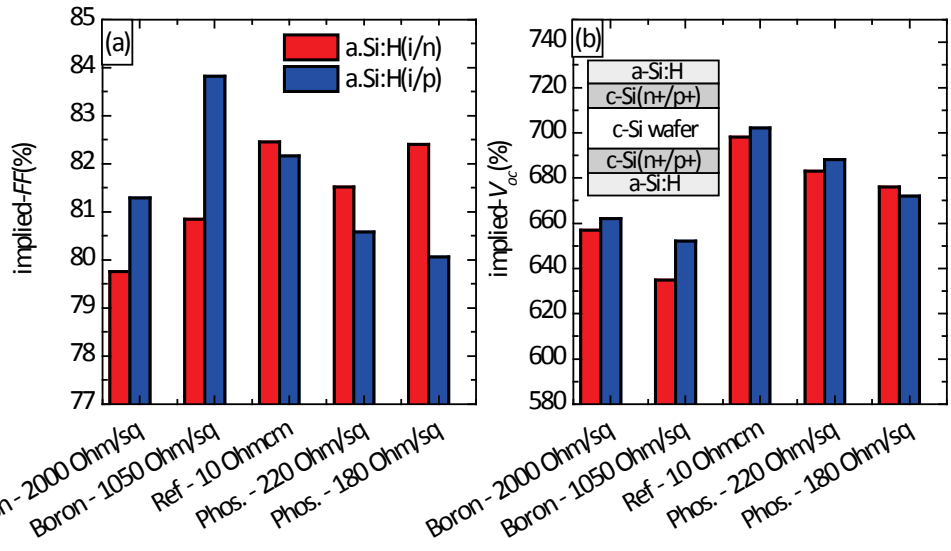


Figure 5.17: (a) Implied-*FF* and (b) implied-V_{OC} of symmetric lifetime samples passivated by either a-Si:H(i/n) or a-Si:H(i/p) layers.

We now discuss homo-hetero solar cells results for an increasing a-Si:H(i) thickness series based on Figure 5.18(e)–(l). The data are an average of three 2×2 cm^2 cells. The graphs of Figure 5.18(e)–(h) give cell parameters for lightly-doped implanted devices and Figure 5.18(i)–(l) for

heavily-doped implanted devices. First, we observe that for lightly-doped implanted devices, the V_{oc} values are higher than for heavily-doped ones, as expected from the J_0 data (section 5.3). Second, for increasing a-Si:H(i) layer thickness for the reference and lightly-doped implanted solar cells, the V_{oc} and *FF* increases. Conversely, these parameters hardly evolve for the heavily-doped implanted solar cells. This is in agreement with the fact that, for such samples, field-effect passivation plays an important role, diminishing the role of chemical passivation. Interestingly, we note that a-Si:H passivation layers deposited in a contaminated PECVD chamber lead to severe passivation losses on undoped wafers but hardly any losses on heavily-doped wafers (data not shown).

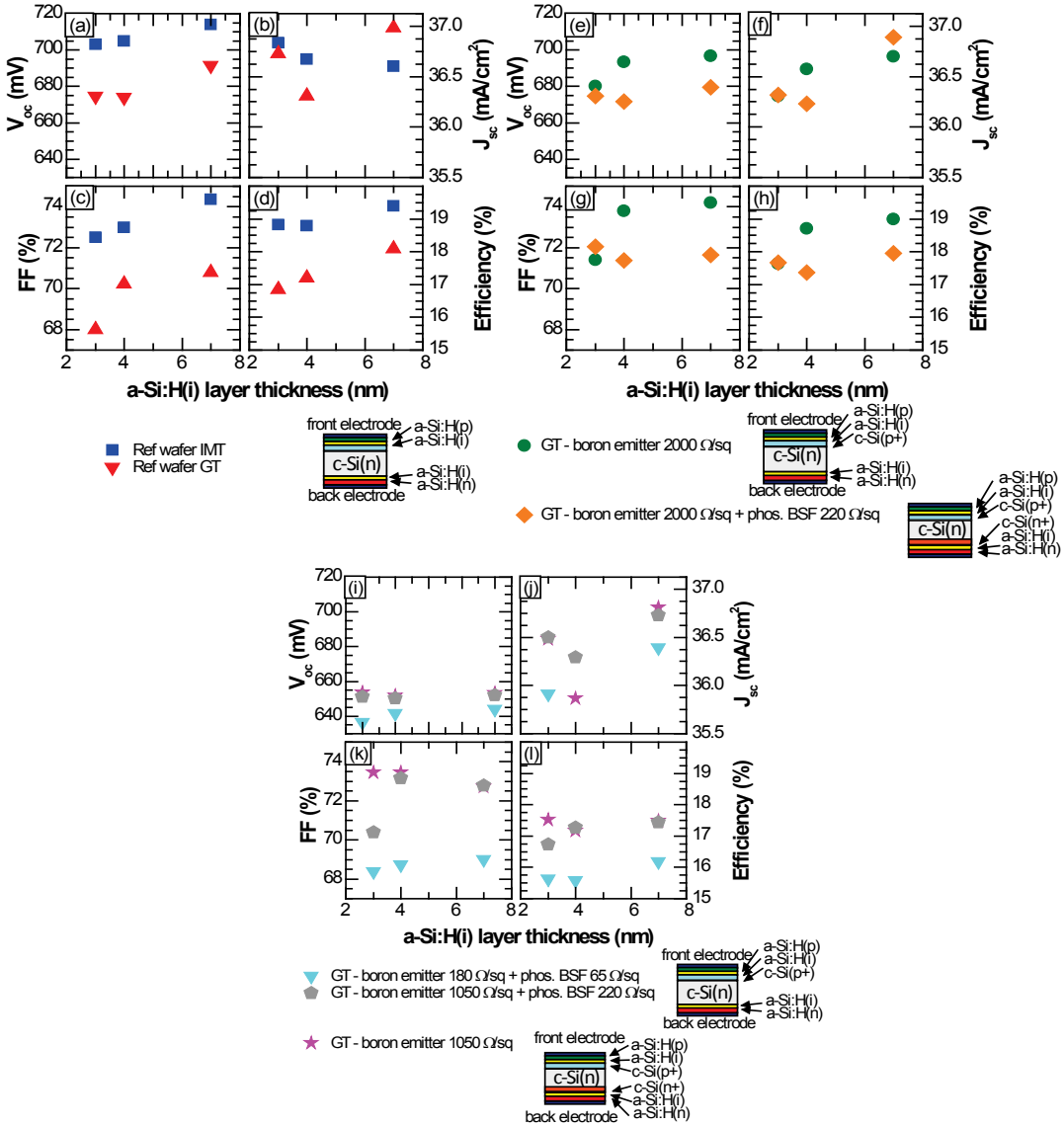


Figure 5.18: *JV* parameters of (a)–(d) SHJ solar cells on c-Si(n) wafers from IMT and Georgia Institute of Technology (GT), (e)–(h) homo-hetero solar cells on GT wafers with lightly ion-implanted surfaces and (i)–(l) homo-hetero solar cells on GT wafers with heavily ion-implanted surfaces with various a-Si:H(i) layer thicknesses.

Concerning the J_{sc}, we observe the expected current increase with decreasing the a-Si:H thickness only in our data for the IMT reference SHJ. This might be explained by the inhomogeneities in the GT wafers, observed by photoluminescence imaging, which could screen this effect.

As observed in [Holman 2012], we do not observe an increase in *FF* with decreasing a-Si:H layer thickness. We rather observe a decrease in *FF* with decreasing a-Si:H(i) layer thickness, which might be explained by pseudo-*FF* losses counterbalancing the gain in transport.

From these results, we conclude that in homo-hetero devices with heavily-doped regions, a thinner a-Si:H(i) layer can then be used without negatively affecting the V_{oc}.

5.4.3.3 Solar cell results: Ion implantation a-Si:H(p) thickness series

As in homo-hetero devices, the homojunction already defines the selectivity of the contact. The doped amorphous layer, especially the a-Si:H(p) layer, could have different requirements for such devices than for a standard SHJ and might be even removed. Figure 5.19 shows *JV* curves of a SHJ solar cell and a homo-hetero device without an a-Si:H(p) layer. We observe, in both cases, an extremely low V_{oc}, as already pointed out in section 4.4 for SHJ solar cells. This highlights the role of the a-Si:H(p) layer for contact resistivity issues [Kanicki 1988]. Thus, the c-Si(p+) emitter does not prevent the formation of the inverse diode-like feature occurring at the c-Si/a-Si:H(i)/TCO contact. We nevertheless observe a difference in the V_{oc} value depending on the doping of the c-Si surface emitter, validating the need to consider the c-Si/a-Si:H/TCO contact as whole and not separating these contacts.

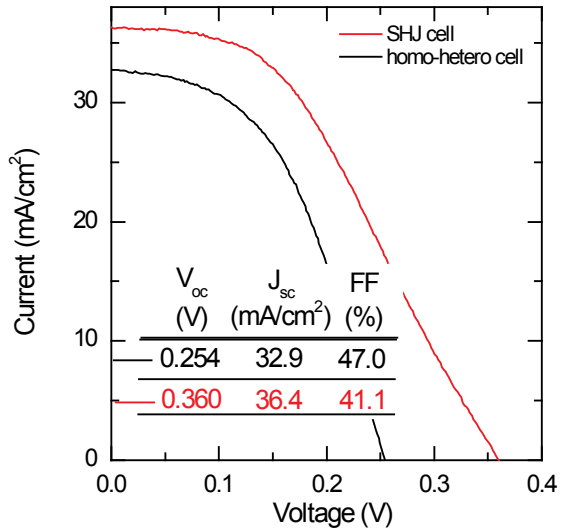


Figure 5.19: SHJ and homo-hetero device without an a-Si:H(p) layer at the front side between the a-Si:H and TCO.

A 2-nm-thick a-Si:H(p) layer prevents the formation of this detrimental diode, as shown in Figure 5.20. Nevertheless, for this thin layer, the *FF* values are systematically lower than for a thicker a-Si:H(p) layer (Figure 5.20(c)). Conversely, as expected, the J_{sc} values are higher for the thin a-Si:H-based devices due to lower parasitic absorbance [Holman 2012].

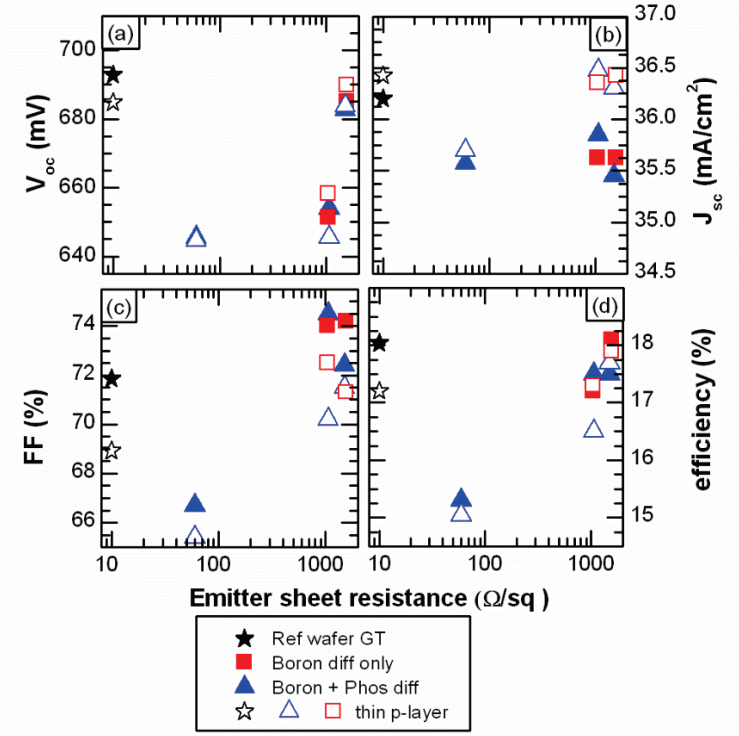


Figure 5.20: 2-nm-thick (thin, full symbol) and 5-nm-thick (thick, empty symbol) a-Si:H(p) for SHJ and homo-hetero devices.

5.4.3.4 Homo-hetero solar cell properties: *FF* analysis

In this section, to investigate the properties of the homo-hetero cells, we focus on the behavior of the homo-hetero cells under illumination and temperature by monitoring the *JV* characteristics. We then analyze the *FF* of the cells using the method described in section 4.5.

Figure 5.21 plots the temperature dependence of the *JV* parameters for three selected homo-hetero structures featuring various homojunctions and a reference SHJ cell. We observe a difference in the relative temperature coefficient (T_{coeff}) between the SHJ reference and the heavily implanted homo-hetero cell (blue data points), namely -0.23 %/°C for the former and -0.26 %/°C for the latter. Nevertheless, the T_{coeff} of the homo-hetero solar cells is much lower than that of a homojunction solar cell (typically -0.4 %/°C). Two effects are known to dictate the T_{coeff}: passivation and transport barriers. Here, a barrier effect, decreasing the T_{coeff}, must be compensating for the increase of the T_{coeff} due to the lower passivation quality.

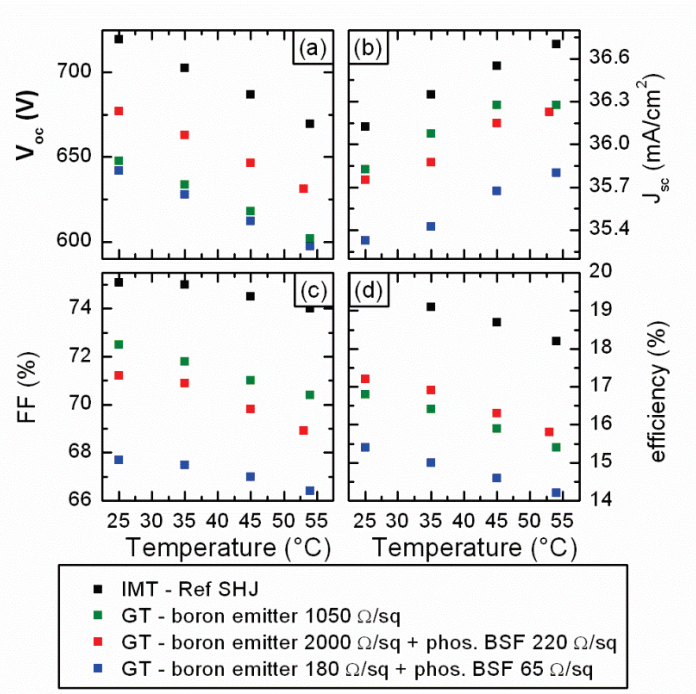


Figure 5.21: Temperature dependence of the *JV* parameters.

For the same devices, we measured the illumination dependence (Figure 5.22) and compared them with a homojunction cell. For all devices, we observe a decrease in V_{oc} while lowering the illumination for all structures (Figure 5.22(a)), as expected from the one-diode equation. However, the *FF* of the homo-hetero and the homojunction devices decreases with decreasing illumination, unlike the *FF* of the SHJ solar cell (Figure 5.22(b)). Typically, the gradual increase in *FF* with decreasing illumination points to series resistance dominating the cell behavior. Conversely, the homojunction behavior is usually explained by the dependence of the *FF* on the V_{oc} and possibly by low shunt resistance.

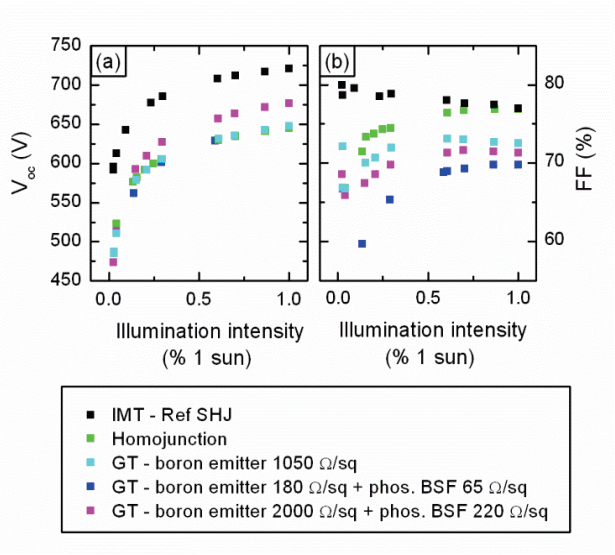


Figure 5.22: Illumination dependence on the (a) V_{OC} and (b) *FF*.

Eventually, a FF analysis on the cells in Figure 5.21 and Figure 5.22 is plotted in Figure 5.23, following the work presented in section 2.4, section 4.5, and [Khanna 2013, Pysch 2007]. Importantly, we confirm that a reduced R_s value is obtained for the homo-hetero devices compared to SHJ solar cells (section 5.3). However, higher losses linked to the recombination current of a non-ideal diode and recombination in the space-charge region are observed for homo-hetero devices compared to diffusion-free devices. These two effects mostly balance each other with the GT wafers. We observe moreover, as expected, negligible resistance losses associated with shunt resistance for all devices. Now comparing these losses compared to losses in homo-junction solar cells, we observe that $J_{0,\neq 1}$ diode losses are unexpectedly higher. This might be due to design losses in our cells due to un-passivated edges.

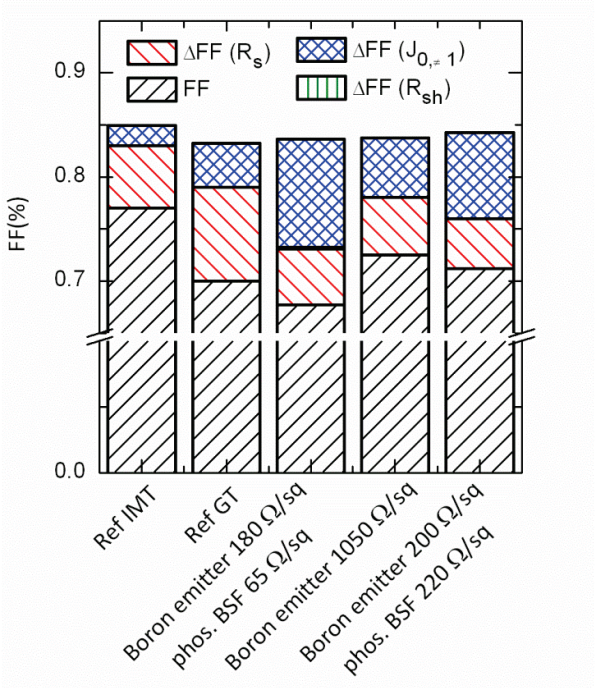
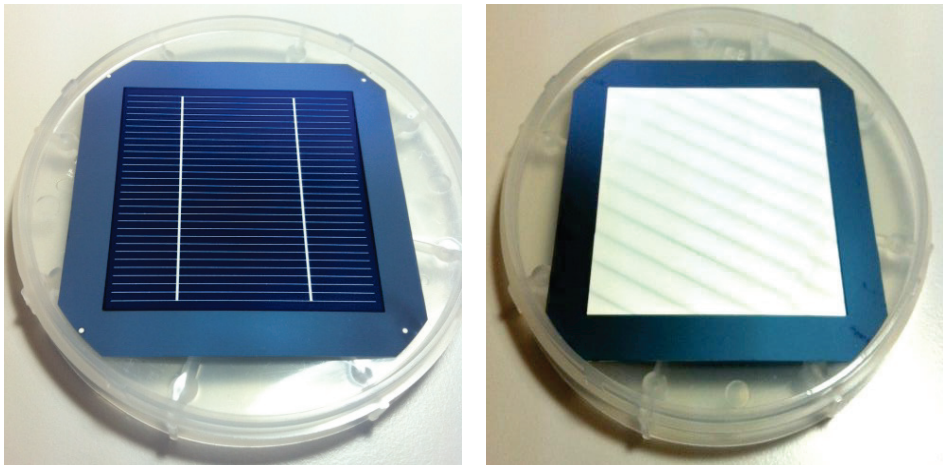


Figure 5.23 *FF* analysis of homo-hetero solar cells compared to reference SHJ solar cells.

With the optimized layer thickness, a 18.9% homo-hetero structure could be achieved with a V_{oc} of 696 mV, a *FF* of 74.3% and a J_{sc} of 36.6 mA/cm^2.

5.4.4 Improvement of the homo-hetero solar cell design

As seen in section 5.4.2, the new cell design does not passivate the edges around the cell. This could result in a relative efficiency loss of 3–4% on a 4 cm^2 cell [Aberle 1995]. Scaling up the size of the cell decreases these relative losses as the perimeter increases linearly with size whereas the area increases quadratically. Therefore, a new cell design was developed: a 6×6 cm^2 cell on a pseudo square wafer.



(a) (b)

Figure 5.24 Photograph of the (a) front and (b) back of a baseline 6×6 cm^2 SHJ cell.

To optimize the metallization to balance shadowing and series resistance losses, a design with two bus bars and 30 fingers was developed. To be as close as possible to the case in which the cells are inter-connected by ribbons and in which no losses occur in the bus bar, the bus bars were optimized for contact stripes, also known as pogo-pins, measurements. The photogenerated current is thus collected by the pins which are separated by 11.5 mm to limit the influence of the voltage drop across the bus bar [Hohl-Ebinger 2008]. In the middle, the central voltage probe is 3 mm away from the two first current probes due to practical limitations. As for 2×2cm^2 cells, a four-wire measurement is performed using a dual-lamp Wacom solar simulator (xenon and halogen lamps). As the contact stripes shade the cell area close to the bus bar, the *JV* measurement is taken in two steps: (1) the current is measured using Kelvin probes (no shadowing) (2) the pogo-pins setup is then used and the *JV* lamp intensity of the xenon lamp is adjusted to obtain the same current as with the unshaded cell. Even though this measurement is more time consuming than a single-step measurement using Kelvin probes as in the case of 2×2 cm^2 cells, a design using three bus bars would be needed for Kelvin probe measurement on a 6×6 cm^2 resulting in a supplementary 2.4% shadow loss (over 0.5% abs. in efficiency). With this narrow bus bar design, a *FF* loss of 2% is typically observed if the pogo-pins setup is not used. Thus, it should be systematically used for this design.

The following section uses this new 6×6 cm^2 cell design.

5.4.5 Passivating contacts solar cells with diffused wafers

Imec kindly provided diffused wafers used to fabricate homojunction solar cells:

- 1-3 Ωcm p-type wafers with a $POCl_3$ diffusion with a sheet resistance of 86 Ω/sq (approximately 10^{19} cm^{-3} surface concentration and depth of ~0.5 µm ([Tous 2013]).
- 4-5 Ωcm n-type wafers with a BBr_3 diffusion with a sheet resistance of 91 Ω/sq (profile not disclosed).

First, the recombination current pre-factor was measured on symmetrically diffused wafers with a passivating thermal oxide after a forming gas anneal at imec. The wafers were then send to EPFL, where the oxide was stripped in a diluted HF solution and the surface was passivated using a-Si:H layers. Results of the recombination current pre-factor are given in Table 5:1.

Table 5:1 Recombination current pre-factor (J_0) of symmetric samples.

Wafer type	Diffusion type	J_0 (fA/cm^2)		
		SiO_x (FGA)	a-Si:H(i/n)	a-Si:H(i/p)
n	BBr_3	182		62
p	BBr_3	154		30
n	$POCl_3$	121	143	
p	$POCl_3$	191	99	

Single-side diffused wafers were obtained by a single-side back-etching of 1 µm (imec). Homo-hetero solar cells were then processed using the latest 6×6 cm^2 design and dry-etching patterning. The results are presented in Table 5:2.

Table 5:2 Efficiency of homo-hetero solar cells based on standard homojunction diffusion (6×6 cm^2 cells).

	V_{OC} (mV)	J_{SC} (mA/cm^2)	*FF* (%)	Efficiency (%)
Homo-hetero cells (6×6 cm^2 cells)				
n-type wafer BBr_3 diffusion, front emitter	0.687	37.24	75.84	19.4
p-type wafer, $POCl_3$ diffusion, rear emitter	0.679	37.00	75.1	18.87
Homojunction cells (156×156 mm^2**)**				
n-PERT, n-type wafer, BBr_3 diffusion ([Tous 2014])	0.676	38.4	79.2	20.5
p-PERL, p-type wafer, $POCl_3$ diffusion ([Tous 2014])	0.661	39	80	20.6
Heterojunction cells (6×6 cm^2 cells)				
n-type wafer, Imec reference, front emitter	0.702	36.19	69.3	17.60
p-type wafer, Imec reference, rear emitter	0.703	38.44	75.73	20.47
n-type wafer, IMT reference, front emitter	0.722	38.76	77.38	21.64

We observe that, compared to homojunction solar cells, the homo-hetero devices yield higher V_{oc}s but lower *FF*, resulting respectively from lower recombination losses at contacts and higher series resistance losses. The J_{sc} of the homo-hetero solar cells is slightly lower, as well. However, this should be overcome as test structures were used with no patterning at the front side and no double anti-reflective coating nor copper plating [Geissbühler 2014] to optimize the current[12].

Improving the V_{oc} from 661 (676) to 679 mV (687 mV) while maintaining equivalent J_{sc} and *FF* would increase the efficiency by 0.6% (0.4%) absolute. In addition, the homo-hetero devices yield a temperature coefficient of -0.27%, very similar to the one of a conventional heterojunction solar cell, as discussed in section 5.4.3.4. This difference in temperature coefficient between the two cell's architectures results in the homo-hetero solar cell outperforming the conventional homojunction solar cell for temperature above 60 °C, as shown in Figure 5.25. This occurs despite the initial difference in efficiency of over 1% abs. at 25 °C (homojunction solar cell: 20.5% and homo-hetero solar cell: 19.4%). This is of major importance as a photovoltaic module operated in the field may operate at temperatures up to 90°C [Alonso García 2004, Kurtz 2011].

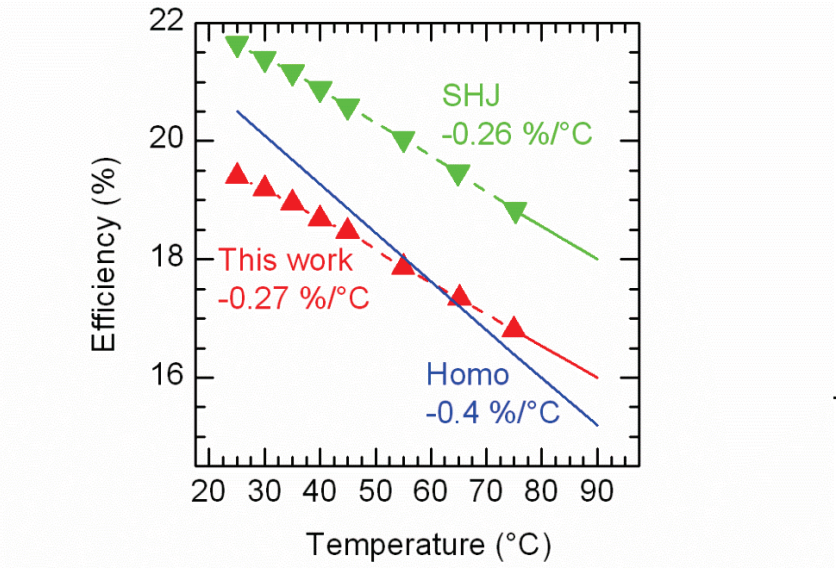


Figure 5.25: Temperature dependence of the efficiency of a homo-hetero, homojunction and heterojunction solar cell. Symbols indicate measured data points and line extrapolated values.

[12] Two different measurement setups were used, implying possible discrepancies between the setups.

5.5 Conclusions

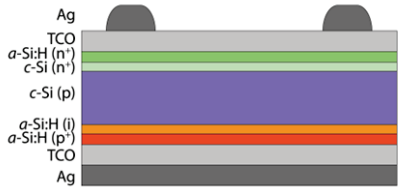
Homojunction solar cells featuring passivating contacts were demonstrated on crystalline silicon wafers with emitters formed by (1) epitaxial films grown by low-temperature plasma-enhanced chemical vapor deposition (PECVD), (2) ion implantation and (3) diffusion. Here, we highlight the main findings of this chapter:

- Thin a-Si:H layers efficiently passivate both n- and p-type surfaces for doping concentration ranging from 10^{15} to 10^{20} cm^{-3}.
- The homo-hetero structures featuring epitaxially grown emitters on polished surfaces are limited by the short deposition time needed for the a-Si:H layers.
- In homo-hetero devices, the a-Si:H(i) layer may be first thinned for highly doped surfaces while maintaining similar surface passivation due to the enhanced field-effect passivation. Second, even though the selectivity of the contact arises from the homojunction, the optimal a-Si:H(p) layer thickness coincides with that of a heterojunction solar cell, due to contact properties with the TCO. A detailed analysis of the devices confirmed high voltages over the full injection range for these passivating contact devices, resulting in high V_{oc}s. Reduced series resistance compared to a SHJ solar cell was also demonstrated for the homo-hetero devices.
- Compared to high-efficiency homojunction devices processed on an optimized diffusion profile, our passivating contact devices, for similar diffusion profiles, show an increase in V_{oc}, corresponding to a gain of 0.4–0.6% in absolute efficiency. However, the *FF* is significantly lower for these devices compared to a homojunction solar cell due to series resistance losses stemming from the hetero-contact. Engineering of this contact should overcome this resistance, as discussed in Chapter 4.
- The homo-hetero solar cells with diffused emitters may outperform state-of-the-art homojunction solar cells with similar diffused emitters at high temperatures (<60 °C).

The main homo-hetero devices architecture processed in this thesis and their corresponding record efficiency are summarized in Figure 5.26.

Homo-hetero solar cells

Front phosphorus **epitaxial** homojunction (15 nm at 10^{19} cm^{-3})

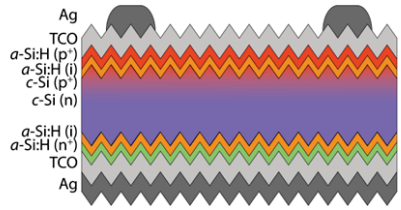


Eff.: 15.2%

V_{OC} (mV)	J_{SC} (mA/cm²)	*FF* (%)
633	31.5	75.7

wafer: p-type, FZ, 2 Ωcm, 300 µm, polished
cell size: 2×2 cm^2
layer thickness: a-Si:H(i/p+) : ~ 25 nm
a-Si:H(n+) : ~ 5 nm

Front boron **ion implanted** homojunction (2000 Ω/sq)

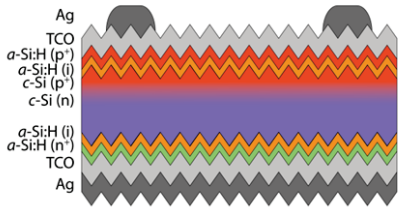


Eff.: 18.9%

V_{OC} (mV)	J_{SC} (mA/cm²)	*FF* (%)
696	36.6	74.3

wafer: n-type, CZ, 5 Ωcm, 180 µm, textured
cell size: 2×2 cm^2,
layer thickness: ~ 18 nm a-Si:H(i/p+)
~ 16 nm a-Si:H(i/n+)
partners: GeorgiaTech

Front boron **diffused** homojunction (91 Ω/sq)

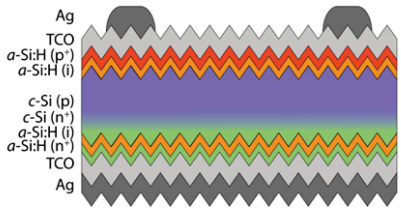


Eff.: 19.4%

V_{OC} (mV)	J_{SC} (mA/cm²)	*FF* (%)
687	37.2	75.8

wafer: n-type, CZ, 4 Ωcm, 170 µm, textured
cell size: 6×6 cm^2
layer thickness: : ~18nm a-Si:H(i/p+)
~22 nm a-Si:H(i/n+)
partners: imec

Rear phosphorus **diffused** homojunction (86 Ω/sq)

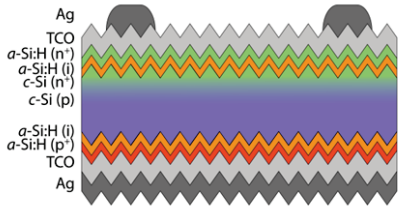


Eff.: 18.9%

V_{OC} (mV)	J_{SC} (mA/cm²)	*FF* (%)
679	37.0	75.1

wafer: p-type, CZ, 2 Ωcm, 180 µm, textured
cell size: 6×6 cm^2
layer thickness: ~18 nm a-Si:H(i/p+)
~22 nm a-Si:H(i/n+)
partners: imec

Front phosphorus **diffused** homojunction (86 Ω/sq)



Eff.: 18.6%

V_{OC} (mV)	J_{SC} (mA/cm²)	*FF* (%)
681	37.7	74.5

wafer: p-type, CZ, 2 Ωcm, 180 µm, textured
cell size: 6×6 cm^2
layer thickness: : ~20 nm a-Si:H(i/p+)
~18 nm a-Si:H(i/n+)
partners: imec

Figure 5.26: Main results for homo-hetero devices achieved in this thesis. CZ stands for Czochralski wafers and FZ for float-zone wafers.

To conclude, this chapter successfully demonstrated that passivating contacts improve the open-circuit voltage of homojunction solar cells and increase their performance when operated at typical cell temperature in the field (> 25 °C).

Chapter 6 Conclusions and perspectives

6.1 Summary

For standard silicon homojunction solar cells, the trade-off between contacting and surface passivation is perhaps the most important factor limiting further progress in energy-conversion efficiency improvements. Fundamentally, it arises because of the recombinative nature of the metal-semiconductor interface of the contacts used so far. In this thesis we investigated a novel carrier-selective passivating contact to resolve this long-standing problem. Our contact is inspired by silicon heterojunction (SHJ) technology, and essentially inserts a layer stack consisting of hydrogenated amorphous silicon (a-Si:H) layers and a transparent conductive oxide (TCO) between the wafer surface and the metal contact. The a-Si:H films passivate the crystalline silicon (c-Si) surface and increase the carrier selectivity of the contact by film doping. The TCO increases the design freedom in electrical interface engineering. The homo-hetero structure of a solar cell featuring such passivating contacts is sketched in Figure 5.21.

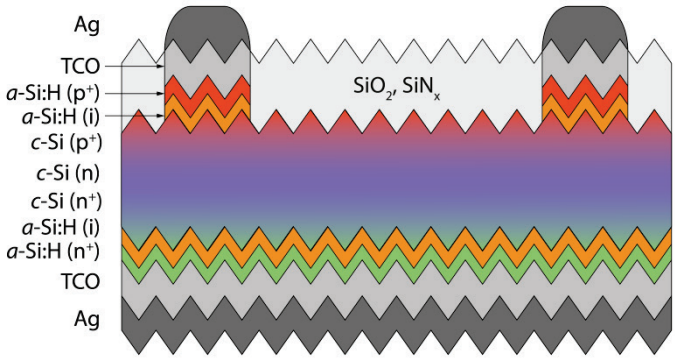


Figure 6.1: Homo-hetero device ultimate design.

When applied in a patterned design, as shown in Fig. 6.1, this hybrid technology can uniquely combine the advantages of silicon heterojunction solar cells (low recombination losses thanks to passivating contacts, which enable high voltages at open-circuit V_{oc} and maximum-power-point conditions) and of homojunction solar cells (high short-circuit current (J_{sc}) thanks to low optical losses, high fill factor (*FF*) thanks to low contact resistivity, and possible processing-induced wafer improvements by impurity gettering during homojunction formation).

With such an objective in mind, we investigated three ways of forming a c-Si doping gradient, representing the homojunction: by thermal diffusion, by ion implantation and by silicon homo-epitaxial growth (Chapter 3). For the first method, as diffusion occurs on both sides of the wafer, we developed a plasma-etching process to have single-side diffused wafers. We find that stringent wafer cleaning is required after the plasma etching to remove Si particles and impurities. Second, as ion implantation directly produces single-side junctions, the process of the homo-hetero device is facilitated. Third, to simplify the process flow of the homo-hetero passivating contacts and amount of required device processing equipment, we demonstrated the fabrication of phosphorus-doped homo-epitaxial films by using the same deposition technique as for SHJ contacts, i.e. low-temperature (≤ 180 °C) plasma enhanced chemical vapor deposition (PECVD). A systematic analysis of the growth, microstructure and electronic properties of such epitaxial films was presented. The deposition conditions providing the highest epitaxial quality for homo-hetero devices were determined. This study also highlighted the importance of controlling the unintentional presence of an interface layer between the c-Si substrate and the epitaxial film, impacting the electronic properties of the deposited material.

We then investigated specific properties of SHJ solar cells, specially aimed at developing and optimizing the hetero-contacts for our specific application (Chapter 4). As pioneered by Panasonic, these contacts consist of the following structure, starting from the wafer side: c-Si(n)/a-Si:H(i)/a-Si:H(n or p)/TCO/Ag, to form either the electron or hole contact. We studied the contact formation and observed a sharp degradation of the passivation quality after TCO sputtering. We showed that this damage is partially caused by the plasma luminescence during sputtering, which is an unexpected result. The electronic quality of the a-Si:H layers is recovered by low-temperature annealing. However, the microscopic structure of these films is permanently changed, as observed from precise infrared absorbance spectroscopy. To examine whether a fully damage-free transparent electrode deposition process can yield devices with higher efficiency, we explored atomic-layer-deposited TCOs. Such TCOs were inserted into the contact as buffer layers to mitigate the sputter damage. We found that atomic layer deposition (ALD) does not degrade the passivating layers and a thin ALD layer efficiently protects against sputtering damage. However, for a-Si:H layers optimized for sputtering, this protective layer does not necessarily yield higher internal voltages in the device, once the full layer stack is annealed. For SHJ solar cells with ALD protective layers, we report two additional notable observations. First, using temperature-dependent *JV* measurement and transmission electron microscopy, we identified the persistent presence of a thin silicon oxide layer between the a-Si:H layers and the TCO. We found that this layer acts as an undesired transport barrier, impeding efficient collection of the holes and electrons, resulting in increased series resistance losses. Second, we showed that a-Si:H thin layers do not recover from sputter damage, indicating that soft deposition techniques might be necessary for devices with thinner a-Si:H layers. Moreover, using ALD TCO layers, we confirmed that the recombination statistics at the c-Si/a-Si:H(i/p) interface are negatively affected by the mere presence of the TCO (independent of the precise deposition technique): The

presence of the TCO can alter the surface potential in such a way that it yields increased recombination losses in the low injection range. This range is important for the voltage at maximum power point, and these recombination losses can be anticipated to result in a 2-3% *FF* decrease. Conversely, at the c-Si/a-Si:H(i/n) interface, the recombination statistics are not affected, or are even slightly improved (depending on the TCO work function). To evaluate whether the TCO work function is pinned at the a-Si:H/TCO interface, we investigated MIS-like test structures. This revealed that the TCO work function varies at the interface, indicating that the TCO work function offers a degree of freedom in optimizing the contact. Eventually, we focused on contact resistivity. We showed that transfer length measurements could be used to characterize electron (but not hole collectors) on n-type wafers. To access the contact resistivity of the hole contact, either vertical structures or direct characterization of the solar cell's performance is needed. For the latter, a *FF* analysis method was described to discriminate between recombination and resistance losses. This method can be used for all other possible design of passivating contacts for c-Si–based solar cells.

Eventually, we combined a homojunction with the silicon heterojunction contact to form a homo-hetero device with passivating contacts (Chapter 5). We first showed that a-Si:H layers give state-of-the-art passivation for n-type surfaces as well as very high passivation for p-type surfaces, yielding thus fully symmetric passivation. Interestingly, the contact resistivity of highly phosphorus-doped n-type surfaces was shown to be lower than for lightly doped surfaces. We then implemented homo-hetero contacts in test devices to make a proof-of-concept. These test devices were passivated over the full front area. We evaluated three types of devices: homo-epitaxial, ion-implanted and diffused emitters in homo-hetero devices. The first generation device design had carriers leaking outside the device area using the highly doped region as a conductive channel, which severely impacted device performance. We showed that such losses are efficiently investigated by laser-beam-induced-current measurements. An optimized design using dry etching patterning was then developed. Using ion-implanted homo-hetero devices, we pointed out that the a-Si:H(i) layer could be thinner when highly doped c-Si surfaces were used, indicating that field-effect passivation is effective in such devices. Despite the homojunction and thus the separation of the carriers before the a-Si:H layers, the a-Si:H(p) doped layer is nevertheless needed for its contacting properties. When removed, the external voltage drops to 250–400 mV. A 2-nm-thick a-Si:H(p) mostly prevents this V_{oc} drop. Eventually, homo-hetero devices were processed with an optimized diffused emitter as also used in high-efficiency c-Si homojunction solar cells. We showed that, compared to conventional homojunction solar cells with the same emitter, the V_{oc} increased by 10 to 20 mV. The *FF* in the homo-hetero devices is dominated by resistive losses and non-ideal-diode recombination. Based on the results of Panasonic [Panasonic 2014, Taguchi 2014], we can infer that engineering this contact should overcome this limitation. Importantly, we show an excellent relative temperature coefficient for these devices (-0.27 %/°C) which results in the homo-hetero solar cell outperforming the homojunction solar cell at temperatures above 60 °C.

6.2 Perspectives

The novel passivating contacts presented in this thesis efficiently reduce the recombination losses of silicon homojunction solar cells, leading to higher voltages in the device throughout the full carrier injection range. This leads to higher open-circuit voltages and also affects positively the fill factor of solar cells. However, this gain is at present still overcome by resistive losses. These can likely be reduced by contact engineering, however. Furthermore, the low temperature coefficient provides a competitive advantage for these structures, greatly reducing the levelized cost of energy for these homo-hetero solar cells.

The major issue to be investigated for these contacts to become mainstream technology remains their complexity; the need to deposit multiple layers by several deposition techniques and patterning adversely weight against their implementation in homojunction production lines, so far. Indeed, these passivating contacts require, in addition to the conventional c-Si equipment, PECVD and sputtering tools. To reduce the cost and complexity of these passivating contacts, the TCO layer could be removed as neither lateral transport nor optical constraints are required. In our structures, removing the TCO layer induces high *FF* losses but optimizing the metal, including its work function, might prevent these losses. This would eliminate the need for an extra processing step and corresponding deposition tool. The device structure could then be similar to the contacts developed with Bullock *et al.* in which aluminum is used as the contacting metal and an a-Si:H/aluminum alloy forms [Bullock 2014b, Bullock 2014c]. Moreover, Zhang *et al*. evidenced that sputtering could be used for a-Si:H passivation layer deposition [Zhang 2014]. This might also promote these silicon homo-hetero contacts, as sputtering is usually a cheaper deposition technique than PECVD. Additionally, the ultimate device structure requires patterning methods to locally form the SHJ contacts while using transparent layers such as dielectrics between the contacts. However, low-cost patterning techniques, such as inkjet printing and plasma etching, are being investigated and could provide attractive processing solutions in the not-too distant future.

To conclude, conventional c-Si solar cells need to decrease recombination losses at their contacts. Passivating contacts will become a key path to overcome this limitation. Research must find the most suitable materials and structure to form a carrier-selective contact with an optimal band alignment to have low contact resistivity and a high carrier selectivity to avoid recombination losses. Moreover, to avoid patterning complexity, lateral transport capabilities and a wide bandgap material are needed as well. If such a solution is found, it could lead to a breakthrough of photovoltaics as mainstream technology for energy production.

Appendix A

The first months of this thesis were dedicated to the setting up of a thermal desorption system (TDS) from Hiden Analytical (Figure A.1) for state-of-the-art research in thin-film solar cells and analysis of various materials.

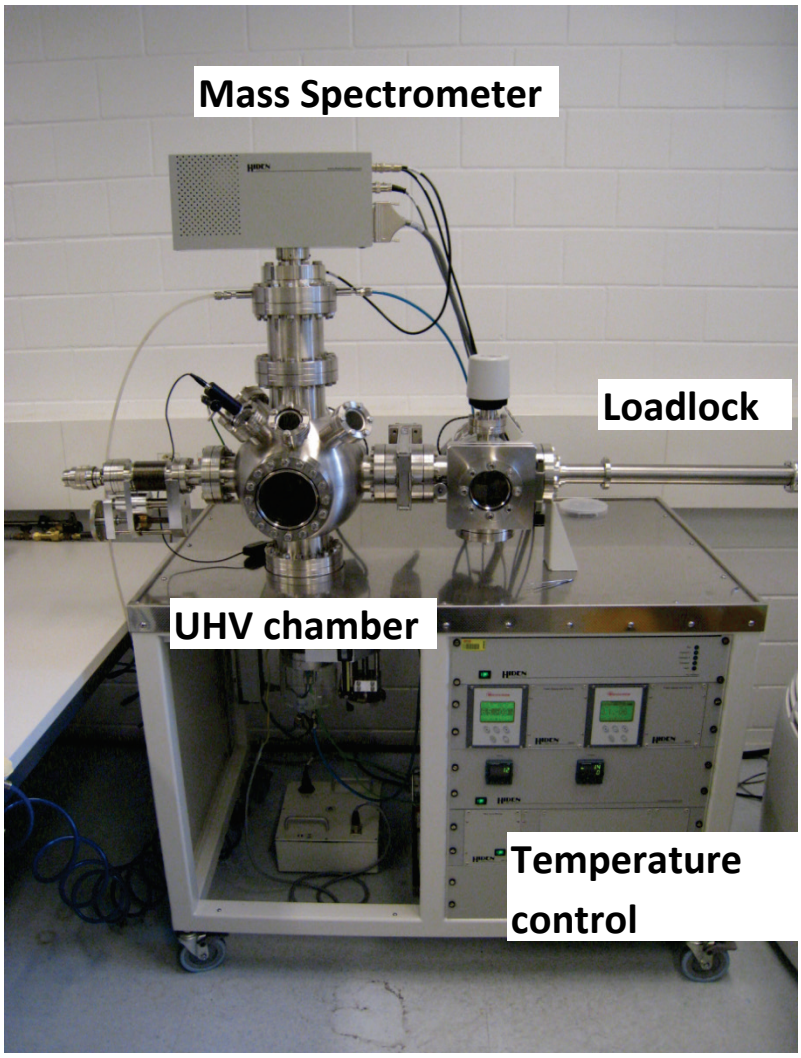


Figure A.1: Thermal desorption system.

More specifically, TDS would be used to investigate the silicon-hydrogen bonding environment in intrinsic and doped amorphous silicon and microcrystalline silicon films ranging from a monolayer to several micrometers thick, to characterize the thermal desorption of relevant elements (mainly H, H_2, D, D_2, HD, H_2O,…) from films under linear temperature ramp heating, but also under isothermal heating, and to study time-resolved material changes of films under annealing.

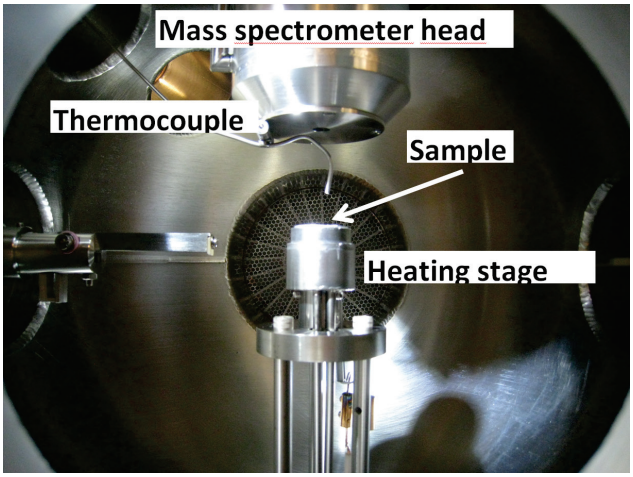


Figure A.2: Ultra-high vacuum chamber of the TDS setup.

However, the temperature control of the system was not accurate. This was due to heating of the sample by the underlying MoO_x stage and by a point contact thermocouple on the sample as shown in Figure A.2. This setup induced a temperature gradient in the sample, which broadened the effusion peaks, induced reproducibility issues and triggered the melting of the thermocouple. Moreover, a background signal, coming from wires of the heating stage, limited the sensitivity of the system. After several months of trials and new thermocouple designs, the system was returned to the manufacturer.

Appendix B

Lead iodide perovskites ($(CH_3NH_3)PbI_3$) are now attracting increasing attention of the photovolatics community [Green 2014b]. They have an especially well-suited bandgap and band offsets for field-effect passivation of crystalline silicon (c-Si), as illustrated in Figure B.1. Here, we investigate the use of lead iodide perovskites as a passivating layer on c-Si.

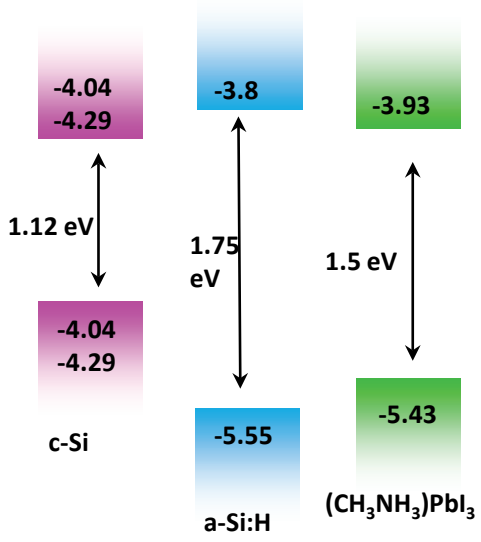


Figure B.1: Band energies for c-Si, hydrogenated amorphous silicon (a-Si:H) and $(CH_3NH_3)PbI_3$ [Kim 2012, Lide 2008].

To test this passivation, n-type and p-type 300-µm-thick c-Si wafers were first passivated on one side by a-Si:H to act as an ideal passivation layer. Secondly, the native oxide of the c-Si was removed in an hydrofluoric acid solution (5%, 30s). $(CH_3NH_3)PbI_3$ in dimethylformamide and gamma-Butyrolactone solvents were then directly spin-coated on the un-passivated side of the c-Si wafer. Jun-Ho Yum and Soo-Jin Moon (EPFL, Laboratory of Photonics and Interfaces) kindly provided the solutions. The samples were then either placed on a hot plate to dry to solvents between 80–100 °C or left in air to dry. The passivation quality of the perovskites was then investigated using photoluminescence imaging. A slightly higher PL signal was obtained on a p-type wafer passivated with perovskites, whereas a slight decrease was observed on an n-type wafer. This indicates that a field-effect passivation could be occurring (positive charging of the

perovskites). Nevertheless, as with using photoconductance measurements, the measured difference was within the measurement error, meaning the passivation effect of the perovskites is very weak. This is partially explained by the low coverage ratio of the perovskites on the wafer surface obtained using such solutions, as illustrated in Figure B.2

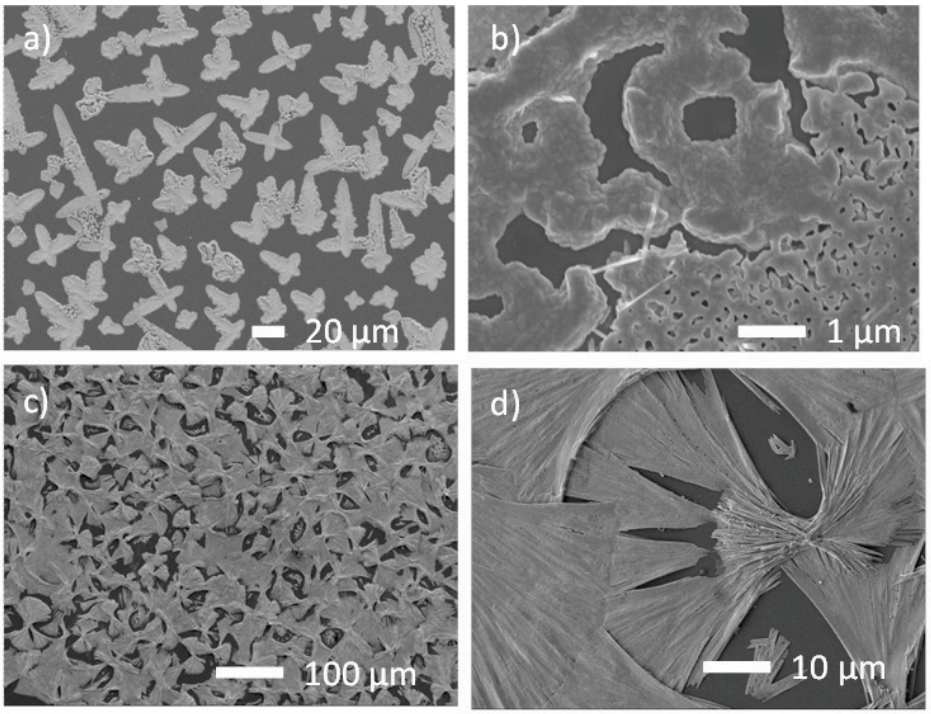


Figure B.2: Scanning electron microscope images of perovskite spin-coated on a c-Si wafer (2000 rpm with an acceleration of 500 rpm) dissolved in GBL dried on a hot plate at 80 °C with two different magnification ((a) and (b)) and in DMF dried in ambient air ((c) and (d)).

The most promising use of this material is as the top cell of a c-Si-based solar cell, as evidenced in a first analysis. A project was then developed to study more specifically the potential of such tandem cells [Löper 2014].

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Demaurex B., De Wolf S., Descoeudres A., Holman Z. C., Ballif C., Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering, Applied Physics Letters 101(17):171604, 2012.

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