Multi-Band Outphasing Power Amplifier Design for Mobile and Base stations

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To my parents…

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Abstract

New generations of wireless communication systems require linear efficient RF power amplifiers (PAs) for higher transmission data rates and longer battery life. On the contrary, conventional PAs are normally designed for peak efficiency under maximum output power (P_{out}). Thus, in power back-off, the overall efficiency degrades significantly and the average efficiency is much lower than the efficiency at maximum P_{out}. Chireix outphasing PA, also called LINC (Linear amplification using Non-linear Components), is one of the most promising techniques to improve the efficiency at power back-off. In this method, a variable envelope input signal is first decomposed into two constant-envelope phase-modulated signals and then amplified using two highly efficient non-linear PAs. The output signals are combined preferably in a loss-less power combiner to build the desired output signal. In this way, the PA exhibits high efficiency with good linearity.

In this thesis, first we analyze a complex model of outphasing combiner considering its nonidealities such as reflection and loss in transmission lines (TL). Then we propose a compact model with analytical formula that is validated through several comparative tests using ADS and Spectre RF. Furthermore, we analyze the effect of reactive load in Chireix combiner with stubs (a parallel inductor and capacitor), while distinguishing between its capacitive and inductive parts. It is demonstrated that only the capacitive part of the reactive load degrades the performances. Based on this, a new architecture (Z-LINC) is proposed where the power combiner is designed to provide a zero capacitive load to the PAs whatever the outphasing angle. The theory describing the operations of the system is developed and a 900 MHz classical LINC and Z-LINC PAs are designed and measured. In addition, a miniaturization technique is proposed which employs $\lambda/8$ or smaller TLs instead of conventional $\lambda/4$ TLs in outphasing power

combiner. This technique is applied to implement a 900 MHz PA using LDMOS power transistors.

Besides single-band PAs, dual-band PAs are more and more needed because of an increasing demand for wireless communication terminals to handle multi-band operation. In chapter 5, a new compact design approach for dual-band transmitters based on a reconfigurable outphasing combiner is proposed. The objective is to avoid the cumbersome implementations where several PAs and matching network are used in parallel. The technique is applied to design a dual band PA with a fully integrated power combiner in 90 nm CMOS technology. An inverter-based class D PA topology, particularly suitable for outphasing and multimode operations is presented. The TLs in the combiner, realized using a network of on-chip series inductors and parallel capacitors, are reconfigurable from $\lambda/4$ in 1800 MHz to $\lambda/8$ in 900 MHz. In order to maximize the efficiency, the on-chip inductors are implemented using high quality factor on-chip slab inductors. The measured maximum P_{out} at 900/1800 MHz are 24.3 and 22.7 dBm with maximum efficiencies of 51% and 34% respectively.

Keywords: Chireix, outphasing, LINC, power amplifier, power combiner, transmission line, slab inductor, dual band, LDMOS, CMOS, RF integrated circuits.

Résumé

Les nouvelles générations de systèmes de communication sans fils nécessitent des amplificateurs linéaires de puissance RF pour des vitesses de transmission de données plus rapides et des batteries ayant des durées de vie plus longues. Au contraire, les PAs conventionnels sont normalement conçus pour un rendement optimum à la puissance de sortie maximum. Ainsi, à la puissance reculer l'efficacité totale est significativement réduite et l'efficacité moyenne est bien plus basse que l'efficacité au maximum Pout. "Chireix outphasing PA" aussi appelé LINC (Linear amplification using Non-linear Components) est une des techniques les plus prometteuses pour améliorer l'efficacité à la puissance back-off. Dans cette méthode, un signal d'entrée d'enveloppe variable est d'abord décomposé en deux signaux à phase modulée d'enveloppe constante et ensuite est amplifié en utilisant deux PAs non linéaire de haute efficacité. Les signaux de sortie sont combinés préférentiellement en combinateur de puissance sans perte pour construire le signal de sortie voulu. De cette façon, le PA présente une haute efficacité avec une bonne linéarité.

Dans cette thèse, nous analysons tout d'abord un modèle complexe de combinateur déphasé en considérant ses caractéristiques non idéales telles que la réflexion et les pertes dans les lignes de transmission (TL). Ensuite nous proposons un modèle compact avec une formule analytique qui est validée à travers plusieurs tests comparatifs en utilisant ADS et Spectre RF. Par la suite, nous analysons l'effet de charge réactive dans le combinateur Chireix avec des plaques (un inducteur parallèle et une capacité), en distinguant les parties capacitives et inductives. Il est démontré que seule la partie capacitive de la charge réactive dégrade les performances. Basée la dessus, une nouvelle architecture (Z-LINC) est proposée dans laquelle le combinateur de

puissance est conçu pour fournir une charge zéro capacitive au PAs quel que soit l'angle de déphasage. La théorie qui décrit les opérations du système est développée, un 900 MHz LINC classique et Z-LINC PAs sont conçues et mesurés. De plus, une technique de miniaturisation est proposée qui emploie lambda/8 ou de plus petits TLs à la place des conventionnels lambda/4 TLs dans le combinateur de puissance déphasé. Cette technique est appliquée en implémentant un 900 MHz PA en utilisant des LDMOS transistors de puissance.

Outre les PAs à une seule bande, les PAs à deux bandes sont de plus en plus nécessaires à cause de la demande croissante pour les terminaux de communication sans fils pour gérer des opérations à bandes multiples. Dans le dernier chapitre, une nouvelle approche de design compact pour des transmetteurs à deux bandes, basée sur un combinateur de déphasage reconfigurable, est proposée. L'objectif est d'éviter les implémentations lourdes où les nombreux PAs et le "matching network" sont utilisés en parallèle. Cette technique est appliquée pour concevoir un PA à bande double avec un combinateur de puissance totalement intégré dans une technologie CMOS 90 nm. Un inverseur, basé sur la classe D et une topologie PA particulièrement approprié pour des opérations de déphasage et multimode, est présenté. Les TLs dans le combinateur, réalisés en utilisant un réseau de on-chip capacités en série et d'inducteurs en parallèle, sont reconfigurables de lambda/4 à 1800 MHz à lambda/8 à 900 MHz. Afin de maximiser l'efficacité, les inducteurs on-chip sont implantés en utilisant des plaques d'inducteurs on-chip de hauts facteurs de qualité. Les P_{out} maximums mesurés à 900/1800 MHz sont 24.3 et 22.7 dBm avec des efficacités maximums de 51% et 34% respectivement.

Mots clés: Chireix, déphasage, LINC, amplificateur de puissance, combinateur de puissance, lignes de transmission, plaques d'inducteurs, doubles bandes, LDMOS, CMOS, circuits intègres RF.

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1 Introduction

1.1 Wireless communication Evolution, Challenges and Future Possibilities

The wireless market has experienced a remarkable development since introducing the first modern mobile phone systems, with a steady increase in the number of subscribers, new application areas, and higher data rates. For instance, the first handheld mobile phone demonstrated by Martin Cooper of Motorola, was weighted around 1 Kg with less than 35 minutes talk time (Fig. 1-1) [1]. Now, with more than 6 billion wireless phone subscribers around the world, cellular phones are used as a GPS navigator, a multimedia center, a shopping terminus, a compact camera and lastly a telephone.

Cellular phones are not the sole example of a market that has prompted recent research activity but also wireless local-area networks (WLAN's) are another relatively new application of radio frequency (RF) circuit design. As mobile phones and wireless connectivity have become consumer mass markets, the major goal of the integrated circuit (IC) manufacturers is to provide low-cost solutions to maximize their profits. Accordingly, the inevitable task and ultimate goal of the modern wireless communication industry is the full integration of analog, digital and even RF circuits. To this end, the industry has devoted great effort to designing wireless terminals using a common semiconductor process that utilizes a single chip. The RF circuits have been predominantly designed in GaAs FET and silicon bipolar, due to the better performance [2].

Fig. 1-1: Enormous development in mobile industry; Martin Cooper shows his first handheld mobile phone and one latest small smart phone [1].

However, during the last decade, complementary metal oxide semiconductor (CMOS) has been the extensive choice for digital integrated circuits due to its high level of integration, low-cost, and constant improvements in performance [2]. To minimize the costs and allow full integration of a whole radio System-on-Chip (SoC), it is desirable to integrate the digital, analog and RF blocks in a single CMOS chip.

1.2 Motivation

While digital circuits benefit from the technology scaling, because of the intrinsic drawbacks of standard CMOS processes from the RF perspective, several obstacles, especially low quality factor (Q) passive inductors, lossy and low resistive substrate, and low breakdown voltage of transistors [3], are hindering the realization of a fully-integrated CMOS transceiver. Low oxide breakdown voltage forces high output power CMOS RF power amplifiers (PAs) to operate under low input impedance and high current levels where they are sensitive to parasitics. On the other hand, efficiency is a big concern in linear PAs. Because of power back-off in modern communication systems, it is essential to improve the efficiency of the PA when it is not operating at its maximum output power. Since the PA is often the most power hungry component in the transmitter, its efficiency dominates system overall efficiency and thus battery

life-time of portable devices. The same problem happens in cellular base stations where a significant portion of the operating costs, come from losses in the PAs, including electricity expenses and additional costs because of bulky heat sinks. As a result, implementation of RF front-ends especially the PA in CMOS technology remains challenging task. This has recently triggered extensive studies to investigate the impact of different efficiency enhancement and linearization techniques, such as polar modulation and outphasing, in advanced CMOS technologies.

We mentioned that from a performance oriented point of view, CMOS technologies are not a good choice to implementing RF PAs. However, CMOS technology follow an aggressive down-scaling roadmap that is unbeatable when compared to any other semiconductor technology. Therefore, the integrability and versatility of CMOS technologies will be welcomed. Narrowing down the focus to the cost of PAs, CMOS technologies would be the cheapest among other candidates such as III-V HBT, III-V PHEMT, SiGe HBT, and MOSFET technologies [2].

Besides low efficiency drawback of RF PAs at power back-off, multi-band connectivity is another issue to be dealt with in modern communication systems. Both mobile phone systems and WLANs have recently experienced a shift from a single to multi-standard connectivity. For example, a smart phone such as Galaxy S4 connects to 802.11 b/g/n Wi-Fi, Bluetooth 4.0, GLONASS, GPS, GSM / GPRS / EDGE, UMTS / HSDPA / HSUPA, and CDMA / EV-DO Revision A standards. These standards operate on the following frequencies: 800MHz, 850MHz, 900MHz, 1.9GHz, 2.1GHz, 2.4GHz, and 5.0GHz [4]. Today, each frequency requires its own wireless radio, as shown in Fig. 1-2.

This trend has been accelerated by the emergence of new communication technologies, such as software defined radio (SDR) and Cognitive Radio (CR) [5]. In fact, the success of SDR and CR technologies depends largely on the ability to design agile terminals, able to work simultaneously in different frequency bands and supporting various modulation schemes. Although several advances have been made in this direction, the success was restricted to the baseband and RF front-ends circuits [6]. Because of its challenging design, the PA has been excluded from this trend. Except a few attempts that are principally based on MEMS adaptive

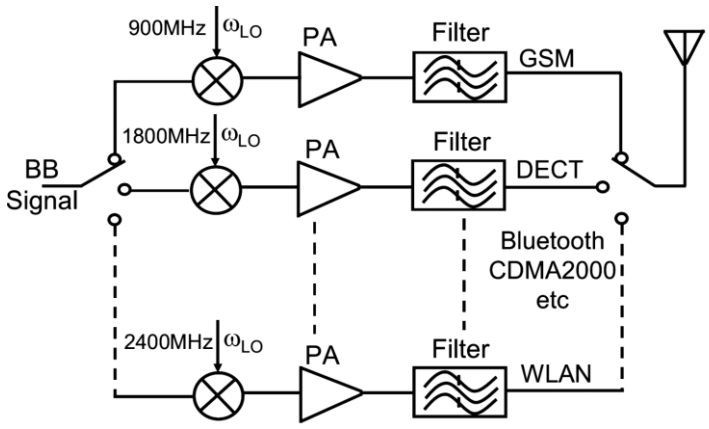

Fig. 1-2: Conventional multi-standard transmitter with dedicated PA for each band.

matching networks [7], the multi-PAs implementations are still the dominant choice [8]. Thus, the second objective of the project is implementing the multi-band PAs. In chapter 5, we address the possibility of integrating dual-band, linear and power-efficient PAs in nanometer CMOS technologies at GHz frequencies.

1.3 Thesis Organization

The outline of this thesis is as follow:

Chapter II briefly reviews several PA's performance metrics and different efficiency enhancement and linearization techniques. These techniques are compared and their benefits and drawbacks are briefly summarized. Furthermore, prevalent technologies for RF PAs are reviewed and compared. The device scaling and power supply trend in CMOS technology and its effect on PA design are also explained in this chapter.

Chapter III, provides a comprehensive analysis of outphasing PA modeling methods and challenges. A new analyzing method using a circuit-oriented approach is proposed. The new expressions are validated through several comparative tests using ADS and SpectreRF. Finally, the theoretical analysis is enhanced by including the losses in the power combiner.

Chapter IV explains the implementation of two outphasing PAs using LDMOS transistors. In this chapter we first explain the feature of the employed transistor. Then, two approaches of

designing outphasing TX are explained, Zero capacitive LINC and power combiner miniaturization technique. Furthermore, simulation and measurement results are presented to validate the designs.

In chapter V, a prototype of the proposed outphasing CMOS PA is illustrated. The design procedure of a single band, slab- based power combiner and theoretical analysis of the proposed dual band outphasing power combiner are explained. In addition, the details of the PA design, its challenges, and the reliability issues in CMOS PAs are also described. To validate the design, the simulation and measurement results are presented.

Chapter VI, discuss the challenges in measuring the linearity performance of the outphasing PA and chapter VII concludes the thesis.

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2 Introduction to the power amplifiers

Designing a PA for wireless communication standards that uses complex modulation schemes, needs a good understanding of the characteristics of the PA. This is essential to optimize its performance in terms of linearity and efficiency. There are different ways to measure the PA's linearity and the efficiency such as Spectral mask, EVM, Drain efficiency and PAE. In this chapter we will discuss these indices.

Furthermore, a trade-off between linearity and efficiency always exists in classic power amplifiers. Linear mode PAs like class-A and class-AB are good for linearity and switch mode PAs like class-E and class-F are good for efficiency. To overcome this trade-off, efficiency enhancement techniques such as Doherty, LINC, Envelop tracking and Polar Modulation are employed. In this chapter, these techniques and the appropriate technologies to implement mobile/base-station PAs are compared.

2.1 Power Amplifier metrics

Output power is one of the key figures in designing PAs. It can be calculated [1] by measuring output voltage over the matched load or connecting PA output to the power meter (Fig. 2-1),

$$P_{out} = S_L^2 \Big/ 2R_L , \tag{2-1}$$

where S_L is the voltage amplitude of the output signal. The gain of the PA can be defined as

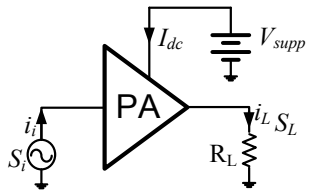

Fig. 2-1: Simplified schematic of a PA.

$$\text{Power Gain} : A_P = {P_{out}}/{P_{in}}, \tag{2-2}$$

$$\text{Voltage Gain} : A_v = {S_L}/{S_i}, \tag{2-3}$$

where S_i and P_{in} are the input voltage amplitude and the input power respectively. A_P and A_V are equal in *dB* if the input and output impedance are equal and matched. The efficiency of a PA is a critical factor to measure how effectively input DC power is converted to RF power. The input DC power is,

$$P_{dc} = V_{supp} \times I_{dc}, \tag{2-4}$$

Thus, the efficiencies can be defined as,

$$\text{Drain Efficiency} : \eta_D = 100 \times {P_{out}}/{P_{dc}}, \tag{2-5}$$

$$\text{Power Added Efficiency} : PAE = 100 \times {(P_{out} - P_{in})}/{P_{dc}}. \tag{2-6}$$

The term *PAE*, shows the ratio between the RF power added by the PA, and its DC power consumption. It is a better representative of the PA efficiency than the Drain efficiency, as it includes P_{in}. The most convincing method to measure the efficiency performance of the PA, used to amplify the variable envelope signal, is the average efficiency as it directly relates to the battery life time.

$$\overline{\eta}_{AVG} = 100 \times {\left(\overline{P}_{out} - \overline{P}_{in}\right)}/{\overline{P}_{dc}}, \tag{2-7}$$

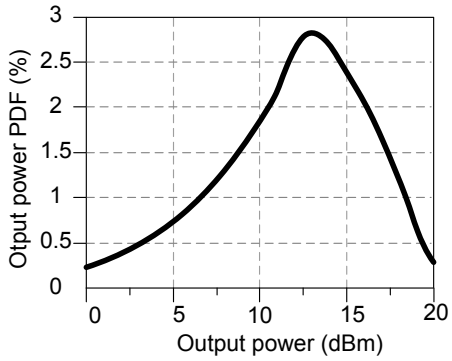

Fig. 2-2: Output power Probability Density Function (PDF).

and the average input and output power can calculated as

$$\overline{P}_{out} - \overline{P}_{in} = \int_{0}^{P_{out},\max} \left(P_{out}(P_{out}) - P_{in}(P_{out})\right) \times PDF(P_{out}) dP_{out}, \tag{2-8}$$

$$\overline{P}_{out} - \overline{P}_{in} = \int_{0}^{P_{out},\max} P_{dc}(P_{out}) \times PDF(P_{out}) dP_{out}, \tag{2-9}$$

where $PDF(P_{out})$ is the output power Probability Density Function (PDF) shown in Fig. 2-2.

Two important parameters, P_{sat} and P_{1dB} are used to characterize PA output power. P_{sat} shows that maximums output power level, while P_{1dB} indicates output power level when the gain falls by 1dB below its linear value shown in Fig. 2-3.

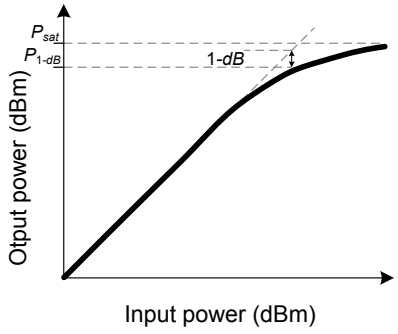

Fig. 2-3: P_{sat} and $P_{1\text{-}dB}$ of the PA output power.

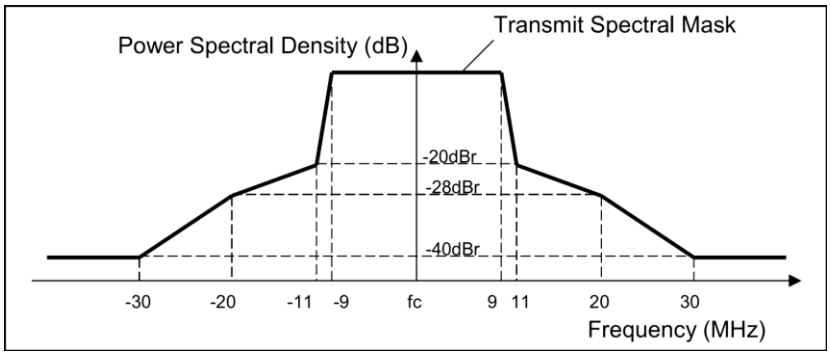

Fig. 2-4: Spectral mask versus frequency [2].

The PA linearity can be quantified by using output power spectral mask. Although the transmitted signal spectrum should be limited to the assigned frequency band, the transmitter nonlinearity spreads the spectrum to the adjacent channels. Each wireless standard has its own specific spectral mask. In general, it shows the in-band power density as a flat top and a mask that limits the out-of-band power radiation. Fig. 2-4 shows the spectral mask of a standard versus frequency. Another signal linearity metric is the Error Vector Magnitude (EVM) that is calculated on I and Q plane (Fig. 2-5). Due to several imperfections in the PA like non-linearity of the transistors, IQ imbalance, gain variations, noise, the constellation points of the transmitted signal deviate from their ideal locations. The difference between the measured signal and the ideal reference signal generates the error vector and in general is defined as the rms value of the error vector over time. The EVM value can be defined as

$$EVM = \left| \vec{e} \middle/ \vec{r} \right| . \tag{2-10}$$

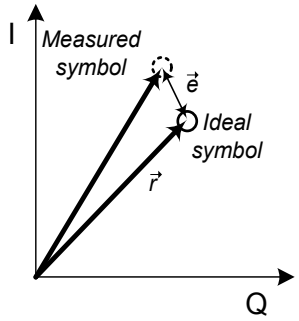

Fig. 2-5: EVM representation in IQ plane.

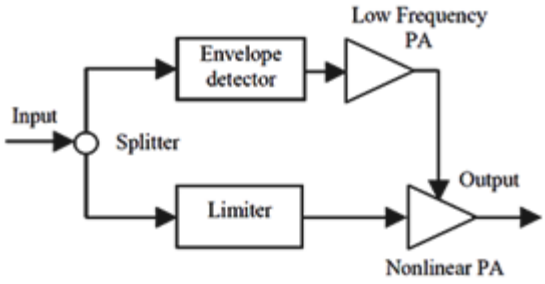

Fig. 2-6: Schematic of polar modulation/EER technique [3].

2.2 Efficiency enhancement techniques

As discussed in previous section, complex modulations used in modern wireless communications impose considerable linearity requirements on the transmitter. As a result, PA efficiency should be sacrificed to provide the required linearity. To avoid this trade-off in linear PAs, a variety of new PA architecture have been proposed. Such architectures should satisfy the linearity limitation of the standard with an enhanced efficiency in power back-off mode. Among different types of new architecture, four important techniques are polar modulation, Doherty amplifier, Pulse-Width Pulse-Position Modulation (PWPM), and outphasing modulation.

2.2.1 Polar modulation

Polar modulation (Fig. 2-6), also known as Envelope Elimination and Restoration (EER) technique [3], was first introduced by Kahn in 1952. In a simplified model shown in Fig. 2-6, the amplitude and phase information in the variable envelope input signal are separated using an envelope detector and a limiter. As the envelope information is eliminated from the input signal, it can be amplified by a highly efficient switching PAs. The amplitude information is then amplified through a low frequency PA (Supply Modulator) and restored when modulates the PA's power supply. This method transfers efficiency-linearity trade-off from PA side to the Supply Modulator. To reach the highest efficiency, switching PAs are used in the supply modulator as well. But the efficiency of the supply modulator degrades significantly as bandwidth increases. During Cartesian to Polar conversion, the bandwidth of the amplitude signal expands by a factor of 5-10. As a result, this technique is typically suitable for low-

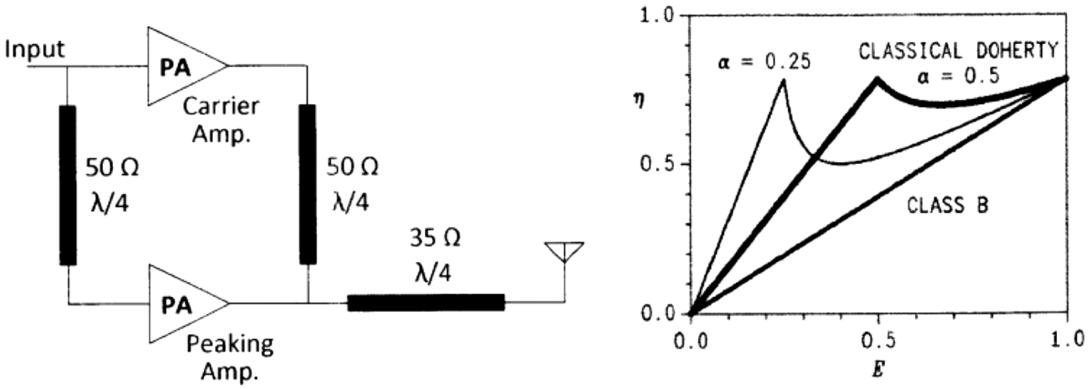

Fig. 2-7: Doherty PA and its normalized efficiency versus normalized output power [4].

bandwidth applications. Another drawback of the Polar modulation is the delay mismatch between the envelope and phase paths. This issue is exacerbated in GHz range frequencies.

2.2.2 Doherty Amplifier

The Doherty PA (Fig. 2-7) was first reported in 1936 by William H. Doherty of Bell Laboratories that was originally implemented using vacuum tubes [4], [5]. Fig. 2-7 shows its simple schematic which consists of a main and an auxiliary PA. The main (carrier) PA is biased in class-B/AB mode while the auxiliary (Peaking) PA is biased in Class-C mode. With this configuration, the auxiliary PA turns on only after the input amplitude exceeds a specific value. This means that at small input power, only the main PA is operational. As the input power is increasing the PA reaches its first maximum efficiency point. At this moment, the auxiliary PA is turned on. By reaching the maximum output power, the efficiency of the auxiliary PA and thus the total efficiency reach their maximum value. Therefore, the Doherty PA enhances the efficiency over a wide range of output power. The location of first peaking efficiency can be optimized depending on the PDF (Probability Density Function) of the output power. The main drawbacks of this technique is the three $\lambda/4$ TLs which is very difficult to integrate at the typical frequencies used in modern telecommunication systems (0.8-3 GHz).

2.2.3 Pulse-Width Pulse-Position Modulation (PWPM)

The Pulse-Width Pulse-Position Modulation (PWPM) technique employs pulse width modulated input signal to generate variable envelope output signal (Fig. 2-8). The output voltage

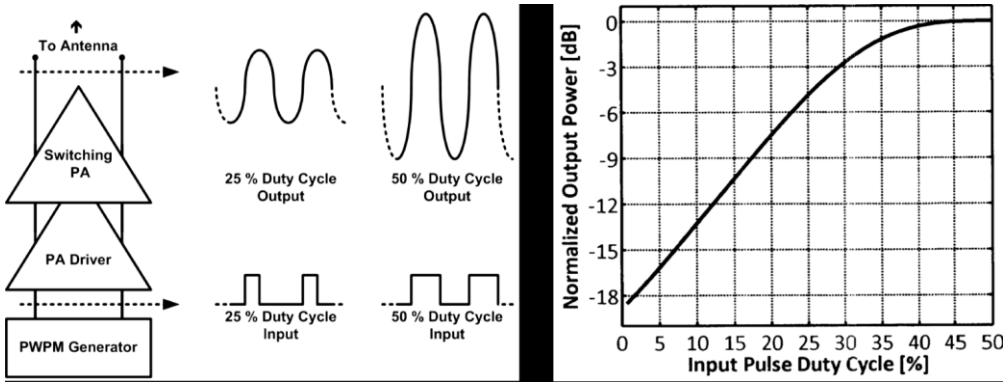

Fig. 2-8: Generalized PWPM PA and output power of an ideal Class E PA versus input pulse duty cycle [6].

in a Class-E [6] switching PA, depends on the conduction interval of the transistors and thus the duty cycle of input signal. The output phase is controlled by the position of the input pulse. PWPM achieved higher efficiency than the standard Doherty PA because it uses Switching PAs instead of Class-B/AB/C PAs. The main drawback of PWPM technique is its small PAPR (Peak to Average Power Ratio). For instance, Fig. 2-8 shows that in an ideal Class-E PA, the power back-off is less than 20 dB when the duty cycle is reduced to 1%. Besides the difficulty of generating such narrow pulses in GHz applications, these pulses are usually filtered by the large transistor input capacitance. In practice, the PAPR is less than 10 dB that is lower than the modern communication requirements.

2.2.4 Outphasing Modulation

Outphsing technique, also named LINC (linear amplification using nonlinear components), was first proposed by Chireix in 1935 [7]. In this technique, the variable amplitude input signal (Fig. 2-9) decomposed to two phasors with constant envelope using signal component separator (SCS) shown in Fig. 2-9. By means of this decomposition the amplitude information transfers to phase domain. Thus, highly efficient switching PAs are used to amplify the phasors. The output of the PAs are summed in the power combiner to produce a linear amplified version of the input signal. In the next chapter, detailed theoretical analysis outphasing is explained.

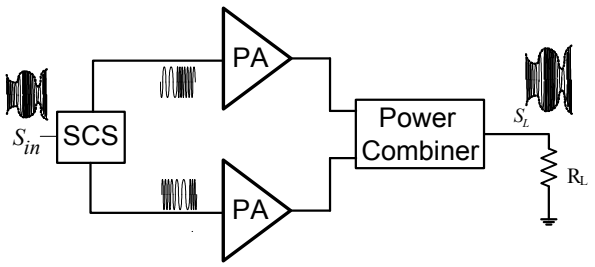

Fig. 2-9: Simple schematic of outphasing modulation.

One of the drawbacks of Outphaisng, is its power combiner. Typical combiners (e.g. Wilkinson) achieve its maximum efficiency only at maximum output power. But, when the phasors are outphased and the output power is decreased, the remaining power is wasted in power combiner isolating resistor. This results in a degraded efficiency in power back-off. In the next chapter, our solutions for efficient combining will be explained. Delay mismatch is another drawback of outphasing technique. Fortunately, unlike polar modulation, the two paths are identical. Thus, the mismatch is minimized by using improved layout strategies in integrated applications. In the next chapter, the details of outphasing modulation will be discussed.

2.3 Technology selection for power amplifiers

In this section, we describe two major semiconductor technologies CMOS and LDMOS, to implement integrated PAs for mobile applications and high-power PAs for base-station applications. Silicon has been preferred as semiconductor material because of its integrability and functionality along with a constant increase in its performance. By combining the low cost and integration capabilities of CMOS/BiCMOS, these technologies were the choice of RF transceivers with fully-integrated PAs, as long as RF and system design goals can be achieved. As wireless functionality has been integrated into more and more applications and entered mass-consumer markets, silicon-based technologies have continuously replaced the traditional semiconductors. Currently, the market of integrated wireless transceivers is dominated by CMOS, where fully-integrated solutions, including the PA, have been presented. Silicon-based technologies will be the choice for high volume and cost sensitive markets, but is not expected to be the choice when the PA metrics are very high gain, very high output power, and extremely low noise.

First, a short comparison of the specific properties of III-V compounds and silicon is given here because it was one of the first semiconductors used in RF design and is still used in PA design. Key characteristics of the basic materials are shown in Table 2.1. For example, the carrier velocity and mobility of the electrons are higher than the holes and its difference is much larger in III-V devices (e.g. GaAs) than for silicon devices [8]. In addition, the carrier velocity and mobility of electrons are lower in silicon devices. Because of the large gap in complementary III-V devices and the lower hole carrier velocity and mobility in GaAs, silicon technologies are more suitable for high speed complementary logic applications. Conversely, for high-speed applications, n-based GaAs devices has advantageous as long as no complementary devices are used.

Thermal conductivity is another important factor in complementary logic circuits. Considering too many transistors for example in an integrated PA, heating dissipation may cause problem. Thus, a good thermal conductivity of the substrate material is mandatory to ensure that the chip is not overheated. The comparable integration level in GaAs is typically limited to approximately 1000 transistors [8].

Substrate resistivity is another weakness of the silicon devices that is relatively low compared to the III-V semiconductors, and degrades the quality factor of integrated passives [9]. An advantage of silicon and CMOS is its production cost, and the relative speed performance between the electron and hole carrier based devices. This makes silicon a superior choice for complementary logic circuits. Integration of PA could further reduce the cost and BiCMOS solves the integration of the PA and with better RF performance of the bipolar devices compared to the MOSFET devices. It has around 20% higher mask count and thus a higher price for the same technology [10].

Although GaAs has a lower mask price thus lower prototype cost, Silicon has the advantage of higher yield and using larger wafers. As a result Silicon is the cheaper option in mass fabrication.

The historical trend of CMOS scaling has enabled high-speed CMOS devices a preferable solution in complementary logic circuits, and the trend is expected to continue, but at the expense

of lower supply voltages. The supply voltage and thus the RF output power of III-V technologies are higher. Therefore these technologies is the dominant choice in the market of PAs for handset applications [11]. For higher output power, SiC, GaN, and also LDMOS have better performance over the other devices, because of their higher supply voltage and thermal conductivity, with the cost of a lower level of integration.

Table 2.1. Comparison of semiconductor Technologies [8]

	Silicon	SiC	InP	GaAs	GaN
Electron mobility a 300K [cm^2/Vs]	1500	700	5400	8500	1000-2000
Hole mobility at 300K [cm^2/Vs]	450	n.a	150	400	n.a
Bandgap [eV]	1.1	3.26	1.35	1.42	3.49
Critical breakdown field [MV/cm]	0.3	3.0	0.5	0.4	3.0
Thermal conductivity [W/(cm K)]	1.5	4.5	0.7	0.5	>1.5
Substrate resistivity [Ωcm]	1-20	1-20	>1000	>1000	>1000
Number of transistors in IC	>1 billion	<200	<500	<1000	<50
Transistors	MOSFET, Bipolar, HBT, LDMOS	MESFET, HEMT	MESFE, HEMT, HBT	MESFET, HEMT, HBT	MESFET, HEMT
Costs prototype, mass fabrication	High, low	Very high, n.a.	High, very high	Low, high	Very high, n.a.

2.3.1 LDMOS power transistors

About 20 years ago LDMOS (Laterally Diffused Metal-Oxide-Semiconductor) transistors were introduced as a replacement of BJT (Bipolar Junction Transistor) for RF power applications [12]. In fact, LDMOS devices are enhanced Nchannel MOSFETs (Metal-Oxide-

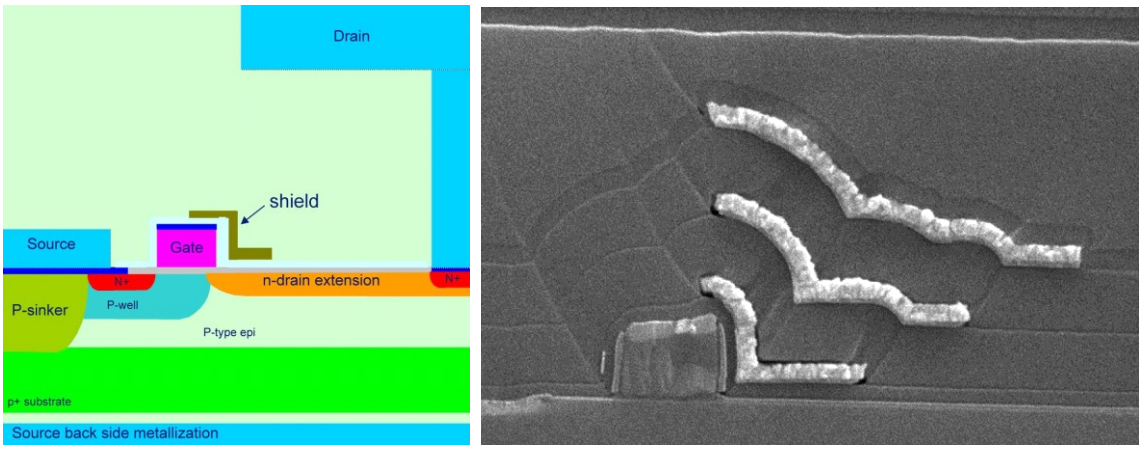

Fig. 2-10: LDMOS cross section schemantic and photo [12].

Semiconductor Field-Effect Transistor). Today, LDMOS technology is the leading RF power technology for base station applications, in particular for GSM-EDGE at 1 and 2 GHz, WCDMA at 2.2 GHz and more recently for WiMax applications at 2.7 GHz and 3.8 GHz. The power range of LDMOS spans more than three decades ranging from a few watts for driver devices up to hundreds of watts for base station applications.

The cross section of the device (Fig. 2-10) is optimized for high frequency and high voltage operation with small parasitic capacitance. It is designed to realize higher f_T, lower third order intermodulation and higher g_m and gain at high power level. These specifications enables to design PAs with better efficiency and fewer gain stages compare to BJT. Its main difference with standard CMOS is that an LDMOS transistor has a drain extension region to support a higher breakdown voltage. To provide high power, LDMOS devices are mounted with multiple fingers in parallel inside the package (Fig. 2-12). The flange is soldered to the source at backside of the device however the drain and gate are connected via bond wires to the pads. The input and output impedance of the device can be below a few ohms, thus input and output matching could be employed inside the package to transform the impedance level.

Fig. 2-11 shows a summary of the preferred technologies for today's PA design as a function of output power and operating frequency. It is shown that LDMOS is expanding towards the high frequency and high power applications.

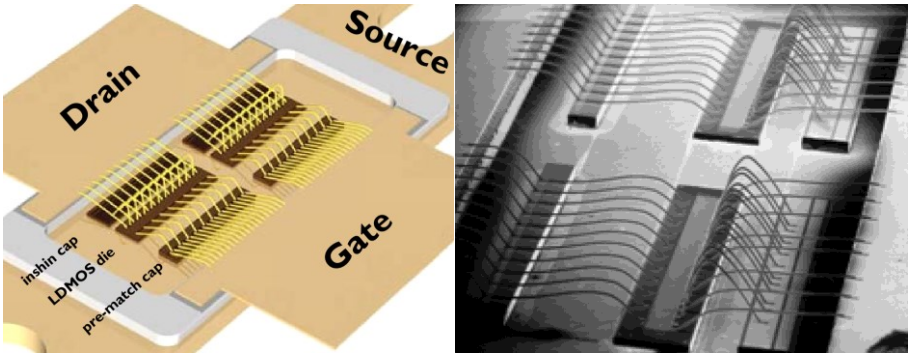

Fig. 2-12: LDMOS device with input and output matching inside the package [12].

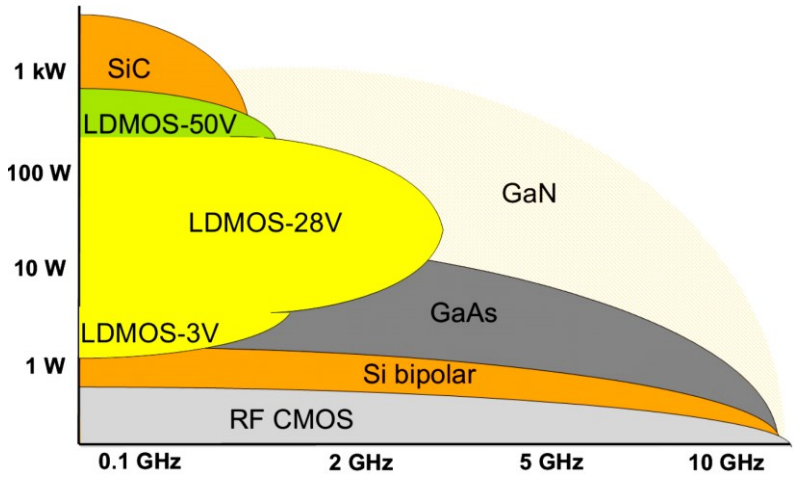

Fig. 2-11: Technology selection based on operating frequency and output power [13].

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3 Theoretical analysis

The design of PAs, particularly for highly efficient and linear operation, remains a difficult problem that needs theoretical models for preliminary analysis, parameters specification and performance optimization before starting circuits design and simulation. In the particular case of outphasing PA, the theoretical analysis with an ideal power combiner was proposed first in [1]. This work was later completed in [2] by considering the effect of impedance mismatch between the amplifiers and the combiner. Despite the simplification of the problem by neglecting the power combiner non-idealities, the expressions describing outphasing TX are too complex and far from intuitive [2]. This chapter provides a comprehensive analysis of outphasing PA modeling methods and challenges. We study different types of outphasing combiners and explain how they introduce reactive loads and impact the efficiency and linearity of the PA. Then, we analyze a complex model of Chireix combiner considering the reflection due to impedance mismatch and the effects of compensating stubs. Afterwards, a new analyzing method using a circuit-oriented approach is proposed. A simplified analytical formula expressing the output power directly in terms of the non-distorted input phase is derived. The new expressions are validated through several comparative tests using ADS and SpectreRF. Finally, the theoretical analysis is enhanced by including the losses in the power combiner.

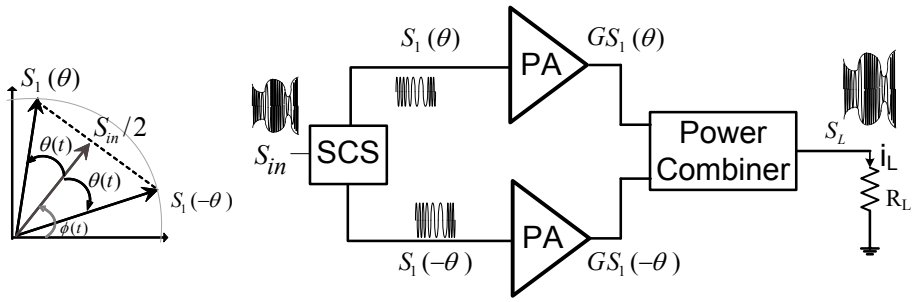

Fig. 3-1: Simplified diagram of Outphasing Tx.

3.1 Classical outphasing PA modeling with ideal voltage sources

Our analysis starts by considering the classical outphasing PA [1], [3] shown in Fig. 3-1. The envelope modulated input signal

$$S_{in}(t) = |S_{in}(t)|e^{j\varphi(t)}, \tag{3-1}$$

is transformed in two constant envelope signals

$$S_1(\pm\theta(t)) = S_m e^{j(\varphi(t)\pm\theta(t))}, \tag{3-2}$$

where

$$\theta(t) = \cos^{-1}\left(|S_{in}(t)|/2S_m\right). \tag{3-3}$$

Since the signals $S_1(\pm\theta)$ exhibit no envelope variation, highly efficient nonlinear PAs (e.g. class F, D or saturated class B) can be used for their amplification [4]. After amplification, the signals are combined, resulting ideally in an amplified replica of the input signal at the antenna, i.e.

$$S_L(t) = G(S_1(\theta) + S_1(-\theta)) = GS_{in}(t). \tag{3-4}$$

where G is the gain of the non-linear PAs. An efficient power combining method is needed to combine the two amplified outphased signals and produce the desired output signal. Basically two families of power combiners can be used for this operation: isolating combiners (e.g. Hybrid

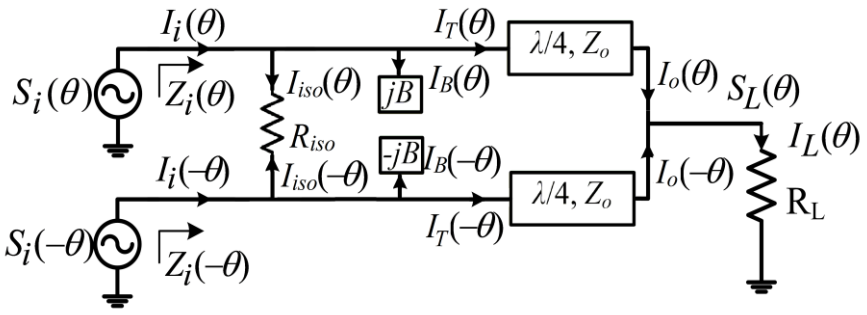

Fig. 3-2: A general four-terminal combiner, a) Wilkinson with $B = 0$, b) Chireix with $R_{iso} = \infty$ and $B = 0$, and c) Chireix with stub and $R_{iso} = \infty$.

or Wilkinson) and non-isolating combiners (e.g. Chireix [3] or transformers [5]). Fig. 3-2 shows a general four-terminal outphasing combiner. Each PA replaced by an ideal voltage source without loss of generality. From (3-2) and Fig. 3-1, the signal at the input of power combiner is

$$S_i(\pm\theta(t)) = GS_1(\pm\theta(t)) = GS_m e^{j(\varphi(t)\pm\theta(t))}. \tag{3-5}$$

For simplicity, the phase of the input signal, $\varphi(t)$, can be ignored without affecting the analysis. Therefore we can write

$$S_i(\pm\theta) = S_{max} e^{\pm j\theta}, \tag{3-6}$$

where $S_{max} = GS_m$. Now we replace the PAs by ideal voltage sources (without loss of generality), as illustrated in Fig. 3-2 and we use ABCD matrix of the TL with an electrical length $\alpha = 90°$ and a characteristic impedance of Z_o

$$\begin{bmatrix} S_i \\ I_T \end{bmatrix} = M_{\lambda/4} \begin{bmatrix} S_L \\ I_o \end{bmatrix} = \begin{bmatrix} \cos\alpha & jZ_o \sin\alpha \\ \dfrac{j\sin\alpha}{Z_o} & \cos\alpha \end{bmatrix}_{\alpha=90^\circ} \begin{bmatrix} S_L \\ I_o \end{bmatrix} = \begin{bmatrix} 0 & jZ_o \\ j/Z_o & 0 \end{bmatrix} \times \begin{bmatrix} S_L \\ I_o \end{bmatrix}, \tag{3-7}$$

the output current and voltage are expressed as follows,

$$I_o(\pm\theta) = -j.\frac{1}{Z_o}.S_i(\pm\theta) = -j.\frac{1}{Z_o} S_{max} e^{\pm j\theta}, \tag{3-8}$$

$$S_L(\theta) = Z_L \times I_L(\theta) = Z_L.(I_o(+\theta) + I_o(-\theta)) = -j.\frac{2R_L}{Z_o} S_{max}\cos(\theta)\,. \tag{3-9}$$

The output power is therefore given by

$$\left|P_{out}(\theta)\right| = \left|\frac{S_L^2(\theta)}{2R_L}\right| = \frac{2R_L}{Z_o^2} S_{max}^2 \cos^2(\theta)\,, \tag{3-10}$$

and varies from 0 at $\theta = 90$ to its maximum value ($2R_L S^2_{max}\, Z_o^{-2}$) at $\theta = 0$. In order to calculate the input power (P_{in}) and thus the efficiency, we start by analysing the input resistance. From (3-7) and (3-9) the input current of Wilkinson power combiner in Fig. 3-2.a, can be expressed as

$$I_{i,Wilk}(\theta) = I_T + I_{iso} = \frac{2R_L}{Z_o^2} S_{max}\cos(\theta) + \left(S_i(+\theta) - S_i(-\theta)\right)/R_{iso}\,, \tag{3-11}$$

In a matched condition where $R_{iso} = Z^2_O/R_L$, the input impedance of the Wilkinson combiner is

$$Z_{i,Wilk}(\pm\theta) = S_i(\pm\theta)/I_{i,Wilk}(\pm\theta) = \frac{Z_o^2}{2R_L}\,. \tag{3-12}$$

In isolating condition, the input impedance and thus the input power are independent of θ. Indeed, the constant value of $Z_{i,wilk}$ results in a constant input power,

$$\left|P_{in,Wilk}(\theta)\right| = \left|\frac{S_i^2(\theta)}{2Z_{i,Wilk}(\theta)}\right| + \left|\frac{S_i^2(-\theta)}{2Z_{i,Wilk}(-\theta)}\right| = \frac{2R_L}{Z_o^2} S_{max}^2\,. \tag{3-13}$$

As a consequence the efficiency of Wilkinson combiner,

$$\eta_{Wilk}(\theta) = \frac{\left|P_{out}\right|}{\left|P_{in,Wilk}\right|} \times 100 = \cos^2(\theta) \times 100\ (\%) \propto \left|P_{out}(\theta)\right|, \tag{3-14}$$

is significantly degraded when θ is increased (power back-off mode). The difference between input and output power, is wasted as heat in the isolating resistor (R_{iso}). This loss nullifies the efficiency advantage inherent to the use of non-linear PAs and thus, limits the attractiveness of these combiners for LINC. In contrast, a non-isolating power combiner (Fig. 3-2.b) preserves

the LINC efficiency even in power back-off mode [1]. In this method the isolating resistor is removed to provide a pure reactive power combiner, commonly known as Chireix combiner. In this case, from (3-7) and (3-9) we have

$$I_{i,Chireix}(\pm\theta) = \frac{2R_L}{Z_o^2} S_{max} \cos(\theta), \tag{3-15}$$

$$\begin{aligned} Z_{i,Chireix}(\pm\theta) &= S_i(\pm\theta) / I_{i,Chireix}(\pm\theta) = \frac{Z_o^2}{R_L}.(1 \pm j\tan(\theta)) \\ &= \left[Y_{i,Chireix}(\pm\theta)\right]^{-1} = \left[\frac{R_L}{Z_o^2}.(2\cos^2(\theta) \mp j\sin(2\theta))\right]^{-1}. \end{aligned} \tag{3-16}$$

In Chireix combiner the magnitude of the input impedance,

$$\left|Z_{i,Chireix}(\pm\theta)\right| = \frac{Z_o^2}{2R_L\cos(\theta)}, \tag{3-17}$$

represents an increasing function of θ for $0° < \theta < 90°$. Consequently, the input power

$$\left|P_{in,Chireix}(\theta)\right| = \left|\frac{S_i^2(\theta)}{2Z_{i,Chireix}(\theta)}\right| + \left|\frac{S_i^2(-\theta)}{2Z_{i,Chireix}(-\theta)}\right| = \frac{2R_L}{Z_o^2} S_{max}^2 \cos(\theta), \tag{3-18}$$

is a decreasing function of θ, which results in an improved efficiency in power back-off. In fact we can write,

$$\eta_{Chireix}(\theta) = \frac{\left|P_{out}\right|}{\left|P_{in,Chireix}\right|} \times 100 = \cos(\theta) \times 100 \ (\%) \propto \sqrt{\left|P_{out}(\theta)\right|}. \tag{3-19}$$

Although Chireix combiner exhibits better efficiency compare to Wilkinson combiner, it still suffers from a diminution of the efficiency at high power back-off, principally because of the reactive loads introduced by the $\lambda/4$ TLs. Indeed, from (3-16) the imaginary part of the input admittance is

$$\mathrm{Im}\left(Y_{i,Chireix}(\pm\theta)\right) = \mp R_L \sin(2\theta) / Z_o^2. \tag{3-20}$$

Now, by placing the shunt stubs $\pm jB$, as shown in Fig. 3-2.c, and by choosing its susceptance as

$$B = R_L \sin(2\theta_0) / Z_o^2 , \tag{3-21}$$

the imaginary part of the input impedance becomes null at the specific angle θ_0 and at 90 - θ_0 [1]. Therefore, the theoretical efficiency reaches 100% at these two angles. The input impedance of Chireix combiner with stub can be expressed as

$$Z_{i,Stub}(\pm\theta) = Z_{i,Chireix}(\pm\theta) \left\| B^{-1} = \frac{Z_o^2}{R_L} . \left(2\cos^2(\theta) \mp j(\sin(2\theta) - \sin(2\theta_0))\right)^{-1} . \right. \tag{3-22}$$

Thus, the input power and efficiency are given by

$$\left|P_{in,Stub}(\theta)\right| = \left|\frac{S_i^2(\theta)}{2Z_{i,Stub}(\theta)}\right| + \left|\frac{S_i^2(-\theta)}{2Z_{i,Stub}(-\theta)}\right| = \frac{R_L}{Z_o^2} S_{max}^2 \sqrt{4\cos^4(\theta) + (\sin(2\theta) - \sin(2\theta_0))^2} \tag{3-23}$$

$$\eta_{Stub}(\theta) = \frac{\left|P_{out}\right|}{\left|P_{in,stub}\right|} \times 100 = \frac{2\cos^2(\theta)}{\sqrt{4\cos^4(\theta) + (\sin(2\theta) - \sin(2\theta_0))^2}} \times 100 \ (\%) . \tag{3-24}$$

Fig. 3-3 summarized the input impedance of the mentioned combiners and shows their efficiencies versus normalized output power. As expected, Chireix combiner with stub exhibits the best efficiency performance, with a theoretical value of 100 % for the output powers corresponding to θ_0 and at 90 - θ_0.

3.2 Modeling outphasing PA considering PA's non-idealities

In the models developed in the last section, the PAs were replaced by ideal voltage source. In practical cases however, voltage mode PAs (e.g. class D or F) can be approximated by an ideal voltage source and a series resistance to consider their finite output impedance in the models. On the other hand, the combiner provides variable loads with θ (3-22) and hence working in a matched condition for all output powers is impossible [2]. The principal

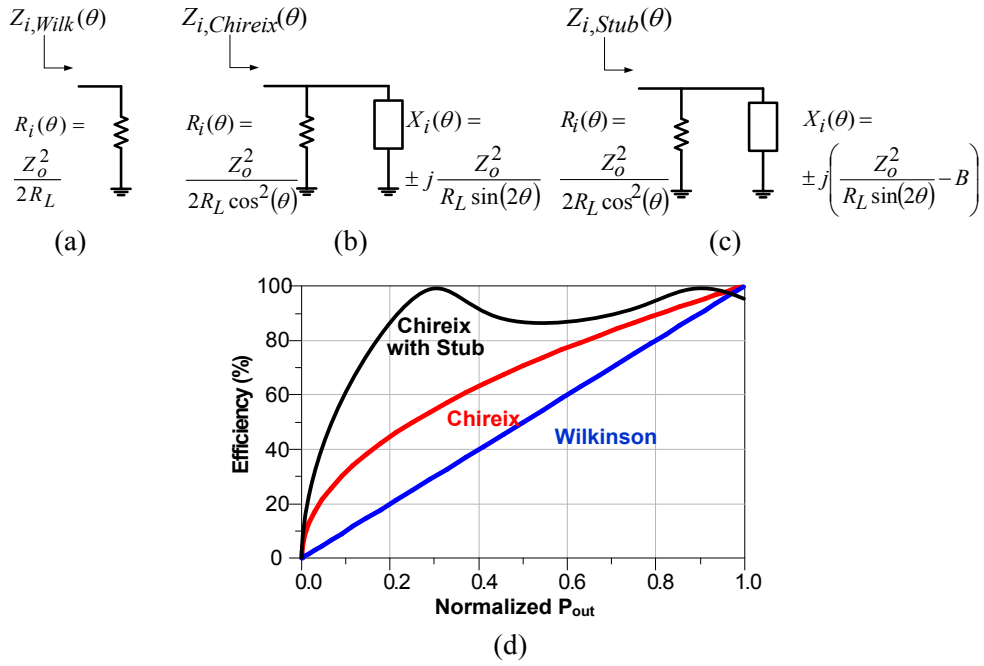

Fig. 3-3: The input impedance of a) Wilkinson, b) Chireix and c) Chireix with stub power combiners. d) Efficiency vs. Normalized P_{OUT} for different types of combiners.

consequence of this mismatch is a reflection of power at the output of the PAs. A PA driving a mismatched load (with a reflection coefficient of Γ) has an efficiency equal to $(1-|\Gamma|^2)\eta_{max}$; where η_{max} is the efficiency of a PA driving a matched load.

Fig. 3-4.a shows PAs driving Chireix combiner with stubs. Unlike previous section, here we use two PAs with a gain of G and output resistance of Z_1. El-Asmar et al. demonstrate in [2] after a tremendous theoretical calculations, the following expression for Z_2 as a function of θ and the normalized stub suceptance β, when reflected waves are considered:

$$Z_2(\beta,\theta^*) = \frac{1}{y^2/R_L\left(2\cos^2(\theta^*) + j[\beta - \sin(2\theta^*)\right)}, \tag{3-25}$$

where $y = R_L/Z_o$ and $\beta = B.R_L/y^2$. And θ^* is given by

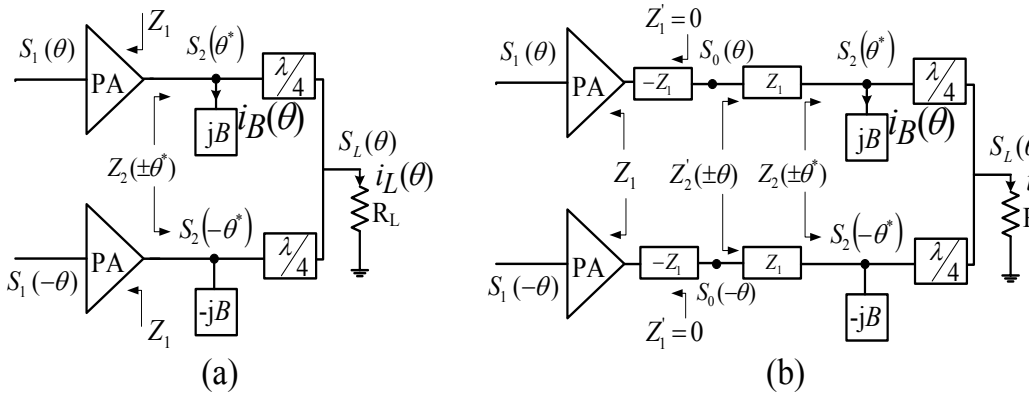

Fig. 3-4: a) Chireix-Outphasing topology with stub and b) simplified topology.

$$\theta = \theta^* - \text{phase}(1 + \Gamma(\beta, \theta^*)) \,. \tag{3-26}$$

where $\Gamma(\beta,\theta^*)$ is the reflection coefficient caused by the mismatch between Z_1 and the power combiner input impedance, Z_2,

$$\Gamma(\beta, \theta^*) = \frac{Z_2(\beta, \theta^*) - Z_1}{Z_2(\beta, \theta^*) + Z_1} \,. \tag{3-27}$$

The output voltage and efficiency according to [2] are

$$S_L(\beta, \theta^*) = 2y.G.S_{max} \left|1 + \Gamma(\beta, \theta^*)\right| . \cos(\theta^*) \,, \tag{3-28}$$

$$\eta(\beta, \theta^*) = \frac{8y^2 \cos^2(\theta^*)}{\left(1 + 2y^2 \cos^2(\theta^*)\right)^2 + y^4 \left(\beta - \sin(2\theta^*)\right)^2} \times 100 \ (\%) \,, \tag{3-29}$$

where θ^* can be derived from the following equation [2]

$$\cos(\theta^*) = \frac{1 + y^2 \beta \tan(\theta)}{\sqrt{\left(1 + y^2 \beta \tan(\theta)\right)^2 + \left((1 + 2y^2)\tan(\theta) - y^2 \beta\right)^2}} \,. \tag{3-30}$$

In outphasing Tx, the phase (θ) and the amplitude (S_m) are accurately calculated in order to reproduce the envelope variation of the modulated signal at the antenna. The unavoidable distortion of these parameters results in a severe degradation of the transmitted signal.

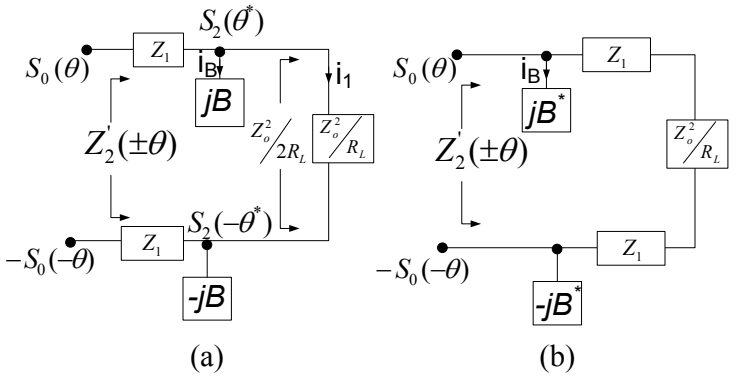

Fig. 3-5: a) Chireix-outphasing topology with stub and b) simplified topology.

Nevertheless, the complexity of the mathematical treatment of the nonlinear relations between η, θ^* and θ illustrated in (3-29) and (3-30), makes the development and implementation of pre-distortion functions extremely difficult.

3.3 Circuit oriented approach to simplify Chireix outphasing PA

In this section, we introduce an alternative method [6] to investigate the possible circuit transformations that would simplify the mathematical treatment and enable a more compact model. Because the phase distortion θ^* is the origin of the complexity of (3-30), we propose to bypass this parameter during the analysis. For this, we will create fictive nodes with voltages $S_0(\pm\theta)$, by adding the impedances $-Z_1$ and $+Z_1$ at the output of the PA (Fig. 3-4.b). In fact, the impedances seen at these points (i.e Z_1') are zero and thus the reflection coefficients (Γ) are equal to 1, which explains the non-distortion of the phase and amplitude at these nodes. $S_0(\pm\theta)$ is thus expressed as

$$S_0(\pm\theta) = G.S_1(\pm\theta).[1+\Gamma] = 2GS_m e^{\pm j\theta}. \tag{3-31}$$

Notice that this transformation enables us to express $Z_2(\pm\theta^*)$ in terms of the non-distorted phase θ if $Z_2'(\pm\theta)$ is known (i.e. $Z_2(\pm\theta^*) = Z_2'(\pm\theta) - Z_1$). In order to calculate $Z_2'(\pm\theta)$, other transformations are required. The impedances seen at the input of the two $\lambda/4$ transition lines at $\theta^* = 0$ are equal to $Z_o^2/2R_L$. Consequently, the part of the circuit driven by $S_0(\pm\theta)$ in Fig. 3-4.b

can be simplified to the circuit (a) in Fig. 3-5. Now we assume that the current i_B in Fig. 3-5.a is very small respect to i_1. This assumption will be validated later. In this case, we can write

$$\left|S_2(\theta^*=0)\right| = \frac{Z_o^2 \big/ 2R_L}{Z_o^2 \big/ 2R_L + |Z_1|}\left|S_0\right| = \left|i_B\right| B^{-1}. \tag{3-32}$$

Since i_B is very small, it has a negligible impact on the current over Z_1. Therefore, we can shift the place of the stubs in Fig. 3-4 towards the nodes $S_0(\pm\theta)$, as shown in Fig. 3-5.b. On the other hand, in order to keep the currents i_L and thus, i_B the same in Fig. 3-5 (a) and (b), the value of B is changed to B^*, calculated from (3-32) as

$$B^* = \left|i_B\right| \big/ \left|S_0\right| = B\frac{Z_o^2 \big/ 2R_L}{Z_o^2 \big/ 2R_L + |Z_1|}. \tag{3-33}$$

In this way, the circuit (a) of Fig. 3-5 is simplified to (b), where the two signals $S_0(\pm\theta)$ differentially drive the impedance Z_3 ($Z_3 = 2Z_1 + Z_O^2/R_L$). This enables to determine $Z_2'(\pm\theta)$ as

$$Z_2'(\pm B,\pm\theta) = \left(\frac{1}{Z_3}\frac{S_0(\theta)+S_0(-\theta)}{S_0(\pm\theta)} \pm jB\right)^{-1} = \left[\frac{1}{Z_3}\left(2\cos^2(\theta) \pm j\left(B^* Z_3 - \sin(2\theta)\right)\right)\right]. \tag{3-34}$$

Now, we return to the circuit of the transmitter in Fig. 3-4.b and we express the Z_2 (i.e. $Z'_2 - Z_1$) and S_i in terms of the non-distorted phase and amplitude (i.e. θ and $G.S_m$) as

$$Z_2(\pm\theta) = \left[\frac{1}{Z_3}\left(2\cos^2(\theta) \pm j\left(B^* Z_3 - \sin(2\theta)\right)\right)\right]^{-1} - Z_1. \tag{3-35}$$

$$S_2(\pm\theta) = S_0(\pm\theta).\left(1 - Z_1 \big/ Z_2'(\pm\theta)\right) = 2GS_m e^{\pm j\theta}.\left[1 - \frac{Z_1}{Z_3}\left(2\cos^2(\theta) \pm j\left(B^* Z_3 - \sin(2\theta)\right)\right)\right] \tag{3-36}$$

This approach makes it possible to completely bypass θ^* (3-30) and its inherent complex mathematical treatment. The power delivered to the load can now be determined from (3-35) and (3-36) in terms of the non-distorted phase and amplitude as

$$P_{out} = Mag\left(S_2(\pm\theta)\right)^2 \mathrm{Re}\left(1/Z_2(\pm\theta)\right). \tag{3-37}$$

On the other hand, the theoretical determination of the efficiency is more complex since it depends on dc power consumption of the PAs. To gain insights into efficiency evolution with design parameters we will make two assumptions. First, we can suppose the maximum voltage that the PA (i.e. in saturation) can deliver to a load, when its output impedance is null, is equal to its power supply (V_{DD}). In our case, this means that V_{DD} is equal to $2GS_m$. Furthermore, the dc current consumed by the PA is in general, proportional to its output RF current (e.g. $I_{dc} = k.(i_1 + i_B) = k.2GS_m.\mathrm{Mag}(1/Z_2')$, k is a constant). From that, we can define a normalized efficiency as

$$\eta_N = k\frac{P_{out}}{P_{dc}} \times 100 = \frac{Mag\left(S_2(\pm\theta)\right)^2 \mathrm{Re}\left(1/Z_2(\pm\theta)\right)}{(2GS_m)^2\, Mag\left(1/Z_2'(\pm\theta)\right)} \times 100\ (\%)\ . \tag{3-38}$$

Notice that in practice the harmful effect of the imaginary part of Z_1 (e.g. the drain parasitic capacitance) can be cancelled by using it as a part of the $\lambda/4$ transmission line. We can thus, consider that Z_1 is a real number in the equations. On the other hand, the shunt susceptance elements $\pm B^*$ are chosen to nullify the imaginary parts of Z_2 at a certain predefined phase (e.g. at $\theta = \theta_o$ (3-21)) Consequently, the magnitude of Z_2 reaches its maximum and the combiner input current its minimum at $\theta = \theta_o$ and at $\theta = 90° - \theta_o$, thereby maximizing the efficiency at these two specific values. Besides, the values of θ_o are chosen quite small in practical cases (typically $5° < \theta_o < 20°$ and thus, from (3-21) we have $0.086 < B/(2R_L/Z_o^2) < 0.3$). In fact, the susceptance elements optimize the efficiency between $\theta = \theta_o$ and $\theta = 90° - \theta_o$, but decrease this figure outside this interval (Fig. 3-7.b). In order to keep the interval where the efficiency is optimized (i.e. $90° - 2.\theta_o$) large enough, θ_o should be chosen reasonably small (typically smaller than 20°). In this case the signals $S_0(\pm\theta)$ in Fig. 3-5.a see an impedance of $1/(\pm jB)$) in parallel with a smaller impedance of $Z_o^2/2R_L$ (at least 3 to 4 times smaller), which justifies the assumption that i_B is very small with respect to i_1 used to transform the circuit (a) to (b) in Fig. 3-5.

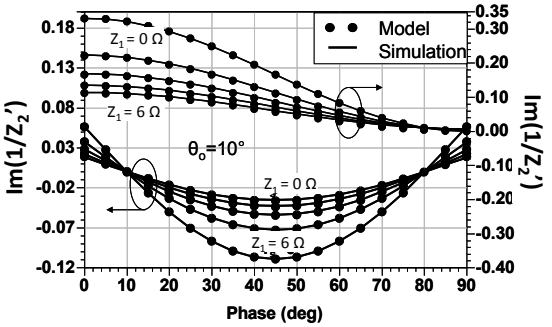

Fig. 3-6: The simulated and calculated imaginary and real part of Y'$_2$ versus θ with Z_1 varying from 0 to 6 Ω and B calculated for θ_o =10.

3.4 Validation of the proposed model

To verify the accuracy and the limits of the developed expressions, the imaginary and the real parts of $Z'_2(\theta)$ for the circuit in Fig. 3-5 are simulated using ADS and compared with the ones calculated using (3-34) for a relatively small θ_o. The results, shown in Fig. 3-6, illustrate the excellent agreement between the theory and the simulation. The simulated and calculated P_{out} and η_N for different values of Z_1 and B are shown in Fig. 3-7. The results of the proposed model and ADS simulations are practically the same for small values of θ_o. The relative error starts to be significant only for θ_o higher than 15 and for higher value of power back off.

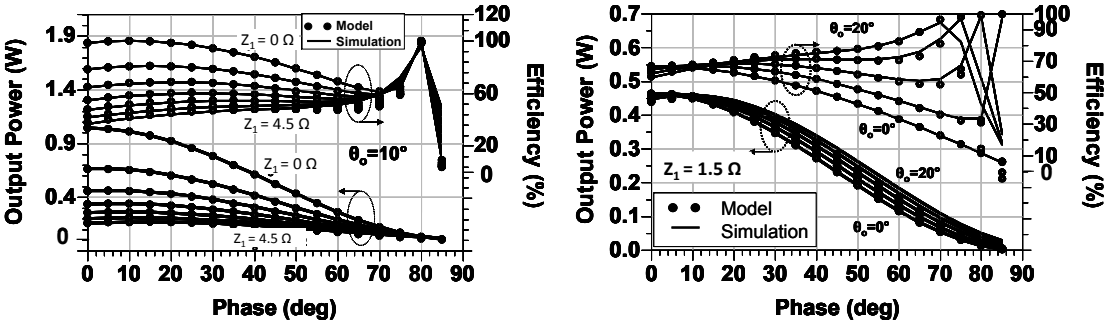

Fig. 3-7: Simulated and calculated output power and normalized efficiency (η_N) versus phase (θ) with a) Z_1 varying from 0 to 4.5 Ω with a step of 0.75 Ω, b) B varying from 0 to 0.1 (i.e. θ_o varying from 0° to 20° in steps of 5°).

3.5 Losses consideration in outphasing power combiner

Another parameter that impacts significantly the performances of outphasing PA and that will be added to the model is the losses in the combiner. Fig. 3-8 shows a simple representation of one branch of outphasing combiner. The characteristic impedance of the two $\lambda/4$ TLs, constituting the combiner, is Z_o ($Z_o = (L/C)^{0.5}$). The distributed impedances r_s are added to consider the effect of the inductors losses [7]. In fact, inductors exhibit a limited quality factor due to metal wire resistance, capacitive coupling and magnetic coupling to the substrate. These detrimental effects are exacerbated in the case of on-chip planar inductors. Despite the recent intensive research effort, the Q of monolithic inductors has been limited to less than 10 in modern CMOS technology [7]. This value can be improved to around 20 if an ultra-thick top metal is used.

In ideal case (i.e. $r_s = 0$), the impedance seen at the input of the $\lambda/4$ TL (Z_i) is equal to $Z_o^2/2R_L$. If we consider r_s (circuit (a) in Fig. 3-8), the expression of this input impedance is very hard to estimate. Without this relation, it is impossible neither to design the lumped elements of the $\lambda/4$ TL nor to anticipate the phase-to-power transfer function of the transmitter. An alternative method is to investigate the possible circuit transformations that would simplify the mathematical treatment and enable a compact model. For this we propose to demonstrate that after some valid approximations, the circuit (a) can be represented by a parasitic resistance in series with an ideal TL and thus, replaced by the circuit (b). In this case, the input impedance would be equal to r_e in series with $Z_o^2/2R_L$.

First, consider the general circuit (a) in Fig. 3-8. This TL is realized using (n-1) units. If n-1 is an odd number and if the electrical length of each unit is $\lambda/4$, the total electrical length of (a) will be also $\lambda/4$. In this case, the input impedance of this circuit can be written as

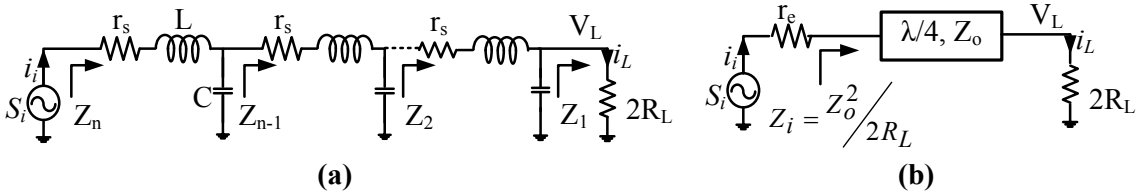

Fig. 3-8: a) Transmission line and b) its model for Chireix-LINC.

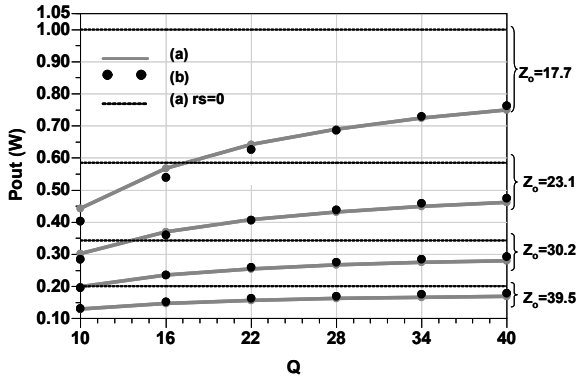

Fig. 3-9: Simulated output power of the circuits of Fig. 3-8 (a and b) with Q varying from 10 to 40 and Z_o varying from 17.7 Ω to 39.5 Ω .

$$Z_n = r_s + \frac{Z_o^2}{Z_{n-1}} = r_s + Z_o^2\left(r_s + \frac{Z_o^2}{Z_{n-2}}\right)^{-1}. \tag{3-39}$$

If we assume that r_s is very small compared with Z_o^2/Z_{n-2} (which is in general the case) and by using Taylor development of (3-39) we can demonstrate that

$$Z_n = r_s + Z_{n-2}\left(1 - r_s\frac{Z_{n-2}}{Z_o^2}\right). \tag{3-40}$$

Now, consider (without loss of generality) a three elements $\lambda/4$ TL (i.e. $n = 4$). In this case, we have

$$Z_{n-2} = Z_2 = r_s + \frac{Z_o^2}{2R_L}, \tag{3-41}$$

$$Z_n = Z_4 = 2r_s - \frac{r_s}{Z_o^2}\left(r_s + \frac{Z_o^2}{2R_L}\right)^2 + \frac{Z_o^2}{2R_L}. \tag{3-42}$$

The analysis of (3-42) reveals that the circuit (a) is equivalent to the circuit (b) with

$$r_e = 2r_s - \frac{r_s}{Z_o^2}\left(r_s + \frac{Z_o^2}{2R_L}\right)^2 . \qquad (3\text{-}43)$$

To verify the accuracy of this transformation, the output power P_{out} (i.e. Mag(I_L)×Mag(V_L)/2) versus Q is simulated for the circuits (a) and (b). The results are shown in Fig. 3-9. In the simulations, S_o, f_o, n and R_L are assumed to be equal to 2.5 V, 2.5 GHz, 4 and 50 Ω, without loss of generality. L, C and Q are calculated from f_o, Z_o and r_s as

$$L = \frac{Z_o}{4nf_o} \;\; ; \;\; C = \frac{1}{Z_o 4nf_o} \;\; and \;\; Q = \frac{L\omega}{r_s} . \qquad (3\text{-}44)$$

The simulations were achieved for Q varying from 10 to 40. Z_o is varied from 17.7 to 39.5 Ω in order to have P_{out} (rs = 0) varying from 0.2 to 1 W. As illustrated, a quasi-perfect matching between the model and the original circuit is found in all the tested configurations. To illustrate the detrimental impact of the inductor losses, the output power in the ideal case (i.e. r_s = 0) is also shown in the same figure. As expected, the more the required output power is high (e.g. 1 W) the more r_s is detrimental. For instance in the case of Q equal to 10 and Z_o equal 17.7 Ω, the output power deteriorates by more than 40 % compared to the value with Q equal to 40 and by more than 55 % compared to the ideal case.

3.6 Validation of the proposed model

In the following analysis, we will see how the transformation made in Fig. 3-8, simplifies the theoretical analysis of the LINC transmitter without any loss in the accuracy. Fig. 3-10 illustrates an equivalent Chireix-based LINC topology. The impedance r_e include the distributed losses of the TLs inductors. Its value versus Q is calculated from (3-43) and (3-44). The impedances seen at the input of the two ideal $\lambda/4$ TLs at θ = 0 are equal to $Z_o^2/2R_L$. Notice that the determination of this input impedance is only possible because of the transformation that eliminate the distributed r_s (i.e. (a) to (b) of Fig. 3-8). As a consequence, outphasing PA can be simplified to the circuit shown in Fig. 3-10, where the two signals differentially drive the

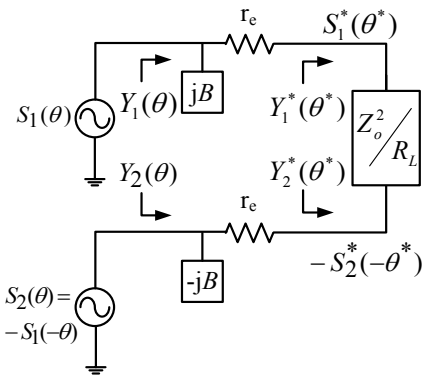

Fig. 3-10: Equivalent schematic of LINC.

impedance Z' ($Z' = 2r_e+Z_o^2/R_L$). In this case, mathematical treatment of the system is easier, and compact analytical expressions of $Y_{1,2}$ can be derived as

$$Y_{1,2}(\pm\theta,\pm B) = \frac{1}{Z'}\frac{S_1(\theta)+S_2(-\theta)}{S_{1,2}(\pm\theta)} \pm jB = \frac{1}{Z'}\left[2\cos^2(\theta) \pm j\left(B.Z' - \sin(2\theta)\right)\right] \tag{3-45}$$

with Z' is

$$Z' = 2r_e + \frac{Z_o^2}{R_L} = 4r_s - \frac{2r_s}{Z_o^2}\left(r_s + \frac{Z_o^2}{2R_L}\right)^2 + \frac{Z_o^2}{R_L}. \tag{3-46}$$

The admittances $Y^*_{1,2}$ and the voltage $S^*_{1,2}$ shown in Fig. 3-10 are calculated from (3-45) as

$$Y^*_{1,2}(\pm\theta) = \left(\frac{1}{Y_{1,2}(\pm\theta, B=0)} - r_e\right)^{-1}, \tag{3-47}$$

$$S^*_{1,2}(\pm\theta) = \left(1 - r_e Y_{1,2}(\pm\theta, B=0)\right)\ S_{1/2}(\pm\theta). \tag{3-48}$$

The power delivered to the load can be determined by simulation as

$$P_{out} = Mag(I_L)Mag(V_L)/2. \tag{3-49}$$

It can be also calculated theoretically as

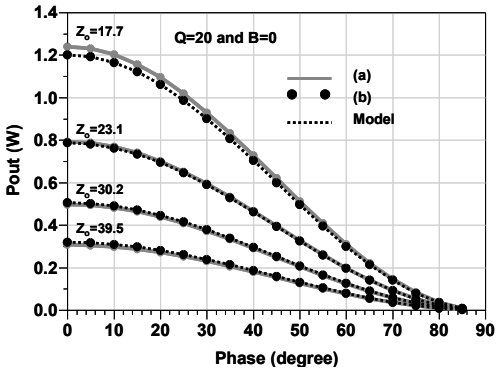

Fig. 3-11: Output power vs phase, simulated using (3-49) for a LINC with the circuit (a) and (b) of Fig. 3-8 as TLs and calculated (Model) using (3-50) with $Q = 20$, $B = 0$ and Zo varying from 17.7 to 39.5.

$$P_{out} = Mag^2\left(S^*_{1,2}(\pm\theta)\right)\mathrm{Re}\left(Y^*_{1,2}(\pm\theta)\right). \tag{3-50}$$

The efficiency of the system can be determined by simulation or theoretically by using the following relation

$$\eta = \frac{P_{out}}{P_{in}} = \frac{Mag^2\left(S^*_{1,2}(\pm\theta)\right)^2\,\mathrm{Re}\left(Y^*_{1,2}(\pm\theta)\right)}{{S_o}^2 Mag\left(Y_{1,2}(\pm\theta)\right)} \times 100\ (\%)\ . \tag{3-51}$$

The simulated and calculated P_{out} for different values of Z_o is shown in Fig. 3-11. The curves (a) represents the simulated output power using (3-49) for a LINC with a TL without any approximation (i.e. (a) of Fig. 3-10). The curves (model) are the calculated P_{out} using (3-50). As illustrated, the results of the proposed model and the ADS simulations are practically the same. It is worth noting that the intrinsic nonlinearity of Chireix combiners, widely cited in the literature [2], [8] and [9] is mainly due to the difficulty to anticipate their phase-to-power transfer function. Consequently, the developed analytical expressions which describes this transfer function and includes the losses in the power combiner, is very important for the linearity of the operations. With the help of these relations, it is possible to reconstruct the envelope variation at the output of the transmitter by digitally controlling the phase in the baseband and thus, to make the pre-distortion algorithms more accurate.

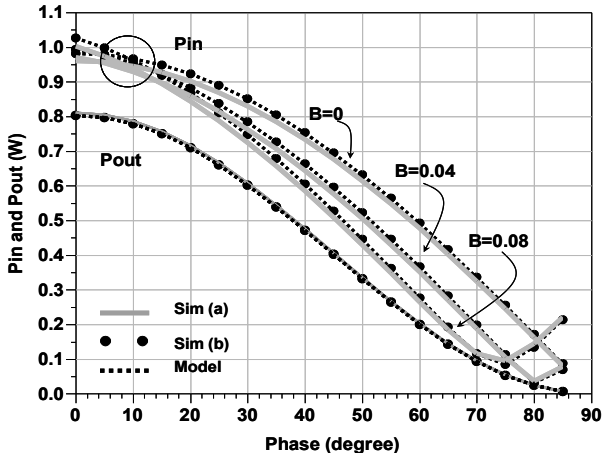

Fig. 3-12: Output and input power vs phase for a LINC with the circuit (a) and (b) of Fig. 3-8 as TLs and calculated (Model) using (3-50) with Q = 20, Zo = 22.8 and B varying from 0 to 0.08.

Fig. 3-12 shows the Output and input power vs phase. The curves (a) represents the simulated input/output power for a LINC with a TL without any approximation (i.e. (a) of Fig. 3-8). The curves (model) are the calculated P_{out} using (3-50). The matching here also is quasi perfect. As illustrated, adding shunt susceptance elements has a noticeable impact only on P_{in} and not on P_{out}. In fact, the more B is high the more P_{in} decreases over practically all the values of the phase. This diminution improves the efficiency as illustrate in Fig. 3-13.

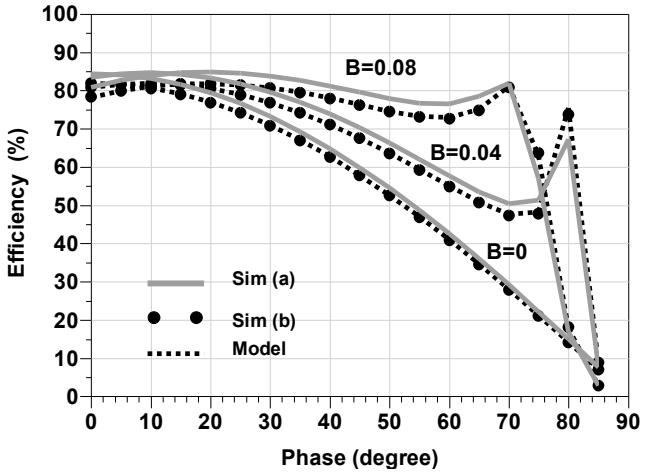

Fig. 3-13: Simulated and calculated efficiency with Q = 20, Zo = 22.8 and B varying from 0 to 0.08.

3.7 Summary

This chapter presented the theoretical analysis of outphasing combiners including isolating and non-isolating ones. We showed how the reflection in Chireix combiner increases the complexity of the analysis and a simplified solution was presented. This solution applies for a relatively small θ_o (3-21) which is typically chosen between 5° and 20°. In the section 3.5, we mainly focused on modeling the losses in TLs that is useful principally in lossy on-chip TLs and inductors. As a result, a compact model has been derived. This analytical model provides a promising solution for LINC design automation and optimization with different PA topology candidates and power combiner parameters. The linearity and efficiency of the system has been re-examined in light of the new analytical expressions of the model. The developed mathematical representations of the efficiency and of the nonlinear phase-to-power transfer function are also particularly useful to optimize the power consumption and to build pre-distortion algorithms for outphasing transmitters.

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4 Modified LINC architecture for base station applications

Efficiency enhancement for cellular base station transmitters is a continuing effort in telecommunication industry. High data rate increases the peak-to-average power ratios of the transmitted signals, which increases the power consumption and decreases the average efficiency. In consequence, new architectures are required to address this dilemma. Chireix outphasing transmitter, which was discussed in previous chapter, is one possible candidate.

This chapter, mainly focuses on designing relatively high power (2 to 10 W) outphasing PAs for base station applications. Two approaches are proposed to design efficient power combiner, considering the interaction between the power combiner and the PA. First, a "Zero Capacitive Load" concept is introduced. In this method, the power combiner is designed to provide zero capacitive load at the input of the power combiner for the whole operating region. We will show that with this criteria the efficiency will be improved significantly compared to the classical LINC. Second approach, provides a relatively compact design utilizing reduced size λ/m TL (m>4) instead of conventional "quarter-wavelength" combiners. The theoretical analyses are followed by simulation and experimental results at 900 MHz.

4.1 Variable reactive load in LINC

A comprehensive analysis of LINC was presented in chapter 3. From equation (3-25), the admittance Y (i.e. $1/Z(\theta^*)$) at the input of the power combiner shown in Fig. 4-1 can be expressed in terms of θ^* as [1]-[3]

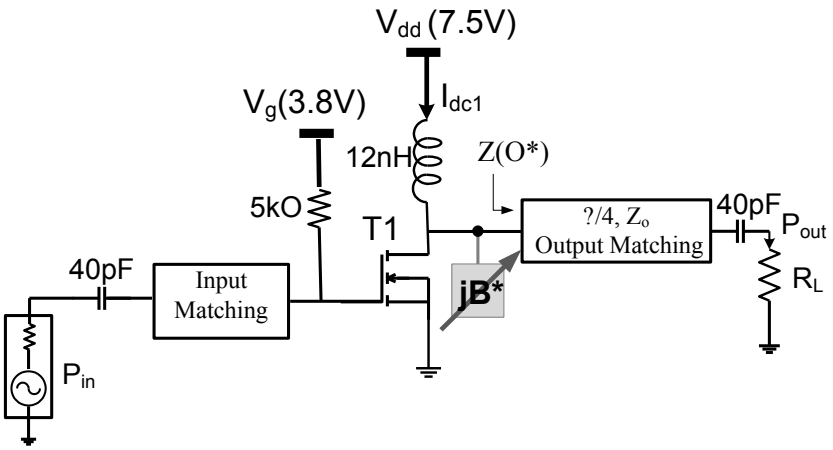

Fig. 4-1: Schematic of the PA designed to be used in the LINC Tx.

$$Y(\pm\theta^*) = \frac{R_L}{Z_o^2}\left[2\cos^2\left(\theta^*\right) \pm j\left(B.\frac{Z_o^2}{R_L} - \sin(2\theta^*)\right)\right]. \qquad (4\text{-}1)$$

Equation (4-1) shows that without the shunt susceptance elements (B = 0 S), lossless power combiner (LPC) presents a capacitive load to the first PA and an inductive load to the second. The role of the shunt elements, B given by (3-21), is to cancel these reactive loads at a predefined angle θ_o [1]. With this new configuration, the output power reaches its maximum around $\theta^* = \theta_o$ where there is no reactive power loss. In order to optimize this maximum power, the output impedance of the circuit driving the LPC should be matched to the magnitude of $Z(\theta_o)$ (i.e. $Z_o^2/[2R_L \cos^2(\theta_o)]$). When we add the stubs ($\pm B$) to LPC, the magnitude of Y_1 becomes even smaller at $\theta^* = \theta = \theta_o$ and at $\theta^* = \theta = 90° - \theta_o$ where $|Y|$ equals $2R_L \cos^2(\theta_o)/Z_o^2$ instead of $2R_L \cos(\theta_o)/ Z_o^2$. Therefore, the efficiency exhibits maximums at these two specific angles [4].

In order to verify the supremacy of Chireix-LINC at circuit level, the PA of Fig. 4-1 is designed. A 900 MHz LDMOS (ST PD84001) is used as RF power transistor, without loss of generality. The output matching network is designed to match the output transistor impedance (5 Ω) to R_L (50 Ω) and to have an electrical length of $\lambda/4$. The objective of the variable shunt susceptance element (jB^*) is to emulate the side effect of the reactive load introduced by the Chireix LPC.

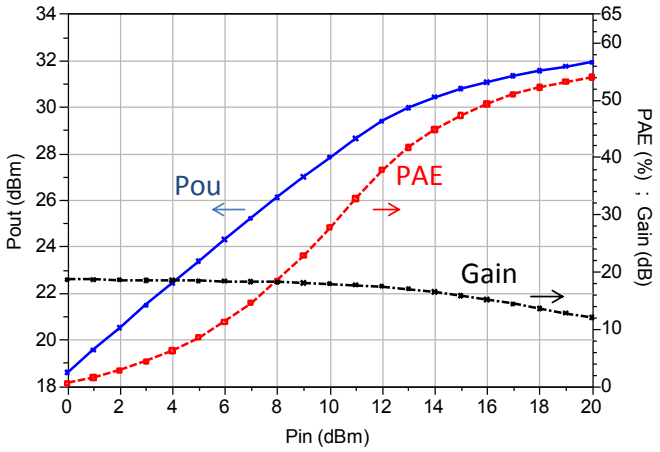

Fig. 4-2: Simulated output power and power added efficiency of the PA with V_{dd} = 7.5 V and P_{in} varying from 0 to 20 dBm.

Fig. 4-2 shows the simulated output power (P_{out}), power added efficiency (PAE) and gain of the PA with P_{in} varying from 0 to 20 dBm with B equal to zero. The simulations demonstrate the contrast between the high efficiency in the saturated mode (up to 55 %) and its sharp drop in power back-off mode. Fig. 4-3 shows the simulated P_{out} and PAE of the PA for different values of B*. The simulations illustrate the contradictory effect of the shunt element depending on the sign of its susceptance. For B* equal to zero, the simulated values of PAE and P_{out} are 45 % and 1.35 W. However, when B* is positive (a capacitive shunt element) the P_{out} and efficiency are decreased significantly (e.g. PAE degrades to 27 % at B* = 0.1 S,). In contrast, an inductive

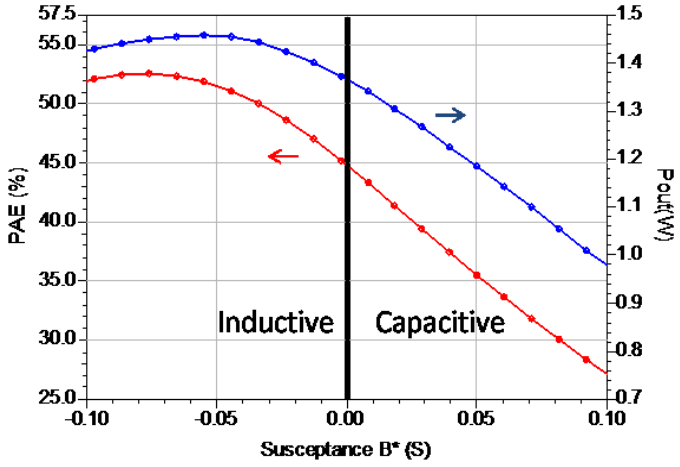

Fig. 4-3: Simulated P_{out} and PAE of the PA shown in Fig. 4-1 with V_{dd} = 7.5 V, P_{in} = 16 dBm and B* varying from -0.1 S to 0.1 S.

shunt element results in slight improvement of the overall performances (e.g. *PAE* and P_{out} improves to 53 % and 1.45 W for $B^* = -0.1$ S). This behavior is explained by the fact that both the capacitive shunt element and the parasitic drain to bulk capacitance of the power transistor (C_{db}) need to be charged to $2V_{dd}$ and discharged to zero during the PA operation. This results in power dissipation, thereby, degrading *PAE*. This degradation increases with the frequency and the value of the parasitics. In contrast, the inductive shunt element compensates the inherent parasitic capacitance (C_{db}) and avoids the power dissipation required for its charging-discharging. Note that the degradation due to capacitive load, is much more important than the improvement with inductive load.

The PA in Fig. 4-1 is used to build the Chireix Outphasing transmitter. The final circuit is shown in Fig. 4-4. A third $\lambda/4$-TL (TL2) is added to have an electrical length of $-\lambda/4$ between the transistors ($T_{1,2}$) and the load (R_L) because a $\pm\lambda/4$ electrical length is required in Chireix power combiner[4]. It can be demonstrated that, in this configuration, the admittance Y_3 (i.e. $1/Z_3$) is proportional to Y_1 and can be expressed similarly to (4-1) as

$$Y_3(\pm\theta^*) = \frac{Z_{o2}^2}{Z_{o3}^2}\frac{R_L}{Z_{o1}^2}\left[2\cos^2(\theta^*) \pm j\left(B.\frac{Z_{o1}^2}{R_L} - \sin(2\theta^*)\right)\right] \qquad (4\text{-}2)$$

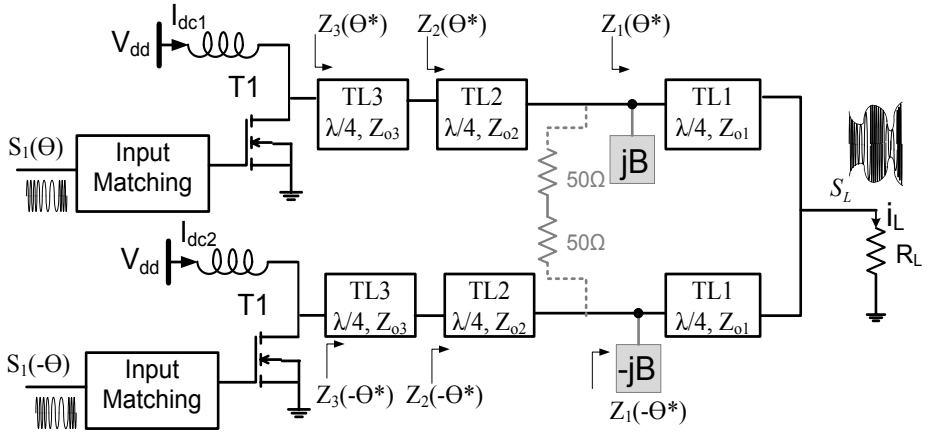

Fig. 4-4: Schematic of the Chireix-LINC using the PA of Fig. 4-1. The Chireix combiner is transformable to Wilkinson combiner by adding two 50 Ω resistors.

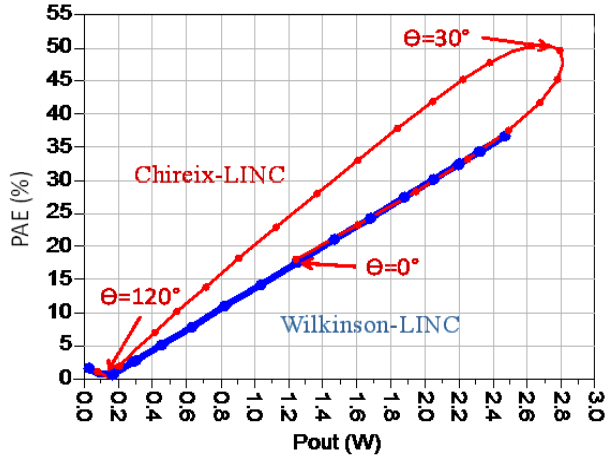

Fig. 4-5: Simulated *PAE* vs P_{out} of Chireix-LINC and Wilkinson-LINC with V_{dd} = 7.5 V, P_{in} = 18 dBm and θ varying from 0 to 120°.

In order to match Z_{out} of TL2 to $Z_{o1}^2/(2R_L \cos^2(\theta_o))$ (the optimal value for power), the characteristic impedance Z_{o2} is chosen to be $50/(\sqrt{2}\cos(\theta_o))$. Without loss of generality, the value of θ_o and thus B are chosen to be 30° and 9 mS respectively. The Chireix combiner is designed to be transformable to Wilkinson combiner by adding two 50 Ω resistors at its inputs, as shown Fig. 4-4. During the operation of Wilkinson Outphasing TX, the impedances seen by the PAs and thus the magnitude of their RF output current and dc power consumption are almost constant independently of the Outphasing angle. In fact, in power back-off mode the power that is not delivered to the load is dissipated through the 50 Ω resistors. Consequently, the more P_{out} decreases the more *PAE* decreases. The comparative study of the Wilkinson and Chireix results, will be used to analyze the trade-off between the detrimental effect of the variable reactive load and the benefits of the lossless nature of the power combiners.

Fig. 4-5 shows the simulated *PAE* versus P_{out} of the Chireix-LINC, when the Outphasing angle (θ) is varied from 0° to 120°. The maximum power (~ 2.8 W) is achieved around the impedance matching condition $\theta = \theta_o$ = 30° and a minimum around 90°+30°. The results when the Chireix is transformed to Wilkinson by adding the two 50 Ω resistors, are shown in the same figure. The transistor level simulations show that the performances of Chireix are not as high as the theoretical analysis predictions.

Fig. 4-6 shows the variation of the imaginary parts of the admittances $B_{1,2}$ seen by the two PAs (i.e. $B_1 = \text{imag}(1/Z_3(\theta^*)$ and $B_2 = \text{imag}(1/Z_3(-\theta^*))$, Z_3 is shown in Fig. 4-4). As expected, $B_{1,2}$

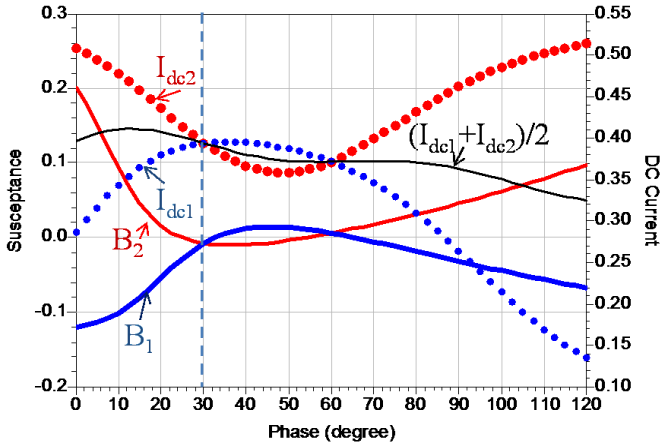

Fig. 4-6: Simulated imaginary parts of the admittances seen by the PAs ($B_{1,2}$) and the dc current consumed by the Chireix-LINC ($I_{dc1,2}$).

are cancelled at θ_o = 30° and 90° - θ_o = 60°. Between 30° and 120°, the range of interest, $B_{1,2}$ varies from – 0.1 S to 0.1 S. The dc currents ($I_{dc1,2}$) consumed by the two PAs are also reported. The results show a strong correlation between the variation of the reactive loads and the power consumptions of the PAs. When B increases and becomes positive (capacitive mode), the power consumption increases and when B decreases and becomes negative (inductive mode), the power consumption decreases. Similar to Fig. 4-3, this behavior is explained by the fact that both the capacitive load (B_2) and C_{db} need to be charged to $2V_{dd}$ and discharged to zero during the PA operation. This results in power dissipation in the second branch thereby, increasing I_{dc2}. In contrast, the inductive load (B_1) compensates the inherent parasitic capacitance and avoids the power dissipation which explains the I_{dc1} drop in Fig. 4-6. The total dc current consumed by the two PAs is also reported in Fig. 4-6. This current is practically constant, just like in Wilkinson Tx, which explains the similar performances of the two configurations illustrated in Fig. 4-5. Therefore, the benefit of the lossless nature of Chireix LPC is counterbalanced by the detrimental effect of its capacitive load in power back-off mode. Obviously, C_{db} can be compensated by two shunt inductors in series with dc-block capacitors at the output of the power transistors. Nevertheless, the quality factor of the inductors and the variability of their resonance frequency can have a destructive impact on P_{out} and PAE.

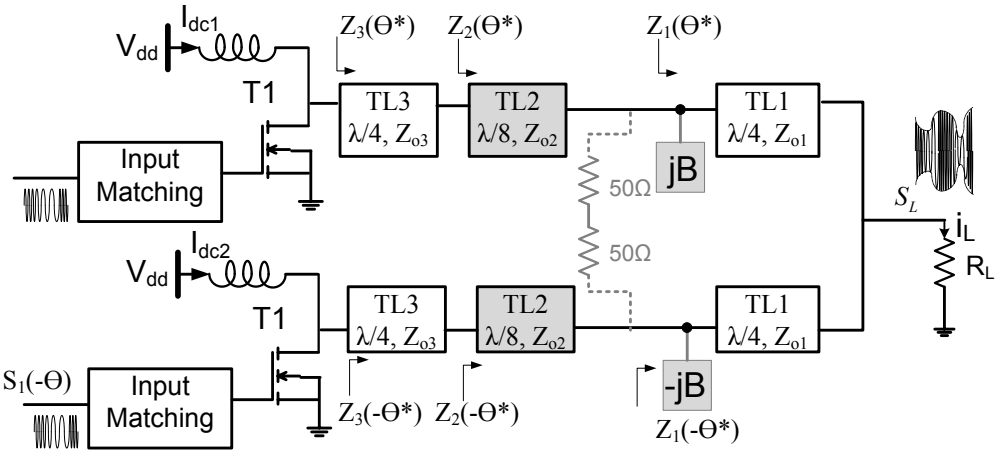

Fig. 4-7: Schematic of the proposed Z-LINC. The power combiner is transformable to Wilkinson by adding the two 50 Ω resistors.

4.2 Theoritical analysis of Zero-capacitive LINC (Z-LINC) concept

In order to recover the exceptional theoretical performances of LINC TXs, an ideal power combiner have to provide a zero capacitive load to the PAs [5]. Fig. 4-7 shows a proposed architecture, referred to Z-LINC, which satisfies this condition. In fact, TL2 in Z-LINC, are designed to have an electrical length of $\lambda/8$ and thus their input admittances $Y_2(\pm\theta^*)$ can be defined as

$$Y_2(\pm\theta^*) = [Y_1(\pm\theta^*) + jY_{o2}]/[1 + j(Y_1(\pm\theta^*)/Y_{o2})] \tag{4–3}$$

where $Y_{o2} = 1/Z_{o2}$ is the characteristic conductance of TL2. The admittance Y_1 can be written as $G_1 + jB_1$, where G_1 and B_1, the input conductance and susceptance of TL1, are given respectively by the real and the imaginary part of (4-1). By expressing Y_2 as $G_2 + jB_2$ and separating the imaginary and real parts of (4–3), we can demonstrate that

$$G_2(\pm\theta^*) = [2G_1(\pm\theta^*)Y_{o2}^2]/[(Y_{o2} - B_1(\pm\theta^*))^2 + G_1^2(\pm\theta^*)] \tag{4-4}$$

$$B_2 = \frac{Y_{o2}(Y_{o2}^2 - {B_1}^2(\pm\theta^*) - {G_1}^2(\pm\theta^*))}{(Y_{o2} - B_1(\pm\theta^*))^2 + {G_1}^2(\pm\theta^*)} \tag{4-5}$$

In the same way, by expressing Y_3 as $G_3 + jB_3$, considering that Y_3 is equal to $(Z_{o3}{}^2\,(G_2{+}jB_2))^{-1}$ and separating its imaginary and real parts, we can demonstrate that

$$G_3(\pm\theta^*) = \frac{1}{Z_{o3}^2|Y_2|^2}\frac{2G_1(\pm\theta^*)Y_{o2}^2}{(Y_{o2} - B_1(\pm\theta^*))^2 + {G_1}^2(\pm\theta^*)}, \tag{4-6}$$

$$B_3(\pm\theta^*) = \frac{-1}{Z_{o3}^2|Y_2|^2}\frac{Y_{o2}(Y_{o2}^2 - {B_1}^2(\pm\theta^*) - {G_1}^2(\pm\theta^*))}{(Y_{o2} - B_1(\pm\theta^*))^2 + {G_1}^2(\pm\theta^*)}. \tag{4–7}$$

Equation (4–7) represents the susceptance of the reactive loads seen by the PAs in Z-LINC. In order to determine its nature (inductive or capacitive) we have to determine the sign of it. Therefore, G_1 and B_1 are replaced by the real and the imaginary part of (4-1). In addition, to be close to the matching condition we suppose that Z_{o2} and Z_{o1} are equal to R_L and $\sqrt{2}\,R_L$. With these transformations we can demonstrate that

$$B_3(\pm\theta^*) = \frac{Y_{o2}^3}{Z_{o3}^2|Y_2|^2}\frac{\overbrace{\left[\cos^4(\theta^*) + (0.5\sin(2\theta_o) - 0.5\sin(2\theta^*))^2 - 1\right]}^{F(\theta^*)}}{(Y_{o2} - B_1(\pm\theta^*))^2 + {G_1}^2(\pm\theta^*)}. \tag{4–8}$$

Equation (4–8) shows that $B_3(\pm\theta^*)$ have the same sign as the function $F(\theta^*)$. The values of the function F for θ^* varying from θ_o to $90° + \theta_o$, are calculated for different values of θ_o. As shown in Fig. 4-9, the function is negative in almost all the practical situations, which proves that the reactive loads seen by the PAs are inductive for both branches ($B_3(\pm\theta^*) < 0$).

This theoretical result is also demonstrated by circuit level simulations. Fig. 4-8 shows the variation of the imaginary parts of the admittances $B_{1,2}$ seen by the two PAs of Z-LINC ($B_1 = \text{imag}[1/Z_3(\theta^*)]$ and $B_2 = \text{imag}[1/Z_3(-\theta^*)]$). As expected, both B_1 and B_2 are negative in the whole range of interest (θ^* between 30° and 120°). The dc currents ($I_{dc1,2}$) consumed by the two PAs are also reported in Fig. 4-8. In contrast to the previous design (Fig. 4-6), the power consumptions of both PAs decreases when θ increases thereby, improving the *PAE* in power back-off mode.

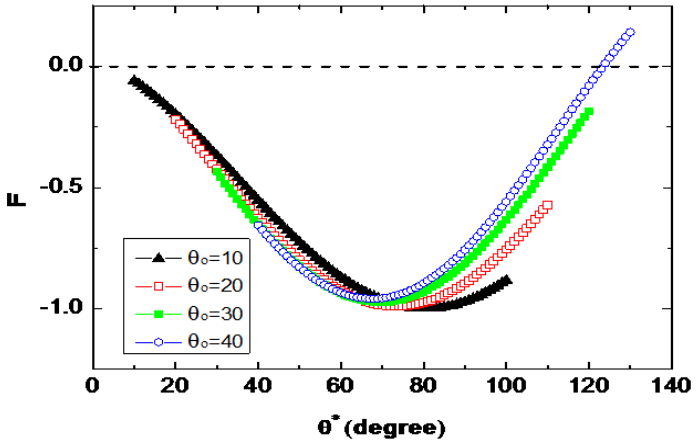

Fig. 4-9: Calculated values of the function F in (4–8) for θ* varying from θ_o to 90° + θ_o and θ_o equal to 10, 20, 30, and 40 degree.

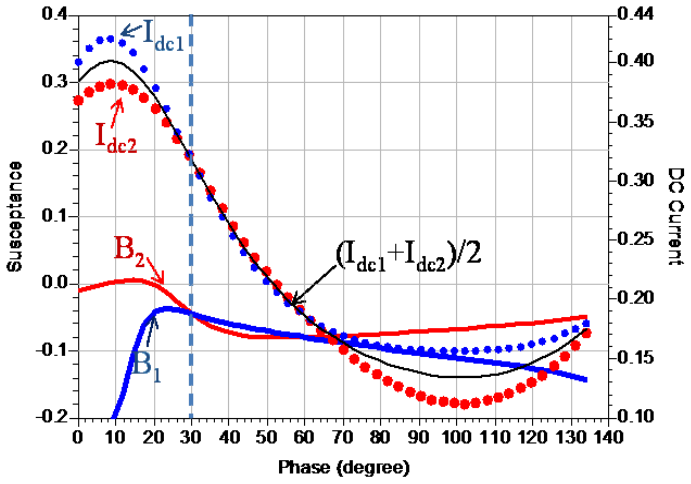

Fig. 4-8: Simulated imaginary parts of the admittances seen by the PAs ($B_{1,2}$) and the consumed dc currents in Z-LINC .

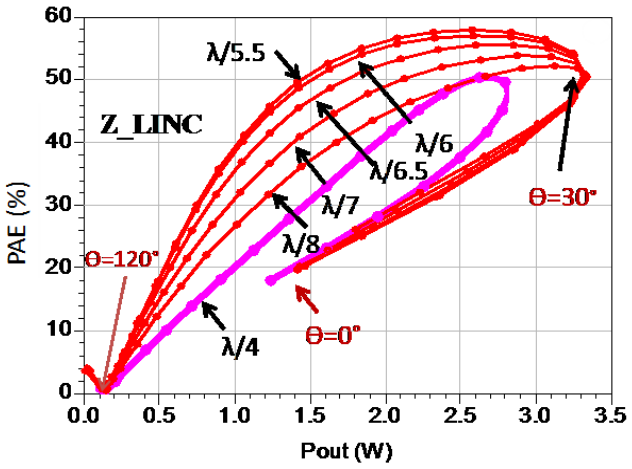

Fig. 4-10: Simulated *PAE* vs. P_{out} of Z-LINC with V_{dd} = 7.5 V, P_{in} = 18 dBm, θ varying from 0 to 120° with different values for TL2 electrical length.

Fig. 4-10 shows the simulated P_{out} and *PAE* of Z-LINC, when the θ is varied from 0° to 120°. As expected, the maximum power is achieved around $\theta = \theta_o = 30°$ (the impedance matching condition) and the minimum around 90° + 30°. The superior performance of Z-LINC compared to Wilkinson and Chireix based LINC (Fig. 4-5) is obvious. A significant improvement of the efficiency is achieved over a wide range of power back-off. The performances are improved more by the optimization of the electrical length of TL2. In this design the optimal value of TL2 is $\lambda/6$ as shown in Fig. 4-10. In addition, beyond $\lambda/5$ the performances degrade significantly in power back-off region.

4.3 Reduced size power combiner with shorter TLs

As it was shown in previous section, Z-LINC needs three TLs for each branch and the size of the TLs tends to be bulky and even prohibitive below *X*-band. Consequently, miniaturization techniques are necessary for a compact and cost effective implementation. In this section, we explain the impelemention of a 10-W, 900-MHz LDMOS outphasing PA using Z-LINC and TL reduced-size technique. A reduced size technique based on shorter TLs compensated by shunt capacitors has been proposed for hybrid couplers [6]. Nevertheless, it has been never used or tested for LPC.

The proposed LINC topology with a Chireix LPC is shown in Fig. 4-11. The λ/4-TL1 is designed to have 50 Ω as an input impedance at $\theta = 0$ (i.e. $Z_{o1}^2/(2R_L) = 50\ \Omega$) and thus, a characteristic impedance Z_{o1} of 70.7 Ω. The PAs in Fig. 4-11 are designed using 4-W, 900-MHz LDMOS (ST PD85004) as RF power transistors without loss of generality. TL3 is designed to match the output impedance of the transistors (~8 Ω) to 50 Ω and to make the PAs working close to class F mode (i.e. electrical length = λ/4). Avoiding the capacitive loading of the PAs, improves significantly the *PAE* while the power is backed-off. The curve TL2:λ/8 in Fig. 4-12 shows the simulated *PAE* versus P_{out} of Z-LINC and illustrates the superior performance of Z-LINC compared to the classical Chireix based LINC (i.e. TL2:λ/4 curve).

Another drawback of LPC is the bulky size of its λ/4 TLs. The size problem is exacerbated in LINC with class-F PAs, where a multitude of λ/4-TLs are used for the input/output matching networks of the two branches (Fig. 4-11). In order to achieve a reasonably compact design, the λ/4-TLs can be substituted by λ/8-TLs with a characteristic impedance of Z'_0 and two shunt capacitors (C') at its ends. We can demonstrate that the two configurations have the same admittance matrix if Z'_0 and C' are given by [7]

$$Z_0^{'} = \sqrt{2}Z_0 \ \ and \ \ C' = (2\pi . f_R \sqrt{2} Z_0)^{-1} \tag{4-9}$$

The technique is applied to the modified LINC PA of Fig. 4-11 [7]. The lengths of all TLs (LPC and the matching networks) are divided by two while shunt capacitors (given by (4-9)) are added to compensate the shorter electrical lengths. The new modified Z-LINC with some extra-

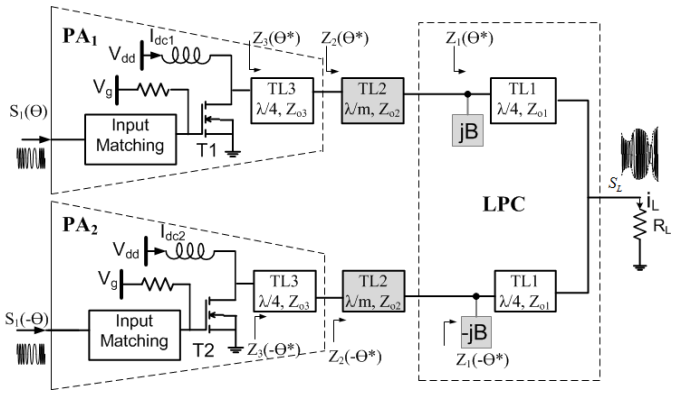

Fig. 4-11: Classical (m = 4 for TL2) and modified (m = 8 for TL2) LINC topologies.

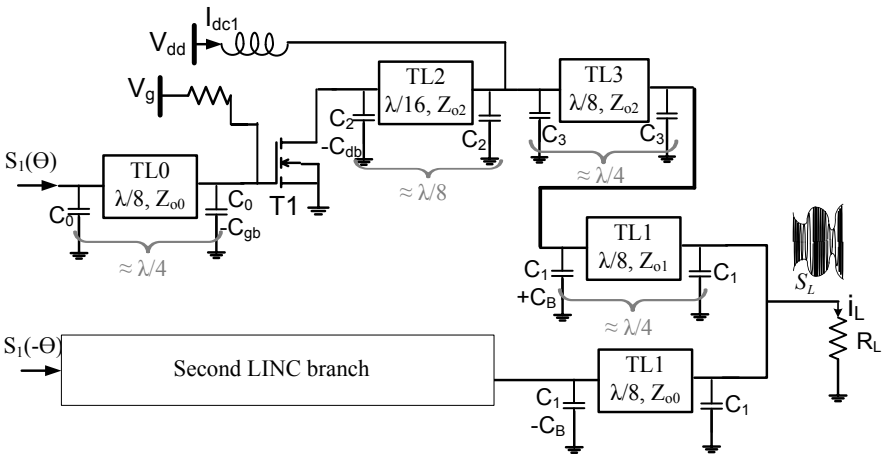

Fig. 4-12: Modified Z-LINC topology, implemented using shorter TLs and shunt capacitors.

changes motivated by practical design issues and simulation-based optimization, is shown in Fig. 4-12. In fact, it is impossible to connect the choke directly to the drain of the power transistors due to their large footprints. It is thus preferable to permute the TL2 and TL3 and put the shorter TL2 directly at the output of the transistors. Its size can be even divided by two or four ($\lambda/16$ or $\lambda/32$) with higher shunt capacitors, C', to emulate the required $\lambda/8$ TL. The parasitic capacitors, C_{db} and C_{gb}, are compensated by the shunt capacitors which are given by (4-9). In the same way, the stubs are replaced by $C_B = B/\omega$, and combined with the capacitors of the transformation, as illustrated in Fig. 4-13. The optimized *PAE* versus P_{out} of this new

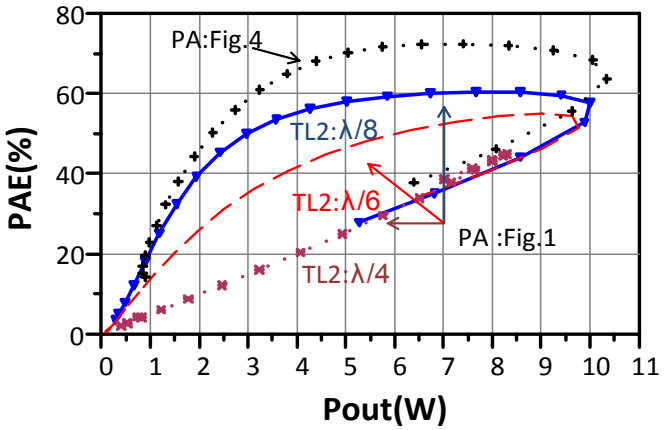

Fig. 4-13: Simulated *PAE* versus P_{out} of the circuit in Fig. for θ varying from 0 to 120° and with m = 4, 6, 8 (V_{dd} = 13.5 V, V_g = 3.8 V, P_{in} = 19 dBm and θ_o = 20°).

architecture is shown in curve PA of Fig. 4-13. A significant improvement of the *PAE* is achieved across a wide power back-off range.

4.4 Laboratory tests

In this part, first general layout considerations for PA PCB designs are explained. Then the measurement setup and the implemented circuits to validate the theoretical analysis of ZLINC and reduced-size power combiner are discussed.

4.4.1 Layout considerations

A good layout design, optimizes the overall area, thermal stress, and interaction between traces and components, considering design rules. In our case, the routing of the two branches are absolutely symmetric to minimize the mismatch. The voltage sources are placed close to the transistors to minimize the interconnection impedance and the conduction voltage drop across the PCB traces to achieve best voltage regulation, current transient response and system efficiency. Parallel capacitors with power supply are mounted on-board to provide high frequency currents of the PA.

The best news when a PA works is when its temperature is low. As power flows through the PA, both passive and active components generate heat. Thus, special care should be taken to properly route high-power paths. Resistance in copper traces can account for significant power loss and heat generation on a board if not used appropriately. Power combiner traces must be chosen as wide as possible, and thicker copper traces should be used. As a rule of thumb, the minimum trace width per amp for a 10°C rise in temperature, should be bigger than 10 mil for 1 oz copper.

Heat generated in passive components and especially the LDMOS transistors must be dissipated to the cooler ambient air around the devices. This heat is generally dissipated through the cupper surface of the PCB. Large copper planes are used to increase the available area on the PCB for heat dissipation. Vias are placed to maximize the heat transfer from the top layer to the bottom side. According to the simulation results (Fig. 4-13), the PA generates upto around 4 W power loss as heat at maximum output power. Thus, a 4-W heat sink placed at the back side

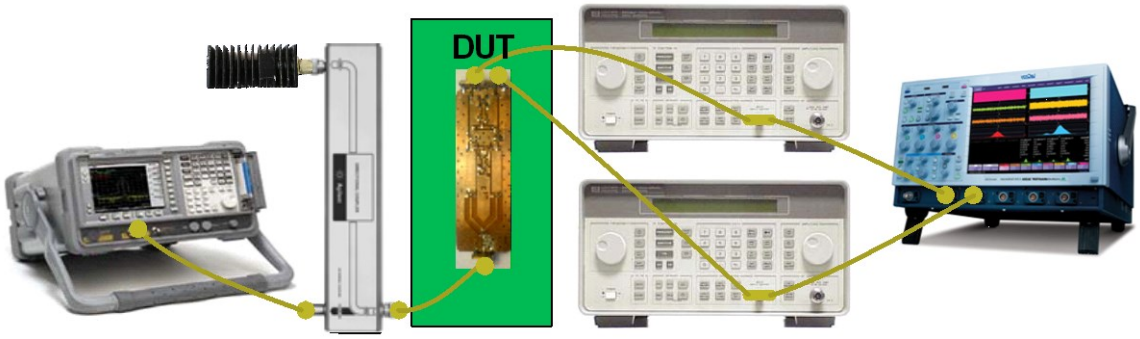

Fig. 4-14: Measurement setup used to measure LDMOS transistors modified LINC PAs.

of the 10-W PA's PCB to remove heat from the circuit and distribute it to the ambient air. Furthermore, silica gel is used to decrease the thermal resistivity and thus, ease of heat transfer between the heat sink and the bottom layer.

4.4.2 Measurement setup

Fig. 4-14 shows the measurement setup which consists of two coupled Agilent 8648C Synthesized RF Signal Generators to generate input signals. The phase difference of the input signal is measured by a Lecroy WaveMaster 8000A oscilloscope. The output signal of the device under test (DUT) is attenated by using a -30dB directional coupler and measured by an Agilent 4404B spectrum analyzer. Another port of directional coupler is connected to a 20-W air-cooled matched load to dissipate output power as heat.

4.4.3 Measurement results of the 2-W PAs

To validate experimentally the Z-LINC concept, a prototype (circuit of Fig. 4-7) was fabricated using two LDMOS power transistors (PD84001). An FR4 substrate with $\varepsilon_r = 4.8$ and a thickness of 0.51 mm was used for the printed circuit board (PCB). The matching circuits as well as the combiner are designed using micro-strip lines. The compensating susceptance elements are implemented using a shunt inductor (27 nH) and capacitor (1 pF). A photo of

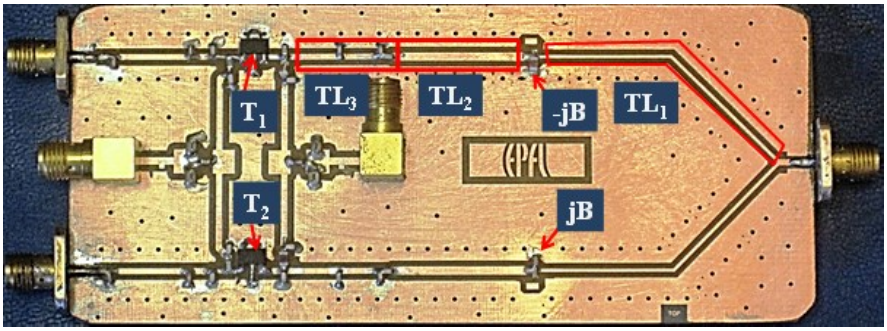

Fig. 4-15: Photo of the Z-LINC prototype.

Z-LINC prototype is shown in Fig. 4-15. The option $\lambda/8$ for TL2 was chosen on this prototype. For comparison, the classical Chireix and Wilkinson LINC (Fig. 4-4 with and without the 50 Ω resistors) were fabricated using the same components and substrate. Fig. 4-16 shows measured P_{out} and PAE of Z-LINC when the θ is varied. Three input powers (14 dBm, 16 dBm, and 18 dBm) are tested. For P_{in} = 18 dBm, a maximum P_{out} of 2.8W with a PAE of 58 % is achieved. The plots demonstrate the double functionality of the circuit. First, we can vary continuously the output power by changing the Outphasing angle θ at the input and thus, we can realize any kind of complex modulation (e.g. WCDMA or LTE). In parallel, we can step down the maximum output power (e.g. from 3 to 1 W depending on the distance from the base station) by decreasing the value of P_{in} (e.g. from 18 to 14 dBm) while keeping an optimized overall efficiency. The

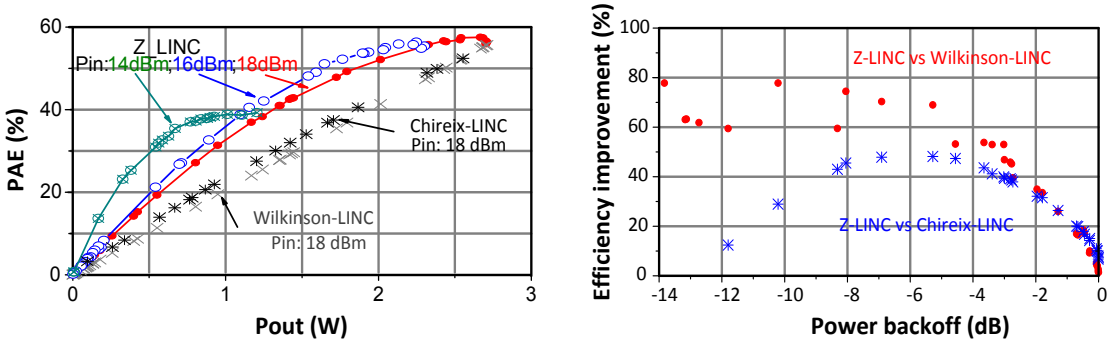

Fig. 4-16: a) Measured PAE vs. P_{out} of Z-LINC for P_{in} = 14, 16 and 18 dBm. The measured results of Wilkinson-LINC and Chireix-LINC are also reported. b) Relative efficiency improvement ($\Delta PAE/PAE$) of Z-LINC with respect to the classical Chireix and Wilkinson LINC with P_{in} = 18 dBm.

measurement results are in line with the simulations and can be improved more by optimizing the electrical length of TL2 (Fig. 4-10). A significant efficiency improvement ($\Delta PAE/PAE$) of around 50 to 70 % is reported over a wide range of power back-off when we use Z-LINC instead of Chireix or Wilkinson.

To examine the idea of optimizing TL2 (Fig. 4-10), three PCBs are designed with variable TL2 lengths (Fig. 4-17). Each circuit is measured with maximum length of TL2 and then it is cut and soldered to a shorter length. Moreover, the circuits benefits from shorter TLs ($\lambda/8$ and $\lambda/16$ for circuit (b) and (c) respectively) at input and output stages of the LDMOS transistors. The results in Fig. 4-18 shows an agreement with the simulation (Fig. 4-10) with respect to the TL2 length variation. The measurements demonstrate $\lambda/5.7$ as the optimum value for TL2. With regard to the shorter TLs, the measured efficiencies versus output power do not indicate any significant difference. In other words, by adding capacitors we save PCB area significantly without sacrificing performance.

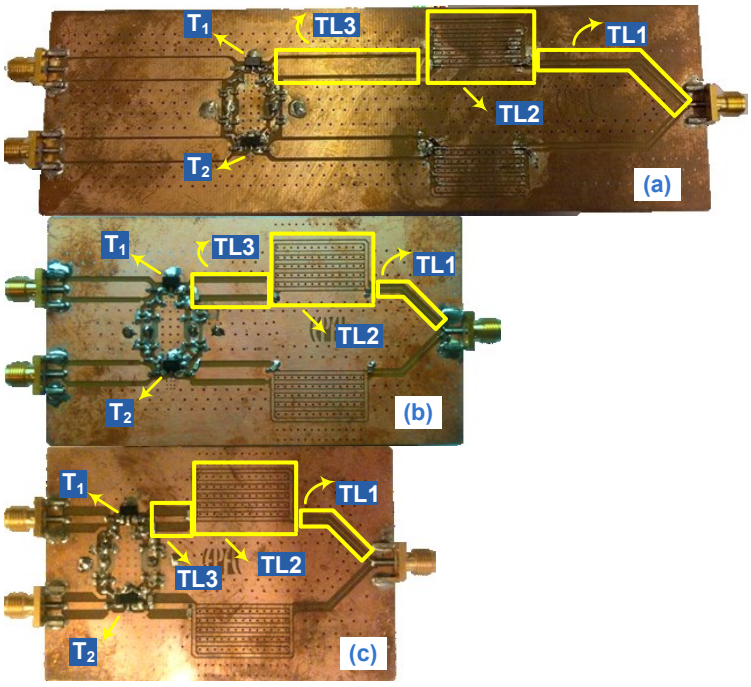

Fig. 4-17: Z-LINC prototypes with variable TL2 and shorter TL as input and output stages of LDMOS transistors (T_1 and T_2) respectively for circuits (a), (b) and (c) .

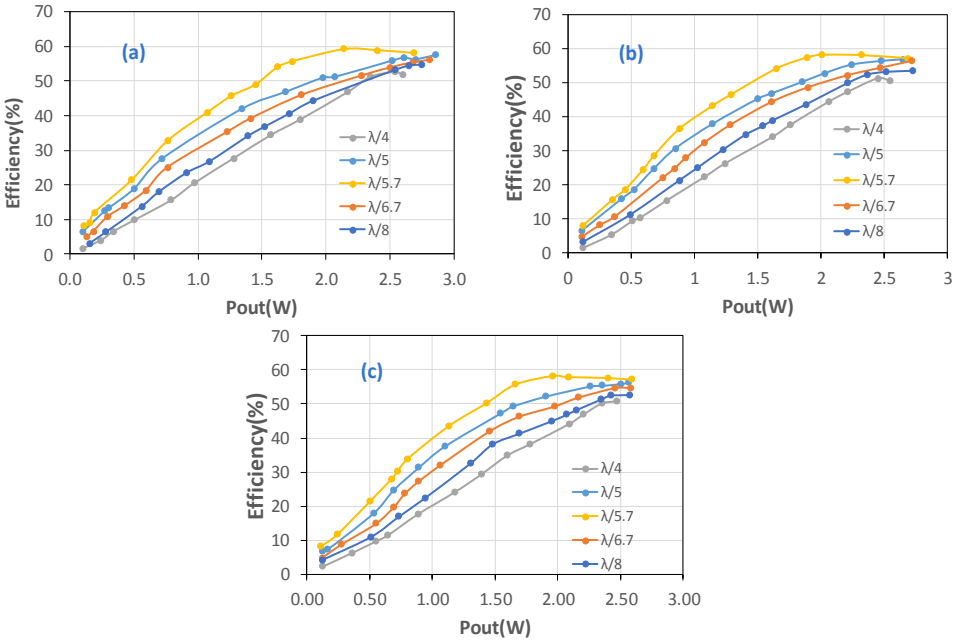

Fig. 4-18: Measured efficiency versus output power for the prototypes shown in Fig. 4-17.

4.4.4 Measurement results of the 10-W PA

The circuit shown in Fig. 4-12, was fabricated using two LDMOS power transistors (ST PD85004). The matching circuits as well as the combiner are designed using microstrip lines and lumped components. An FR4 substrate with $\varepsilon_r = 4.8$ and a thickness of 0.51 mm was used as PCB. The photo of the fabricated prototype is shown in Fig. 4-19.

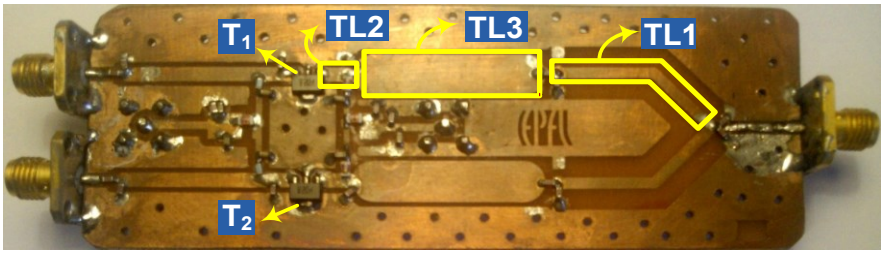

Fig. 4-19: Photo of Z-LINC prototype with shorter TLs.

Fig. 4-20.a shows the measured *PAE* versus input Outphasing angle (θ) for P_{in} equal to 19 dBm. A maximum P_{out} of 9.33 W with a *PAE* of 70 % is achieved at $\theta = 20°$. The minimum P_{out} is 9 mW for θ=110°, thereby demonstrating a wide dynamic range of ~30dB for P_{out}. The broadband capability of the system is illustrated in Fig. 4-20.b shows the measured P_{out} as a function of frequency. The -3dB bandwidth is around 300 MHz. The continuous variation of the output power versus θ and its bandwidth demonstrates the potential ability of the system to generate any kind of complex modulation (e.g. WCDMA or LTE). Fig. 4-20.c illustrates the measured phase error which is quite small (8° as maximum absolute error). Fig. 4-21 shows the measured *PAE* at 900 MHz versus P_{out}. The measured *PAE* at 3 and 6 dB power back-off are 63 % and 50 % respectively. The reference curves, Ref. 1 and Ref. 2, are calculated respectively by assuming that the efficiency is proportional to P_{out} (like in the ideal class A) and proportional to the square root of P_{out} (like in the ideal class B). Ref. 3 shows measured *PAE* versus P_{out} when the two PAs are designed to work in Class B and the P_{out} is varied by sweeping the input

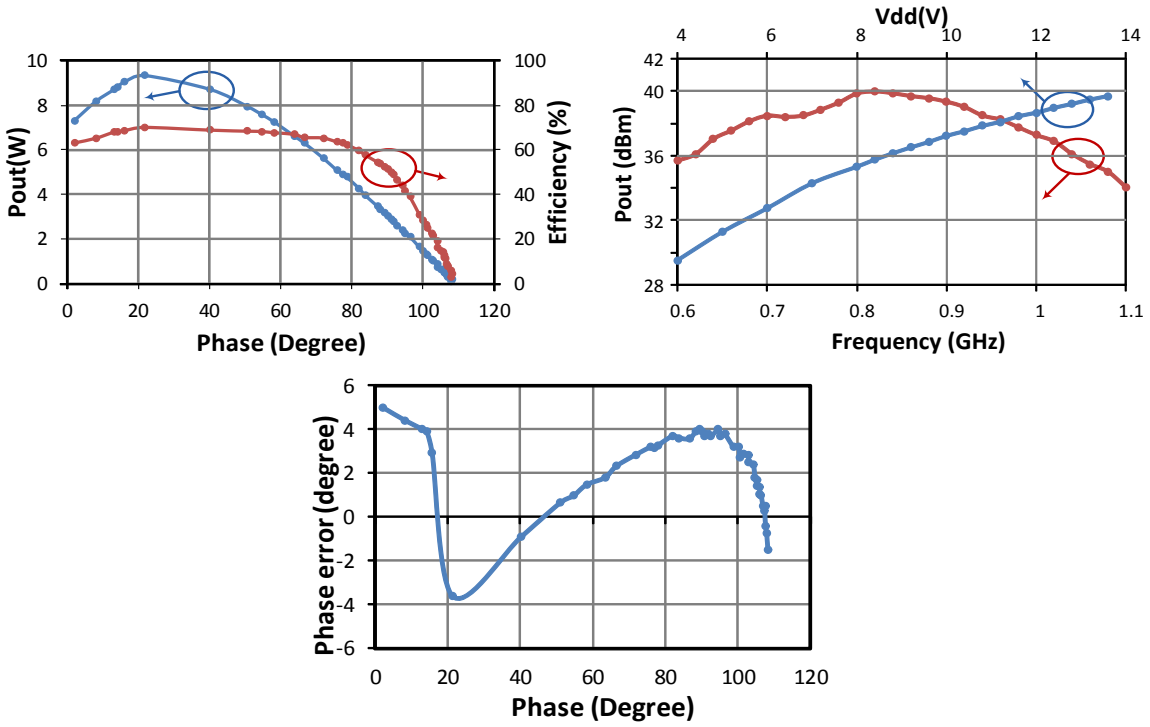

Fig. 4-20: a) Measured P_{out} and *PAE* versus input outphasing angle (θ), b) Measured P_{out} versus frequency and supply voltage, c) Measured Phase Error versus θ.

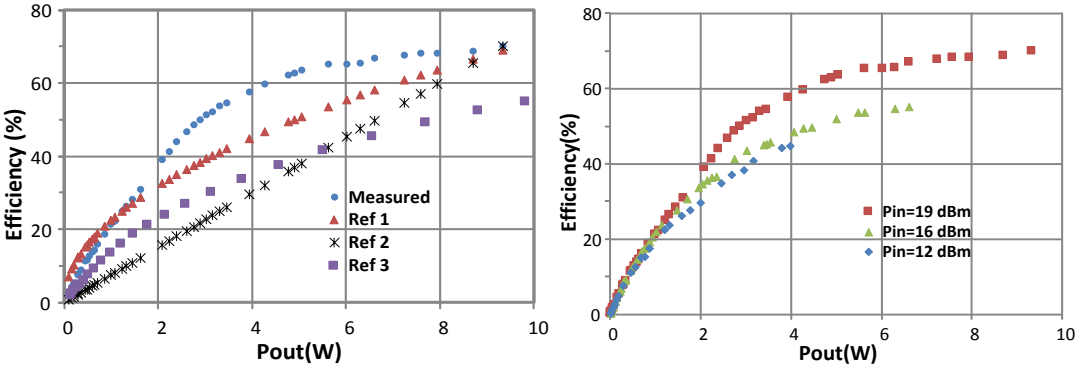

Fig. 4-21: a) Measured Efficiency versus Output power, b) Measured Efficiency versus Output power for different P_{in} .

power. As illustrated the superior performances of the modified Z-LINC over all the other configurations is significant.

4.5 Conclusion

A new approach for linear amplification with nonlinear components (Z-LINC) that provides a zero capacitive loading to the PAs over the whole power back-off range has been presented. The PA capacitive loading has been identified as the major drawback that annihilates the performances of classical LINC. The superior performances of Z-LINC has been explained theoretically and proven experimentally through a set of comparative studies with conventional Chireix and Wilkinson LINC implementations. In addition, a new technique to reduce the size of the TLs, is applied to Z-LINC. Based on the shorter transmission line ($\lambda/8$) compensated with shunt capacitors, a mid-range Z-LINC PA (9.33 W) is implemented using LDMOS transistor for base station applications. Shorter TLs are used for the non-isolated power combiner as well as the input/output matching networks, thereby reducing the area of the circuit.

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5 A Miniaturized Power Combiner for Multi-Band outphasing Transmitters

The today's massive deployment of broadband networks and their relentless adaptation to the emerging high data rate standards resulted in an urgent need for multi-standard terminals enabling proper interoperability and seamless connectivity to the plethora of networks. This trend has been accelerated by the emergence of new communication technologies, such as software defined radio (SDR) and Cognitive Radio (CR) [1]. The success of SDR and CR technologies depends highly on the ability to design miniaturized agile terminals, able to work simultaneously in different frequency bands and supporting various modulation schemes. This chapter proposes a new approach to extend outphasing operation to multi-band frequencies. We analyze a miniaturized dual-band power combiner implementation using lumped elements and the design of a modified class D PA. Afterwards, the fabricated prototype as well as its measured performances are discussed.

5.1 Dual-band outphasing PA

In fact, using parallel multi-transceivers, each one optimized for a specific standard, will obviously result in an unsupportable large area and thus a prohibitive final cost. Although several advances have been made in reconfigurable circuits and systems, the effort was restricted to the baseband and RF front-end circuits [2], [3]. Because of its challenging design, the power amplifier (PA) and its power supply has been excluded from this trend. Except a few attempts that are principally based on bulky MEMS adaptive matching networks [4], the multi-PAs implementations are still the dominant choice [5]. The challenge is exacerbated if a fully

integrated implementation using CMOS technology is targeted. In fact, the low CMOS oxide breakdown voltage limits the output power, while the low substrate resistivity increases the losses in the passive components used in the matching network and power supply circuits [6], [7].

The trickiest part of an outphasing PA to be integrated, is its power combiner. Particularly, the two quarter-wavelength transmission lines ($\lambda/4$-TLs) composing the combiners are the principal area consuming parts [8]. Their large size tends to be bulky and even prohibitive below X-Band [8]. Consequently, miniaturization techniques are necessary for a compact and cost effective implementation. A solution is the replacement of the cumbersome $\lambda/4$ TLs by their equivalent LC network in order to facilitate their integration.

5.1.1 Classical implementation

Regarding to our explanation in section 3-1, basically two families of power combiners can be used for outphasing operation: isolating combiner (e.g. Hybrid or Wilkinson) and non-isolating combiner (e.g. Chireix [9]-[11] or transformers [12]). In isolating combiners, when the input signals are out-phased in order to vary the amplitude, power is wasted as heat in the isolation resistor. This loss nullifies the efficiency advantage inherent to the use of non-linear PAs and thus, limits the attractiveness of these combiners for outphasing. In contrast, non-isolating power combiner preserves the outphasing efficiency even in power back-off mode [13].

Fig. 5-1a (without C_L) illustrates an ideal model of non-isolating Chireix combiner where two TLs with a characteristic impedance Z_0 are driven by the ideal voltage source $S_i(\pm\theta)$. For simplicity's sake, the phase $\varphi(t)$ of the input signal is ignored. For an effective combining operation the TLs should be quarter wavelength (i.e. λ/m with $m = 4$ in Fig. 5-1) [14]. In this case the input admittances at $\theta = B = 0$ are purely conductive, i.e. $Y_{i,\lambda/4}(0,0) = 2R_L/Z_0^2$. More importantly, the output impedance of each branch ($Z_{out1,2}$ in Fig. 5-1), calculated after shortening the corresponding ideal source, becomes infinite. This condition is very important, since it

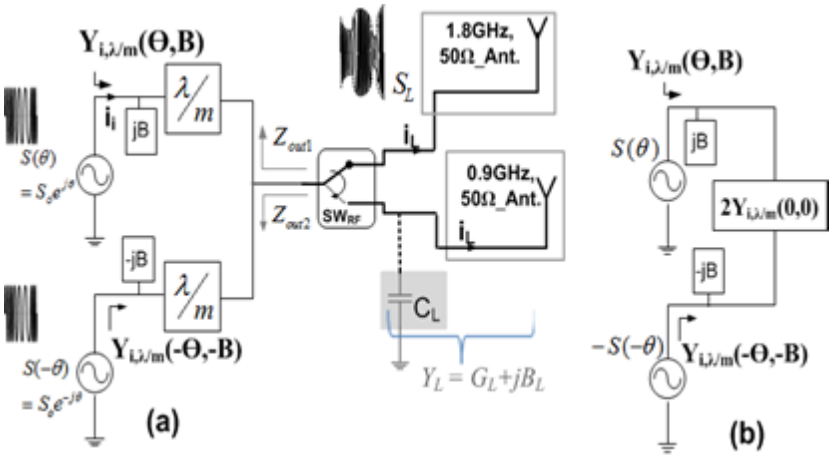

Fig. 5-1: (a) Simplified schematic of proposed dual-band outphasing PA and (b) its equivalent simplified circuit.

guarantees the superposition of the two input voltages at the load and thus, the summation operation (3-4). Consequently, the circuit (a) of Fig. 5-1a can be simplified to the circuit (b) with the admittance $Y_{i,\lambda/4}(\theta, B)$ given by [14], [15]

$$\begin{aligned} Y_{i,\lambda/4}(\theta,B) &= \frac{Y_{i,\lambda/4}(0,0)}{2}\frac{S_i(\theta)+S_i(-\theta)}{S_i(\theta)} + jB \\ &= R_L Z_0^{-2}.\left[2\cos^2(\theta)+ j(B(Z_0^2/R_L)-\sin(2\theta))\right]. \end{aligned} \tag{5-1}$$

Note that the optional shunt susceptance elements $\pm B$ are added in Chireix combiner, in order to nullify the imaginary part of $Y_{i,\lambda/4}(\theta, B)$ at a certain predefined phase (e.g. at $\theta = \theta_0$), thereby maximizing the efficiency at $\theta = \theta_0$ and $\theta = 90° - \theta_0$ [11].

5.1.2 Reconfigurable non-isolating power combiner

We propose using the outphasing topology for a dual-band transmitter working at f and $f/2$ (e.g. 1.8 and 0.9 GHz). Ideally the architecture should use the same PAs and the same combiner for the two bands, as illustrated in Fig. 5-1. Only one extra RF switch is used to select one of the two antennas (e.g. low insertion loss GaAs SPDT switch). Note that the targeted operating frequencies (0.9 and 1.8 GHz) are quite different, thereby making the implementation using a single broadband antenna impractical.

The configuration in Fig. 5-1, however, exhibits dramatic performance degradation at the lower band. In fact, the electrical length of the TLs becomes $\lambda/8$ at $f/2$, which changes completely the nature of the power combiner. The input admittance seen by each PA at $\theta = B = 0$ is no more purely conductive (like $\lambda/4$) but given by

$$Y_{i,\lambda/8}(0,0) = \left(Y_L/2 + jG_0\right)\left(1 + j\left(Y_L/2G_0\right)\right)^{-1}, \tag{5-2}$$

where $Y_L = 1/R_L$ and $G_0 = 1/Z_0$. The reactive loads at the output of the PAs are in general, detrimental for the power efficiency. In addition, the output impedance of each branch ($Z_{out1,2}$ in Fig. 5-1), calculated after shortening the corresponding ideal source, are not infinite as for $\lambda/4$ but equal to $-jZ_0$ according to (5-2). Consequently, the superposition principle used in calculating output power is no more valid and the performances at the lower band are severely deteriorated.

In order to overcome this problem, we propose to start by canceling the reactive part of $Y_{i,\lambda/8}(0,0)$. For this we add a susceptive shunt element, C_L in parallel with R_L (i.e. $Y_L = G_L + jB_L$), as shown in Fig. 5-1. In this case, by writing $Y_{i,\lambda/8}(0,0)$ as $G_{i,\lambda/8} + jB_{i,\lambda/8}$ in (5-2), we can demonstrate that

$$G_{i,\lambda/8} = G_L G_0^2 \left[(G_0 - B_L/2)^2 + (G_L/2)^2\right]^{-1}, \tag{5-3}$$

$$B_{i,\lambda/8} = \frac{G_0\left(G_0^2 - (B_L/2)^2 - (G_L/2)^2\right)}{(G_0 - B_L/2)^2 + (G_L/2)^2}. \tag{5-4}$$

Equation (5-4) shows that the undesired susceptance $B_{i,\lambda/8}$ can be nullified if B_L in Fig. 5-1 is given by

$$B_L = \pi.f.C_L = 2 \times \sqrt{G_0^2 - (G_L/2)^2}\ . \tag{5-5}$$

In this case, the input impedance at $f/2$ calculated from (5-2) becomes purely conductive and equal to

$$Y_{i,\lambda/8}(0,0) = G_L\left(2 - B_L Z_0\right)^{-1}. \tag{5-6}$$

On the other hand, $Z_{out1,2}$ of the $\lambda/8$ power combiner with C_L (Fig. 5-1), after shortening the corresponding ideal source $S(\pm\theta)$, can be expressed as

$$Z_{out1,2,\lambda/8}(0,0) = -2j(B_L - 2G_0)^{-1}. \tag{5-7}$$

Consequently, the condition $Z_{out1,2,\lambda/8}$ infinite, necessary for the superposition, imposes another value for C_L given by

$$B_L = \pi.f.C_L = 2G_0. \tag{5-8}$$

The values of C_L given by (5-5) and (5-8) converge if G_0^2 is chosen very high compared to $(G_L/2)^2$. This condition is in general valid if the power combiner is used also for impedance transformation. Actually, in practical outphasing design, the impedance $Z_{i,\lambda/4}(0,0)$ seen by the PAs (i.e. $Z_0^2/(2R_L)$) is generally chosen much smaller than R_L (50 Ω) in order to have enough output power under low voltage supply. In other words, G_0^2 should be quite high compared to $G_L^2/2$ and thus quite high compared to $(G_L/2)^2$. The value of C_L given by (5-5) and (5-8) are thus quite similar and the two conditions (purely resistive input impedance, $Z_{i,\lambda/8}(0,0)$, and infinite output impedance, $Z_{out1,2,\lambda/8}(0,0)$,) are valid. Consequently, the circuit's simplification (a) to (b), shown in Fig. 5-1, becomes also effective at $f/2$, with $Y_{i,\lambda/8}(0,0)$ given by (5-6). The analytical expression for $Y_{i,,\lambda/8}(\theta, B)$ derived using the circuit (b) of Fig. 5-1 is then

$$Y_{i,\lambda/8}(\theta, B) = \frac{Y_{i,\lambda/8}(0,0)}{2}.\left[2\cos^2(\theta) + j\left(2B / Y_{i,\lambda/8}(0,0) - \sin(2\theta)\right)\right]. \tag{5-9}$$

In summary, the $\lambda/8$ power combiner will behaves like a Chireix combiner if the value of the added capacitor is given by (5-5) and if $Z_0^2/(2R_L)$ is quite small compared to R_L.

Note that according to (5-1) and (5-9), for $B = 0$, the magnitude of $Y_{i,\lambda/m}(\theta,0)$ (i.e. $Y_{i,\lambda/m}(0,0)$ $\cos(\theta)$) decreases when θ increases, thereby decreasing the RF output currents of the PAs. Consequently, the PA power consumption, generally proportional to their RF output current, decreases when the output power backed-off [11], whence the interest of non-isolating combiner.

In order to validate the concept of the reconfigurable power combiner, the circuit Fig. 5-1a is analyzed using ADS. A model of a commercial GaAs antenna switch with 0.3 dB insertion

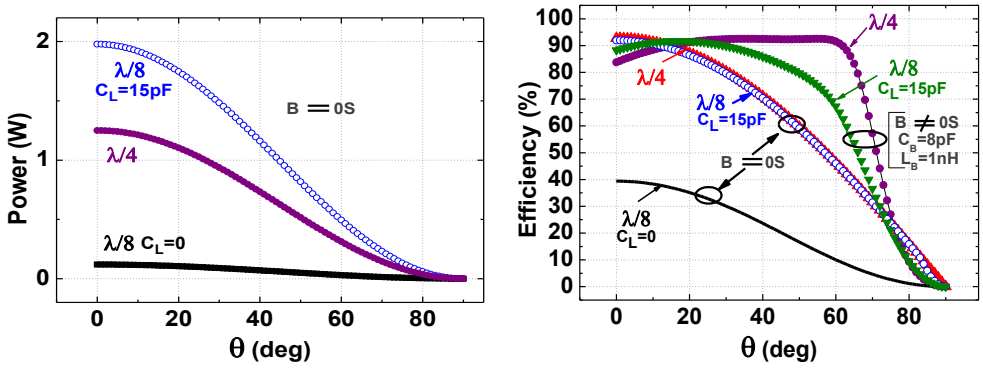

Fig. 5-2: Simulated output power and efficiency of the circuit Fig. 5-1a at 1.8 GHz ($\lambda/4$), 0.9 GHz ($\lambda/8$), without stub ($B = 0$) and with stub (implemented using $C_B = 8$ pF and $L_B = 1$ nH and corresponding to $B = 0.09$ S at 1.8 GHz).

loss and 25 dB isolation is used in the simulations. The values of 2.5 V, 1.8 GHz, 22.3 Ω and 50 Ω are chosen for S_i, f, Z_0 and R_L without loss of generality. With this configuration, the value of $Z_{i,\lambda/8}(0,0)$ (i.e. 5 Ω) is very small compared to R_L and thus, the relations (5-5) and (5-8) give the same values for C_L i.e. 15 pF.

The simulated output power ($P_{out} = |S_L.i_L|/2$) and the efficiency ($\eta = 100\times P_{out}/(S_i.|i_i|)$) versus the outphasing angle (θ) are shown in Fig. 5-2. The results, demonstrate the reconfigurability of the power combiner, with quite similar performances at f and $f/2$ and significant degradation at the lower band if C_L is removed ($C_L = 0$).

The lower power of the $\lambda/4$ configuration is due to the value of $Z_{i,\lambda/4}(0,0)$ (i.e. $Z_0^2/(2R_L) = 5$ Ω) compared to $Z_{i,\lambda/8}(0,0)$ (i.e. 3 Ω from (5-6)).

Fig. 5-3 shows the variation of the real and imaginary parts of the admittances $Y_{i,\lambda/4}(\theta, B)$ and $Y_{i,\lambda/8}(\theta, B)$. As expected, according to (5-1) and (5-9), if B is equal to $Y_{i,\lambda/m}(0,0)\sin(2\theta_o)/2$, the imaginary part of $Y_{i,\lambda/m}(\theta, B)$ is nullified at $\theta = \theta_0$ and $\theta = 90° - \theta_0$. Therefore, η is maximized at these two specific angles [11] as illustrated in Fig. 5-2. $\pm jB$ are implemented using $C_B = 8$ pF and $L_B = 1$ nH, corresponding $\theta_0 = 30°$ at 1.8 GHz. Note that even if B is optimized for f, it also improves the efficiency at $f/2$. In this case, the imaginary parts of $Y_{i,\lambda/8}(\theta, \pm B)$ are not nullified at the same phase, that is why the $P_{out,\lambda/8}$ is slightly less than $P_{out,\lambda/4}$ at $\theta = 90° - \theta_0$ shown in

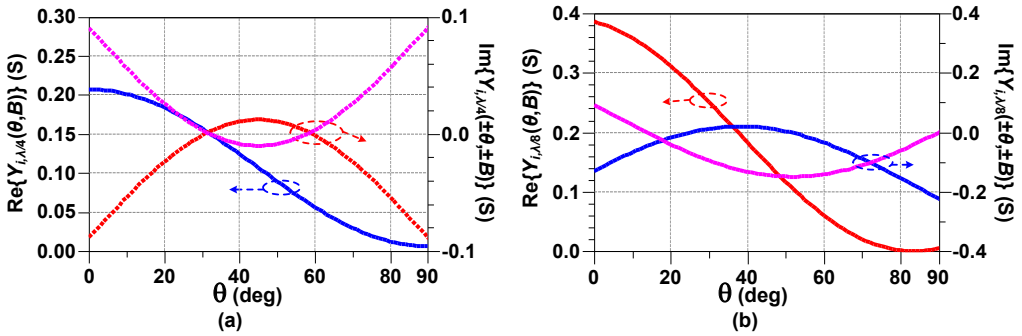

Fig. 5-3: Simulated real and imaginary parts of the input admittance, $Y_{i,\lambda/m}(\theta, B)$ with stub (realized using the same parameters as Fig. 5-2) at a) 1.8 GHz ($\lambda/4$), and b) 0.9 GHz. ($\lambda/8$).

Fig. 5-3. Moreover, the real parts of the input impedances, shown in Fig. 5-3, are decreasing functions of θ and proportional to $\cos^2(\theta)$ in agreement with (5-1) and (5-9).

5.2 Power Amplifier Design

In general, the more the PA behaves like an ideal voltage source (e.g. class D or F) the more it is suitable for outphasing [16]. Fig. 5-4a shows the modified class D circuit proposed for our PA. This architecture enables to work reliably under a voltage supply equal to two times the nominal voltage of the technology. In the proposed topology, we use two series of preamplifiers working from 0 to V_{dd} /2 and from V_{dd} /2 to V_{dd}, driving respectively the power nMOS and pMOS transistors in the last stage. The technology is CMOS 90 nm with a nominal supply voltage of 1.2 V and the oxide breakdown voltage of 3V.

5.2.1 Reliability issues in CMOS technology

The main reliability problems in CMOS technology are the gate oxide breakdown caused by the gate to source (V_{GS}), gate to drain voltage (V_{GD}) and the hot carriers generated by the drain to source voltage (V_{DS}). Gate oxide breakdown results in a permanent damage to the transistor. It is initiated by tunneling current because of electric field across the gate oxide. It can cause defects in the oxide or silicon/oxide interface [17]. Considering very thin gate oxide in advanced CMOS technologies (e.g. 2.4 nm in 90 nm CMOS process), it needs quite a small voltage for

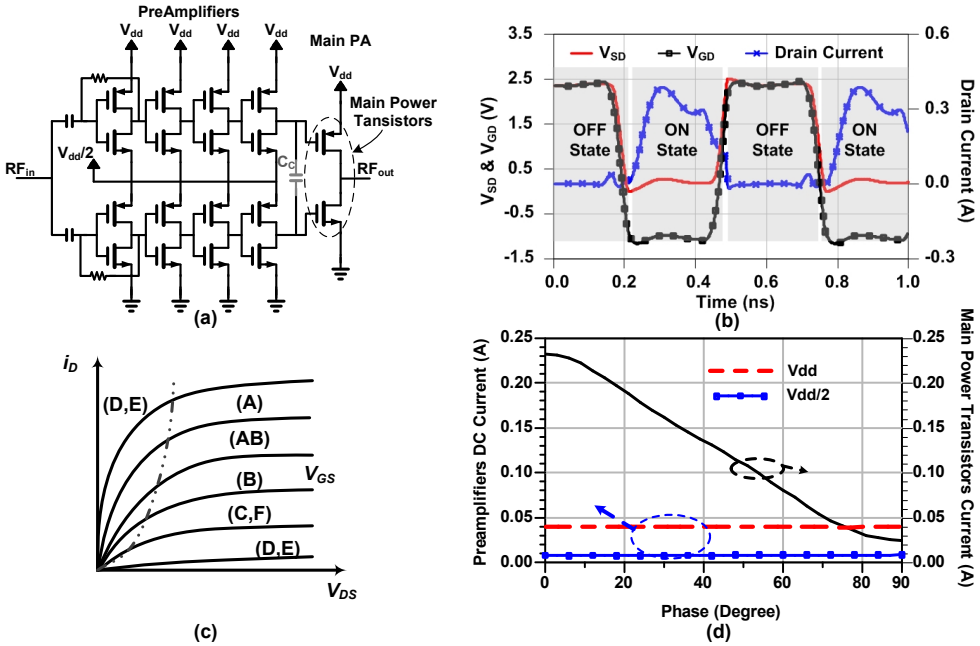

Fig. 5-4: a) Proposed modified Class D PA, b) V_{SD}, V_{GD} and Drain current versus time for main PMOS transistor, c) Typical operating point of different PAs [22], d) DC current consumption by preamplifier and main power transistors.

such a defect to occur. However, the acceptable gate-oxide voltage becomes smaller as the gate oxide thickness is reduced in more advanced process technologies. Aoki in [17] shows that the highest stress areas occur at the source and drain oxide edges and thus in design process we must ensure that V_{GS} and V_{GD} voltages never exceed prespecified values, given by the technology.

On the other hand, hot carrier degradation is caused by the accelerated carriers in the drain-source electric field. Thus, in short channel devices, this field can be very high, and carriers can achieve a very high speed. Some of these "hot" charge carriers collide with the lattice before arriving at the drain with sufficient energy to cause impact ionization [17]. Usually this damage is occurring in the drain region where the electric field is very high, resulting an increase in on-resistance and knee voltage. These defects reduce the PA performance [21]. Unlike the gate oxide breakdown, the hot carrier degradation is not intrinsically catastrophic. To have a noticeable hot carrier degradation, it is required to have high V_{DS} and considerable drain current (I_D) at the same time (Fig 5-4c). Thus, it can be prevented by avoiding high channel current when drain voltage is high [17, 22]. To check the reliability issue in the power PMOS transistor for instance, the variation of the V_{GD}, V_{SD} and I_D of this transistor during the operations is shown in Fig. 5-4b. It illustrates that V_{GD} never exceeds 2.5 V (ditto for V_{GS} and V_{DS}) which is well

below the oxide breakdown of the transistor. On the other hand, because of high lateral electric field in the channel, Hot Carrier Injection (HCI) may happen. To avoid any HCI risk at the power transistors, they could be replaced by thick oxide transistors or a cascode configuration. The trade-off is an increase in the parasitic capacitance or series resistance of the transistors. During ON state (Fig. 5-4b), when V_{DS} exceeds a threshold around 0.5 V, I_D drops to zero. Therefore, the lateral electric field is small in the presence of current and the probability of HCI is negligible. The analysis of the reliability of the power nMOS leads to the same conclusions. For comparison, Fig. 5-4d shows the typical biasing points of different PAs [22]. For example, in non-switching PAs like class AB, the presence of high drain current with high voltage over drain and source may cause HCI degradation.

In addition, stacking the preamplifiers between 0, V_{dd} /2 and V_{dd} enables to save power because the top and bottom preamplifiers reuse the current and work only under a dc voltage equal to V_{dd} /2. Since V_{dd} /2 voltage reference, supplies both top and bottom preamplifiers, its dc current is negligible (Fig. 5-4d). As a result, it could be replaced by an RC voltage divider. The second problem that can decrease the efficiency is the current flowing from V_{dd} to ground through the two power transistors (NMOS and PMOS). A synchronization capacitor (C_C) can be placed between their gates in order to minimize the time overlap during which these two transistors are both open. The last problem in class D integration is a large parasitic capacitor at the output of the PA. This can be solved by absorbing the parasitic capacitor in the capacitor used to emulate the $\lambda/4$ TL in the power combiner (section 5.3).

5.3 Implementation

The proposed multi-band outphasing concept is generic and can be used with any class of saturated PA. By way of illustration and without loss of generality, the modified class D PA [12], [18], is used to drive the dual-band outphasing power combiner. Since the integration of TLs is generally unfeasible at the targeted frequencies (0.9 and 1.8 GHz), we proposed to use a lumped-element implementation, as shown in Fig. 5-5. We propose to consider λ/m TLs to broaden the analysis. In this general case, L and C can be expressed in terms of Z_0 (the characteristic impedance) and τ_D (the total delay) as

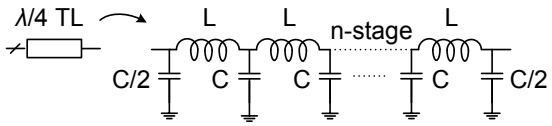

Fig. 5-5: n-stage LC model of a transmission line (TL).

$$Z_0 = \sqrt{L/C}\,, \tag{5-10}$$

$$\tau_D = n\sqrt{LC} = (mf)^{-1}, \tag{5-11}$$

where n is the number of segments. Using (5-10) and (5-11) we can demonstrate that

$$C = \frac{1}{nmf_o Z_o}, \tag{5-12}$$

$$L = \frac{Z_o}{nmf_o}, \quad L_t = 2nL = \frac{2Z_o}{mf_o}, \tag{5-13}$$

where L_t is the total value of the power combiner inductance. It gives an estimation of the area and thus cost of the implementation. In order to gain an insight into the variation of L_t with the design parameters, we consider the particular case of $\lambda/4$ TLs. We can express L_t as [18],

$$L_t = \frac{S_i}{f}\sqrt{\frac{R_L}{2P_{out}}}\,. \tag{5-14}$$

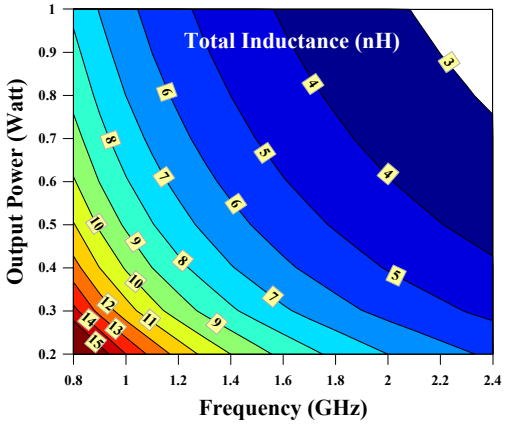

Fig. 5-6: The value of the power combiner inductance versus frequency and output power with a 50-Ω antenna resistance and a S_i of 1.25 V.

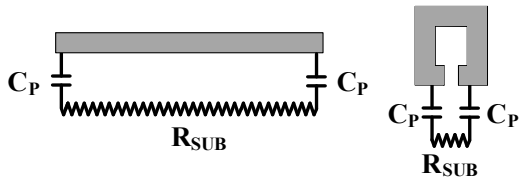

Fig. 5-7: Fundamental model of a slab and one-turn spiral inductor.

Equation (5-14) shows the variation of L_t with different design parameters that is illustrated in Fig. 5-6. The multidimensional curves are realized by assuming an R_L of 50 Ω and a S_i of 1.25 V. From this figure, we see that the more the frequency and the power are high, the less the inductors will be cumbersome. In addition, it shows that several nH are required in all the situations. High inductors value constitutes a critical limitation, not only for the area but also for the efficiency of the PA. In fact, inductors exhibit a limited quality factor due to the metal wire resistance, capacitive and magnetic coupling to the substrate. These detrimental effects are exacerbated in the case of on-chip planar inductors. Despite the recent intensive research effort, the Q of monolithic inductors has been limited to less than 10 in modern CMOS technology. This value can be improved to around 20 if an ultra-thick top metal layer (UTM) is used. However, the limited quality factor of the on-chip spiral inductors, causes a degradation of the outphasing power and efficiency [14]. The simulations show that the output power and thus the efficiency deteriorates by more than 50% for Q equal to 10 compared to the ideal case [14]. Alternatively, slab inductors can reach very high quality factors if they are designed with a relatively small inductance (typically $Q > 30$ if $L < 0.3$ nH [18]). For a given length and metal width, the slab inductor length is shorter than the perimeter of the single turn spiral loop of the same inductance. This is due to the negative mutual inductance between the segments on the opposite sides of the single turn spiral (Fig. 5-7). Furthermore, the shunt resistance through the substrate (R_{SUB}) between the two terminals of the slab inductor is higher when compared to that of the single turn spiral inductor due to the larger distance between them (Fig. 5-7). Therefore, slab inductors have smaller series resistance and substrate losses, and present a higher Q, when compared to the single or multi turn spiral inductors [17]. However, the critical problem with the slab inductor is its low inductance to length ratio (around 0.5 nH/mm). For instance, the total inductance of a U shape slab inductor with a 1 mm length of each side is lower than 1.5 nH. This value is well below the requirements for a $\lambda/4$-based combiner, as shown in Fig. 5 6. For instance, if we target 500 mW on a 50-Ω antenna using a V_{dd} (i.e. ~ 2Si) of 2.5 V, the estimated total

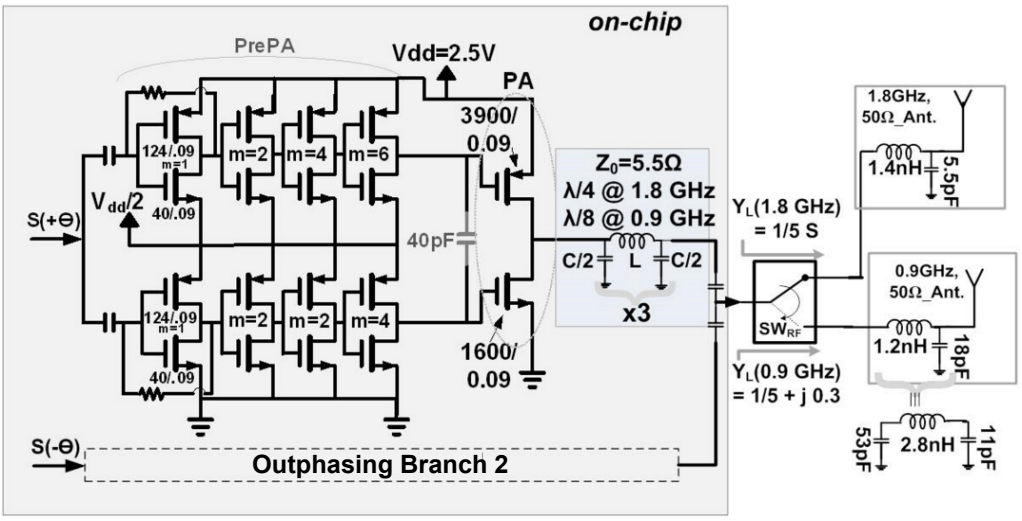

Fig. 5-8: Schematic of the proposed dual-band outphasing PA.

inductance is 5 nH (5-14). In order to reduce this value, the load resistance R_L is decreased to 5 Ω, which results in L = 0.26 nH and C = 8.6 pF. Consequently, high-Q (~35 @ 1.8 GHz) and relatively compact (80×440 μm^2) slab inductors were designed using a 3D electromagnetic simulator. In addition, to the quality factor advantage, the simple geometry of slab inductors makes the outphasing design more compact and the matching between its two branches more effective compared to spiral inductors alternative. An off-chip LC circuit, optimized for each band, is used to filter out the undesired signals and to match 5 Ω to the 50-Ω antenna. The required C_L (53 pF from (5-5) is placed in parallel with lower band antenna and its LC circuit. The resulting network can be simplified from three to two off-chip components as shown in Fig. 5-8.

The simulated output power (P_{out} = $|S_L.i_L|/2$) and the efficiency ($\eta = 100\times(P_{out} - P_{in})/P_{dc}$) versus the outphasing angle (θ) are shown in Fig. 5-9. P_{dc} is the dc power consumed by the PAs and their drivers. Here also, the results, confirm the reconfigurability of the power combiner, with quite good performances at f as well as $f/2$. The benefit of the shunt susceptance elements ±B, however, is negligible and far below what was expected from the power combiner analysis (Fig. 5-2). In fact, class D PA is in general, relatively insensitive to the variable reactive load of (5-1). The impact of compensating elements (±B) is therefore negligible. For simplicity's sake and to minimize the design area, the silicon implementation will be limited to the configuration without stub (i.e. B = 0). Reference curves calculated by assuming that the efficiency is

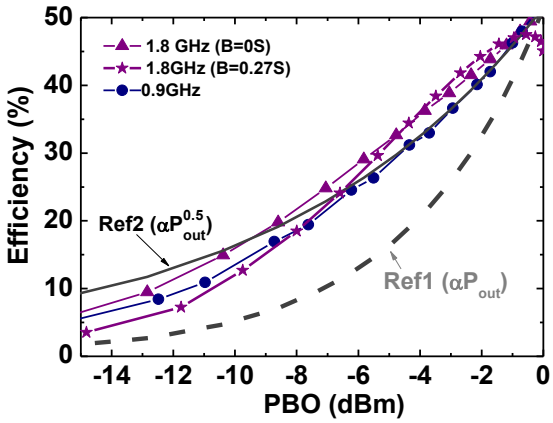

Fig. 5-9: Simulated efficiency versus power back-off (PBO) of the circuit in Fig. 5-8 at 1.8 GHz ($\lambda/4$), 0.9 GHz ($\lambda/8$), without stub ($B = 0$) and with stub ($B = 0.27$ S corresponding to $\theta_0 = 32°$). Ref1 and Ref2 are calculated by assuming ideal Class A (proportional to P_{out}) and ideal class B (proportional to $P_{out}^{0.5}$) respectively.

proportional to P_{out} (like in ideal class A or AB) and proportional to the square root of P_{out} (like in ideal class B) are also shown in (Fig. 5-9). As illustrated, even without the compensation elements ($\pm jB$), the proposed design behaves like an ideal, yet unrealizable, class B PA in the two bands. In addition, a class A, AB or B PA will have obviously, a lower maximum efficiency compared to a switching class D PA, designed in the same technology.

5.4 Measurement Results

The photograph of the prototype fabricated in 90 nm CMOS is shown in Fig. 5-10a. The 3.24 mm^2 die was bonded on the PCB with the off-chip components detailed in Fig. 5-8. The measurement setup (Fig. 5-10b) consists of two Agilent 8648C Synthesized RF Signal Generators to generate input signals and one Agilent 4404B spectrum analyzer to measure output signal spectrum. The two signal generators are coupled via their 10 MHz reference port to avoid any undesired phase variation in input signals. The input signals phase difference is measured by a Lecroy WaveMaster 8000A oscilloscope. Fig. 5-11 shows the measured and theoretic output power as a function of the input phase (θ) for the two bands. The theoretic P_{out} is calculated as $P_{out,max}\,\mathrm{Cos}^2(\theta)$ where $P_{out,max}$ is the maximum measured P_{out} at $\theta = 0$. A maximum output power of 24.0 and 22.4 dBm was measured at 0.9 and 1.8 GHz. These values include the

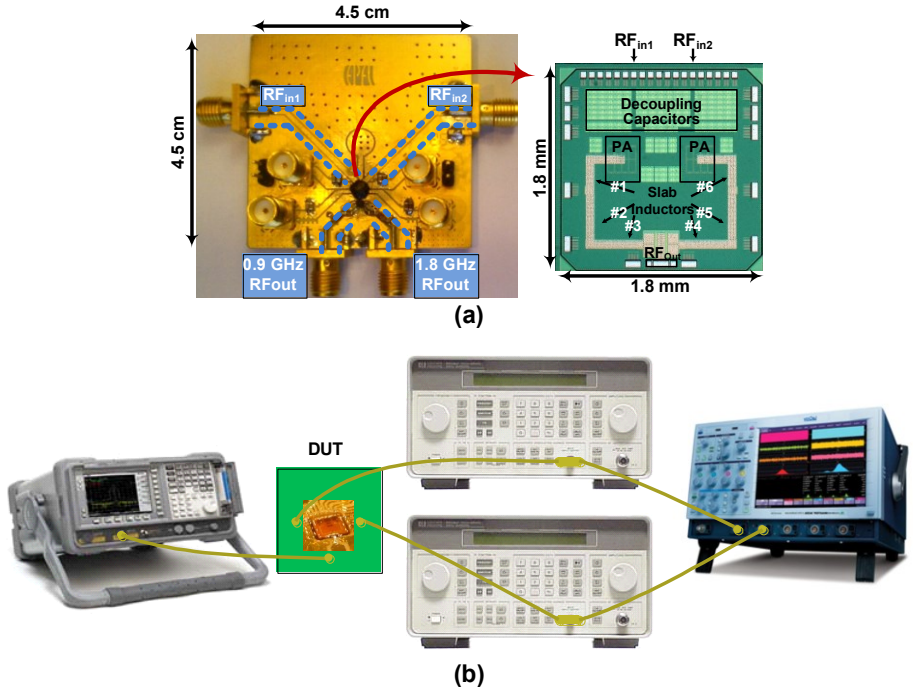

Fig. 5-10: a) Photograph of the PCB and the chip and b) Measurement setup consisting of two Agilent 8648C Synthesized RF Signal Generators, one Agilent 4404B spectrum analyzer, one Lecroy WaveMaster 8000A oscilloscope and the device under test (DUT).

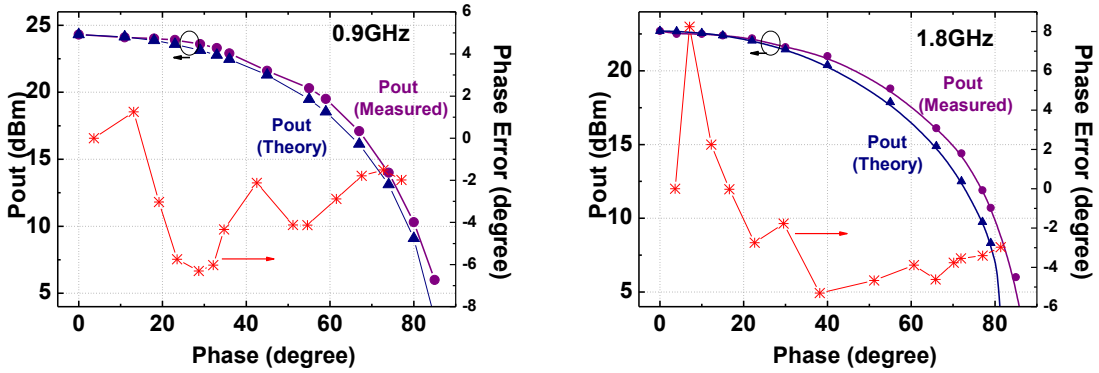

Fig. 5-11: Measured and theoretical Pout versus input phase at 0.9 and 1.8 GHz and the corresponding phase error.

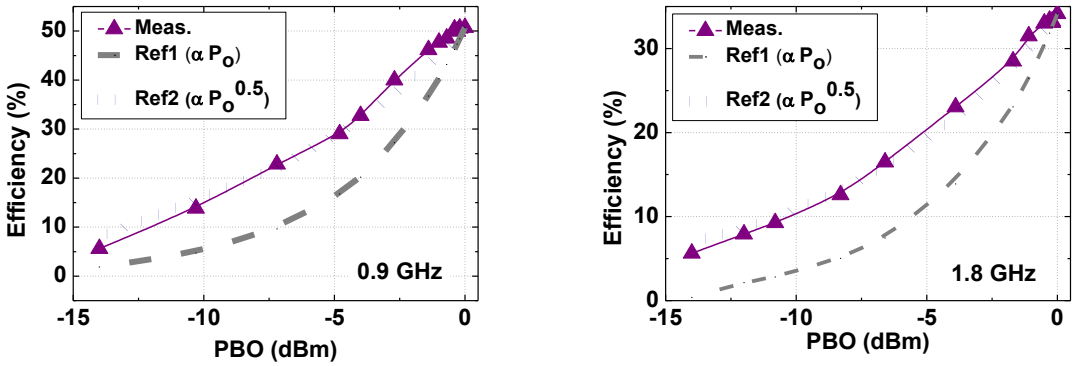

Fig. 5-12: Measured efficiencies versus power back-off at (a) 0.9 and (b) 1.8 GHz and the corresponding reference curves (Ref1 and Ref2) which are calculated by assuming ideal Class A (proportional to P_{out}) and ideal class B (proportional to $P_{out}^{0.5}$) PAs respectively.

0.3 dB insertion loss of the commercial off-chip RF switch. The plots demonstrate the ability to modulate the output power by changing the phase θ for the two bands. The difference between the theoretical and measured curves illustrates the fact that the PAs cannot be considered utterly as ideal sources. This is also illustrated by the phase error determined by $\theta - \cos^{-1}(P_{out,meas.}/P_{out,max})$ shown on the same figure. The measured phase error is quite small (8° as maximum absolute error).

Fig. 5-12 shows the measured efficiencies at 0.9 and 1.8 GHz versus power back-off (PBO). PBO is the difference between the measured P_{out} and its maximum. The reference curves in Fig. 5-12 are calculated by assuming that the efficiency is proportional to P_{out} (like in the ideal class A or AB) and proportional to the square root of P_{out} (like in the ideal class B) . As expected from the simulation analysis, the proposed design behaves like an ideal, yet unrealizable, class B PA with no quiescent current. Note that digitally modulated PAs can exhibits the same behavior [19], but with a relatively complex design. This results illustrates the impact of the decrease of $Y_{i,\lambda/m}$ $(\pm\theta,0)$ with θ, predicted by (5-1) and (5-9) and the associated efficiency improvement at high power back-off (about 50% improvement compared to Ref1 at a PBO of -6 dB).The broadband capability of the PA in the two bands is illustrated in Fig. 5-13 by the measured P_{out} as a function of frequency.

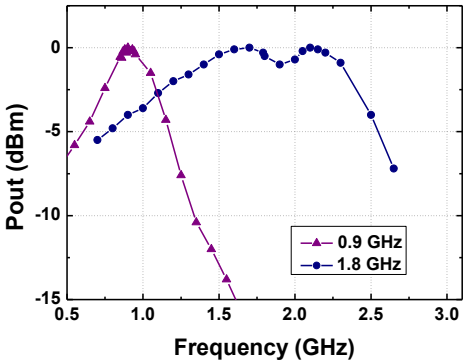

Fig. 5-13: Measured P_{out} versus frequency for the two bands.

Table I. summarizes the performances of the proposed design and compares them to the state of the art dual-band PAs. As illustrated, the proposed solution is a valuable alternative compared to [5] where two separated amplifiers (optimized for each bands) are used or to [19], where a fully integrated PA driving differentially an off-chip broadband matching network and an external balun is used. Another switchless multi-band approach using four bondwire inductors was reported in [20].

Table 5-1: Performance Comparison of Dual-Band PAs

Ref	**Freq (GHz)**	**CMOS (nm)**	**Po_{max} (dBm)**	**η_{max} (%)**	**$\eta_{\|-6dB\ PBO\|}$ (%)**
[5]	2.4/5	65	28.3/26.7	35/25	20/14
[19]	0.8/2	130	23.5/25.2	40/47	20/23.5
[20]	2.45/3.8	180	23.4/24.5	42/39	20/19*
This work	0.9/1.8	90	24.3/22.7	51/34	27/18

5.5 Conclusion

A new design approach for a compact multi-band power amplifier has been presented. It was demonstrated that by using only one extra capacitor, the electrical length and thus the total area of the power combiner can be divided by two, while preserving the full functionality of the outphasing system. The technique in combination with a lumped elements implementation of TLs, enabled a significant miniaturization and thus a full integration of the power combiner.

Actually, an on-chip implementation of the TL, using a classical stripline topology, is unfeasible at the targeted X-band frequencies. As a result, a compact on-chip reconfigurable outphasing power amplifier operating at frequencies as low as 0.9 and 1.8 GHz has been achieved. The outphasing operation has been experimentally demonstrated with a significantly improved efficiency in the two operating bands. This work paves the way to the adoption of power combiners as a viable alternative in terms of integration and flexibility compared to the classical adaptive power and DC-DC converter used in EER.

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6 Discussion on the linearity of the proposed PA

Switching PAs in conjunction with non-isolating power combiner result in a significant improvement of the system efficiency. However, this advantage comes at the cost of a difficult theoretical prediction of the phase to power transfer function. As the test chip only includes the PA side not the signal components separator (SCS), to measure the implemented PA in a multi-channel OFDM (Orthogonal Frequency-Devision Multiplexing) system, the digital outphase conversion should be implemented off-chip. It provides the two outphase input signals to the PAs by using two vector signal generators with OFDM capability, such as "Rohde & Schwarz SMIQ 06B". Both vector signal generators must have custom I-Q modulations with built-in baseband generators capable of multi-channel OFDM.

6.1 Outphase-component signal generator

An OFDM system [1] transmit blocks of symbols in parallel using multiple orthogonal carrier frequencies. Typically, a raw bits stream of each sub-channel (Fig. 6-1), are mapped to appropriate symbols based on the modulation, such as QAM (Quadrature Amplitude Modulation), QPSK (Quadrature Phase Shift Keying). Then, the group of symbols from parallel channels, is fed to the IDFT (Inverse Discrete Fourier Transform) block. In IDFT block frequency domain vectors are transformed to time-domain vectors and serialized in a time domain Parallel to Serial multiplexer. The serial OFDM symbols are separated to I and Q

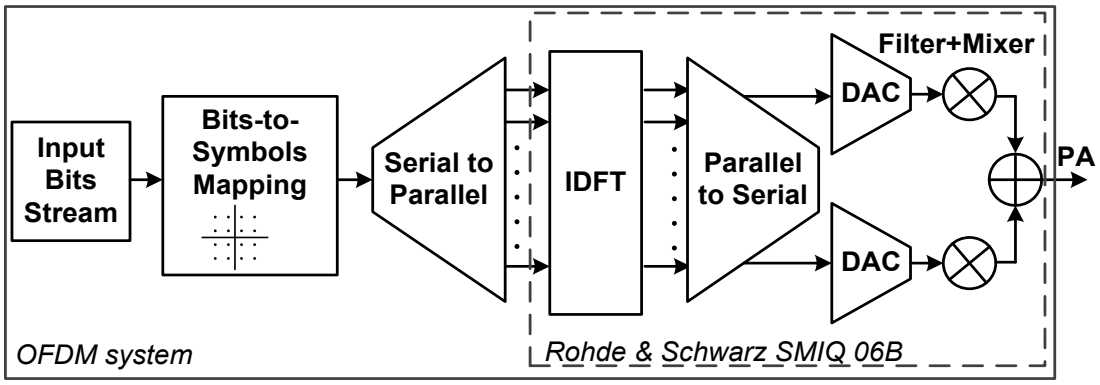

Fig. 6-1: Functionality of an OFDM system.

channels and converted to baseband signals using two DACs (Digital to Analog Converter). After filtering the baseband signals, they are unconverted by mixers and fed to the PA.

To generate the outphase signals for outphasing PAs, the IDFT function could be performed on the input sub-channel modulation symbols to generate OFDM vector using a programing software like C++ or Matlab (Fig. 6-2). Then, inside the software the OFDM vectors are converted to outphase signals and transformed back to the new sub-channel modulation symbols to feed the vector signal generators. Note that these vectors have arbitrary I-Q modulation because of outphasing transformation, thus the custom I-Q modulation option of the vector signal generator is mandatory. In addition, both generators should be synchronized both in Baseband (Symbol sync in/out) and RF (RF sync in/out) frequencies to ensure the correct timing.

Because of the equipment limitations, we use ADS tool that enables to co-simulate RF circuits at transistor level and their response to complex modulated signals generated by 3GPP RF source. In the next part, the performance of the implemented PA will be examined using ADS and measurement results.

6.2 Linearity performance of the Dual-Band Outphasing PA

In fact, the designed switching PAs did not behave exactly like ideal source, which was the fundamental assumption of the theoretical analysis in ideal outphasing PA. Consequently, generating the required outphasing angles, leads to a spectral distortion. The distortion problem

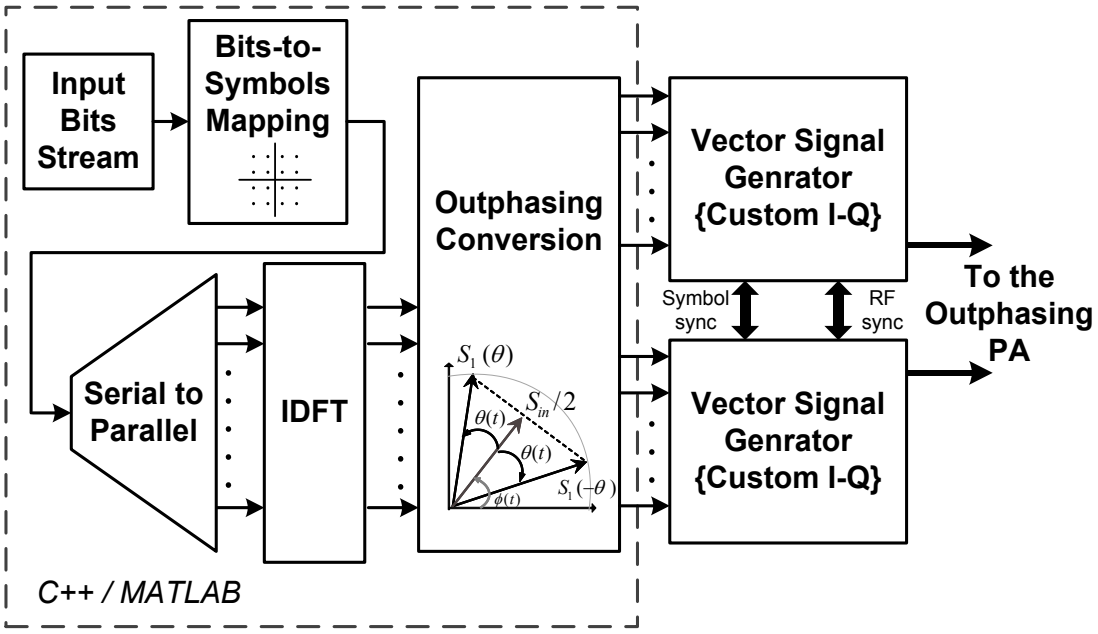

Fig. 6-2: Generating outphase input signal.

is accentuated by the bandwidth expansion of the outphased signals $S(\pm\theta)$ compared to S_{in} [2], [3]. Nevertheless, the digital nature of the signal component separator (SCS), used to generate $S(\pm\theta)$, makes its efficient implementation with powerful predistortion algorithm easier. For instance, a sub-mW all-digital SCS has been experimentally demonstrated in [4]. Several predistortion methods with successful application to broadband standards (e.g. EDGE and WCDMA) have been already published for isolating and non-isolating power combiners [5], [6]. However, it is fundamental to give some insight on the bandwidth of the system with the novel combiner and its capabilities with respect to different modern communication standards. Fig. 6-3 shows the simulated output power versus frequency of the multiband PA introduced in previous chapter (Fig. 5-8). As expected the capacitor added to the combiner at 0.9 GHz narrows relatively its bandwidth. Nevertheless, it remains a priori sufficient for the practical standards.

Fig. 6-4 shows the simulated transfer function from input phase to output amplitude voltage (Distorted). For comparison, the expected phase to amplitude transfer function determined by applying following equations from chapter 3,

$$S_L(t) = A_v(S(\theta) + S(-\theta)) = A_v S_{in}(t)\,, \tag{6-1}$$

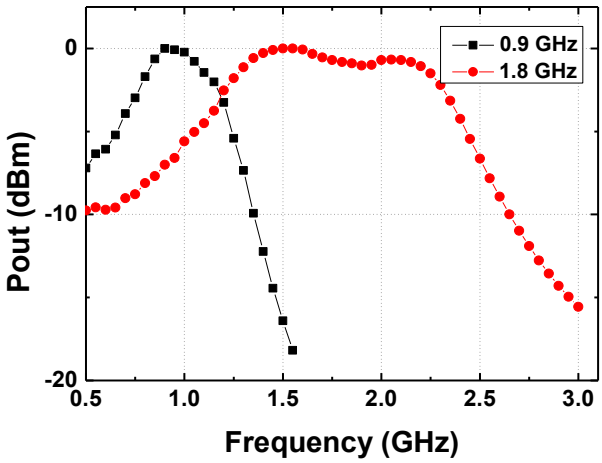

Fig. 6-3: Simulated output power versus frequency for the two bands of the circuit in Fig. 5-8.

$$\theta(t) = \cos^{-1}\left(|S_{in}(t)| / 2S_0\right), \tag{6-2}$$

to the simulated output signal (S_L), is shown in the same figure (Ideal). Note that the difference between the two curves is quite small (-6° as maximum error) and thus would generate a limited signal distortion. Furthermore, the phase error can be fitted using a polynomial approximation [7]. The model (Fig. 6-4), stored in a lookup table, can be used by the SCS to generate the pre-distorted S($\pm\theta$) [8]. In practice, the values of the lookup table should be updated continuously during the PA operation. For this, a feedback signal from the output is commonly used during the calibration.

For further assessment, the ADS tool that enables to co-simulate RF circuits at transistor level and their response to complex modulated signals generated by DSP, is used. The circuit in Fig. 5-8, was implemented in an ADS test bench as shown in Fig. 6-5. A modulated EDGE and WCDMA signal sources are used to drive the circuit. The complex signal is translated to its polar form. The magnitude is transformed to a phase according to (6-2) and predistorted using the polynomial model shown in Fig. 6-4. The resulting spectrums are shown in Fig. 6-6. The simulated error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) for WCDMA and EDGE signals are shown in the same figure. As illustrated, the spectrums are quite symmetric and the mask is respected. The simulated ACLR is about 46 dB and 54 dB at

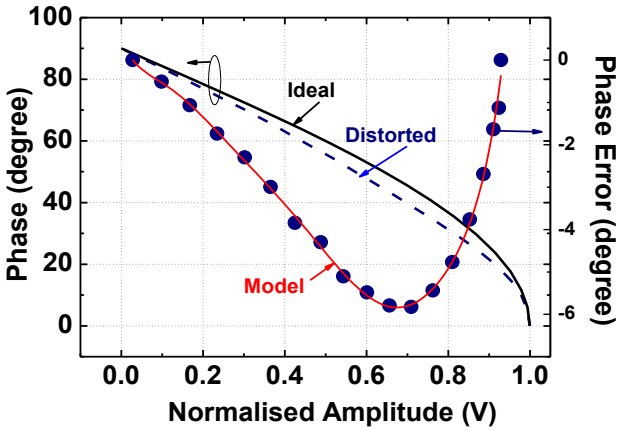

Fig. 6-4: Ideal and simulated distorted phases versus normalized output amplitude at the antenna of the circuit in Fig. 5-8 and the corresponding phase error (difference between the simulated and ideal phase) with its 3rd order polynomial fitting model.

5 MHz and 10 MHz for both upper and lower adjacent channels at 1.95 GHz. At 5 MHz the ACLR is degraded to 37 dB for the 0.9 GHz band. This is due to the distortion introduced by the narrow bandwidth of the modified power combiner at this frequency. Nevertheless, the system passes all the 3GPP specifications (i.e. ACLR (5MHz) = 33dB, ACLR (10MHz) = 43 dB and EVM = 17.5 %) in the two bands and with a comfortable margin.

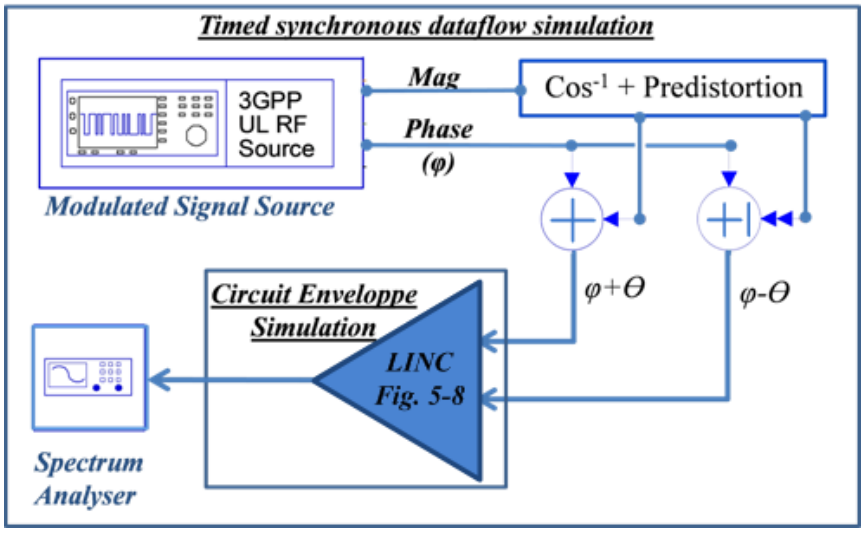

Fig. 6-5: ADS test bench used for system level simulation.

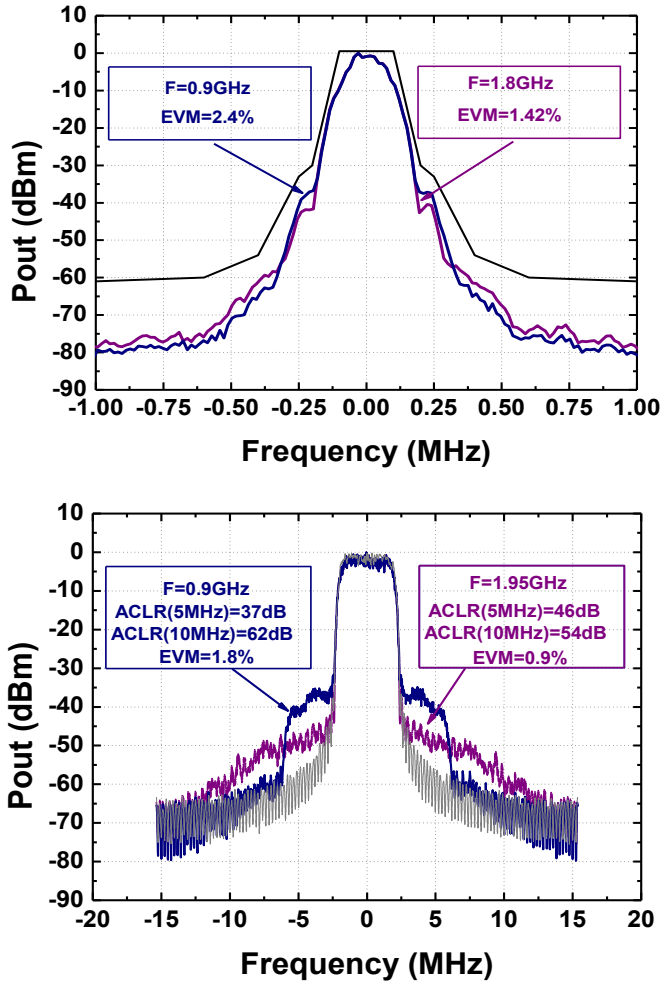

Fig. 6-6: Normalized output power spectrums, EVM and ACLR simulated using the test bench of Fig. 6-5 for EDGE and WCDMA test signals.

6.3 Conclusion

To test the outphasing PA under modulated signal, a special setup is needed. The SCS functionality should be implemented in a programming language like C++ or Matlab. Then, the modulated signals are fed into the two vector signal generators to generate outphase input signal for outphasing PA. This could also be done by using ADS tool to co-simulate measured PA and its response to complex modulated signals generated by 3GPP RF source.

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7 Summary and Conclusion

7.1 Summary

This research has investigated the design and implementation of multi-band outphasing power amplifier (PA) for mobile and base station applications. Essential metrics of PAs, efficiency enhancement techniques and selected technologies for PA implementation were reviewed. In addition to the theory of outphasing topology, a detailed discussion on the proposed "circuit oriented approach to simplify the chireix outphasing PA" and "simplified model of lossy transmission lines" were provided. Based on these concept, two approaches, "Zero Capacitive Load", and "Outphasing combiner with reduced size λ/m TL", were introduced. The theoretical analysis of these methods were followed by simulation and experimental results. Furthermore, a new methodology to extend outphasing operation to multi-band frequencies were introduced. This methodology was verified by design, simulation and implementation of a miniaturized dual-band power combiner and a modified class D PA at 900 and 1800 MHz.

7.2 Conclusion

Complex modulations used in modern wireless communications impose stringent linearity and power back-off requirements for the transmitters resulted in sacrificing PA efficiency. Among different efficiency enhancement techniques discussed in Chapter 2, outphasing is one of the most promising methods to improve the efficiency in power back-off mode. Unfortunately, the theoretical analysis of an outphasing PA considering the effect of impedance

mismatch between PA and combiner, were too complex and far from intuitive. In chapter 3, we proposed a new method to derive a simplified analytical formula expressing the output power directly in terms of the non-distorted input phase. This theoretical analysis is enhanced by including the losses in outphasing power combiner. The ADS simulation results show an agreement between simulations and theoretical expressions. Based on this model, the "Zero Capacitive Load" concept were introduced. In this method, the power combiner and stubs were designed in a way that they provide zero capacitive loading to the Z-LINC PA over the whole power back-off range. Because the capacitive loading has been identified as the major drawback that annihilates the performances of classical LINC. A 2-W Z-LINC PA was implemented to experimentally prove the superior performance of Z-LINC through a set of comparative studies with conventional Chireix and Wilkinson LINC PAs. Besides, a new technique to reduce the size of TLs, is applied to Z-LINC. Based on the shorter TLs ($\lambda/8$) compensated with shunt capacitors, a mid-range Z-LINC PA (9.33 W) is implemented for base station applications. Shorter TLs are used for the non-isolated power combiner as well as the input/output matching networks, thereby reducing the area of the circuit by a factor of two. LDMOS technology is used to implementation of the latter PA that is the leading RF power technology for base station applications, in particular for the frequency range of 1 to 10 GHz, and the power range of a few watts up to hundreds of watts.

On the other hand, an urgent need for multi-standard terminals has been accelerated by the emergence of new communication technologies, such as software defined radio and Cognitive Radio. Their success depends highly on the ability to design multi-band multi-standard PAs. In chapter 5, we introduced a dual-band outphasing PA utilizing $\lambda/4$- $\lambda/8$ TLs as power combiner, and modified Class D PAs. The power combiner implemented on-chip using lumped elements. However, the limited quality factor of on-chip passive components, cause a degradation of the outphasing power and efficiency. Therefore, high quality slab inductors and MIM capacitors were used to implement a low-loss power combiner. On the PA side, the modified Class D architecture enables to work reliably under a voltage supply equal to two times the nominal voltage of the technology. The multi-band PA prototype was fabricated in 90 nm CMOS technology. Because of the low cost and integration capabilities of CMOS technology, it is the

choice of RF transceivers with fully-integrated PAs, as long as RF and system design goals can be achieved. With CMOS transistors in advanced technologies, the output power is usually less than 1 W.

7.3 Future Directions

Research in dual-band PAs is still emerging and our proposed techniques could be applied to new applications. Some directions are presented in the following discussion.

7.3.1 Hybrid implementation

At low output power, other efficiency enhancement techniques, such as power supply modulation or EER discussed in chapter 2, can be used as a hybrid solution with outphasing PA. In this method, the power supply is switched to a lower voltage level to decrease the dc power consumption thus improving the efficiency at low output power. The power supply could be digitized in few steps to avoid the complexity of EER.

7.3.2 Integration of Doherty PA using "reduced-size TL" technique

The Doherty PA is one the efficiency enhancement techniques discussed in chapter 2. The main drawback of this technique is its three $\lambda/4$ TLs which is very difficult to integrate at the typical frequencies used in modern telecommunication systems (0.8-3 GHz). Two proposed techniques explained in this thesis, "Lumped element model of the TL" and "reduced-size power combiner", could be used to integrate Doherty PA.

7.3.3 Z-LINC and HEMT devices

The Z-LINC concept explained in chapter 4, can be employed to design multi-hundred-watt PAs using HEMT (High-Electron-Mobility Transistor) devices. HEMT devices such as GaN HEMT operates with a power supply voltage up to 50 V, similar to the range of the power feeder voltage of 48 V, which is commonly used for communication equipment. By extracting the device characteristics and using the Z-LINC methodology, high-power (100-500W) high-efficiency PAs can be designed for base-station applications.

7.3.4 WLAN IEEE 802.11 application

The multiband approach presented in chapter 5 can be applied to the wireless LAN adaptors. The WLAN IEEE 802.11b/g/n radios utilize the 2.4GHz frequency band and the IEEE 802.11a

radio utilizes the 5GHz frequency band. The one octave frequency difference between the bands makes it a perfect candidate for the proposed multiband outphasing technique.

7.3.5 Reduced size $\lambda/16$ TL

It is worth to research on extending the application of reduced size TLs to $\lambda/16$. The similar approach given in chapter 5, can be used for $f/4$ (i.e. 450MHz). In fact, by using the same topology of Fig. 5-8 and by choosing the value of C_L equal to 78 pf, the input admittance, $Y_{i,\lambda/16}(\theta, B)$, exhibits the same behavior as $Y_{i,\lambda/4}(\theta, B)$ shown in Fig. 5-3. The simulation in Fig. 7-1 shows that the real part of $Y_{i,\lambda/16}(\theta, B)$ exhibits the same behavior as $Y_{i,\lambda/4}(\theta, B)$, varying from 1.3 S to zero while its imaginary part is nullified around $\theta = \theta_0$ and $\theta = 90° - \theta_0$. Note that the real part of $Y_{i,\lambda/16}$ at $\theta = 0$, is significantly higher than $Y_{i,\lambda/4}$ which means that the expected output power will be also higher.

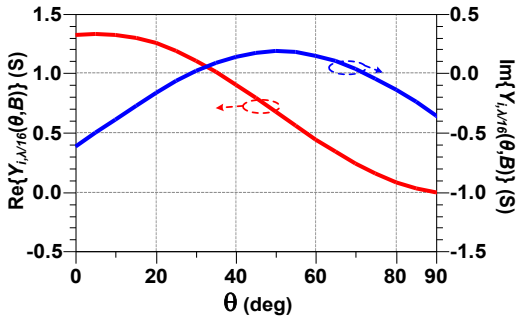

Fig. 7-1: Simulated real and imaginary parts of the input admittance, $Y_{i,\lambda/16}(\theta, B)$ with stub (realized using the same parameters as Fig. 5-3 at 450MHz.

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