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IcySoC RTD 2013

FNSNF

Cross-Layer Inexact Design for Low-Power Applications

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Abstract

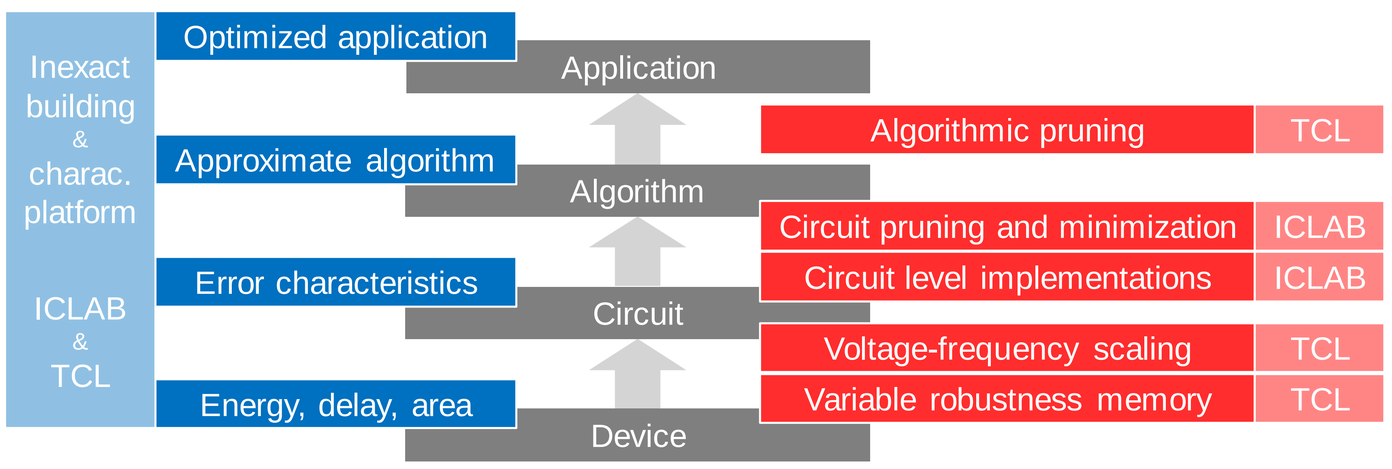
Achieving miniaturization, low-power and real-time data processing requires always more expensive design constraints and margins. Guard bands and worst case safety margins coupled with error correction units to ensure perfect calculations and robustness against Process-Voltage-Temperature (PVT) variations strongly deteriorate chip performance, power and cost efficiency.

Approximate and error tolerant circuits are a radical new approach to trade calculation accuracy for better speed, power, area and yield. The IcySoC project platform revisits low-power and low-voltage VLSI design through a cross-layer combined inexact design framework.

Inexact characterization and co-design framework

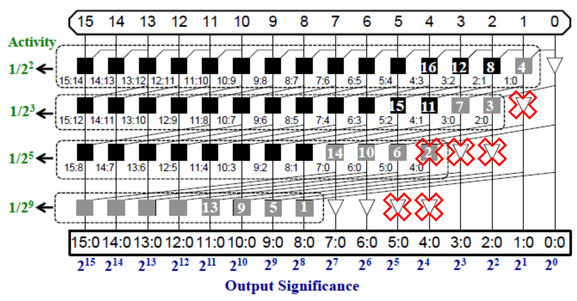
Inexact design techniques used independently at any level of the system has been proved to lead to significant gains in energy efficiency. However, fully exploiting the potential of these techniques requires cross-level work to adapt to the desired application.

By joining forces in a bottom-up approach, two labs at EPFL collaborate in this project, combining their respective inexact design methodologies to a holistic framework for low-power design.

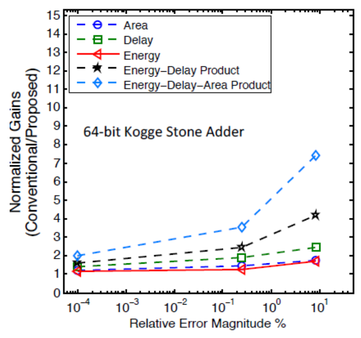


Circuit pruning and minimization

Pruning consists in deleting circuit's gates or cells having the lowest Significance-Activity Product (SAP).

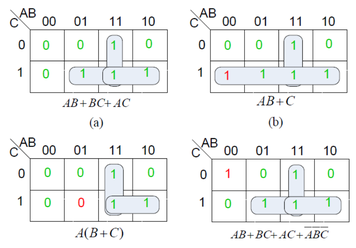


Ranking Scheme for a 16 bits Kogge-Stone adder [1]

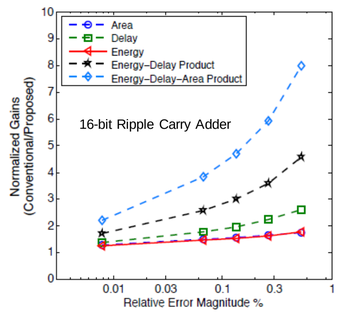


Gains up to 8X in energy-delay-area product [1]

Minimization consists in introducing bit flips in Karnaugh maps of logic functions in order to reduce circuit complexity.



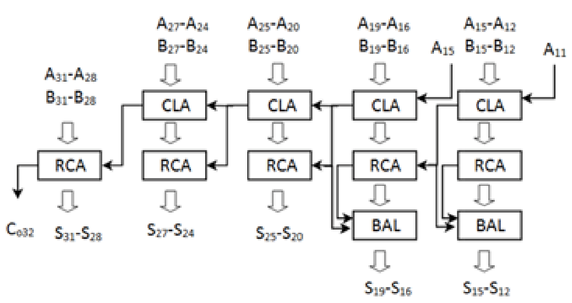
Example of K-Maps of the (a) initial Correct Function (carry of a full adder) (b) function with a favorable 0 to 1 bit flip (c) function with a favorable 1 to 0 bit flip (d) function with a non-favorable 0 to 1 bit flip [2]



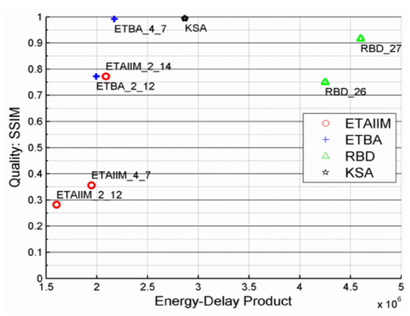
Gains up to 8X in energy-delay-area product [2]

Circuit level implementations

The main idea in working at circuit level is to conceive fundamentally different circuit schemes to better control the calculation error characteristics and allow more efficient pruning and minimization of these circuits.



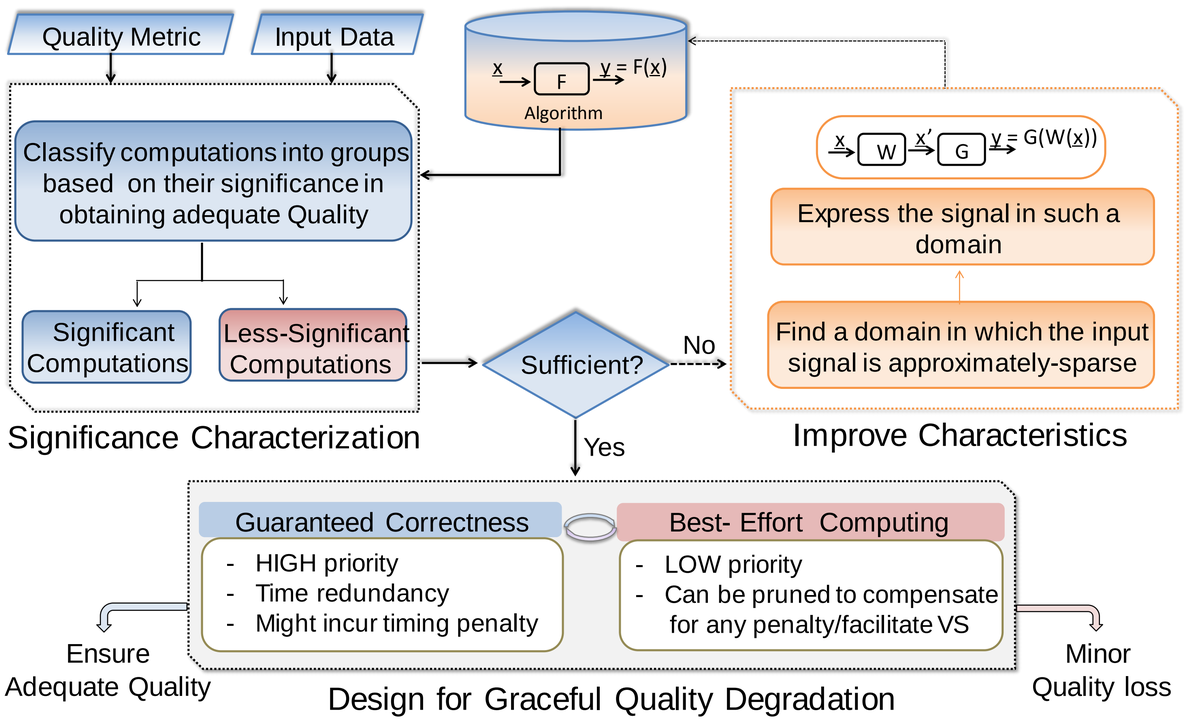
Approximate speculative adder ETBA: carry speculations at different levels prevent long propagations of carry propagates [3]



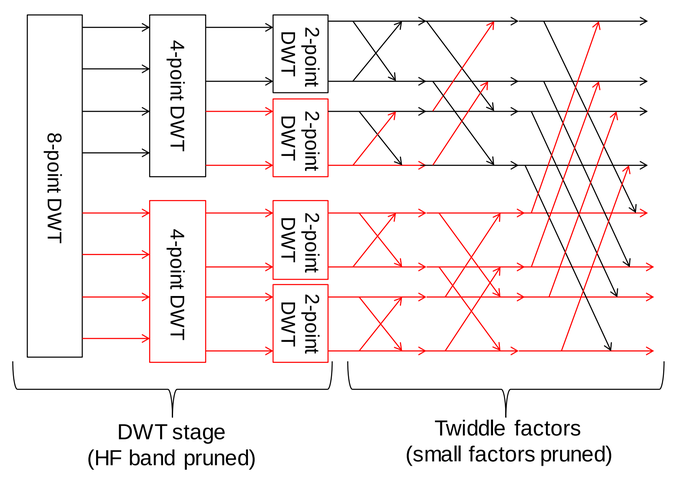
Quality and Energy-Delay product of JPEG decompression using different speculative adders (ETBA and ETAIIM [4]) versus Kogge-Stone Adder (KSA) and reduced bandwidth Ripple Carry Adder (RBD) [3]

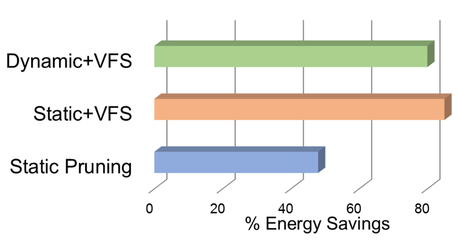
Algorithmic pruning

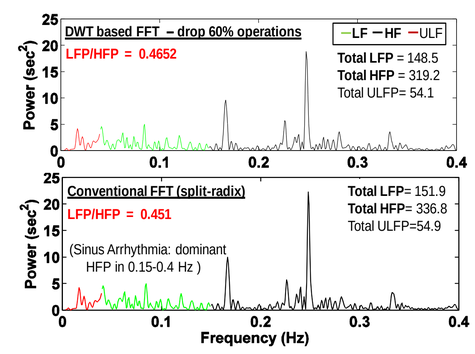
Pruning at the algorithm level consists of classifying the significance of computations and skipping the less-significant ones for adjusting to dynamically changing hardware capabilities and for saving power.



- Application to FFT and Spectral Analysis of Heart Rate







- Quality-loss does not affect the ability of detecting any sinus arrhythmia condition [5]
- Many other applications [6, 7]

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[2] A. Lingamneni *et al.*, Parsimonious circuits for error-tolerant applications through probabilistic logic minimization, *PATMOS*, 2011.
[3] M. Weber *et al.*, Balancing Adder for error tolerant applications, *ISCAS*, 2013.
[4] N. Zhu *et al.*, An enhanced low-power high-speed Adder For Error-Tolerant application, *ISIC*, 2009.
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[6] G. Karakonstantis *et al.*, Process-Variation Resilient & Voltage-Scalable DCT Architecture for Robust Low-Power Computing, *IEEE Trans. on VLSI Systems,* 2010.
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