Electrical Transport Properties of Single-Layer WS_2

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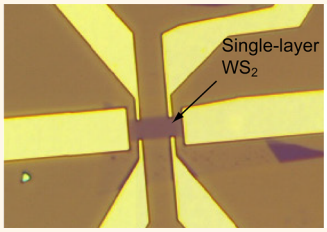
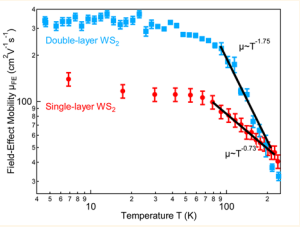
ABSTRACT We report on the fabrication of field-effect transistors based on single layers and bilayers of the semiconductor WS_2 and the investigation of their electronic transport properties. We find that the doping level strongly depends on the device environment and that long *in situ* annealing drastically improves the contact transparency, allowing four-terminal measurements to be performed and the pristine properties of the material to be recovered. Our devices show n-type behavior with a high room-temperature on/off current ratio of $\sim 10^6$. They show clear metallic behavior at high charge carrier densities and mobilities as high as ~ 140 cm^2/(V s) at low temperatures (above 300 cm^2/(V s) in the case of bilayers). In the insulating regime, the devices exhibit variable-range hopping, with a localization length of about 2 nm that starts to increase as the Fermi level enters the conduction band. The promising electronic properties of WS_2, comparable to those of single-layer MoS_2 and WSe_2, together with its strong spin−orbit coupling, make it interesting for future applications in electronic, optical, and valleytronic devices.





KEYWORDS: tungsten disulfide (WS_2) · transition metal dichalcogenides (TMD) · two-dimensional (2D) electronics · layered semiconductor · contacts · mobility

Transistor scaling issues related to increased heat dissipation due to short-channel effects clearly show the strong need for new materials with enhanced characteristics for electronics. Two-dimensional (2D) materials and transition metal dichalcogenides (TMDs) among them are widely investigated at the moment, due to the rich diversity of mechanical, electronic, and optoelectronic properties. Initiated in 2004 by the isolation of graphene,[1] which further became one of the most intensively investigated materials, the field expanded to other 2D materials such as TMDs. Despite its outstanding carrier mobility,[2] graphene lacks a band gap, which limits its applications in electronics. TMDs on the other hand are a family of materials with a wide variety of electronic properties.[3] Typically described by the formula MX_2, where M stands for a transition metal (Mo, W, Nb, Ta) and X for a chalcogenide atom (S, Se, Te), this material family is composed of semiconductors (MoS_2, $MoSe_2$, WS_2, WSe_2, ...), metals ($NbTe_2$, $TaTe_2$, ...), and superconductors (NbS_2, $NbSe_2$, ...). Among the semiconductors in the family of TMDCs, MoS_2 isolated in the single-layer form was first to attract attention, demonstrating high on/off current ratio and low off-state current.[4] Integrated circuits based on single-layer MoS_2,[4] bilayer MoS_2 (ref 5), signal amplifiers,[6] and nonvolatile memory cells[7] were also demonstrated as well as highly flexible field-effect transistor devices based on ultrathin MoS_2.[8] The presence of a direct band gap[9−12] in MoS_2 due to the 2D confinement[12] makes it interesting for applications in optoelectronics, for example in ultrasensitive[13] photodetectors.[14] At low temperatures, metal−insulator transition in single-layer MoS_2 devices with top-[15] and back-gates were observed.[16] Demonstration of high-performance devices in the back-gated geometry,[16,17] with electron mobilities of >60 cm^2 V^{-1} s^{-1} at room temperature, highlighted another important property of these materials: the strong influence of the adsorbates from the atmosphere on their electronic properties.

WS_2 is another representative of the family of semiconducting TMDs. According to optical measurements, the single-layer form exhibits a direct band gap of at least 2.0 eV.[18] Theoretical models predict that among the semiconducting 2D TMDs[19] WS_2 should have the highest mobility due

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to the reduced effective mass. WS_2 could also be very interesting because of the strong spin−orbit coupling induced valence band splitting,[20] which results in spin-valley coupling.[21] While the valence band splitting for MoS_2 is ≈150 meV, because of the larger mass of W atoms, it is almost three times larger (≈426 meV) in WS_2, which would allow easier observation of the valley Hall effect than in MoS_2.[21,22]

The need for large-area deposition of TMDs resulted in interest in large-scale growth methods, including CVD growth of WS_2 in single-layer form.[23−25] All these outline the need for data on the electrical performance and transport properties of single-layer WS_2. Recent reports of transistors made of multilayer WS_2 (ref 26) showed the potential of this material. Vertical transistors based on WS_2/graphene heterostructures were also integrated with flexible substrates.[27] Recent reports on liquid-gated multilayer[28] and single-layer[29] WS_2 gave an estimate of the mobility of charge carriers of 44 $cm^2/(V\ s)$ at room temperature.[29] Temperature-dependent transport of multilayer WS_2 in the insulating regime was also recently investigated on SiO_2 and BN substrates.[30] Temperature-dependent transport measurements on single-layer WS_2 with a solid gate, which are desirable for practical applications, are still missing. In this article we aim to complete the picture and provide experimental material regarding the transport properties of this material. After careful annealing in vacuum, we were able to probe both the insulating and the metallic conduction regime in this material as a function of temperature, reaching high mobilities at room temperature and observing the crossover into the metallic conduction regime at lower temperatures.

RESULTS AND DISCUSSION

Device Performance in Air and in Vacuum. We first focus on the room-temperature performance of our back-gated WS_2 field-effect transistors. An optical micrograph of a typical device is shown in Figure 1b. Bias voltage is applied between drain and source electrodes, while the voltage drop across the channel is measured between probes labeled V_1 and V_2

We first characterize a typical double-layer WS_2 device in air, in vacuum, and after annealing in vacuum and compare these results (Figure 2). In air, the device shows p-type behavior with channel current I_{ds} = 1 nA at gate voltage $V_g = -70$ V and bias voltage V_{ds} = 1 V. Pumping down the chamber provides access to both branches of conductance, as shown in Figure 2a. During this experiment, we reached a pressure $p = 2.7 \times 10^{-5}$ mbar before annealing (green curve in Figure 2a) and $p = 5 \times 10^{-7}$ after 40 h annealing at 115 °C (blue curve in Figure 2a). As the pressure is decreased, the conductance on the electron side is enhanced, while the p-type conductance is suppressed. Figure 2b shows the threshold voltage V_{th} as a function of

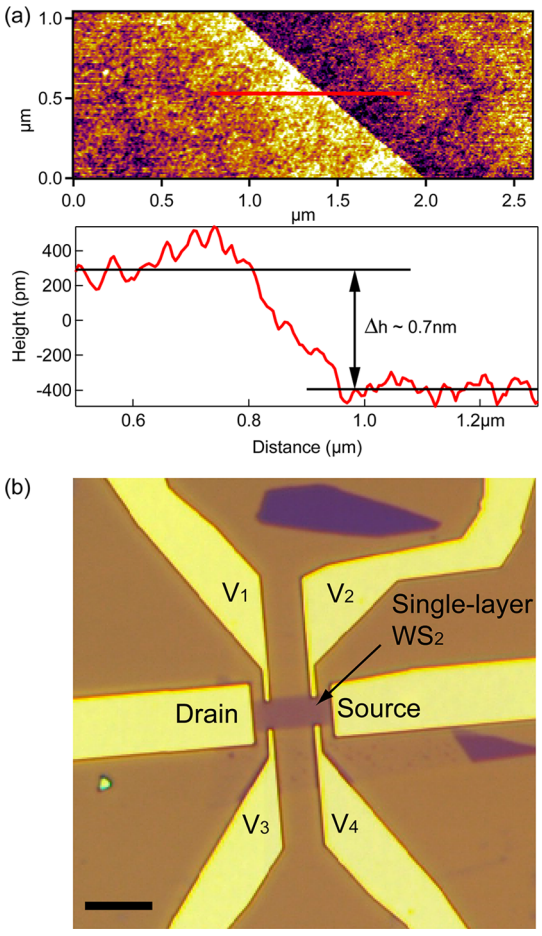

Figure 1. Fabrication of single-layer WS_2 transistors. (a) AFM image of single-layer WS_2 exfoliated on 270 nm of SiO_2 and the corresponding height profile (along the red line), from which a height of 0.7 nm can be extracted. Black lines are guides for the eyes indicating the step height. (b) Optical micrograph of the device presented in this manuscript based on single-layer WS_2 in the Hall bar geometry. Device length $L = 6.8\ \mu$m and width $W = 2.5\ \mu$m. Scale bar is 5 μm long.

pressure with the V_{th} decreasing as the pressure is reduced. At the same time, we notice an improvement of almost 2 orders of magnitude in the ON current after annealing. This indicates that, while doping is sensitive to pressure, *in situ* annealing dramatically improves charge carrier injection from the Au contacts. We further analyze the current−voltage $I_{ds}-V_{ds}$ curves at a fixed gate voltage V_g = 60 V before (Figure 2c) and after (Figure 2d) annealing. While the curve before annealing in vacuum is asymmetric and hysteretic, the $I_{ds}-V_{ds}$ curve after annealing is symmetric, with an increased ON current and reduced hysteresis. We have also studied devices with different contacting materials (Ti/Au and Ag/Au, in addition to Au). The results are presented in Figures S1 and S2a in the Supporting Information and reveal that the devices with Au contacts show highest ON currents and lowest contact resistance.

The dependence of device performance on vacuum conditions and annealing is in agreement with

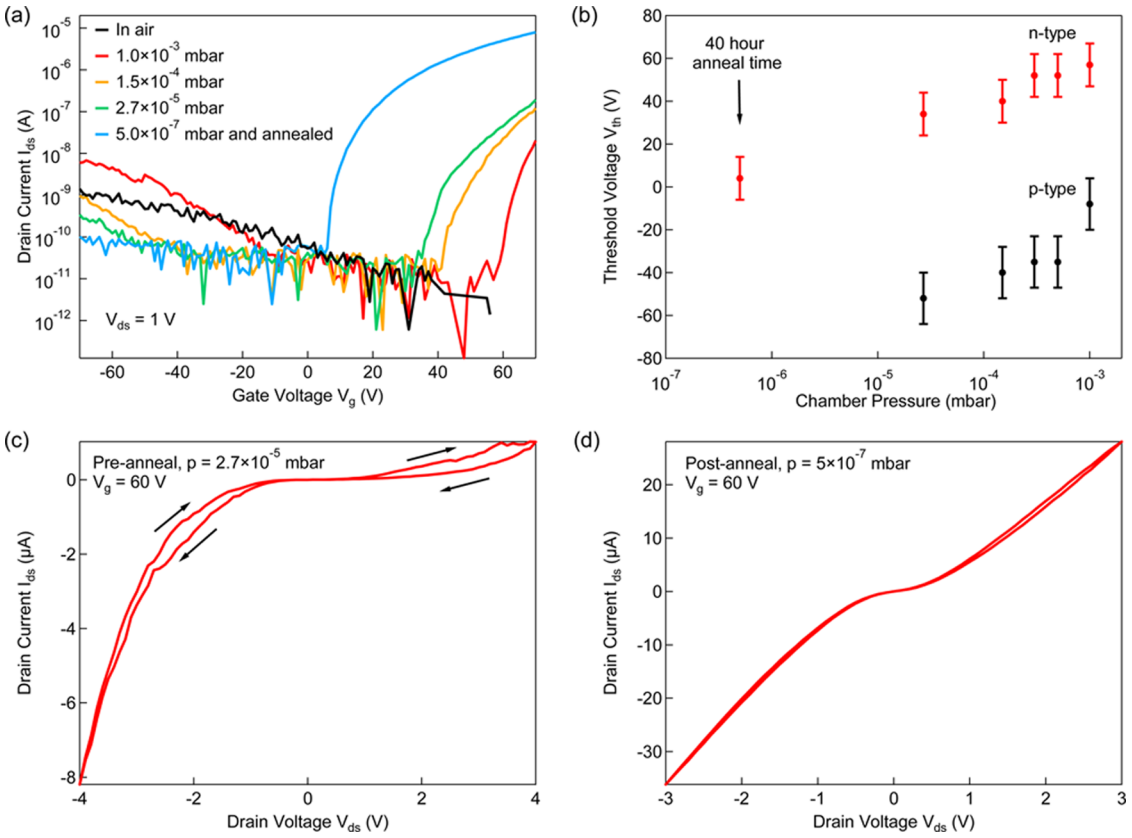

Figure 2. Characterization of a double-layer WS_2 transistor in vacuum and the effect of annealing. (a) Current as a function of gate voltage ($I_{ds}-V_g$) in air, in vacuum, and after annealing. (b) Threshold voltage V_{th} for p-type and n-type conduction as a function of pressure in the system. (c) Dependence of device current I_{ds} on the bias voltage V_{ds} ($I_{ds}-V_{ds}$) for a fixed value of gate voltage V_g = 60 V before annealing in the vacuum chamber. (d) Same as (c), after annealing for 40 h at 115 °C.

previous reports on bilayer[31] and monolayer[17] MoS_2 devices. In these reports, a similar shift of V_{th} was observed and attributed to the presence of adsorbed H_2O and O_2 from the atmosphere and their removal *via in situ* annealing, while recent theoretical calculations predict[32] that the absorption of H_2, O_2, and H_2O on the surface of MoS_2 can result in p-type doping. Our observations confirm that WS_2 devices also show a performance increase following annealing in vacuum. Their performance in atmospheric conditions is however markedly worse than in the case of MoS_2.

In the case of double-layer WS_2, we were able to observe both branches of conductance, while after annealing the p-type transport disappeared due to the shift of V_{th}. Recovery of n-type doping after *in situ* annealing in the WS_2 flakes, grown by vapor phase transport with Br as a transport agent, is in agreement with previous observations of intrinsic doping of synthetically grown[33,34] and natural[14] TMD crystals. The presence of halogen atoms as impurities was recently observed even in natural samples[14] and might be responsible for the excess of electrons in the inspected flakes.

We now turn to single-layer devices. Figure 3 shows the room-temperature characterization of a single-layer WS_2 transistor in vacuum and the effect of *in situ* annealing. This device has a length of 6.8 μm, width of 2.5 μm, and distance between the voltage probes of 3.7 μm. As shown in Figure 2, placing the device in vacuum results in a shift of V_{th} toward negative values, revealing the pristine electronic state of the material, in the absence of strong doping by the adsorbates. Further annealing improves the ON-state current and provides further shift of V_{th}. We perform characterization of a chosen device with different annealing times up to 145 h in vacuum. Figure 3a shows the $I_{ds}-V_g$ curves for different annealing times, while Figure 3b presents the dependence of the sheet conductivity on the back-gate voltage V_g for different annealing times. In Figure 3c we show the extracted two-terminal and four-terminal resistance for the fixed gate voltage for the same device. Interestingly, while the four-terminal resistance reaches saturation after 60−80 h of annealing, the two-terminal resistance keeps decreasing. We also extracted the field-effect mobility μ_{FE} from our four-terminal measurements, using the expression $\mu_{FE} = [d\sigma/dV_g] \times [1/C_{ox}]$, where σ is the sheet conductivity of the channel and $C_{ox} = 1.28 \times 10^{-8}$ F cm^{-2}, the geometric back-gate capacitance per unit area. The values of two-terminal and four-terminal mobility are presented in Figure 3d. While the four-terminal

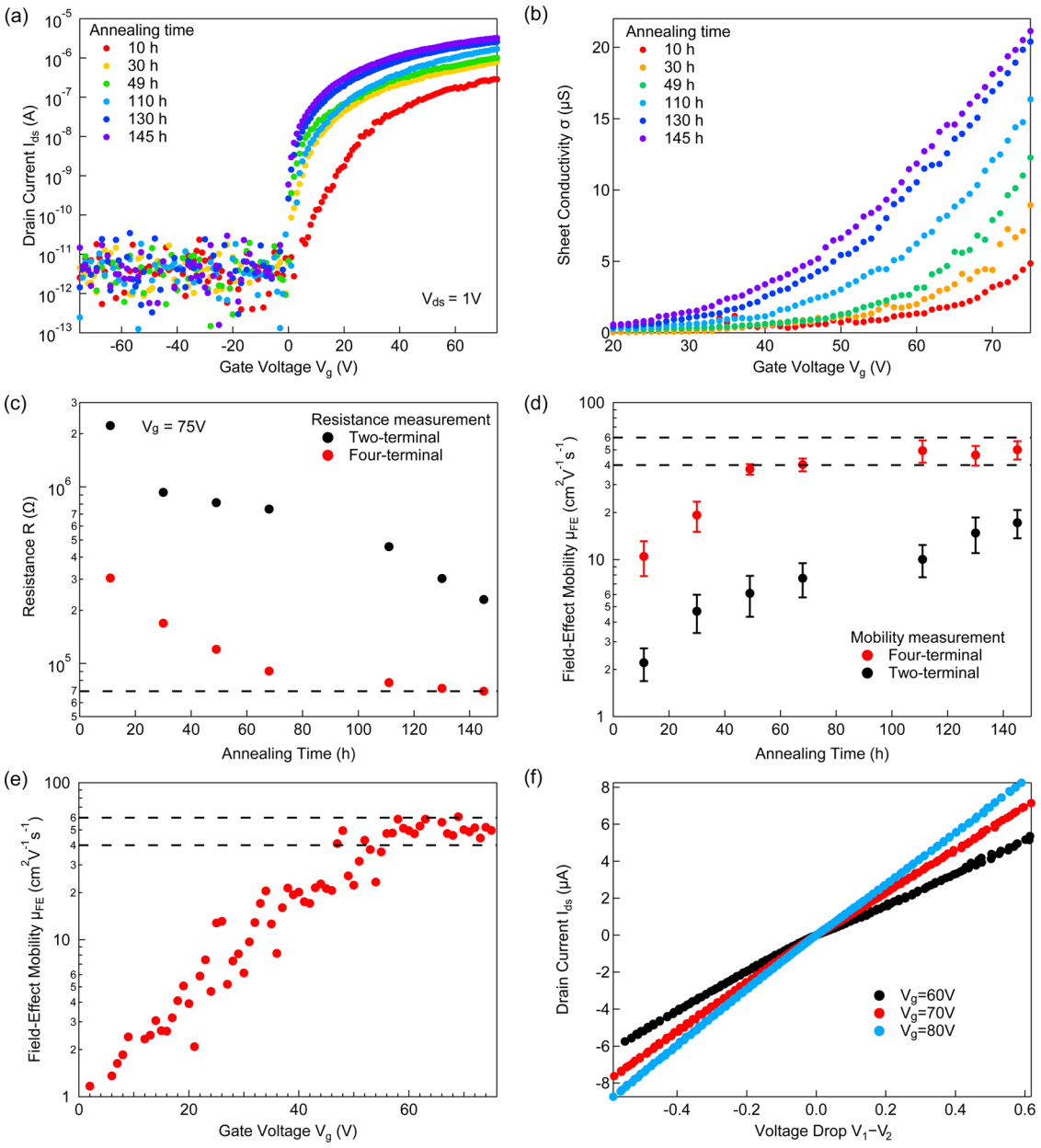

Figure 3. Performance of the single-layer WS_2 transistor in vacuum. (a) Current–voltage I_{ds}–V_g curves for the device recorded at different stages during the annealing process. (b) Sheet conductivity σ as a function of gate voltage V_g for the same annealing times as in (a). (c) Resistance as a function of annealing time at fixed gate voltage (V_g = 75 V). Red markers: four-terminal measurements, black markers: two-terminal measurements. Four-terminal resistance reaches a plateau at ~70 kΩ indicated by the dashed line after 60 h of annealing, while the two-terminal resistance continues to decrease during the entire annealing procedure. (d) Field-effect mobility of single-layer WS_2 *vs* the annealing time. Red markers: four-terminal mobility, black markers: two-terminal mobility. Dashed lines are given as a guide for the range of extracted mobilities. (e) Room-temperature four-terminal mobility, extracted from the red curve in (a) after 145 h of annealing. Dashed lines indicate the range of mobility achieved in the linear regime ($\sigma \approx V_g$). (f) Current *vs* voltage drop between the voltage probes after 145 h of annealing in vacuum. The linear dependence implies the correct measurements of four-terminal mobility.

mobility already saturates at $\mu_{FE} \approx 40\ cm^2\ V^{-1}\ s^{-1}$ after 60 h of annealing, the two-terminal mobility continues to improve gradually. This is in line with our previous observation that the annealing does not influence doping but improves the contact resistance.

Figure 3e presents the extracted value of four-terminal field-effect mobility as a function of the back-gate voltage V_g after the last annealing step (145 h). The values are extracted by numerically differentiating the conductivity, thus introducing noise in the data. We can see that the mobility *vs* V_g reaches a plateau at high V_g, which corresponds to a linear dependence of σ on V_g. This behavior is similar to recent observations in MoS_2 and is an indication of device performance limited by short-range scattering.[35] Dashed lines provide a reference for the minimum and maximum values of mobility in this regime. From this curve, we extract a value for the room-temperature mobility of $\mu_{FE} = 50 \pm 7\ cm^2\ V^{-1}\ s^{-1}$.

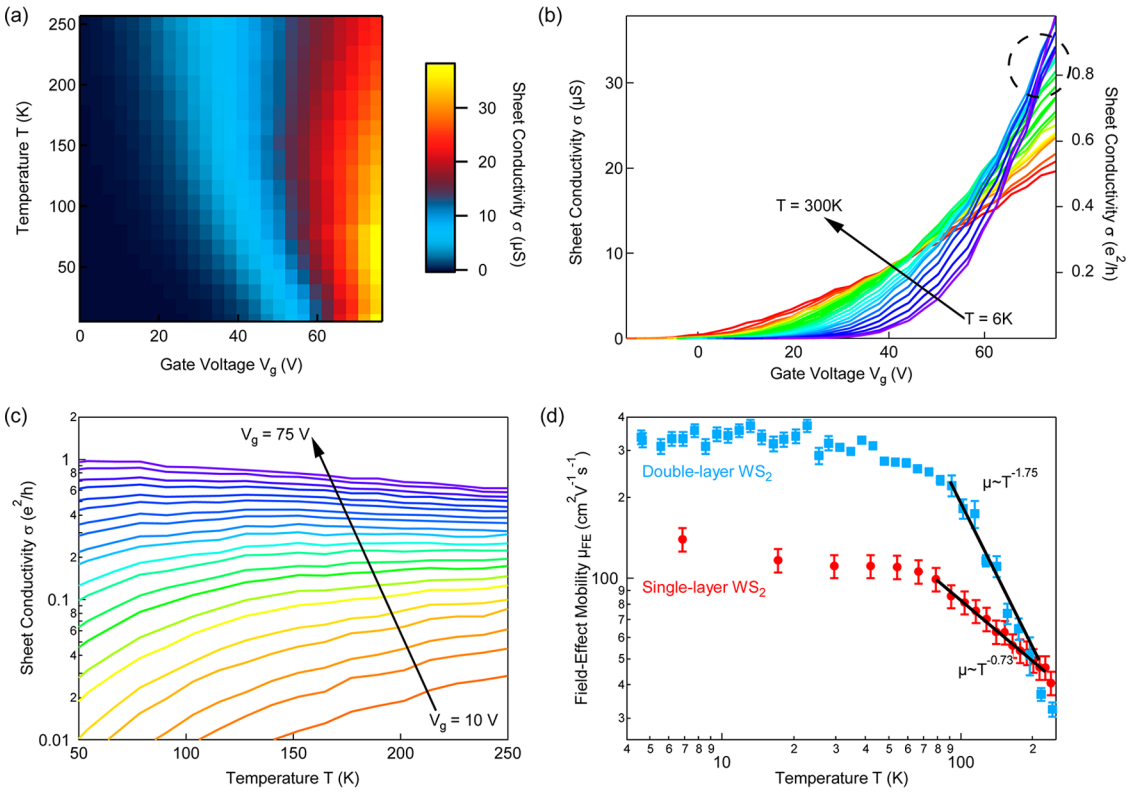

Figure 4. Temperature-dependent electrical characterization of the single-layer WS_2 device. (a) Dependence of the four-terminal sheet conductivity on gate voltage and temperature. The lower left corner exhibits the maximum sheet conductivity, corresponding to high gate voltages and low temperatures. (b) Sheet conductivity *vs* gate voltage (V_g) for different temperatures. The area highlighted with the dashed circle represents the crossover region from the insulating (V_g < 70 V) to the metallic regime (V_g > 70 V) at low temperatures (between 5 and 80 K). (c) Dependence of the sheet conductivity in units of e^2/h on the temperature for different gate voltages. (d) Four-terminal field-effect mobility *vs* temperature extracted from the gate voltage range between 65 and 75 V. Red markers correspond to single-layer WS_2; blue, double-layer WS_2. The solid black lines are fits to the model $\mu \propto T^{-\gamma}$ in the 83−220 K temperature range.

To evaluate the accuracy of these measurements, we show in Figure 3f the drain current as a function of the voltage drop between the two voltage probes (V_1 and V_2). The dependence is linear in the entire range of applied bias voltage V_{ds} (±2 V) for the range of gate voltages V_g, where we extract the field-effect mobility ($V_g \approx 60-80$ V). This confirms that the four-terminal conductivity measurements are reliable and not influenced by Schottky barriers that could be present at the voltage probes. Finally, we estimate the I_{on}/I_{off} ratio for this device after the final step of annealing. The ratio $I_{on}/I_{off} \approx 10^6$, estimated with an applied bias of $V_{ds} = 1$ V (Figure S3b), is larger than previously reported values in the case of multilayer WS_2 (ref 26) because of the enhanced electrostatic control achieved in single layers.

Temperature-Dependent Electrical Transport. After investigating single- and double-layer WS_2 devices in vacuum and at room temperature, we move on to the temperature-dependent study of electronic transport. The devices were annealed in the cryogenic setup until the saturation of the four-terminal mobility could be reached. The four-terminal sheet conductivities as a function of gate voltage V_g and temperature are presented in Figure 4a in the form of a 2D map.

A crossover from an insulating regime at low gate voltages (decrease of conductivity with decreasing temperature) to a metallic regime (increase of conductivity with decreasing temperature) is observed around $V_g \approx 70$ V (see region in dashed circle in Figure 4b). Similar observations have been made in the case of MoS_2 (ref 15). Figure 4c presents the values of sheet conductivity in units of e^2/h, where e is the elementary charge and h the Planck constant. The crossover region between insulating and metallic states corresponds to a value of the sheet conductivity slightly lower than e^2/h. This is consistent with values reported in top-gated[15] as well as back-gated[16] MoS_2 devices.

We now investigate the temperature dependence of the mobility in the metallic regime, presented in Figure 4d. We plot here the four-terminal mobility *vs* temperature T for the single-layer and double-layer device. As the temperature is lowered from 220 K, the field-effect mobility for the single-layer device (double-layer) increases until ≈83 K, where it saturates at 120−140 $cm^2\ V^{-1}\ s^{-1}$ (above 300 $cm^2\ V^{-1}\ s^{-1}$ for the double-layer). In the high-temperature part (83−220 K), the dependence of the mobility on the temperature

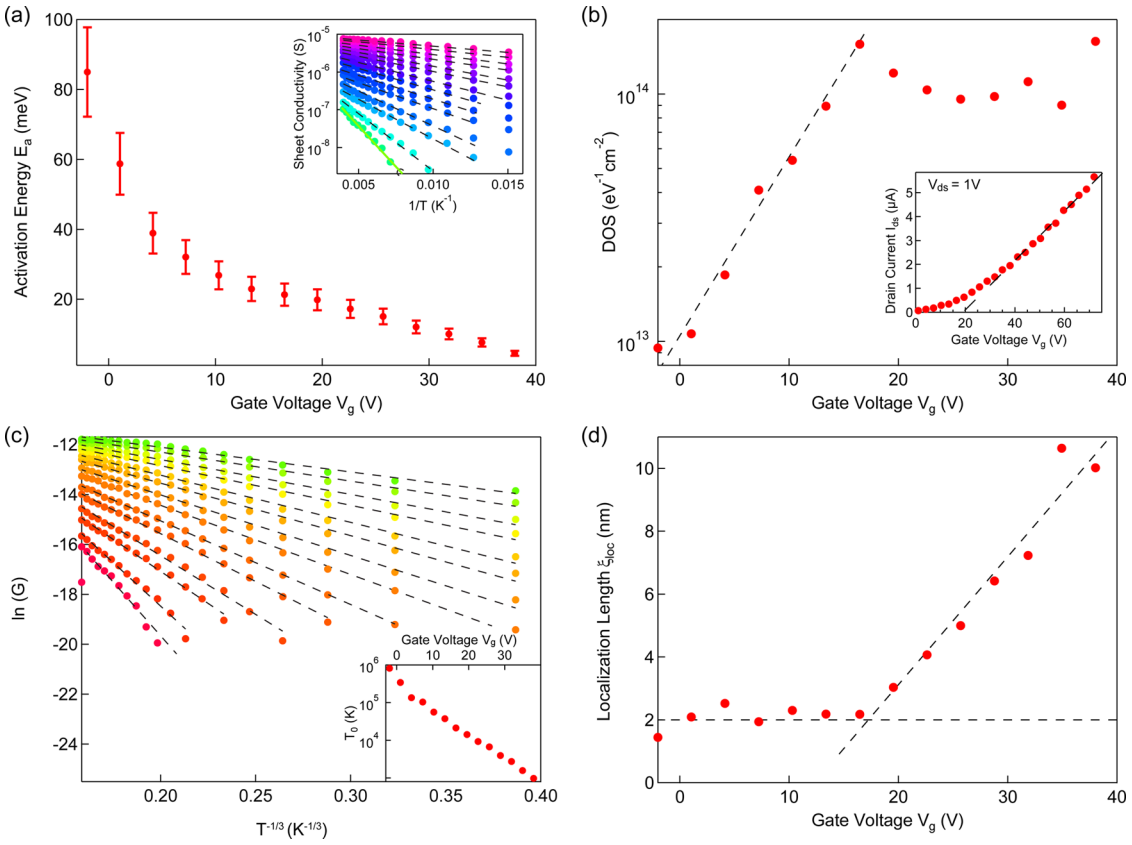

Figure 5. Electrical transport in the insulating regime of single-layer WS_2. (a) Activation energy E_a as a function of gate voltage V_g extracted from the Arrhenius plots of the sheet conductivity (inset) in the high-temperature range. (b) Density of states extracted from the activation energy. Inset: $I_{ds}-V_g$ curve for the same device recorded at room temperature with linear extraction of V_{th} (dashed line). (c) Logarithm of sheet conductivity plotted as a function of $T^{-1/3}$ for different gate voltages. The variable range hopping parameter T_0 (shown in inset) can be extracted from the slopes of the line fits. (d) Dependence of localization length on the gate voltage V_g. Dashed lines are guides for the eye.

follows a power-law dependence $\mu_{FE} \propto T^{-\gamma}$, with a temperature damping factor $\gamma = 0.73$ (fits are shown as black lines in Figure 4d). This value is similar to that reported in encapsulated single-layer MoS_2 (ref 15) and smaller than in unencapsulated single-layer MoS_2 (ref 16). This temperature dependence has been ascribed to a complex interplay between homopolar phonon mode quenching,[36,37] temperature-dependent screening,[38] and charged-impurity scattering.[39] For the double-layer device, the power-law fit results in the damping factor $\gamma = 1.75$, indicating fundamental differences in interaction with phonons and charged impurities in comparison to the single-layer case.

Insulating Regime. The behavior in the insulating regime can be studied in the frameworks of thermally activated and variable-range hopping models. First, from the high-temperature activation behavior (inset of Figure 5a) we can extract the activation energy (Figure 5a) by fitting the sheet conductivity with the expression $G(T) = G_0 e^{-E_a/k_B T}$ where G_0 is a constant, E_a the activation energy, k_B the Boltzmann constant, and T the temperature. This activation energy corresponds to the thermal activation of charge carriers at the Fermi energy into the conduction band. Its dependence on gate voltage thus gives us the dependence of the Fermi energy on gate voltage, *i.e.*, the density of states (DOS) just below the conduction band edge. The variation of the Fermi energy E_F with the gate voltage V_g is $dE_F/dV_g = C_{ox}/(C_{ox} + C_t)$, where C_{ox} is the back-gate capacitance and $C_t = e^2 D(E)$ the quantum capacitance, from which the DOS $D(E)$ could be extracted.

This DOS is shown in Figure 5b. As the gate voltage is decreased, we see that the DOS first assumes a constant value below $D_{2D}^{exp} \approx 2 \times 10^{14}$ eV^{-1} cm^{-2}, close to the expected value for the DOS in the conduction band of WS_2: $D = g_v \times m^*/\pi\hbar^2$,[40] where $g_v = 2$ stands for the valley degeneracy and m^* is the electron effective mass, which we take from recent theoretical calculations to be $m^* = 0.34m_0$.[19] We find $D_{2D}^{theory} = 2.85 \times 10^{14}$ eV^{-1} cm^{-2}. At lower gate voltages, the DOS exhibits an exponential decrease (dashed line in Figure 5b). Such an exponential tail near the conduction band edge has been recently observed in MoS_2.[41] Notice that the drop in the DOS corresponds to the room-temperature threshold voltage measured from the linear extrapolation of the output curve to zero, as shown in the inset of Figure 5b. The values of DOS ($D \approx 10^{13}$ eV^{-1} cm^{-2}) measured around $V_g = 0$ V on the

other hand are comparable with the ones obtained with the same model for monolayer MoS_2 (ref 41), which is in general attributed to the density of trap states inside the gap.

In the lower temperature regime (temperature between 20 and 250 K), the variable range hopping (VRH) model,[42,43] characterized by the expression $\sigma \propto e^{-(T_0/T)^{1/3}}$, can be used to describe electrical transport in the WS_2 device. Using the VRH model, one can extract the localization length $\xi_{loc} = (13.8/k_B D T)^{1/2}$ where D is the density of states.[44] Using the values of D extracted from the high-temperature regime (Figure 5b), together with the values of T_0 extracted from the VRH model (Figure 5c), we can determine the localization length as a function of the gate voltage. As shown in Figure 5d, this value is constant and close to 2 nm, while the E_F stays inside the band gap, in agreement with a recent report in few-layer WS_2.[30] As the gate voltage is increased above the threshold voltage, the localization length starts to linearly increase, indicating the onset of electron delocalization.

CONCLUSIONS

In conclusion, by removing adsorbates and atmospheric contaminants using *in situ* annealing, we could study the electronic properties of pristine single-layer and double-layer WS_2. Our measurements show that WS_2 is a 2D semiconductor with promising electronic properties. A field-effect mobility of $50 \pm 7\ cm^2\ V^{-1}\ s^{-1}$ at room temperature and a current modulation I_{on}/I_{off} of $\sim 10^6$ are comparable to those of single-layer MoS_2. The annealing experiments allowed us to outline the important differences between adsorbate removal and contact annealing. The careful annealing procedure also allowed low-temperature transport measurements to be performed in a four-terminal configuration. We observed a crossover between an insulating and a metallic behavior at high charge densities. The mobility shows a power law dependence on temperature and saturates below 83 K at 140 $cm^2\ V^{-1}\ s^{-1}$ for the single-layer case and above 300 $cm^2\ V^{-1}\ s^{-1}$ for the double-layer case. Transport in the insulating regime was modeled as well, which allowed us to observe the same exponential band-tail in single-layer WS_2 as the one recently inspected in single-layer MoS_2,[41] as well as to extract the localization length. Our results indicate the high quality of presented WS_2 field-effect transistors, on par with similar MoS_2 and WSe_2-based devices.[45,46] The back-gated device configuration used in this work can be further improved by using high-k dielectrics and top gates, which will be the subject of future work.

METHODS

WS_2 single crystals were grown using the vapor-phase transport method,[47] with Br as the transport agent. Ultrathin WS_2 flakes were obtained by micromechanical cleavage of these crystals on degenerately doped n++ silicon covered with 270 nm thermally grown SiO_2. The thickness of the crystals was determined by noncontact mode atomic force microscopy (AFM) (Figure 1a) and correlated with optical contrast between the crystal and the substrate. Single- and double-layer WS_2 crystals were located, and six-terminal devices were fabricated using electron-beam lithography (EBL), followed by thermal evaporation of 90 nm thick Au contacts. Other metals, in particular Ti/Au (2/50 nm) and Ag/Au (5/45 nm) stacks, were studied as well, with results presented in Supporting Information Figure S1. The samples were subsequently annealed to reduce the contact resistance in Ar/H_2 flow.[4] Some devices with irregular shape were further patterned using a second step of EBL, followed by O_2 plasma etching. Several steps of thermal annealing were performed in vacuum at a base pressure of 10^{-6} mbar to remove adsorbates and approach the pristine state of the material. Four-terminal electrical measurements were performed to remove the influence of contact resistance.

AFM imaging is performed using an Asylum Research Cypher AFM. After Au contact deposition, devices are annealed in 100 sccm Ar and 10 sccm H_2 flow at 200 °C for 2 h. Electrical characterization is carried out using an Agilent E5270B parameter analyzer and a home-built vacuum annealing setup at a base pressure of 10^{-6} mbar. Cryogenic measurements were performed in an Oxford Instruments Heliox cryo-magnetic system.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Performance of devices in vacuum, comparison of device performance for different contact metals, and dependence of mobility as a function of annealing time. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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