Enhanced Interpolated-DFT for Synchrophasor Estimation in FPGAs: Theory, Implementation, and Validation of a PMU Prototype

Paolo Romano, *Student Member, IEEE*, and Mario Paolone, *Senior Member, IEEE*

***Abstract*— The literature on the subject of synchrophasor estimation (SE) algorithms has discussed the use of interpolated discrete Fourier transform (IpDFT) as an approach capable to find an optimal tradeoff between SE accuracy, response time, and computational complexity. Within this category of algorithms, this paper proposes three contributions: 1) the formulation of an enhanced-IpDFT (e-IpDFT) algorithm that iteratively compensates the effects of the spectral interference produced by the negative image of the main spectrum tone; 2) the assessment of the influence of the e-IpDFT parameters on the SE accuracy; and 3) the discussion of the deployment of IpDFT-based SE algorithms into field programmable gate arrays, with particular reference to the compensation of the error introduced by the free-running clock of A/D converters with respect to the global positioning system (GPS) time reference. The paper finally presents the experimental validation of the proposed approach where the e-IpDFT performances are compared with those of a classical IpDFT approach and to the accuracy requirements of both P and M-class phasor measurement units defined in the IEEE Std. C37.118-2011.**

***Index Terms*— Discrete Fourier transform (DFT), field programmable gate array (FPGA), IEEE Std. C37.118, interpolated discrete Fourier transform (IpDFT), phasor measurement unit (PMU), synchrophasor.**

I. Introduction

THE core component of a phasor measurement unit (PMU) is represented by the synchrophasor estimation (SE) algorithm, whose choice is driven by three main factors: 1) its accuracy; 2) its response times; and 3) its computational complexity [1].

Concerning points 1) and 2) PMUs need to be compliant with the requirements imposed by the IEEE Std. C37.118.1-2011 [2]. This standard defines synchrophasor, frequency, and rate of change of frequency (ROCOF) measurements as well as accuracy limits for the majority of operating conditions under both steady-state and dynamic conditions. In this respect, the above mentioned IEEE Std. has also introduced the well-known PMU performance classes P and M. In particular, class-P PMUs are devices whose applications require fast response and no explicit filtering (i.e., power systems protections), whereas class-M PMUs are devices intended for applications that could be undesirably effected by aliased signals and do not require a fast response time.

As known, the main task of a SE algorithm is to assess the parameters of the fundamental tone of a signal using a previously acquired set of samples representing a portion of an acquired waveform (i.e., node voltage and/or branch/nodal current). For this reason, points 1) and 2) are inherently coupled and, usually, better accuracies imply larger response times and vice versa. In addition, as the phasor is, by definition, a static representation of a sinusoidal waveform, the SE might be largely biased when the grid frequency drifts from the nominal one and, more generally, during network dynamic conditions. To cope with 1) and 2), different techniques have been proposed as summarized below.

Typically, most of the SE algorithms are based on the direct implementation of the discrete Fourier transform (DFT), or its algorithmic version—fast Fourier transform (FFT)—applied to quasi-steady state signals. Based on the window length, DFT-based algorithms can be grouped into multicycle, one-cycle, or fractional-cycle DFT estimators performing recursive and nonrecursive updates [3]–[5]. To improve their accuracy, DFT-based algorithms can be used in combination with weighted least-squares [6] or Kalman filter-based methods [7]. Non-DFT-based SE methods have also been proposed. These include wavelet-based algorithms [8] and those based on the more recent dynamic phasor concept. The latter have been proposed stand-alone [9] or in combination with other techniques like, for instance, signal subspace [10], weighted least-squares [11], [12] or adaptive filters methods [13].

Within the category of DFT-based SE algorithms, to achieve an optimal tradeoff between the estimation accuracy and response time, the use of time-windows in combination with the well-known interpolated-discrete Fourier transform (IpDFT) technique has been first proposed in [14] and [15] and further developed in [16]–[19]. More in particular, contributions [18] and [19] have proven that the effects of long and short-range leakage can be considerably minimized by adopting suitable windows functions and IpDFT schemes, respectively, [20], [21]. The advantages of this kind of approaches refer to the relatively simple implementation and low-computational complexity capable of achieving reasonable

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The authors are with the Distributed Electrical System Laboratory, École Polytechnique Fédérale de Lausanne, Lausanne CH-1015, Switzerland (e-mail: paolo.romano@epfl.ch; mario.paolone@epfl.ch).

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accuracy and response times after a careful selection of the algorithm parameters.

However, the majority of these references has neglected the effects of the spectral interference when formulating the SE algorithm. This phenomenon is associated to the long-range spectral leakage and is responsible of the cross-influence among all the various tones composing the signal spectrum. If the specific PMU application requires high-accuracy levels, neglecting this phenomenon can cause non-negligible errors in the SE.

In addition, with reference to the previously-listed point 3), few of the above-mentioned references have considered the computational complexity of the proposed methods and, to the best of our knowledge, none of them has addressed the problem of its effective deployment into embedded systems.

Within this context and based on what was preliminarily presented in [22], this paper illustrates in details: 1) the analytical formulation; 2) the implementation; and 3) the experimental validation of a DFT-based SE algorithm, hereafter called enhanced-IpDFT (e-IpDFT). The algorithm, specifically designed for highly accurate PMUs, has been designed to meet the accuracy limits of P-class PMUs but, also, to satisfy the majority of M-class PMUs requirements. It extends the DFT-interpolation scheme proposed in [15] by considering the effects of the spectral interference produced by the negative image of the main spectrum tone and compensating it by means of the iterative process proposed in [23]. In particular, with respect to [22], this contribution presents and analyzes in details the following additional items.

1) The analytical comparison between the e-IpDFT algorithm and the IpDFT method proposed in [15].
2) The analytical formulation and experimental validation of a ROCOF estimator, suitably-designed to maintain high-accuracy levels in every typical operating condition.
3) A detailed analysis of the algorithm sensitivity to both its sampling frequency and window length and the description of the criteria applied to find a set of parameters that optimizes the e-IpDFT algorithms performances.
4) The nontrivial aspects related to the the deployment of e-IpDFT-based algorithms into a field programmable gate array (FPGA)-based PMU prototype, with particular reference to the compensation of the error introduced by the free-running clock of A/D converters on the estimated synchrophasor's phase and frequency.
5) A complete metrological characterization of the proposed PMU prototype, in which the performances of the e-IpDFT algorithm are compared with those of the classical IpDFT approach proposed in [15] and to the IEEE Std. limits [2].

The structure of this paper is as follows. Section II provides the analytical description of the proposed e-IpDFT SE algorithm. Then, Sections III and IV present the algorithm parameter selection and its deployment into an FPGA-based PMU prototype, respectively. Section V comments the experimental results of the obtained PMU prototype with respect to the majority of the compliance tests defined in [2]. Finally, Section VI concludes this paper with the remarks and the conclusions.

II. e-IpDFT-Based SE Algorithm

A. Theoretical Background

DFT-based SE algorithms are notoriously characterized by two main sources of error: 1) aliasing and 2) spectral leakage.

Aliasing is usually corrected by two possible approaches: 1) using adequate anti-aliasing filters or 2) increasing the sampling frequency to values much larger than the highest spectrum component contained in the sampled signal.

On the other hand, spectral leakage arises when the sampling process is not synchronized with the fundamental tone of the signal under analysis and the DFT is computed over a noninteger number of cycles of the input signal [21]. Since accurately synchronizing the sampling process with the fundamental frequency component of the signal is purely theoretical, several approaches have been applied to reduce this bias. Mainly these methods refer to the usage of: 1) windowing functions aiming at mitigating the effect of long-range leakage [20] and 2) proper DFT interpolation schemes aiming at correcting the effects of the short-range leakage and reducing the inaccuracies introduced by the DFT frequency resolution [14], [15]. In addition, if long-range leakage is not properly compensated by windowing, an additional source of error is associated to the presence of cross interaction between spectrum tones that are very close each other, the so-called spectral interference [23], [24].

Based on these considerations, the proposed e-IpDFT algorithm combines three different approaches to reduce the impact of the previously described sources of error: 1) windowing; 2) DFT-interpolation; and 3) iterative process for the compensation of the spectral interference generated by the negative image of the main frequency component of the signal. In the following sections a detailed description of the proposed SE algorithm is given.

B. Classical IpDFT Formulation

Typically, a power system quantity (i.e., branch/nodal current or node voltage) can be modeled as a signal characterized by a main tone fluctuating around the rated frequency of the system (i.e., 50 or 60 Hz). The signal is sampled by the PMU each $t_s = 1/f_s$ (being f_s the PMU sampling frequency), and collected over the time window $T = N \cdot t_s$ ($N \in \mathbb{N}$) sufficiently short so that the signal can be assumed stationary within it:

$$s(n) = A_1 \cos(2\pi f_1 n t_s + \varphi_1), \quad n \in [0, N-1] \qquad (1)$$

where A_1, f_1, and φ_1 are the amplitude, frequency, and phase of the main tone of the spectrum that are supposed to be constant over the whole observation interval.

It should be noticed that the signal model expressed by (1) is consistent with the IpDFT analysis that will be presented in next sections, but does not necessarily match the characteristics of realistic power-system signals. Indeed, these are typically characterized by several orders of distortion, including: 1) superposed harmonics and interharmonics components; 2) superposed decaying DC offset; 3) amplitude and

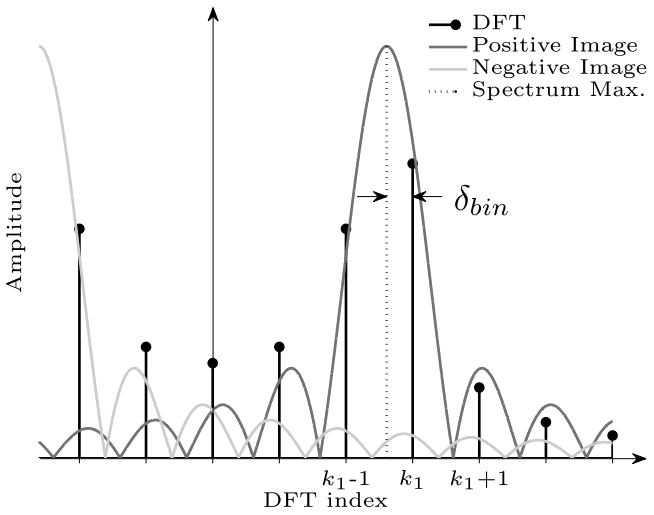

Fig. 1. Definition of δ_{bin} and qualitative representation of short- and long-range spectral leakage.

phase modulation; 4) frequency sweep; and 5) amplitude or phase step.

Let us also suppose that signal frequency satisfies the following inequality:

$$|f_1 - f_0| \leq \frac{\delta_f}{2} \tag{2}$$

where f_0 is the rated frequency of the system (i.e., 50 or 60 Hz) and, as it will be clarified next, δ_f is the DFT frequency resolution. This hypothesis guarantees that the location of the DFT maximum is fixed for typical PMU operating conditions, simplifying considerably the algorithm's formulation and implementation.

If $\{w(n)\}$ is the adopted window sequence, then the DFT of (1), can be expressed as

$$S(k) = \frac{1}{B}\sum_{n=0}^{N-1} w(n)\cdot s(n)\cdot e^{-jk\beta_n}, \quad k \in [0, N-1] \tag{3}$$

where $B = \sum_{n=0}^{N-1} w(n)$ and $\beta_n = (2\pi n)/N$. Because of its intrinsic simplicity, in what follows we make reference to a classical Hann window function [20].

To estimate the main tone frequency f_1 and the related synchrophasor (i.e., its amplitude A_1 and phase φ_1) the signal spectrum can be interpolated within the frequency interval defined by (2). In particular, as the true frequency value f_1 may fall between two subsequent DFT bins, it can be expressed as a function of the DFT frequency discretization step $\delta_f = 1/T$ as

$$f_1 = (k_1 + \delta_{\text{bin}})\cdot \delta_f \tag{4}$$

where $-0.5 < \delta_{\text{bin}} \leqslant 0.5$ is the deviation of f_1 from the relative DFT maximum $k_1\delta_f$ (Fig. 1). As shown in [24], based on the hypothesis of adopting a sampling frequency that is much larger than the fundamental tone frequency ($f_s \gg f_0$), δ_{bin} can be expressed with the following linear interpolation formula:

$$\delta_{\text{bin}} = \varepsilon \cdot \frac{2-\alpha}{1+\alpha} \tag{5}$$

where α is the ratio between the highest and second highest tone magnitudes of the DTF spectrum

$$\alpha = \frac{|S(k_1)|}{|S(k_1+\varepsilon)|} \tag{6}$$

being $\varepsilon = \text{sign}\left(|S(k_1+1)| - |S(k_1-1)|\right)$.

In agreement with [24], an estimate of the set of parameters $\{f_1, A_1, \varphi_1\}$ can be given on the basis of (4) and the following relationships:

$$A_1 = 2\,|S(k_1)|\cdot \frac{\pi\delta_{\text{bin}}\cdot\left(1-\delta_{\text{bin}}^2\right)}{\sin(\pi\delta_{\text{bin}})} \tag{7}$$

$$\varphi_1 = \angle S(k_1) - \pi\delta_{\text{bin}}. \tag{8}$$

C. e-IpDFT Formulation

As anticipated in Section II, the spectral leakage is also responsible of the so-called spectral interference, i.e., a cross influence of the various tones composing the frequency spectrum. As a consequence, the bins $S(k_1)$ and $S(k_1+\varepsilon)$ are not only originated by the main tone of $s(t)$, but also influenced by the tails produced by the other tones composing the signal spectrum [14]. In particular, this phenomenon is amplified when the long-range spectral leakage is significant and cannot be properly compensated by a suitably-chosen window function. Since classical IpDFT-based methods, like those presented in [14]–[19], usually neglect the effect of this phenomenon when estimating the synchrophasor, they might be corrupted by the previously described bias.

Within this context, the scope of this section is presenting an approach, called e-IpDFT, capable of estimating and compensating for the spectral interference produced by the negative image of the main spectrum tone.

Indeed, by choosing a sampling rate f_s that is assumed to be much larger than the nominal frequency of the system f_0, the positive and negative images of the main spectrum tone turn out to be very close to the DC component and therefore each other. As a consequence (Fig. 1), the highest and second highest bins of the spectrum $\{S(k_1), S(k_1+\varepsilon)\}$ are produced by two main contributions: 1) the main lobe of the fundamental frequency tone and 2) the tails of the corresponding negative spectrum image (i.e., the so-called self-interaction). Based on this assumption, the DFT spectrum can be expressed in terms of the positive and negative images of the main frequency tone [24] and the following relation can be derived:

$$S(k) = \frac{1}{B}\left[V_1\cdot W\left(\frac{k\Delta f - f_1}{\Delta f}\right) + V_1^*\cdot W\left(\frac{k\Delta f + f_1}{\Delta f}\right)\right] \tag{9}$$

where $V_1 = (A_1/2j)\,e^{j\varphi_1}$, V_1^* is its complex conjugate and $W(f)$ represents the Fourier transform of the selected windowing sequence, that, for the case of the Hann window, is

$$W_H(k) = -0.25\cdot W_R(k-1) + 0.5\cdot W_R(k) - 0.25\cdot W_R(k+1) \tag{10}$$

being W_R the Fourier transform of the rectangular window

$$W_R(k) = e^{-j\pi k(N-1)/N}\cdot\frac{\sin(\pi k)}{\sin(\pi k/N)}. \tag{11}$$

Replacing (4) in (9), the highest and second highest bins can then be approximated as

$$S(k_1) = \frac{1}{B}\left[V_1 \cdot W(-\delta_{\text{bin}}) + V_1^* \cdot W(2k_1 + \delta_{\text{bin}})\right] \tag{12}$$

$$S(k_1 + \varepsilon) = \frac{1}{B}\left[V_1 \cdot W(\varepsilon - \delta_{\text{bin}}) + V_1^* \cdot W(2k_1 + \varepsilon + \delta_{\text{bin}})\right] \tag{13}$$

where the spectral interference coming from the corresponding negative spectrum image is represented by

$$\Gamma \triangleq \frac{1}{B} \cdot V_1^* \cdot W(2k_1 + \delta_{\text{bin}}) \tag{14}$$

$$\Omega \triangleq \frac{1}{B} \cdot V_1^* \cdot W(2k_1 + \varepsilon + \delta_{\text{bin}}). \tag{15}$$

Based on the initial parameters set $\{f_1, A_1, \varphi_1\}$ given by (4), (7), and (8), the amount of self-interaction between the negative and positive spectrum images can be computed and subtracted form the original bins to obtain an improved α estimate ($\widetilde{\alpha}$)

$$\widetilde{\alpha} = \frac{|\widetilde{S}(k_1)|}{|\widetilde{S}(k_1 + \varepsilon)|} = \frac{|S(k_1) - \Gamma|}{|S(k_1 + \varepsilon) - \Omega|}. \tag{16}$$

This process can be either iterated a predefined number of times or performed until a given convergence criterion is achieved and bring to a more accurate and final estimation for the set of parameters $\{f_1, S_1, \varphi_1\}$.

In the proposed implementation (see Section IV), due to the stringent time requirements, this correction is iterated only once. As demonstrated in the experimental validation presented in Section V, this single-iteration correction is enough to improve considerably the algorithm performances.

D. ROCOF Estimator

The ROCOF can be computed through any finite difference formula for the approximation of the analytical derivative of the estimated frequency. To minimize its impact on the ROCOF response time, a classical backward first-order approximation of a first-order derivative was chosen

$$\dot{f}(n) = \frac{f_1(n) - f_1(n-1)}{T_{\text{RR}}} \tag{17}$$

where $T_{\text{RR}} = 1/f_{\text{RR}}$, being f_{RR} the PMU reporting rate.

Since finite-difference formula are well known for deteriorating the signal-to-noise ratio of the input quantity, (17) may degrade the ROCOF estimation well outside the accuracy limits specified by [2] (particularly when the system is in steady-state conditions where the IEEE Std. requirements are more demanding). In view of this, the proposed ROCOF estimator is characterized by an additional stage that, based on the detected state of the targeted power system quantity, performs the smoothing of the estimated $\dot{f}(n)$ by means of a low-pass filter (LPF). If the PMU detects dynamic conditions, $\text{ROCOF}(n) = \dot{f}(n)$ and the LPF is bypassed. If the PMU detects static conditions, $\text{ROCOF}(n) = \text{LPF}(\dot{f}(n))$ (Fig. 2).

More specifically, the detection of a superposed transient to the synchrophasor is implemented as a finite-state machine characterized by two states {S1, S2}, associated to static and dynamic conditions, respectively. The transition between the two states is based on the instantaneous values of the first $\dot{f}(n)$ and second-order derivatives $\ddot{f}(n)$ of the estimated frequency with respect to the threshold values $\{th_1, th_2, th_3\}$.

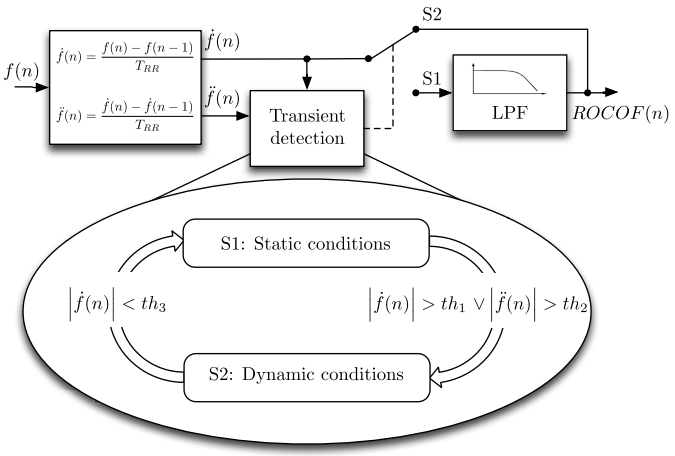

Fig. 2. Block scheme of the proposed ROCOF estimator and finite-state machine representation.

TABLE I
VALUES OF THE PARAMETERS USED IN THE ROCOF ESTIMATOR

a_1	b_0	b_1	th_1 [Hz/s]	th_2 [Hz/s^2]	th_3 [Hz/s]
-0.5913	0.2043	0.2043	3	25	0.035

On the other hand, the LPF has been implemented as a first-order infinite impulse response LPF that, as known, can be described in terms of the following difference equation:

$$y(n) = b_0 x(n) + b_1 x(n-1) - a_1 y(n-1) \tag{18}$$

being x and y the input and output of the LPF and a_i and b_i the feedback and feedforward filter coefficients, respectively.

The threshold values $\{th_1, th_2, th_3\}$, together with the LPF coefficients $\{a_1, b_0, b_1\}$, have been suitably tuned in to order remove as much as possible the estimation noise, without affecting the transient behavior of the ROCOF. As an example, their values for a reporting frequency of 50 frames-per-second fps are given in Table I.

III. SELECTION OF THE ALGORITHM PARAMETERS

As it can be expected, the performances of the e-IpDFT algorithm, in both static and dynamic conditions, might be influenced by the choice of two parameters: 1) its sampling frequency f_s and 2) its window length T. Their optimal selection is constrained by several factors, mainly represented by: 1) the assumptions behind the algorithm formulation (see Section II); 2) the accuracy and response times requirements defined in the IEEE Std. C37.118.1-2011 [2]; and 3) the computational limits of the chosen hardware platform.

In what follows, Section III-A and III-B discusses the sensitivity of the e-IpDFT algorithm to both the sampling frequency f_s and the window length T and define a meaningful range for both parameters by considering the above-mentioned points 1) and 2). Indeed, point 3) depends on the choice of the

embedded system that will host the SE algorithm and cannot be discussed in this Section. Finally, Section III-C presents a procedure to quantify the impact of the sampling frequency f_s and window length T on the accuracy of the proposed e-IpDFT approach and identify an optimal set of parameters.

A. Algorithm Sensitivity to Sampling Frequency

The sampling frequency f_s must first satisfy the hypothesis behind the formulation of the interpolation scheme (i.e., $f_s \gg f_0$). Indeed, the δ_{bin} formula illustrated in (5) is as accurate as the ratio f_0/f_s gets smaller.

In addition, the sampling frequency must be chosen sufficiently high to avoid aliasing effects on the acquired signal and disregard the presence of relevant filters that are generally causing a worsening of the PMU accuracy. Since in steady state the highest harmonic components that characterize the spectrum of distorted voltage/current signals in power systems rarely exceed 10 kHz, according to the Nyquist–Shannon theorem, the following analysis has been focused on the sampling frequencies range between 1 and 50 kHz.

B. Algorithm Sensitivity to Window Length

The window length T defines the DFT frequency resolution $\delta_f = 1/T$ that, in turn, determines the feasibility of the proposed interpolation scheme. Indeed, to estimate the exact position of the main spectrum tone, the DFT maximum needs to be detectable. This is not the case when considering windows shorter than two periods of the main frequency component as they do not guarantee this hypothesis in every operating condition. In this respect, the lower bound for T is a window containing two periods of a signal at the rated system frequency f_0. On the other hand, to satisfy the assumption behind (2) for typical PMU operating conditions (i.e., $|f_1 - f_0| \leq 5$ Hz), it is clear that T cannot contain more than 5 cycles of a signal at the rated system frequency f_0.

In addition, the window length affects the PMUs performances during dynamic transients (i.e., the PMU response times). Namely, a PMU characterized by a long window is generally more accurate in static conditions but, simultaneously, it is characterized by slower response times to step changes in the input signals. As a consequence, the window length must be chosen in a tradeoff between the desired accuracies of the proposed algorithm and the PMU response times to dynamic conditions of the power system.

Finally, it is worth mentioning that a window containing an integer number of periods of the main frequency component, helps in reducing the effects of spectral leakage particularly when $f_1 \approx f_0$. In this respect and based on the above-listed considerations, the optimal selection of T has been limited to windows containing 2–5 cycles of a signal at the rated system frequency f_0.

C. Simulation Results

To quantify the influence of the two parameters on the e-IpDFT algorithm accuracy and response times, the algorithm has been simulated on a general purpose computer with floating-point accuracy. In particular, to stress the e-IpDFT capability in compensating the effects of the spectral leakage, a single-tone signal, characterized by a rated frequency $f_0 = 50.1$ Hz, was used.

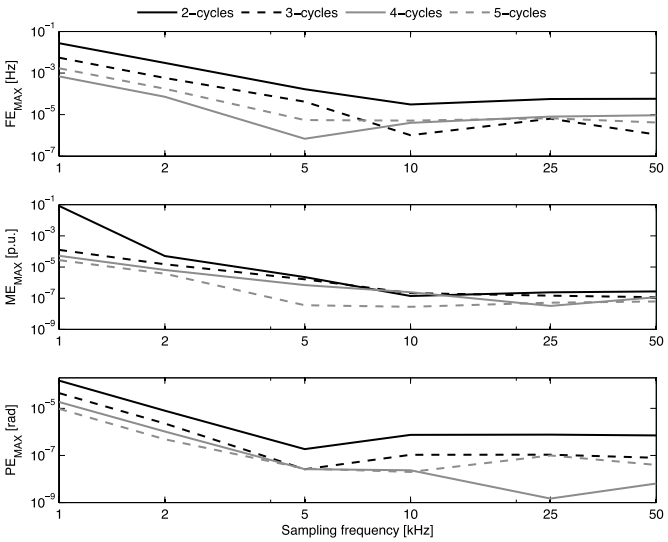

Fig. 3. Simulation results for the assessment of the influence of both sampling frequency and window length on the SE accuracy.

The simulation results are shown in Fig. 3. It shows the maximum errors in the frequency, magnitude, and phase estimations as a function of the sampling frequency over the previously defined range [1, 50] kHz. In particular, based on the above-listed considerations, Fig. 3 shows the simulation results obtained with window lengths containing 2–5 cycles of a signal at the rated system frequency f_0.

Fig. 3 shows the following trend: 1) the e-IpDFT algorithm performances increase by increasing the sampling frequency f_s and 2) the number of cycles (i.e., the window length T). In particular, it is visible how the magnitude error monotonically decrease as a function of the sampling frequency, whereas the frequency and phase errors exhibit a constant behavior for sampling frequencies larger than 10 kHz. In general, by adopting a sampling frequency of 50 kHz, the errors are reduced by at least three orders of magnitude, with respect to a similar e-IpDFT estimator characterized by a sampling frequency of 1 kHz.

In view of the above and to satisfy the requirements of the IEEE Std. C37.118.2011 in terms of response time for class-P PMUs, an observation time window containing three periods of a signal at the rated system frequency f_0 and a sampling frequency of 50 kHz were selected. Nevertheless, it is also worth noting that the same algorithm can provide lower, but still satisfactorily performances by reducing the sampling frequency. This peculiarity of the e-Ip-DFT enables its deployment in hardware platforms characterized by different performances.

IV. Algorithm Deployment Into an FPGA-Based PMU Prototype

The SE algorithm has to be integrated into a PMU prototype that needs to include, at least, the following

hardware units: 1) a set of A/D converters; 2) a time-synchronization unit; 3) a processing unit hosting the SE algorithm; and 4) a network interface for the synchrophasor data streaming. In particular, as for point 3), the availability of advanced and time-deterministic computational platforms like FPGAs, justifies the definition of dedicated algorithms for the SE deployed in this specific hardware. In this respect, this section focuses on the adaptation of the proposed e-IpDFT algorithm to an FPGA-based PMU prototype.

Regardless of the chosen hardware platform, the PMU processing unit needs to implement at least three parallel processes performing: 1) the PMU synchronization with an absolute time reference; 2) the signal acquisition and buffering; and 3) the SE based on the chosen algorithm. In what follows, a detailed description of the deployment of the proposed e-IpDFT algorithm into an FPGA-based prototype, is illustrated with respect to the above-listed processes.

A. UTC-Time Synchronization

As known, synchrophasor measurements need to be referenced to a common UTC-time source to provide accurately time-tagged measurements [2]. In this respect, the PMU time synchronization can be achieved by means of several kinds of technologies like: 1) ethernet-based timing protocols (e.g., IEEE 1588 [25] and NTP/SNTP [26]); 2) serial time-codes (e.g., IRIG-B [27]); or 3) satellites-based systems (e.g., global positioning system (GPS), GLONASS, and Galileo [28]). In what follows, the PMU time-synchronization is performed using the GPS because of its accuracy, stability, and relatively low cost.

Regardless of the chosen technology, several approaches to provide synchronized measurements of synchrophasor, frequency and ROCOF exist. In general, they can be separated in two categories: 1) direct synchronization of the sampling process to the UTC-time by means of dedicated phase-locked-loop circuitry and 2) free-running sampling process integrated with an *a posteriori* synchronization. Among them, the second one has been adopted in the proposed PMU prototype, because of its generality and intrinsic simplicity.

To perform the above mentioned *a posteriori* synchronization, both the signal acquisition and SE are triggered by the rising edge of a GPS-pulse-per-second (PPS) synchronized square waveform (named hereafter subPPS) characterized by a frequency $f_{\text{subPPS}} = f_{\text{RR}}$ (Fig. 4).

B. Signal Acquisition and Buffering

To achieve the highest IEEE Std. [2] reporting rate requirements (i.e., a new estimation every nominal power system period) with the proposed multicycle e-IpDFT algorithm, the only solution is to process partially overlapped portions of data. In particular, based on the chosen window length containing three periods (see Section III) of a signal at the rated system frequency, these requirements can be satisfied by adopting a four stages pipeline architecture for each input channel. As shown in Fig. 4, based on the subPPS rising edge, each pipeline alternately collects the required amount of data (N samples) in dedicated memories and, once they have been filled, activates a flag that triggers the SE on the previously acquired set of data.

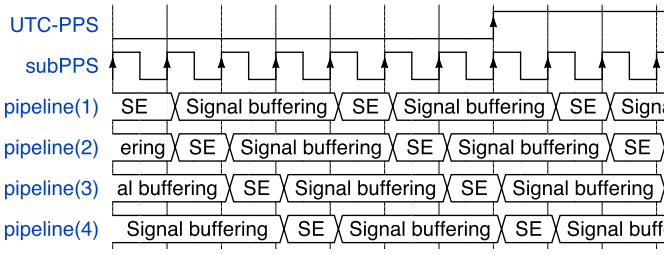

Fig. 4. Digital timing diagram of the proposed PMU architecture (SE).

As previously mentioned, the approach proposed in this section considers a free running sampling process. This approach, besides simplifying the PMU architecture, introduces unavoidable timing issues that, based on the fact that PMUs are inherently equipped with accurate timing units like GPS, can be compensated.

1) Phase Offset Compensation: A common problem occurring when a free running clock is used for the signal acquisition refers to the fact that the synchrophasor phase is known with an accuracy that, neglecting the uncertainties due to the SE algorithm, is correlated to the sampling time t_s. In particular, such an uncertainty corresponds, for $f_s = 50$ kHz and a rated system frequency of 50 Hz, to a bias up to 2π mrad (0.36°). In this respect, the algorithm applies a further step on the FPGA level to improve the estimation of the synchrophasor phase φ_1: since the sampling of $s(t)$ is triggered in correspondence of a rising edge of the subPPS square waveform (Fig. 4), it is possible to freeze the UTC time stamp of the first sample of $s(t)$ and calculate the time delay between the rising edge of the subPPS waveform and the first sample of the window. Based on these consideration, the final phase estimation may include this compensation as follows:

$$\varphi_c = \varphi_1 + \Delta\varphi = \varphi_1 + 2\pi f_1 (t_0 - t_{\text{subPPS}}) \tag{19}$$

where φ_1 has been defined in (8), t_0 and t_{subPPS} are the absolute time of the first sample of the window and of the rising edge of the subPPS square wave, respectively.

2) Sampling Clock Drift Compensation: Another problem refers to the fact that any free running sampling clock (usually implemented with a quartz crystal oscillator) does not run at the exact frequency specified by its data sheet. On the contrary, it is affected by a small but continuous drift that, if accumulated, may bring to considerable errors in the waveform parameters estimation. In general, the sampling clock drift—usually expressed in units of part per million (ppm)—depends on its quality, the exact power it gets from a DC source, the surrounding temperature and other environmental variables, but also depends on the specific fabrication procedure of the quartz oscillator. Thus, even though the data sheets of quartz oscillator declare a maximum clock drift in the order of ± 100 ppm, typical values observed during tests run at environment temperature on several devices were equally distributed in the range between ± 10 ppm. These specific values correspond to a misestimation of a single period of a 50-kHz

sampling clock in the order of ±0.2 ns, that, accumulated over a window of, for instance, $N = 3000$ samples, may result into a misestimation of the window length in the order of ±0.6 μs. Basically, as we are acquiring portions of waveform that are stretched in one way or another, the computed DFT may be consecutively misinterpreted resulting in non-negligible misestimation of the waveform parameters. In particular, the previously reported maximum error of ±0.6 μs will directly bias the DFT frequency resolution Δf and, consequently affect the estimated frequency f_1 with a maximum error in the order of 5 mHz for a signal at a rated frequency of 50 Hz.

Since, PMUs are inherently equipped with accurate time reference units like GPS, the FPGA clock error η can be measured in real-time over sufficiently long observation windows (1–10 s) as

$$\eta(m) = \frac{t_m - t_{m-M}}{M \cdot t_s} - 1 \tag{20}$$

where t_m and t_{m-M} represent the absolute times of the samples at the end and the beginning of the observation window, respectively, M is the window length expressed in equivalent number of samples and t_s is the nominal sampling time. To be noticed that, based on (20), the FPGA clock error ε is assumed to be negative when $f_s > f_{s,\text{nom}}$, positive when $f_s < f_{s,\text{nom}}$, where $f_{s,\text{nom}}$ is the nominal sampling frequency (i.e., 50 kHz in our case).

Every time the FPGA clock error is updated, the DFT frequency resolution can be adequately compensated as

$$\delta_f(m) = \delta_{f,\text{nom}} \cdot (1 - \eta(m)) \tag{21}$$

and the frequency estimation improved.

As previously mentioned, the sampling clock drift is mainly affected by temperature. In the specific case of PMU applications, the environmental temperature of an electrical substation is not usually controlled and may largely bias the PMUs performances. In this respect, a dedicated test was designed to prove the proposed approach when the temperature changes according to a typical temperature profile of an electrical substation (i.e., in the range between 5 °C and 40 °C). Two different PMU prototypes, both based on the proposed e-IpDFT approach, were installed into a temperature-controlled chamber simulating the above mentioned profile, and the performances with and without the clock error compensation were compared. Fig. 5, showing the results collected during a test run over 24 h, demonstrates that, despite the clock error variations along the day, the proposed approach is capable of compensating for the temperature effects and improving the frequency estimation up to one order of magnitude.

C. Synchrophasor and Frequency Estimation

The deployment of a SE algorithm into an FPGA-based PMU prototype must respect not only the available hardware resources, but also the PMU reporting rates and latency limits defined in [2]. To satisfy both constraints, the proposed e-IpDFT algorithm's data flow was separated in three parts: 1) the DFT analysis of the windowed input signal as explained by (3); 2) the classical IpDFT scheme defined by the set equations (4)–(8); and 3) the proposed e-IpDFT extension for

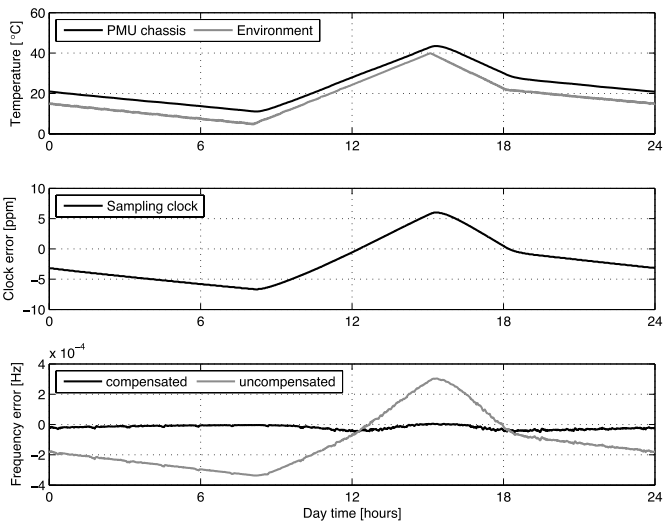

Fig. 5. 24-h test showing the effects of the compensation of the sampling clock drift.

the compensation of the spectral interference produced by the negative image of the main spectrum tone, as formulated in (9)–(16).

Regarding task 1) the typical implementation of the DFT usually involves a FFT algorithm that, despite being very efficient when the knowledge of the full spectrum is needed, it turns out to be really ineffective when only a subset of the N-point DFT must be computed. Actually, since both the classical IpDFT and the proposed e-IpDFT algorithms only assume the knowledge of the highest and second highest bins of the spectrum, $S(k_1)$ and $S(k_1 + \varepsilon)$, respectively, the computational burden needed by the DFT analysis can be considerably reduced. Indeed, based on the inherent nature of the problem, the second highest bin of the spectrum can only be located beside the spectrum maximum k_1. In particular, it will be on its left if $f_1 < k_1\delta_f$, on its or right if $f_1 > k_1\delta_f$. Therefore, as its position cannot be *a priori* determined, only three bins of the entire discrete spectrum must be computed, namely, those associated to DFT indices $\{k_1 - 1, k_1, k_1 + 1\}$. Index k_1 can be fixed *a priori* once the nominal frequency of the power system is known and once the sampling frequency f_s and the window length N are chosen (i.e., the DFT discretization step Δf is fixed)

$$k_1 = \lceil f_0/\delta_f \rfloor = \lceil f_0 N/f_s \rfloor \tag{22}$$

where $\lceil \rfloor$ represents the nearest integer function.

In addition, the Hann windowing can be directly incorporated into the DFT computation by multiplying the DFT weights of the three bins with the Hann window profile

$$\mathbb{R}\text{e}\{S(k)\} = \frac{1}{B}\sum_{n=0}^{N-1} s(n) \cdot [w(n) \cdot \cos(2\pi kn/N)] \tag{23}$$

$$\mathbb{I}\text{m}\{S(k)\} = -\frac{1}{B}\sum_{n=0}^{N-1} s(n) \cdot [w(n) \cdot \sin(2\pi kn/N)] \tag{24}$$

where the expression between square brackets can be easily precomputed and stored in six memories (three for the $\mathbb{R}$e part

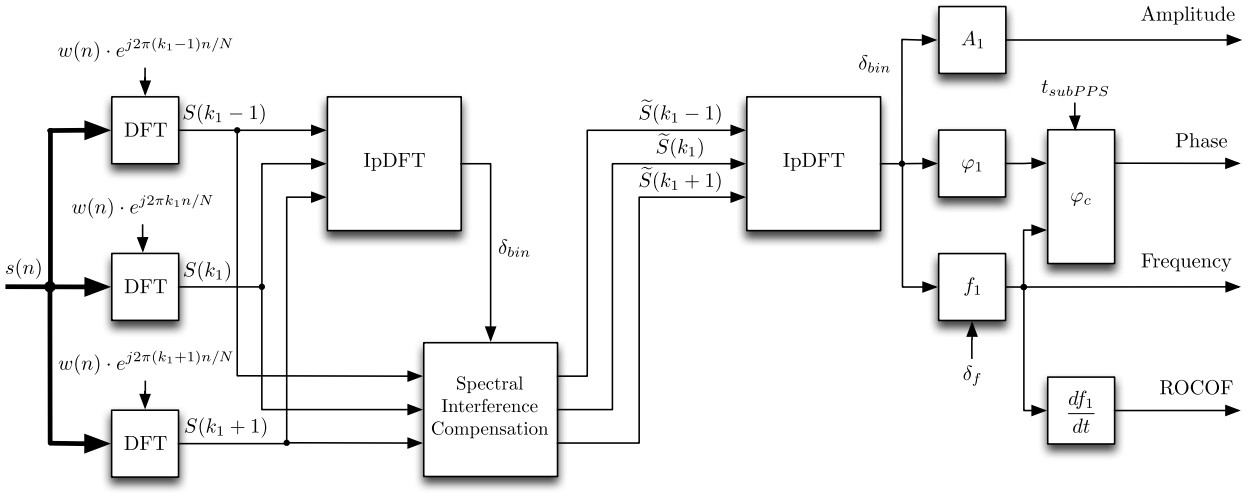

Fig. 6. Block scheme describing the proposed e-IpDFT SE algorithm.

and three for the $\mathbb{I}$m part) inside the FPGA. Based on these assumptions the DFT computation of the three bins results into six parallel N consecutive multiply-and-accumulate operations, which are really fast and optimized in any FPGA target (Fig. 6).

After the DFT bins are computed, tasks 1) and 2), namely, the IpDFT classical approach and the proposed e-IpDFT enhancement can be sequentially applied. Finally, the phase compensation and the ROCOF estimation as described in Sections II-D and IV-B, respectively, can be performed. The resulting block scheme describing the global structure of the implemented PMU algorithm is shown in Fig. 6.

D. FPGA Utilization

Based on the above-listed considerations, the algorithm described in Section II has been fully deployed into a National Instruments Compact-Rio embedded control and acquisition system characterized by a reconfigurable Virtex-5 LX110 FPGA. The FPGA is characterized by a clock frequency of 200 MHz, 17 280 slices (each one of them containing four LUTs and four flip-flops), 128 blocks of RAM (each one can store up to 32 kbits of data) and 64 DSP48E slices (each one characterized by a 25 $\times$ 18 multiplier, an adder and an accumulator). The sampling of the voltage and current waveforms is realized by means of two parallel 24-bits delta–sigma converters, characterized by a sampling rate up to 50 kS/s and an input signal dynamic of 300 V_{RMS} for the voltage and 5 A_{RMS} for the current. These input modules are directly controlled by the FPGA chassis that is synchronized to the UTC–GPS signal by means of a stationary GPS unit with a time uncertainty of $\pm$100 ns.

The compilation results are shown in Table II. They make reference to a PMU characterized by 3 voltage and 3 current inputs and are obtained using a standard Xilinx compiler. To be noticed that, as the overall FPGA occupation reached only the 55% of this platform, this algorithm may be deployed in less performing FPGAs.

TABLE II
FPGA COMPILATION RESULTS

Total Slices	Slice Registers	Slice LUTs	DSP48	Block RAMs
54.5%	29.6%	38.6%	62.5%	29.7%

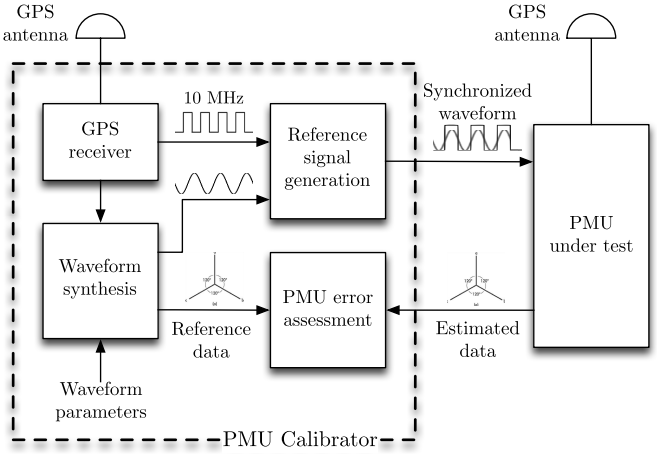

Fig. 7. Block diagram of the developed system for the PMU metrological characterization.

V. PMU METROLOGICAL CHARACTERIZATION

The PMU metrological characterization can be performed by means of a PMU calibrator that implements the following generic steps (Fig. 7): 1) presynthesis of a user-selectable waveform; 2) synchronization of the generation clock with an UTC-time source; 3) generation of the presynthesized waveform which, based on the accuracy level of the proposed hardware, can be regarded as reference; and 4) PMU error assessment.

Based on these observations, it is clear how the key aspect of any system for testing and accurately characterizing a PMU is related to the possibility of generating reference signals characterized by extreme time and amplitude accuracies.

In this respect, the experimental validation of the developed PMU has been carried out using reference waveforms generated by means of a GPS-synchronized function generator based on the PCI extensions for instrumentation (PXI) architecture. The system is composed by a National Instruments PXI 1042Q chassis on which the following devices are connected: 1) a NI PXI-6682 GPS IRIG-B timing and synchronization module and 2) a NI PXI-6281 high-accuracy low-voltage (± 10 V) generation board and NI PXI-8110 high-performance Intel Core 2 Quad Q9100-based embedded controller. With respect to the above mentioned considerations, this system can be regarded as a reference for two main reasons: 1) the synchronization of the generation clock with the GPS–PPS signal is achieved with an accuracy of less than 25 ppm and a skew less than 1 ns and 2) the generation of the signal is performed using an high-performances generation board characterized by an output accuracy of 1540 μV over a signal range of ± 10 V.

Based on this architecture, most of the tests described in [2] for both static and dynamic conditions were implemented but, for the sake of brevity, only results making reference to nominal frequency $f_0 = 50$ Hz and reporting rate $f_{RR} = 50$ fps are shown. In addition, it should be noticed that the PMU metrological characterization has been carried out using reference voltage signals characterized by an amplitude equal to the 3% of the PMU A/D input range. As a consequence, larger signals would only reduce the quantization error at the A/D converters output resulting into better performances of the proposed PMU.

The accuracy assessment presented in this section compares the performances of the proposed e-IpDFT algorithm (continuous lines) with those of the classical IpDFT approach (dashed lines) and with the IEEE Std. [2] accuracy limits. The errors are expressed in terms of the standard quantities defined in [2], i.e., the total vector error (TVE), the frequency error (FE), the rate of frequency error (RFE) and, for step tests only, the PMU response time (RT). In every figure the TVE, FE, and RFE, together with the related class P and M accuracy limits, are shown using a logarithmic scale and are computed over a 20-s window of SEs at the maximum reporting rate. Their behavior is described in terms of their maximum, average, and standard deviation values apart from step and frequency ramp tests, where the errors are instantaneous.

Finally, this Section illustrates and comments the PMU performances with respect to: 1) the presence of a decaying DC offset superposed to a single tone signal and 2) the proposed ROCOF estimator.

A. IEEE Std. C37.118-2011 Static Compliance Verification

With reference to steady state conditions, two cases have been analyzed as requested by [2]: 1) single-tone signals characterized by a constant frequency in the range $f_0 \pm 5$ Hz (Fig. 8) and 2) distorted signals characterized by a 10% single harmonic superposed to the nominal frequency tone (Fig. 9) in the frequency range between 100 and 2500 Hz. The errors are reported as a function of the nominal frequency and the harmonic component frequency for single tone and distorted signals, respectively.

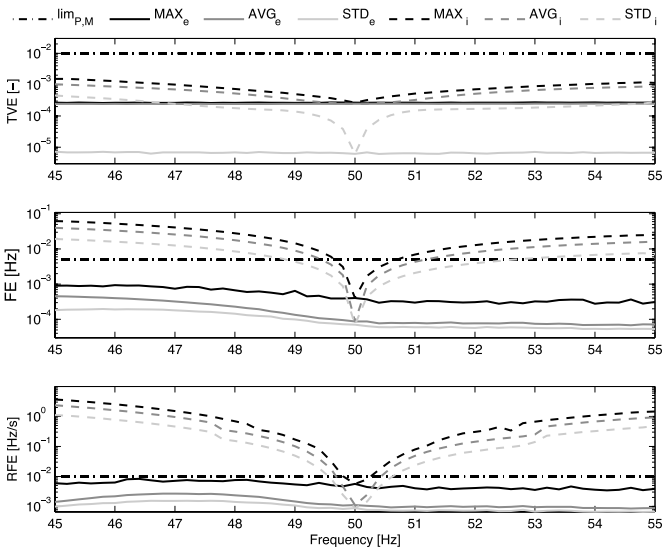

Fig. 8. Static tests with single-tone signals. Subscripts *e* and *i* identify the errors of the e-IpDFT and the classical IpDFT algorithms, respectively.

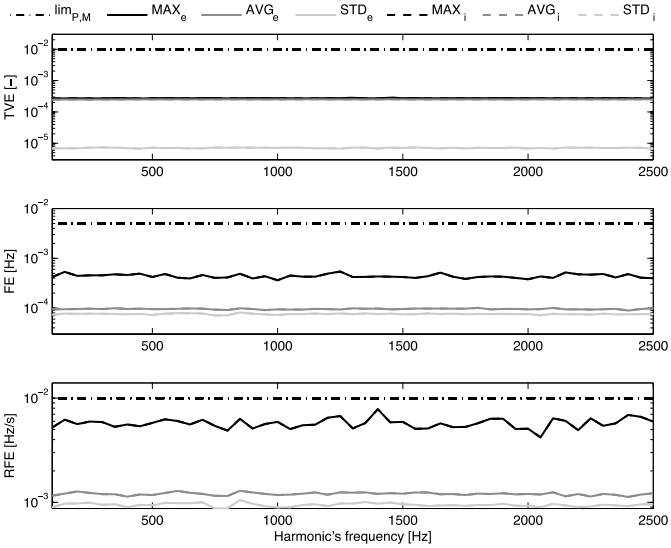

Fig. 9. Static tests with multitone signals. Subscripts *e* and *i* identify the errors of the e-IpDFT and the classical IpDFT algorithms, respectively.

As it can be observed, in the case of the proposed e-IpDFT approach, the TVE, FE, and RFE are extremely flat and almost two orders of magnitude below the required limits. They are not affected neither by the nominal frequency of the signal (Fig. 8), nor by the presence or by the order of the superposed harmonic component (Fig. 9).

On the other hand, with the classical IpDFT approach, the performances of the PMU are largely biased by the nominal frequency of the signal. In particular, the effects of the spectral interference are visible when the nominal frequency of the signal deviates from 50 Hz and, therefore, the effects of spectral leakage are more significant (particularly FE and RFE plots of Fig. 8). Concerning the case of distorted signals, the performance of the classical IpDFT algorithm are instead comparable with the proposed e-IpDFT approach as the effects of leakage are practically negligible.

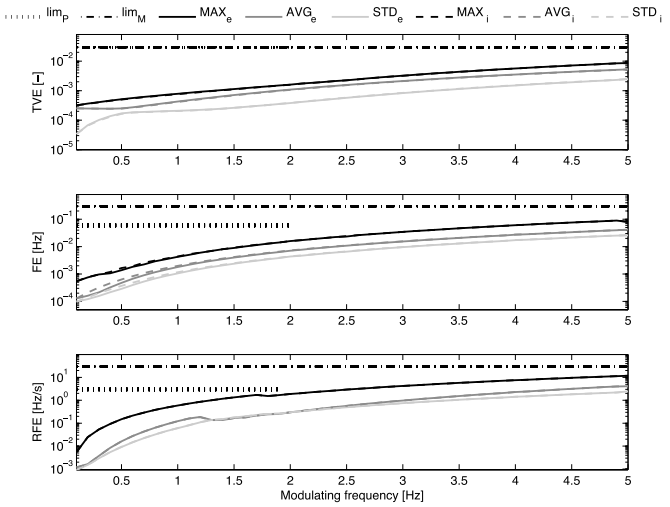

Fig. 10. Dynamic tests with combined amplitude and phase modulation. Subscripts *e* and *i* identify the errors of the e-IpDFT and the classical IpDFT algorithms, respectively. The modulating frequency needs to cover the ranges [0.1, 2] and [0.1, 5] Hz for class P and M, respectively.

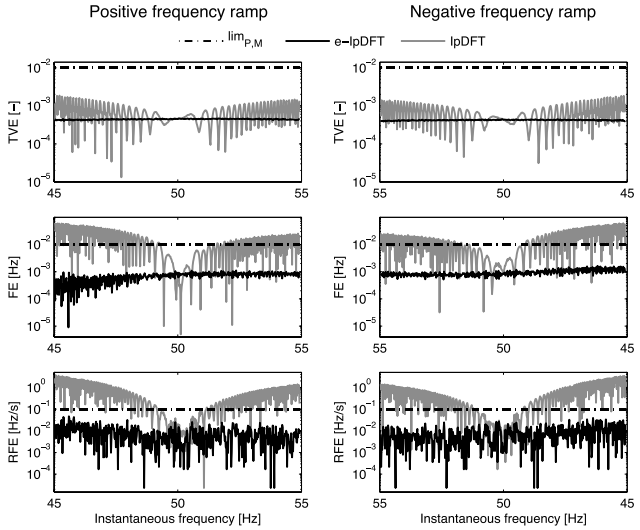

Fig. 11. Dynamic tests with (a) positive and (b) negative frequency ramp.

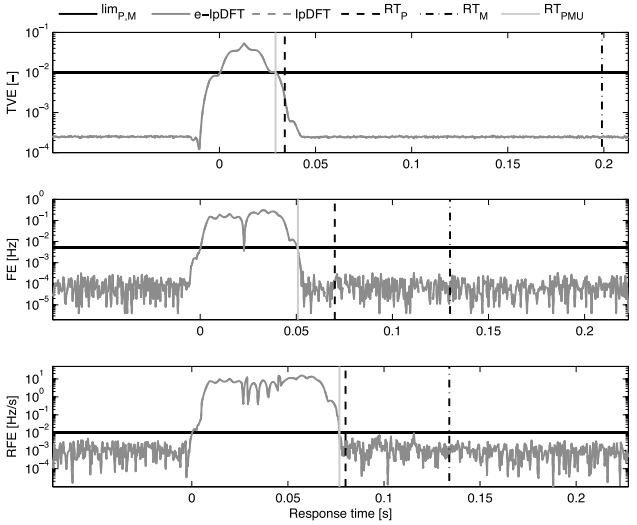

Fig. 12. Dynamic tests with positive amplitude step. Time $t = 0$ corresponds to the moment when the estimated quantity exceeds the IEEE Std. limits.

As known, the latest version of the IEEE Std. C37.118.1-2011 [2] has introduced, for M-class PMUs only, a challenging out of band interference test, aimed at verifying the PMU capability to reject interharmonics signals. This specific test introduces an additional spectrum tone that, due to spectral leakage, interferes with the main spectrum tone and corrupts considerably the estimations provided by the e-IpDFT algorithm. As a consequence, the proposed e-IpDFT algorithm cannot be compliant to the IEEE Std. limits for this test, as it has been conceived to compensate for the spectral leakage produced by the negative spectrum image of the main spectrum tone only. In this respect, the performances of the e-IpDFT approach in the case of out-of band interfering signals, are similar to those of a classical IpDFT algorithm as the ones illustrated in [18].

B. IEEE Std. C37.118-2011 Dynamic Compliance Verification

Concerning dynamic conditions, the reference signal generator has been programmed, according to the tests defined in [2], to generate single-tone signals characterized by: 1) combined phase and amplitude modulations; 2) frequency-sweep; and 3) amplitude and phase steps.

As for 1), a set of reference signals characterized by modulating frequencies in the range between 0.1 and 5 Hz, with frequency steps of 0.1 Hz, were synthesized and applied at the PMU inputs. Fig. 10 shows the corresponding estimation errors and highlights the different limits and modulating frequency ranges for classes P and M, respectively. In this case, the errors of the classical IpDFT and the proposed e-IpDFT are comparable and, despite a worsening of the performances with higher modulating frequencies, the PMU demonstrates to perform well within the IEEE Std. requirements.

Concerning 2), the frequency has been linearly varied in the range between 45 and 55 Hz [positive ramp, Fig. 11(A)] and 55 and 45 Hz [negative ramp, Fig. 11(B)] at a rate of ± 1 Hz/s. It can be observed that the performances of the proposed e-IpDFT algorithm, here reported as a function of the instantaneous frequency, are well within the limits and characterized by the expected flatness. In the case of the IpDFT algorithm instead, the same behavior observed in Fig. 8 is visible; when the instantaneous frequency deviates from the rated one, the PMU errors increase exceeding eventually the IEEE Std. limits.

Finally, regarding 3), reference signals characterized by positive steps applied to amplitude (10% of the nominal voltage, Fig. 12) and phase (10°, Fig. 13) were generated. For a more accurate assessment of the PMU response time, the equivalent oversampling approach proposed in [2] using 50 subtests was adopted. Figs. 12 and 13 show the TVE, FE, and RFE profiles during the step change as a function of measured response time. As expected, the performances of the classical IpDFT and the proposed e-IpDFT approach are the same, as the proposed spectral interference compensation scheme does

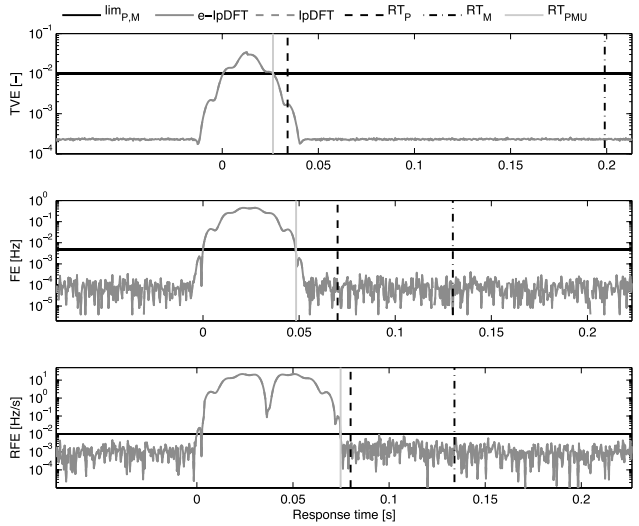

Fig. 13. Dynamic tests with positive phase step. Time $t = 0$ corresponds to the moment when the estimated quantity exceeds the IEEE Std. limits.

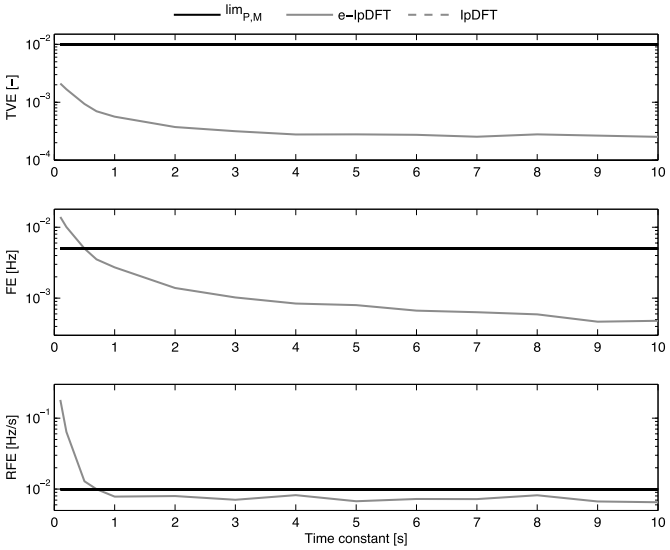

Fig. 14. Test with a decaying DC offset characterized by a time constant in the range between 0.1 and 10 s and an initial value equal to 70% of the nominal magnitude of the single-tone signal.

not affect the response time performances of the e-IpDFT algorithm. Both figures show that, after an unavoidable initial synchrophasor misestimation, the PMU errors always return below the required accuracy limits within the allowed response time [2] for both classes P and M.

C. PMU Accuracy Assessment With Decaying DC Offset

In addition to the set of test defined in [2], a further one has been implemented to evaluate the PMU performances when a decaying DC offset is superposed to a single-tone signal at the rated frequency of the system f_0

$$s(t) = A\cos(2\pi f_0 t) + A_{\mathrm{DC}} \cdot e^{-t/\tau} \tag{25}$$

where the decaying DC offset is modeled in terms of its time constant τ and its initial value A_{DC}.

The values of these parameters have been selected to represent typical waveforms of short-circuit currents taking place in a power grid. In particular, Fig. 14 shows the maximum TVE, FE, and RFE when applying a decaying DC offset characterized by an initial value A_{DC} equal to 70% of the nominal magnitude of the single-tone signal and a time constant τ in the range between 0.1 and 10 s.

As it can be noticed, the PMU performances deteriorate as the value of time constant τ becomes smaller (i.e., the dynamic becomes faster). This is expected, since in such a condition the signal cannot be anymore considered stationary within the time window T. In general, by comparing the PMU errors with the IEEE Std. limits for single-tone signals (Fig. 14), it can be noticed that for $\tau > 0.7$ s, the PMU performances are within the IEEE Std. limits and can be compared with those characterizing single-tone signal test.

D. Effectiveness Evaluation of ROCOF Estimator

To prove the effectiveness of the ROCOF estimator proposed in Section II-D, Fig. 15 shows the comparison between the RFE of the above-mentioned estimator and an

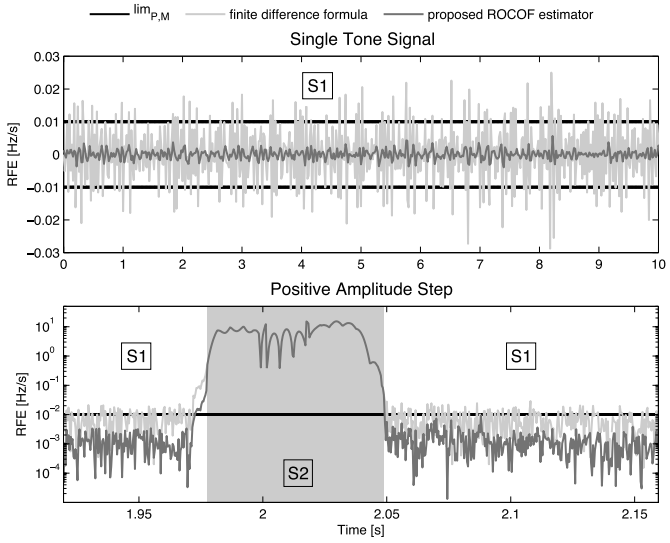

Fig. 15. Comparison between the proposed ROCOF estimator and a classical finite difference formula for the approximation of the first-order derivative of frequency.

estimator based on the finite difference formula expressed by (17) only. To demonstrate its efficiency during both static and dynamic conditions, the comparison is performed using different input signals: 1) single-tone and 2) amplitude step tests.

In particular, the upper graph compares the two estimators when the PMU inputs are fed with a single-tone signal characterized by a nominal frequency of 50 Hz. During this test it is evident that the proposed ROCOF estimator never leaves its state S1 (static conditions) and that the low-pas filter, when activated, improves significantly the ROCOF accuracy in static conditions. On the other hand, the estimator based on (17) is not compliant with the IEEE Std. limits.

The lower graph compares the two estimator during a step change in the synchrophasor amplitude. As it can be noticed,

before and after the step the proposed estimator outperforms the simple one described by (17) as it detects static conditions (state S1) and activates the low-pass filter. On the other hand, during the step change, the estimator identifies a sudden change in the estimated synchrophasor, changes its state in S2 (dynamic conditions) and deactivates the low-pass filter. As it can be noticed during this period (the gray area in the graph), the proposed ROCOF estimator is superposed to the simple one, allowing the fastest possible recovery to normal operating conditions.

VI. Conclusion

This paper has presented an enhanced IpDFT algorithm for the SE and a complete procedure for the development of a PMU prototype. The proposed e-IpDFT-based SE algorithm represents an extension of the classical IpDFT approach as it includes a scheme for the compensation of the effects of the self-interaction between the positive and the negative images of the spectrum. This modification has been conceived to improve the PMU performances during both static and dynamic conditions and, simultaneously, allow a feasible deployment of the algorithm into an FPGA-based PMU prototype.

In particular, with respect to a previously published contribution [22], this paper has illustrated and discussed the following additional items: 1) an analytical comparison between the classical IpDFT and the proposed e-IpDFT approach; 2) the analytical formulation and experimental validation of a ROCOF estimator; 3) a detailed analysis of the algorithm sensitivity to its parameters; 4) the description of the algorithm deployment into an FPGA-based PMU prototype; and 5) a complete metrological characterization of the developed PMU according to the static and dynamic tests required by the IEEE Std. C37.118.1-2011 [2].

The obtained results have demonstrated that the proposed approach effectively compensates the effects of the spectral interference produced by the negative image of the main spectrum tone and improves the SE when the instantaneous frequency of the system deviates from the rated one. In particular, with reference to the set of tests defined in [2], such a compensation has demonstrated its benefits during: 1) static tests with single tone signals and 2) dynamic tests with frequency ramps. In addition, a proper selection of the algorithm parameters, combined with the inherent nature of the proposed process, has allowed to develop a PMU capable of satisfying all the class P requirements together with the majority of them for class M with the only exception of the out-of-band interference tests.

We can conclude that the proposed algorithm and the developed PMU prototype exhibit peculiar characteristics enabling their use in several applications for both transmission and distribution networks.

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Paolo Romano (S'09) was born in Italy in 1987. He received the B.Sc. (Hons.) and M.Sc. (Hons.) degrees in electronics engineering from the University of Genova, Genova, Italy, in 2008 and 2011, respectively. He is currently pursuing the Ph.D. degree with the Distributed Electrical System Laboratory, Swiss Federal Institute of Technology, Lausanne, Switzerland.

His current research interests include the development of synchrophasor estimation algorithms and their integration into advanced phasor measurement units for the real-time monitoring of active distribution networks, and time synchronization applied to power system monitoring.

Mario Paolone (M'07–SM'10) was born in Italy in 1973. He received the M.Sc. (Hons.) degree in electrical engineering and the Ph.D. degree from the University of Bologna, Bologna, Italy, in 1998 and 2002, respectively.

He was a Researcher of Electric Power Systems at the University of Bologna in 2005, where he was with the Power Systems Laboratory until 2011. In 2010, he was an Associate Professor with Politecnico di Milano, Milano, Italy. He is currently an Associate Professor with the Swiss Federal Institute of Technology, Lausanne, Switzerland, where he was the EOS Holding Chair of the Distributed Electrical Systems Laboratory. He has authored and co-authored more than 170 scientific papers published in reviewed journals and presented at international conferences. His current research interests include power systems with particular reference to real-time monitoring and operation, power system protections, power systems dynamics, and power system transients.

Dr. Paolone is the Secretary and a member of several IEEE and Cigré Working Groups. He was the Co-Chairperson of the Technical Committee of the 9th edition of the International Conference of Power Systems Transients in 2009. He was a recipient of the IEEE EMC Society Technical Achievement Award in 2013.