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LOW POWER 3D SERIAL TSV LINK FOR HIGH BANDWIDTH CROSS-CHIP COMMUNICATION

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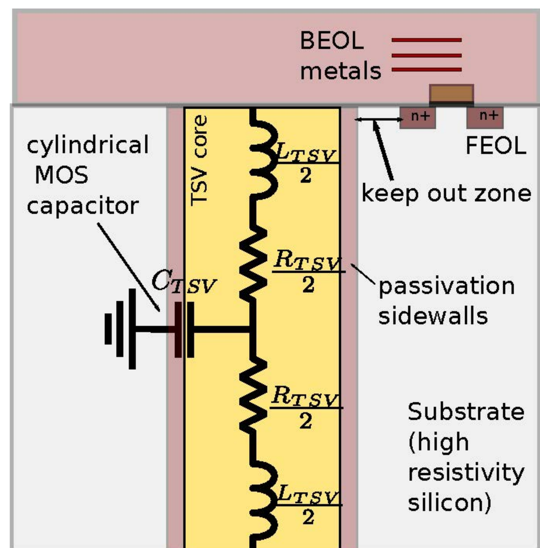
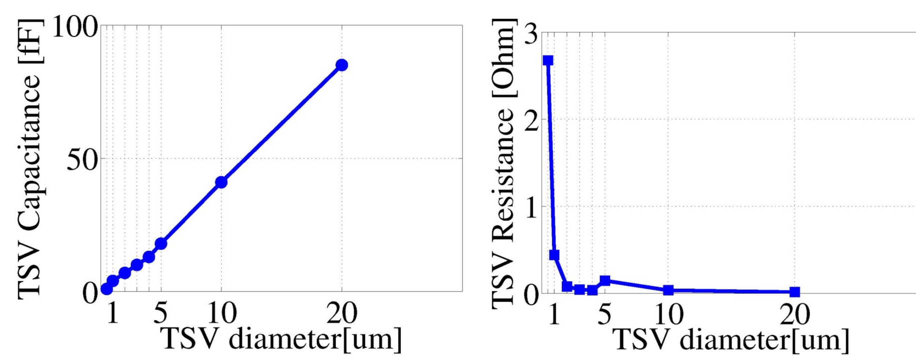
ABSTRACT

3D-ICs based on TSV technology provide high bandwidth inter-chip connections. The drawback is that most of the existing TSVs consume a large amount of silicon real estate. We present circuit-level design and analysis of area efficient, low power, high-data-rate 3D serial TSV links. A design space exploration is performed and trade-offs in terms of area, power and performance are presented. Circuit simulations of RC-extracted layouts in 40nm CMOS-technology reveals that 8:1 serialization efficiently balances area consumption and energy efficiency. Using 10µm-diameter TSV technology, an 8Gb/s serial link consumes only 84fJ/bit with 10X area reduction over 8b parallel bus.

TSV TECHNOLOGY



- TSV silicon-proven model [1][2].
- KOZ of 2.5µm around each TSV.



Diameter [µm]	Height [µm]	Resistance [mΩ]	Capacitance [fF]	Inductance [pH]
5	50	147	18	46
10	50	36	41	36
40	50	7	174	20

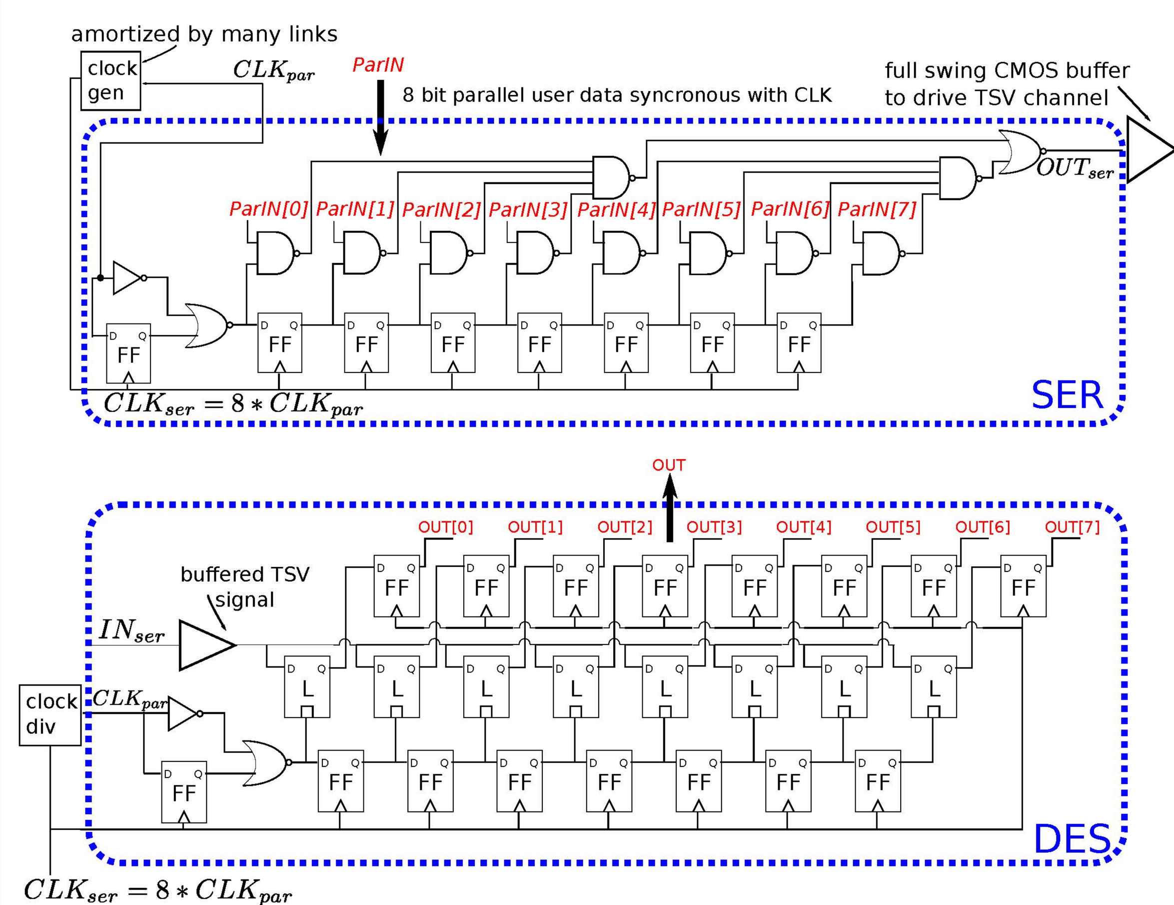
TSV characteristics:

- Excellent high frequency properties.
- Footprint is bigger compared to the BEOL vias.

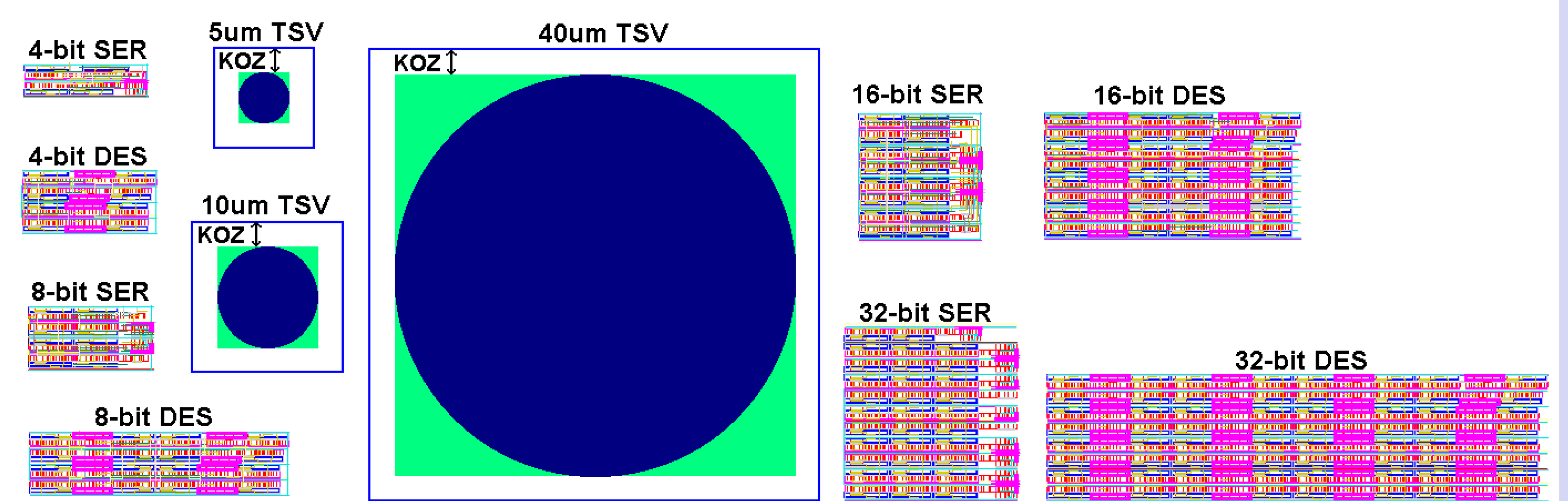
Minimize number of TSVs without sacrificing vertical data bandwidth.

SERDES CIRCUIT DESIGN

High speed 3D serial vertical link: N slow speed channels at a frequency f_{par} are serialized into a high speed data stream at $f_{ser} = N \times f_{par}$, where $N = serialization\ level$.



- Serializer architecture based on [3].
- Transmission Gate Flip-Flop (TGFF).
- Implemented in 40nm TSMC CMOS technology.

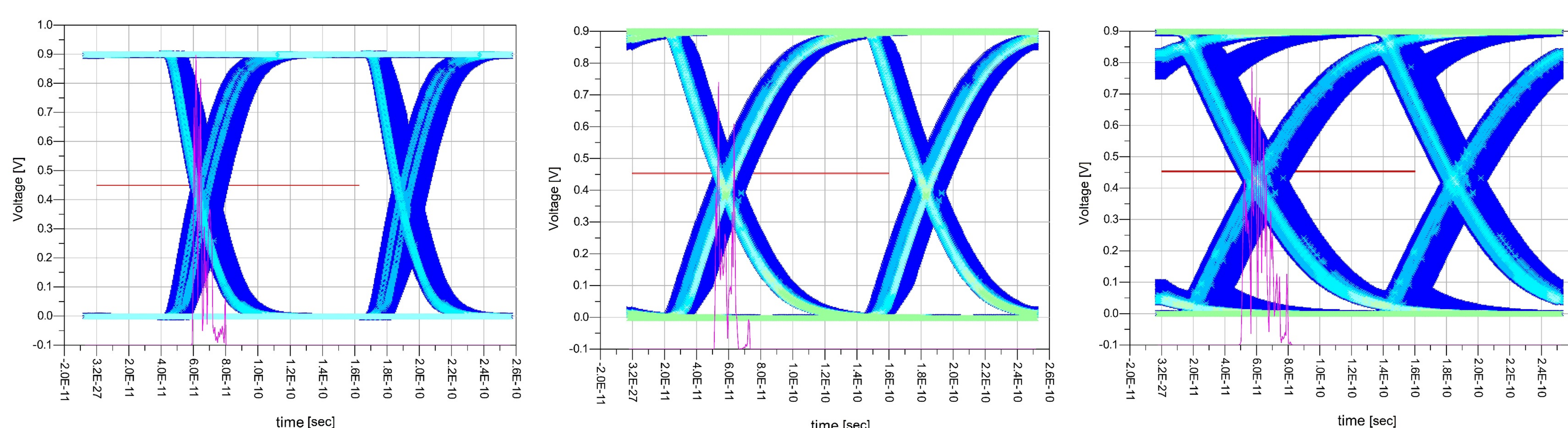


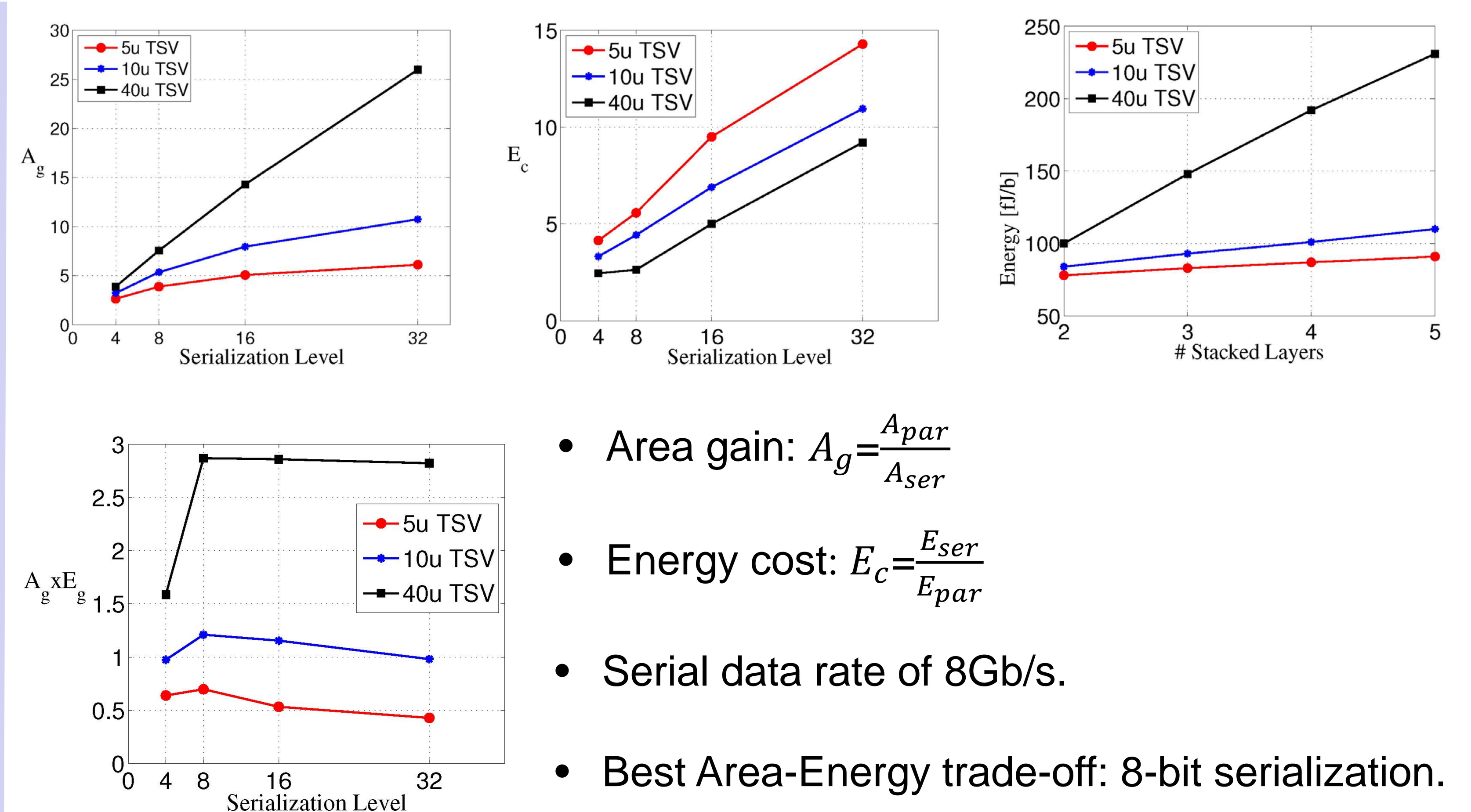
Serialization level	4	8	16	32
Area Serializer [µm²]	40.57	80.62	106.53	301.69
Area Deserializer [µm²]	86.82	165.63	260.53	637.51

EXPERIMENTAL RESULTS

A PRBS input stream is sent at a serial data rate of 8Gb/s. The energy efficiency is extracted averaging the power consumption over 80,000 received bits.

TSV diameter	5 µm	10 µm	40 µm
Paralel link energy [fJ/bit]	14	19	38
4-bit SERDES energy [fJ/bit]	58	63	93
8-bit SERDES energy [fJ/bit]	78	84	100
16-bit SERDES energy [fJ/bit]	133	131	190
32-bit SERDES energy [fJ/bit]	200	208	350





- Area gain: $A_g = \frac{A_{par}}{A_{ser}}$
- Energy cost: $E_c = \frac{E_{ser}}{E_{par}}$
- Serial data rate of 8Gb/s.
- Best Area-Energy trade-off: 8-bit serialization.

CONCLUSIONS

The potential of 3D IC stacking has a limitation caused by the large area footprint of its vertical interconnects. In this paper we propose a 3D serial link that reduces the number of TSVs in a 3D IC maintaining the performance unvaried. A serialization scheme is proposed in order to exploit the TSVs' high bandwidth. We show how the serialization level can affect both area and energy for different TSV technologies. For a mature TSV technology such as 40µm, 15X area reduction can be achieved within a low power budget for 16-bits serialization. Moreover, a serialization level of 8-bit guarantees a good balance between area consumption and energy efficiency across all the explored TSVs.

[1] M. Goldfarb et al. Modeling via hole grounds in microstrip. Microwave and Guided Wave Letters, IEEE, 1(6):135 –137, june 1991.
[2] G. Katti, et al. Electrical modeling and characterization of through silicon via for three-dimensional ics. Electron Devices, IEEE Transactions on, 57(1):256 –262, jan. 2010.
[3] M. Kurisu, et al. 2.8 gb/s 176 mw byte-interleaved and 3.0 gb/s 118 mw bit-interleaved 8:1 multiplexers. In Solid-State Circuits Conference, 1996. Digest of Technical Papers. 42nd ISSCC., 1996 IEEE International, pages 122–123, 1996.