# High Performance, Vertically Stacked SiNW/Fin Based 3D FETs for Biosensing Applications

THÈSE N$^{O}$ 6258 (2014)

PRÉSENTÉE LE 27 JUIN 2014

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DES DISPOSITIFS NANOÉLECTRONIQUES
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Suisse
2014

*The illiterate of the 21st century will not be those who cannot read and write,*
*but those who cannot learn, unlearn, and relearn.*
*Knowledge is the most democratic source of power.*

– **Alvin Toffler**

*Let no man deceive himself. If any man among you seemeth to be wise in this world, let him become a fool, that he may be wise.*

–**1 Corinthians 3:18**

*To my late mother…*

# Acknowledgements

I want to thank Prof. A.M. Ionescu for giving me the opportunity to work at the Nanolab, for his trust, for giving us so much freedom to explore, mature and become better engineers and scientists. Though sometimes hard to find, your advice is always thoughtful, insightful and it shows you care about your students. You also have a hilarious side by the way. You, Karin and Isabelle have created a lab where people are happy to be at, I will miss the Nanolab. Isabelle and Karin, thank you for all your help you are truly the best. Marie Halm, you go above and beyond to help us and are always super kind and welcoming, thank you for being so great. To my wonderful PhD jury and president: Dr. Urs Duerig, Prof. Van den Berg, Prof. Guillermo Villanueva, and Prof. Martin Gijs thank you for your fair and kind comments about my work. Thank you for your critical assessment about what was missing and for all your input. I really appreciate that you took the time and effort to review my thesis. To my fellow Nanolabers: Alejito Russu, Livio Lattanzio, Luca De Michielis, Mariazel Maqueda, Emmanuel Casu, Pankaj Sharma, Wladek Grabinski, Antonios Bazigos, Sara Rigante, Cem Alper, Sebastian Bartsch-Garcia Marquez, Wolfgang Vitale, Clara Moldovan, Matthieu Bartolome and Nilay Dagtekin and EPFL friends: Lucian Barbut, Enver Kilinc, Nasibeth Pouransi, Banafsheh Abasahl, and Hamide Jafarpoorchekab you have enriched my life in Lausanne and helped me greatly during my PhD, thank you. Especially Banita and Hamide you girls have taught me a lot, it has been a pleasure to have you as a friend. To the other two of the "trío fantástico:" Arnab Biswas (aka. Anoldo) and Hoel Güerin (Hoelino), thank you for being so funny all the time. Arnoldo I know you will miss me but you can come visit us whenever you want. Hoelino who am I gonna complain about life in general with now? A mi "office-mate" y post-doc personal, y la mejor co-supervisora, algún día, en otro lugar hablaremos en Español siempre, gracias por todo. You have been a great friend, I am really glad we got to spend all this time together, your advice and attitude in life is always positive and I will forever remember your face during my defense ☺. To my colleagues and friends from Tyndall (Giorgos Fagas, Ran Yu, Olan Lotti, Yordan Georgiev) and Imperial (Adrian Nightingale), it was a pleasure to work with

you. Yordan, thank you for all your kind advice and great sense of humor. We have to work together again. Thanks to my master students Xander Van Kooten and Natacha Berthaut for their hard work during your time at the Nanolab. To the staff of the CMi, in particular Didier Bouvet, Cyrille Hibert, Phillipe Flückiger, Claudia D'Agostino, Kevin Lister, Zdenek Benes, Joffrey Pernollet, Antony Guillet, and Laszlo Petho thank you for your support and mentoring, you make the work of many people at EPFL possible.

To my love Mat, ten years, two continents, eight cities, at least twelve moves, three degrees, four universities, three jobs and millions of yummy tortillas later, thank you for loving me, taking care of me and always pushing me forward. I love you, the PhD is for the two of us. To Ruth, Bernhard and Oma Berchtold, thank you for being my wonderful Swiss family, believing in me and caring for me. I am really grateful to have you in my life. A mi familia, especialmente a mamá Luz, papá Ramón, Karina, Gustavo, Martha, Carmen y Ramón gracias por estar siempre conmigo aunque sea de lejos. Sin ustedes nunca se hubiera podido lograr nada. Tama, Penny, Julie, my little girls always make smile, I am proud of you. To Karina and Martha especially, you have been my biggest supporters and inspiration, where would I be without you? You are my aunts, sisters, mothers, everything. I love you. A Gustavo, there are no words to describe my admiration for you, I couldn't pick a better farther, but you did pick me, thank you. A papá Ramón, gracias por siempre decirme que yo iba ser presidenta de México, todavía no, pero ahí vamos. A mamá Luz, me parezco tanto a ti que me da miedo. Ma, te admiro de muchas maneras y sin ti mi vida no seria lo mismo, pero por que no te portas bien? Los amo y les debo todo a ti y a papa Ramón. To my mother, I have never ever known somebody with so much drive to work, study and be happy no matter what, even in the worst most painful of times. I wish I had an ounce of your sarcastic sense of humor. I miss you, love you and think of you every day.

# Abstract

Nanostructured 3D materials such as vertically stacked silicon nanowires (SiNW) and Fins have long been suggested as promising candidates for a myriad of sensing applications. Such structures are of great interest for implementations that could particularly benefit from the possibility of detecting bio-important molecules at ultra-low concentrations with high selectivity. Nonetheless, their integration into bio-compatible electronic devices has proved challenging. To achieve commercial success into the highly stringent medical device market for example, their fabrication by cheap yet reliable mass production methods needs to be positively attained. Careful design of the fabrication process flow is further complicated when dealing with possibly fragile structures that need to operate reliably in a liquid (possibly corrosive) environment and perfect protection for the integrated circuit (IC) components is mandatory. In this work, 3D vertically stacked silicon nanowire and Fin field effect transistors (FETs) featuring a high density array (up to 8 × 20 SiNWs, > 4 Fins vertically stacked) of fully depleted, ultra-thin (SiNWs diameters down to $d_{NW}$ ~ 15 - 30 nm, Fin width/height $F_w$ ~ 30 nm/$F_h$ ~ 150 nm), long ($L$ < 10 μm) and suspended channels have been successfully designed and fabricated by a top-down, complementary metal oxide semiconductor (CMOS) compatible process on silicon-on-insulator (SOI) and bulk-Si substrates. Through a clever design, optimization of critical steps, and by simply leaving the stacked nanostructures within their $SiO_2$ enclosure until the end of the fabrication process (at which point they can be easily released in a buffered oxide etch) it is possible to produce robust, uniform and reliable electronic biosensor devices. Our fabrication scheme is competitive in terms of scaling and NW density (with a vertical density as high as 10 SiNWs/μm) in comparison to other bottom-up and top-down approaches with the added benefit of using a CMOS-compatible, high yield (> 90%) and reproducible process.

SiNWs and Fins (single or one level arrays) continue to draw great interest as biological sensors having the potential to provide low cost, real time, label-free, ultra-sensitive and selective (through surface modification) detection for a countless number of analytes. The nanoscale dimensions give rise to large surface to volume ratios ($S/V$) and consequently to high sensitivities due to an improved gate electrostatic control (nanoscale cross sections) and a large surface area for biomolecule attachment (sensing). The vertical stacking in our structure allows for higher utilization of the Si substrate, high output currents and high chances for biomolecule interaction as the number of conduction channels increases in two directions (Z, X). Also, as the NWs/Fins are suspended, their entire surface area is exposed to the sensing analyte for detection. The configuration of the 3D sensor additionally offers excellent electrostatic control of the channels by the possibility of applying symmetric or asymmetric gate potentials to tune the subthreshold slope (and hence the sensitivity) and optimize the power consumption. The vertically stacked liquid-gated FET structures produced here additionally show superb transistor characteristics with low drain leakage currents $I_{off} < 20 \times 10^{-6}$ mA/μm, high on-currents $I_{on} > 1$ mA/μm (normalized to nanowire diameter $d_{NW} = 30$ nm), high $I_{on}/I_{off}$ ratios > $10^6$, great maximum transconductance values $g_m > 10$ μS and subthreshold slopes $SS = d(V_{Ref})/d(log_{10}I_d)$ as low as 85 mV/dec in an electrolyte solution. An excellent $I_d - V_{SG}$ subthreshold slope of ~ 75 mV/dec was achieved (in isopropanol) with the suspended structures thanks to the high backgate coupling that controls the $SS$ as the $V_{BG}$ increases (~ 100 mV/dec when $V_{BG} = 0$ V *vs.* ~ 75 mV/dec when $V_{BG} = 1.5$ V). State-of-the-art detection of ultra-low concentrations of the protein streptavidin (~ 17 aM) with a biotinylated $SiO_2$ gate dielectric was successfully demonstrated (with large current changes ~ 500 nA). Furthermore, high, long-term and reproducible pH sensing responses with a drain current change per pH value $\Delta I_d/pH$ of up to 0.8 dec/pH were also achieved with a (3-Aminopropyl)-triethoxysilane (APTES) modified $SiO_2$ sensor gate dielectric (when operated in the subthreshold regime). Finally, a vertically stacked SiNW FET fabricated on bulk-Si was efficiently realized as a proof-of-concept device for its future implementation into low cost biosensing systems. **Keywords: SiNW, FinFET, sensor, biosensor, 3D, vertically stacked, bio-FET, ISFET, streptavidin, pH sensor.**

# Zusammenfassung

Nanostrukturierte 3D Materialien wie vertikal gestapelte Silizium-Nanodrähte (SiNW) und Fins sind seit langem als vielversprechende Kandidaten für eine Vielzahl von Sensoranwendungen vorgeschlagen worden. Solche Strukturen sind von großem Interesse für Implementierungen die besonders von der Möglichkeit profitieren könnten, bio-wichtige Moleküle bei extrem niedrigen Konzentrationen mit hoher Selektivität zu erkennen. Dennoch hat sich ihre Integration in bio-kompatible elektronische Geräte als Herausforderung erwiesen. Für einen kommerziellen Erfolg, beispielsweise im hochstringenten Markt für medizinische Geräte, ist die Herstellung mit kostengünstigen und dennoch zuverlässigen Methoden der Massenproduktion erforderlich. Die sorgfältige Gestaltung des Fabrikationsprozessablaufs wird noch komplizierter wenn es sich um Strukturen handelt die möglicherweise zerbrechlich sind, zuverlässig in einer flüssigen (möglicherweise ätzender) Umgebung arbeiten müssen und ein perfekter Schutz der Komponenten des integrierten Schaltkreis (IC) zwingend notwendig ist. In dieser Arbeit wurden 3D vertikal gestapelte Silizium-Nanodrähte und Fin-Feldeffekttransistoren (FETs) mit einem Array von hoher Dichte (bis zu 8 × 20 SiNWs, > 4 Fins vertikal gestapelt) vollständig verarmter, ultra-dünner (SiNWs Durchmesser bis hinunter zu $d_{NW}$ ~ 15 - 30 nm, Fin Breite/Höhe $F_w$ ~ 30 nm/$F_h$ ~ 150 nm), langer ($L$ < 10 μm) suspendierter Kanäle entworfen und erfolgreich mit einem Top-Down, CMOS (Complementary metal–oxide–semiconductor) kompatiblen Prozess auf SOI (Silicon on insulator) und Bulk-Siliziumsubstrat hergestellt. Durch ein geschicktes Design, durch Optimierung der kritischen Schritte und durch die Beibehaltung der gestapelten Nanostrukturen innerhalb ihres $SiO_2$-Gehäuses bis zum Ende des Herstellungsprozesses (an welcher Stelle sie leicht durch eine gepufferten Oxidätzung freigelegt werden) ist es möglich, robuste, gleichmäßige und zuverlässige elektronische Biosensoren zu produzieren. Unser Fertigungsschema ist wettbewerbsfähig im Hinblick auf Skalierung und SiNW-Dichte (mit einer vertikalen Dichte bis zu 10 SiNWs/μm) im Vergleich zu anderen Bottom-Up und Top-Down Ansätzen, jedoch mit dem zusätzlichen Vorteil dass ein CMOS-kompatibler und reproduzierbarer Prozess mit hoher Ausbeute (> 90%) verwendet werden kann.

SiNWs und Fins (Einzelne oder Arrays in einer Ebene) ziehen weiterhin großes Interesse als Biosensoren auf sich, da sie das Potential haben zu niedrigen Kosten, in Echtzeit, markierungsfrei, hochempfindlich und selektiv (durch Oberflächenmodifikation) eine unzählige Anzahl von Analyten zu erkennen. Die nanoskalige Dimensionen führen zu großen Oberflächen-Volumen-Verhältnissen ($S/V$) und damit zu hohen Empfindlichkeiten aufgrund einer verbesserten elektrostatischen Gate-Steuerung (nanoskalige Querschnitte) und einer großen Oberfläche für die Biomolekülanbindung (Erkennung). Die vertikale Stapelung in unserer Struktur ermöglicht eine höhere Ausnutzung des Siliziumsubstrats, hohe Ausgangsströme und hohe Wahrscheinlichkeiten für Biomolekül-Wechselwirkungen durch die steigende Anzahl der Leitungskanäle in zwei Richtungen (Z, X). Da die Nanodrähte/Fins aufgehängt sind, liegt ihre gesamte Oberfläche zum Nachweis der zu erkennenden Analyten frei. Die Konfiguration des 3D-Sensors bietet zusätzlich eine ausgezeichnete elektrostatische Steuerung der Kanäle durch die Möglichkeit symmetrische oder asymmetrische Gate-Potentiale zur Abstimmung der Empfindlichkeit und zur Optimierung des Stromverbrauchs zu erzeugen. Die hier produzierten vertikal gestapelten flüssigkeitsgesteuerten FET-Strukturen zeigen zusätzlich hervorragende Transistoreigenschaften wie niedrige Drain-Leckströme $I_{off} < 20 \times 10^{-6}$ mA/µm, hohe Ein-Ströme $I_{on} > 1$ mA/µm (normalisiert auf den Nanodraht-Durchmesser $d_{NW}$ = 30 nm), hohe Ein-/Aus-Stromverhältnisse $> 10^6$, große maximale Gegenwirkleitwerte $g_m > 10$ µS und unterschwellige Eigenschaften $SS$ so niedrig wie 85 mV/dec in einer Elektrolytlösung. Ausgezeichnete $I_d - V_{SG}$ unterschwellige Eigenschaften (75 mV/dec in Isopropanol) wurden mit den suspendierten Strukturen dank der hohen Back-Gate Kopplung, die die SS kontrolliert wenn $V_{BG}$ erhöht wird ($V_{BG}$ = 1.5 V), erreicht. Der Nachweis von ultra-niedrigen Konzentrationen des Proteins Streptavidin (~ 17 aM) entspricht der Stand der Technik und wurde mit einem biotinylierten $SiO_2$ Gate-Dielektrikum erfolgreich demonstriert. Außerdem wurden hohe, langfristige und reproduzierbare pH-Sensorantworten mit einer Drain-Stromänderung pro pH-Wert $\Delta I_d/pH$ von bis zu 0.8 dec/pH auch mit einem (3-Aminopropyl)-triethoxysilan (APTES) modifizierten $SiO_2$-Gate-Dielektrikum (beim Betrieb im unterschwelligen Regime) demonstriert. Schließlich wurde als Machbarkeitsnachweis ein vertikal gestapelter SiNW FET auf Bulk-Siliziumsubstrat für eine zukünftige Implementierung in kostengünstige Biosensorsysteme hergestellt. **Keywords: SiNW, FinFET, sensor, biosensor, 3D, vertikal gestapelte, bio-FET, ISFET, streptavidin, pH sensor.**

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# Technical Acronyms and Abbreviations

| Acronym/Abbreviation | Description |
|---|---|
| ADE | Analog design environment |
| AFM | Atomic force microscopy |
| ALD | Atomic layer deposition |
| APTES | (3-Aminopropyl)-triethoxysilane |
| APTMS | (3-Aminopropyl)-trimethoxysilane |
| BCA | Binary collision approximation |
| BG | Backgate |
| BOE | Buffered oxide etch |
| BOX | Bottom oxide, buried oxide |
| BSA | Bovine serum albumin |
| $c$ | Fitting parameter |
| $C_{BG}$ | Backgate capacitance |
| $C_{diff}$ | Differential capacitance |
| $C_{dl}$ | Double layer capacitance |
| $C_{dm}$ | Depletion width capacitance |
| $C_{LG}$ | Solution gate capacitance |
| CLSM | Confocal laser scanning microscopy |
| CMi | Center for micro-technology |
| CMOS | Complementary metal oxide semiconductor |
| $C_{ox}$ | Gate oxide capacitance |
| CVD | Chemical vapor deposition |
| D | Drain |
| DG | Dual-gate/double-gate |
| DIBL | Device induced barrier lowering |
| DMF | Dimethylformamide |
| DNA | Deoxyribonucleic acid |
| $d_{NW}$ | Nanowire diameter |
| EBL | Electron beam lithography |
| e-BRAINS | Best reliable intelligent ambient nano sensor system |
| EOT | Equivalent oxide thickness |
| EPFL | École Polytechnique Fédérale de Lausanne |
| FET | Field effect transistor |
| FG | Front-gate |
| $F_h$ | Fin height |
| FIB | Focused ion beam |
| $F_W$ | Fin width |

| Acronym/Abbreviation | Description |
|---|---|
| GAA | Gate all around |
| GCS | Gouy-Chapman-Stern mode |
| $g_m$ | Transconductance |
| $g_{m,max}$ | Maximum transconductance |
| $H$ | Height |
| $\hbar$ | Normalized Plank's constant |
| HEPES | (4-(2-hydroxyethyl)-1-piperazineethanesulfonic acid |
| HMDS | Hexamethyldisiloxane |
| $I$ | Ionic strength |
| IBS | Ion beam services |
| IC | Integrated circuit |
| ICP | Inductively coupled plasma |
| $I_d$ | Drain current |
| ID | Inner diameter |
| $I_{d\phi 0}$ | Baseline current |
| $I_{d\phi 1}$ | Current induced by the sensing event |
| $I_{leak1(DG)}$ | Leakage current measured from side-gate 1 |
| $I_{leak2(DG)}$ | Leakage current measured from side-gate 1 |
| $I_{off}$ | Leakage, off-current |
| $I_{on}$ | On-current |
| IPA | Isopropanol |
| ISFET | Ion sensitive field effect transistor |
| ITE | Institute of Electron Technology |
| JNT | Junctionless nanowire transistor |
| $k_{ATEC}$ | ATEC-CONT probe with Concorde-nose like tip spring constant |
| $k_B$ | Boltzmann constant |
| $k_{MPP}$ | Veeco/Bruker MPP21220 probe spring constant |
| $L$ | Length |
| LAAS | Laboratory for Analysis and Architecture of Systems |
| $L_G$ | Local-gate/liquid-gate |
| LOR | Lift-off-resist |
| LTO | Low thermal oxide |
| $m^*$ | Effective carrier mass |
| MC | Monte-Carlo |
| MEMS | Microelectromechanical systems |
| MMA | Methyl methacrylate |
| MOSFET | Metal oxide semiconductor field effect transistor |
| $n$ | Electron |
| $N_A$ | Avogadro number |
| $N_{ch}$ | Channel doping concentration |
| $N_d$ | Doping concentration |
| $n_i$ | Intrinsic doping concentration |

| Acronym/Abbreviation | Description |
|---|---|
| $N_{SD}$ | S/D doping concentration |
| NW | Nanowire |
| OD | Outer diameter |
| OTA | Operational transconductance amplifiers |
| $p$ | Proton |
| PBS | Phosphate buffered saline |
| PCB | Printed circuit board |
| PCR | Polymerase chain reaction |
| PDMS | Polydimethylsiloxane |
| PE | Polyethylene |
| $pH_{pzc}$ | pH near the point of zero charge |
| PMMA | Poly methyl methacrylate |
| PSA | Prostate specific antigen |
| PTFE | Polytetrafluoroethylene |
| $q$ | Elementary charge |
| $Q_B$ | Depletion layer charge in the silicon |
| $Q_m$ | Mobile charge density |
| $Q_{ox}$ | Oxide charge |
| $Q_{SS}$ | Interface charge |
| $R_C$ | Contact resistance |
| RE | Reference electrode |
| REFET | Reference FET |
| RIE | Reactive ion etching |
| $R_{NW}$ | SiNW resistance |
| RTA | Rapid thermal anneal |
| S | Source |
| S | Silicon spacer |
| $SR$ | Sensitivity or sensor response |
| $S_V$ | Seebeck coefficient |
| S/V | Surface to volume ratio |
| SB | Site-binding |
| SCE | Short channel effects |
| SEM | Scanning electron microscopy |
| SG | Side-gate |
| SiNAPS | Semiconducting nanowire platform for autonomous sensors |
| SiNW | Silicon nanowire |
| SOI | Silicon-on-insulator |
| SRH | Shockley-Read-Hall |
| $SS$ | Subthreshold slope |
| $T$ | Temperature |
| T | Trench opening |
| TCAD | Technology computer aided design |

| Acronym/Abbreviation | Description |
|---|---|
| $t_d$ | Dielectric thickness |
| TG | Top-gate |
| TLM | Transfer length method |
| TNI | Tyndall National Institute |
| $t_R$ | Response time |
| $T_{si}$ | Silicon thickness |
| TSV | Through silicon vias |
| $U_T$ | Thermal voltage |
| $V_{BG}$ | Backgate potential |
| $V_d$ | Drain potential |
| $V_{fb}$ | Flat-band |
| $V_{FG}$ | Front-gate voltage |
| $V_G$ | Gate voltage |
| $V_{LG}$ | Local-gate potential, liquid-gate potential |
| VLS | Vapour liquid solid |
| VOC | Volatile organic carbon |
| $V_{ov}$ | Overdrive voltage |
| $V_{Ref}$ | Reference electrode potential |
| $V_s$ | Source to drain potential |
| $V_{SG}$ | Side-gate voltage |
| $V_{th}$ | Threshold voltage |
| $W$ | Width |
| XPS | X-ray photoelectron spectroscopy |
| $ZT$ | The dimensionless figure of merit (thermoelectric devices) |
| $\alpha$ | Sensitivity parameter |
| $\alpha'$ | Coupling efficiency |
| $\beta_{int}$ | Intrinsic buffer capacitance of the dielectric |
| $\varepsilon_o$ | Vacuum dielectric constant |
| $\varepsilon_r$ | Dielectric constant of the material |
| $\varepsilon_{si}$ | Silicon permittivity |
| $\kappa$ | Thermal conductivity of the material |
| $\lambda$ | Transfer length |
| $\lambda_D$ | Debye screening length of solution |
| $\lambda_L$ | Debye screening length |
| $\mu$ | Carrier mobility |
| $\mu_e$ | Electron mobility |
| $\mu_h$ | Hole mobility |
| $\rho_c$ | Specific contact resistance |
| $\sigma$ | Electrical conductivity |
| $\phi$ | Workfunction |
| $\phi_0$ | Surface potential |
| $\phi_f$ | Fermi potential |

| Acronym/Abbreviation | Description |
|---|---|
| $\varphi_M$ | Work function of the gate electrode |
| $\varphi_{Si}$ | Work function of silicon |
| $\phi_{MS}$ | Work function difference between the gate material and silicon |
| $\chi_{sol}$ | Solution's dipole moment |

# Chapter 1 Thesis overview

Vertically stacked silicon nanowire (SiNW) or Fin field effect transistor (FET) based biosensors with the potential to be integrated into low power, 3D heterogeneous systems have been investigated, developed, fabricated and characterized for this thesis' work. SiNWs have been widely investigated over two decades for their great potential to be implemented into biosensor systems [1]. However, due to its far from straight forward execution, vertically stacked SiNWs/Fin FET based sensors had never been realized in the past. These 3-dimensional structures were chosen as the basic building blocks for sensing applications as the nanostructure stacking allows for the high utilization of the silicon substrate, high output currents and great opportunities for sensing as the number of conduction channels increases in two directions (array of channels). The latter is of particular interest and of fundamental importance for sensing applications that require ultra-low concentration analyte detection. These are just a few of the benefits of the type of structure proposed in this thesis.

The goal of this thesis' work is to produce a SiNW sensor addressing many of the elements that have been found problematic in literature independently over years of research to finally yield highly robust, reliable, and ultra-sensitive devices using top-down, complementary metal oxide semiconductor (CMOS) compatible, conventional clean room fabrication processes with the added advantage of using vertically stacked structures for sensing. Furthermore, a key consideration during the entire development stage was the compatibility of the fabrication process (and robustness of the structure) with a 3D heterogeneous integration strategy.

This work was performed within the framework of two different projects funded by the European commission (FP-7); e-BRAINS (Best Reliable Intelligent Ambient Nano Sensor System, [2]) and SINAPS (Semiconducting Nanowire Platform for Autonomous Sensors, [3]) in collaboration with several industrial partners and academic or research institutions. In particular, our partnership with Tyndall National Institute (TNI) in Cork, Ireland and Imperial College London in England

was key for their collaborative efforts with our institution (École Polytechnique Fédérale de Lausanne, EPFL, Switzerland) with respect to the functionalization of the nanostructures for sensing and the microfluidic platform development, respectively. The sensor set-up and characterization was performed as well as a cooperative effort among these two institutions and ours.

A common goal shared by SiNAPS and e-BRAINS (Figure 1-1) is for the development, fabrication and testing of devices that perform different functions (sensing, harvest energy, fluid delivery, communication, power management, *etc.)* and that can be more efficiently realized and optimized separately to be ultimately combined and integrated into a complete heterogeneous system. Both projects focus on the development of a platform that could operate either autonomously (harvest energy from the environment - SiNAPS) or operate at low powers (e-BRAINS). For that reason, the fabrication scheme should allow for the efficient heterogeneous integration of our sensor device with other components either by the use of through silicon vias (TSVs) or otherwise.

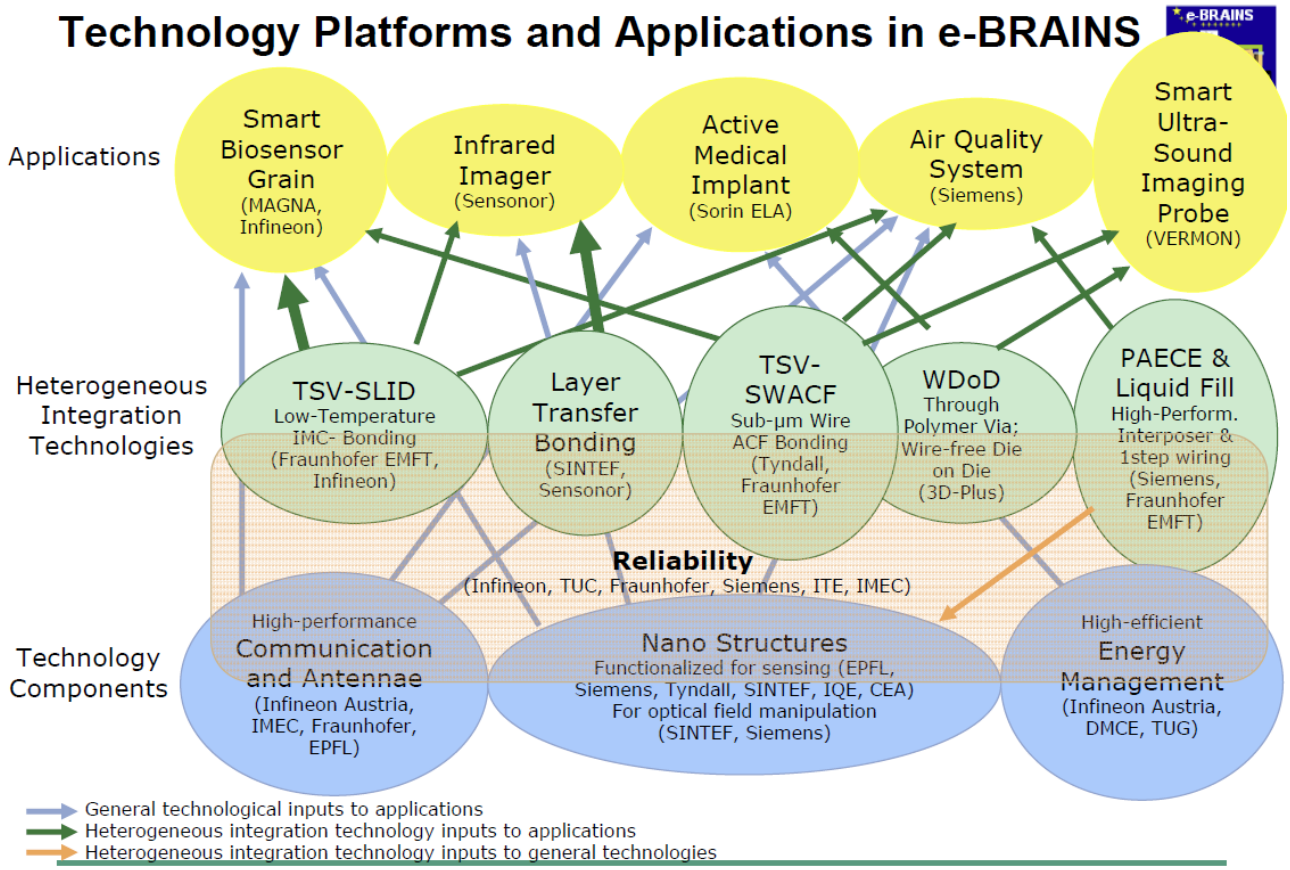
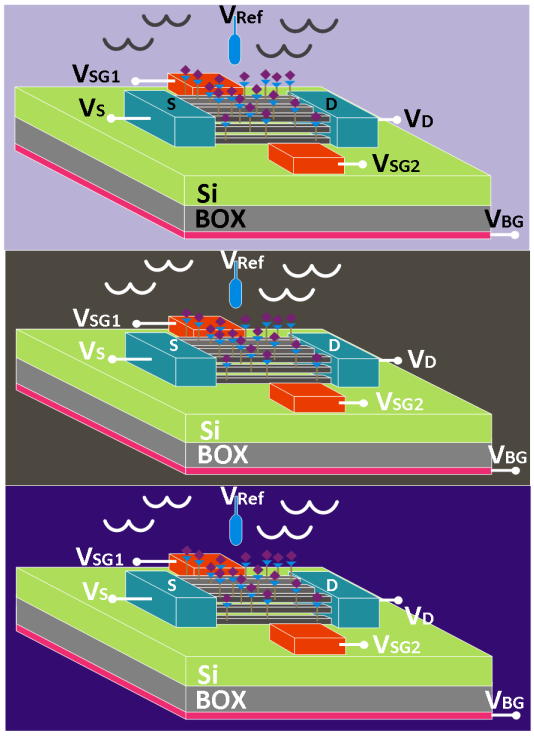



**Figure 1-1:** Technology platforms and applications in e-BRAINS, adapted from [2].

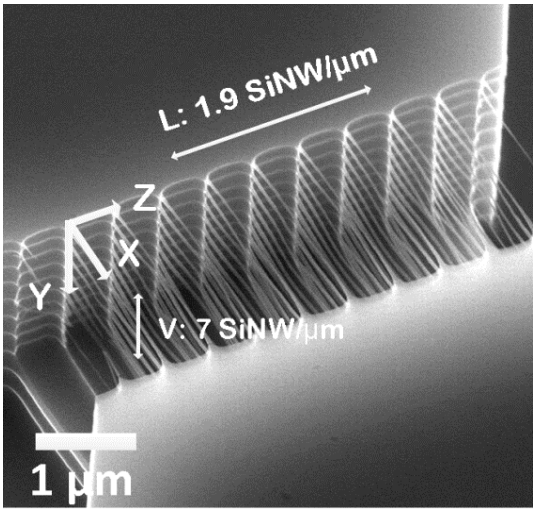
In here the reader will be walked through the development thought process, fabrication efforts, and electrical characterization in a liquid environment to elucidate the potential of such device for future biosensing commercial applications. Finally, the vertically stacked SiNW FET will be demonstrated as a highly sensitive device for the ultra-low detection of streptavidin and for the high sensor response of pH. In the outlook we present several future applications that could potentially benefit from the type of structure developed here. A brief introduction of each chapter of this thesis is written here to give an overview.

# Chapter 2: Introduction



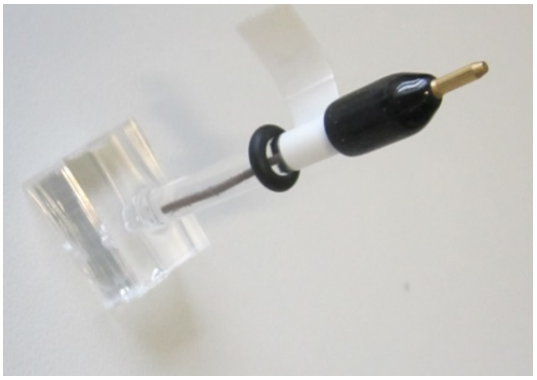

In this chapter, state-of-the-art examples that demonstrate the extraordinary potential that SiNW FETs have for current and possible future sensing applications are first presented to elucidate the motivation behind this thesis' work. The theoretical background to help the reader throughout the rest of the thesis is provided in this chapter. The planar ion sensitive field effect transistor (ISFET) by Bergveld and the general principle of operation of the ISFET is given in here as well. The benefits of using SiNW-based FET biosensors are stated and the vertically stacked SiNW/Fin FET biosensor developed in this work is introduced. The sensor applications studied in this work are shown and some device characteristics that influence the sensing performance of the structure considered during the design phase are finally presented.

## Chapter 3: Fabrication of vertically stacked nanostructures



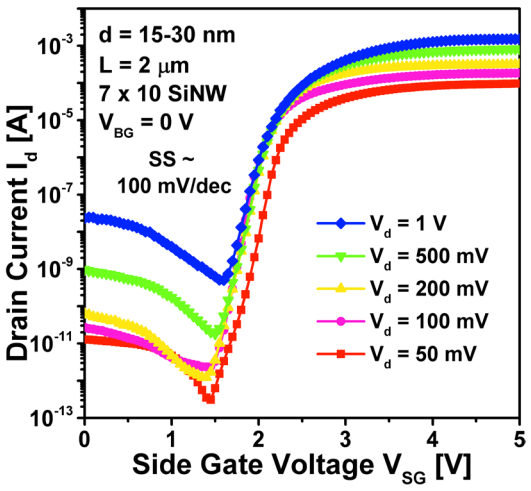

In this chapter, a fully-CMOS compatible, top-down process (based on the BOSCH process) for the successful fabrication of a high density (up to 10 SiNWs/µm in the vertical direction), vertically stacked SiNW FET, with ultra-thin ($d_{NW}$ < 35 nm), suspended and long (< 10 µm) channels, to be implemented into a biosensor is widely described. Some of the issues faced when designing, fabricating and surface functionalizing such a device for selective sensing are furthermore explored. This chapter shows that with simple and straightforward modifications of the process flow there is potential for the device to be integrated into a heterogeneous system by the possible use of through silicon vias (TSVs). Finally, it is shown that in particular, alumina covered (10 nm) SiNW arrays are remarkably strong (with channels as long as 4 µm) not breaking even when forces as large as 100 nN are applied in a racking movement of an atomic force microscopy (AFM) tip.

## Chapter 4: Methods and functionalization challenges



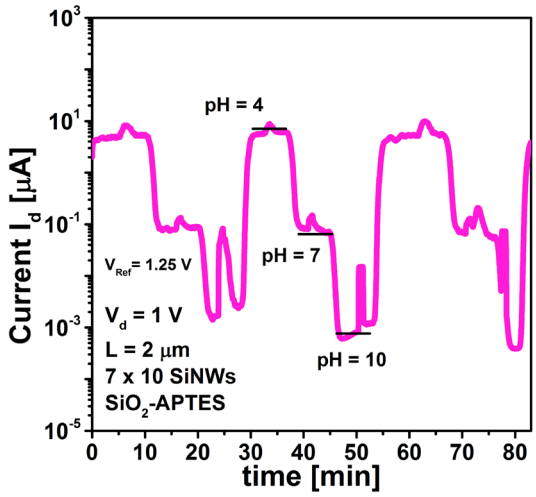
In this chapter, the methods and experimental set-up used to perform the transistor and sensing characterization of the fabricated 3D structure are described. The experimental methods used to accomplish the surface modification for pH (aminosilanization) and streptavidin (biotinylation) sensing are also discussed. Two different oligonucleotide immobilization protocols (amino or thiol-based) have been explored and some functionalization challenges and lessons learned are explained in detail here.

## Chapter 5: Transistor characterization




The transistor characteristics and performance of the FET-structure in a dry and liquid environment before and after the $SiO_2$ that surrounds the SiNWs is removed are investigated in this chapter. The configuration of the 3D FET will be shown to offer excellent electrostatic control of the SiNW channels with low drain leakage currents $I_{off} < 20 \times 10^{-6}$ mA/µm, high on-currents $I_{on} > 1$ mA/µm (normalized to nanowire diameter $d_{NW} = 30$ nm), high $I_{on}/I_{off}$ ratios $> 10^6$ and subthreshold slopes as low as 85 mV/dec in an electrolyte solution. Also by the possibility of asymmetric gate voltages an excellent $I_d - V_{SG}$ subthreshold slope of ~ 75 mV/dec is achieved in isopropanol.

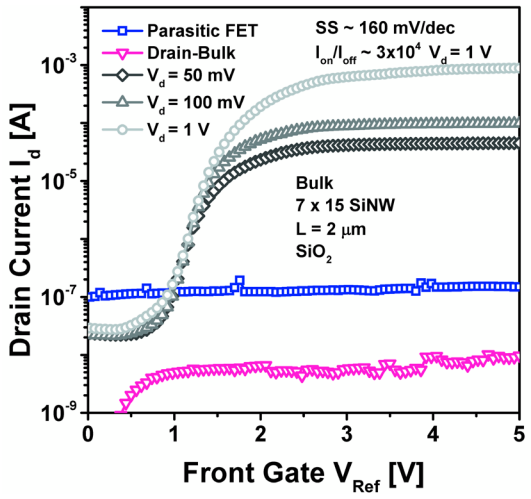
## Chapter 6: Sensor characterization




The sensing performance characterization results for pH and streptavidin sensing under transient conditions are finally given in this chapter. The 3D vertically stacked silicon nanowire field effect transistor is in here successfully demonstrated as a highly robust and sensitive pH and streptavidin sensor. The excellent FET performance characteristics, high number of NWs and efficient functionalization result in a high performing device. High (up to 0.8 dec/pH), long term and reproducible pH sensing responses will be shown with APTES modified and unmodified $SiO_2$ sensor surfaces when the device is operated in the subthreshold regime. High drain current responses > µA/pH were also measured in the strong-inversion region. The continuous operation of the device for pH sensing over extended periods of time will be demonstrated. The detection of ultra-low

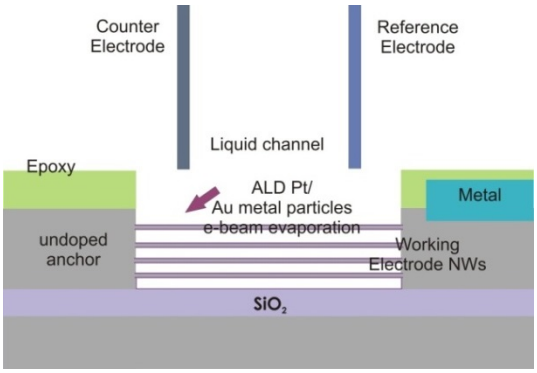
concentrations (down to ~ 17 aM) of the protein streptavidin will be finally shown with a biotinylated $SiO_2$ gate dielectric device being the main contribution of this work.

# Chapter 7: The low cost vertically stacked sensor




The most obvious future extension of the structure proposed here, the vertically stacked SiNW sensor fabricated in bulk silicon is successfully demonstrated in this chapter. The low cost to manufacture such structures could drive the successful implementation of the vertically stacked sensor into the biosensor market. The bulk-based structure will be shown to have excellent transistor characteristics as well with high $I_{on}/I_{off}$ ratios > $10^4$ and low subthreshold slopes $SS$ ~ 160 mV/dec.

# Chapter 8: Conclusion and outlook




In this chapter, the main results are summarized and some general conclusions for the work presented in this thesis are given. Then, several devices for a myriad of applications that could benefit from the type of structure developed in here are proposed. For example, the vertically stacked structure can as well be used for their application as amperometric sensors with very few modifications. Thermoelectric devices could also benefit from crystalline, uniformly dense, strong vertically stacked SiNW structures fabricated with a top-down, CMOS compatible approach.

# Chapter 2 Introduction

The general theoretical background to help the reader throughout the rest of the thesis is given in this chapter. Silicon nanowire field effect transistors provide a versatile platform for the ultra-sensitive and selective detection for a myriad of bio-important molecules as will be shown in this chapter. The vertically stacked structure is presented in here and different design considerations taken into account while developing the nanosensor are addressed.

## 2.1 Motivation

The selective detection of specific biomarkers present in several body fluids such as saliva, blood, amniotic fluid, breast milk, and sweat, to name a few, at ultra-low concentrations may allow for the early, and possibly non-invasive diagnosis of disease, monitoring of illness progression, genetic disorder screening and surveying of drug efficiency during treatment [4].

Nowadays nevertheless the invasive collection (*e.g.,* drawing of blood) of bio-fluids for external analysis by label-based detection methods most commonly occurs and dominates the medical diagnostics world. These techniques involve the use of fluorescent dyes or radioisotopes (among others) as tags [5]. Ultra-low concentrations are difficult to be measured due to the inherent low sensitivity of such methods (low signal produced at low concentrations). Also the complementary molecule has to be modified (possible interference with dye molecule) which is time consuming and requires specialized personnel to perform the procedure [5]. There is an impending need to overcome the limitations that label-based techniques impose especially when multiplex detection of several species *in-tandem* and *in-vivo* may be necessary.

Silicon nanowire field effect transistors (SiNW FETs) have been investigated for a large number of applications such as disease marker screening [6, 7], non-invasive clinical testing and early diagnostics of asymptomatic diseases such as diabetes and cancer [8, 9] and many non-clinical applications such as the monitoring of explosive materials [10], an application that can prove interesting for homeland security. They have been shown to provide a low cost, real time response, label-free,

ultra-sensitive (at extremely low concentrations ~ fM) and selective (through surface modification) platform for detecting simple molecules [1, 11-13], viruses [12], proteins [1, 14-18], deoxyribonucleic acids (DNA) [14], and pH [1, 6, 11, 19-31] among others, while not requiring large sampling quantities motivating our research efforts.

Some of the most notable application examples in literature with high potential for clinical diagnostics are the fM detection of prostate specific antigen (PSA) a protein marker for prostate cancer [6, 7], the detection of breast cancer serum biomarker protein CA15.3 down to 110 pM (limit relevant for clinical applications) [9], the specific ssDNA strand recognition for genetic disease analysis [32] and the enzyme modified (urease) SiNW FET for low detection (mM) of urea in bio-fluids [33]. Highly sensitive detection of polar ($N_2O$, NO, CO, *etc.*) and non-polar analytes (hexane, octane, *etc.*) in the gas phase through an appropriate surface functionalization protocol (*e.g.*, organic receptor attachment) has also been shown [13, 34] making SiNW FETs interesting for the non-invasive detection of volatile organic carbons (VOCs) disease biomarkers present in human breath or even for environmental monitoring. Zheng *et al*. [30] developed a SiNW-based array for the multiplexed fM detection of different cancer markers to make diagnosis of complex diseases more accurate. All these examples serve to demonstrate the potential that SiNW FETs offer in general for a broad range of sensing applications.

## 2.2 Field effect transistors as biosensors

The ion sensitive field effect transistor (ISFET) was introduced by Bergveld in the early 1970's [35]. The ISFET is analogous to a planar metal oxide semiconductor field effect transistor (MOSFET, Figure 2-1) except that the gate dielectric is exposed to a solution. In comparison to a MOSFET where the gate electrode has direct contact with the gate dielectric, a reference electrode (RE) or local-gate (LG) electrode is instead inserted into the analyte contacting the gate ($V_G$ gate voltage, $V_{LG}$ local-gate voltage, $V_s$ source voltage, $V_d$ drain voltage, $V_{BG}$ backgate voltage). Ions in solution or charged molecules can therefore influence the gate potential and exert electrostatic control on the source to drain current $I_d$, thus be sensed [20].

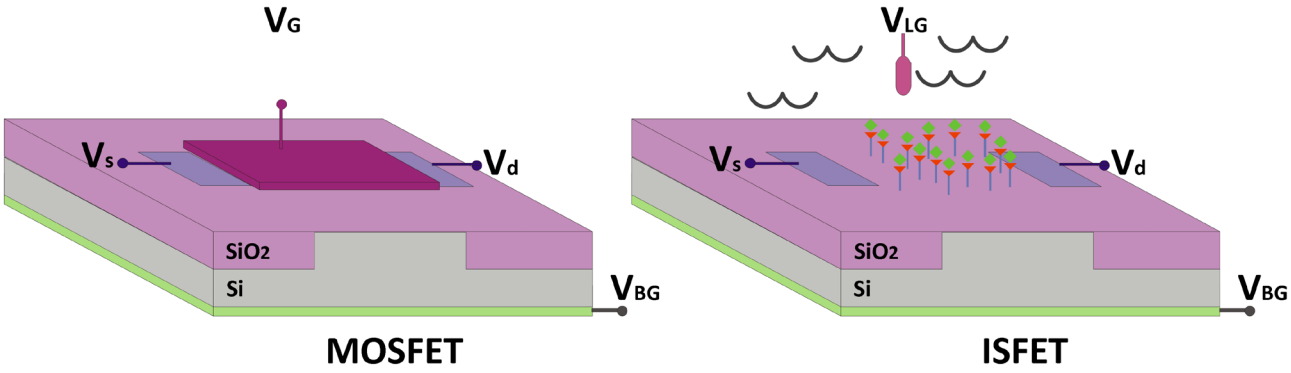



**Figure 2-1:** Schematic of planar MOSFET and ISFET.

## 2.3 Principle of operation

For a conventional MOSFET in the linear region, when the gate voltage is greater than the threshold voltage ($V_G > V_{th}$), and the drain potential is lesser than the gate overdrive voltage ($V_d < V_G - V_{th}$), the drain current relationship with respect to $V_G$ is given by Equation 2.1, [36]:

$$I_d = C_{ox}\mu_e \frac{W}{L}\left[(V_G - V_{th})V_d - \frac{1}{2}V_d^2\right]$$

**Equation 2.1**

$C_{ox}$ is gate oxide capacitance per unit area, $W$ and $L$ are the width and length of the channel and $\mu_e$ is the electron mobility. With the threshold voltage given by Equation 2.2, [36]:

$$V_{th} = \frac{\phi_M - \phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f$$

**Equation 2.2**

$\phi_M$ and $\phi_{Si}$ are the work function of the gate electrode and the silicon respectively, $q$ is the elementary charge and $Q_{ox}$, $Q_{SS}$ and $Q_B$ are the oxide charge, interface charge and depletion layer charge in the silicon accordingly. Finally, $\phi_f$ is the Fermi potential. In analogy, for an equivalent ISFET, ad-

sorbed charged molecules produce a surface potential $\phi_0$ on the gate oxide resulting in a $V_{th}$ change Equation 2.3, [36]:

$$V_{th} = V_{Ref} - \varphi_0 + \chi^{sol} - \frac{\phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f$$

**Equation 2.3**

$V_{Ref}$ is the reference electrode potential and $\chi_{sol}$ the solution's dipole moment. For a fixed $V_{Ref}$, only the surface potential changes as a function of pH. The ISFET drain current then becomes (Equation 2.4, [36]):

$$I_d = C_{ox}\frac{W}{L}\left[\left(V_G - V_{ref} + \varphi_0 - \chi^{sol} + \frac{\phi_{Si}}{q} + \frac{Q_{ox} + Q_{SS} + Q_B}{C_{ox}} - 2\phi_f\right)V_d - \frac{1}{2}V_d^2\right]$$

**Equation 2.4**

The surface potential change with pH change has been derived from the site-binding (SB) and Gouy-Chapman-Stern (GCS) model [25, 37-40], Equation 2.5:

$$\frac{d\varphi_0}{dpH} = 2.303\alpha\frac{k_B T}{q}$$

**Equation 2.5**

$k_B$ is the Boltzmann constant, $T$ the absolute temperature and $\alpha$ is the dimensionless sensitivity parameter ($\alpha$ = 0 – 1), Equation 2.6:

$$\alpha = \frac{1}{\left(2.3kTC_{diff}/q^2\beta_{int}\right) + 1}$$

**Equation 2.6**

$C_{diff}$ is the differential capacitance that depends on the sensing solution's ion concentration and the $\beta_{int}$ is the intrinsic buffer capacitance of the dielectric. The sensitivity parameter therefore reaches unity depending on the gate dielectric utilized, the ionic concentration of the solution and temperature. The resulting threshold voltage shift $\Delta V_{th}$ in the $I_d - V_{Ref}$ characteristic reaches the thermodynamic Nernst limit of 59.5 mV/pH (at room temperature $T$ = 300 K) when the sensitivity parameter $\alpha$ approaches unity.

Figure 2-2 illustrates how the inherent transistor characteristics of the FET device, namely the subthreshold slope $SS = dV_G/d(\log_{10} I_d)$ and the $\Delta V_{th}$ shift resulting from the electric field induced by a sensing event both represent an upper limit to the sensitivity of a given device when this is biased in the subthreshold region.

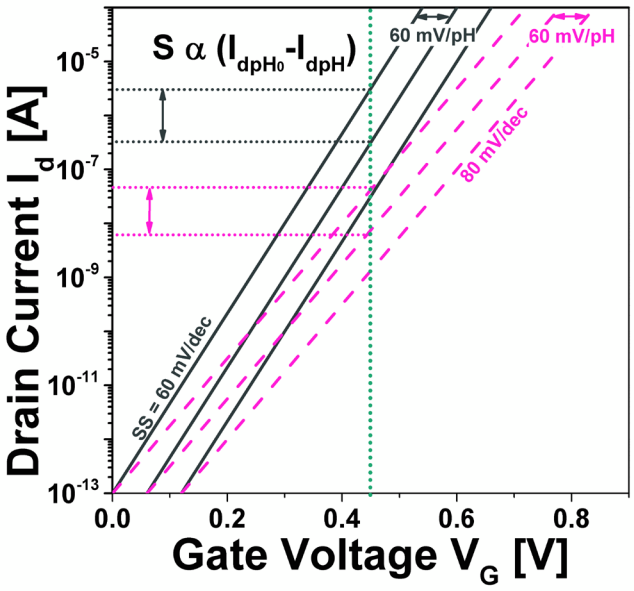



**Figure 2-2:** $I_d - V_G$ curves illustrating how the drain current and hence the sensitivity changes with a change of pH that induces a $V_{th}$ shift of 60 mV/pH, for a transistor with a $SS$ slope of 60 mV/dec (grey-solid curves) and 80 mV/dec (pink-dashed curves), in subthreshold.

Typically, the global sensitivity $SR$ or sensor response is defined as the absolute $SR = (I_{d\psi 0} - I_{d\psi 1})$ or relative variation of current $SR = (I_{d\psi 0} - I_{d\psi 1})/ I_{d\psi 0}$ due to a difference in the external potential. $I_{d\psi 0}$ is the baseline current and $I_{d\psi 1}$ is the current induced by the sensing

event. This sensor response is dependent on the operating point at which sensor measurements are carried out [6, 19]. In the subthreshold region the drain current changes exponentially as a function of source to gate potential, hence the larger sensor responses.

It is well known that for a field effect transistor the subthreshold slope is limited to ~ 60 mV/dec at room temperature for standard transistors [41]. The current change per pH ($\Delta I_d/pH$, and hence the sensitivity of the device) reaches a maximum of 1 dec/pH for a device with a $SS$ of 60 mV/dec for which a pH change induces an ideal Nerstenian $V_{th}$ shift of almost $\Delta V_{th}/pH$ = 60 mV/pH at room temperature (grey-solid curves, Figure 2-2). Even if the sensing surface can provide a Nerstenian response of 60 mV/pH ($\alpha \rightarrow 1$), when the subthreshold slope of the device increases the sensitivity suffers (pink-dashed curves, Figure 2-2).

## 2.4 SiNW FETs

Continuous feature size scaling has driven the CMOS technology roadmap for over 50 years [42]. Offering solutions to some of the major challenges for further device scaling (*e.g.*, degraded gate electrostatics, threshold voltage roll-off, large drain induced barrier lowering (DIBL), high sub-threshold slopes, large static power consumption, unbalanced voltage scaling, and other short channel effects, SCE), SiNWs and FinFETs have been widely investigated and had long been proposed as the necessary technology extension to continue with Moore's law predictions for the next several years [43]. They also have the advantage of being compatible with planar technology. For gate-all-around (GAA) SiNWs in particular, the gate influences the channel potential from more than one side and therefore the increased doping in the channel that is needed to control the gate in planar devices but leads to a degraded performance is no longer required [43, 44]. They have also been shown to have enhanced on-currents $I_{on}$ and a low leakage currents $I_{off}$ making them good candidates for high performance devices [45].

### 2.4.1 SiNW FET biosensors

Silicon nanowire FETs were first implemented for pH sensing by Cui *et al.* [1] in the early 2000's. SiNWs and Fins offer large surface to volume ($S/V$) ratios due to their nanoscale dimensions. Figure 2-3a shows an schematic of a single SiNW FET biosensor structure. The presence of a few

charged molecules on the SiNW surface can modulate the carrier distribution over their entire cross sectional conduction pathway making the devices exceptionally sensitive compared to the traditional planar (surface-only modulation) sensor that Bergveld introduced [1, 32, 46]. Hence, they continue to draw great interest for their potential integration into highly sensitive systems.

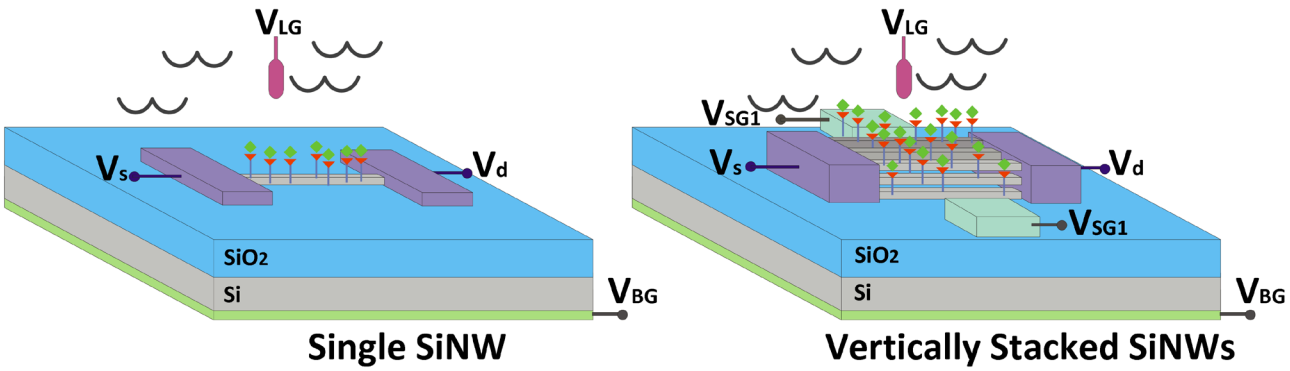



**Figure 2-3:** Schematic of single SiNW FET biosensor and vertically stacked SiNW FET biosensor (3 rows of 3 SiNWs vertically stacked).

## 2.4.2 The vertically stacked SiNW FET biosensor

The design, fabrication and characterization a SiNW or Fin based 3D FET structure for biosensing applications with many of the elements that have been found to offer high sensitivities, robustness and long term reliability after decades of research, is the goal of this work. The device proposed here is shown schematically in Figure 2-3b. It consists of source $V_s$ and drain $V_d$ contacts and one or two symmetrical Pt gates to the sides $V_{SG}$. The NWs or Fins are stacked in between the source and drain anchors and can be operated using an integrated reference electrode ($V_{LG}$, *or* $V_{Ref}$), side-gates or backgate electrode through a liquid with both front and backgates strongly coupled electrostatically in a GAA configuration.

The 3D device proposed here offers certain advantages. The 3D stacking allows for the high utilization of the silicon substrate, high output currents [43, 47] and high opportunities for sensing interactions as the number of conduction channels increases. The SiNW cavities can furthermore be used for trapping small cells, viruses, *etc.*, or be implemented as molecular sieves depending on the type fluid manipulation necessary [48]. Also, in comparison to the typical dry etch-SOI [14] or

bottom-up assembly–based FET biosensor [49] in which the NWs rest directly on top of an insulator layer, here the Fins/NWs are suspended and fully immersed in a liquid solution and consequently their entire surface area is available for biomolecule attachment and sensing. In order to have fully depleted channels, reach high mobilities [50] and high sensitivities [51] an SOI wafer with a low doped silicon device layer is used in the fabrication of ultra-thin Fin/NW arrays (Fin width, $F_w$ < 40 nm, nanowire diameter, $d_{NW}$ < 35 nm). The fabrication approach utilized here furthermore takes advantage of the natural scalloping effect created in silicon by the CMOS compatible BOSCH (reactive ion etch, RIE) dry etch process in combination with thermal oxidation to create a highly reproducible 3D SiNW structure as will be shown in Chapter 3 of this thesis.

## 2.4.3 Junctionless SiNW biosensors

Junctionless transistors (JNTs) are said to be so because the source and drain extensions have the same type and doping concentration as the conduction channel (*i.e.*, $p^+$–$p^+$–$p^+$, $n^+$–$n^+$–$n^+$) [52-55]. They typically have high doping channel concentrations and with no *p*–*n* junctions or doping gradients they are essentially resistors with a gate electrode that controls the carrier density [52, 56-59]. Figure 2-4a shows a schematic diagram of a tri-gated p-type junctionless Fin-FET sensor in a SOI substrate. Figure 2-4b shows also typical tri-gated n-channel junction-based enhancement Fin sensor for comparison.

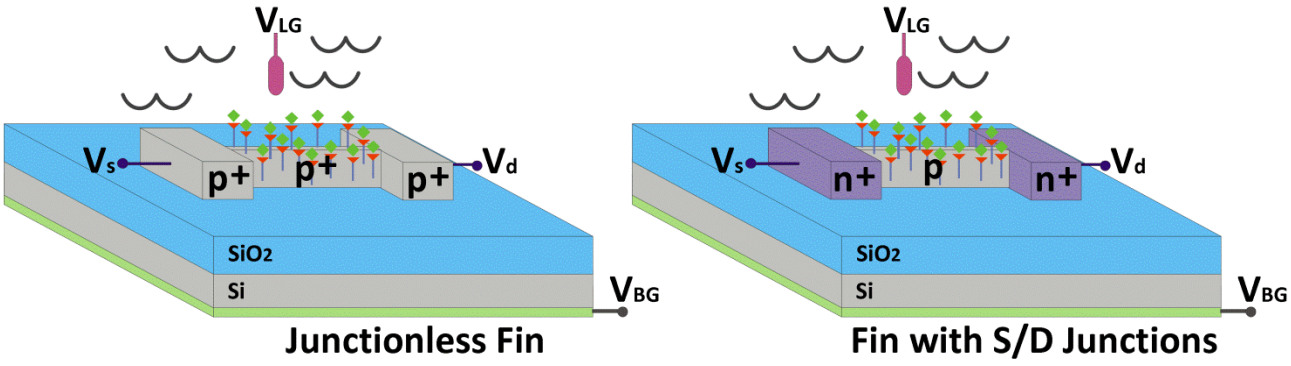



**Figure 2-4:** Schematic of JNT FinFET SOI junctionless sensor system, left. Source-channel-drain regions have same type $P^+$-$P^+$-$P^+$ and doping concentrations $N_d$, without junctions, n-channel enhancement mode FinFET SOI sensor system. *N-P S/D* junctions are clearly shown in schematic (right).

Tri-gated JNTs of the type schematically shown here (Figure 2-4b) were investigated experimentally by Tyndall National Institute (SiNAPS partners) for their implementation into a biosensor system. Technology computer aided design (TCAD) simulations were performed for the same type of structures (tri-gated enhancement mode and JNT, Appendix A. The simulations for the JNTs were performed as a function of gate dielectric constant ($\varepsilon_r$ = 1.7, 3.9), geometrical dimensions ($L$ = 0.5, 1, 2 μm, $F_h$ = 10, 20, 30, 45 nm and $F_w$ = 10, 20, 30 nm) and doping concentration (boron B, $N_d = 10^{18}$ cm$^{-3}$, $10^{19}$ cm$^{-3}$, $2 \times 10^{19}$ cm$^{-3}$) for a p-type SiNW/Fin tri-gated junctionless FET. Enhancement mode devices with $\varepsilon_r$ = 1.7 and L = 500 nm were also simulated as a function of $F_h$ = 10, 20, 30, 45 nm and width $F_w$ = 10, 20, 30 nm. In here we discuss briefly the main results and some important considerations for their integration into a 3D vertically stacked structure.

The operation of the JNT is based on the depletion or accumulation of carriers in the highly doped semiconductor channel [53, 55]. The threshold voltage can be tuned by changing different parameters such as the NW/Fin width, height, doping concentration and surface passivation/dielectric characteristics [56]. As can be seen in Appendix A and [60, 61], the geometrical characteristics of the device greatly influence the $V_{th}$ and $SS$. The $SS$ for thin Fin devices ($F_w$ = 10 nm) is almost unchanged with increasing $F_h$. Only when the doping channel concentration increases to high values ($N_d = 2 \times 19$ cm$^{-3}$) the $SS$ increases to a greater extent as a function of $F_h$. The subthreshold slope reaches the thermal limit of MOSFETs for all studied JNT structures with a Fin width $F_w$ = 10 nm ($SS$ < 67 mV/dec) but it degrades with increasing $F_h$, $F_w$, $L$ and doping concentration. The $SS$ changes most dramatically as the $F_w$ is increased from 10 ($SS$ = 60.97 mV/dec) to 30 nm (230 mV/dec) for high channel doping concentrations ($N_d = 2 \times 10^{19}$ cm$^{-3}$ and $\varepsilon_r$ = 1.7). The subthreshold slope also increases slightly with increasing channel length. In the case of the threshold voltage variation with respect to $F_h$ and $F_w$ it was found to change minimally for low doping concentrations for all $F_h$, $F_w$ and $L$. The $V_{th}$ nonetheless changes the most as well for high channel doping concentrations. In comparison to JNT neither the $SS$ nor the $V_{th}$ change significantly for enhancement mode devices with $F_w$ and $F_h$ and $N_{ch}$. Only when the channel doping concentration is very high the $V_{th}$ shifts to a greater extent but even then for $N_{ch} = 10^{19}$ cm$^{-3}$ the threshold voltage shift is only $\Delta V_{th}$ = 0.063 V with increasing $F_h$ from 10 to 45 nm with the highest change occurring when the $F_w$ increases from 10 nm to 30 nm with a $\Delta V_{th}$ = 0.331 V.

Having no doping concentration gradients, JNTs could offer a certain amount of flexibility with respect to the fabrication process. Since no *S*/*D* implantation is required, this may reduce fabrication induced variability and may relax thermal budget requirements (no impurity diffusion during thermal processing steps) [58, 62, 63]. Furthermore, the SiNW/Fin FET-type device investigated by TCAD simulations can be easily fabricated by direct patterning by electron beam lithography and dry etching with an SOI substrate [64]. The device layer thickness reproducibility is not an issue as current SOI technology allows for the manufacture of wafers with ultra-thin silicon device layers (below 50 nm) with tight uniformity specifications within a few Angstroms (6-sigma range of less than 1 nm), below 2% [65]. These are all possible advantageous qualities for the fabrication of miniaturized sensor devices and their heterogeneous integration with other components. Nonetheless, their implementation into a vertically stacked structure by BOSCH in a research cleanroom may prove more difficult since both the *SS* and $V_{th}$ can change significantly with $F_w$, $F_h$, and $N_d$ in comparison to enhancement mode devices. Though this may not be an issue in an industrial setting, as will be seen in the next chapter, a broad NW diameter range (*e.g.*, $d_{NW} = 15 - 30$ nm) is achieved for the fabricated vertically stacked SiNW devices in this work. This issue will be further discussed in Section 3.6 of this thesis.

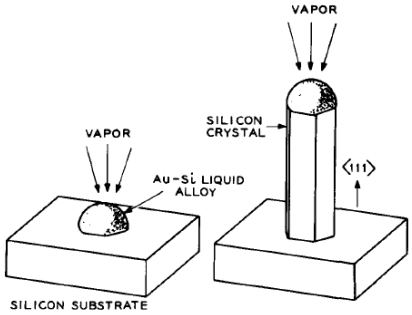
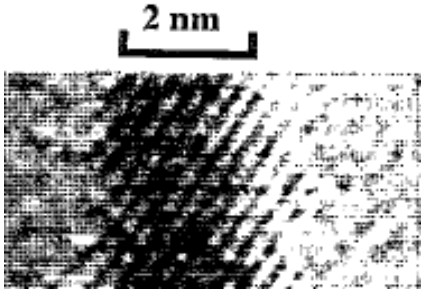
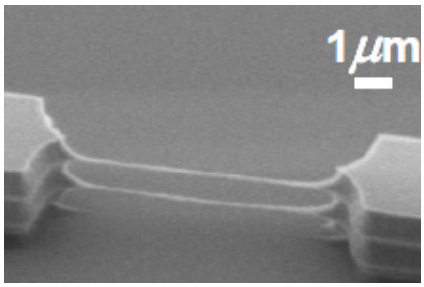
## 2.5 State-of-Art: vertically stacked nanostructure fabrication

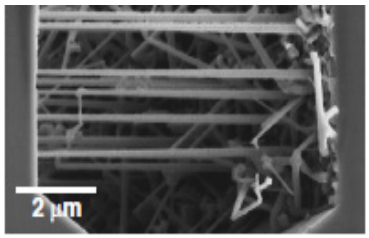
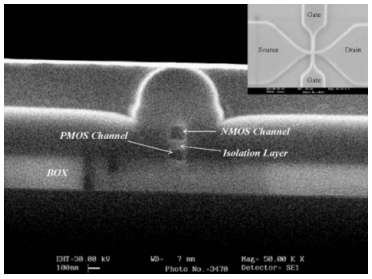
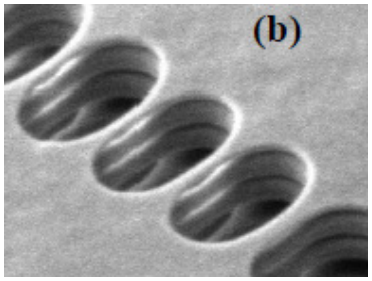
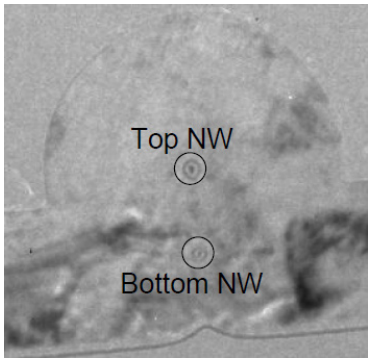
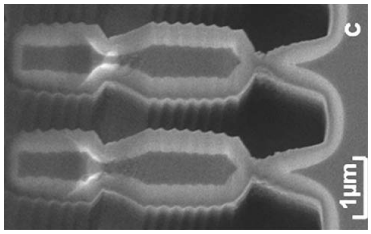
SiNWs were first prepared in the mid 1960's at the Bell Telephone Laboratories by growing them as crystalline Si whiskers by the vapor-liquid-solid (VLS) technique (a bottom-up approach) [66]. By VLS a metal catalyst is needed for the SiNW growth at temperatures as high as 1000 °C. With this method the nanowires had to then be transferred and aligned into a wafer or another substrate for further processing. This process is limited as it introduces too much variation, is complicated and only certain geometries can be produced. It was not until the early 1990's that a top-down method that uses self-limiting thermal oxidation (low temperature thermal oxidation, 800 °C) for fabricating silicon nanowires down to the nm scale on silicon wafer substrates was proposed by a group from Stanford [67, 68]. Active areas were first patterned by electron beam lithography (EBL) and defined by a reactive ion etch process with the resulting structures further being reduced in diameter by self-limiting oxidation. Vertically stacked SiNWs were first fabricated a decade later by Doherty *et al*. [69]. This group from Berkley utilized the BOSCH process (isotropic $SF_6$ plasma

etch followed by a passivation $C_4F_8$ step in consecutive cycles) with which they first produced scalloped trenches that serve as the basis for the silicon nanowires that are later formed by thermal oxidation. The Hewlett Packard Laboratories soon thereafter produced high density vertically stacked nano-bridges by a method that combines conventional top-down fabrication techniques with the bottom-up VLS growth of SiNWs [70]. Metal catalyzed SiNWs are horizontally grown from a patterned <111>-oriented vertical Si sidewall to bridge an opposing wall. This method nevertheless does not produce uniformly stacked arrays, nor is the thickness or shape of the produced SiNWs uniform from sidewall to sidewall. Another method was then proposed by Samsung to fabricate vertically stacked Fins/SiNWs by using double layer SOI (two single crystal Si films separated by an oxide layer) wafers produced by oxygen implantation [71, 72]. Needless to say, this fabrication process can be complicated and expensive. Not long after, the Deleonibus group from CEA –LETI in France [73-75] and the Kwong group [43, 47] from the Institute of Microelectronics in Singapore utilized an epitaxy-based approach to realize arrays of vertically stacked nano-beams and nanowires, respectively in order to increase current drive. The GAA transistors are realized by the alternate deposition of epitaxial Si and Ge/SiGe layers followed by a dry etch Fin definition. The Kwong group [43, 47] uses the different oxidation rates of the Ge and SiGe layers with respect to Si and a buffered oxide etch (BOE) wet etch process to release the NWs. The Deleonibus group [73-75] alternatively, separates the SiNWs by an isotropic selective dry etch. While the number of nanowires that can be stacked in the vertical dimension is technically unlimited, it can be expensive and time consuming due to the need for epitaxial layer deposition. Also, such high NW density may not be necessary and can hinder their implementation into biosensing applications. Furthermore, lattice mismatch between Si and SiGe limits the thickness of the Si layer so that only silicon nano-beams, nano-ribbons or NWs can be easily fabricated [76]. The Kwong group [44] subsequently used a similar fabrication scheme to that of Liu *et al*. [67, 68] to create a vertically stacked twin transistor except that active areas were patterned and etched down to the buried oxide (BOX) in an SOI substrate to create Fins. Then, due to a self-limiting oxidation process two silicon nanowire cores are formed instead of one, one on top and one at the bottom of the Fin. Although the twin SiNW fabrication scheme is interesting, it is limited as only two SiNWs vertically stacked can be formed.

Ng *et al*. [77] were finally the first to finally use the much simpler BOSCH process as proposed by Doherty *et al*. [69] to produce a high NW density FET in a GAA configuration in bulk-Si. Bopp *et al.* [76] from EPFL proposed a similar approach that also utilizes the BOSCH process to create vertically stacked Fins as will be seen in Section 3.2. The fabrication evolution from a single SiNW and the different approaches proposed over the years to create vertically stacked structures are furthermore summarized in the following Table 2-1.

**Table 2-1:** The evolution of the vertically stacked SiNW/Fin FET

| Figure | Fabrication approach description | Ref./Year |
|---|---|---|
|  | Si whiskers from metal (Au) droplet by VLS method ($SiCl_4$ vapor), bottom-up approach. | Wagner *et al.* [66]<br>Bell Telephone Laboratories<br>1964 |
|  | Single level SiNWs by EBL + RIE and self-limiting dry oxidation, first top-down approach, SiNWs $d_{NW}$ < 10 nm. | Liu *et al.* [67]<br>Stanford<br>1993 |
|  | First to propose fabrication of vertically stacked SiNWs by BOSCH followed by thermal oxidation, top-down approach. | Doherty *et al*. [69]<br>Berkeley<br>2003 |

| Figure | Fabrication approach description | Ref./Year |
|---|---|---|
|  | Metal catalyzed growth of SiNWs on a patterned vertical silicon wall to bridge opposing wall. Top-down method. | Islam *et al.* [70] Hewlett Packard 2004 |
|  | 3D stacked SiNW/Fin transistor and inverter using double layer SOI. | Chan *et al.,* [71] Samsung 2004 |
|  | 3D vertically stacked transistor Si, SiGe/Ge epitaxial deposition and selective isotropic etch or oxidation followed by BOE release, top-down approach | Institute of Microelectronics, Singapore [47] 2006 |
|  | Vertically stacked twin SiNWs non-volatile memory, Fins are defined by dry etch, NWs are formed by self-limiting oxidation that forms twin stacked wires. | Institute of Microelectronics, Singapore [44] 2007 |
|  | Vertically stacked Fins by BOSCH, $SF_6$ isotropic etch and thermal oxidation. | Bopp *et al.* [76] EPFL 2010 |

As previously mentioned, the concept of using the natural scalloping effect resulting from consecutive BOSCH cycles has also been utilized in this work. It allows for the 3D integration of stacked structures utilizing typical and inexpensive semiconductor/MEMS (microelectromechanical systems) fabrication processes. With the BOSCH process it is also possible to create ultra-thin, suspended, single crystalline long structures propitious for FET based biosensors. Nonetheless, as will be seen in Chapter 3 of this thesis careful design and optimization of not only the BOSCH process recipe, oxidation and wet-etch parameters but the initial mask layout is indispensable to fully take advantage of this approach.

## 2.6 State-of the-Art: pH and biotin-streptavidin sensing

Biotin-streptavidin was chosen as a model system to investigate the performance of our vertically stacked SiNW sensor for protein detection as it is well known, has one of the strongest non-covalent binding interactions in nature, and very fast association kinetics [1, 14-17]. Furthermore, protein sensing in general is interesting because of the lack of a polymerase chain reaction (PCR) equivalent amplification process (typically used to make millions of copies of a particular DNA sequence for analysis) for proteins [5]. This presents an important need for the direct detection and identification of proteins at ultra-low concentrations that can potentially be addressed by SiNW FET biosensors [5].

Table 2-2 shows the state-of-the art results for protein (avidin, streptavidin, biotin, *etc.)* sensing realized with SiNW FETs. Their geometrical dimensions (*H*: height, *L*: length, *W*: width), type of structure (ribbon, trapezoidal, *etc.*) type of substrate used (silicon-on-insulator: SOI, or bulk silicon), fabrication approach (top-down or bottom-up), type of gating (BG: backgate, TG: top-gate, RE: Reference electrode, *etc.*) and lowest concentration limits achieved are included in the table when available for comparison. The lowest protein concentrations reported to have been measured in literature (to the author's knowledge) by SiNW/Fin FET based sensors alone are in the order of the tenths of fM [14-16]. Attomolar protein concentrations have also been detected before by the use of SiNW-FET based biosensors when used in conjunction with electrodes for the pre-concentration of the protein by electro-kinetic transport and integrated in a common chip [78], for example. Though the sensing result specifics will be presented in Section 6.2.4, they are summa-

rized here in Table 2-2 for comparison. It will be shown that with the SiNW array developed in this work it was possible to measure down to 17 aM of streptavidin.

**Table 2-2:** State-of-the-art for SiNW-FET based protein sensing. APTMS: (3-Aminopropyl)-trimethoxysilane, HEPES: 4-(2-hydroxyethyl)-1 piperazineethanesulfonic acid.

| Description | Substrate fabrication | Dimensions | Gating | Concentration Limits | Remarks | Ref. |
|---|---|---|---|---|---|---|
| Single trapezoidal SiNWs | SOI Top-down | W = 50 nm H = 25 nm | BG | 1 nM -10 fM streptavidin detection floor 70 aM | -$SiO_2$ surface biotin modified - Different pH values investigated | Stern *et al.* [14] |
| SiNWs Array | Bulk-Si Bottom-up | NA | BG | 10 pM streptavidin | $SiO_2$ surface biotin modified | Cui *et al.* [1] |
| Si nano-ribbon | SOI Top-down | W = 45-100 nm H = 50 nm L = 1.2 µm | BG | 10 fM streptavidin | $SiO_2$ surface biotin modified | Elfström *et al.* [15] |
| Random SiNWs | Bulk-Si Bottom-up | NA | N/A | 15 fM biotin | -$SiO_2$ surface APTMS-avidin modified -Modified prior to SiNW placement to reduce sensing area | Li *et al*. [16] |
| Single SiNW | SOI Top-down | W = 1 µm H = 45 nm L = 10 µm | RE | 200 fM streptavidin | -$SiO_2$ surface HEPES modified -NHS-$PEG_4$ linker biotin modified | Duan *et al.* [17] |
| SiNW + electrodes for electrokinetic preconcentration | NA | NA | NA | aM cancer protein (prostate specific antigen) PSA | Coplanar microelectrodes to sides of SiNW to form concentrated stream near NW surface | Gong [78] |
| **SiNW 3D Array** | **SOI Top-down** | **$d_{NW}$ = 15-30 nm L = 2 – 4 µm** | **RE** | **Down to 17 aM streptavidin** | **Up to 7 × 20 SiNW array** | **This work Buitrago *et al.* [79]** |

Furthermore, pH plays a key role in different biologically important processes and is an important parameter for both intra and extra cellular health [80]. The shape, activity and ultimate functionality of proteins [80] and other biologically relevant molecules, depends on the pH of the bathing medium [81, 82]. Aside of being important for clinical applications, accurate pH sensing at broad ranges is also necessary for environmental [83] and food industry [84] implementations. Consequently, pH sensing has also been investigated in this thesis. Table 2-3 shows the state-of-the-art results for pH sensing with SiNW FET sensors when $SiO_2$ alone is used as the gate dielectric or this oxide has been modified by an organic linker such as APTES. The transistor performance characteristics ($I_{on}$, $I_{off}$, $I_{on}/I_{off}$ ratios, $SS$) and sensitivity characteristics ($\Delta I_d/pH$ and $\Delta V_{th}/pH$) are additionally included in the table when available. The table also includes our results for comparison.

**Table 2-3:** State-of-the-art literature results for SiNW-FET based pH sensing when $SiO_2$ is used as the gate dielectric alone or it has been surface functionalized.

| Description | Substrate fabrication | Dimensions | Gating | pH response Transistor performance | Remarks | Ref. |
|---|---|---|---|---|---|---|
| Single trapezoidal SiNWs | SOI Top-down | W = 50 nm H = 25 nm | BG | $\Delta I_d$/pH ~ 0.82 – 1 dec/pH (pH = 6 – 8) | -surface not modified -High operation voltages used | Stern *et al.* [14] |
| SiNWs array | Bulk-Si Bottom-up | NA | BG | $\Delta I_d$/pH = 100 nA/pH (pH = 2 – 9) | -surface not modified: $\Delta V_{th}$/pH non-linear -APTES modified: $\Delta V_{th}$/pH linear | Cui *et al.* [1] |
| SiNW array | SOI Top-down | W = 50 nm L = 10 µm | Integrated RE | $\Delta V_{th}$/pH = 40 mV/pH (pH = 2 – 12) $I_{on}/I_{off} = 10^5$ SS = 100 mV/dec | -surface not modified: $\Delta V_{th}$/pH non-linear -Static measurements | Kim *et al.* [21] |
| FinFET array | SOI Top-down | W = 15 nm H= 85 nm L = 10 µm | Integrated RE | $\Delta I_d$/pH ~ 0.5 dec/pH $\Delta V_{th}$/pH = 35 mV/pH (pH = 4 – 10) $I_{on}/I_{off} = 10^7$ SS = 80 mV/dec | surface not modified: $\Delta V_{th}$/pH linear | Rim *et al.* [22] |

| Description | Substrate fabrication | Dimensions | Gating | pH response Transistor performance | Remarks | Ref. |
|---|---|---|---|---|---|---|
| Single triangular SiNWs | SOI Top-down | L = 16 µm W = 20 nm | BG | $\Delta I_d$/pH = 80 nA (pH = 5 – 9) | -surface not modified -APTES modified | Gao *et al.* [85] |
| SiNW array triangular | SOI Top -down | W = 10 nm H = 100 – 140 nm | BG TG (Pt) | $\Delta V_{th}$/pH = 48 mV/pH | -surface not modified: $\Delta V_{th}$/pH non-linear | De *et al.* [86] |
| Single SiNWs | SOI Top -down | W = 100 nm H = 55 nm L = 5 µm | BG RE | $\Delta V_{th}$/pH = 59 mV/pH | -surface not modified -High operation voltages used | Presnov *et al.* [30] |
| Thin film resistor, Hall-bar configuration | Top -down SOI | W = 80 µm H = 30 nm Hall-bar center L = 240 µm | RE BG | $\Delta V_{th}$/pH = 50 mV/pH | -$SiO_2$ surface not modified -High operation voltages used | Nikolaides *et al.* [31] |
| SiNW array | SOI Top-down | W = 100 nm – 1 µm H = 55 nm L = 3 µm | BG RE | $\Delta I_d$/pH ~ 0.35 dec/pH (pH = 2 – 10) $\Delta V_{th}$/pH = 41 mV/pH SS = 85mV/dec | -$SiO_2$ surface not modified: $\Delta V_{th}$/pH linear | Vu *et al.* [87] |
| SiNW array nano-gratings | SOI Top-down | W = 50 nm H = 30 nm L = 20 µm | RE | $\Delta I_d$/pH = nA/pH (pH = 2 – 9) $\Delta V_{th}$/pH = 50 mV/pH $I_{on}/I_{off} = 10^6$ SS = 80 mV/dec down to 63 mV/dec | -surface APTES modified: $\Delta V_{th}$/pH linear | Regonda *et al.* [29] |
| **SiNW 3D Array** | **SOI Top-down** | **$d_{NW}$ = 15-30 nm L = 2 – 4 µm** | **RE** | **$\Delta I_d$/pH = up to 10ths of µA/pH (pH = 4 – 10) $\Delta V_{th}$/pH = 50 mV/pH $I_{on}/I_{off} > 10^6$ SS ~ 95 mV/dec down to 85 mV/dec** | **-surface not modified: $\Delta V_{th}$/pH non-linear -APTES modified: $\Delta V_{th}$/pH linear** | **This work Buitrago *et al.* [79]** |

# 2.7 Design considerations

## 2.7.1 SiNW/Fin cross section, channel doping concentration

The Debye screening length $\lambda_L$ is the characteristic length over which a charged particle can exert electrostatic control on a semiconductor surface (*e.g.*, ~ 40 nm for a $10^{16}$ $cm^{-3}$ doped silicon) [88], Equation 2.7:

$$\lambda_L = \sqrt{\frac{\varepsilon_r \varepsilon_0 k_B T}{q^2 N_d}}$$

**Equation 2.7**

With $\varepsilon_r$ being the relative dielectric constant of the material, $\varepsilon_0$ being the vacuum dielectric constant, $q$ being the elementary charge and $N_d = n + p$ being the concentration of electrons and holes ($n$ and $p$), respectively, for doped semiconductors, $k_B$ being the Boltzmann's constant and $T$ being the absolute temperature. When the NW/Fin dimensions are comparable or higher than $\lambda_D$, molecular gating is more efficient and better control of the conducting channel is achieved which also translates to high sensitivities [18, 51]. Because the Debye length depends on the channel doping concentration ($\lambda_L \propto \sqrt{1/N_d}$), it has been shown in literature that lightly doped channels exhibit greater sensitivities than highly doped or undoped channels [51, 89, 90].

In terms of the FET performance, low channel doping concentrations are necessary to have fully depleted channels for high electrostatic control of the channel and reach high carrier mobilities [50]. For all these reasons, in this work an SOI wafer with a low doped silicon device layer is used and ultra-thin Fin/NW arrays (Fin width, $F_W$ < 40 nm, nanowire diameter, $d_{NW}$ < 35 nm) were targeted for fabrication.

## 2.7.2 Sensing area

The kinetics of sensing for a single nanowire system have been simulated before as a function of NW dimensions by the use of traditional transport modelling equations [91]. With the assumption that there is no active method of directing biomolecules to the SiNW area, the authors found the

NW length to be a critical dimension for analyte accumulation on the NW surface. That is because the sensor response depends on the total analyte flux (# molecules/time × area) over the sensing wire. For such a system long channels $L > 100$ nm were found to be necessary to guarantee biological interaction with the single NW surface at ultra-low concentrations (pM) within reasonable time scales.

Mass transport limitations undoubtedly exist in microfluidic channels for which mixing mostly occurs by diffusion. In such systems, biomolecules present in pM concentrations may have lower possibilities to be detected. Squires *et al*. [92] explores this issue by furthermore taking into account different competing physical processes (target molecule diffusion, target molecule interaction with other target molecules, *etc.*) that happen in a more realistic microfluidic biosensor experiment as fM concentrations have been reported in literature within single NW systems [14] that cannot be explained by traditional transport modelling. The highly dense NW structure presented here provides a large surface area and therefore higher chances for sensing interactions addressing this issue.

## 2.7.3 Sensing interface

One aspect that deserves some thought when designing a sensor structure is the surface passivation material which acts as a gate dielectric. $SiO_2/SiO_x$ has been found to be not to the best pH sensitive material inducing less than ideal non-linear threshold voltage shifts per pH (for broad pH ranges 2 – 12) of 35 – 50 mV/pH [21, 22, 31, 86, 87, 93] as can be seen in Table 2-3. High-$\kappa$ dielectrics such as $HfO_2$ [28, 94], $Al_2O_3$ [27, 94] and $Ta_2O_5$ [40] have been used to achieve near ideal and linear Nerstenian pH responses (59 mV/pH at room temperature) independent of ionic strength [94]. Table 2-4 shows state-of-the art results for SiNW pH sensors for which a high-$\kappa$ dielectric layer has been used. These oxides can furthermore be modified or left untouched for pH sensing. Atomic layer deposition (ALD) layers of high-$\kappa$ dielectrics have also been used to prevent charge penetration through the oxide to the SiNWs and reduce leakage currents through the liquid [19]. Nonetheless, one must remember that the SiNW-dielectric interface is also important for the electrical stability of the device. For example, $HfO_2$ deposited directly on top of Si or native oxide has been shown to degrade the transistor characteristics (large subthreshold slopes and hysteresis) due to

interface charge trapping. It has been shown therefore necessary to deposit or grow an interfacial $SiO_2$ buffer layer [95-97]. Though native oxide forms spontaneously when Si is exposed to air (~ 2 nm), to deposit or grown a high quality oxide may nevertheless be difficult or impossible due to the thermal budget limitations imposed by certain fabrication process flows such as ours as will be presented later in this thesis (Section 5.4.6, Section 6.1.1).

**Table 2-4:** State-of-the-art literature results for SiNW-FET based pH sensing when an insulator with a high-$\kappa$ dielectric constant is used. HMDS: Hexamethyldisiloxane.

| Description | Substrate fabrication | Dimensions | Gating | pH response Transistor performance Current levels | Remarks | Ref. |
|---|---|---|---|---|---|---|
| FinFET array | SOI Top-down | W = 6 nm H = 26.5 nm L = 5 µm | RE | $\Delta I_d$/pH ~ 0.9 dec/pH, ~ 650%/pH (pH = 4 – 10) $\Delta V_{th}$/pH = 59 mV/pH SS = 77 mV/dec | $SiO_2$/$HfO_2$ surface not modified: $\Delta V_{th}$/pH linear | Zafar *et al.* [28] |
| Single triangular SiNWs | SOI Top-down | H = 140, 100 nm W = 20 nm | BG RE | -$\Delta V_{th}$/pH = 57.8 mV/pH $Al_20_3$ -$\Delta V_{th}$/pH = 40 mV/pH -$\Delta V_{th}$/pH = 50 mV/pH | -$Al_2O_3$, $SiO_2$ surfaces not modified: $\Delta V_{th}$/pH non-linear -APTES and HMDS modified : $\Delta V_{th}$/pH linear | Chen *et al.* [27] |
| Single SiNWs | SOI Top-down | W = 100 - 1000 nm H = 80 nm L = 6 µm | RE | (pH = 3 – 10) $\Delta V_{th}$/pH = 56 mV/pH SS = 100 mV/dec | $Al_2O_3$, $HfO_2$ surface not modified: $\Delta V_{th}$/pH linear | Tarasov *et al.* [94] |

As an alternative, covalently bound organic layers have been proposed as superior insulating materials to $SiO_2$/$SiO_x$ on silicon alone [98-100], Table 2-2. The passivation of the silicon surface via strong covalent Si–O–Si bonds can provide well defined and stable layers with insulating properties [101]. Particularly, APTES has been widely used not only as a sensitive layer but as well as a chemical linker for further surface modification as it is done in this thesis. APTES is a highly reac-

tive organosilane that forms covalent bonds to hydroxyl-terminated (–O–H) surfaces through silanization chemistry [100]. The covalent bonding of APTES to the oxide surface results in a surface termination with both amine ($–NH_2$) and silanol (–Si–OH) groups that can undergo protonation or deprotonation as a function of pH [1]. At low pH values the $–NH_2$ groups are protonated to $-NH_3^+$ acting as a positive gate thus increasing the drain current for n-type FETs. When the surface is exposed to a high pH solution the Si–OH groups at the surface are deprotonated (negative gate) to $SiO^-$ and the $I_d$ decreases accordingly. In comparison to unmodified $SiO_2$ surfaces APTES functionalized SiNW FETs show linear $\Delta V_{th}/pH$ (up to 50 mV/pH for broad pH ranges) due to the presence of both amine and silanol groups with different acid dissociation constants [1, 21, 27, 29, 36, 86].

In this work, APTES is furthermore used as a linker for subsequent biotin surface modification. Biotin acts as a specific receptor for streptavidin (target molecule) sensing [1, 14-17].

## 2.7.4 Sensing analyte

The characteristic Debye screening length $\lambda_D$ of a solution is defined by Equation 2.8:

$$\lambda_D = \sqrt{\frac{\varepsilon_r \varepsilon_0 k_B T}{2 N_A q^2 I}}$$

**Equation 2.8**

$I$ is the ionic strength in [mol/L], $\varepsilon_0$ is the vacuum dielectric constant, $\varepsilon_r$ is the dielectric constant of the solution (80 for water), $k_B$ is the Boltzmann's constant, $T$ is the absolute temperature, $N_A$ is the Avogadro number and $q$ is the elementary charge. Dilute buffer solutions with low ionic strengths have been widely used in order to improve the sensor response of the device by increasing the Debye screening length ($\lambda_D \, \alpha \, \sqrt{1/I}$). Nonetheless, it is important to consider that the function, stability, net charge and biological activity of protein molecules depend on the ionic concentration, ion species, and pH of the solution [46, 102, 103]. Streptavidin has for example a weakly acidic isoelectric point (pI ~ 5.6) and therefore a negative charge at pH = 7.4 [17]. The bound streptavidin-biotin system leads to a reduced drain current for an n-type channel FET. In here, a medium range concentration of 10 mM solution of phosphate buffered saline (PBS) with pH = 7.4 has been used.

### 2.7.5 Gating

As previously discussed, the FET sensor response or current change is dependent on the operating point at which the sensor measurements are carried out. For that reason, a reference electrode is an indispensable part of a FET measurement set-up. Fundamentally its function is to provide a stable electrical contact to the test electrolyte and define the operation point of the FET sensor [104-106]. It must also provide for an electrode-electrolyte interface potential that does not vary with electrolyte composition (pH, ionic concentration) so that changes in $I_d$ of the device are a measure only of changes in its electrolyte-gate insulator interface [104-106]. Commercial reference electrodes (*e.g.*, Ag/AgCl or calomel) provide that function. In here, not only Pt side-gates were directly patterned on the chip for quick characterization of the FET characteristics of the device, but an Ag/AgCl electrode was integrated for accurate sensing measurements in an electrolyte environment.

For true miniaturization and successful integration of FET sensors into portable, low cost systems it is necessary to eliminate the use of the external reference electrode typically needed to provide a stable contact to the solution. Pt, as a noble metal is inherently less sensitive to corrosion. However, such an electrode still does not provide a stable reference over time. For that reason, the use of a pseudo reference electrode (noble metal) integrated into a differential pair circuit has been explored before in order to circumvent this issue [104, 107-109]. The differential circuit consists of an ion sensitive (ISFET), an insensitive reference FET (REFET). The quasi reference electrode instability in an electrolyte can be cancelled by applying differential sensing, in which two similar devices can be used to cancel common-mode inputs such as noise or, in this case, potential variations at the electrode/electrolyte interface [110]. Though differential pairs are often implemented as operational transconductance amplifiers (OTA) using six active devices (2 p-type and 4 n-type MOSFETs), the use of resistors as loads is necessary here as the fabrication of MOSFETs is not directly compatible with our current process flow. A resistor based ISFET/REFET differential circuit was explored through Cadence 6 Analog Design Environment (ADE) and was found to be a theoretically a suitable implementation for our current biosensing system (Appendix B, the vertically stacked nanowire sensor was first modeled using Verilog-A). For the actual application of the differential circuit with our devices the REFET surface passivation would need to be accomplished as well. This is nonetheless, beyond the scope of this thesis' work. Additionally, the Pt side-gate was ultimately

found to react with the electrolyte solution over time (Chapter 5) and therefore is also not suitable for such implementation.

SiNW based FET sensors when operated in a double gate configuration (*e.g.*, $V_{Ref}$ and backgate $V_{BG}$) have been reported to show threshold voltage shifts with pH surpassing the Nernst limit of $\Delta V_{th}/pH$ ~ 60 mV/pH [19, 24, 26, 111-113] as can be seen in Table 2-5. Different authors theorize that in the backgate-liquid-gate configuration one gate can act as a driving gate that controls the current flow within the NW while the other acts a supporting gate that amplifies the threshold voltage shift as a function of pH [24, 113].

**Table 2-5:** State-of-the-art literature results for SiNW-FET based pH sensing when a double gate (DG) configuration has been used to amplify the pH sensing response. SG*:* side-gate.

| Description | Substrate fabrication | Dimensions | Gating | pH response Transistor performance | Remarks | Ref. |
|---|---|---|---|---|---|---|
| Single SiNWs | SOI<br>Top-down | W = 100 nm<br>H = 50 nm<br>L = 20 µm | DG:<br>SG<br>RE | $\Delta I_d$/pH = 10 nA/pH $\Delta V_{th}$/pH = up to 720 mV/pH | -$SiO_2$ surface not modified<br>-High operation voltages used | Yoo *et al.*<br>[25] |
| nanoplate | SOI<br>Top-down | W = 2 µm<br>L = 20 µm<br>H = 27 nm | DG:<br>SG -Pt<br>BG | $\Delta I_d$/pH = 0.7 dec/pH<br>$\Delta V_{th}$/pH = 150 mV/dec | -$SiO_2$ surface not modified<br>-Operation point investigation | Elibol *et al.*<br>[26] |
| Polysilicon NW | Bulk<br>SOI<br>Top-down | W = 40 nm L = 10 µm | DG:<br>BG<br>SG | $\Delta V_{th}$/pH = 110 mV/pH<br>SS = 450 mV/dec | -$SiO_2$ surface not modified | Chen *et al.*<br>[114] |
| Si nanoplate SiNW pair | Top-down | Plate:<br>W = few µm<br>H = 100 nm | SG<br>BG<br>nanoplate | $\Delta V_{th}$/pH = 10 V/pH | -$SiO_2$ surface not modified | Go *et al.*<br>[112] |
| Single SiNWs | SOI<br>Top-down | W = 700 nm<br>H = 60 nm<br>L = 10 µm | BG<br>FG<br>RE | $\Delta V_{th}$/pH = up to 220 mV/pH<br>SS = 80-100 mV/dec (dry BG) | -$SiO_2$ surface not modified<br>-Little hysteresis<br>-High operating voltage used | Knopfmacher *et al.*<br>[19] |
| Single SiNWs | SOI<br>Top-down | W = 110 nm<br>H = 55 nm<br>L = 1 µm | Two SGs by SiNW sides | $\Delta V_{th}$/pH = 68 mV/pH<br>SS = 500 mV/dec | -$SiO_2$ surface not modified | Ahn *et al.*<br>[24] |

Nonetheless, the Nernst theory describes a thermodynamic system for which the sensitivity parameter $\alpha$ is fundamentally limited by the gate dielectric utilized, the ionic concentration of the solution, and temperature [36] as seen before in Section 2.3.

In this work, the NW channels can be gated by a backgate and by one or two of the symmetrical platinum side-gates through a solution. With this configuration, when ideal bias conditions are utilized, it is possible to gate the stack of NWs more efficiently from different sides in order to achieve excellent transistor characteristics (improved *SS*) that should consequently -in theory- improve the sensitivity of the device. This will be seen in Section 5.4.7 of this thesis when the device is gated through isopropanol (IPA). Yet, as previously discussed, the Pt electrodes do not provide a stable contact when an electrolyte is used and for that reason such behavior was only investigated with isopropanol.

## 2.8 Summary

Silicon nanowire field effect transistors continue to draw attention for a large number of applications in the biosensor field. They are interesting due to their nanoscale channel dimensions that allow for the presence of just a few charged molecules on the SiNW surface to exert electrostatic control over the drain to source current making the devices greatly sensitive compared to the traditional planar ISFET. The inherent transistor characteristics of the device, the $\Delta V_{th}$ shift resulting from the electric field induced by a sensing event (dependent on the gate dielectric, ionic concentration, *etc.*), and the availability of surface area for sensing interactions all limit the sensor response or the lowest concentration possible to be measured with such nano-devices. A vertically stacked sensor consisting of an array of suspended NWs or Fins in between the source and drain anchoring contacts with symmetrical Pt gates to the sides has been proposed here. The main contributions for the implementation of such device are:

- The potential to for ultra-low concentration sensing due to the high density array of available sensing channels. The high number of channels also provides high drain currents.
- The possibility to operate the field effect transistor using an integrated reference electrode, side-gates or backgate in a GAA-type configuration through a liquid.

- The structure can be fabricated by a top-down, CMOS compatible processes. With the BOSCH process one can take advantage of the natural scalloping effect created in silicon to form ultra-thin, stacked, suspended structures for high sensitivities at low cost.

# Chapter 3 Fabrication of vertically stacked Si nanostructures

In the next sections of this thesis the process optimization and development efforts for the successful fabrication of stand-alone vertically stacked structures (short-loop processes) and their eventual implementation into FET biosensor systems will be described. The short-loop process optimization was necessary to efficiently produce uniform, robust, thin and highly dense structures. The majority of the fabrication steps were performed at the center for micro-technology (CMi) at EPFL, Switzerland. The microfluidic channels were designed and fabricated in collaboration with Imperial College London, London, UK as part of the SiNAPS European project.

## 3.1 Short-loop process optimization-vertically stacked SiNWs

The short-loop process (for both SiNWs and Fins) consists only of one electron beam (e-beam) masking level. Silicon test wafers with a 5 inch diameter, doped p-type boron (0.1 – 100 Ohm · cm) with a thickness of 525 ± 25 μm and <100> orientation were used. A low temperature oxide (LTO) is first deposited as a hard mask (50 – 100 nm) on a test wafer (Figure 3-1a, cross section and top-view of the wafer). ZEP-520A (Nippon-Zeon), a positive high resolution e-beam resist is patterned by e-beam lithography in a Vistec EBPG500 system (Figure 3-1b). LTO as a hard mask is necessary in order to be able to make structures with many NWs vertically stacked. The hard mask is subsequently defined by a selective anisotropic dry etch ($SF_6$ and $C_4F_8$ mixed). The wafers are processed in an Alcatel AMS200 inductively coupled plasma (ICP) etching system (Figure 3-1c). The mask layout is designed so that the nanostructures are semi-embedded into the silicon but completely isolated from each other with side cavities to avoid high topography problems. This configuration allows for better bonding with the microfluidic channel/system integrated at the top of the device while leaving enough room for biomolecule diffusion from the sides and the top of the NW/Fin stack. The side cavities also allow for the fast visualization by scanning electron microscopy (SEM, Zeiss Leo 1550 or Zeiss Merlin) and AFM probing.

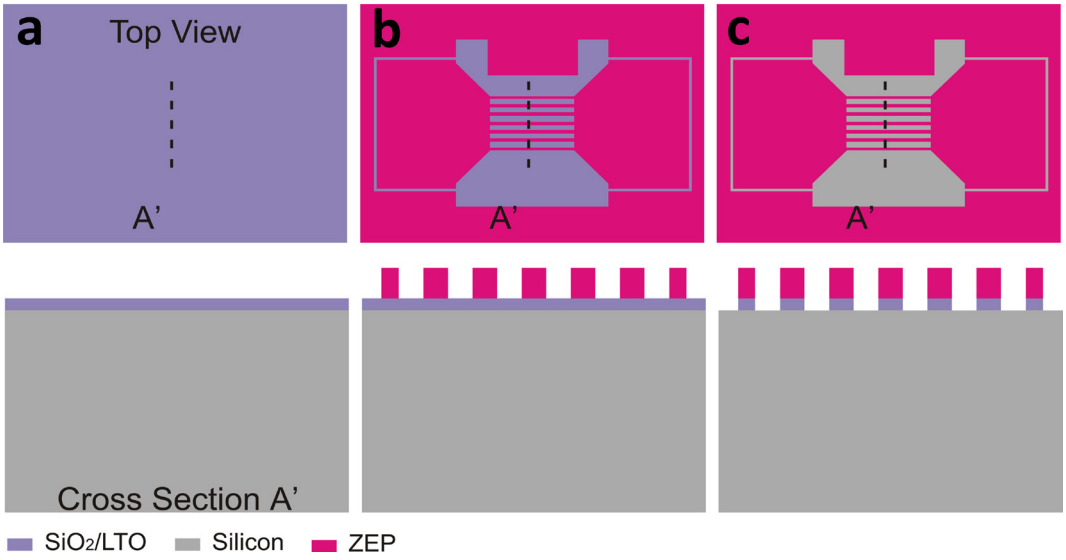



**Figure 3-1:** Schematic top-view and cross section of A' of (a) wafer with LTO hard mask, (b) ZEP definition after e-beam patterning and (c) hard mask defined by dry etch.

Once the hard mask has been patterned, scallops are formed by a BOSCH process in the same ICP plasma tool (Figure 3-2a). The NWs are finally defined by thermal oxidation (Centrotherm Oven, 950 °C) in a dry oxygen atmosphere (Figure 3-2b) and released from their silicon dioxide enclosure in a BOE (7:1, 40% $NH_4F$ in $H_20$: 49% HF) wet etch bath (Figure 3-2c). The structures can then be easily dried in an $N_2$ stream.

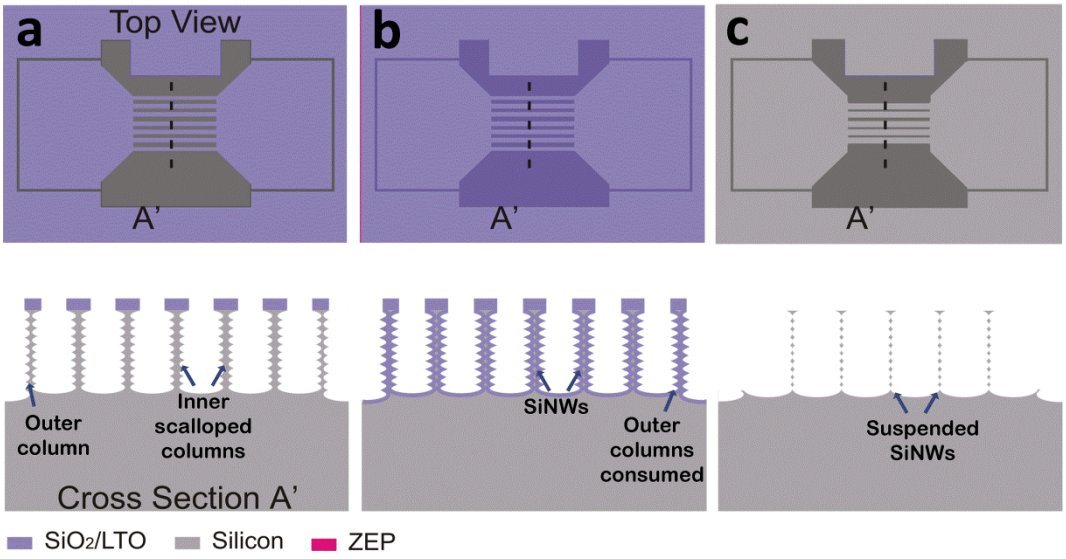



**Figure 3-2:** Schematic top-view and cross section of A' of (a) scalloped columns after BOSCH, (b) SiNWs formed after thermal oxidation and (c) suspended NWs formed after BOE wet etch.

The BOSCH process utilized here consists of a $C_4F_8$ passivation step (1 s), an $O_2$ (1 s) cleaning step and a $SF_6$ (2 s) isotropic etch step in consecutive pulsed cycles. Figure 3-3 shows this schematically. The $C_4F_8$ polymer passivation step serves to protect the trench sidewalls and it is first in the cycle after the hard mask has been patterned. An $O_2$ plasma step follows and functions to remove the polymer and open up the bottom of the scallop. The final step in the cycle is the $SF_6$ isotropic etch that lastly defines the scallop. The process temperature that offered the most reproducible results by reducing local reaction rates was 0 °C. The recipe was optimized to create round scallops that do not vary significantly in size and shape from top to bottom of the trench.

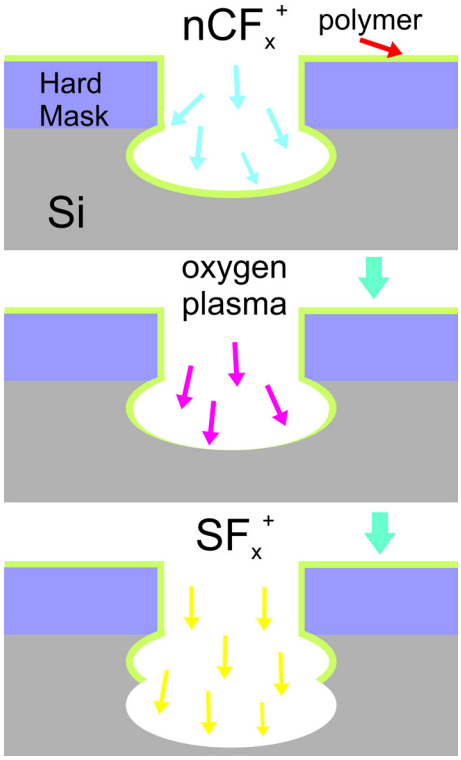



**Figure 3-3:** Schematic of BOSCH process cycle steps.

Different trench opening T (from 100 nm to 400 nm) and silicon spacer S (from 100 to 300 nm) width combinations were investigated. The outmost silicon spacers are deliberately smaller than the inner ones (schematically shown in Figure 3-4) in order to create outer dummy columns. The outmost scallops are wider than the inner ones due to the nature of the BOSCH process producing oddly shaped outer columns. For this reason the outer columns are designed so that the silicon

core is nearly or completely consumed during thermal oxidation and then later removed by the BOE release step.

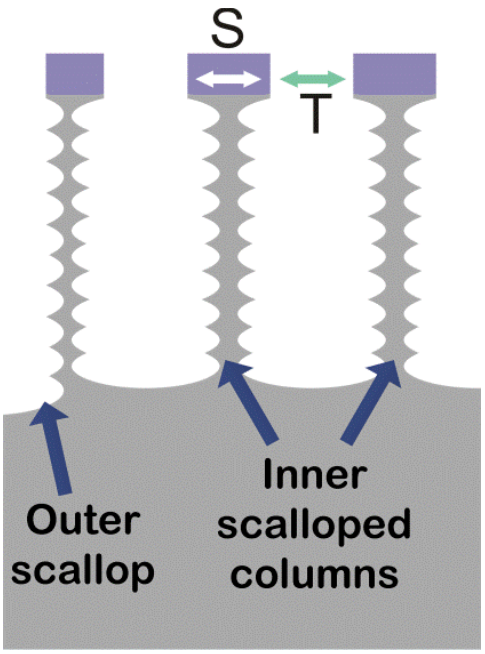



**Figure 3-4:** Trench opening T and silicon spacer S shown schematically. Left outer silicon spacer designed to be smaller than inner ones to be consumed after thermal oxidation. Scallop shape depends on trench opening width which results in oddly shaped outer column.

The SEM cross section micrographs of the structures with different S and T dimensions as they are processed under the same process conditions (temperatures, times, *etc.*) after BOSCH (Figure 3-5), thermal oxidation (Figure 3-6), and the BOE wet etch (Figure 3-7) are presented for comparison in the next page.

One can see in Figure 3-5 that the trench opening determines the shape and height of the scallop, with bigger openings resulting in bigger, deeper scallops. It is therefore clear from the figure that the trench opening dimensions ultimately determine the nanowire density (NWs/μm) in the vertical direction with T = 100 nm and T = 400 nm having the highest and lowest NW density respectively. The silicon trench spacing in combination with the trench opening dimensions determine the horizontal nanowire density.

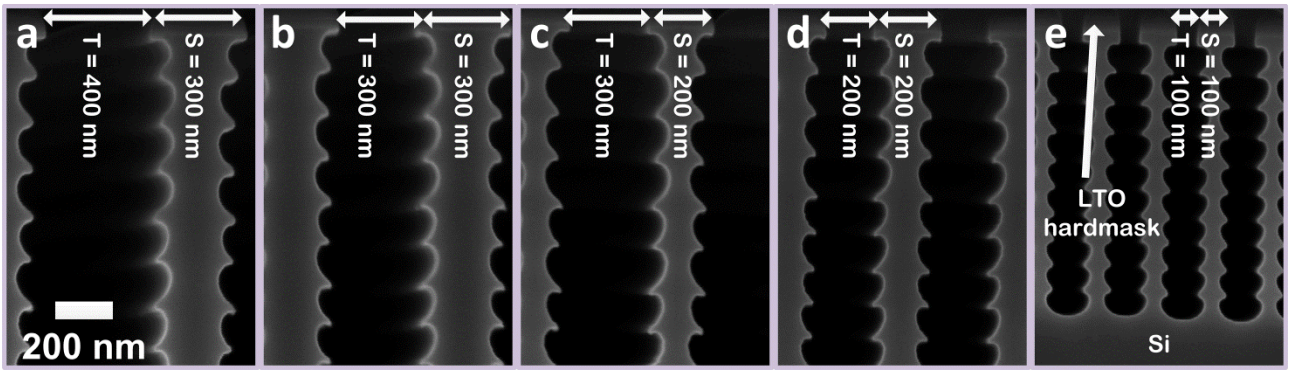



**Figure 3-5:** SEM cross section views of scalloping resulting from the BOSCH process with different trench openings and silicon spacer dimensions: (a) T = 400 nm, S = 300 nm, (b) T = 300 nm, S = 300 nm, (c) T = 300 nm, S = 200 nm, (d) T = 200 nm, S = 200 nm, (e) T = 100 nm, S = 100 nm. T determines the height of the scallop.

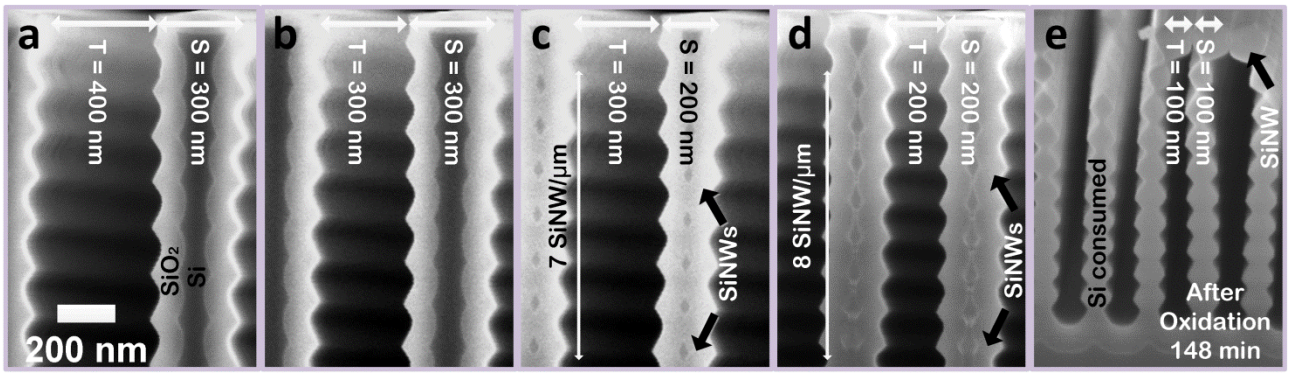



**Figure 3-6:** SEM cross section views of the SiNWs resulting after the scalloped structures from Figure 3-5 have been processed under the same thermal oxidation conditions.

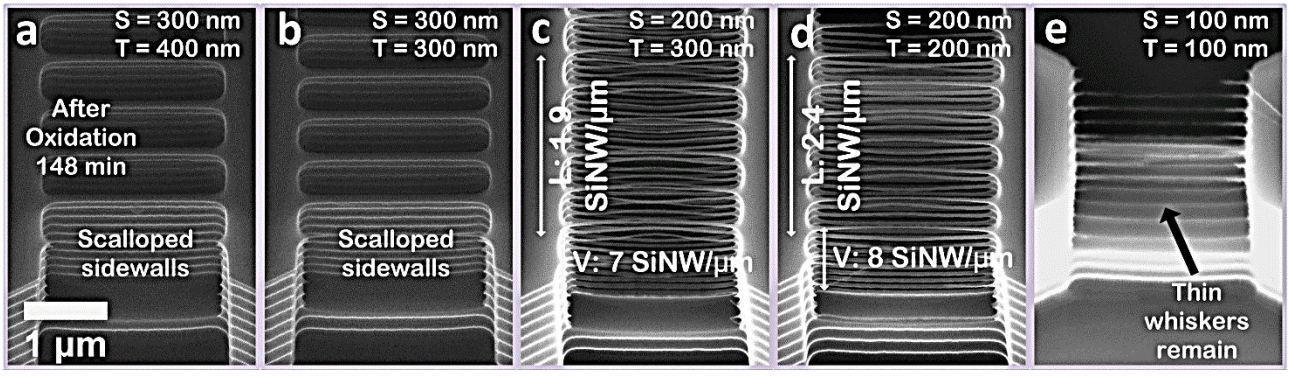



**Figure 3-7:** SEM top-side tilted-views of SiNWs and undulating columns resulting from the BOSCH process with different trench openings and silicon spacer dimensions as shown above after thermal oxidation and BOE $SiO_2$ removal.

The oxidation parameters (time, precursor gases, flows, and temperature) together with the BOE bath process specifications (dilution, time, *etc.*) but to a lower extent, ultimately define the final NW dimensions.

Figure 3-6a and b show that the oxidation time chosen (148 min) is not sufficient to consume enough of the Si to form NWs at the center of every two adjacent scallops for all of the S and T dimensions investigated (S = 400 nm, T = 300 nm and S = 300 nm, T = 300 nm). For the same oxidation time but smaller S (S = 200 nm, T = 300 nm and S = 200 nm, T = 200 nm) it is possible to form NWs as can be seen in Figure 3-6c and d. Finally, when S < 200 nm the Si is fully consumed when the same oxidation time is utilized. It is possible to see in Figure 3-6c and d that although a bigger trench opening (larger scallop) promotes the formation of smaller nanowires with the same oxidation process time the lateral and vertical NW density suffers. Also, the diameter range is much wider for the bigger trenches after the BOE release (Figure 3-7c and d). The NWs are uniformly distributed in the vertical direction and do not vary significantly in size from top to bottom. Arrays of nanowires with a vertical density of 6.25, 7, 8 and 10 SiNWs/μm, lateral density of 1.35, 1.6, 1.9, 2.4 and 5 SiNWs/μm (Figure 3-7) respectively, average diameters from 15 to 30 nm have been successfully released.

The silicon spacer dimensions are also important. First of all, one must avoid designing the silicon spacers too wide because though the structures can be reduced in diameter by increasing the thermal oxidation time, this induces stress. When releasing the nanowires from their silicon dioxide enclosure after being dramatically reduced by oxidation, they tend to bend and break due to the stress that builds up during this process. Second of all, if the silicon spacer width is too small as to almost create the nanowires through the BOSCH process alone nevertheless it is not possible to create uniform and reproducible structures with high density (> 4 – 6 vertically stacked NWs, Figure 3-8). This is because there is an inherent variation in the vertical direction from nanowire to nanowire going from top to bottom since the consecutive passivation/etch steps are cycled with the same process times. As we create more and more scallops the previous ones are also being passivated and etched again. Also, the process gases have to diffuse further into the trench. The variation becomes especially pronounced as some NWs at the top of the trench start to detach from the scalloped column at some point during the etching when the silicon spacer width is too small

(< 100 nm). If some structures are broken during the process, it can change the process gas flow patterns tremendously (the opening determines the final scallop dimensions) and therefore odd structures are formed.

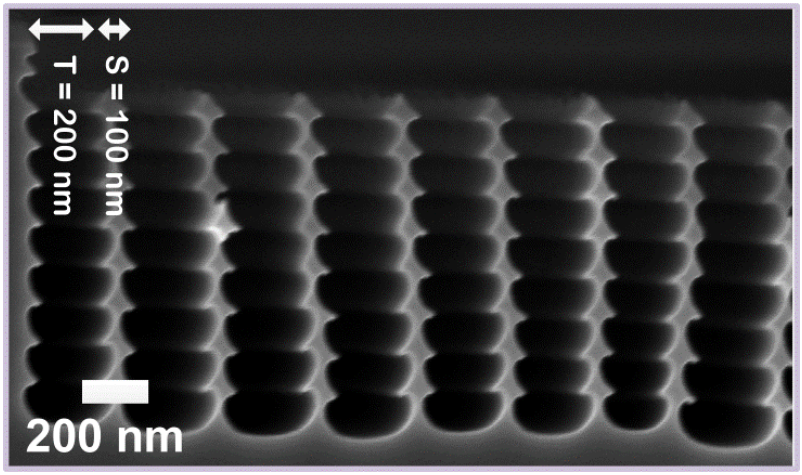



**Figure 3-8:** SEM cross section views of scalloping resulting from the BOSCH process with a trench opening and silicon spacer dimensions of T = 200 nm, S = 100 nm. Non-uniform scallops result.

In this work we were able to create structures with a high vertical and lateral NW density (10 and 5 SiNWs/μm in the vertical and horizontal directions, respectively) when S and T = 100 nm (Figure 3-9). Nonetheless, as we reduce the trench opening and silicon spacer dimensions the fabrication process becomes more sensitive to process variations making it difficult to implement reproducibly into sensor system fabrication flow. Also, it is important to keep in mind that analyte diffusion may be limiting as the space in between the NWs can be significantly reduced with increasing NW density.

Zipping and stiction between the NWs due to the water capillary action during rinsing and drying was expected but not actually experienced in this work. For that reason, in order to dry the structures after the BOE wet etch and rinse, the samples used to be placed in an ethanol or isopropanol (IPA) bath followed by a $CO_2$ supercritical drying step. However, it was soon noted that for the inter-nanowire distances studied here, a simple water rinse and ambient air dry were enough to dry the samples well.

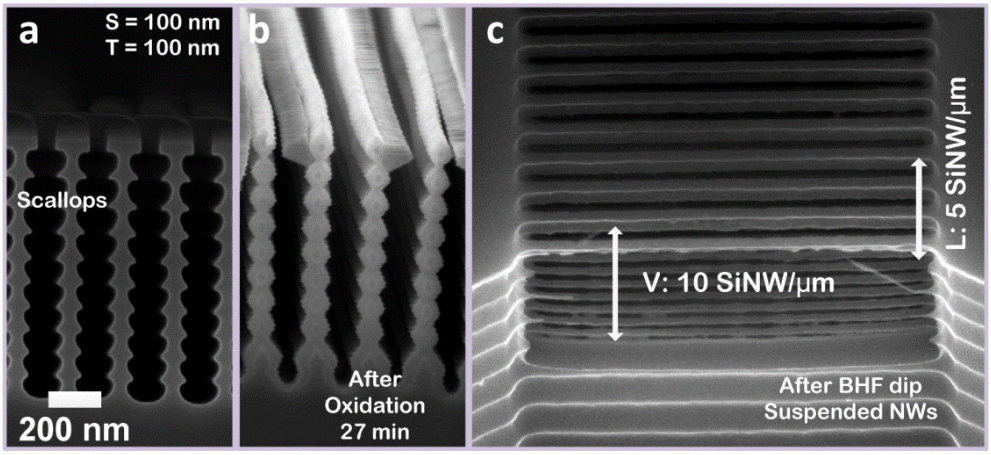



**Figure 3-9:** SEM cross section of highest density structure with T = 100 nm, S = 100 nm, (a) after BOSCH, (b) after thermal oxidation and (c) after BOE etch ($d_{NW}$ ~ 15-25 nm).

Figure 3-10 shows part of our development efforts to reduce NW diameter and to tailor the vertical and lateral NW density by the implementation of different mask dimensions (S and T) and oxidation time (148, 168 and 232 minutes) after the NWs have been released by the BOE wet process.

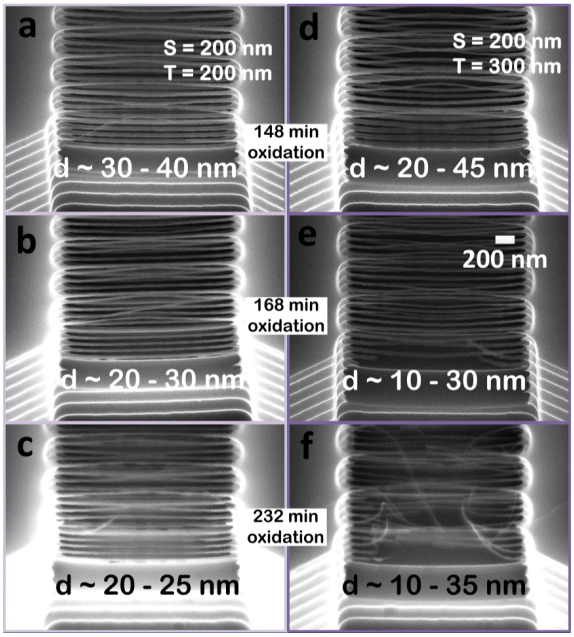



**Figure 3-10:** SEM top-side, tilted-views of SiNWs formed with the same T and S dimensions, S = T = 200 nm (a – c), S = 200 nm, T = 300 nm (d – f) but oxidized with different times.

Structures with channels as long as 5 µm and target diameters below 35 nm can be easily fabricated without significant bending or breaking of the NWs as can be seen in Figure 3-11. Thicker nanowires are possible to be made longer but are of no interest to this work as they have been found to offer lower sensitivities (lower S/V). Very thin NWs (< 15 nm) can be fabricated by thermal limiting oxidation (800 °C) but do not survive after the BOE release step. In this work, the minimum nanowire length is mostly limited by the ion implantation needed to create the deep junction wells in order to be able to contact as many NWs in the vertical direction as possible. This will be shown in Section 3.3.2.

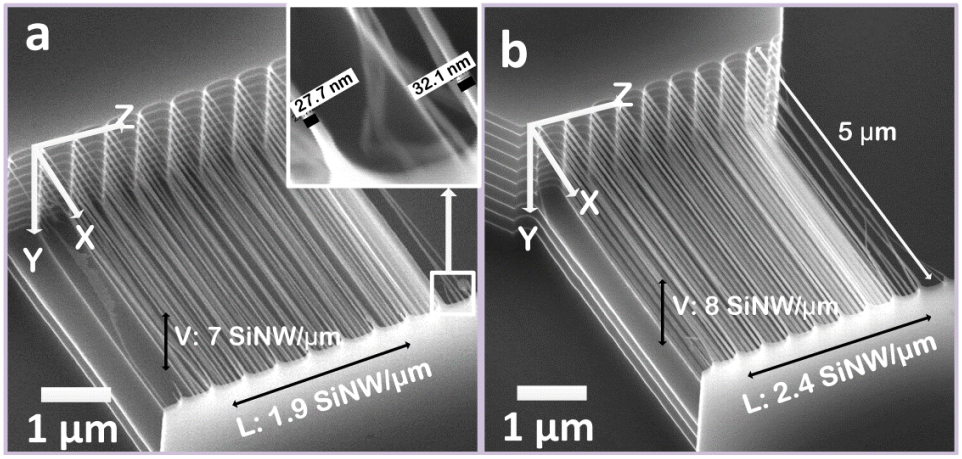



**Figure 3-11:** SEM top-side tilted-views of SiNWs resulting from the BOSCH process with different trench openings and silicon spacer dimensions after thermal oxidation and BOE $SiO_2$ removal for structures with L = 5 µm and: (a) T = 300 nm, S = 200 nm, (b) T = 200 nm, S = 200 nm. High number of channels N in two directions (y, z) can be achieved.

## 3.2 Short-loop process optimization-vertically stacked Fins

Similarly to the short-loop process for SiNWs, an LTO mask is deposited on a test wafer and patterned by an e-beam lithography/RIE step. After the hard mask has been patterned the vertically stacked Fins were produced using two different fabrication routes. The first involved a combination of the BOSCH process to create "vertical" walls (scalloped) and an $SF_6$ isotropic etch in order to separate the different Fins (Figure 3-12) similar to the process that Bopp *et al*. [76] introduced. This method for developing vertically stacked Fins is only suitable for much larger structures nevertheless > 200 nm as the scalloped side walls promote the formation of not only Fins but nan-

owires during thermal oxidation due to the natural variation from top to bottom of the trench induced by the BOSCH process.

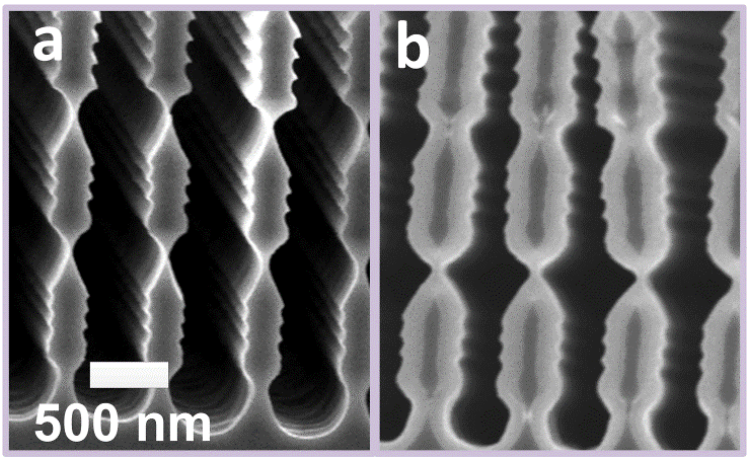



**Figure 3-12:** SEM cross sections of Fins formed with a combination of BOSCH and isotropic dry etches before (a) and after (b) oxidation.

In order to be able to produce thin Fins, an anisotropic silicon etch ($C_4F_8$, $SF_6$ mixed) was then investigated to create straight and smooth vertical sidewalls. The second fabrication method uses a combination of anisotropic ($SF_6$ and $C_4F_8$ mixed to create straight walls) and isotropic $SF_6$ silicon dry etches as well to separate one Fin from the next (Figure 3-13). With this method, only the top Fin has straight sidewalls as the consecutive formation of droplet shaped Fins is instead promoted.

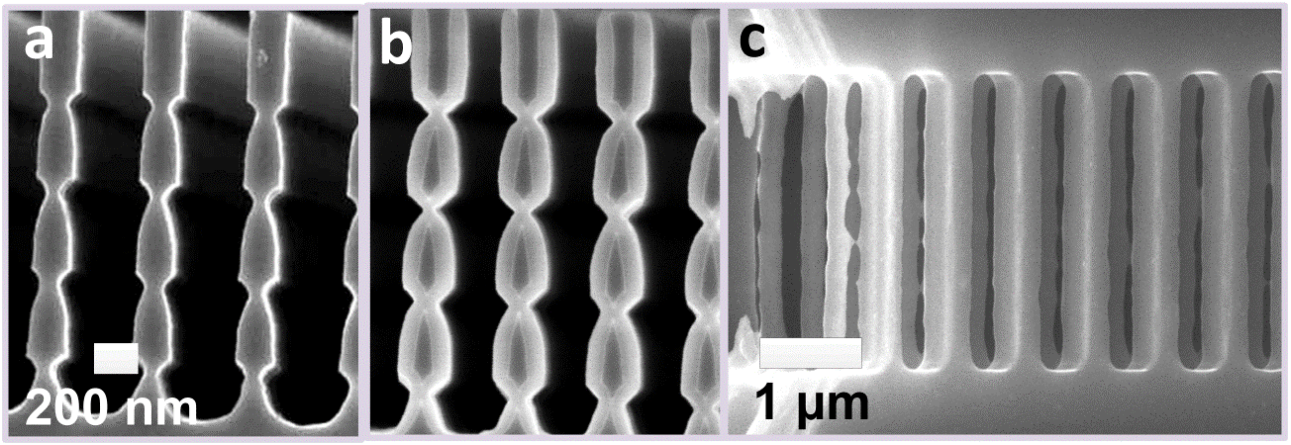



**Figure 3-13:** SEM cross sections of Fins formed with a combination of anisotropic and isotropic (non-sharp scallop) dry etch steps before oxidation (a), after oxidation (b) and top-side view of Fins after BOE release (c).

In a variation of this process route an $O_2$ step was introduced after the $C_4F_8$ passivation before the $SF_6$ isotropic etch to produce rounder separations, straightener walls (Figure 3-14) and reduce the droplet shape appearance of the Fins. It is possible to create structures that are thinner than 150 nm with this process.

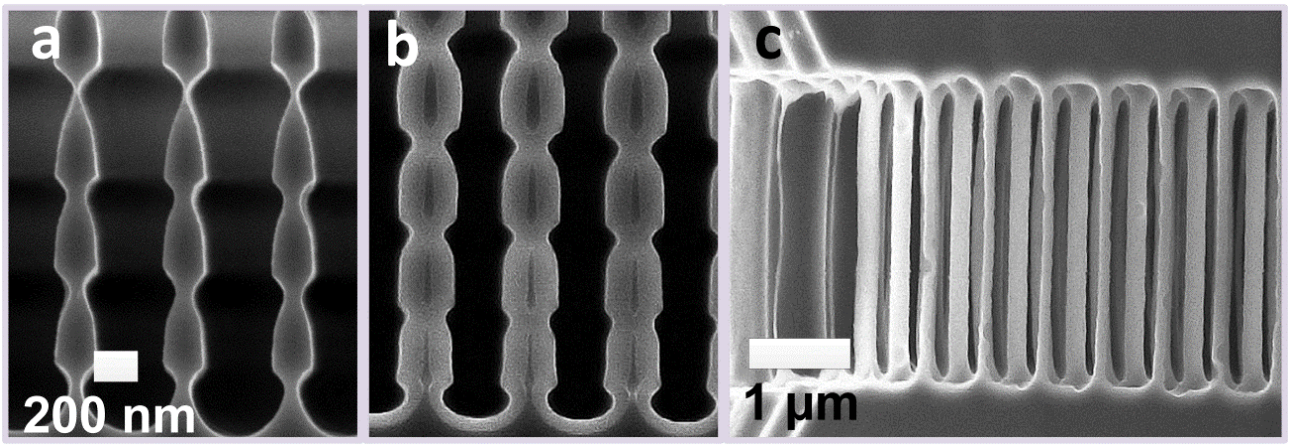



**Figure 3-14:** SEM cross sections of Fins formed with a combination of anisotropic and isotropic (sharp scallop with $O_2$ step included) etches before oxidation (a), after oxidation (b) and top-side view after BOE release (c).

## 3.3 Vertically stacked sensor process flow

In here, only the approach for the fabrication of the vertically stacked SiNW sensor are presented yet it is clear that the same process flow can be used for the Fin-based structures with the correct implementation of the Fin formation part. Due to cost considerations only vertically stacked SiNW-based sensor devices were fabricated.

The process flow consists of 6 different masking levels with 4 of them being e-beam lithography steps. SOI wafers (SOITEC) with a BOX and device layer thickness of 1 µm each (p-type boron, 1 - 10 Ohm · cm) are used as well as test wafers for reference.

With a device layer thickness of 1 µm we can fabricate devices with 7 and 8 NWs vertically stacked (for S = 200 nm, T = 300 nm and S = 200 nm T = 200 nm device structures respectively). Source and drain contact pads are isolated by patterning SU-8 so that only the sensing elements are exposed to

the liquid environment. The device can then be further isolated by a polydimethylsiloxane (PDMS) microfluidic channel though which analytes can make contact with the NW stack.

### 3.3.1 Mask 1: NW formation

In this first masking level a thin layer of LTO is first deposited as a hard mask. ZEP is used to pattern the oxide by e-beam lithography (Figure 3-15) and the vertically stacked nanowires are already formed by first producing scalloped trenches by BOSCH followed by thermal oxidation as previously described in the short-loop process section.

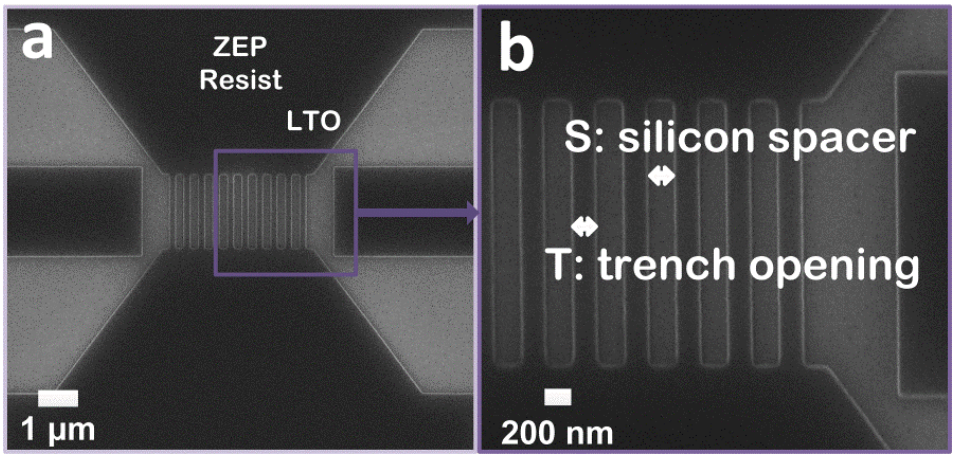



**Figure 3-15:** (a, b) SEM top-view and close-up of pattern after e-beam with silicon spacer and trench openings clearly labeled.

### 3.3.2 Mask 2: Implantation

#### 3.3.2.1 Monte-Carlo simulations

Monte-Carlo (MC) process simulations were first performed with Sentaurus Process 2010.12 [115] in order to determine the required implant dose, ion energy, rapid thermal anneal (RTA) flat times and mask thickness required to contact as many NWs in the vertical direction as possible without significant lateral spread. MC simulations are of particular importance to calculate the dopant redistribution within each of the vertically stacked NWs when NW dimensions are below 60 nm. Analytic implantation models use simple Gaussian functions and are only accurate for the calculation of ion distributions in bulk. MC uses a statistical approach for the calculation of the penetra-

tion of implanted ions into the target and accumulation of crystal damage based on the binary collision approximation (BCA) [115]. Atomistic computer simulations based on BCA have been found to be a precise and efficient tool to calculate the as implanted dopant distributions [116]. A structure resembling a 2D cross section of the vertically stacked structure was built first with Sentaurus Device Editor 2010.12 and then imported into Sentaurus Process to perform the MC implant process simulation. Simulations were carried out for a wafer with a 100 crystal orientation and an initial boron doping concentration of $5 \times 10^{15}$ $cm^{-3}$. They were performed as a function of different implant energies and doses at a 7° tilt angle and 0° rotation. The necessary thickness of the $SiO_2$ mask layer was as well determined by MC simulations. The SiNWs were simulated to be 50 nm in height and 2 μm in length separated by silicon dioxide blocks of 70 nm in height. The mask openings were placed on the sides starting right next to where the NWs begin/end.

### 3.3.2.2 Monte-Carlo simulation results

Figure 3-16 shows the simulated contour plots of the net activated dopant redistribution for different implant doses from $10^{15}$ to $5 \times 10^{16}$ $cm^{-2}$ while we keep the implant energy constant at 320 keV. The RTA temperature (1000 °C), and flat process time (30 seconds) were kept constant. An ion implantation energy of 320 keV, a dose of $10^{16}$ $cm^{-3}$ phosphorous and RTA flat process time of 30 seconds at 1000 °C were found to be appropriate process parameters to form S/D contact wells (up to one micron in depth) for an $N^+$ phosphorous concentration above $10^{17}$ $cm^{-3}$ along the vertical direction connecting each NW. An implant mask of $SiO_2$ with a thickness of 1 μm was determined to be appropriate for the implantation energies needed here. It is clear that the number of NWs that can be vertically stacked is limited by the implantation. Though it is possible to fabricate structures with up to 16 NWs in the vertical direction, a prohibitively expensive high energy and high dose implantation (> 320 keV, > $10^{16}$ $cm^{-3}$) was determined to be needed to connect the vertically stacked NWs beyond this device thickness (for S/D phosphorous concentration levels > $10^{18}$ $cm^{-3}$). Also, higher implantation energies (> 320 keV) require thicker oxide implant mask thicknesses (> 1 μm) limiting the resolution of the *S/D* implant openings. Furthermore, the lateral spread resulting from the high implant energies (up to 0.5 μm here) also limits the use of vertically stacked silicon nanostructures and it limits the NW length (in here to > 1 μm). For these reasons, intermediate NW/Fin sizes between $L = 2 - 20$ μm were targeted for fabrication. The implantation is the main

constraint to the number of NWs that can be vertically stacked not only for sensor structures but principally for their implementation on typical logic FETs where state-of-the-art devices have much shorter NW lengths.

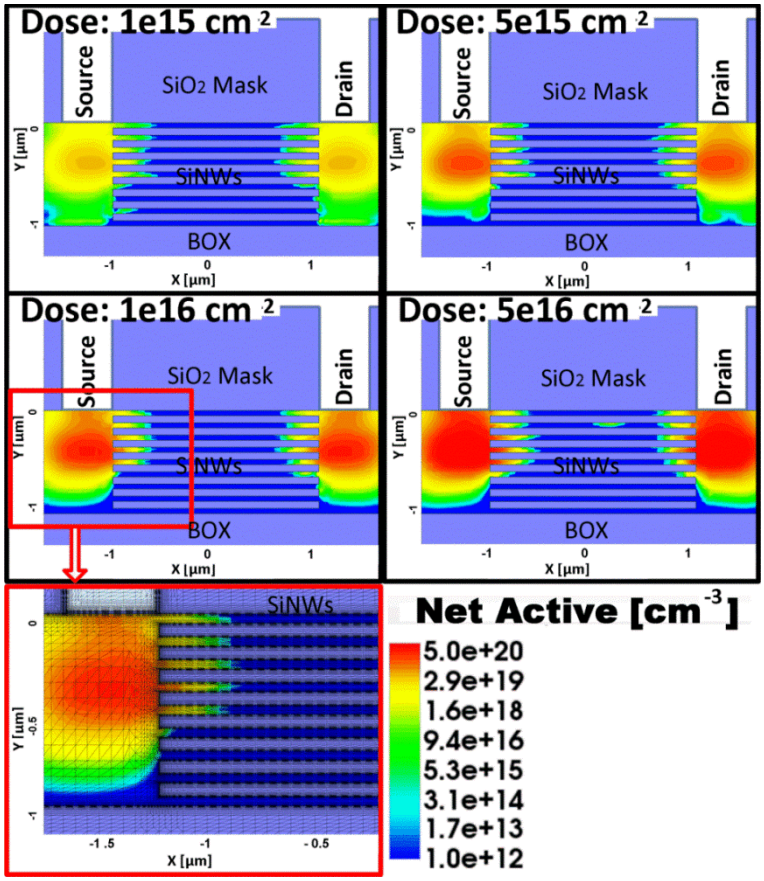



**Figure 3-16:** Contour plots of the net active concentration (B + P) of the simulated vertically stacked NW cross sections with increasing implantation doses from 1e15 to 5e16 $cm^{-2}$ with constant energy (320 keV), RTA temperature (1000 °C) and RTA flat time of 30 seconds. The meshed simulated contour plot of the corresponding simulated structure is also shown.

### 3.3.2.3 Implantation and RTA

The phosphorous ion implantation to introduce impurity atoms into the source and drain regions was performed with the process parameters determined by the MC simulations. In order to accomplish electrical isolation from the bulk-Si, the outline that defines each device was designed to have a width larger than the trench openings used to form the NW precursor scallops by the BOSCH process (T = 300 nm or 200 nm), Figure 3-17a. This guarantees that as the last NW scallop is formed it will touch the SOI BOX so that every device "floats" on top of an insulator $SiO_2$ layer

(1 µm, Figure 3-17b). The side trenches include raised silicon blocks to support the side electrode/s. A thick LTO layer (> 1 µm) is then deposited as a hard mask for ion implantation (Figure 3-17c). Together with the thermally grown oxide enclosing the NWs the LTO serves to protect the structures throughout the rest of the process flow (Figure 3-17d). LTO was chosen as the implant mask material because photoresist could be burnt by the high implantation energies needed to create deep wells necessary to contact many NWs in the vertical direction (1 µm). Also because the source and drain areas for ion implantation had to be defined by e-beam lithography due to alignment requirement limitations at the CMi. Thick resist layers are also incompatible with e-beam lithography due to electron depth penetration restrictions. An anisotropic dry etch process defines the S/D areas in the LTO mask. RTA is then performed for ion activation (1000° C, 30 s). The implantation has been performed outside of EPFL by Ion Beam Services (IBS) in Peynier, France and the RTA was performed at the Laboratory for Analysis and Architecture of Systems (LAAS) in Toulouse France.

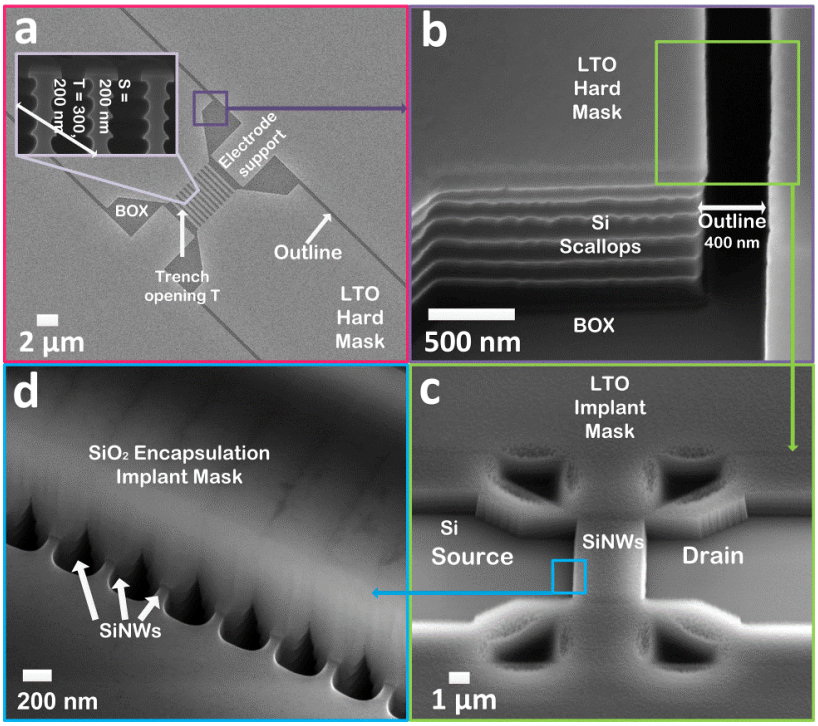



**Figure 3-17:** (a) Top-side view of etched structure's outline, inset shows the scallops produced by BOSCH (S = 200 nm and T = 200 or 300 nm), (b) tilted-side view of scalloped outline right on top the SOI's BOX layer, (c) tilted-side view of structure after LTO hard mask is deposited and S/D openings are etched for implantation.

### 3.3.3 Mask 3 and 4: Side-gate and S/D contact metallization

Metallization was divided into two different masking steps. Electron-beam lithography was necessary to meet the alignment requirements for patterning the Pt side-gates on top of the raised support blocks. Optical lithography was needed to create thick contact layers for the S/D pads.

The side-gate areas are defined by e-beam lithography of a methyl methacrylate + poly methyl methacrylate (MMA/PMMA) bilayer. Ti/Pt (20, 150 nm respectively) is then deposited by e-beam evaporation in a Leybold-Optics Lab 600H evaporator. Pt was chosen as it has been found to be a stable electrode material, resistant towards BOE and biocompatible (non-toxic). The metal will be exposed to BOE when releasing the NWs from their silicon dioxide encapsulation. Also this side electrode/s will be in contact to the electrolyte solution during sensing experiments.

The source and drain contacts are defined in a second lift-off process by optical lithography with a bilayer of lift-off-resist (LOR) and AZ1512HS positive tone resist and e-beam evaporation of Ti/Al/Pt (20 nm, 1.1 μm, 10 nm respectively). The annealing process to create ohmic contacts was performed for 25 minutes at 425 °C in a $H_2/N_2$ atmosphere. Figure 3-18 shows the structures after metallization.

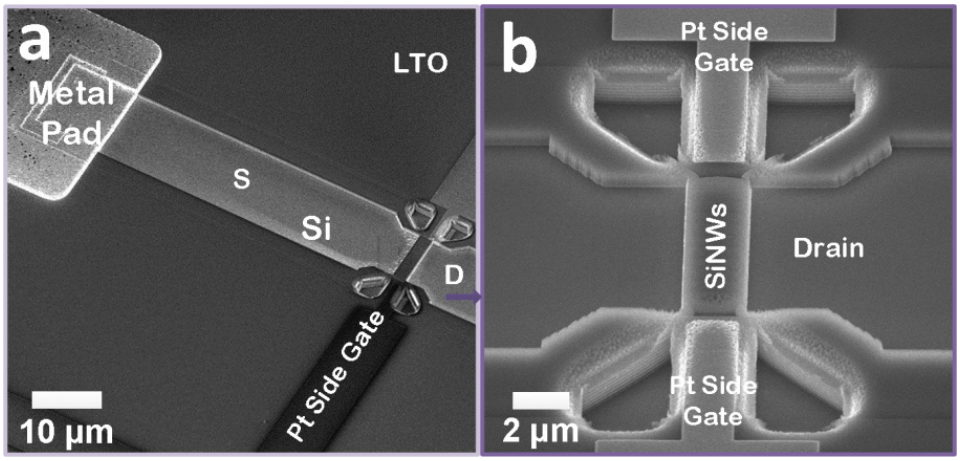



**Figure 3-18:** (a) SEM tilted-view after metallization of contact pads by lift-off and (b) magnified view of side-gated device.

### 3.3.4 Mask 5: SU-8 protection mask

In this masking level the isolation of the sensor structure is achieved by the optical lithography patterning of SU-8 (2 – 3 μm thick). SU-8 is a negative tone epoxy based resist that has been found to be chemically and thermally resistant [117]. It is stable up to its decomposition temperature (380 °C). This is important as the subsequent dielectric deposition happens at 200 °C. The entire wafer/chip is covered with an SU-8 epoxy layer except for small windows (30 × 30 μm$^2$) where the NWs will have contact with the sensing or gating liquid (Figure 3-19). The side-gates are also left partially unexposed in order to make contact with the sensing liquid environment and establish a liquid potential.

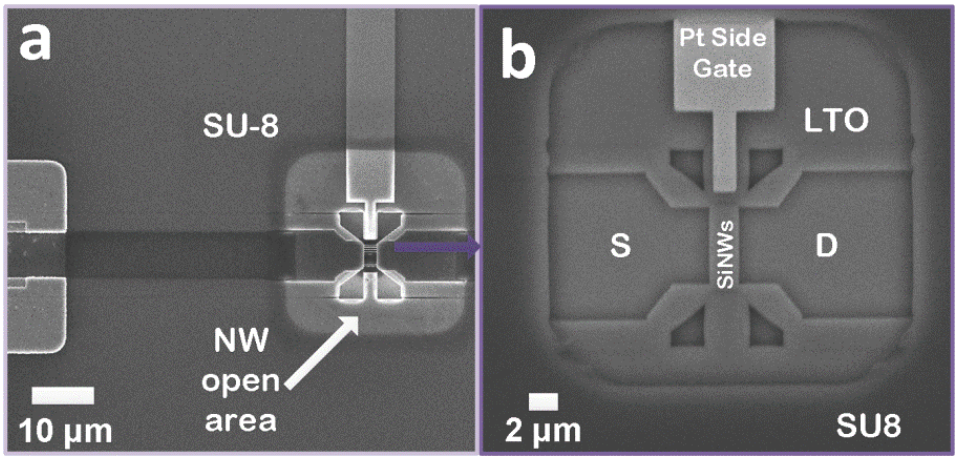



**Figure 3-19:** (a) SEM top-side and (b) magnified views after SU-8 definition by optical lithography. Only the NW/Fin area is exposed.

The contact pad areas (100 × 100 μm$^2$) located on either side of the chip and 1 mm away from the sensing window are also left open. Wire bonding to a printed circuit board (PCB) or direct electrical probing can then be easily accomplished. The chip layout allows for enough space for a microfluidic channel to be directly bonded to the top of the structures. A droplet can also be simply placed on top of the NW window to allow for liquid gating and quick electrical characterization as done here to be shown in Chapter 5.

### 3.3.5 Mask 6: NW release

In this masking level, a last e-beam lithography step is necessary to define a small area in ZEP resist (700 nm) where the NWs are located. ZEP is resistant against BOE. This allows to selectively remove $SiO_2$ surrounding the NWs alone and avoid over etching neighboring areas. The same window can also be used to selectively deposit metal nanoparticles around the NWs alone. Gold surface coverage is for example necessary for Thiol surface treatment for certain DNA functionalizations. The ZEP resist can be easily removed in an oxygen plasma.

Since protons can penetrate the Si-oxide layers leading to a large leakage current a thin alumina or another dielectric surface layer can then be deposited on top of the whole structure in order to efficiently suppress the leakage current. The whole structure can then be covered with a dielectric ($Al_2O_3$ or $HfO_2$, 5-12 nm) by atomic layer deposition.

## 3.4 Analyte delivery

Microfluidic channels (150 μm wide) are fabricated within a solid PDMS (elastomeric material) stamp that can be subsequently bonded to the device chip for direct analyte delivery to the SiNW sensor array.

The layout consists of two parallel lines of devices as can be seen in Figure 3-20a. The small channel dimensions minimize the exposure of the rest of the wafer to the testing solution with only small (μL) sample volumes required for analysis. PDMS stamps can be molded from a SU-8 master (Figure 3-20b) fabricated by conventional optical lithography methods [118] and then be attached using a "stamp-and-stick" technique which utilizes liquid uncured PDMS as an adhesive [119]. Incubation at 60 °C for two hours cures the PDMS and completes the adhesion. This bonding technique gives a strong but non-permanent bond and does not require any pre-treatment of the sensor device. This is particularly important as it may be necessary to perform to surface functionalize the device prior to stamp bonding. In order to ensure perfect alignment of the microfluidic channel with the sensors a micrometer controlled x-y-z stage was used to place the microfluidics onto the sample chip (Figure 3-20c).

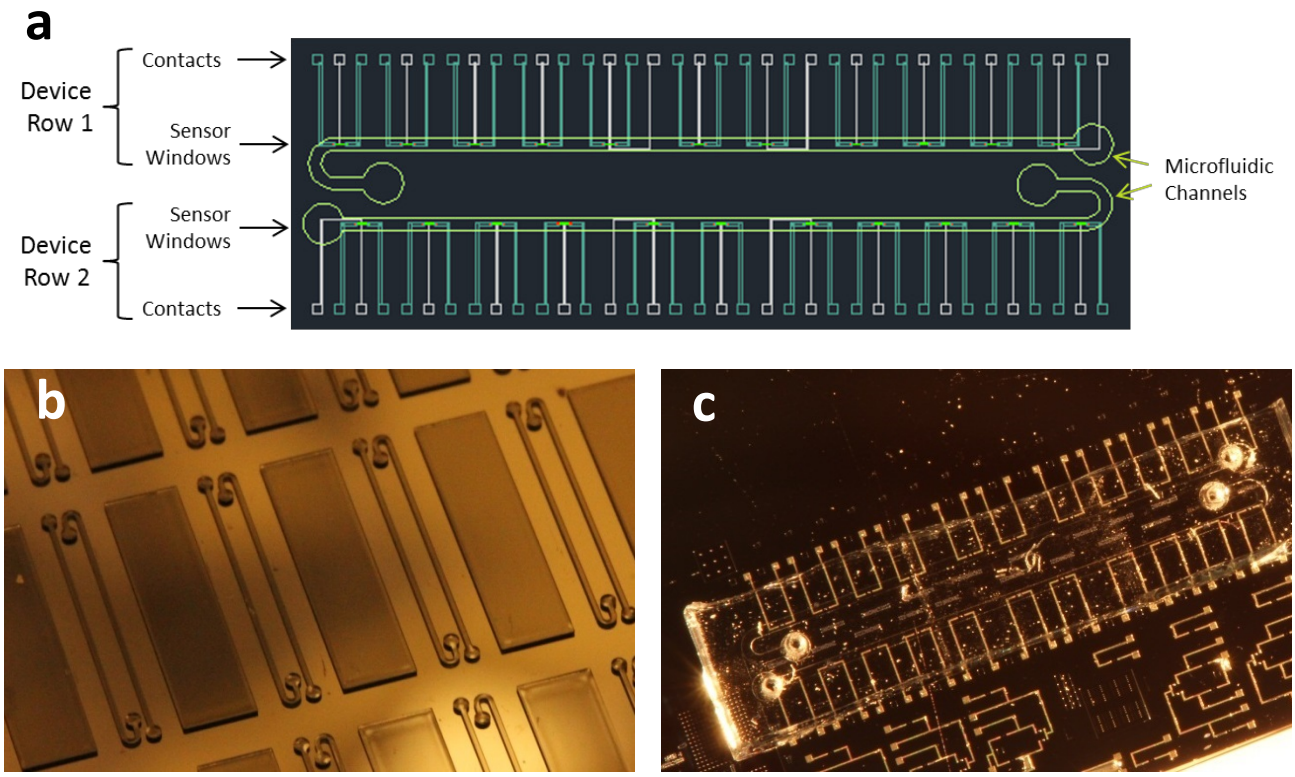



**Figure 3-20:** Schematic showing layout of devices and the microfluidic channel geometry used to supply the sensors with fluid (a), SU-8 mold and (c) PDMS microfluidic stamp on top of chip. Courtesy of A. M. Nightingale, Imperial College London.

Access holes with diameters ~ 400 μm are drilled on the top and sides of the stamp to link the channel to external tubing. The inlet/outlets of the microfluidic stamp can be connected to lengths of polytetrafluoroethylene (PTFE) tubing which fits snugly into the pre-drilled access holes at the end of each channel so that fluid could be administered and collected from the outside of the probe station.

The PDMS substrate provides enough interfacial area to allow strong bonding between the device and substrate but is narrow enough to still allow access to the device contacts. Once administered, fluid is contained within the channels which are aligned over the sensor windows. In this fashion it is therefore possible to controllably deliver liquid analyte to the sensor area while protecting the rest of the device architecture from exposure.

Figure 3-21 shows the final vertically stacked nanowire structure from a close-up to the SiNWs (a - c) to the global view of the resulting integrated devices (f). Contact access is possible on the outer sides of the chip (Figure 3-21d). Access to the sensor structures is possible through small windows on the SU-8 isolation layer at the center of each sensor (Figure 3-21e). Figure 3-21f shows the PDMS substrate sitting on top of the device substrate.

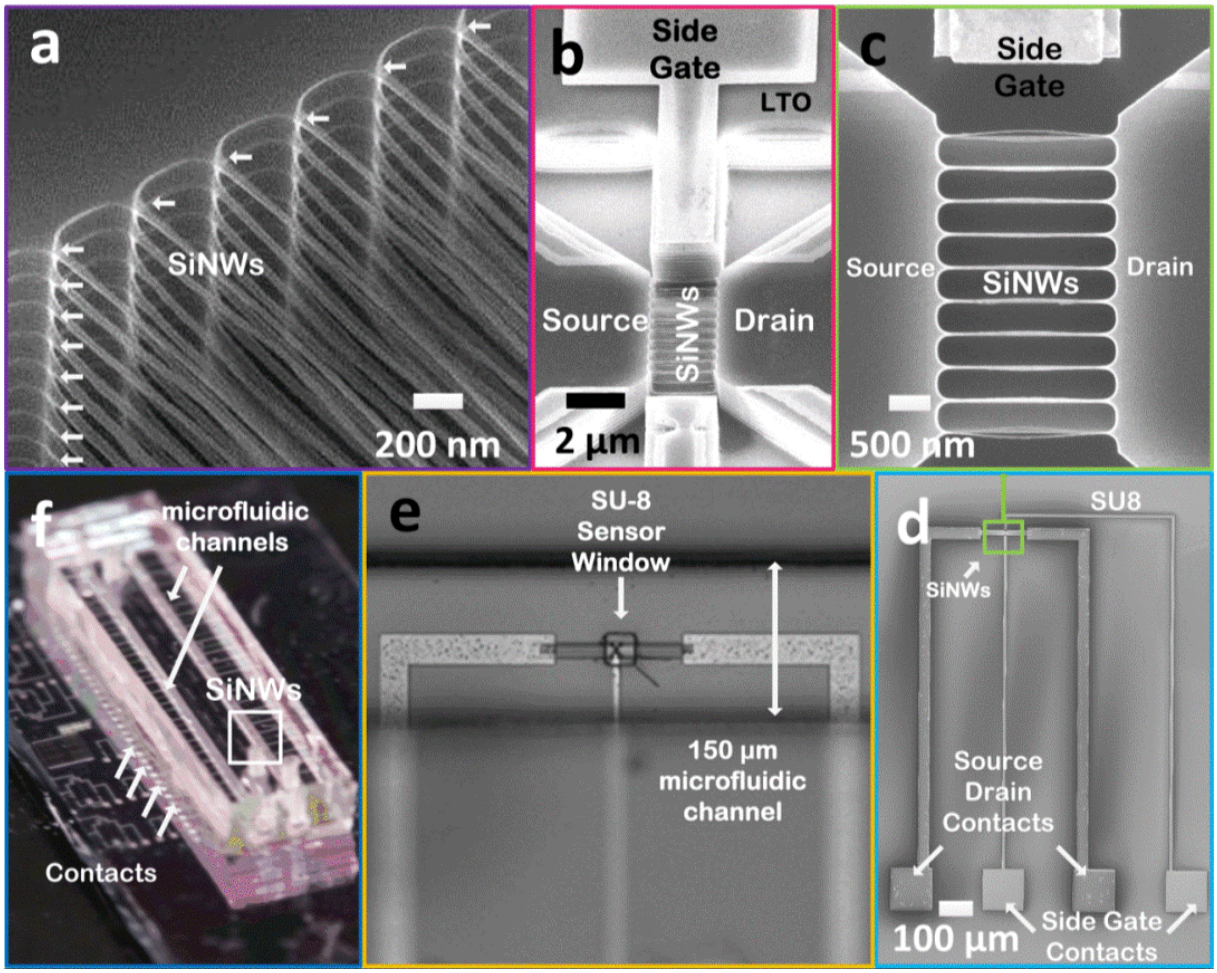



**Figure 3-21:** (a) SEM tilted-view of SiNWs, (b) SEM top-side tilted-view showing side-gate from side and (c) top-view, (d) SEM top-side view of entire structure that shows source/drain and side-gate contacts. (e) Image showing top-view of PDMS stamp containing 150 µm-wide microfluidic channel on top of SU-8 sensor window, (f).

## 3.5 Heterogeneous system integration

A smart fabrication approach and design is necessary to achieve a 3D FET sensor consisting of particularly thin and suspended channels to be integrated into a 3D heterogeneous system. The different components of this system can be connected by directly stacking them with integrated through silicon vias. The fabrication approach previously introduced takes advantage of the natural scalloping effect created in silicon by the CMOS compatible BOSCH process in combination with thermal oxidation to create a highly reproducible 3D SiNW structure. The SiNWs are furthermore safely enclosed within an LTO/$SiO_2$ enclosure throughout the fabrication process and if necessary throughout the TSV implementation.

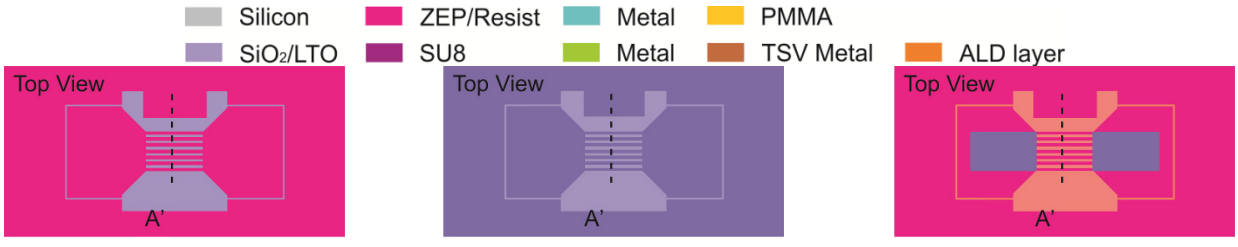
### 3.5.1 Process flow with TSV integration

There are several approaches for the fabrication of TSVs [120]. The TSV-first approach (from the front side of the wafer) has a limited thermal budget if Cu for example is to be used (Cu melting point: 1084 °C). Thermal oxidation and rapid thermal anneal after implantation (>1000 °C) are indispensable steps in our fabrication process and therefore the TSV first approach with Cu is incompatible with the current process flow. Because the sensor will need to be exposed to the environment or to a microfluidic device the processing of the TSV from the wafer's back to front side is more appropriate. The vias can then be fabricated almost at the end of the current process flow, after the SU-8 patterning.

The main steps in the proposed process flow with TSV integration are presented in Table 3-1 and shown schematically in Figure 3-22 in the next pages. The regular flow steps and TSV steps are clearly marked. The SiNWs are safely enclosed within an LTO/$SiO_2$ enclosure offering a higher degree of flexibility.

**Table 3-1:** Short description of process steps for 3D integration.

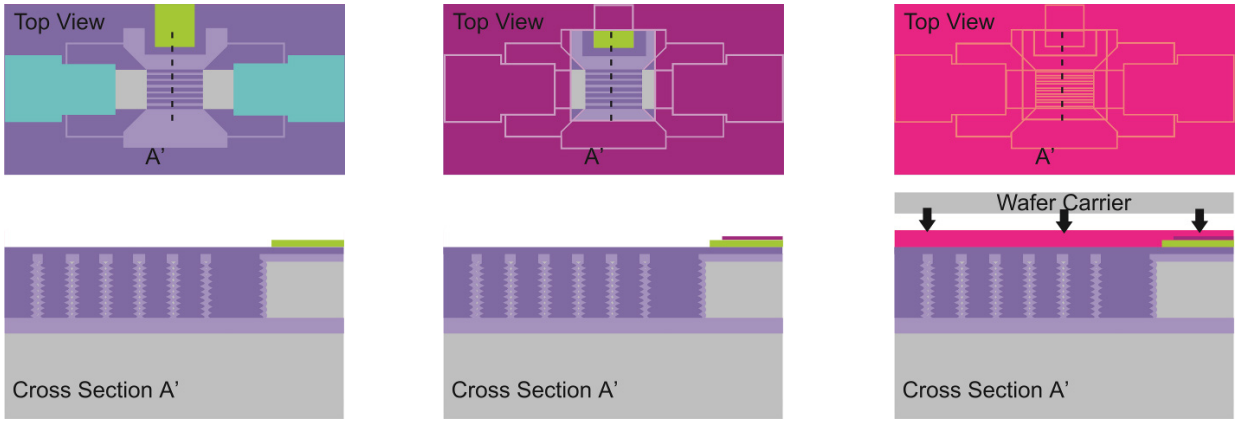
| Step | Process |
|---|---|
| **Mask 1** | NW formation: Hard mask patterning by e-beam lithography and dry etch, scallops produced by BOSCH, NW formation by thermal oxidation, LTO implant hard mask deposition. |
| **Mask 2** | Implantation: S/D areas defined by e-beam lithography and dry etching, Ion implantation at 320 keV, $10^{16}$ $cm^{-3}$ phosphorous and RTA 30 s at 1000 °C. |
| **Mask 3, 4** | Metallization: TiPt side-gate patterning by lift-off using e-beam lithography, TiAl S/D metallization by lift-off and optical lithography. |
| **Mask 5** | SU-8 isolation: Optical lithography patterning of SU-8, S/D contact and NW areas left open. |
| **TSV1** | Carrier wafer bonding: "Sensor wafer" flipped and glued temporarily with PMMA to carrier wafer, TSVs to be fabricated from back to front side of sensor wafer. |
| **TSV2** | Wafer thinning: Grinding to thin down wafer (50-100 µm). |
| **TSV3** | TSV formation: TSV openings by BOSCH, isolation layer deposition (LTO or α-Si) by low temp plasma process, seed layer (for metallization) deposition by sputtering or CVD (chemical vapor deposition), electroplating of vias. |
| **TSV4** | Carrier wafer removal: "Sensor wafer" bonded to second carrier wafer from back, first carrier wafer and PMMA removal from front. |
| **Mask 6** | NW release: Small area around NWs is patterned by e-beam, ZEP resist protects wafer, BOE $SiO_2$ etch to release NWs, conformal deposition of a gate dielectric ($Al_2O_3$, $HfO_2$) possible by ALD. Microfluidic stamps made of PDMS can be easily attached by "stamp-and-stick" method. |




***Mask 1:*** *Scalloped structure after BOSCH.*

***Mask 1:*** *NW formation by oxidation and LTO deposition (implant hard mask).*

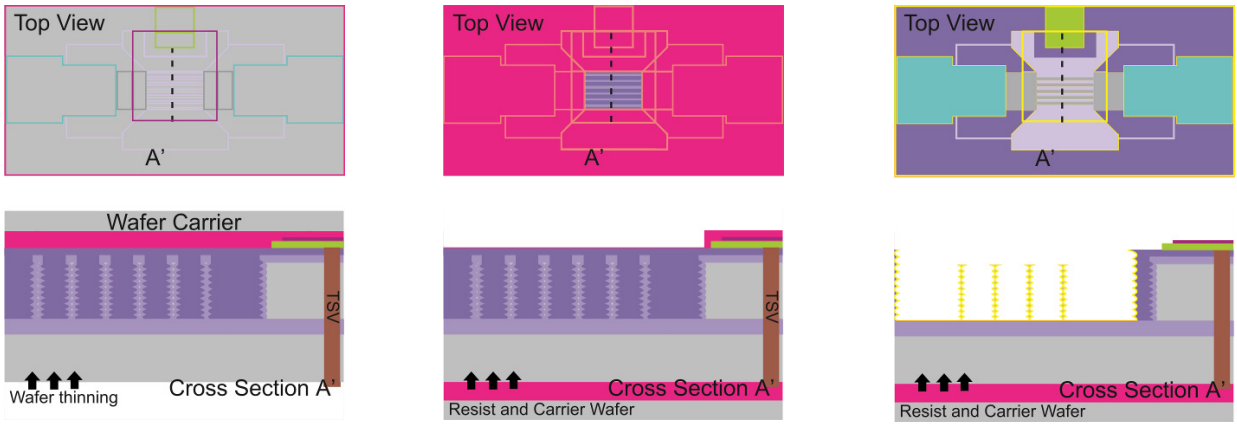
***Mask 2:*** *S/D hard mask patterning by e-beam and dry etch.*




***Mask 3, 4:*** *Side-gate and S/D contact metallization by lift-off.*

***Mask 5:*** *SU8 isolation by optical lithography.*

***TSV1:*** *wafer flipped and glued temporarily with PMMA to carrier wafer.*




***TSV2, 3:*** *wafer thinning, isolation and TSV metallization by electroplating.*

***TSV4:*** *wafer bonded to other carrier from top, PMMA removal.*

***Mask 6:*** *small ZEP window patterning by e-beam around NWs.*

***Mask 6:*** *NW release, ALD deposition of gate dielectric.*

**Figure 3-22:** Top and cross section schematic views of structure after specified process steps with TSV integration.

The wafer can be flipped and glued temporarily to a carrier in order to be thinned down by grinding Figure 3-23. A resist such as PMMA is sufficient to bond the wafer to a carrier. After wafer thinning the TSV openings can be made by a BOSCH process (50-100 μm). A passivation and isolation layer then needs to be deposited with a low temperature plasma process. Typical passivation and isolation layers include polysilicon or amorphous silicon (*α-Si*) and a low thermal oxide respectively. Temperatures greater than 200 °C are not recommended if PMMA is to be used as a bonding material. A seed metal layer needs to be first deposited by sputtering or a chemical vapor deposition (CVD) method. The main metal conductor can then be deposited by electroplating to achieve high aspect ratios. After TSV processing, the wafer can then be flipped again and bonded to a carrier wafer from the backside and the rest of the process flow can be continued as usual.

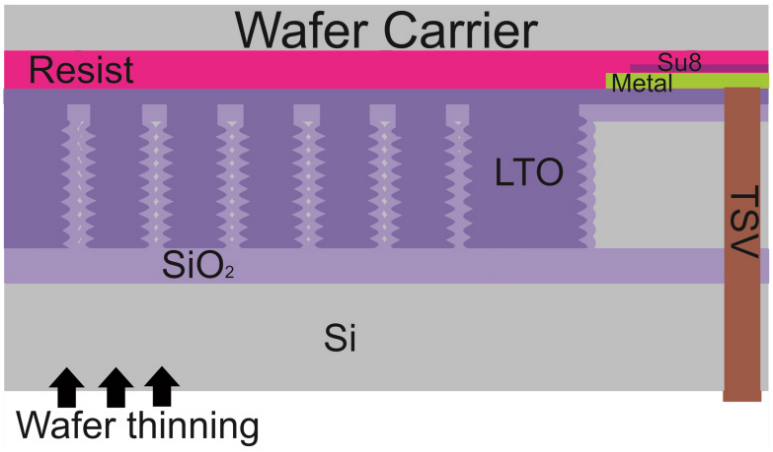



**Figure 3-23:** Cross section schematic view of structure with TSV. NWs are safely enclosed within the $SiO_2$ and LTO making TSV fabrication possible.

## 3.6 Fabrication challenges

### 3.6.1 Fabrication of 3D structures and yield

An important point to keep in mind for the technology presented here is that any process variation or inherent process non-uniformity is furthermore exacerbated as the wafer moves along from the e-beam mask patterning step to the mask etch to the scallop formation by BOSCH and finally to the SiNW formation step by thermal oxidation. The process flow as a whole has to be developed to

withstand a certain degree of non-uniformity. Otherwise the technologist risks ending up with fully consumed structures of simply scalloped walls as the NWs are released from their $SiO_2$ encapsulation until the end of the process, leaving the process engineer no options for addressing the issue. In order to prevent this, the trench opening and silicon spacer dimension combinations need to be specified to allow for these potentially big variations in process conditions that are later highlighted to achieve relatively thin SiNW structures < 35 nm. In here, the intermediate dimensions studied S = T = 200 nm and S = 200 nm, T = 300 nm afforded us that flexibility. Nonetheless, variation in NW thickness (die-to-die) does occur (*e.g.*, 15 – 30 nm, for S = 200 nm and T = 300 nm). Such variation would pose a problem for junctionless based FET sensors for example for which the subthreshold slope and threshold voltage values are known to change as a function on NW dimensions [52]. From TCAD simulations (presented in Appendix A) for enhancement mode devices, for the targeted NW widths < 35 nm we know that for low doped devices small changes in fin height and width do result in significant changes of the transistor characteristics (subthreshold slope, $I_{on}$, $I_{off}$, $V_{th}$, *etc.*) allowing a certain amount of tolerance at least from the transistor device performance point of view.

Seven random dies from two SOI (with 7 or 8 NWs vertically stacked respectively) wafers were picked to be monitored from start to finish during the fabrication process. Prior to oxide removal the yield (percentage of working devices) for both SOI wafers was found to be > 90% (from $I_d - V_d$ and $I_d - V_{BG}$ measurements). It is worth mentioning nevertheless that only a couple of dies had non-functional devices and yields < 100%. For these dies metallization was incomplete or broken due to adhesion and uniformity problems during the lift-off process at the edges of the wafer. This can easily be resolved in an industrial setting where process control can be monitored more tightly.

After oxide removal 6 random dies on each wafer were selected for SEM inspection. In particular it was important to determine the percentage of devices that had broken NWs and to what extent. A few broken NWs per array should not affect the overall transistor performance (only the output current) of the device. For the first SOI wafer (with 7 NWs vertically stacked) over 94% (34 total devices on each die) of the devices were found to have more than 80% of unbroken SiNWs. For the second SOI wafer (with 8 NWs vertically stacked, 28 total devices on each die) this decreases to less than 60%. For the most part both wafers were processed together or around the same time

frame with the exception of the BOSCH process (number of vertically stacked NWs dependent on # of BOSCH cycles), oxidation, and source and drain contact metallization. Nonetheless the breaking point for the second SOI wafer seems to originate where the LTO implantation mask has been misaligned the most. Though both wafers were supposed to be processed with the same implantation parameters, the process was performed externally and no information was possible to be obtained. It is also possible that during the dry etch (single wafer process) to pattern the implant mask the LTO was also ruined. In any case, the implantation step/dry etch LTO mask patterning were suspect due to the fact that two other wafers were fabricated and implanted allegedly under the same process conditions did not present this kind of damage.

The most important example that showcases the robustness of the sensor structure is the European project collaboration that happened between the e-BRAINS and SiNAPS consortiums. As the Nanolab lacked the capability of doing liquid based sensing experiments it needed to cooperate with other partners. In order to characterize the sensor structures for their sensing capabilities the devices were shipped from EPFL where they were fabricated to Tyndall for surface modification and from there on to Imperial, where fluid delivery stamps were attached. These samples were then brought back over to Tyndall or EPFL (borrowing pumps and other material from Imperial and Tyndall) where the sensing experiments actually took place. All throughout the shipping and handling the structures survived without a problem (by SEM inspection).

## 3.6.2 Mechanical characterization by AFM

Atomic force microscopy was also used as a tool for investigating the mechanical properties of 3D test structures containing stacks of SiNWs. AFM was used as a tool to determine under which circumstances the SiNWs break as a result of the horizontal raking movement of the tip. The NWs may be stressed not only during the fabrication process but during biomolecule functionalization for sensing as previously mentioned and therefore the characterization and determination of mechanical strength and robustness is of particular importance. The tests were done in cooperation with the Institute of Electron Technology (ITE) in Warsaw, Poland [121].

The general idea of the AFM based tests performed here is presented in Figure 3-24. The test structures utilized here consist of 7 × 10 or 7 × 20 SiNWs arrays with lengths $L$ = 2, 3 and 4 μm, Figure

3-24a. A Veeco Nanoman microscope with a NanoScope V controller was used for the experiments. Veeco/Bruker MPP21220 probes (Figure 3-24c) were used for the raking experiments (nominal length × width × thickness: 450 μm, 50 μm, 1.5 μm, nominal tip height 10 - 15 μm, measured spring constant $k_{MPP}$ = 0.8 $Nm^{-1}$), while a Nanosensors ATEC-CONT probe with a visible Concorde-nose like tip was used for the SiNW spring constant estimation (measured spring constant $k_{ATEC}$ = 0.21 $Nm^{-1}$). During the breaking tests the AFM microscope was operated in contact mode while the position of the tip was controlled using offset values, providing precise X-Y positioning with sub-micrometer resolution. One single movement through three consecutive structures (Figure 3-24b) of 90 μm was made along the line perpendicular to the nanowires with a speed of 50 μm/s.

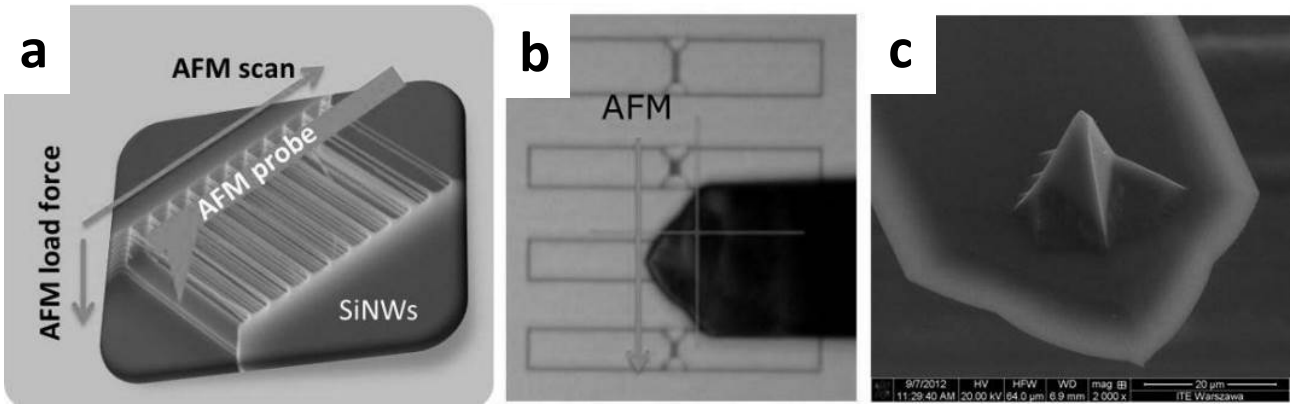



**Figure 3-24:** (a) AFM-based testing methodology, (b) view during the AFM test, (c) SEM images of the one of the AFM probes used– Bruker MPP31220. Adapted from [121].

AFM measurements were performed with vertical load forces varying from 20 nN to 100 nN on stand-alone SiNW test structures with a native oxide (O – sample) surface ($d_{NW}$ ~ 25 - 40 nm, $L$ = 2, 3 and 4 μm) and on structures subsequently covered with 10 nm of atomic layer deposition alumina $Al_2O_3$ (A – sample). Selected SEM images of the vertically stacked SiNWs structures before and after AFM probing are presented in Figure 3-25.

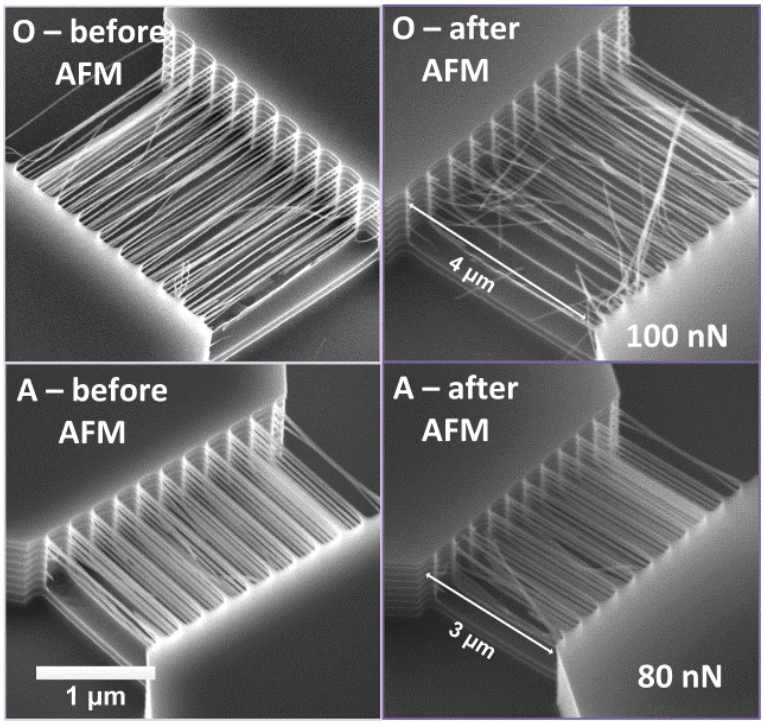



**Figure 3-25:** SEM top-side tilted images of test structures with native oxide alone (L = 4 µm) and with an ALD $Al_2O_3$ layer (L = 3 µm) before and after AFM with a load force of 100 and 80 nN respectively. Courtesy of T. Bieniek, ITE.

The results are summarized in Table 3-2. It is clear from the table that SiNWs covered by ALD alumina (10 nm) are much stronger than those left bare (with a native oxide/$SiO_2$ dielectric). Even at 100 nN of applied force long wires ($L$ = 4 µm) do not break.

**Table 3-2:** AFM results as the tip is raked against 7 × 10 SiNWs structures with increasing lengths $L$ = 2, 3, 4 µm with different load forces (20 – 100 nN). Courtesy of T. Bieniek, ITE.

| AFM applied force | 20 nN | | | 40 nN | | | 60 nN | | | 80 nN | | | 100 nN | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NW lenght | A | B | C | A | B | C | A | B | C | A | B | C | A | B | C |
| | 2um | 3um | 4um | 2um | 3um | 4um | 2um | 3um | 4um | 2um | 3um | 4um | 2um | 3um | 4um |
| Sample O - normal | | | | | | | | | | | | | | | |
| Sample A - Al. (10nm) | | | | | | | | | | | | | | | |

| | |
|---|---|
| | NW's survive |
| | NW's partially survive |
| | NW's not survive |

The lateral deflection signal was also recorded during the scan (Figure 3-26). The spring constant was estimated from force spectroscopy curves (cantilever deflection *vs.* scanner extension, Figure 3-27). For this calculation the deflection of the cantilever is measured before the SiNW is broken due to excessive pushing by the tip.

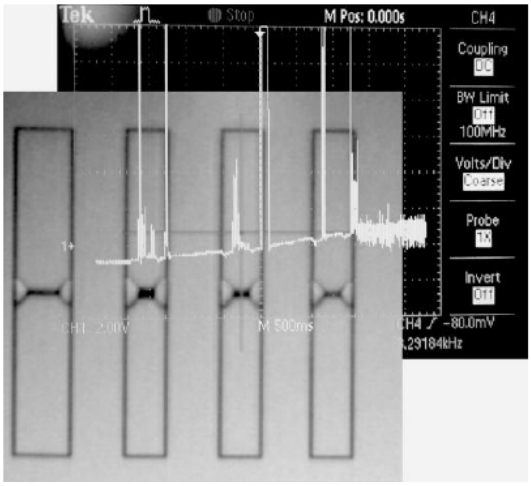



**Figure 3-26:** Lateral signal recorded compared with an optical image of the structures. There is a rise in the signal when the tip strikes the wires. Adapted from [121].

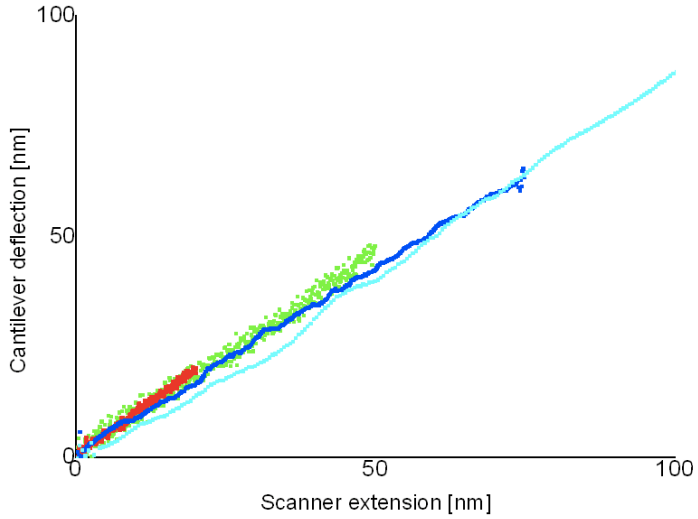



**Figure 3-27:** Force microscopy curves for 7 × 10 SiNWs structures $L$ = 2 µm. Adapted from [121].

A spring constant of 1.25 N/m was estimated for a single alumina coated SiNW of length of $L$ = 2 μm from the measured force spectroscopy curve. The measurement is performed before the nanowire is broken due to excessive deflection induced by the cantilever tip. Assuming that the SiNW can be treated as a double-clamped beam with a 45° rotated square cross-section the spring constant was calculated by $k_{SiNW} = 16Ea^4L^{-3} \sim 1.12$ Nm$^{-1}$ (side of square $a$ = 40 nm and using the Young modulus for bulk-Si <100>, $E$ = 180 GPa [122]). This value is in good agreement with the measured spring constant.

## 3.7 Summary

A fully CMOS compatible, top-down fabrication process for the effective implementation of a robust, high density SiNW vertically stacked field effect transistor structure for biosensing applications was successfully developed. A smart fabrication approach and design is of necessity to achieve a 3D FET sensor that consists of many thin and suspended channels with the potential to be integrated into a 3D heterogeneous system. The different components of this system can potentially be connected by the use of through silicon vias for example, and therefore the process flow as a whole was devised with such an implementation in mind. The main contributions of this work are summarized as follows:

- Through the careful design of the trench opening and silicon spacer width dimensions of the mask (2D) that defines the final dimensions of the 3D structure and the optimization of the BOSCH process, it was possible to create round and short scallops that promote the formation of SiNWs in arrays that are uniformly distributed and where the nanostructures not vary significantly in size from top to bottom of the trench.

- High density arrays of nanowires with a vertical density of 6.25, 7, 8 and 10 SiNWs/μm and a lateral density of 1.35, 1.6, 1.9, 2.4 and 5 SiNWs/μm, respectively, have been effectively released. Up to 16 NWs were possible to be stacked in the vertical direction.

- The FET arrays fabricated here have ultra-thin ($d_{NW}$ < 35 nm), suspended and long (< 10 μm) SiNWs for maximum sensitivities (high $S/V$ ratios).

- It was determined that the main limitation to the number of NWs that can be stacked in the vertical direction is the ion implantation to produce highly doped junctions. A prohibitively expensive high energy and high dose implantation (> 320 keV, > $10^{16}$ $cm^{-3}$) was determined to be needed to connect the NWs in the vertical direction beyond a one micron device thickness.

- In here, the mask layout was designed so that the nanostructures can be semi-embedded into the silicon but completely isolated from each other with side cavities to avoid high topography problems yet allow sufficient room for biomolecule diffusion. This configuration allows for better bonding with the microfluidic channel/system. The small microfluidic channel dimensions can furthermore minimize the exposure of the rest of the wafer to the testing solution.

- The process flow as a whole was successfully developed to withstand a certain degree of non-uniformity. The SiNWs are moreover safely enclosed within an LTO/$SiO_2$ enclosure throughout the process flow and if necessary throughout the possibly harsh TSV implementation. High yields can be achieved and greatly robust vertically stacked structures can be produced with such process. Prior to oxide removal the yield was found to be ~ 90%.

- Finally, atomic force microscopy was also used as a tool for investigating the mechanical properties of 3D test structures containing stacks of SiNWs. Nanowires covered by ALD alumina (10 nm) were found to be particularly strong. Even long wires (with $L$ = 4 μm) do not break when forces as large as 100 nN are applied in a racking movement of the AFM tip. The alumina covered wires ($L$ = 2 μm) were found to have a spring constant of 1.25 N/m.

# Chapter 4 Methods and functionalization challenges

This chapter first describes the methods and experimental set-up used to characterize the vertically stacked structures electrically. The sensing performance characterization details are as well explained in the first part of this chapter and should help the reader understand the experimental results relating to other parts of the thesis. The second part of this chapter, describes the different surface functionalization methods investigated. Furthermore, some of the challenges and lessons learned during the development of two different oligonucleotide immobilization protocols (amino or thiol-based) are finally presented.

## 4.1 Electrical characterization

### 4.1.1 Transistor characterization under dry, ambient conditions

The transistor characterization results described in Section 5.2 of this thesis were obtained in ambient conditions at room temperature with a PMC probing system and a HP 4156C semiconductor parameter analyzer at EPFL. The structures were characterized electrically in dry conditions when completely surrounded by a thick oxide layer (prior to oxide removal by BOE) and then after release ($SiO_2$ removal by BOE). The light was switched off.

### 4.1.2 Transistor characterization in wet, ambient conditions

The liquid-gated static measurements results described in Section 5.4 of this thesis were obtained under ambient conditions at room temperature using a Microtech Cascade probe station and an HP 4155B semiconductor device parameter analyzer at EPFL. The devices were characterized after the SiNWs have been released. A droplet of isopropanol or PBS buffer solution (pH = 7.0) is placed on top of the device of interest in order to allow liquid gating with the suspended SiNWs and the Pt side-gates or backgate and then covered with a glass slide to prevent fast evaporation of the liquid during the measurements. The light was switched on.

## 4.2 Sensor characterization

The sensor performance characterization experiments shown in Chapter 6 were made using a Microtech cascade manual probe station and Agilent semiconductor device parameter analyzer B1500 at Tyndall National Institute and/or an HP 4155B semiconductor device parameter analyzer at EPFL, Figure 4-1a. The light was switched off.

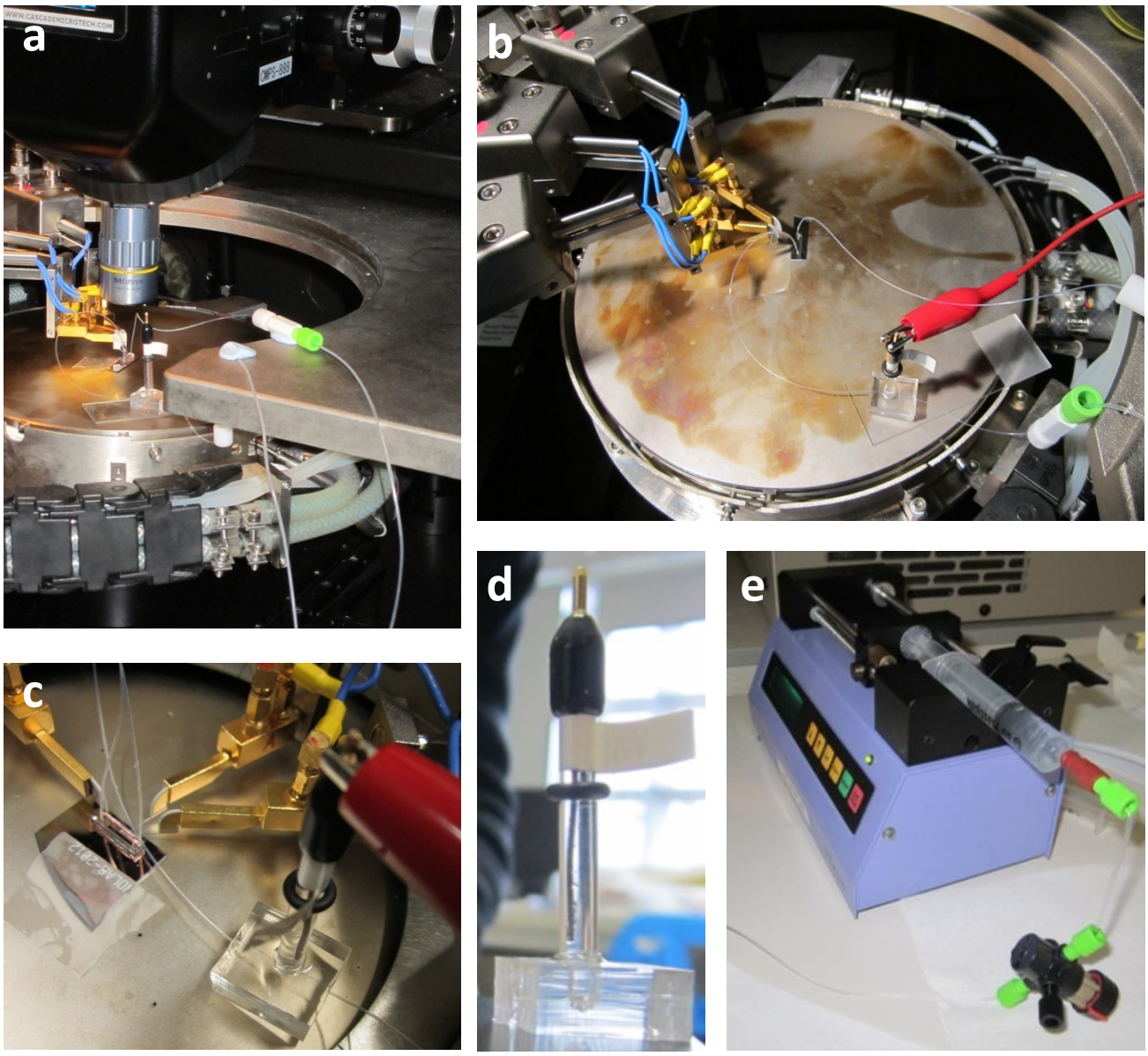



**Figure 4-1:** (a, b, c) Images showing an integrated device ready for measurement within the Cascade probe station with the tubing used to hydrodynamically transfer fluid to/from the device with integrated flow-cell reference electrode. (b) Reference electrode and flow cell close-up. (e) Syringe pump with attached T-junction 10 cm away from syringe exit.

Figure 4-1 shows the measurement set-up used for the characterization of the sensor capabilities of our 3D structure used in Tyndall. Figure 4-1a, b, c show the device being tested inside the Cascade probe station (also used in transient measurements) with the connecting tubing and reference electrode/flow cell shown as well.

Since the Pt side-gate potential has been shown to change as a function of pH and in general does not provide a stable potential over time in an electrolyte solution, a constant liquid potential during the sensor characterization was finally maintained by the use of an Ag/AgCl reference electrode (ALS RE-1S, 4 mm barrel diameter) incorporated into a flow cell (Figure 4-1d) and attached to the microfluidic channels by PTFE tubing, Figure 4-1a, b, c. The flow cell was tailor-made at Imperial College, London. It consists of a small volume chamber (~1 μL) at the base of the electrode which is supplied via a 1 mm diameter channel fabricated in PDMS.

Fluid delivery was possible by bonding a PDMS stamp that includes microfluidic channels to the top of the chip as previously discussed in Section 3.4. The solution was delivered to each sensor structure at a rate of 100 – 150 μL/min with a syringe (BD Plastipak, 10 ml) propelled by a pump (Harvard, Pump 11+, Figure 4-1e). From the syringe, the flow passed through polyethylene (PE) tubing (inner diameter ID 0.4mm, outer diameter OD 1.0mm). Inside the probe station (Figure 4-1a, b, c), the tubing was downsized (OD 0.4 mm ID 0.1 mm PTFE tubing) using interconnect junctions fabricated in-house from PDMS. Commercially available interconnects can also be used (Upchurch Scientific). The smaller tubing was required to interface to the PDMS stamp by inserting into the pre-drilled holes, but could not be used for the entire length of the fluid supply lines due to excessive back-pressure.

Three commercially available PBS solutions (Fisher Scientific) of varying pH (4, 7 and 10) values were utilized for pH sensing experiments. For the streptavidin sensing experiments, small quantities of streptavidin solution were introduced within a continuous stream of PBS buffer solution. The analyte solution (streptavidin solution on PBS) can be injected separately into the main channel solution by the use of a T-junction located about 10 cm away from the syringe exit (Figure 4-1e). From the T-junction, the flow continued along the PE tubing (~ 1 m) into the probe station. Standard fittings from Upchurch Scientific were used for all connections.

## 4.3 Organic surface functionalization

The organic surface functionalization chemistry utilized for the sensing experiments was developed at Tyndall National Institute in Cork, Ireland as part of the SiNAPS European project collaboration with EPFL. The surface functionalization chemistry established in Tyndall was first developed on planar Si substrates then transferred to silicon nanowires and finally to the vertically stacked structures. The binding of the biotin-linker to the planar surface was monitored and characterized by X-ray photoelectron spectroscopy XPS. Fluorescence spectroscopy was then used to monitor dye conjugated streptavidin molecules to biotinylated surfaces. In here we will only introduce some of the key elements that deal with the functionalization protocol for completeness and we refer the reader to [123] for further details.

A preliminary separate study with the goal of determining the type of surface material and functionalization protocol that could yield the highest oligonucleotide binding affinity for DNA sensing applications was performed in stand-alone vertically stacked SiNW test structures by Magna Diagnostics in collaboration with EPFL. Due to technical issues no final oligonucleotide immobilization protocol was determined and therefore no oligonucleotide immobilization method was ever implemented on complete fabricated devices for sensing. Nonetheless, the study did yield important clues about the possibility of achieving selective surface modification due to surface roughness. This will be discussed shortly. In here we give some details about the functionalization protocols used.

### 4.3.1 Aminosilanization for pH sensing

Silanization chemistry involving the reaction between hydroxyl terminated surfaces and organosilanes was used for this work. Figure 4-2 illustrates the different surface modification steps from hydroxyl termination to biotinylation. The SiNW devices (with $SiO_2$ or $HfO_2$ surfaces) were treated in a piranha solution (3:1, $H_2SO_4$:$H_2O_2$) for one hour at 80 °C to leave clean hydroxyl-terminated (Si-OH) surfaces and remove any left-over organic contamination. The piranha treated surface show very low contact angles indicative of highly hydrophilic surfaces. A solution of 5 v/v % APTES in anhydrous toluene was then administered and left to react with the surface for 3 hours at 50 °C and finally rinsed with anhydrous toluene, deionized water and dried under $N_2$.

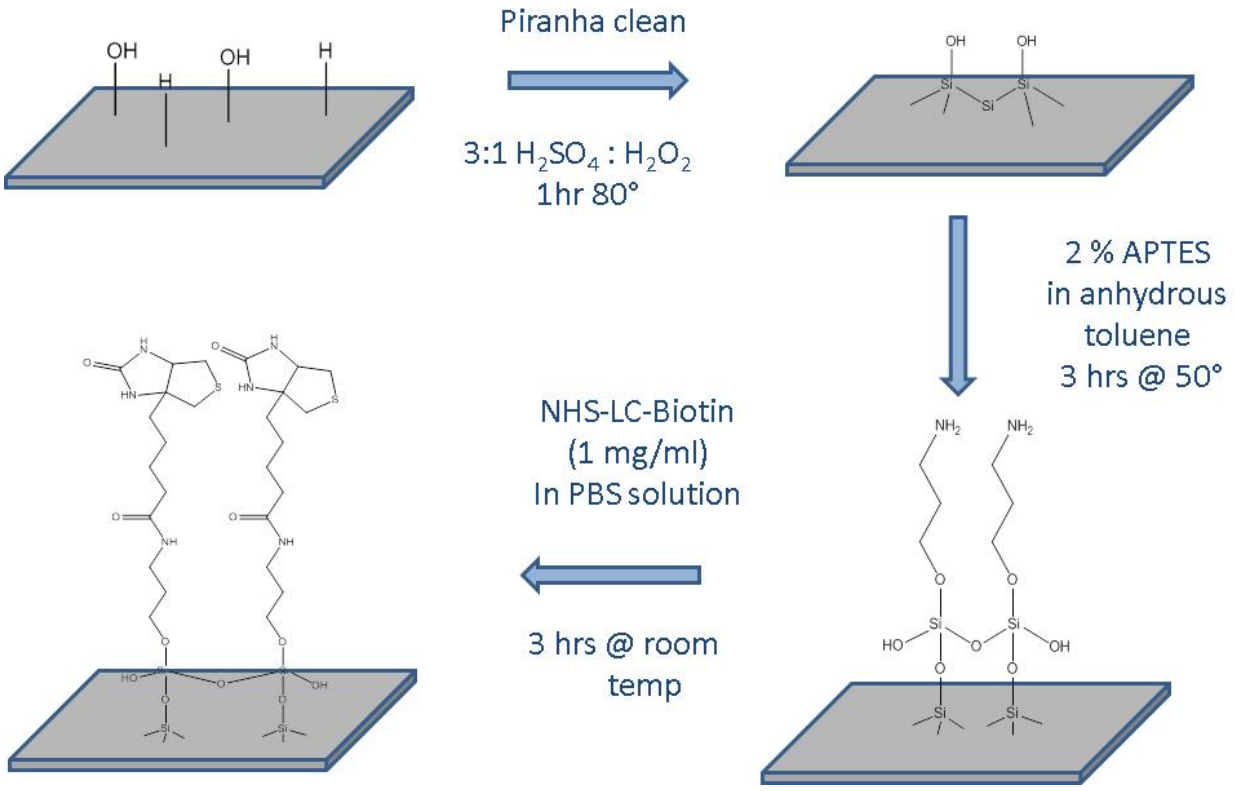



**Figure 4-2:** Cartoon illustrating surface modification protocol: hydroxylation, APTES modification, biotinylation. Courtesy of O. Lotty, Tyndall National Institute, Cork, Ireland.

## 4.3.2 Biotinylation for streptavidin sensing

The previously aminosinalized samples were subsequently biotinylated using succinimidyl 100 µL of 6-(biotinamido)hexanoate (NHS-LC-biotin) and 2 mL of PBS (pH = 7.4, 1 mg/mL) in Dimethylformamide (DMF) for 3 hours at room temperature. The surfaces were rinsed with PBS and deionized water and dried under nitrogen. The NHS-LC-biotin reacts with the primary amine of the surface-tethered silane to leave a biotinylated surface. Contact angle measurements changed from 19° (highly hydrophilic) to ~70° (less hydrophilic), consistent with successful surface modification.

## 4.3.3 Oligonucleotide immobilization for DNA sensing

Two different methods for oligonucleotide (short, single-stranded nucleic acid fragments) immobilization were tested. The first one involves the use of thiol-modified oligonucleotides directly bound onto hydroxylated Au coated SiNWs test structures. The second one involves the immobili-

zation of amino-modified oligonucleotides to the SiNW surface (ALD $HfO_2$, $Al_2O_3$ 5 and 10 nm or $SiO_2$) via an APTES linker. The test structures utilized here consist of 7 × 10 SiNWs arrays with lengths from 2 to 20 μm and fabricated as described in Section 3.2 of this thesis.

The oligonucleotide immobilization and hybridization efficiency is studied by means of fluorescence detection by confocal laser scanning microscopy (CLSM). Optical detection of immobilized oligonucleotides was done by visualization of the Cy3-labeled conjugate. Though no actual functional sensor structures were ever modified for DNA sensing, important observations can be drawn from the study and will be presented here.

#### 4.3.3.1 Silanization based approach

For the silanization based surface modification, the samples are washed with deionized water and isopropanol and finally dried at room temperature for 10 minutes. The samples are then placed in an oxide activation solution (25% $NH_3$, 30% $H_2O_2$, and $H_2O$, 4 :1 :7) in a glass staining box and then placed in an oven for 5 minutes at 70 °C to create a hydroxyl terminated chemical oxide. Deionized water is used to rinse the samples and then placed in a 5% APTES solution in acetone and incubated for 24 hours at room temperature in a glass staining box to complete the aminosilanization of the devices. Subsequently, the samples are placed in an oven for 40 minutes to dry at 120 °C. The sample is cooled at room temperature and super-glued to a glass slide for further processing. A 20 mM solution of $BS_3$ in PBS was dripped onto the samples and incubated for 20 minutes. The sample is cooled at room temperature and super-glued to a glass slide for further processing. A solution of 30 μM of oligonucleotide (Amino-DG74) dissolved in PBS was dripped onto the sample and left to react for 60 minutes. Afterwards, the sample-surface was blocked with 1% bovine serum albumin (BSA) in PBS. The chip is then washed with deionized water and dried at room temperature. The remaining part of the procedure is carried out in the dark. 30 μM of Cy3-DG74 dissolved in PBS was dripped onto the samples and left for 60 minutes to react with the sample. The chip is then washed with deionized water and dried at room temperature. Finally a picture of the sample can be taken using CLSM at a wavelength of 570 nm at various magnifications.

The fluorescence signals produced as a result of the Cy3-labeled oligomer hybridization to their corresponding pairs are shown in Figure 4-5. Figure 4-5a shows a 5 × 4 array of vertically stacked

structures with Figure 4-5b showing a magnified view of single structure after hybridization. The first two column of devices in a have not been oxidized enough and consist of scalloped trenches, the last column does not have anything in the middle of the butterfly structure they have been have been completely consumed by the oxidation. Though some immobilization was found to be taking place at the butterfly structure around the nanowires (left corner Figure 4-5b), the strongest signals were detected primarily at the SiNWs (center of Figure 4-5b).

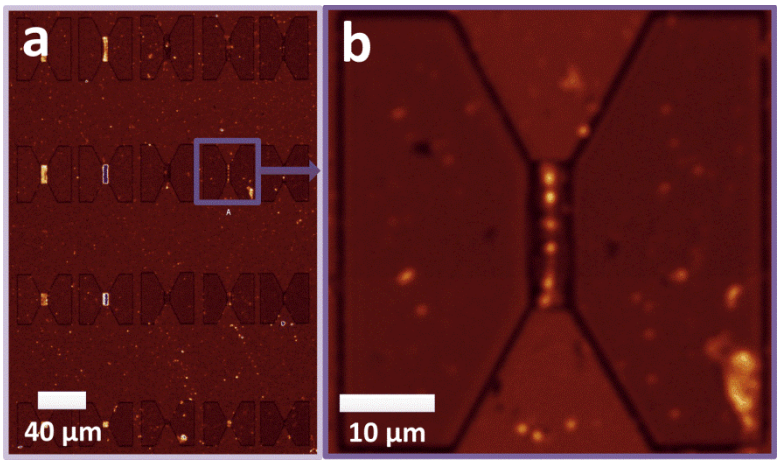



**Figure 4-3:** (a) Scanned fluorescent image taken by CLSM at 40X magnification and (b) amplified view of butterfly structures after silanization and oligonucleotide immobilization at 63X magnification. The fluorescence signal is highest at the center of the structure where the NWs are.

A difference in roughness due to the BOE etch appears to the major cause for this "selective" immobilization since the entire surface is chemically similar. These results prove that biomolecules can be immobilized with a certain degree of specificity at the site of the NWs with the protocols used. The same results were found for all dielectrics ($HfO_2$, $Al_2O_3$, or native oxide/$SiO_2$) used with the highest signal intensities found for structures when a native oxide/$SiO_2$ dielectric is used followed by alumina covered structures. True selective surface modification is limited nevertheless, as the entire area is available and open for functionalization. Another possibility would be to use the ZEP resist window throughout the functionalization/immobilization process as a protective mask. Nonetheless, the use of ZEP would not be possible if hydroxylation by the use of a piranha solution is to be used during the silanization procedure.

On the other side, only the NWs and exposed anchoring sides should produce an electrical signal with biomolecule conjugation for sensing. SU-8 covers all but a small window of 30 × 30 μm² around the SiNWs. Also, the BOX layer of the SOI wafer isolates the structure so that even if the bottom or surrounding areas have been modified they would not produce an electrical signal (only optical). One important point to keep in mind nevertheless, is that unintended biomolecule attachment as the analyte flows through the microfluidic channel prior to reaching the sensing structure would efficiently reduce the concentration of that molecule, making it more difficult to be detected.

Furthermore as previously mentioned, it is of primary importance to produce SiNW structures robust enough to endure a possibly harsh functionalization process. For that reason the samples were inspected before and after the different surface modification procedures by SEM in order to verify that the structures have not been damaged. Figure 4-4a shows the top-side tilted-view and close up (Figure 4-4b) of a butterfly test-structure after the silanization and oligonucleotide immobilization procedure.

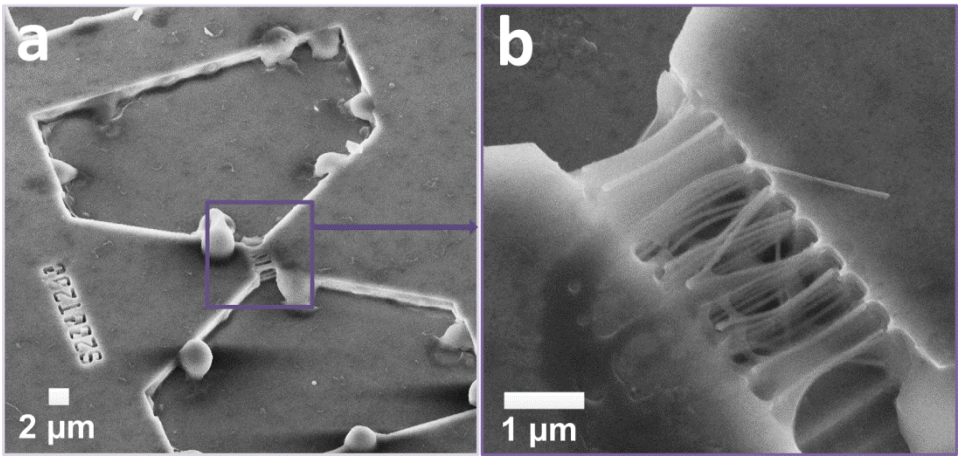



**Figure 4-4:** (a) Top-side tilted-view of butterfly test structure covered with a 10 nm ALD $Al_2O_3$ conformal layer after the silanization based oligomer immobilization and hybridization process and (b) close-up with some SiNWs broken.

Though it is clear from Figure 4-4b that some SiNWs are broken we believe that the breakage only occurred until after the successful hybridization, drying and storage of the samples as the nanowires are still present within the organic mesh and seem to be pulled by it. Also, no breakage or

clumping was seen when the slightly simpler silanization or biotinylation procedure was performed by Tyndall with their own protocols as described previously.

### 4.3.3.2 Thiolation based approach

Gold was deposited selectively on the SiNW area through the ZEP-window used to selectively remove the $SiO_2$ around them by BOE as described in Section 3.3.5 (Figure 4-5a) by electron beam evaporation (Figure 4-5b). Due to the directionality of the evaporation process the sample had to be placed on an angle in the evaporator and then rotated 180° for a second tilted deposition process in order to achieve Au coverage on both sides of the SiNW stack. 5 nm of Gold are deposited per evaporation step on each side.

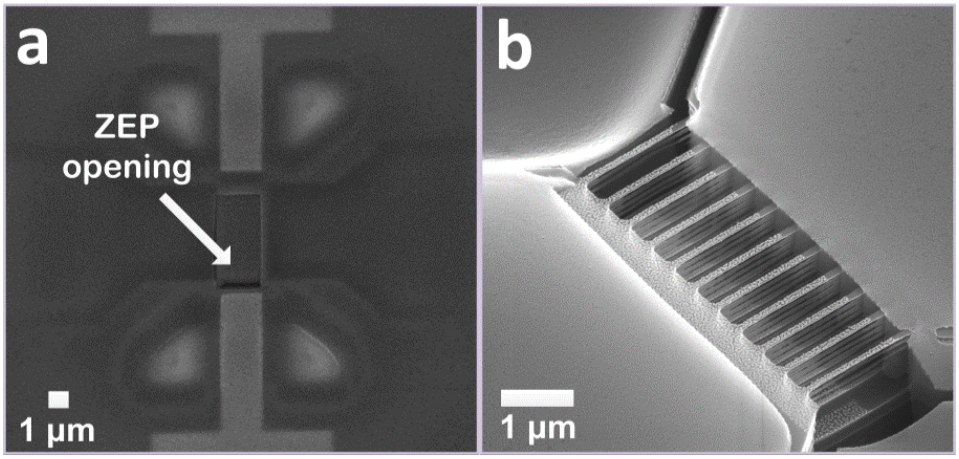



**Figure 4-5:** (a) SEM top-view of ZEP window to selectively remove $SiO_2$ around NW area and (b) released structure on which Au has been deposited by e-beam evaporation through ZEP window. The ZEP window is slightly misaligned to the left, allowing for Au deposition on the top of the S/D anchor.

The samples are again washed with deionized water and isopropanol and dried in an $N_2$ stream. They are then hydroxylated in a piranha solution (25% $H_2SO_4$, 30% $H_2O_2$, 7:3) for 10 minutes. Deionized water is used to rinse the samples and then placed in an oven for 10 minutes to dry at 120 °C. The sample is cooled at room temperature and super-glued to a glass slide for further processing. A solution of 30 µM of oligonucleotide (thiol-DG74) dissolved in PBS was dripped onto the sample and left to react for 60 minutes. Afterwards, the sample-surface was blocked with 1% bovine serum albumin (BSA) in PBS. The chip is then washed with deionized water and dried at

room temperature. The remaining part of the procedure is carried out in the dark. 30 μM of Cy3-DG74 dissolved in PBS was dripped onto the samples and left for 60 minutes to react with the sample. The chip is then washed with deionized water and dried at room temperature.

When the thiol-based oligonucleotide immobilization protocol was used no optical signal was observed by CLSM pointing to an unsuccessful immobilization/hybridization. The structures were also observed by SEM after the surface functionalization was performed, Figure 4-6. In comparison to the results when the oligonucleotide immobilization by a silanization-based protocol is used, no breakage, pulling or clumps were observed by the thiol-based method. This also demonstrates that the SiNW breakage observed in b must be caused by the drying up process after hybridization and not by the functionalization method itself.

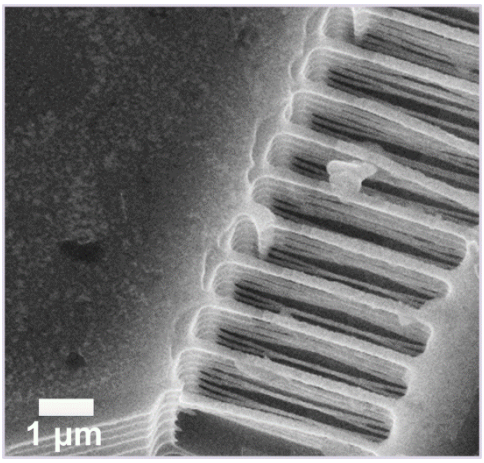



**Figure 4-6:** Top-side tilted-view of butterfly test structure after the thiol-based oligomer immobilization.

## 4.4 Summary

The experimental details for the electrical and sensing characterization of the 3D devices have been described in this chapter. Additionally, the different functionalization protocols used in this thesis have been discussed. The main contributions of this chapter are:

- A simple method to electrically characterize the structures through a liquid (IPA) by the use of the Pt side-gates and backgate was established.

- A dedicated set-up for biotin-streptavidin and pH sensing was arranged.
- An efficient functionalization protocol for the biotinylation and aminosilanization of the 3D structures was implemented.
- The main difference in surface roughness resulting from the selective BOE etch around the NW array was shown to be beneficial for the selective silanization by APTES and the oligo-nucleotide immobilization protocol.

# Chapter 5 Transistor characterization

3D vertically stacked silicon nanowire FETs featuring high density arrays (up to 8 × 20 SiNWs) of ultra-thin, fully depleted channels are characterized electrically for their implementation into robust biosensing systems. The devices consist of vertically stacked SiNWs anchored in between highly doped ($n^+$ phosphorous > $10^{18}$ $cm^{-3}$) source and drain extensions as described in Section 2.4.2. The structures were first characterized electrically in dry conditions when completely surrounded by a thick oxide layer (prior to oxide removal by BOE) and after release.

## 5.1 Device description

The final fabricated structure with released SiNWs is shown in Figure 5-1a. It consists of source $V_s$ and drain $V_d$ contacts and one or two symmetrical Pt gates to the sides $V_{SG}$. The ultra-thin ($d_{NW}$ < 35 nm) SiNWs may be surrounded by a conformal high-$\kappa$ gate dielectric ($HfO_2$) or silicon dioxide and gated all around by an integrated reference electrode ($V_{Ref}$), a backgate and one or two symmetrical platinum side-gates through a liquid. The liquid-gated electrical characterization results are presented in Section 5.4 of this thesis.

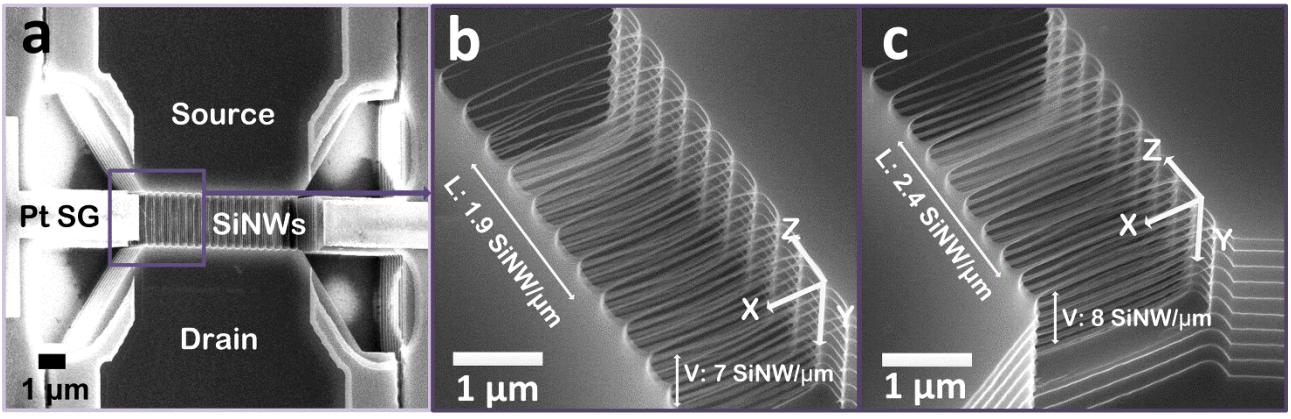



**Figure 5-1:** SEM top-side tilted-views of SiNWs arrays with two different vertical and horizontal SiNW densities and diameters: (a) V = 7 SiNWs/µm, H = 1.9 SiNWs/µm, $d_{NW}$ = 15 – 30 nm and (b) V = 8 SiNWs/µm, H = 2.4 SiNWs/µm, $d_{NW}$ = 25 – 35 nm ($L$ = 2 µm).

Two types of arrays of SiNWs were characterized here. The first type is shown in Figure 5-1b and has a constant density of 7 SiNWs/µm in the vertical direction and 1.9 SiNWs/µm in the horizontal direction. The second structure shown in Figure 5-1c has a density of 8 SiNWs/µm in the vertical direction and 2.4 SiNWs/µm in the horizontal direction. Devices with varying number of SiNWs in the horizontal direction (10, 15 and 20 SiNWs) and source to drain lengths ($L$ = 2, 3, 4 µm) were characterized.

## 5.2 Dry characterization prior to SiNW release

### 5.2.1 Contact characterization

The 3D FET device drain current curves as a function of drain potential ($I_d$ – $V_d$, with $V_{BG} = V_{SG} = 0$ V) were first obtained in ambient conditions (dry, room temperature) prior to removing the $SiO_2$ that surrounds the NWs in order to assess the quality of the electrical contacts. Figure 5-2a, b show the $I_d$ – $V_d$ curves for different device structures within the same die with an increasing number of NWs before and after the contact anneal, respectively.

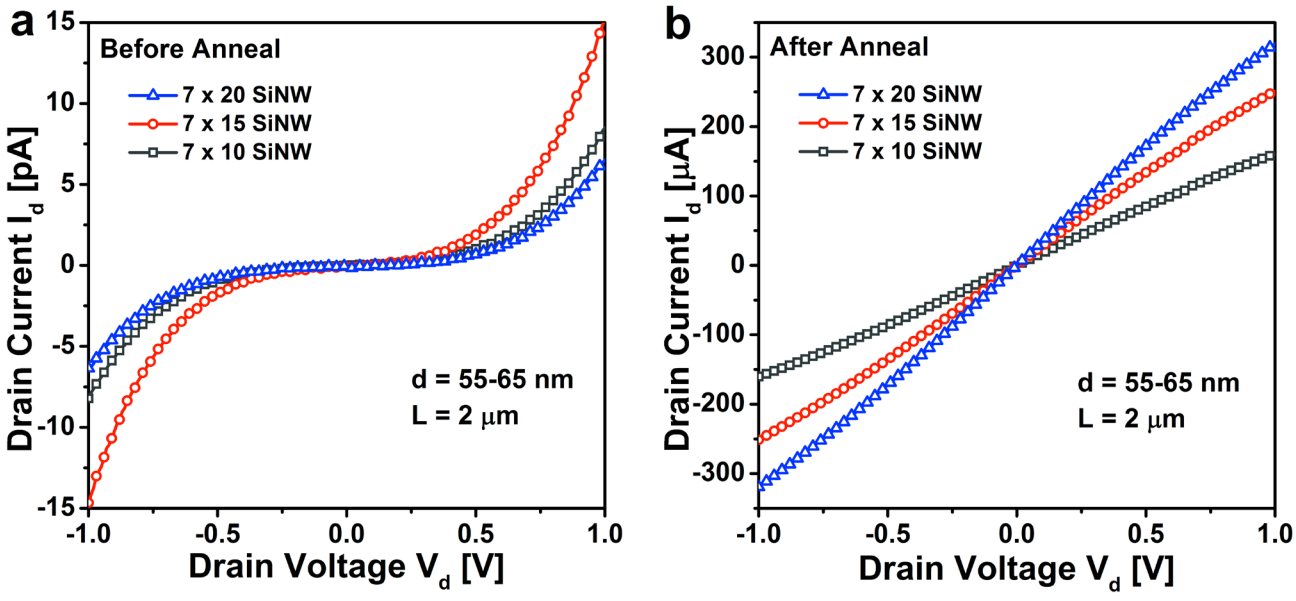



**Figure 5-2:** $I_d$ – $V_d$ output characteristics for devices with different NW densities: 10, 15, 20 NWs × 7 NWs (a) before and (b) after metal anneal respectively. The NWs are still within their $SiO_2$ encapsulation and therefore the NW size still bigger than the targeted size $d_{NW}$ < 40 nm.

Prior to the thermal anneal, non-linear $I_d - V_d$ curves are observed due to the Schottky barriers at the contact metal-Si interface. Low current levels in the order of pA and no particular dependence of $I_d$ with number of NWs or length are seen before the anneal. A high current level rise is observed after the anneal (increasing with NW number).

Using the transfer length method (TLM) [124] we obtain a contact resistance of $R_C$ ~ 2.9 kΩ/contact, SiNW resistance $R_{NW}$ ~ 753 Ω/NW and finally a specific contact resistance of $\rho_c$ ~ 3.3x10$^{-3}$ Ω cm$^2$ from $I_d - V_d$ curves for structures with different SiNW lengths within the same die ($L$ = 2, 3 and 4 μm, $d_{NW}$ ~ 55 – 65 nm, 7 × 10 SiNW array) assuming that the SiNW dimensions, doping concentrations and contact dimensions are constant for the different devices. This is a reasonable assumption for devices within the same die, in close proximity of each other. The total resistance is described by Equation 5.1, [124]:

$$R_T = R_{NW} + 2R_c \approx R_s \frac{L}{d_{NW}} + 2\frac{\rho_c}{\lambda d_{NW}}$$

**Equation 5.1**

Where $R_s$ is the sheet resistance (Ω/sq.) and $\lambda$ is the transfer length, Equation 5.2:

$$\lambda = \sqrt{\rho_c / R_s}$$

**Equation 5.2**

By plotting the total current $R_T$ *vs.* the $L$ of the NW array one can obtain the contact, SiNW and the specific contact resistance from the slope and y-intercept.

The contact resistance after the anneal was found to contribute < 5% to the total electrical resistance for the devices measured, which together with the linearity of the $I_d - V_d$ characteristics suggest ohmic behavior (contact where carriers are free to flow with voltage independent resistance). The SiNW diameters were determined from cross-sections made by focused ion beam (FIB, FEI Nova 600 NanoLab). Device performance is highly dependent on the quality of the metal-semiconductor

contact. In order to achieve low contact resistances, high doping concentration levels (> $10^{19}$ $cm^{-3}$, close to Si-metal interface as per MC simulations) have been accomplished by ion implantation and rapid thermal anneal. Also, aluminum with a work function value (~ 4.1 V) close to that of the electron affinity of the n-Si (~ 4.15 V) [125] was chosen as the metal contact. An annealing step to produce a Si/Al alloy at the interface and reduce the resistivity was as well incorporated into the process flow and finally the contact area $A_c$ ($R_c = \rho_c/A_c$) was designed to be quite large (> 10 × 10 μm²) to improve the performance of the metal/semiconductor contact.

## 5.2.2 Transfer characteristics

The $I_d - V_{BG}$ curves ($V_d$ = 1 V, 50 mV, $V_S$ = 0 V, the side-gates were left floating) for arrays with 7 × 10 SiNWs and $d_{NW}$ = 45 – 55 nm as the channel length ($L$ = 2, 3, 4 μm) increases are shown in Figure 5-3.

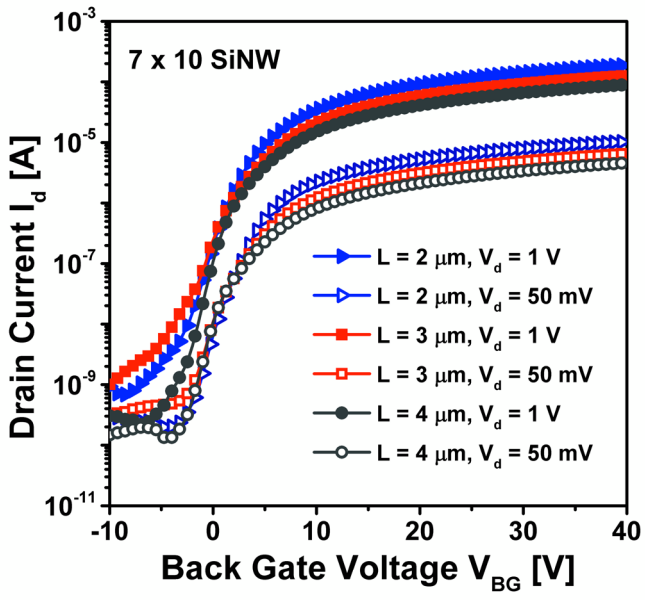



**Figure 5-3:** $I_d - V_{BG}$ curves for high ($V_d$ = 1 V) and low ($V_d$ = 50 mV) drain potentials for 7 × 10 SiNWs structures ($V_{SG}$ = 0 V, $d_{NW}$ = 45 – 55 nm) prior to oxide removal by BOE) as the length increases $L$ = 2, 3 and 4 μm.

The $I_{on}$ current defined as the current at which $V_{BG}$ = 10 V and $V_d$ = 50 mV, normalized to $d_{NW}$ = 55 nm, was found to be 40.5 μA/μm for the structure with $L$ = 2 μm and decreases with NW

length. The leakage current ($I_{off}$) defined as the $I_d$ at $V_{BG}$ = 0 V, for $V_d$ = 50 mV was found to be 0.1 μA/μm (also normalized to $d_{NW}$ = 55 nm for the same structure). The $I_{on}/I_{off}$ was found to be ~390. A high backgate potential is needed in order to operate the device with a $V_{th}$ = 11.6 V. The threshold voltage $V_{th}$ is defined as the voltage for which the drain current reaches a value of $I_d = (100\ \mu A * d_{NW}/L)$. A subthreshold slope of 1.6 V/dec was extracted from Figure 5-3. Approximately 70 nm of silicon oxide surround the SiNWs prior to oxide removal. Electrostatic control through the thick oxide ($\varepsilon_r$ = 3.9) under dry conditions was therefore found to be poor as the high $SS$ and $V_{th}$ values indicate.

## 5.3 Dry characterization after SiNW release

After the oxide was removed to produce suspended SiNWs, the devices were characterized electrically under ambient, dry conditions, at room temperature by the use of the backgate and Pt sidegates. Native oxide forms spontaneously (~ 2 nm) around the suspended nanowires after they are exposed to air, acting as a gate dielectric.

The measured drain current curves as a function of drain potential ($I_d - V_d$) with increasing backgate voltage values ($V_{BG}$ = 0 – 40 V, $V_{SG}$ = 0 V) for a representative array with 7 × 10 SiNWs, $L$ = 3 μm and $d_{NW}$ = 15 – 30 nm (determined by SEM) are shown in Figure 5-4. The normal operation of n-type device transitioning from linear to saturation regimes as the drain voltage increases is observed. The SiNW diameter decreases after the BOE etch to remove the $SiO_2$ that surrounds the SiNWs. This, together with the lower dielectric constant of air ($\varepsilon_r$ = 1, *vs*. $SiO_2$ $\varepsilon_r$ = 3.9) may explain the lower currents found when the suspended structures are measured under dry, ambient conditions in air. The $I_d - V_d$ characteristics when $V_{BG}$ = 0 V and $V_{SG}$ = 0 V (not visible) are still linear demonstrating that the contacts have not been damaged throughout the rest of the fabrication process flow.

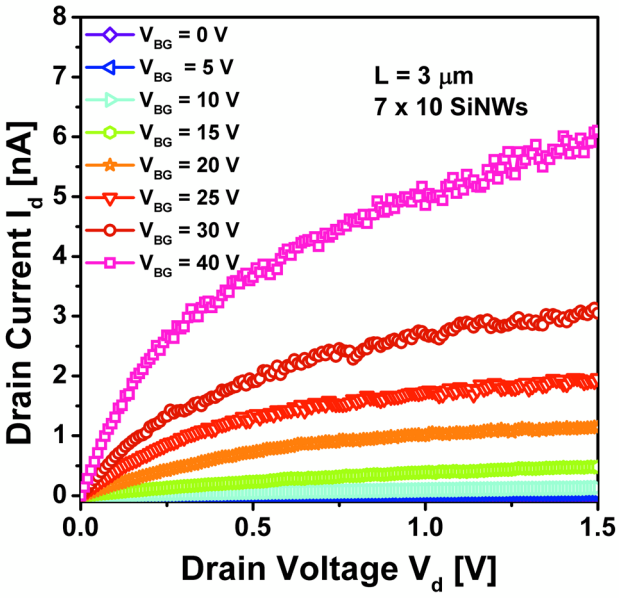



**Figure 5-4:** $I_d$ – $V_d$ curves with increasing backgate potentials ($V_{BG}$ from 0 to 40 V) for a 7 × 10 SiNWs structure after oxide removal ($V_{SG}$ = 0 V, $L$ = 3 µm, $d_{NW}$ = 15 – 30 nm).

The $I_d$ – $V_{BG}$ curves for the same device with increasing double-gate voltage ($V_{DG}$, simultaneously biasing both side-gates) while keeping the $V_d$ = 1 V constant are shown in Figure 5-5. The $I_{off}$, $I_{on}$ (normalized to $d_{NW}$ = 30 nm, $I_{on}$ is $I_d$ when $V_{BG}$ = 30 V) and $I_{on}/I_{off}$ when $V_{DG}$ = 0 V were found to be 1.2 × $10^{-6}$ mA/µm, 0.5 µA/µm, > $10^2$ and respectively. A subthreshold slope of 7.5 V/dec and $V_{th}$ (here defined as the voltage for which the drain current reaches a value of $I_d = (100\,nA * d_{NW}/L)$) was found be ~ 13.5 V from the same curve. The threshold voltage decreases with increasing positive DG potentials. Also, a slight subthreshold slope improvement is observed in the $I_d$ – $V_{BG}$ characteristics as the $V_{DG}$ increases towards more positive values. The $SS$ decreases from ~ 7.5 V/dec when $V_{DG}$ = 0 to ~ 6.7 V/dec for $V_{BG}$ = 40 V. Furthermore, the $SS$ degrades with increasing negative $V_{DG}$ values ($SS$ ~ 19 V/dec, $V_{BG}$ = - 40 V) as the inversion layer on each channel decreases with a negative gate potential consistent with the behavior of an n-type device. It is important to remember that the NWs are suspended and have no direct contact to the Pt side-gates or BOX. The Pt side-gates are located 1 µm away (relatively far away) from the last NW from each side of the array as

can be seen in Figure 5-1. Therefore, poor electrostatic control by the use of the backgate or side-gates is expected through air as evident from their transistor characteristics.

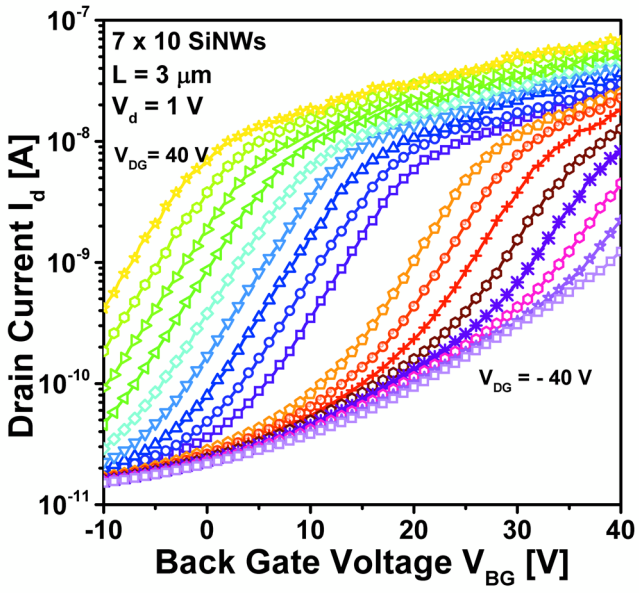



**Figure 5-5:** $I_d$ – $V_{BG}$ as the double gate potential $V_{DG}$ increases from -40 V to 40 V for a 7 × 10 SiNWs structure after oxide removal ($V_d$ = 1 V $L$ = 3 μm, $d_{NW}$ = 15 – 30 nm).

## 5.4 Liquid-gated experiments after SiNW release

### 5.4.1 Transistor characteristics

The structures with suspended SiNWs were then characterized electrically in a liquid environment (isopropanol IPA, $\varepsilon_r$ = 18) by the use of the backgate or Pt side-gates. Native oxide acts as a gate dielectric. The measurements were repeated several times. The use of the Pt electrode to gate the SiNW array with isopropanol proved to produce repeatable measurements with IPA (Figure 5-6, 8 × 10 SiNW, $L$ = 2 μm, $d_{NW}$ = 25 – 35 nm).

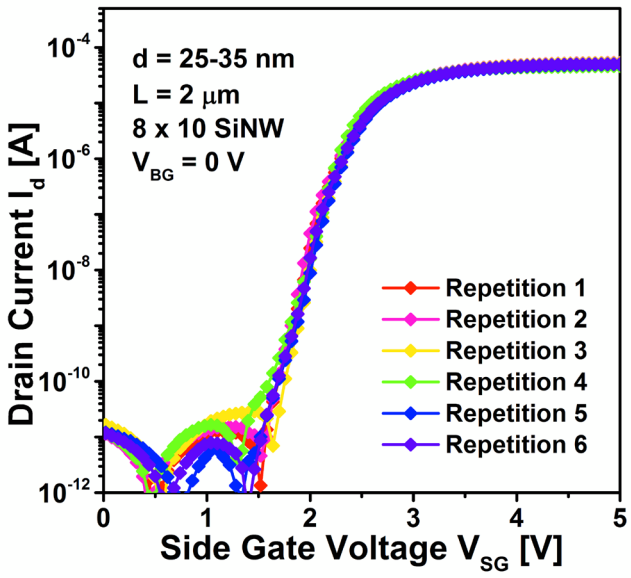



**Figure 5-6:** $I_d$ – $V_{SG}$ measurement repeated several times for a 8 × 10 SiNWs structure, $L$ = 2 µm, $d_{NW}$ = 25 – 35 nm, $V_d$ = 50 mV and $SiO_2$ gate dielectric.

The transistor characteristics obtained for different devices with the same parameters (length and number of NW) within the same die were found to be comparable (Figure 5-7). Nonetheless, there is still a threshold voltage variation ($V_{th}$ = 2.43 ± 0.98 V) among devices that it is believed most likely due to fabrication related non-uniformity typically encountered in a non-dedicated fabrication facility. In Section 3.6 of this thesis we discuss some strategies to ameliorate process related issues. Though the electrical performance characteristics ($V_{th}$, $SS$) of typical enhancement mode SiNW devices have been found not to change significantly with NW width and height for widths > 10 nm [61, 126], for liquid-gated SiNW devices there has been found a $V_{th}$ dependence with width for much thicker structures (> 50 nm) that the authors assign to a higher sensitivity of the NWs to surface charges [18] that may explain the wide variation found here.

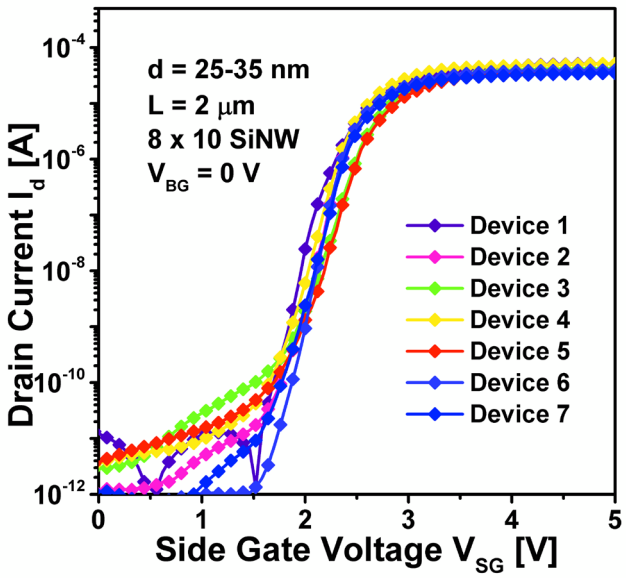



**Figure 5-7:** $I_d$ – $V_{SG}$ measurements for different devices with the same geometric characteristics within the same die for a 8 × 10 SiNWs structure, $L$ = 2 µm, $d_{NW}$ = 25 –35 nm, $V_d$ = 50 mV and $SiO_2$ gate dielectric

The $I_d$ – $V_{SG}$ curves for a forward (solid) and reverse (open) sweep are shown in Figure 5-8 for a 8 × 15 SiNW structure with $L$ = 2 µm. The $V_{th}$ shifts slightly towards the left indicating a positive charge accumulation. Injected interface charges that do not dissipate as the gate bias polarity changes lead to a shift in the threshold voltage [127]. Hysteresis can affect the short term, and long term drift of the sensor response [128]. In here little hysteresis (< 15 mV) is found indicating small surface and interface ($Si/SiO_2$) defect induced charge trapping [127]. Injected interface charges can be eliminated by an annealing step at high temperatures (> 950 °C) in a nitrogen atmosphere for example [129], but this is not compatible with our current fabrication process.

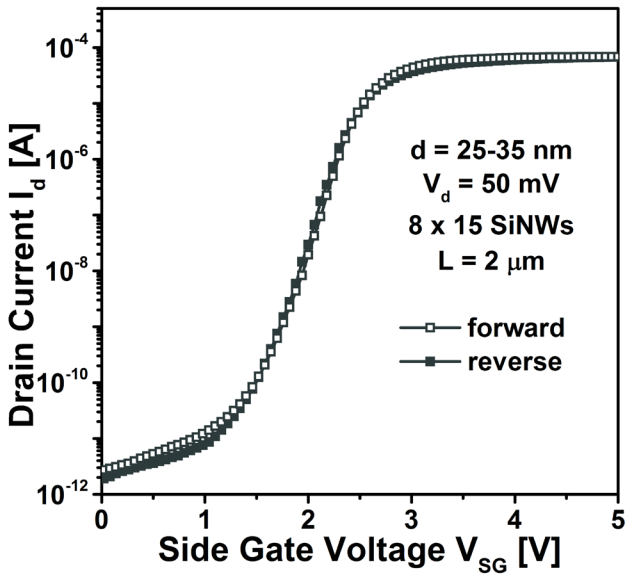



**Figure 5-8:** $I_d - V_{SG}$ curves for forward (solid) and reverse (open) sweep for a 8 × 10 SiNWs structure, $L$ = 2 μm, $d_{NW}$ = 25 – 35 nm and $SiO_2$ gate dielectric.

Nonetheless, extreme care during the fabrication process serves to ameliorate the presence of impurities at the $Si/SiO_x$ interface and surface contamination that may degrade the transistor and sensor performance. Exposure to radiation induced traps (during e-beam lithography, ion implantation, e-beam evaporation, *etc.*) and mobile impurity ions ($Na^+$) is reduced by leaving the SiNWs safely enclosed within $SiO_2$ until the end of the fabrication process flow.

## 5.4.2 Leakage and $I_{on}$ current

The $I_d - V_{SG}$ ($V_S = V_{BG} = 0$ V) for increasing drain potentials ($V_d$ = 50 mV – $V_d$ = 1 V) for structures with 7 × 10 and 8 × 10 SiNWs, $L$ = 2 μm are presented in Figure 5-9a, and b respectively.

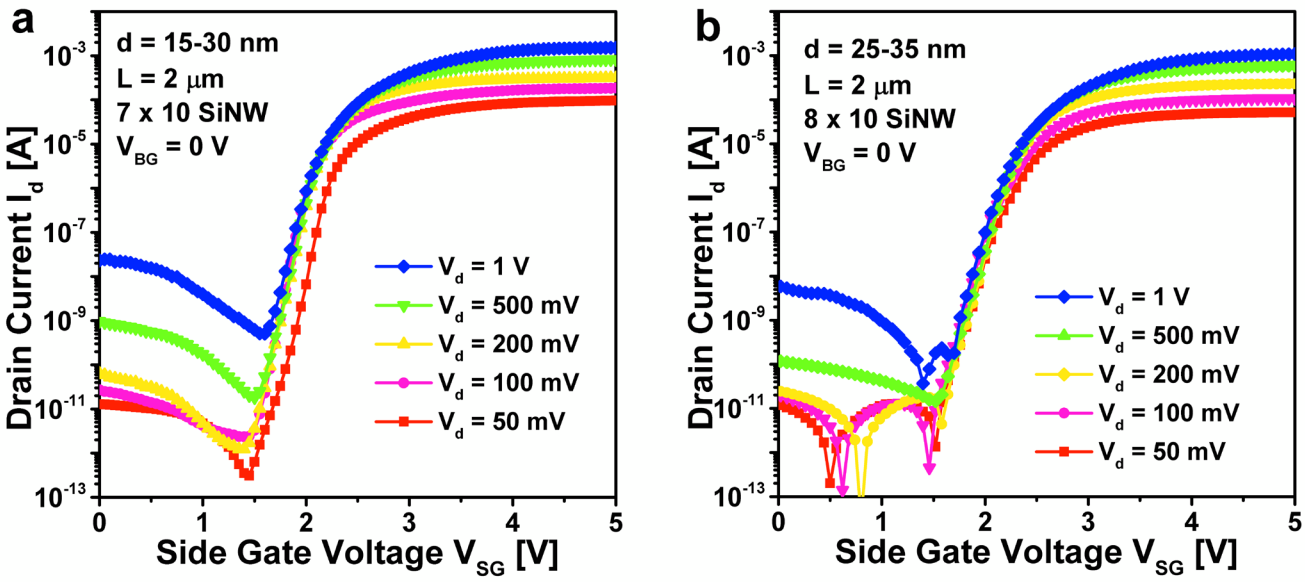



**Figure 5-9:** $I_d$ – $V_{SG}$ for increasing drain potentials ($V_d$ =50 mV – 1 V) for a (a) 7 × 10 SiNWs structure, $d_{NW}$ = 15-30 nm and (b) a 8 × 10 SiNWs structure, $d_{NW}$ = 25-35 nm with $L$ = 2 μm, $SiO_2$ gate dielectric.

The drain-leakage current here is the current at $V_{SG}$ = 0 V. The $I_{on}$ current is defined as the value of $I_d$ at $V_{SG}$ = 3 V (normalized to average NW diameter). In terms of device performance, at low drain potentials $V_d$ < 500 mV, the devices show very low drain leakage currents ($I_{off}$ < 2.1 × $10^{-6}$ mA/μm), high $I_{on}$ (> 2 mA/μm) and high $I_{on}/I_{off}$ ratios (> $10^6$) as can be seen in Figure 5-9 and Figure 5-10. At high drain potentials nevertheless, the $I_{off}$ increases dramatically (*e.g.*, $I_{off}$ > 7 × $10^{-4}$ mA/μm when $V_d$ = 1 V) degrading the $I_{on}/I_{off}$ ratio down to < 1.7 × $10^4$ ($V_d$ = 1 V). Leakage currents through the liquid from source to drain are reduced by covering all but a small area around the NWs with an SU-8 layer. At high drain potentials nonetheless, high leakage currents from source to drain are still observed. The electrical characteristics of devices with increasing number of NW channels and increasing length $L$ dimensions are also compared. The devices with the highest number of nanowires 7 × 20 and 8 × 20 (Figure 5-11a) and the shortest lengths (Figure 5-11b) have the highest on-state currents as was also seen through TCAD simulations, Appendix A.

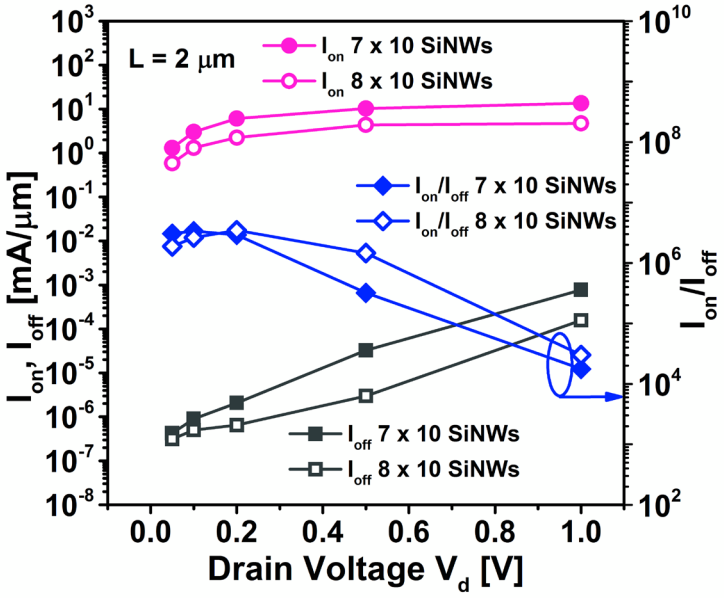



**Figure 5-10:** $I_{on}$ and $I_{off}$ (left) normalized to nanowire diameter ($d_{NW}$ = 15-30 nm for 7 × 10 SiNWs and $d_{NW}$ = 25-35 nm or 8 × 10 SiNWs FET) and $I_{on}/I_{off}$ current ratios (right) as a function of drain voltage with $L$ = 2 µm, $SiO_2$ is the gate dielectric.

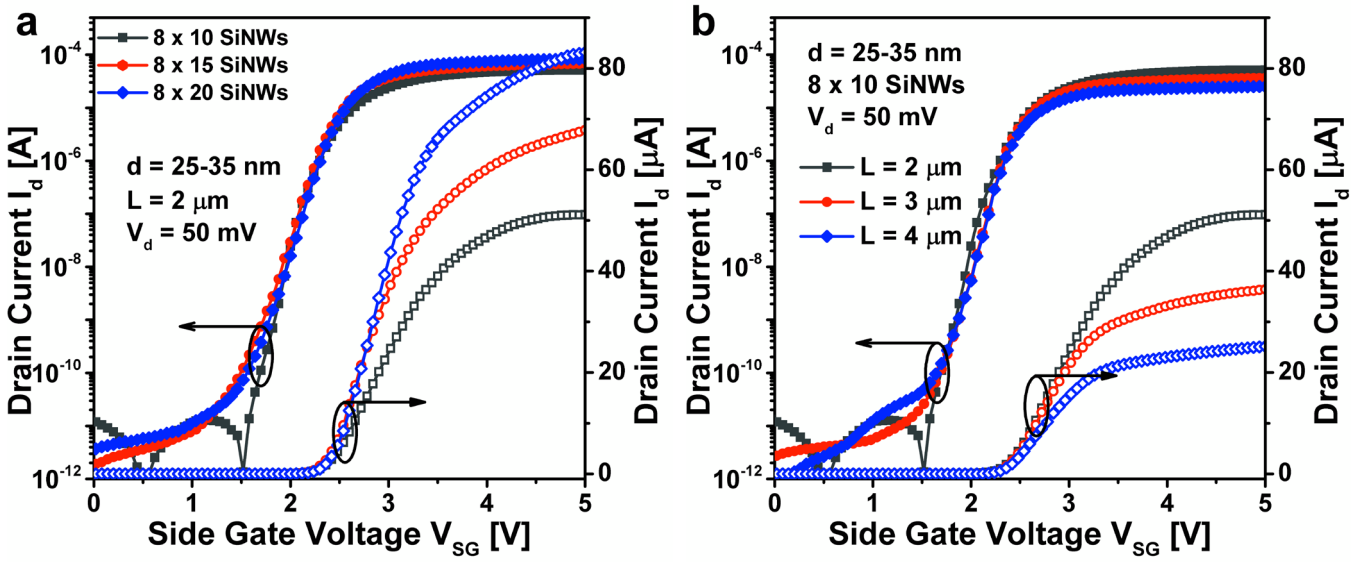



**Figure 5-11:** (a) $I_d - V_{SG}$ curves when $V_d$ = 50 mV for structures with a constant vertical density of 8 SiNWs/µm and increasing number of NWs in the horizontal direction (10, 15, 20 SiNWs) with $L$ = 2 µm, $d_{NW}$ = 25-35 nm, (b) for 8 × 10 SiNWs structures with increasing channel lengths ($L$ = 2, 3 and 4 µm).

### 5.4.3 Transconductance

The transconductance $g_m = (dI_d/dV_{SG})$ is a measure of the sensitivity to surface charges. A high transconductance value means a bigger change in drain current for a given change in surface charge which translates to higher device sensitivities. For that reason, the maximum transconductance gate voltage is sometimes chosen as the operating point for sensor measurements [130]. High maximum transconductance values > 10 µS were found for all devices, (Figure 5-12, right axis). The maximum transconductances values increase with the number of NWs and decrease for increasing lengths.

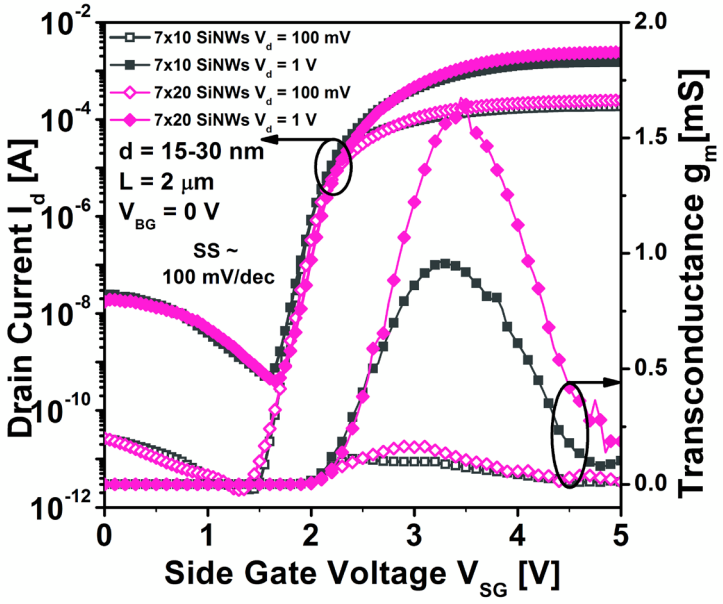



**Figure 5-12:** $I_d - V_{SG}$ curves at high and low drain potentials for 7 × 10 and 7 × 20 SiNWs structures with $L$ = 2 µm, $d_{NW}$ = 15-30 nm, tested in a liquid environment (left). Transconductances for the same devices are shown on the right axis.

### 5.4.4 Drain induced barrier lowering

The DIBL ($V_{d,high}$ = 1 V and $V_{d,low}$ = 100 mV) for all devices was found to be relatively small (< 70 mV/V), Equation 5.3. Though the NWs here are long ($L$ = 2, 3, 4 µm) by any standards, as the drain potential increases, it can also have a bigger influence on the surface potential along the NW gate channel through the liquid (drain/source parasitic capacitance through the liquid to the NW

stack) resulting in an increase of electron injection from source to drain through the NWs. The low DIBL nevertheless points out to the fact the leakage current occurs mostly from source to drain through the liquid.

$$DIBL = \frac{V_{th}|_{V_{d,low}} - V_{th}|_{V_{d,high}}}{V_{d,low} - V_{d,high}}$$

**Equation 5.3**

## 5.4.5 Subthreshold slope

The *SS* values calculated from $I_d - V_{SG}$ curves ($V_{BG}$ = 0 V and $V_d$ = 50 mV) were found to be steep *SS* < 100 mV/dec and < 130 mV/dec for both types of structures 7 × 10 and 8 × 10 SiNWs structures, respectively. The excellent electrostatic control that can be achieved through the liquid as the NWs are gated in a gate all around (multiple-gate) manner serves to produce transistors with low *SS*. These values are comparable to the lowest subthreshold slope values reported in literature for liquid-gated SiNW FET devices as can be seen in Table 2-3 and Table 2-4 of this thesis.

## 5.4.6 Gate dielectric

The SiNW-dielectric interface is important for the electrical stability of the device. An inner oxide (native oxide) would provide a stable contact to the NW whereas the outer dielectric provides a stable contact with the liquid. $SiO_2$ is also not the best pH selective material (as previously mentioned in the introduction of this thesis), and it has been found not to provide a stable contact between the liquid and the sensor [39] since protons can penetrate the Si-oxide layers leading possibly to large leakage currents [19].

ALD layers of high-$\kappa$ dielectrics have been typically used to prevent charge penetration through the native oxide to the SiNWs and to reduce leakage currents through the liquid ($\varepsilon_r$ = 25 for $HfO_2$ [96] *vs.* $\varepsilon_r$ = 3.9 for $SiO_2$). For these reasons, $HfO_2$ and $Al_2O_3$ (10 nm) were deposited as a gate dielectric. Figure 5-13 shows the $I_d - V_{SG}$ curves for different drain potentials for a device before and after the deposition of $HfO_2$. The first observation to note from Figure 5-13 nonetheless is that the $I_{off}$ current does not seem to decrease after the deposition of ALD $HfO_2$. Although it was thought to be

a good strategy to lower the drain leakage current from source to drain through the liquid at high drain potentials in particular ($V_d$ > 500 mV) the high-$\kappa$ dielectric deposition only seems to lower the $I_{on}$ current for these devices.

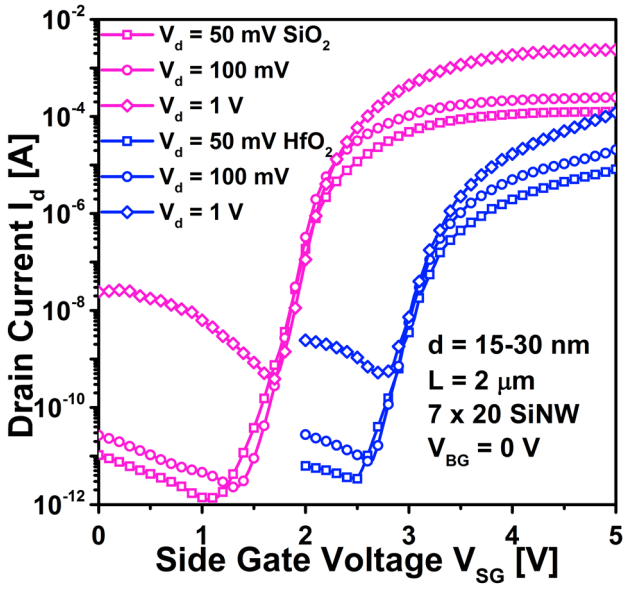



**Figure 5-13:** $I_d$ – $V_{SG}$ curves at high and low drain potentials for 7 × 10 SiNWs ($V_d$ = 50, 100 mV, 1 V) with and without $HfO_2$, $L$ = 2 µm, $d_{NW}$ = 25-40 nm.

It is clear from Figure 5-13 (7 × 20 SiNWs, $L$ = 2µm, 10 nm $HfO_2$ gate dielectric) that the deposition of the $HfO_2$ degrades the transistor characteristics of our devices. The $SS$ increases from ~ 100 mV/dec to ~ 150 mV/dec after the $HfO_2$ deposition. The threshold voltage also increases to > 3 V.

It has already been shown in literature that the deposition of $HfO_2$ directly on Si or native oxide degrades the transistor characteristics due to an increased number of dangling bonds [97] and charge trapping density at the Si-dielectric interface [28, 95, 96]. The formation of a higher quality $SiO_2$ interface layer (in comparison to native oxide) by thermal oxidation for example has been found to reduce such effects [28, 95, 96]. Also, the post-deposition thermal anneal (400 °C) in an oxidizing ambient has been found to reduce dangling bond type defects [97] and the trapping density can be drastically reduced at anneal temperatures of 600 °C [96]. Nonetheless, the fact that the

NWs are not released and available to dielectric deposition until the very end of the fabrication flow prohibits the use of processes that require temperatures above 380 °C (the degradation temperature of the SU-8 epoxy resist that protects the sensor from the liquid environment). This, together with the possible unstable process conditions of the ALD deposition, may degrade the transistor characteristics of our devices with $HfO_2$.

From Equation 5.4 one can see that the $SS$ is affected by the insulator dielectric constant $\varepsilon_r$ and the thickness $t_{ox}$ [125].

$$SS = \frac{kT}{q}\left(\frac{d(log_{10}I_d)}{dV_G}\right)^{-1} = 2.3\frac{kT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right)$$

**Equation 5.4**

For fully depleted devices, the depletion width $W_{dm}$ extends through the bulk of the semiconductor channel and the capacitance ratio $C_{dm}/C_{ox} \sim (\varepsilon_{si}t_{ox}/\varepsilon_r W_{dm})$ is relatively small reducing the $SS$. The calculated depletion width capacitance $C_{dm}$ here is ~ 9.65 nF/cm$^2$. The gate oxide capacitance when $SiO_2$ alone (assuming a native oxide thickness of 2 nm) is used as a dielectric was calculated to be > 1.5 times $C_{ox\text{-}SiO2}$ = 6.72 fF the value of that when $HfO_2$ is placed on top of the native oxide $C_{ox\ SiO2+HfO2}$ = 4.06 fF assuming a cylindrical concentric dielectric geometry for a single NW. This reduction of the gate oxide capacitance when 10 nm of $HfO_2$ is deposited on top of the native oxide around the NWs mostly accounts for the degraded subthreshold slope values.

Figure 5-14 shows the $I_d - V_{SG}$ curves for a device before and after the deposition of ALD $Al_2O_3$ (10 nm). Just as with the $HfO_2$ deposition the transistor characteristics of our devices degrade after the ALD deposition. Worth noting is the drastic threshold voltage increase from 2.3 V to 6.3 V. One thing to keep in mind as well is the fact that the dielectric is also being deposited on top of the side-gate electrodes as the ALD deposition is not selective. The coverage should decrease the effectiveness of the gate electrode though the liquid. This effect together with the reduced gate oxide capacitance serves to increase the threshold voltage shift greatly. Another thing to keep in mind is that when sweeping the Pt side-gate voltage it was noted through the Probe station's microscope that at potentials greater than 5 V (for electrolytes, > 10 V for IPA), bubbles start to appear most

likely due to reactions happening at the electrode's surface. This makes the use of alumina not reasonable for long term sensing operation being the $V_{th}$ so high for such devices.

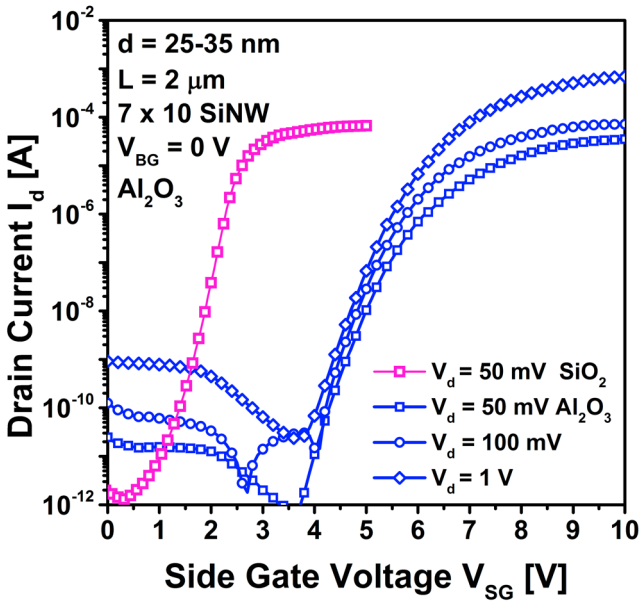



**Figure 5-14:** $I_d$ – $V_{SG}$ curves at high and low drain potentials for 7 × 10 SiNWs ($V_d$ = 50, 100 mV, 1 V) with and without $Al_2O_3$ ($V_d$ = 50 mV), $L$ = 2 μm, $d_{NW}$ = 25-40 nm.

## 5.4.7 Symmetric and asymmetric gating in a liquid environment

Figure 5-15 shows the $I_d$ – $V_{SG}$ with increasing $V_{BG}$, while keeping the $V_d$ = 50 mV constant for a 7 × 10 SiNWs structure. The configuration of the 3D vertically stacked sensor permits an enhanced electrostatic control of the SiNW channels by the possibility of applying symmetric or asymmetric gate potentials through the liquid IPA. In the dual gate configuration one gate acts as the tuning gate and the other as the driving gate of the FET. Figure 5-16a shows that as the $V_{BG}$ potential increases from 0 to 3 V the $V_{th}$ shifts towards the left (from ~ 2.24 V to ~ 0.13 V for 7 × 10 SiNWs). The $V_{th}$ changes the most when the tuning gate voltage is low ($V_{BG}$ < 1.5 V) and then remains almost unchanged for higher $V_{BG}$. As the $V_{BG}$ increases, the $I_d$ – $V_{SG}$ slope becomes steeper with the $SS$ decreasing (from ~100 mV/dec to the excellent value of ~ 75 mV/dec, for a 7 × 10 SiNW structure, $L$ = 2 μm), Figure 5-16b.

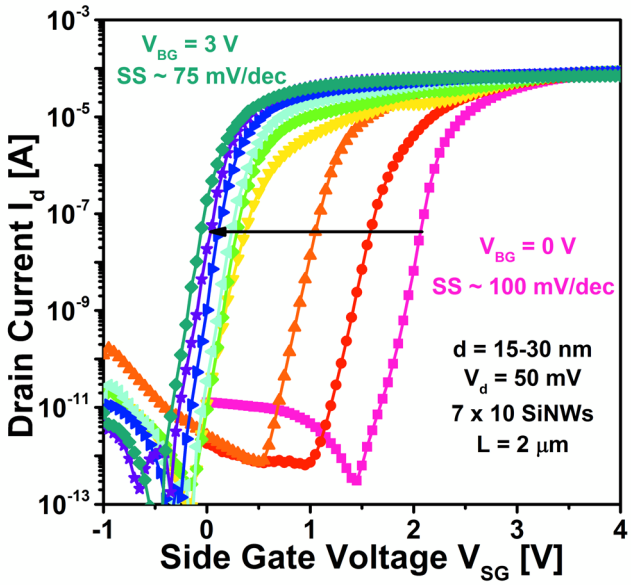



**Figure 5-15:** $I_d$ – $V_{SG}$ curves for different backgate potentials ($V_{BG}$ = 0 – 3 V) for a 7 × 10 SiNWs structure, $L$ = 2 µm, $d_{NW}$ = 15-30 nm, $V_d$ =50 mV, $SiO_2$ gate dielectric.

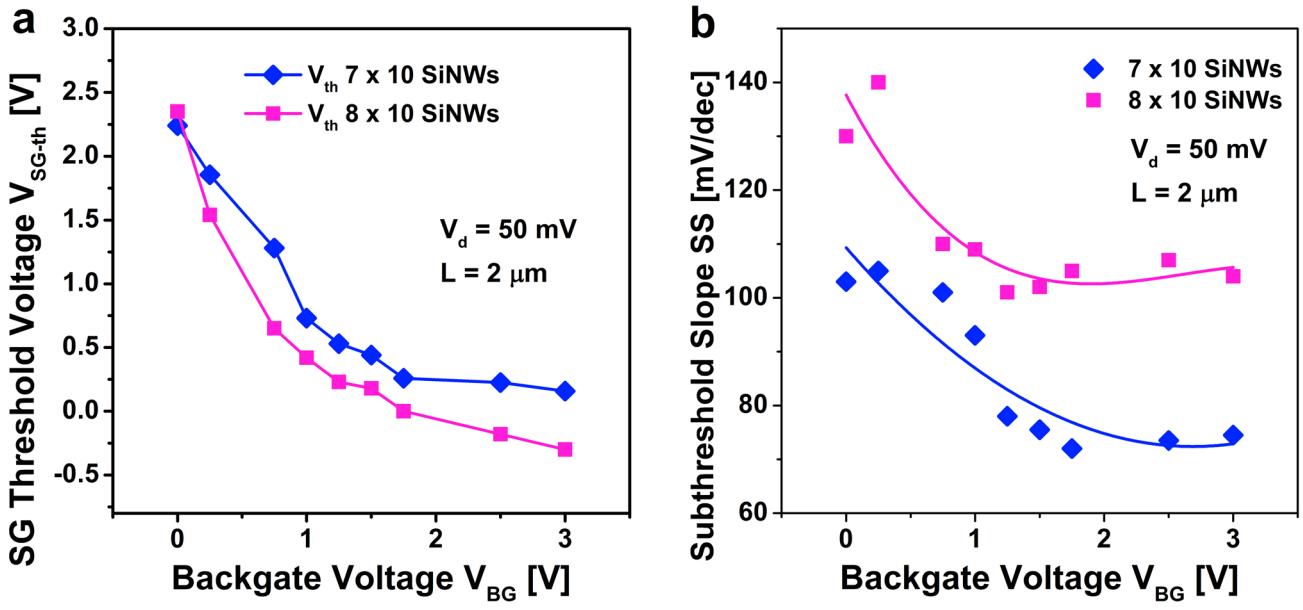



**Figure 5-16:** (a) $V_{th}$ from $I_d$ – $V_{SG}$ curves as the backgate voltage value increases from 0 to 3 V and (b) $SS$ from $I_d$ – $V_{SG}$ curves as the backgate voltage value increases from 0 to 3 V for a 7 × 10 and 8 × 10 NWs structure, $L$ = 2 µm, $V_d$ = 50 mV, $SiO_2$ gate dielectric.

The maximum transconductance $g_{m,max}$ values were extracted from the measured $I_d - V_{SG}$ curves as the backgate potential is increased are plotted in Figure 5-17. Though the transconductance values generally increase with increasing backgate voltages, they do not change significantly with backgate voltage at low drain bias potentials just as previously found in literature [131].

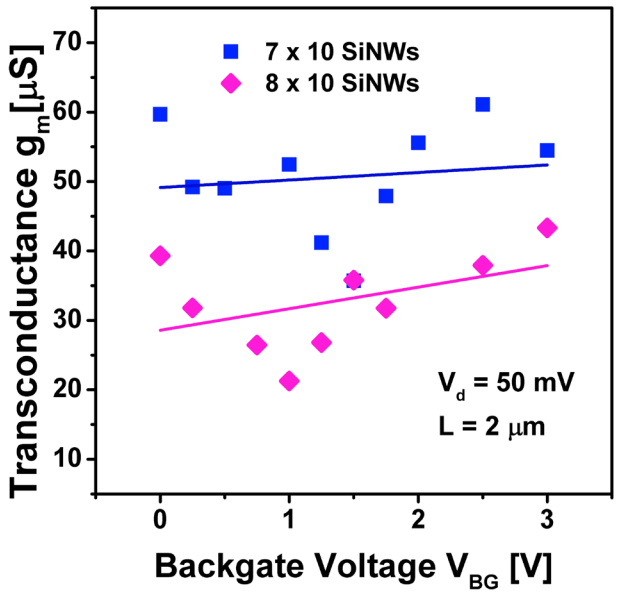



**Figure 5-17:** Extracted maximum transconductances from $I_d - V_{SG}$ curves as the backgate voltage value increases from 0 to 3 V for a 7 × 10 and 8 × 10 NWs structure, $L$ = 2 μm at low drain biases $V_d$ = 50 mV, tested in a liquid environment.

When a side-gate is used as a tuning gate and the backgate as the primary gate, a threshold voltage shift and subthreshold slope improvement are also observed in the $I_d - V_{BG}$ curves (Figure 5-18). The $V_{th}$ shifts to the left from 1.6 V to 1.1 V and the $SS$ decreases from ~ 106 mV/dec to ~ 77 mV/dec (7 × 10 SiNW structure, $L$ = 2 μm) as the $V_{SG}$ increases from 0 to 0.5 V. The coupling efficiency, typically defined by parameter $\alpha'$ as the ratio between the limiting $SS$ at room temperature (60 mV/dec) and the measured $SS$ ($\alpha' = 60\ mV/dec/SS_{measured}$), for the same tuning gate potential (0.5 V), can be compared when either the backgate or the side-gates are used as the primary gates. The backgate coupling when $V_{SG}$ = 0.5 V is $\alpha'$ = 0.8 in comparison to the side-gate coupling $\alpha'$ = 0.6 for the same tuning gate potential ($V_{BG}$ = 0.5). This, together with the lower threshold voltages val-

ues found when the backgate is used as the primary gate indicates a more efficient backgate coupling.

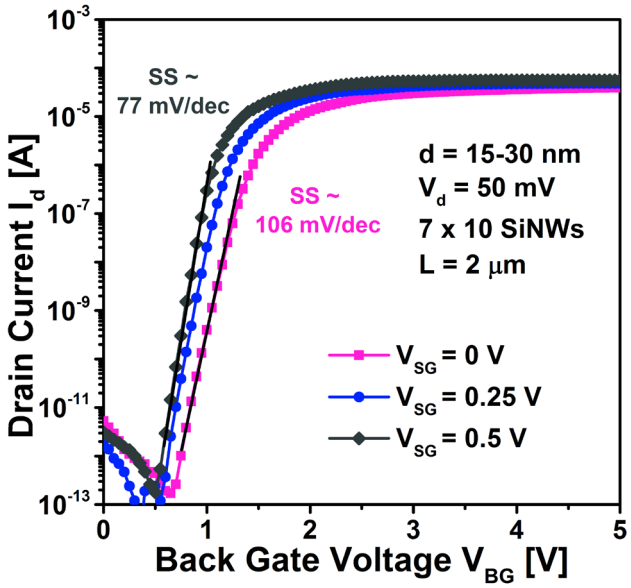



**Figure 5-18:** $I_d - V_{BG}$ curves for different side-gate potentials ($V_{SG}$ from 0 V to 0.5 V) for 7 × 10 SiNWs structure, $L$ = 2 µm, $d_{NW}$ = 15-30 nm, $V_d$ =50 mV, $SiO_2$ gate dielectric.

Figure 5-19 shows the drain current as one side-gate (single gate, $SG_1$) is swept while keeping the other one ($SG_2$) grounded ($V_{SG2} = V_S = V_{BG} = 0$ V) or two side-gates (double gate, DG) are swept simultaneously with the same potential (7 × 10 SiNW structure, $L$ = 2 µm, $V_d$ = 50 mV). The $V_{th}$ is reduced by 300 mV but in comparison to the asymmetric front-back gating it does not change/improve the subthreshold slope significantly. Figure 5-19 also shows the corresponding leakage currents measured from each side-gate (S to side-gate current) during the experiment. $I_{leak1(DG)}$ and $I_{leak2(DG)}$ denote the leakage current measured from each of the side-gates respectively as both are swept together. $I_{leak1(DG)}$ and $I_{leak2(DG)}$ almost coincide as the gates are symmetrical to the sides of the SiNWs. $I_{leak1(SG1)}$ and $I_{leak2(SG2)}$ denote the leakage current measured from each of the side-gates respectively, as one ($SG_1$) is swept ($V_{SG1}$) while keeping the other one ($SG_2$) grounded at $V_{SG2} = 0$ V. The side-gate leakage current was found to be low not increasing above 50 nA until after large side-gate potentials are utilized > 3 V. The drain current when the side-gate voltage is < 3 V is still almost 5 orders of magnitude greater than the side-gate leakage current.

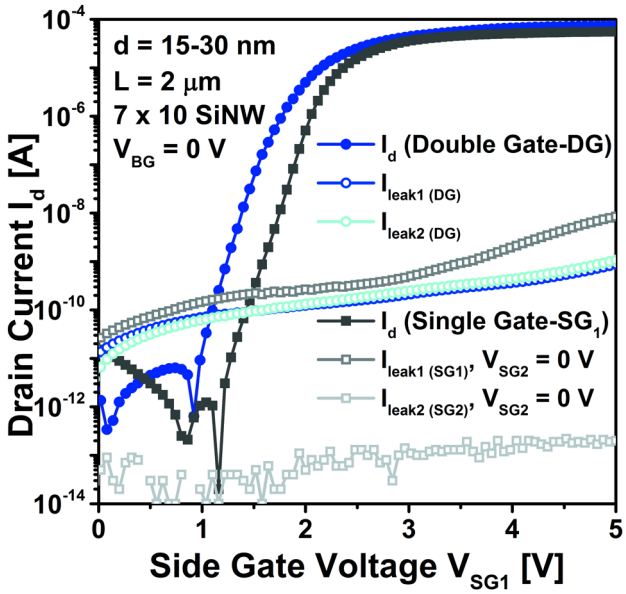



**Figure 5-19:** $I_d$, and side-gate leakage currents as either one (SG) of the side-gates are swept alone or both side-gates (DG) are swept together for a 7 × 10 SiNWs structure, $L$ = 2 µm tested in a liquid environment.

Figure 5-20 also shows the drain current when one side-gate is used as the tuning gate and the other as the primary gate.

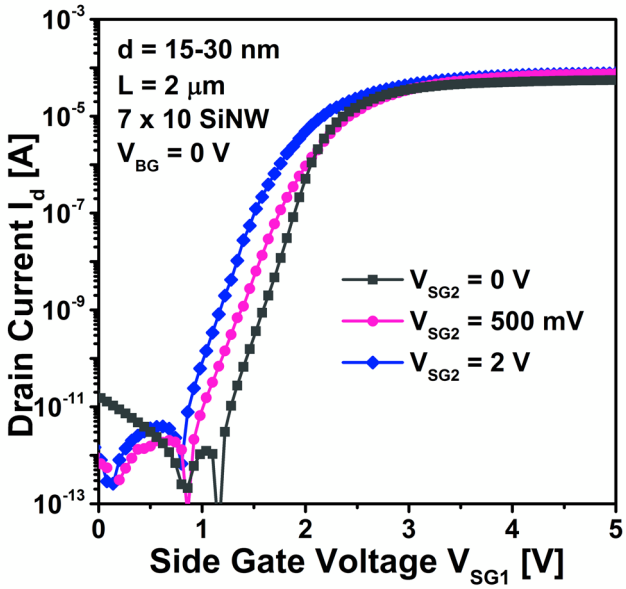



**Figure 5-20:** $I_d$ as one side-gate is swept ($SG_1$) and the other is kept constant ($SG_2$) for a 7 × 10 SiNWs structure, $L$ = 2 µm, $SiO_2$ gate dielectric.

It is clear from Figure 5-19 and Figure 5-20 that for both cases the $V_{th}$ shifts but in comparison to the asymmetric front-back gating it does not change/improve the subthreshold slope significantly.

The SU-8 sensing window is designed to be small to reduce side-gate coupling through the liquid to the source and drain anchors. Nevertheless, part of the source and drain anchors are exposed to the solution as well. Both, the backgate and side-gates can accumulate or deplete the source and drain as well. In particular, the backgate can not only influence the S/D indirectly through the liquid but directly as the structure sits on top of the BOX layer. Therefore, two competing effects happen as we apply a positive potential through any of the gates. First, an inversion channel that extends to the whole NW cross section can be easily formed. Second, as this potential is also felt at the source and drain, electrons can also be pulled away from the NW channels and towards the BOX oxide or S/D anchor surfaces as the potential increases. In traditional SOI based SiNW systems, the backgate capacitance $C_{BG}$ is dominated by the BOX layer and the solution gate capacitance $C_{LG}$ depends on the double layer capacitance of the solution $C_{dl}$ as well as on the native oxide capacitance [113]. Since the backgate in our system can also influence the SiNW gate channels through the solution, the double layer capacitance, native oxide capacitance and BOX layer capacitance all contribute to backgate capacitance and hence the higher backgate coupling efficiency.

When ideal bias conditions are utilized, it is possible to gate the stack of SiNWs through the liquid more efficiently from different sides in order to achieve low subthreshold slopes that translate to higher device sensitivities.

## 5.5 Transfer characteristics in an electrolyte

Finally, Figure 5-21 shows the $I_d - V_{SG}$ transfer characteristics ($V_d$ = 50 mV and 1 V) for a 7 × 10 SiNW structure with $L$ = 2 μm, $d_{NW}$ = 15-30 nm and native oxide as a gate dielectric measured in a buffered saline solution (PBS) with pH ~ 7.0 ($\varepsilon$ ~ 80). The *SS* decreases to the excellent value of 87 mV/dec and the $V_{th}$ shifts to 1.93 V (*vs.* 2.24 for device gated in IPA) as expected as the PBS has a higher dielectric constant. These *SS* values are comparable to the lowest subthreshold slope values reported in literature for electrolyte gated SiNW FET devices (~ 80 – 100 mV/dec) [21, 22, 28, 29].

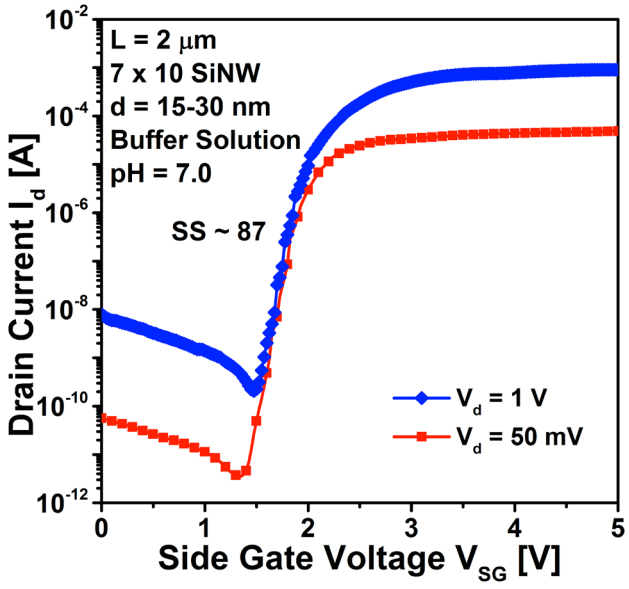



**Figure 5-21:** $I_d$ – $V_{SG}$ curves at high and low drain potentials for 7 × 10 SiNWs ($V_d$ = 50 mV, 1 V), $L$ = 2 μm, $d_{NW}$ = 15-30 nm, $SiO_2$ gate dielectric, tested in PBS (pH = 7).

One thing to keep in mind nevertheless, is that after several $I_d$ – $V_{SG}$ cycles when gating the devices with the Pt electrode through an electrolyte, the device starts turning black when observed through the prober's microscope and the device eventually becomes non-functional. Though platinum being a noble metal is inherently less sensitive to corrosion, it is clear that the side-gate electrode is reacting with the electrolyte. Such effect was not observed when isopropanol was used. It was also noted that bubbles started to appear as well at lower $V_{SG}$ voltages ~ 5 V (*vs.* ~ 10 V for IPA).

## 5.6 Summary

3D vertically stacked silicon nanowire field effect transistors featuring a high density array of fully depleted channels, varying number of NWs in the horizontal direction (10, 15 and 20 NWs) and different channel lengths ($L$ = 2, 3, 4 μm) featuring ultra-small SiNW diameters (down to $d_{NW}$ ~ 15 – 30 nm) have been successfully characterized electrically in a dry and a liquid environment for their implementation into a robust biosensing system. The channels can be surrounded by conformal high-$\kappa$ gate dielectrics ($HfO_2$ or $Al_2O_3$), and their conductivity can be uniquely con-

trolled by three gates; a backgate and two symmetrical Pt side-gates through a liquid, offering unique subthreshold slope tuning with high gate coupling. The main findings of this chapter are summarized here:

- Excellent low contact resistances were found after the thermal anneal. The contact resistance was found to contribute < 5% to the total electrical resistance. The linear $I_d - V_d$ characteristics suggest ohmic behavior.
- The transistor characteristics ($I_d - V_{SG}$) obtained for different devices within the same die when tested in a liquid environment were found to be comparable.
- The Pt electrodes were found to provide a stable contact when IPA is used to gate the vertically stacked device producing superimposable $I_d - V_{SG}$ characteristics.
- Little $I_d - V_{SG}$ hysteresis (< 15 mV) is found indicating small surface and interface ($Si/SiO_2$) defect induced charge trapping.
- The low doped SOI substrate and thin NW diameters reduce the drain leakage currents ($I_{off} < 10^{-6}$ mA/μm), for excellent $I_{on}/I_{off}$ ratios ($> 10^6$) in the $I_d - V_{SG}$ transistor characteristics.
- High maximum transconductance values $g_m > 10$ μS were found for all devices in the $I_d - V_{SG}$ characteristics.
- The *SS* values from the $I_d - V_{SG}$ curves were found to be steep *SS* < 100 mV/dec (7 × 10 SiNW structures with $d_{NW}$ = 15-30 nm) indicating excellent electrostatic control through the liquid.
- The ALD high-κ deposition (10 nm) increases the *SS* and induces a large $V_{th}$ shift. The gate oxide capacitance for $SiO_2$ (assumed to be 2 nm thick) alone was calculated to be > 1.5 times $C_{ox\text{-}SiO2}$ = 6.72 fF the value of that when $HfO_2$ is placed on top of the native oxide $C_{ox\ SiO2+HfO2}$ = 4.06 fF. This, together with the fact that the dielectric is also being deposited on top of the side-gate electrodes, effectively decreasing the effectiveness of the gate electrode though the liquid, results in an increased threshold voltage and degraded subthreshold slopes.

- The configuration of the 3D FET offers excellent electrostatic control of the SiNW channels by the possibility of applying symmetric or asymmetric gate potentials. High backgate coupling was found. As $V_{BG}$ increases, the $I_d - V_{SG}$ slope becomes steeper with $SS$ decreasing from ~100 mV/dec ($V_{BG}$ = 0 V) to the excellent value of ~ 75 mV/dec at $V_{BG}$ = 1.5 V (for 7 × 10 SiNW structures with $d_{NW}$ = 15-30 nm).

# Chapter 6 Sensor performance characterization

The sensor performance characterization experiments were carried out at room temperature under transient conditions. The 3D vertically stacked sensors were preliminarily characterized for pH and streptavidin sensing when gated by one of the local Pt side-gates. The main goal of this part of our work was to show proof-of principle operation and demonstrate that the PDMS microfluidic channel bonding and analyte-specific device functionalization methods were appropriate for this purpose. The structures were then fully characterized for pH and streptavidin detection with the use of an integrated reference electrode flow cell. Devices with a $SiO_2$ or $HfO_2$ gate dielectric that has been functionalized with APTES for pH sensing or left unmodified as will be described in this chapter. APTES can furthermore be used as a linker to biotin for streptavidin sensing.

## 6.1 Side-gated results

### 6.1.1 pH sensing with aminosilanized $HfO_2$ or $SiO_2$ gate dielectric

The drain current curves measured over time ($I_d - t$) as the pH value is changed from 4 to 10 for an array with 7 × 10 SiNWs, $L$ = 2 μm, $d_{NW}$ = 25 – 40 nm and with a $HfO_2$-APTES functionalized surface as the device is operated in the strong ($V_{SG}$ = 3.5 V) and weak inversion ($V_{SG}$ = 3 V) regime with, $V_d$ = 1 V are shown in Figure 6-1 and Figure 6-2. An intermediate flow rate of 100 μL/min (unless otherwise noted) is used in order to prevent PDMS microfluidic stamp popping and because higher flow rates deplete the solution supply too fast in all the sensing experiments unless otherwise noted. Figure 6-3 shows the drain current as a function of pH as extracted from the corresponding $I_d - t$ measurements. When the device is operated in weak inversion there is a large exponential change in the drain current with pH. In strong inversion the $I_d$ changes linearly with pH and the current levels are as well higher as anticipated. Nonetheless, even in strong inversion the measurement is noisy and generally the traces drift over time.

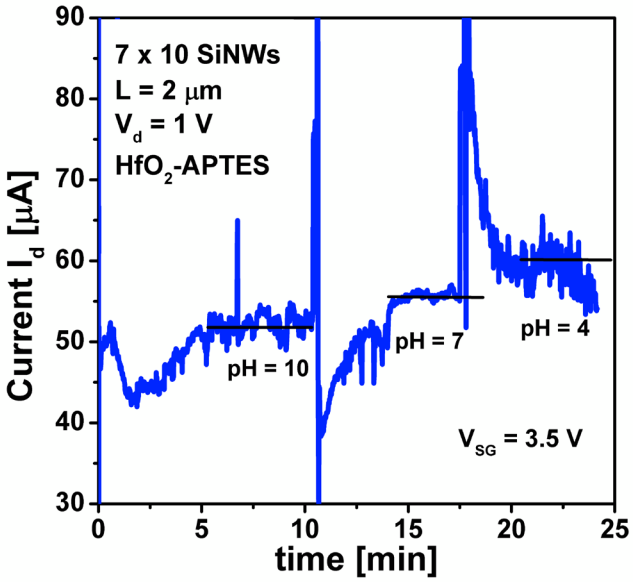



**Figure 6-1:** $I_d - t$ as the pH value is changed from pH = 4 to 10 for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm, $d_{NW}$ = 25 – 40 nm $V_d$ = 1 V and an $HfO_2$ gate dielectric as the device is operated in strong inversion $V_{SG}$ = 3.5 V.

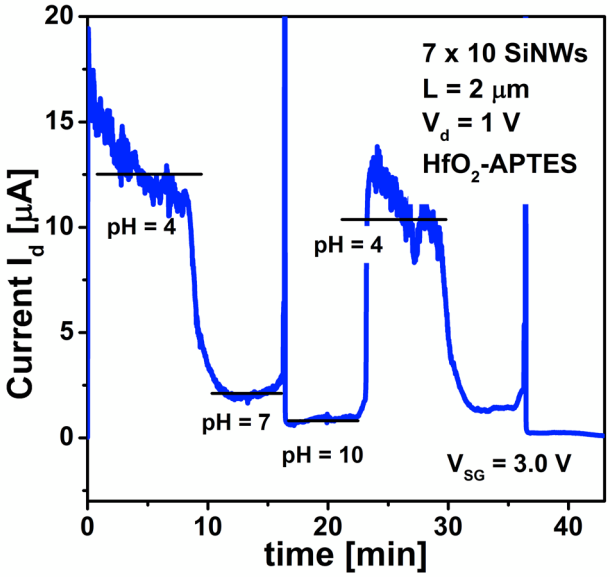



**Figure 6-2:** $I_d - t$ as the pH value is changed from pH = 4 to 10 for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm, $d_{NW}$ = 25 – 40 nm $V_d$ = 1 V and an $HfO_2$ gate dielectric as the device is operated in weak inversion $V_{SG}$ = 3.0 V.

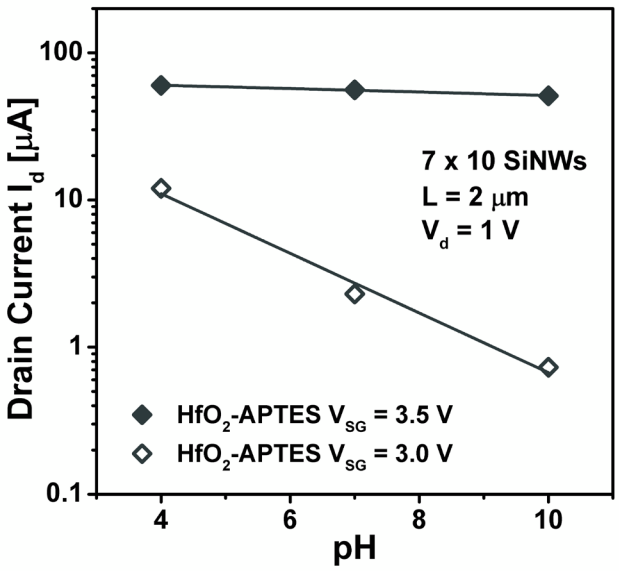



**Figure 6-3:** $I_d$ as the pH value is changed from pH = 4 to 10 for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm, $d_{NW}$ = 25 – 40 nm and an $HfO_2$ gate dielectric as the device is operated in the weak inversion ($V_{SG}$ = 3 V) and strong inversion ($V_{SG}$ = 3.5 V) regime, $V_d$ = 1 V.

The same type of device but with a silicon dioxide (APTES modified) gate dielectric was also measured in the strong inversion region ($V_{SG}$ = 3.5 V, Figure 6-4). The relative sensitivity $SR = (I_{d\psi 0} - I_{d\psi 1})/ I_{d\psi 0}$ with respect to the current measured at pH = 4 ($I_{d\phi 0}$ and $I_{d\phi 1}$ are the baseline current and the current induced by the sensing event respectively) is plotted in Figure 6-5 for the $SiO_2$ and $HfO_2$ gate dielectric structures when both are operated in strong inversion for comparison. As shown before in Section 5.4.6 of this thesis, the transistor characteristics degrade after the $HfO_2$ ALD deposition. In particular, the $SS$ increases that the $I_{on}$ current decreases after the $HfO_2$ deposition. For that reason, it is expected that when comparing the pH response of both devices when measured in the same operation regime for the current levels measured to be higher when $SiO_2$ alone is used and for the relative sensitivity to be high for this device as well as can be seen in Figure 6-4 and Figure 6-5.

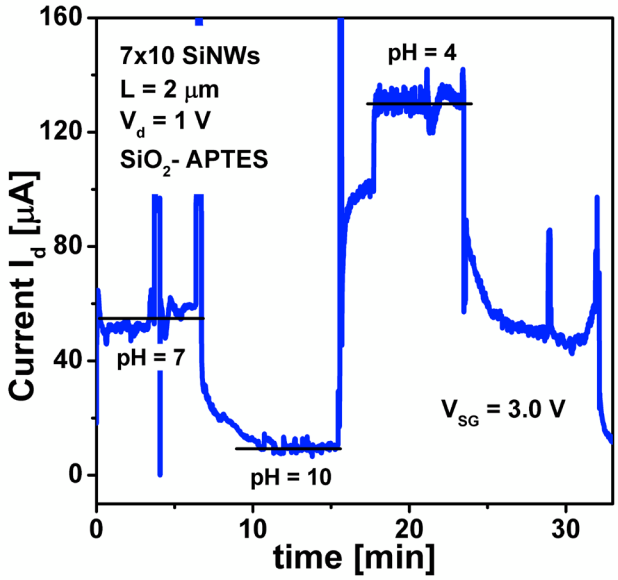



**Figure 6-4:** $I_d - t$ as the pH value is changed from pH = 4 to 10 for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm and a $SiO_2$ gate dielectric as the device is operated in the linear regime with $V_{SG}$ = 3 V, $V_d$ = 1 V.

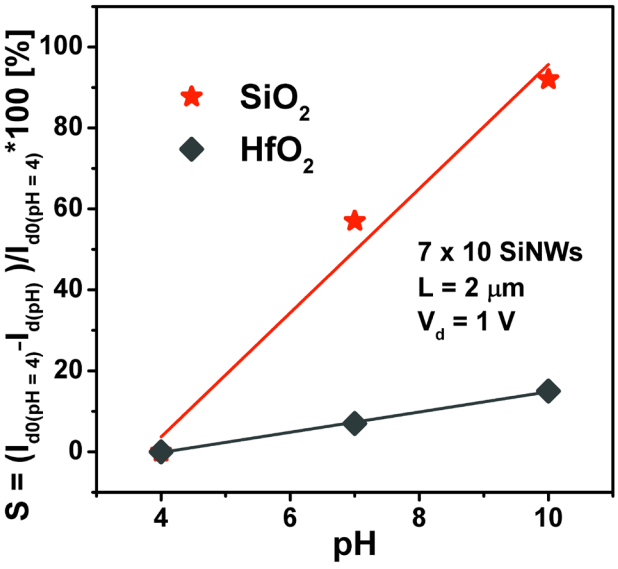



**Figure 6-5:** Relative sensitivity as a function of pH for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm and $V_d$ = 1 V with a $HfO_2$ or $SiO_2$ gate dielectric as the devices are operated in the strong inversion regime.

Long term studies of the pH sensing capabilities of the sensor structure when gated by the Pt side electrodes were not possible. As already mentioned in Section 5.5 of this thesis, it was noted that the Pt side-gate electrode is reacting with the electrolyte solution which leads to the eventual failure of the device. It has been found before in literature that such an electrode does not provide a stable reference with an electrolyte since the potential at the electrode/solution interface changes as a function of the composition and pH of the solution [105, 106]. Nonetheless, the use of the Pt electrode allowed us to quickly assess if the devices were functional or not and whether they had been affected or destroyed by the functionalization protocol. The APTES functionalization and subsequent microfluidic stamp attachment did not seem to compromise the performance of the devices. Also, no darkening of the sensor structure or reactions with the Pt electrode when gated by the isopropanol was observed. It was therefore possible to easily characterize our devices by simply placing a glass slide on top of the structures and gate them through IPA.

### 6.1.2 Streptavidin sensing with $SiO_2$ gate dielectric

We proceeded to test the response of biotin modified SiNWs to streptavidin. For the initial testing, with biotinylated devices we observed fluctuations in the drain current when carrying out measurements under transient conditions with the use of the Pt side-gates. We also noticed that the response of the device in static conditions did not suffer from the fluctuations observed under fluid flow. Therefore, it was decided to ascertain whether any response could be seen from a large administration of streptavidin.

Figure 6-6 shows the drain current measured as a function of time for an array with 7 × 10 SiNWs, $L = 2$ μm, diameter $d_{NW} = 15 - 30$ nm and a biotin-modified $SiO_2$ surface at low drain voltages ($V_d = 50$ mV) when operated in the subthreshold region $V_{GS} = 1.6$ V under certain conditions as will be described shortly.

A steady stream (150 μl/min) of PBS (pH = 7.4) was first injected into the dry microfluidic channel, which yielded a fluctuating signal on the order of a few μA. Drying the channel (the device still wet as verified by looking into the prober's microscope) with an injection of air at $t \approx 10$ min gave a smooth signal of approximately 0.3 μA. Flowing PBS again gave a fluctuating signal and subsequent administration of air gave a smooth response of approximately 1 μA. Having seen the signal

response under PBS flow and after air is introduced into the channel, 0.1 ml of a 0.4 μM solution of streptavidin in PBS was administered, followed by a flow of PBS which should remove any unbound streptavidin. Under the flushing flow of PBS there was no discernible change in signal magnitude compared to before the streptavidin administration as there is too much fluctuation in the drain current. On addition of air, however, the signal decreased sharply down to nA levels. Comparison of the response under air before and after streptavidin shows a difference in signal response of over two orders of magnitude, which indicates a positive and definite change following streptavidin administration. This preliminary experiment shows the functionality of nanowire sensor for the detection of streptavidin.

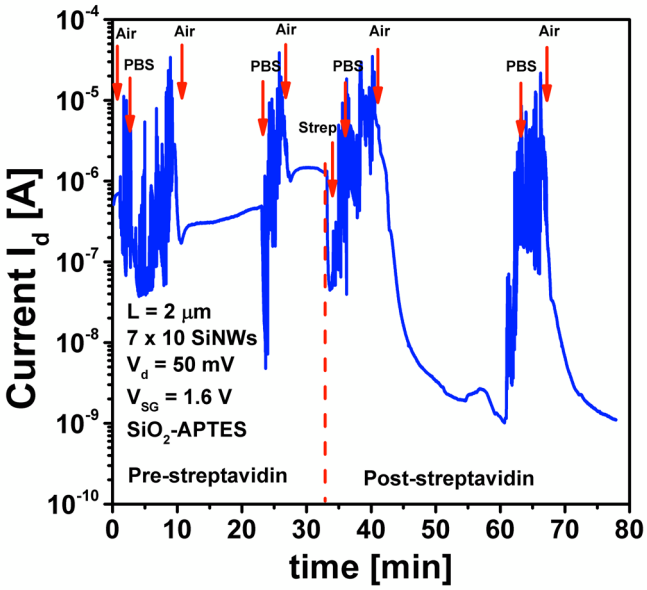



**Figure 6-6:** $I_d - t$ as the pH value is changed from pH = 4 to 10 as the device is operated in the subthreshold regime $V_{SG}$ = 1.6 V, $V_d$ = 50 mV for a biotin functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm, $d_{NW}$ = 15 – 30 nm and a $SiO_2$ gate dielectric.

## 6.2 Reference electrode results

As previously mentioned in the introduction of this chapter the devices were then fully characterized for pH and streptavidin sensing by gating the structures with a reference electrode integrated into a flow cell as the Pt gates do not provide a stable contact with the electrolyte solution.

### 6.2.1 pH sensing with aminosilanized surfaces

The drain current *vs.* reference electrode potential curves ($I_d - V_{Ref}$) for high and low drain voltages ($V_d$ = 50 mV, 1 V) as the pH value changes (pH = 4, 7, 10) for an array with 7 × 10 SiNWs and $L$ = 2 μm, $SiO_2$-APTES functionalized are shown in Figure 6-7.

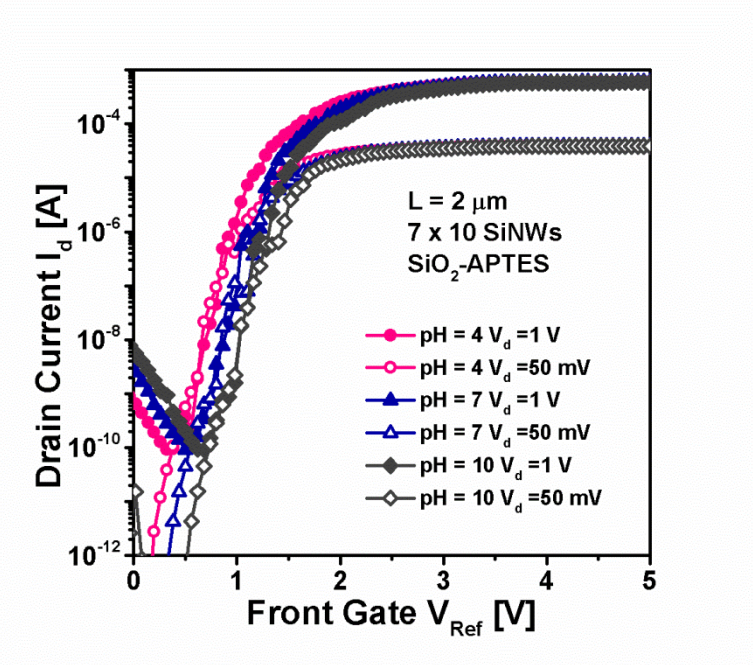



**Figure 6-7:** $I_d - V_{Ref}$ curves as the pH increases (pH = 4, 7, 10) for high and low drain potentials $V_d$ = 50 mV, 1 V for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm, $d_{NW}$ = 15 – 30 nm and a $SiO_2$ gate dielectric.

These curves are representative of all devices measured. The sensors exhibit excellent transistor characteristics. The drain-leakage current is defined as the $I_d$ at $V_{Ref}$ = 0 V. The $I_{on}$ current here is the value of $I_d$ at $V_{Ref}$ = 3 V (normalized to average NW diameter $d_{NW}$ = 30 nm). In terms of device performance the devices show low drain leakage currents $I_{off}$ < 20 × $10^{-6}$ mA/μm, high $I_{on}$ > 1 mA/μm currents and high $I_{on}/I_{off}$ ratios > $10^6$. Devices with subthreshold slopes $SS = d(V_{Ref})/d(log_{10}I_d)$ as low as 85 mV/dec were found with the average being 95 mV/dec. As expected for APTES functionalized devices [1, 21, 27, 29, 36, 86], the transfer characteristic curves shift linearly towards more positive values ($V_{Ref}$) with increasing pH without $SS$ degradation.

The average threshold voltage ($V_{Ref}$ when $I_d = (100\,\mu A * d_{NW}/L)$) shift $\Delta V_{th}$ per pH was estimated to be $\Delta V_{th}/pH$ ~ 50 mV/pH. High maximum transconductance values $g_{m,max}$ of ~ 50 μS (from $g_m = (dI_d/dV_{Ref})$ when $V_d$ = 50 mV) were extracted from the measured $I_d$ *vs.* $V_{Ref}$ curves. Transconductance values give a measure of the sensitivity to surface charges. The reported FET characteristics are among the best reported in literature for liquid-gated transistors as shown in Table 2-3 and Table 2-4 of this thesis [21, 22, 28, 29].

Continuous operation may be necessary for certain applications and therefore the electrical stability of the sensor over extended periods (> 1 hr.) of time is of paramount importance. The time dependent stability of the sensor was investigated by exposing the sensor to different pH buffer (pH = 4, 7, 10) solutions in repeated cycles (3) over time (~ 85 min). Figure 6-8 shows the drain current *vs.* time as the device is operated in the subthreshold regime ($V_{Ref}$ = 1.25 V, $V_d$ = 1 V). Clear signal steps are observed as the pH value changes. A high quasi-exponential drain current response ($\Delta I_d/pH$) of up to ~ 0.70 dec/pH is obtained in the subthreshold regime for this device. The average response time $t_R$, defined as the time required to reach 90% of the response signal was in average below 60 s. The temporary flow rate fluctuations resulting from the brief disturbance that happens during syringe switching can be observed as repeatable spikes in the $I_d - t$ traces. This is because flow rate fluctuations can induce changes in the streaming potential at the gate oxide surface [132]. These fluctuations are particularly evident when the device is operated in the subthreshold and weak inversion regimes. As it is indicative from this jump, it takes about 250 seconds for the solution to reach the SiNW structure as it travels through the tubing.

Figure 6-9 shows the drain current as a function of pH as extracted from the corresponding $I_d - t$ measurements from the subthreshold $V_{Ref}$ = 1, 1.25 V, weak inversion $V_{Ref}$ = 1.5 V and strong inversion $V_{Ref}$ = 3 V regimes. Good reproducibility of the measured sensor drain current and stability over time is found. Though the drain current drifts slightly downwards after each cycle the sensor response has been shown to be reproducible and the drift to be < 10 % of the average current at each pH value tested.

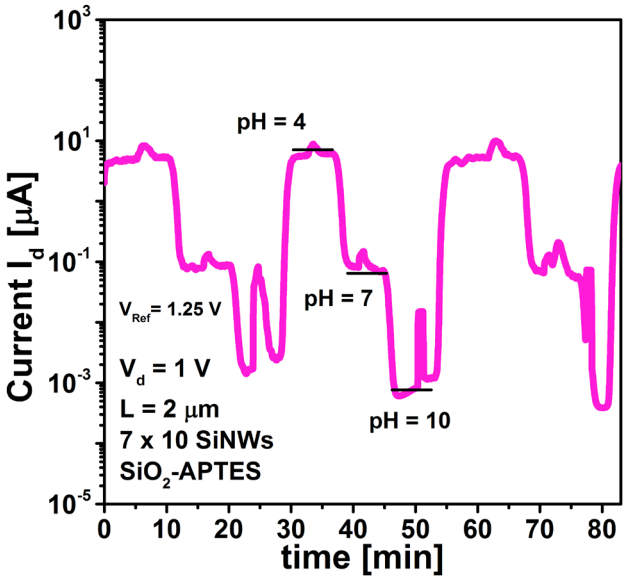



**Figure 6-8:** $I_d$ – $t$ as the pH value is changed from pH = 4 to 10 as the device is operated in the subthreshold regime for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 µm, $d_{NW}$ = 15 – 30 nm and a $SiO_2$ gate dielectric.

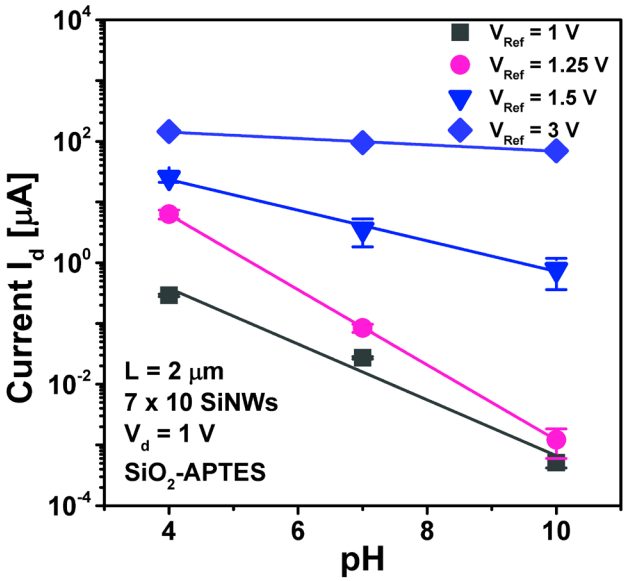



**Figure 6-9:** $I_d$ – pH as the pH value is changed from pH = 4 to 10 as the device is operated below threshold $V_{Ref}$ = 1, 1.25 V and in weak inversion $V_{Ref}$ = 1.5 V and strong inversion $V_{Ref}$ = 3 V for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 µm, $d_{NW}$ = 15-30 nm and a $SiO_2$ gate dielectric.

When the device is operated in strong inversion the $I_d$ changes linearly with pH and the current levels are as well higher as expected (Figure 6-10). Not surprisingly, larger relative current changes with pH are found when the device is operated in the subthreshold regime.

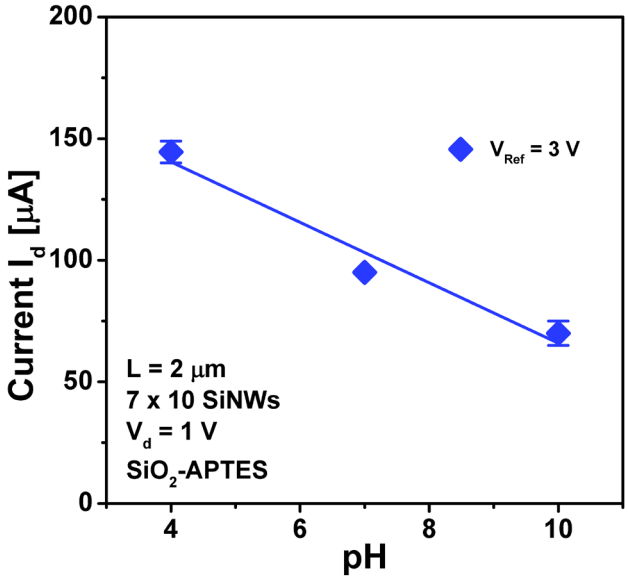



**Figure 6-10:** $I_d - pH$ as the pH value is changed from pH = 4 to 10 for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm, and a $SiO_2$ gate dielectric as the device is operated in strong inversion $V_{Ref}$ = 3 V plotted in a linear scale (Figure 6-9).

$I_d - pH$ for different devices within the same die was measured as the number of NWs increases as shown in Figure 6-11a. The drain current changes consistently vary with pH with the levels increasing as the number of NWs increase. The devices show reproducible large responses to changes to/from acidic and basic media. The sensor response among different devices within the same die is repeatable for the full range of operation from subthreshold to strong inversion as can be also seen in Figure 6-11b for a structure with 7 × 15 SiNWs, $L$ = 2 μm.

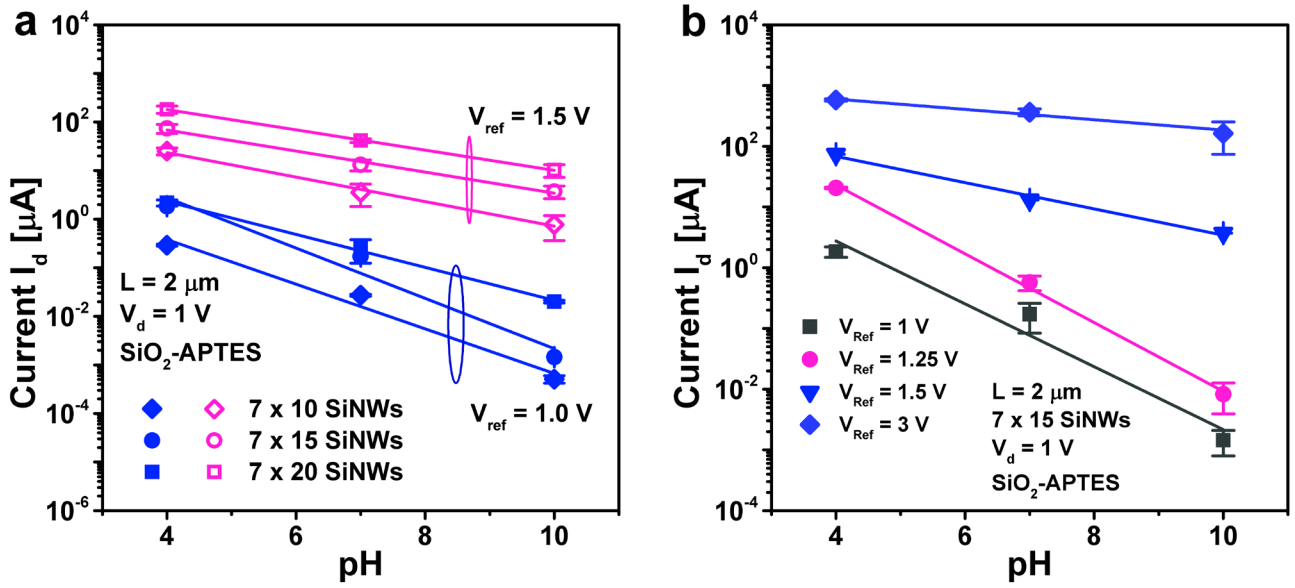



**Figure 6-11:** (a) $I_d$ – $pH$ for structures with increasing number of SiNWs 7 × 10, 15, 20µm as the device is operated in subthreshold and weak inversion $V_{Ref}$ = 1, 1.5 V, respectively and (b) $I_d$ – pH as the device is operated below threshold $V_{Ref}$ = 1, 1.25 V and in weak inversion $V_{Ref}$ = 1.5 V and strong inversion $V_{Ref}$ = 3 V for 7 × 15 SiNWs array. Devices are APTES functionalized, have channel lengths $L$ = 2 µm, $d_{NW}$ = 15 – 30 nm and a $SiO_2$ gate dielectric.

## 6.2.2 pH sensing with unmodified $SiO_2$ surfaces

The drain current *vs.* pH for a $SiO_2$ - not functionalized array with 7 × 10 SiNWs and $L$ = 4 µm operated in the subthreshold regime is shown in Figure 6-12. The corresponding $I_d$ – $pH$ for different operation regimes ($V_{Ref}$ = 1, 1.25, 1.5, 3 V) for the same structure is also shown in Figure 6-13. In comparison to APTES modified devices the drain current does not change linearly as a function of pH. This is consistent with literature results for SiNWs with unmodified $SiO_2$ gate insulators [1, 21, 27, 36, 86]. Small $I_d$ changes with pH near the point of zero charge of bare $SiO_2$ ($pH_{pzc}$ ~ 2), and large $I_d$ changes with pH above pH > 5 (making the full pH sensing range (2 – 12) non-linear) have been found before in literature [1, 86].

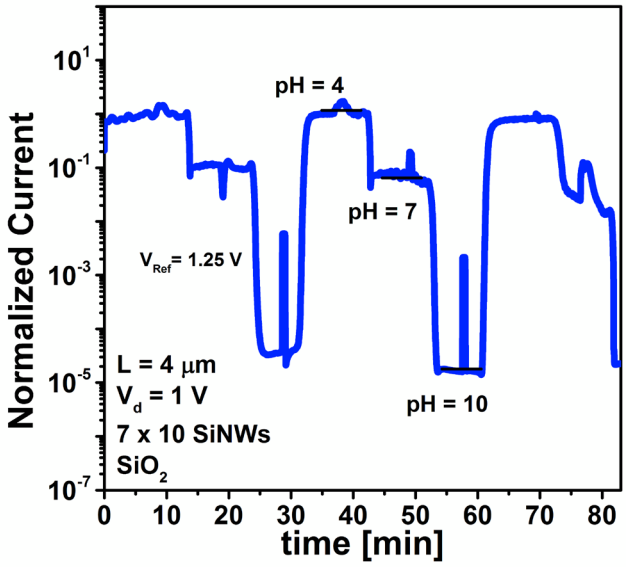



**Figure 6-12:** (a) $I_d$ – $t$ as the pH value is changed from pH = 4 to 10 as the device is operated in the subthreshold regime $V_{Ref}$ = 1.25 V, $V_d$ = 1 V for an unmodified $SiO_2$ structure with 7 × 10 SiNWs, $L$ = 4 µm, $d_{NW}$ = 15-30.

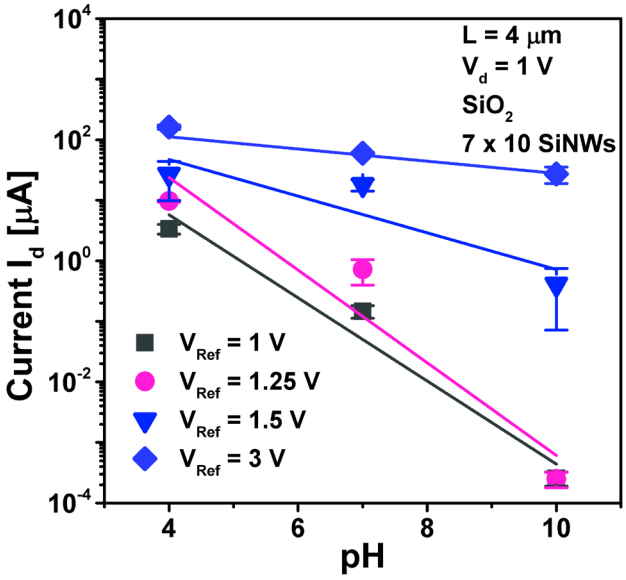



**Figure 6-13:** $I_d$ – pH as the pH value is changed from pH = 4 to 10 as the device is operated below threshold $V_{Ref}$ = 1, 1.25 V and in weak inversion $V_{Ref}$ = 1.5 V and strong inversion $V_{Ref}$ = 3 V for an unmodified $SiO_2$ structure with 7 × 10 SiNWs, $L$ = 4 µm, $d_{NW}$ = 15-30.

### 6.2.3 Robust and long term operation

The robustness and mechanical stability of the vertically stacked array has already been investigated by applying vertical load forces up to 100 nN by an atomic force microscopy probe as shown in Section 3.6.2 of this thesis. Nonetheless, it was important to verify that the structures could withstand a certain amount of stress and handling outside of a lab environment and still remain functional after some days. Figure 6-14 shows the normalized (divide by maximum value) drain current *vs.* pH as the device is operated in the weak and strong inversion regime ($V_{Ref}$ = 1.5, 3 V, $V_d$ = 1 V) before and after the device was dropped one meter away from the ground. The responses were found to be comparable and reproducible.

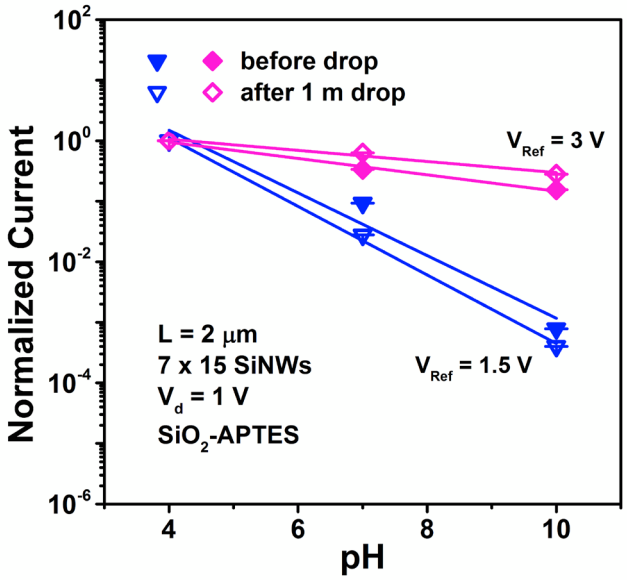



**Figure 6-14:** Normalized $I_d$ – $pH$ response before and after a one meter drop from the ground for an APTES functionalized a structure with 7 × 15 SiNWs, $L$ = 2 µm, and a $SiO_2$ gate dielectric as the device is operated in weak and strong inversion $V_{Ref}$ = 1.5, 3 V, respectively.

The long term stability was also explored by measuring the sensor response with respect to pH 10 days after the initial measurements. Figure 6-15 and Figure 6-16 are shown as examples when a device is operated in weak and in strong inversion, respectively. The measurements are repeatable and generally overlap. Long term stability and repeatability was achieved due to the robust fabrication process and in particular due to the robust SU-8 insulator layer protecting the device.

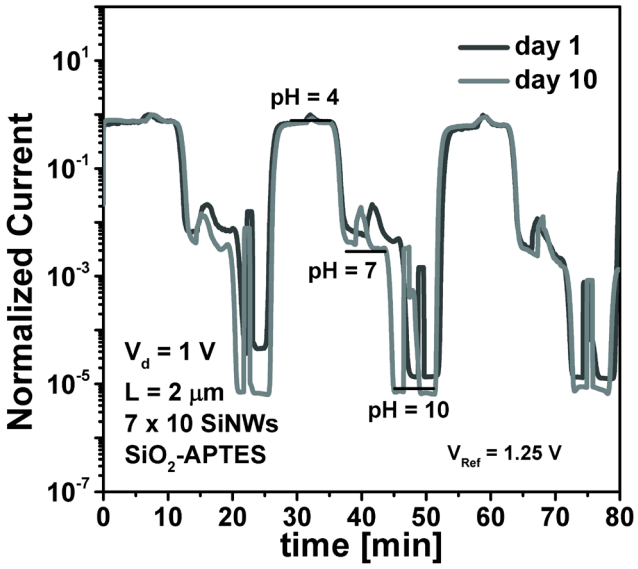



**Figure 6-15:** (a) $I_d$ – $t$ as the pH value is changed in cycles (3) from pH = 4 to 10, $V_d$ = 1 V in the subthreshold regime at high drain voltage potentials $V_d$ = 1 V and 10 days after the first measurement for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm.

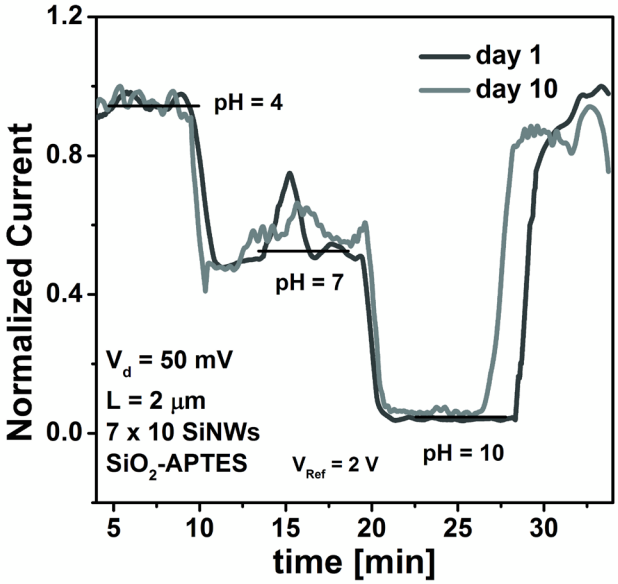



**Figure 6-16:** $I_d$ – $t$ as the pH value is changed and the device is operated in strong inversion at low drain voltage potentials $V_d$ = 50 mV and 10 days after the first measurement for an APTES functionalized structure with 7 × 10 SiNWs, $L$ = 2 μm.

The device shows reproducible large responses (up to 0.8 dec/pH in subthreshold) in the subthreshold and strong inversion (~ 5 µA/pH) regime.

The long term reliability for a $SiO_2$ - not functionalized array was as well tested by measuring the sensor response 10 days after the initial measurements. Figure 6-17 shows the $I_d - pH$ characteristics as the device is operated in strong inversion ($V_{Ref}$ = 2 V) at high and low drain potentials ($V_d$ = 50 mV, 1V) for an non-functionalized 7 × 10 SiNWs structure with $L$ = 2 µm. The measurements were as well found to be are repeatable and generally overlap.

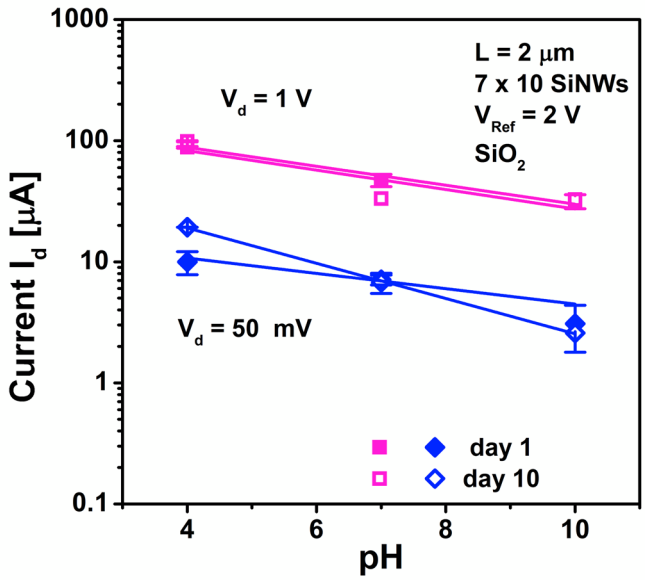



**Figure 6-17:** $I_d - t$ as the pH value is changed from pH = 4 to 10 as the device is operated in the strong inversion $V_{Ref}$ = 2 V at high ($V_d$ = 1 V) and low ($V_d$ = 50 mV) drain potentials and 10 days after the initial measurement for an unmodified $SiO_2$ structure with 7 × 10 SiNWs, $L$ = 4 µm, $d_{NW}$ = 15 – 30.

## 6.2.4 Streptavidin sensing

Biotinylated sensor structures have been characterized for streptavidin sensing with the use of the integrated reference electrode. Figure 6-18 shows the drain current response over time at constant operating conditions (in strong inversion, $V_{Ref}$ = 2 V, $V_d$ = 50 mV) as 100 µL of solutions with increasing concentrations of streptavidin (520 aM – 420 fM in PBS, pH = 7.4) are introduced and subsequently washed away by a PBS flow to remove any left-over unbound streptavidin molecules

(for a structure with 7 × 10 SiNWs, $L$ = 4 μm and $SiO_2$ biotinylated surface). The strong streptavidin-biotin interaction guarantees that only weakly bound or excess streptavidin molecules are washed away by the successive PBS flow.

Figure 6-19 similarly shows the $I_d - t$ sensor response for another structure (with 7 × 10 SiNWs and $L$ = 3 μm) as even lower concentrations are being measured (17 aM – 420 fM) and the device is operated in the subthreshold region ($V_{Ref}$ = 1.5 V, $V_d$ = 50 mV). A negligible decrease in the drain current is observed when a PBS blank (control) is introduced at (at $t$ ~ 5 min for the first structure and at $t$ ~ 12 min for the second structure, Figure 6-18 and Figure 6-19, respectively) for both devices indicating that the flow conditions associated with the injection do not affect the measurement and that the syringe and injection ports had not been contaminated with streptavidin from previous testing. When the first streptavidin binding at ultra-low concentrations (520 aM at $t$ ~ 8 min and 17 aM for the first and second device at $t$ ~ 17 min, respectively) a large (> 500 nA) clear drop in current is observed. 17 aM is the lowest concentration of streptavidin ever reported in literature to be sensed by a FET-based sensor without other means of pre-concentrating the solution [1, 14-17].

The response time $t_R$ was found to be again under a minute reaching the full sensor response within 4 minutes and therefore no mass transport limitations are found. Subsequent solution additions with increasing streptavidin concentrations reveal a continuous stepwise decrease in the current response up to a concentration of 420 pM. For each concentration introduced a drain current change is observed until the device saturates and either the drain current level does not change any further or momentarily drops. The functionalized SiNW surface may be fully coated with protein and therefore the sensor response saturates beyond the picomolar range for the structures measured.

It is important to keep in mind that the APTES/biotin surface modification does not only happen at and around the array. A large surface area outside of the SiNW region may have also been biotin modified [133]. Though the microfluidic channel reduces the interaction area, target molecules may still bind with surrounding receptor molecules prior to reaching the sensor structure, reducing the analyte target molecule concentration [16].

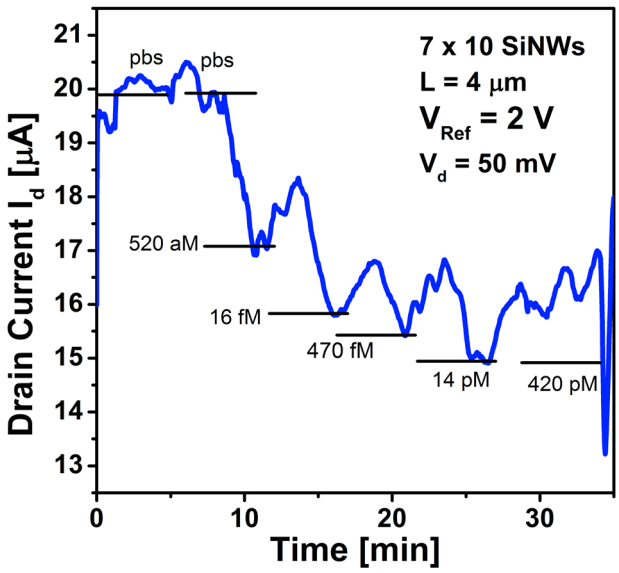



**Figure 6-18:** $I_d - t$ as increasing concentrations of streptavidin in PBS solutions are administered for a structure with 7 × 10 SiNWs, $L$ = 4 μm as the device is operated in strong inversion regime $V_{Ref}$ = 2 V, $V_d$ = 50 mV.

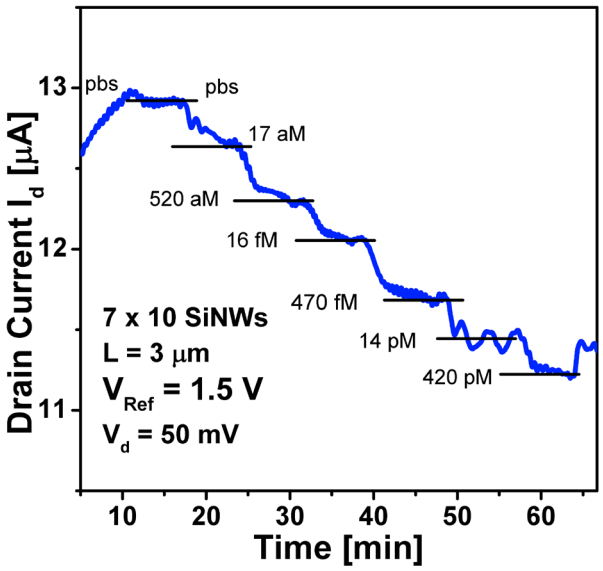



**Figure 6-19:** $I_d - t$ as increasing concentrations of streptavidin in PBS solutions are administered for a structure with 7 × 10 SiNWs, $L$ = 3 μm as the device is operated in the weak inversion regime $V_{Ref}$ = 1.5 V, $V_d$ = 50 mV.

It is also important to remember that there is a limited time in which the streptavidin can actually bind to the sensor structure as the remainder unbound streptavidin is immediately washed away by PBS. This indicates in fact that much lower streptavidin concentrations are possible to be detected with our biosensor system.

Figure 6-20 shows the corresponding $I_d - V_{Ref}$ characteristic before and after the experiment for the latter device with 7 × 10 SiNWs and $L$ = 3 µm. The $I_d - V_{Ref}$ characteristics before and after the experiment (Figure 6-20) are noticeably different, with the threshold voltage increasing consistent with the streptavidin binding to the device (as mentioned above, streptavidin protein is negatively charged at pH = 7.4).

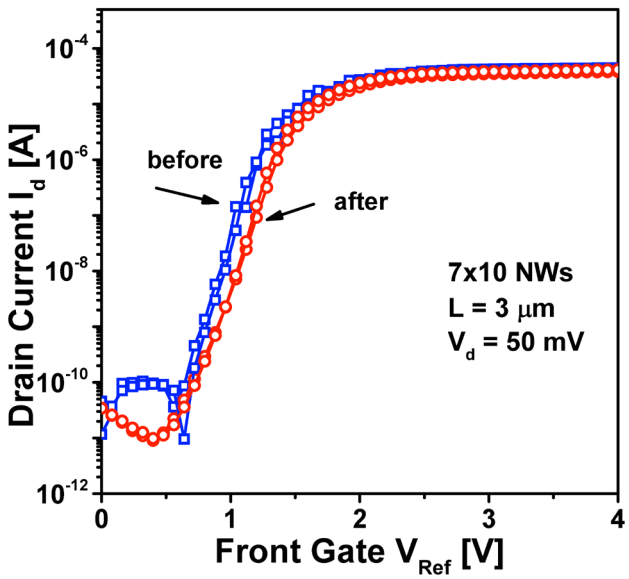



**Figure 6-20:** $I_d - V_{Ref}$ for a biotinylated structure with 7 × 10 SiNWs and $L$ = 3 µm before and after the streptavidin in PBS solutions were administered ($V_{Ref}$ = 1.5 V, $V_d$ = 50 mV).

## 6.3 Summary

A 3D vertically stacked silicon nanowire field effect transistor has been successfully demonstrated as a highly robust and sensitive pH and streptavidin sensor for the first time, this being the main contribution of this thesis' work. The SOI fabricated structures featuring a high density array (up

to 7 × 20 SiNW) of fully depleted channels, varying number of NWs in the horizontal direction (10, 15 and 20 NWs) and different channel lengths (2, 3, 4 μm) were effectively characterized:

- The excellent FET performance characteristics (average subthreshold slopes $SS$ ~ 95 down to 85 mV/dec, leakage currents $I_{off} < 2 \times 10^{6}$ mA/μm, normalized to $d_{NW}$ = 30 nm, high $I_{on}/I_{off}$ ratios > $10^{6}$) and efficient functionalization lead to high pH sensor responses.

- The average threshold voltage shift $\Delta V_{th}$ per pH was estimated to be ~ 50 mV/pH for APTES functionalized $SiO_2$ dielectric devices. High (up to 0.8 dec/pH), long term and reproducible pH sensing responses were also shown with APTES modified and unmodified $SiO_2$ sensor surfaces when the device is operated in the subthreshold regime. High drain current responses > μA/pH were measured in the strong-inversion region.

- The continuous operation of the device for pH sensing over extended periods (> 1 hr.) of time was demonstrated with good reproducibility of the measured sensor drain current and stability over time.

- The drain current drift was found to be < 10 % of the average current at each pH value tested. The responses were found to be comparable and reproducible over time and after the structures have been stressed by being dropped one meter away from the ground revealing a robust structure.

- The detection of ultra-low concentrations (down to ~ 17 aM) of the protein streptavidin was furthermore shown with a biotinylated $SiO_2$ gate dielectric device. To our knowledge this is one of the lowest protein concentrations ever measured by SiNW-based FET sensors without the use of pre-concentrating methods.

# Chapter 7 Low cost vertically stacked sensor

A big driver for the successful introduction of SiNW FET structures into the biosensor market is the low cost manufacture of such devices using conventional mass production CMOS/MEMS compatible processes. As previously mentioned, the use of costly SOI substrates and complicated epitaxial layered fabrication methods have been the most typically used approaches used in literature for producing stacked devices. Their fabrication with the use of inexpensive bulk-Si wafers has therefore been considered here.

## 7.1 Bulk fabricated SiNW FETS

The fabrication of vertically stacked Fins and NW structures in bulk-Si (without the use of epitaxy layers) for their application on integrated circuit (IC) systems has been explored before with mixed or unclear results [76]. For example, due to the S/D diffusion doping utilized during the proposed process flow by Bopp *et al*. [76, 134] for fabricating vertically stacked Fins, the resulting parasitic transistor dominates the electric characteristics of the device. This choice of contact doping causes the ineffective isolation of the Fins/NWs from the bulk and in overall the performance of the transistor is degraded. Ng. *et al*. [77] on the other hand achieved vertically stacked GAA devices (3 channels) with excellent transistor characteristics ($SS$ = 62 mV/dec, $I_{on}/I_{off}$ ratio of $10^8$) but the contribution to the $I_d - V_G$ curves of the parasitic conduction underneath the SiNWs through the bulk-Si is not discussed in the publication.

The fabrication of a vertically stacked device for biosensor applications had never been presented before in literature by any fabrication means or in any substrate (bulk or SOI) to the author's knowledge. Even examples of single level SiNWs (single or arrays) fabricated on bulk-Si by top-down CMOS compatible methods and implemented as FET biosensors are scarce [114, 135, 136]. Table 7-1 shows the few examples that exist in literature (to the author's knowledge) for SiNW FET biosensors fabricated in bulk silicon by a top-down approach. It is worth noting that Ahn *et al.* [135] performed a high dose boron channel-stop implantation to suppress the leakage current

through the buried substrate and placed two polysilicon side-gates to the side of the Fin. For further isolation from the buried substrate they formed a shallow trench isolation oxide hence the low $I_{off}$ currents achieved.

**Table 7-1:** State-of-the-art literature results for SiNW-FET based biosensors fabricated by top-down processes in bulk silicon.

| Description | Substrate fabrication | Dimensions | Gating | Transistor performance Current levels | Remarks | Ref. |
|---|---|---|---|---|---|---|
| Fin Array | Bulk Top down | H = 65 – 120 nm W = 18 – 40 nm L = 8 – 12 µm | RE | $\Delta V_{th}$/pH = 58 mV/pH SS ~ 300 mV/dec $I_{on}/I_{off}$ ~ $10^4$ ~nA/pH pH = (3 – 10) $I_{off}$ ~ 0.1 nA | $HfO_2$ surface not modified | Rigante *et al.* [136] |
| Single SiNW | Bulk Top down | NA | Poly-si SGs to sides of SiNW | SS ~ 400 mV/dec $I_{off}$~ pA $I_{on}/I_{off}$ ~ $10^4$ | -$SiO_2$ surface not modified -Channel-stop implantation used sto supress leakage current | Ahn *et al.* [135] |
| Polysilicon NW | Bulk Top down | W = 40 nm L = 10 µm | DG: BG SG | $\Delta V_{th}$/pH = 110 mV/pH SS = 450 mV/dec | -$SiO_2$ surface not Modified -$\Delta V_{th}$/pH amplified by DG configuration | Chen *et al*. [114] |
| **Vertically stacked SiNWs** | **Bulk Top down** | **$d_{NW}$ = 15 – 30 nm L = 10 µm** | **RE** | **SS = 160 mV/dec $I_{on}/I_{off} > 3 \times 10^4$ $I_{off}$ ~ 20 nA** | **-$SiO_2$ surface biotin modified -tested on PBS** | **This work** |

## 7.2 The vertically stacked bulk sensor

### 7.2.1 Transistor characteristics

Figure 7-1 shows the $I_d - V_{Ref}$ curves with increasing drain potential ($V_d$ = 50, 100, 1 V) for a vertically stacked SiNW structure (7 × 15 SiNWs and $L$ = 2 μm, biotinylated and tested in a PBS solution) fabricated in bulk and the parasitic MOSFET characteristics determined from an equivalent device for which the NWS are purposely not present. It is clear from Figure 7-1 that the current passing through the SiNWs is dominant with the parasitic current being several orders of magnitude less than the drive current of the entire device.

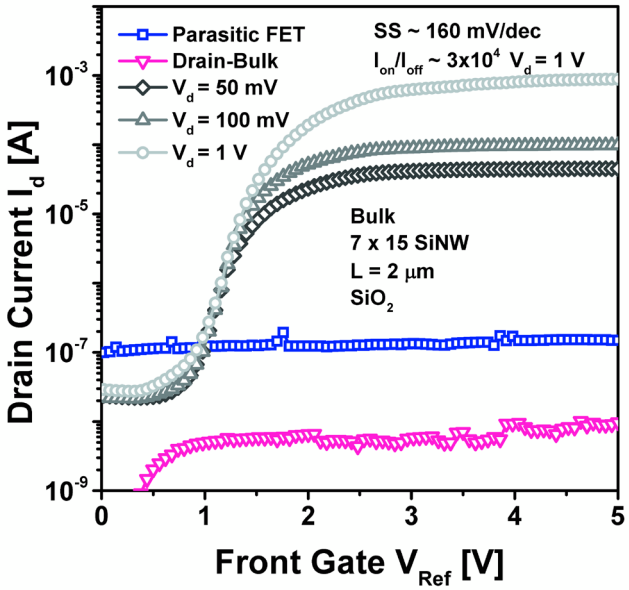



**Figure 7-1:** $I_d - V_{Ref}$ for a biotinylated structure with 7 × 15 SiNWs, $L$ = 2 μm and fabricated in bulk-Si in PBS solutions for different drain voltage potentials $V_d$ = 50, 100 mV, 1 V).

Leakage current does not only occur from the source to the drain through the liquid but as well through the parasitic MOSFET underneath the SiNWs. The leakage current passing through the parasitic MOSFET can be suppressed to a certain extent by the smart design of the vertically stacked device. In here, the correct determination of the *S*/*D* implantation parameters provides adequate isolation between the bulk and the bottom of the anchor pads, sufficiently suppressing the parasitic MOSFET conduction and resulting still high $I_{on}/I_{off} > 10^4$ ratios ($V_d$ = 1 V). Nonetheless,

the $I_{off}$ is still dominated by the leakage current passing through the parasitic MOSFET. One possible solution for future implementations would be to stack more NWs than the implantation can reach. This way the nanowires themselves would act as resistive paths for electron conduction. Also the distance electrons would have to travel from the bottom of the implantation pocket to the bulk-Si at the bottom of the trench would increase and the $I_{off}$ current could possibly decrease further. The bulk devices offer high $I_{on}/I_{off} > 10^4$ ratios and subthreshold slopes as low as 160 mV/dec without using any particular modification to the fabrication process to that implemented on SOI wafers. They have therefore great potential as a cheap alternative to the proposed sensing system proposed here.

## 7.3 Summary

A liquid-gated vertically stacked SiNW FET fabricated on bulk-Si was efficiently demonstrated for its future implementation into low cost biosensing systems. Though leakage current still occurs from the source to drain anchors through the parasitic MOSFET underneath the SiNWs, excellent $I_{on}/I_{off}$ ratios > $10^4$ and low subthreshold slopes $SS$ ~ 160 mV/dec were found for the bulk-Si based devices. Therefore, such a structure could still be efficiently used when operated specially in the strong inversion regime.

# Chapter 8 Conclusion and outlook

In this chapter the most relevant contributions of this work will be summarized. Also in here we explore possible future direct or indirect implementations for the type of structures developed in this thesis.

## 8.1 Achieved results

A 3D vertically stacked silicon nanowire field effect transistor has been successfully designed, fabricated and electrically characterized in a dry and liquid environment for its future implementation into a heterogeneous sensing system. Furthermore, a highly robust, high pH sensor response stacked nanostructure FET was demonstrated and a 3D streptavidin sensor was developed for the first time. The devices feature high density arrays (7 or 8 × 20 SiNW) of fully depleted, ultra-thin channels with varying number of NWs in the horizontal direction (10, 15 and 20 NWs) and different channel lengths (2, 3, 4 μm). State-of-the art sensor responses were possible due to their excellent FET performance characteristics (average subthreshold slopes $SS$ ~ 95 down to 85 mV/dec, leakage currents $I_{off} < 2 \times 10^6$ mA/μm, normalized to $d_{NW} = 30$ nm, high $I_{on}/I_{off}$ ratios > $10^6$), appropriate surface functionalization and high number of SiNWs available for sensing interactions. The detection of ultra-low concentrations (down to ~ 17 aM) of the protein streptavidin was shown with a biotinylated $SiO_2$ gate dielectric device. Also a vertically stacked SiNW FET was fabricated on bulk-Si, was demonstrated as a low cost alternative to the SOI-based sensor. Though leakage current still occurs from the source to drain anchors through the parasitic MOSFET underneath the SiNWs, excellent $I_{on}/I_{off}$ ratios > $10^4$ and low subthreshold slopes $SS$ ~ 160 mV/dec were found for the bulk-Si based devices. The structures developed here show great potential for the selective sensing of disease biomarkers when ultra-low concentration detection is needed.

## 8.2 Outlook

### 8.2.1 Amperometric vertically stacked SiNW sensor

Deshpande *et al.*, [137] proposed a heterogeneous Au/Pt nanowire device for the amperometric sensing of glucose (Figure 8-1a). They propose a heterogeneous working electrode that serves to provide two different and essential functions to enhance the amperometric detection of glucose; delivers available enzyme immobilization surface (Au) and provides sufficient oxidation current (reaction with Pt surface). The enzyme glucose oxidase (immobilized on the Au side of the nanowire) catalyzes the reaction of glucose to gluconic acid and hydrogen peroxide. Furthermore, the decomposition of hydrogen peroxide can be catalyzed by the Pt (on the other side of the NW) for higher sensing performances.

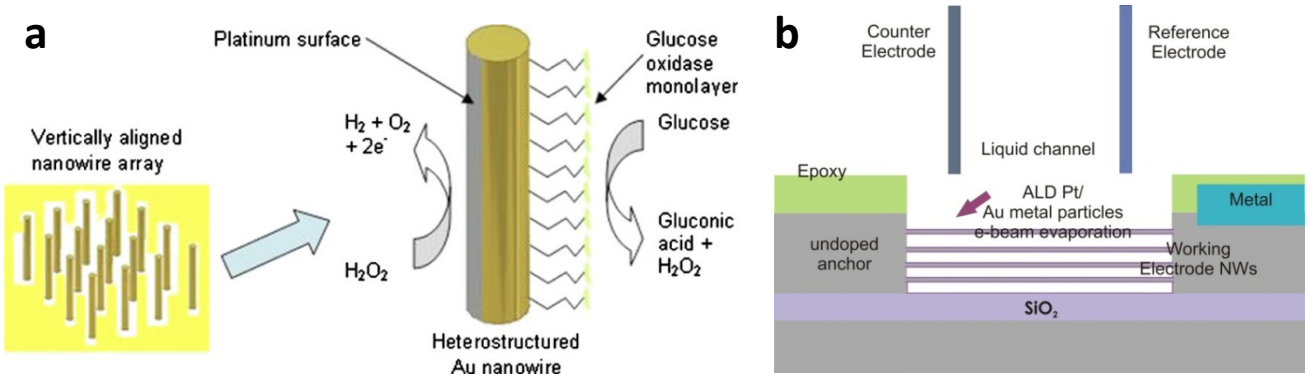



**Figure 8-1:** (a) Schematic of hetero-structure Au/Pt nanowire for glucose amperometric sensing, modified from [137]. (b) Schematic cross section of proposed vertically stacked SiNW amperometric sensor.

As previously discussed in of this thesis, it is possible to deposit metal on the SiNW array by e-beam evaporation (though the ZEP window used to selectively remove $SiO_2$ around the SiNWs) on an angle and therefore it is possible to coat the vertically stacked structures with dissimilar metals from each side of the structure. Therefore it is possible to produce a similar structure to that of Deshpande *et al.*, by a top-down CMOS compatible process (Figure 8-1b). This vertically stacked heterogeneous metal amperometric type sensor that can be used not only for glucose sensing but for a myriad of analytes (depending on the immobilized enzyme and metals used). Similarly to our current sensing measurement set-up, a commercial Ag/AgCl electrode and Pt wire can be integrat-

ed to act as a reference and counter electrode, respectively. In a three electrode amperometric sensing configuration a constant potential is applied between the reference and working electrode. The electrochemical reaction (oxidation/reduction reaction) occurs at the working electrode. The current changes as the analyte of interest is oxidized at the anode or reduced at the cathode can be measured (current changes measured between the working and counter electrode). That is the counter electrode provides the current required for the electrochemical reaction to occur at the working electrode. This type of device has in fact been already fabricated. Nonetheless measurements are ongoing.

### 8.2.2 Energy harvester with vertically stacked SiNWs

Using a similar process flow as the one proposed in this thesis, a vertically stacked silicon nanowire based thermoelectric device can be easily fabricated. A single or several SiNW arrays connected in series by anchoring Si blocks (or lines, micro-spacers) can be integrated into a single or double clamped suspended beam thermocouple structure to convert waste heat (*e.g.*, microcooling of a microprocessor) into electrical energy (Figure 8-2a, [138]).

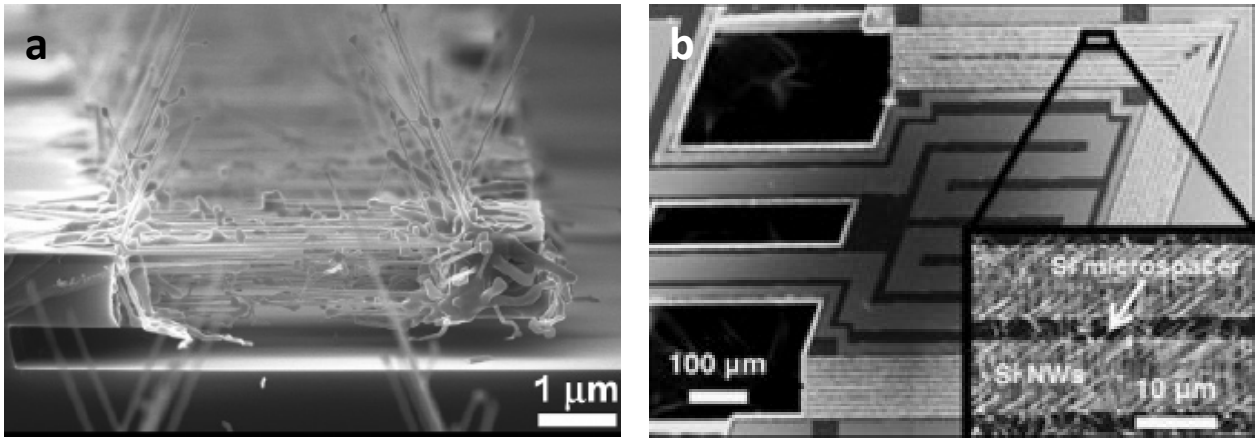



**Figure 8-2:** (a) SEM image of cross section view of suspended SiNW array micro-paddle fabricated by VLS, modified from [138]. (b) Thermally isolated suspended Si mass connected to the bulk-Si through the SiNW array, adapted from [139].

A power generator can also be achieved by the use of a thermally isolated suspended mass connected to the to the bulk silicon through the SiNW array to achieve high thermal gradients (Figure 8-2b, [139]). The natural separation between the cold and hot parts of the thermoelectric device by

the use of low thermal mass suspended SiNW arrays serves to develop large temperature differences to improve the thermoelectric performance of the structure [138]. The same type of device can not only be used for energy harvesting but for hot-spot cooling, for example (integrated circuits, IC chips).The performance of a thermoelectric device (conversion of temperature difference to electric potential) is dependent upon fundamental properties of the thermoelectric material itself. The dimensionless figure of merit ($ZT$) that describes how efficiently a material is able to produce thermoelectric power is given by Equation 8.1:

$$ZT = \frac{\sigma {S_V}^2 T}{\kappa}$$

**Equation 8.1**

Where $\sigma$ is the electrical conductivity, $S_V$ is the Seebeck coefficient, $T$ is the temperature and $\kappa$ is the thermal conductivity of the material. Both the Seebeck coefficient and the electrical conductivity of the material of interest need to be large but they relate to each other and as the Seebeck coefficient increases the electrical conductivity decreases. Also, generally if the electrical conductivity increases so does the thermal conductivity as electrons are also carriers of heat. For that reason, efforts to improve the thermoelectric performance have been focused on not only synthesizing new materials altogether but on the development of nanostructures/or nanostructured material for which fundamental material properties change drastically from their bulk counterparts. SiNWs (best value for a SiNW $d_{NW}$ ~ 50 nm at room temperature $ZT$ ~ 0.6 [140])have been shown to have enhanced thermoelectric properties in comparison to bulk-Si ($ZT$ ~ 0.01 [141]). They have been shown to have similar electrical conductivities and Seebeck coefficients to that of bulk-Si but their thermal conductivity has been shown to be much lower [140, 141] which in turn greatly improves the thermoelectric figure of merit $ZT$. For our thermoelectric device, the vertically stacked SiNWs acts as the thermoelectric material itself. As silicon nanowires possess low thermal conductivities high temperature gradients are expected. Furthermore, by linking several arrays in series maximum temperature gradients can be achieved. In this work, ultra-thin ($d_{NW}$ ~ 15 – 30 nm) and long SiNW arrays up to 5 μm in length have been able to be fabricated in a reliable, controlled and reproducible manner which should furthermore improve the thermal gradient produced along the structures.

The vapor liquid solid growth method has been the typical approach for fabricating such type of devices. Nonetheless, as can be seen from Figure 8-2a and b, and as previously mentioned in the introduction of this thesis, precise control of the NW size, density and growth location is difficult to achieve with such fabrication method. It has been demonstrated in this thesis that with the simple BOSCH process it is possible to fabricate reproducible single crystalline vertically stacked SiNW devices with a high vertical and horizontal NW density, with suspended, well defined, ultra-thin SiNWs diameters. The average thicknesses possible by VLS are relatively large ~ 100 nm [138, 139], this can be improved by BOSCH for maximum temperature gradients. The BOX underneath the thermocouple array can be easily removed by BOE to create the suspended structure. With such approach, reproducible uniform density arrays, with consistent NW sizes from anchor to anchor, from top to bottom of the trench can be easily fabricated with a top-down, fully CMOS compatible technique. Precise control of the location of the NWs only depends on the trench opening and silicon spacer dimension, something not easily achievable by the VLS method. Also, the VLS method introduces an extra resistance. The catalyst metal precursor (nanoparticles) used to grow the NWs lies in between the grown nanowire and the opposing Si contacting wall leading to degraded electrical contact performances. Also the progressive reduction in the amount of catalyst available as the NW growth produces arrays with non-uniform diameters [142]. Our fabrication approach proposed in this thesis could be easily adapted to produce such thermoelectric type of devices with the added benefits of using a top-down, CMOS compatible, reliable and robust process.

### 8.2.3 Vertically stacked SiNW-based cantilever flow sensor

SiNWs have also been shown to exhibit superior piezoresistive properties [143]. Vertically stacked SiNW arrays could also be implemented into a cantilever flow sensor with a single or several SiNW arrays connected in series by anchoring Si spacers to produce a single clamped cantilever with a wide-paddle ending. The wide-paddle at the end of the cantilever can be placed directly on the path of the flow. The flow induced deflection of the cantilever translates to a piezoresistive change. A similar structure has been proposed before by Zhang *et al.,* [144] in which the SiNWs are located at the anchor point between the wide paddle and the substrate to induce maximum strain. Fluid flow can induce stress on the SiNWs which results in a piezoresistance change, Figure 8-3.

Our current process flow could be easily modified to implement such type of flow sensor structures.

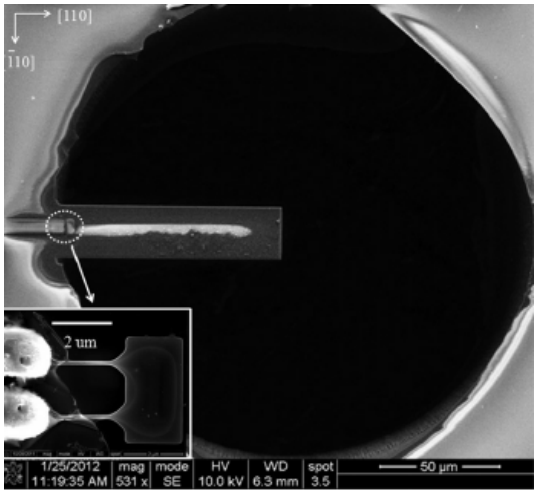



**Figure 8-3:** SEM image of SiNW-based cantilever flow sensor, adapted from [144].

# Appendix A: TCAD Simulations

## A.1. Junctionless and enhancement mode tri-gated structures

Tri-gated enhancement mode and junctionless nanowire transistors were investigated through 3D TCAD simulations performed as a function of geometrical dimensions and channel doping concentration. The tri-gated structures simulated here resemble the SOI FinFET devices fabricated and investigated experimentally for biosensing applications by Tyndall National Institute within the SiNAPS European Project [64, 145]. The simulation results are briefly introduced here but more thoroughly explained in a previous publication [61].

### A.1.1. TCAD Simulations

3D TCAD simulations using Sentaurus Device e.2010.12 have been performed as a function of gate dielectric constant ($\varepsilon_r$ = 1.7, 3.9), geometrical dimensions ($L$ = 0.5, 1, 2 μm, $F_h$ = 10, 20, 30, 45 nm and $F_w$ = 10, 20, 30 nm) and doping concentration (boron B, $N_d$ = $10^{18}$ $cm^{-3}$, $10^{19}$ $cm^{-3}$, 2 × $10^{19}$ $cm^{-3}$) for a p-type SiNW/Fin tri-gated junctionless FET. Two different types of dielectric materials were investigated in this study. First, the dielectric constant $\varepsilon_r$ = 1.7 of the organic monolayer $SiC_{16}H_{33}$ passivating an oxide free silicon surface as determined by Faber *et al.*, [98] and thickness $t_d$ = 1.78 nm were utilized in the simulation. This mimics the functionalization scheme employed in this work assuming that the dielectric properties of this organic monolayer are similar to the functionalization of interest. $SiO_2$ as a gate dielectric material ($\varepsilon_r$ = 3.19) was also investigated. The simulations were built to include 145 nm of buried oxide. The lateral S/D extensions are 10 nm on each side of the gate channel. The *S*/*D* contacts are simulated as ohmic. The front-gate voltage $V_{FG}$ is swept keeping the backgate grounded $V_{BG}$ = 0 V for high and low drain voltage potentials of $V_d$ = - 1 V and - 50 mV. The gate electrode was simulated as $n^+$ polysilicon (2 × $10^{20}$ $cm^{-3}$, workfunction $\phi$ = 4.1 V). The geometric parameters (Fin height $F_h$, width $F_w$ and channel length $L$ indicated) as well as the channel doping concentration $N_d$ have been varied.

Enhancement mode devices with $\varepsilon_r$ = 1.7 and L = 500 nm were also simulated as a function of $F_h$ = 10, 20, 30, 45 nm and width $F_w$ = 10, 20, 30 nm. The enhancement mode simulated device is n-type (p-type substrate, n-channel). For our simulations the source is grounded $V_S$ = 0 V. The source and drain extensions are doped n-type phosphorous $N_{SD} = 2 \times 10^{20}$ cm$^{-3}$. The nanowire channel is p-doped boron with a changing channel doping concentration from $N_{ch} = 10^{16}$ cm$^{-3}$ to $10^{19}$ cm$^{-3}$.

All simulated devices are gated from the front and from the sides, in tri-gate FET architecture. The drain current $I_d$ is iteratively computed by solving the Poisson's and continuity's majority carrier equations (holes for JNT and electrons for enhancement) throughout the cross-section of the Fin. The drift-diffusion model is used for the carrier transport in the semiconductor without impact ionization. A mobility degradation model is also being implemented for carrier scattering effects in highly doped semiconductors for the JNT simulated devices. A doping dependent carrier mobility model was also included as well as an electric field dependent model with Shockley-Read-Hall (SRH) carrier recombination/generation.

## A.1.2. Transistor characteristics

Simulated drain current curves as a function of front-gate voltage ($I_d - V_{FG}$) are presented in Figure A1- 1a (left-axis) for a JNT structure with $F_w$ = 10 nm, $F_h$ = 45 nm, $\varepsilon_r$ = 1.7, $N_d = 10^{18}$ cm$^{-3}$, and $L$ = 500 nm. The right axis shows the calculated transconductance $g_m$. This figure illustrates the different JNT conduction regimes: (i) $V_{FG} >> V_{th}$ for flatband $V_{fb}$, the point at which the current is $I_d = q\mu_h N_d(F_w F_h)V_d/L$ ($q$: charge and $\mu_h$: hole mobility) and the JNT becomes a simple resistor, (ii) $V_{FG} < V_{fb}$ accumulation, (iii) $V_{FG} = V_{fb}$ flatband, (iv) $V_{fb} < V_{FG} < V_{th}$ partial channel depletion, and (iv) $V_{FG} = V_{th}$ threshold. Figure A1- 1b shows the $I_d - V_d$ output characteristics for devices with $F_w$ = 10 nm, $F_h$ = 45 nm, $L$ = 500 nm, $N_d = 10^{18}$ cm$^{-3}$ and two different gate. We can see the normal operation of a p-type junctionless device.

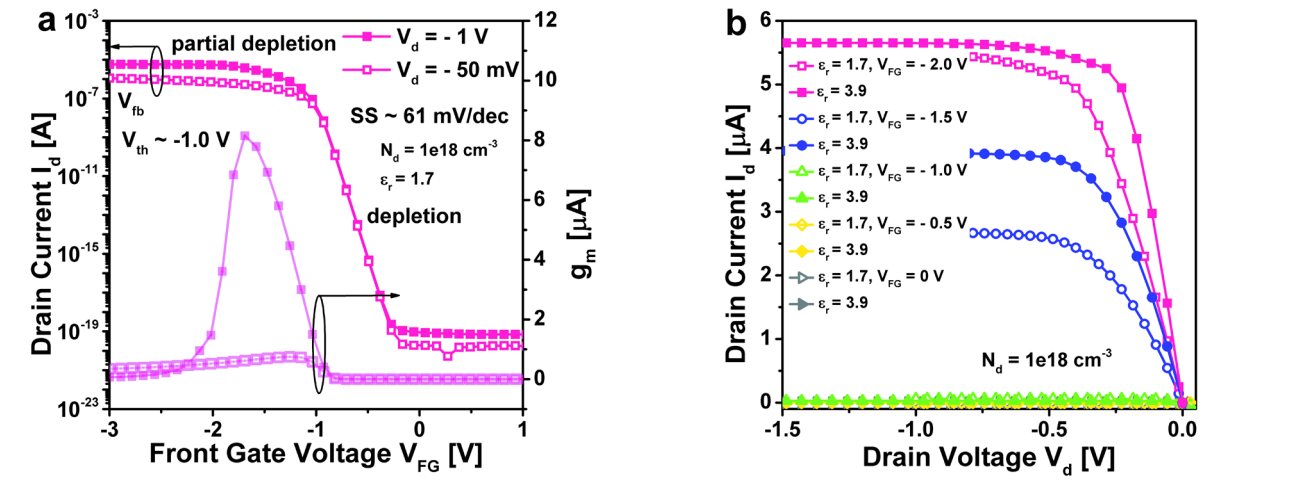



**Figure A1- 1:** (a) $I_d$ – $V_{FG}$ (left) and $g_m$ (right) at low ($V_d$ = - 50 mV) and high ($V_d$ = -1 V) drain potentials for a device with $F_w$ = 10 nm, $F_h$ = 45 nm, $N_d$ = $10^{18}$ cm$^{-3}$, $\varepsilon_r$ = 1.7 and $L$ = 500 nm. (b) $I_d$ – $V_d$ output characteristics for $V_{FG}$ = -2, -1.5, -1, -0.5, and 0 V for a devices with $F_w$ = 10 nm, $F_h$ = 45 nm $L$ = 500 nm for $N_d$ = $10^{18}$ cm$^{-3}$ for different gate dielectrics for tri-gated JNT.

The simulated $I_d$ – $V_{FG}$ for structures with $F_w$ = $F_h$ = 10 nm, length $L$ = 500 nm and different channel doping concentrations $N_d$ = $10^{18}$ cm$^{-3}$, $10^{19}$ cm$^{-3}$, 2 × $10^{19}$ cm$^{-3}$ are shown for two different gate dielectrics $\varepsilon_r$ = 1.7 (Figure A1- 2a ) and for $SiO_2$ $\varepsilon_r$ = 3.9 (Figure A1- 2b). The right axes (light shade) shows the linear $I_d$ – $V_{FG}$ curves and calculated transconductance, respectively.

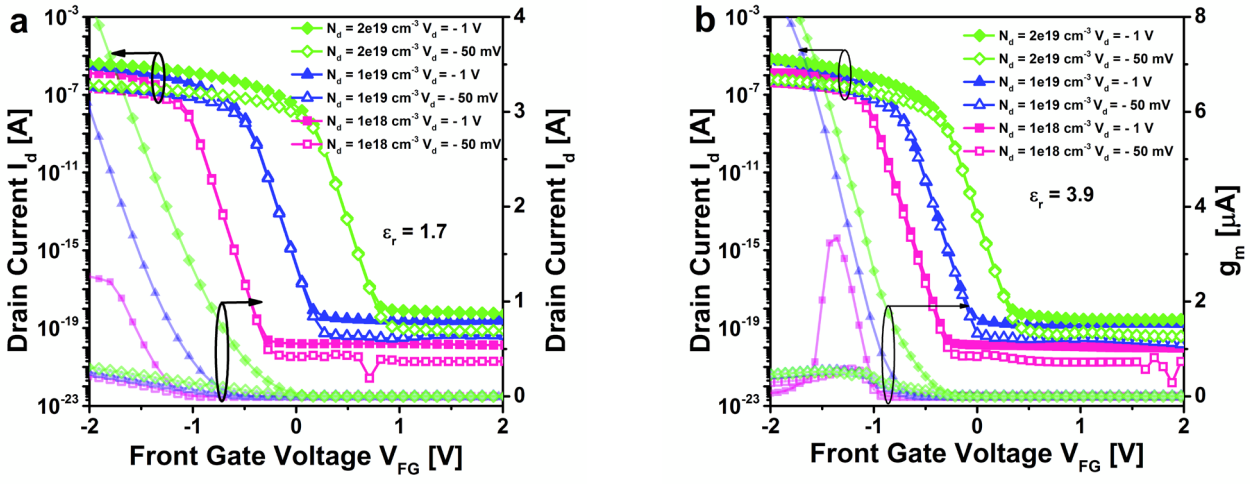



**Figure A1- 2:** $I_d$ – $V_{FG}$ curves (log scale left) at low ($V_d$ = - 50 mV) and high ($V_d$ = -1 V) drain potentials for a JNT device with $F_w$ = $F_h$ = 10 nm, $L$ = 500 nm and increasing $N_d$ for a device with $\varepsilon_r$ = 1.7 (a), $\varepsilon_r$ = 3.9 (b). The right axes of (a) shows the respective linear $I_d$ – $V_{FG}$ curves and (b) the transconductance $g_m$.

Similarly the simulated $I_d$ – $V_{FG}$ for tri-gated enhancement mode devices with $F_w = F_h = 10$ nm, length $L = 500$ nm and different channel doping concentrations $N_{ch} = 10^{16}$ cm$^{-3}$, $10^{17}$ cm$^{-3}$, $10^{18}$ cm$^{-3}$ and $10^{19}$ cm$^{-3}$ for $\varepsilon_r = 1.7$ at high drain vias $V_d = 1$ V are shown in Figure A1- 3.

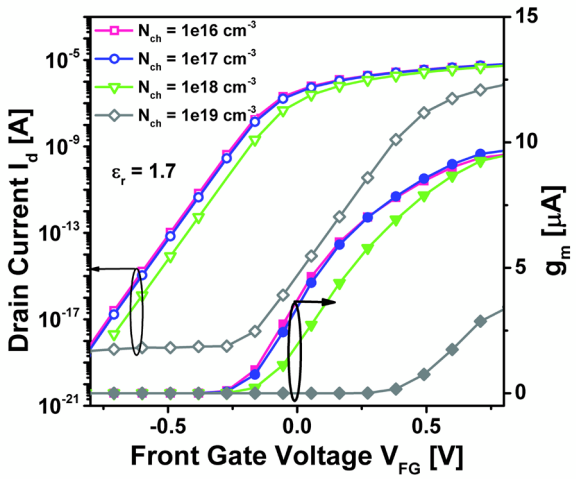



**Figure A1- 3:** $I_d$ – $V_{FG}$ curves (log scale left, linear right) at high ($V_d = 1$ V) drain potentials for a device with $F_w = F_h = 10$ nm, $L = 500$ nm and increasing $N_{ch}$ for tri-gated enhancement mode devices *with* $\varepsilon_r = 1.7$.

As a general trend, the maximum current $I_{on}$ increases with increasing doping concentration $N_d$ or channel doping concentration $N_{ch}$ for enhancement mode devices, $F_h$ and $F_w$. The $I_{on}$ also decreases for increasing channel lengths $L$ as expected due to the higher total resistance of higher channel lengths.

## A.1.3. Subthreshold slope

Figure A1- 4a and b shows the *SS* as function of increasing $F_h$ and $F_w$, respectively for different $N_d$ while keeping the other constant at $F_h = F_w = 10$ nm and $\varepsilon_r = 1.7$, $L = 500$ nm for junctionless devices. For JNT devices with small cross sections ($10 \times 10$ nm$^2$) the *SS* does not change significantly with increasing doping concentration. The *SS* for thin Fin devices ($F_w = 10$ nm) is almost unchanged with increasing $F_h$ and only when the doping channel concentration increases to $N_d = 2 \times 19$ cm$^{-3}$ the *SS* increases with $F_h$. In Figure A1- 4b one can see that *SS* does not change significantly with increasing $F_w$ except when the doping concentration increases to $N_d = 2 \times 10^{19}$ cm$^{-3}$. The *SS* for JNTs is slightly degraded for devices with a gate insulator $\varepsilon_r = 1.7$ *vs.* $\varepsilon_r = 3.9$ (not shown). The subthresh-

old slope reaches the thermal limit of MOSFETs for all studied JNT structures with a Fin width $F_w$ = 10 nm ($SS$ < 67 mV/dec). It degrades with increasing $F_h$, $F_w$, $L$ and doping concentration.

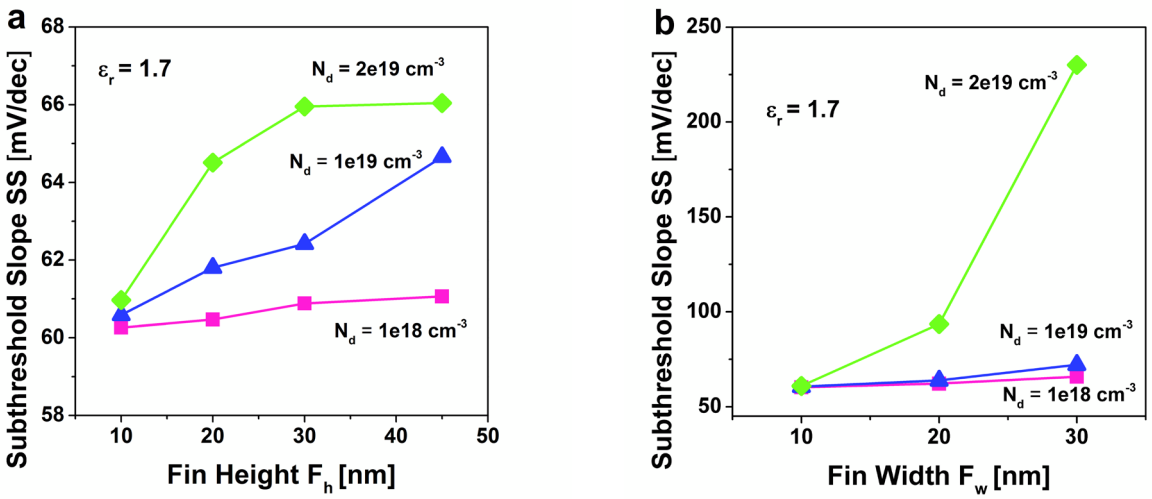



**Figure A1- 4:** (**a**) $SS$ as function of increasing $F_h$ for different $N_d$ with constant $F_w$ =10 nm, $\varepsilon_r$ = 1.7, $L$ = 500 nm, $V_d$ = -1 V. (b) $SS$ as function of increasing $F_w$ for different $N_d$ with constant $F_h$ = 10 nm, $\varepsilon_r$ = 1.7, $L$ = 500 nm, $V_d$ = 1 V for a JNT.

The $SS$ changes most dramatically as the $F_w$ is increased from 10 ($SS$ = 60.97 mV/dec) to 30 nm (230.07 mV/dec) for high channel doping concentrations $N_d = 2 \times 10^{19}$ cm$^{-3}$ and $\varepsilon_r$ = 1.7. The sub-threshold slope also increases slightly with increasing $L$ (not shown). The $SS$ degradation is much more pronounced for structures with higher doping concentrations $N_d = 10^{19}$, $2 \times 10^{19}$ cm$^{-3}$. This is understandable as the higher the doping concentration the stronger the induced electric field for channel carrier depletion and efficient turn-off.

It can be seen in Figure A1- 5a, b that the $SS$ does not change significantly with increasing $F_h$ *or* $F_w$ for the enhancement mode devices for the NW/Fin dimensions investigated here ($F_h \leq 45$ nm, $F_w \leq 30$ nm). All enhancement mode devices simulated show excellent subthreshold slopes ~ 60 mV/dec which may lead to high sensitivities. The low $SS$ found are due to the small cross sections and high S/V that allow for an excellent gate electrostatic control even at high channel doping concentrations. Only for high channel doping concentrations and large $F_w$ = 30 nm the $SS$ increases to 74.4 mV/dec.

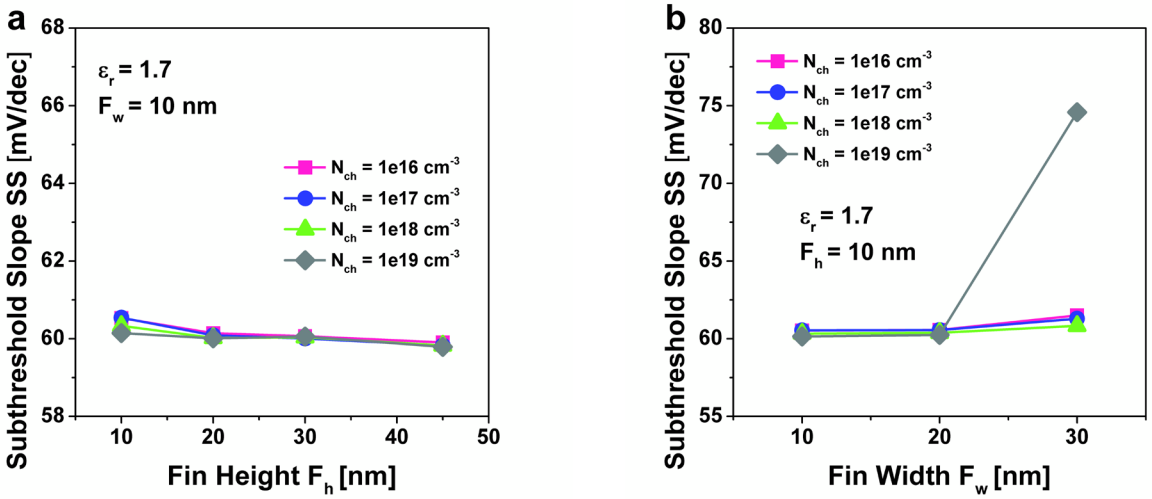



**Figure A1- 5:** *SS* as a function of increasing $F_h$ (a) and increasing $F_w$ (b) for different channel doping concentrations and $V_d$ = 1V for enhancement mode devices with gate insulator dielectric $\varepsilon_r$ = 1.7.

## A.1.4. Threshold voltage

The threshold voltage $V_{th}$ was defined as the voltage for which the drain current reaches a value of $I_d = (100\ nA * F_w/L)$. Figure A1- 6a, b shows the extracted $V_{th}$ values for the simulated JNT devices as a function of increasing $F_h$ and $F_w$ for different doping concentrations when $\varepsilon_r$ = 1.7 and $L$ = 500 nm. For good electrostatic control, the cross section area ($F_h F_w$) needs to be small enough to allow depletion of carriers and efficiently turn-off the JNT [53]. For increasing doping concentrations it is harder to turn-off the device for a given $F_w$ and $F_h$. The threshold voltage increases and goes from negative towards more positive values as the fin height and doping concentrations increase in agreement with literature results [146]. For low doping concentrations the $V_{th}$ variation is minimal nevertheless for all $F_h$, $F_w$, $L$ and it changes the most when $N_d$ = 2 × $10^{19}$ $cm^{-3}$. When $N_d$ = $10^{18}$ $cm^{-3}$, and $\varepsilon_r$ = 1.7, the threshold voltage shift is $\Delta V_{th}$ = 0.093 V with increasing $F_h$ from 10 to 45 nm, whereas when $N_d$ = 2 × $10^{19}$ $cm^{-3}$ $\Delta V_{th}$ = 0.890 V. For low doping levels, the side-gates are enough to completely deplete the channel; the top-gate does not have any impact, which translates into $V_{th}$ depending only on $F_w$. With a high doping level, the side-gates are not enough to deplete completely the channel, which translates into $V_{th}$ depending more on the height (relates to the thickness that the top-gate has to deplete in order to turn off the device). The $V_{th}$ variation with $F_h$

and $F_w$ is not as pronounced for devices with $SiO_2$ dielectric constants, *e.g.*, when $N_d = 2 \times 10^{19}$ cm$^{-3}$, $\Delta V_{th} = 0.414$ V as the $F_h$ is increased from 10 to 45 nm, almost 50% less than when $\varepsilon_r = 1.7$. Though the threshold voltage variation increases with doping concentration, it is also not as pronounced for devices with Fin widths of 10 nm in accordance with previous literature results that have shown that for small cross section structures (< 10 × 10 nm$^2$) the $V_{th}$ change with doping concentration is almost negligible [147]. Our simulation results do not show a strong $V_{th}$ dependence with increasing gate length $L$ for the long channel devices investigated here (0.5 – 2 μm), not shown.

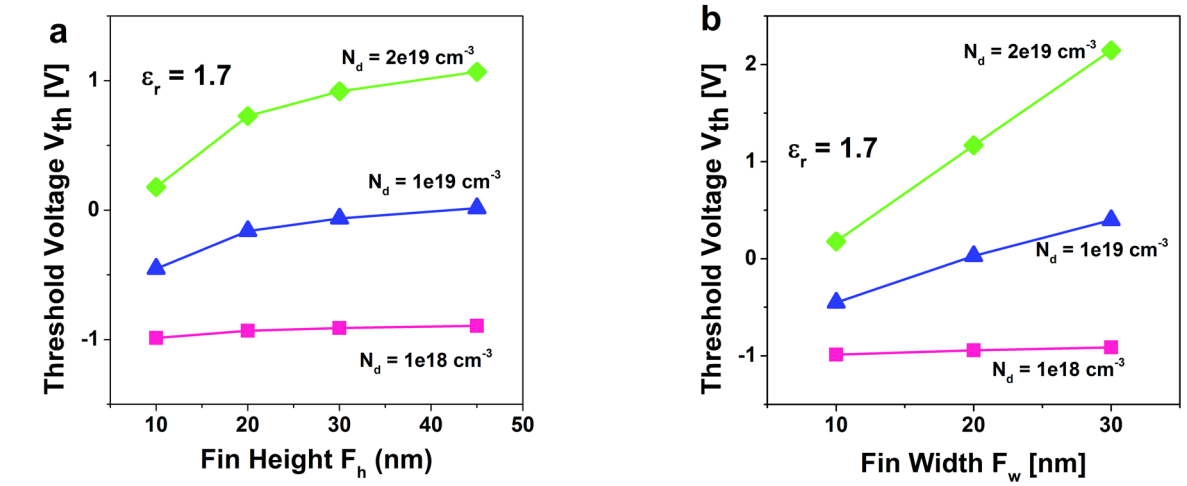



**Figure A1- 6:** $V_{th}$ variation as a function of $F_h$ (a) and $F_w$ (b) for different $N_d$ for JNT devices with constant $F_w$ *or* $F_h$ = 10 nm, $L$ = 500 nm, $V_d$ = -1 V for an insulator dielectric $\varepsilon_r = 1.7$.

Figure A1- 7a, b shows the extracted $V_{th}$ values for the simulated enhancement mode devices as a function of increasing $F_h$ (a) and $F_w$ (b) for different $N_{ch}$ ($\varepsilon_r = 1.7$, $L$ = 500 nm). In comparison to JNT the $V_{th}$ for enhancement mode devices does not change significantly with $F_w$ and $F_h$ and $N_{ch}$. Only when the channel doping concentration is very high the $V_{th}$ shifts to a greater extent. Even for high channel doping concentrations $N_{ch} = 10^{19}$ cm$^{-3}$ the threshold voltage shift is $\Delta V_{th} = 0.063$ V with increasing $F_h$ from 10 to 45 nm with the highest change occurring when the $F_w$ increases from 10 nm to 30 nm with a $\Delta V_{th} = 0.331$ V.

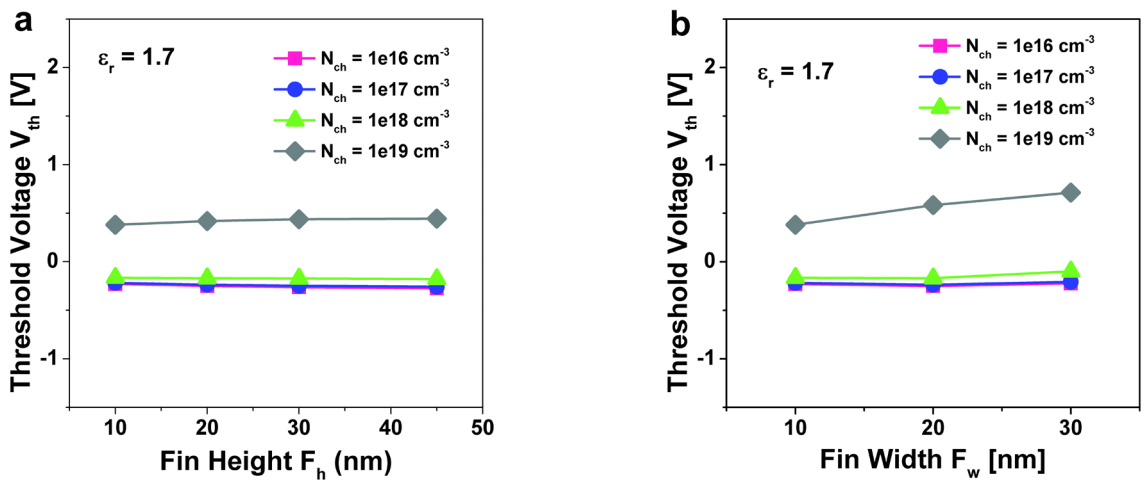



**Figure A1- 7:** $V_{th}$ variation as a function of $F_h$ (a) and $F_w$ (b) for different $N_d$ for enhancement mode devices with constant $F_w$ = 10 nm and $F_h$ = 10 nm respectively, $L$ = 500 nm, $V_d$ = 1 V for an insulator dielectric $\varepsilon_r$ = 1.7.

## A.2. Gate-all-around structures

N-type SiNW/Fin GAA enhancement mode structures that resemble the type of devices fabricated here were also investigated through TCAD simulations.

### A.2.1. TCAD Simulations

For the SiNW/Fin GAA enhancement mode devices, the TCAD simulations were perfumed using Sentaurus Device 2009.06c as a function geometrical dimensions ($L$ = 2, 5, 10 µm, $F_h$ = 20 – 100 nm and $F_w$ = 20 – 60 nm), doping concentration (boron B, $N_d$ = $10^{18}$ cm$^{-3}$, $10^{19}$ cm$^{-3}$, 2 × $10^{19}$ cm$^{-3}$) and multiple channels (1 – 3 vertically stacked structures). The source and drain extensions are doped n-type phosphorous $N_{SD}$ = $10^{20}$ cm$^{-3}$. The nanowire channel is p-doped boron with a changing channel doping concentration from $N_{ch}$ = $10^{15}$ cm$^{-3}$ to $10^{19}$ cm$^{-3}$. The gate oxide thickness was simulated to be 2 nm (native oxide) with a gate dielectric being $HfO_2$ of 5 nm. The drain current $I_d$ is iteratively computed by solving the Poisson's and continuity's majority carrier equations (electrons for enhancement) throughout the cross-section of the Fin. The drift-diffusion model is used for the carrier transport in the semiconductor without impact ionization. A doping and transverse field dependent mobility model was used.

## A.2.2. Transistor characteristics

The simulated $I_d - V_{FG}$ for the GAA enhancement mode devices with increasing channel doping concentrations $N_{ch}$ and $F_w = F_h = 20$ nm, length $L = 2\mu m$ is shown in Figure A1- 1a. Figure A1- 1b shows the $I_d - V_{FG}$ characteristics for GAA enhancement mode devices as the number of Fins increases from one to three for a SiNW $F_w = F_h = 20$ nm and a Fin $F_w = 20$ nm, $F_h = 40$ nm.

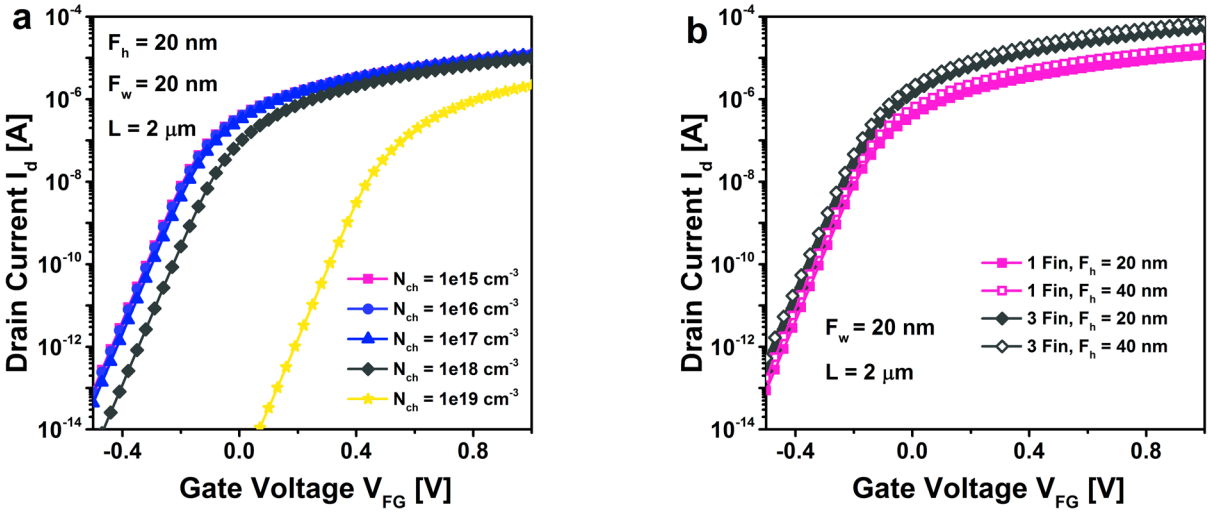



**Figure A2- 1:** (a) $I_d - V_{FG}$ at a low ($V_d$ = - 50 mV) drain potentials for a device with $F_w$ = 20 nm, $F_h$ = 20 nm and increasing channel doping concentrations $N_{ch} = 10^{15} - 10^{19}$ cm$^{-3}$ and $L$ = 2 µm. (b) $I_d - V_{FG}$ at a low ($V_d$ = - 50 mV) drain potentials for devices with one or three Fins with different dimensions, $N_{ch} = 10^{15}$ cm$^{-3}$ and $L$ = 2 µm.

## A.2.3 Results

The same trends found for tri-gated enhancement mode devices were found here, not surprisingly, and therefore all the details will not be repeated. Only the main results will be summarized here. The $V_{th}$ does not change significantly with $F_w$ and $F_h$ and $N_{ch}$. Only when the channel doping concentration is very high the $V_{th}$ shifts to a greater extent. The $SS$ does not change significantly with increasing $F_h$ *or* $F_w$. All enhancement mode devices simulated show excellent subthreshold slopes ~ 60 mV/dec which may lead to high sensitivities. As a general trend, the maximum current $I_{on}$ increases with increasing channel doping concentration $N_{ch}$, $F_h$ and $F_w$. The $I_{on}$ also decreases for increasing channel lengths $L$.

# Appendix B: ISFET/REFET differential pair

Differential pair circuits with an integrated local noble metal electrode ($V_{LG}$) have been previously explored in literature for planar ISFETs [108, 109] in order to get rid of the bulky, external reference electrode. In here we investigate their implementation with vertically stacked SiNW biosensors. The differential circuit consist of an ISFET (or sensing FET), an ion-insensitive reference FET (REFET) and an active or passive load. With the use of a differential pair, any gate voltage that is common to both ISFETS and REFET will not appear at the output. A requirement that follows from the behavior of the differential circuit is that the ISFET must be more sensitive to charged species than the REFET. Several passivation methods for the REFET have been explored, from thick oxide encapsulations that keep the bound ions far away from the nanowire core [104] to surface passivation of open $OH^-$ sites [148] using a self-assembled monolayer (SAM) of silane with long alkyl chains [109]. This is however beyond the scope of this work and was not explored any further. The differential pair is often implemented as an operational transconductance amplifier (OTA) using six active devices (2 p-type and 4 n-type FETs) as this is a favorable option in terms of silicon area . However, MOSFETs are not directly compatible with our current process flow but resistors are. Therefore we propose a resistor-based ISFET/REFET differential circuit.

## B1.1. Differential circuit with resistors

The OTA is based on the assumption that both the ISFET and the REFET are perfectly matched (Figure B1- 1 ). Consequently, if the gate voltage is equal for both devices, the bias current $I_0$ flowing through resistor $R_S$ will split equally between the sensing and reference branch. The output voltages $V_{o,ISFET}$ and $V_{o,REFET}$ will then be identical and equal to $V_{DD} - V_{R_L} = V_{DD} - R_L\, I_0/2$. It is therefore clear that for equal gate voltages ($V_{G,ISFET} = V_{G,REFET}$) we have $V_{o,ISFET} = V_{o,REFET}$ and hence the differential output voltage $V_{od}$ will be equal to zero [149]. When $V_{o,ISFET} \neq V_{o,REFET}$, the differential output voltage will no longer be zero. Instead it will be a measure of the concentration of the molecule of interest.

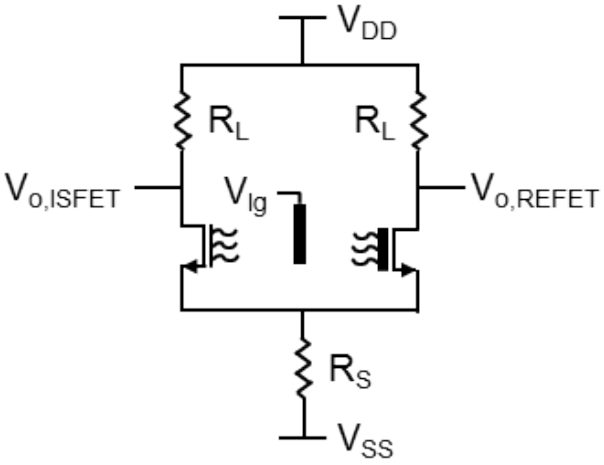



**Figure B1- 1:** Differential operational transconductance amplifier (OTA) with (a) passive source and passive load.

## B.1.2. Simulations

The circuit design was explored through Cadence 6 Analog Design Environment (ADE) with the Spectre simulations. For this, the vertically stacked nanowire sensor had to be first modeled using Verilog-A.

Several models for surrounding gate (SG) FETs were considered [150-152]. All derive an analytical solution for the drain current $I_d$ using a charge-based approach. In order to adapt for our for vertically stacked SiNW structure and considering the large inter-wire spacing $d_{iw} \geq 100\,nm$ with respect to the wire diameter $d_w \leq 30\,nm$, the wires are considered as independent parallel SGFETs, allowing us to model them as a single large transistor in the absence of a backgate voltage $V_{BG}$. After some manipulations, a key relationship common to all charge-based models can be found that relates the voltages to the mobile charge inside the channel [151], Equation B. 1. Where $V_{ch}$ is the quasi-Fermi potential, $V_{GS}$ is the gate-to-source voltage, $V_{th}$ is the threshold voltage, $\Delta V_{th}$ provides an adaptation of the threshold voltage to the SGFET structure, $Q_i$ is the mobile (inversion) charge density and $H$ is a parameter specific to this model.

$$V_{GS} - V_{th} - \Delta V_{th} - V_{ch} = q_i + \ln(Q_i) + \ln(1 + HQ_i)$$

**Equation B. 1**

The drain current can then be expressed as a function of the inversion charges at the ends of the wire [153]. Where $\mu$ is the carrier mobility, $R$ is the wire radius, $L$ is the wire length and $C_{ox}$ is the oxide capacitance, $Q_0 = 4\varepsilon_{Si}/(U_T R)$ and $Q_s$ and $Q_d$ are calculated after (Equation B. 2) using $V_s$ and $V_d$ for the channel Fermi level respectively

$$I_d = \frac{2\pi\mu R}{L}\left[2U_T(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + Q_0 U_T \ln\left(\frac{Q_d + Q_0}{Q_s + Q_0}\right)\right]$$

**Equation B. 2**

The model is completed by adding a pH sensitive contribution for the threshold voltage assuming a Nerstenian shift of 60 mV/pH (Figure B1- 2a). The Verilog-A implementation of the model allowed us to proceed with the circuit level simulations.

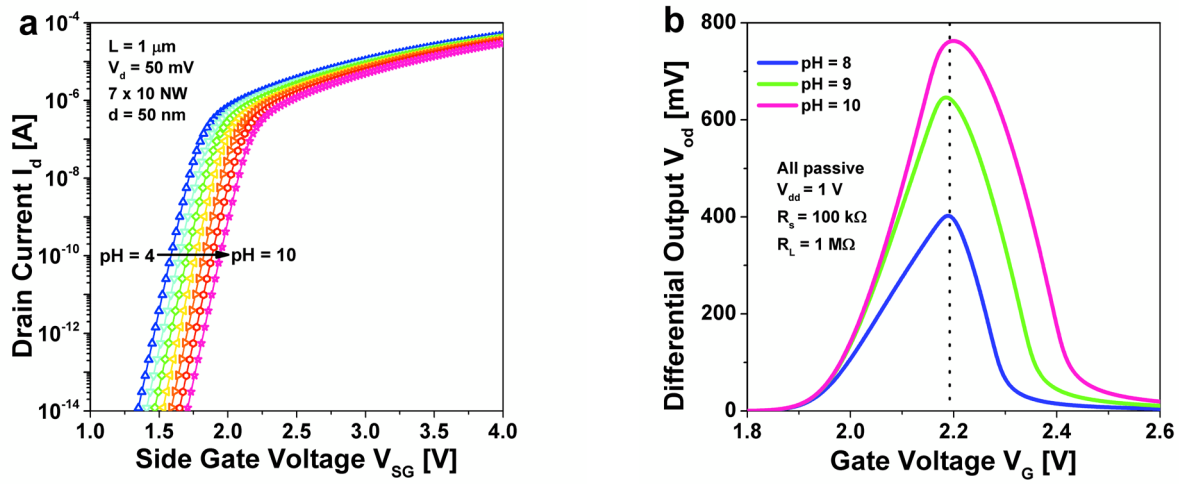



**Figure B1- 2: (a)** $I_d$ – $V_G$, for structures with $L$ = 1 µm, $d_{NW}$ = 25nm, $t_{ox}$ = 2 nm, $\mu$ = 300 cm²/Vs. (b) Simulations of the differential OTA with passive source and passive load. ISFET/REFET: $L$ = 1 µm, $d_{NW}$ = 50nm, $t_{ox}$ = 2 nm, $\mu$ = 300 cm²/Vs, $N$=70 wires, $N_a$=$10^{15}$ cm$^{-3}$.

In order to gain insight in the characteristics of the stacked silicon nanowire device and circuit, simulations were run in the Cadence 6 Analog Design Environment with the Spectre simulator. The maximum sensitivity was achieved with source and load resistance $R_S = 100\ \text{k}\Omega, R_L = 1\ M\Omega$ (Figure B1- 2). The maximum sensitivity is achieved at $V_G \approx 2.2$ V.

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# Publications

## Journal Papers:

1. E. Buitrago, M. Fernández-Bolaños, Y.M. Georgiev, R. Yu, O. Lotty, J.D. Holmes, A.M. Nightingale, A.M. Ionescu, Electrical Characterization of High Performance, Liquid-Gated Vertically Stacked SiNW-Based 3D FET for Biosensing Applications, Sensors and Actuators B: Chemical, In Press, Accepted, (2014).

2. E. Buitrago, M. Fernández-Bolaños, Y.M. Georgiev, R. Yu, O. Lotty, J.D. Holmes, A.M. Nightingale, A.M. Ionescu, High Performance Vertically Stacked SiNW-Based 3D FET for the Attomolar Detection of Streptavidin and High Response pH Sensing, Biosensors and Bioelectronics, Under Review (2014).

3. H. Guerin, H. Le Poche, R. Pohle, L. Bernard, E. Buitrago, R. Ramos, J. Dijon, A. M. Ionescu, High-yield, In-situ Fabrication and Integration of Horizontal Carbon Nanotube Arrays at the Wafer Scale for Robust and Reliable Ammonia Sensors. Carbon, (2014), Under Review.

4. E. Buitrago, M. Fernández-Bolaños, S. Rigante, C.F. Zilch, N. Schröter, A.M. Nightingale, A.M. Ionescu, The Top-Down Fabrication of a 3D-Integrated, Fully CMOS-Compatible FET Biosensor Based on Vertically Stacked SiNWs and FinFETs, Sensors and Actuators B: Chemical, 193 (2014) 400.

5. G. Fagas, M. Nolan, Y. Georgiev, R. Yu, O. Lotty, N. Petkov, J. Holmes, G. Jia, B. Eisenhawer, A. Gawlik, F. Falk, N. Khosropour, E. Buitrago, M. Fernández-Bolaños, F. Krummenacher, A.M. Ionescu, M. Kayal, A.M. Nightingale, J. Mello, E. Puik, F. Bent, R. Lafeber, R. Ramaneti, H. Tong, C. Rijn, Component design and testing for a miniaturised autonomous sensor based on a nanowire materials platform, Microsyst. Technol, (2014) 1-18.

6. E. Buitrago, G. Fagas, M. Fernández-Bolaños, Y.M. Georgiev, M. Berthomé, A.M. Ionescu, Junctionless Silicon Nanowire Transistors for the Tunable Operation of a Highly Sensitive, Low Power Sensor, Sensors and Actuators B: Chemical, 183 (2013) 1.

7. E. Buitrago, M. Fernández-Bolaños, A.M. Ionescu, Vertically Stacked Si Nanostructures for Biosensing Applications, Microelectronic Engineering, 97 (2012) 345.

8. M. Fernández-Bolaños, E. Buitrago, A.M. Ionescu, RF MEMS Shunt Capacitive Switches Using AlN Compared to $Si_3N_4$ Dielectric, Journal of Microelectromechanical Systems, 21 (2012) 1229.

9. C. Roth, G. Oberbossel, E. Buitrago, R. Heuberger, P.R. von Rohr, Nanoparticle Synthesis and Growth in a Continuous Plasma Reactor from Organosilicon Precursors, Plasma Processes and Polymers, 9 (2012) 119.

# Conferences/Workshops/Meetings:

1. E. Buitrago, M. Fernández-Bolaños, Y.M. Georgiev, R. Yu, O. Lotty, J.D. Holmes, A.M. Nightingale, A.M. Ionescu, Attomolar Streptavidin and pH Low Power Sensor Based on 3D Vertically Stacked SiNW FETs, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Hsinchu, Taiwan (2014).

2. E. Buitrago, M. Fernández-Bolaños, Y.M. Georgiev, R. Yu, O. Lotty, J.D. Holmes, A.M. Nightingale, A.M. Ionescu, Functionalized 3D 7x20-array of Vertically Stacked SiNW FET for Streptavidin Sensing, Annual Device Research Conference (DRC), Notre Dame, IN (2013).

3. E. Buitrago, G. Fagas, M. Fernández-Bolaños, Y.M. Georgiev, M. Berthomé, A.M. Ionescu, Junctionless Silicon Nanowire Transistors for the Tunable Operation of a Highly Sensitive, Low Power Sensor, International Conference on Bio-sensing Technology, Sitges, Spain (2013).

4. N. Schröter, E. Buitrago, M. Fernandez-Bolaños, W. Raberg, M. Meindl, J. Schotter, C. Zilch, A.M. Ionescu, Immobilization of DNA to Planar and Nanostructured Chip-Surfaces for the Detection of Pathogen-Specific Biomolecules on a Magnetic Bead Based Diagnostic Platform, International Conference on Bio-sensing Technology, Sitges, Spain (2013).

5. E. Buitrago, M. Fernández-Bolaños, A.M. Ionescu, Vertically Stacked Silicon Nanowire for Biosensing Applications, Micro Nano Fabrication Annual Review Meeting, Lausanne, Switzerland (2013).

6. T. Bieniek, G. Janczyk, P. Janus, P. Grabiec, G. Wielgoszewski, T. Gotszalk, M. Moczała, E. Buitrago, A.M. Ionescu, M. Fernandez-Bolaños, Reliability and Robustness Investigation of 3D Vertically Stacked Silicon Nanowire Structures Using AFM Based Techniques, Nanotech Conference and Expo, Washington, DC, USA (2013).

7. T. Bieniek, G. Janczyk, P. Janus, P. Grabiec, M. Nieprzecki, G. Wielgoszewski, M. Moczała, E. Buitrago, A.M. Ionescu, M. Fernandez-Bolaños, Reliability and Robustness Investigation of Novel Nanosensor Structures Using AFM-based Techniques, Innovative Technologies in Medicine (ITMED), Bialystok, Poland (2013).

8. E. Buitrago, M. Fernández-Bolaños, Y.M. Georgiev, R. Yu, O. Lotty, J.D. Holmes, A.M. Nightingale, A.M. Ionescu, Functionalized 3D 7x20-array of Vertically Stacked SiNW FET for Streptavidin Sensing, Swiss-Japanese Symposium on Nanomedicine and Imaging Frontiers EPFL, Lausanne, EPFL (2013).

9. T. Bieniek, G. Janczyk, P. Janus, P. Grabiec, M. Nieprzecki, G. Wielgoszewski, M. Moczała, E. Buitrago, A.M. Ionescu, M. Fernandez-Bolaños, Silicon Nanowires Reliability and Robustness Investigation Using AFM-based Techniques, Electron Technology Conference, Ryn, Poland (2013), p. 89022L.

10. E. Buitrago, G. Fagas, M. Fernández-Bolaños, A.M. Ionescu, Silicon Nanowires for Biosensing Applications, Zero Power Workshop, Barcelona, Spain (2012).

11. E. Buitrago, M. Fernández-Bolaños, A.M. Ionescu, Vertically Stacked Silicon Nanowire for Biosensing Applications, Micro Nano Fabrication Annual Review Meeting, Lausanne, Switzerland (2012).

12. T. Bieniek, G. Janczyk, P. Janus, P. Grabiec, G. Wielgoszewski, T. Gotszalk, M. Moczała, E. Buitrago, A.M. Ionescu, M. Fernandez-Bolaños, Reliability Investigation by Examination of dedicated MEMS/ASIC and NW's Test Structures related to novel 3D SiP and Nano-Sensors Systems, IEEE International Workshop on Three-Dimensional Stacked Integrated Circuits (3D-Test), Anaheim, CA, USA (2012).

13. E. Buitrago, M. Fernández-Bolaños, A.M. Ionescu, 3D Vertically Stacked SiNWs for Biosensing Applications, LEA Micro-Engineering Workshop, Saline Royale d'Arc et Senans, France (2012).

14. E. Buitrago, M. Fernández-Bolaños, A.M. Ionescu, 3D Vertically Stacked Nanostructures for Biosensing Applications, International Conference on Micro and Nano Engineering (MNE), Berlin (2011).

15. E. Buitrago, M. Fernández-Bolaños, A.M. Ionescu, Vertically Stacked Silicon Nanowire for Biosensing Applications, Micro Nano Fabrication Annual Review Meeting, Lausanne, Switzerland (2011).

16. M. Fernández-Bolaños, P. Ramm, R. Pufall, E. Buitrago, C. Zilch, H. Guerin, H. Le Poche, P. Pohle, P. Popescu, A.M. Ionescu, Heterogeneous Integration for Nanosensor Systems – the EU-Project e-BRAINS, Solid State Device and Materials SSDM, Fukuoka, Japan (2013).

# Elizabeth Buitrago - Curriculum Vitae

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## Education

- PhD Microsystems and Microelectronics, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, June 2014 (expected).
- MSc Process Engineering, Eidgenössische Technische Hochschule Zürich (ETHZ), Switzerland, September 2010.
- BSc Chemical Engineering, University of California San Diego (UCSD), USA, June 2005.

## Research

***PhD Thesis:*** **High Performance Vertically Stacked SiNW/Fin Based 3D FETs for Biosensing Applications, October 2010 – Present**

**Nanolab – EPFL: Prof. A. M. Ionescu, Dr. M. Fernández-Bolaños**

Research, development, simulation (3D TCAD-Sentaurus process, device) and fabrication of silicon nanowire (junctionless and vertically stacked) field effect transistors (FET) for their implementation into robust biosensing systems. Surface modification for pH and streptavidin (model systems) sensing and electrical characterization. Multi-institution (Tyndall National Institute, Imperial College London and EPFL) cooperation within two European projects: e-Brains and SiNAPS. Teaching and supervision of master students. **Proficiency in semiconductor fabrication/tools:** e-beam lithography, chemical vapor deposition (CVD), atomic layer deposition (ALD), dry, wet etch, scanning electron microscopy (SEM), focused ion beam (FIB), ion implantation, etc.

***Master Thesis*****: Plasma Surface Modification of Powders with Various Precursors, March 2010 – August 2010**

**Transport Processes and Reactions Laboratory – ETHZ: Prof. R. Von Rohr, Dr. C. Roth**

Temperature sensitive substrate powders were treated in a plasma enhanced chemical vapor deposition (PECVD) downstream reactor and simultaneously dispersed and mixed with silica nanoparticles generated in the plasma process. Different organosilicon precursors were investigated for the optimization of flowability and wettability process parameters that are important for transportation, encapsulation, and dosing among other applications. **Analytical methods**: ATR-FTIR, flow-

ability determination with ring shear tester, laser diffraction for particle size distribution, tensiometer for contact angle determination.

**$SnO_2$ with Ag Nanoelectrodes for Sensing Ultra-Low Acetone Concentrations, Spring 2009**
**Particle Technology Laboratory (PTL)**
**ETHZ: Prof. S. Pratsinis, Dr. H. Keskinen, Dr. A. Tricoli**
Sensitivity and selectivity of nanostructured sensors with Ag nanoparticles as nanoelectrodes deposited below a functional porous $SnO_2$ nanostructured film as synthesized by flame spray pyrolysis (FSP) direct deposition were investigated for the detection of ultra-low concentrations of acetone as applicable for diabetes diagnostics. **Analytical methods:** X-ray diffraction (XRD), BET nitrogen adsorption, etc.

**The Effect of Dopants on $TiO_2$ Solar Cell Efficiency, Spring 2009**
**Particle Technology Laboratory (PTL)**
**ETHZ: Prof. S. Pratsinis, Dr. A. Teleki, Dr. A. Tricoli**
Nb, Ru and Fe doped titanium dioxide nanoparticles were synthesized by a one-step FSP technique. $TiO_2$ band-gap reduction by doping for future investigation of its effect on the efficiency of dye sensitized solar cells. **Analytical methods:** UV-vis, etc.

**REU (Research Experience for Undergrads), summer of 2003 and 2004**
**Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, University of Arizona: Prof. F. Shadman**
Developed photocatalytic stainless screen meshes for degradation of extremely low concentrations of organics using Sol-Gel methods and chemical vapor deposition of $TiO_2$.

**Laboratory Technical Training Program, La Jolla CA, January 2003 – April 2003**
**Practical lab experience at UCSD, inhibition of rabbit muscle isozymes by Vitamin C: Prof. P. Russell, Dr. A. Williams**
Received training in laboratory techniques, centrifuge, UV/VIS spectrometry, enzyme assays, protein purification, statistical analysis.

## Industrial Experience

**Micron Technology, Manassas VA, September 2007- October 2008**
***Process Engineer* 2 – Wet process, Shift, 300 mm Wafer FAB**

- Direct and sustain process improvements using statistical process control (SPC).
- Strategically identify and analyze process failures.
- Audit process recipes, configure hardware and use procedural methods to perform process enhancements.

- Identifying, understanding, and resolving defect issues, assisting area technicians trouble-shooting problems, improving preventative maintenance procedures, and optimizing overall tool performance.
- Proficiency across all wet process modules and toolsets is necessary in order to be able to dis-position lots efficiently, prevent scrap and continuously improve wet process capabilities.

**AMI Semiconductor, Pocatello ID, January 2006 – January 2007**

***Primary Process Engineer* – Metal Deposition and Rapid Thermal Processing**

- Worked directly with production and the engineering team to review existing procedures to identify and implement cost, quality and productivity improvements.
- Sustaining, data analysis, continuous improvement of current procedures, cost savings, new process introduction.

## Skills

Bilingual (Spanish, English), very basic (French, German)

## Honors and Activities

- Triton Engineering Council Representative for the American Institute of Chemical Engineers (AICHE) 2003-2005.
- Donald F. Othmer Sophomore Academic Excellence Award (AICHE).
- IEEE EPFL student branch member
- IEEE Transactions on Electron Devices (TED) Journal Reviewer