Technologies and Platforms for Cyberphysical Systems

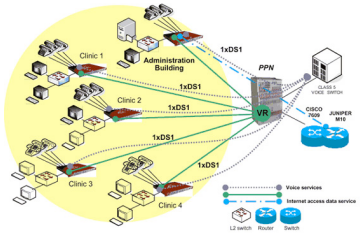
Giovanni De Micheli

Outline

- **Introduction**
- Technological innovations
  - Emerging nanotechnologies and devices
- Architectural trends
  - Multiprocessing, NoCs, and 3D integration
- Cyberphysical applications
  - The nano-tera.ch program
- Conclusions

Emerging societal and economic issues

- Strengthening welfare
  - Better, affordable health care and wellness
  - Dealing with ageing and young population
- Mitigating risks
  - Preventing catastrophes and pandemics
  - Monitoring the environment
- Ensuring sustainability
  - Smart energy production and distribution
  - Intelligent water management
- Enhancing security
  - Smart zero-emission data-center design
  - Preventing cyber and physical attacks

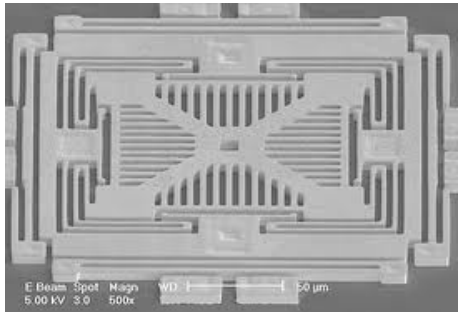


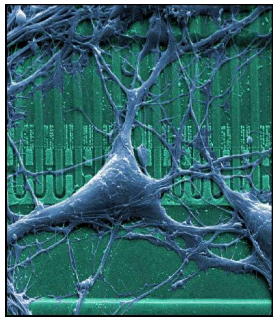
Cyberphysical systems

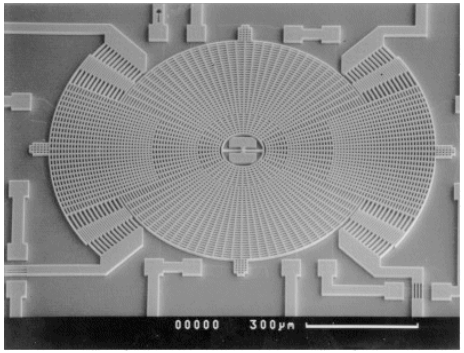
[Courtesy: J. Rabaey]

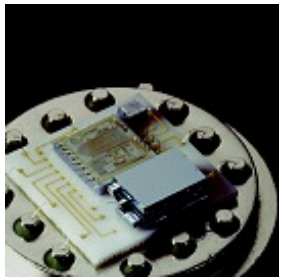
The sensory interface

- The *More than Moore* revolution









[Courtesy: ST]

[Courtesy: Carrara EPFL]

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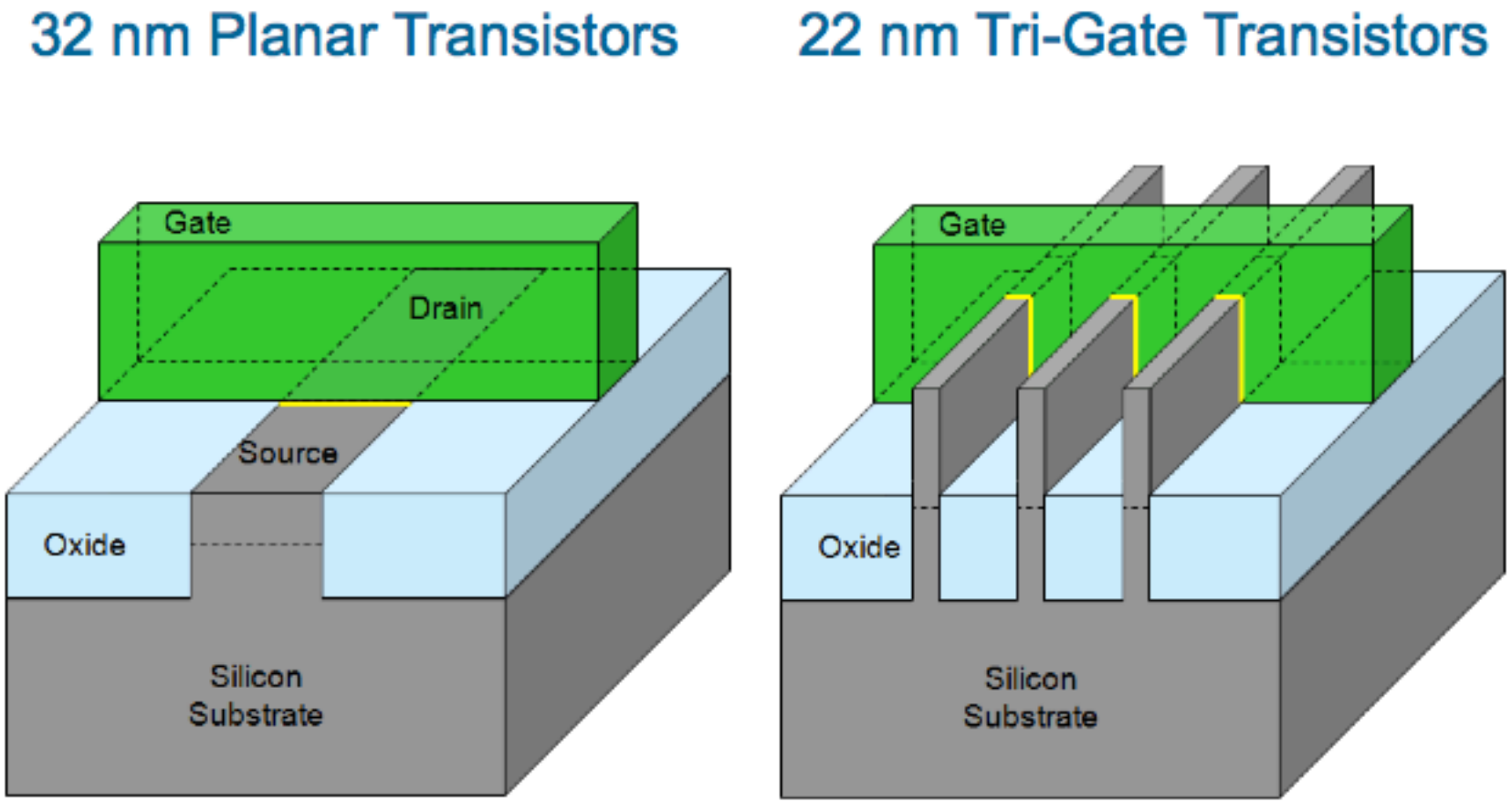
The emerging nano-technologies

- System technology is build bottom-up, starting from materials and their properties
- New devices exploit functional geometries at the molecular level
  - Quantum confinement
- There is a plethora of new materials and processing steps/flows
  - More than 50 elements in a regular CMOS process
- *Enhanced* silicon CMOS is likely to remain the main manufacturing process

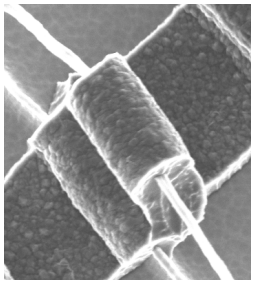
22 nm Tri-Gate Transistors

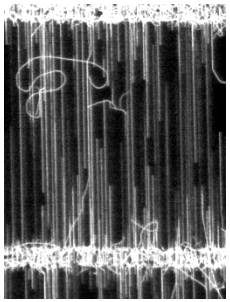


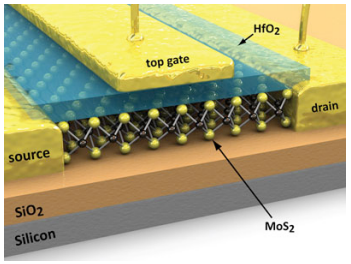
[Courtesy: M. Bohr]

Beyond CMOS

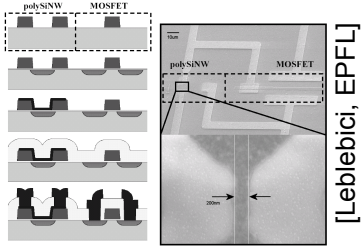
- Nano-technology provides us with new devices



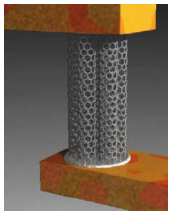




- Can they mix and match with standard CMOS technology ?



[Leblebici, EPFL]

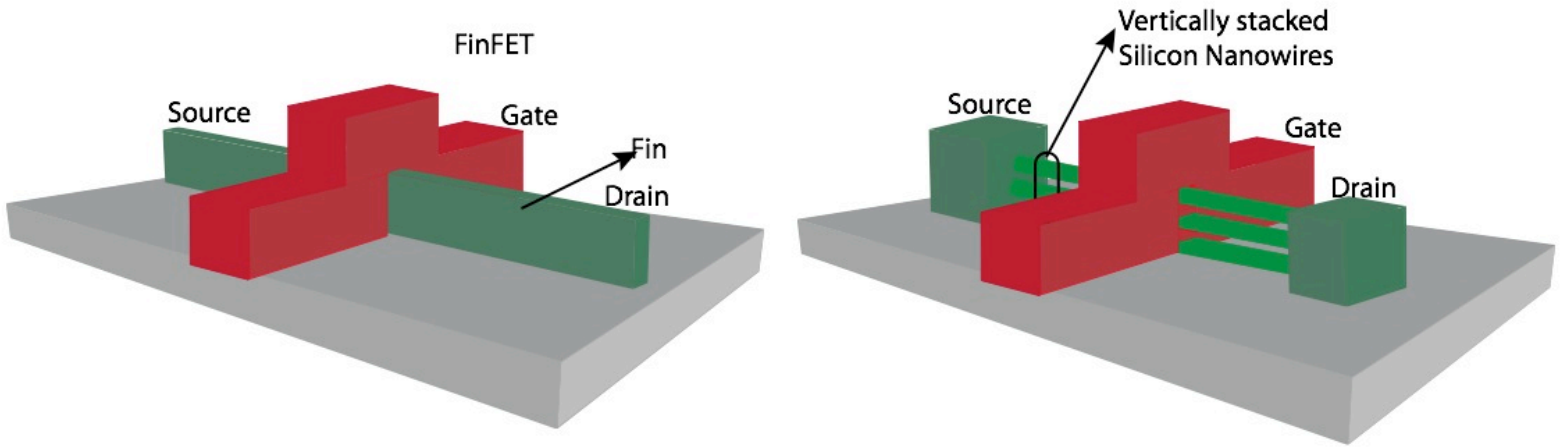


[Infineon]

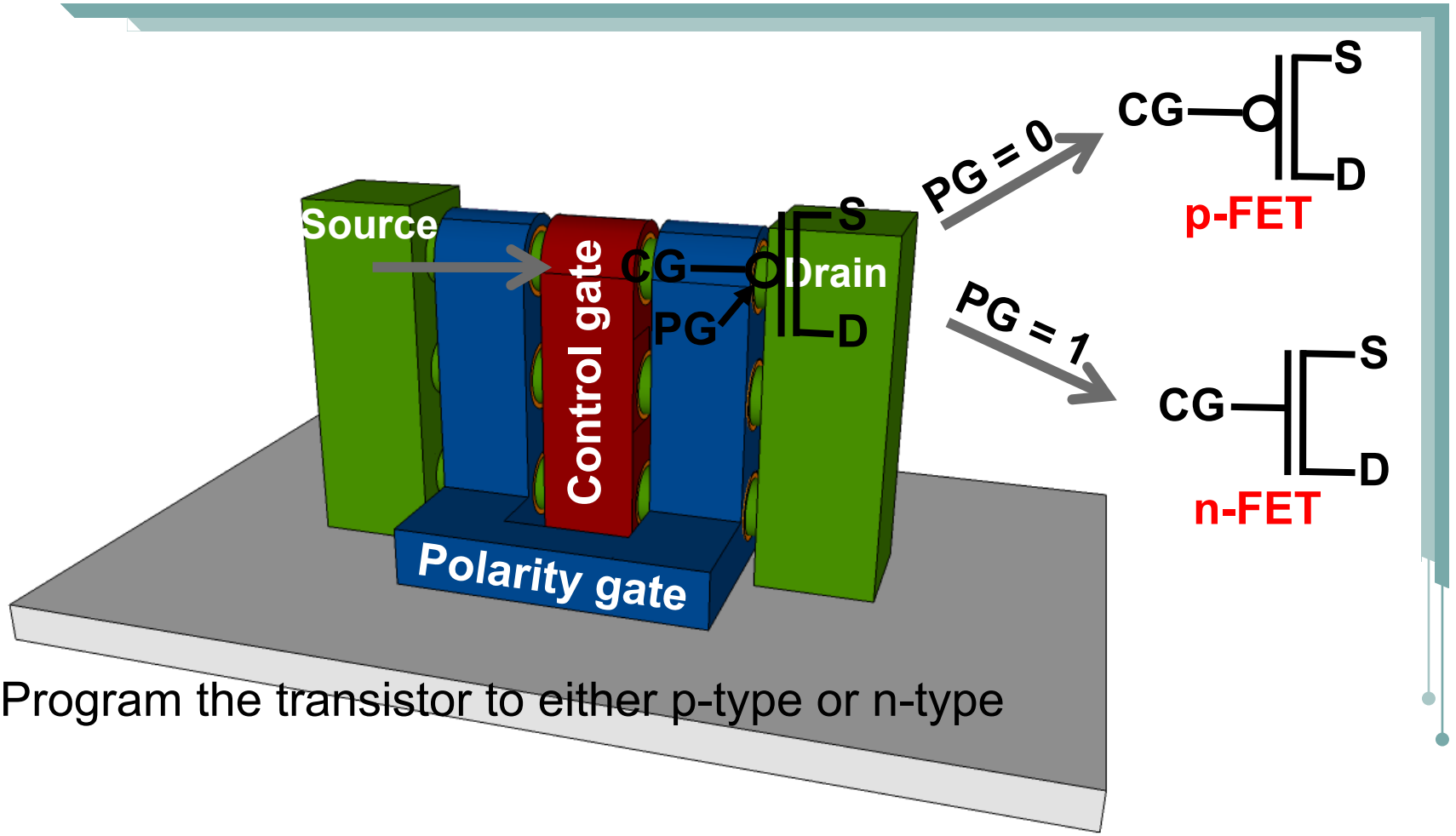
[Mitra, Stanford]

- What is the added value?

FinFETs versus SiNW FETs



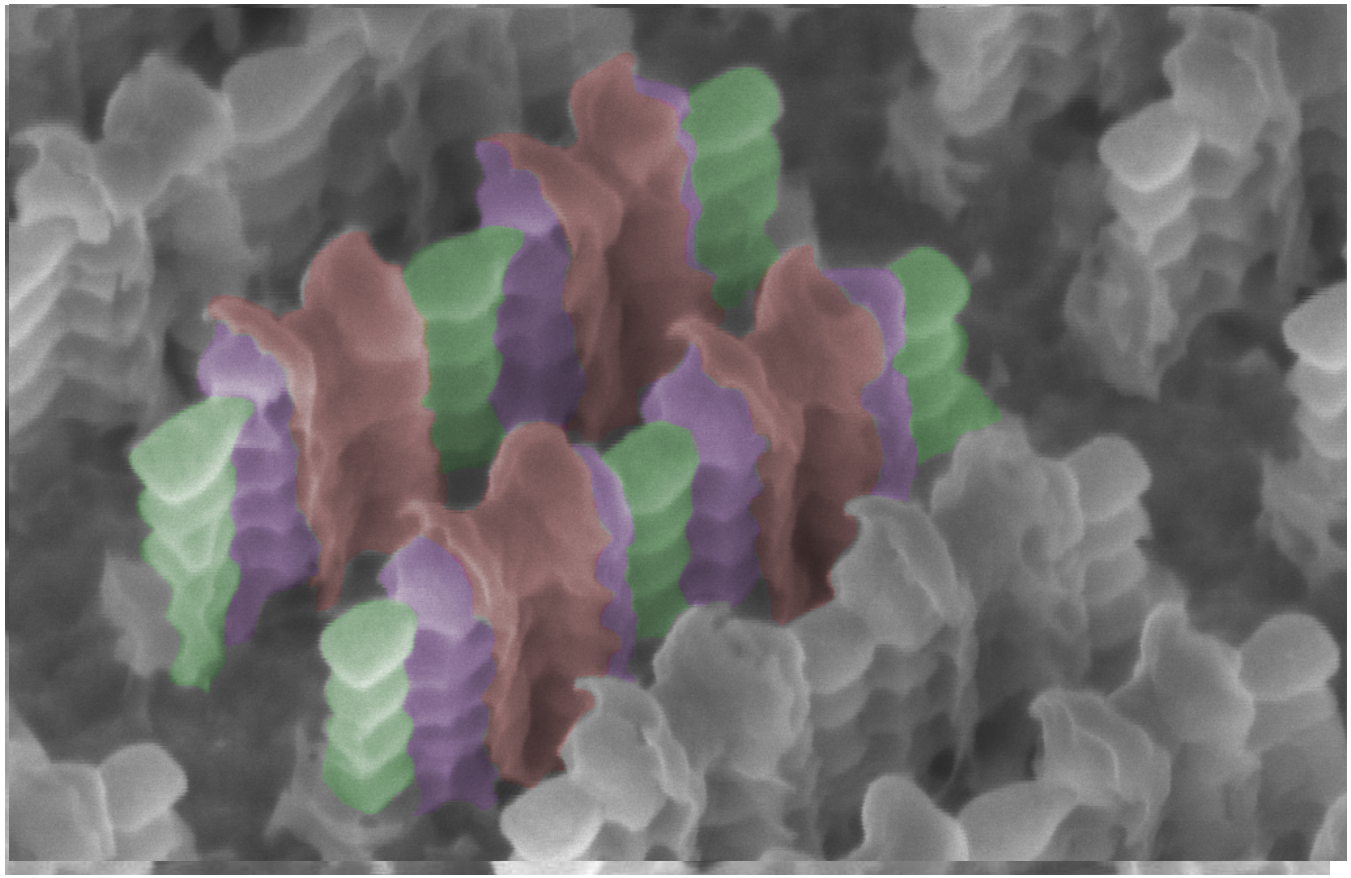
Double Independent gate SiNW FET



- Program the transistor to either p-type or n-type

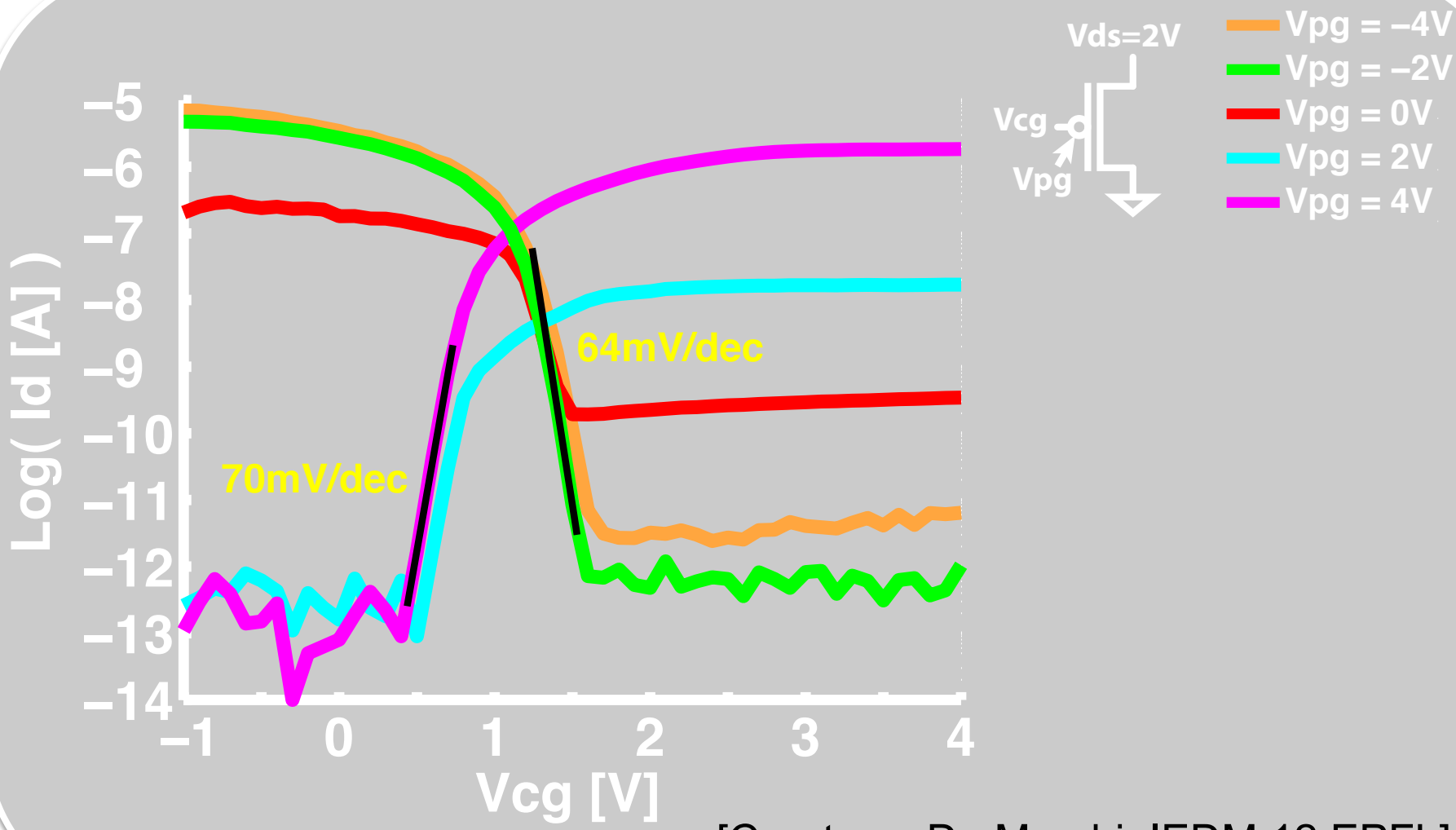
Silicon Nanowire Transistors

- Gate all around transistors
- Double gate to control polarity



[Courtesy: De Marchi, EPFL]

Device I_d/V_{cg}



[Courtesy: De Marchi, IEDM 12 EPFL]

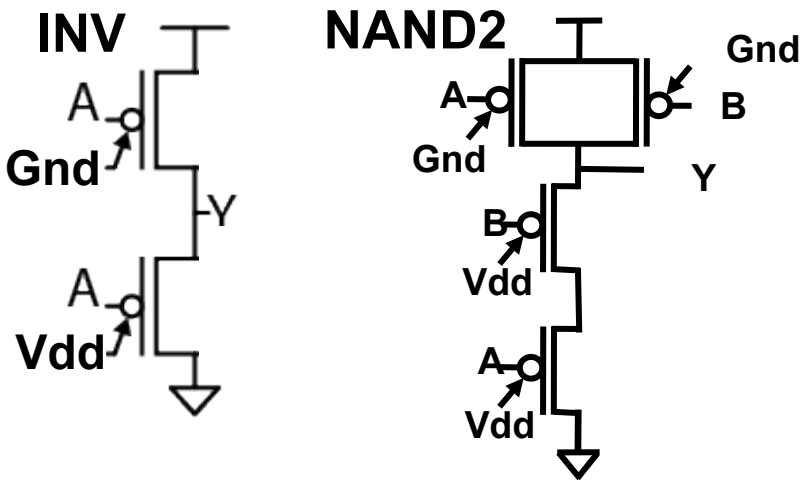
Logic level abstraction

- Three terminal transistors are switches
  - A loaded transistor is an *inverter*
- Controllable-polarity transistors compare two values
  - A loaded transistor is an *exclusive or* (EXOR)
- The intrinsic higher computational expressiveness leads to more efficient data-path design
- The larger number of terminals must be compensated by smart wiring

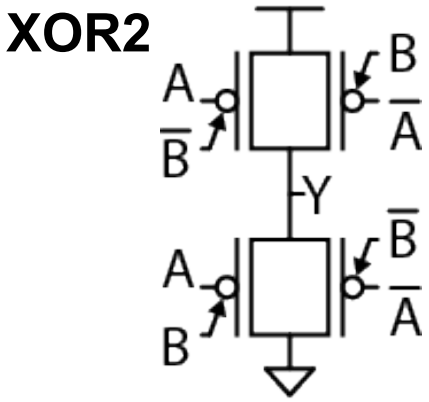
New Design Paradigm: Ambipolar Logic

- CMOS complementary logic efficient only for negative-unate functions (INV, NAND, NOR…etc)
- Ambipolar logic is efficient for both unate and binate functions
- Optimal for XOR and XNOR dominated circuits

Negative Unate functions	Binate functions



Similar to regular CMOS

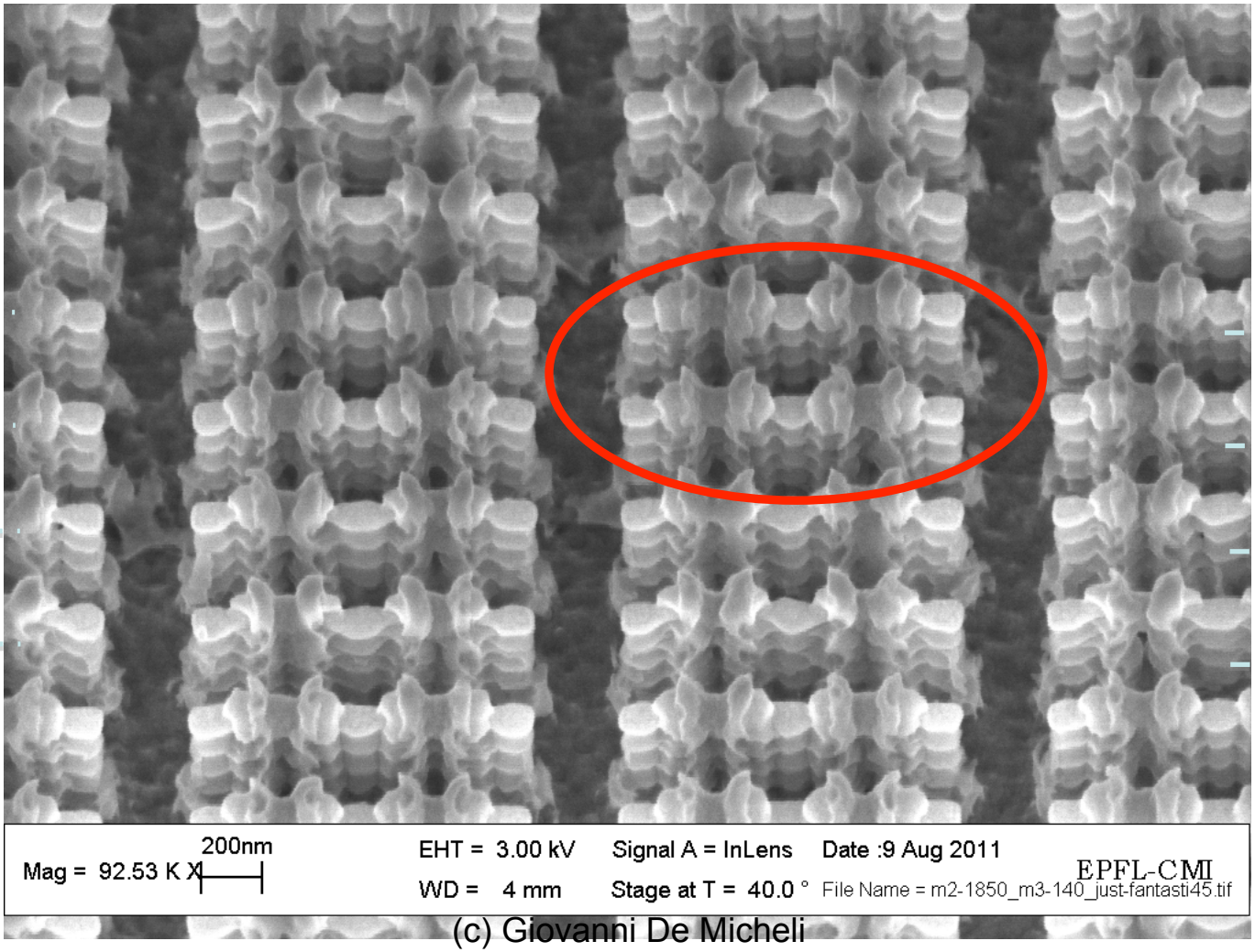


Only 4 transistors when compared to 8 transistors with a regular CMOS

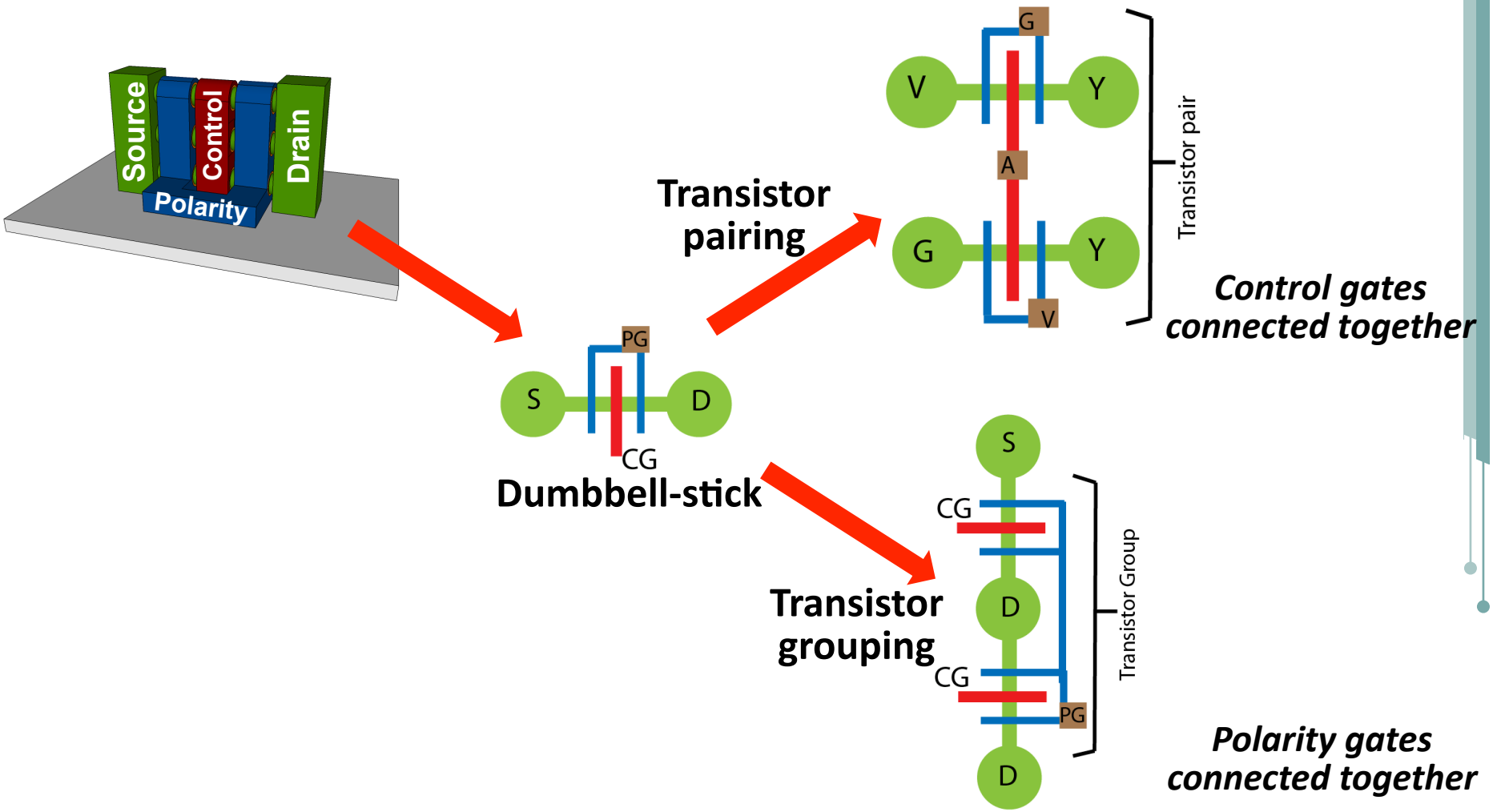
[Courtesy: H. Ben Jamaa, '08]

Sea-of-Tiles (SoT)

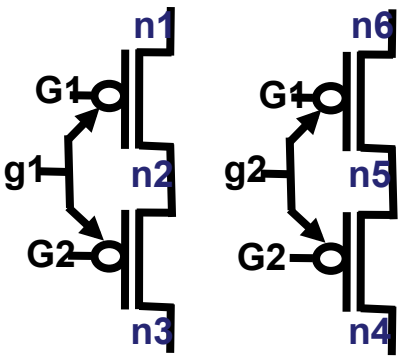
- Homogeneous array of Tiles

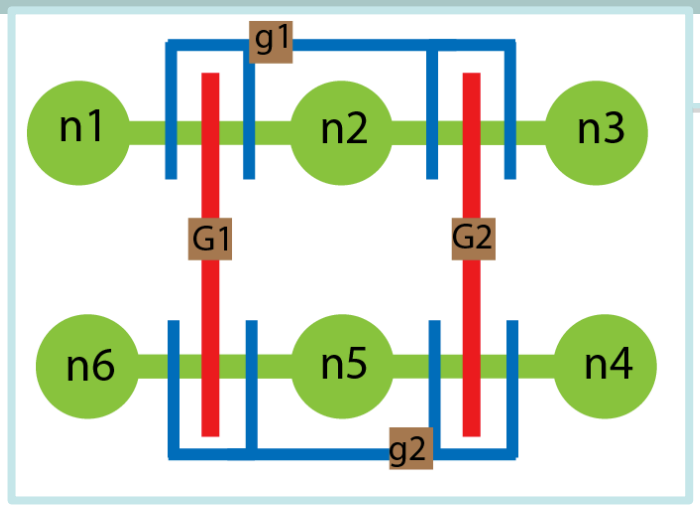


Dumbbell-stick diagrams



Layout abstraction and regularity with *Tiles*

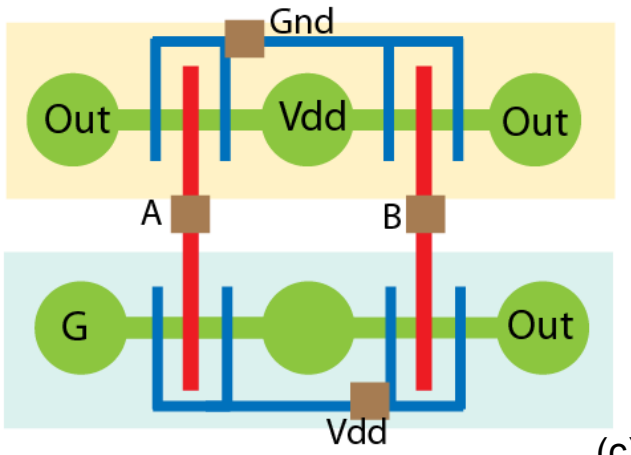




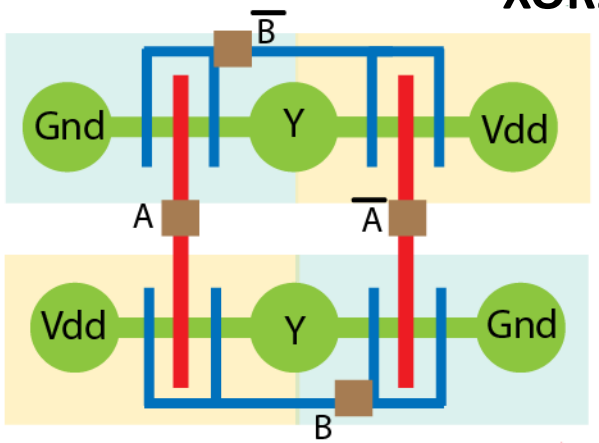
Tile

Two transistor pairs grouped together

NAND2



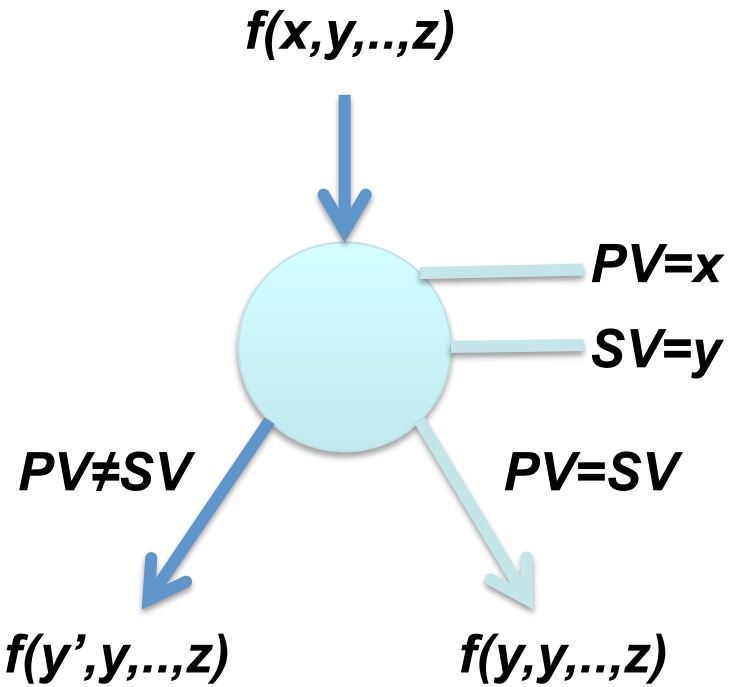
XOR2



[Courtesy: Bobba, DAC 12]

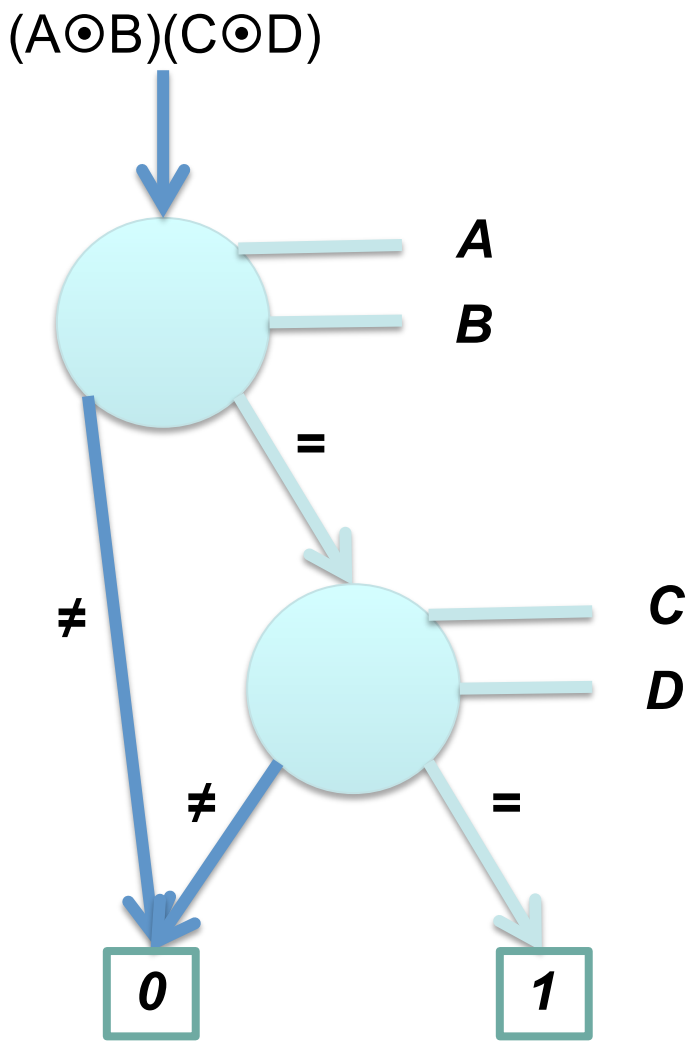
Biconditional Binary Decision Diagrams

- Binary Decision Diagrams where Shannon's expansion is replaced by the *biconditional* expansion
- *Biconditional* expansion: $f(x,y,..,z) = (x \oplus y) f(y',y,..,z) + (x \overline{\oplus} y) f(y,y,..,z)$



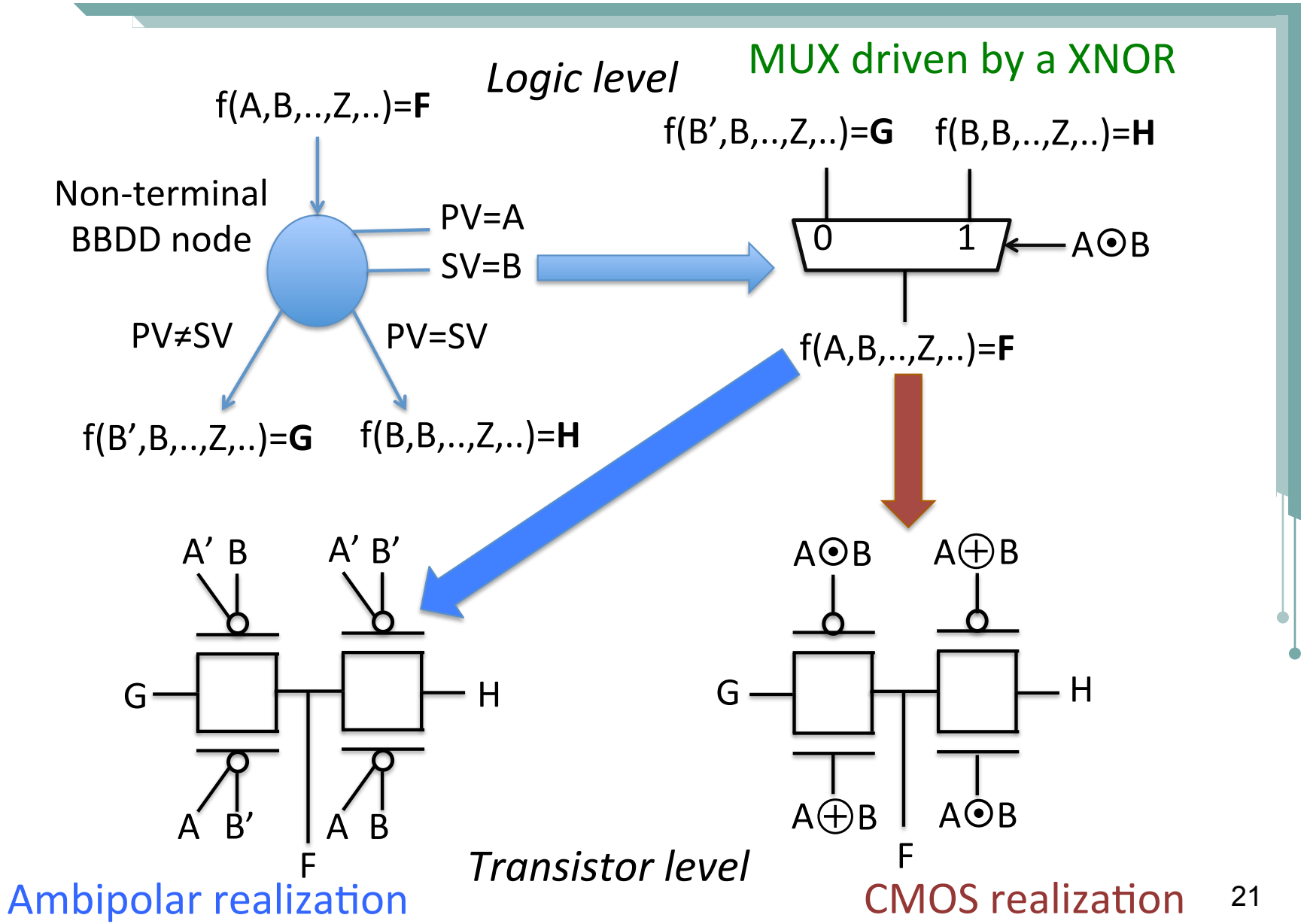
- Each BBDD node:
  - Has two branching variables
  - Implements the *biconditional* expansion
  - Reduces to Shannon's expansion for single-input functions

BBDD: Example (A⊙B)(C⊙D)

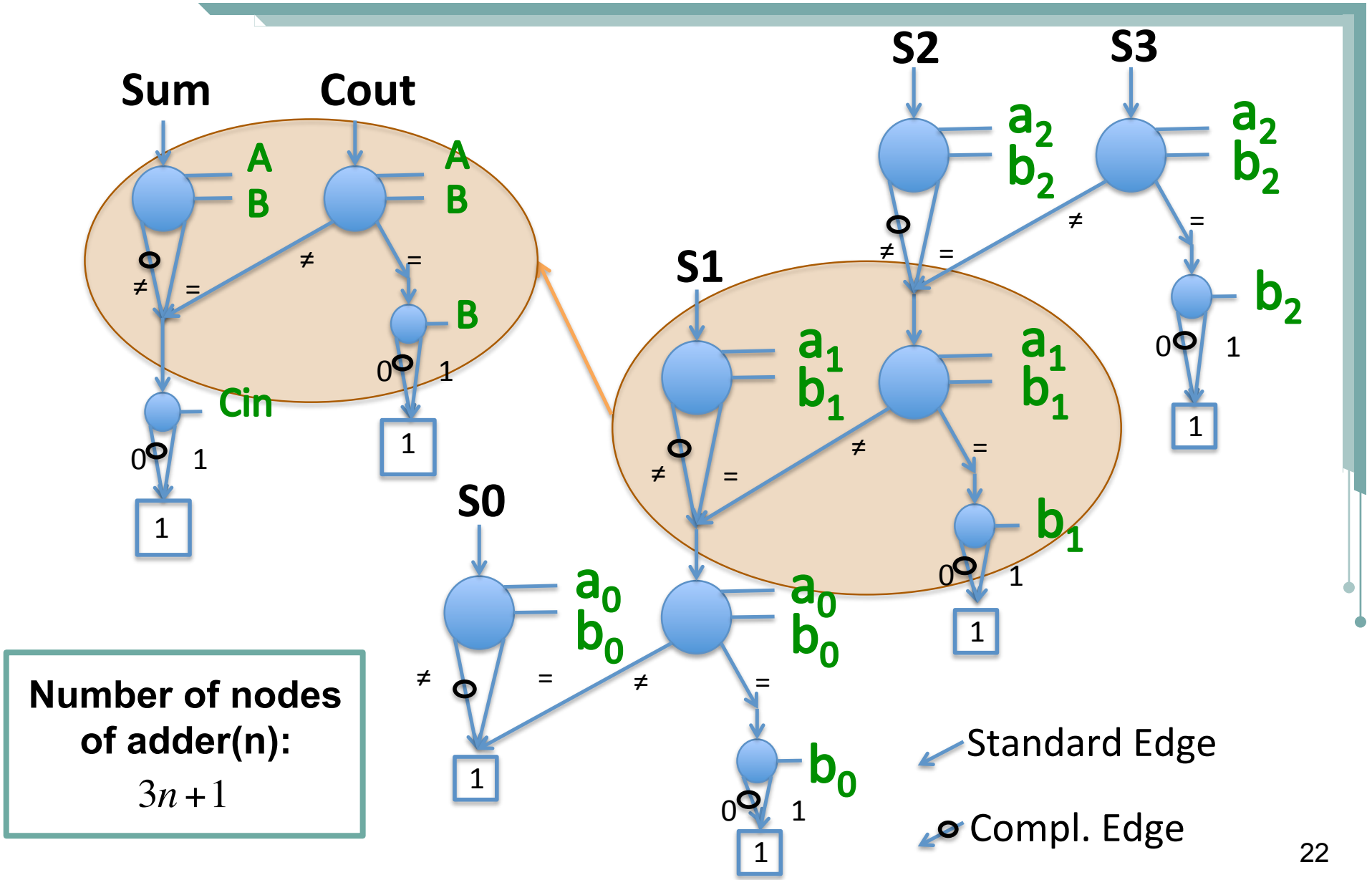


(A⊙B)(C⊙D):
if A==B, then
if C==D, then
true
else **false**
else **false**

Efficient Direct Mapping of BBDD Nodes



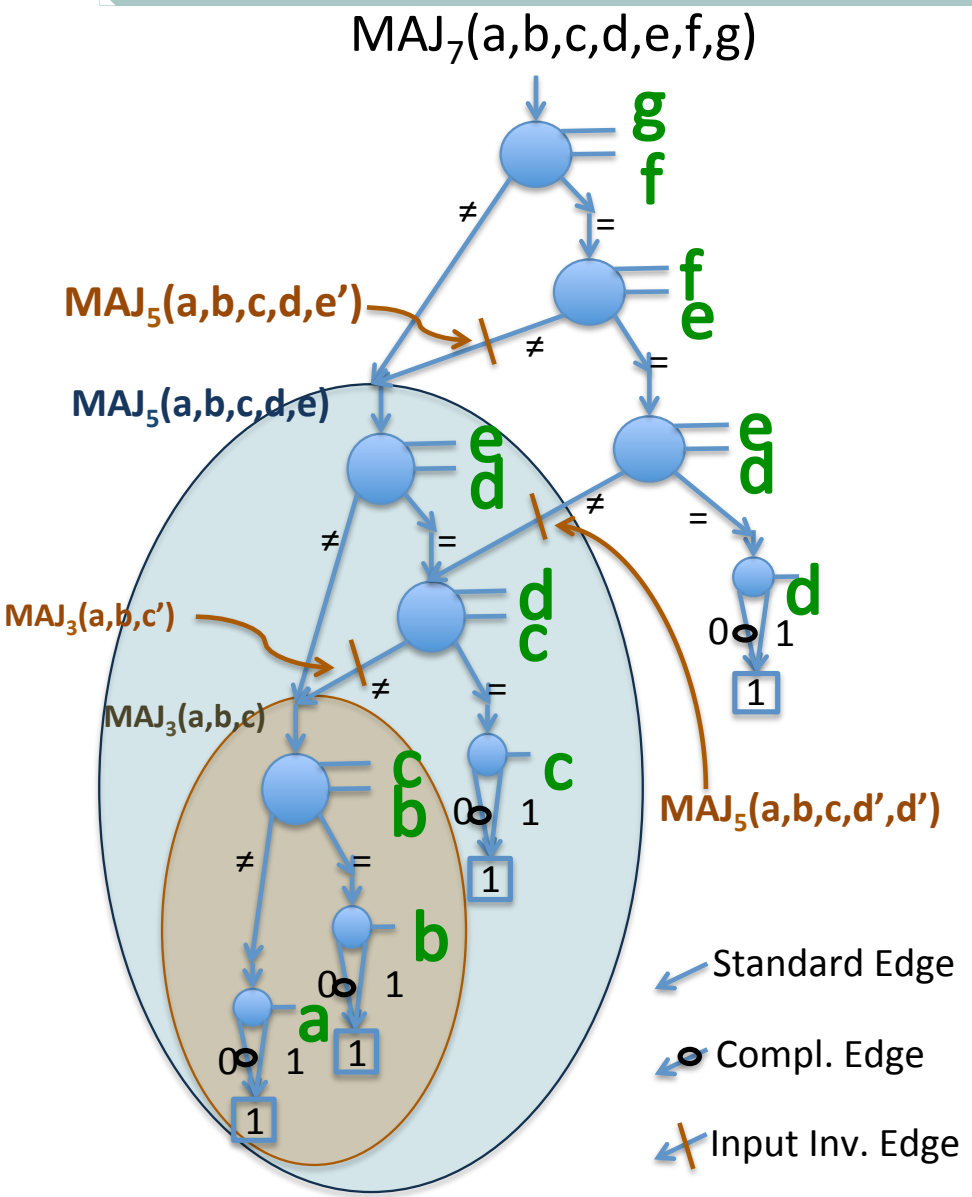
BBDDs are Compact (Adder Function)



Number of nodes of adder(n):

$3n+1$

BBDDs are Compact (Majority Function)



Number of nodes of MAJ(n):

$$\frac{1}{8}n^2+\frac{1}{2}n+\frac{11}{8}$$

MAJ(3): 4

MAJ(5): 7

MAJ(7): 11

....

Summary – technological innovations

- New materials and new device geometries
  - Silicon FIN-FETs and NanoWires
- New-properties
  - Controlled polarity transistors
- Design opportunities
  - More efficient design of data paths and computational units
  - Higher computational density

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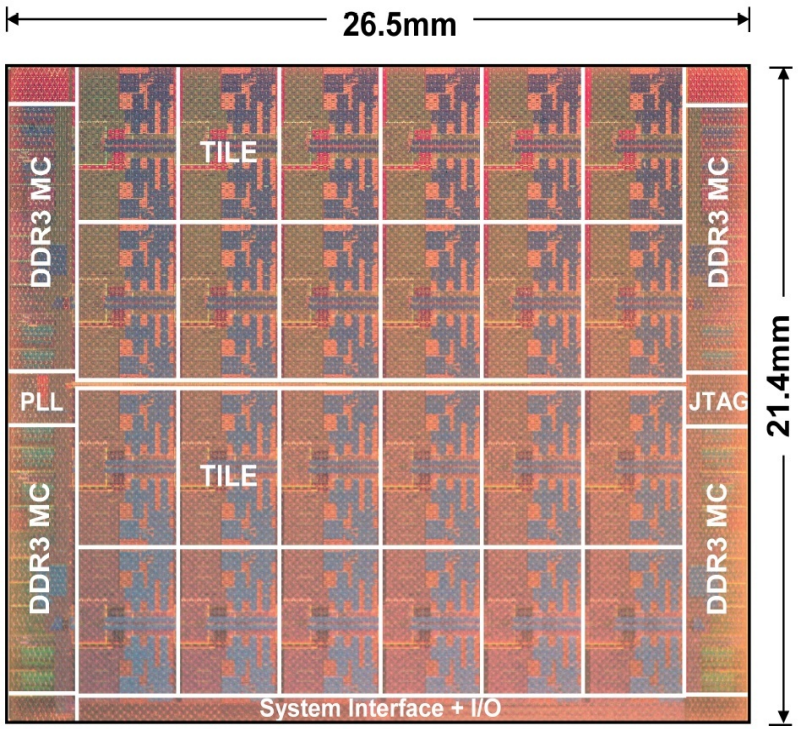
System architectural trends

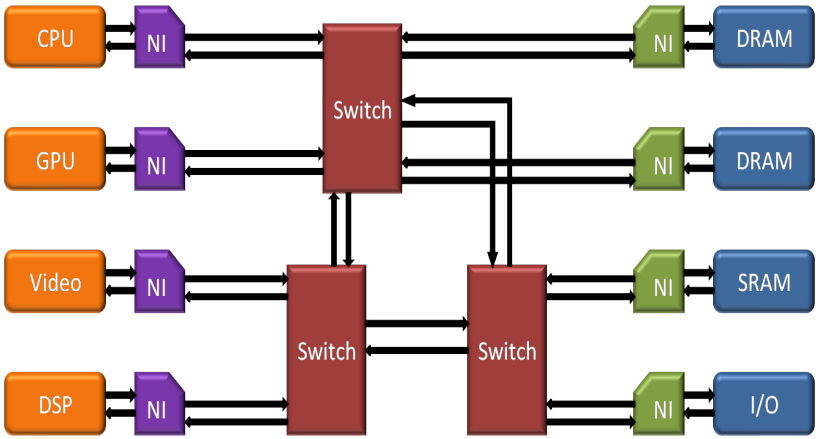


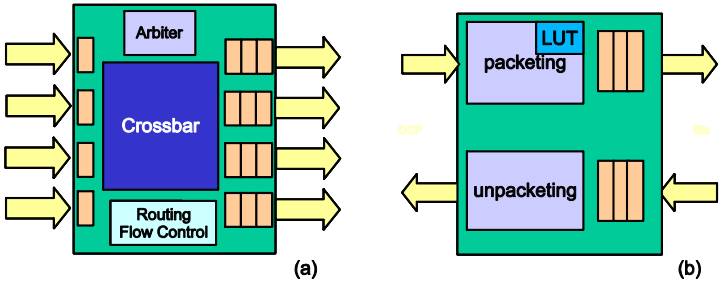
Intel Single-Chip Cloud Computer

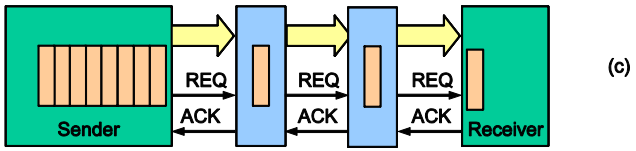
[Courtesy: Hoçward, ISSCC 2010]

- Move towards many-core
  - Frequency scaling has leveled-off
  - Exploit application-level parallelism
- On-chip communication
  - Bottleneck for system performance
- Networks-on-Chip (NoC)
  - Adopted as scalable interconnect
  - [Benini & De Micheli 2002]

Networks-on-Chip Scalable Interconnect





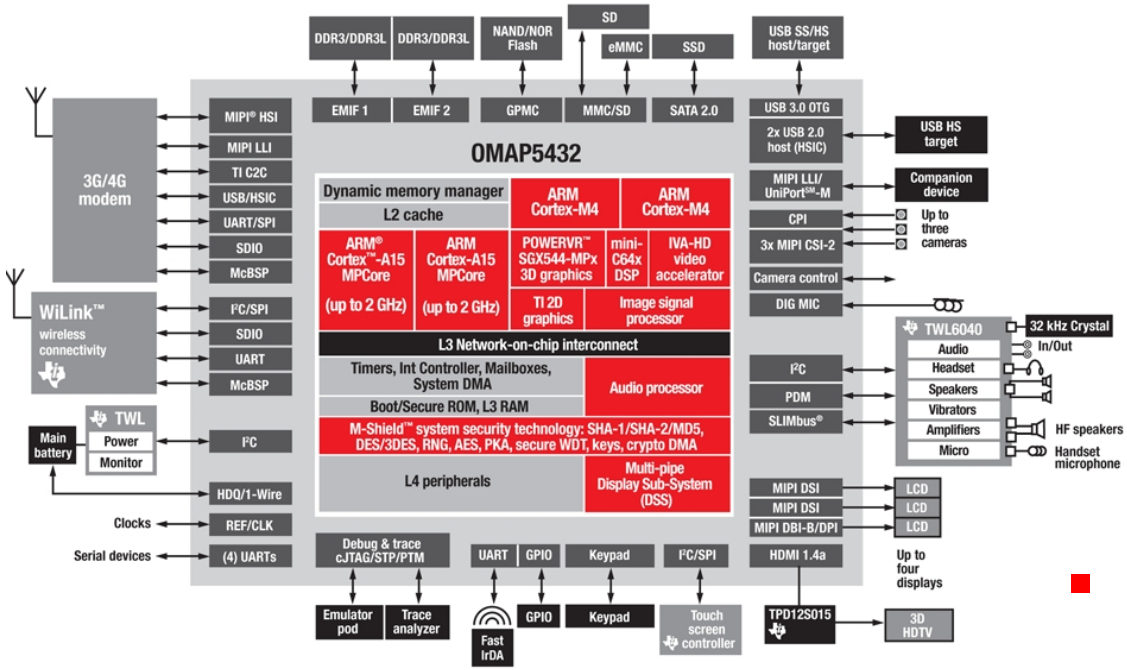


xpipes library

[Courtesy: Stergiou DATE 2005]

- NoC modular architecture
  - Network Interfaces (NIs)
  - Switches
  - Links
- Scalable
  - Multiple parallel transactions
  - Segmented point-to-point wires
- Used in prototypes and products
  - Intel Polaris, SCC, Bone
  - TI OMAP, Tilera TILE-Gx

Specialization for Power Efficiency

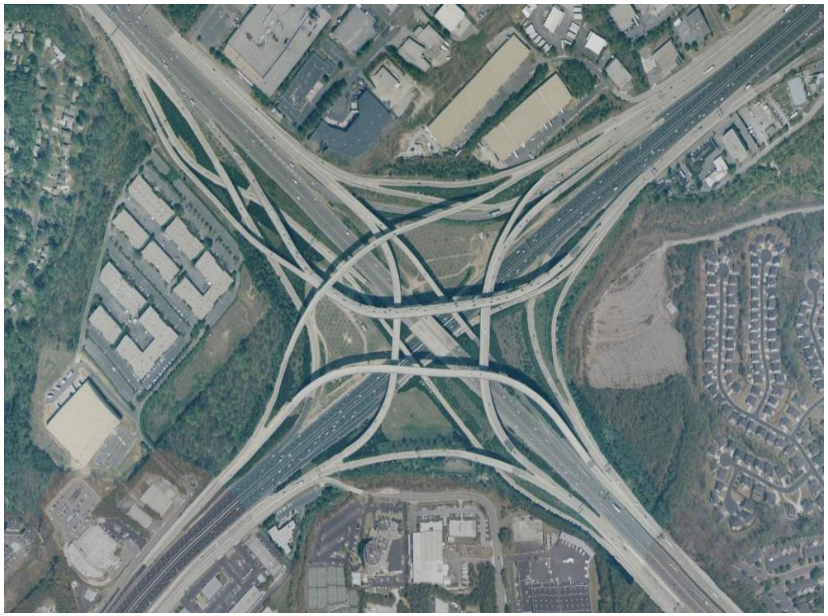


TI OMAP 5 application platform

- Limited power budget for mobile applications
  - Trade-off programmability for power-efficiency
  - Specialized heterogeneous IP-cores
- Communication is a major power consumer
  - Traffic patterns are known
  - Application specific NoC design is needed

Application specific NoCs

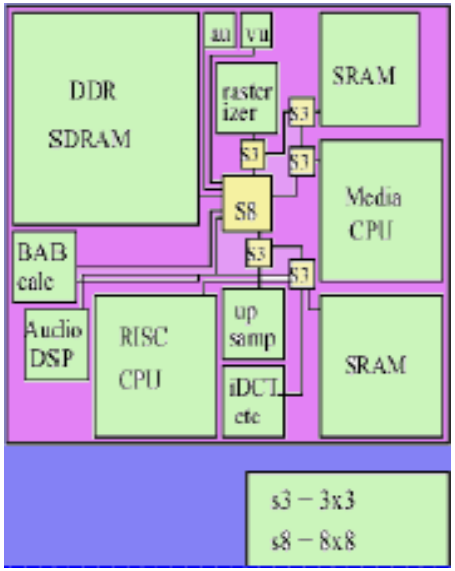
?

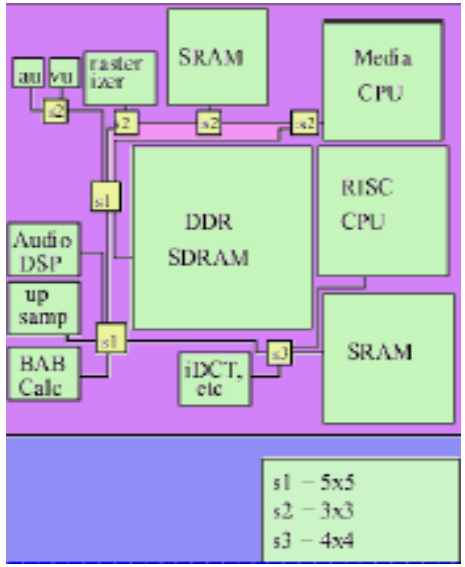


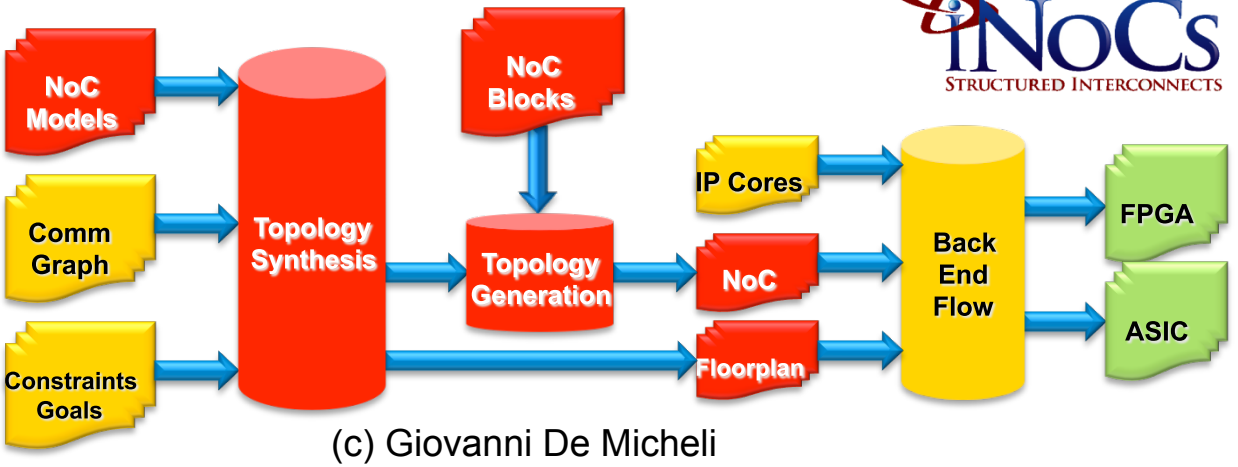
- Challenges
  - Many parameters (i.e., data-size, frequency, connectivity)
  - Tools are required to find the best topology
- New technologies
  - More IP-cores
  - More constraints (i.e., 3D-IC vertical connectivity)

Design automation for NoCs

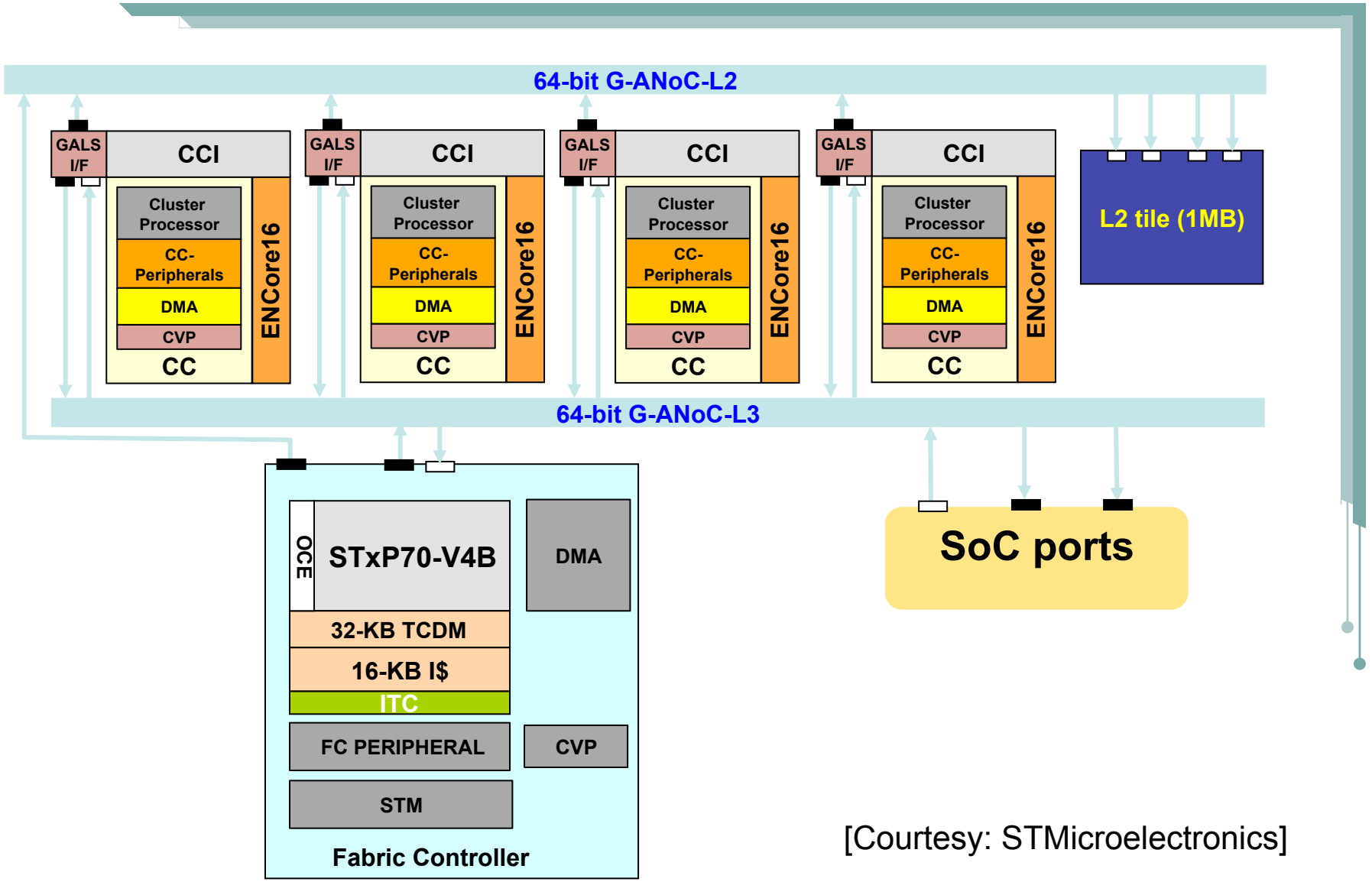
- Large design space
  - What topology ?
  - Which mapping ?
  - Which routes to use ?
- Optimize parameters
  - Link width, buffer sizes
- Simulate, verify, test





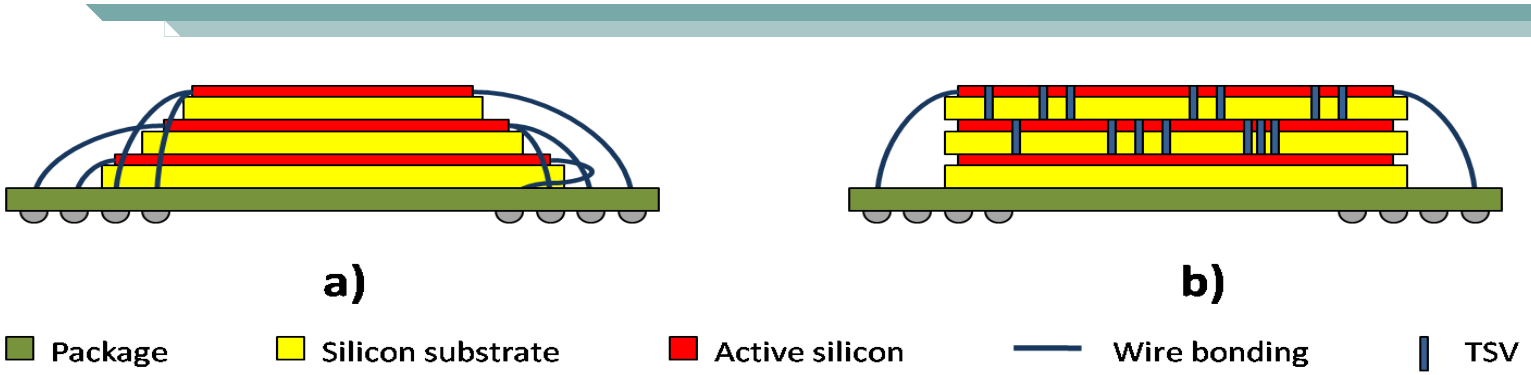


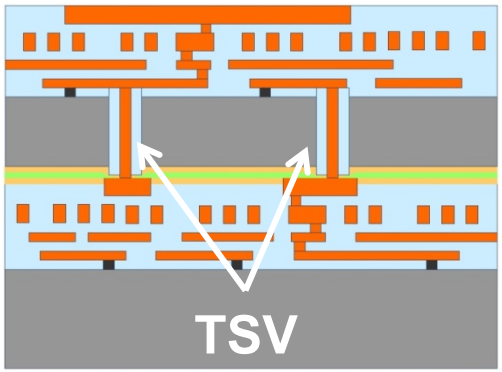
STHORM ANoC



[Courtesy: STMicroelectronics]

Three Dimensional Integration



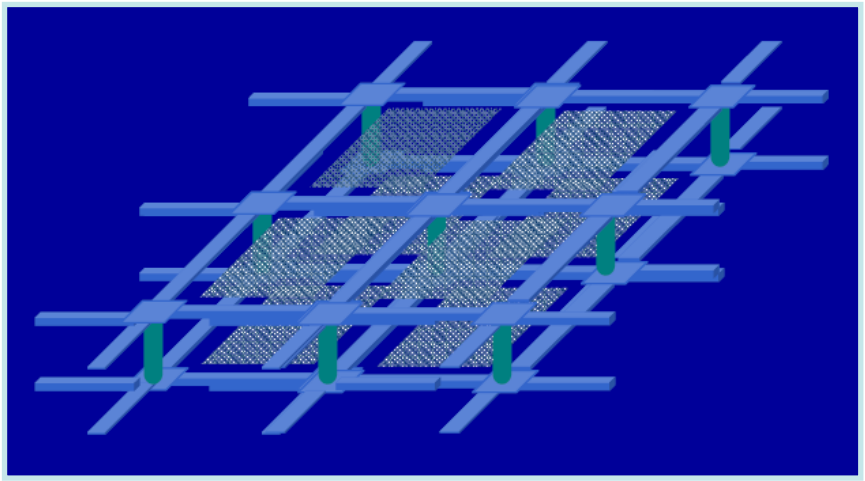


[E. Beyne ITC 06]

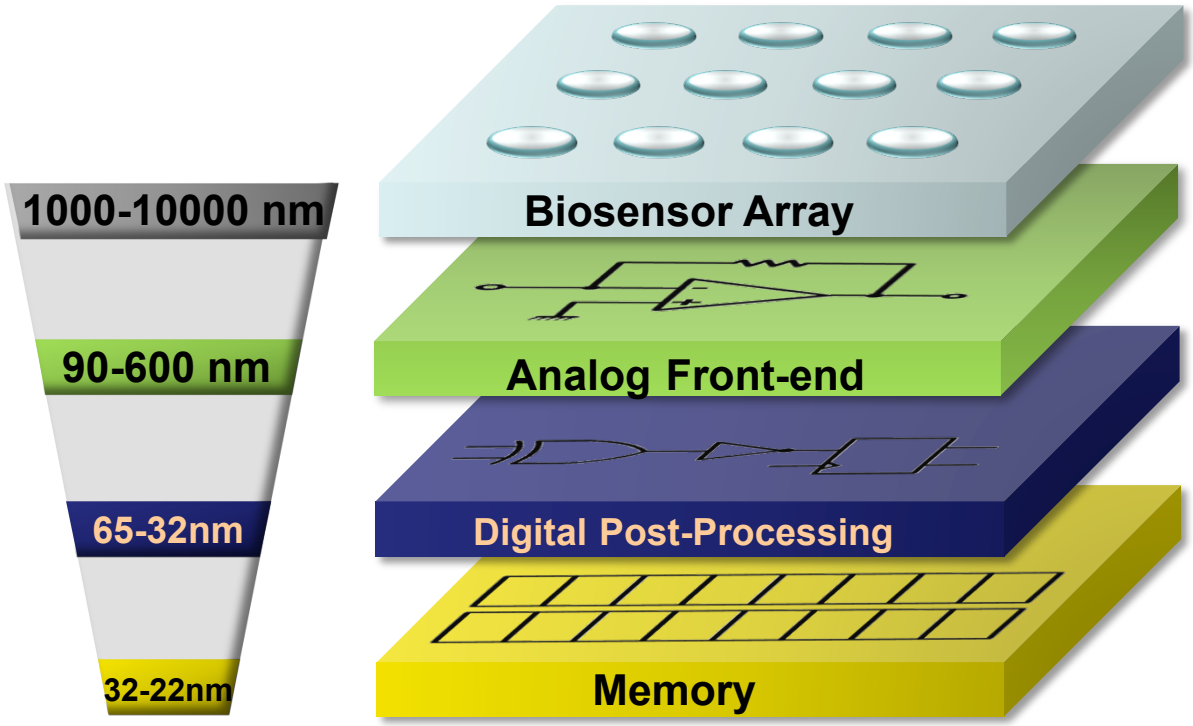
- System in Package
  - Better form factor
  - Limited vertical connectivity
- Monolithic Integration
  - New experimental process (LETI)
  - New use of RRAMs in BEOL
- Stacking with *Through Silicon Vias*
  - Reduce average length of on-chip global wires
  - Increase performance
    - Processor/memory systems – Wide I/O
  - Heterogeneous integration

3D NoC Design

- Use NoCs to support Wide I/O
- Challenges:
  - Meet application constraints in a 3D structure
    - Bandwidth, latency
    - Which topology, switches, layers and floorplan locations?
  - Meet 3D technology constraints
    - Maximum available TSV constraints
    - Communication between adjacent layers



Extending 3D Integration to sensing



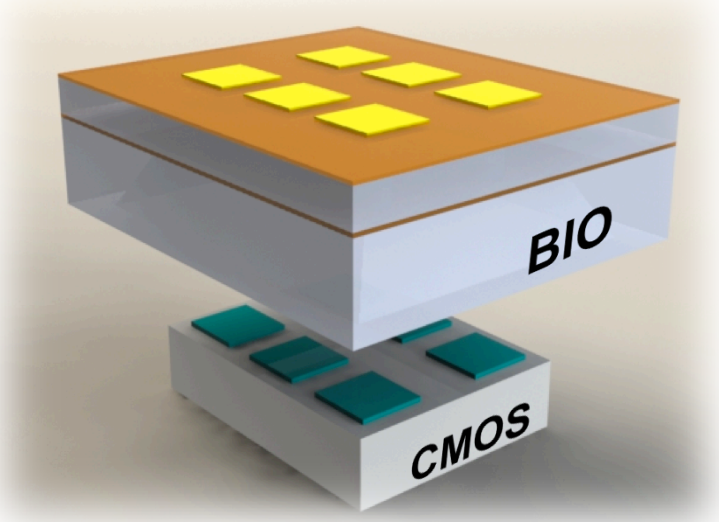
Custom micro-fabrication for the bio-layer

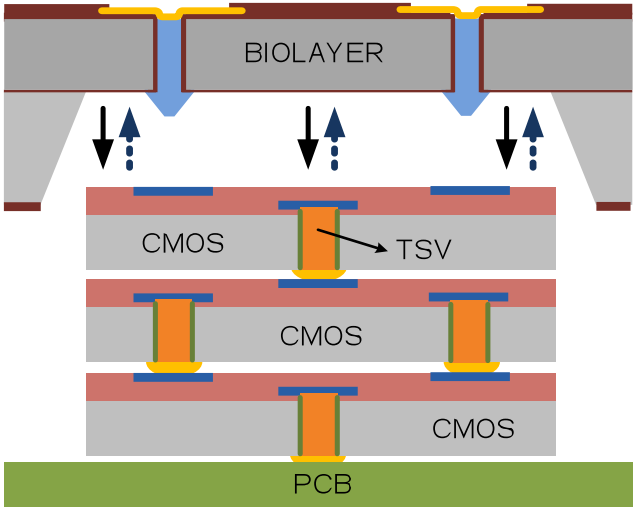
Technologies enabling low noise operation for the analog circuits

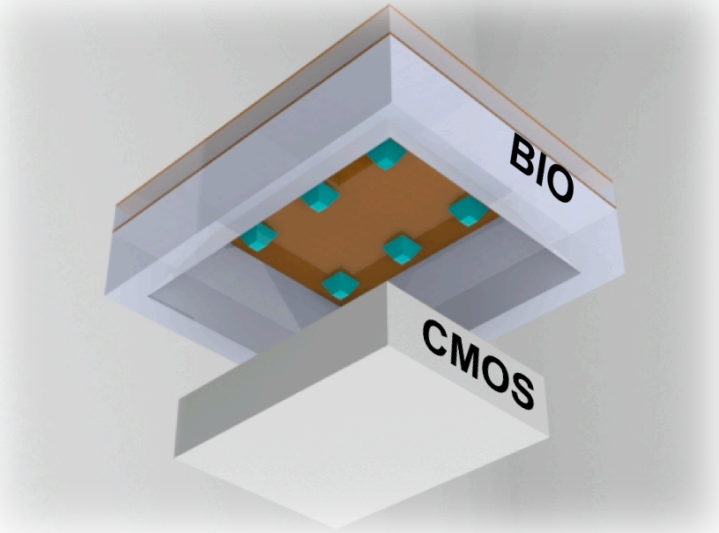
High speed/density CMOS technologies for digital circuits and memories

[Courtesy Guiducci: 2010]

Disposable bio-layer



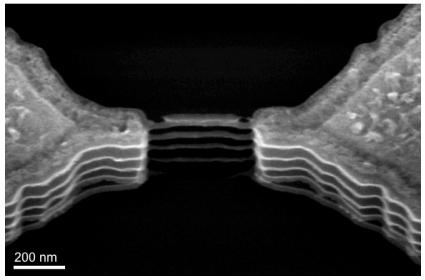


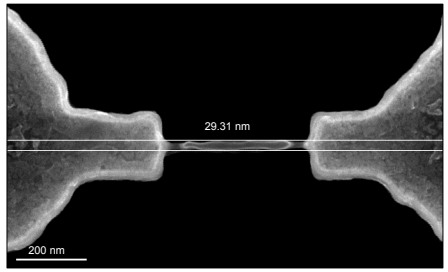


- No need for cleaning. Bio-layer is disposed after each measurement and CMOS layers are used repeatedly
- Increased sensitivity and array density due to vertical interconnections from the bio-layer to the readout electronics
- Sophisticated algorithms for highly-specific target identification run on-chip DSP and memory

[C. Guiducci 2010]

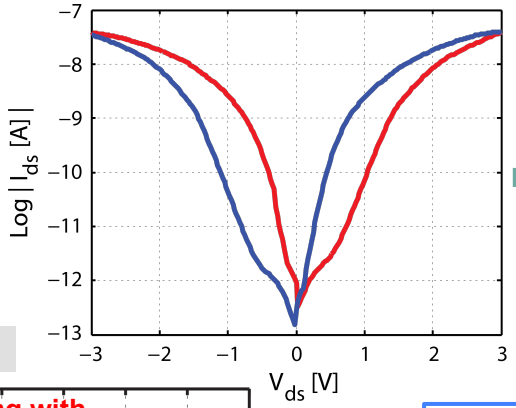
Memristive SiNW-based Biosensors

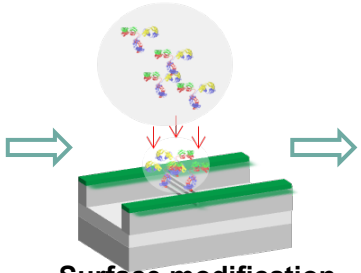


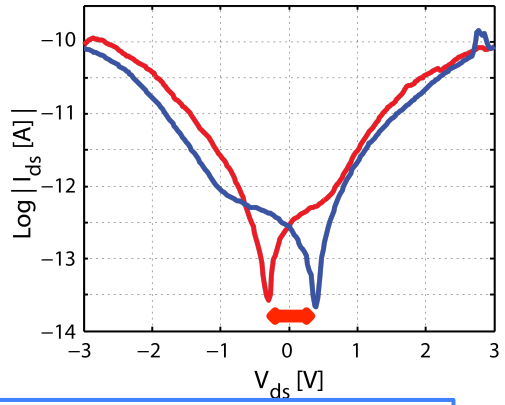


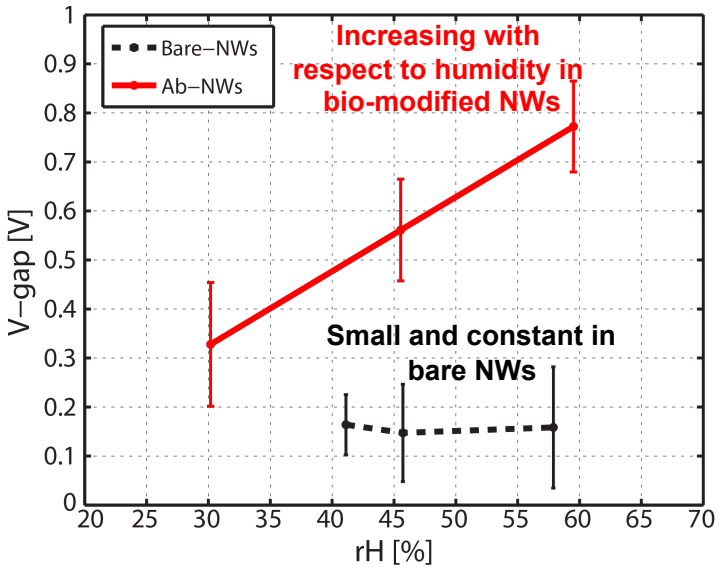
F. Puppo, IEEE T. Nanobiosci., submitted

- Crystalline, free-standing, Silicon Nanowires manifest memristive conductivity due to the nano-scale of the fabricated structures
- The voltage-gap between the forward and backward current minima in I/V curves increases after NW functionalization with antibodies

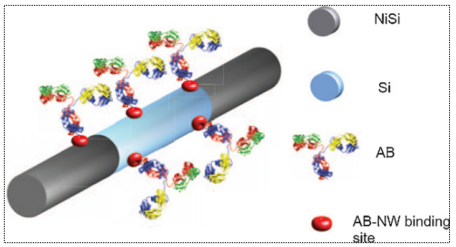








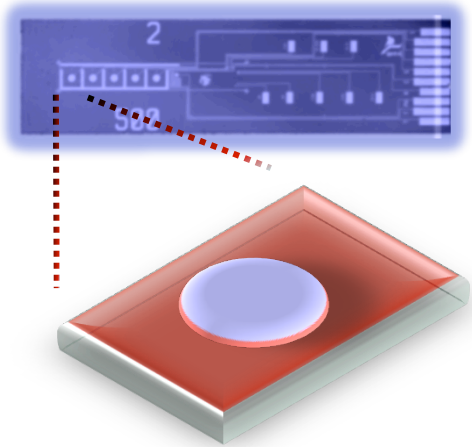
In a controlled humidity range, Si NW device sense antigen molecules (i.e., cancer biomarkers) thanks to molecule up-take (immuno-recognition events) displayed by voltage gap changes.



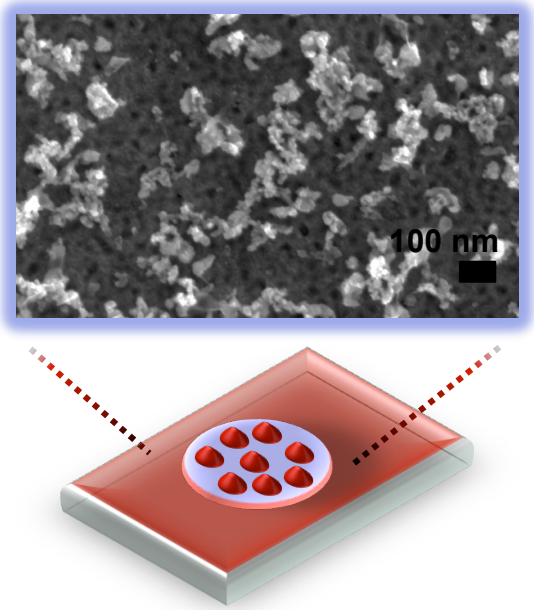
S. Carrara et al. ,
Sens. Actuators B, *2012*

CVD-MWCNTs for electrochemical biodevices

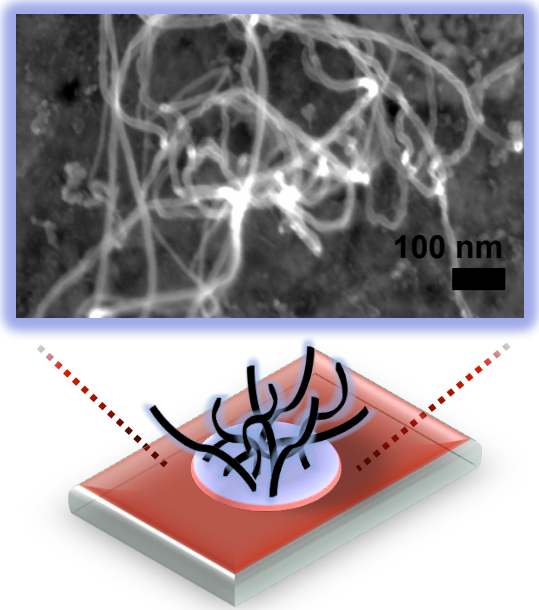
1. Microfabricated biosensor



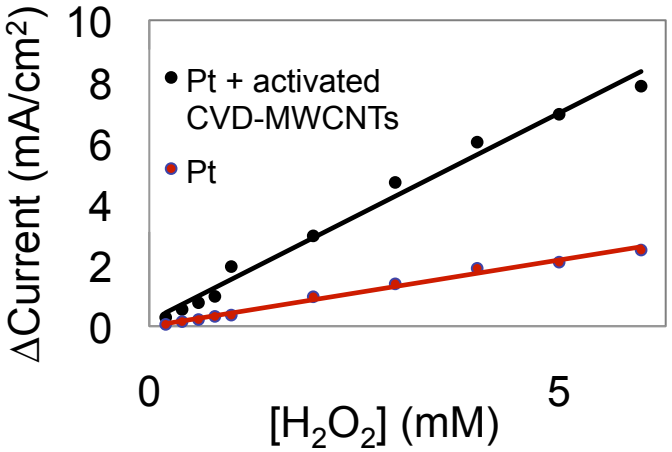
2. Iron catalyst nanoparticles electrodeposition



3. CVD-MWCNTs grown onto working electrodes



4. Electrochemical detection of a biocompound by using Pt electrodes nanostructured with CVD-MWCNTs

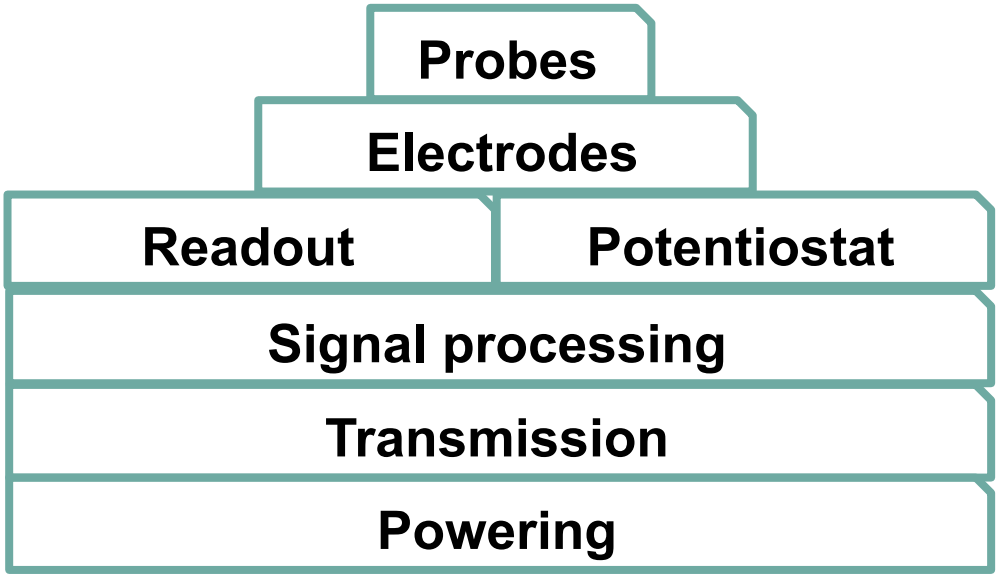


Objective

MWCNTs directly grown by CVD onto Pt microelectrode-array to enhance sensing performance of electrochemical biodevices

Integrated sensing platforms

- Specific components
  - Probes and electrodes
  - Chambers and fluidic circuits
- Electronic components
  - Transconductance amplifier and data conversion
  - Transmission and powering



Summary – architectural trends

- Multi-processing *component-based* design paradigm
- Networks on Chip to address communication challenge
  - Adopted by virtually all manufacturing companies
  - Different flavors to address different application domains
- 3-Dimensional integration
  - Lower latency in multiprocessing system
  - Enabler of heterogeneous integration
- Hybridization of technologies
  - Support for integrated sensing and processing

Outline

- Introduction
- Technological innovations
  - Emerging nanotechnologies and devices
- Architectural trends
  - Multiprocessing, NoCs, and 3D integration
- **Cyberphysical applications**
  - **The nano-tera.ch program**
- Conclusions

Mission

Research, Design & Engineering of complex tera-scale systems using nano-scale devices and technologies

Foster research and crossbreeding of technologies

Main application domains are Health and Environment, with Energy and Security as transversal support areas

- Develop new markets
- Improve living standards
- Better the quality of health and environment
- Foster a vision of engineering with social objectives
- Promote related educationl programs

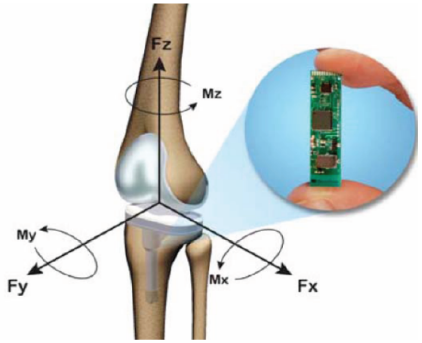
nano-tera.ch

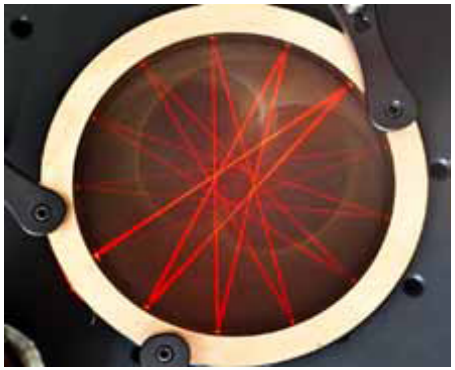
Nano-Tera.ch: key figures

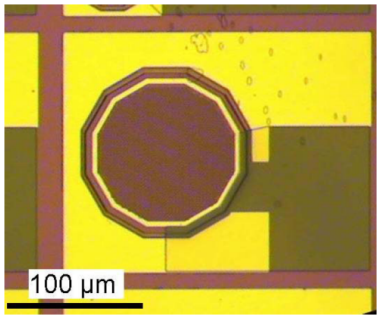
- ~ 120 projects funded since 2009
- ~ 30 MCHF/year (approximatively 50% in cash + institutional matching)
- ~ 35 Swiss research institutions involved
- ~150 research groups
- ~700 researchers
- ~180 PhD thesis supported
- ~ 750 papers published
- ~ 1300 presentations
- ~35 awards
- ~ 25 patents filed

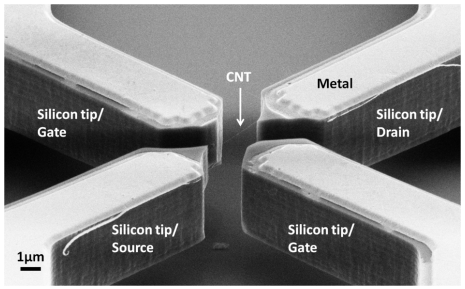
	TOTAL since beginning of the program		
	Journals, books	Conf. Proceedings	Total
RTD 2009	200	202	**402**
RTD 2010	95	161	**256**
RTD add-on	2	4	**6**
NTF	18	36	**54**
SSSTC	9	10	**19**
	324	413	**737**

Examples of research projects

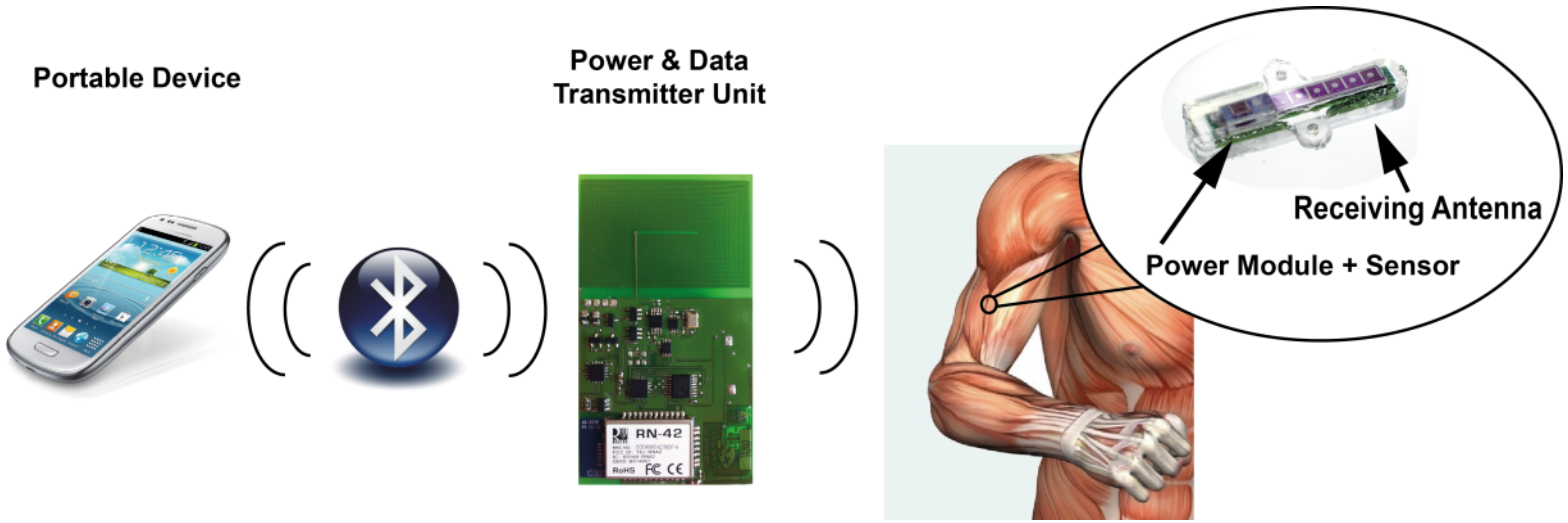








Implanted sensor

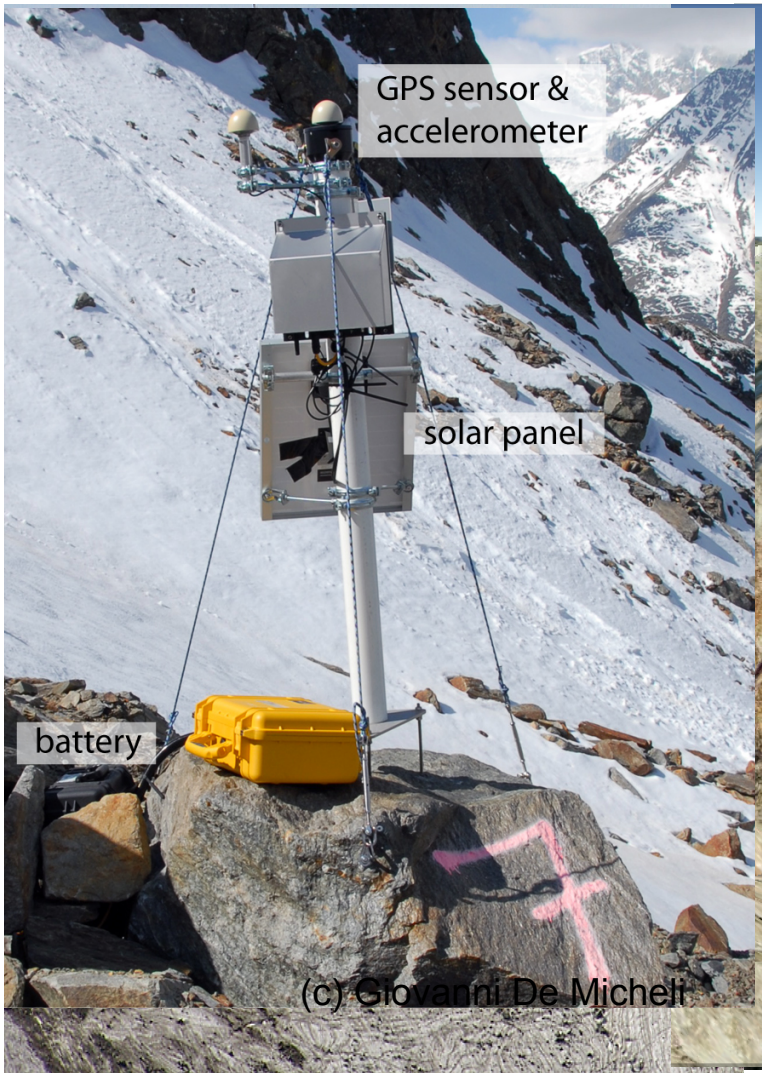


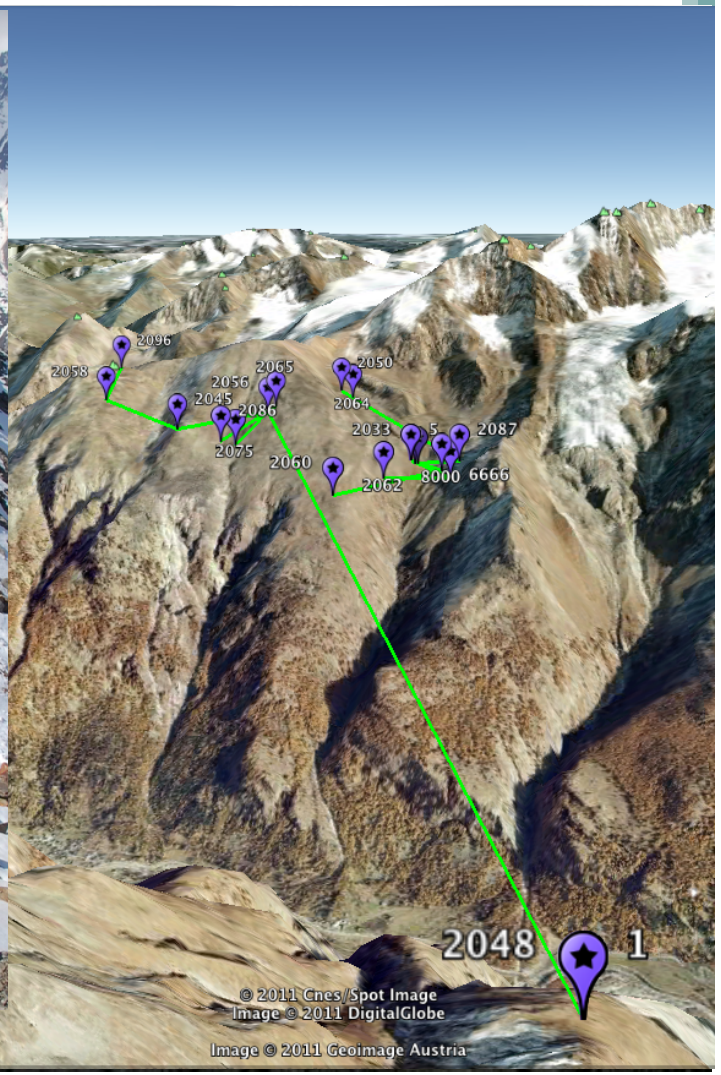
X-Sense

Monitoring alpine mass movements at multiple scales

Lothar Thiele (ETHZ)

Target: Safety in an alpine environment
Technology: Networked stations for rock/ice movement





ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Universität Zürich

GAMMA REMOTE SENSING

Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
Confederaziun svizra

Swiss Confederation

Federal Office for the Environment FOEN

Summary – nano-tera

- Nano-Tera.ch exploits **new technologies** and devices:
  - *Integrated electronics* and *sensors*
- With the objective of building **heterogeneous** systems:
  - Monitor health in patients, disabled and elderly
  - Monitor the environment for pollution and to prevent disasters
- And with the final goal of increasing the **well-being** of individuals and communities
  - Key contribution of engineering to coping with complex societal and economic problems
  - Requiring large and collaborative intellectual effort

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- **Conclusions**

Conclusions

- Cyberphysical systems can support the solution of important societal and economic problems
- Cyberphysical systems exploit ubiquitous connectivity and new sensing modalities
- New technologies enrich CMOS with novel devices
  - *Silicon nanowire* and *carbon-based* devices
  - *Controlled polarity* can be efficiently used in logic design
- New architectures and design styles:
  - *Regularity* of the fabric is key to robustness
  - 3-Dimensional integration gives an extra degree of freedom
- Hybridization of new technologies opens new frontiers

Thank you